

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CURRENT LIGHTING SOLUTIONS, LLC
D/B/A GE CURRENT

Petitioner,

v.

JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD.

Patent Owner.

Case No. IPR2023-00676
Patent No. 9,939,140

**DECLARATION OF JOSHUA PHINNEY, PH.D. IN SUPPORT OF
PATENT OWNER'S PRELIMINARY RESPONSE**

I. INTRODUCTION

1. I have been retained by Super Lighting to address issues brought forth in Current Lighting Solution's IPR Petition ("IPR2023-00676") against U.S. Pat. No. 9,939,140 (the "'140 Patent").

2. As an initial matter, I testified in the trial captioned *Jiaxing Super Lighting Electric Appliance Co. Ltd. v. CH Lighting Technology Co. Ltd.*, No. 6:20-cv-00018-ADA (W.D. Tex.). As part of my testimony, I testified that the '140 Patent's claims are not anticipated or rendered obvious by the circuits of Ivey345 and Sadwick. Current's Petition, which adds other references that do not address the core circuits at issue, does not change my opinion that the claims of the '140 Patent are valid.

3. I am being compensated for my time. My compensation is not contingent on any result.

4. I understand that Super Lighting is submitting my declaration to the PTAB with its preliminary response, and that the response is preliminary in nature. Because of this, I have not provided my full opinion and have not addressed the entirety of the record. In no way should be construed that my not addressing an item is a concession, or that I otherwise bear an opinion on it one way or another. If the PTAB decides to institute, I will more fully provide an opinion.

A. Qualifications

5. I am a Principal Engineer in the Electrical and Semiconductors practice at Exponent, a multidisciplinary science and engineering consulting firm with headquarters at 149 Commonwealth Drive, Menlo Park, California 94025.

6. I received a Ph.D. in Electrical Engineering from the Massachusetts Institute of Technology (“MIT”) in 2005. I also earned S.M. and B.S. degrees in Electrical Engineering from MIT and the University of Illinois, Chicago, respectively. My doctoral work centered on the miniaturization of power converters, including voltage regulator modules for application processors and GPUs. I received my Masters in Electrical Engineering from MIT in 2001, and my Bachelors in Electrical Engineering from University of Illinois, Chicago in 1999. I am the co-inventor on patents for improving the performance of capacitors, EMI filters, and common-mode chokes.

7. For my publications related to both my Master’s and Ph.D. thesis, I received the William M. Portnoy Prize Paper Award (2003) and the IEEE Power Electronics Society Transactions Prize Paper Award (2004).

8. After earning my Ph.D., I joined Exponent and have led technical investigations pertaining to power systems, industrial electronics, portable electronic devices, microcomputers, and electromechanical devices. My job functions include analyzing hardware and software of these devices to understand

their modes of failure, and testifying regarding these devices in legal matters involving patents and trade secrets.

9. I have testified regarding the software-defined features, internal circuitry, and physical embodiments of electronic equipment. Regarding circuitry, I have testified regarding the power electronics and communication circuitry in microcomputers, portable electronic devices, peripherals, and machine controllers. In particular, I have testified regarding power-sequencing and power-on behavior of laptop computers, desktop computers, rack-mounted servers, and mobile terminals. In addition, I have testified regarding power management in computers and portable electronic devices, including the historical state of the art in power management between 1990 to 2020.

10. Regarding the mechanical elements of electronic equipment, I have testified regarding buttons and touch interfaces, connectors, linear and rotary actuators, position-measuring devices, and the design and construction of modular housings for computerized equipment and peripherals. In particular, I have testified regarding user interfaces (including buttons, indicators, touch interfaces and card readers) as they are constructed in relation the housing and underlying electronic assemblies, including PCBs, flex printed circuits, and other connector assemblies within the housing of electronic equipment. I have also conducted design reviews and performed failure analysis of printed circuit boards (“PCBs”).

I have laid out multilayer PCBs, including multilayer PCBs with controlled impedance, and worked directly with PCB fabricators to ensure performance and yield.

11. In addition to the forgoing, I perform electromagnetic assessment of utility and communication infrastructure. These issues include permitting, interference, and environmental impact of radar, AC and HVDC transmission lines, substations, photovoltaic installations, generators, broadcast antennas, and electrified mass transit systems.

12. Additional details about my employment history, fields of expertise, publications, and testimony are further described in my curriculum vitae, which is attached as Exhibit A.

B. Materials Reviewed

13. My opinions expressed in this declaration are based on documents and materials identified in this declaration, including the '140 patent, the prior art references and background materials discussed in this declaration, and the other references specifically identified in this declaration. I have considered these materials in their entirety, even if only portions are discussed here. The following is an exemplary list of the materials on which I based on opinion.

II. CLAIM CONSTRUCTION

14. I understand that terms are to be given their plain and ordinary meaning. I have applied this meaning in my declaration. I reserve the right to supplement my opinions if the PTAB institutes. In my opinion, a POSITA would have at least a bachelor's degree in Electrical Engineering or a comparable field and 3 years of experience designing lighting fixtures or systems, or equivalents. Extensive experience and technical training may substitute for educational requirements, while advanced education may substitute for experience. I note that I was a POSITA during the relevant period.

III. STANDARDS OF OBVIOUSNESS

15. Even if a patent claim is not anticipated, I understand that the claim is invalid if it claims an aspect of an invention that would be obvious to a POSITA at the time of the alleged invention. Specifically, I understand that if the differences between the asserted claim and a single prior art reference or a combination of prior art references are such that the subject matter as a whole would have been obvious to a POSITA at the time the invention was made, a patent may be invalid for "obviousness." In evaluating obviousness, I understand that one must look at the claimed subject matter as a whole and through the eyes of a POSITA at the time the invention was made. In other words, I understand and have been informed by counsel that when determining obviousness, one considers the

perspective of a hypothetical POSITA. I further understand that the asserted claims of the patent should be read from the point of view of a POSITA at the time the claimed invention was made. To evaluate whether a patent claim would have been obvious, I understand that one may analyze the interrelated teachings of multiple prior art references.

16. I further understand that it is assumed a hypothetical POSITA knows and has all relevant prior art in the field of endeavor covered by the asserted patent and all analogous prior art. I understand that the POSITA must interpret the references for what they teach based on the skill level of that person. A POSITA is not necessarily an expert, and the question is what the POSITA would think, not what someone who's an expert in the field would think.

17. I also understand and have been informed by counsel that a determination of obviousness is made after weighing the following factors: (1) level of ordinary skill in the pertinent art; (2) the scope and content of the prior art; (3) the differences between the prior art as a whole and the claim at issue; and (4) as appropriate, secondary considerations of non-obviousness.

18. I understand that an obviousness evaluation can be made by using a single reference or by combining several prior art references. For example a single reference, when considered in view of the knowledge of a POSITA, could render a claim obvious.

19. I understand that an explicit teaching, suggestion, or motivation to combine prior art references is not required. I also understand that an obviousness analysis involving two or more references generally must account for a reason why a POSITA would have made a particular combination and that there would have been a reasonable expectation of success. I understand that the POSITA's common sense or ordinary creativity can be used by itself as a motivation for combining references. I also understand that use of common sense or ordinary creativity does not require a specific hint or suggestion in a prior art reference, but only a reasoned explanation of the application of common sense.

20. I understand that a particular combination of prior art references can be made by merely showing that it was obvious to try the combination. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, common sense may be a good reason for a POSITA to pursue known options.

21. In evaluating obviousness, both the prior art and the claimed invention should be viewed through the knowledge and understanding of a POSITA at the time of the invention—hindsight should not be used to decide whether a claim is obvious.

22. I understand that at least the following rationales may support a finding of obviousness: (1) combining prior art elements according to known

methods to yield predictable results; (2) simple substitution of one known element for another to obtain predictable results; (3) use of a known technique to improve similar devices (methods, or products) in the same way; (4) applying a known technique to a known device (method, or product) ready for improvement to yield predictable results; (5) “obvious to try”—choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; (6) a predictable variation of work in the same or a different field of endeavor if a POSITA would be able to implement the variation; (7) there existed a known problem for which there was an obvious solution encompassed by the patent’s claims at the time of the claimed invention; (8) known work in one field may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to a POSITA; and (9) some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

23. I also understand that evidence of so-called “objective indicia” or “secondary considerations” should be considered when determining whether an asserted claim would have been obvious. “Objective indicia” include: (1) commercial success attributable to the invention; (2) long-felt but unsolved need for the invention; (3) failure of others; (4) skepticism by experts; (5) praise by

others; (6) teaching away by others; (7) recognition of a problem which the claimed invention addresses; (8) copying by others; and (9) unexpected results. But these secondary considerations only apply if there is a “nexus” between the asserted secondary consideration and claimed invention, and the secondary considerations cannot be due to extraneous factors, such as marketing or unclaimed features of an embodiment of the invention.

24. I also understand that if others having ordinary skill in the field independently made the claimed invention at about the same time the inventor made the invention, often referred to as “simultaneous invention,” this can be an indication of obviousness. I understand that simultaneous invention can be persuasive evidence that the claimed apparatus or method was merely the product of ordinary engineering skill. I understand that invention even within a year can be considered a comparatively short time.

IV. GROUNDS 1-4 DO NOT RENDER THE CLAIMS OBVIOUS

25. I have provided an excerpt of representative claim 1 below.

[1pre] 1. An installation detection circuit configured in a light-emitting diode (LED) tube lamp configured to receive an external driving signal,

[1a] the installation detection circuit comprising:

a pulse generating circuit configured to output one or more pulse signals;

[1b] wherein the installation detection circuit is configured to detect during at least one of the one or

more pulse signals whether the LED tube lamp is properly installed on a lamp socket, based on detecting a signal generated from the external driving signal; and

[1c] a switch circuit coupled to the pulse generating circuit, wherein the one or more pulse signals control turning on and off of the switch circuit;

[1d] wherein the installation detection circuit is further configured to:

when it is detected during one of the one or more pulse signals that the LED tube lamp is not properly installed on the lamp socket, control the switch circuit to remain in an off state to cause a power loop of the LED tube lamp to be open; and

[1e] when it is detected during one of the one or more pulse signals that the LED tube lamp is properly installed on the lamp socket, control the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state,

[1f] wherein the signal generated from the external driving signal is a sampling signal on the power loop, the installation detection circuit further comprises a detection determining circuit configured to detect the sampling signal for determining whether the LED tube lamp is properly installed on the lamp socket, and the power loop includes the switch circuit and the detection determining circuit, and

[1g] wherein the pulse generating circuit is configured to output one or more pulse signals independent of whether the detection determining circuit detects the sampling signal.

C. GROUND 1

26. In my opinion, Ivey345 and Ivey813 do not render obvious the claims.

27. Principally, Ivey345 has a two-switch mechanism. One switch 135 controls a test current path. The other switch 175 (blue) controls the LEDs, and main power loop of the circuit. The switch 135 (red) is turned on and off by oscillator 130, which the Petitioner has described as having a clocked output. Oscillator 130 clearly does not control switch 175, and the claim “one or more pulse signals control turning on and off of the switch circuit” is plainly not taught. The other challenged independent claims have similar limitations. Because these claim limitations are plainly not met on their face, I have left my preliminary opinion shorter. Should the Board institute, I reserve the right to provide further detail.

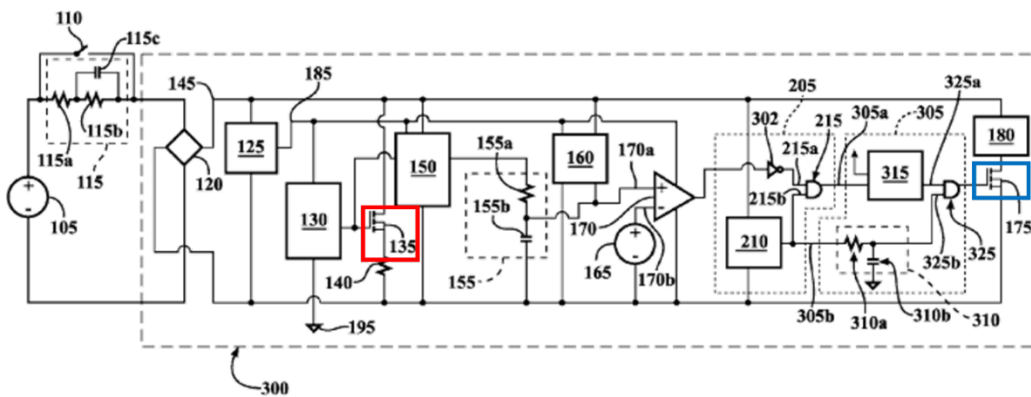


FIG. 3

28. It is also my opinion that a POSITA would not have been motivated to use Ivey345's circuit in an LED tube lamp. This is because oscillator 130 continually triggers switch 135, and Petitioner describes this in its analysis as a clock signal, e.g., a signal that has a duty cycle of 50%. A rectified voltage derived

from a mains voltage of 120V AC RMS (Root Mean Squared) (340V peak-to-peak) is a fairly high DC voltage that – when connected across a continuously switched path – provides an average current I_{RMS} . In Ivey345 this switched source is effectively an always-on current source, connected to ground through test load 140.

29. This is not problematic in Ivey345 because it is directed to bulb lights, and not tube lights. For bulbs, the current path to ground will ensure that a person touching an exposed portion of the bulb will not be the sole path to ground, and will instead be a secondary path due to the always-on current source and test-load path.

30. The types of bulbs contemplated by Ivey345 are below:

Threaded	Bayonet	Pinned
		

31. The shock concern for bulbs is a person touching one terminal of the bulb, but not a person providing the sole ground path to ground. This single-path

concern occurs when Ivey345's circuit is used in a tube lamp. In a tube lamp, it is often the case that one end is used for AC mains source, and the other end is used for ground. This creates a singular path to ground if a person improperly installs a tube lamp. The below demonstrative shows how the Ivey345 circuit creates a singular path to ground if used in a tube lamp.

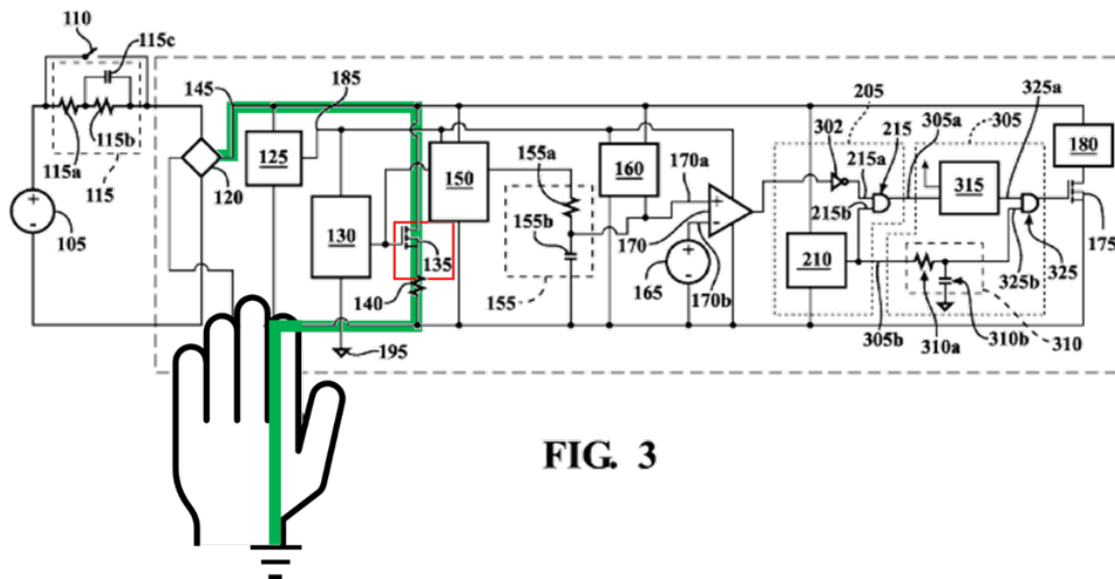


FIG. 3

32. In my opinion, a POSITA would not have designed a circuit where there is a real risk that the sole path to ground for a current source is a human installer. Because of this, it is my opinion that a POSITA would not have used Ivey345's circuit of FIG. 3 in an LED tube lamp.

33. Because I believe the lack of motivation is clear, I have made my opinion brief. Should the Board institute, I reserve the right to supplement my opinion with more detail.

combination, because the oscillator is ORed, meaning that the output will always be “1” as the oscillator continuously outputs a “1.”

36. In my opinion, a POSITA would have not made these modifications for two simple reasons.

37. First, Ivey345’s main load shut-off latch 315 is nullified via the Petitioner-added OR gate. Main load shut-off latch 315 is designed to turn off the switch in case of a person on the line. Ivey345 at [0044]-[0045]. This is apparent from the original Ivey345 FIG.3 (reproduced below) which has the main load shut-off latch 315 inputted to an AND gate, and the AND gate’s output is input to the main load switch 175. An AND gate needs all inputs to be “1” in order for it to output a “1,” and if any input is “0,” a “0” output will result. This means that main load shut-off latch 315 can, by itself, disable the switch 175 and power line in the original Ivey345 FIG. 3. Petitioner’s OR-gate destroys this operation, by wiring the output of the AND gate to an OR gate input with the oscillator 130.

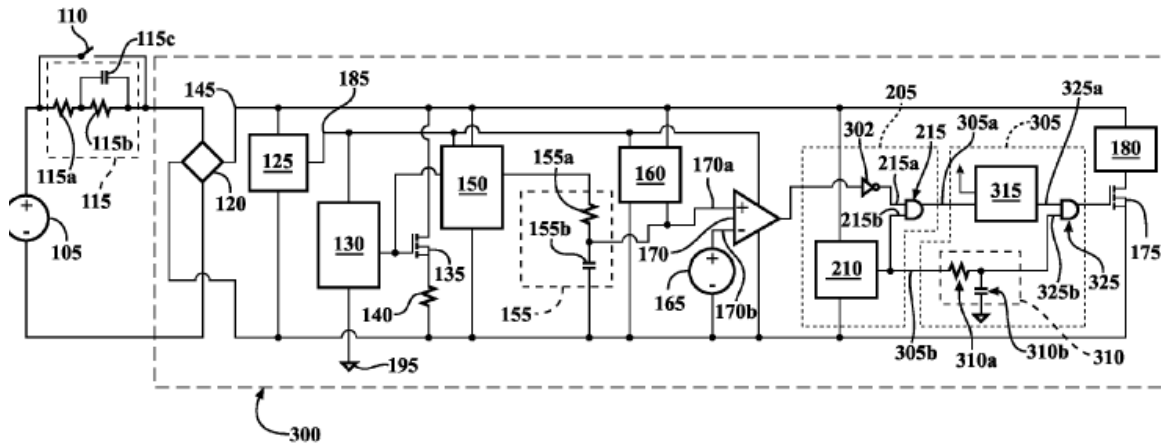


FIG. 3

38. Second, Petitioner's tying of an oscillator 130 to the switch 175 provides a power loop that – because of its continuously switching – can draw an average current I_{RMS} . This is because oscillator 130 continually triggers switch 175 in Petitioner's combination, and Petitioner describes this in its analysis as a clock signal, e.g., a signal that has a duty cycle of 50%. As noted previously, a rectified voltage off of a mains voltage of 120V AC RMS (Root Mean Squared) (340V peak-to-peak) is a fairly high DC voltage. A POSITA would regard this as a shock risk because it creates an LED tube lamp with effectively continuous conduction, and a singular path to ground (through an installer) should the installer touch the ground pin of the tube lamp while the source pin is attached to a voltage source. A POSITA would therefore not have been motivated to create Petitioner's suggested modifications to Ivey345 (*i.e.*, having oscillator 130 control the main load switch 175).

39. Because I believe the lack of motivation and untaught elements are very clear, I have made my opinion brief. Should the Board institute, I reserve the right to supplement my opinion with more detail.

E. GROUND 3-4

40. Petitioner's analysis does not fix or address the above-described problems.

II. CONCLUSION

41. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001; and further that such willful false statements may jeopardize the validity of the application or any patent issued thereon. I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Executed on August 30, 2023 in Garden City, NY.



Joshua Phinney, Ph.D.