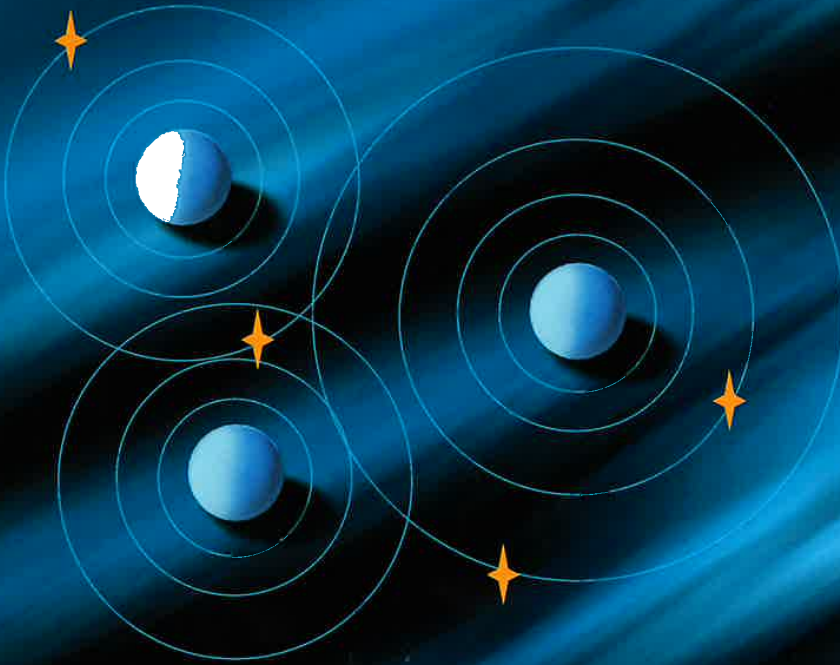




WIRELESS ACCESS NETWORKS

Fixed Wireless Access and WLL Networks
– Design and Operation

MARTIN P. CLARK

Wireless Access Networks

Fixed Wireless Access and WLL
Networks — Design and Operation

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Martin P. Clark
*Telecommunications Consultant,
Eppstein, Germany*

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Martin Clark
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Part I

Fundamentals of Fixed Wireless

Appendix 6

Forward Error Correction Codes

General

The basic principle of *Forward Error Correction (FEC)* is the addition of a number of *code* bits to a user signal to reduce the probability of a *bit error* arising during transmission of that user signal. For a user signal string of length k bits to be encoded we must find at least $2k$ separate and *orthogonal* codes — one distinct *codeword* for each possible bit combination in the original signal.

The *Hamming distance* (d) defines the difference in value of the individual codewords. Specifically, the Hamming distance is the minimum number of bit positions by which the individual codewords differ from one another. The larger the Hamming distance, the greater is the capability of the code to *detect* and *correct* errors in the presence of *noise* or *errors* introduced during transmission.

The number of errors that can be *corrected* is less than or equal to $(d - 1)/2$. The number of errors that can be *detected* is less than or equal to d .

There are five main types of forward error correction codes:

- *block codes* (including Hamming codes);
- *cyclic codes*;
- *BCH (Bose–Chaudhuri–Hocquenghem)* codes;
- *Reed–Solomon* codes;
- *Convolutional codes* (including *Viterbi codes*)

We briefly discuss the principles and mechanism of each of these types of codes.

Block Codes

Block codes break up the user data stream into a series of blocks of k bits in length. To each block, a code block of $(n - k)$ bits is added to make an n -bit *codeword*. The code is described by the notation (n, k) block code.

Thus, for example, a $(15, 4)$ code has 15 bit codewords, 11 bits of which are real coded user data, and four bits are *parity bits*. An example of a $(7, 3)$ code was given in Chapter 6.

In mathematical notation, the coding takes place as follows:

$$\mathbf{c} = \mathbf{d}[\mathbf{G}]$$

where $\mathbf{c}$ is a vector representing the *codeword*, $\mathbf{d}$ is the vector of the user data, and $[\mathbf{G}]$ is the *generator matrix*.

The generator matrix is a matrix of dimensions k by n , made up of the *identity matrix* $[\mathbf{I}]$ and the *parity matrix* $[\mathbf{P}]$ (the matrix $[\mathbf{P}]$ identifies, for each of the parity bits, which bit positions in the user-data signal are used to calculate the parity):

$$[\mathbf{G}] = [\mathbf{I}\mathbf{P}]$$

An example of the various matrices and vectors for a simple (7, 3) block code might be as shown below. (Actually, these are the actual matrices relevant to the example we discussed in Chapter 6, but with the bits rearranged so that the data bits appear in the first three positions of the codeword and the parity bits thereafter):

$$\mathbf{d} = (0 \ 1 \ 1 \ 1)$$

$$\mathbf{G} = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 & 1 \end{bmatrix}$$

(The last three columns generate the parity bits. The rows of the column indicate which bits of the data are to be used for the calculation. The first parity bit will be based on bits 1, 2 and 4.)

$$\mathbf{c} = (0 \ 1 \ 1 \ 1 \ 0 \ 0)$$

The matrix multiplication is performed *modulo 2*. The effect of this multiplication is to add $n-k$ parity bits to the end of the user data signal of k bits.

At the receiving end, the user data part of the signal (as received) is again subjected to the same parity calculation. The $n-k$ parity check result generated by the receiver is represented by the matrix formula $\mathbf{d}'[\mathbf{P}]$, where $\mathbf{d}'$ is that part of the received codeword representing the user data. The result should be equal to the received parity bit code $\mathbf{c}_p$. This can be determined by electronic hardware by a modulo 2 addition (which is equivalent to a modulo 2 subtraction). The result should be 0:

$$\mathbf{d}'[\mathbf{P}] + \mathbf{c}_p = [\mathbf{0}]$$

For our example above, let us assume that the data is received with a bit error at position three of the user data. This is equivalent to the second example of Figure 6.14:

$$\text{Received codeword} = \frac{(0 \ 1 \ 0 \ 1 \ 1 \ 0 \ 0)}{\mathbf{d}'} \frac{\mathbf{c}_p}{1 \ 0 \ 0}$$

$$\mathbf{d}' = (0 \ 1 \ 0 \ 1)$$

$$\mathbf{P} = \begin{pmatrix} 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \\ 1 & 1 & 1 \end{pmatrix}$$

$$\mathbf{c}_p = (1 \ 0 \ 0)$$

$$\mathbf{d}[\mathbf{P}] + \mathbf{c}_p = (0 \ 1 \ 0) + (1 \ 0 \ 0) = (1 \ 1 \ 0)$$

If the result is not 0 (as in our example above), then the values in the resulting vector can be used to determine the exact bit position of the error(s), and thus be used to correct them. Because of the rearrangement of the position of the bits, the correction values (3, 5, 6 and 7) will not, however, have the same meaning as in Chapter 6. Instead, these values will represent errors respectively at positions (1, 2, 3 and 4).

Our efforts to explain the process using matrix notation is because this aids the design of digital electronic circuitry.

Cyclic Codes

Cyclic codes are a special type of block code, in which each of the valid codewords are a simple lateral shift of one another. Thus, if one valid code of a (10, 3) cyclic code is:

$$\mathbf{c} = (1 \ 0 \ 1 \ 0 \ 1 \ 0 \ 0 \ 1 \ 0 \ 0)$$

then

$$\mathbf{c} = (0 \ 1 \ 0 \ 1 \ 0 \ 0 \ 1 \ 0 \ 0 \ 1)$$

is also a valid code, as is

$$\mathbf{c} = (1 \ 0 \ 1 \ 0 \ 0 \ 1 \ 0 \ 0 \ 1 \ 0)$$

etc.

Using a cyclical structure of different codes enables us to correct larger blocks of errors than those possible with non-cyclic codes. A generator matrix with particular qualities is required to generate a *cyclic code*. In particular, the generator matrix for a cyclic code always has a value '1' as its last element (i.e. in the k th row of the n th column).

If we consider our example of the last section on block codes, we had a valid (7, 3) codeword of:

$$\mathbf{c} = (0 \ 1 \ 1 \ 1 \ 1 \ 0 \ 0)$$

(For the data value $\mathbf{d} = 0111$ the parity values were 100)

For this to be a cyclic code, all the other codes:

$$\begin{array}{ll} \mathbf{c} = (0 \ 0 \ 1 \ 1 \ 1 \ 1 \ 0) & \mathbf{c} = (1 \ 1 \ 0 \ 0 \ 0 \ 1 \ 1) \\ \mathbf{c} = (0 \ 0 \ 0 \ 1 \ 1 \ 1 \ 1) & \mathbf{c} = (1 \ 1 \ 1 \ 0 \ 0 \ 0 \ 1) \\ \mathbf{c} = (1 \ 0 \ 0 \ 0 \ 1 \ 1 \ 1) & \mathbf{c} = (1 \ 1 \ 1 \ 1 \ 0 \ 0 \ 0) \end{array}$$

must also be valid code words. But they are not. Another valid codeword is usually $\mathbf{c} = (0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0)$.

The data value (0 0 1 1), for example, yields the codeword (0 0 1 1 0 0 1), and not the allowed cyclic code (0 0 1 1 1 1 0).

The codeword $\mathbf{c} = (0 \ 0 \ 0 \ 1 \ 0 \ 0 \ 0)$ could also not be a valid (7, 3) cyclic codeword. Why? Because if it were, then $\mathbf{c} = (0 \ 0 \ 0 \ 0 \ 1 \ 0 \ 0)$ would also have to be a valid codeword. This is not possible, for a parity value of '1' is not possible for non-zero user data (the first four bits of the codeword). Not all block codes are cyclic codes!!

So, never mind the non-cyclic codes, how do we conceive the *generator matrix* of a cyclic code? By starting with the *generator polynomial* (the last row of the matrix).

For an (n, k) code we expect $n-k$ bits of user data and a k -bit parity code.

The *generator polynomial* has the form $x^{n-k} + ax^{n-k-1} + \dots + 1$ (a value is '1' or '0') and appears as the last row of the *generator matrix* in the form (for an example (7, 4) cyclic code):

$$\begin{bmatrix} x & x & x & x & x & x & x \\ x & x & x & x & x & x & x \\ 0 & 0 & 1 & 1 & 1 & 0 & 1 \end{bmatrix}$$

The first $n-k-1$ elements of the row must be zeros, and the last element must be a '1'. In other words, the generator polynomial is a polynomial of order k (first element x^k). The generator polynomial in this case is $x^4 + x^3 + x^2 + 1$. This determines the properties of the code, and defines one of the valid codewords, in this case (0 0 1 1 1 0 1). The full generator matrix is:

$$\begin{bmatrix} 1 & 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 & 1 & 0 & 1 \end{bmatrix}$$

The valid codewords are:

$$\begin{array}{ll} \mathbf{c} = (0 & 0 & 0 & 0 & 0 & 0 & 0) & \mathbf{c} = (1 & 0 & 0 & 1 & 1 & 1 & 0) \\ \mathbf{c} = (0 & 0 & 1 & 1 & 1 & 0 & 1) & \mathbf{c} = (1 & 0 & 1 & 0 & 0 & 1 & 1) \\ \mathbf{c} = (0 & 1 & 0 & 0 & 1 & 1 & 1) & \mathbf{c} = (1 & 1 & 0 & 1 & 0 & 0 & 1) \\ \mathbf{c} = (0 & 1 & 1 & 1 & 0 & 1 & 0) & \mathbf{c} = (1 & 1 & 1 & 0 & 1 & 0 & 0) \end{array}$$

BCH Codes (Bose–Chaudhuri–Hocquenghem)

BCH-Codes are cyclic codes designed to provide for multiple error correction. The most commonly used BCH-codes are Reed–Solomon codes.

Reed–Solomon Codes

When talking about *Reed–Solomon* codes, it is common to talk about the coding of *symbols*. In many data applications, for example full *bytes* or *octets* (of 8 bits each) are used to represent a given alphanumeric *symbol*. For 8 bits there are $q = 256$ ($q = 2^8$) possible different symbols (values). Thus, we must have 256 different codewords available.

A Reed–Solomon code is a *block code* and *cyclic code* of type (n, k) as we previously discussed. The input number of data bits is $n-k$ and the codeword symbols are n bits in length. It is usual that the value of n be restricted to no more than $q-1$ (i.e. $n < q$). In our example, this means a maximum value of $n = 255$.

The code is often quoted in terms of its byte size. A typical code might be (64, 24), thus 40 bytes of data are protected with 24 bytes of code (64 bytes total). Each codeword would be $64 \times 8 = 512$ bytes long. However, of the 2^{512} combinations available, only 64^{24} combinations (i.e. $2^{6 \times 24} = 2^{144}$) combinations would actually be used. This enables up to $24/2 = 12$ symbol errors to be corrected.

Convolutional Codes

Convolutional codes work on a shift register basis. A string of consecutive bits of the input user data stream (of K bits in length, where K is the *constraint length* of the code). This string of bits are subject to a series of *modulo 2* summation actions (in effect, parity checks). The number of summation codes to which the K -bit sequence is subjected is denoted by v . The coding which results from a $1/v$ coder using v different code summations is called a $1/v$ *convolutional code*.

Figure A6.1 illustrates $\frac{1}{2}$ convolutional coder with a *constraint length* of $K=3$.

The two codes being used (in alternation to produce the output bitstream) are:

$$c_1 = d_0 + d_1 + d_2$$

$$c_2 = d_0 + d_2$$

Table A6.1 illustrates the output from this coder.

Convolutional codes of *constraint length* $K=7$ are often used, with a codeword length of 28 or 35 bits ($v=4$ or 5).

The *shift register* nature of convolutional codes makes them very easy to implement in a digital electronic circuit design. In addition, the complete codeword does not have to have been received before decoding can commence. This minimises the signal delays caused during transmission.

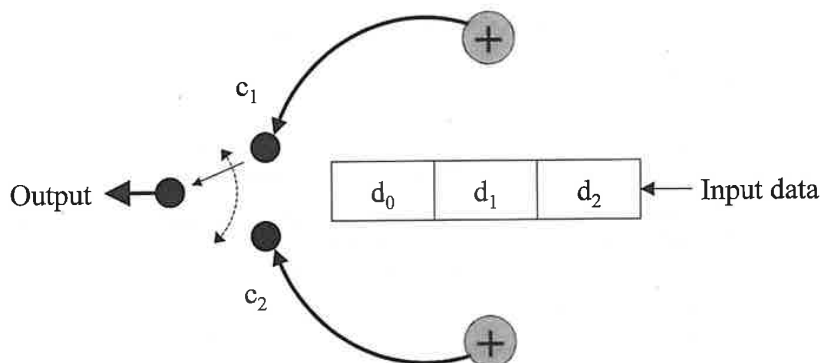


Figure A6.1 $\frac{1}{2}$ convolutional coder with constraint length $K=3$

Table A6.1 Convolutional code and output

Time interval	1	2	3	4	5	6	7	8
Input bitstream	0	1	1	0	1	0	0	1
Bits in register ($d_0d_1d_2$)	000	000	011	110	101	010	100	001
Output variable	c_1 c_2	c_1 c_2	c_1 c_2	c_1 c_2	c_1 c_2	c_1 c_2	c_1 c_2	c_1 c_2
Output bitstream	0 0	1 1	0 1	0 1	0 0	1 0	1 1	1 1

Viterbi Codes

Viterbi codes are a particular type of convolutional code. In particular, Viterbi determined a methodology for the correct decoding (or rather the most likely correct interpretation or *maximum likelihood* decoding) of incorrectly received codewords.

Coding Gain

One talks of the *coding gain* achieved by using *Forward Error Correction (FEC)*. This gain is the effective improvement in the *receiver sensitivity* of the receiver (we defined this term in Chapter 6). The improvement in sensitivity results from the correction of some of the errors (resulting in an improvement in the signal quality) at a given received signal power. Typical coding gains due to FEC are around 3 to 6 dB.