

SYSTEM AND METHOD FOR PERFORMING BROADBAND TRANSMISSION OVER AN OPTICAL NETWORK

FIELD OF THE INVENTION

5 [0001] The present invention relates to optical fiber communications generally, and more specifically to a system and method for performing broadband transmission rates over an optical network.

BACKGROUND OF THE INVENTION

10 [0002] In Datacom, Telecom and Storage Access Network (SAN) applications that operate at very high data rates of 10Gbps and higher have consistently attracted hundreds of millions of research and development investment dollars to improve the overall port density provided by system vendor solutions. These improvements in port density have primarily been obtained through power and thermal improvements of a
15 given physical layer implementation by eliminating MUX/DEMUX functions, reducing pin count and increasing the serial interface data rate of the optical module. Since Service Provider's business case demands that System Vendor's cost and performance efficiencies continue to exceed previous generation designs and implementation capabilities, System Vendors are forced to explore new methods for reducing power
20 while enabling higher levels of system-on-a-chip integration, versatility and reducing thermal characteristics. Other issues like Electro Magnetic Interference (EMI) that is generated by these new platforms are a constant ongoing challenge to system vendors and component suppliers.

[0003] In an effort to standardize, harmonize and set aggressive cost, power, area
25 and performance goals the industry, System Vendors have sponsored and supported Multi-Source Agreements (MSA) between several component suppliers that define and specify all the physical and electrical requirements for optical transponders and transceivers. For example, over the past few years both the Datacom and Telecom industries have seen a race toward smaller and lower power optical 10Gbps platforms.
30 Component vendors started with an initial IEEE driven 300-pin specification that specified sixteen 622Mbps electrical interfaces. Component manufactures continued the

race with two MSAs called X2 and XPAK both of which specified four 3.125Gbps channels on the electrical interface side (also known as media attachment layer). A competing Xenpak MSA that was physically smaller while maintaining the same pin count and four serial 3.125Gbps channel interface followed this. And now the latest and most advanced 10Gbps optical transceiver MSA based on a 10Gbps XFI serial interface called the XFP MSA and only consumes 30-pins. This rush of investment, development and improvement in the industry, during an industry wide market slowdown, is a large indicator of the importance System Vendors and Service Providers place on port density and the impact greater density has on business cases for Datacom, Telecom and SAN markets. Some estimates are that the industry will save close to a billion dollars of additional capital expenditures over the next 3 years due mainly to the per port power and area density improvements stemming from the XFP MSA for each Line card deployed.

[0004] There are practical system chip-to-chip interface design challenges at the PHY layer however with the XFP due to the 10Gbps serial interface data rate which cause component PHY manufactures to incur a greater amount of investment CMOS fab processes due to the 10GHz serial data rate circuit requirements. And since these new processes suffer from high leakage current and other production reliability issues, the proliferation of the XFP may stall and cause significant delay in the deployment of new high density 10Gbps line cards. In addition, direct modulation of 10Gbps data rates cause significant restrictions on the reach for a given implementation over all types of fiber. Addressing these practical constraints that plagues all high-speed PHY and PMD implementations while enabling more performance, functionality and data rate flexibility from a single optical transceiver and PHY subsystem is a tremendous value to Component Suppliers, System Vendors and Service Providers.

[0005] This invention solves these practical PHY & PMD constraints for 10Gbps and higher data rate applications and enables extremely high-density solutions equivalent to those found at 1Gbps and below. Remarkable improvements in system power consumption, thermal performance and reach along with system interface simplifications that address practical chip-to-chip interface designs and EMI issues are enabled via this invention. From a Service Provider, System Vendor or Component Supplier perspective, this invention will profoundly improve the overall financial and service offerings that

bound every business case in the Telecom, Datacom and SAN markets and has the potential of revolutionizing point-to-multipoint deployments.

SUMMARY OF THE INVENTION

5 [0006] A system and method for performing broadband transmission rates over an optical network using a plurality of fibers, m-ary modulation, channel equalization, coding, forward error correction and a plurality of bi-directional optical sub-assemblies within a single optical transceivers.

BRIEF DESCRIPTION OF THE DRAWINGS

10 [0007] FIG. 1 is a block diagram of a combined Physical Medium Attachment (PMA) and Physical Coding Sublayer (PCS) device according to an exemplary embodiment of the invention.

[0008] FIG. 2 is a block diagram of a Physical Medium Dependent (PMD) device
15 according to an exemplary embodiment of the invention.

[0009] FIG. 3 is a block diagram of a combined PMA/PCS and PMD device called a PHY according to an embodiment of the invention.

[0010] FIG. 4 is a block diagram of a Passive Optical Network (PON) utilizing the PHY according to an embodiment of the invention.

20 [0011] FIG. 5 is a block diagram of an example PMA/PCS device according to an exemplary embodiment of the invention.

[0012] FIG. 6 is a block diagram of an example PMD device according to an exemplary embodiment of the invention.

[0013] FIG. 7 is a block diagram of an example PHY device according to an
25 exemplary embodiment of the invention.

DETAILED DESCRIPTION

[0014] The invention involves a complex design of digital, analog and optical components in two primary parts. One part called a PMA/PCS and the other PMD in the
30 vernacular of I.E.E.E 802.3. The total of these two parts is called a PHY and is a significant portion of the Physical layer in an OSI 7 Layer reference model. The

PMA/PCS device would be a mixture of digital and analog that with current technology can be manufactured in the same process in CMOS. The PMD could be a mixture of analog in a SiGe process with optical components within an optical transceiver. An example of a preferred exemplary embodiment of the invention would have; transmission rates from 155 Mbits/sec to 10 Gbits/sec; would employ an XGMII interface connecting to the PMA/PCS device but other interface protocols are possible; would also be employed in a Passive Optical Network (PON). The former example to be discussed in a concluding section with references to FIG 5, 6 and 7. Higher rates of transmission are envisioned possible with advancements in technologies. The following will discuss the PMA/PCS device 100 followed by the PMD device 200. The preferred exemplary embodiment of the invention would have two transmit and receive paths from PMA/PCS to PMA/PCS device and will be discussed as such but a single or plurality of transmit and receive paths are possible.

[0015] FIG. 1 is a block diagram of a combined Physical Medium Attachment (PMA) and Physical Coding Sublayer (PCS) device 100 according to an exemplary embodiment of the invention. The preferred exemplary embodiment would employ an asynchronous or synchronous interface that is represented by the TX Path 101 and RX Path 108 blocks. These blocks would manage the PMA/PCS interface that feed data into 101 and get data from 108 the TC-Layer block 106. The Transmission Convergence Layer (TC-Layer) 106 block is crucial for a PON. The TC-layer is responsible to create the transport system that user traffic will exploit. The need for a TC-Layer arises in PONs because of its tree-based topology in a physical layer that must be hidden from higher layers where layer 2 bridging functions are performed. The TC-Layer could, for design performance of the embodiment, perform the additional functions of an Equalizer state machine and an outer encoder and outer decoder. The TC-Layer 106 would send outgoing data to the Scrambler and Digital DEMUX block 102. The purpose of the scrambler 102 would be to randomize the data for possible improvement of the transmission. The purpose of the Digital DEMUX 102 would be to split into a plurality the transmitting data streams that would maintain the aggregated data rate equivalent to the input to the Digital DEMUX 102. As mentioned previously the envisioned embodiment would have two transmit and receive paths. The advantage in splitting

transmit and receive paths is that the bit clock rates are reduced at the cost of an additional fibers. Reducing the bit clock on fiber has the effect of improving optical loss budget thereby increasing reach and/or number of clients in a point-to-multipoint PON network. Again embodiments of the invention need not split transmit and receive paths.

5 After digital DEMUX, the two transmit paths have analogous processing blocks. In order to improve the energy per bit required to deliver the transmitting data an encoding method is employed and is represented by blocks 103a & 103b. If the TC-Layer 106 employs an outer encoder/decoder then the encoding method of 103a & 103b would be an inner encoding method and the system would be enabling forward error correction
10 (FEC) recovery of bit errors. To improve communications performance by enabling the transmitted signals to better withstand the effects of various channel impairments and to increase the number of bits per symbol transmitted by the invention, the Modulation (MOD) 104a & 104b is performed. Following MOD the transmitting data would be converted to an analog signal by a Digital to Analog Converter (DAC) 105a and 105b
15 that would include ability to shape the signal for improved transmission performance. On the path of reception of data, the data would be received as an analog signal therefore an Analog to Digital Converter (ADC) 112a & 112b would be needed. To aid the ADC, a Clock Recovery (CR) 113 device is needed that is capable of recovering the clock of m-ary data. A second CR is not needed because a Digital Delay Loop (DDL) 114 can be
20 used to aid the other ADC 112b. Note that a PON system is assumed to have a closed clock loop where the OLTs transmit clock is used to synchronize the entire PON system, which implies that PON client's recovered receive clock is used for the upstream transmit transmission. Following the ADCs 112a & 112b, the received data is processed through an Equalization method 111a & 111b to remove unwanted noise added by various
25 channel impairments. After equalization the received data would be sent into a De-Modulation/Decoder 110a & 110b block to demodulate and decode the received data. Next, the received data is descrambled and MUXed back together before being feed into the TC-Layer 106 by the De-Scrambler and Digital MUX 109 block.

[0016] FIG. 2 is a block diagram of a Physical Medium Dependent (PMD) device
30 according to an exemplary embodiment of the invention. The inputs and outputs of the PMD are analog signals. As discuss before, the preferred embodiment would have two

transmit and receive paths hence there would be two Laser Drivers 203a & 203b; two Bidirectional optical sub-assemblies often referred to as simply Bidi 202a & 202b; and two Linear Amplifiers 211a & 211b. The Bidis would employ at a minimum a Transimpedance Amplifier (TIA) 205a & 205b, a Laser Diode 206a & 206b and a Photo Diode 207a & 207b. The PMD 200 could employ a course equalization method 210a & 210b and a Receive Sensitivity Signal Interface (RSSI) that reports the measured received power. The preferred embodiment would have a serial interface (PMD intf.) 204 to enable control 209 of the course equalization 210a & 210b and the RSII1 212a and RSII2 212b.

10 [0017] FIG. 3 is a block diagram of a combined PMA/PCS and PMD device called a PHY according to an embodiment of the invention. FIG. 3 shows the two fibers 300a & 300b as envisioned in the preferred embodiment. The fibers would have particular wavelength for the transmit path and a particular wavelength for the receive path. The PMA/PCS and PMD devices are connected with analog signals capable of very high data rates; 301a & 301b; 303a and 303b. The serial interface is connected between them 302 and FIG. 3 shows the asynchronous or synchronous interface 304 and 305.

[0018] FIG. 4 is a block diagram of a Passive Optical Network (PON) utilizing the PHY according to an embodiment of the invention. The envisioned PON network with the OLT 400 and ONTs 401 are connected by the PHY through fibers and splitters.

[0019] FIG. 5 is a block diagram of an example PMA/PCS device according to an exemplary embodiment of the invention. In the example, a specific implementation of the embodiment of the invention is discussed. The example is designed to implement a 10Gbit/sec PON. For the asynchronous or synchronous interface the asynchronous XGMII interface 501 & 508 is chosen. GPON, a current PON standard from the I.T.U. used for 2.5Gbps and below data rates, is chosen for the TC-Layer implementation 506 with the addition of equalization training control and a reed-solomon encoder/decoder. GPON has it own defined Scrambler and De-scrambler method and would be implemented with the Digital MUX and DEMUX, blocks 502 & 509. For the encoding method, a 4/5 trellis method 503a & 503b is selected along with QAM-32 for the modulation 504a & 504b. With a 10Gbit/sec PON using QAM-32 modulation on dual

fibers leaves a 1.25G Symbol/sec as the symbol rate of the transmitted carrier. Therefore a 1.25GHz 5-bit DAC 505a & 505b with a corresponding 1.25G 6-bit ADC 512a & 512b are needed. The CR 513 and DDL 514 would be designed appropriately to handle the 1.25G Symbol/sec rates. Similarly if the 10G user data rate PON were to be enabled via 12.5G 8B/10B XAUI interface, a 12.5Gbit/sec implementation would translate into a 1.56G symbol/sec modulation rate. The equalization method selected is a Decision Feedback Equalization 511a & 511b or possibly a blind equalization method. De-modulation and Viterbi decoding 510a & 510b are selected to complement the example design decisions already made.

10 [0020] FIG. 6 is a block diagram of an example PMD device according to an exemplary embodiment of the invention. The example PMD device would comply with the Small Form-factor Pluggable (SFP) 600 specification. This specification has constraints on all physical aspects such as package size and pins. The SFP 600 would contain the necessary; LDs 603a & 603b; LAs 611a & 611b; TIAs 605a & 605b; RSSIs 15 612a & 612b; Course EQs 610a & 610b; and PDs 607a & 607b. The SFP 600 would use Distributed Feedback (DFB) edge emitter laser diodes 606a & 606b and a Monitor Photo Diode (MPD) 613a & 613b. The SFP would have an I²C bus interface 604 that would allow control by the PMA/PCS device of the Course EQs 610a & 610b, RSSIs 612a & 612b and MPD.

20 [0021] FIG. 7 is a block diagram of an example PHY device according to an exemplary embodiment of the invention. The PMA/PCS and PMD are connected through high-speed analog lines 701a 701b & 703a 703b, as well as the I²C bus 702. XGMII 704 & 705 connections for the PMA/PCS are shown as well.

25 [0022] Although the invention has been described in terms of exemplary embodiments, it is not limited thereto. Rather, the appended claims should be construed broadly, to include other variants and embodiments of the invention, which may be made by those skilled in the art without departing from the scope and range of equivalents of the invention.

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