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**UTILITY
PATENT APPLICATION
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(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	1972.1540001
First Inventor	Michael MANTOR
Title	A Processing Unit that Enables Asynchronous Task Dispatch
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☐ Fee Transmittal Form (e.g., PTO/SB/17)
2. ☐ Applicant claims small entity status.
See 37 CFR 1.27.
3. ☒ Specification [Total Pages 24]
Both the claims and abstract must start on a new page
(For information on the preferred arrangement, see MPEP 609.01(a))
4. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets 6]
5. Oath or Declaration [Total Sheets _____]
 - a. ☐ Newly executed (original or copy)
 - b. ☐ A copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 18 completed)
 - c. ☐ **DELETION OF INVENTOR(S)**
Signed statement attached deleting inventor(s)
name in the prior application, see 37 CFR
1.63(d)(2) and 1.33(b).
6. ☒ Application Data Sheet. See 37 CFR 1.76
7. ☐ CD-ROM or CD-R in duplicate, large table or
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Prior application information: Examiner _____ Art Unit: _____

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This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

MANTOR *et al.*

Appl. No.: To Be Assigned

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For: **A Processing Unit That Enables
Asynchronous Task Dispatch**

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**Authorization to Treat a Reply as Incorporating an
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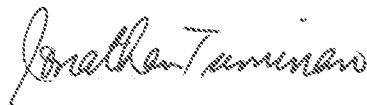
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Sir:

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Respectfully submitted,

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APPLICATION DATA SHEET

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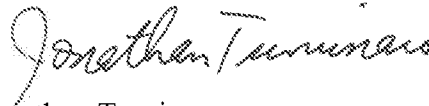
This application claims benefit under 35 U.S.C. § 119(e) to U.S. Provisional Patent Application No. 61/239,712, entitled "A Processing Unit that Enables Asynchronous Task Dispatch," to Mantor *et al.*, filed September 3, 2009.

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A PROCESSING UNIT THAT ENABLES ASYNCHRONOUS TASK DISPATCH

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CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims benefit under 35 U.S.C. § 119(e) to U.S. Provisional Patent Application No. 61/239,712, entitled "A Processing Unit that Enables Asynchronous Task Dispatch," to Mantor et al., filed September 3, 2009, the entirety of which is hereby incorporated by reference as if fully set forth herein.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention is generally directed to computing operations performed in computer systems. More particularly, the present invention is directed to a processing unit, such as a graphics-processing unit (GPU), that performs computing operations and applications thereof.

Background

[0003] A GPU is a complex integrated circuit that is adapted to perform data-parallel computing tasks, such as graphics-processing tasks. A GPU may, for example, execute graphics-processing tasks required by an end-user application, such as a video-game application. The GPU may be a discrete (i.e., separate) device and/or package or may be included in the same device and/or package as another processor (e.g., a central processing unit (CPU)). For example, GPUs are frequently integrated into routing or bridge devices such as, for example, Northbridge devices.

[0004] There are several layers of software between the end-user application and the GPU. The end-user application communicates with an application-programming interface (API). An API allows the end-user application to output graphics data and commands in a standardized format, rather than in a format that is dependent on the

GPU. Several types of APIs are commercially available, including DirectX® developed by Microsoft Corporation of Redmond, Washington and OpenGL® promulgated by the Khronos Group. The API communicates with a driver. The driver translates standard code received from the API into a native format of instructions understood by the GPU. The driver is typically written by the manufacturer of the GPU. The GPU then executes the instructions from the driver.

[0005] A graphics-processing task performed by a GPU typically involves complex mathematical computations, such as matrix and vector operations. To perform a single graphics-processing task, a GPU may execute a plurality of different threads (sequence of instructions). Each thread may comprise a shader program, such as a geometry shader, a pixel shader, a vertex shader, or the like. Each thread (e.g., shader program) is typically associated with a set of state data (such as texture handles, shader constants, transform matrices, or the like) that is locally stored in data-storage units of the GPU. The locally stored state data is called a *context*.

[0006] To efficiently execute the various threads (e.g., shader programs) of a single graphics-processing task, the GPU includes an array of processing elements, called a shader core. The array of processing elements is organized into single-instruction, multiple-data (SIMD) devices. Multiple threads (e.g., shader programs) may be issued to the shader core at the same time, with the data needed to execute each thread (e.g., shader program) being distributed in parallel to different processing elements of the shader core. The different processing elements may then perform operations on the data in parallel. In this way, a GPU can perform the complex mathematical computations required for a graphics-processing task more quickly than a typical central-processing unit (CPU). As a result, if a computing system includes a GPU, graphics-processing tasks (and other types of data-parallel processing tasks) are typically passed to the GPU, rather than the CPU.

[0007] To pass tasks to the GPU, an operating-system (OS) scheduler stores the tasks in a command buffer. A conventional GPU processes one command buffer at a time. The OS scheduler serially places tasks in the command buffer, and the GPU typically processes the tasks in the order in which they are placed in the command buffer. In some instances, however, the GPU may process tasks out of the order in which they were placed in the command buffer. For example, the GPU may interrupt the

execution of a first task to execute a more-important (e.g., low-latency) task that was placed in the command buffer after the first task.

[0008] To perform the more-important (e.g., low-latency) task before the first task has finished completing in the shader core of the GPU, a conventional GPU performs a *context switch*. That is, the state data associated with the threads of the first task are swapped into back-up storage units maintained by the conventional GPU, and new state data associated with the threads (e.g., shader programs) of the more-important (e.g., low-latency) task are retrieved and placed in the data-storage units of the shader core. The shader core then executes the threads (e.g., shader programs) of the more-important (e.g., low-latency) task based on the new state data in the data-storage units. After the more-important (e.g., low-latency) task finishes executing, the state data associated with the threads of the more-important (e.g., low-latency) task are flushed from the data-storage units, and the state data from the threads of the first task are swapped back into the data-storage units of the shader core. Then, the shader core can resume executing the threads of the first task.

[0009] Although context switching allows a GPU to process tasks out of the order in which they were placed in the command buffer, context switching is problematic for several reasons. As an initial matter, a substantial amount of time is required to perform a context switch, thereby limiting the performance of the GPU. Also, context switching requires additional local memory (e.g., back-up storage units) to store the context that is being switched. The additional local memory takes up precious chip area, resulting in a larger GPU.

[0010] In addition to requiring a substantial amount of time and area, context switching makes the GPU ineffective at processing low-latency, high-priority tasks. To prepare the shader core for executing a low-latency, high-priority task, a conventional GPU must perform a context switch. The time associated with the context switch (e.g., hundreds of clock cycles) makes the *effective* time for executing the low-latency, high-priority task relatively long, even though the *actual* time for executing the low-latency, high-priority task may be relatively short (e.g., tens of clock cycles).

[0011] Given the foregoing, what is needed is a processing unit that can efficiently process important (e.g., low-latency) tasks without context switching.

BRIEF SUMMARY OF EMBODIMENTS OF THE INVENTION

- [0012] Embodiments of the present invention meet the above-described needs by providing methods, apparatuses, and systems for enabling asynchronous task dispatch and applications thereof.
- [0013] For example, an embodiment of the present invention provides a processing unit that includes a plurality of virtual engines and a shader core. The plurality of virtual engines is configured to (i) receive, from an operating system (OS), a plurality of tasks substantially in parallel with each other and (ii) load a set of state data associated with each of the plurality of tasks. The shader core is configured to execute the plurality of tasks substantially in parallel based on the set of state data associated with each of the plurality of tasks. The processing unit may also include a scheduling module that schedules the plurality of tasks to be issued to the shader core.
- [0014] In another embodiment, the processing unit is defined in software. In this embodiment, a computer-program product includes a computer-readable storage medium containing instructions which, if executed on a computing device, define the processing unit.
- [0015] In a further embodiment, the processing unit is included in a computing system. In this embodiment, the computing system includes a memory, a first processing unit, a second processing unit, and a bus coupled to the memory, the first processing unit, and the processing unit. An example computing system may include, but is not limited to, a supercomputer, a desktop computer, a laptop computer, a video-game console, an embedded device, a handheld device (e.g., a mobile telephone, smart phone, MP3 player, a camera, a GPS device, or the like), or some other device that includes or is configured to include a processing unit.
- [0016] Another embodiment of the present invention provides a computer-implemented method for processing tasks in a processing unit. This computer-implemented method includes several operations. In a first operation, a plurality of tasks are received, from an operating system (OS), in parallel with each other. In a second operation, a set of state data associated with each of the plurality of tasks is loaded. In a third operation, the plurality of tasks are executed substantially in parallel in a shader core based on the set of state data associated with each of the

plurality of tasks. This computer-implemented method may also include scheduling the plurality of tasks to be issued to the shader core.

[0017] A further embodiment of the present invention provides a computer-implemented method for providing tasks to a processing unit. This method includes several operations. In a first operation, a plurality of tasks are received from one or more applications, wherein each task includes an indication of a priority type. In a second operation, the processing unit is provided with the plurality of tasks and the indication of the priority type associated with each task. In an embodiment, instructions stored on a computer-readable storage medium of a computer-program product may cause a computing device to perform this method, if the instructions are executed by the computing device.

[0018] Further features and advantages of the invention, as well as the structure and operation of various embodiments of the invention, are described in detail below with reference to the accompanying drawings. It is noted that the invention is not limited to the specific embodiments described herein. Such embodiments are presented herein for illustrative purposes only. Additional embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

BRIEF DESCRIPTION OF THE DRAWINGS/FIGURES

[0019] The accompanying drawings, which are incorporated herein and form part of the specification, illustrate the present invention and, together with the description, further serve to explain the principles of the invention and to enable a person skilled in the relevant art(s) to make and use the invention.

[0020] FIG. 1 is a block diagram illustrating an example computer system in accordance with an embodiment of the present invention.

[0021] FIG. 2 is a block diagram of an example GPU in accordance with an embodiment of the present invention.

[0022] FIGS. 3A and 3B are block diagrams illustrating example work flows for issuing tasks to virtual engines of a GPU in accordance with an embodiment of the present invention.

[0023] FIG. 4 illustrates a more-detailed example work flow for issuing tasks to virtual engines of a GPU in accordance with an embodiment of the present invention.

[0024] FIG. 5 depicts a block diagram of an example computer system in which an embodiment of the present invention may be implemented.

[0025] The features and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings, in which like reference characters identify corresponding elements throughout. In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally similar elements. The drawing in which an element first appears is indicated by the leftmost digit(s) in the corresponding reference number.

DETAILED DESCRIPTION

I. Overview

[0026] Embodiments of the present invention provide a processing unit that enables asynchronous task dispatch and applications thereof. In the detailed description that follows, references to "one embodiment," "an embodiment," "an example embodiment," etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases are not necessarily referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with an embodiment, it is submitted that it is within the knowledge of one skilled in the art to affect such feature, structure, or characteristic in connection with other embodiments whether or not explicitly described.

[0027] In accordance with an embodiment, a processing unit includes a plurality of virtual engines embodied on a single shader core. Each virtual engine is configured to receive data-parallel processing tasks (e.g., graphics-processing tasks and general-compute tasks) and independently execute these tasks on the single shader core. In this way, the processing unit may execute two or more different streams of processing tasks — such as, a first stream of low-latency processing tasks and a second stream of standard graphics-processing tasks — without requiring a context switch. Executing two or more different streams of processing tasks provides the low-latency benefits of

context switching without the overhead associated with stopping and draining the processing unit of data. In fact, embodiments of the present invention enable multiple contexts to exist and be executed (substantially) simultaneously in a single shader core.

[0028] For illustrative purposes only, and not limitation, embodiments of the present invention will be described herein in terms of a GPU. A person skill in the relevant art(s) will appreciate, however, that embodiments of the present invention may be applied to other types of processing units, such as central processing units and coprocessors, that receive streams of processing tasks. These other types of processors are contemplated within the spirit and scope of the present invention.

[0029] In embodiments, the GPU processes a plurality of commands buffers. Low-latency processing tasks may, for example, be placed in a first command buffer, and standard graphics-processing tasks may, for example, be placed in a second command buffer. A first virtual engine of the GPU retrieves the low-latency processing tasks, and a second virtual engine of the GPU retrieves the standard graphics-processing tasks. Tasks from each virtual engine are then issued to a single shader core substantially in parallel with each other.

[0030] To enable the single shader core to (substantially) simultaneously process tasks from two or more different virtual engines, resources of the shader core are partitioned in space and/or time. To achieve spatial partitioning, for example, a first (e.g., low-latency) task from a first virtual engine is issued to a first subset of processing elements (SIMDs) of the shader core, and a second (e.g., standard graphics) task from a second virtual engine is issued to a second subset of processing elements (SIMDs) of the shader core. To achieve temporal partitioning, for example, the first and second tasks share a percentage of time of the processing elements (SIMDs) of the shader core. In an embodiment, the GPU includes a scheduling module to schedule the tasks from the two or more different virtual engines for execution on the shader core.

[0031] Sharing the resources of the GPU to provide a plurality of virtual engines in accordance with embodiments of the present invention improves the use of the GPU resources, especially on large chips. Two or more streams of tasks can be issued to a single shader core, enabling the GPU to efficiently use computational and

input/output facilities. For example, resources (e.g., SIMDs) of the GPU shader core can be divided between concurrent tasks based on demand, priority, and/or preset limits — while temporarily enabling any one task to (substantially) fully consume the resources of the GPU.

[0032] Further details of an example GPU in accordance with an embodiment of the present invention are described below. Before providing these details, however, it is helpful to describe an example system in which such a GPU may be implemented.

II. An Example System

[0033] FIG. 1 is a block diagram of a computing system 100 according to an embodiment. Computing system 100 includes a CPU 102, a GPU 110, and may optionally include a coprocessor 112. In the embodiment of FIG. 1, CPU 102 and GPU 110 are shown as separate blocks. This is for illustrative purposes only, and not limitation. A person skilled in the relevant art(s) will understand that CPU 102 and GPU 110 may be included in separate packages or may be combined in a single package or integrated circuit.

[0034] Computing system 100 also includes a system memory 104 that may be accessed by CPU 102, GPU 110, and coprocessor 112. In embodiments, computing system 100 may comprise a supercomputer, a desktop computer, a laptop computer, a video-game console, an embedded device, a handheld device (e.g., a mobile telephone, smart phone, MP3 player, a camera, a GPS device, or the like), or some other device that includes or is configured to include a GPU.

[0035] GPU 110 assists CPU 102 by performing certain special functions (such as, graphics-processing tasks and data-parallel, general-compute tasks), usually faster than CPU 102 could perform them in software. GPU 110 includes a plurality of virtual engines that share resources of a single shader core. In this way, the plurality of virtual engines of GPU 110 can execute a plurality of tasks substantially in parallel. In embodiments, GPU 110 may be integrated into a chipset and/or CPU 102. Additional details of GPU 110 are provided below.

[0036] Coprocessor 112 also assists CPU 102. Coprocessor 112 may comprise, but is not limited to, a floating point coprocessor, a GPU, a networking coprocessor, and

other types of coprocessors and processors as would be apparent to a person skilled in the relevant art(s).

[0037] GPU 110 and coprocessor 112 communicate with CPU 102 and the system memory over a bus 114. Bus 114 may be any type of bus used in computer systems, including a peripheral component interface (PCI) bus, an accelerated graphics port (AGP) bus, a PCI Express (PCIE) bus, or another type of bus whether presently available or developed in the future.

[0038] In addition to system memory 104, computing system 100 further includes local memory 106 and local memory 108. Local memory 106 is coupled to GPU 110 and may also be coupled to bus 114. Local memory 108 is coupled to coprocessor 112 and may also be coupled to bus 114. Local memories 106 and 108 are available to GPU 110 and coprocessor 112 respectively in order to provide faster access to certain data (such as data that is frequently used) than would be possible if the data were stored in system memory 104.

[0039] In an embodiment, GPU 110 and coprocessor 112 decode instructions in parallel with CPU 102 and execute only those instructions intended for them. In another embodiment, CPU 102 sends instructions intended for GPU 110 and coprocessor 112 to respective command buffers.

[0040] Although not specifically illustrated in FIG. 1, computing system 100 may also include or be coupled to a display device (e.g., cathode-ray tube, liquid crystal display, plasma display, or the like). The display device is used to display content to a user (such as, when computing system 100 comprises a computer, video-game console, or handheld device).

III. An Example GPU

[0041] As mentioned above, GPU 110 includes a plurality of virtual engines embodied on a shader core. Each virtual engine is configured to execute a stream of processing tasks provided by an OS scheduler, wherein each processing task of a given stream may include a plurality of individual processing threads. Because GPU 110 includes a plurality of virtual engines, GPU 110 can execute the different streams of processing tasks from the OS scheduler without requiring a context switch. In fact, in embodiments GPU 110 (substantially) simultaneously executes tasks from a

plurality of streams, which correspond to a plurality of different contexts, in a single shader core by sharing resources of the shader core among the tasks.

[0042] FIG. 2 is a block diagram illustrating example hardware components of GPU 110. Referring to FIG. 2, GPU 110 includes a command processor 230, input logic (including a vertex analyzer 208, scan converter 212, and arbitration logic 222), a shader core 214, output logic 224, and a memory system 210. Each of these components is described below.

A. Command Processor

[0043] Command processor 230 receives tasks (e.g., graphics-processing and general-compute tasks) from one or more command buffers filled by the OS scheduler. As illustrated in FIG. 3, command processor 230 includes a plurality of virtual engines that share resources of GPU 110. The different virtual engines of command processor 230 process different types of tasks.

[0044] In the embodiment of FIG. 2, command processor 230 includes a first background engine 202A, a second background engine 202B, a real-time low-latency engine 202C, a primary 3D engine 202D, and a low-latency 3D engine 202E. Background engines 202 process low-priority tasks. It is to be appreciated, however, that command processor 230 may include other types of virtual engines. Background engines 202 take over the resources of GPU 110 only when no other virtual engines are using the resources of GPU 110. Real-time low-latency engine 202C has priority access to the resources of GPU 110 in order to process high-priority tasks. Primary 3D engine 202D processes standard graphics-processing tasks, and low-latency 3D engine 202E processes high-priority graphics-processing tasks. Low-latency 3D engine 202E has priority access to the graphics-processing resources of GPU 110.

[0045] Before being issued to shader core 214 of GPU 110, tasks from command processor 230 are provided to input logic.

B. Input Logic

[0046] Input logic arbitrates which tasks are issued to shader core 214. In an embodiment, input logic implements a software routine to schedule the tasks for execution in shader core 214 based on the availability of the resources of shader

core 214 and the relative priority of the various tasks. In the embodiment of FIG. 3, input logic includes graphics pre-processing logic (which prepares graphics-processing tasks for issuance to shader core 214) and arbitration logic 222 (which provides tasks to shader core 214).

[0047] Graphics pre-processing logic includes vertex analyzer 208 and scan converter 212. Tasks from primary 3D engine 202D and low-latency 3D engine 202E are sent to the graphics pre-processing logic. First-in, first-out (FIFO) buffer 204A receives the tasks from primary 3D engine 202D, and FIFO buffer 204B receives the tasks from low-latency 3D engine 202E. Multiplexer 206 provides tasks from one of FIFO buffers 204 to vertex analyzer 208.

[0048] Vertex analyzer 208 identifies shader programs associated with a graphics-processing and/or general-compute task and schedules when each shader program can be launched in shader core 214 based on input and output data that will be available. In addition to scheduling shader programs for launch, vertex analyzer 208 also generates pointers to a vertex buffer and includes connectivity data. The pointers are used to read vertices from a vertex buffer. If a vertex has already been processed and is stored in the vertex buffer, vertex analyzer 208 may read that vertex from the vertex buffer, so that a vertex is only processed one time. The connectivity data specifies how vertices fit together to make a primitive (e.g., triangle), so that the primitive can be rasterized properly.

[0049] Vertex analyzer 208 sends graphics-processing tasks to scan converter 212 and sends general-compute tasks to arbitration logic 222. Scan converter 212 traverses the primitives to determine pixels to be processed by shader core 214. Scan converter 212 then sends the pixels to arbitration logic 222. Arbitration logic 222 includes a plurality of multiplexers to provide the tasks from the different virtual engines of command processor 230 to shader core 214.

C. Shader Core

[0050] Shader core 214 includes a plurality of processing elements 220 for executing the tasks provided to GPU 110. Processing elements 220 are arranged as SIMD devices, enabling shader core 214 to execute a plurality of data-parallel processing tasks (substantially) simultaneously. To enable shader core 214 to (substantially)

simultaneously process tasks from the plurality of virtual engines of command processor 230, processing elements 220 of shader core 214 are partitioned in space and/or time.

[0051] To achieve spatial partitioning, different subsets of processing elements 220 are configured to execute different tasks. For example, a first (e.g., low-latency) task from a first virtual engine (e.g., real-time low-latency engine 202C) may be issued to a first subset of processing elements 220 of shader core 214, and a second (e.g., standard graphics) task from a second virtual engine (e.g., primary 3D engine 202D) may be issued to a second subset of processing elements 220 of shader core 214. Each subset of processing elements 220 then independently executes the task it received.

[0052] To achieve temporal partitioning, different processing tasks of different virtual engines share a percentage of time of processing elements 220 of shader core 214. From the example above, the first and second tasks share a percentage of time of processing elements 220 of shader core 214.

[0053] Shader core 214 also includes one or more local data shares (LDS) 228 for storing data used by processing elements 220 to execute the processing tasks provided by the OS scheduler. LDS 228 stores state data associated with each task to be executed by shader core 214. In an embodiment, LDS 228 stores the state data of a plurality of different contexts, enabling shader core 214 to (substantially) simultaneously execute a plurality of different tasks from OS scheduler associated with the plurality of different contexts without requiring a context switch.

[0054] Intermediate results of processing elements 220 may be reprocessed in shader core 214. For example, processing elements 220 may implement a plurality of different shader programs (e.g., geometry shader, vertex shader, pixel shader, tessellation shader, or the like) to complete a single graphics-processing task provided by the OS scheduler. The intermediate results of the different shader programs are sent back to vertex analyzer 208 and/or scan converter 212 and eventually recirculated to processing elements 220. After processing elements 220 have completed a task provided by the OS scheduler, the final results are provided to output logic 224.

D. Output logic

[0055] Output logic 224 includes a plurality of buffers, including write-combining caches, depth buffers, and color buffers. The write-combining caches combine data to be written to off-chip memory, enabling efficient access to off-chip memory. The depth buffers buffer results for z-testing. The color buffers buffer results for color blending. After performing the processes associated with the write-combining caches, depth buffers, and color buffers, output logic 224 provides the results to memory system 210.

E. Memory System

[0056] Memory system 210 includes one or more on-chip caches and one or more off-chip memory interfaces. Memory system 210 is coupled to each of command processor 230, vertex analyzer 208, scan converter 212, shader core 214, and output logic 224. When data is needed by any of these components to execute a shader program, a request is made to the on-chip cache of memory system 210. If there is a hit in the on-chip cache (i.e., the requested data is in the on-chip cache), the data is forwarded to the component that requested it. If there is a miss in the on-chip cache (i.e., the requested data is not in the on-chip cache), the requested data must be retrieved from off-chip memory (e.g., system memory 104 of FIG. 1) via the off-chip memory interface of memory system 210. After the data is retrieved from off-chip memory, the data is forwarded to the component that requested it. In addition, the data is also stored in the on-chip cache using cache memory techniques that are well known to persons skilled in the relevant art(s).

IV. Example Operation

[0057] GPU 110 is configured to execute a plurality of streams of processing tasks provided by an OS scheduler. The plurality of streams of processing tasks may be generated by a single application or more than one application.

[0058] FIG. 3A illustrates an example in which shader core 214 (substantially) simultaneously executes two (or more) different streams of processing tasks, wherein the streams of processing tasks are generated by a single application 302. Application

302 may be, for example, an end-user application that generates graphics-processing tasks (such as a video-game application, a computer-aided design (CAD) application, or the like) or an end-user application that generates general-compute tasks (e.g., mathematical algorithms, physics simulations, or the like) to be executed on a GPU. Referring to FIG. 3A, application 302 generates a first task 308A and a second task 308B. Each task 308 that application 302 generates includes a priority type. For example, application 302 may indicate that first task 308A is a low-latency, high-priority task and second task 308B is a standard priority task. OS scheduler 310 receives the tasks generated by application 302 and issues the tasks to different virtual engines of GPU 110. For example, OS scheduler 310 issues first task 308A to a first virtual engine 312A and issues second task 308B to a second virtual engine 312B. The tasks from each virtual engine 312 are then (substantially) simultaneously executed by shader core 214 of GPU 110.

[0059] FIG. 3B illustrates an example in which shader core 214 (substantially) simultaneously executes two (or more) different streams of processing tasks, wherein each stream is generated by a different application. As illustrated in FIG. 3B, a first processing task 330A is generated by a first application 302A, and a second processing task 330B is generated by a second application 302B. Each task 330 includes a priority type. OS scheduler 310 receives tasks 330 and issues them to different virtual engines of GPU 110. For example, OS scheduler 310 issues first task 330A to a first virtual engine 332A and issues second task 330B to a second virtual engine 332B. The tasks from each virtual engine 332 are then (substantially) simultaneously executed by shader core 214 of GPU 110.

[0060] In the examples of FIGS. 3A and 3B, GPU 110 receives both the tasks and the priority types. To provide the priority type to GPU 110, application 302 provides bits to an API indicating the priority type of each task. The API, in turn, provides this information to the driver of GPU 110. In an embodiment, GPU 110 includes a scheduling module that schedules the tasks to be executed on shader core 214 based, at least in part, on the priority type specified by the application.

[0061] Although the examples of FIGS. 3A and 3B illustrate shader core 214 executing only two streams of processing tasks, this is for illustrative purposes only, and not limitation. It is to be appreciated that shader core 214 may (substantially)

simultaneously execute two or more streams of processing tasks generated by one or more applications.

[0062] For example, FIG. 4 is an example workflow, illustrating various layers of software and hardware between one or more applications running on a computing system (e.g., computing system 100) and GPU 110 included in the computing system. In the embodiment of FIG. 4, there are two different types of processing units, CPU 102 and GPU 110. In addition, two applications — a first application 402A and a second application 402B — are running on the computer system. CPU 102 provides the primary functionality required by applications 402. For example, CPU 102 may include a plurality of cores 412A-N, wherein first application 402A runs primarily on a first core 412A and second application 402B runs primarily on a second core 412N.

[0063] During the course of running, applications 402 may generate a plurality of tasks 404A-D to be executed on GPU 110 rather than CPU 102. Tasks 404 may comprise data-parallel processing tasks (e.g., graphics-processing tasks, general-compute tasks, or the like) that GPU 110 can likely perform faster than CPU 102 could perform them in software. Each task 404 includes an indication of the priority type as specified by the applications 402 (like the priority type included in the tasks illustrated in FIGS. 3A and 3B). In a conventional system, an OS scheduler would provide tasks 404 to a single command buffer in a serial fashion, and a conventional GPU would serially process the tasks. Unlike such a conventional system, OS scheduler 310 provides each task 404 to one of a plurality of command buffers 420A-N based on the priority type specified by the applications 402. For example, OS scheduler 310 provides a first type of task (e.g., high-priority tasks) to first command buffer 420A, a second type of task (e.g., graphics-processing tasks) to second command buffer 420B, and so on.

[0064] GPU 110 includes a plurality of virtual engines 432A-N, each configured to service one of command buffers 420A-N. For example, a first virtual engine 432A is configured to service first command buffer 420A; a second virtual engine 432B is configured to service second command buffer 420B; and an N-th virtual engine 432N is configured to service N-th command buffer 420N. Tasks from virtual engines 432 are then (substantially) simultaneously executed by shader core 214 as described above. In an embodiment, a scheduling module 434 of GPU 110 schedules the tasks

to be executed by shader core 214 based on at least the following conditions: (i) the priority type specified by applications 402; (ii) the relative priority between the tasks 404 processed by virtual engines 432; and (iii) the availability of resources within shader core 214. For example, scheduling module 434 may divide the resources of shader core 214 between concurrent tasks 404 based on demand, priority, and/or preset limits — while temporarily enabling any one of tasks 404 to fully consume the resources of GPU 110. By executing two or more different streams of processing tasks in shader core 214, GPU 110 provides the low-latency benefits of context switching without the overhead associated with the storing, swapping, and draining data associated with context switching.

V. Example Computer Implementation

[0065] Embodiments of the present invention may be implemented using hardware, software or a combination thereof and may be implemented in one or more computer systems or other processing systems. An example of a computer system 500 is shown in FIG. 5.

[0066] Computer system 500 includes one or more processors, such as processor 504. Processor 504 may be a general purpose processor (such as, a CPU 102) or a special purpose processor (such as, a GPU 110). Processor 504 is connected to a communication infrastructure 506 (*e.g.*, a communications bus, cross-over bar, or network). Various software embodiments are described in terms of this exemplary computer system. After reading this description, it will become apparent to a person skilled in the relevant art(s) how to implement the invention using other computer systems and/or architectures.

[0067] Computer system 500 includes a display interface 502 that forwards graphics, text, and other data from communication infrastructure 506 (or from a frame buffer not shown) for display on display unit 530.

[0068] Computer system 500 also includes a main memory 508, preferably random access memory (RAM), and may also include a secondary memory 510. The secondary memory 510 may include, for example, a hard disk drive 512 and/or a removable storage drive 514, representing a floppy disk drive, a magnetic tape drive, an optical disk drive, *etc.* The removable storage drive 514 reads from and/or writes

to a removable storage unit 518 in a well known manner. Removable storage unit 518 represents a floppy disk, magnetic tape, optical disk, *etc.* which is read by and written to by removable storage drive 514. As will be appreciated, the removable storage unit 518 includes a computer usable storage medium having stored therein computer software and/or data.

[0069] In alternative embodiments, secondary memory 510 may include other similar devices for allowing computer programs or other instructions to be loaded into computer system 500. Such devices may include, for example, a removable storage unit 522 and an interface 520. Examples of such may include a program cartridge and cartridge interface (such as that found in video game devices), a removable memory chip (such as an erasable programmable read only memory (EPROM), or programmable read only memory (PROM)) and associated socket, and other removable storage units 522 and interfaces 520, which allow software and data to be transferred from the removable storage unit 522 to computer system 500.

[0070] Computer system 500 may also include a communications interface 524. Communications interface 524 allows software and data to be transferred between computer system 500 and external devices. Examples of communications interface 524 may include a modem, a network interface (such as an Ethernet card), a communications port, a Personal Computer Memory Card International Association (PCMCIA) slot and card, *etc.* Software and data transferred via communications interface 524 are in the form of signals 528 which may be electronic, electromagnetic, optical or other signals capable of being received by communications interface 524. These signals 528 are provided to communications interface 524 via a communications path (*e.g.*, channel) 526. This channel 526 carries signals 528 and may be implemented using wire or cable, fiber optics, a telephone line, a cellular link, an radio frequency (RF) link and other communications channels.

[0071] In this document, the term “computer-readable storage medium” is used to generally refer to media such as removable storage drive 514 and a hard disk installed in hard disk drive 512. These computer program products provide software to computer system 500.

[0072] Computer programs (also referred to as computer control logic) are stored in main memory 508 and/or secondary memory 510. Computer programs may also be

received via communications interface 524. Such computer programs, when executed, enable the computer system 500 to perform the features of the present invention, as discussed herein. In particular, the computer programs, when executed, enable the processor 504 to perform the features of the present invention. Accordingly, such computer programs represent controllers of the computer system 500.

[0073] In an embodiment, the software may be stored in a computer program product and loaded into computer system 500 using removable storage drive 514, hard drive 512 or communications interface 524. The control logic (software), when executed by the processor 504, causes the processor 504 to perform the functions of embodiments of the invention as described herein.

VI. Example Software Implementations

[0074] In addition to hardware implementations of processing units (e.g., CPU 102 and/or GPU 110), such processing units may also be embodied in software disposed, for example, in a computer-readable medium configured to store the software (e.g., a computer-readable program code). The program code causes the enablement of embodiments of the present invention, including the following embodiments: (i) the functions of the systems and techniques disclosed herein (such as, providing tasks to GPU 110, scheduling tasks in GPU 110, executing tasks in GPU 110, or the like); (ii) the fabrication of the systems and techniques disclosed herein (such as, the fabrication of GPU 110); or (iii) a combination of the functions and fabrication of the systems and techniques disclosed herein.

[0075] This can be accomplished, for example, through the use of general-programming languages (such as C or C++), hardware-description languages (HDL) including Verilog HDL, VHDL, Altera HDL (AHDL) and so on, or other available programming and/or schematic-capture tools (such as circuit-capture tools). The program code can be disposed in any known computer-readable medium including semiconductor, magnetic disk, or optical disk (such as CD-ROM, DVD-ROM). As such, the code can be transmitted over communication networks including the Internet and internets. It is understood that the functions accomplished and/or structure provided by the systems and techniques described above can be represented in a core

(such as a GPU core) that is embodied in program code and may be transformed to hardware as part of the production of integrated circuits.

VII. Conclusion

[0076] It is to be appreciated that the Detailed Description section, and not the Summary and Abstract sections, is intended to be used to interpret the claims. The Summary and Abstract sections may set forth one or more but not all exemplary embodiments of the present invention as contemplated by the inventor(s), and thus, are not intended to limit the present invention and the appended claims in any way.

WHAT IS CLAIMED IS:

1. A processing unit comprising:
 - a plurality of virtual engines configured to (i) receive, from an operating system (OS), a plurality of tasks substantially in parallel with each other and (ii) load a set of state data associated with each of the plurality of tasks; and
 - a shader core configured to execute the plurality of tasks substantially in parallel based on the set of state data associated with each of the plurality of tasks.
2. The processing unit of claim 1, wherein the shader core comprises:
 - a first plurality of processing elements configured to execute a first task based on a first set of state data associated with the first task; and
 - a second plurality of processing elements configured to execute a second task based on a second set of state data associated with the second task.
3. The processing unit of claim 1, wherein the plurality of virtual engines comprises (i) a first queue configured to receive a first type of task and (ii) a second queue configured to receive a second type of task.
4. The processing unit of claim 3, wherein the first type of task comprises a low-latency task and the second type of task comprises a regular-latency task.
5. The processing unit of claim 3, wherein the first type of task comprises a graphics-processing task and the second type of task comprises a general-compute task.
6. The processing unit of claim 1, further comprising:
 - a scheduling module that schedules the plurality of tasks to be issued to the shader core.

7. A computer-program product comprising a computer-readable storage medium containing instructions that, if executed on a computing device, define a processing unit comprising:

a plurality of virtual engines configured to (i) receive, from an operating system (OS), a plurality of tasks substantially in parallel with each other and (ii) load a set of state data associated with each of the plurality of tasks; and

a shader core configured to execute the plurality of tasks substantially in parallel based on the set of state data associated with each of the plurality of tasks.

8. The computer-program product of claim 7, wherein the shader core comprises:
a first plurality of processing elements configured to execute a first task based on a first set of state data associated with the first task; and

a second plurality of processing elements configured to execute a second task based on a second set of state data associated with the second task.

9. The computer-program product of claim 7, wherein the plurality of virtual engines comprises (i) a first queue configured to receive a first type of task and (ii) a second queue configured to receive a second type of task.

10. The computer-program product of claim 9, wherein the first type of task comprises a low-latency task and the second type of task comprises a regular-latency task.

11. The computer-program product of claim 9, wherein the first type of task comprises a graphics-processing task and the second type of task comprises a general-compute task.

12. The computer-program product of claim 7, wherein the processor further comprises:

a scheduling module that schedules the plurality of tasks to be issued to the shader core.

13. A computing system, comprising:

a memory;

a processing unit; and

a bus coupled to the memory and the processing unit,

wherein the processing unit comprises:

a plurality of virtual engines configured to (i) receive, from an operating system (OS), a plurality of tasks substantially in parallel with each other and (ii) load a set of state data associated with each of the plurality of tasks; and

a shader core configured to execute the plurality of tasks substantially in parallel based on the set of state data associated with each of the plurality of tasks.

14. The computing system of claim 13, wherein the shader core comprises:

a first plurality of processing elements configured to execute a first task based on a first set of state data associated with the first task; and

a second plurality of processing elements configured to execute a second task based on a second set of state data associated with the second task.

15. The computing system of claim 13, wherein the plurality of virtual engines comprises (i) a first queue configured to receive a first type of task and (ii) a second queue configured to receive a second type of task.

16. The computing system of claim 15, wherein the first type of task comprises a low-latency task and the second type of task comprises a regular-latency task.

17. The computing system of claim 15, wherein the first type of task comprises a graphics-processing task and the second type of task comprises a general-compute task.

18. The computing system of claim 13, wherein the processing unit further comprises:

a scheduling module that schedules the plurality of tasks to be issued to the shader core.

19. A computer-implemented method for processing tasks in a processing unit, comprising:

receiving, from an operating system (OS), a plurality of tasks in parallel with each other;

loading a set of state data associated with each of the plurality of tasks; and

executing the plurality of tasks substantially in parallel in a shader core based on the set of state data associated with each of the plurality of tasks.

20. The computer-implemented method of claim 19, wherein the executing comprises:

executing a first task in a first plurality of processing elements of the shader core based on a first set of state data associated with the first task; and

executing a second task in a second plurality of processing elements of the shader core based on a second set of state data associated with the second task.

21. The computer-implemented method of claim 19, wherein the receiving comprises:

queueing a first type of task in a first queue; and

queueing a second type of task in a second queue.

22. The computer-implemented method of claim 21, wherein the first type of task comprises a low-latency task and the second type of task comprises a regular-latency task.

23. The computer-implemented method of claim 21, wherein the first type of task comprises a graphics-processing task and the second type of task comprises a general-compute task.

24. The computer-implemented method of claim 19, further comprising:
scheduling the plurality of tasks to be issued to the shader core by using a scheduling module of the processing unit.

25. A computer-implemented method for providing tasks to a processing unit, comprising:

receiving a plurality of tasks from one or more applications, wherein each task includes an indication of a priority type; and

providing, to the processing unit, the plurality of tasks and the indication of the priority type associated with each task.

A PROCESSING UNIT THAT ENABLES ASYNCHRONOUS TASK DISPATCH

ABSTRACT

A processing unit that includes a plurality of virtual engines and a shader core. The plurality of virtual engines is configured to (i) receive, from an operating system (OS), a plurality of tasks substantially in parallel with each other and (ii) load a set of state data associated with each of the plurality of tasks. The shader core is configured to execute the plurality of tasks substantially in parallel based on the set of state data associated with each of the plurality of tasks. The processing unit may also include a scheduling module that schedules the plurality of tasks to be issued to the shader core.

1051018_1.DOC

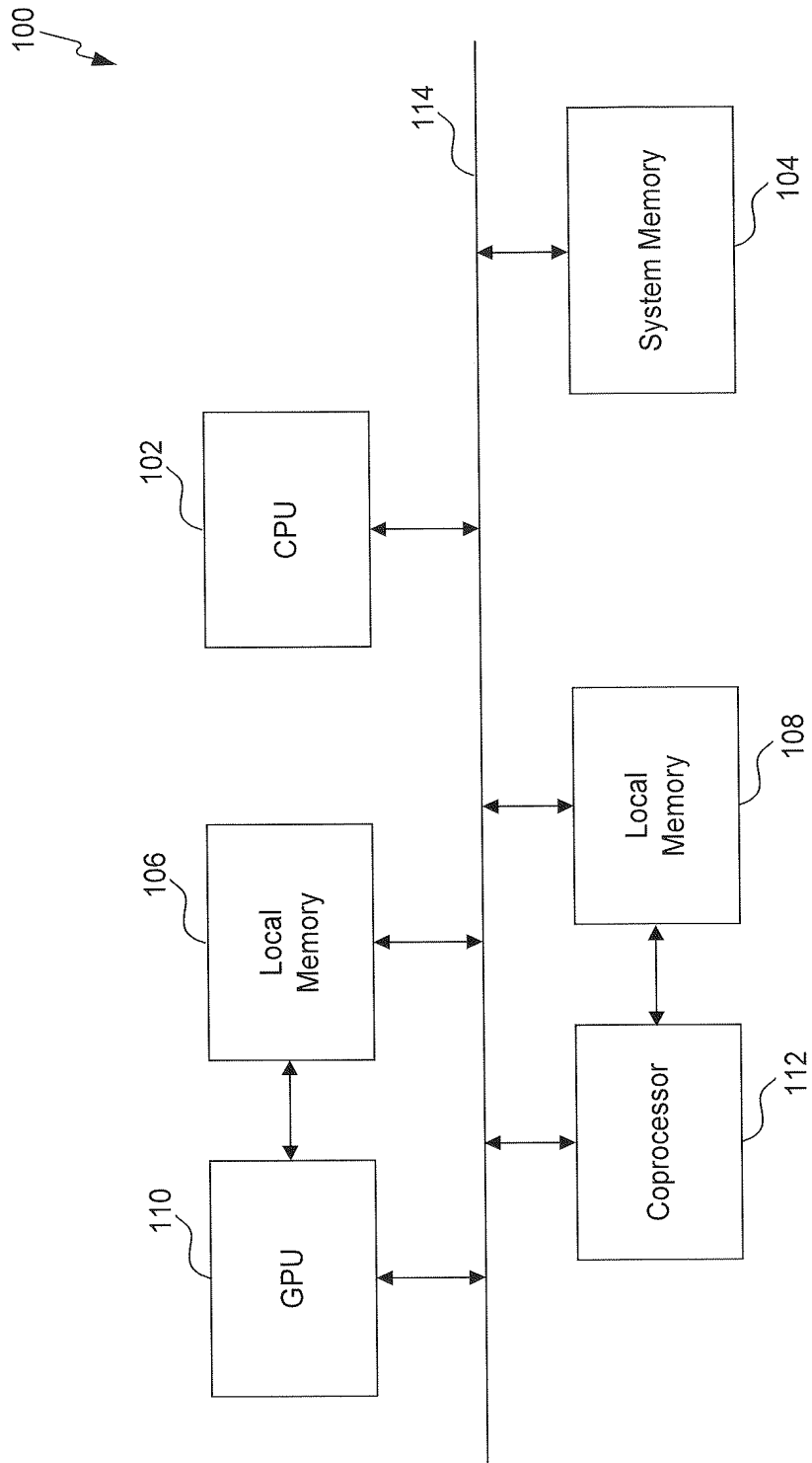


FIG. 1

1022173v1/1

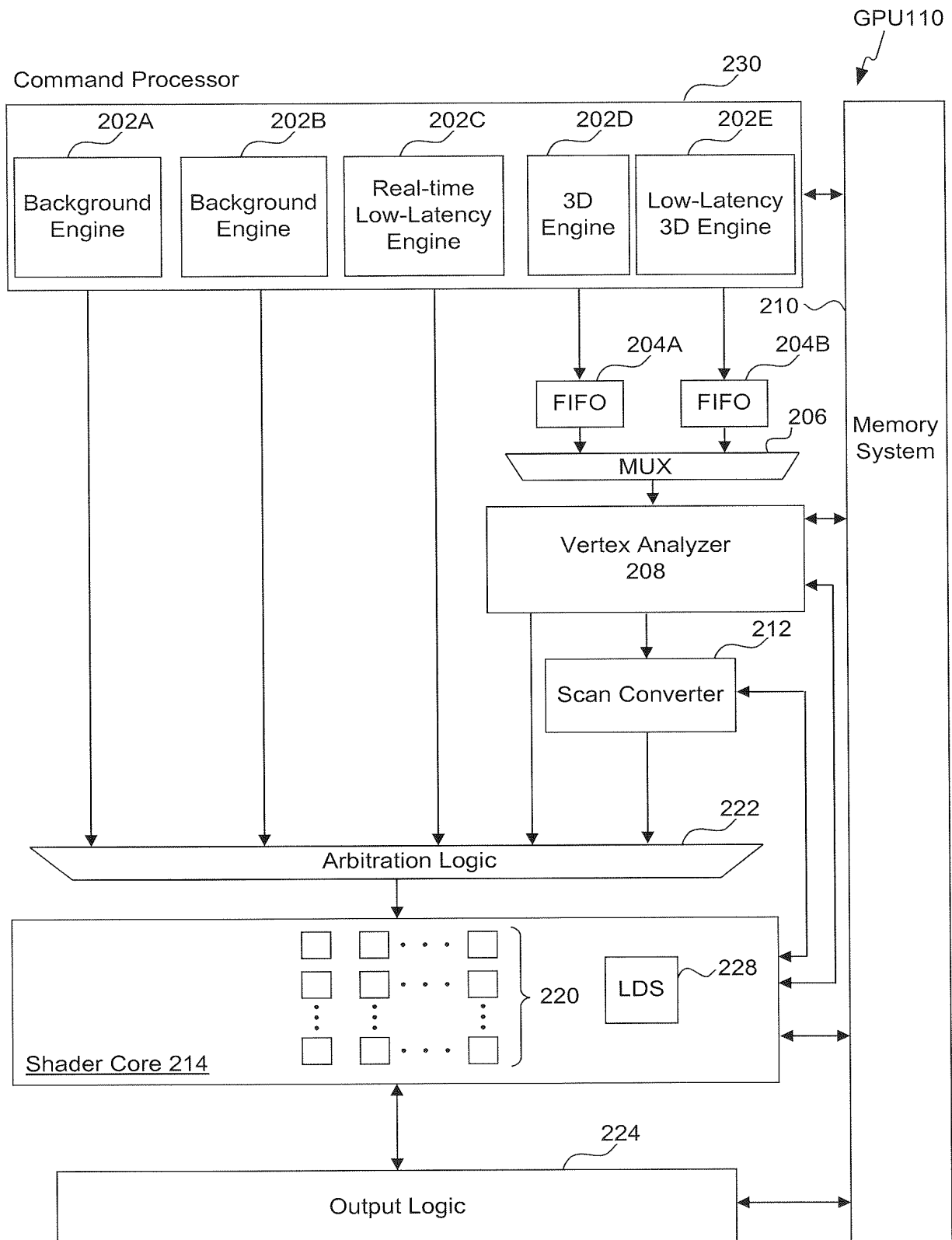


FIG. 2

1022173v1/2

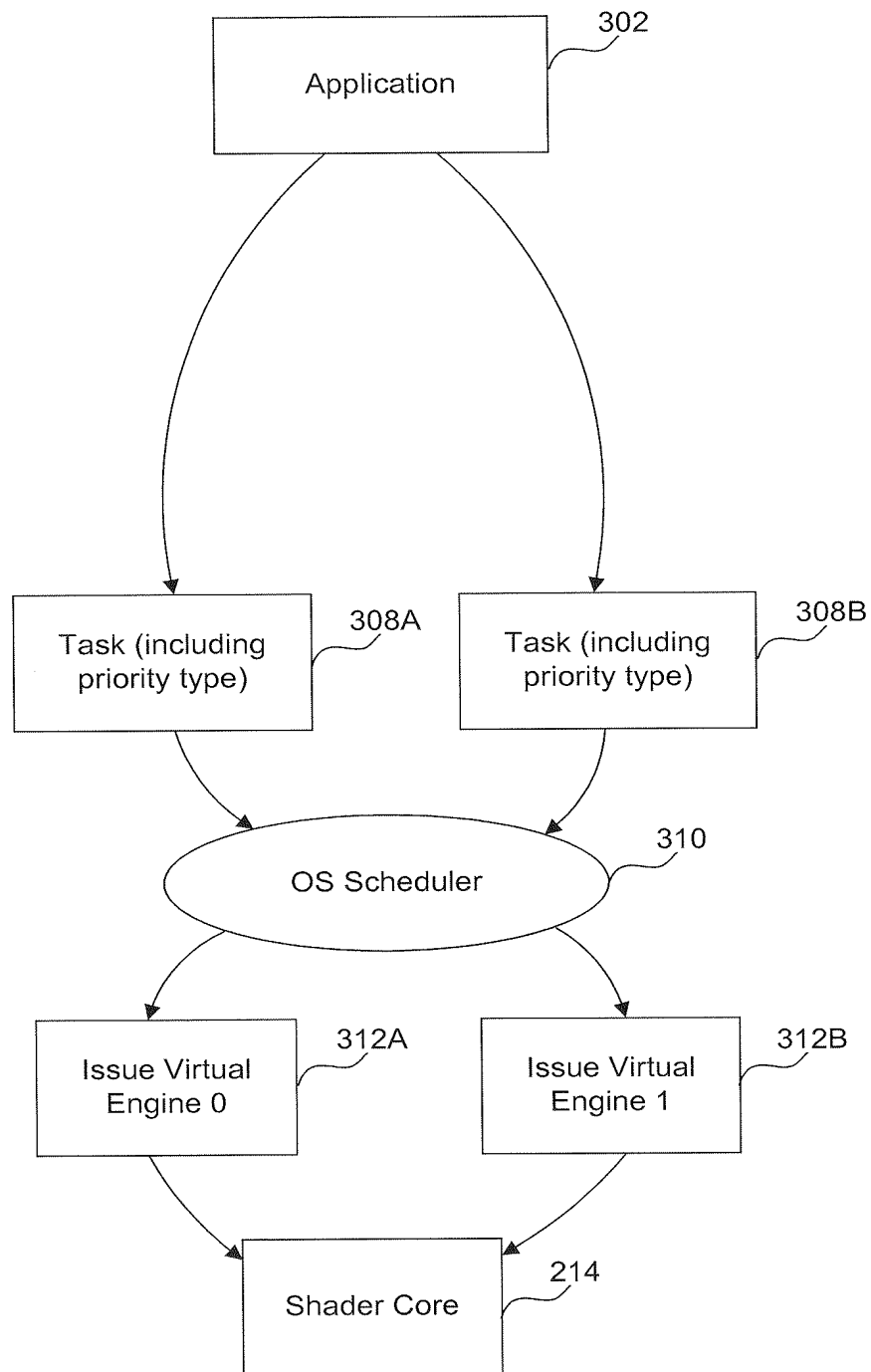


FIG. 3A

1022173v1/3

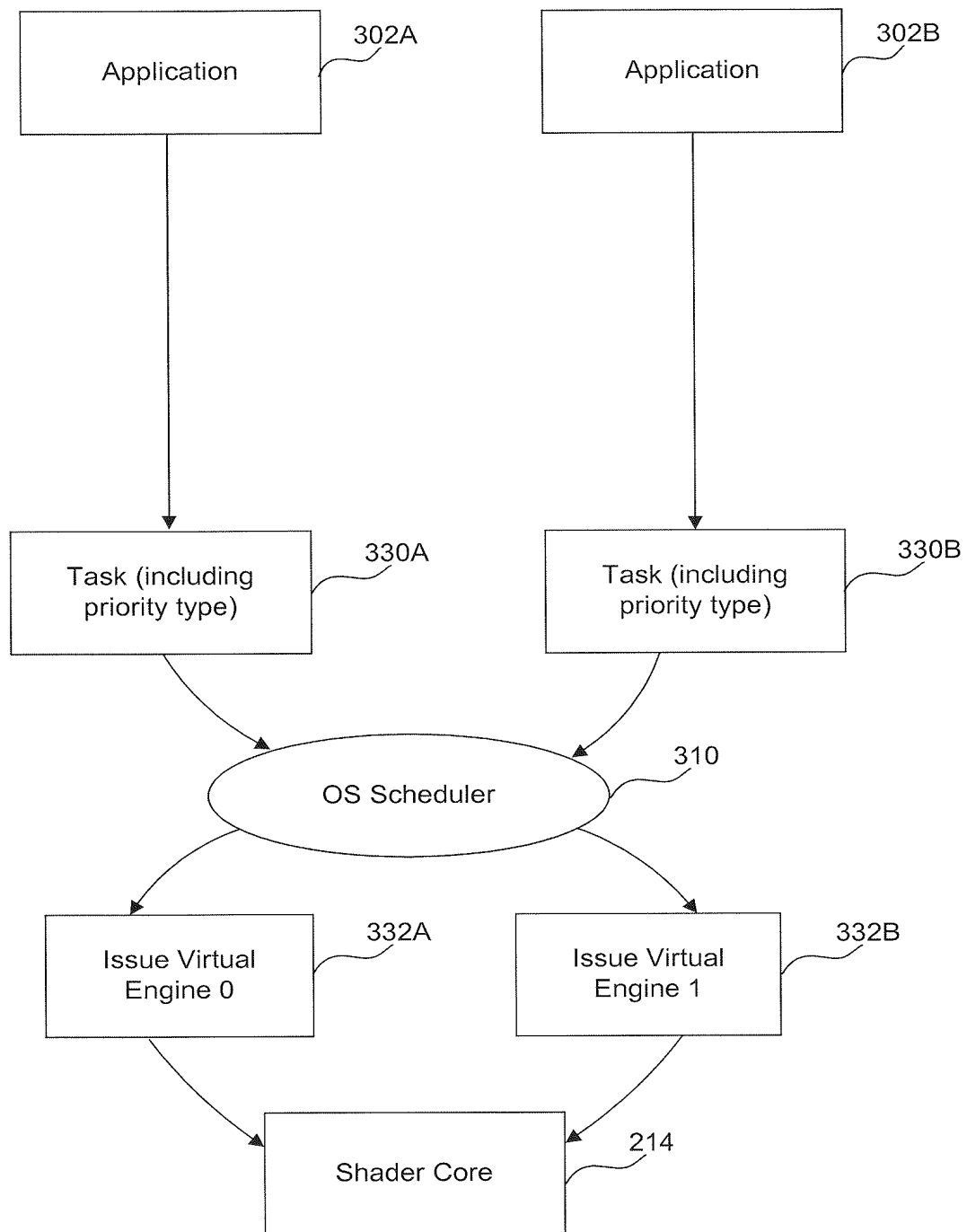


FIG. 3B

1022173v1/4

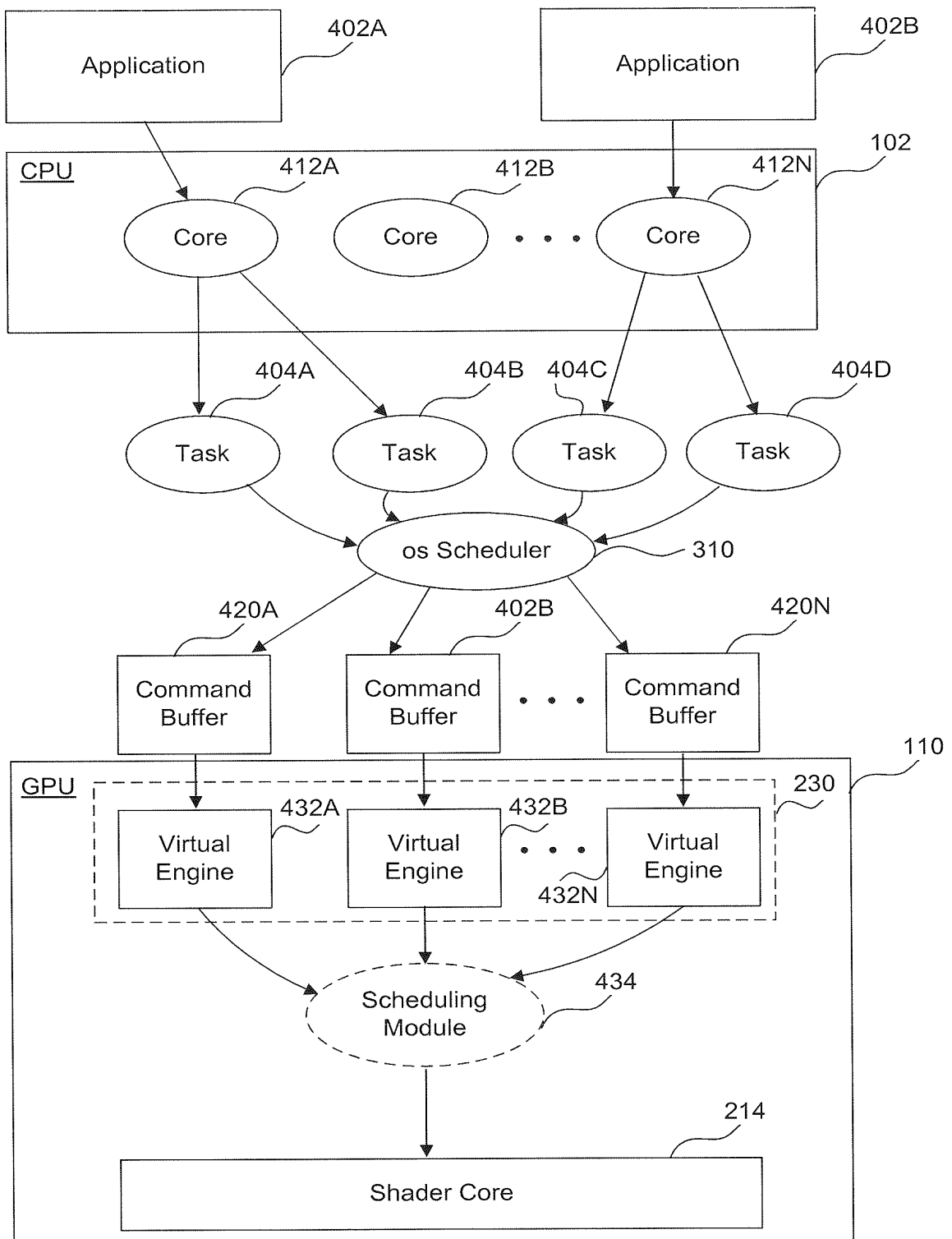


FIG. 4

1022173v1/5

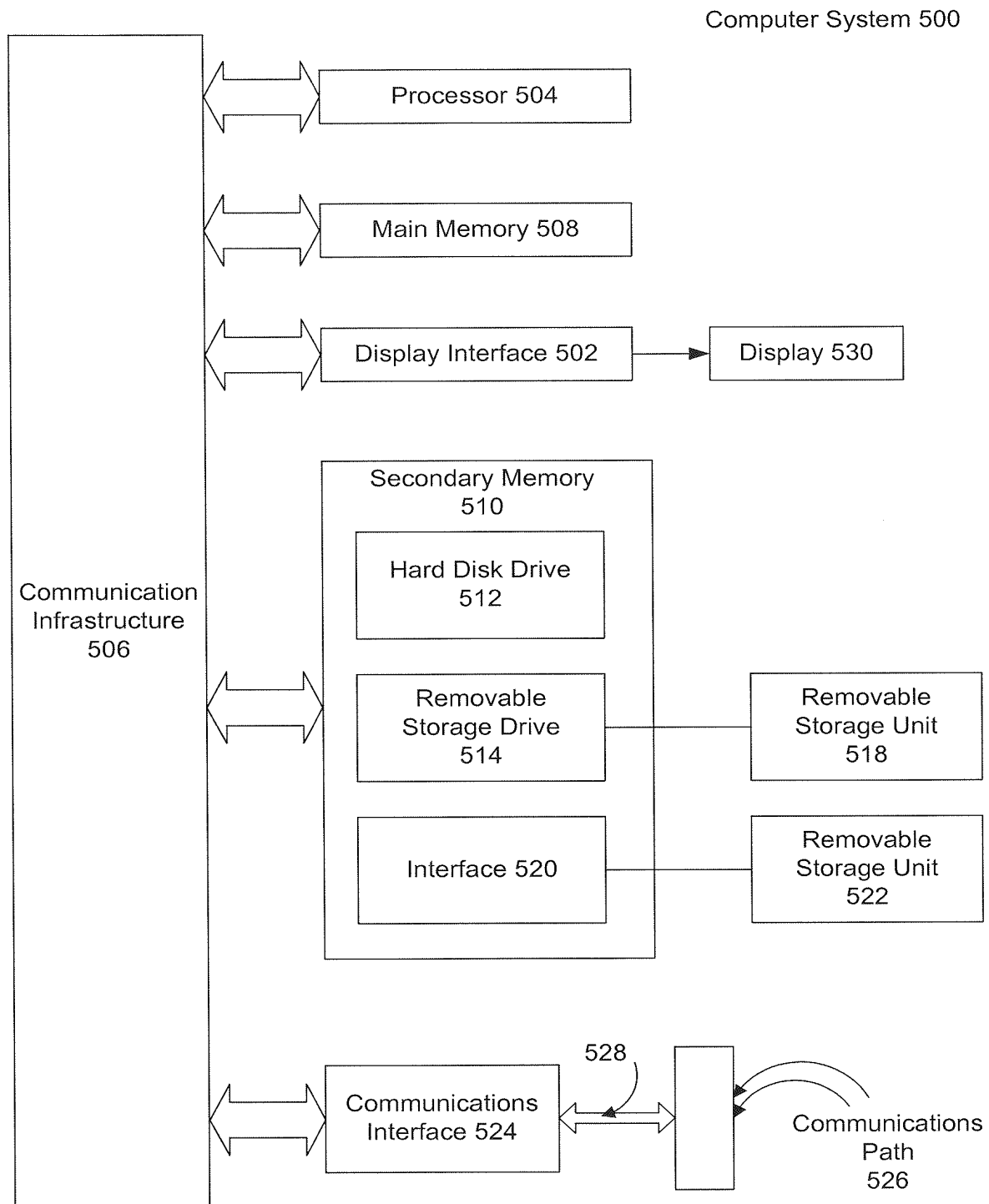


FIG. 5

1022173v1/6

Electronic Acknowledgement Receipt

EFS ID:	8340970
Application Number:	12874134
International Application Number:	
Confirmation Number:	6612
Title of Invention:	A Processing Unit that Enables Asynchronous Task Dispatch
First Named Inventor/Applicant Name:	Michael MANTOR
Customer Number:	26111
Filer:	Jonathan Tuminaro/Kim Perry
Filer Authorized By:	Jonathan Tuminaro
Attorney Docket Number:	1972.1540001
Receipt Date:	01-SEP-2010
Filing Date:	
Time Stamp:	19:46:03
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		19721540001.pdf	2264288 3a958e46d4969999b8c9fa77c74a5fe2438800db	yes	37

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Miscellaneous Incoming Letter	1	2
	Transmittal of New Application	3	3
	Authorization for Extension of Time all replies	4	4
	Application Data Sheet	5	7
	Specification	8	26
	Claims	27	30
	Abstract	31	31
	Drawings-only black and white line drawings	32	37

Warnings:

Information:

Total Files Size (in bytes):	2264288
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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September 1, 2010

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: U.S. Non-Provisional Utility Patent Application under 37 C.F.R. § 1.53(b)
Appl. No. To Be Assigned; Filed: Herewith
For: **A Processing Unit that Enables Asynchronous Task Dispatch**
Inventors: MANTOR *et al.*
Our Ref: 1972.1540001

Sir:

The following documents are transmitted herewith for appropriate action by the U.S. Patent and Trademark Office:

1. Utility Patent Application Transmittal Form (PTO/SB/05);
2. Authorization to Treat a Reply As Incorporating An Extension of Time Under 37 C.F.R. § 1.136(a)(3);
3. U.S. Utility Patent Application entitled:

A Processing Unit that Enables Asynchronous Task Dispatch

and naming as inventors:

Michael MANTOR and Rex MCCRARY

the application comprising:

- a. an Application Data Sheet (37 C.F.R. § 1.76);
- b. specification containing:
 - i. 19 pages of description prior to the claims;
 - ii. 4 pages of claims (25 claims);
 - iii. a one (1) page abstract; and
- c. 6 sheets of drawings: (Figures 1, 2, 3A, 3B, 4 and 5).

Realtek Ex. 1002

Commissioner for Patents
September 1, 2010
Page 2

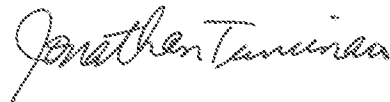
The above-listed documents are filed electronically through EFS-Web.

Correspondence should be sent to Customer Number 26111.

This patent application is being submitted under 37 C.F.R. § 1.53(b) without Declaration and without filing fee.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



Jonathan Tuminaro
Attorney for Applicants
Registration No. 61,327

TAW/JT/kc
Enclosures

Filing Date:

09/01/10

Approved for use through 7/31/2006. OMB 0651-0032

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

12/874,134

APPLICATION AS FILED – PART I

(Column 1)

(Column 2)

SMALL ENTITY

OTHER THAN
SMALL ENTITY

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE (37 CFR 1.16(a), (b), or (c))		
SEARCH FEE (37 CFR 1.16(k), (l), or (m))		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		
TOTAL CLAIMS (37 CFR 1.16(i))	25 minus 20 =	5
INDEPENDENT CLAIMS (37 CFR 1.16(h))	5 minus 3 =	2
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))		

RATE (\$)	FEE (\$)
X 26 =	
X 110 =	
N/A	
TOTAL	

OR

RATE (\$)	FEE (\$)
	330
	540
	220
X 52 =	260
X 220 =	440
N/A	
TOTAL	1790

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

(Column 1)

(Column 2)

(Column 3)

SMALL ENTITY

OTHER THAN
SMALL ENTITY

AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total (37 CFR 1.16(i))	*	Minus	**	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=
	Application Size Fee (37 CFR 1.16(s))				
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					

RATE (\$)	ADDITIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL ADD'T FEE	

OR

OR

OR

OR

OR

RATE (\$)	ADDITIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL ADD'T FEE	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
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	Independent (37 CFR 1.16(h))	*	Minus	***	=
	Application Size Fee (37 CFR 1.16(s))				
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					

RATE (\$)	ADDITIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL ADD'T FEE	

OR

OR

OR

OR

OR

RATE (\$)	ADDITIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Realtek Ex. 1002

Case No. IPR2023-00687

Page 40 of 228



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/874,134	09/01/2010	2628	0.00	1972.1540001	25	5

CONFIRMATION NO. 6612

26111

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

FILING RECEIPT



OC000000043637816

Date Mailed: 09/24/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Michael MANTOR, Orlando, FL;
Rex McCrary, Oviedo, FL;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/239,712 09/03/2009

Foreign Applications

If Required, Foreign Filing License Granted: 09/21/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/874,134**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

Processing Unit that Enables Asynchronous Task Dispatch

Preliminary Class

345

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER**Title 35, United States Code, Section 184****Title 37, Code of Federal Regulations, 5.11 & 5.15****GRANTED**

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/874,134	09/01/2010	Michael MANTOR	1972.1540001

CONFIRMATION NO. 6612

FORMALITIES LETTER



OC000000043637817

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Date Mailed: 09/24/2010

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
Applicant must submit \$330 to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).
- The oath or declaration is missing.
A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Additional claim fees of \$700 as a non-small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.
- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of \$130 for a non-small entity, must be submitted with the missing items identified in this notice.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is \$1920 for a non-small entity

- \$330 Statutory basic filing fee.
- \$130 Surcharge.
- The application search fee has not been paid. Applicant must submit \$540 to complete the search fee.

- The application examination fee has not been paid. Applicant must submit **\$220** to complete the examination fee for a non-small entity.
- Total additional claim fee(s) for this application is **\$700**
 - **\$440** for **2** independent claims over 3.
 - **\$260** for **5** total claims over 20.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.

<https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at <http://www.uspto.gov/ebc>.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/tle/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

RAYMOND J. WERNER
OF COUNSEL
(202) 772-8711
RWERNER@SKGF.COM



January 31, 2011

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 6612
Mail Stop Missing Parts

Re: U.S. Patent Application
Appl. No. 12/874,134; Filed: September 1, 2010
For: **A Processing Unit that Enables Asynchronous Task Dispatch**
Inventors: MANTOR *et al.*
Our Ref: 1972.1540001

Sir:

In reply to the "Notice to File Missing Parts of Non-Provisional Application," dated September 24, 2010, Applicants transmit the following documents for appropriate action by the U.S. Patent and Trademark Office:

1. Online Credit Card Payment Authorization for \$3,030.00 to cover:

<u>\$1,090.00</u>	Patent Application fee (including basic filing, search and examination fees);
<u>\$ 700.00</u>	Excess claims fee;
<u>\$ 130.00</u>	Surcharge for late filing fee or Declaration; and
<u>\$1,110.00</u>	Petition for Extension of Time Under 37 C.F.R. § 1.136(a)(3);
2. Petition for Extension of Time Under 37 C.F.R. § 1.136(a) (Form PTO/SB/22);
3. Original Declaration, executed by Michael Mantor; and
4. Original Declaration, executed by Rex McCrary.

The above-listed documents are filed electronically through EFS-Web.

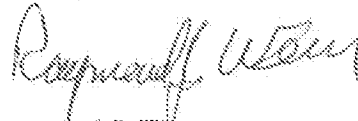
Realtek Ex. 1002

Commissioner for Patents
January 31, 2011
Page 2

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036. If extensions of time under 37 C.F.R. § 1.136 other than those otherwise provided for herewith are required to prevent abandonment of the present patent application, then such extensions of time are hereby petitioned, and any fees therefor are hereby authorized to be charged to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

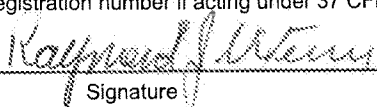


Raymond J. Werner
Attorney for Applicants
Registration No. 34,752

Enclosures

RJW/agj
1286208_1.DOC

Under the paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a) FY 2009 <i>(Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).)</i>		Docket Number (Optional) 1972.1540001	
Application Number 12/874,134		Filed September 1, 2010	
For A Processing Unit that Enables Asynchronous Task Dispatch			
Art Unit 2628		Examiner (To Be Assigned)	
This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application. The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):			
	<u>Fee</u>	<u>Small Entity Fee</u>	
☐ One month (37 CFR 1.17(a)(1))	\$130	\$65	\$ _____
☐ Two months (37 CFR 1.17(a)(2))	\$490	\$245	\$ _____
☒ Three months (37 CFR 1.17(a)(3))	\$1110	\$555	\$ <u>1,110.00</u>
☐ Four months (37 CFR 1.17(a)(4))	\$1730	\$865	\$ _____
☐ Five months (37 CFR 1.17(a)(5))	\$2350	\$1175	\$ _____
☐ Applicant claims small entity status. See 37 CFR 1.27.			
☐ A check in the amount of the fee is enclosed.			
☒ Payment by credit card. Form PTO-2038 is attached.			
☐ The Director has already been authorized to charge fees in this application to a Deposit Account.			
☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number <u>19-0036</u> .			
WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.			
I am the ☐ applicant/inventor.			
☐ assignee of record of the entire interest. See 37 CFR 3.71.			
Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96).			
☐ attorney or agent of record. Registration Number _____			
☒ attorney or agent under 37 CFR 1.34.			
Registration number if acting under 37 CFR 1.34 <u>34,752</u>			
 _____ Signature		<u>31 January 2011</u> _____ Date	
<u>Raymond J. Werner</u> _____ Typed or printed name		<u>(202) 371-2600</u> _____ Telephone Number	
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.			
☒ Total of <u>1</u> forms are submitted.			

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Declaration for Patent Application

Atty. Docket No. 1972.1540001

As a below named inventor, I hereby declare that:

My residence, mailing address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter that is claimed and for which a patent is sought on the invention entitled **A Processing Unit That Enables Asynchronous Task Dispatch**, the specification of which is attached hereto unless the following box is checked:

☒ was filed on September 1, 2010;
as United States Application Number or PCT International Application Number
12/874,134; and
was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. § 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

Authorization to Permit Access to Application by Participating Offices

☒ If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the above-identified application is filed access to the above-identified patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPC, or other intellectual property office in which a foreign application claiming priority to the above-identified application is filed to have access to the application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the application-as-filed with respect to: 1) the above-identified application, 2) any foreign application to which the above-identified application claims priority under 35 USC 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the above-identified US application, and 3) any U.S. application from which benefit is sought in the above-identified application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing the Authorization to Permit Access to Application by Participating Offices.

Claim of Foreign Priority Benefits

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or (f) or § 365(b) of any foreign application(s) for patent, inventor’s or plant breeder’s rights certificate(s), or § 365(a) of any PCT international application, which designated at least one country other than the United States of America, listed below, and have also identified below, by checking the box, any foreign application for patent, inventor’s or plant breeder’s rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?	
				YES	NO
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

Appl. No. 12/874,134
Atty. Docket No. 1972.1540001

Send Correspondence to: Customer No. 26111

Direct Telephone Calls to: (202) 371-2600

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first inventor:	Michael MANTOR
Signature of first inventor:	<i>Michael Mantor</i> Date: 1/24/2010
Residence:	Orlando, Florida
Citizenship:	US
Mailing Address:	1620 Pinar Drive Orlando, Florida 32825

Full name of second inventor:	Rex McCRARY
Signature of second inventor:	Date:
Residence:	Oviedo, Florida
Citizenship:	US
Mailing Address:	758 Summer Oaks Ct. Oviedo, Florida 32765

11/17/10 J.DOC

Declaration for Patent Application

Atty. Docket No. 1972.1540001

As a below named inventor, I hereby declare that:

My residence, mailing address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter that is claimed and for which a patent is sought on the invention entitled **A Processing Unit that Enables Asynchronous Task Dispatch**, the specification of which is attached hereto unless the following box is checked:

☐ was filed on ____;
as United States Application Number or PCT International Application Number ____;
and
was amended on ____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. § 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

Authorization to Permit Access to Application by Participating Offices

☐ If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the above-identified application is filed access to the above-identified patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPC, or other intellectual property office in which a foreign application claiming priority to the above-identified application is filed to have access to the application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the application-as-filed with respect to: 1) the above-identified application, 2) any foreign application to which the above-identified application claims priority under 35 USC 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the above-identified US application, and 3) any U.S. application from which benefit is sought in the above-identified application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing the Authorization to Permit Access to Application by Participating Offices.

Claim of Foreign Priority Benefits

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or (f) or § 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or § 365(a) of any PCT international application, which designated at least one country other than the United States of America, listed below, and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?	
				YES	NO
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

Send Correspondence to: Customer No. 26111

Direct Telephone Calls to: (202) 371-2600

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first Inventor:	Michael MANTOR
Signature of first Inventor:	Date:
Residence:	Orlando, Florida
Citizenship:	US
Mailing Address:	1620 Pinar Drive Orlando, Florida 32825

Full name of second Inventor:	Rex MCCRARY
Signature of second Inventor:	Date: Jan 25, 2011
Residence:	Oviedo, Florida
Citizenship:	US
Mailing Address:	758 Summer Oaks Ct. Oviedo, Florida 32765

1025965_1.DOC

Electronic Patent Application Fee Transmittal

Application Number:	12874134			
Filing Date:	01-Sep-2010			
Title of Invention:	Processing Unit that Enables Asynchronous Task Dispatch			
First Named Inventor/Applicant Name:	Michael MANTOR			
Filer:	Raymond Jay Werner/Angela G. Jones-Gardella			
Attorney Docket Number:	1972.1540001			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Claims in excess of 20	1202	5	52	260
Independent claims in excess of 3	1201	2	220	440
Miscellaneous-Filing:				

Realtek Ex. 1002

Case No. IPR2023-00687

Page 55 of 228

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Late filing fee for oath or declaration	1051	1	130	130
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 3 months with \$0 paid	1253	1	1110	1110
Miscellaneous:				
Total in USD (\$)				3030

Electronic Acknowledgement Receipt

EFS ID:	9338705
Application Number:	12874134
International Application Number:	
Confirmation Number:	6612
Title of Invention:	Processing Unit that Enables Asynchronous Task Dispatch
First Named Inventor/Applicant Name:	Michael MANTOR
Customer Number:	26111
Filer:	Raymond Jay Werner/Angela G. Jones-Gardella
Filer Authorized By:	Raymond Jay Werner
Attorney Docket Number:	1972.1540001
Receipt Date:	31-JAN-2011
Filing Date:	01-SEP-2010
Time Stamp:	11:25:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$3030
RAM confirmation Number	9911
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi-Page	Pages

Realtek Ex-1002
MessageID: 2028-00687
Case No: 2028-00687 (if appl.)

1		19721540001replytontfmp.pdf	2077266 166cdfa7bd169dd02cef87648e5f1413453fd33e	yes	9
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Applicant Response to Pre-Exam Formalities Notice		1	2	
	Extension of Time		3	3	
	Oath or Declaration filed		4	9	
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	41752 c97a7a9a27fe11ad252f32570d0bea75d48d0955	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			2119018		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/874,134	09/01/2010	2628	1920	1972.1540001	25	5

CONFIRMATION NO. 6612

26111

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

UPDATED FILING RECEIPT



Date Mailed: 02/08/2011

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Michael MANTOR, Orlando, FL;
Rex McCrary, Oviedo, FL;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/239,712 09/03/2009

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 09/21/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/874,134**

Projected Publication Date: 05/19/2011

Non-Publication Request: No

Early Publication Request: No

Title

Processing Unit that Enables Asynchronous Task Dispatch

Preliminary Class

345

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER**Title 35, United States Code, Section 184****Title 37, Code of Federal Regulations, 5.11 & 5.15****GRANTED**

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 12/874,134				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	330			
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	540			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	220			
TOTAL CLAIMS (37 CFR 1.16(j))	25 minus 20 =	*				x 52 =	260			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	5 minus 3 =	*				x 220 =	440			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	1790			
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x =			x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =			x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE			TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x =			x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =			x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE			TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										

POWER OF ATTORNEY FROM ASSIGNEE

Advanced Micro Devices, a corporation of Delaware, having a principal place of business at One AMD Place, Sunnyvale, California 94088, is assignee of the entire right, title, and interest for the United States of America (as defined in 35 U.S.C. §100), by reason of an Assignment to the Assignee executed on 1. _____ and 2. _____, of an invention known as **A Processing Unit that Enables Asynchronous Task Dispatch** (Attorney Docket No. 1972.1540001), that is disclosed and claimed in a patent application of the same title by the inventors Michael MANTOR and Rex MCCRARY (said application has a Filing Date or a 371(c) Date of September 1, 2010, at the U.S. Patent and Trademark Office, and having Application Number 12/874,134).

For the purpose of PAIR, the **Customer Number is 26111**.

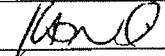
The Assignee hereby appoints the practitioners associated with **CUSTOMER NUMBER 26111** as my/our attorneys or agents to prosecute the application identified above, and any continuation, divisional, continuation-in-part, or reissue application thereof, and to transact all business in the U.S. Patent and Trademark Office connected therewith. The Assignee hereby grants said practitioners associated with **CUSTOMER NUMBER 26111** the power to insert on this Power of Attorney any further identification that may be necessary or desirable in order to comply with the rules of the U.S. Patent and Trademark Office.

Send correspondence to:

CUSTOMER NUMBER 26111

Direct phone calls to 202-371-2600.

FOR: Advanced Micro Devices

SIGNATURE: 

BY: KEVIN O'NEIL

TITLE: DIRECTOR, PATENTS & LICENSING

DATE: FEBRUARY 10, 2011

1087157_1.DOC

STATEMENT UNDER 37 CFR 3.73(b)

Atty. Docket No. 1972.1540001

Applicant/Patent Owner: Mantor et al.

Application No./Patent No.: 12/874,134 Filed/Issue Date: September 1, 2010

Titled: A Processing Unit that Enables Asynchronous Task Dispatch

Advanced Micro Devices, Inc., a

corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;
2. ☐ an assignee of less than the entire right, title, and interest in
(The extent (by percentage) of its ownership interest is _____ %); or
3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 025720, Frame 0001, or for which a copy therefore is attached.

OR

- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

- ☒ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Kevin O'Neil
Signature

KEVIN O'NEIL

Printed or Typed Name

February 10, 2011
Date

DIRECTOR - PATENTS & LICENSING
Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

PATENT APPLICATION

ASSIGNMENT OF U.S. PATENT APPLICATION

This is an assignment of patent rights between inventors **Michael MANTOR** and **Rex McCrary** (hereinafter referred to as "Inventors") and Advanced Micro Devices, Inc., having a place of business at One AMD Place, Sunnyvale, California 94088 (hereinafter referred to as "Assignee").

WHEREAS, Inventors have caused to be prepared a United States Patent Application in the Inventors' names entitled **A Processing Unit That Enables Asynchronous Task Dispatch**, having application no. 12/874,134, filed on September 1, 2010, having a docket number of 1972.1540001 (hereinafter referred to as the "Invention"); and

WHEREAS, Assignee has a desire to acquire all rights, title, and interest in the Invention.

NOW, THEREFORE, the parties agree as follows:

1. Inventors hereby sell, assign, and transfer their entire right, title, and interest in the Invention and all patents that may be granted therefrom due to divisions, reissue, substitutions, extensions, continuations, and continuations-in-part to the Assignee.
2. Inventors hereby sell, assign, and transfer their entire right, title, and interest in any foreign (non-U.S.) national patent application, invention registration, or equivalent (Foreign Applications) claiming approximately the same subject matter of the Invention to the Assignee.
3. The transfer set forth in Paragraph (2) is in consideration for the sum of one U.S. dollar (US\$1) (or its equivalent) and/or other consideration for which both parties acknowledge to be valuable, having been conveyed to the Inventors by the Assignee. Consideration may include at least one of the following: employment, an independent contractor agreement, monetary payment, or other benefit hereby acknowledged as received.
4. Inventors hereby authorize and request the Commissioner of Patents and Trademarks to issue the patent for the Invention, and all resulting patents therefrom, insofar as Inventor's interest is concerned, to the Assignee.
5. Inventors further agree to execute any and all powers of attorney, applications, assignments, declarations, affidavits, and any other papers in connection therewith necessary to perfect such rights, title, and interest in the Assignee.
6. Inventors hereby yet further agree to, with respect to the referenced patent application, at the expense of the Assignee:
 - i) testify in any legal proceedings,
 - ii) sign all lawful papers,
 - iii) execute all divisional, continuation, continuation-in-part, reissue and substitute applications,

Appl. No. 12/374,134
AMD File No. 918111

(iv) make all lawful oaths, and assist in vesting title in the Assignee and to aid the Assignee to obtain and enforce proper protection for the subject matter of the invention in all countries, and

v) notify Assignee promptly (by facsimile or first class mail) of any subpoena or contact by any person other than Assignee or its agents regarding the invention or resultant patent(s) issuing therefrom, and in any event at least one week prior to any deposition, legal inquiry or legal proceeding relating to the above identified invention.

This assignment is executed on the date(s) of which the Inventors have signed.

Inventor Signature:

Michael J. Mantor

Date 1/24/2011

State/Province of:

Florida

Regional Municipality of:

Orlando

Before me personally appeared said Michael MANTOR and acknowledge the foregoing instrument to be his free act and deed this _____ day of _____ 2010.

Seal

(Notary)

OR

Witness #1

[Signature]

(Signature)

CASIEL

(Print Name)

Witness #2

[Signature]

(Signature)

John H. Mantor

(Print Name)

Inventor Signature:

Date: _____

State/Province of: _____)

Regional Municipality of: _____)

Before me personally appeared said **Rex McCRARY** and acknowledge the foregoing instrument to be his free act and deed this _____ day of _____ 2010.

Seal

_____ (Notary)

OR

Witness # 1 _____ (Signature)

Witness#2 _____ (Signature)

_____ (Print Name)

_____ (Print Name)

PATENT APPLICATION

ASSIGNMENT OF U.S. PATENT APPLICATION

This is an assignment of patent rights between inventors **Michael MANTOR and Rex McCRARY** (hereinafter referred to as "Inventors") and Advanced Micro Devices, Inc., having a place of business at One AMD Place, Sunnyvale, California 94088 (hereinafter referred to as "Assignee").

WHEREAS, Inventors have caused to be prepared a United States Patent Application in the Inventors' names entitled **A Processing Unit That Enables Asynchronous Task Dispatch**, having application no _____, filed on _____, having a docket number of **1972.1540001** (hereinafter referred to as the "Invention"); and

WHEREAS, Assignee has a desire to acquire all rights, title, and interest in the Invention.

NOW, THEREFORE, the parties agree as follows:

1. Inventors hereby sell, assign, and transfer their entire right, title, and interest in the Invention and all patents that may be granted therefrom due to divisions, reissue, substitutions, extensions, continuations, and continuations-in-part to the Assignee.
2. Inventors hereby sell, assign, and transfer their entire right, title, and interest in any foreign (non-U.S.) national patent application, invention registration, or equivalent (Foreign Applications) claiming approximately the same subject matter of the Invention to the Assignee.
3. The transfer set forth in Paragraph (2) is in consideration for the sum of one U.S. dollar (US\$1) (or its equivalent) and/or other consideration for which both parties acknowledge to be valuable, having been conveyed to the Inventors by the Assignee. Consideration may include at least one of the following: employment, an independent contractor agreement, monetary payment, or other benefit hereby acknowledged as received.
4. Inventors hereby authorize and request the Commissioner of Patents and Trademarks to issue the patent for the Invention, and all resulting patents therefrom, insofar as Inventor's interest is concerned, to the Assignee.
5. Inventors further agree to execute any and all powers of attorney, applications, assignments, declarations, affidavits, and any other papers in connection therewith necessary to perfect such rights, title, and interest in the Assignee.
6. Inventors hereby yet further agree to, with respect to the referenced patent application, at the expense of the Assignee:
 - i) testify in any legal proceedings,
 - ii) sign all lawful papers,
 - iii) execute all divisional, continuation, continuation-in-part, reissue and substitute applications,

iv) make all lawful oaths, and assist in vesting title in the Assignee and to aid the Assignee to obtain and enforce proper protection for the subject matter of the Invention in all countries, and

v) notify Assignee promptly (by facsimile or first class mail) of any subpoena or contact by any person other than Assignee or its agents regarding the Invention or resultant patent(s) issuing therefrom, and in any event at least one week prior to any deposition, legal inquiry or legal proceeding relating to the above identified invention.

This assignment is executed on the date(s) of which the Inventors have signed.

Inventor Signature:

Date: _____

State/Province of: _____)

Regional Municipality of: _____)

Before me personally appeared said **Michael MANTOR** and acknowledge the foregoing instrument to be his free act and deed this _____ day of _____ 20____.

Seal

_____ (Notary)

OR

Witness # 1 _____ (Signature)

Witness#2 _____ (Signature)

_____ (Print Name)

_____ (Print Name)

Inventor Signature:

Rex McCrary

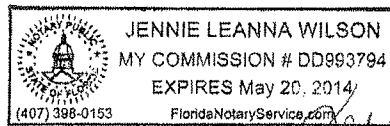
Date: Jan 25, 2011

State/Province of: FL

Regional Municipality of: Oviedo

Before me personally appeared said **Rex McCRARY** and acknowledge the foregoing instrument to be his free act and deed this 25th day of January 2011.

Seal



Jennie Leanna Wilson (Notary)

OR

Witness # 1 _____ (Signature)
_____ (Print Name)

Witness#2 _____ (Signature)
_____ (Print Name)

Electronic Acknowledgement Receipt

EFS ID:	9432100
Application Number:	12874134
International Application Number:	
Confirmation Number:	6612
Title of Invention:	Processing Unit that Enables Asynchronous Task Dispatch
First Named Inventor/Applicant Name:	Michael MANTOR
Customer Number:	26111
Filer:	Raymond Jay Werner/Angela G. Jones-Gardella
Filer Authorized By:	Raymond Jay Werner
Attorney Docket Number:	1972.1540001
Receipt Date:	11-FEB-2011
Filing Date:	01-SEP-2010
Time Stamp:	20:08:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		080131PowerofattorneyandStatement373.pdf	2019171 c22a4588535cca3aa7a79303dcac142c662483af	yes	9

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Miscellaneous Incoming Letter	1	1
	Power of Attorney	2	2
	Assignee showing of ownership per 37 CFR 3.73(b).	3	9
Warnings:			
Information:			
Total Files Size (in bytes):		2019171	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

RAYMOND J. WERNER
OF COUNSEL
(202) 772-8711
RWERNER@SKGF.COM



February 11, 2011

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 6612
Art Unit 2628

Re: U.S. Utility Patent Application
Application No. 12/874,134; Filing Date: September 1, 2010
For: **A Processing Unit that Enables Asynchronous Task Dispatch**
Inventors: MANTOR *et al.*
Our Ref: 1972.1540001

Sir:

Transmitted herewith for appropriate action are the following documents:

1. A copy of an original executed Power of Attorney from Assignee; and
2. A copy of an original executed Statement Under 37 C.F.R. § 3.73(b). The Assignment document was, or concurrently is, submitted for recordation pursuant 37 C.F.R. § 3.11.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Raymond J. Werner
Attorney for Applicants
Registration No. 34,752

Enclosures

TAW/RJW/agi
1320848_1.DOC



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/874,134	09/01/2010	Michael MANTOR	1972.1540001

CONFIRMATION NO. 6612

POA ACCEPTANCE LETTER

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005



Date Mailed: 02/22/2011

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/11/2011.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/s/brahim/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Title:Processing Unit that Enables Asynchronous Task Dispatch

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

MANTOR *et al.*

Appl. No.: 12/874,134

Filed: September 1, 2010

For: **Processing Unit that Enables
Asynchronous Task Dispatch**

Confirmation No.: 6612

Art Unit: 2628

Examiner: Tung, Kee M.

Atty. Docket: 1972.1540001

Information Disclosure Statement

Mail Stop Amendment

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Sir:

Listed on accompanying IDS Forms PTO/SB/08a equivalent and/or PTO/SB/08b equivalent are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

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This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

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Atty. Dkt. No. 1972.1540001

- ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
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- ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
- ☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).
- ☒ 5. Documents US1-US3 and FP1 were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided as document NPL1 in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38 and MPEP 609.04(a)(III).
- ☐ 6. A concise explanation of the relevance of the non-English language document(s) appears below in accordance with 37 C.F.R. § 1.98(a)(3).
- ☒ 7. Copies of documents FP1 and NPL1 are submitted. However, in accordance with 37 C.F.R. § 1.98(a)(2), no copies of U.S. patents and patent application

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publications cited as documents US1-US3 on the attached IDS Forms are submitted.

- ☐ 8. Copies of the _____ documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No. _____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).
- ☐ 9. It is expected that the examiner will review the prosecution and cited art in the parent application no(s). _____ in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.
- ☐ 10. In accordance with the Federal Circuit decision in *Dayco Prods., Inc. v. Total Containment, Inc.* 329 F.3d 1358 (Fed. Cir. 2003), Applicants submit herewith Office Actions from the co-pending U.S. Patent Application No. _____, filed _____, as documents _____ to _____. The identification of these Office Actions is not to be construed as a waiver of secrecy as to those applications now or upon issuance of the present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during examination.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

Atty. Dkt. No. 1972.1540001

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



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Date: October 28, 2011

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Substitute for form 1449/PTO		<i>Complete if Known</i>	
		Application Number	12/874,134
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Filing Date	September 1, 2010
		First Named Inventor	Michael MANTOR
		Art Unit	2628
		Examiner Name	Tung, Kee M.
Sheet	1	of	1
		Attorney Docket Number	1972.1540001

U.S. PATENT DOCUMENTS					
Examiner initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	US1	6,252,600 B1	06-26-2001	Kohli et al.	
	US2	2008/0109810 A1	05-08-2008	Pronovost et al.	
	US3	2009/0160867 A1	06-25-2009	Grossman	
	US4				
	US5				
	US6				
	US7				
	US8				
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	US11				
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	US18				
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FOREIGN PATENT DOCUMENTS						
Examiner initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	76
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
	FP1	EP 0 475 421 A2	03-18-1992	Hughes Aircraft Co.		
	FP2					
	FP3					
	FP4					
	FP5					
	FP6					
	FP7					
	FP8					

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Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT***(Use as many sheets as necessary)***Complete if Known**

Sheet 1 of 1

Application Number	12/874,134
Filing Date	September 1, 2010
First Named Inventor	Michael MANTOR
Art Unit	2628
Examiner Name	Tung, Kee M.
Attorney Docket Number	1972.1540001

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
	NPL1	International Search Report and Written Opinion, dated September 29, 2011, for PCT Appl. No. PCT/US2010/047786, 14 pages.	
	NPL2		
	NPL3		
	NPL4		
	NPL5		
	NPL6		
	NPL7		
	NPL8		
	NPL9		
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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.



(12) **EUROPEAN PATENT APPLICATION**

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(51) Int. Cl.5: **G06F 9/46**

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(54) **Dual hardware channels and hardware context switching in a graphics rendering processor.**

(57) An improved graphics processor (10) has rapid response to higher priority tasks. It is implemented with multiple channels of FIFO input circuits and with task interrupt and context switching capability. The graphics processor (10) servicing a first channel task is interrupted when a higher priority task is available in a second channel. Context switching facilitates interrupting of the lower priority first channel task, then saving of the context of the first channel task, then performing higher priority second channel task, then restoring the interrupted first channel task, and then continuing with the processing of the restored first channel task. It is also implemented with concurrent downloading from a host computer (14) and processing by the graphics processor (10) and implemented with general purpose graphics processing capability, including multi-level nested interrupts and nested subroutines

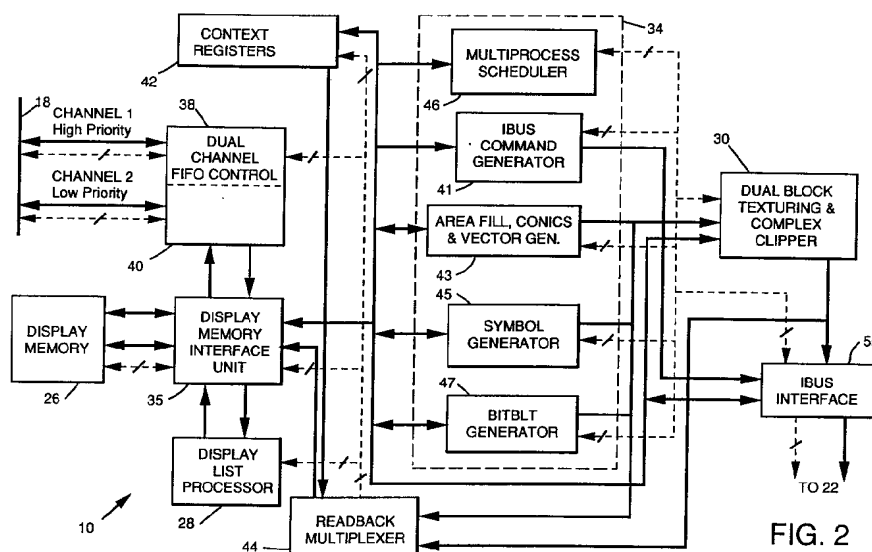


FIG. 2

EP 0 475 421 A2

CROSS REFERENCE TO RELATED APPLICATIONS

The present application is related to contemporaneously filed patent applications: Serial No. 07/582,697 filed on September 14, 1990 (European Patent Application ... Attorney's Docket 2405P299EP), entitled "Multifunction Cogenerator", Serial No. 07/582,696 filed on September 14, 1990 (European Patent Application ... Attorney's Docket 2405P302EP), entitled "Dual Programmable Block Texturing and Complex Clipping in a Graphics Processor", Serial No. 07/582,710 filed on September 14, 1990, entitled "Concurrent General Purpose and DMA Processing in a Graphics Rendering Processor", Serial No. 07/582,728 filed on September 14, 1990 (European Patent Application ... Attorney's Docket 2405P300EP), entitled "Integrated Area Fill, Conics and Vector Generator in a Graphics Processor", Serial No. 07/582,694 filed on September 14, 1990, entitled "Hardware Bit Block Transfer Processor", Serial No. 07/582,693 filed on September 14, 1990, entitled "Hardware Symbolology and Text Generator in a Graphics Processor", and Serial No. 07/582,695 filed on September 14, 1990, entitled "Multiprocess Scheduler in a Graphics Processor", all by John M. Peaslee and Jeffrey C. Malacarne, whose teachings are incorporated herein by reference.

BACKGROUND

The field of the invention is display systems and in particular graphics processors for display systems that provide multiple channels and context switching between channels.

Many types of graphics systems require fast response to operator inputs and cursor movements. Often, a fast response must occur while a graphics processor is performing a low priority task, such as generating a background map. Existing graphics processors are implemented with a single channel that cannot respond rapidly to priority tasks. Such systems have relatively poor response to higher priority tasks. This is because the graphics processor is implemented to finish the current task before invoking a next task. There is no provision for assigning priorities to tasks. This is because, even if a subsequent task is a higher priority task, the graphics processor must complete the current task before invoking the higher priority task.

SUMMARY OF THE INVENTION

A prioritized multiple channel configuration having context switching solves important graphic system problem of fast response. The present invention is an improvement in graphics processors, using multiple channels having context switching and FIFOs to provide rapid response to higher priority tasks. A graphics processor servicing a first channel task is interrupted when a higher priority task is available in a second channel. Context switching facilitates interrupting of the lower priority first channel task, then saving of the context of the first channel task, then performing higher priority second channel task, then restoring the interrupted first channel task, and then continuing with the processing of the restored first channel task.

The present invention efficiently solves the problem by providing two prioritized input channels sharing a single graphics processor. The graphics tasks requiring fast update are usually sent through the high priority channel. The graphics tasks not requiring fast update are usually sent through the low priority channel. Also, multiple host processors are readily accommodated and can each use both channels.

A preferred embodiment of the present invention comprises one or a plurality of stored program computers for generating a plurality of display lists. Each display list includes a plurality of graphic instructions. A plurality of FIFOs are coupled to the one or more stored program computers for storing the plurality of display lists. A graphics processor is coupled to the plurality of FIFOs for generating graphic pixel signals in response to the plurality of display lists stored by the plurality of FIFOs. A bit map memory is coupled to the graphics processor for storing the graphic pixel signals. A display monitor is coupled to the bit map memory for generating a display in response to the graphic pixel signals stored by the bit map memory. The plurality of FIFOs may each store a different display list.

The graphics processor the present invention includes a context switching circuit for switching context between different display lists stored by different ones of the plurality of FIFOs and for generating the graphic pixel signals in response to the different display lists. It also includes an interrupt input circuit for generating an interrupt signal and an interrupt execution circuit coupled to the interrupt input circuit and to the plurality of FIFOs for interrupting the generation of graphic pixel signals in response to the interrupt signal and in response to a first display list stored by the plurality of FIFOs.

The interrupt input circuit generates graphic pixel signals in response to the interrupt signal and in response to a second display list stored by the plurality of FIFOs. It includes a restore control circuit coupled to the interrupt execution circuit for generating a restore signal in response to the second display list stored by the plurality of FIFOs and includes a restore execution circuit coupled to the restore control

circuit and to the interrupt execution circuit for restoring the context of the first display list in response to the restore signal. It also includes a concurrent processing circuit coupled to the plurality of FIFOs for processing at least one of the plurality of display lists concurrently with the generating of the display list generated by the stored program computer. It also includes a nested subroutine circuit for controlling the generating of the graphic pixel signals under nested subroutine control.

In addition, a method of providing context switching in a display system comprising a FIFO and a graphics processor is disclosed. The method comprises the following steps. Transferring a first display list to the FIFO. Initiating processing of the first display list by the graphics processor. Transferring a second display list to the FIFO. Interrupting processing of the first display list by the graphics processor and storing a context of the first display list. Initiating processing of the second display list by the graphics processor. Detecting completion of processing of the second display list by the graphics processor. Restoring the context of the first display list. Continuing processing of the first display list by the graphics processor.

Accordingly, a feature of the present invention is to provide an improved display system and method. Another feature of the present invention is to provide an improved graphics processor. Another feature of the present invention is to provide a general purpose graphics processor. Another feature of the present invention is to provide multi-level nested interrupt capability for a graphics processor. Another feature of the present invention is to provide a nested subroutine capability for a graphics processor. Another feature of the present invention is to improve response time of a graphics processor. Another feature of the present invention is to reduce latency time of a graphics processor. Another feature of the present invention is to provide concurrent downloading and graphics processing. Another feature of the present invention is to provide DMA downloading of display lists. Another feature of the present invention is to provide a multiple channel graphics processor. Another feature of the present invention is to provide a multiple channel FIFO input for a graphics processor. Another feature of the present invention is a context switching interrupt structure to facilitate higher priority processing.

BRIEF DESCRIPTION OF THE DRAWINGS

The various features and advantages of the present invention will become apparent from the following detailed description taken in conjunction with the accompanying drawings, wherein like references numerals designate like structural elements, and in which:

Fig. 1 is a block diagram representation of a graphics processor system that employs dual hardware channels and hardware context switching in accordance with the principles of the present invention;

Fig. 2 is a detailed block diagram of the graphics processor of Fig. 1;

Fig. 3 is a block diagram representation of the interface between the graphics processor and a bus that illustrates aspects of the present invention;

Fig. 4 is a detailed block diagram of the context register shown in Fig. 2;

Fig. 5 is a detailed block diagram of the dual channel FIFO controller of Figs. 2 and 3;

Fig. 6 is a memory map representation of a FIFO; and

Fig. 7 is a memory map representation of an attribute stack.

DETAILED DESCRIPTION

Referring to the drawings, FIG. 1 is a block diagram of a generalized graphic display system including a dual channel multifunction cogenerator 10 of which the present invention forms a part. FIG. 2 shows a block diagram of the cogenerator 10 of which a dual channel FIFO controller 38, 40 and context registers 42 of the present invention forms a functionally distinct part. The cogenerator 10 is a dual channel, hardware based device which operates in conjunction with one or more general purpose data processing systems, such as a military command and control system, wherein the simplified system is shown in FIG. 1. Briefly, the system comprises one or more real time data processors 14 and other real time data accumulating devices such as a radar system 16 and other cogenerators 17. The host processor 14 and the radar scan converter 16, for example, feed data into the cogenerator 10 via a multifunction bus 18 where it is combined with graphics data generated by the cogenerator 10. The cogenerator 10 outputs a complete set of data for generation of a graphics display via a 64-bit bidirectional interconnect image bus 20 into a bit map memory 22 and then by way of a video bus 23 to a display system 24. The cogenerator 10 may include various other input devices such as manual input output devices, multiple real time processors, bulk memory devices and the like.

A detailed description of the cogenerator 10 is given in copending commonly assigned United States patent application Serial No. 07/582,697 entitled, "Multifunction Cogenerator," the teachings of which are

incorporated herein by reference. In overview, however, the cogenerator 10 is a high performance single chip graphics rendering processor. It generates multiple graphics primitives and performs general purpose processing functions. The cogenerator accepts graphic commands over a thirty-two bit bidirectional host input port from a processor such as the host processor 14 of FIG. 1. The cogenerator 10 processes these commands and then draws into the bit mapped memory 22. The cogenerator 10 "draws" into the bit mapped memory 22 over the image bus 20. "Drawing" is performed by entering binary one and zero signals (drawing ones and drawing zeros herein) into individual memory locations of the bit mapped memory 22. Typically, the bit mapped memory 22 has multiple memory layers with the layers corresponding to color and intensity of graphic display pixels. The image bus 20 is a 64 bit bidirectional multi-user bus. The cogenerator 10 can draw graphic primitives such as symbols, polylines, rectangles, circles, ellipses, arcs, polygon fills, and perform bit block transfers (BITBLT) between the cogenerator 10, the host processor 14, and the bit mapped memory 22.

Directly associated with the cogenerator 10 is a tri-ported display memory 26. The display memory 26 stores all commands and parameters and includes appropriate logic required for the cogenerator 10 to function properly. The memory address space in a working embodiment is 4 megabytes by 32 bits. The cogenerator 10 interfaces with either DRAMS, SRAMS, and/or PROMS. The display memory 26 is accessible by the cogenerator 10 display list processor 28, the cogenerator 10 internal graphics generator 30, and the host processor 14. Stored in the display memory 26 are two first in, first out (FIFO) memory buffers one of the buffers being assigned a higher operational priority than the other and there being one buffer memory for each of two drawing channels. An address stack is provided for each FIFO buffer to store subroutines calls. An attribute stack stores all internal cogenerator attributes for hardware context switching, a sin/cosine table for drawing graphics, and up to 128 font tables to draw stroked and/or dot matrix symbols and characters. A large display list region is also provided.

The display memory 26 is comprised of up to four million words of RAM organized as 32 bit data words and appropriate buffer logic. The contents of the display memory 26 may be organized as shown in Table I below. The host processor 14 has the ability to perform random reads and writes at any address within the display memory 26 address space. The cogenerator 10 monitors the input of data from the host processor 14 to the display memory 26 to synchronize updating of data from the host processor 14 with the output of graphics signals therefrom.

A dual channel FIFO buffer controller 38, 40 interfaces the cogenerator 10 to the host processor 14. The FIFO buffer controller 38, 40 are responsible for performing all interfacing duties such as proper "hand shaking" when the bus 18 is performing data transfers. The host processor 14 is able to both read and write to the cogenerator 10 and the display memory 26. When the host processor 14 reads or writes to the display memory 26, the FIFO buffer controller 38, 40 actually perform the read or write operations to the display memory 26 for the host processor 14. An address stack is provided internally within each FIFO buffer controller 38, 40 to store subroutine calls, an attributes stack to store all internal attributes required by the cogenerator 10 to perform hardware context switching, a sine/cosine table of drawing conics and primitives, up to 128 font tables to draw both stroked and dot matrix symbols and characters and a large display list region. The FIFO buffer controller 38, 40 is also responsible for arbitrating high and low priority channels to the cogenerator 10.

A display memory interface unit 35 performs the actual display memory 26 memory cycles. It is essentially a tri-port memory controller. The display memory 26 is used by both the host processor 14, and the cogenerator 10.

A display list processor 28 performs all of the cogenerator 10 command and display list processing. Commands are sent to the cogenerator 10 from the host processor 14. The display list processor 28 handles the various ways that commands can be sent to the cogenerator 10. The display list processor 28 interfaces to the display memory 26 using the display memory interface unit 35, reads commands from the FIFO buffers as well as performs other functions. When a command is given to the display list processor 28, the display list processor 28 processes the command and determines what action to take. The cogenerator 10 provides many different commands and sequences. A more detailed description of tile display list processor is given in copending commonly assigned United States patent application Serial No. 07/582,710 entitled "Concurrent General Purpose and DMA Processing in a Graphics Rendering Processor," the teachings of which are incorporated herein by reference.

Context registers 42 store all of the cogenerator attributes. These attributes define the current state of the cogenerator 10. The current state may include a large number of parameters such as: cogenerator operational mode; draw pointer position; foreground color; background color; clipping window dimensions; etc. The contents of the cogenerator 10 are important as they define the personality of the cogenerator 10 at any given time and all attributes are user programmable. This gives a user considerable flexibility in

operating the display system.

Also provided is a readback multiplexer 44 which is a large data multiplexer. It is used to multiplex data to the display memory interface unit 35 which is directed to either the display memory 26 or back to the host processor 14 via bus 18. Three sources of readback data are the context registers 42, a graphics generator 34 defined within the dashed block in FIG. 2, and the block texturing and complex clipping processor 30. If the data is intended for the host processor 14 it will be sent through the FIFO buffer controller 38, 40 by the display memory interface unit 35. The graphics generator 34 is connected to the readback multiplexer 44 for various cogenerator 10 drawing operations. The block texturing and complex clipping processor 30 also sends data to the readback multiplexer 44 for various cogenerator 10 operations.

The graphics generator 34 generates all of the cogenerator 10 primitives and symbols and performs bit block transfers (BITBLTs). The graphics generator 34 includes a multiprocess scheduler 46, a command generator 41, an area fill conic and vector generator 43, a symbol generator 45, and a BITBLT address generator 47. The area fill, conics and vector generator 43 creates digital signals representing graphics primitives such as polylines, rectangles, circles, ellipses and polygons and area fills. These primitive signals are next combined with other digital signals representing alphanumeric and other symbols, which are generated in a symbol generator 45, and with yet a third set of signals generated by block texturing and complex clipping processor 30 to produce the final set of signals which is then transferred by the BITBLT address generator 47 into specified pixel addresses in the bit mapped memory 22. Typically, the hit mapped memory 22 has multiple memory layers which set the color and intensity for the graphics display defined for each pixel location therein.

The multiprocess scheduler 46 controls data transfers between elements of the cogenerator 10. The multiprocess scheduler 46 uses a branched scheduler approach to control the several operations and apply certain characteristics of a software operating system thereto. This promotes functional independence between various cogenerator 10 sequences and provides a mechanism for inter-unit communication.

The area fill, conic and vector generator 43 calculates mathematical solutions for drawing geometric primitives. The symbol generator 45 generates alpha numeric symbols. The BITBLT address generator 47 provides a general purpose mechanism for moving rectangular blocks of image data in the bit map memory 22 and the display memory 26.

Detailed descriptions of the above-described devices are given in copending commonly assigned United States patent applications Serial No. 07/582,728 entitled "Integrated Area Fill, Conics and Vector Generator in a Graphics Processor", Serial No. 07/582,694 entitled "Hardware Bit Block Transfer Processor", Serial No. 07/582,693 entitled "Hardware Symbolology and Text Generator in a Graphics Processor", and Serial No. 07/582,695 entitled "Multiprocess Scheduler in a Graphics Processor," the teachings of which are incorporated herein by reference.

Referring now to Fig. 3, a dual channel FIFO controller 38, 40 couples the display memory interface unit 35 in the graphics cogenerator 10 with the host processor 14 through the multifunction bus 18. A pair of conventional multifunction bus interface circuits 60, 61 couple the graphics processor 10 to the multifunction bus 18. The bus interface circuits 60, 61 are coupled to the display memory interface unit 35 and to dual FIFO control circuits 62, 63. The dual FIFO control circuits 62, 63 are coupled to the display memory interface unit 35.

The dual channel FIFO controller 38, 40 communicates data (instructions and attributes) between the display memory interface unit 35 and the host computer 14. It receives output data from the display memory interface unit 35 on an output data line 315 and communicates this output data through the bus interface circuits 60, 61 to the host processor 14 on the multifunction bus 18. It also receives input data from the host processor 14 on the multifunction bus 18 through the bus interface circuits 60, 61 and communicates this input data to the dual FIFO control circuits 312, 313 on the input data lines 66, 67. The dual FIFO control circuits 62, 63 implement a conventional FIFO algorithm to load data into the FIFOs.

Referring to Fig. 4, a more detailed block diagram of the context registers 42 is shown. The context registers 42 are comprised of 21 attribute registers 51-1 to 51-21, and attribute register load controller 52 and an attribute multiplexer 53. The context registers 42 are coupled to the display memory interface unit 35, to the display list processor 28, and the readback multiplexer 44 as indicated in Fig. 4.

To start a context switch, the cogenerator 10 processes a "PUSH attributes" command. The display list processor 28 reads in a command from the display memory 26. A PUSH command is placed into either the FIFO buffers or a display list. A command decoder (not shown) detects a PUSH command and informs a display list command interpreter (not shown) that selects the attribute data bus input to the readback multiplexer 44. This bus runs from the context registers 42 to the readback multiplexer 44 as shown in Fig. 2. The output of the readback multiplexer 44 is sent to the display memory interface unit 35. The display list processor 28 selects the attribute bus for input to the display memory interface unit 35 so all the

cogenerator attributes are sequentially loaded into the attribute stack located in the display memory 26. The attribute stack is a 1K block of memory broken up into 32 tables each having 32 entries. Each table holds one cogenerator context, or state, typically with some unused entries.

Once the attribute bus is selected for input to the display memory interface unit 35, the command interpreter in the display list processor 28 sends the attribute select code to the context registers 42. The interpreter cycles through 21 codes to extract all 21 attribute register values out of the context registers 42. This happens sequentially to perform the PUSH operation. The attribute select code connects to the attribute multiplexer 53 in the context registers 42. The first code sent selects attribute register 1 for output. The attribute multiplexer 53 drives the data to the readback multiplexer 44. The first attribute value is at the input to the display memory interface unit 35. The command interpreter in the display list processor 28 controls the attribute stack address generator (not shown).

Fig. 5 shows a block diagram of the FIFO controller 38, 40. The dual channel FIFO controller 38, 40 receives a command from the host processor 14. A channel 2 interface transceiver 70 accepts the data, address and provides proper handshaking with the host processor 14 to complete the bus transfer. The channel 2 interface transceiver 70 then activates a channel 2 request. A priority controller 71 monitors both channel 1 request and channel 2 request activity. In this case channel 1 is idle and channel 2 has received a command for FIFO2. The function of the channel 2 interface transceiver 70 is to set priority and determine what kind of memory cycle to perform. When the channel 2 interface transceiver 70 determines the cycle type, it tells the display memory cycle requestor 72 to perform the cycle. The priority controller 71 receives a channel 2 request and loads the input data register 73 with the data sent from the host processor 14. The input data register 73 sends its contents to the display memory cycle requestor 72. An address decoder 74 decodes the current host processor address. The priority controller 71 uses this information to determine what the host processor 14 is attempting to do. In this case a write to FIFO2 is occurring. The priority controller 71 selects the FIFO2 write pointer from a FIFO controller 75. The priority controller 71 controls an address multiplexer 76 and selects the FIFO2 write pointer. The address multiplexer 76 sends the FIFO2 write pointer value to the display memory cycle requestor 72. Now the priority requestor 71 commands the display memory cycle requestor 72 to perform a write cycle to FIFO2. The display memory cycle requestor 72 has the proper address and data. It now issues a cycle request to the display memory interface unit 35. A channel 1 transceiver 65 and output data register 69 are employed.

A memory map of the display memory 26 is shown in Table 1. The display memory 26 is implemented with RAM chips having 4 million (4M) 32 bit words. The display memory 26 is accessed with various address registers, FIFO pointers, and stack pointers multiplexed together to form a multi-ported memory. Addresses having 22 bits is sufficient for addressing the 4M word display memory 26. Because many of the addressing circuits have a limited address space, a hardwired block address limiting the programmable bits provides circuit efficiencies. For example, the FIFO 1 pointers addressing words 1024 to 2047 are implemented with a 10 bit programmable address, hardwiring the 11 MSBs (bits 10 to 21) to a zero state and hardwiring the next less significant MSB (bit 9) to a one state. The 32 bit output of the display memory 26 is fanned out to all of the destinations.

In Table I, the memory map of the display memory 26 shows the locations and capacities of the stored information. The term K, as in 1K, means thousands of words of memory and the term M, as in 4M, means millions of words of memory. Memory addresses and memory capacities more than 1K words are often shown herein as being rounded off for convenience of discussion. However, in a preferred embodiment, the rounded off numbers are implemented with binary numbers. For example, 1K implies 1024 and 4K implies 4096.

An unused set of 8 words located at the bottom of the display memory 26 (words 0 to 7) are reserved for future use. An interrupt table having 247 words (words 8 to 255) is located above the unused 8 words at the bottom of the display memory 26 and is used to store interrupt vectors. A pair of subroutine stacks, subroutine stacks 1 and 2, having 256 words (words 256 to 511) and 512 words (words 512 to 1K), respectively, are located above the interrupt table near the bottom of the stack are used to store the return addresses from subroutine calls. Subroutine stack 1 stores return addresses for subroutine calls from channel 1 and subroutine stack 2 stores return addresses for subroutine call from channel 2. A pair of FIFOs, the higher priority FIFO (FIFO 1) and the lower priority FIFO (FIFO 2) having 1K words (words 1K to 2K) and 4K words (words 2K to 6K), respectively, are located above the subroutine stacks. These FIFOs are used to store the input display lists and individual command packets from the host processor 14. An attribute stack having 1K words (words 6K to 7K) is located above the FIFOs and is used to store attributes for context switching. A sine/cosine table having 1K words (words 7K to 8K) is located above the attribute stack and is used for conics rendering. Font tables, 128 tables each having 4K words totaling 512K words (words 8K to 520K), is located above the sine/cosine tables and is used for symbols and text rendering. A

display list memory having 3.5M words (words 520K to 4M) is located above the font tables at the top of the display memory 26.

5	TABLE I		TABLE II	
	MEMORY ADDRESS	DATA TYPE	COGEN DRAW DRAW POINTER	
10	4M	} DISPLAY LIST	XY ADDRESS OFFSET VALUE	
	520K		FOREGROUND COLOR	
15		} FONT TABLE	BACKGROUND COLOR	
	8K		COLOR MASK	
		} SINE/COSINE TABLE	BMM ADDRESS	
20	7K		CLIPPING WINDOW 1	
		} ATTRIBUTE STACK	CLIPPING WINDOW 2	
	6K		CLIPPING WINDOW 3	
25		} FIFO 2	SYMBOL ATTRIBUTES 1	
	2K		SYMBOL ATTRIBUTES 2	
		} FIFO 1	LINE TEXTURE 1	
30	1K		LINE TEXTURE 2	
		} SUBROUTINE STACK 2	DEFINE TEXTURE 1	
	512		DEFINE TEXTURE 2	
35		} SUBROUTINE STACK 1	DEFINE BITBLT SOURCE BLOCK	
	256		ADDR XY SYMBOL STRING POSITION	
		} INTERRUPT TABLE	DDA TEXTURE & POLYLINE STATE	
40	8		DM_POINTER 1	
		} UNUSED	DM_POINTER 2	
	0			

Referring now to Fig. 6, a FIFO memory map is implemented in the display memory 26 in accordance with Table I. Each FIFO is implemented with a read counter storing a read pointer and a write counter storing a write pointer, contained in the FIFO control circuits 312, 313. The FIFO memory is implemented in the display memory 26 at addresses 1K to 6K. It is implemented in a conventional manner, where the next word to be read is addressed by the read pointer and the next word to be written is addressed by the write pointer. When a word is written, the write pointer is incremented to the next memory write address. When a word is read, the read pointer is incremented to the next memory read address. When the read address or write address gets to the last memory address at the top of the FIFO, memory address 6143 for FIFO 2 and memory address 2047 for FIFO 1, the pointer wraps around to the bottom of the FIFO. memory address 2048 for FIFO 2 and memory address 1024 for FIFO 1.

Because of the wrap around of the pointers, either one of the pointers can catch up with the other pointer. Additional logic is implemented in the FIFO control circuits 312, 313 to interlock FIFO operation in a conventional manner. First, circuitry is provided to insure that the read pointer does not pass the write pointer during a FIFO empty condition. When the read pointer catches up with and equals the write pointer address, processing from this FIFO is disabled until the write pointer is advanced past the read pointer. Second, circuitry is provided to insure that the write pointer does not pass the read pointer during a FIFO

full condition. When the write pointer catches up with and equals the read pointer address, loading into this FIFO from the host processor 14 is disabled until the read pointer is advanced past the write pointer. This is implemented by disabling the acknowledge signal on the multifunction bus 18 back to the host computer 14 when the FIFO is full.

Referring now to Fig. 7, an attribute stack is implemented in the display memory 26 in accordance with Table I. The graphics processor 10 is implemented with a comprehensive set of internal attributes. These attributes combine to define the current state of the graphics cogenerator 10. The state of the graphics cogenerator 10 defines the personality of operation. The attribute stack, implemented as a push down stack, allows a programmer to store up to 32 different states each having 21 attributes. The attribute stack pointers and attribute stack control circuitry are implemented to be self contained within the graphics cogenerator 10.

The attribute stack is implemented as a 1K block of memory partitioned into 32 tables, each table having 32 words. Because the system is implemented with 21 attribute registers, each attribute table in the stack call accommodate one full graphic context of 21 attributes and 11 spare words. It is implemented with a counter storing a stack pointer that is incremented through 21 addresses to push a table of attributes into the attribute stack and is decremented 21 addresses to pop a table of attributes out of the attribute stack. The context circuitry is contained in the context register unit. It is implemented in a conventional manner, such as with the interrupt stack in the Motorola 68HC11. Many different attribute sets may be configured. One set of 21 attributes is listed in Table II.

The attributes stored in these registers are pushed into the attribute stack in the display memory 26 in response to an interrupt and are popped out of the attribute stack in the display memory 26 in response to completion of interrupt processing. A RETURN instruction is placed at the end of the interrupting task instruction set to restore the context of the interrupted task for continued processing of the interrupted task. Interrupt implementation is discussed in greater detail in the related patent application entitled "General Purpose and DMA Processing in a Graphics Rendering Processor."

An interrupt vectors the processor operation to a display list in the display list region of the display memory 26. For example, a lower priority display list being processed out of the lower priority FIFO 2 or out of the display list region of display memory 26 may be interrupted by a software interrupt in the higher priority FIFO 1 to process a display list in the display list region. Interrupts are processed when the graphics cogenerator 10 is processing information from the FIFO or from the display list region. An interrupt vectors the processor operation to the display list region. This processing may be implemented to be concurrent with the loading of this display list using the DMA concurrent processing feature discussed in the related patent application entitled "Concurrent General Purpose and DMA processing in a Graphics Rendering Processor." An interrupt automatically stores the return address in an interrupt stack implemented in the display memory interface unit 35.

The context switching capability allows multiple display list routines to be nested. It also allows multiple host processors 14 to download different display list routines to the graphics processor 10 for processing, where each display list routine can have a different context. The display list routines are interrupted with multi-level nested interrupt capability. This permits a second routine to interrupt a first routine that is being processed, a third routine to interrupt the second interrupting routine that is being processed, a forth routine to interrupt the third interrupting routine that is being processed, and so forth. The attributes of each interrupted routine are pushed into the attribute stack to make the attribute registers available for the attributes of the interrupting routine. As interrupting routines are completed, a concluding RETURN instruction in the routine pops the attributes of the last interrupted routine from the attribute stack and execution of the instructions of this last interrupted routine is commenced. This is known as context switching. The attribute stack is 32 levels deep. This allows 32 nested display list subroutines to be used. A push operation sequentially stores all of the attributes stored by the context registers into the attribute stack at the current attribute stack pointer position. The programmer can then overwrite any or all of the internal attributes in the attribute registers. Effectively, this is a nondestructive overwrite operation because the overwritten attributes may be restored with a pop operation from the attribute stack. The pop operation sequentially restores a complete set of 21 attributes from the current attribute stack read pointer location. The subroutine stack facilitates subroutine nesting without context change, implementing up to 256 levels of nesting for channel 1 and up to 512 levels of nesting for channel 2.

The general purpose graphics processing capability, including multi-level nested interrupts and nested subroutines, and the concurrent processing capability are discussed in detail in the related patent application entitled, "Concurrent General Purpose and DMA Processing in a Graphics Rendering Processor."

The nested subroutine feature may be used both, within the same channel and across channels. For

example, three display list routines A, B and C will be discussed. Initially, the system is executing display list routine-A on channel 2. Then display list routine-B is sent to channel 1. The graphics cogenerator 10 then context switches to channel 1 to process display list routine-B. The current state of the graphics cogenerator 10 for routine-A is pushed onto the attribute stack. Execution of routine-B is then initiated. Routine-B has new attributes which overwrite the routine-A attributes in the context registers. While processing routine-B, routine-C interrupts routine-B on channel 1. The graphics cogenerator 10 then stays on channel 1 to process display list routine-C. This is because channel 2 has a lower priority than channel 1 and hence channel 2 is inhibited from interrupting channel 1 processing. The current state of the graphics cogenerator 10 for routine-B is also pushed onto the attribute stack. Execution of routine-C is then initiated. Routine-C has new attributes which overwrite the routine-B attributes in the context registers. When execution of routine-C is completed, then the graphic processor 10 context switches back to routine-B on channel 1. The attributes of routine-B are popped off of the top of the attribute stack into the context registers. The routine-B attributes overwrite the routine-C attributes in the context registers. The graphics cogenerator 10 then starts processing routine-B from the point where it was interrupted. When execution of routine-B is completed, then the graphics cogenerator 10 context switches back to channel 2, pops the routine-A attributes off of the attribute stack, overwriting the routine-B attributes in the context registers. The graphics cogenerator 10 then starts processing routine-A from the point where it was interrupted. This example shows a simple scenario of context switching and nested interrupts and subroutines.

Many alternative embodiments may be implemented from the teachings herein. For example, the FIFOs may be implemented with dedicated memory in place of the shared display memory 26. Also, the stack may be implemented with dedicated memory in place of the shared display memory 26. Also, multiple channels exceeding two channels, such as three channels or six channels, can readily be implemented. Also, various portions of the system may be implemented with a micro processor, such as a Motorola 68040 or an AMD 29000, programmed to implement the system operations. Also, a dedicated data path and a dedicated host processor 14 may be implemented in place of the multifunction bus 18 and a general purpose host processor 14. Also, the graphics system may be implemented for example by a stored program processor or by a special purpose hardwired processor. Stored program processors may be implemented for example by microprocessors, by array processors, or by RISC processors.

Thus there has been described a new and improved graphic display system and method. It is to be understood that the above-described embodiments are illustrative of some of the many specific embodiments that represent applications of the principles of the present invention. Clearly, numerous and varied other arrangements may be designed by those skilled in the art without departing from the scope of the invention.

Claims

1. A display system characterized by:

- a stored program computer (14) for generating a plurality of display lists, each display list including a plurality of graphic instructions;
- a plurality of FIFOs (26, FIFO1, FIFO2) coupled to the stored program computer (14) for storing the plurality of display lists; and
- a graphics processor (10) coupled to the plurality of FIFOs (26, FIFO1, FIFO2) for generating graphic pixel signals in response to the plurality of display lists stored by the plurality of FIFOs (26, FIFO1, FIFO2).

2. The system of claim 1, characterized by the plurality of FIFOs (26, FIFO1, FIFO2) each storing a different display list and wherein the graphics processor (10) includes a context switching circuit for switching context between different display lists stored by different ones of the plurality of FIFOs (26, FIFO1, FIFO2) and generating the graphic pixel signals in response to the different display lists.

3. The system of claim 1 or 2, characterized in that the plurality of FIFOs (26, FIFO1, FIFO2) each store a different display list and that the graphics processor (10) comprises:

- an interrupt input circuit for generating an interrupt signal; and
- an interrupt execution circuit coupled to the interrupt input circuit and to the plurality of FIFOs (26, FIFO1, FIFO2) for interrupting the generating of graphic pixel signals in response to the interrupt signal and in response to a first display list stored by the plurality of FIFOs (26, FIFO1, FIFO2) and for generating graphic pixel signals in response to the interrupt signal and in response to a second display list stored by the plurality of FIFOs (26, FIFO1, FIFO2).

4. The system of claim 3, characterized by a context memory coupled to the interrupt input circuit for storing the context of the first display list in response to the interrupt signal.
5. The system of claim 3 or 4, characterized by a push down stack coupled to the interrupt input circuit for storing the context of the first display list in response to the interrupt signal.
6. The system of any of claims 3 - 5, characterized by:
 - a restore control circuit coupled to the interrupt execution circuit for generating a restore signal in response to the second display list stored by the plurality of FIFOs (26, FIFO1, FIFO2); and
 - a restore execution circuit coupled to the restore control circuit and to the interrupt execution circuit for restoring the context of the first display list in response to the restore signal.
7. The system of any of claims 1 - 6, characterized in that the stored program computer (14) is provided with a plurality of stored program computers each for generating at least one of the plurality of display lists and wherein the plurality of FIFOs (26, FIFO1, FIFO2) are coupled to the plurality of stored program computers (14) for storing the plurality of display lists from the plurality of stored program computers (14).
8. The system of any of claims 1 - 7, characterized in that the graphics processor (10) is provided with a concurrent processing circuit (17) coupled to the plurality of FIFOs (26, FIFO1, FIFO2) for processing at least one of the plurality of display lists concurrent with the generating of the display list being generated by the stored program computer (14).
9. The system of any of claims 1 - 8, characterized in that the graphics processor (10) is provided with a multi-level nested interrupt circuit for controlling the generating of the graphic pixel signals under multilevel nested interrupt control.
10. The system of any of claims 1 - 9, characterized in that the graphics processor (10) is provided with a nested subroutine circuit controlling the generating of the graphic pixel signals under nested subroutine control.
11. The system of any of claims 1 - 10, characterized by:
 - a bit map memory (22) coupled to the graphics processor (16) for storing the graphic pixel signals; and
 - a display monitor (24) coupled to the bit map memory (22) for generating a display in response to the graphic pixel signals stored by the bit map memory (22).
12. The system of any of claims 1 - 11, characterized by:
 - a first and a second hardware channel comprising high and low priority processing channels;
 - a dual channel FIFO controller (38, 40) coupled to the first and second hardware channels that interface with a plurality of host computers (14);
 - said controller (38, 40) comprising means for allowing the plurality of host computers (14) to utilize the first and the second hardware channels by providing hardware context switching such that a first host computer (14) interrupts the second host computer (14) operating on the first channel by saving the second host computer's current context on an attribute stack, and upon the first host computer (14) completing an operation, the context of the first host computer (14) is restored and the second host computer (14) resumes processing.
13. A display system, characterized by:
 - a stored program computer (14) for generating display lists;
 - a display memory (26) coupled to the stored program computer (14) for storing the display lists;
 - a graphics processor (10) coupled to the display memory (26) for generating pixel signals in response to the display lists;
 - a context switching arrangement that interfaces between the stored program computer (14) and the graphics processor (10), said context switching arrangement having:
 - first and second hardware channels comprising high and low priority processing channels;
 - a dual channel FIFO controller (38, 40) coupled to the first and second hardware channels for interfacing between the stored program computer (14) and the display memory (26) and

selectively loading the display lists into first and second FIFO buffers in the display memory (26);

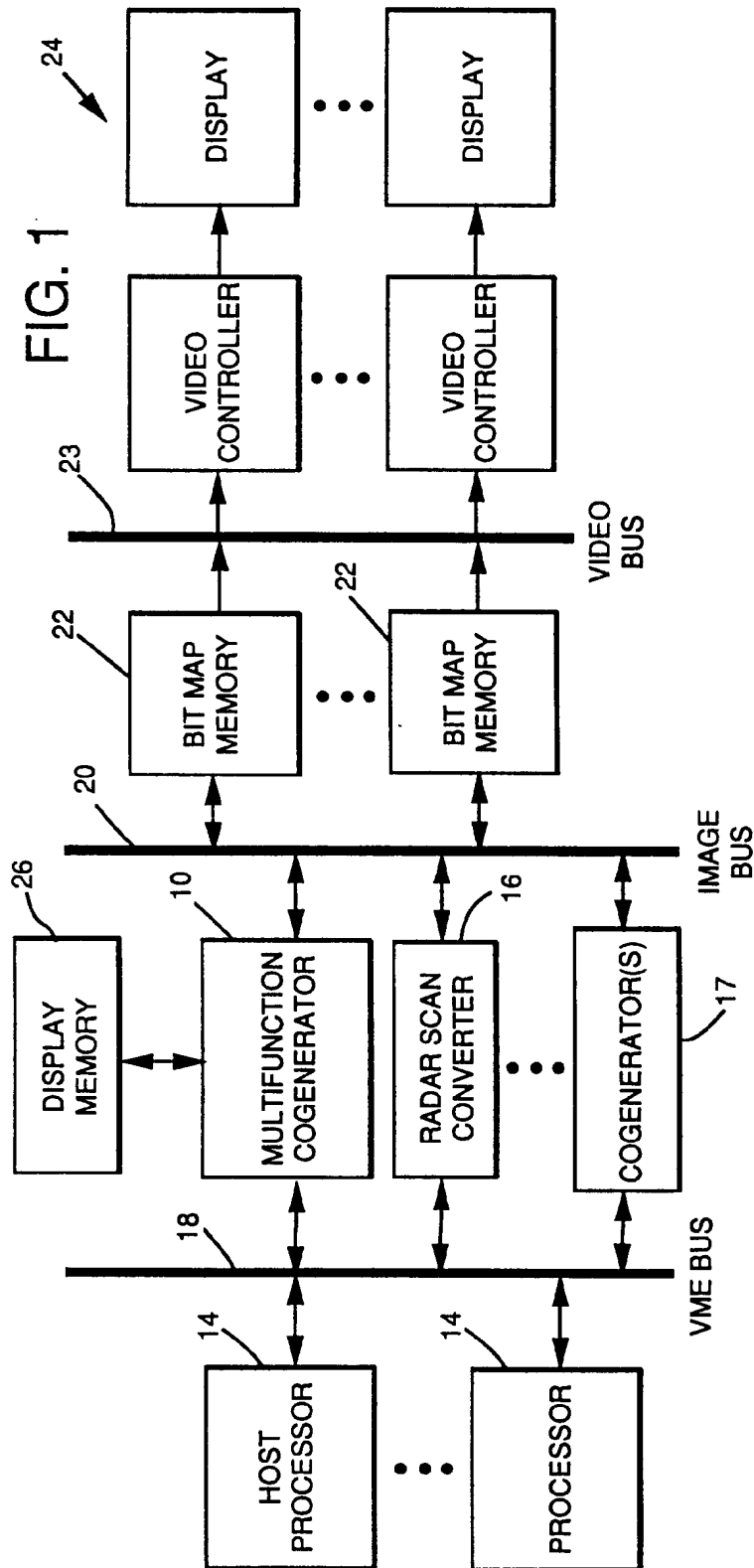
- an interrupt circuit coupled to the graphics processor (10) and the display memory (26) for interrupting the processing of a low priority display list and initiating the processing of a higher priority display list; and
- a plurality of context registers (42) for storing context attributes associated with each of the display lists and a readback multiplexer (44) for restoring the attributes of the low priority display list once the higher priority display list has been processed.

- 10 **14.** The system of claim 13, characterized in that the dual channel FIFO controller (38, 40) comprises:
- first and second hardware channels comprising high and low priority processing channels;
 - a dual channel FIFO controller (38, 40) coupled to the first and second hardware channels that interface with a plurality of host computers (14);
 - a dual channel interrupt controller that processes first and second interrupt signals; and
 - 15 - a programmable priority structure that defines task priority as either Int1 (high) Int2, FIFO1, FIFO2 (low) or Int1 (high), FIFO1, Int2, FIFO2 (low).

- 15.** The system of claim 13 or 14, characterized in that said interrupt circuit is provided with means for allowing the plurality of stored program computers (14) to utilize the first and the second hardware channels by providing hardware context switching such that a first computer (14) interrupts the second computer (14) operating on the first channel by saving the second computer's current context on an attribute stack, and upon the first computer (14) completing an operation, the context of the first computer (14) is restored whereupon the second computer (14) resumes processing.

- 25 **16.** A method of operating a display system comprising a FIFO (26, FIFO1, FIFO2) and a graphics processor (10), characterized by the steps of:
- transferring a first display list to the FIFO (26, FIFO1, FIFO2);
 - initiating processing of the first display list by the graphics processor (10);
 - transferring a second display list to the FIFO (26, FIFO1, FIFO2);
 - 30 - interrupting processing of the first display list by the graphics processor (10) and storing a context of the first display list;
 - initiating processing of the second display list by the graphics processor (10);
 - detecting completion of processing of the second display list by the graphics processor (10);
 - restoring the context of the first display list; and
 - 35 - continuing processing of the first display list by the graphics processor (10).

- 17.** A method of operating a display system comprising a stored program computer (14) for generating display lists, each display list including a plurality of instructions, a plurality of FIFOs (26, FIFO1, FIFO2) coupled to the stored program computer (14) for storing the display lists, a graphics processor (10) coupled to the plurality of FIFOs (26, FIFO1, FIFO2) for generating pixel signals in response to a display list, an interrupt circuit coupled to the graphics processor (10) for interrupting operation thereof, and a context memory coupled to the graphics processor (10) and to the interrupt circuit for storing a context in response to interruption of operation, characterized by the steps of:
- transferring a first display list from the stored program computer (14) to a first one of the plurality of the FIFOs (26, FIFO1, FIFO2);
 - 45 - initiating processing of the first display list by the graphics processor (10);
 - transferring a second display list from the stored program computer (14) to a second one of the plurality of the FIFOs (26, FIFO1, FIFO2);
 - interrupting processing of the first display list by the graphics processor (10) and storing a context of the first display list in the context memory;
 - 50 - initiating processing of the second display list by the graphics processor (10);
 - detecting completion of processing of the second display list by the graphics processor (10);
 - restoring the context of the first display list stored by the context memory; and
 - continuing processing of the first display list by the graphics processor (10).



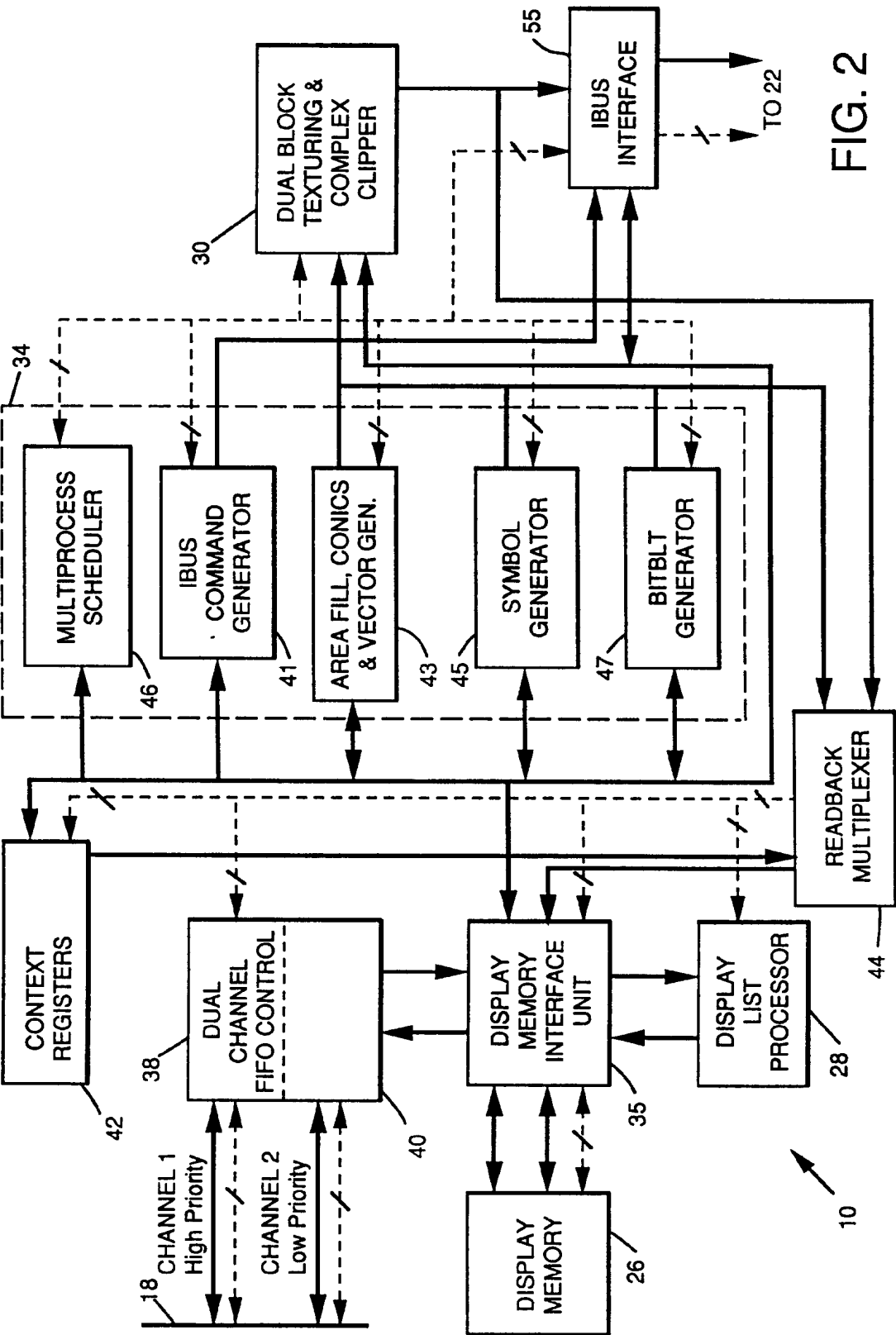


FIG. 2

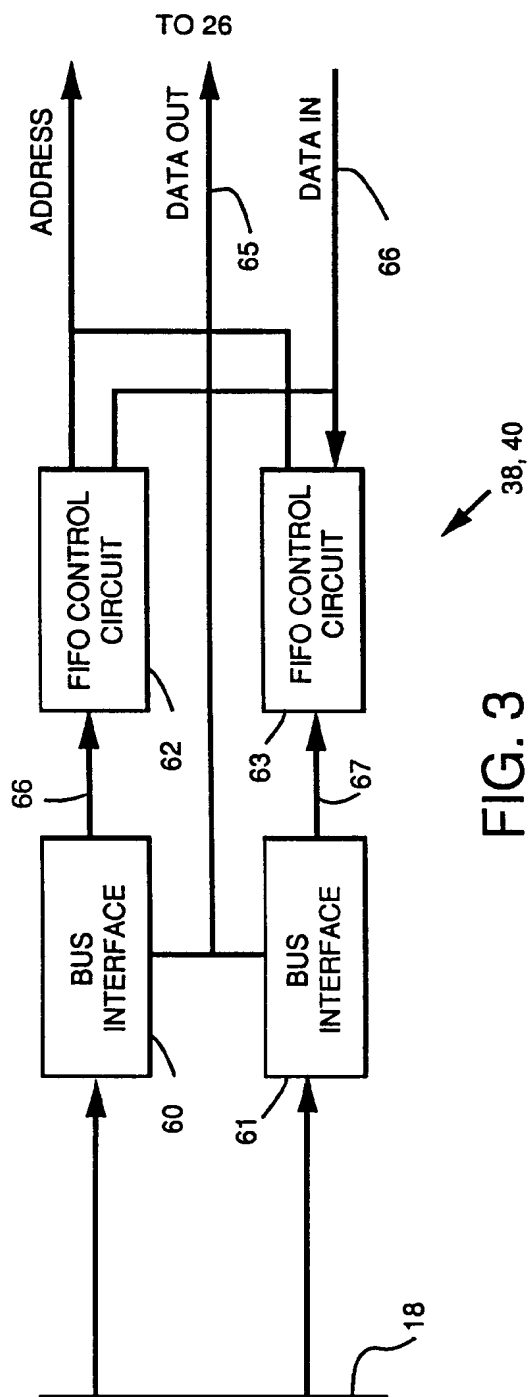


FIG. 3

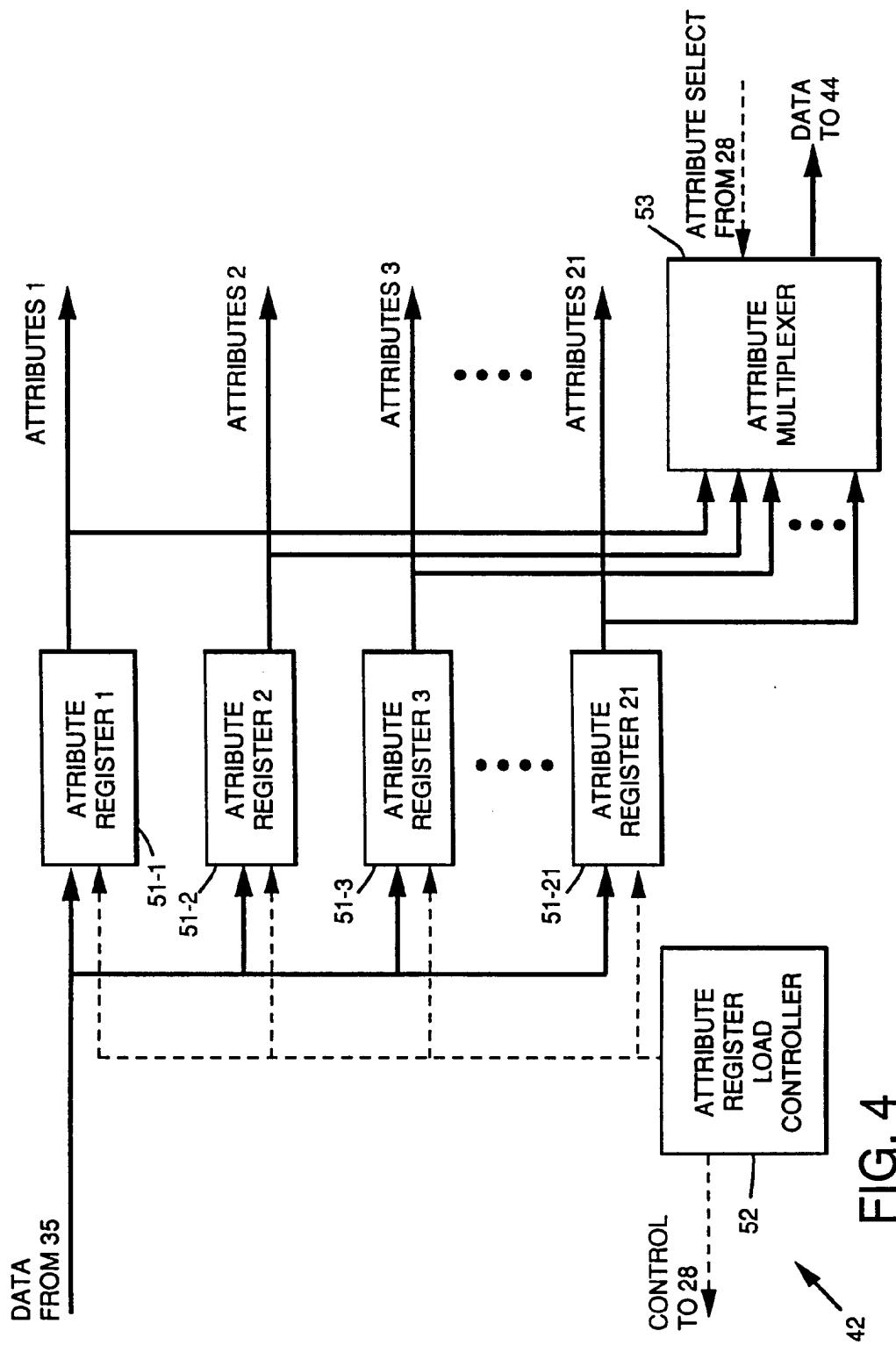
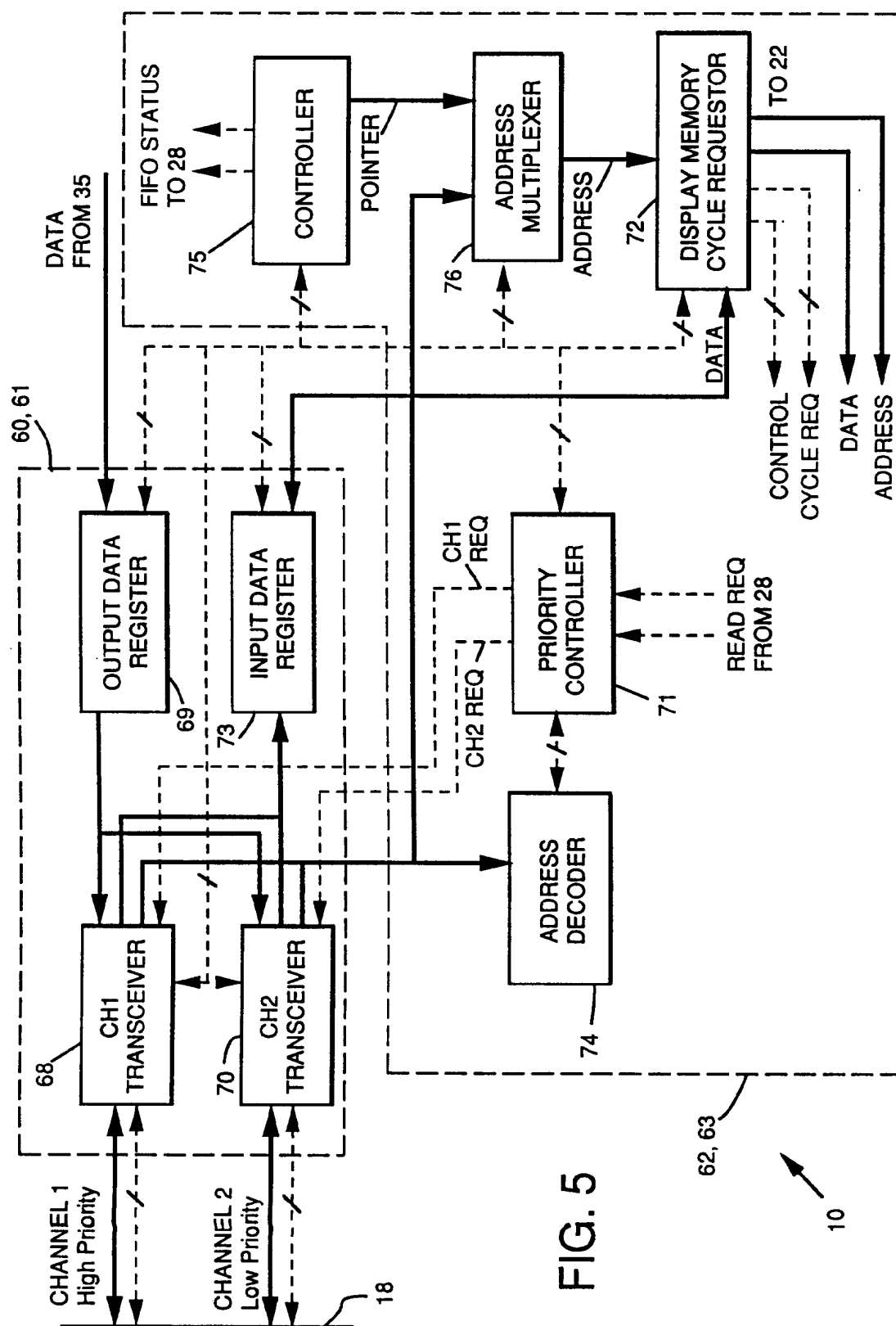


FIG. 4



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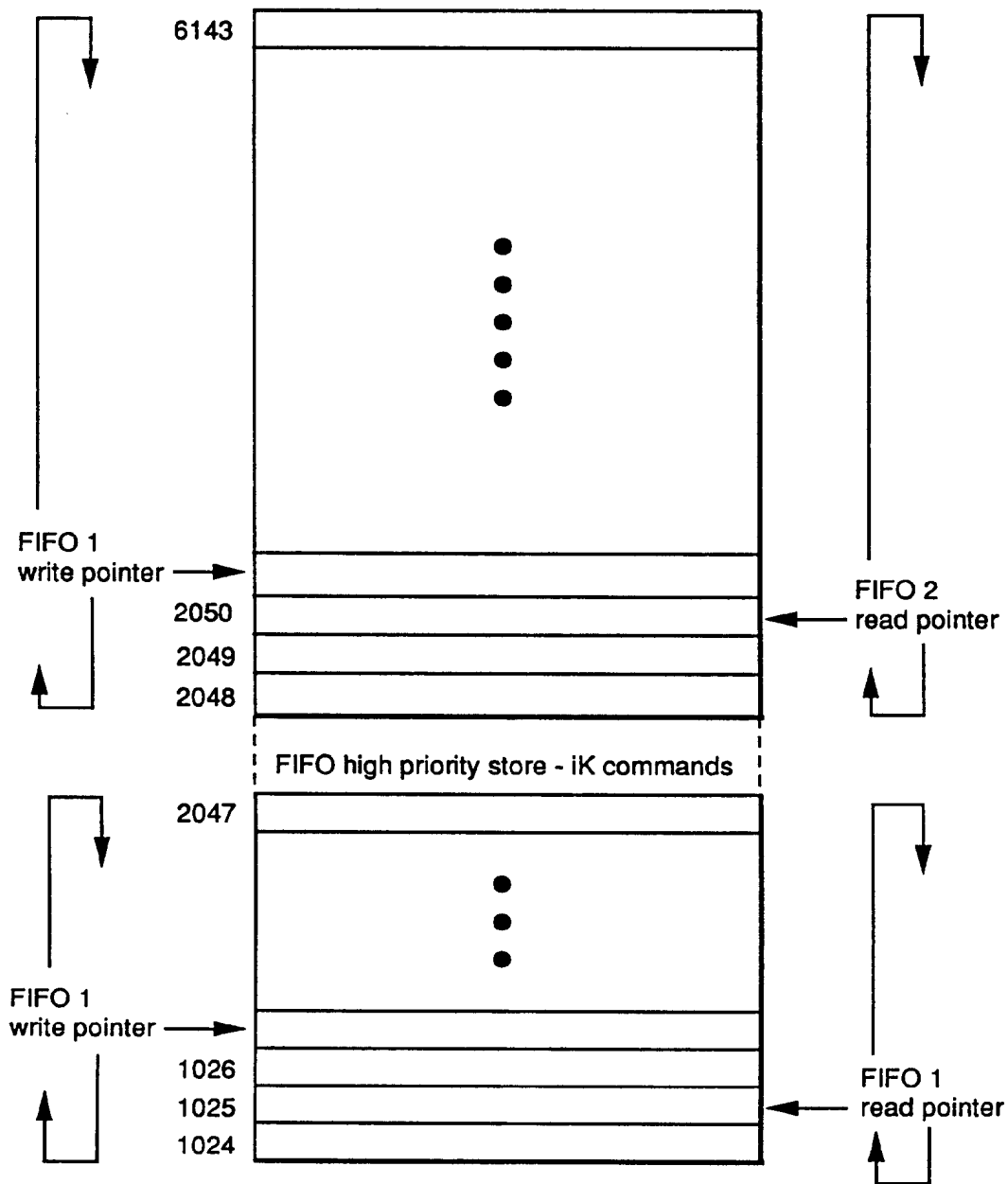


FIG. 6

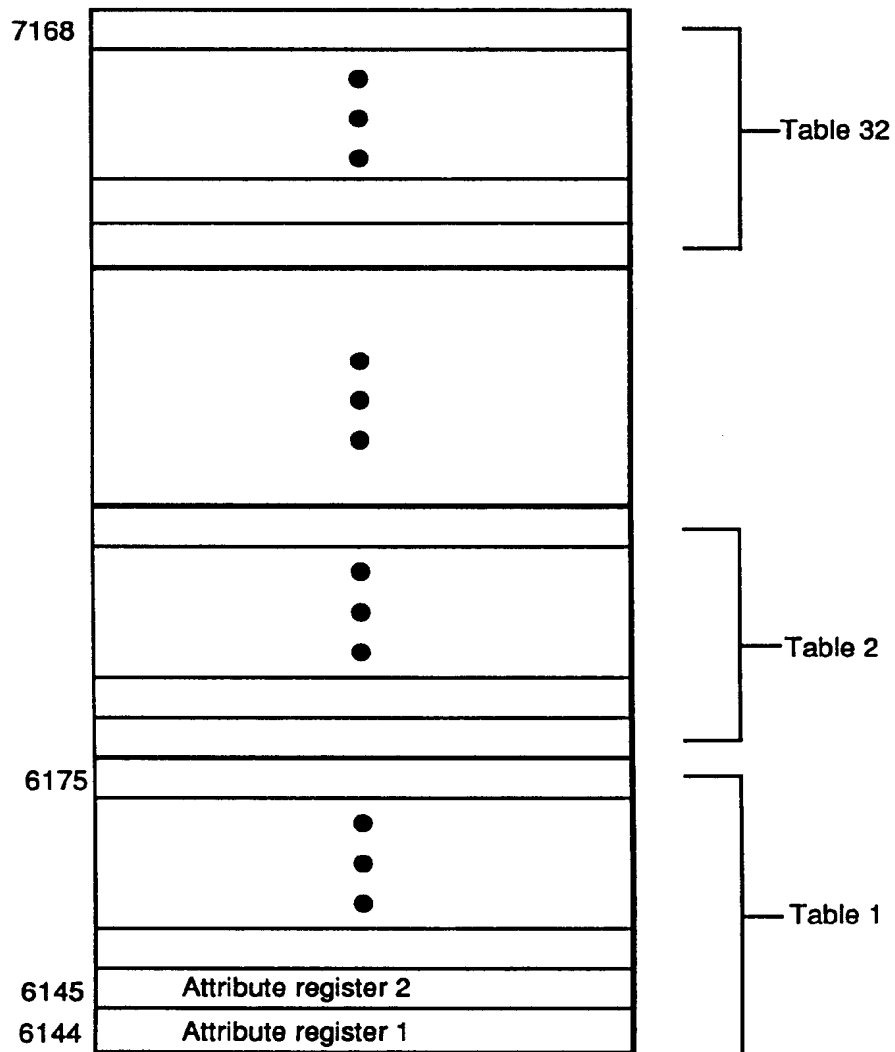


FIG. 7

PATENT COOPERATION TREATY

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Sterne, Kessler, Goldstein & Fox,
P.L.L.C.

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For more detailed instructions, see PCT Applicant's Guide, l_ . al Ph. . pa graphs 9.004 - 9.011.
- ☐ The appli_ s .b y not.f. _ no _ . on. se_ . port . l_ . tabl is.d _ _ _ c l_ . _ und.
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- ☐ **With regard to any protest** again_ pay_ . () addit_ . fee (s) und_ Rule 40.2, _ . l_ . is not.f. _ :
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PCT Applicant's Guide, N. i_ . Ch _ . rs .

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's filing reference 1972154PC01	FOR FURTHER ACTION as well as, where applicable, in 5 below.	Form PCT/ISA 220
International application No. PCT/US2010/047786	International filing date (day/month/year) 03/09/2010	(Elected) Priority Date (day/month/year) 03/09/2009
Applicant ADVANCED MICRO DEVICES, INC.		

This international search report has been prepared by the International Searching Authority in accordance with Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 4 sheets.

☒ It is also accompanied by a copy of each of the documents cited in this report.

1. Basis of the report

a. With regard to the language, the international search was carried out in the basis of:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into _____, which is the language of the translation furnished for the purposes of the international search (Rule 12.3(a) and 23.1(b)).

b. ☐ This international search report has been tabulated taking into account the rectification of an obvious mistake authorized by notification of the Authority under Rule 91 (Rule 43.6bis(a)).

c. ☐ With regard to the nucleotide and/or amino acid sequence disclosures in the international application, see Box No. I.

2. ☐ Certain claims were found unsearchable (See Box No. II)

3. ☐ Unity of invention is lacking (See Box No. III)

4. With regard to the title,

☐ the text is as received as submitted by the applicant.

☒ the text has been tabulated in accordance with the Authority's guidelines as follows:

GRAPHIC PROCESSING UNIT COMPRISING A COMMAND PROCESSOR WITH MULTIPLE BUFFERS TO ENABLE ASYNCHRONOUS CONCURRENT DISPATCH OF TASKS OF DIFFERENT TYPE ON A SHADER CORE

5. With regard to the abstract,

☒ the text is as received as submitted by the applicant.

☐ the text has been tabulated in accordance with Rule 38.2(b), as authorized by the Authority in accordance with Box No. IV. The abstract may, within the limits of the date of mailing of this international search report, be submitted by communication to the Authority.

6. With regard to the drawings,

a. The figures of the drawings will be published with the abstract as Figure No. 4

☐ as suggested by the applicant.

☐ as selected by the Authority, because the applicant failed to suggest a figure

☒ as selected by the Authority, because the figure is better adapted to the invention.

b. ☐ None of the figures should be published with the abstract

Realtek Ex. 1002

Case No. IPR2023-00687

Page 103 of 228

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2010/047786

A. CLASSIFICATION OF SUBJECT MATTER

INV. G06F9/50 G06F15/163 G06T15/_ G06T1/20
ADD.

Acc'd i. l. n. i. a. l. P. e. Class. fic. (IPC) . to bo. n. i. a. l. class. fic. i. l. d. IPC

B. FIELDS SEARCHED

M. n. m. u. m. c. d. (class. fic. i. sys. m. follow. b. y class. fic. . . . symbols)
G06F G06T

Do. c. d. m. n. m. u. m. t. exte. su. s. a. i. ncl. u. d. . n. t. f. i. e. l. d. s. c. d.

Electr. c. d. a. base cons. u. l. d. dur. t. i. a. l. (na. d. a. ba. d. , w. pract. ca. l. r. ms. us.)

EP0-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Cit. i. l. , wi. i. ndicati. , w. a. p. p. r. o. p. r. e. , ... t. l. e. v. a. passages	Releva. cla. m. No.
X	US 2_8 /109810 A1 (PRONOVOST STEVE [US] ET AL) 8 May 2_8 (2_ 8-05-08)	1-3,5-9, 11_5 , 17-21, 23-25
Y	abstract; cla_ ms 1-7,9_ 3 5_7 par. raphs [_19] - [_ 21]; figure 1 par. raphs [_ 22] - [_ 24]; figure 2 par. raphs [_05], [_ 25] - [_ 27]; f_ gures 3,4,5	4 0 6, 22
X	EP 0 475 421 A2 (HUGHES AIRCRAFT CO [US]) 18 March 1992 (1992-03_ 8)	25
Y	abstract; cla_ ms 1-3 3_4 6-17 page 2, l_ nes 20-26	4 0 6, 22
A	p. e 4, l_ nes 1-49; f_ gure 2 p. e 6, l_ nes 12-29; f_ gure 5	1,3,7,9, 13,15, 19,21
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☒ Furt. r. s. a. l. i. s. d. . n. t. co. i. n. u. Box C.

☒ See p. e. fam. ly . nex.

* Special ca. l. g. i. e. s. c. i. d. cu. s.

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21 September 2011

D. e. ma. i. l. t. i. e. m. i. a. l. se. port

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Na. d. ma. i. l. add. s. s. t. ISA/
Europe. P. e. Offi. 'ce, P. B. 5818 P. e. l. a. 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Au. Z. offic.
Realtek Ex. 1002
Case No. IPR2023-00687
de Junca, Irène
Page 104 of 228

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2010/047786

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 6 252 600 B1 (KOHLI ASHU [US] ET AL) 26 June 2001 (2001-06-26) abstract; claims 1,19,25 column 4, line 31 - column 5, line 13; figure 3 -----	25 1,3,7,9, 13,15, 19,21
X A	US 2009/160867 A1 (GROSSMAN MARK S [US]) 25 June 2009 (2009-06-25) claims 1,13,21 paragraphs [0025] - [0027]; figure 5 paragraph [0020]; figure 4 -----	25 6,12,18, 24

Realtek Ex. 1002

Case No. IPR2023-00687

Page 105 of 228

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2010/047786

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 2008109810	A1	08-05-2008	NONE	
EP 0475421	A2	18-03-1992	CA JP	2050658 A1 4299389 A
				15-03-1992 22-10-1992
US 6252600	B1	26-06-2001	NONE	
US 2009160867	A1	25-06-2009	NONE	

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

see form PCT/ISA/220

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY (PCT Rule 43bis.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (sec.d sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International applicati. N o.
PCT/US2010/047786

International filing date (day/month/year)
03.09.2010

Priority date (day/month/year)
03.09.2009

International Patent Classificati. (IPC) or both nati.al classificati. and IPC
INV. G06F9/50 G06F15/163 G06T15/00 G06T1/20

Applicant
ADVANCED MICRO DEVICES, INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis _ t _ . .I.
- ☐ Box No. II Prior_
- ☐ Box No. III Non-establishm. t _ i _ w.th _ gard _ novel _ inv.t ive step d industr.al a l cab.l.
- ☐ Box No. IV Lack _ un _ _ inv. ton
- ☒ Box No. V Reas. _ statem.t und Rule 43 bis.1(a)(.) w.th regard _ novel _ inv. tive step d n dustr.al appl.cabili _ citat.ons d ex pl.at.s _ su _ ort.ng such statem.t
- ☐ Box No. VI C.ta.n docum.ts _ c.t.
- ☒ Box No. VII C.ta.n defects .n t _ nt.t.al a _ l.c. on
- ☒ Box No. VIII Certa.n observati.s on t _ nt. _ tial a _ l.c. _

2. FURTHER ACTION

If a dem.d for _nt. _ t.al p.l imi.r y examin. _ is made, _ is _ .I. w.ll usually be c.s.d. _ be a writt. _ on _ t. Intern. io.l P.l.m.r y Exam.n.rg Authori ("IPEA") except that _s does not a ly whe t. a l.c. t chooses A uthor. oth. _ t h.s.e _ be t. IPEA d t. chos. IPEA has not.f t. Int.t.al Bu.au und. Rule 66.1bis(b) .at writt. _ in.s _ .s Intern. io.l Search.rg Author. _ will not be so c.s.d..

If th.s _ .I. is, as provid. above _ c.s.d. _ be a writt. _ n _ t. IPEA, t. a l.c.t. s .nvl. _ submit to t. IPEA a writt. _ ply _ geth. _ whe a r _ r _ e, w.th am.d.m. ts, befo. t. ex pirat. _ 3 m _ s from t. date _ ma.l.rg _ Form PCT /ISA/220 or befo. t. exp.r. _ 22 m.s _ from t. pr.or. d. e, wh.c.v. ex _ p.s l _ .

For fur. _ tis _ , see Form PCT/ISA/220.

3. For furth. deta.ls, see notes _ Form PCT /ISA/220.

Name and mailing address of the ISA:



European Patent Office
D-80298 Munich
Tel. +49 89 2399 - 0
Fax: +49 89 2399 - 4465

Date of completi. of
this opini.

see form
PCT/ISA/210

Authorized Officer

Realtek Ex. 1002
de Junca Irène
Case No. IP2023-00687
Telephone N o. +49 89 2399-6014
Page 107 of 228



**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

Inventor's Application No.
PCT/US2010/047786

Box No. I Basis of the opinion

1. With regard to the **language**, it is hereby established one of the following:
- ☒ The invention is disclosed in the language in which it was filed.
- ☐ A translation of the invention into the language of a translation furnished for the purpose of filing the search (Rule 12.3(a) and 23.1 (b)).
2. ☐ This invention has been established in accordance with **rectification of an obvious mistake** authorized by not in itself to its Authority under Rule 91 (Rule 43b.1(a)).
3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the invention as a disclosure, it is hereby established one of the following:
- a. (means)
- ☐ on paper.
- ☐ in electronic form
- b. (time)
- ☐ in the invention as disclosed.
- ☐ together with the international application in electronic form
- ☐ subsequently to its Authority for the purpose of search
4. ☐ In addition, in the case of a multiple sequence of a sequence list, it has been filed or furnished, the relevant sequences of the information in the subsequence or additional sequence is identical to the application of the filing do not go beyond the application of the filing, a further, we furnish.
5. Additional comments:

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes: Claims <u>4, 5, 10, 11, 16, 17, 22, 23, 25</u>
	No: Claims <u>1-3, 6-9, 12-15, 18-21, 24</u>
Inventive step (IS)	Yes: Claims
	No: Claims <u>1-25</u>
Industrial applicability (IA)	Yes: Claims <u>1-25</u>
	No: Claims

2. Citations and explanations

see separate sheet

Box No. VII Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Summary

- Claims 1, 3, 7, 9-10, 13, 15-16, 19, 21-22 and 25 do not meet the requirements of Article 6 PCT.
- The subject-matter of independent claims 1, 7, 13 and 19 is not new (Article 33(2) PCT).
- The subject-matter of independent claim 25 does not involve an inventive step in the sense of Article 33(3) PCT.
- Dependent claims 2-6, 8-12, 14-18 and 20-24 do meet the requirements of the PCT in respect of novelty and/or inventive step (Articles 33(2) 33(3) PCT).

Documents

Reference is made to the following documents:

D1 US 2008/109810 A1 - PRONOVOST STEVE [US] et AL - 8 May 2008

Re Item V - Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1 Preliminary remarks

- 1.1 The term "shader core" used in claim 1 is defined on page 2 paragraph [0005] as a dedicated processing unit in a GPU. This interpretation will be used in the rest of the communication.
- 1.2 Claim 1 refers to a feature called "virtual engine" whereby the term "virtual" in combination with "engine" is ambiguous and vague. However, the dedicated processing unit [page 6 paragraph [0026]; page 9 paragraph [0040]] defined in the term "virtual engine" means embodiment of a shader, which means which actually guide to execute a stream of tasks from the OS scheduler, and to execute these tasks on the single shader. Further dedicated processing [page 7 paragraphs [0028-0029]; page 8 paragraph [0034]] still the plurality of virtual engines shall be sources (spatial and/or temporal partitioning). Said single shader to enable simultaneous execution of tasks issued from different virtual engines. Thus a "virtual engine" is not identical to a dedicated processing unit using a given portion of the source code (i.e. partition) of the single shader to execute the tasks it handles. This interpretation will be used in the rest of the communication.
- 1.3 Dependent claims 4, 10, 16 and 22 refer to the features "low-latency task" and "regular-latency task". The dedicated processing [page 2 lines 24, 26, 30-31; page 3 lines 1-3, 15-16, 23, page 15 lines 11-16] defined in a "low-latency task" is a more important task (a task with a high priority level), but does not provide any further definition of a "regular-latency task". However, it is considered that a "regular-latency task" is a task which has no high-priority level and its execution will be used in the rest of the communication.

1.4 B. on the script [page 2 lines 24,26,30-31; page 3 lines 1-3,15-16,23, page 15 lines 11-16] the term "priority" used in claim 25 will be interpreted as a priority level. It will attack.

2 Independent claims

The present invention does not meet the criteria of Article 33(1) PCT, because the subject matter of claims 1, 7, 13 and 19 is not new in the sense of Article 33(2) PCT and the subject matter of claim 25 does not involve an inventive step in the sense of Article 33(3) PCT.

2.1 Independent claim 1 (processing unit)

Dumitru discloses (italics will be used to indicate the original word in the present invention; underlined words in the following are used for emphasis; strikeout words lead to unclear terms and/or expressions; references in brackets refer to the document):

A processing unit [page 1: abstract; page 1 (100); page 3 (3)] - graphical processing unit (GPU) comprising:

→ *a plurality of virtual engines [page 1: abstract, page 1 - 1.5 with multiple GPUs] configured to receive, from an operating system (OS), a plurality of tasks [page 1: GPU contexts of execution] substantially in parallel with each other [page 1: GPUs [20]-[21] - GPU contexts of execution] can be controlled by the user mode driver against a virtual address and typically a display scheduler on the graphics unit with in [page 1: GPUs [23] & page 2 (210) - hardware queue for every parallel graphics finishing by the display driver; page 1: GPUs [23] & page 3 - model of parallelism for multiple GPUs] and load a set of state data associated with each of the plurality of tasks [page 1: paragraph [21] - Each GPU context has a pool of state DMA buffers, with in each buffers can only be built against the graphics unit within the [page 1: 1.5] [claim 9 & page 1: GPUs [24] - The kernel mode driver maintains a buffer pool. The graphics unit DMA buffers are taken from the scheduler and accumulated. Thus data contained in the DMA buffers is written to each GPU context is loaded for the graphics];*

and

→ *a shader core [page 1: 1.5] configured to execute the plurality of tasks substantially in parallel [page 1: claim 2 & page 1: GPUs [20] - Multiple GPU contexts of execution (GPU context) can be controlled against a virtual address; paragraph [21] - the user mode driver can typically use (121, 122, 123) on which each context will be executed. The buffers [page 1: 1.5] based on the set of state data associated with each of the plurality of tasks [page 1: paragraph [21] - Each GPU context has a pool of state DMA buffers, with in each buffers can only be built against the graphics unit within the [page 1: 1.5] node; claim 9 & page 1: GPUs [24] - The kernel mode driver maintains a buffer pool. The graphics unit DMA buffers are taken from the scheduler and accumulated.]*

2.2 Like prior art claims 7, 13 a. 1 9

The same ... of claim 1 applied, means means is, to the subject-matter of the
computer program (claims 7 (computer program), 13 (computer system) a. 1 9 (method)),
wherein the also claimed not new.

2.3 Independent claim 25 (method)

Project scheduling process. A process unit is well-known to the skilled person. The
unit is a (3D rendering) of the is applied. For sake of comparison it is mentioned
in the text book "Operating Systems" by A. W. S. Tannenbaum (second edition, published
in 1997 - ISBN 0-13-638677) and by citations in the prior art. [section 2.4.2
on pages 85-86; figure 2-23]. This claim teaches each process is a unit. It is a
its own unit. Group processes in the unit. As to the project scheduling, among
the claims, broadly, broadly, broadly, broadly, each class. Thus a scheduling unit. Such a
basic priority-scheduling algorithm performs the set of the multiple tasks, each task
is assigned a priority, a set of the over the process unit (CPU) with tasks broadly on
the assigned priority. Therefore the subject-matter of claim 25 does not involve an inventive
step over the teaching of D1 combined with the basic knowledge of the skilled person.

3 Dependent claims

Dependent claims 2-6, 8-12, 14-18 a. 20 -24 do not contain any features which, in
combination with the features of any claim which they further meet, are required of the
PCT in order to constitute an inventive step over the following:

3.1 As to claims 2, 8, 14, 20 : D1 [figure 1 & paragraph [0019]; figure 3 & paragraphs [0005],[0025]] discloses
a first plurality of process elements (Node 0) for executing a first task (3D rendering) and a
second plurality of process elements (Node 1) for executing a second task (video
process).

3.2 As to claims 3, 9, 15, 21 : D1 [figure 2; paragraph [0023]; claims 9-10] discloses a first queue
("Hardware Queue Line 0" or "Hardware Queue Line 1"). The NODE 0 processes the tasks
of type "3D rendering" and a second queue ("Hardware Queue") processes the tasks of type
"video".

3.3 As to claims 4, 10, 16, 22 :

As explained in the claim 3, a "low-latency task" is a task with a
high priority level. A "regular-latency task" is a task with a high priority level. Thus the
priority level of a "low-latency task" is higher than the priority level of a "regular-latency task".
However, the next task to be processed is based on a priority level which is customary
practice known from the skilled person.

- 3.4 As claimed in 5, 11, 16, 23: Claimed skill requires understanding of the feature "general compute task" as a task executable by a CPU and the feature "graphics processing task" as a task executable by a GPU. The subject-matter of claim 5, 1, 13 and 23 defines the first type of task as a "graphics processing task" and the second type of task as being a "general compute task". However, tasks belonging to the same group of tasks (graphics processing tasks) and tasks belonging to the same group of tasks (general compute tasks) may be of different types of tasks (like 3D graphics processing tasks, video processing tasks) and accumulated on different hardware queues, could also be parallel, with execution involving skill, technique, "general compute tasks" and new type of tasks being executable on a GPU.
- 3.5 As claimed in 6, 12, 18, 24: D1 [claim 5; paragraphs [0022]-[0023] & figure 2 (scheduler thread)] discloses a scheduler thread scheduling a plurality of tasks being issued to a shad. core (no.).

Re Item VII Certain defects in the international application

- 4 The following defects have been identified:
- 4.1 The claim does not contain sufficient signs in parentheses, Rule 6.2(b) PCT.
- 4.2 The independent claim is not in the two-part form vis-à-vis D1, Rule 6.3(b) PCT.
- 4.3 D1 is not mentioned in the description, Rule 5.1(a)(i) PCT.
- 4.4 The word "split and" in the script [page 6, paragraph [0027] last sentence] is not clear and should be moved from the publication (PCT Guidelines Part II Chapter V - 5.30).

Re Item VIII Certain observations on the international application

- 5 Although claims 19 and 25 have been drafted separately, they are effectively to the same subject-matter and differ from each other only with regard to the initial of the subject-matter which object is sought and/or in respect of the terminology used. The subject-matter of the claim is not clear and does not meet the requirements of Article 6 PCT.
- 6 Claim 1, 3, 7, 9-10, 13, 15-16, 19, 21-22 and 25 do not meet the requirements of Article 6 PCT. It follows that:
- 6.1 Claim 1, 3, 7, 9, 13, 19 and 21 fail to define a feature called "virtual engine" whereby the term "virtual" in combination with "engine" is ambiguous and vague. This leaves the reader in doubt as to the meaning of the technical feature which it defines, thereby making the definition of the subject-matter of said claim unclear.

- 6.2 The expression "*substantially in parallel*" is used in claims 1, 7, 13 and 19. However, the relative term "*substantially*" has no well-recognized meaning and its use is in doubt as to the manner in which it is to be applied. It is noted that the definition of the subject-matter of claim 19 is unclear.
- 6.3 Claims 1, 7, 13 and 19 use the word *a set of state data associated with each of the plural of tasks* "whereby the state data could be in a predetermined kind of information related to the task, such as, for example, like the save execution of a task prior to a task context switching. However, the description [page 2 lines 3-4] on the definition of *state data* being data related to the handling, scheduling, transformation, or other like task, the word *state data* thus has not a precise execution of a task, but consists of a data which is used to execute the task. Consequently, claim 1 is not supported by the description as required by Article 84 EPC, its scope is broad, though justified by the description and drawings.
- 6.4 The relative term "*regular*" in combination with the term "*latency*", used in the word *regular-latency task* in claims 4, 10, 16 and 22 has no well-recognized meaning and its use is in doubt as to the manner in which it is to be applied. It is noted that the definition of the subject-matter of claim 19 is unclear, Article 6 PC T.
- 6.5 The word *"each task includes an indication of a priority"* and *"the indication of priority associated with each task"* is used in claim 25. First, the term "*priority*" is ambiguous and vague and its use is in doubt as to the manner in which it is to be applied. It is noted that the definition of the subject-matter of claim 19 is unclear, Article 6 PC T. Second, it is noted that the definition of the subject-matter of claim 19 is unclear, Article 6 PC T. Third, the word "*indication of a priority*" is included in the claim, but suggested with the task in the said method step. It is not a sufficient skill person who the indication of the priority type should be provided since it is included in the task provided in the process unit. Therefore, the definition of the subject-matter of claim 25 is unclear.

Possible steps after receipt of the international search report (ISR) and written opinion of the International Searching Authority (WO-ISA)

General information	For an international application filed on or after 01/01/2004 the competent ISA will establish an ISR. It is accompanied by the WO-ISA. Unlike the former written opinion of the IPEA (Rule 66.2 PCT), the WO-ISA is not meant to be responded to, but to be taken into consideration for further procedural steps. This document explains about the possibilities.
Amending claims under Art. 19 PCT	Within 2 months after the date of mailing of the ISR and the WO-ISA the applicant may file amended claims under Art. 19 PCT directly with the International Bureau of WIPO. The PCT Rules of 2004 did not change this procedure. For further information please see Rule 46 PCT and the PCT/ISA/220 decision concerning Non-stoppable PCT/ISA/220.
Filing a demand for international preliminary examination	In principle, the WO-ISA will not consider the written opinion of the IPEA. This should, in many cases, make it unnecessary to file a demand for international preliminary examination. If the applicant nevertheless wishes to file a demand this must be done no later than 3 months after the date of mailing of the ISR/WO-ISA or 22 months after priority date, whichever expires later (Rule 54bis PCT). Amendments under Art. 34 PCT can be filed with the IPEA at the same time as filing the demand (Rule 66.1 (b) PCT). If a demand for international preliminary examination is filed and no comments/amendments have been received the WO-ISA will transmit the IPEA to an IPRP (International Preliminary Report on Patentability) which would merely reflect the conclusions of the WO-ISA. The demand can still be withdrawn (Art. 37 PCT).
Filing informal comments	After receipt of the ISR/WO-ISA the applicant may file informal comments with the WO-ISA directly with the International Bureau of WIPO. These will be communicated to the designated Offices together with the IPRP (International Preliminary Report on Patentability) 30 months from the priority date. Please also fill in the next box.
End of the international phase	At the end of the international phase the International Bureau of WIPO will transmit the WO-ISA or, if a demand was filed, the written opinion of the IPEA to the IPRP, which will be transmitted together with the possible informal comments to the designated Offices. The IPRP replaces the IPEA (International preliminary examination report).
Relevant PCT Rules and more information	Rule 43 PCT, Rule 43bis PCT, Rule 44 PCT, Rule 44bis PCT, PCT Newsletter 12/2003, OJ 11/2003, OJ 12/2003

Electronic Acknowledgement Receipt

EFS ID:	11292197
Application Number:	12874134
International Application Number:	
Confirmation Number:	6612
Title of Invention:	Processing Unit that Enables Asynchronous Task Dispatch
First Named Inventor/Applicant Name:	Michael MANTOR
Customer Number:	26111
Filer:	Theodore A. Wood/Delain Crooks
Filer Authorized By:	Theodore A. Wood
Attorney Docket Number:	1972.1540001
Receipt Date:	28-OCT-2011
Filing Date:	01-SEP-2010
Time Stamp:	17:07:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		19721540001.pdf	1031989 c54ee519a71064433c2aca8805c47a572a79e116	yes	9

	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Miscellaneous Incoming Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	7	
	Information Disclosure Statement (IDS) Form (SB08)		8	9	
Warnings:					
Information:					
2	Foreign Reference	19721540001FP1REFERENCE.pdf	1184866 a34c7c7af87b96c30ae6511f29933a6ceb8a467f	no	18
Warnings:					
Information:					
3	Non Patent Literature	19721540001NPL1REFERENCE.pdf	151170 c5174a30fa2bcc16f340de8eede00531199a2d17	no	14
Warnings:					
Information:					
Total Files Size (in bytes):			2368025		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

THEODORE A. WOOD
DIRECTOR
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October 28, 2011

Commissioner for Patents
PO Box 1450
Alexandria, VA22313-1450

Confirmation No. 6612
Art Unit 2628
Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Application No. 12/874,134; Filing Date: September 1, 2010
For: **Processing Unit that Enables Asynchronous Task Dispatch**
Inventors: MANTOR *et al.*
Our Ref: 1972.1540001

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Information Disclosure Statement;
2. Form PTO/SB/08a (1 sheet) listing 4 documents (US1-US3 and FP1);
3. Form PTO/SB/08b (1 sheet) listing 1 documents (NPL1); and
4. Copies of cited documents (FP1-FP1 and NPL1).

The above-listed documents are filed electronically through EFS-Web.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Theodore A. Wood
Attorney for Applicants
Registration No. 52,374

TAW/jeg
Enclosure(s)

1435770_1.DOCX



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
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www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
12/874,134		2628	



Correspondence Address/Fee Address Change

The following fields have been set to Customer Number 91505 on 05/11/2012

- Correspondence Address

The address of record for Customer Number 91505 is:

91505

Sterne, Kessler, Goldstein & Fox P.L.L.C.

1100 New York Avenue N.W.

Washington, DC 20005



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/874,134

09/01/2010

Michael MANTOR

1972.1540001

6612

91505 7590 07/18/2013
Sterne, Kessler, Goldstein & Fox P.L.L.C.
1100 New York Avenue N.W.
Washington, DC 20005

EXAMINER

CRAWFORD, JACINTA M

ART UNIT

PAPER NUMBER

2677

MAIL DATE

DELIVERY MODE

07/18/2013

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 12/874,134	Applicant(s) MANTOR ET AL.	
	Examiner JACINTA M. CRAWFORD	Art Unit 2677	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 1 September 2010.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 5) ☒ Claim(s) 1-25 is/are pending in the application.
5a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) _____ is/are allowed.
- 7) ☒ Claim(s) 1-25 is/are rejected.
- 8) ☐ Claim(s) _____ is/are objected to.
- 9) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 01 September 2010 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some * c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☒ Notice of References Cited (PTO-892) | 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>10/28/2011</u> . | 4) ☐ Other: _____ |

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on October 28, 2011 was filed after the mailing date of the application on September 1, 2010. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 112

2. The following is a quotation of 35 U.S.C. 112(b):
(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1, 7, 13, and 19 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention. Claims 1, 7, 13, and 19 recite the limitation, “receive, from an operating system, a plurality of tasks substantially in parallel with each other...a shader core configured to execute the plurality of tasks substantially in parallel...”(claim 1) where the term "substantially" is not definite.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –
(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 25 is rejected under pre-AIA 35 U.S.C. 102(e) as being anticipated by Jiao et al. (US 8,345,053).

As to claim 25, Jiao et al. disclose a computer implemented method for providing tasks to a processing unit, comprising: receiving a plurality of tasks from one or more applications, wherein each task includes an indication of a priority type (*Figure 2 illustrates threads from graphics program where threads may indicate specific tasks performed, where the instructions indicate specific operations to perform on each thread, which can be considered "indicating a priority type," column 2, lines 65-66*); and providing, to the processing unit, the plurality of tasks and the indication of the priority type associated with each task (*Figures 2 and 3 illustrates threads received by MUX and further by thread scheduler to distribute to hardware units as illustrated, column 2, lines 60-62 and column 4, lines 19-28*).

Claim Rejections - 35 USC § 103

6. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-24 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Jackson (US 2011/0050712) in view of Jiao et al. (US 8,345,053).

As to claim 13, Jackson discloses a computing system, comprising:

a memory (*Figure 2, memory 270*); a processing unit (*Figure 2, host 103*); and a bus coupled to the memory and the processing unit (*as denoted by arrows*), wherein the processing unit comprises a plurality of virtual engines configured to (i) receive, from an operating system (OS), a plurality of commands and translate the commands to be further processed to render an image by the graphics hardware (*i.e. Figure 1, virtual machines 121 with virtual graphics devices 220, Figure 2; see Figure 3*).

Jackson differs from the invention defined in claim 13 in that Jackson does not disclose (i) receive, from an operating system (OS), a plurality of tasks substantially in parallel with each other and (ii) load a set of state data associated with each of the plurality of tasks; and a shader core configured to execute the plurality of tasks substantially in parallel based on the set of state data associated with each of the plurality of tasks.

Jiao et al. disclose a computing system, comprising:

a memory (*i.e. Figure 1, main memory 160*); a processing unit (*i.e. graphics processor 120*); and a bus coupled to the memory and the processing unit (*i.e. Figure 1 notes arrows which denotes connection/coupling*), wherein the processing unit comprises: a plurality of engines (*i.e. Figures 2 and 3 notes various engines, flow controller 212, ALU core 220, elementary function core 230, etc*) configured to (i) receive, from an operating system (OS), a plurality of tasks substantially in parallel with each other (*Figure 2 illustrates threads from graphics programs where threads may indicate specific tasks performed, where the threads allow a program to have multiple tasks performed simultaneously by different units, see column 2, lines 21-29; NOTE: Figure 2 notes threads enter through MUX 208 to thread scheduler 210 and further distributed by thread scheduler to various hardware units in parallel, which would denote receiving in parallel, column 2, lines 58-62, and column 4, lines 21-23; operating system inherent in computing system*) and (ii) load a set of state data associated with each of the plurality of tasks (*column 2, lines 21-29 notes the threads may indicate specific tasks performed with a set of one or more instructions, where the instructions indicate specific operations to perform on each thread, column 2, lines 65-66*); and a shader core configured to execute the plurality of tasks substantially in parallel based on the set of state data associated with each of the plurality of tasks (*Figure 2, shader 130 notes hardware units/engines to execute tasks in parallel, see column 4, lines 17-19*).

Art Unit: 2677

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Jiao et al.'s system and also the function of receiving and executing tasks in parallel to enhance the functionality of multitasking and reduce processing time which ultimately enhances the performance of the overall system.

Claims 1, 7, and 19 are similar in scope to claim 13 above, and are therefore rejected under similar rationale.

As to claims 2, 8, 14, and 20, Jackson modified with Jiao et al. disclose the shader core comprises: a first plurality of processing elements configured to execute a first task based on a first set of state data associated with the first task; and a second plurality of processing elements configured to execute a second task based on a second set of state data associated with the second task (*Jiao, Figures 2 and 3 notes various hardware units for performing tasks*).

As to claims 3, 9, 15, and 21, Jackson modified with Jiao et al. disclose the plurality of virtual engines comprises (i) a first queue configured to receive a first type of task and (ii) a second queue configured to receive a second type of task (*Jackson, Figure 1 illustrates plural virtual machines where the virtual graphics devices receives commands, Figure 3; Jiao, column 4, lines 9-17 notes hardware units to operate independently; line 59-64 notes each hardware unit may include its own instruction decoder*).

Art Unit: 2677

As to claims 4, 10, 16, and 22, Jackson modified with Jiao et al. disclose the first type of task comprises a low-latency task and the second type of task comprises a regular-latency task (*Jiao, Figures 2 and 3 illustrates hardware units such as ALU core and elementary function core which may perform general operations, see column 3, lines 5-24, where the texture sampler may perform graphics processing, see column 2, lines 35-40 and column 4, lines 34-40*).

As to claims 5, 11, 17, and 23, Jackson modified with Jiao et al. disclose the first type of task comprises a graphics-processing task and the second type of task comprises a general-compute task (*Figures 2 and 3 illustrates hardware units such as ALU core and elementary function core which may perform general operations, see column 3, lines 5-24, where the texture sampler may perform graphics processing, see column 2, lines 35-40 and column 4, lines 34-40*).

As to claims 6, 12, 18, and 24, Jackson modified with Jiao et al. disclose the processing unit further comprises: a scheduling module that schedules the plurality of tasks to be issued to the shader core (*Jiao, Figures 2 and 3, thread scheduler 210*).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JACINTA M. CRAWFORD whose telephone number is (571)270-1539. The examiner can normally be reached on M-F 8:00a.m. - 5:00p.m. EST.

Art Unit: 2677

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JACINTA M CRAWFORD/
Primary Examiner, Art Unit 2677

Notice of References Cited	Application/Control No. 12/874,134		Applicant(s)/Patent Under Reexamination MANTOR ET AL.	
	Examiner JACINTA M. CRAWFORD		Art Unit 2677	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-8,345,053	01-2013	Jiao et al.	345/505
*	B	US-2007/0030278	02-2007	Prokopenko et al.	345/506
*	C	US-2007/0273698	11-2007	Du et al.	345/501
*	D	US-2011/0050712	03-2011	Jackson, Adam D.	345/503
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes 	Application/Control No. 12874134	Applicant(s)/Patent Under Reexamination MANTOR ET AL.
	Examiner JACINTA M CRAWFORD	Art Unit 2677

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
345	502, 505	7/14/2013	JMC
718	102, 103	7/14/2013	JMC

SEARCH NOTES		
Search Notes	Date	Examiner
EAST; Inventor and Assignee search	7/14/2013	JMC
NPL search	7/14/2013	JMC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

	/JACINTA M CRAWFORD/ Primary Examiner.Art Unit 2677
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Equivalent of Form PTO/SB/08a(07-09)

Substitute for form 1449/PTO		Complete if Known	
		Application Number	12/874,134
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Filing Date	September 1, 2010
		First Named Inventor	Michael MANTOR
		Art Unit	2628
		Examiner Name	Tung, Kee M.
		Attorney Docket Number	1972.1540001
Sheet	1	of	1

U.S. PATENT DOCUMENTS					
Examiner initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	US1	6,252,600 B1	06-26-2001	Kohli et al.	
	US2	2008/0109810 A1	05-08-2008	Pronovost et al.	
	US3	2009/0160867 A1	06-25-2009	Grossman	
	US4				
	US5				
	US6				
	US7				
	US8				
	US9				
	US10				
	US11				
	US12				
	US13				
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	US16				
	US17				
	US18				
	US19				
	US20				

FOREIGN PATENT DOCUMENTS						
Examiner initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	†6
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
	FP1	EP 0 475 421 A2	03-18-1992	Hughes Aircraft Co.		
	FP2					
	FP3					
	FP4					
	FP5					
	FP6					
	FP7					
	FP8					

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Examiner Signature	Date Considered
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

Equivalent of Form PTO/SB/08b(7-09)

Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Application Number	12/874,134
				Filing Date	September 1, 2010
				First Named Inventor	Michael MANTOR
				Art Unit	2628
				Examiner Name	Tung, Kee M.
Sheet	1	of	1	Attorney Docket Number	1972.1540001

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
	NPL1	International Search Report and Written Opinion, dated September 29, 2011, for PCT Appl. No. PCT/US2010/047786, 14 pages.	
	NPL2		
	NPL3		
	NPL4		
	NPL5		
	NPL6		
	NPL7		
	NPL8		
	NPL9		
	NPL10		

1435747_1.DOCX

Examiner Signature	/Jacinta Crawford/	Date Considered	07/13/2013
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.



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BIB DATA SHEET

CONFIRMATION NO. 6612

SERIAL NUMBER 12/874,134	FILING or 371(c) DATE 09/01/2010 RULE	CLASS 345	GROUP ART UNIT 2677	ATTORNEY DOCKET NO. 1972.1540001	
APPLICANTS Michael MANTOR, Orlando, FL; Rex McCrary, Oviedo, FL; ** CONTINUING DATA ***** This appln claims benefit of 61/239,712 09/03/2009 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 09/21/2010					
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /JACINTA M Acknowledged CRAWFORD/ Examiner's Signature	☐ Met after Allowance JC Initials	STATE OR COUNTRY FL	SHEETS DRAWINGS 6	TOTAL CLAIMS 25	INDEPENDENT CLAIMS 5
ADDRESS Sterne, Kessler, Goldstein & Fox P.L.L.C. 1100 New York Avenue N.W. Washington, DC 20005 UNITED STATES					
TITLE Processing Unit that Enables Asynchronous Task Dispatch					
FILING FEE RECEIVED 1920	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

<i>Index of Claims</i> 	Application/Control No. 12874134	Applicant(s)/Patent Under Reexamination MANTOR ET AL.
	Examiner JACINTA M CRAWFORD	Art Unit 2677

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		DATE							
Final	Original	07/14/2013							
	1	✓							
	2	✓							
	3	✓							
	4	✓							
	5	✓							
	6	✓							
	7	✓							
	8	✓							
	9	✓							
	10	✓							
	11	✓							
	12	✓							
	13	✓							
	14	✓							
	15	✓							
	16	✓							
	17	✓							
	18	✓							
	19	✓							
	20	✓							
	21	✓							
	22	✓							
	23	✓							
	24	✓							
	25	✓							

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

MANTOR et al.

Appl. No.: 12/874,134

Filed: September 1, 2010

For: **Processing Unit That Enables
Asynchronous Task Dispatch**

Confirmation No.: 6612

Art Unit: 2677

Examiner: Crawford, Jacinta M.

Atty. Docket: 1972.1540001

Amendment and Reply Under 37 C.F.R. § 1.111

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

In reply to the Office Action dated July 18, 2013 ("Office Action"), Applicants submit the following Remarks.

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (*Currently Amended*) A processing unit comprising:

a plurality of ~~virtual~~ engines configured to ~~[[i)]]~~ receive, from an operating system (OS), a plurality of tasks ~~substantially in parallel with each other and (ii) and to~~ load a set of state data associated with each of the plurality of tasks; and

~~a shader core configured to receive the plurality of tasks from at least one of the plurality of engines and to execute a first task from the plurality of tasks substantially in parallel while executing a second task from the plurality of tasks based on the set of~~ respective state data associated with each of the ~~plurality of~~ first and second tasks.

2. (*Currently Amended*) The processing unit of claim 1, wherein the shader core comprises:

a first plurality of processing elements configured to execute ~~[[a]]~~ the first task based on a first set of state data associated with the first task; and

a second plurality of processing elements configured to execute ~~[[a]]~~ the second task based on a second set of state data associated with the second task.

3. (*Currently Amended*) The processing unit of claim 1, wherein the plurality of ~~virtual~~ engines comprises ~~[[i)]]~~ a first queue configured to receive a first type of the first task and ~~[[ii)]]~~ a second queue configured to receive a second type of the second task.

4. (*Currently Amended*) The processing unit of claim ~~[[3]]~~ 1, wherein the first ~~type of~~ task comprises a low-latency task and the second ~~type of~~ task comprises a regular-latency task.

5. (*Currently Amended*) The processing unit of claim ~~[[3]]~~ 1, wherein the first ~~type of~~ task comprises a graphics-processing task and the second ~~type of~~ task comprises a general-compute task.

6. (*Currently Amended*) The processing unit of claim 1, further comprising:
a scheduling module ~~that schedules~~ configured to schedule the plurality of tasks to be issued to the shader core based on a priority associated with each of the plurality of tasks.

7. (*Currently Amended*) A computer-program product comprising a computer-readable storage medium containing instructions that, if executed on a computing device, define a processing unit comprising:

a plurality of ~~virtual~~ engines configured to ~~[(i)]~~ receive, from an operating system (OS), a plurality of tasks ~~substantially in parallel with each other and (ii) and to~~ load ~~a set of~~ state data associated with each of the plurality of tasks; and

a shader core configured to receive the plurality of tasks from at least one of the plurality of engines and to execute a first task from the plurality of tasks substantially in parallel while executing a second task from the plurality of tasks based on the set of respective state data associated with each of the ~~plurality of~~ first and second tasks.

8. (*Currently Amended*) The computer-program product of claim 7, wherein the shader core comprises:

a first plurality of processing elements configured to execute ~~[[a]]~~ the first task based on a first set of state data associated with the first task; and

a second plurality of processing elements configured to execute ~~[[a]]~~ the second task based on a second set of state data associated with the second task.

9. (*Currently Amended*) The computer-program product of claim 7, wherein the plurality of ~~virtual~~ engines comprises ~~[[i)]]~~ a first queue configured to receive ~~a first type of the first~~ task and ~~[[ii)]]~~ a second queue configured to receive ~~a second type of the second~~ task.

10. (*Currently Amended*) The computer-program product of claim ~~[[9]]~~ 7, wherein the first ~~type of~~ task comprises a low-latency task and the second ~~type of~~ task comprises a regular-latency task.

11. (*Currently Amended*) The computer-program product of claim ~~[[9]]~~ 7, wherein the first ~~type of~~ task comprises a graphics-processing task and the second ~~type of~~ task comprises a general-compute task.

12. *(Currently Amended)* The computer-program product of claim 7, wherein the ~~processor~~ processing unit further comprises:

a scheduling module ~~that schedules~~ configured to schedule the plurality of tasks to be issued to the shader core based on a priority associated with each of the plurality of tasks.

13. *(Currently Amended)* A computing system ~~[[,]]~~ comprising:

a memory;

a processing unit; and

a bus coupled to the memory and the processing unit,

wherein the processing unit comprises:

a plurality of ~~virtual~~ engines configured to ~~[(i)]~~ receive, from an operating system (OS), a plurality of tasks ~~substantially in parallel with each other and~~ (ii) and to load a set of state data associated with each of the plurality of tasks; and

a shader core configured to receive the plurality of tasks from at least one of the plurality of engines and to execute a first task from the plurality of tasks ~~substantially in parallel while executing a second task from the plurality of tasks~~ based on ~~the set of~~ respective state data associated with each of the ~~plurality of~~ first and second tasks.

14. *(Currently Amended)* The computing system of claim 13, wherein the shader core comprises:

a first plurality of processing elements configured to execute ~~[[a]]~~ the first task based on a first set of state data associated with the first task; and

a second plurality of processing elements configured to execute ~~[[a]]~~ the second task based on a second set of state data associated with the second task.

15. *(Currently Amended)* The computing system of claim 13, wherein the plurality of ~~virtual~~ engines comprises ~~[[i)]]~~ a first queue configured to receive ~~a first type of the first task~~ and ~~[[ii)]]~~ a second queue configured to receive ~~a second type of the second task~~.

16. *(Currently Amended)* The computing system of claim ~~[[15]]~~ 13, wherein the first ~~type of~~ task comprises a low-latency task and the second ~~type of~~ task comprises a regular-latency task.

17. *(Currently Amended)* The computing system of claim ~~[[15]]~~ 13, wherein the first ~~type of~~ task comprises a graphics-processing task and the second ~~type of~~ task comprises a general-compute task.

18. *(Currently Amended)* The computing system of claim 13, wherein the processing unit further comprises:

a scheduling module ~~that schedules~~ configured to schedule the plurality of tasks to be issued to the shader core based on a priority associated with each of the plurality of tasks.

19. (*Currently Amended*) A computer-implemented method for processing tasks in a processing unit, the computer-implemented method comprising:

receiving, from an operating system (OS) with a plurality of engines, a plurality of tasks in parallel with each other;

loading a set of state data associated with each of the plurality of tasks; [[and]]

receiving, with a shader core, the plurality of tasks from at least one of the plurality of engines; and

executing, with the shader core, a first task from the plurality of tasks substantially in parallel in a shader core based on the set of while executing a second task from the plurality of tasks based on state data associated with each of the plurality of first and second tasks.

20. (*Currently Amended*) The computer-implemented method of claim 19, wherein the executing comprises:

executing [[a]] the first task in a first plurality of processing elements of the shader core based on a first set of state data associated with the first task; and

executing [[a]] the second task in a second plurality of processing elements of the shader core based on a second set of state data associated with the second task.

21. (*Currently Amended*) The computer-implemented method of claim 19, wherein the receiving, with the plurality of engines, the plurality of tasks comprises:

queueing a first type of queueing the first task in a first queue; and

queueing a second type queueing the second task in a second queue.

22. *(Currently Amended)* The computer-implemented method of claim [[21]]
19, wherein the first ~~type of~~ task comprises a low-latency task and the second ~~type of~~
task comprises a regular-latency task.

23. *(Currently Amended)* The computer-implemented method of claim [[21]]
19, wherein the first ~~type of~~ task comprises a graphics-processing task and the second
~~type of~~ task comprises a general-compute task.

24. *(Currently Amended)* The computer-implemented method of claim 19,
further comprising:

scheduling the plurality of tasks to be issued to the shader core ~~by using a~~
~~scheduling module of the processing unit based on a priority associated with each of the~~
plurality of tasks.

25. *(Currently Amended)* A computer-implemented method for providing
tasks to a processing unit, the computer-implemented method comprising:

receiving a plurality of tasks from one or more applications, wherein each task
~~includes~~ comprises an indication of a priority type; and

providing, to the processing unit, the plurality of tasks and the indication of the
priority type associated with each task, wherein the processing unit comprises:

a plurality of engines configured to receive the plurality of tasks and to load state
data associated with each of the plurality of tasks; and

a shader core configured to receive the plurality of tasks from at least one of the
plurality of engines and to execute a first task from the plurality of tasks while executing

a second task from the plurality of tasks based respective state data associated with each of the first and second tasks.

26. (New) The processing unit of claim 1, wherein the shader core comprises a plurality of processing elements, wherein each of the processing elements corresponds to a respective engine from the plurality of engines and is configured to execute one or more tasks from its respective engine.

27. (New) The processing unit of claim 1, wherein the shader core comprises a plurality of processing elements, wherein at least one of the processing elements is configured to dedicate a first processing time to the first task and a second processing time to the second task.

Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendments, claims 1-27 are pending in the application, with claims 1, 7, 13, 19 and 25 being the independent claims. Claims 1-25 are sought to be amended. Applicants respectfully reserve the right to prosecute similar or broader claims, with respect to the amended claims, in the future. Claims 26 and 27 are sought to be added. Exemplary support for the new claims can be found in paragraphs [0051] and [0052] of the as-filed specification. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendments and following remarks, Applicants respectfully request that the Examiner reconsider all outstanding rejections and that they be withdrawn.

Rejection Under 35 U.S.C. § 112

Claims 1, 7, 13 and 19 are rejected under 35 U.S.C. § 112(b) or 35 U.S.C. § 112 (pre-AIA), second paragraph, as allegedly being indefinite. Without acquiescing to the propriety of the rejection, these claims have been amended to address the section 112 rejection. Applicants therefore respectfully request that the Examiner reconsider and withdraw the rejection under 35 U.S.C. § 112 and pass claims 1, 7, 13 and 19 to allowance.

Rejection Under 35 U.S.C. § 103

Claims 1-24 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent Appl. Pub. No. 2011/0050712 to Jackson (“Jackson”) in view of U.S. Patent No. 8,345,053 to Jiao et al. (“Jiao”). Applicants respectfully traverse.

Claims 1, 7, 13 and 19 recite features distinguishable over the applied references.

For example, claim 1 recites:

a plurality of engines configured to receive the plurality of tasks and to load state data associated with each of the plurality of tasks; and

a shader core configured to receive the plurality of tasks from at least one of the plurality of engines and to execute a first task from the plurality of tasks while executing a second task from the plurality of tasks based respective state data associated with each of the first and second tasks.

Claims 7, 13 and 19, using their respective language, recite similar distinguishing features. Neither Jackson nor Jiao disclose these features.

Applicants agree with the Examiner that Jackson does not disclose the recited “plurality of engines” of claims 1, 7, 13 and 19. *See* Office Action, p. 4. Jiao does not cure the deficiencies of Jackson.

Rather, in reference to FIG. 2 of Jiao, the Examiner points to flow controller 212, ALU core 220, elementary function core 230 and other internal components of shader core 130 as allegedly disclosing the recited “plurality of engines” of claims 1, 7, 13 and 19. *See* Office Action, p. 5. At the same time, the Examiner also points to shader core 130 as allegedly disclosing the recited “shader core” of claims 1, 7, 13 and 19. *See id.*

The above assertions by the Examiner do not satisfy the claim features of claims 1, 7, 13 and 19. Specifically, claim 1 recites that the “shader core [is] configured to receive the plurality of tasks from at least one of the plurality of engines.” Since the

Examiner points to the internal components of shader core 130 in FIG. 2 of Jiao as allegedly disclosing the recited “plurality of engines,” shader core 130 cannot “receive the plurality of tasks from at least one of the plurality of engines” as required by the claims. This is because the internal components of shader core 130 and shader core 130 are one in the same. Jiao therefore does not teach or suggest the recited “plurality of engines” and “shader core” of claims 1, 7, 13 and 19.

Since Jackson and Jiao do not teach or suggest at least the above-noted distinguishing features, these references cannot be used to establish a *prima facie* case of obviousness for claims 1, 7, 13 and 19. At least based on their dependencies from claims 1, 7, 13 and 19, claims 2-6, 8-12, 14-18 and 20-24 should also be patentable over the applied references, as well as for their respective distinguishing features.

Applicants respectfully request that the Examiner reconsider and withdraw the rejection under 35 U.S.C. § 103 and pass claims 1-24 to allowance.

Rejection Under 35 U.S.C. § 102

Claim 25 is rejected under 35 U.S.C. §102(e) as allegedly being anticipated by Jiao. Applicants respectfully traverse.

Claim 25 recites features distinguishable over the applied reference. For example, claim 25 recites:

a plurality of engines configured to receive the plurality of tasks and to load state data associated with each of the plurality of tasks; and

a shader core configured to receive the plurality of tasks from at least one of the plurality of engines and to execute a first task from the plurality of tasks while executing a second task from the plurality of tasks based respective state data associated with each of the first and second tasks.

These distinguishing features are similar to those recited in claims 1, 7, 13 and 19. Jiao does not teach or suggest these distinguishing features as discussed above.

Applicants respectfully request that the Examiner reconsider and withdraw the rejection under 35 U.S.C. § 102 and pass claim 25 to allowance.

New Claims 26 and 27

Claims 26 and 27 depend from claim 1, which is patentable over the applied references as discussed above. At least based on their dependency from claim 1, claims 26 and 27 should also be patentable over the applied references, as well as for their respective distinguishing features.

Applicants respectfully request that the Examiner pass claims 26 and 27 to allowance.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



Christian A. Camarce
Attorney for Applicants
Registration No. 65,021

Date: October 18, 2013

1100 New York Avenue, N.W.
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1754422_1.DOCX

Electronic Patent Application Fee Transmittal

Application Number:	12874134			
Filing Date:	01-Sep-2010			
Title of Invention:	Processing Unit that Enables Asynchronous Task Dispatch			
First Named Inventor/Applicant Name:	Michael MANTOR			
Filer:	Christian Andy Camarce/Stacy Hill			
Attorney Docket Number:	1972.1540001			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Claims in Excess of 20	1202	2	80	160
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:	Realtek Ex. 1002 Case No. IPR2023-00687			

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				160

Electronic Acknowledgement Receipt

EFS ID:	17167329
Application Number:	12874134
International Application Number:	
Confirmation Number:	6612
Title of Invention:	Processing Unit that Enables Asynchronous Task Dispatch
First Named Inventor/Applicant Name:	Michael MANTOR
Customer Number:	91505
Filer:	Christian Andy Camarce/Stacy Hill
Filer Authorized By:	Christian Andy Camarce
Attorney Docket Number:	1972.1540001
Receipt Date:	18-OCT-2013
Filing Date:	01-SEP-2010
Time Stamp:	14:47:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 160
RAM confirmation Number	1199
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi-Page	Pages

1		19721540001replyfiled10182013.pdf	1630865 73c05cec56ecec0ca732754cee88bb19e764f3ee	yes	15				
	Multipart Description/PDF files in .zip description								
	Document Description		Start	End					
	Miscellaneous Incoming Letter		1	1					
	Amendment/Req. Reconsideration-After Non-Final Reject		2	2					
	Claims		3	10					
	Applicant Arguments/Remarks Made in an Amendment		11	15					
Warnings:									
Information:									
2	Fee Worksheet (SB06)	fee-info.pdf	30365 9ae3cb191b2f1695460116c72f01761201d52332	no	2				
Warnings:									
Information:									
Total Files Size (in bytes):			1661230						
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.									

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October 18, 2013

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 6612
Art Unit 2677
Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Appl. No. 12/874,134; Filing Date: September 1, 2010
For: **Processing Unit that Enables Asynchronous Task Dispatch**
Inventors: MANTOR *et al.*
Our Ref: 1972.1540001

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. Online Credit Card Payment Authorization in the amount of \$160.00 to cover:
\$160.00 Excess claims fee; and
2. Amendment and Reply Under 37 C.F.R. §1.111.

The above-listed documents are filed electronically through EFS-Web.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

A handwritten signature in blue ink, appearing to read 'Christian A. Camarce'.

Christian A. Camarce
Attorney for Applicants
Registration No. 65,021

CAC/smh
Enclosure(s)

1761010_1.DOCX



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/874,134

09/01/2010

Michael MANTOR

1972.1540001

6612

91505 7590 01/14/2014
Sterne, Kessler, Goldstein & Fox P.L.L.C.
1100 New York Avenue N.W.
Washington, DC 20005

EXAMINER

CRAWFORD, JACINTA M

ART UNIT

PAPER NUMBER

2618

MAIL DATE

DELIVERY MODE

01/14/2014

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 12/874,134	Applicant(s) MANTOR ET AL.	
	Examiner JACINTA M. CRAWFORD	Art Unit 2618	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10/18/2013.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-27 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-27 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date ____.
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date ____.
- 4) ☐ Other: ____.

DETAILED ACTION

1. This action is in response to communications: Amendment filed October 18, 2013.
2. Claims 1-27 are pending in this case. Claims 1-25 have been amended. Claims 26 and 27 have been newly added. This action is made FINAL.

Claim Rejections - 35 USC § 103

3. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.
4. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-26 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Jackson (US 2011/0050712) in view of Jiao et al. (US 8,345,053).

As to claim 13, Jackson discloses a computing system comprising:

Art Unit: 2618

a memory (*Figure 2, memory 270*); a processing unit (*Figure 2, host 103*); and a bus coupled to the memory and the processing unit (*as denoted by arrows*), wherein the processing unit comprises a plurality of engines configured to receive, from an operating system (OS), a plurality of commands and translate the commands to be further processed to render an image by the graphics hardware (*i.e. Figure 1, virtual machines 121 with virtual graphics devices 220, Figure 2; see Figure 3*).

Jackson differs from the invention defined in claim 13 in that Jackson does not disclose receive, from an operating system (OS), a plurality of tasks and to load state data associated with each of the plurality of tasks; and a shader core configured to receive the plurality of tasks from at least one of the plurality of engines and to execute a first task from the plurality of tasks while executing a second task from the plurality of tasks based on respective state data associated with each of the first and second tasks.

Jiao et al. disclose a computing system, comprising:

a memory (*i.e. Figure 1, main memory 160*); a processing unit (*i.e. Figure 1, 100*); and a bus coupled to the memory and the processing unit (*i.e. Figure 1 notes arrows which denotes connection/coupling*), wherein a graphics processor (*Figure 1, graphics processor 120*) to receive, from an operating system (OS), a plurality of tasks (*Figure 2 illustrates threads from graphics programs where threads may indicate specific tasks performed, where the threads allow a program to have multiple tasks performed simultaneously by different units, see column 2, lines 21-29; NOTE: Figure 2 notes threads enter through MUX 208 to thread scheduler 210*

Art Unit: 2618

and further distributed by thread scheduler to various hardware units in parallel, which would denote receiving in parallel, column 2, lines 58-62, and column 4, lines 21-23; operating system inherent in computing system) and to load state data associated with each of the plurality of tasks (column 2, lines 21-29 notes the threads may indicate specific tasks performed with a set of one or more instructions, where the instructions indicate specific operations to perform on each thread, column 2, lines 65-66); and a shader core configured to receive the plurality of tasks and to execute a first task from the plurality of tasks while executing a second task from the plurality of tasks based on respective state data associated with each of the first and second tasks (Figure 2, shader 130 notes hardware units/engines to execute tasks in parallel, see column 4, lines 17-19).

Jiao et al. does not disclose the shader core configured to receive the plurality of tasks from at least one of the plurality of engines. However, Jackson illustrates the plurality of virtual machines (*virtual machines 131*) to forward data and commands to graphics processing unit 135 via hypervisor 132. Jiao et al. illustrate its shader core as part of a graphics processor (*Figure 1, graphics processor 120*), and the graphics processor to receive programs and/or threads which indicates tasks and state data to be forwarded to the shader core for execution (note it is well known that Figure 1 is part of a computing system and comprises a host processor/CPU). Therefore, Jackson modified with Jiao et al. would render the multiple virtual machines of Jackson to forward data and commands (or programs and/or threads indicating tasks and state data as noted in Jiao) to graphics processor 120 and further to shader core 130 of Jiao et al.

Art Unit: 2618

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Jiao et al.'s system and also the function of receiving and executing tasks in parallel to enhance the functionality of multitasking and reduce processing time which ultimately enhances the performance of the overall system.

Claims 1, 7, and 19 are similar in scope to claim 13 above, and are therefore rejected under similar rationale.

As to claims 2, 8, 14, and 20, Jackson modified with Jiao et al. disclose the shader core comprises: a first plurality of processing elements configured to execute the first task based on a first set of state data associated with the first task; and a second plurality of processing elements configured to execute the second task based on a second set of state data associated with the second task (*Jiao, Figures 2 and 3 notes various hardware units for performing tasks*).

As to claims 3, 9, 15, and 21, Jackson modified with Jiao et al. disclose the plurality of engines comprises a first queue configured to receive the first task and a second queue configured to receive the second task (*Jackson, Figure 1 illustrates plural virtual machines where the virtual graphics devices receives commands, Figure 3; Jiao, column 4, lines 9-17 notes hardware units to operate independently; line 59-64 notes each hardware unit may include its own instruction decoder*).

Art Unit: 2618

As to claims 4, 10, 16, and 22, Jackson modified with Jiao et al. disclose the first task comprises a low-latency task and the second task comprises a regular-latency task (*Jiao, Figures 2 and 3 illustrates hardware units such as ALU core and elementary function core which may perform general operations, see column 3, lines 5-24, where the texture sampler may perform graphics processing, see column 2, lines 35-40 and column 4, lines 34-40*).

As to claims 5, 11, 17, and 23, Jackson modified with Jiao et al. disclose the first task comprises a graphics-processing task and the second task comprises a general-compute task (*Figures 2 and 3 illustrates hardware units such as ALU core and elementary function core which may perform general operations, see column 3, lines 5-24, where the texture sampler may perform graphics processing, see column 2, lines 35-40 and column 4, lines 34-40*).

As to claims 6, 12, 18, and 24, Jackson modified with Jiao et al. disclose the processing unit further comprises: a scheduling module configured to schedule the plurality of tasks to be issued to the shader core based on a priority associated with each of the plurality of tasks (*Jiao, Figures 2 and 3, thread scheduler 210*).

As to claim 25, Jackson discloses a computer implemented method for providing tasks to a processing unit, the computer-implemented method comprising:
a plurality of engines configured to receive, from an operating system (OS), a plurality of commands and translate the commands to be further processed to render an image by the

Art Unit: 2618

graphics hardware (*i.e. Figure 1, virtual machines 121 with virtual graphics devices 220, Figure 2; see Figure 3*)

Jiao et al. disclose receiving a plurality of tasks from one or more applications, wherein each task comprises an indication of a priority type (*Figure 2 illustrates threads from graphics program where threads may indicate specific tasks performed, where the instructions indicate specific operations to perform on each thread, which can be considered "indicating a priority type," column 2, lines 65-66*); and providing, to the processing unit, the plurality of tasks and the indication of the priority type associated with each task (*Figures 2 and 3 illustrates threads received by MUX and further by thread scheduler to distribute to hardware units as illustrated, column 2, lines 60-62 and column 4, lines 19-28*), wherein the processing unit comprises: a graphics processor (Figure 1, graphics processor 120) configured to receive the plurality of tasks (*Figure 2 illustrates threads from graphics programs where threads may indicate specific tasks performed, where the threads allow a program to have multiple tasks performed simultaneously by different units, see column 2, lines 21-29; NOTE: Figure 2 notes threads enter through MUX 208 to thread scheduler 210 and further distributed by thread scheduler to various hardware units in parallel, which would denote receiving in parallel, column 2, lines 58-62, and column 4, lines 21-23; operating system inherent in computing system*) and to load state data associated with each of the plurality of tasks (*column 2, lines 21-29 notes the threads may indicate specific tasks performed with a set of one or more instructions, where the instructions indicate specific operations to perform on each thread, column 2, lines 65-66*); and a shader core configured to receive the plurality of tasks from at least one of the plurality of engines and to execute a first

Art Unit: 2618

task from the plurality of tasks while executing a second task from the plurality of tasks based on respective state data associated with each of the first and second tasks (*Figure 2, shader 130 notes hardware units/engines to execute tasks in parallel, see column 4, lines 17-19*).

Jiao et al. does not disclose the shader core configured to receive the plurality of tasks from at least one of the plurality of engines. However, Jackson illustrates the plurality of virtual machines (*virtual machines 131*) to forward data and commands to graphics processing unit 135 via hypervisor 132. Jiao et al. illustrate its shader core as part of a graphics processor (*Figure 1, graphics processor 120*), and the graphics processor to receive programs and/or threads which indicates tasks and state data to be forwarded to the shader core for execution (note it is well known that Figure 1 is part of a computing system and comprises a host processor/CPU). Therefore, Jackson modified with Jiao et al. would render the multiple virtual machines of Jackson to forward data and commands (or programs and/or threads indicating tasks and state data as noted in Jiao) to graphics processor 120 and further to shader core 130 of Jiao et al, thus the shader core configured to receive the plurality of tasks from at least one of the plurality of engines.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Jiao et al.'s system and also the function of receiving and executing tasks in parallel to enhance the functionality of multitasking and reduce processing time which ultimately enhances the performance of the overall system.

Art Unit: 2618

As to claim 26, Jackson modified with Jiao et al. disclose the shader core comprises a plurality of processing elements wherein each of the processing elements corresponds to a respective engine from the plurality of engines and is configured to execute one or more tasks from its respective engine (*Jackson, Figure 1 illustrates virtual machines 131 to forward data and commands to graphics processing unit 135 modified with Jiao, Figure 1 illustrates graphics processor 130 to receive programs and/or threads and forward to shader core, i.e. Figures 2 and 3 notes various engines, flow controller 212, ALU core 220, elementary function core 230, etc., part of shader core 130; note it can be noted that respective engines corresponds to respective tasks where Jackson notes each virtual machine may include a virtual graphics device and receive commands to render a scene, [0022] thru [0025] and Jiao notes some processing elements of the shader core may be task specific,*).

6. Claim 27 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Jackson (US 2011/0050712) in view of Jiao et al. (US 8,345,053) as applied to claim 1 above, and further in view of Miller et al. (US 2009/0109230).

As to claim 27, Jackson modified with Jiao et al. disclose the shader core comprises a plurality of processing elements (*Jiao, i.e. Figures 2 and 3 notes various engines, flow controller 212, ALU core 220, elementary function core 230, etc., part of shader core 130*), but does not disclose wherein at least one of the processing elements is configured to dedicate a first processing time to the first task and a second processing time to the second task.

However, Miller et al. disclose at least one of the processing element is configured to dedicate a first processing time to the first task and a second processing time to the second task (*Figure 4 illustrates how a task is may be executed by each processor, see associated text*).

It would have been obvious to one of ordinary skill in the art at the time of the invention to consider the processing time of tasks since each task may be different and require different capabilities, i.e. power and performance, as noted in Miller et al. to appropriately execute each task in a plural processing system.

Response to Arguments

7. Applicant's arguments filed October 18, 2013 have been fully considered but they are not persuasive. Applicant amends independent claims 1, 7, 13, 19, and 25 to recite the limitations or similar limitations, “ a plurality of engines configured to receive the plurality of tasks and to load state data associated with each of the plurality of tasks; and a shader core configured to receive the plurality of tasks from at least one of the plurality of engines and to execute a first task from the plurality of tasks while executing a second task from the plurality of tasks based on respective state data associated with each of the first and second tasks” (claim 1). Applicant argues on pages 11-13 of the amendment filed that the prior art cited does not disclose the limitations of the claims, more specifically, in the previous rejection, the Examiner notes the plurality of engines to be part of shader core of Jiao and “since the Examiner points to the

Art Unit: 2618

internal components of shader core 130 in FIG. 2 of Jiao as allegedly disclosing the recited “plurality of engines,” shader core 130 cannot “receive the plurality of tasks from at least one of the plurality of engines” as required by the claims. This is because the internal components of shader core 130 and shader core 130 are one in the same” (last paragraph of page 11 and first paragraph of 12). However, the Examiner modifies the rejection in light of the amendments to note that the virtual machines of Jackson are noted as the plurality of engines and how is it modified with Jiao to incorporate the shader core, thus teaching the limitations as recited. Please see the rejection and notes above.

8. Applicant also argues on page 13 regarding newly added claims 26 and 27. Please see the rejection and notes above.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

Art Unit: 2618

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Taylor et al. (US 2003/0030643) disclose a system and method of forwarding state data to a shader engine via a plurality of memories.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JACINTA M. CRAWFORD whose telephone number is (571)270-1539. The examiner can normally be reached on M-F 8:00a.m. - 5:00p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Zarka can be reached on (571)270-1578. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2618

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JACINTA M CRAWFORD/
Primary Examiner, Art Unit 2618

Notice of References Cited	Application/Control No. 12/874,134		Applicant(s)/Patent Under Reexamination MANTOR ET AL.	
	Examiner JACINTA M. CRAWFORD		Art Unit 2618	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-8,284,205	10-2012	Miller et al.	345/502
*	B	US-2003/0030643	02-2003	Taylor et al.	345/531
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes 	Application/Control No. 12874134	Applicant(s)/Patent Under Reexamination MANTOR ET AL.
	Examiner JACINTA M CRAWFORD	Art Unit 2618

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
345	502, 505	7/14/2013	JMC
718	102, 103	7/14/2013	JMC
345	501	1/11/2014	JMC
	EAST updated search	1/11/2014	JMC

SEARCH NOTES		
Search Notes	Date	Examiner
EAST; Inventor and Assignee search	7/14/2013	JMC
NPL search	7/14/2013	JMC
EAST updated search	1/11/2014	JMC
NPL updated search	1/11/2014	JMC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

	/JACINTA M CRAWFORD/ Primary Examiner.Art Unit 2618
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	5	("20110050712" "8345053").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/11 14:26
S2	1466	(load\$4 near3 (state near data))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/11 14:38
S3	198179	"345"/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/11 14:38
S4	45	S2 and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/11 14:38
S5	8	("6252600" "20080109810" "20090160867").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/11 15:02
S6	5	"20090109230"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/11 15:49

EAST Search History (Interference)

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<i>Index of Claims</i> 	Application/Control No. 12874134	Applicant(s)/Patent Under Reexamination MANTOR ET AL.
	Examiner JACINTA M CRAWFORD	Art Unit 2677

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	07/14/2013	01/11/2014						
	1	✓	✓						
	2	✓	✓						
	3	✓	✓						
	4	✓	✓						
	5	✓	✓						
	6	✓	✓						
	7	✓	✓						
	8	✓	✓						
	9	✓	✓						
	10	✓	✓						
	11	✓	✓						
	12	✓	✓						
	13	✓	✓						
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	16	✓	✓						
	17	✓	✓						
	18	✓	✓						
	19	✓	✓						
	20	✓	✓						
	21	✓	✓						
	22	✓	✓						
	23	✓	✓						
	24	✓	✓						
	25	✓	✓						
	26		✓						
	27		✓						

**Amendment Under 37 C.F.R. § 1.116
Expedited Procedure – Art Unit 2618**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

MANTOR et al.

Appl. No.: 12/874,134

Filed: September 1, 2010

For: **Processing Unit That Enables
Asynchronous Task Dispatch**

Confirmation No.: 6612

Art Unit: 2618

Examiner: Crawford, Jacinta M.

Atty. Docket: 1972.1540001

Amendment and Reply Under 37 C.F.R. § 1.116

Mail Stop AF

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

In reply to the Final Office Action dated January 14, 2014 (“Final Office Action”), Applicants submit the following Amendment and Remarks.

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (*Currently Amended*) ~~A processing unit~~ An apparatus comprising:

a plurality of engines associated with a first processing unit and configured to receive, from ~~an operating system (OS)~~ a scheduling module associated with a second processing unit, a plurality of tasks and to load state data associated with each of the plurality of tasks; and

a shader core associated with the first processing unit and configured to receive the plurality of tasks from at least one of the plurality of engines and to execute a first task from the plurality of tasks while executing a second task from the plurality of tasks based on respective state data associated with each of the first and second tasks.

2. (*Currently Amended*) The ~~processing unit apparatus~~ of claim 1, wherein the shader core comprises:

a first plurality of processing elements configured to execute the first task based on a first set of state data associated with the first task; and

a second plurality of processing elements configured to execute the second task based on a second set of state data associated with the second task.

3. (*Currently Amended*) The ~~processing unit apparatus~~ of claim 1, wherein the plurality of engines comprises a first queue configured to receive the first task and a second queue configured to receive the second task.

4. *(Currently Amended)* The ~~processing unit~~ apparatus of claim 1, wherein the first task comprises a low-latency task and the second task comprises a regular-latency task.

5. *(Currently Amended)* The ~~processing unit~~ apparatus of claim 1, wherein the first task comprises a graphics-processing task and the second task comprises a general-compute task.

6. *(Currently Amended)* The ~~processing unit~~ apparatus of claim 1, ~~further comprising: a scheduling module configured to schedule the plurality of tasks to be issued to~~ wherein the shader core is configured to receive the plurality of tasks based on a priority associated with each of the plurality of tasks.

7. *(Currently Amended)* A computer-program product comprising a computer-readable storage medium containing instructions that, if executed on a computing device, define ~~a processing unit~~ an apparatus comprising:

a plurality of engines associated with a first processing unit and configured to receive, from ~~an operating system (OS)~~ a scheduling module associated with a second processing unit, a plurality of tasks and to load state data associated with each of the plurality of tasks; and

a shader core associated with the first processing unit and configured to receive the plurality of tasks from at least one of the plurality of engines and to execute a first task from the plurality of tasks while executing a second task from the plurality of tasks based on respective state data associated with each of the first and second tasks.

8. *(Previously Presented)* The computer-program product of claim 7, wherein the shader core comprises:

 a first plurality of processing elements configured to execute the first task based on a first set of state data associated with the first task; and

 a second plurality of processing elements configured to execute the second task based on a second set of state data associated with the second task.

9. *(Previously Presented)* The computer-program product of claim 7, wherein the plurality of engines comprises a first queue configured to receive the first task and a second queue configured to receive the second task.

10. *(Previously Presented)* The computer-program product of claim 7, wherein the first task comprises a low-latency task and the second task comprises a regular-latency task.

11. *(Previously Presented)* The computer-program product of claim 7, wherein the first task comprises a graphics-processing task and the second task comprises a general-compute task.

12. *(Currently Amended)* The computer-program product of claim 7, wherein ~~the processing unit further comprises a scheduling module configured to schedule the plurality of tasks to be issued to the shader core~~ is configured to receive the plurality of tasks based on a priority associated with each of the plurality of tasks.

13. (*Currently Amended*) A computing system comprising:

a memory;

a first processing unit; and

a bus coupled to the memory and the first processing unit, wherein the first processing unit comprises:

a plurality of engines configured to receive, from an ~~operating system~~
(~~OS~~) a scheduling module associated with a second processing unit, a plurality of tasks and to load state data associated with each of the plurality of tasks; and

a shader core configured to receive the plurality of tasks from at least one of the plurality of engines and to execute a first task from the plurality of tasks while executing a second task from the plurality of tasks based on respective state data associated with each of the first and second tasks.

14. (*Previously Presented*) The computing system of claim 13, wherein the shader core comprises:

a first plurality of processing elements configured to execute the first task based on a first set of state data associated with the first task; and

a second plurality of processing elements configured to execute the second task based on a second set of state data associated with the second task.

15. (*Previously Presented*) The computing system of claim 13, wherein the plurality of engines comprises a first queue configured to receive the first task and a second queue configured to receive the second task.

16. *(Currently Amended)* The computing system of claim 13, wherein the first task comprises a low-latency task and the second task comprises a regular-latency task.

17. *(Previously Presented)* The computing system of claim 13, wherein the first task comprises a graphics-processing task and the second task comprises a general-compute task.

18. *(Currently Amended)* The computing system of claim 13, wherein ~~the processing unit further comprises a scheduling module configured to schedule the plurality of tasks to be issued to the shader core~~ is configured to receive the plurality of tasks based on a priority associated with each of the plurality of tasks.

19. *(Currently Amended)* A computer-implemented method ~~for processing tasks in a processing unit, the computer-implemented method comprising:~~

receiving, with a plurality of engines associated with a first processing unit, a plurality of tasks, wherein the plurality of engines receive the plurality of tasks from a scheduling module associated with a second processing unit;

loading state data associated with each of the plurality of tasks;

receiving, with a shader core associated with the first processing unit, the plurality of tasks from at least one of the plurality of engines; and

executing, with the shader core, a first task from the plurality of tasks while executing a second task from the plurality of tasks based on state data associated with each of the first and second tasks.

20. *(Previously Presented)* The computer-implemented method of claim 19, wherein the executing comprises:

executing the first task in a first plurality of processing elements of the shader core based on a first set of state data associated with the first task; and

executing the second task in a second plurality of processing elements of the shader core based on a second set of state data associated with the second task.

21. *(Previously Presented)* The computer-implemented method of claim 19, wherein the receiving, with the plurality of engines, the plurality of tasks comprises:

queuing the first task in a first queue; and

queuing the second task in a second queue.

22. *(Previously Presented)* The computer-implemented method of claim 19, wherein the first task comprises a low-latency task and the second task comprises a regular-latency task.

23. *(Previously Presented)* The computer-implemented method of claim 19, wherein the first task comprises a graphics-processing task and the second task comprises a general-compute task.

24. *(Currently Amended)* The computer-implemented method of claim 19, ~~further comprising scheduling the plurality of tasks to be issued to the shader core~~
wherein the receiving, with the shader core, the plurality of tasks from the at least one of

the plurality of engines comprises receiving, with the shader core, the plurality of tasks
based on a priority associated with each of the plurality of tasks.

25. *(Currently Amended)* A computer-implemented method ~~for providing tasks to a processing unit, the computer-implemented method~~ comprising:

receiving, from a first processing unit, a plurality of tasks from one or more applications, wherein each task comprises an indication of a priority type; and

providing, to ~~[[the]]~~ a second processing unit, the plurality of tasks and the indication of the priority type associated with each task, wherein the second processing unit comprises:

a plurality of engines configured to receive the plurality of tasks and to load state data associated with each of the plurality of tasks; and

a shader core configured to receive the plurality of tasks from at least one of the plurality of engines and to execute a first task from the plurality of tasks while executing a second task from the plurality of tasks based respective state data associated with each of the first and second tasks.

26. *(Currently Amended)* The ~~processing unit apparatus~~ of claim 1, wherein the shader core comprises a plurality of processing elements, wherein each of the processing elements corresponds to a respective engine from the plurality of engines and is configured to execute one or more tasks from its respective engine.

27. *(Currently Amended)* The ~~processing unit apparatus~~ of claim 1, wherein the shader core comprises a plurality of processing elements, wherein at least one of the

processing elements is configured to dedicate a first processing time to the first task and a second processing time to the second task.

Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendments, claims 1-27 are pending in the application, with claims 1, 7, 13, 19 and 25 being the independent claims. Claims 1-7, 12, 13, 16, 18, 19 and 24-27 are sought to be amended. Applicants respectfully reserve the right to prosecute similar or broader claims, with respect to the amended claims, in the future. These changes are believed to introduce no new matter, and their entry is respectfully requested.

This reply should be entered after final rejection because it does not require further search or consideration and because it places the application in condition for allowance or better condition for appeal.

Based on the above amendments and following remarks, Applicants respectfully request that the Examiner reconsider all outstanding rejections and that they be withdrawn.

Rejections Under 35 U.S.C. § 103

Proposed Combination of Jackson and Jiao

Claims 1-26 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent Appl. Pub. No. 2011/0050712 to Jackson ("Jackson") in view of U.S. Patent No. 8,345,053 to Jiao et al. ("Jiao"). Applicants respectfully traverse.

Without acquiescing to the propriety of the rejection, claims 1, 7, 13, 19 and 25 have been amended to clarify features distinguishable over the applied references. For example, claim 1 recites:

a plurality of engines associated with a first processing unit and configured to receive, *from a scheduling module associated with a second processing unit*, a plurality of tasks and to load state data associated with each of the plurality of tasks; and

a shader core associated with the first processing unit and configured to receive the plurality of tasks from at least one of the plurality of engines and to execute a first task from the plurality of tasks while executing a second task from the plurality of tasks based on respective state data associated with each of the first and second tasks.

Emphasis added.

Claims 7, 13, 19 and 25 recite similar distinguishing features. Neither Jackson nor Jiao disclose these features.

Applicants agree with the Examiner in that

“Jackson differs from the invention defined in claim 13 in that Jackson does not disclose receive, from an operating system (OS), a plurality of tasks and to load state data associated with each of the plurality of tasks; and a shader core configured to receive the plurality of tasks from at least one of the plurality of engines and to execute a first task from the plurality of tasks while executing a second task from the plurality of tasks based on respective data associated with each of the first and second tasks.”

Final Office Action, p. 3, emphasis in original.

Jiao does not cure the deficiencies of Jackson.

Jiao discloses a graphics processor with parallel scheduling and execution of threads. *See* Jiao, Title. In referring to FIG. 2 of Jiao (reproduced below), Jiao states that “[w]ithin shader core 130, a multiplexer (Mux) 208 receives threads from programs 110a through 110n and provides these threads to a thread scheduler 210. Thread scheduler 210 performs various functions to schedule and manage execution of the threads . . .” *Id.*, 2:58-62. In particular, “[t]hread scheduler 210 may determine which hardware unit to use for each instruction . . . Thread scheduler 210 may then issue different instructions to

different hardware units for execution in parallel, which may significantly increase throughput.” *Id.*, 4:19-23. In other words, thread scheduler 210 is within shader core 130 and issues instructions to hardware units that are also within shader core 130. Thread scheduler 210 and the hardware units are not associated with different processing units; rather, they are associated with the same processing unit—namely, shader core 130. Jiao therefore does not teach or suggest “***a shader core associated with the first processing unit and configured to receive the plurality of tasks from at least one of the plurality of engines . . .***,” in which the plurality of engines are “associated with a first processing unit and configured to receive, ***from a scheduling module associated with a second processing unit***, a plurality of tasks and to load state data associated with each of the plurality of tasks,” as recited in claim 1 (emphasis added) and similarly-recited in claims 7, 13, 19 and 25.

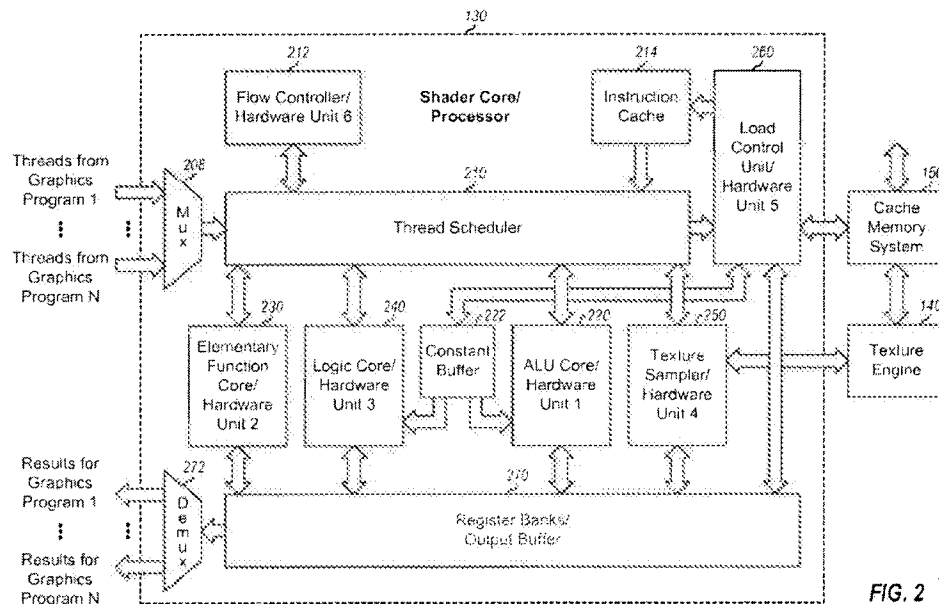


FIG. 2 of Jiao

Since Jackson and Jiao do not teach or suggest at least the above-noted distinguishing features, these references cannot be used to establish a *prima facie* case of

obviousness for claims 1, 7, 13, 19 and 25. At least based on their dependencies from claims 1, 7, 13 and 19, claims 2-6, 8-12, 14-18, 20-24 and 26 should also be patentable over the applied references, as well as for their respective distinguishing features.

Proposed Combination of Jackson, Jiao and Miller

Claim 27 is rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Jackson in view of Jiao, as applied to claim 1, and further in view of U.S. Patent Appl. Pub. No. 2009/0109230 to Miller et al. ("Miller"). Applicants respectfully traverse.

Miller is not used by the Examiner, nor does it teach or suggest, the above-noted distinguishing features of claim 1. Since the applied references do not teach or suggest at least the above-noted distinguishing features, these references cannot be used to establish a *prima facie* case of obviousness for claim 1. At least based on its dependency from claim 1, claim 27 should also be patentable over the applied references, as well as for its respective distinguishing features.

In view of the above, Applicants respectfully request that the Examiner reconsider and withdraw the rejections under 35 U.S.C. § 103 and pass claims 1-27 to allowance.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the

Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



Christian A. Camarce
Attorney for Applicants
Registration No. 65,021

Date: MARCH 13, 2014

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

1813959_1.DOCX

Electronic Acknowledgement Receipt

EFS ID:	18463613
Application Number:	12874134
International Application Number:	
Confirmation Number:	6612
Title of Invention:	Processing Unit that Enables Asynchronous Task Dispatch
First Named Inventor/Applicant Name:	Michael MANTOR
Customer Number:	91505
Filer:	Christian Andy Camarce/Maya Bennett
Filer Authorized By:	Christian Andy Camarce
Attorney Docket Number:	1972.1540001
Receipt Date:	13-MAR-2014
Filing Date:	01-SEP-2010
Time Stamp:	16:36:07
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		19721540001amendment.pdf	1700950 8b69a1ef9fc1599d9494929b8f9242c5b30f196d	yes	15

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Transmittal Letter	1	1
	Response After Final Action	2	2
	Claims	3	10
	Applicant Arguments/Remarks Made in an Amendment	11	15

Warnings:

Information:

Total Files Size (in bytes):	1700950
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

CHRISTIAN A. CAMARCE
ASSOCIATE
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CCAMARCE@SKGF.COM



March 13, 2014

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 6612
Art Unit 2618
Attn: Mail Stop AF

Re: U.S. Utility Patent Application
Appl. No. 12/874,134; Filing Date: September 1, 2010
For: **Processing Unit that Enables Asynchronous Task Dispatch**
Inventors: MANTOR *et al.*
Our Ref: 1972.1540001

Commissioner:

Transmitted herewith for appropriate action is an **Amendment and Reply under 37 C.F.R. § 1.116**.

The above-listed document is filed electronically through EFS-Web.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

A handwritten signature in black ink, appearing to read 'Christian A. Camarce'.

Christian A. Camarce
Attorney for Applicants
Registration No. 65,021

CAC:mlb
Enclosure

1824998_1

Realtek Ex. 1002

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/874,134	Filing Date 09/01/2010	☐ To be Mailed
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO**APPLICATION AS FILED – PART I**

(Column 1)

(Column 2)

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	03/13/2014	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 27	Minus	** 27	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 5	Minus	*** 5	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/ALLYSON PURNELL/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2. Realtek Ex. 1002

Case No. IPR2023-00687

Page 189 of 228



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/874,134

09/01/2010

Michael MANTOR

1972.1540001

6612

91505 7590 04/01/2014
Sterne, Kessler, Goldstein & Fox P.L.L.C.
1100 New York Avenue N.W.
Washington, DC 20005

EXAMINER

CRAWFORD, JACINTA M

ART UNIT

PAPER NUMBER

2618

MAIL DATE

DELIVERY MODE

04/01/2014

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	Application No. 12/874,134	Applicant(s) MANTOR ET AL.	
	Examiner JACINTA M. CRAWFORD	Art Unit 2618	AIA (First Inventor to File) Status No

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 13 March 2014 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.
NO NOTICE OF APPEAL FILED

1. ☒ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance;
(2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:

a) ☐ The period for reply expires _____ months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection. The current period for reply expires _____ months from the mailing date of the prior Advisory Action or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.

Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANT'S FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because

a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);

b) ☐ They raise the issue of new matter (see NOTE below);

c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).

5. ☐ Applicant's reply has overcome the following rejection(s): _____.

6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

7. ☒ For purposes of appeal, the proposed amendment(s): (a) ☒ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

9. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).

10. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

11. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

12. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:
Applicants amend independent claims 1, 7, 13, 19, and 25. Applicants argue on pages 10-14 that the prior art cited does not teach or suggest the limitations of the newly amended claims. However, these claims would require further consideration and search since the limitations were not previously presented.

13. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____

14. ☐ Other: _____.

STATUS OF CLAIMS

15. The status of the claim(s) is (or will be) as follows:
Claim(s) allowed: _____
Claim(s) objected to: _____
Claim(s) rejected: 1-27

**Amendment Under 37 C.F.R. § 1.116
Expedited Procedure – Art Unit 2618**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

MANTOR et al.

Appl. No.: 12/874,134

Filed: September 1, 2010

For: **Processing Unit That Enables
Asynchronous Task Dispatch**

Confirmation No.: 6612

Art Unit: 2618

Examiner: Crawford, Jacinta M.

Atty. Docket: 1972.1540001

Amendment and Reply Under 37 C.F.R. § 1.116

Mail Stop AF

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Do not enter
3/24/2014 JC

Commissioner:

In reply to the Final Office Action dated January 14, 2014 (“Final Office Action”), Applicants submit the following Amendment and Remarks.

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Request for Continued Examination (RCE) Transmittal

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	12/874,134
Filing Date	September 1, 2010
First Named Inventor	Michael MANTOR
Art Unit	2677
Examiner Name	Tung, Kee M.
Attorney Docket Number	1972.1540001

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. **Submission required under 37 CFR 1.114** Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

a. ☒ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

ii. ☒ Other enter Amendment and Reply Under 1.116 previously filed on March 13, 2014

b. ☐ Enclosed

i. ☐ Amendment/Reply

iii. ☐ Information Disclosure Statement (IDS)

ii. ☐ Affidavit(s)/ Declaration(s)

iv. ☐ Other _____

2. Miscellaneous

a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

b. ☐ Other _____

3. Fees

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to

a. ☒ Deposit Account No. 19-0036

i. ☒ RCE fee required under 37 CFR 1.17(e)

ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)

iii. ☐ Other _____

b. ☐ Check in the amount of \$ _____ enclosed

c. ☒ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature	<i>Christian A. Camarce</i>	Date	<u>APRIL 14, 2014</u>
Name (Print/Type)	Christian A. Camarce	Registration No.	65,021

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature		Date	
Name (Print/Type)			

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2. **Realtek Ex. 1002**

Case No. IPR2023-00687

Page 193 of 228

Electronic Patent Application Fee Transmittal

Application Number:	12874134			
Filing Date:	01-Sep-2010			
Title of Invention:	Processing Unit that Enables Asynchronous Task Dispatch			
First Named Inventor/Applicant Name:	Michael MANTOR			
Filer:	Christian Andy Camarce/Stacy Hill			
Attorney Docket Number:	1972.1540001			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for Continued Examination	1801	1	1200	1200
Total in USD (\$)				1200

Electronic Acknowledgement Receipt

EFS ID:	18753108
Application Number:	12874134
International Application Number:	
Confirmation Number:	6612
Title of Invention:	Processing Unit that Enables Asynchronous Task Dispatch
First Named Inventor/Applicant Name:	Michael MANTOR
Customer Number:	91505
Filer:	Christian Andy Camarce/Stacy Hill
Filer Authorized By:	Christian Andy Camarce
Attorney Docket Number:	1972.1540001
Receipt Date:	14-APR-2014
Filing Date:	01-SEP-2010
Time Stamp:	14:21:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1200
RAM confirmation Number	572
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi-Page	Pages

Realtek Ex-1002
MessageID: 2013-09-06 14:21:22
Case No: 2013-09-06 14:21:22
Pages: 1002
If appl.)

1		19721540001rce.pdf	104524 3aa11f2545cb21470577a08f1a0a9f2f8d2e679c	yes	2
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Miscellaneous Incoming Letter		1	1	
	Request for Continued Examination (RCE)		2	2	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30306 d662b029feb8bedba2563a4a38a0704d85a4d53	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			134830		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

CHRISTIAN A. CAMARCE
ASSOCIATE
(202) 772-8895
CCAMARCE@SKGF.COM



April 14, 2014

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 6612
Art Unit 2618
Attn: Mail Stop RCE

Re: U.S. Utility Patent Application
Appl. No. 12/874,134; Filing Date: September 1, 2010
For: **Processing Unit that Enables Asynchronous Task Dispatch**
Inventors: MANTOR *et al.*
Our Ref: 1972.1540001

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. Online Credit Card Payment Authorization in the amount of \$1,200.00 to cover:
\$1,200.00 Request for Continued Examination fee; and
2. Request for Continued Examination Request (RCE) Transmittal.

The above-listed documents are filed electronically through EFS-Web.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

A handwritten signature in cursive script that reads "Christian A. Camarce".

Christian A. Camarce
Attorney for Applicants
Registration No. 65,021

CAC/smh
Enclosure(s)

1838040_1.DOCX

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/874,134	Filing Date 09/01/2010	☐ To be Mailed
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO**APPLICATION AS FILED – PART I**

(Column 1)

(Column 2)

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	04/14/2014	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 27	Minus	** 27	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 5	Minus	***5	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
TOTAL ADD'L FEE						0	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
TOTAL ADD'L FEE						

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/DENISE HOPKINS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2. **Realtek Ex. 1002****Case No. IPR2023-00687****Page 199 of 228**

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/874,134	Filing Date 09/01/2010	☐ To be Mailed
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

(Column 1)

(Column 2)

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	04/14/2014	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 27	Minus	** 27	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 5	Minus	*** 5	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
TOTAL ADD'L FEE						0	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
TOTAL ADD'L FEE						

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/DENISE HOPKINS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2. **Realtek Ex. 1002**

Case No. IPR2023-00687

Page 200 of 228



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

91505 7590 05/22/2014
Sterne, Kessler, Goldstein & Fox P.L.L.C.
1100 New York Avenue N.W.
Washington, DC 20005

EXAMINER

CRAWFORD, JACINTA M

ART UNIT

PAPER NUMBER

2618

DATE MAILED: 05/22/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/874,134

09/01/2010

Michael MANTOR

1972.1540001

6612

TITLE OF INVENTION: PROCESSING UNIT THAT ENABLES ASYNCHRONOUS TASK DISPATCH

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	08/22/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

91505 7590 05/22/2014
Sterne, Kessler, Goldstein & Fox P.L.L.C.
1100 New York Avenue N.W.
Washington, DC 20005

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/874,134	09/01/2010	Michael MANTOR	1972.1540001	6612

TITLE OF INVENTION: PROCESSING UNIT THAT ENABLES ASYNCHRONOUS TASK DISPATCH

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	08/22/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
CRAWFORD, JACINTA M	2618	345-505000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached. ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.	2. For printing on the patent front page, list (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 1 _____ 2 _____ 3 _____
---	---

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE _____ (B) RESIDENCE: (CITY and STATE OR COUNTRY) _____

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted: ☐ Issue Fee ☐ Publication Fee (No small entity discount permitted) ☐ Advance Order - # of Copies _____	4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above) ☐ A check is enclosed. ☐ Payment by credit card. Form PTO-2038 is attached. ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).
---	---

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

Realtex Ex. 1002



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/874,134	09/01/2010	Michael MANTOR	1972.1540001	6612
91505	7590	05/22/2014	EXAMINER	
Sterne, Kessler, Goldstein & Fox P.L.L.C. 1100 New York Avenue N.W. Washington, DC 20005			CRAWFORD, JACINTA M	
			ART UNIT	PAPER NUMBER
			2618	
DATE MAILED: 05/22/2014				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 12/874,134	Applicant(s) MANTOR ET AL.	
	Examiner JACINTA M. CRAWFORD	Art Unit 2618	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 4/14/2014.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-27. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|---|
| 1. ☐ Notice of References Cited (PTO-892) | 5. ☐ Examiner's Amendment/Comment |
| 2. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ | 6. ☐ Examiner's Statement of Reasons for Allowance |
| 3. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 7. ☐ Other _____. |
| 4. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____. | |

/JACINTA M CRAWFORD/
Primary Examiner, Art Unit 2618



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UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
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 P.O. Box 1450
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BIB DATA SHEET

CONFIRMATION NO. 6612

SERIAL NUMBER 12/874,134	FILING or 371(c) DATE 09/01/2010 RULE	CLASS 345	GROUP ART UNIT 2618	ATTORNEY DOCKET NO. 1972.1540001	
APPLICANTS INVENTORS Michael MANTOR, Orlando, FL; Rex McCrary, Oviedo, FL; ** CONTINUING DATA ***** This appln claims benefit of 61/239,712 09/03/2009 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 09/21/2010					
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /JACINTA M Acknowledged CRAWFORD/ Examiner's Signature	☐ Met after Allowance JC Initials	STATE OR COUNTRY FL	SHEETS DRAWINGS 6	TOTAL CLAIMS 25	INDEPENDENT CLAIMS 5
ADDRESS Sterne, Kessler, Goldstein & Fox P.L.L.C. 1100 New York Avenue N.W. Washington, DC 20005 UNITED STATES					
TITLE Processing Unit that Enables Asynchronous Task Dispatch					
FILING FEE RECEIVED 2080	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	5	("20110050712" "8345053").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/05/18 12:25
S2	2423	345/426.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/05/18 13:00
S3	4398	(shader and parallel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/05/18 13:01
S4	409	S2 and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/05/18 13:01
S5	1247	S3 and schedul\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/05/18 13:01
S6	83	S2 and S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/05/18 13:03
S7	982	345/505.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/05/19 08:33
S8	4398	(shader and parallel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/05/19 08:33
S9	196	S7 and S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/05/19 08:33
S10	68	S9 and schedul\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/05/19 08:34
S11	2180	345/501.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/05/19 08:34
S12	188	S8 and S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/05/19 08:34
S13	55	S12 and schedul\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/05/19 08:34

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S14	3	(shader same schedul\$4 same parallel).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/05/19 09:28

5/ 19/ 2014 9:28:38 AM
C:\Users\jcrowford1\Documents\EAST\Workspaces\12874134c.wsp

Issue Classification 	Application/Control No. 12874134	Applicant(s)/Patent Under Reexamination MANTOR ET AL.	
	Examiner JACINTA M CRAWFORD	Art Unit 2618	

CPC						
Symbol					Type	Version
G06F		9		5066	I	2013-01-01
G06F		9		5027	F	2013-01-01
G06T		15		005	I	2013-01-01
G06T		1		20	I	2013-01-01
G06F		9		5061	I	2013-01-01

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version

NONE		Total Claims Allowed: 27	
(Assistant Examiner)	(Date)		
/JACINTA M CRAWFORD/ Primary Examiner.Art Unit 2618	05/19/2014	O.G. Print Claim(s) 1	O.G. Print Figure 2
(Primary Examiner)	(Date)		

Issue Classification 	Application/Control No. 12874134	Applicant(s)/Patent Under Reexamination MANTOR ET AL.
	Examiner JACINTA M CRAWFORD	Art Unit 2618

☐ Claims renumbered in the same order as presented by applicant															
☐ CPA															
☐ T.D.															
☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	19	17												
2	2	20	18												
3	3	21	19												
4	4	22	20												
5	5	23	21												
6	6	24	22												
9	7	25	23												
10	8	26	24												
11	9	27	25												
12	10	7	26												
13	11	8	27												
14	12														
15	13														
16	14														
17	15														
18	16														

NONE	Total Claims Allowed: 27	
(Assistant Examiner)	(Date)	
/JACINTA M CRAWFORD/ Primary Examiner.Art Unit 2618	05/19/2014	O.G. Print Claim(s) 1
(Primary Examiner)	(Date)	O.G. Print Figure 2

Search Notes 	Application/Control No. 12874134	Applicant(s)/Patent Under Reexamination MANTOR ET AL.
	Examiner JACINTA M CRAWFORD	Art Unit 2618

CPC- SEARCHED		
Symbol	Date	Examiner
G06F 15/00, 15/16-161, 15/80-8092; G06T 1/00-0092	5/19/2014	JMC

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
345	502, 505	7/14/2013	JMC
718	102, 103	7/14/2013	JMC
345	501	1/11/2014	JMC
	EAST updated search	1/11/2014	JMC
	EAST updated search	5/19/2014	JMC

SEARCH NOTES		
Search Notes	Date	Examiner
EAST; Inventor and Assignee search	7/14/2013	JMC
NPL search	7/14/2013	JMC
EAST updated search	1/11/2014	JMC
NPL updated search	1/11/2014	JMC
EAST updated search	5/19/2014	JMC
NPL updated search	5/19/2014	JMC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	see EAST search	5/19/2014	JMC

	/JACINTA M CRAWFORD/ Primary Examiner.Art Unit 2618
--	--

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

91505 7590 05/22/2014
 Sterne, Kessler, Goldstein & Fox P.L.L.C.
 1100 New York Avenue N.W.
 Washington, DC 20005

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/874,134	09/01/2010	Michael MANTOR	1972.1540001	6612

TITLE OF INVENTION: PROCESSING UNIT THAT ENABLES ASYNCHRONOUS TASK DISPATCH

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	08/22/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
CRAWFORD, JACINTA M	2618	345-505000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 **Sterne, Kessler,**
 2 **Goldstein & Fox PLLC**
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

Advanced Micro Devices, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Sunnyvale, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☒ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number **19-0036** (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
☐ Applicant asserting small entity status. See 37 CFR 1.27
☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
 NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature Christian Camarce

Date AUGUST 19, 2014

Typed or printed name **Christian Camarce**

Registration No. **65,021**

Electronic Patent Application Fee Transmittal

Application Number:	12874134			
Filing Date:	01-Sep-2010			
Title of Invention:	PROCESSING UNIT THAT ENABLES ASYNCHRONOUS TASK DISPATCH			
First Named Inventor/Applicant Name:	Michael MANTOR			
Filer:	Christian Andy Camarce/Stacy Hill			
Attorney Docket Number:	1972.1540001			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960
Extension-of-Time:	Realtek Ex. 1002 Case No. IPR2023-00687			

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt

EFS ID:	19897956
Application Number:	12874134
International Application Number:	
Confirmation Number:	6612
Title of Invention:	PROCESSING UNIT THAT ENABLES ASYNCHRONOUS TASK DISPATCH
First Named Inventor/Applicant Name:	Michael MANTOR
Customer Number:	91505
Filer:	Christian Andy Camarce
Filer Authorized By:	
Attorney Docket Number:	1972.1540001
Receipt Date:	19-AUG-2014
Filing Date:	01-SEP-2010
Time Stamp:	09:50:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		19721540001.pdf	109361 dabad5721f960a2f6470e6bfa128684ebfbc7642	yes	2

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Miscellaneous Incoming Letter	1	1
	Issue Fee Payment (PTO-85B)	2	2

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30465	no	2
			2fd3c233daae61a8b3e646bb321252f94c20cc66		

Warnings:

Information:

Total Files Size (in bytes):			139826
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

CHRISTIAN A. CAMARCE
ASSOCIATE
(202) 772-8895
CCAMARCE@SKGF.COM



August 19, 2014

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 6612
Mail Stop Issue Fee

Re: Allowed U.S. Utility Patent Application
Appl. No. 12/874,134; Filed: September 1, 2010
For: **Processing Unit That Enables Asynchronous Task Dispatch**
Inventors: MANTOR *et al.*
Our Ref: 1972.1540001

Commissioner:

In response to the **Notice of Allowance and Fee(s) Due** dated May 22, 2014, the following documents are transmitted for appropriate action by the U.S. Patent and Trademark Office:

1. Issue Fee Transmittal (Form PTOL-85); and
2. Online Credit Card Payment Authorization for \$960.00 to cover:
\$960.00 - Issue Fee.

The above-listed documents are filed electronically through EFS-Web.

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Christian A. Camarce
Attorney for Applicants
Registration No. 65,021

CAC/smh
Enclosure(s)

1891205_1.DOCX

Realtek Ex. 1002

PART B - FEE(S) TRANSMITTAL

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 Alexandria, Virginia 22313-1450
 or **Fax** (571)-273-2885

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91505 7590 05/22/2014
 Sterne, Kessler, Goldstein & Fox P.L.L.C.
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 Washington, DC 20005



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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/874,134	09/01/2010	Michael MANTOR	1972.1540001	6612

TITLE OF INVENTION: PROCESSING UNIT THAT ENABLES ASYNCHRONOUS TASK DISPATCH

08/20/2014 ZJUWAR2 00000002 190036 12874134
 01 FC:1501 960.00 DA

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	08/22/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
CRAWFORD, JACINTA M	2618	345-505000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

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- 1 Sterne, Kessler,
 2 Goldstein & Fox PLLC
 3 _____

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(A) NAME OF ASSIGNEE

Advanced Micro Devices, Inc.

(B) RESIDENCE: (CITY AND STATE OR COUNTRY)

Sunnyvale, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

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☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

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NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature Christian Camarce
 Typed or printed name **Christian Camarce**

Date August 19, 2014
 Registration No. **65,021**



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/874,134	10/07/2014	8854381	1972.1540001	6612

91505 7590 09/17/2014
Sterne, Kessler, Goldstein & Fox P.L.L.C.
1100 New York Avenue N.W.
Washington, DC 20005

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 952 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Michael MANTOR, Orlando, FL;
Rex McCrary, Oviedo, FL;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

Realtek EX-1002

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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:



Practitioners associated with the Customer Number:

25310

OR



Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:



The address associated with Customer Number:

25310

OR

☐ Firm or Individual Name			
Address			
City	State	Zip	
Country			
Telephone	Email		

Assignee Name and Address:

Advanced Micro Devices, Inc.
One AMD Place
Sunnyvale, CA 94088**A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.****SIGNATURE of Assignee of Record**

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	/Gregory Suh/	Date	2/11/2014
Name	Gregory Suh	Telephone	408-749-3840
Title	Senior Corp. Counsel II, Patents		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Realtek Ex. 1002

Case No. IPR2023-00687

Page 220 of 228

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Mantor et al.

Application No./Patent No.: 12/874,134

Filed/Issue Date: September 1, 2010

Titled: PROCESSING UNIT THAT ENABLES ASYNCHRONOUS TASK DISPATCH

Advanced Micro Devices, Inc., a

corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;
2. ☐ an assignee of less than the entire right, title, and interest in
(The extent (by percentage) of its ownership interest is _____ %); or
3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 025720, Frame 0001, or for which a copy therefore is attached.

OR

- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

- ☒ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Gregory Suh/

2/11/2014

Signature

Date

Gregory Suh

Sr. Corp. Counsel II, Patents

Printed or Typed Name

Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Case No. IPR2023-00687

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Page 222 of 228

Privacy Act Statement

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4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	20309448
Application Number:	12874134
International Application Number:	
Confirmation Number:	6612
Title of Invention:	PROCESSING UNIT THAT ENABLES ASYNCHRONOUS TASK DISPATCH
First Named Inventor/Applicant Name:	Michael MANTOR
Customer Number:	91505
Filer:	Steven J. Gelman/Dawn Larsen
Filer Authorized By:	Steven J. Gelman
Attorney Docket Number:	1972.1540001
Receipt Date:	02-OCT-2014
Filing Date:	01-SEP-2010
Time Stamp:	13:25:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	AMD_080131_US_NP_Power_o f_Attorney_20141002.PDF	233460 8009f048769222654207044600dca71e075f 9c64	no	2

Warnings:

Information:

Realtek Ex. 1002
Case No. IPR2023-00687

2	Assignee showing of ownership per 37 CFR 3.73.	AMD_080131_US_NP_373b_Statement_20141002.PDF	422978 d87453afac326e4f8d917544f992683c1cd81677	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			656438		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/874,134	09/01/2010	Michael MANTOR	

25310
VOLPE AND KOENIG, P.C.
DEPT. AMD
UNITED PLAZA
30 SOUTH 17TH STREET
PHILADELPHIA, PA 19103

CONFIRMATION NO. 6612
POA ACCEPTANCE LETTER



Date Mailed: 10/10/2014

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/02/2014.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/rmtturner myles/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/874,134	09/01/2010	Michael MANTOR	1972.1540001

91505
Sterne, Kessler, Goldstein & Fox P.L.L.C.
1100 New York Avenue N.W.
Washington, DC 20005

CONFIRMATION NO. 6612
POWER OF ATTORNEY NOTICE



Date Mailed: 10/10/2014

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/02/2014.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/rmtturner myles/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
filed in the U.S. District Court Eastern District of Texas, Marshall Division on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 2:22-cv-00134	DATE FILED 5/5/2022	U.S. DISTRICT COURT Eastern District of Texas, Marshall Division
PLAINTIFF ADVANCED MICRO DEVICES, INC.; and ATI TECHNOLOGIES ULC		DEFENDANT TCL INDUSTRIES HOLDINGS CO., LTD.; TCL INDUSTRIES HOLDINGS (H.K.) LIMITED; TCL ELECTRONICS HOLDINGS LIMITED; TCL TECHNOLOGY GROUP CORPORATION; TCL CORPORATION
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,742,053	6/22/2010	ATI Technologies ULC
2 8,760,454	6/24/2014	ATI Technologies ULC
3 11,184,628	11/23/2021	ATI Technologies ULC
4 8,468,547	6/18/2013	Advanced Micro Devices Inc., ATI Technologies ULC
5 8,854,381	10/7/2014	Advanced Micro Devices Inc.

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy Realtek Ex. 1002

Case No. IPR2023-00687

Page 228 of 228