CURRICULUM VITA

MASSOUD PEDRAM

Personal Information

Charles Lee Powell Chair in Electrical Engineering and Computer Science
University of Southern California
Ming Hsieh Department of Electrical Engineering
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URL: http://www.mpedram.com/
Wiki: https://en.wikipedia.org/wiki/Massoud_Pedram

Impact on the Field

- Advancing the theory and practice of energy-efficient computing and introducing methodologies, hardware/software solutions, and design automation algorithms and tools for increasing computation speed and reducing power dissipation in CMOS circuits and systems including parallel and distributed computing systems, quantum computing, superconductor electronics and superconductive computing, cryptosystem hardware design

Research Interests

- Computer-aided design methodologies and tools for CMOS circuits and systems, energy-efficient computing, power/timing modeling and analysis in VLSI circuits, power/thermal management, power conversion and regulation, electrical energy storage systems, embedded systems, power-aware wireless networks, cloud computing and data center resource management, computer architecture, parallel and distributed computing, post-CMOS devices and circuits including quantum processors and superconductive electronics, and homomorphic computing

Education

- University of California at Berkeley, Ph.D. in Electrical Engineering and Computer Sciences, 1991
- University of California at Berkeley, M.S. in Electrical Engineering and Computer Sciences, 1989
- California Institute of Technology, B.S. in Electrical Engineering, 1986

Employment History

- Charles Lee Powell Chair in Electrical Engineering and Computer Science in the Viterbi School of Engineering, University of Southern California, 2017-present

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- Stephen and Etta Varra Professor in the Viterbi School of Engineering, University of Southern California, 2013-2017
- Professor, Department of Electrical Engineering, University of Southern California, 2000-2012
- Associate Professor, Department of Electrical Engineering, University of Southern California, 1996-2000
- Assistant Professor, Department of Electrical Engineering, University of Southern California, 1991-1996
- Part-time Research Position, Xerox Palo Alto Research Center, 1987-1989
- Graduate Student Researcher, Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, 1986-1991

Honors and Awards

- Best Paper Award of the *Int'l Symp. on Quality Electronic Design*, Mar. 2020
- Best Paper Award of the *Asia and South Pacific Design Automation Conference, Jan. 2019*
- USC Viterbi School of Engineering Senior Research Award, 2017
- "For contributions to modeling and design of low power VLSI circuits and systems, and energy efficient computing," *IEEE Circuits and Systems Society Charles A. Desoer Technical Achievement Award,* 2015
- The *Second Most Prolific and Second Most Cited Author Awards* from the 20th Anniversary *Int'l Symp. on Low Power Electronics and Design*, Rome, Italy, Jul. 2015
- *Frequent Author Award* (Top Three Author Award) at the 20th Anniversary *Asia and South Pacific Design Automation Conference*, Chiba/Tokyo, Japan, Jan. 2015
- ACM SIGDA *Distinguished Service Award*, 2014
- Best Paper Award of the *ACM/IEEE Int'l Symp. on Low Power Design and Electronics*, Aug. 2014
- Best Paper Award of the IEEE Computer Society Annual Symp. on VLSI, Jul. 2014
- Recognized as one of the four DAC Prolific Authors (with 50+ papers) and the DAC Bronze Cited Author at the 50th anniversary of the Design Automation Conf., Austin, TX, Jun. 2013
- 2013 DAC Volunteer Service Award sponsored by IEEE CEDA
- Best Paper Awards of the 1989, 2000, and 2012 IEEE Int'l Conference on Computer Design, VLSI in Computers and Processors
- ACM Distinguished Scientist, 2008
- ACM SIGDA Service Award, 2004
- "For contributions to the theory and practice of low-power design and CAD," IEEE Fellow, 2001
- ACM SIGDA Distinguished Service Award, 2000
- Presidential Early Career Award for Scientists and Engineers, 1996
- NSF's Young Investigator Award, 1994
- NSF's Research Initiation Award, 1992
- 2007 IEEE Trans. on Circuits and Systems Guillemin-Cauer Best Paper Award
- Honorable Mention Award at the 2008 Int'l Symp. on Low Power Electronics and Design
- Best Paper Awards of the 33rd ACM/IEEE Design Automation Conference, Jun. 1996 and the 42nd ACM/IEEE Design Automation Conference, Jun. 2005
- Distinguished Paper Citation of the IEEE Int'l Conference on Computer Aided Design, 1990
- 1996 IEEE Circuits and Systems Society VLSI Systems Trans. Best Paper Award

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University Service

- Member of the Computer Engineering Faculty Recruitment Committee, 2010-2011, 2013/2014, 2014/2015, 2016-2017
- Member of the VSoE Research Committee at USC, Sept. 2013 - 2017
- Member of the VSoE Transformative Faculty Hire Committee, Sept. 2013 - 2016
- Member of the Ming Hsieh Institute's Advisory Council, Jul. 2013 – Dec. 2015
- Chair of a faculty Promotion Committee in the EE department, 2014/2015, 2016-2017
- Member of the EE Dept. Faculty Recruitment Committee, 2014/2015
- Served on the Best Dissertation Selection Committee in the EE Dept., 2013
- Internal reviewer for an NSF Career Program proposal, 2013
- Chaired committee for evaluating Janet Roveda's Recruitment as an associate professor, 2012
- Division Director of USC Computer Engineering Division, Dec. 2005-Jun. 2010, and Acting Division Director at the end of 2012 and early 2013
- Served as the Chair of the 2005 Distinguished Lecture Series of the EE Dept.
- Served as the Associate Director of the CENG division of the EE Department at USC from 1998 to 2001
- Served on various departmental committees including the Faculty Merit Review Committee, Faculty Recruitment Committee, and the Promotion Committees in the EE department
- Chaired the Outstanding Research Paper Award Committee of the EE-Systems Department at USC in 1999
- Served on the Graduate Student Admissions Committee for entering M.S. and Ph.D. students in the CENG division of the EE-Systems Department at USC

Professional Service

- Served as technical area lead and panel moderator for the NSF Workshop on Micro/Nano Circuits and Systems Design in Dec 2020
- Participated in and contributed to the Computing Community Consortium (CCC) "Next Steps in Quantum Computing: Computer Science's Role," May 22-23, 2018
- Associate Editor of *Research, A Science Partner Journal*, 2018-present
- Served on the IEEE CASS Fellow (Selection) Committee, 2018
- Executive Committee Chair of the *Int'l Symp. on Low Power Electronics and Design*, July 2012 - present
- Editor-in-Chief of the *ACM Trans. on Design Automation of Electronic Systems*, Jun. 2008–May 2014
- Inaugural Editor-in-Chief of the *IEEE Journal on Emerging and Selected Topics in Circuits and Systems,* Jan. 2010–Dec. 2013
- Served as a member of the 2011 Selection Committee for the ACM SIGDA Outstanding New Faculty Award
- Served as the Chair of the Selection Committee for the IEEE CEDA and ACM SIGDA 2010 *A. Richard Newton Technical Impact Award in Electronic Design Automation*
- General Co-chair of the 2010 *IEEE Int'l Symp. on Circuits and Systems*, Paris, France
- Associate Editor
    - Foundations and Trends in Electronic Systems and Circuits Journal, Now Publishers, Inc. of Delft, 2006-2014

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    - Journal of Low Power Electronics, 2005-2014
    - IEEE Trans. on Computer Aided Design, 1997-2006
    - IEEE Trans. on Circuits and Systems I, 2002-2003
    - ACM Trans. on Design Automation of Electronic Systems, 1998-2004
- Distinguished Lecturer/Speaker
    - Association for Computing Machinery (ACM), 2007-2015
    - IEEE Solid State Circuits Society, 2001-2007
- VP of Publications of the IEEE Circuits and Systems Society, 2005-2006
- Chair of the Distinguished Lecturer Program, IEEE Circuits and Systems Society, 2003-2004
- Member of the Board of Governors, IEEE Circuits and Systems Society, 2000-2003
- Member of the ACM-SIGDA Advisory Board, managing the ACM Outstanding Ph.D. Dissertation Award in Electronic Design Automation, the DAC Young Student Support Program, the Multimedia Monograph Series, and the SIGDA Technical Committees, 1996-2009
- Chair of the Best Paper Award Committee for the IEEE Trans. on Computer Aided Design, 1999
- Member of the Research or Technical Advisory Board
    - Atrenta Inc., 2003-2015
    - Envis Inc., 2006-2009
    - PwrLite Inc., 2007-2009
    - Fulcrum Microsystems, 2001-2004
    - Aplus Design Technologies Inc., 2000-2003
    - Magma Design Automation Inc., 1997-2002
    - EPIC Design Technology, 1994-1997
- General Chair
    - *Int'l Symp. on Quality of Electronic Design*, San Jose, CA, Apr. 2007
    - *Int'l Symp. on Physical Design*, Monterey, CA, Apr. 2003
    - *Int'l Symp. on Low Power Electronics and Design*, Monterey, CA, Aug. 1997
    - *Int'l Symp. on Low Power Design*, Laguna, CA, Apr. 1995
- Technical Chair
    - *Int'l Symp. on Physical Design*, Del Mar, CA, Apr. 2002
    - *Int'l Symp. on Low Power Electronics and Design*, Monterey, CA, Aug. 1996
    - *Int'l Workshop on Low Power Design*, Napa Valley, CA, Apr. 1994
- Executive Committee Member
    - *Int'l Symp. on Low Power Electronics and Design*, since 1996
    - *Int'l Conference on Computer Aided Design*, since 2006
- Technical Program Committee Member
    - *The 18th CSI International Symposium on Computer Architecture & Digital Systems*, Tehran, Iran, Oct. 7-8, 2015
    - *Int'l Conference on Hardware/Software Codesign and System Synthesis*, 2013-2015
    - *Symp. on Embedded Systems for Real-Time Multimedia (ESTIMedia),* 2007-2012
    - *Symp. on VLSI Design, Automation and Test (VLSI-DAT)*, 2012
    - 2009 *Great Lakes Symp. on VLSI*
    - 2008 IEEE Int'l Design and Test Workshop, Tunisia
    - *Symp. on VLSI Design, Automation and Test (VLSI-DAT)*, Hsinchu, Taiwan, 2009
    - NanoArch, 2007-2008
    - *The 13th CSI Computer Conference* (CSICC'08), Kish Island, Iran, March 9-11, 2007
    - Conference on VLSI – *Design Automation Technologies*, Taipei, Taiwan, 2006-2007
    - 1998-2000 *Int'l Conference on Computer Aided Design*
    - 1998-2001 *Int'l Symp. on Physical Design*

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- 1997-2000 *Int'l Workshop on Logic Synthesis*
- 2000 *Asia and South Pacific Design Automation Conference*
- 1998-2003 *Design Automation and Test in Europe Conference*
- 1994-2000 *Int'l Symp. on Low Power Electronics and Design*
- 2001-2003 *Int'l Symp. on Quality of Electronic Design*

US Patents

[S1] Nazemi: Mahdi (Los Angeles CA); Fayyazi; Arash (Los Angeles CA); Esmaili; Amirehossein (Los Angeles CA); Pedram; Massoud (Beverly Hills CA), "System and Method for Hybrid Arithmetic and Logic Processing of Neural Networks," United States Provisional Patent filed on Dec. 23, 2021. Application Number: 63293500.

[S2] Zhang; Bo (Los Angeles CA); Chen; Zeming (Los Angeles CA); Pedram; Massoud (Beverly Hills CA); "Design of High-Performance and Scalable Montgomery Modular Multiplier Circuits," International Patent Filed on May 7, 2021, Application Number: PCT/US2021/028896.

[S3] Pasandi; Ghasem (Los Angeles, CA); Pedram; Massoud (Beverly Hills CA), "Efficient pipelined architecture for superconducting single flux quantum logic circuits utilizing dual clocks," United States Patent **11,303,281**, Issued: Apr. 4, 2022, Filed: Apr. 5, 2021.

[S4] Katam; Naveen (Los Angeles, CA); Mukhanov; Oleg (Elmsford, NY); Pedram; Massoud (Los Angeles, CA), "Superconductive magnetic field programmable gate array," United States Patent **10,707,873**, Issued: Jul. 7, 2020, Filed: Mar. 21, 2019.

[S5] Pedram; Massoud (Beverly Hills, CA); Iranli; Ali (Los Angeles, CA), "Dynamic backlight scaling for power minimization in a backlit TFT-LCD," United States Patent **8,094,118**, Issued: Jan 10, 2012, Filed: Mar 2, 2006.

[S6] Fallah; Farzan (San Jose, CA); Pakbaznia; Ehsan (Los Angeles, CA); Pedram; Massoud (Beverly Hills, CA); "Sizing and placement of charge recycling (CR) transistors in multithreshold complementary metal-oxide-semiconductor (MTCMOS) circuit," United States Patent **7,834,684**, Issued: Nov 16, 2010, Filed: Oct 31, 2008.

[S7] Fallah; Farzan (San Jose, CA); Abdollahi; Afshin (Los Angeles, CA); Pedram; Massoud (Los Angeles, CA); "Power mode transition in multi-threshold complementary metal oxide semiconductor (MTCMOS) circuits," United States Patent **7,613,942**, Issued: November 3, 2009, Filed: May 31, 2006.

[S8] Fallah; Farzan (San Jose, CA); Amelifard; Behnam (Los Angeles, CA); Pedram; Massoud (Beverly Hills, CA); "Setting threshold voltages of cells in a memory block to reduce leakage in the memory block," United States Patent **7,573,775**, Issued: August 11, 2009, Filed: February 9, 2007.

[S9] Fallah; Farzan (San Jose, CA); Amelifard; Behnam (Los Angeles, CA); Pedram; Massoud (Beverly Hills, CA); "PG-Gated Data Retention Technique for Reducing Leakage in Memory Cells," United States Patent **7,447,101**, Issued: November 4, 2008, Filed: December 22, 2006.

[S10] Fallah; Farzan (San Jose, CA); Pakbaznia; Ehsan (Los Angeles, CA); Pedram; Massoud (Beverly Hills, CA); "Recycling Charge to Reduce Energy Consumption During Mode Transition in Multi-Threshold Complementary Metal-Oxide-Semiconductor (MTCMOS) Circuits," United States Patent **7,400,175**, Issued: July 15, 2008, Filed: May 30, 2007.

[S11] Fallah; Farzan (San Jose, CA), Aghaghiri; Yazdan (Los Angeles, CA), Pedram; Massoud (Los Angeles, CA). "System and method for identifying optimal encoding for a given trace," United States Patent **7,236,107**, Issued: June 26, 2007, Filed: September 20, 2004.

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[S12] Fallah; Farzan (San Jose, CA); Aghaghiri; Yazdan (Los Angeles, CA); Pedram; Massoud (Los Angeles, CA). "Reducing transitions on address buses using instruction-set-aware system and method," United States Patent **6,907,511**, Issued: June 14, 2005, Filed: January 14, 2003.

[S13] Fallah; Farzan (San Jose, CA); Aghaghiri; Yazdan (Los Angeles, CA); Pedram; Massoud (Los Angeles, CA). "System and method for reducing transitions on address buses," United States Patent **6,834,335**, Issued: December 21, 2004, Filed: August 9, 2002.

[S14] Fallah; Farzan (San Jose, CA); Aghaghiri; Yazdan (Los Angeles, CA); Pedram; Massoud (Los Angeles, CA), United States Patent **6,813,700** "Reduction of bus switching activity using an encoder and decoder," Issued: November 2, 2004, Filed: June 3, 2002.

Citation Indices and Top 20 Cited Papers as of August 25, 2022

Google Scholar: total citations: 33,277, h-index=91, i10-index = 513, and g-index=151

1. M. Pedram. "Power minimization in IC design: principles and applications," *ACM Trans. on Design Automation of Electronic Systems*, Vol. 1, No. 1, 1996, pages 3-56. [789 citations]
2. M. Pedram and S. Nazarian. "Thermal modeling, analysis and management in VLSI circuits: Principles and methods," *Proc. of IEEE, Special Issue on Thermal Analysis of ULSI*, Vol. 94, No. 8, Aug. 2006, pages 1487-1501. [500 citations]
3. JM. Chang and M. Pedram. "Energy minimization using multiple supply voltages," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, Vol. 5, No. 4, Dec. 1997, pages 436-443. [475 citations]
4. P. Rong and M. Pedram. "An analytical model for predicting the remaining battery capacity of Lithium-ion batteries," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems,* Vol. 14, No. 5, May 2006, pages 441-451. [470 citations]
5. K. Choi, R. Soma, and M. Pedram. "Fine-grained dynamic voltage and frequency scaling for precise energy and performance trade-off based on the ratio of off-chip access to on-chip computation times," *IEEE Trans. on Computer Aided Design*, Vol. 24, No. 1, Jan. 2005, pp.18-28. [433 citations]
6. E. Macii, M. Pedram, and F. Somenzi. "High level power modeling, estimation and optimization," *IEEE Trans. on Computer Aided Design*, Vol. 17, No. 11, Nov. 1998, pages 1061-1079. [420 citations]
7. Q. Wu, M. Pedram, and X. Wu. "Clock-gating and its application to low power design of sequential circuits," *IEEE Trans. on Circuits and Systems*—I, Vol. 47, No. 3, Mar. 2000, pages 415-420. [418 citations]
8. A. Abdollahi, F. Fallah, and M. Pedram. "Leakage current reduction in CMOS VLSI circuits by input vector control," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, Vol. 12, No. 2, Feb. 2004, pp.140-154. [386 citations]
9. Q. Qiu and M. Pedram. "Dynamic power management based on continuous-time Markov decision processes," *Proc. of 36th Design Automation Conference*, Jun. 1999, pages 555-561. [368 citations]
10. F. Fallah and M. Pedram. "Standby and active leakage current control and minimization in CMOS VLSI circuits," *IEICE Trans. on Electronics*, Special Section on Low-Power LSI and Low-Power IP, Vol. E88–C, No. 4 Apr. 2005, pages 509-519. [362 citations]
11. M. Maleki, K. Dantu, and M. Pedram. "Power-aware source routing protocol for mobile ad hoc networks," *Proc. of Symp. on Low Power Electronics and Design*, Aug. 2002, pages 72-75. [349 citations]

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12. K. Choi, R. Soma and M. Pedram. "Dynamic Voltage and Frequency Scaling based on Workload Decomposition," *Proc. of Symp. on Low Power Electronics and Design*, Aug. 2004, pages 174-179. [314 citations]
13. WC. Cheng, Y. Hou, and M. Pedram. "Power minimization in a backlit TFT-LCD display by concurrent brightness and contrast scaling," *IEEE Trans. on Consumer Electronics*, Vol. 50, No. 1, Feb. 2004, pages 25-32. [308 citations]
14. E. Pakbaznia and M. Pedram. "Minimizing data center cooling and server power costs," *Proc. of Symp. on Low Power Electronics and Design*, Aug. 2009, pages 145-150. [304 citations]
15. A. H. Ajami, K. Banerjee, and M. Pedram. "Modeling and analysis of non-uniform substrate temperature effects in high performance VLSI," *IEEE Trans. on Computer Aided Design*, Vol. 24, No. 6, Jun. 2005, pages 849-861. [284 citations]
16. H. Goudarzi and M. Pedram. "Multi-dimensional SLA-based resource allocation for multi-tier cloud computing systems," *Proc. of IEEE Conf. on Cloud Computing*, Jul. 2011, pages 324-331. [274 citations]
17. D. Singh, J. Rabaey, M. Pedram, F. Catthoor, S. Rajgopal, N. Sehgal, and T. Mozdzen. "Power-conscious CAD tools and methodologies: a perspective," *Proc. of IEEE*, Vol. 83, No. 4, 1995, pages 570-594. [247 citations]
18. M. Pedram and Q. Wu. "Design considerations for battery-powered electronics," *Proc. of 36th Design Automation Conf.,* Jun. 1999, pages 861-866. [242 citations]
19. JM. Chang and M. Pedram. "Register allocation and binding for low power," *Proc. of 32nd Design Automation Conference,* Jun. 1995, pages 29-35. [237 citations]
20. M. Maleki, K. Dantu, and M. Pedram. "Lifetime Prediction Routing in Mobile Ad Hoc Networks," *Proc. of IEEE Wireless Communication and Networking Conf.,* Mar. 2003, pages 1185-1190. [235 citations]

Publications

Books

[B1] M. Pedram and J. Rabaey (editors). *Power-aware Design Methodologies*, Kluwer Academic Publishers, Boston, Jun. 2002.

[B2] JM. Chang and M. Pedram. *Power Optimization and Synthesis at Behavioral and System Levels Using Formal Methods*, Kluwer Academic Publishers, Boston, Jun. 1999.

[B3] S. Iman and M. Pedram. *Logic Synthesis for Low Power VLSI Designs*, Kluwer Academic Publishers, Boston, Nov. 1997.

[B4] J. Rabaey and M. Pedram (editors). *Low Power Design Methodologies*, Kluwer Academic Publishers, Boston, Oct. 1995.

[B5] M. Pedram. *ACM-SIGDA Multimedia Monograph Series*, Volumes 1-12, ACM Publications.

Book Chapters

[BC1] M. Vaeztourshizi, H. Afzali-Kusha, M. Kamal, and Massoud Pedram. "Design Techniques for Approximate Realization of Data-Flow Graphs," in Springer's book titled *Approximate Computing,* Editors: W. Liu and F. Lombardi, 2022.

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[BC2] M.A. Karamuftuoglu, S. Nazar Shahsavani and M. Pedram. "Margin Optimization of Single Flux Quantum Logic Cells," in *Design Automation of Quantum Computers*, Editor: R.O. Topaloglu, Springer Nature, 2022.

[BC3] A. Fayyazi, M. Ansari, M. Kamal, A. Afzali-Kusha, and M. Pedram. "Inverter-based memristive neuromorphic circuit for ultra-low-power IoT smart applications," in IET's book titled *Hardware Architectures for Deep Learning*, Editors: M. Daneshtalab, and M. Modarressi, 2020.

[BC4] M. Hemmat, M. Kamal, A. Afzali-Kusha, and M. Pedram. "Robust Hybrid TFET-MOSFET Circuits in Presence of Process Variations and Soft Errors," in *VLSI-SoC: System-on-Chip in the Nanoscale Era – Design, Verification and Reliability*, Editors: T. Hollstein, J. Raik, S. Kostin, A. Tšertov, I. O'Connor, and R. Reis, Part of the IFIP Advances in Information and Communication Technology book series, Springer, 2017.

[BC5] M. J. Dousti, A. Petraglia, and M. Pedram, "Maximum Power Point Tracking for Thermoelectric Generators Using their Accurate Electrothermal Model," in Advances in Energy Research, M. J. Acosta, Ed., Vol. 26, Nova Science Publishers, 2017.

[BC6] H. Goudarzi and M. Pedram. "Achieving Energy Efficiency in Datacenters by Virtual Machine Sizing, Replication, and Placement," in Elsevier's book titled *Advances in Computers: Energy Efficiency in Data Centers and Clouds*, Editors: A. Hurson and H. Sarbazi-Azad, Vol. 100, Feb. 2016.

[BC7] A. Shafaei, M-J. Dousti, M. Pedram. "Computer-Aided Design for Next-generation Quantum Computing Systems," *in New Developments in Quantum Optics Research*, Editor: N. Stewart, Nova Science Publishers, 2015.

[BC8] N. Chang, M. Pedram, H.G. Lee, Y. Wang, and Y. Kim. "Reconfigurable Photovoltaic Array Systems for Adaptive and Fault-Tolerant Energy Harvesting," in *Nano Devices and Circuit Techniques for Low-Energy Applications and Energy Harvesting*, Editor: C.M. Kyung, KAIST Research Series, Springer, Jul. 2015, pp. 181-209.

[BC9] Y. Wang, X. Lin, and M. Pedram. "Accurate component model-based control algorithm for residential photovoltaic and energy storage systems accounting for prediction inaccuracies," in *Smart Grids: Technologies, Applications and Management Systems*, Editor: L. M. Koga, Electrical Engineering Developments Series, Nova Science Publishers, 2014.

[BC10] H. Goudarzi and M. Pedram. "Profit-maximizing resource allocation for multi-tier cloud computing systems under service level agreements," in *Large Scale Network-Centric Computing Systems*, Editors: H. Sarbazi-Azad and A. Y. Zomaya, Wiley-IEEE Computer Society Press, Oct. 2013.

[BC11] P. Rong and M. Pedram. "A stochastic framework for hierarchical system-level power management," Chapter 4 in *Energy Efficient Distributed Computing Systems*, Editors: A. Y. Zomaya and Y-C Lee, Wiley-IEEE Computer Society Press, Aug. 2012.

[BC12] N. Mohyuddin, E. Pakbaznia, and M. Pedram. "Probabilistic error propagation in a logic circuit using the Boolean difference calculus," Chapter 19 in *Advanced Techniques in Logic Synthesis, Optimizations and Applications*, Editors: S.P. Khatri and K. Gulati, Springer, 2010.

[BC13] A. Iranli and M. Pedram. "System-level power management: an overview," in *The VLSI Handbook Second Edition*, Editor: W-K. Chen, Taylor and Francis, 2006.

[BC14] A. Abdollahi and M. Pedram. "RT-level power minimization techniques," in *SoC: Next Generation Electronics*, Editor: Bashir M. Al-Hashimi, IEE Press, 2005.

[BC15] M. Maleki and M. Pedram. "Power-aware on-demand routing protocols for mobile ad hoc networks," in *Low-Power Electronics Design*, Editor: C. Piguet, CRC Press, 2004.

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[BC16] WC. Cheng and M. Pedram. "Transmittance scaling for reducing power dissipation of a backlit TFT-LCD," in *Ultra Low Power Design*, Editor: E. Macii. Kluwer Academic Publishers, 2004.

[BC17] M. Pedram. "Power simulation and estimation in VLSI circuits," in *The VLSI Handbook*, *Design automation, languages, and simulations*, Editor: W-K. Chen, CRC Press and IEEE Press, 2003, pages 18.1-18.23.

[BC18] M. Pedram. "Advanced power estimation techniques," in *Low Power Design in Deep Submicron Technology*, Editors: J. Mermet and W. Nebel, Kluwer Academic Publishers, 1997.

[BC19] S. Iman and M. Pedram. "Combinational circuit optimization," in *Low Power Design in Deep Submicron Technology*, Editors: J. Mermet and W. Nebel, Kluwer Academic Publishers, 1997.

[BC20] M. Pedram. "Design technologies for Low Power VLSI," in *Encyclopedia of Computer Science and Technology*, Marcel Dekker, Editors: A Kent, J. G. Williams, and C. M. Hall, Vol. 36, 1997, pages 73-96.

[BC21] S. B. K. Vrudhula, M. Pedram, and Y. T. Lai. "Edge-valued binary-decision diagrams," in *Representations of Discrete Functions*, Editors: T. Sasao and M. Fujita, Kluwer Academic Publishers, 1996, pages 109-132.

[BC22] J. Rabaey, M. Pedram, and P. Landman. "Introduction to Low Power Design," in *Low Power Design Methodologies*, Editors: J. Rabaey and M. Pedram. Kluwer Academic Publishers, 1996, pages 1-18.

[BC23] M. Pedram. "Logic synthesis for low power," in *Low Power Design Methodologies*, Editors: J. Rabaey and M. Pedram. Kluwer Academic Publishers, 1996, pages 129-160.

Journal Articles (accepted for publication)

[J1] S. Taghipour, M. Kamal, R. N. Asli, A. Afzali-Kusha and M. Pedram, "LCHC-DFT: A Low-Cost High-Coverage Design-for-Testability Technique to Detect Hard-to-Detect Faults in STT-MRAMs in the Presence of Process Variations," in *IEEE Transactions on Device and Materials Reliability*, 2022.

[J2] B. Zhang, Z. Cheng, and M. Pedram. "An Iterative Montgomery Modular Multiplication Algorithm with Low Area-Time Product," *IEEE Trans. on Computers,* Early Access Article, 24 Feb. 2022.

Journal Articles (published)

2022

[J3] N. Nguyen, H. Vu, M. Pedram, and D. Shin. "An Attachable Battery-Supercapacitor Hybrid for Large Pulsed Load," *IEEE Design & Test*, 39(5):62-69 (2022).

[J4] M. Soltani, M. Kamal, A. Afzali-Kusha, and M Pedram. "An Adaptive Memory Side Encryption Method for Improving Security and Lifetime of PCM-based Main Memory," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, 41(6): 1744-1756 (2022).

[J5] M. Zolfagharinejad, M. Kamal, A. Afzali-Kusha, and M. Pedram. "Posit Process Element for Using in Energy-Efficient DNN Accelerators," *IEEE Trans. Very Large Scale Integrated Systems*, 30(6): 844-848 (2022).

[J6] B. Zhang, Z. Cheng and M. Pedram, "High-Radix Design of a Scalable Montgomery Modular Multiplier with Low Latency," *IEEE Transactions on Computers*, 71(2): 436-449 (2022).

[J7] E. Tanghatari, M. Kamal, A. Afzali-Kusha, and M. Pedram. "Distributing DNN training over IoT edge devices based on transfer learning," *Neurocomputing,* 467: 56-65 (2022).

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[J8] A. Fayyazi, M. Munir, A. Gopikanna, S. Nazarian, and M. Pedram. "A Logic Verification Framework for SFQ and AQFP Superconducting Circuits," *IEEE Trans. on Applied Superconductivity*, 31(9):1-11 (2021).

[J9] M. J. Dousti, Q. Xie, M. Nazemi, and M. Pedram, "Therminator 2: A Fast Thermal Simulator for Portable Devices," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, 40(12): 2528-2541 (2021).

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Recent Invited Talks and Tutorials

[T1] M. Pedram. "Design Methodologies, Circuits, and Architectures for Superconductor Electronic Systems," Proc. of Int'l Symp. on Low Power Electronics and Design, 2022.

[T2] M. Pedram. Talks at DAQ workshop, ICCAD, IEDM, and ISS on Coldflux project and qPALACE tool suite.

[T3] M. Pedram. "State of the art in Electronics Design Automation for Superconductive Electronics," Workshop on Superconductor Electronics, Skytop, Pennsylvania, Oct. 2019.

[T4] M. Pedram. "Superconducting single flux quantum Logic Circuits and Design Tools," Technical University of Munich, Aug. 2019.

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[T5] M. Pedram. "Design Automation Methodology and Tools for Superconductive Electronics," Invited talk at the *Int'l Conf. on Computer Aided Design*, Nov. 7, 2018.

[T6] M. Pedram. "ColdFlux: CAD Methodologies and Tools for Single Flux Quantum Based Superconductive Electronics," Invited talk at the *Applied Superconductivity Conference*, Nov. 1, 2018.

[T7] M. Pedram. "Energy-Efficient Computing: Datacenters, Mobile Devices, and Mobile Clouds," Keynote Speech of the *Int'l Symp. on Green Computing*, Oct. 23, 2019

[T8] M. Pedram. "An Ultra-Low-Power High-Speed Cache Memory Comprising of Hybrid TFET-FinFET SRAM Cells," Invited talk at the Int'l Conf. on Solid State Materials and Devices, Sep. 11. 2018.

[T9] M. Pedram. "ColdFlux: CAD Methodologies and Tools for Single Flux Quantum Based Superconductive Electronics, Project Progress Report," talk given at the First Annual Program Review Meeting, IARPA SuperTools program, Aug. 28, 2018.

[T10] M. Pedram. "ColdFlux: CAD Methodologies and Tools for Single Flux Quantum Based Superconductive Electronics," Presentation at the IARPA SuperTools Site Visit, Jun. 20, 2018.

[T11] M. Pedram. "ColdFlux: CAD Methodologies and Tools for Single Flux Quantum Based Superconductive Electronics--Project Progress Report," Presentation at the IARPA SuperTools Technical Exchange Meeting 1, Apr. 10, 2018.

[T12] M. Pedram. "Coldflux: CAD Tools and Methodologies for SFQ-based Superconductive Electronics." Presentation at the IARPA SuperTools Kickoff meeting, 30 Oct. 2017

[T13] M. Pedram and C. Fourie. "Summary and Perspectives of the Seedling on SCE Design Tools and Methodologies," Presentation at the IARPA C3 Team Meeting, Baltimore, MD, 26 Oct. 2017.

[T14] M. Pedram. "VINE: A Variational Inference-Based Bayesian Neural Network Engine." Presentation to DARPA MTO, Los Angeles CA, 8 Aug. 2017.

[T15] M. Pedram, S. Chen, and E. Eshratifar. "Game Theoretic Approaches to Cyber Security," Presentation to DARPA MTO, Los Angeles CA, 27 Jun. 2017.

[T16] N. Katam, A. Shafaei, and M. Pedram. "Design of Complex Rapid Single-Flux-Quantum Cells with Application to Logic Synthesis," Presentation at the Intern. Superconductive Elec. Conf., Sorrento (Napoli), Italy, 13 Jun. 2017.

[T17] M. Pedram. "Design flow and tool chain for Synthesis and Physical Design of SFQ Circuits. IARPA C3 PI meeting, Baltimore, MD, 7 Apr. 2017.

[T18] M. Pedram. "Review of Superconductive Electronics Technology and SFQ Circuit Design." Presentation at ARM Research (arranged by IARPA), Austin TX, 6 Mar. 2017.

[T19] M. Pedram and C. Fourie. "Design, Optimization, and Demonstration of an FPGA Device for SFQ Circuits and Hybrid SFQ/FinFET Memory," Presentation to IARPA, Baltimore, MD, 21 Feb. 2017.

[T20] M. Pedram and Y. Wang. "SpiNN-SC: Stochastic Computing-Based Realization of Spiking Neural Networks," Presentation to DARPA MTO, Los Angeles CA, 17 Feb. 2017.

[T21] "Inference and Learning with Bayesian Neural Networks: Architecture and Hardware Realization," Invited presentation at DARPA MTO SAGA Concept Summit, Dayton OH, Nov 14, 2016

[T22] "Designing Energy-Efficient and High-Performance VLSI Circuits and Systems in 7nm FinFET Technology," Presentation at Samsung Austin R&D Center Technical Forum, Austin TX, Oct. 18, 2016

[T23] "Cell Library Design and an Integrated Place & Route Tool for RSFQ Logic", Invited Presentation at IARPA C3 Program Review Meeting, Baltimore, MD, Sept. 30, 2016

[T24] "Designing Energy-Efficient and Robust Circuits in 7nm FinFET Technology," Talk at Cadence Distinguished Speaker Series, San Jose, CA, Sept. 21, 2016

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