

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LENOVO (UNITED STATES) INC. and
MOTOROLA MOBILITY LLC
Petitioners

v.

THETA IP, LLC
Patent Owner

Patent No. 7,010,330

**DECLARATION OF R. JACOB BAKER, P.E., PH.D.
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,010,330**

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I, R. Jacob Baker, declare as follows:

I. INTRODUCTION

1. I have been retained by Lenovo (United States) Inc. and Motorola Mobility LLC (collectively, “Petitioners”) as an independent technical expert consultant in connection with the above-captioned *Inter Partes* Review of U.S. Patent No. 7,010,330 (“the ’330 patent”) (Ex. 1001). Although I am being compensated at my normal consulting rate of \$655 per hour for the time I spend on this matter, no part of my compensation is dependent on the outcome of this proceeding or any other related proceeding. I have no other interest in this proceeding.

2. Based on a review of the front page of the ’330 patent, I understand that the ’330 patent is assigned to Theta IP, LLC (“Theta” or “Patent Owner”). In addition, I understand that the application for the ’330 patent, U.S. Patent Application No. 10/784,613, was filed on February 23, 2004. I also understand that U.S. Patent Application No. 10/784,613 claimed the benefit of priority from U.S. Provisional Patent Application No. 60/451,229, filed on March 1, 2003 (“the ’229 application”), and U.S. Provisional Patent Application No. 60/451,230 (“the ’230 application”), both of which are expired provisional applications that were filed on March 1, 2003. (Ex. 1001.)

3. I am familiar with the technology at issue as of March 1, 2003, i.e., the filing date of the '229 application and the '230 application from which the '330 patent claims priority, as explained immediately above.

4. I have been asked to consider how a person of ordinary skill in the art would have understood the claims of the '330 patent and the applied references. More specifically, I have been asked to provide my technical opinion on concepts discussed in the '330 patent and the reference documents, as well as my technical opinion on how these concepts relate to the '330 patent's claim limitations in the context of the written description.

5. In reaching the opinions stated herein, I have considered the '330 patent and the various other documents listed in Section III below in the context of my own education, training, research, knowledge, and personal and professional experiences. My opinions are provided below.

II. QUALIFICATIONS

6. I presently serve as a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas (UNLV). In forming my opinions, I have relied on my knowledge and experience in designing, developing, and researching wireless communication devices and my knowledge of electrical circuit design and fabrication and electrical engineering fundamentals. I am not an attorney and offer

no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person having ordinary skill in the art. I am over 18 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein.

7. I have been teaching electrical engineering at UNLV since 2012. Prior to this position, I was a Professor of Electrical and Computer Engineering at Boise State University from 2000. Prior to my position at Boise State University, I was an Associate Professor of Electrical Engineering between 1998 and 2000 and Assistant Professor of Electrical Engineering between 1993 and 1998 at the University of Idaho. I have been teaching electrical engineering since 1991.

8. I received a Bachelor of Science and Master of Science degrees in Electrical Engineering from UNLV, in 1986 and 1988, respectively. In 1993, I also received a Ph.D. in Electrical Engineering from the University of Nevada, Reno.

9. I have extensive industry and academic experience related to the field of wireless communication and interface circuits. Specifically, I have over 30 years of academic and industry experience in modeling, design, and development of wireless communication devices and circuitry thereon. From 1985 to 1993, I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapon tests at the Nevada Test Site. During this time, I designed, and oversaw the

fabrication and manufacture of over 30 electronic and electronic-optic instruments including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame and bit-syncs, data converters, streak-camera sweep circuits, Pockels cell drivers, micro-channel plate gating circuits, and analog oscilloscope electronics.

10. From 1997 to 1999, I served as a Consultant for Tower Semiconductor, in the design of CMOS integrated circuit cells for various modem chips, interfaces, and serial buses, including charging circuits based upon power up-down circuits using an MOS or bandgap reference, pre-amplifiers, and comparators. I was also a Senior Designer at Micron Technology from 1994 to 2008, working on the development of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, CMOS Image Sensors (CISs), and power supply design. My more recent industry experience includes working with Freedom Photonics on the integration, fabrication, and design of optoelectronics with CMOS integrated circuits, including the design of compact optical transceiver for range finding applications, Geiger mode SiGe receiver for long-range communications, and packaging and testing of numerous chips fabricated in both CMOS and SiGe technologies. I have worked as a consultant at other companies designing electronic circuits, including Sun, Oracle, Contour Semiconductor, Lockheed-Martin, and OmniVision.

11. I have taught courses in integrated circuit design (analog, digital, mixed-signal, memory circuit design, etc.), linear circuits, microelectronics, communication systems, power electronics, and fiber optics. As a processor, I have been the main advisor to over 100 Master's and Doctoral students.

12. I am the author of several books covering the area of integrated circuit design including: DRAM Circuit Design: Fundamental and High-Speed Topics (two editions), CMOS Circuit Design, Layout, and Simulation (four editions), and CMOS Mixed-Signal Circuit Design (two editions). I have authorized, and coauthored, more than 100 papers and presentations in the areas of electronic circuit design. Also, I am the named inventor on over 150 granted U.S. patents, including U.S. Patent No. 8,879,327 titled "Reference Current Sources," U.S. Patent No. 7,330,390 titled "Noise Resistant Small Signal Sensing Circuit for a Memory Device," U.S. Patent No. 6,954,392 titled "Method for Reducing Power Consumption when Sensing a Resistive Memory," and U.S. Patent No. 5,953,276 titled "Fully-Differential Amplifier."

13. I have received numerous awards for my work, including the Frederick Emmons Terman (the "Father of Silicon Valley") Award. The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator's contributions to the profession.

14. I am a Fellow of the IEEE for contributions to memory circuit design. I have also received the IEEE Circuits and Systems Education Award (2011).

15. I have received the President's Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001), all from Boise State University. I have also received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor award four of the years I have been at UNLV.

16. My curriculum vitae, which includes a more detailed summary of my background, experience, patents, designs, and publications, is attached as Appendix A to this Declaration.

III. SUMMARY OF OPINIONS AND MATERIALS REVIEWED

17. All of the opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment. In forming the opinions expressed in this Declaration, while drawing on my knowledge and experience in designing, developing, and researching wireless communication devices and associated circuitry, I reviewed the following documents: the '330 patent (Ex. 1001); the prosecution history of the '330 patent (Ex. 1003); European Patent No. 0999649 A2 ("*Rauhala*") (Ex. 1004); United States Patent No. 6,278,864 ("*Cummins*") (Ex. 1005); United States Patent No. 5,953,640 ("*Meador*") (Ex.

1006); United States Patent No. 5,086,508 (“*Furuno*”) (Ex. 1007); U.S. Patent No. 5,513,387 B2 (“*Saito*”) (Ex. 1008); Claim Construction Order dated January 7, 2021, from *Theta IP, LLC v. Samsung Electronics Co. Ltd., et al.*, 6:20-cv-00160-ADA (W.D. Tx.) (Ex. 1009); Memorandum and Order on Claim Construction dated June 6, 2017 from *Theta IP, LLC v. Samsung Electronics Co. Ltd., et al.*, 2:16-cv-527 (E.D. Tx.) (Ex. 1010); Rudolf F. Graf, *Modern Dictionary of Electronics*, Seventh Edition, 1999 (Ex. 1011); Behzad Razavi, *RF Microelectronics*, Prentice Hall PTR, 1998 (Ex. 1012); Patent Owner’s Claim Construction Brief, *Theta IP, LLC v. Samsung Electronics Co.*, No. 2:16-CV-527-JRG-RSP (E.D. Tex. April 11, 2017), ECF No. 63 (Ex. 1013); Patent Owner’s Claim Construction Reply Brief, *Theta IP, LLC v. Samsung Electronics Co.*, No. W-20-CV-00160-ADA (W.D. Tex. Dec. 16, 2020), ECF No. 45 (Ex. 1014); Phillip A. Laplante, *Electrical Engineering Dictionary*, 2000 (Ex. 1015); A. Kestenbaum et al., *Design Concepts for Process Control*, *Ind. Eng. Chem., Process Des. Dev.*, Vol. 15, No. 1, (1976) (Ex. 1016); Lijun Qian, *Optimal Power Control in Cellular Wireless Systems*, Ph.D. diss., Rutgers The State University of New Jersey, School of Graduate Studies (2001) (Ex. 1017); United States Patent No. 3,880,104 (“*Saye*”) (Ex. 1018); Scheduling Order, *Theta IP, LLC v. Motorola Mobility LLC*, No. 1:22-cv-03441 (N.D. Ill. Sep. 29, 2022), ECF No. 26 (Ex. 1019); United States Patent No. 6,236,365 (“*LeBlanc*”) (Ex. 1020); David A. Johns & Ken

Martin, Analog Integrated Circuit Design, 1997 (Ex. 1021), Mahmood Nahvi, Ph.D. & Joseph A. Edminister, *Schaum's Outline of Theory and Problems of Electric Circuits* (4th ed. 2003) (Ex. 1022).¹

18. My opinions additionally are guided by my appreciation of how a person of ordinary skill in the art (defined in Section IV below) would have understood the claims and specification of the '330 patent at the time of alleged invention of the '330 patent. I have been asked to assume that the time of alleged invention of the '330 patent is March 1, 2003, which is the filing date of the '229 application and the '230 application. My opinions reflect how one of ordinary skill in the art would have understood the '330 patent, the prior art to the patent, and the state of the art at the time of alleged invention of the '330 patent.

19. Based on my experience and expertise, it is my opinion that certain references disclosed all the features recited in claims 1, 23, 29, and 30 ("challenged claims") of the '330 patent, as I discuss in detail below.

¹ In this Declaration, I refer to the written portions of a U.S. patent document by making reference to the column:line number of the patent. I refer to the written portions of an EP patent application publication by making reference to the paragraph number. For all other documents, I refer to the page number of the exhibit.

IV. LEGAL STANDARDS FOR PATENTABILITY

20. I am not an attorney and I offer no opinions on the law itself. My understanding of the relevant legal principles in this section is based on information provided to me by counsel.

1. Obviousness

21. I have been informed by counsel that a patent claim may be found invalid under 35 U.S.C. § 103(a) if the subject matter of the claim as a whole would have been obvious to a hypothetical person of ordinary skill in the art in view of a prior art reference or in view of a combination of references at the time of the alleged invention. I have been informed that obviousness is determined from the perspective of a person of ordinary skill in the art and that the Challenged Claims should be read from the point of view of such a person at the time the alleged invention was made. I have also been informed that a person of ordinary skill in the art is assumed to know and to have all relevant prior art in the field of endeavor covered by the patent in suit, and would thus have been familiar with each of the references cited herein, as well as the background knowledge in the art discussed in IX, and the full range of teachings they contain.

22. I have been informed of two criteria for determining whether a prior art reference is analogous and therefore qualifies as prior art: (1) whether the art is

from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of endeavor of the challenged claims, whether the reference still is reasonably pertinent to the particular problem which the Challenged Claims purport to address. I have additionally been informed that the field of endeavor of a patent is not limited to a specific point of novelty, the narrowest possible conception of the field, or the particular focus within a given field. I have also been informed that a reference may be reasonably pertinent if, even though it may be in a different field, it is one which logically would have commended itself to a patentee's attention in considering his problem because of the subject matter with which it deals.

23. I have further been informed that whether an alleged invention would have been obvious should be analyzed in view of the scope and content of the prior art, the differences (if any exist) between the prior art references and the alleged invention, and the level of ordinary skill in the pertinent art involved. I have been additionally been informed that a prior art reference should be viewed as a whole when performing the above analysis.

24. I have been informed that in considering whether a claimed combination would have been obvious, I may assess whether there were apparent reasons to combine elements in the prior art in the manner claimed in view of interrelated teachings of one or more prior art references, the impact of demands known to the

community or present in the market place, and/or the general knowledge possessed by a person of ordinary skill in the art at the time of alleged invention. I have been informed that other principles may be relevant in evaluating whether an alleged invention would have been obvious, and that these principles may include the following:

- A combination of prior art elements according to known methods is likely to be obvious when it does nothing more than yield predictable results;
- When a known device or technology is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or in a different one, so that if a person of ordinary skill in the art is able to implement a predictable variation, then that variation is likely obvious;
- If a known technique has been used to improve a device, method, or product, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same predictable way, using the technique is obvious unless the actual implementation of the technique is beyond his or her skill;
- An explicit or implicit teaching, suggestion, or motivation in the prior art to combine the prior art references to form the claimed combination may

demonstrate obviousness (but a teaching, suggestion, or motivation to combine is not a requirement for proving obviousness);

- Market demand, rather than scientific literature, can drive design trends and may show obviousness;
- In determining whether the subject matter of a patent claim would have been obvious, neither the motivation nor the purpose of the named inventor controls;
- The subject matter of a patent may be proved obvious by demonstrating that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims;
- Any need or problem known in the field and addressed by the prior art can provide a reason for a person of ordinary skill in the art at the time of the invention to combine the elements in the manner claimed;
- "Common sense" indicates that known items and methods may have obvious uses beyond their primary purposes, and in many cases, a person of ordinary skill in the art would be able to fit the teachings of multiple prior art references together similar to the pieces of a puzzle;
- A person of ordinary skill in the art is also a person of ordinary creativity, and is not an automaton;

- A patent claim may be proved obvious by demonstrating that the claimed combination of elements was “obvious to try,” especially when there exists a design need or market pressure to solve the problem and there are a limited number of identified, predictable solutions such that person of ordinary skill in the art would have had good reason to pursue the known options within his or her technical grasp; and
- One should be careful of relying on hindsight in evaluating whether an alleged invention would have been obvious.

25. I have further been informed that, in making a determination as to whether or not the alleged invention would have been obvious to a person of ordinary skill in the art, the Board might consider the presence of additional objective or secondary factors, such as: commercial success of products which practice the purported invention; a long-felt but unsolved need; teaching away; unexpected results; copying; and industry praise. These factors are typically referred to as “secondary considerations” or “objective indicia” of nonobviousness. I have been informed, however, that for such objective indicia or secondary evidence to be relevant to the obviousness analysis, there must be a causal relationship (known as a “nexus”) between the challenged claim and the objective indicia evidence and that this nexus must be based on what is claimed and novel in the claim, and not something in the prior art. I have also been informed by counsel that even when

objective indicia evidence is present, these secondary considerations may be unable to overcome sufficiently strong primary evidence showing obviousness (*e.g.*, motivation to combine with predictable results).

26. I have been asked by counsel to analyze the patentability of Claims 1-3 and 6-13 (the “Challenged Claims”) of the ’253 patent challenged in the above-referenced Petition. I have been informed that for *Inter Partes* Review (IPR) trials, unpatentability must be shown under a preponderance of the evidence standard. I have been informed that to establish something by a preponderance of the evidence one need only to prove it is more likely true than not true. I have concluded that challenged claims 1 and 23 are unpatentable at least under 35 U.S.C. § 103 based on *Cummins* in view of *Rauhala*; that claim 29 is unpatentable under 35 U.S.C. § 103 based on *Rauhala* in view of *Meador*; claim 30 is unpatentable under 35 U.S.C. § 103 based on *Rauhala* in view of *Meador*, and further in view of *Furuno* under both the preponderance of the evidence standard as well as the higher standard of clear and convincing evidence. I have also concluded that challenged claims 1 and 23 are unpatentable at least under 35 U.S.C. § 103 based on *Cummins* in view of *Rauhala*, and further in view of *Saito*; that claim 29 is unpatentable under 35 U.S.C. § 103 based on *Rauhala* in view of *Meador*, and further in view of *Saito*; claim 30 is unpatentable under 35 U.S.C. § 103 based on *Rauhala* in view of *Meador*, and further in view of *Saito* and *Furuno* under both the preponderance of

the evidence standard as well as the higher standard of clear and convincing evidence.

V. LEVEL OF ORDINARY SKILL IN THE ART

27. I understand that certain issues relating to patent validity must be judged from the perspective of a person of ordinary skill in the relevant art, as I discuss below in my report.

28. Also as discussed below, the invention of the '330 patent relates to processes and circuits used in wireless transceivers, among other things, to reduce power dissipation and thus improve battery life.

29. Based on my knowledge and experience, I understand what a person of ordinary skill in the art would have known at the time of the alleged invention (as I mentioned above). My opinions herein are, where appropriate, based on my understanding of the perspective of a person of ordinary skill in the art at that time. In determining the level of ordinary skill, I have been asked to consider, for example, the types of problems encountered in the field, prior solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the education level of active workers in the field.

30. In my opinion, based on the materials and information I have reviewed, and based on my experience in the technical areas relevant to the '330 patent, a person

of ordinary skill in the art at the time of the alleged invention of the '330 patent would have had a bachelor's degree in electrical engineering, electronics engineering, or the equivalent, and two or more years of experience in wireless communication devices including transceivers and circuitry thereon. This level of skill is approximate. Significantly more practical experience could also qualify one not having the aforementioned education as a person of ordinary skill in the art, while, conversely, a higher level of education could offset a lesser amount of practical experience.

31. I provide my analysis of the '330 patent, the prior art, and my opinions in this Declaration from the perspective of a person of ordinary skill in the art, as I have defined it above, during the relevant time frame stated above (i.e., March 2003), where appropriate.

VI. TECHNICAL BACKGROUND

32. In this section, I discuss the state of the art relevant to the subject matter of the '330 patent, as would have been known, understood, and appreciated by a person of ordinary skill in the art at the time of the alleged invention of the '330 patent. In particular, a person of ordinary skill in the art would have been aware of various developments in the area of wireless communication devices including transceivers and circuitry thereon, as I discuss below.

33. In the 1990s, if not earlier, a person of ordinary skill in the art would have known that the quality of a signal in a radio receiver can be improved by reducing noise and interference to the signal, and that one way to reduce noise and interference is “widening of the linear range of amplifiers and mixers” in the radio receiver by increasing either the operating voltage or the supply current. Ex. 1004 at [0003] However, a disadvantage associated with this method was also known, particularly in the event that the “circuits are specified such that the signal quality requirements will be met even in poor noise and interference conditions.” *Id.* Under such circumstances, the increased operating voltage or supply current would be sustained even when the noise and interference conditions are relatively weak, resulting in “a relatively large supply of energy” which “shortens the battery life.” *Id.*

34. It also was well known that, when the received signal is weak, the signal quality can be improved and intermodulation products can be reduced using “a method in which the strength of the received signal is monitored and the supply current of the mixer is increased if the signal strength of the signal drops.” *Id.* at [0004]. However, a person of ordinary skill in the art would have also recognized a disadvantage associated with such a method, namely that “the supply current will be increased even if the receiver received no other, interfering, signals,” and that

the amplifiers in the receiver will consume “a relatively large continuous current” as “the amplifiers have to be rated for the worst case.” *Id.*

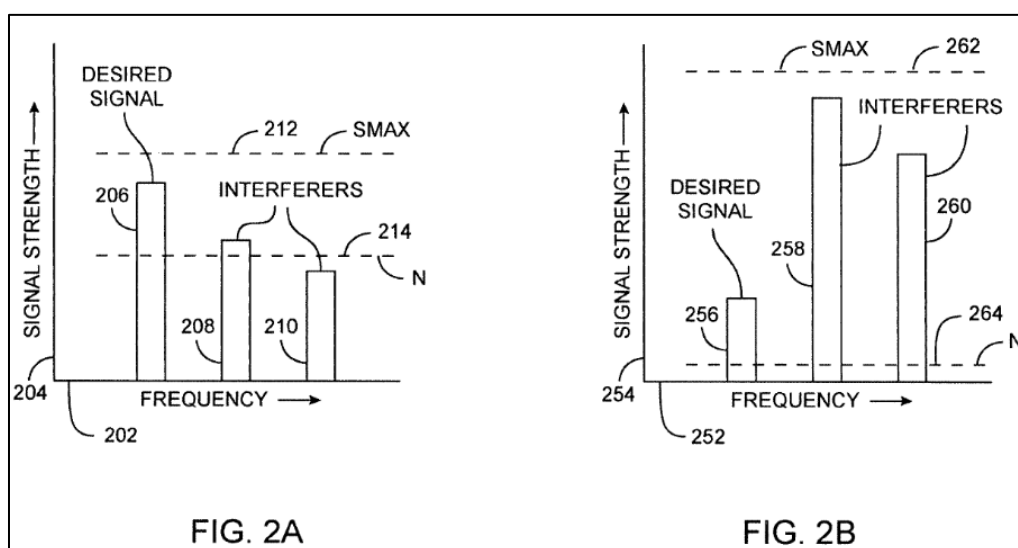
35. In at least 1999, if not earlier, methods and techniques were known for alleviating or minimizing the aforementioned disadvantages, namely power dissipation resulting from a relative large, continuous supply of energy within the receiver, even when the noise and interference conditions do not warrant the increased energy supply. For example, it was well known to keep “the supply currents of the receiver’s front-end amplifiers and at least the first mixer ... relatively low” under “normal conditions i.e., when the signal strength is satisfactory on the receive channel and ordinary on the neighboring channels,” and to increase the supply current “[i]f the signal strength goes below a certain value on the receive channel or exceeds a certain value on a neighboring channel.” *Id.* at [0006]. In this way, the currents supplied to the components of the receiver can be adjusted based on the varying signal conditions. The advantage of such technique was also well known, that “the energy consumption of the receiver can be reduced without degrading the signal quality,” which “means longer life for the battery or, if the life of the battery is kept unchanged, that a smaller battery can be used.” *Id.* at [0007].

36. Thus, the benefits of reduced power dissipation and improved battery life resulting from adjusting currents supplied to components within a radio receiver

based on varying signal conditions were well-known at least a few years prior to the date of the alleged invention, as further indicated by the prior art references I detail below.

VII. THE '330 PATENT

37. The '330 patent describes methods and circuits for reducing power dissipation in wireless transceivers and other electronic circuits and systems. Ex. 1001 at 1:52-55.



38. With reference to FIGS. 2A-2B reproduced above, the '330 patent discloses that “desired signals, interferers, and noise ... may be received by one of the various circuits in a wireless receiver.” *Id.* at 5:28-30. The '330 patent describes that “[i]n the example of FIG. 2A, a received desired signal 206 is large in comparison to interfering signals 208 and 210” and “the acceptable noise floor 214 is relatively high, while maximum signal handling capability Smax 212 (that is the

maximum signal power that can be handled with an acceptable low distortion) needs only to be high enough to accommodate the desired signal.” *Id.* at 5:33-46. In other words, the input spectrum described in FIG. 2A allows the circuit to have “a relatively small dynamic range for proper operation,” which means “the range between Smax 212 and the noise floor 214 is relatively small.” *Id.* at 5:46-50.

39. The ’330 patent describes the input spectrum in FIG. 2A as “that of the best-case input signal” including “a robust desired signal accompanied by no or low-level interferers.” *Id.* at 6:11-13. The ’330 patent goes to explain that, based on the strengths of the desire signal and the interferes shown in FIG. 2A, “the noise floor 214 may be allowed to rise, while the maximum signal handling capability Smax 212 may be reduced.” *Id.* at 6:13-15. In this way, “the receiver circuit may save significant power” because “the circuit’s impedances may be increased, thus reducing required drive currents.” and similarly, “bias currents may be lowered, thus reducing the maximum signal handling capability.” *Id.* at 6:15-20.

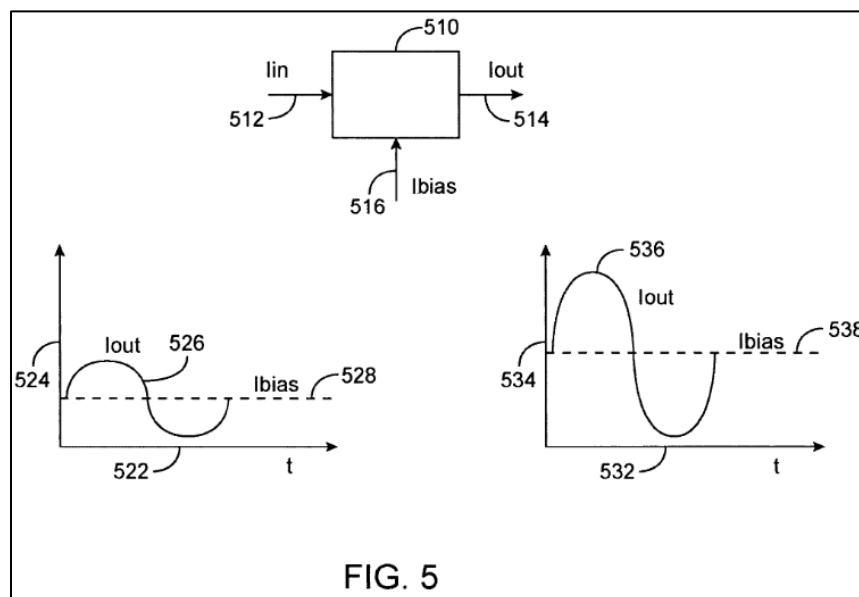
40. The ’330 patent goes on to describe the example of FIG. 2B, where “the desired signal 256 is relatively weak compared to the large interferers 258 and 260.” *Id.* at 5:51-53. Compared to the example of FIG. 2A discussed above, the circuit receiving the input spectrum depicted in FIG. 2B “should have a large dynamic range,” because “the noise floor 264 should be relatively low so as to prevent an unacceptable level of error in the recovery [of] the desired signal 256”

and “the maximum signal handling capability S_{max} 262 should be relatively high to accommodate the large interferers in order to avoid the creation of intermodulation products.” *Id.* at 5:53-63. The ’330 patent explains, with reference to a related figure i.e., FIG. 3, not reproduced herein, that reducing the maximum signal handling capability S_{max} under such circumstances may lead to “a mixing of interferers and the creation of intermodulation products ... one of which in this example occurs at the same frequency as the desired signal.” *Id.* at 6:36-40. Further, the ’330 patent discloses that the desired signal may be lost “if the intermodulation products ... become excessive,” and thus “care should be taken to avoid corruption of the received desired signal.” *Id.* at 6:40-46.

41. The ’330 patent describes that the input spectrum in FIG. 2B “is generally considered the worst-case input signal,” which may be addressed using a “typical design methodology involv[ing] designing a receiver for this condition, specifically the weakest desired signal accompanied by largest interference level.” *Id.* at 6:3-7. For instance, “[c]ircuit impedances and currents are set such that the noise floor 264 is sufficiently low for an acceptable bit-error rate, while bias current are set sufficiently high for the required S_{max} 262.” *Id.* at 6:7-10.

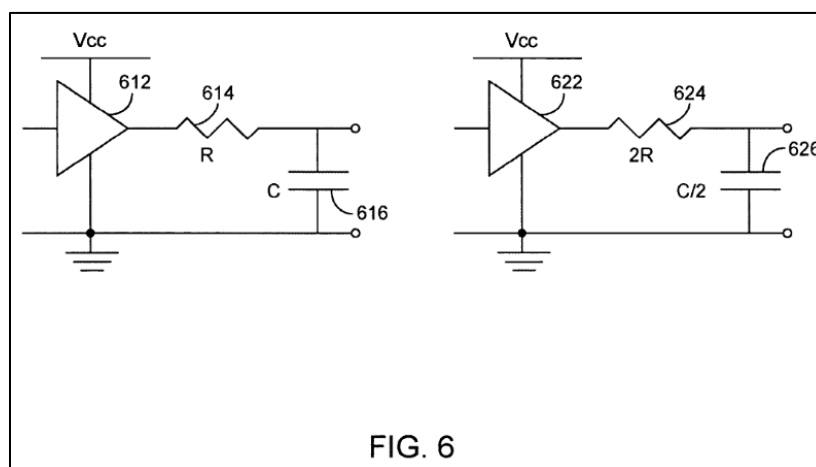
42. The ’330 patent further discloses that, because “[t]he minimum power dissipation for a circuit is proportional to the required maximum signal-to-noise ratio, which is the ratio between S_{max} 212 or 262 and N 214 or 264,” a circuit

receiving an input signal similar to the one shown in FIG. 2A “can dissipate less power than one receiving the input as shown in FIG. 2B, while still achieving an acceptable bit-error rate.” *Id.* at 6:21-27.



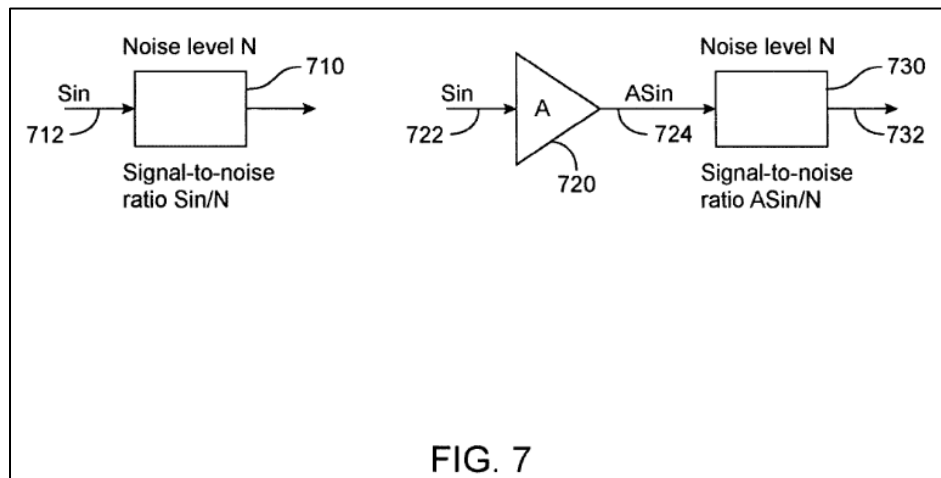
43. With reference to FIG. 5 reproduced above, the '330 patent describes “the relationship between a required bias[] current 516 for a given output signal 514 for a representative circuit 510.” *Id.* at 7:24-26. The '330 patent explains that, “[i]f the output signal current level is relatively low, such as the output current shown as 526, the corresponding bias current 528 may be low.” *Id.* at 7:26-31. On the other hand, “if the output signal current level is larger as with the example 536, the corresponding bias current level 538 should also be high.” *Id.* at 7:29-31. The '330 patent further discloses, “if a bias current is initially set high to handle ... a large input signal, for example a large interferer, this current may be reduced if the input

signal is smaller.” *Id.* at 7:31-34. The ’330 patent discloses ways to reduce the bias current, such as by increasing a resistance “by opening switches across portions of the resistance,” or lowering the bias voltage applied at the base of the device. *Id.* at 7:39-41. The ’330 patent further acknowledges that “[s]everal ways in which this may be done,” namely reducing the bias current, “will be readily understood by one skilled in the art.” *Id.* at 7:42-43.



44. The ’330 patent discusses one such example method of reducing bias currents in a circuit. With reference to FIG. 6 reproduced above, the ’330 patent discloses that “a circuit’s impedances may be scaled to reduce drive currents, and, depending on the circuit configuration used, associated bias currents as well.” *Id.* at 7:44-46. Drivers 612 and 622 have the same frequency response, but “the impedance of the load seen by driver 622 is double that seen by 612, thus the output current required by the driver 622 is reduced by one-half.” *Id.* at 7:47-52. The ’330 patent discloses, when “the output stage of each of these drivers [is]

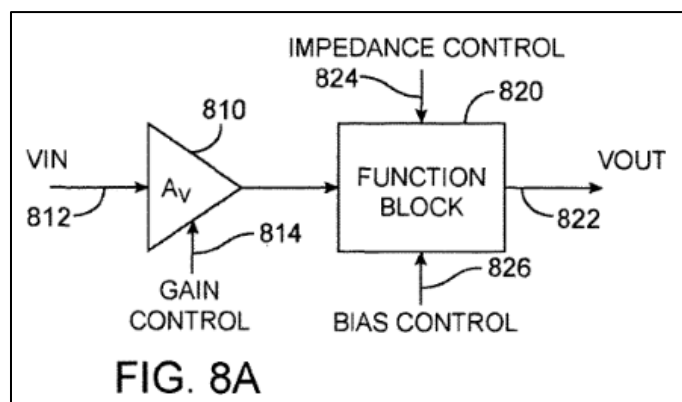
... a Class A emitter follower formed by an emitter follower connected to a current source” and the outputs of the drivers are driven high, “the emitter of driver 622 need supply only one-half the drive current as driver 612.” *Id.* at 7:53-57. In this way, “an impedance can be scaled in order to decrease a circuit’s required drive current.” *Id.* at 7:57-59. The ’330 patent further discloses that “the bias current, that is the current in the pull-down current source can be reduced.” *Id.* at 7:63-65. The ’330 patent again acknowledges that “[m]any other examples where drive currents and possibly bias currents may be reduced will be appreciated by one skilled in the art.” *Id.* at 7:65-67.



45. The ’330 patent discusses another example method of reducing bias currents in a circuit. With reference to FIG. 7 reproduced above, the ’330 patent discloses “a gain element 720 may be inserted in front of a circuit block 730 in order to improve the combined circuit’s signal-to-noise ratio by a factor equal to the gain of the inserted gain block.” *Id.* at 8:3-6. This method is “particularly useful when

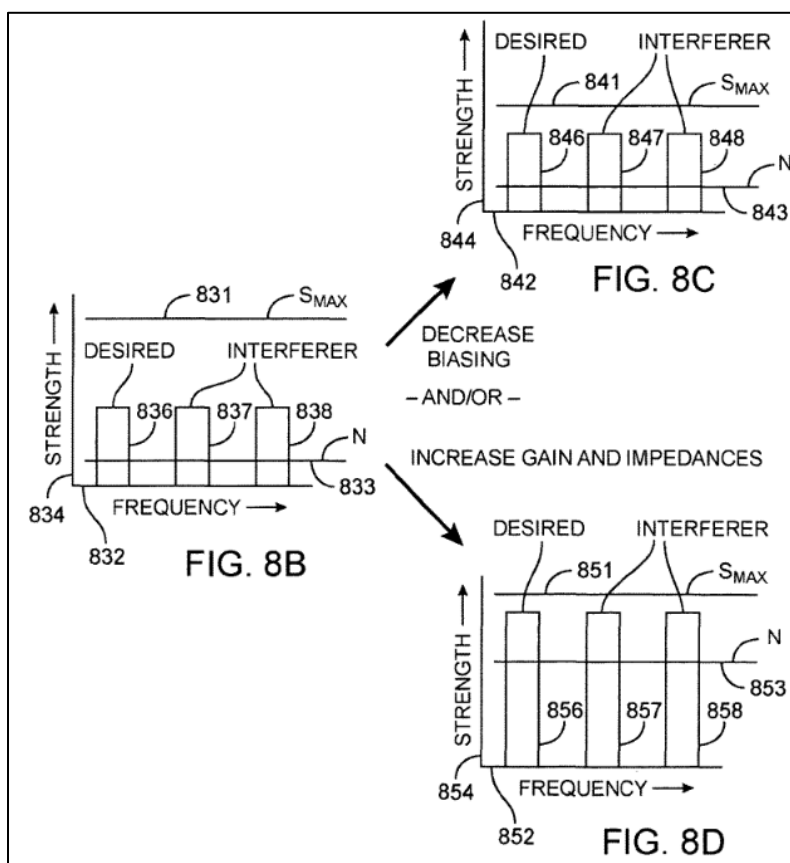
large interferers are absent and the desired received signal is moderate or low,” and “a given signal-to-noise ratio may be maintained while the power is decreased.” *Id.* at 8:6-11. The '330 patent discloses that the gain “may be varied by increasing a current in a differential pair or increasing a load resistance using switches,” and also acknowledges that “[m]any other examples where the gain ... may be varied will be appreciated by one skilled in the art.” *Id.* at 8:12-16.

46. The '330 patent then describes different ways to configure one or more circuits in the transceiver under varying signal conditions, in order to reduce power dissipation. *Id.* at 8:20-10:56. Particularly, the '330 patent discloses that “[t]he included examples are explained for the exemplary situation where biasing and other parameters are set for worst-case conditions, and then changed to save power when it is discovered that the conditions are better-than-worst case.” *Id.* at 9:29-33.



47. First, with reference to FIG. 8A reproduced above, the '330 patent illustrates “a block diagram of a functional block 820 and optional gain element 810,” where “[f]unctional block 820 ... may be a filter, mixer, amplifier, or other circuit or

circuits in a wireless transceiver or other electronic circuits or system” and “[t]he gain of the optional gain element 81[0] is controlled by a gain control signal on line 814.” *Id.* at 8:20-30. The ’330 patent explains that “[a]n input signal is received on line 812 by the optional gain element 824” and “[w]hen the optional gain block 810 is not used, the input signal may be received directly by the function block 820.” *Id.* at 8:25-28. Then, the ’330 patent explains that “[t]he functional block receives an output signal from the optional gain element 810 and provides an output VOUT on line 822.” *Id.* at 8:30-32. The ’330 patent further explains that “[o]ne or more impedances are under control of signals on impedance control lines 824” and “[o]ne or more bias currents in the function block are under control of one or more signals on bias control lines 826.” *Id.* at 8:36-39.

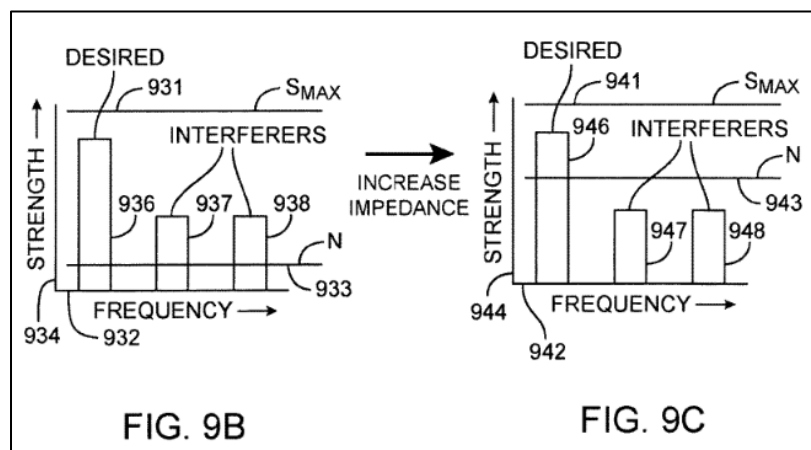


48. With reference to FIG. 8B reproduced above, the '330 patent illustrates "an example input that may be present on line VIN 812," where "a desired signal 836 is relatively weak, as are interfering signals 837 and 838." *Id.* at 8:46-48. As discussed above, the '330 patent explains that "[t]he initial bias and circuit configuration is such that the noise floor 833 and maximum signal handling capacity S_{max} 831 are adjusted for worst case conditions." *Id.* at 8:48-51. The '330 patent then discloses "at least two methods by which the power dissipation for this circuitry may be reduced." *Id.* at 9:1-3.

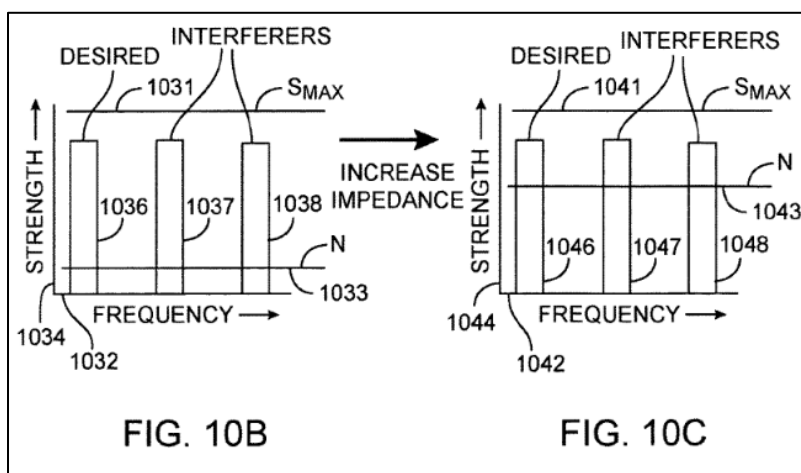
49. For example, with reference to FIG. 8C reproduced above, the '330 patent discloses a first method of reducing power dissipation, where “the bias current is decreased, thereby lowering the maximum signal handling capability 841 as compared to 831, closer to the desired and interfering signal levels.” *Id.* at 9:5-7. The '330 patent again discloses, as discussed above, that “the bias currents ... may be reduced by switching impedances that appear across a voltage thereby changing a resulting bias current ... or by other methods.” *Id.* at 9:8-12. As another example, with reference to FIG. 8D reproduced above, the '330 patent discloses that power dissipation may be reduced by “increasing one or more impedance[s] in function block ... such that drive currents inside that block are reduced,” which “may allow some biasing currents to be reduced.” *Id.* at 9:22-25. This method may have an effect on the circuit such that “S_{max} 851 is held constant as compared [to] S_{max} 831,” “[t]he desired an interfering signals are amplified such that they are closer to the available signaling handling capability 851,” and “the noise floor 853 is raised as compared to noise floor 833.” *Id.* at 9:15-19.

50. The '330 patent also applies the setup illustrated in FIG. 8A, including the gain block, gain control, function block, bias control, and impedance control, to additional example signal conditions discussed below. In other words, each of the subsequent FIGs. 9A, 10A, and 11A in the '330 patent, which is applicable under a

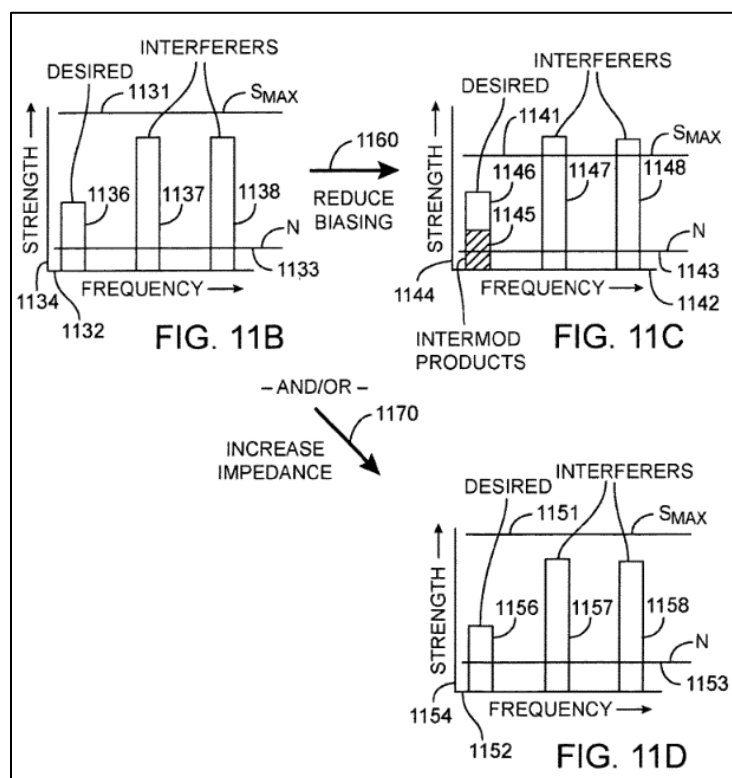
separate and distinct signal condition, is identical to FIG. 8A discussed above, and the same discussion will not be repeated below.



51. With reference to FIG. 9B reproduced above, the '330 patent "shows a spectrum for what may be considered a best-case received signal," where "the desired signal 936 is strong, while the interfering signals 937 and 938 are relatively weak." *Id.* at 9:42-45. The '330 patent explains that, in FIG. 9B, "[t]he maximum signaling capability 931 and noise floor 933 are shown as being set for the worst case conditions," in which "the noise floor 933 is lower than the maximum allowed for proper signal reception." *Id.* at 9:50-53. Therefore, the '330 patent discloses that "one or more impedance[s] in the function block ... may be increased, such that the noise floor 943 rises," as shown in FIG. 9C reproduced above. *Id.* at 9:53-55. The '330 patent further discloses that the increased impedance may also lead to the reduction of "one or more of the driving currents" and "one or more bias current[s]." *Id.* at 9:55-58.



52. With reference to FIG. 10B reproduced above, the '330 patent illustrates "a received signal that may be received on line VIN," where "the desired signal 1036 and interferers 1037 and 1038 are each relatively large." *Id.* at 10:1-3. Again, the '330 patent explains that "the noise floor 1033 and maximum signal handling capability 1031 are initially set for the worst case conditions." *Id.* at 10:8-10. The '330 patent further explains, with reference to FIG. 10C reproduced above, "[s]ince the desired signal is relatively large ... the noise floor may be allowed to rise, a[s] shown by noise floor 1043," and "[s]ince the desired signal 1046 and interferers 1047 are large, the maximum signal handling capability S_{max} 1041 remains constant." *Id.* at 10:12-15. The '330 patent then discloses "the noise floor is increased by increasing impedances in the function block," which "reduces the required drive current, and may allow for a reduction in bias current," leading to reduced power dissipation. *Id.* at 10:15-18.



53. With reference to FIG. 11B reproduced above, the '330 patent illustrates “an exemplary input signal that may be received by the gain control element ... on line VIN,” where “the desired signal 1136 is relatively low or weak while the interfering signals 1137 and 1138 are large.” *Id.* at 10:27-31. Again, the '330 patent explains that “the maximum signal handling capability 1131 and the noise floor 1133 are initially set for worst case conditions.” *Id.* at 10:37-38. Then, the '330 patent further explains that, although “power savings may not be achievable over the worst case settings,” for example when “the desired signal is sufficiently low, while the interferers are sufficiently high,” there may be at least two different

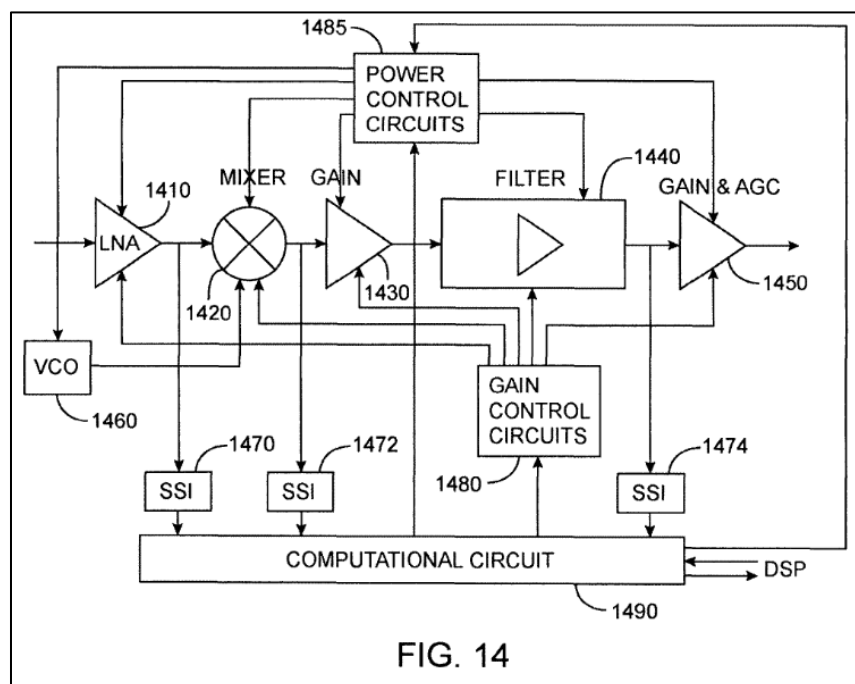
ways to save power “if the desired signal is somewhat larger than the worst case condition.” *Id.* at 10:38-44.

54. For example, with reference to FIG. 11C reproduced above, the ’330 patent discloses one of the ways to reduce power dissipation, where “the maximum signal handling capability 1141 [is] lowered.” *Id.* at 10:45-46. The ’330 patent further discloses that, although lowering the maximum signal handling capability may “clip and distort” the interfering signals, “thereby creating intermodulation products 1145, which distort the desired signal 1146,” power may still be reduced “[s]o long as care is taken to not corrupt the desired signal 1146 beyond an acceptable limit, typically measured by a bit-error rate.” *Id.* at 10:46-52. As another example, with reference to FIG. 11D reproduced above, the ’330 patent discloses that power may be saved by raising the noise floor 1153, “so long as the noise floor is not sufficiently high that the system bit-error rate becomes unacceptable.” *Id.* at 10:53-56.

1210 RECEIVED SIGNAL		1220 RESPONSE TO RECEIVED SIGNAL		
SIGNAL STRENGTH	INTERFERER STRENGTH	DECREASE S _{MAX}	INCREASE IMPEDANCE <u>NOT</u> GAIN	INCREASE IMPEDANCE <u>AND</u> GAIN
1230 SMALL	SMALL	YES	NO	YES
1240 LARGE	SMALL	NO	YES	NO
1250 LARGE	LARGE	NO	YES	NO
1260 SMALL	LARGE	NO	NO	NO

FIG. 12

55. The '330 patent then provides a summary of the above-discussed four examples, with reference to FIG. 12D reproduced above.



56. With reference to FIG. 14 reproduced above, the '330 patent provides an illustration of “a portion of a receiver consistent with an embodiment.” The '330

patent discloses that the receiver includes “low-noise amplifier 1410, mixer 1420, gain stage 1430, filter 1440, AGC amplifier 1450, and VCO 1460,” and that the signal strength detection is performed at signal strength indicators 1470, 1472, and 1474. *Id.* at 11:42-47. The ’330 patent further discloses “computational circuit 2470, which in turn controls gain and power control circuits 1480 and 1485” based on the outputs of the signal strength indicator circuits. *Id.* at 11:47-50. Power and gain control circuits 1480 and 1485 then “control the gain, biasing, and impedance levels of the circuits in the receiver signal path.” *Id.* at 11:50-53.

VIII. CLAIM CONSTRUCTION

57. I understand that claim terms are typically given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art, at the time of the alleged invention, which I was asked to assume was in March of 2003. In considering the meaning of the claims, I also understand that one must consider the claim language, specification, prosecution history, and the knowledge of a person of ordinary skill in the art at the relevant time. I have followed these principles in my analysis and provide my opinions with regard to construction of particular terms of the claims below.

A. “dynamically changing” and “dynamically adjust[ed]”

58. The '330 patent uses the phrase “dynamically adjusted” interchangeably with “dynamically changing,” and uses these terms to describe instances in which a second parameter (e.g., an impedance, a bias current, a gain, etc.) is adjusted/changed “based on” or “in response to” a first parameter (e.g., signal strength). See Ex. 1001 at 2:11-15, 22-25, 33-37, 46-48, 57-59 and 2:66 to 3:3.

59. It is my opinion that this term means “adjusting during operation based, at least in part, on information gained during operation.” This construction is consistent with the specification of the '330 patent, the claims, and prosecution history.

60. This construction is supported throughout the specification of the '330 patent. Describing embodiments, the '330 patent repeatedly refers to receiver circuit parameters as “dynamically adjusted” or “dynamically changing” in response to measured conditions. For example, the '330 patent states:

The method itself includes **determining** a first signal strength at a first node in the signal path in the integrated circuit and **dynamically changing** an impedance of a component in the signal path **based on** the first signal strength.

...

The method itself includes **determining** a first signal strength at a first node in the signal path in the integrated circuit and **dynamically changing** a bias current in the signal path **based on** the first signal strength.

...

The method further includes **dynamically changing** a gain of the first circuit **based on** the first signal strength and **dynamically changing** an impedance of a component in the second circuit **based on** the first signal strength.

...

An impedance in the signal path is configured to be **dynamically adjusted in response to** the first signal strength.

...

A bias current in the signal path is configured to be **dynamically adjusted in response to** the first signal strength.

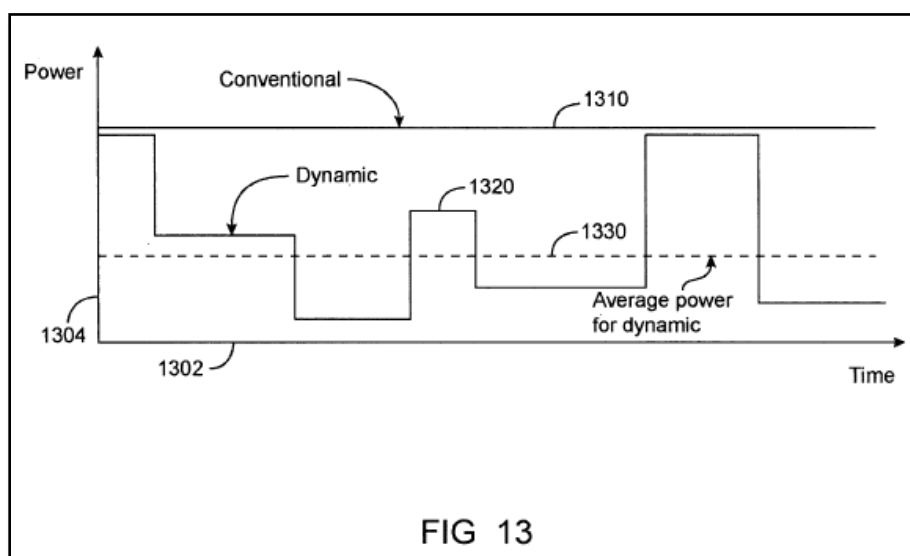
...

A gain of the first circuit is configured to be **dynamically adjusted in response to** the first signal strength, and an impedance in the second circuit is configured to be **dynamically adjusted in response to** the first signal strength.

Ex. 1001 at 2:11-15, 22-25, 33-37, 46-48, 57-59 and 2:66 to 3:3 (emphases added).

61. A person of ordinary skill would have understood from the specification that the signal strength is identified or measured during operation of the system and that that the responsive adjustment occurs during operation of the system, in order to allow the system to “adapt to a better-than-worst-case condition and reduce circuit currents and therefore power dissipation.” Ex. 1001 at 1:46-48. Otherwise, the adjustment would not achieve the supposed benefits (reduced circuit currents and improved power dissipation) touted by the ’330 patent.

62. This construction is also supported by Figure 13, reproduced below, of the ’330 patent. Figure 13 illustrates an example of dynamic adjustment of circuit parameters allegedly resulting in “dynamic power dissipation.” Ex. 1001 at 11:35-39. Power is shown on the Y axis of Figure 13, while time is shown on the X axis. Ex. 1001 at FIG. 13.



63. The '330 patent states that “control of variable gains, impedances, biasing, or combination thereof, allows for a lower average power” dissipation. Ex. 1001 at 11:35-39. A person of ordinary skill would have understood that Figure 13 shows that “dynamic power dissipation” occurs in discrete steps, as opposed to along a continuous curve, and in contrast with “conventional” power dissipation, which is depicted as a straight line (*i.e.*, static). A person of ordinary skill in the art would have understood from Figure 13 and the accompanying description in the specification that “**dynamic** power dissipation” is simply power dissipation that varies over time.

64. Moreover, the proposed construction is consistent with the context of the claims of the '330 patent. For example, claim 1 recites:

determining a first signal strength at a first node in the signal path in the integrated circuit; and

reducing a switching current in the signal path by **dynamically changing** an impedance of a component in the signal path **based on** the first signal strength.

65. Ex. 1001 at 12:63-67 (emphases added). Other claims are structured similarly:

- Claim 23: a first signal strength indicator circuit coupled to the signal path, and configured to **determine a first signal strength**; wherein an impedance in the signal path is configured to be **dynamically adjusted** to reduce a switching current **in response to** the first signal strength.

Id. at 14:23-28 (emphases added).

- Claim 29 recites: a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength; wherein a gain of the first circuit is configured to be **dynamically adjusted in response** to the first signal strength, and wherein an impedance in the second circuit is configured to be **dynamically adjusted in response** to the first signal strength.

Id. at 16:4-12 (emphases added).

66. In the context of the claims, a person of ordinary skill would have understood “dynamically adjust[ed]” and “dynamically changing” to mean adjusting during operation (while receiving a wireless signal) based, at least in

part, on information (signal strengths and/or comparisons thereof) gained during operation.

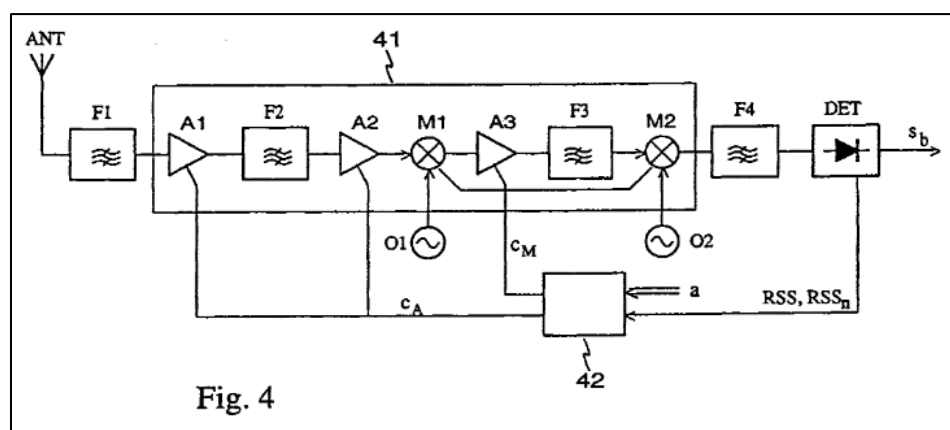
67. Even if the term “dynamically adjusting” is not construed to mean “adjusting during operation based, at least in part, on information gained during operation,” it is still my opinion that the challenged claims are unpatentable. Even under a narrower construction, the cited references would still render the challenged claims unpatentable. *See, e.g., supra* Sections XIV and XV.

IX. OVERVIEW OF THE PRIOR ART

1. *Rauhala* (Ex. 1004)

68. *Rauhala* discloses “a method and an arrangement for linearizing a radio receiver,” to be “applied in the reception circuit of mobile stations.” Ex. 1004 at [0001]. Particularly, *Rauhala* discloses techniques for minimizing certain disadvantages in prior art, namely power dissipation resulting from requiring “a relatively large supply of energy” or “a relatively large continuous current” even when signal conditions at a particular time do not warrant such a large energy supply. *Id.* at [0004]. To that end, *Rauhala* generally discloses the concept of varying the currents supplied to appropriate circuit components based on the condition of the detected signals, which include a signal in a receive channel and a signal in a neighboring channel. For instance, *Rauhala* discloses “[i]n normal conditions, i.e. when the signal strength is satisfactory on the receive channel and

ordinary on the neighboring channels, the supply currents of the receiver's front-end amplifiers and at least the first mixer are kept relatively low" and "[i]f the signal strength goes below a certain value on the receive channel or exceeds a certain value on a neighboring channel, said supply currents are increased." *Id.* at [0006].



69. With reference to FIG. 4 reproduced above, *Rauhala* discloses “a simplified example of a radio receiver” that includes “linear units.” *Id.* at [0012]. The linear units are the amplifiers and mixers in the receiver. In FIG. 4, the amplifiers are designated as A1, A2, and A3 and the mixers are designated as M1 and M2. *Id.*

70. Particularly, with reference to FIG. 4, *Rauhala* discloses an example of how the currents supplied to the linear units are controlled. *Id.* at [0017]. First, “[a] control unit 42 receives from detect[or] DET an indication about either the receive channel signal strength RSS or the strength of any signal on the reception band.” *Id.* The receive channel signal strength is designated as “RSS” and the neighboring

channel signal strength is designated as “RSS_n.” *Id.* at [0013], [0017]. Each signal condition represented by the values of RSS and RSS_n dictates the levels (e.g., high and low) of the currents supplied to the linear units in the receiver. *Id.* at [0017].

	RSS _n	RSS	I _A	I _M
Row 1 →	<S _n	>S ₄	I _{Al}	I _{MI}
Row 2 →	<S _n	≤S ₄	I _{Ah}	I _{MI}
Row 3 →	≥S _n	>S ₄	I _{Ah}	I _{MI}
Row 4 →	≥S _n	≤S ₄	I _{Ah}	I _{Mh}

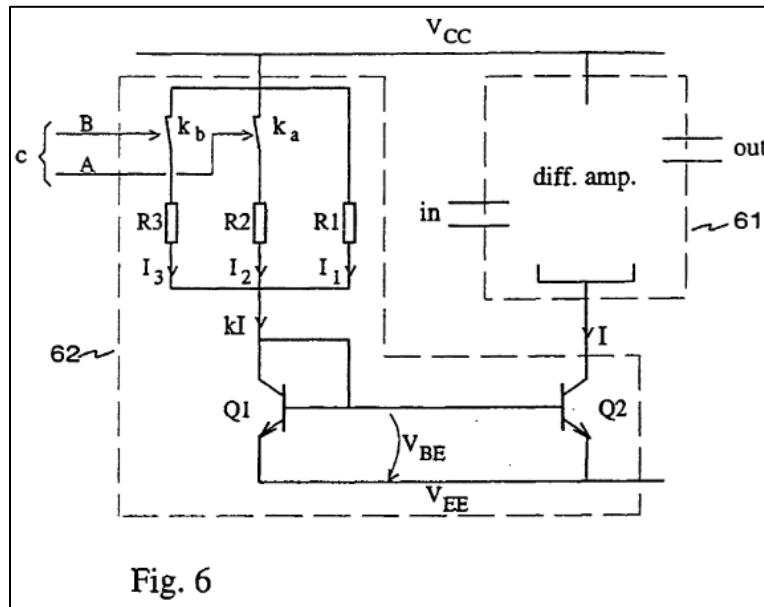
71. Specifically, with reference to the table reproduced above, *Rauhala* discloses different signal conditions and the levels of the currents to be supplied to the linear units under each of the different signal conditions. *Id.* at [0017]. In the table, S_n is a “threshold value ... which corresponds to a relatively high signal strength on the [neighboring] channel,” and S₄ is a “threshold value ... which corresponds to a relatively low receive signal strength.” *Id.* Further, the subindex A refers to “linear units A1 and A2,” meaning I_A is a current supplied to linear units A1 and A2, and the subindex M refers to “linear units M1, A3, and M2,” meaning I_M is a current supplied to linear units M1, A3, and M2. *Id.* Furthermore, the subindex 1 refers to a “lower supply current of the linear unit” and the subindex “h” refers to a “higher supply current.” *Id.* Thus, as an example, “I_{M1} means that the control current in mixers M1 and M2 and in amplifier A3 is set to the lower value.” *Id.*

72. With reference to the table above, *Rauhala* discloses “[w]hen the signal strength on the receive channel is normal or relatively high, and on the neighboring channels normal or relatively low,” which represents the best case signal condition corresponding to Row 1 in the table, “all linear unit supply current are set to the lower values.” *Id.* at [0018]. *Rauhala* further discloses “[w]hen the signal strength on the receive channel drops relatively low and on a neighboring channel relatively high,” which represents the worst case signal condition corresponding to Row 4 in the table, “the supply currents of all linear units are set to the higher values.” *Id.*

73. However, in other signal conditions that are neither best case nor worst base, the current levels supplied may vary between the linear units in the receiver. In other words, a current level supplied to one or more linear units may be different from a current level supplied to one or more other linear units. *Id.* For example, *Rauhala* discloses that “[w]hen the signal strength on the receive channel is at least normal, but relatively high on a neighboring channel,” which represents the condition corresponding to Row 3 in the table, “the supply currents of amplifiers A1 and A2 are set to the higher values and the supply currents of the other linear units to the lower values.” *Id.* Furthermore, *Rauhala* discloses, with reference to Row 2 in the table, a signal condition where the signal strength on the receive channel is relatively low and on the neighboring channels normal or relative low,

in which the supply currents of amplifiers A1 and A2 are set to the higher values and the supply currents of the other linear units to the lower values. *Id.*

74. *Rauhala* also discloses, based on a detected signal condition, the control circuit 42 “provides two one-bit control signals C_A and C_M ” to the amplifiers and mixers, each of the control signals indicating the level of current to be supplied to the receiving linear unit. *Id.* at [0017]. For example, *Rauhala* discloses “[s]ignal C_A is 0 when signal RSS is greater than S4 and signal RSS_n is at the same time smaller than S_n .” *Id.* Otherwise, signal C_A is 1. *Id.* With respect to signal C_M , *Rauhala* discloses that it is “1 when signal RSS is not greater than S4 and signal RSS_n is at the same time at least S_n .” *Id.* “Otherwise, signal C_M is 0.” *Id.* The bits 0 and 1 respectively represent low current and high current. *Id.* Signal C_A is provided to amplifiers A1 and A2, while signal C_M is provided to amplifier A3 and mixers M1 and M2. *Id.*



75. With reference to FIG. 6 reproduced above, *Rauhala* discloses an example of “a linear unit’s supply current control.” *Id.* at [0021]. The supply current control 62 is configured to vary the current supplied to the linear unit 61, by varying the impedance within the enclosed circuit. *Id.* Specifically, “[t]he supply current control circuit 62 comprises transistors $Q1$ and $Q2$, resistors $R1$, $R2$ and $R3$,” as well as switch k_a “in series with resistor $R2$ ” and switch k_b “in series with resistor $R3$.” *Id.* These “series connections are coupled in parallel with resistor $R1$,” forming a three-branch parallel connection. *Id.*

76. In the three-branch parallel connection, “the current of resistor $R1$ is I_1 , the current of resistor $R2$ is I_2 and the current of resistor $R3$ is I_3 .” *Id.* Accordingly, “the current kI of transistor $Q1$ is the sum $I_1+I_2+I_3$.” *Id.* The switches k_a and k_b are controlled based on the bits A and B , respectively, which are received from the

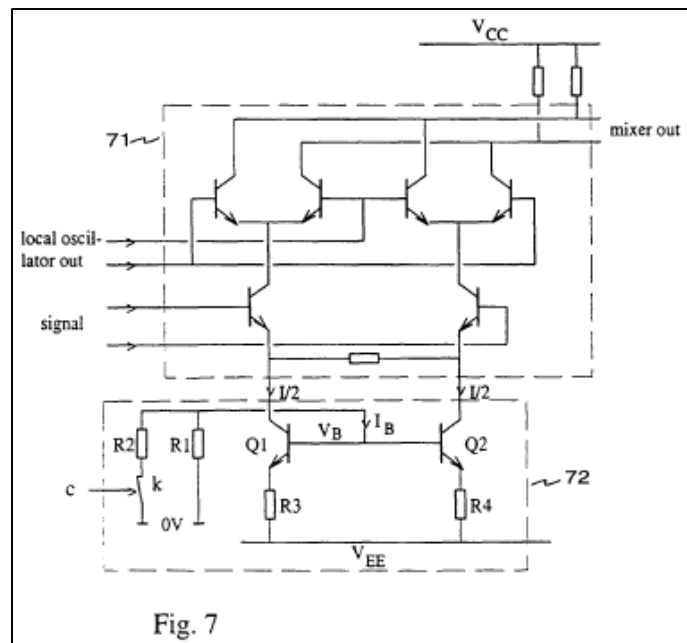
control unit 42. *Id.* For example, when a bit (e.g., A or B) is 0, the corresponding switch (e.g., k_a or k_b) is open, and when the bit is 1, the corresponding switch is closed. *Id.* at 5:4.

B	A	kI	kI/I_1
0	0	I_1	1
0	1	I_1+I_2	2 if $R1=R2$
1	0	I_1+I_3	3 if $R1=2 \cdot R3$
1	1	$I_1+I_2+I_3$	4 if $R1=R2=2 \cdot R3$

77. With reference to the table appearing after paragraph [0021], reproduced above, *Rauhala* discloses different two-bit digital signals (e.g., A and B) received at the supply current control 62 and the corresponding current kI of transistor Q1 generated based on each of the received signals. *Id.* The current I that is supplied to the linear unit 61 will be the same as kI by way of the “current mirror” configuration implemented in the supply current control 62. *Id.* *Rauhala* also discloses another example of a supply current control circuit in FIG. 7, which has a slightly different configuration compared to that of the supply current control circuit in FIG. 6 but follows a similar principle of varying the supply current by varying the impedance. *Id.* at [0022], [0023], FIG. 7.

78. *Rauhala* shows an example of controlling a linear unit's supply current. Ex. 1004 at [0023], FIG. 7. The linear unit 71 is an analog multiplier used as a mixer. *Id.* The mixer receives a RF or IF signal from a local oscillator. The mixer

produces a signal the spectrum of which includes the spectrum of the input signal shifted both upwards and down. *Id.* The control circuit 72 for the supply current I of the analog multiplier 71 includes transistors Q1 and Q2, resistors R1 and R2, and switch k. *Id.*



79. *Rauhala* discloses that the collector of transistor Q1 is coupled to the first branch of the analog multiplier 71, and the collector of transistor Q2 is coupled to the second branch of the analog multiplier. *Id.* The emitter of transistor Q1 and the emitter of transistor Q2 are both coupled to the negative voltage V_{EE} terminal of the voltage supply, the first via a resistor the resistance of which is relatively low, and the latter via resistor R4. *Id.* The bases of transistors Q1 and Q2 are coupled to one another. *Id.*

80. The emitter of transistor Q1 and the emitter of transistor Q2 are both coupled to the negative voltage V_{EE} terminal of the voltage supply, the first via a resistor the resistance of which is relatively low, and the latter via resistor R4. *Id.* The bases of transistors Q1 and Q2 are coupled to one another. *Id.* When the resistances of resistors R3 and R4 are identical and transistors Q1 and Q2 are identical, the collector currents of the transistors are also identical, i.e. half of the analog multiplier's 71 supply current I. *Id.*

81. Resistor R2 and switch k are coupled in series, and this series connection is coupled in parallel with resistor R1. *Id.* One end of the parallel connection is coupled to signal ground and the other end to the bases of transistors Q1 and Q2. *Id.* Switch k is controlled with a one-bit digital signal c. *Id.* When signal c is 0, switch k is open and the control current I_B of transistors Q1 and Q2 is $V_B/R1$, where V_B is the transistors' base voltage. *Id.* When signal c is 1, switch k is closed and the control current I_B is $V_B/R1 + V_B/R2$. Thus, the control current I_B increases, causing the supply current I to increase as well. *Id.* When signal c is 0 and the linear unit supply currents are at their higher values. *Id.*

82. *Rauhala* discloses that the control current I_B depends on the state of switch k. That is I_B is either $V_B/R1 + V_B/R2$ or $V_B/R1$. *Rauhala* discloses that as the control current I_B increases, the supply current I increases. *Id.*

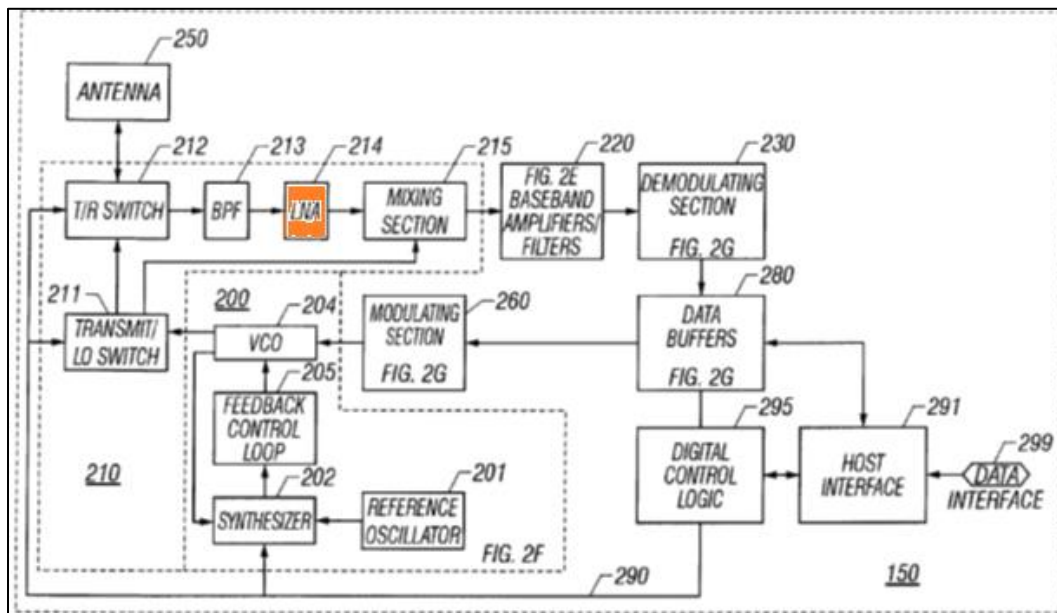
83. *Rauhala* further discloses that in FIG. 7, the resistances of resistors R3 and R4 are identical and transistors Q1 and Q2 are identical, and thus the collector currents ($I/2$) of the transistors are also identical, i.e. half of the analog multipliers 71 supply current I . *Id.*

84. In summary, *Rauhala* discloses a radio receiver including a supply current control circuit that is configured to control, based on a received digital signal indicative of a signal condition experienced by the receiver, currents supplied to amplifiers and mixers in the receiver, by varying the impedance of the circuit through adding or removing resistance. *Id.* at 5:1-15, FIG. 6, and FIG. 7.

2. Cummins (Ex. 1005)

85. *Cummins* discloses “[a] method of receiving a signal using an integrated circuit.” Ex. 1005 at 5:33-37. For example, *Cummins* discloses “a radio frequency (RF) transceiver for data communication.” *Cummins* discloses that a transceiver 150 is on an integrated circuit as it “is disposed within a PCMCIA format package described above, with an antenna, RF and digital circuitry integrated on a single printed circuit board (PCB) disposed within the PCMCIA package.” *Id.*

86. *Cummins* discloses “low noise amplifier (LNA) 214 for amplification before being applied to [a] mixing section 215”. Ex. 1005 at 6:1-2 and FIG. 2F (annotated below).

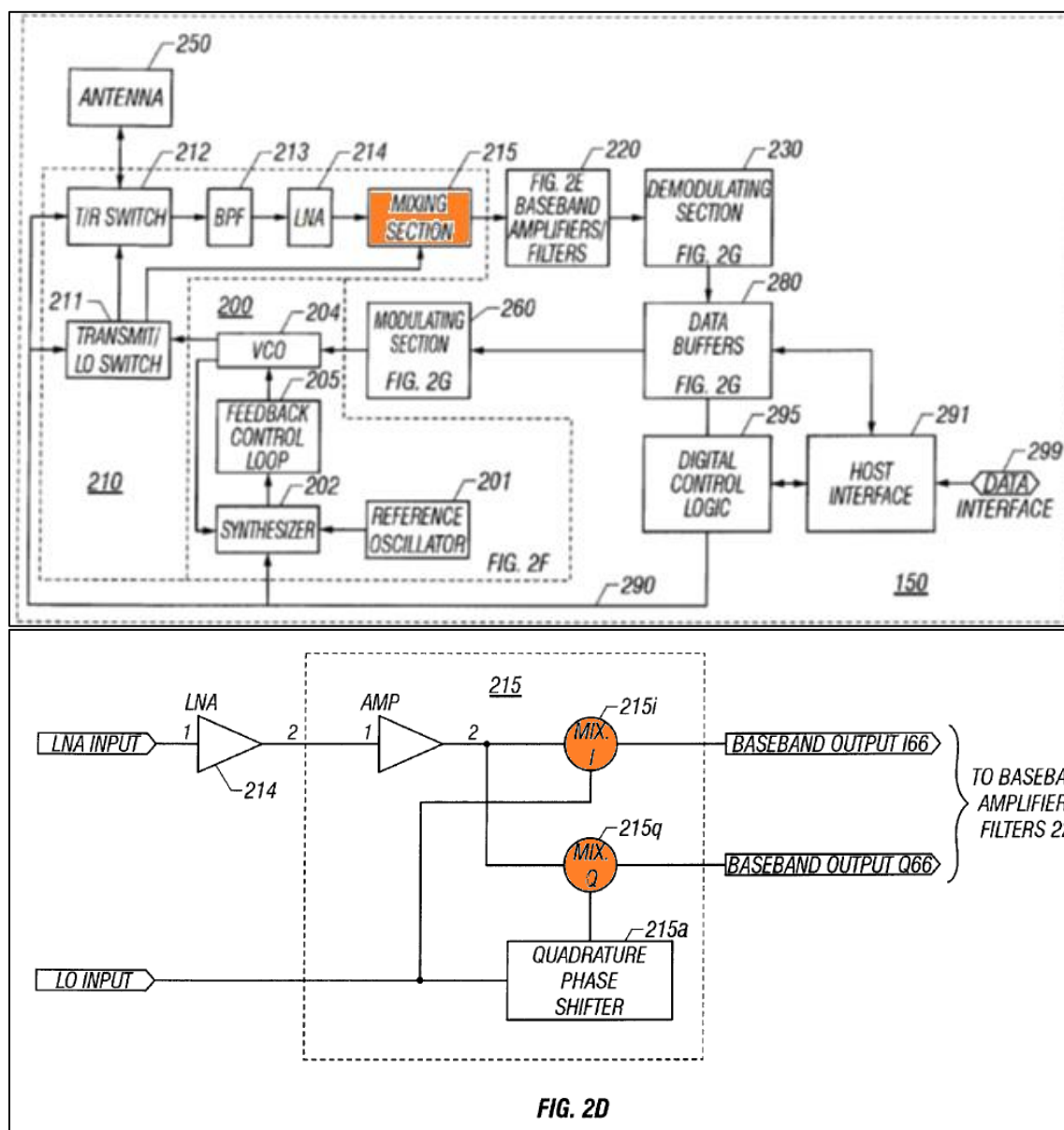


87. Cummins discloses a mixer having an input coupled to an output of the low-noise amplifier. Ex. 1005 at 6:1-2 and FIGS. 2D and 2F (annotated below).

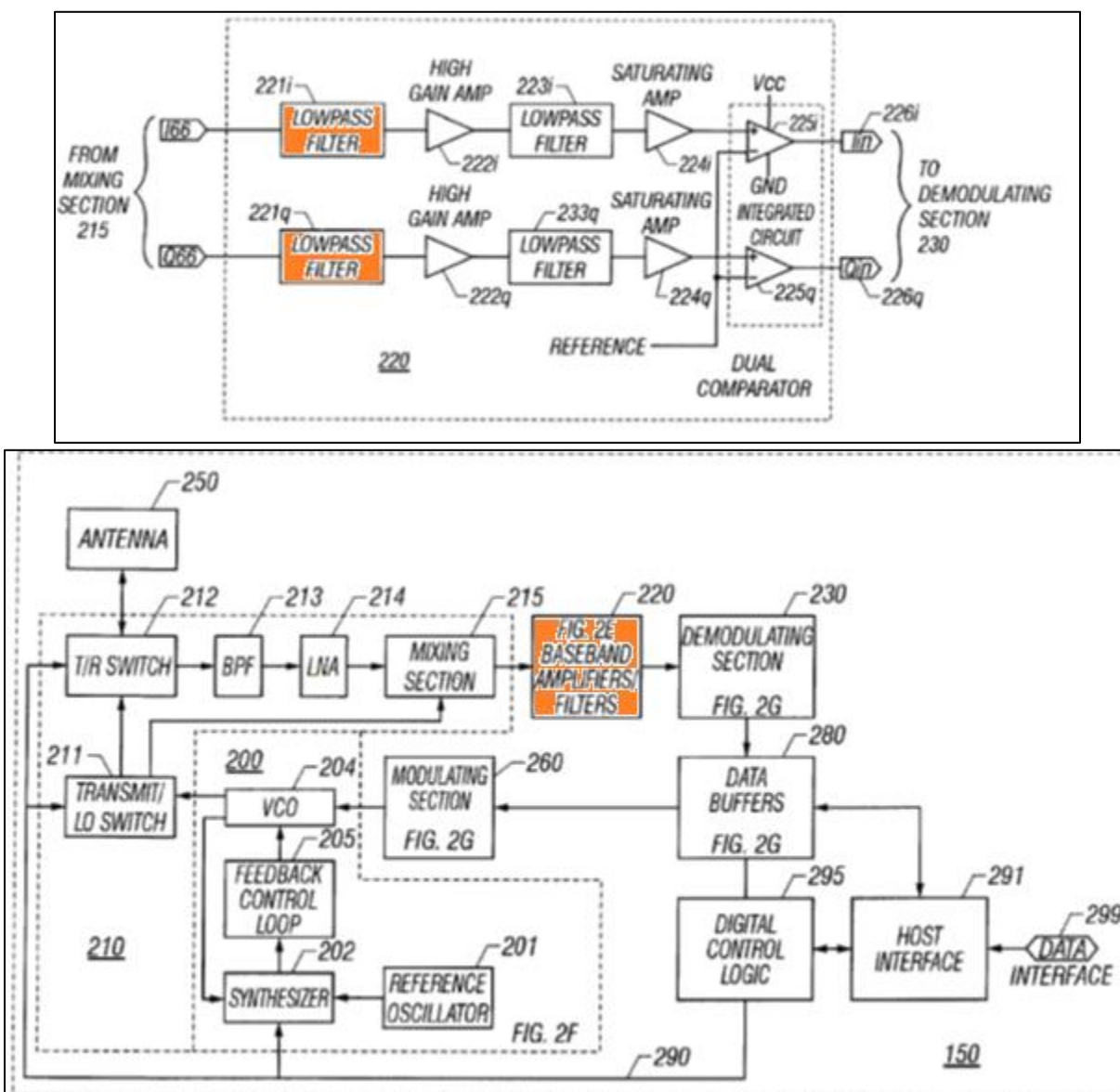
Cummins discloses that mixing section 215 include I and Q

mixers 215 i and 215 q. Ex. 1005 at 7:1-12. Cummins further discloses that

mixers 215 i and 215 q are double balanced so they balance out the LO signals, and the input signal from the LNA, at the output of each mixer. *Id.*



88. Referring to FIG. 2E, *Cummins* discloses low pass filters 221i and 221q are coupled to an output of mixers 215i and 215q. Ex. 1005 at 7:19-23 and FIGS. 2E and 2F (annotated below).



89. Cummins discloses that:

“[p]ower consumption is also another major concern in portable transceivers. Most commercially available portable radio transceivers, such as cellular phones, transmit in the 1-3 watt ranges. As such, it is not possible to run such transceivers for an extended period (days) using a small battery, for example, a disposable 9 volt battery or a small number of AAA batteries, commonly used to power the newer generations of palm top PCs. Instead, most conventional portable transceivers require larger Ni-Cad batteries which typically operate for at most 8 hours before requiring a recharge. As

such, most conventional RF transceiver designs are unsuitable for incorporation in low power portable computers such as a lap-top or palm-top personal computer (PC).”

Ex. 1005 at 2:31-44.

90. *Cummins* also discloses that:

“there is a need for a compact, low cost and low power RF transceiver having an efficient contention resolution capability that fits into a housing sized within a compact form factor, for use with PCs and/or peripherals.”

Id. at 3:1-4.

3. Meador (Ex. 1006)

91. *Meador* is directed in general to radio transceivers, and more particularly, to integrated circuit devices that implement transceiver functions. Ex. 1006 at 1:5-7.

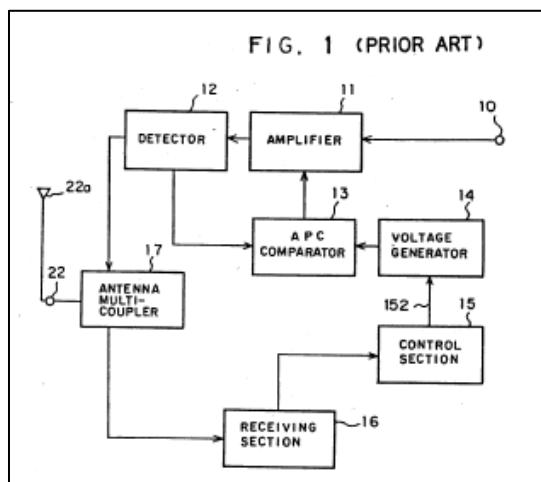
Meador discloses that there has been a desire to integrate as many functions as feasible on a single integrated circuit when implementing a radio transceiver, and that an entire transceiver system integrated on a common substrate would tend to reduce cost and increase reliability. Therefore, a configurable single-chip radio transceiver is needed. Ex. 1006 at 1:27-37.

92. *Meador* discloses a configurable single-chip transceiver integrated circuit (IC) architecture. The single-chip transceiver IC has multiple on-chip circuits that implement receiver functions, transmitter functions, and audio processing functions, among others. In the preferred embodiment, the single-chip transceiver IC supports radio configurations having off-chip implementations of corresponding

on-chip circuits for performing receiver front-end functions, synthesizer functions, reference oscillator functions, and audio processing functions. Ex. 1006 at 1:66 – 2:13. The resultant integrated transceiver system allows for flexibility in improving performance and functionality. Ex. 1006 at 7:63-65.

4. *Furuno* (Ex. 1007)

93. *Furuno* discloses a transmitting output control section for an automobile telephone set of a conventional type. In the figure, 10 is a transmitting signal input terminal at which a transmitting signal is to be received; 11 is an amplifier for amplifying the transmitting signal. Ex. 1007 at 1:16-35. *Furuno* teaches that element 12 is a detector which detects the level of an output signal of the amplifier 11. *Id.* *Furuno* teaches element 13 is an automatic power control comparator (hereinafter referred to as APC comparator) which constitutes a transmitting power control means in which a DC voltage output by the detector 12 and an output of a voltage generator 14. *Id.* The APC comparator 13 compares the DC voltage and the specified voltage and adjusts the amplification factor (gain) of the amplifier 11 so that both voltages are in balance. *Id.*



5. *Saito* (Ex. 1008)

94. *Saito*, titled "Automatic Gain Control Circuit," relates to electronic circuitry to automatically adjust the gain of an amplifier in a receiver of a mobile device.

Ex. 1008 at 1:5-7. *Saito* explains that one-stage gain switching of the prior art is insufficient for managing intermodulation distortion and disturbance over a broad range of input signal levels. *Id.* at 1:13-22. To improve signal reception over a broad range of input signal levels, *Saito* teaches that the gain of the amplifier is controlled “at multiple stages by [a] gain control signal” and that “a gain control unit comprising one or a plurality of continuous feedback systems is added.” *Id.* at 41-54.

95. *Saito* states that the automatic gain control circuitry is directed to “reducing reception disturbance resulting from intermodulation distortion for input levels of a broad range from the reception of a small input signal to the reception of a large input signal in receivers.” *Id.* at 1:34-40. *Saito* explains that the automatic gain

control circuitry includes “reception field level detection means” which “outputs a gain control signal in accordance with the reception field level.” *Id.* at 1:41-47.

96. In an embodiment, *Saito* teaches that “variable attenuators 20, 21, can continuously vary the damping quantity by the gain control signal outputted from the reception field level detection means 22, which constitute the continuous feedback system”. Ex. 1005 at 6:17-27. *Saito* explains that the “continuous feedback system . . . operate[s] to keep the input level of the received signal processing circuit always constant.” Ex. 1005 at 6:20-27. *Saito* contends that such gain control “eliminat[es] the intermodulation distortion in a wide range of reception field levels ranging from the input of the very fine signal to the input of the large signal.” Ex. 1005 at 7:51-62.

X. EXPLANATION OF MY OPINIONS

97. The following sections provides my opinion that claims 1, 23, 29, and 30 of the '330 patent are invalid as anticipated or rendered obvious by the prior art.

98. Below, I address each claim element on an element-by-element basis for each reference and/or combination of references, as well as the motivation to combine references and reasonable expectation of success in doing so. Given certain similar claim elements and the use of the same references in multiple combinations, many of the explanations herein would apply to multiple claim elements and reasons that a person of ordinary skill would be motivated to

combine these references and have a reasonable expectation of success in doing so. Therefore, my explanation regarding a certain claim element and certain reference or combination may also apply to other claim elements or the use of that same reference in another combination for the same or a similar claim element. This applies even if there is no explicit incorporation by reference. Furthermore, while I have cited portions of each reference to provide my opinions below, I may rely on additional portions to further support those opinions, or portions of other references, including portions identified above where I discussed the prior art and technology background.

XI. CUMMINS IN COMBINATION WITH RAUHALA DISCLOSES OR SUGGESTS ALL FEATURES OF CLAIMS 1 and 23 OF THE '330 PATENT

1. Claim 1

99. It is my opinion that *Cummins* in combination with *Rauhala* discloses each and every element of claim 1.

a. Claim 1[i]. “A method of receiving a signal using an integrated circuit”

100. *Cummins* discloses “a radio frequency (RF) transceiver for data communication.” Ex 1005 at 5:33-37. *Cummins* discloses that a transceiver 150 is on an integrated circuit as it “is disposed within a PCMCIA format package described above, with an antenna, RF and digital circuitry integrated on a single

printed circuit board (PCB) disposed within the PCMCIA package.” *Id.* It is my opinion that a person of ordinary skill would have recognized that an integrated circuit is “[m]ultiple, interconnected circuit elements, contained on or in a common substrate that function as a unit and not separately.” Ex. 1011 at 9. Thus, *Cummins* discloses an integrated circuit since its antenna, RF, and digital circuitry are integrated on a PCB (i.e., a common substrate). It is my opinion that *Cummins* discloses receiving a signal using an integrated circuit, since the transceiver 150 is disposed on an integrated circuit. A person of ordinary skill would have understood that transceiver 150 would receive signals, because a transceiver is the “combination of radio transmitting and receiving equipment in a common housing, usually for portable or mobile use and employing some common circuit components for both transmitting and receiving.” Ex. 1011 at 12.

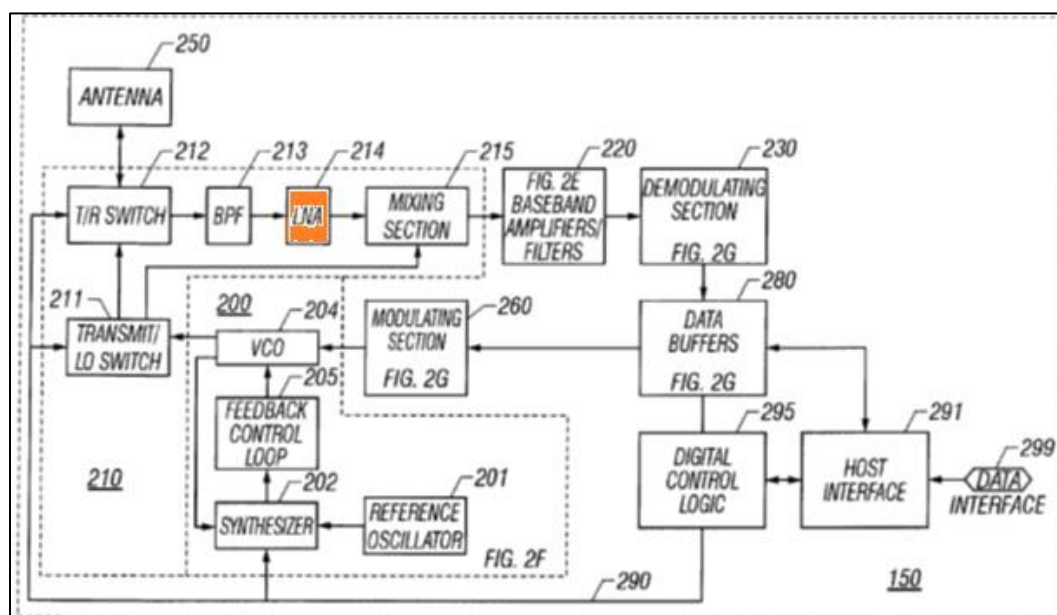
101. *Cummins* also explicitly discloses that its transceiver has a “receive mode.” *Cummins* discloses that “[i]n a receive mode, switch 212 routes the signal received via antenna 250.” Ex. 1005 at 3:28-29. *Cummins* discloses that “[a] pair of switches, T/R switch 212 and transmit/LO switch 211, provide a means for selectively coupling antenna 250 to either the receiver portion or the transmitter portion of transceiver 150.” Ex. 1005 at 6: 12-15.

102. *Cummins* is disposed on an integrated circuit because *Cummins* discloses that transceiver 150, an antenna, RF, and digital circuitry are integrated on a single

printed circuit board. Thus, it is my opinion that *Cummins* discloses receiving a signal (via the receiver of transceiver 150), on an integrated circuit.

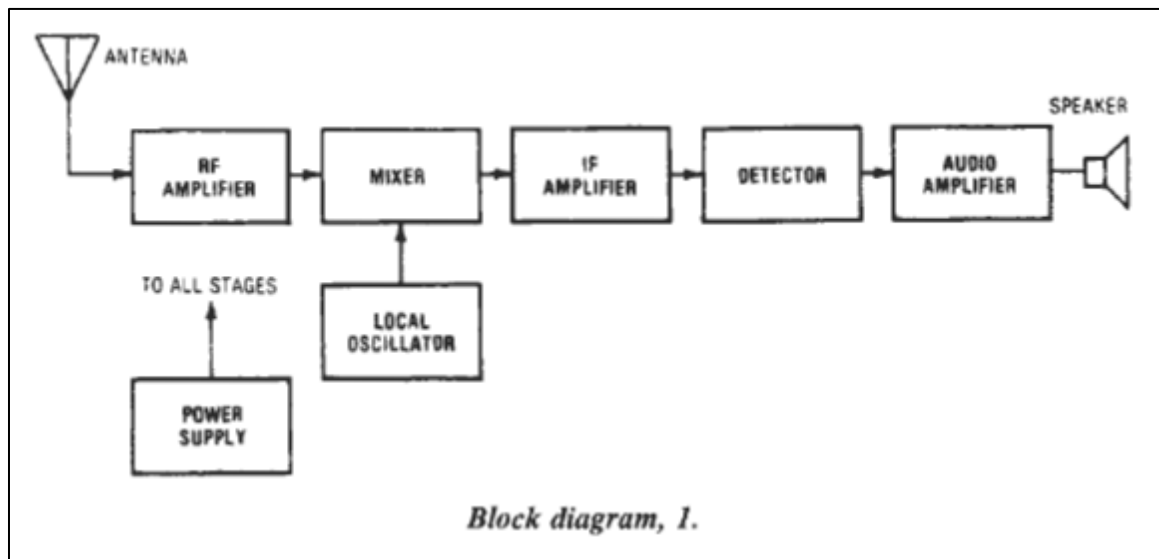
b. Claim 1[ii]. “the integrated circuit comprising a signal path including a low-noise amplifier configured to receive the signal”

103. *Cummins* discloses this feature. *Cummins* discloses “low noise amplifier (LNA) 214 for amplification before being applied to [a] mixing section 215”. Ex. 1005 at 6:1-2 and FIG. 2F (annotated below). *Cummins* discloses that, “[i]n a receive mode, switch 212 routes the signal received via antenna 250 through a broad band filter 213 to the input of low noise amplifier (LNA) 213.” Ex. 1005 at 5:55 to 6:2.



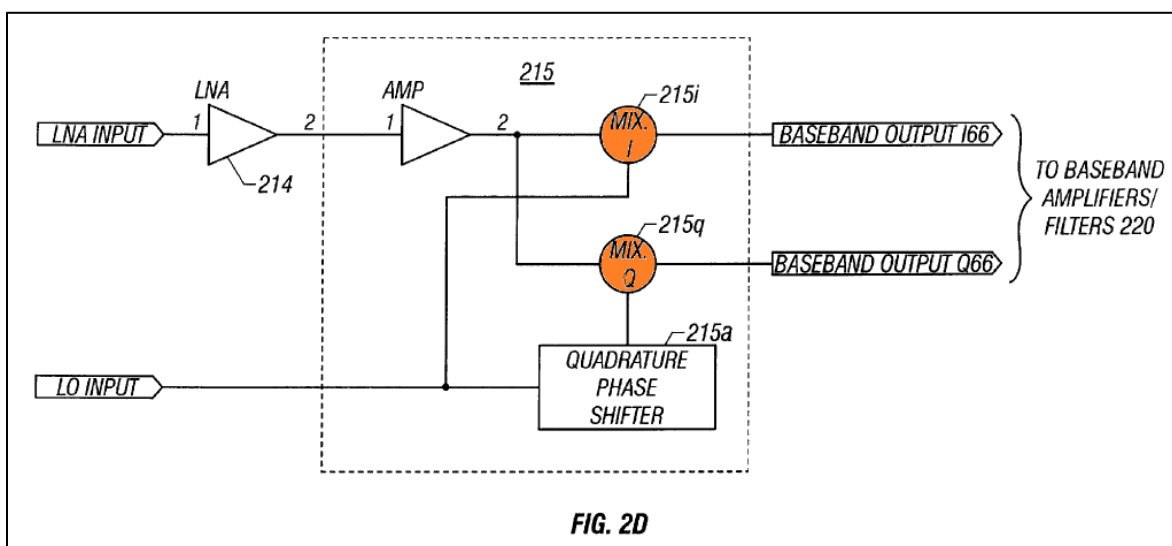
104. A person of ordinary skill in the art would have recognized that, for example, FIG. 2F is a block diagram that is a “diagram in which their essential

systems units are drawn as blocks, and their relationship to each other is indicated by appropriately connected lines. The path of the signal or energy may be indicated by lines or arrows” and a “chart that graphically depicts the functional relationships of hardware making up a system. The block diagram serves to indicate the various data and control signal paths between functional units of the system hardware.” Ex. 1011 at 7.



Id.

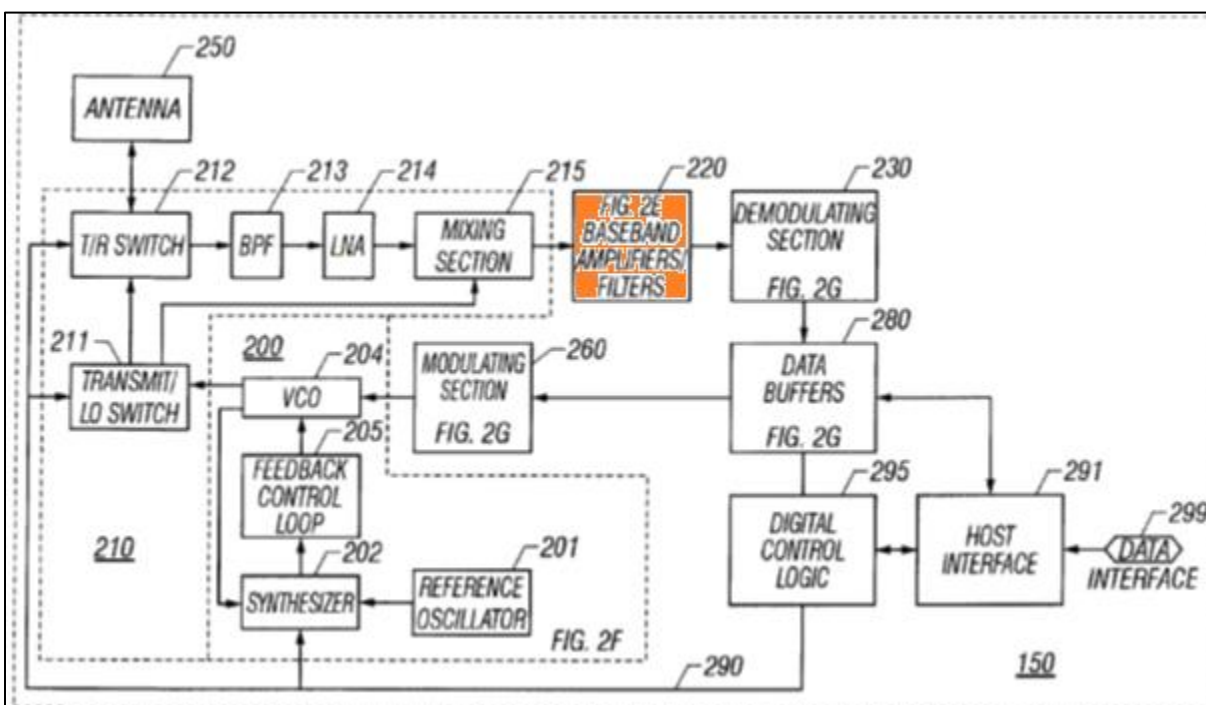
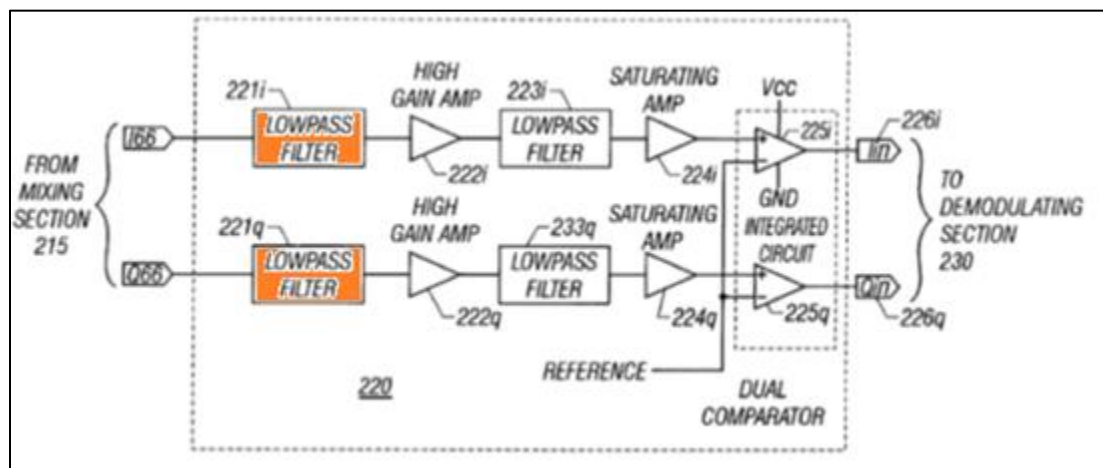
It is my opinion that a person of ordinary skill in the art would have understood that the block diagrams FIGS. 2D, 2E, and 2F of *Cummins* show that transceiver 150 (already established to be on an integrated circuit) includes a signal path, and that the components represented in the block diagrams, including the LNA 214, the mixing section 215, and the filters 220, are included in the signal path.



d. Claim 1[iv]. “a low-pass filter having an input coupled to an output of the mixer”

Cummins discloses “the output signals of mixers 215 i and 215 q, i.e. Ibb and Qbb, are processed separately by baseband amplifiers/filters section 220. First signals Ibb and Qbb are filtered by low pass filters 221 i and 221 q.” Ex. 1005 at 7:19-23 and FIGS. 2E and 2F (annotated below). The block diagram of FIGS. 2F shows an arrow indicating a signal path directly coupling mixing section 215 to “FIG. 2E BASEBAND AMPLIFERS/FILTERS.” See Ex. 1005 at FIG. 2F. FIG. 2E shows “[f]irst signals Ibb and Qbb are filtered by low pass filters 221 i and 221 q,” and as shown in FIG. 2E, low pass filters 221 I and 221 q are the first components within functional block 220 to receive the signals Ibb and Qbb from mixing section 215.

Ex. 1005 at 7:21-22 and FIGS. 2E and 2F.



e. **Claim 1[v]. “determining a first signal strength at a first node in the signal path in the integrated circuit”**

106. To the extent that *Cummins* does not explicitly disclose determining a first signal strength at a first node in the signal path in the integrated circuit, it is my

opinion that *Rauhala* teaches such limitations in a device that aims to solve the same technical problems as *Cummins*.

107. For example, *Cummins* discloses that:

“[p]ower consumption is also another major concern in portable transceivers. Most commercially available portable radio transceivers, such as cellular phones, transmit in the 1-3 watt ranges. As such, it is not possible to run such transceivers for an extended period (days) using a small battery, for example, a disposable 9 volt battery or a small number of AAA batteries, commonly used to power the newer generations of palm top PCs. Instead, most conventional portable transceivers require larger Ni-Cad batteries which typically operate for at most 8 hours before requiring a recharge. As such, most conventional RF transceiver designs are unsuitable for incorporation in low power portable computers such as a lap-top or palm-top personal computer (PC).”

Ex. 1005 at 2:31-44.

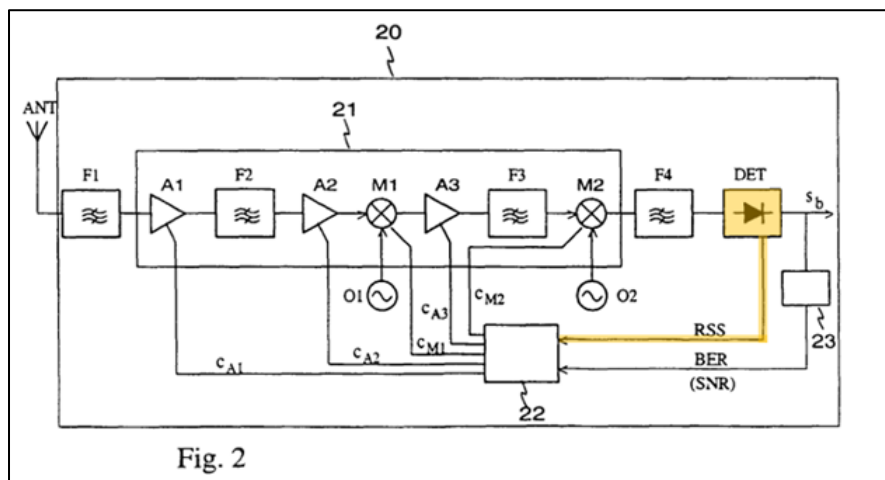
108. *Cummins* also discloses that:

“there is a need for a compact, low cost and low power RF transceiver having an efficient contention resolution capability that fits into a housing sized within a compact form factor, for use with PCs and/or peripherals.”

Ex. 1005 at 3:1-4.

109. *Rauhala* describes methods “for linearizing a radio receiver” in which “the energy consumption of the receiver can be reduced without degrading the signal quality.” Ex. 1004 at [0001], [0007]. *Rauhala* states that such techniques are “appli[cable] in the reception circuits of mobile stations,” such as mobile phones, which are transceivers. Ex. 1004 at [0001], [0012].

110. *Rauhala* discloses that a signal path includes a detector DET coupled to an output of a filter. Ex. 1004 at [0012] and FIG. 2 (annotated below). *Rauhala* further teaches that “[d]etector DET provides information about the signal strength (RSS) on the channel to which the receiver is tuned.” Ex. 1004 at [0013].



111. *Rauhala* discloses that in “normal conditions, i.e. when the signal strength is satisfactory on the receive channel and ordinary on the neighboring channels, the supply currents of the receiver's front-end amplifiers and at least the first mixer are kept relatively low. If the signal strength goes below a certain value on the receive channel or exceeds a certain value on a neighboring channel, said supply currents are increased.” Ex. 1004 at [0006].

112. It is my opinion that a person of ordinary skill in the art would have recognized that the *Rauhala*’s detector DET determines the strength of signal RSS at a “first node in the signal path,” as required by claim 1 of the ’330 patent. FIG. 2 of *Rauhala* is a block diagram showing a signal path comprising functional units

(as blocks) and control signal paths (as lines and arrows between the blocks). Ex. 1004 at FIG. 2. It is my opinion that FIG. 2 of *Rauhala* is a block diagram that is a “diagram in which their essential systems units are drawn as blocks, and their relationship to each other is indicated by appropriately connected lines. The path of the signal or energy may be indicated by lines or arrows” and a “chart that graphically depicts the functional relationships of hardware making up a system. The block diagram serves to indicate the various data and control signal paths between functional units of the system hardware.” Ex. 1011 at 7.

113. Detector DET is shown as a functional block in the block diagram and signal path of FIG. 2 (between filter F4 and control unit 22). Ex. 1004 at FIG. 2. A node is a “physical connection between two electrical components in a circuit.” Ex. 1015 at 3. It is my opinion that detector DET is therefore determining signal strength of RSS at a node between two electrical components of the *Rauhala* circuit - e.g., 1) filter F4 and 2) control unit 22). Ex. 1004 at FIG 2. Therefore, *Rauhala* is determining a first signal strength at a node in the signal path.

114. As a result of the techniques of *Rauhala*, “the energy consumption of the receiver can be reduced without degrading the signal quality,” leading to “longer life for the battery or [. . .] a smaller battery can be used.” Ex. 1004 at [0007].

115. As such, it is my opinion that *Rauhala* is in the same technical field as *Cummins* and the '330 patent, because all three relate to wireless transceivers, and

in particular to reducing power consumption for wireless transceivers in order to improve battery life. A person of ordinary skill would have recognized the similarities between *Cummins* and the *Rauhala* device and have been motivated to combine them make a device that improves battery life in a wireless transceiver like *Cummins*, and doing so by determining signal strength and adjusting impedances and supply currents like in *Rauhala*.

116. A person of ordinary skill would have had a reasonable expectation of success in combining the disclosures of *Cummins* and *Rauhala* at least because both combinations would have used known technologies (for example, the well-known wireless transceiver of *Cummins*) according to known methods (for example determining signal strength to adjust impedance and supply current as in *Rauhala*) to yield predictable results (for example, improving battery life or reducing battery size of the *Cummins* device).

117. Moreover, it is my opinion that modification of *Cummins* with the teachings of *Rauhala* would have amounted to nothing more than the use of a known technique to improve a similar device, and the results of the modification would have been predictable. This is because at the time of the invention, a person of ordinary skill would have had the requisite skill level to readily modify the device disclosed by *Cummins* to implement the teachings of *Rauhala*. Moreover, such

modifications of *Cummins* would have been routine for the person of ordinary skill as they use well-known elements with no change in their respective functions.

f. Claim 1[vi]. “reducing a switching current in the signal path”

118. As will be explained in further detail below, it is my opinion that one of ordinary skill in the art would have recognized that the collector current $I/2$ is a “switching current.”

119. The '330 specification does not expressly define “switching current.”

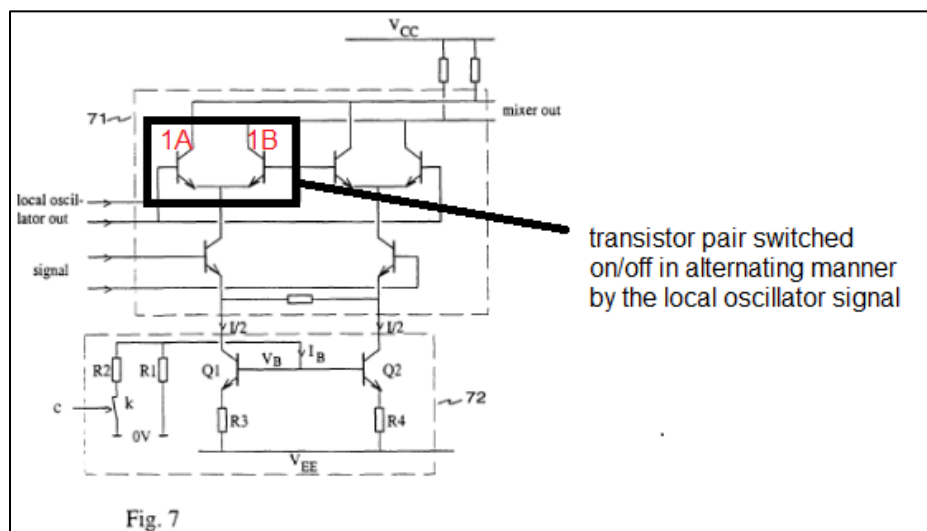
However, the patentee did expressly define “switching current” to be “a dynamic or transient current that occurs during voltage transitions,” during prosecution of the '330 patent. In particular, in the response, the patentee argued that:

A bias current is not the same as a switching current. One skilled the art understands that a bias current is a DC or quiescent current, while a switching current is a dynamic or transient current that occurs during voltage transitions. (See for example, the pending application, Figure 6 and related discussion.) Accordingly, the cited references do not show or suggest reducing a switching current in the signal path by dynamically changing an impedance of a component in the signal path as required by the claim.

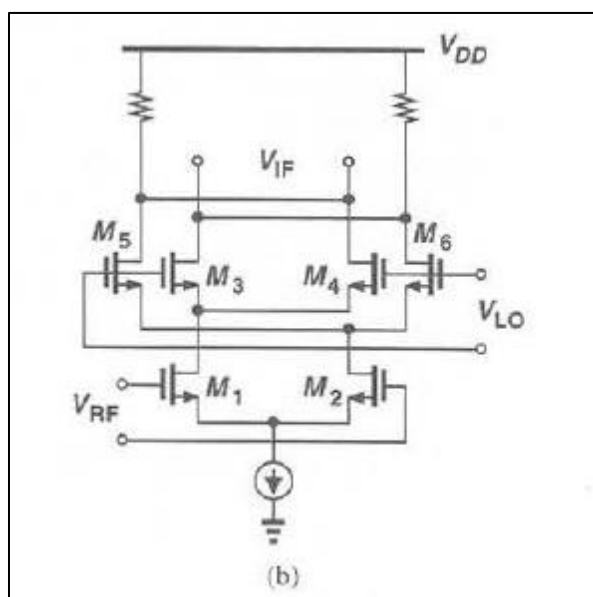
Ex. 1003 at 163.

120. FIG. 7 of *Rauhala* shows a double-balanced mixer with two switching pairs of transistors. Ex. 1004 at [0023] and FIG. 7. The switching pairs are driven by a local oscillator. *Id.* A first switching pair includes a first transistor (annotated 1A) and a second transistor (annotated 1B). *Id.* It is my opinion that a person of

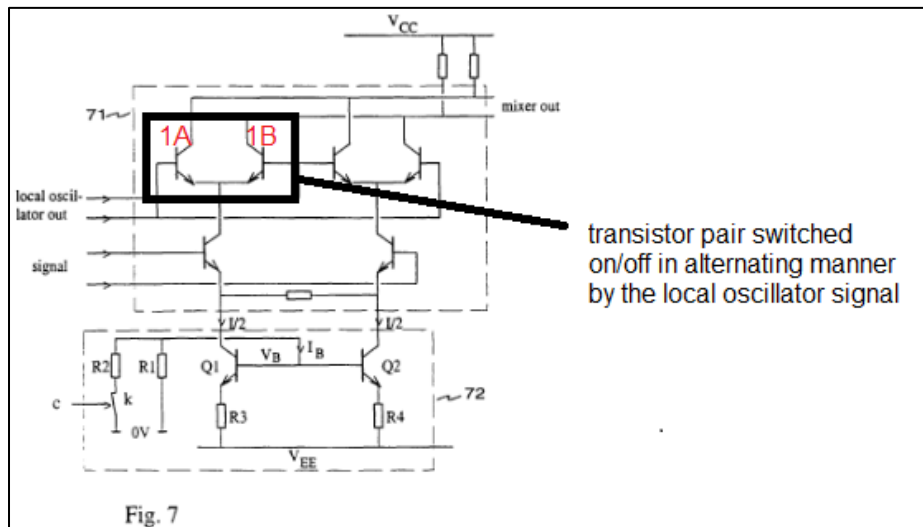
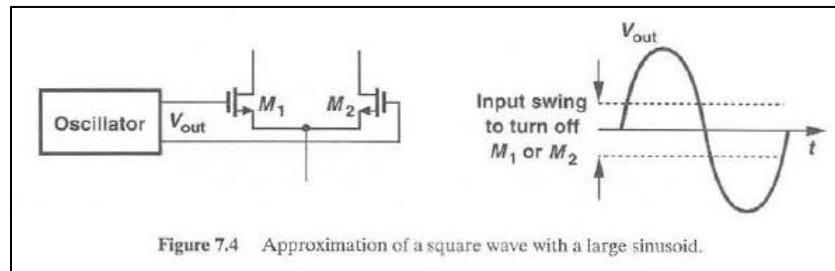
ordinary skill in the art would have understood that the signal from the local oscillator would switch first transistor 1A and second transistor 1B in a complementary manner.



121. A double-balanced mixer is well-known, see Ex. 1012 at 5-6. For example, FIG. 6.19b (reproduced below), where M3 and M4 are a first switching, differential pair and M5 and M6 are a second switching, differential pair. *Id.*



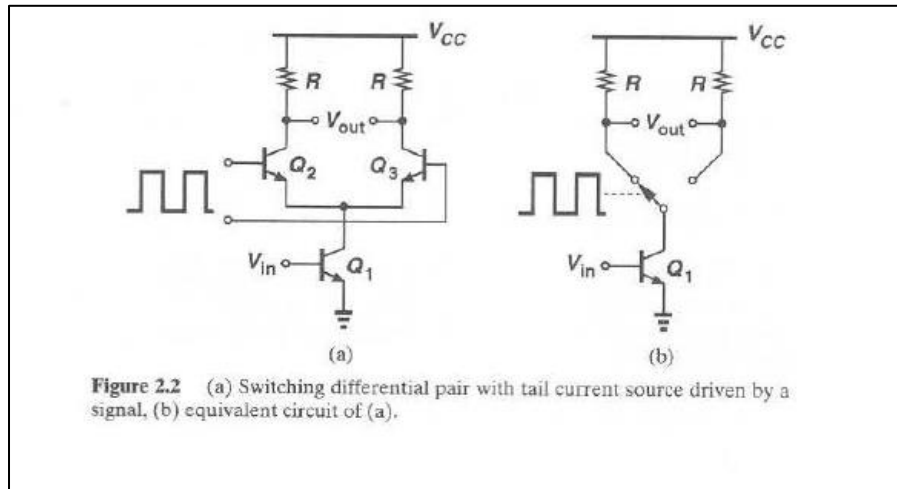
122. *Rauhala* FIG. 7 shows a local oscillator output being directed to each of the two switching pairs. As evidenced by Ex. 1012 at FIG. 7.4, the local oscillator of *Rauhala* would output an oscillating signal that switches the pair of transistors 1A/1B on and off in an alternating fashion. Ex. 1012 at 7. That is, when first transistor 1A is on, second transistor 1B is off. Also, when second transistor 1B is on, first transistor 1A is off.

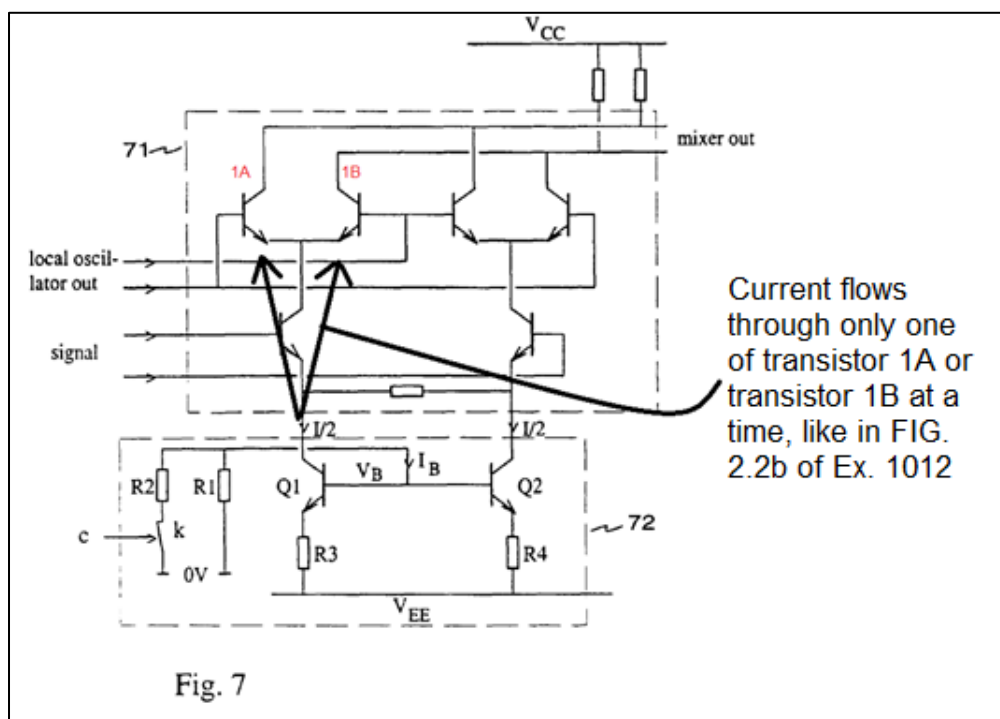


123. Ex. 1012 also shows how a local oscillator signal is used for switching in a mixer. Ex. 1012 at 4. FIG. 2.2a (reproduced below) specifically shows switching a differential pair of transistors using a local oscillator signal, and FIG. 2.2b (also reproduced below) shows the equivalent circuit of the differential pair switching on

an off. In other words, FIG. 2.2b, shows how the local oscillator signal switches the differential pair on and off, so that current flows through only one transistor of the differential pair at a given time.

124. Annotated FIG. 7 of *Rauhala* below shows how current $I/2$ is directed to one of transistor 1A or transistor 1B at a time, in the same manner as Ex. 1012 at FIGS. 2.2a and 2.2b.



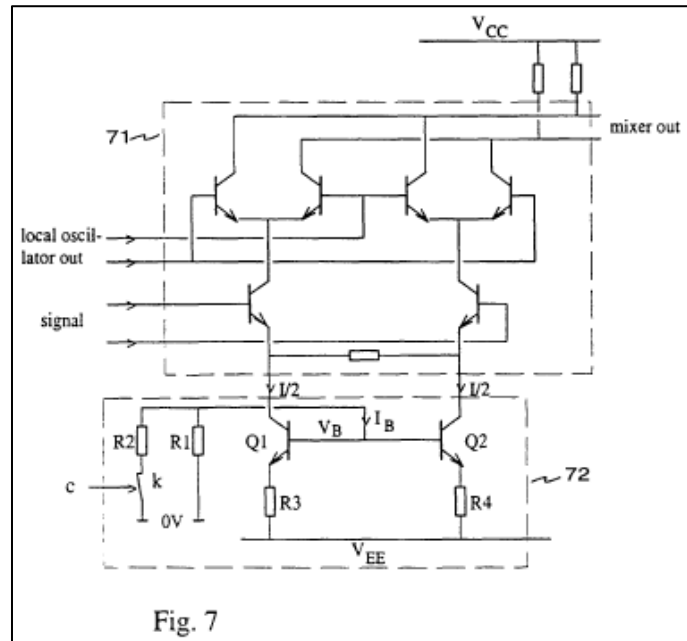


125. Therefore, it is my opinion that a person of ordinary skill would have understood that the current $I/2$ directed to transistors 1A and 1B is a “switching current” as defined by the patentee because it is “a dynamic or transient current that occurs during voltage transitions.” Each on-off switching event at transistors 1A/1B of *Rauhala* is a voltage transition. It is my opinion that current $I/2$ is dynamic because it is transient and dynamic, as it is constantly switched from first transistor 1A or second transistor 1B.

- g. **Claim 1[vii]. “[reducing a switching current in the signal path] by dynamically changing an impedance of a component in the signal path based on the first signal strength”**

126. *Rauhala* shows two resistors R1 and R2 that are in parallel to one another.

Ex. 1004 at [0023] and FIG. 7.



127. Therefore, the resistance of the parallel circuit can be switched between two different resistance configurations. Ex. 1004 at [0023]. The first (low) resistance configuration is when the switch k is closed such that resistor R2 is placed in parallel with R1. *Id. Rauhala* discloses that the control current I_B when switch k is closed is equal to $V_B/R1 + V_B/R2$, where V_B is the magnitude of the transistors' base voltage (e.g., the current through resistor R1 is $(0 - V_B)/R1$ but V_B is a negative voltage and so $-V_B$ is a positive voltage, that is, $-V_B$ is the magnitude of

VB). *Id.* A person of ordinary skill in the art would have understood that as more resistors are added in parallel in a circuit, the equivalent resistance of the circuit decreases and the total current of the circuit increases. *See* Ex. 1022 at 4-5. As shown in Fig. 3-4 of Ex. 1022, “[f]or three circuit elements connected in parallel as shown in Fig. 3-4, KCL states that the current i entering the principal node is the sum of the three current leaving the node through the branches.” *Id.*

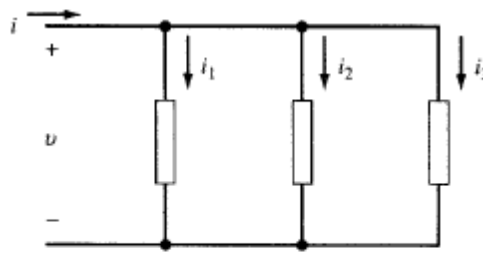


Fig. 3-4

$$i = i_1 + i_2 + i_3$$

128. The second (high resistance) configuration is when the switch k is open such that the resistance of the circuit is equal to R_1 . *Rauhala* discloses that the control current I_B when switch k is open is equal to a low value VB/R_1 . Ex. 1004 at [0023].

129. The impedance (high or low), and the control current (low or high), based on the state of switch k is summarized in the table below.

Switch k	Impedance	Control Current I_B
Closed	Low	High (VB/R_1)

		+ V_B/R_2)
Open	High	Low (V_B/R_1)

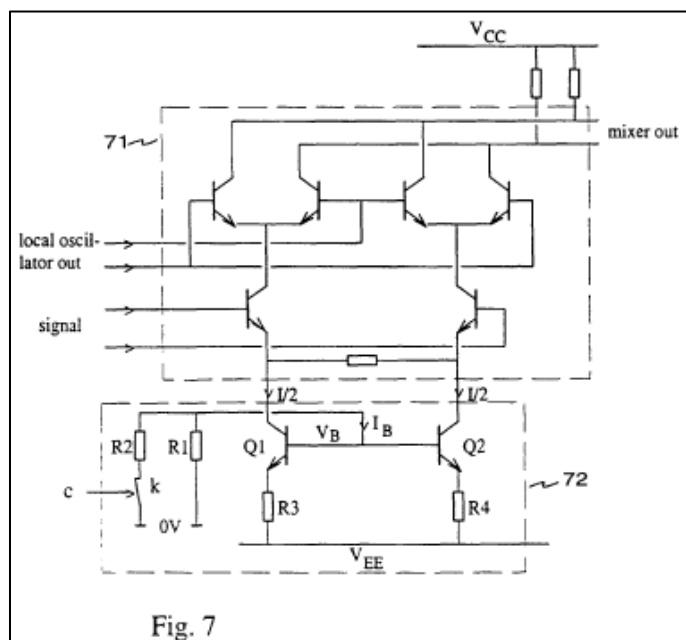
130. In the example of FIG. 7, the state of switch k depends on the control signal c. Ex. 1004 at [0023]. When signal c is 0, switch k is open. *Id.* When signal c is 1, switch k is closed. *Id.*

Control signal c (dependent on signal strength)	k	Impedance	Control Current I_B
1	Closed	Low	High (V_B/R_1 + V_B/R_2)
0	Open	High	Low (V_B/R_1)

131. *Rauhala* discloses that as the control current I_B increases, the supply current I increases. Ex. 1004 at [0023]. A person of ordinary skill would have understood that as control current I_B decreases, the current flowing in Q1 and Q2 decreases, since the current in Q1 and Q2 is controlled by I_B , and thus the supply current I, that provides current to Q1 and Q2 (and thus the rest of the circuit) also would decrease.

132. *Rauhala* further discloses that in FIG. 7, the resistances of resistors R3 and R4 are identical and transistors Q1 and Q2 are identical, and thus the collector

currents ($I/2$) of the transistors are also identical, i.e., the analog multiplier 71 receives a supply current I from $Q1$ and $Q2$. Ex. 1004 at [0023].



133. Since the control current I_B is reduced when the impedance of control circuit 72 is increased, and supply current (I) is reduced when the control current is reduced, a person of ordinary skill would have understood that the collector current $I/2$ is reduced when the impedance of the control circuit 72 is increased. See Ex. 1021 at 4 and FIG. 1.27, reproduced below (showing a linear relationship between the base current I_B and the collector current I_C).

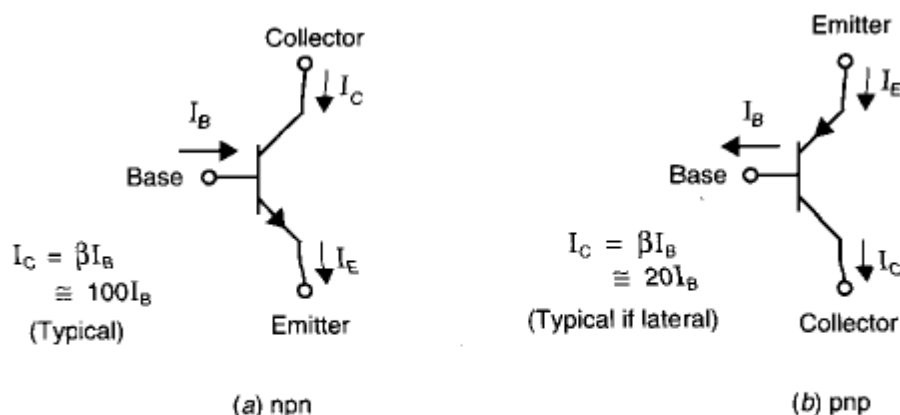


Fig. 1.27 The symbols representing (a) an npn bipolar-junction transistor and (b) a pnp bipolar-junction transistor.

134. These relationships are summarized in the table below.

Control signal c (dependent on signal strength)	k	Impedance	Control Current I_B	Supply Current I	Collector Current $I/2$
1	Closed	Low	High ($V_B/R_1 + V_B/R_2$)	High	High
0	Open	High	Low (V_B/R_1)	Low	Low

h. Claim 1[viii]. “[dynamically changing an impedance of a component in the signal path] based on the first signal strength”

135. *Rauhala* discloses that the detected signal strength RSS is directed to a control unit 22. Ex. 1002 at [0013] and FIG. 2. Control unit 22 outputs control signals to the linear units (e.g., the amplifiers and mixers). *Id.* For example, control signal cM1 sets the supply current of mixer M1 and signal cM2 sets the supply current of mixer M2. *Id.*

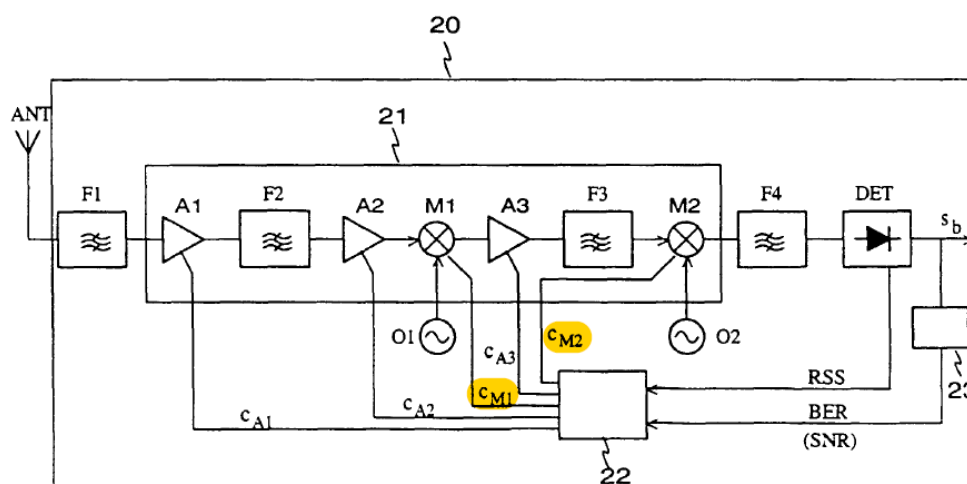
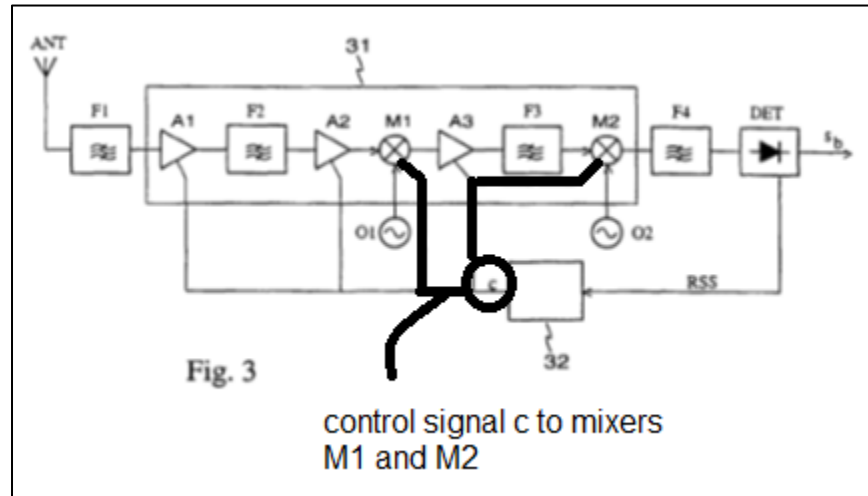


Fig. 2

136. *Rauhala's* FIG. 3 is one example of supply current control for the linear units. Ex. 1004 at [0015]. A control unit 32 only receives the receive signal strength RSS information which has threshold values S31 and S32. *Id.* The control unit 32 produces one one-bit control signal *c*, which is taken to all linear units A1, A2, M1, A3 and M2. *Id.* The supply current of a given linear unit has two values. Supply currents are controlled with signal *c* according to the annotated table below. *Id.*

RSS	<i>c</i>	I_i	
$\leq S31$	0	I_h	high current condition
$>S31, <S32$	1	I_l	low current condition
$\geq S32$	0	I_h	high current condition

137. The control signal *c* is taken to all linear units, including each of the mixers M1 and M2. *Id.*



138. The value of control signal *c* depends upon the detected signal strength RSS. *Id.* When the measured current is below threshold S31, signal *c* is 0 and the linear unit (including amplifier) supply currents are at their higher values. *Id.* The relatively large supply currents help reduce the effects of possible interference from outside the receive channel. *Id.* When the signal strength RSS is between S31 and S32, signal *c* is 1 and the supply currents are at their lower values. *Id.* The relatively small supply currents help reduce energy consumption. *Id.* The relationship of the detected signal strength RSS and the control signal *c* is shown again in the table below.

139. *Rauhala* discloses other schemes for controlling the supply current of mixers M1 and M2 based on the signal strength indication. For example, FIGS. 4 and 5

show more complicated schemes for controlling the supply current to mixers M1 and M2. Ex. 1004 at [0017]-[0020]. Furthermore, the disclosed value of *c* (as either 0 or 1) does not uniformly correspond to the same high or low current state. For example, when *c* is 0 in the scheme of FIG. 3, the mixer is in a high current state, and when *c* is 1, the mixer is in a low current state. Ex. 1004 at [0015]. However, in the scheme of FIG. 4, when “signal *c*_M is 0, the supply current in question is lower, and conversely, if signal [*c*]_M is 1, the supply current is higher.” Ex. 1004 at [0017].

140. It is my opinion that a person of ordinary skill in the art would have recognized that signal strength being measured by *Rauhala* is dynamic and changing based on various factors. *LeBlanc* illustrates that it was well-known in the art to a person of ordinary skill that the behavior of wireless signals (including their strength) is unique and complicated, and is affected by multiple factors. Ex. 1020 at 2:40-51. For example, *LeBlanc* states that:

The behavior of a mobile radio signal in the general environment is unique and complicated.

...

Factors include terrain undulations, fixed and variable clutter, atmospheric conditions, internal radio characteristics of cellular and PCS systems, such as frequencies, antenna configurations, modulation schemes, diversity methods, and the physical geometry of direct, refracted and reflected waves between the base stations and the mobile.

Id.

It is my opinion that a person of ordinary skill would have understood that signal strength being measured by the *Rauhala* patent, changes based on the environment of the signal being measured, as evidenced by *LeBlanc*. *Rauhala* relates to mobile phones, and thus, the environment of the signals being measured by *Rauhala* will be constantly changed during the use of the mobile phone in different areas, and therefore will experience different terrain undulations, different amounts of fixed and variable clutter, different atmospheric conditions, and the like, resulting in different measured signal strength.

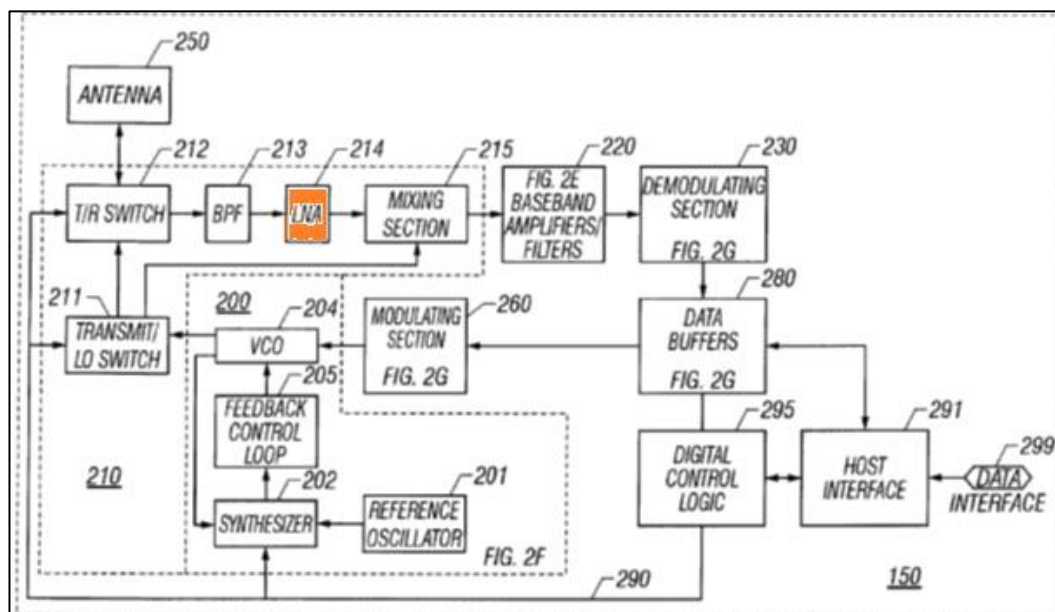
2. Claim 23

141. It is my opinion that *Cummins* in combination with *Rauhala* discloses each and every element of claim 23.

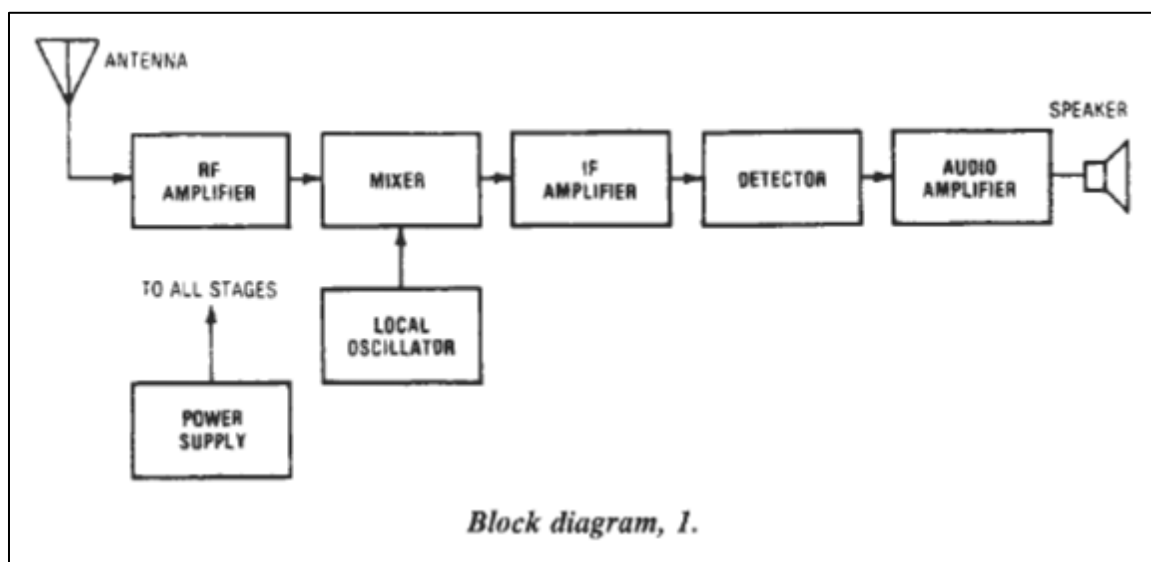
a. Claim 23[i]. “A wireless transceiver integrated circuit comprising: a receiver comprising a signal path”

142. *Cummins* discloses “a radio frequency (RF) transceiver for data communication.” Ex. 1005 at 5:33-37. *Cummins* discloses that a transceiver 150 is on an integrated circuit as it “is disposed within a PCMCIA format package described above, with an antenna, RF and digital circuitry integrated on a single printed circuit board (PCB) disposed within the PCMCIA package.” *Id.* It is my opinion that a person of ordinary skill would have recognized that an integrated circuit is “[m]ultiple, interconnected circuit elements, contained on or in a common

substrate that function as a unit and not separately.” Ex. 1011 at 9. Thus, *Cummins* discloses an integrated circuit since its antenna, RF, and digital circuitry are integrated on a PCB (i.e., a common substrate).



143. A person of ordinary skill would have recognized that, for example, FIG. 2F is a block diagram that is a “diagram in which their essential systems units are drawn as blocks, and their relationship to each other is indicated by appropriately connected lines. The path of the signal or energy may be indicated by lines or arrows” and a “chart that graphically depicts the functional relationships of hardware making up a system. The block diagram serves to indicate the various data and control **signal paths** between functional units of the system hardware.” Ex. 1011 at 7 (emphasis added).

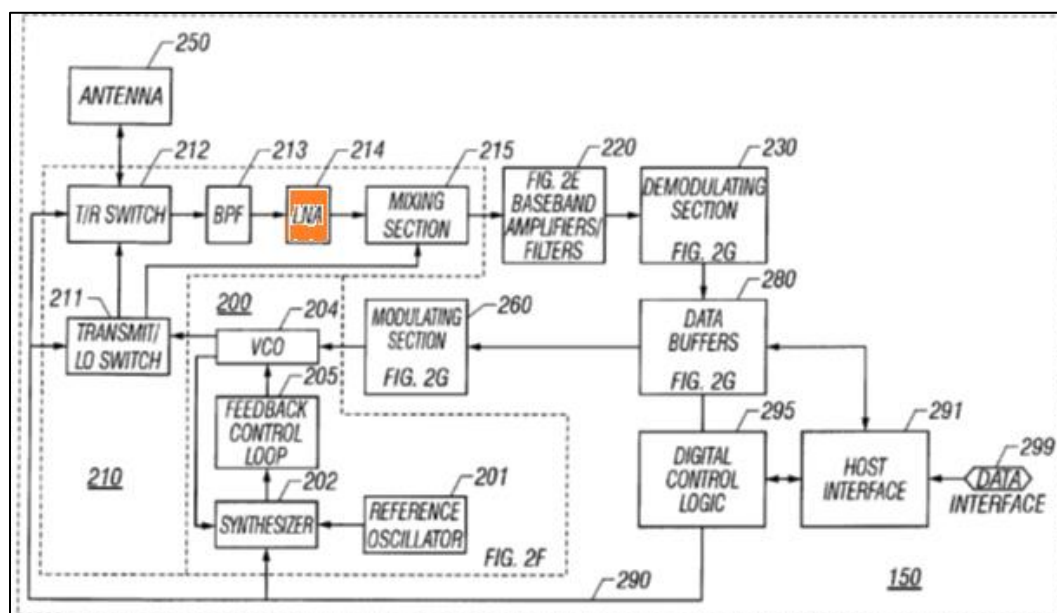


Id.

144. It is my opinion that a person of ordinary skill in the art would have understood that the block diagrams FIGS. 2D, 2E, and 2F of *Cummins* show that transceiver 150 (already established to be on an integrated circuit, *see supra* Section (XI)(1)(a)) includes a signal path, and that the components represented in the block diagrams, including the LNA 214, the mixing section 215, and the filters 220, are included in the signal path. *See supra* Section (XI)(1)(a).

b. Claim 23[ii]. “a low-noise amplifier”

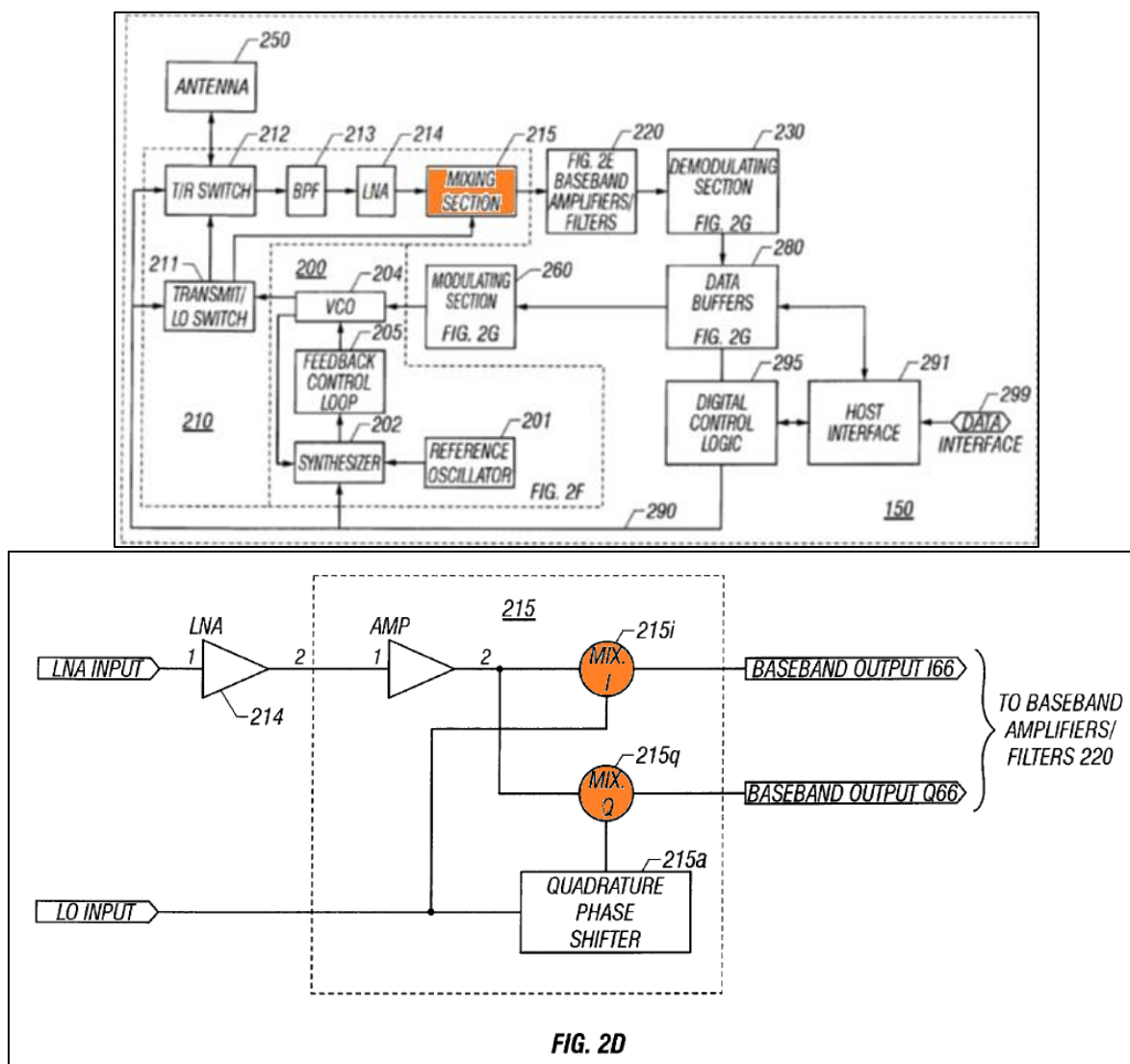
145. *Cummins* discloses this feature. *Cummins* discloses “low noise amplifier (LNA) 214 for amplification before being applied to [a] mixing section 215”. Ex. 1005 at 6:1-2 and FIG. 2F (annotated below).



c. Claim 23[iii]. “a mixer having an input coupled to an output of the low-noise amplifier”

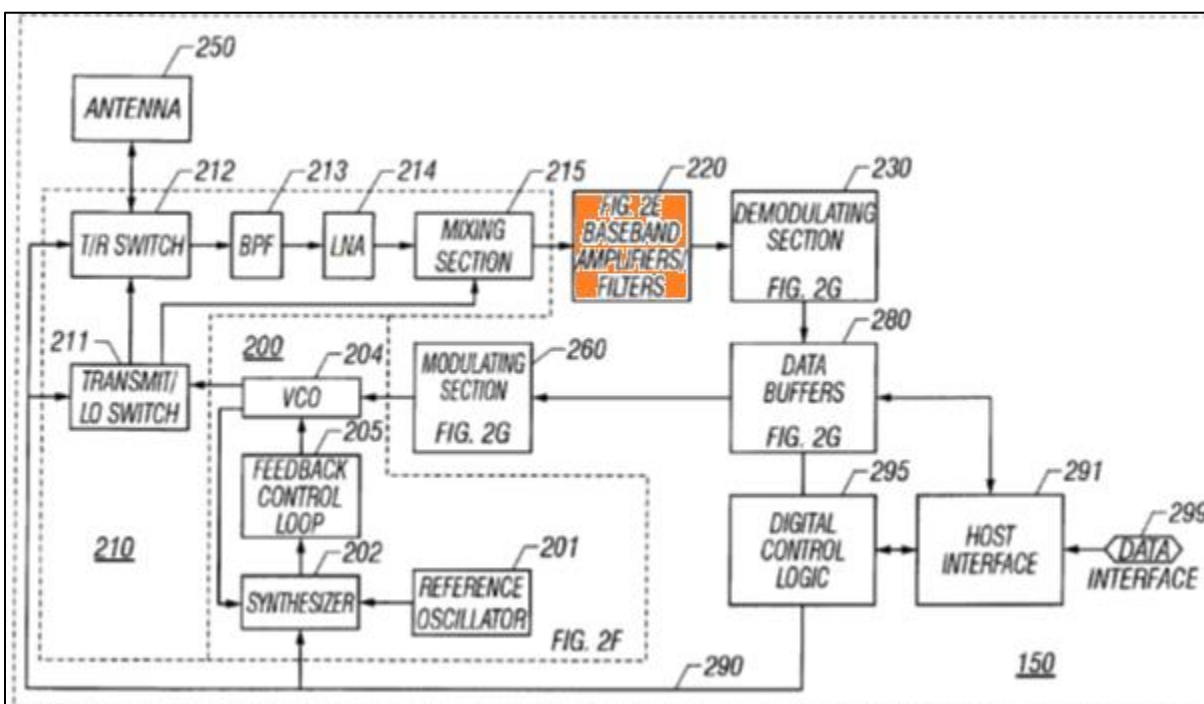
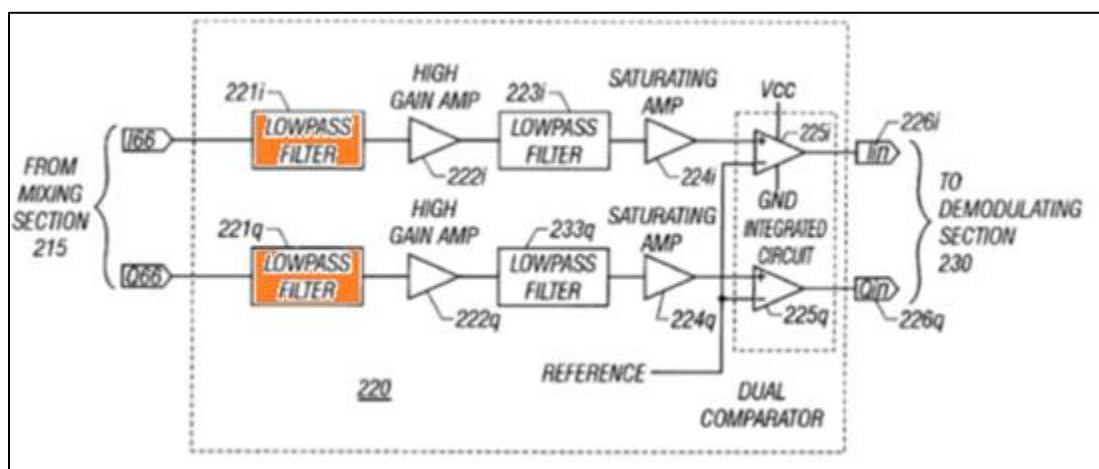
146. *Cummins* discloses a mixer having an input coupled to an output of the low-noise amplifier. Ex. 1005 at 6:1-2 and FIGs. 2D and 2F (annotated below).

Cummins discloses that mixing section 215 include I and Q mixers 215 i and 215 q. Ex. 1005 at 7:1-12. *Cummins* further discloses that mixers 215 i and 215 q are double balanced so they balance out the LO signals, and the input signal from the LNA, at the output of each mixer. *Id.*



d. **Claim 23[iv]. “a low-pass filter having an input coupled to an output of the mixer”**

147. Cummins discloses a low-pass filter having an input coupled to an output of the mixer. Referring to FIG. 2E, Cummins discloses low pass filters 221i and 221q are coupled to an output of mixers 215i and 215q. Ex. 1005 at 7:19-23 and FIGs. 2E and 2F (annotated below).



- e. **Claim 23[v]. “a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength”**

148. To the extent that *Cummins* does not explicitly disclose determining a first signal strength at a first node in the signal path in the integrated circuit, it is my

opinion that *Rauhala* teaches such limitations in a device that aims to solve the same technical problems as *Cummins*.

149. For example, *Cummins* discloses that:

“[p]ower consumption is also another major concern in portable transceivers. Most commercially available portable radio transceivers, such as cellular phones, transmit in the 1-3 watt ranges. As such, it is not possible to run such transceivers for an extended period (days) using a small battery, for example, a disposable 9 volt battery or a small number of AAA batteries, commonly used to power the newer generations of palm top PCs. Instead, most conventional portable transceivers require larger Ni-Cad batteries which typically operate for at most 8 hours before requiring a recharge. As such, most conventional RF transceiver designs are unsuitable for incorporation in low power portable computers such as a lap-top or palm-top personal computer (PC).”

Ex. 1005 at 2:31-44.

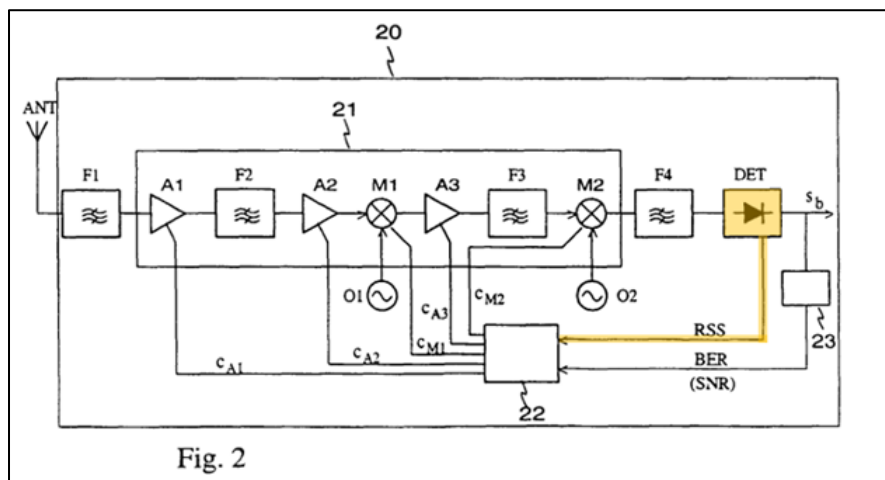
150. *Cummins* also discloses that:

“there is a need for a compact, low cost and low power RF transceiver having an efficient contention resolution capability that fits into a housing sized within a compact form factor, for use with PCs and/or peripherals.”

Ex. 1005 at 3:1-4.

151. *Rauhala* describes methods “for linearizing a radio receiver” in which “the energy consumption of the receiver can be reduced without degrading the signal quality.” Ex. 1004 at [0001], [0007]. *Rauhala* states that such techniques are “appli[cable] in the reception circuits of mobile stations,” such as mobile phones, which are transceivers. Ex. 1004 at [0001], [0012].

152. *Rauhala* discloses that a signal path includes a detector DET coupled to an output of a filter. Ex. 1004 at [0012] and FIG. 2 (annotated below). *Rauhala* further teaches that “[d]etector DET provides information about the signal strength (RSS) on the channel to which the receiver is tuned.” Ex. 1004 at [0013].



153. It is my opinion that a person of ordinary skill in the art would have recognized that the *Rauhala*’s detector DET is coupled “to the signal path,” as required by claim 23. Detector DET is shown as a functional block in the block diagram and signal path of FIG. 2 (between filter F4 and control unit 22). Ex. 1004 at FIG 2.

154. It is my opinion that a person of ordinary skill would have recognized that, for example, FIG. 2 of *Rauhala* is a block diagram that is a “diagram in which their essential systems units are drawn as blocks, and their relationship to each other is indicated by appropriately connected lines. The path of the signal or energy may be indicates by lines or arrows” and a “chart that graphically depicts the functional

relationships of hardware making up a system. The block diagram serves to indicate the various data and control **signal paths** between functional units of the system hardware.” Ex. 1011 at 7 (emphasis added).

155. Therefore, it is my opinion that a person of ordinary skill in the art would have understood that the *Rauhala* detector DET is coupled to the signal path.

156. *Rauhala* discloses that in “normal conditions, i.e. when the signal strength is satisfactory on the receive channel and ordinary on the neighboring channels, the supply currents of the receiver's front-end amplifiers and at least the first mixer are kept relatively low. If the signal strength goes below a certain value on the receive channel or exceeds a certain value on a neighboring channel, said supply currents are increased.” Ex. 1004 at [0006].

157. As a result of the techniques of *Rauhala*, “the energy consumption of the receiver can be reduced without degrading the signal quality,” leading to “longer life for the battery or [. . .] a smaller battery can be used.” Ex. 1004 at [0007].

158. As such, it is my opinion that *Rauhala* is in the same technical field as *Cummins* and the '330 patent, because all three relate to wireless transceivers, and in particular to reducing power consumption for wireless transceivers in order to improve battery life. A person of ordinary skill would have recognized the similarities between *Cummins* and the *Rauhala* device and have been motivated to combine them make a device that improves battery life in a wireless transceiver

like *Cummins*, and doing so by determining signal strength and adjusting impedances and supply currents like in *Rauhala*.

159. A person of ordinary skill would have had a reasonable expectation of success in combining the disclosures of *Cummins* and *Rauhala* at least because both combinations would have used known technologies (for example, the well-known wireless transceiver of *Cummins*) according to known methods (for example determining signal strength to adjust impedance and supply current as in *Rauhala*) to yield predictable results (for example, improving battery life or reducing battery size of the *Cummins* device).

160. Moreover, it is my opinion that modification of *Cummins* with the teachings of *Rauhala* would have amounted to nothing more than the use of a known technique to improve a similar device, and the results of the modification would have been predictable. This is because at the time of the invention, a person of ordinary skill would have had the requisite skill level to readily modify the device disclosed by *Cummins* to implement the teachings of *Rauhala*. Moreover, such modifications of *Cummins* would have been routine for the person of ordinary skill as they use well-known elements with no change in their respective functions.

f. Claim 23[vi]. “[wherein an impedance in the signal path is configured to be dynamically adjusted to] reduce a switching current [in response to the first signal strength]”

161. As will be explained in further detail below, it is my opinion that one of ordinary skill in the art would have recognized that the collector current $I/2$ is a “switching current.”

162. The ’330 specification does not expressly define “switching current.”

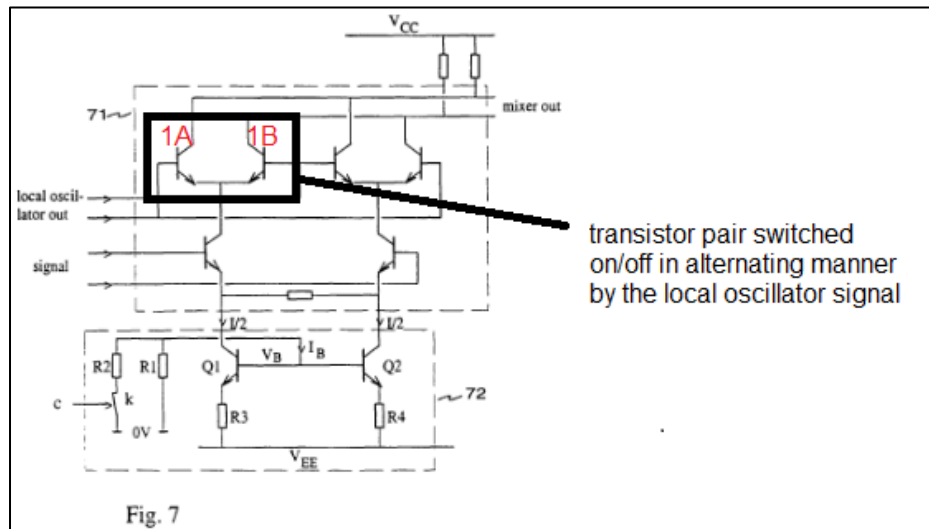
However, the patentee did expressly define “switching current” to be “a dynamic or transient current that occurs during voltage transitions,” during prosecution of the ’330 patent. In particular, In the response, the patentee argued that:

A bias current is not the same as a switching current. One skilled the art understands that a bias current is a DC or quiescent current, while a switching current is a dynamic or transient current that occurs during voltage transitions. (See for example, the pending application, Figure 6 and related discussion.) Accordingly, the cited references do not show or suggest reducing a switching current in the signal path by dynamically changing an impedance of a component in the signal path as required by the claim.

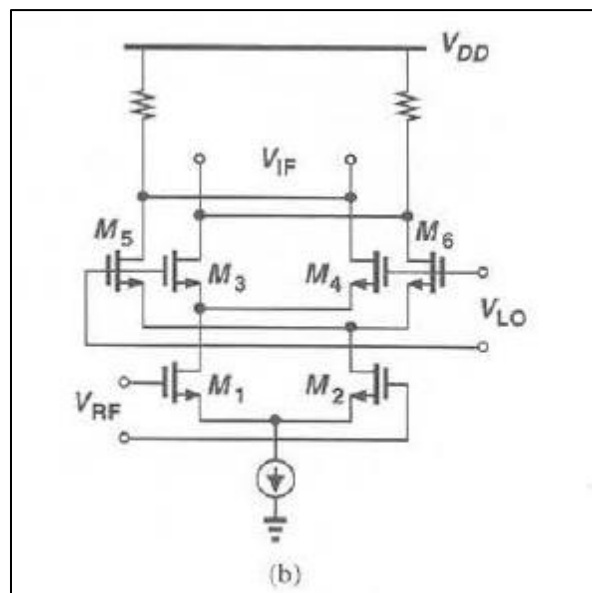
Ex. 1003 at 163.

163. FIG. 7 of *Rauhala* shows a double-balanced mixer with two switching pairs of transistors. Ex. 1004 at [0023] and FIG. 7. The switching pairs are driven by a local oscillator. *Id.* A first switching pair includes a first transistor (annotated 1A) and a second transistor (annotated 1B). *Id.* It is my opinion that a person of ordinary skill in the art would have understood that the signal from the local

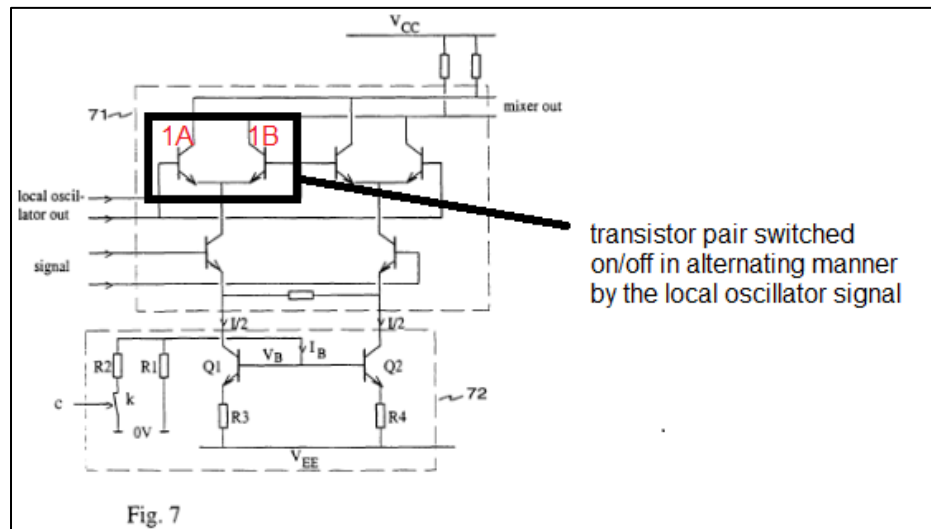
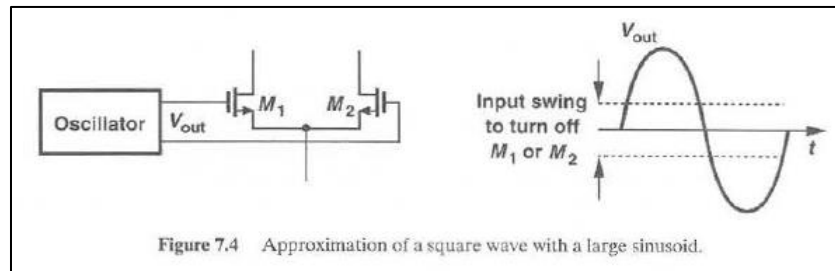
oscillator would switch first transistor 1A and second transistor 1B in a complementary manner.



164. A double-balanced mixer is well-known, see Ex. 1012 at 5-6. For example, FIG. 6.19b (reproduced below), where M3 and M4 are a first switching, differential pair and M5 and M6 are a second switching, differential pair. *Id.*



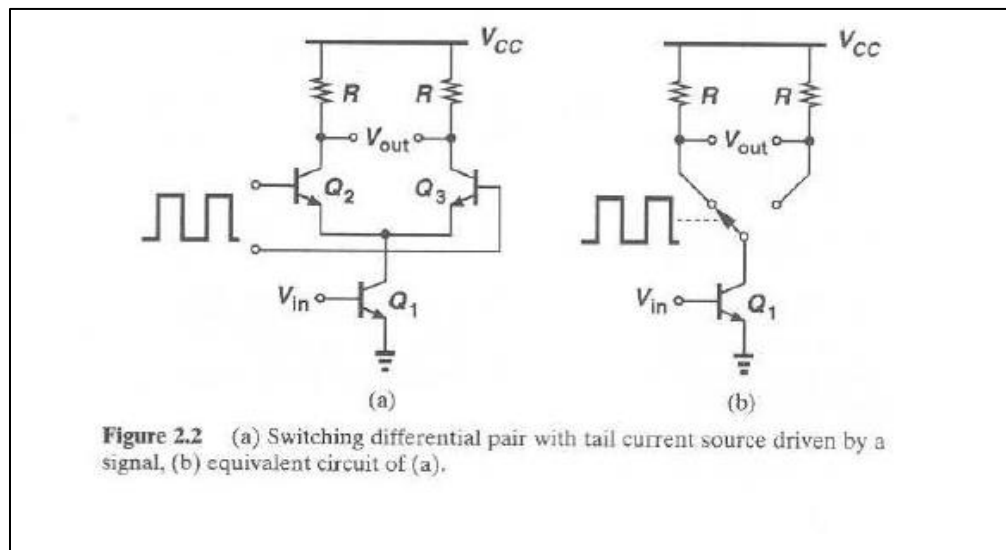
165. *Rauhala* FIG. 7 shows a local oscillator output being directed to each of the two switching pairs. As evidenced by Ex. 1012 at FIG. 7.4, the local oscillator of *Rauhala* would output an oscillating signal that switches the pair of transistors 1A/1B on and off in an alternating fashion. Ex. 1012 at 7. That is, when first transistor 1A is on, second transistor 1B is off. Also, when second transistor 1B is on, first transistor 1A is off.

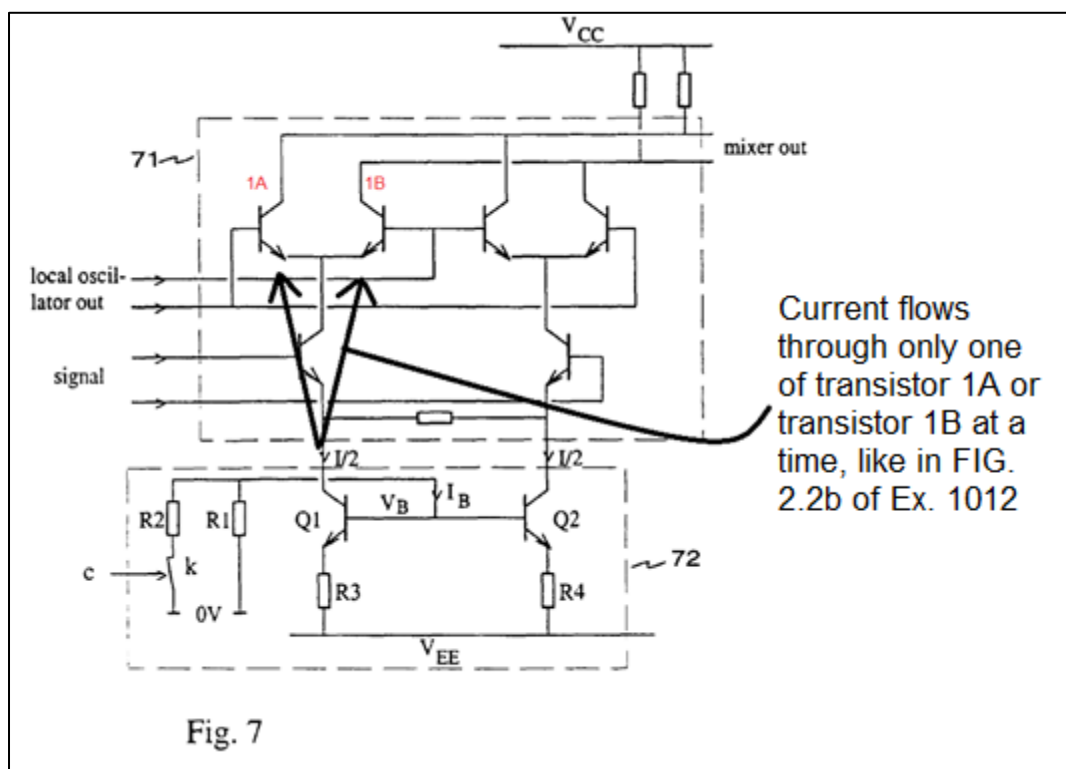


166. Ex. 1012 also shows how a local oscillator signal is used for switching in a mixer. Ex. 1012 at 4. Fig. 2.2a (reproduced below) specifically shows switching a differential pair of transistors using a local oscillator signal, and FIG. 2.2b (also reproduced below) shows the equivalent circuit of the differential pair switching on

an off. In other words, FIG. 2.2b, shows how the local oscillator signal switches the differential pair on and off, so that current flows through only one transistor of the differential pair at a given time.

167. Annotated FIG. 7 of *Rauhala* below shows how current $I/2$ is directed to one of transistor 1A or transistor 1B at a time, in the same manner as Ex. 1012 at FIGs. 2.2a and 2.2b.



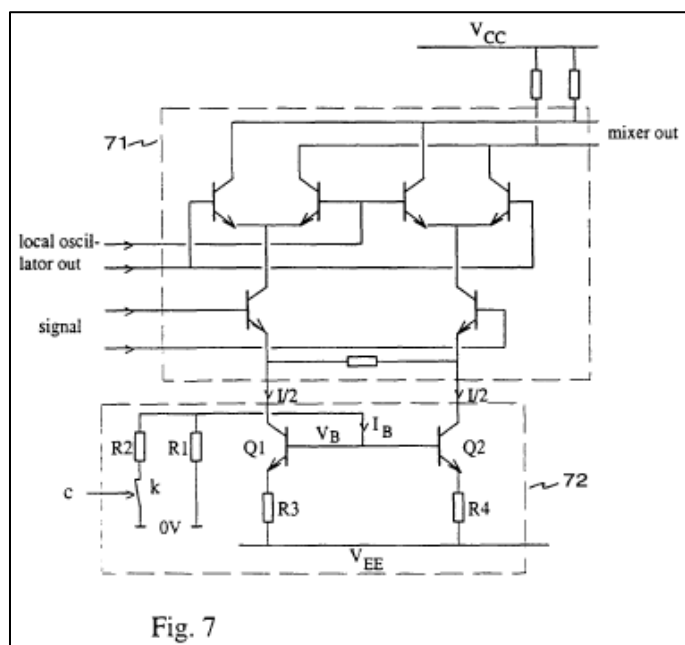


168. Therefore, it is my opinion that a person of ordinary skill would have understood that the current $I/2$ directed to transistors 1A and 1B is a “switching current” as defined by the patentee because it is “a dynamic or transient current that occurs during voltage transitions.” Each on-off switching event at transistors 1A/1B of *Rauhala* is a voltage transition. The current $I/2$ is dynamic because it is transient and dynamic, as it is constantly switched from first transistor 1A or second transistor 1B.

- g. Claim 23[vii]. “wherein an impedance in the signal path is configured to be dynamically adjusted [to reduce a switching current in response to the first signal strength]”**

169. *Rauhala* shows two resistors R_1 and R_2 that are in parallel to one another.

Ex. 1004 at [0023] and FIG. 7.



170. Therefore, the resistance of the parallel circuit can be switched between two different resistance configurations. Ex. 1004 at [0023]. The first (low) resistance configuration is when the switch k is closed such that resistor R2 is placed in parallel with R1. *Id. Rauhala* discloses that the control current I_B when switch k is closed is equal to $V_B/R1 + V_B/R2$, where V_B is the magnitude of the transistors' base voltage (e.g., the current through resistor R1 is $(0 - V_B)/R1$ but V_B is a negative voltage and so $-V_B$ is a positive voltage, that is, $-V_B$ is the magnitude of

VB). *Id.* A person of ordinary skill in the art would have understood that as more resistors are added in parallel in a circuit, the equivalent resistance of the circuit decreases and the total current of the circuit increases. *See* Ex. 1022 at 4-5. As shown in Fig. 3-4 of Ex. 1022, “[f]or three circuit elements connected in parallel as shown in Fig. 3-4, KCL states that the current i entering the principal node is the sum of the three current leaving the node through the branches.” *Id.*

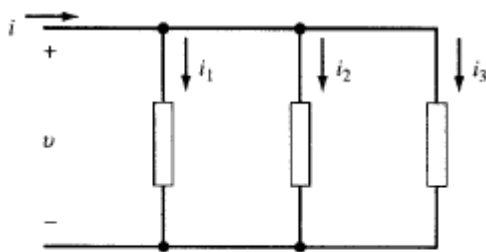


Fig. 3-4

$$i = i_1 + i_2 + i_3$$

171. The second (high resistance) configuration is when the switch k is open such that the resistance of the circuit is equal to R1. *Rauhala* discloses that the control current I_B when switch k is open is equal to a low value $VB/R1$. Ex. 1004 at [0023].

172. The impedance (high or low), and the control current (low or high), based on the state of switch k is summarized in the table below.

Switch k	Impedance	Control Current I_B
Closed	Low	High ($VB/R1$)

		+ V_B/R_2)
Open	High	Low (V_B/R_1)

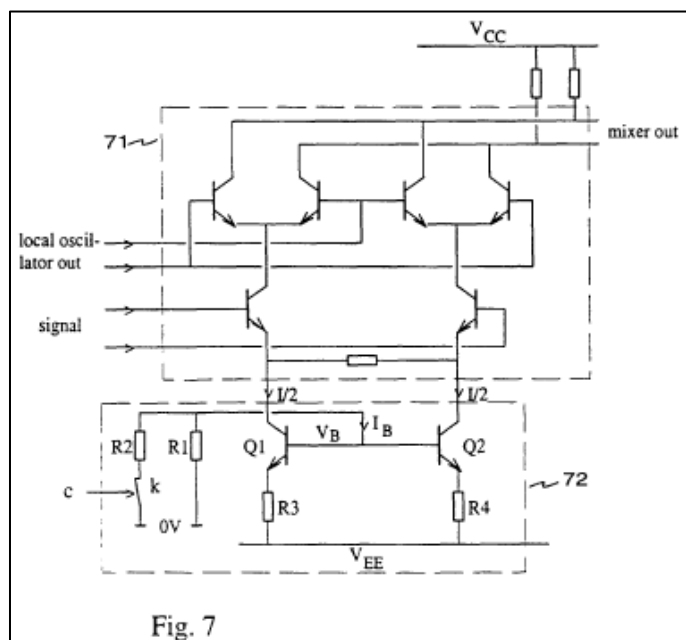
173. In the example of FIG. 7, the state of switch k depends on the control signal c. Ex. 1004 at [0023]. When signal c is 0, switch k is open. *Id.* When signal c is 1, switch k is closed. *Id.*

Control signal c (dependent on signal strength)	k	Impedance	Control Current I_B
1	Closed	Low	High (V_B/R_1 + V_B/R_2)
0	Open	High	Low (V_B/R_1)

174. *Rauhala* discloses that as the control current I_B increases, the supply current I increases. Ex. 1004 at [0023]. A person of ordinary skill would have understood that as control current I_B decreases, the current flowing in Q1 and Q2 decreases, since the current in Q1 and Q2 is controlled by I_B , and thus the supply current I, that provides current to Q1 and Q2 (and thus the rest of the circuit) also would decrease.

175. *Rauhala* further discloses that in FIG. 7, the resistances of resistors R3 and R4 are identical and transistors Q1 and Q2 are identical, and thus the collector

currents ($I/2$) of the transistors are also identical, i.e., the analog multiplier 71 receives a supply current I from Q1 and Q2. Ex. 1004 at [0023].



176. Since the control current I_B is reduced when the impedance of control circuit 72 is increased, and supply current (I) is reduced when the control current is reduced, a person of ordinary skill would have understood that the collector current $I/2$ is reduced when the impedance of the control circuit 72 is increased. *See* Ex. 1021 at 4 and FIG. 1.27, reproduced below (showing a linear relationship between the base current I_B and the collector current I_C).

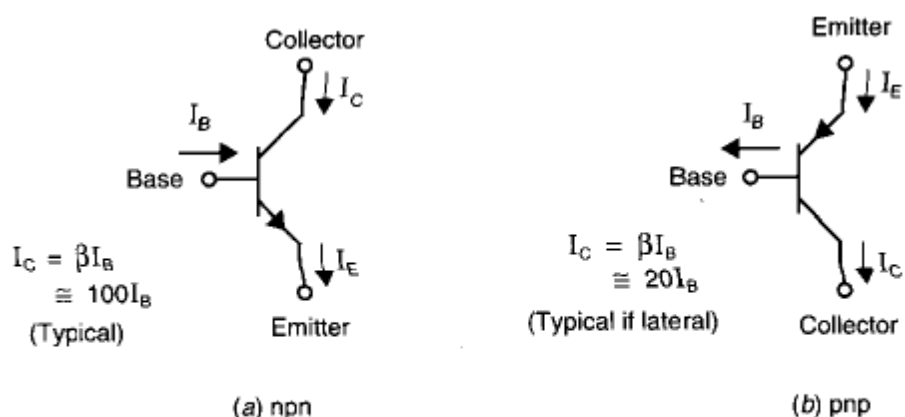


Fig. 1.27 The symbols representing (a) an npn bipolar-junction transistor and (b) a pnp bipolar-junction transistor.

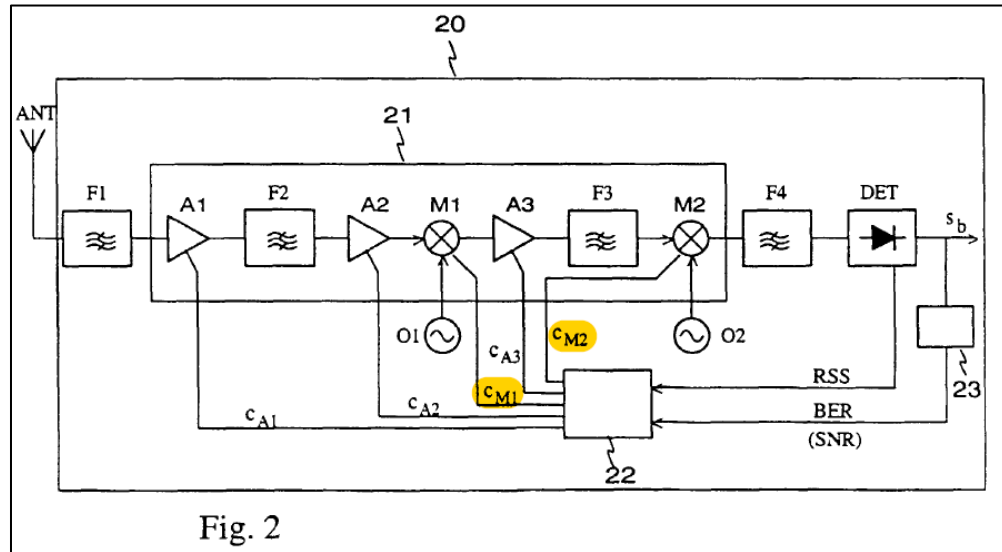
177. These relationships are summarized in the table below.

Control signal c (dependent on signal strength)	k	Impedance	Control Current I_B	Supply Current I	Collector Current I/2
1	Closed	Low	High ($V_B/R_1 + V_B/R_2$)	High	High
0	Open	High	Low (V_B/R_1)	Low	Low

h. Claim 23[viii]. “[wherein an impedance in the signal path is configured to be dynamically adjusted to reduce a switching current] in response to the first signal strength”

178. *Rauhala* discloses that the detected signal strength RSS is directed to a control unit 22. Ex. 1002 at [0013] and FIG. 2. Control unit 22 outputs control signals to the linear units (e.g., the amplifiers and mixers). *Id.* For example, control

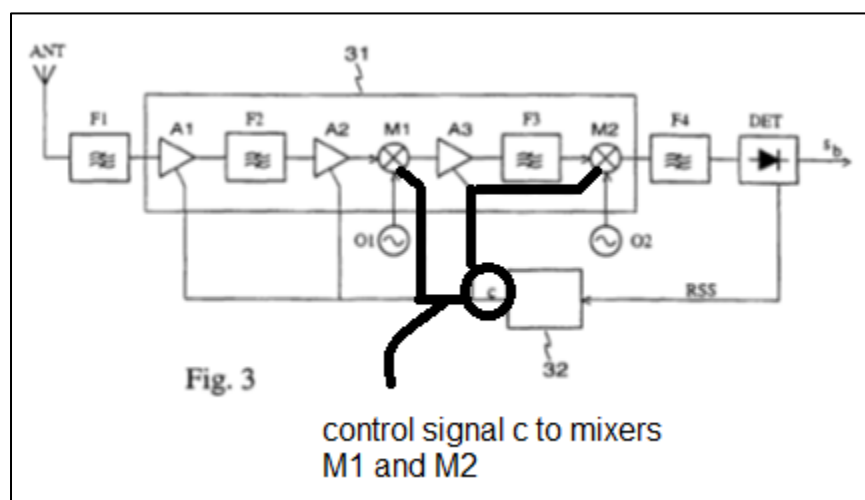
signal cM1 sets the supply current of mixer M1 and signal cM2 sets the supply current of mixer M2. *Id.*



179. *Rauhala's* FIG. 3 is one example of supply current control for the linear units. Ex. 1004 at [0015]. A control unit 32 only receives the receive signal strength RSS information which has threshold values S31 and S32. *Id.* The control unit 32 produces one one-bit control signal c, which is taken to all linear units A1, A2, M1, A3 and M2. *Id.* The supply current of a given linear unit has two values. Supply currents are controlled with signal c according to the annotated table below. *Id.*

RSS	c	I_i	
$\leq S31$	0	I_h	high current condition
$>S31, <S32$	1	I_l	low current condition
$\geq S32$	0	I_h	high current condition

180. The control signal c is taken to all linear units, including each of the mixers M1 and M2. *Id.*



181. The value of control signal c depends upon the detected signal strength RSS. *Id.* When the measured current is below threshold S31, signal c is 0 and the linear unit (including amplifier) supply currents are at their higher values. *Id.* The relatively large supply currents help reduce the effects of possible interference from outside the receive channel. *Id.* When the signal strength RSS is between S31 and S32, signal c is 1 and the supply currents are at their lower values. *Id.* The relatively small supply currents help reduce energy consumption. *Id.* The

relationship of the detected signal strength RSS and the control signal c is shown again in the table below.

182. *Rauhala* discloses other schemes for controlling the supply current of mixers M1 and M2 based on the signal strength indication. For example, FIGs. 4 and 5 show more complicated schemes for controlling the supply current to mixers M1 and M2. Ex. 1004 at [0017]-[0020]. Furthermore, the disclosed value of c (as either 0 or 1) does not uniformly correspond to the same high or low current state. For example, when c is 0 in the scheme of FIG. 3, the mixer is in a high current state, and when c is 1, the mixer is in a low current state. Ex. 1004 at [0015]. However, in the scheme of FIG. 4, when “signal c_M is 0, the supply current in question is lower, and conversely, if signal [] c_M is 1, the supply current is higher.” Ex. 1004 at [0017].

183. It is my opinion that a person of ordinary skill in the art would have recognized that signal strength being measured by *Rauhala* is dynamic and changing based on various factors. *LeBlanc* illustrates that it was well-known in the art to a person of ordinary skill that the behavior of wireless signals (including their strength) is unique and complicated, and is affected by multiple factors. Ex. 1020 at 2:40-51. For example, *LeBlanc* states that:

The behavior of a mobile radio signal in the general environment is unique and complicated.

...

Factors include terrain undulations, fixed and variable clutter, atmospheric conditions, internal radio characteristics of cellular and PCS systems, such as frequencies, antenna configurations, modulation schemes, diversity methods, and the physical geometry of direct, refracted and reflected waves between the base stations and the mobile.

Id.

184. It is my opinion that a person of ordinary skill would have understood that signal strength being measured by the *Rauhala* patent, changes based on the environment of the signal being measured, as evidenced by *LeBlanc*. *Rauhala* relates to mobile phones, and thus, the environment of the signals being measured by *Rauhala* will be constantly changed during the use of the mobile phone in different areas, and therefore will experience different terrain undulations, different amounts of fixed and variable clutter, different atmospheric conditions, and the like, resulting in different measured signal strength.

185.

XII. RAUHALA IN COMBINATION WITH MEADOR DISCLOSES OR SUGGESTS ALL FEATURES OF CLAIM 29 OF THE '330 PATENT

186. It is my opinion that *Cummins* in combination with *Rauhala* discloses each and every element of claim 29.

1. Claim 29

a. Claim 29[i]. “A wireless transceiver integrated circuit comprising:”

187. *Rauhala* describes methods “for linearizing a radio receiver” in which “the energy consumption of the receiver can be reduced without degrading the signal quality.” Ex. 1004 at [0001], [0007]. *Rauhala* states that such techniques are “appli[cable] in the reception circuits of mobile stations,” such as mobile phones, which are transceivers. Ex. 1004 at [0001], [0012].

188. *Meador* is directed “in general to radio transceivers, and more particularly, to integrated circuit devices that implement transceiver functions.” Ex. 1006 at 1:5-7. *Meador* discloses that “[t]here has been a desire to integrate as many functions as feasible on a single integrated circuit when implementing a radio transceiver”, and that “[a]n entire transceiver system integrated on a common substrate would tend to reduce cost and increase reliability.” *Meador* discloses that “a configurable single-chip radio transceiver is needed.” Ex. 1006 at 1:27-37.

189. *Meador* discloses a “configurable single-chip transceiver integrated circuit (IC) architecture.” Ex. 1006 at 1:66-67. The “single-chip transceiver IC has multiple on-chip circuits that implement receiver functions, transmitter functions, and audio processing functions, among others.” Ex. 1006 at 2:1-2:3.

190. The resultant integrated transceiver system allows for flexibility in improving performance and functionality. Ex. 1006 at 7:63-65.

191. As such, *Meador* is in the same technical field as *Rauhala* and the '330 patent, because all three relate to wireless transceivers, and in particular to reducing power consumption for wireless transceivers in order to improve battery life. It is my opinion that a person of ordinary skill would have recognized the similarities between *Rauhala* and the *Meador* device, and have been motivated to combine them make a device that improves reliability and reduces cost of a device like *Rauhala*, and doing so by integrating as many functions as feasible onto an integrated circuit as in *Meador*.

192. It is my opinion that a person of ordinary skill would have had a reasonable expectation of success in combining the disclosures of *Rauhala* and *Meador* at least because both combinations would have used known technologies (for example, the well-known wireless transceiver of *Rauhala*) according to known methods (for example integrating transceiver components onto a single integrated circuit as in *Meador*) to yield predictable results.

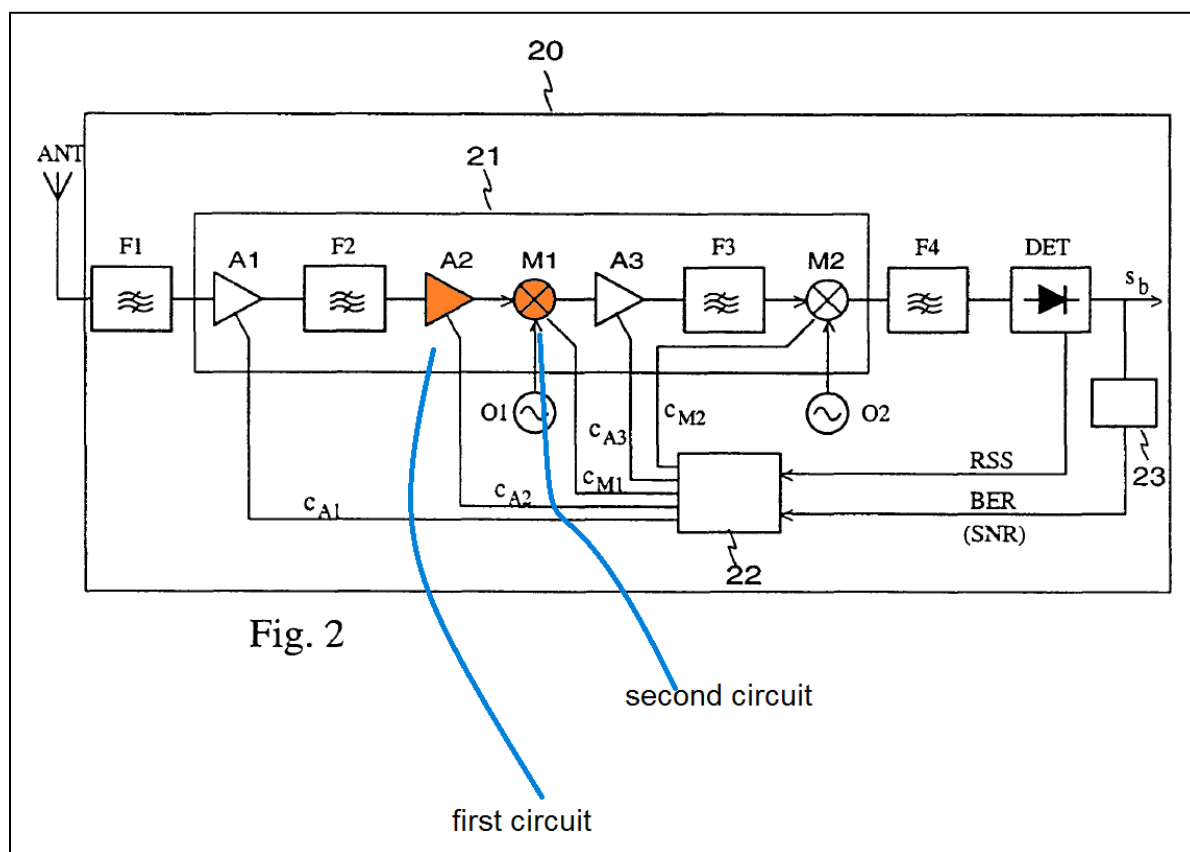
193. Moreover, it is my opinion that modification of *Rauhala* with the teachings of *Meador* would have amounted to nothing more than the use of a known technique to improve a similar device, and the results of the modification would have been predictable. This is because at the time of the invention, a person of

ordinary skill would have had the requisite skill level to readily modify the device disclosed by *Rauhala* to implement the teachings of *Meador*. Moreover, such modifications of *Rauhala* would have been routine for the person of ordinary skill as they use well-known elements with no change in their respective functions.

b. Claim 29[ii]. “a receiver comprising a signal path, the signal path comprising: a first circuit; and a second circuit having an input coupled to an output of the first circuit”

194. *Rauhala* Fig. 1 is a simplified example of a radio receiver without the low-frequency components. An antenna ANT is coupled to a duplex filter F1, which is needed e.g. in mobile phones. Filter F1 is coupled to a low-noise pre-amplifier A1. Amplifier A1 is coupled to a channel selector filter F2 in the tuner, and filter F2 is coupled to an amplifier A2. The output of amplifier A2 is coupled to the first input of a first mixer M1. Ex. 1004 at [0012]. FIG. 2, reproduced below, shows a similar path structure as FIG. 1. Ex. 1004 at [0013].

195. *Rauhala* teaches a receiver signal path comprising at least an amplifier, a mixer and a filter. Ex. 1004 at [0013]. A person of ordinary skill would have understood that *Rauhala*’s amplifier A2 is a first circuit, and that *Rauhala*’s mixer M1 is a second circuit coupled to an output of the first circuit (the amplifier A2).



196. A person of ordinary skill in the art would have understood that a circuit is an “interconnection of a number of devices in one or more closed paths to perform a desired electrical or electronic function. Example of simple circuits are high- or low-pass filters, multivibrators, oscillators, and amplifiers.” Ex. 1011 at 8.

Furthermore, a mixer is a “circuit that generates output frequencies equal to the sum and difference of two input frequencies.” Ex. 1011 at 10. The specification of the '330 patent further discloses that amplifiers and mixers are each considered a “circuit.”

Embodiments of the present invention may be used to reduce the power dissipation of one or more of these included circuits. For example, the power

dissipation in the low-noise amplifier 102, down-convert mixers 104 and 106, low pass filters 108 and 110, or baseband amplifiers 114 and 116 may be optimized. Also, power dissipation in up-convert mixers 124 126, variable gain amplifier 128, and power amplifier 130 may also be optimized.

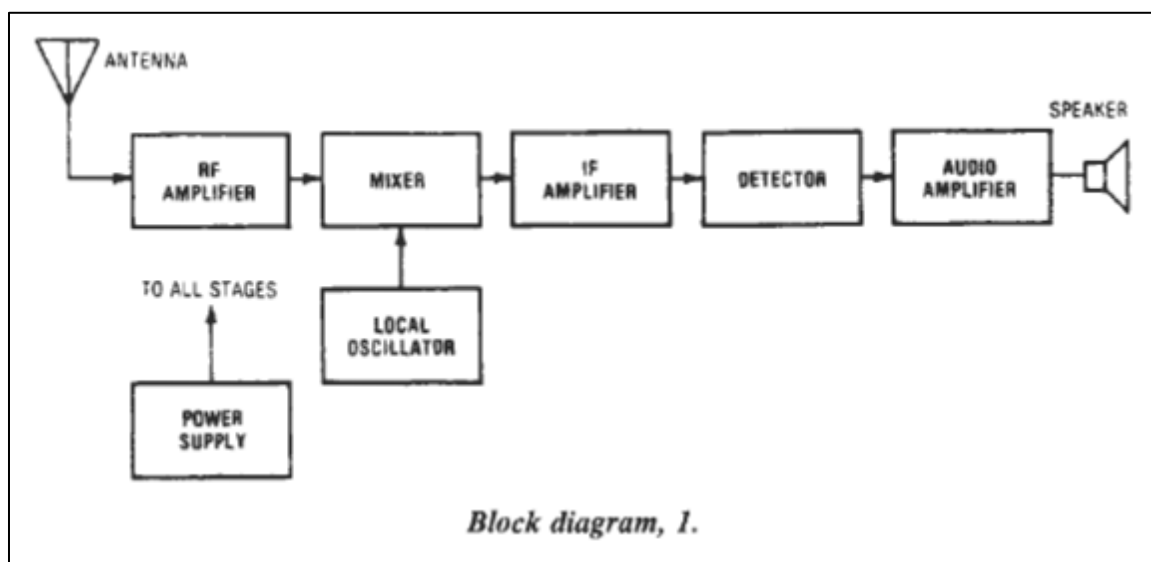
FIG. 8A is a block diagram of a functional block 820 and optional gain element 810 in accordance with an embodiment of the present invention. Functional block 820, like the functional blocks in the following diagrams, may be a filter, mixer, amplifier, or other circuit or circuits in a wireless transceiver or other electronic circuits or system.

Ex. 1001 at 5:4-11 and 8:20-25.

197. Still further, claim 21 of the '330 patent recites that “the first circuit is a low-noise amplifier” and claim 22 of the '330 patent recites that “first circuit is a mixer.” Ex. 1001 at 14:11-14.

198. A person of ordinary skill would have recognized that, for example, FIG. 2 of *Rauhala* is a block diagram that is a “diagram in which their essential systems units are drawn as blocks, and their relationship to each other is indicated by appropriately connected lines. The path of the signal or energy may be indicates by lines or arrows” and a “chart that graphically depicts the functional relationships of hardware making up a system. The block diagram serves to indicate the various data and control **signal paths** between functional units of the system hardware.”

Ex. 1011 at 7 (emphasis added).

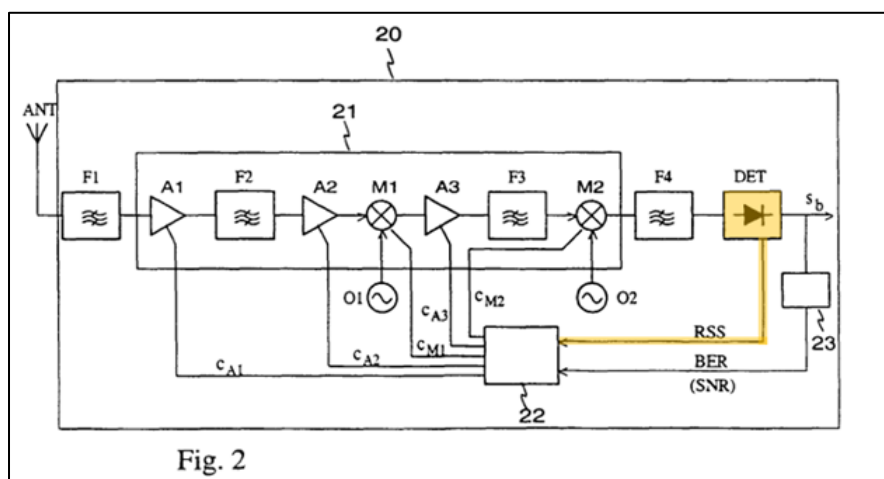


Id.

199. It is my opinion that a person of ordinary skill in the art would have understood that the block diagram of FIG. 2 of *Cummins* shows a signal path, and that the components represented in the block diagrams, amplifier A2 and mixer M1, and others, are included in the signal path.

c. Claim 29[iii]. “a first signal strength indicator circuit coupled to the signal path, and configured to determine a first signal strength”

200. *Rauhala* discloses that a signal path includes a detector DET coupled to an output of a filter. Ex. 1004 at [0012] and FIG. 2 (annotated below). *Rauhala* further teaches that “[d]etector DET provides information about the signal strength (RSS) on the channel to which the receiver is tuned.” Ex. 1004 at [0013].



201. It is my opinion that a person of ordinary skill in the art would have recognized that the *Rauhala*'s detector DET is coupled "to the signal path," as required by claim 23. Detector DET is shown as a functional block in the block diagram and signal path of FIG. 2 (between filter F4 and control unit 22). Ex. 1004 at FIG 2.

202. It is my opinion that a person of ordinary skill would have recognized that, for example, FIG. 2 of *Rauhala* is a block diagram that is a "diagram in which their essential systems units are drawn as blocks, and their relationship to each other is indicated by appropriately connected lines. The path of the signal or energy may be indicates by lines or arrows" and a "chart that graphically depicts the functional relationships of hardware making up a system. The block diagram serves to indicate the various data and control **signal paths** between functional units of the system hardware" Ex. 1011 at 7 (emphasis added).

203. Therefore, it is my opinion that a person of ordinary skill in the art would have understood that the *Rauhala* detector DET is coupled to the signal path.

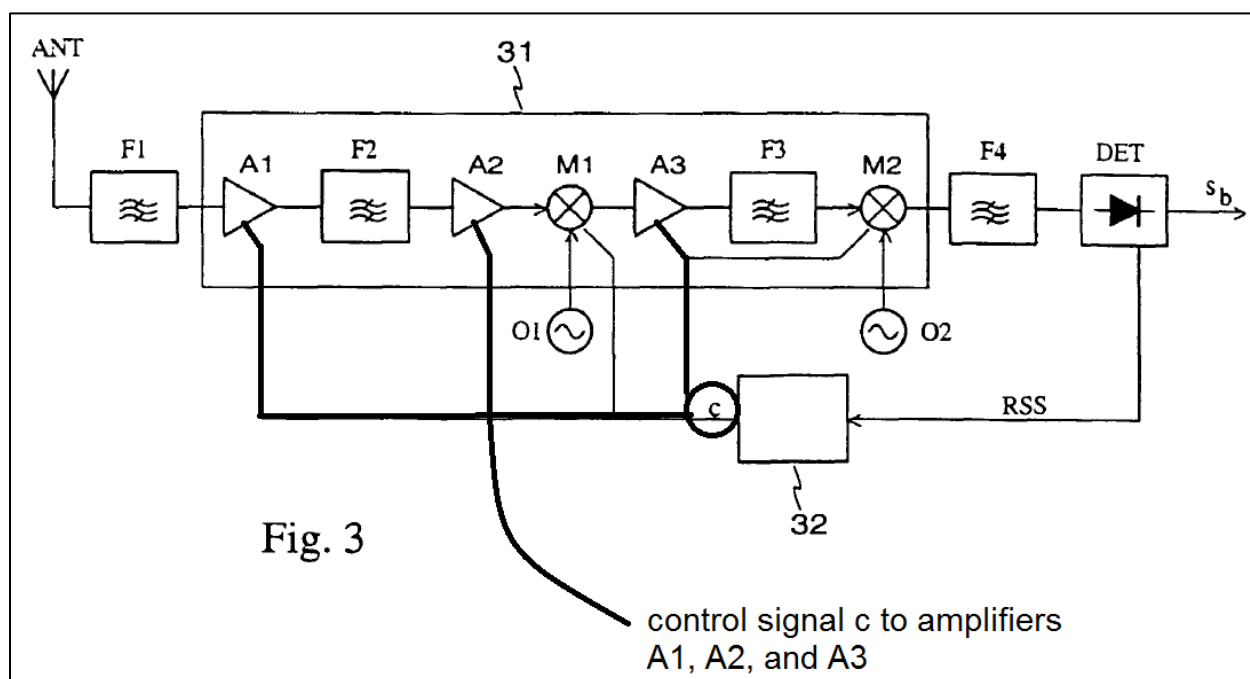
d. Claim 29[iv]. “wherein a gain of the first circuit is configured to be dynamically adjusted in response to the first signal strength”

204. *Rauhala* discloses that the detected signal strength RSS is directed to a control unit 22. Ex. 1002 at 13. Control unit 22 outputs control signals to the linear units (e.g., the amplifiers and mixers). *Id.* For example, control signal cA1 sets the supply current of amplifier A1. *Id.* Similarly, signal cA2 sets the supply current of amplifier A2, signal cM1 that of mixer M1, signal cA3 that of amplifier A3, and signal cM2 that of mixer M2. *Id.*

205. *Rauhala*’s FIG. 3 is one example of supply current control for the linear units. Ex. 1004 at [0015]. A control unit 32 only receives the receive signal strength RSS information which has threshold values S31 and S32. *Id.* The control unit 32 produces one one-bit control signal c, which is taken to all linear units A1, A2, M1, A3 and M2. *Id.* The supply current of a given linear unit has two values. Supply currents are controlled with signal c according to the annotated table below. *Id.*

RSS	c	I_i	
$\leq S31$	0	I_h	high current condition
$>S31, <S32$	1	I_l	low current condition
$\geq S32$	0	I_h	high current condition

206. The control signal c is taken to all linear units, including each of the amplifiers A1, A2, and A3. *Id.*



207. The value of control signal c depends upon the detected signal strength RSS. *Id.* When the measured current is below threshold S31, signal c is 0 and the linear unit (including amplifier) supply currents are at their higher values. *Id.* The relatively large supply currents help reduce the effects of possible interference from outside the receive channel. *Id.* When the signal strength RSS is between S31

and S32, signal c is 1 and the supply currents are at their lower values. *Id.* The relatively small supply currents help reduce energy consumption. *Id.* The relationship of the detected signal strength RSS and the control signal c is shown again in the table below.

208. *Rauhala* discloses other schemes for controlling the supply current of mixers M1 and M2 based on the signal strength indication. For example, FIGS. 4 and 5 show more complicated schemes for controlling the supply current to amplifiers A1, A2, and A3. Ex. 1004 at [0017]-[0020]. Furthermore, the disclosed value of c (as either 0 or 1) does not uniformly correspond to the same high or low current state. *Rauhala* also discloses that the control signal c can be a two-bit digital signal Ex. 1004 at [0021].

209. It is my opinion that a person of ordinary skill in the art would have recognized that signal strength being measured by *Rauhala* is dynamic and changing based on various factors. *LeBlanc* illustrates that it was well-known in the art to a person of ordinary skill that the behavior of wireless signals (including their strength) is unique and complicated, and is affected by multiple factors. Ex. 1020 at 2:40-51. For example, *LeBlanc* states that:

The behavior of a mobile radio signal in the general environment is unique and complicated.

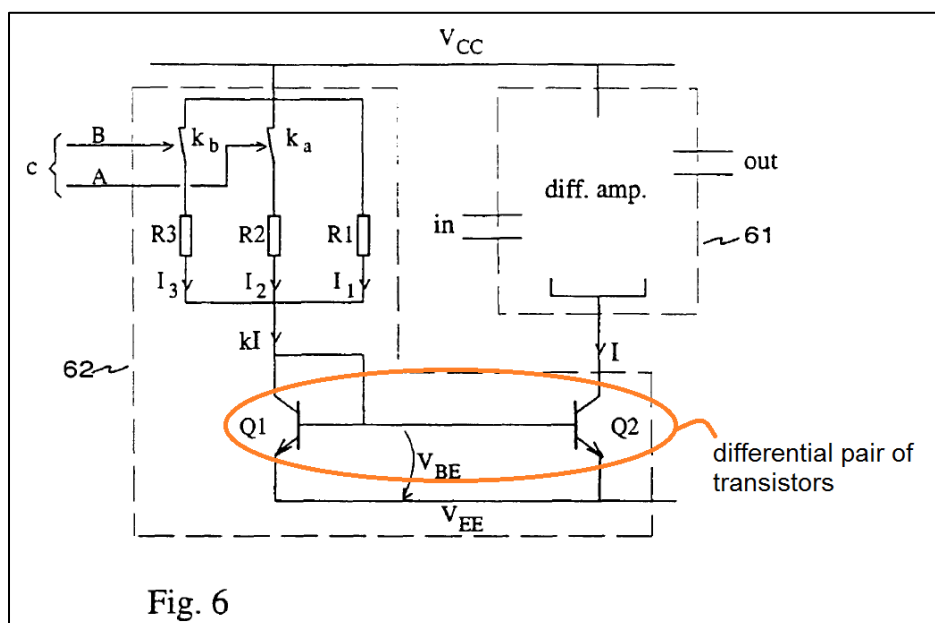
...

Factors include terrain undulations, fixed and variable clutter, atmospheric conditions, internal radio characteristics of cellular and PCS systems, such as frequencies, antenna configurations, modulation schemes, diversity methods, and the physical geometry of direct, refracted and reflected waves between the base stations and the mobile.

Id.

210. It is my opinion that a person of ordinary skill would have understood that signal strength being measured by the *Rauhala* patent, changes based on the environment of the signal being measured, as evidenced by *LeBlanc*. *Rauhala* relates to mobile phones, and thus, the environment of the signals being measured by *Rauhala* will be constantly changed during the use of the mobile phone in different areas, and therefore will experience different terrain undulations, different amounts of fixed and variable clutter, different atmospheric conditions, and the like, resulting in different measured signal strength.

211. Fig. 6 of *Rauhala* in particular shows an example of supply current control for an amplifier 61. Ex. 1004 at [0021]. In this example the amplifier 61 is a differential amplifier, a “diff. amp.” that is biased, as in Fig. 7, using transistors Q1 and Q2. *Id.*



212. The supply current for the amplifier is controlled by changing the impedance of control circuit 62, using control signals A and B, which form a two bit control signal c (where $c = AB$). *Id.* The control signal c is based on the determined signal strength RSS. Ex. 1004 at [0013]-[0021]. The control for current kI and the current I is described in the table below. *Id.* Therefore, the impedance of the control circuit 62 and the total supply current $kI + I$ is based on the determined signal strength RSS.

B	A	kI	kI/I_1
0	0	I_1	1
0	1	$I_1 + I_2$	2 if $R1 = R2$
1	0	$I_1 + I_3$	3 if $R1 = 2 \cdot R3$
1	1	$I_1 + I_2 + I_3$	4 if $R1 = R2 = 2 \cdot R3$

213. It is my opinion that a person of ordinary skill in the art would have understood that *Rauhala*'s control of amplifier supply current/impedance is gain control of the amplifier.

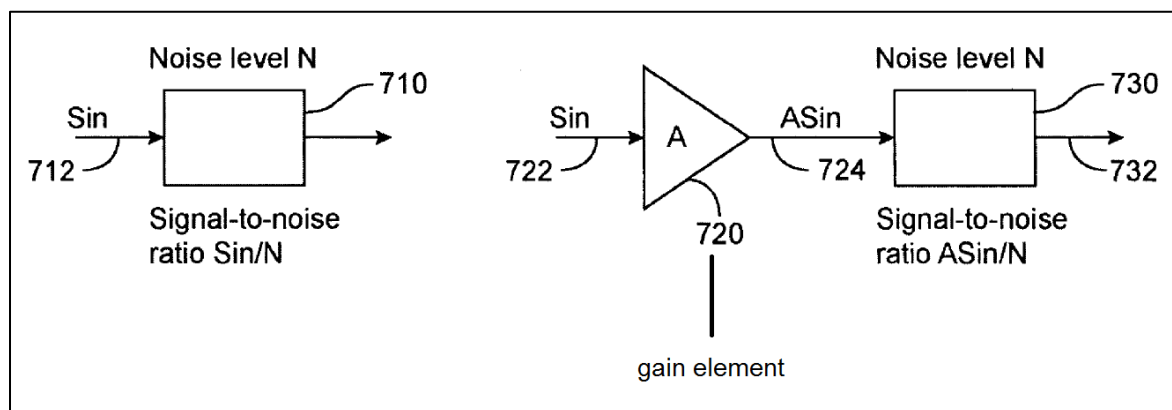
214. Indeed, the specification of the '330 patent discloses:

FIG. 7 illustrates another degree of freedom that made be employed to reduce current levels in a transceiver. Specifically, a gain element 720 may be inserted in front of a circuit block 730 in order to improve the combined circuit's signal-to-noise ratio by a factor equal to the gain of the inserted gain block. This is particularly useful when large interferers are absent and the desired received signal is moderate or low. Specifically, gain is added to the signal while impedances are increased, which raise the noise floor. In this way, a given signal-to-noise ratio may be maintained while the power is decreased.

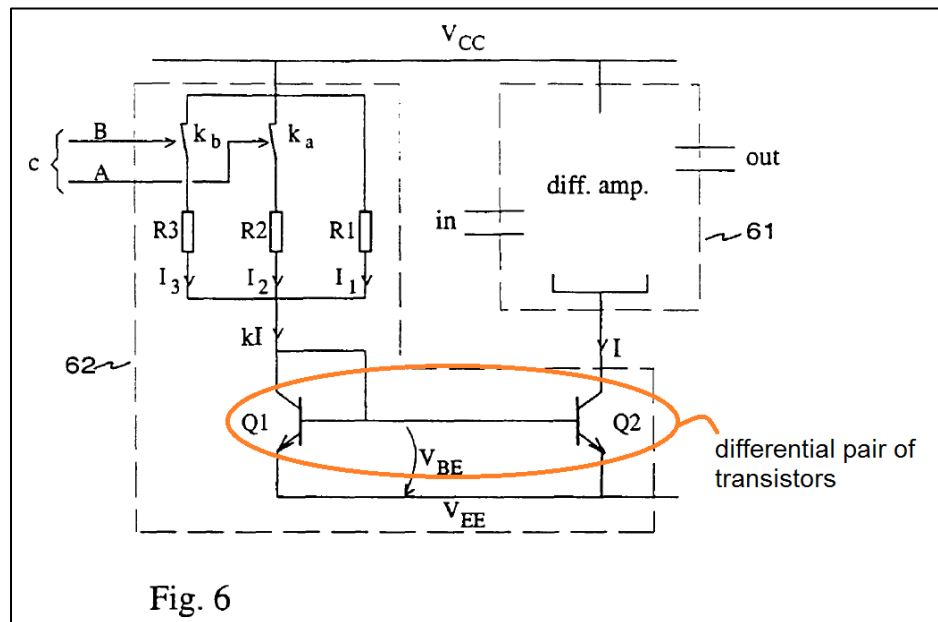
The gain of such an element may be varied by increasing a current in a differential pair or increasing a load resistance using switches. Many other examples where the gain of this element may be varied will be appreciated by one skilled in the art.

These variables, or degrees of freedom, specifically reducing bias currents, increasing impedances, and increasing gain may be used as in the following examples.

Ex. 1001 at 8:1-16 and FIG. 7 (annotated below).



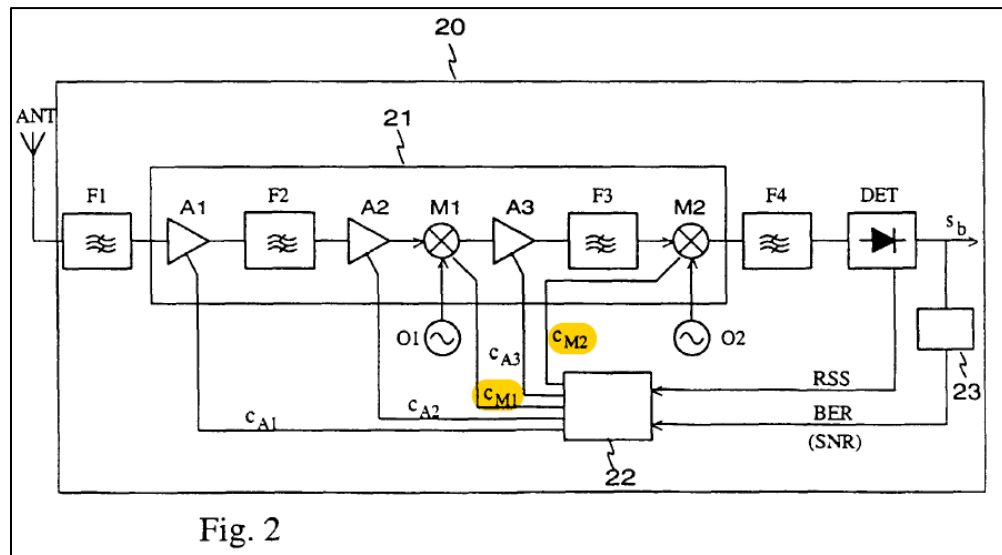
215. It is my opinion that a person of ordinary skill in the art would have recognized that the control of impedance in the control circuit 62 by control signal c (itself dependent on determined signal strength RSS), to adjust the supply current to the differential pair of transistors Q1 and Q2 teaches the claimed feature of “wherein a gain of the first circuit is configured to be dynamically adjusted in response to the first signal strength.” In particular, the ’330 patent itself teaches that the gain of an amplifier (720) may be varied by “increasing a current in a differential pair or increasing a load resistance using switches.” Ex. 1001 at 8:1-16.



- e. Claim 29[v]. “wherein an impedance in the second circuit is configured to be dynamically adjusted in response to the first signal strength.”**

216. It is my opinion that *Rauhala* discloses this claimed feature.

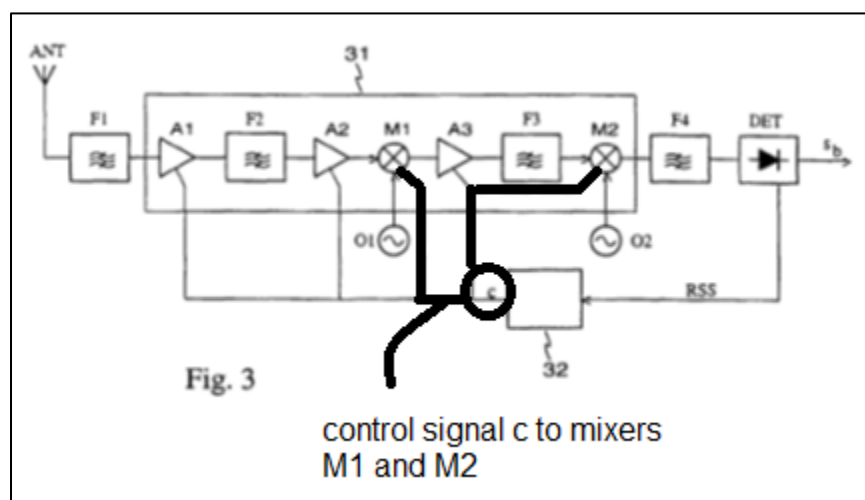
217. *Rauhala* discloses that the detected signal strength RSS is directed to a control unit 22. Ex. 1002 at [0013] and FIG. 2. Control unit 22 outputs control signals to the linear units (e.g., the amplifiers and mixers). *Id.* For example, control signal cM1 sets the supply current of mixer M1 and signal cM2 sets the supply current of mixer M2. *Id.*



218. *Rauhala's* FIG. 3 is one example of supply current control for the linear units. Ex. 1004 at [0015]. A control unit 32 only receives the receive signal strength RSS information which has threshold values S31 and S32. *Id.* The control unit 32 produces one one-bit control signal c, which is taken to all linear units A1, A2, M1, A3 and M2. *Id.* The supply current of a given linear unit has two values. Supply currents are controlled with signal c according to the annotated table below. *Id.*

RSS	c	I_i	
$\leq S31$	0	I_h	high current condition
$>S31, <S32$	1	I_l	low current condition
$\geq S32$	0	I_h	high current condition

219. The control signal c is taken to all linear units, including each of the mixers M1 and M2. *Id.*



220. The value of control signal c depends upon the detected signal strength RSS. *Id.* When the measured current is below threshold S31, signal c is 0 and the linear unit (including amplifier) supply currents are at their higher values. *Id.* The relatively large supply currents help reduce the effects of possible interference from outside the receive channel. *Id.* When the signal strength RSS is between S31 and S32, signal c is 1 and the supply currents are at their lower values. *Id.* The relatively small supply currents help reduce energy consumption. *Id.* The

relationship of the detected signal strength RSS and the control signal c is shown again in the table below.

221. *Rauhala* discloses other schemes for controlling the supply current of mixers M1 and M2 based on the signal strength indication. For example, FIGS. 4 and 5 show more complicated schemes for controlling the supply current to mixers M1 and M2. Ex. 1004 at [0017]-[0020]. Furthermore, the disclosed value of c (as either 0 or 1) does not uniformly correspond to the same high or low current state. For example, when c is 0 in the scheme of FIG. 3, the mixer is in a high current state, and when c is 1, the mixer is in a low current state. Ex. 1004 at [0015]. However, in the scheme of FIG. 4, when “signal c_M is 0, the supply current in question is lower, and conversely, if signal [] c_M is 1, the supply current is higher.” Ex. 1004 at [0017].

222. It is my opinion that a person of ordinary skill in the art would have recognized that signal strength being measured by *Rauhala* is dynamic and changing based on various factors. *LeBlanc* illustrates that it was well-known in the art to a person of ordinary skill that the behavior of wireless signals (including their strength) is unique and complicated, and is affected by multiple factors. Ex. 1020 at 2:40-51. For example, *LeBlanc* states that:

The behavior of a mobile radio signal in the general environment is unique and complicated.

...

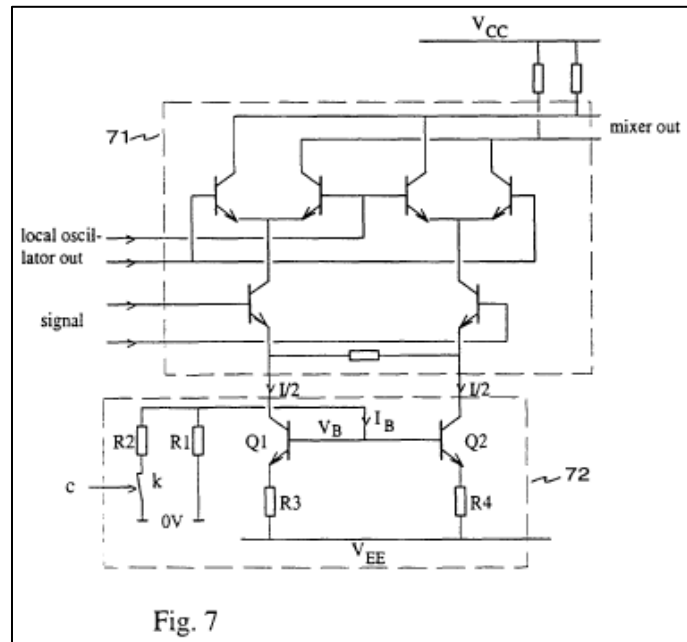
Factors include terrain undulations, fixed and variable clutter, atmospheric conditions, internal radio characteristics of cellular and PCS systems, such as frequencies, antenna configurations, modulation schemes, diversity methods, and the physical geometry of direct, refracted and reflected waves between the base stations and the mobile.

Id.

223. It is my opinion that a person of ordinary skill would have understood that signal strength being measured by the *Rauhala* patent, changes based on the environment of the signal being measured, as evidenced by *LeBlanc*. *Rauhala* relates to mobile phones, and thus, the environment of the signals being measured by *Rauhala* will be constantly changed during the use of the mobile phone in different areas, and therefore will experience different terrain undulations, different amounts of fixed and variable clutter, different atmospheric conditions, and the like, resulting in different measured signal strength.

224. *Rauhala* shows two resistors R1 and R2 that are in parallel to one another.

Ex. 1004 at [0023] and FIG. 7.



225. Therefore, the resistance of the parallel circuit can be switched between two different resistance configurations. Ex. 1004 at [0023]. The first (low) resistance configuration is when the switch *k* is closed such that resistor *R2* is placed in parallel. *Id. Rauhala* discloses that the control current I_B when switch *k* is closed is equal to $V_B/R1 + V_B/R2$, where V_B is the magnitude of the transistors' base voltage (e.g., the current through resistor *R1* is $(0 - V_B)/R1$ but V_B is a negative voltage so $-V_B$ is a positive voltage, that is, $-V_B$ is the magnitude of V_B). *Id.* A person of ordinary skill in the art would have understood that as more resistors are added in parallel in a circuit, the equivalent resistance of the circuit decreases and the total current of the circuit increases. See Ex. 1022 at 4-5. As shown in Fig. 3-4 of Ex. 1022, “[f]or three circuit elements connected in parallel as shown in Fig. 3-

4, KCL states that the current i entering the principal node is the sum of the three current leaving the node through the branches.” *Id.*

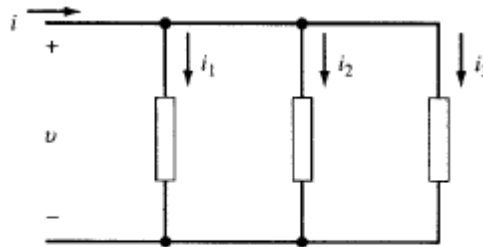


Fig. 3-4

$$i = i_1 + i_2 + i_3$$

226. The second (high resistance) configuration is when the switch k is open such that the resistance of the circuit is equal to R_1 . *Rauhala* discloses that the control current I_B when switch k is open is equal to a low value V_B/R_1 . Ex. 1004 at [0023].

227. The impedance (high or low), and the control current (low or high), based on the state of switch k is summarized in the table below.

Switch k	Impedance	Control Current I_B
Closed	Low	High ($V_B/R_1 + V_B/R_2$)
Open	High	Low (V_B/R_1)

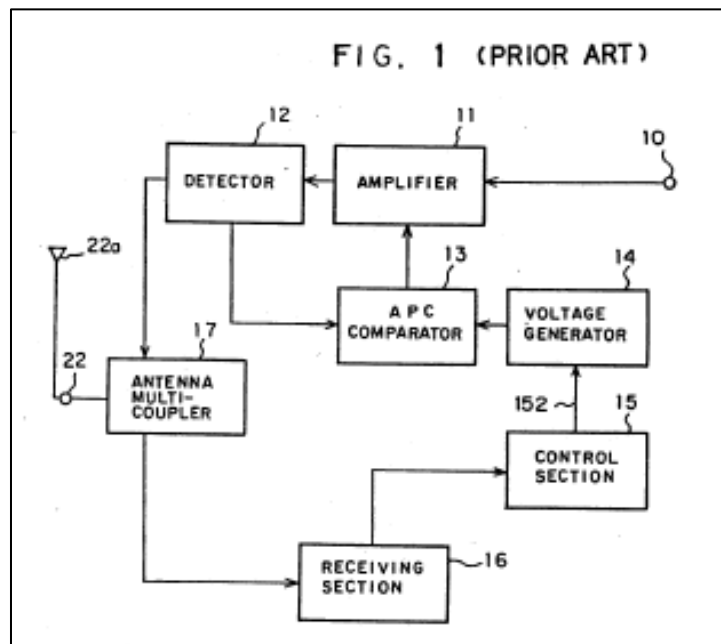
**XIII. RAUHALA IN COMBINATION WITH MEADOR AND FURUNO
DISCLOSES OR SUGGESTS ALL FEATURES OF CLAIM 30 OF
THE '330 PATENT**

1. Claim 30

**a. Claim 30[i]. “The wireless transceiver of claim 29
further comprising a transmitter comprising:”**

228. *Rauhala* states that its techniques are “appli[cable] in the reception circuits of mobile stations,” such as mobile phones, which are transceivers that would include a transmitter. Ex. 1004 at [0001], [0012].

229. *Furuno* discloses a transmitting output control section for an automobile telephone set of a conventional type. In Figure 1 (reproduced below), 10 is a transmitting signal input terminal at which a transmitting signal is to be received and 11 is an amplifier for amplifying the transmitting signal. Ex. 1007 at 1:16-35.



230. It is my opinion that *Furuno* is in the same technical field as *Rauhala*, *Meador*, and the '330 patent, because each of these references relates to wireless transceivers. *See supra* Sections (VII), (IX)(1), and (IX)(3) It is my opinion that a person of ordinary skill would have recognized the similarities between *Furuno* and the *Rauhala* device, and have been motivated to combine them to make a typical transmitter device, and doing so by using well-known transmitter components as explicitly disclosed in *Furuno*.

231. It is my opinion that a person of ordinary skill would have had a reasonable expectation of success in combining the disclosures of *Rauhala* and *Furuno* at least because both combinations would have used known technologies (for example, the well-known wireless transceiver of *Rauhala*) according to known methods (for example the well-known transmitter components as in *Furuno*) to yield predictable results.

232. Moreover, it is my opinion that modification of *Rauhala* with the teachings of *Furuno* would have amounted to nothing more than the use of a known technique to improve a similar device, and the results of the modification would have been predictable. This is because at the time of the invention, it is my opinion that a person of ordinary skill would have had the requisite skill level to readily modify the device disclosed by *Rauhala* to implement the teachings of *Furuno*. Moreover, it is my opinion that such modifications of *Rauhala* would have been

routine for the person of ordinary skill as they use well-known elements with no change in their respective functions.

b. Claim 30[ii]. “a power amplifier”

233. *Furuno* discloses that element 11 from FIG. 1 (reproduced above) is an amplifier for amplifying the transmitting signal. Ex. 1007 at 1:16-35.

c. Claim 30[iii]. “an output-level-sensing circuit coupled to an output of the power amplifier wherein the output-level-sensing circuit is configured to dynamically adjust a gain of the power amplifier”

234. *Furuno* teaches that element 12 is a detector which detects the level of an output signal of the amplifier 11. Ex. 1007 at 1:16-35. *Furuno* teaches element 13 is an automatic power control comparator (hereinafter referred to as APC comparator) which constitutes a transmitting power control means in which a DC voltage output by the detector 12 and an output of a voltage generator 14. *Id.* The APC comparator 13 compares the DC voltage and the specified voltage and adjusts the amplification factor (gain) of the amplifier 11 so that both voltages are in balance. *Id.* *Furuno* discloses that a comparator for automatic gain control is one that “controls the amplification factor of [an] amplifier to make [a] DC voltage output of [a] detector equal to [a] reference voltage. Ex. 1007 at 8:65-68. It is my opinion that a person of ordinary skill in the art would have understood that detector 12 and APC comparator 13 of *Furuno* are an “output-level-sensing circuit

coupled to an output of the power amplifier” that is “configured to dynamically adjust a gain of the power amplifier,” because detector 12 “detects an amplified transmitting signal level.” *Furuno* explicitly states that its disclosed comparator, e.g., APC comparator 13, is carrying out automatic gain control, and *Furuno* states this explicitly. See Ex. 1007 at 7:65-68 (**emphasis added**) (“a comparator for **automatic gain control** which controls the amplification factor of said amplifier to make said DC voltage output of said detector equal to said reference voltage”). Automatic gain control is a dynamic adjustment of the gain of the power amplifier because it changes based on the level detected by detector 12. Automatic gain control is defined as:

A means of controlling gain of a receiver through feedback to suit the strength of the incoming signal. Ideally, the output level at the speaker should remain constant over a wide range of input signals. For low-level inputs the feedback signal is small and gain is high. For stronger signals the feedback loop cuts gain to prevent overload.

Ex. 1011 at 6.

235. Therefore, it is my opinion that a person of ordinary skill in the art would have understood that automatic gain control is a dynamic adjustment of gain, since it is a feedback mechanism for controlling gain **based on** the strength of the incoming signal. Ex. 1011 at 6 (emphasis added).

**XIV. CUMMINS IN COMBINATION WITH RAUHALA AND SAITO
DISCLOSES OR SUGGESTS ALL FEATURES OF CLAIMS 1 AND
23 OF THE '330 PATENT**

1. Claims 1 and 23

236. As discussed herein previously, *Cummins* in combination with *Rauhala* teaches each element of claims 1 and 23. Additionally, it is my opinion that it would have been obvious to modify the threshold-based current controls of *Rauhala* to continuously adjust the supply currents using a continuous feedback system, as described by *Saito*.

237. *Saito* discloses automatic gain control circuitry for use in receivers of mobile devices. Ex. 1008 at 1:34-40. *Saito* states that the automatic gain control circuitry is aimed at “reducing reception disturbance resulting from intermodulation distortion for input levels of a broad range from the reception of a small input signal to the reception of a large input signal in receivers.” Ex. 1008 at 1:34-40. *Saito* explains that the automatic gain control circuitry includes “reception field level detection means” which “outputs a gain control signal in accordance with the reception field level.” *Id.* at 1:41-47. A person of ordinary skill would have understood “the reception field level” referred to by *Saito* to be analogous to signal strength. *Saito* further explains that the gain of radio frequency gain control units is controlled by “an automatic gain control unit comprising one or a plurality of continuous feedback systems.” Ex. 1008 at 1:47-53.

238. In an embodiment, *Saito* teaches that a continuous feedback system is added to the gain control means such that gain control signal output from a reception field detector is continuously varied. Ex. 1008 at 6:17-27. *Saito* explains that the continuous feedback allows the receiver to maintain the signal strength of the input signal to the processing circuit at a constant level, which could not be accomplished using staged gain control alone. Ex. 1008 at 6:20-27. *Saito* contends that such gain control “eliminat[es] the intermodulation distortion in a wide range of reception field levels ranging from the input of the very fine signal to the input of the large signal.” Ex. 1008 at 7:51-62.

239. It is my opinion that it was well known in the art that “continuous feedback” controllers, such as the one disclosed in *Saito* operate using “proportional control,” and do not use thresholds, as set forth below.

240. The *Kestenbaum* article evaluates the “design of PID [proportional-integral-derivative] controllers.” Ex. 1016 at 1. Specifically, the *Kestenbaum* article relates to a “simple continuous feedback controller, as discussed in the optimal control literature,” citing four articles dated between 1942 and 1964. *Id.* *Kestenbaum* then sets out six goals of process control, as they relate to the simple continuous feedback controller:

- 1) Ability to maintain the controlled variable at a given set-point
- 2) Set-point changes should be fast and smooth

- 3) Asymptotic stability and satisfactory performance for a wide range of frequencies
- 4) The controller should be designable with a minimum of information with respect to the nature of the input and the structure of the system
- 5) The controller should be insensitive to change in system parameters
- 6) Excessive control actions should be avoided

Ex. 1016 at 1-3.

241. *Kestenbaum* selects the PID controller for further analysis since “a large literature on PID controller design exists although for many processes simpler PI, or even **proportional controllers**, would often be quite adequate.” Ex. 1016 at 3 (emphasis added). *Kestenbaum* thus equates PID (proportional-integral-derivative) controllers, PI (proportional-integral), and proportional controllers, with the simple “continuous feedback” controllers previously referred to in the *Kestenbaum* article. See also Ex. 1016 at 11-12 (emphasis added) (“The discussion in this paper has centered till now on a very simple problem: **continuous controllers** for over-dampened simple in-out-single out-put systems”); and Ex. 1016 at 12 (emphasis added) (“[i]t should be pointed out that the foregoing discussion dealt mainly with **continuous controllers**”).

242. The *Qian* dissertation is another example of using continuous feedback or proportional controllers, and specifically in power control of wireless systems. See

Ex. 1017 at 6 (emphasis added) (“An optimal distributed closed-loop SIR-based power control scheme is proposed to minimize the squared SIR error. The power change is **proportional** to the SIR error. The optimal **proportional** gain is chosen to achieve the minimum SIR error at the next time instant”); Ex. 1017 at 7 (“A proportional derivative controller is added to the proposed power control scheme in order to reduce the overshoot and improve the transient response”); Ex. 1017 at 25 (“The amount of power change is proportional to the error, and the gain is chosen to achieve the minimum SIR error at the next time instant”).

243. The *Saye* patent provides explicit correspondence for the terms “continuous feedback” and “proportional control.” In particular, in describing a self steering system, *Saye* states that “the system effects **proportional control, i.e., there is continuous feedback** to the device so that the course correction is proportional to the deviation or error.” Ex. 1018 at 1:26-29.

244. Therefore, it is my opinion that a person of ordinary skill would understand that the “continuous feedback” control of *Saito* refers to proportional control.

245. Proportional control is “[a] control system in which corrective action is always proportionate to any variation of the controlled process from its desired value. For example, instead of snapping directly open-closed in the manner of two-position control, a proportional valve will be always positioned at some point between open and closed, depending on the flow requirement of the system at any

given moment.” Ex. 1011 at 11. Proportional controllers do not rely on thresholds because their “corrective action is always proportionate to any variation of the controlled process from its desired value.” Ex. 1011 at 11.

246. It is my opinion that the “continuous feedback” of *Saito* refers to “proportional control” and thus does not rely on the use of thresholds, but would instead take corrective action proportionate to the variation of the controlled process from its desired value.

247. *Cummins*, *Rauhala*, and *Saito* are analogous art as they all relate to wireless receivers.

248. In view of *Saito*, it would have been obvious to a person of ordinary skill to modify *Cummins* in view of *Rauhala* with the teachings of *Saito* to apply a continuous feedback mechanism for continuous adjustment of the supply currents. Indeed, a person of ordinary skill would have been motivated to make such a modification of *Cummins* in view of *Rauhala* at least to maintain a constant quality of a received signal and avoid abrupt changes in quality caused by changing circuit parameters near thresholds.

249. Moreover, modification of *Cummins* in view of *Rauhala* with the teachings of *Saito* would have amounted to nothing more than the use of a known technique to improve a similar device, and the results of the modification would have been predictable. This is because at the time of the invention, a person of ordinary skill

would have had the requisite skill level to readily modify the device disclosed by *Cummins* in view of *Rauhala* to implement the teachings of *Saito*. Moreover, such modifications of *Cummins* in view of *Rauhala* would have been routine for the person of ordinary skill as they use well-known elements with no change in their respective functions.

**XV. RAUHALA IN COMBINATION WITH MEADOR AND SAITO
DISCLOSES OR SUGGESTS ALL FEATURES OF CLAIM 29 OF
THE '330 PATENT**

1. Claim 29

250. As discussed herein previously, *Rauhala* in combination with *Meador* teaches each element of claim 29. Additionally, it is my opinion that it would have been obvious to modify the threshold-based current controls of *Rauhala* to continuously adjust the supply currents using a continuous feedback system, as described by *Saito*.

251. *Saito* discloses automatic gain control circuitry for use in receivers of mobile devices. Ex. 1008 at 1:34-40. *Saito* states that the automatic gain control circuitry is aimed at “reducing reception disturbance resulting from intermodulation distortion for input levels of a broad range from the reception of a small input signal to the reception of a large input signal in receivers.” Ex. 1008 at 1:34-40. *Saito* explains that the automatic gain control circuitry includes “reception field level detection means” which “outputs a gain control signal in accordance with the

reception field level.” *Id.* at 1:41-47. A person of ordinary skill would have understood “the reception field level” referred to by *Saito* to be analogous to signal strength. *Saito* further explains that the gain of radio frequency gain control units is controlled by “an automatic gain control unit comprising one or a plurality of continuous feedback systems.” Ex. 1008 at 1:47-53.

252. In an embodiment, *Saito* teaches that a continuous feedback system is added to the gain control means such that gain control signal output from a reception field detector is continuously varied. Ex. 1008 at 6:17-27. *Saito* explains that the continuous feedback allows the receiver to maintain the signal strength of the input signal to the processing circuit at a constant level, which could not be accomplished using staged gain control alone. Ex. 1008 at 6:20-27. *Saito* contends that such gain control “eliminat[es] the intermodulation distortion in a wide range of reception field levels ranging from the input of the very fine signal to the input of the large signal.” Ex. 1008 at 7:51-62.

253. It is my opinion that it was well known in the art that “continuous feedback” controllers, such as the one disclosed in *Saito* operate using “proportional control,” and do not use thresholds, as set forth below.

254. The *Kestenbaum* article evaluates the “design of PID [proportional-integral-derivative] controllers.” Ex. 1016 at 1. Specifically, the *Kestenbaum* article relates to a “simple continuous feedback controller, as discussed in the optimal control

literature,” citing four articles dated between 1942 and 1964. *Id.* *Kestenbaum* then sets out six goals of process control, as they relate to the simple continuous feedback controller:

- 1) Ability to maintain the controlled variable at a given set-point
- 2) Set-point changes should be fast and smooth
- 3) Asymptotic stability and satisfactory performance for a wide range of frequencies
- 4) The controller should be designable with a minimum of information with respect to the nature of the input and the structure of the system
- 5) The controller should be insensitive to change in system parameters
- 6) Excessive control actions should be avoided

Ex. 1016 at 1-3.

255. *Kestenbaum* selects the PID controller for further analysis since “a large literature on PID controller design exists although for many processes simpler PI, or even **proportional controllers**, would often be quite adequate.” Ex. 1016 at 3 (emphasis added). *Kestenbaum* thus equates PID (proportional-integral-derivative) controllers, PI (proportional-integral), and proportional controllers, with the simple “continuous feedback” controllers previously referred to in the *Kestenbaum* article. See also Ex. 1016 at 11-12 (emphasis added) (“The discussion in this paper has centered till now on a very simple problem: **continuous controllers** for over-

dampened simple in-out-single out-put systems”); and Ex. 1016 at 12 (emphasis added) (“[i]t should be pointed out that the foregoing discussion dealt mainly with **continuous controllers**”).

256. The *Qian* dissertation is another example of using continuous feedback or proportional controllers, and specifically in power control of wireless systems. See Ex. 1017 at 6 (emphasis added) (“An optimal distributed closed-loop SIR-based power control scheme is proposed to minimize the squared SIR error. The power change is **proportional** to the SIR error. The optimal **proportional** gain is chosen to achieve the minimum SIR error at the next time instant”); Ex. 1017 at 7 (“A proportional derivative controller is added to the proposed power control scheme in order to reduce the overshoot and improve the transient response”); Ex. 1017 at 25 (“The amount of power change is proportional to the error, and the gain is chosen to achieve the minimum SIR error at the next time instant”).

257. The *Saye* patent provides explicit correspondence for the terms “continuous feedback” and “proportional control.” In particular, in describing a self steering system, *Saye* states that “the system effects **proportional control, i.e., there is continuous feedback** to the device so that the course correction is proportional to the deviation or error.” Ex. 1018 at 1:26-29.

258. Therefore, it is my opinion that a person of ordinary skill would understand that the “continuous feedback” control of *Saito* refers to proportional control.

259. Proportional control is “[a] control system in which corrective action is always proportionate to any variation of the controlled process from its desired value. For example, instead of snapping directly open-closed in the manner of two-position control, a proportional valve will be always positioned at some point between open and closed, depending on the flow requirement of the system at any given moment.” Ex. 1011 at 11. Proportional controllers do not rely on thresholds because their “corrective action is always proportionate to any variation of the controlled process from its desired value.” Ex. 1011 at 11.

260. It is my opinion that the “continuous feedback” of *Saito* refers to “proportional control” and thus does not rely on the use of thresholds, but would instead take corrective action proportionate to the variation of the controlled process from its desired value.

261. *Rauhala*, *Meador*, and *Saito* are analogous art as they all relate to wireless receivers.

262. In view of *Saito*, it would have been obvious to a person of ordinary skill to modify *Rauhala* in combination with *Meador* with the teachings of *Saito* to apply a continuous feedback mechanism for continuous adjustment of the supply currents. Indeed, a person of ordinary skill would have been motivated to make such a modification of *Rauhala* at least to maintain a constant quality of a received signal and avoid abrupt changes in quality caused by changing circuit parameters near

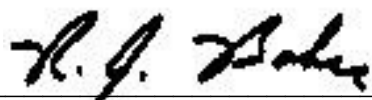
thresholds. Moreover, modification of *Rauhala* with the teachings of *Saito* would have amounted to nothing more than the use of a known technique to improve a similar device, and the results of the modification would have been predictable. This is because at the time of the invention, a person of ordinary skill would have had the requisite skill level to readily modify the device disclosed by *Rauhala* to implement the teachings of *Saito*. Moreover, such modifications of *Rauhala* would have been routine for the person of ordinary skill as they use well-known elements with no change in their respective functions.

XVI. CONCLUSIONS

263. In summary, it is my opinion that the references discussed in this Declaration disclose or suggest all of the features recited in claims 1, 23, 29, and 30 of the '330 patent.

264. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: March 7, 2023

By: 
R. Jacob Baker, P.E., Ph.D.

Appendix A

R. JACOB (JAKE) BAKER, PH.D., P.E.

*Professor Pristinus of Electrical and Computer Engineering
Independent Consultant*

6775 Agave Azul Court
Las Vegas, NV 89120

(208) 850-0517 (Cell)

Email: rjacobbaker@gmail.com

Website: <http://CMOSedu.com/jbaker/jbaker.htm>

PROFESSIONAL SUMMARY

Russel Jacob (Jake) Baker, Ph.D., P.E. (IEEE Student Member 1983, Member 1988, Senior Member 1997, and Fellow 2013) was born in Ogden, Utah, on October 5, 1964. He received the B.S. and M.S. degrees in electrical engineering from the University of Nevada, Las Vegas, in 1986 and 1988. He received the Ph.D. degree in electrical engineering from the University of Nevada, Reno in 1993. His Google Scholar profile is [here](#) and his ResearchGate profile is [here](#).

From 1981 to 1987 he served in the United States Marine Corps (from September of 1982 in the Reserves, Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division). From 1985 to 1993 he worked for E. G. & G. Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapons tests at the Nevada Test Site. During this time, he designed, and oversaw the fabrication and manufacture of, over 30 electronic and electro-optic instruments including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame- and bit-syncs, data converters, streak-camera sweep circuits, Pockels cell drivers, micro-channel plate gating circuits, and analog oscilloscope electronics. From 1991-1992 he was an adjunct faculty member in the department of electrical engineering at the University of Nevada, Las Vegas (UNLV). From 1993 to 2000 he served on the faculty in the department of electrical engineering at the University of Idaho (UI), first as an untenured Assistant Professor and then from 1998 as a tenured Associate Professor. In 2000 he joined a new electrical and computer engineering (ECE) program at Boise State University (BSU) where he was promoted to Full Professor in 2002. He then served as the ECE department chair at BSU from 2004 to 2007. At BSU he helped establish graduate programs in ECE including, in 2006, the university's second PhD degree. In 2012 he re-joined the faculty at UNLV as a tenured Full Professor of ECE. During his service at the UI, BSU, and UNLV he has been the major professor to more than [100 graduate students](#). In addition to this industry and academic experience, he has done consulting, both technical and expert witness, for over [200 companies](#).

Over the last 35+ years his [research/development interests](#) and [publications](#) have been, or currently are, focused on: analog-to-digital/digital-to-analog data conversion and transmission, optoelectronics (imagers, displays, LIDARs, APDs, SiPMs, and associated electronics), analog and digital integrated circuit design and fabrication, design of diagnostic electrical and electro-optic instrumentation for scientific research, integrated electrical/biological circuits and systems, array (memory, imagers, and displays) fabrication and design, CAD tool development and online tutorials, low-power interconnect and packaging (electrical and optical) techniques, design of wired/wireless communication and interface circuits, circuit design for the use and storage of renewable energy, power electronics and power supply design, and the delivery of [online engineering education](#).

Dr. Baker is the named inventor on over [150 US patents](#). He is a member of the honor societies Eta Kappa Nu and Tau Beta Pi, a licensed Professional Engineer, a popular lecturer that has delivered over [50 invited talks](#) around the world, an IEEE Fellow, and the author of the books CMOS Circuit Design, Layout, and Simulation, CMOS Mixed-Signal Circuit Design, and a coauthor of DRAM Circuit Design: Fundamental and High-Speed Topics. He received the 2000 Best Paper Award from the IEEE Power Electronics Society, the 2007 Frederick Emmons Terman Award,

the 2011 IEEE Circuits and Systems Education Award and the 2021 Wiley-IEEE Press Textbook Award for the 4th Edition of his book CMOS Circuit Design, Layout, and Simulation.

His service activities include the IEEE Press Editorial Board (1999-2004), editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018), the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015), the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), Distinguished Lecturer for the SSCS (2012-2015), Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for the IEEE Solid-State Circuits Magazine, IEEE Kirchhoff Award Committee (2020-2023), and advisor for the student branch of the IEEE at UNLV (2013-2023).

INDUSTRY EXPERIENCE

2008 - present: Expert witness in intellectual property disputes in electrical, electro-optic, and computer engineering matters for: 1) district court and ITC patent disputes, 2) inter partes reviews at the PTAB, and 3) arbitrations and mediations.

2013 - 2022: Worked with Freedom Photonics, Santa Barbara, CA, on the integration, fabrication and design, of optoelectronics with CMOS integrated circuits. Work includes the design of compact optical transceivers for range finding applications, high-efficiency integrated silicon avalanche photodetectors for quantum key receivers, Geiger mode SiGe receivers for long-range communications, cryptography, and the fabrication of near-infrared focal plane arrays. Packaging and testing of numerous chips fabricated in both CMOS and SiGe technologies using LEDs, ILDs, PIN, APDs, and ROICs.

2017 - 2019: Worked with Vorpil Research Systems, Las Vegas, NV on the design of integrated circuit electronics and optoelectronics for optical transceivers used in LIDARs/LADARs.

2016 - 2019: Worked with Attollo Engineering on the design of transient digitizers for the capture of high-speed signals for range finders using LEDs and lasers in compact optical transceivers.

2013 - 2018: Working with Mission Support and Test Services, LLC (MSTS, formerly National Security Technologies, LLC, [NSTec]) on the Design and Fabrication of Integrated electrical/photonics application specific integrated circuit (ASIC) design for use in the implementation of diagnostic instrumentation.

2013 - 2015: Consultant for OmniVision. Working on integrating CMOS image sensors (CIS) with memory for very high-speed consumer imager products. Design specialty DRAM, high-speed interfaces between CIS and DRAM, packaging techniques to pair the CIS with DRAM.

2010 - 2013: Worked with Arete' Associates on the design of high-speed compressive transimpedance amplifiers for LADAR projects and the design of ROIC unit cells. Work funded by the U. S. Air Force.

2013: Cirque, Inc. Consulting on the design of analog-to-digital interfaces for capacitive touch displays and pads.

2012: Consultant at Lockheed-Martin Santa Barbara Focal Plane Array. CMOS circuit design and fabrication for the development and manufacture of infrared components and imaging systems with an emphasis on highest sensitivity Indium Antimonide (InSb) focal plane arrays (FPAs) in linear through large staring formats. Product groups include FPAs, integrated dewar assemblies (IDCAs), camera heads, high-speed interfaces between image processors and imaging systems, and infrared imaging systems.

2010 - 2012: Working with Aerius Photonics (and then FLIR Inc. when Aerius was purchase by FLIR) on the design of Focal Plane Arrays funded (SBIRs and STTRs) by the U.S. Air Force, Navy, and Army. Experience with readout integrated circuits (ROICs) and the design/layout of photodetectors in standard CMOS.

2009 - 2010: Sun Microsystems, Inc. (and then Oracle) VLSI research group. Provided consulting on memory circuit design/fabrication and proximity connection (PxC) interfaces to DRAMs and SRAMs for lower power, 3D packaging, for memory modules and controllers implemented with FPGAs and custom ASICs.

2009 - 2010: Contour Semiconductor, Inc. Design of NMOS voltage and current references as well as the design of a charge pump for an NMOS memory chip.

1994 - 2008: Affiliate faculty (Senior Designer), Micron Technology. Designed CMOS circuits for DRAMs including DLLs, PLLs for embedded graphics chips, voltage references and regulators, data converters, field-emitting display drivers, sensing for MRAM (using delta-sigma data conversion topologies), SRAMs, RFIDs, CMOS active pixel imagers and sensors, power supply design (linear and switching), input buffers, etc. Worked on a joint research

project between Micron and HP labs in magnetic memory fabrication and design using the MTJ memory cell. Worked on numerous technologies ranging from LED lighting to medical imaging using CMOS image sensors (too many to list) resulting in numerous US patents (see following list). Considerable experience working with product engineering to ensure high-yield from the production line from fabrication to test. Co-authored a book on DRAM circuit design through the support of Micron. Gained knowledge in the entire memory design process from fabrication to packaging. Developed, designed, and tested circuit design techniques for multi-level cell (MLC) Flash memory using signal processing.

January 2008: Consultant for Nascentric located in Austin, TX. Provide directions on circuit operation (DRAM, memory, and mixed-signal) for fast SPICE circuit simulations.

May 1997 - May 1999: Consultant for Tower Semiconductor, Haifa, Israel. Designed CMOS integrated circuit cells for various modem chips, interfaces, and serial buses including USB circuits, charging circuits based upon power up/down circuits using an MOS or bandgap reference, pre-amplifiers, comparators, etc.

Summer 1998: Consultant for Amkor Wafer Fabrication Services, Micron Technology, and Rendition, Inc., Design PLLs and DLLs for custom ASICs and a graphics controller chip.

Summers 1994 - 1995: Micron Display Inc. Designing phase locked loop for generating a pixel clock for field emitting displays and a NTSC to RGB circuit on chip in NMOS. These displays are miniature color displays for camcorder and wrist watch size color television. Worked on the fabrication and design of video peripheral circuits for these displays.

September - October 1993: Lawrence Berkeley Laboratory. Designed and constructed a 40 A, 2 kV power MOSFET pulse generator with a 3 ns rise-time and 8 ns fall-time for driving Helmholtz coils.

Summer 1993: Lawrence Livermore National Laboratory, Nova Laser Program. Researched picosecond instrumentation, including time-domain design for impulse radar and imaging.

December 1985 - June 1993: (from July 1992 to June 1993 employed as a consultant while finishing up my Ph.D.), E.G.&G. Energy Measurements Inc., Nevada, Senior Electronics Design Engineer. Responsible for the design and manufacturing of instrumentation used in support of Lawrence Livermore National Laboratory's Nuclear Test Program. Responsible for designing and fabricating over 30 electronic and electro-optic instruments including: CCD camera design, communication networks, fiber optic transmitters employing high speed laser drive electronics, receivers employing envelop tracking for DC voltage restoration and regeneration of received information, receiver low noise amplifier design, frame synchronizers for re-assembling transmitted images, high-speed SRAM memory system design with battery back-up, calibration equipment design such as a tunnel diode pulse generator for testing compensation of oscilloscopes and DAC design for calibrating CCD readout electronics, power supply and battery charger designs, sweep circuits for streak cameras, Pockel's cell drive electronics, vertical amplifier design using HBTs for analog oscilloscopes used at the Nevada Test Site, and 10 kV ramp designs using a planar triode to name some of the designs.

This position provided considerable fundamental grounding in EE with a broad exposure ranging from the design of PC boards to, for example, the design of cable equalizers. Summarizing, gained experience in circuit design technologies including: bipolar, vacuum tubes (planar triodes for high voltages), hybrid integrated circuit fabrication and design, GaAs (high speed logic and HBTs), Mach-Zehnder interferometers, Pockels cells, krytrons, power MOSFETs, microwave techniques, power supplies, fiber optic transmitters/receivers, etc.

Summer 1985: Reynolds Electrical Engineering Company, Las Vegas, Nevada. Gained hands on experience in primary and secondary power system design, installation and trouble-shooting electric motors on mining equipment.

ACADEMIC EXPERIENCE

January 1991 – present: Professor of Electrical and Computer Engineering at the **University of Nevada, Las Vegas** from August 2012 to present. From January 2000 to July 2012 held various positions at **Boise State University** including: Professor (2003 – 2012), Department Chair (2004 - 2007), and tenured Associate Professor (2000 - 2003). From August 1993 to January 2000 was a tenured/tenure track faculty member at the **University of Idaho:** Assistant Professor (1993 - 1998) and then tenured Associate Professor (1998 - 2000). Lastly, from January 1991 to May 1993 held adjunct faculty positions in the departments of Electrical Engineering at the University of Nevada, Las Vegas and Reno. Additional details:

- Research is focused on analog and mixed-signal integrated circuit fabrication and design. Worked with multi-disciplinary teams (civil engineering, biology, materials science, etc.) on projects that have been funded by EPA, DARPA, NASA, Army, DMEA, Navy, and the AFRL.
- Current and past research and development interests are:
 - Design and packaging of electrical/optical systems (e.g., LiDARs/LADARs) using LEDs, semiconductor lasers, lens for focusing and directing light, integrated circuits, and associated control and communication systems/circuits.
 - Capacitive sensing techniques using delta-sigma modulation and interfacing to sensors
 - Design of high-voltage and energy switching circuits
 - Circuit design and fabrication for the control, use, and storage of renewable energy using thermoelectric generators
 - Design of electrical/biological/optical circuits and systems using electrowetting on dielectric for automating and controlling biological experiments
 - Design of readout integrated circuits (ROICs) for use with focal plane arrays (FPAs)
 - Heterogeneous integration of III-V photonic devices (e.g., FPAs and VCSELs) with CMOS
 - Methods (e.g., 3D packaging and capacitive interconnects) to reduce power consumption in semiconductor memories, memory modules, and digital systems using custom and non-custom (e.g., FPGAs) implementations
 - Analog and mixed-signal circuit fabrication and design for communication systems, synchronization, energy storage, data conversion, and interfaces
 - The design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g., magnetic, chalcogenide)
 - Reconfigurable electronics design and fabrication using nascent memory technologies such as the memristor to implement FPGAs
 - Finding an electronic, that is, no mechanical component, replacement for the hard disk drive using nascent fabrication technologies
 - Power electronics circuit design for consumers and consumer electronics including power management and adaptive control to reduce power consumption
 - Design of bandpass delta-sigma modulators for IQ demodulation in wireless communication systems in OFDM, WiFi, 802.11, Bluetooth, 3G, 4G, etc.
 - University prototyping, fabricating, and packaging of integrated circuits
- Led, as chair, the department in graduate curriculum (MS and PhD), program development, and ABET accreditation visits.
- Worked with established and start-up companies to provide technical expertise and identify employment opportunities for students.
- Held various leadership and service positions including: ECE chair, graduate coordinator, college curriculum committee (chair), promotion and tenure committee, scholarly activities committee, faculty search committee, university level search committees, etc. Collaborate with College of Engineering faculty on joint research projects.
- Taught courses in circuits, analog IC design, digital VLSI design and fabrication, fiber optics, and mixed-signal integrated circuit design to both on- and, via the Internet, off-campus students. Research emphasis in integrated circuit design using nascent technologies.

EDUCATION

- Ph.D. in Electrical Engineering; December 1993; University of Nevada, Reno, GPA 4.0/4.0. Dissertation Title: *Applying power MOSFETs to the design of electronic and electro-optic instrumentation.*
- M.S. and B.S. in Electrical Engineering; May 1986 and May 1988; University of Nevada, Las Vegas. Thesis Title: *Three-dimensional simulation of a MOSFET including the effects of gate oxide charge.*

MEMBERSHIPS IN PROFESSIONAL AND SCHOLARLY ORGANIZATIONS

IEEE (student, 1983; member, 1988; senior member, 1997; Fellow, 2013)
Member of the honor societies Eta Kappa Nu and Tau Beta Pi
Licensed Professional Engineer

HONORS AND AWARDS

- Consolidated Students of the University of Nevada, Las Vegas (CSUN) Faculty Award, 2017
- Tau Beta Pi UNLV Outstanding Professor of the Year in 2013, 2014, 2015 and 2016
- UNLV ECE Department Distinguished Professor of the Year in 2015
- IEEE Fellow for contributions to the design of memory circuits - 2013
- Distinguished Lecturer for the IEEE Solid-State Circuits Society, 2012 - 2015
- IEEE Circuits and Systems (CAS) Education Award - 2011
- Twice elected to the Administrative Committee of the Solid-State Circuits Society, 2011 - 2016
- Frederick Emmons Terman Award from the American Society of Engineering Education - 2007
- President's Research and Scholarship Award, Boise State University - 2005
- Honored Faculty Member - Boise State University Top Ten Scholar/Alumni Association 2003
- Outstanding Department of Electrical Engineering faculty, Boise State 2001
- Recipient of the IEEE Power Electronics Society's Best Paper Award in 2000
- University of Idaho, Department of Electrical Engineering outstanding researcher award, 1998-99
- University of Idaho, College of Engineering Outstanding Young Faculty award, 1996-97

SERVICE

Reviewer for IEEE transactions on solid-state circuits, circuits and devices magazine, education, instrumentation, nanotechnology, VLSI, etc. Reviewer for several American Institute of Physics journals as well (Review of Scientific Instruments, Applied Physics letters, etc.) Board member of the IEEE press (reviewed dozens of books and book proposals). Reviewer for the National Institutes of Health. Technology editor and then Editor-in-Chief for the Solid-State Circuits Magazine.

Led the Department on ABET visits, curriculum and policy development, and new program development including the PhD in electrical and computer engineering. Provided significant University and College service in infrastructure development, Dean searches, VP searches, and growth of academic programs. Provided university/industry interactions including starting the ECE department's advisory board. Held positions as the ECE department Master's graduate coordinator and coordinator for the Sophomore Outcomes Assessment Test (SOAT).

Also currently serves, or has served, on the IEEE Press Editorial Board (1999-2004), as a member of the first Academic Committee of the State Key Laboratory of Analog and Mixed-Signal VLSI at the University of Macau, as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018), on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), as an Advisory Professor to the School of Electronic and Information Engineering at Beijing Jiaotong University, as a Distinguished Lecturer for the SSCS (2012-2015), as the Technical Program Chair for the IEEE 58th 2015 International Midwest Symposium on Circuits and Systems, MWSCAS 2015, as advisor for the student branch of the IEEE at UNLV (2013-2023), and as the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for the *IEEE Solid-State Circuits Magazine*, and IEEE Kirchhoff Award Committee (2020-2023).

ARMED FORCES

From 1981 to 1987 served in the United States Marine Corps (from September of 1982 in the Reserves, Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division), Honorable Discharge. Military Occupational Specialty (MOS) was Machine Gunner (MOS 0331)

TEXTBOOKS AUTHORED

Baker, R. J., "CMOS Circuit Design, Layout and Simulation, Fourth Edition" *Wiley-IEEE Press*, 1234 pages. ISBN 9781119481515 (2019) **Over 50,000 copies of this book in print.** (Third Edition published in 2010, Revised Second Edition published in 2008, and Second Edition Published in 2005)

Baker, R. J., "CMOS Mixed-Signal Circuit Design," *Wiley-IEEE*, 329 pages. ISBN 978-0470290262 (second edition, 2009) and ISBN 9780471227540 (First Edition published in 2002)

Keeth, B., Baker, R. J., Johnson, B., and Lin, F., "DRAM Circuit Design: Fundamental and High-Speed Topics", *Wiley-IEEE*, 2008, 201 pages. ISBN: 9780470184752

Keeth, B. and Baker, R. J., "DRAM Circuit Design: A Tutorial", *Wiley-IEEE*, 2001, 201 pages. ISBN 0780360141

Baker, R. J., Li, H.W., and Boyce, D.E. "CMOS Circuit Design, Layout and Simulation," *Wiley-IEEE*, 1998, 904 pages. ISBN 9780780334168

BOOKS, OTHER (edited, chapters, etc.)

Saxena, V. and Baker, R. J., "Analog and Digital VLSI," chapter in the CRC Handbook on Industrial Electronics, edited by J. D. Irwin and B. D. Wilamowski, *CRC Press*, 2009 second edition.

Baker, R. J., "CMOS Analog Circuit Design," (A self-study course with study guide, videos, and tests.) IEEE Education Activity Department, 2000. ISBN 0-7803-4822-2 (with textbook) and ISBN 0-7803-4823-0 (without textbook)

Baker, R. J., "CMOS Digital Circuit Design," (A self-study course with study guide, videos, and tests.) *IEEE Education Activity Department*, 2000. ISBN 0-7803-4812-5 (with textbook) and ISBN 0-7803-4813-3 (without textbook)

Li, H.W., Baker, R. J., and Thelen, D., "CMOS Amplifier Design," chapter 19 in the CRC VLSI Handbook, edited by Wai-kai Chen, *CRC Press*, 1999 (ISBN 0-8493-8593-8) and the second edition in 2007 (ISBN 978-0-8493-4199-1)

INVITED TALKS AND SEMINARS

Have given over 50 invited talks and seminars at the following locations: AMD (Fort Collins), AMI semiconductor, Arizona State University, Beijing Jiaotong University, Boise State University, Carleton University, Carnegie Mellon, Columbia University, Dublin City University (Ireland), E.G.&G. Energy Measurements, Foveon, the Franklin Institute, Georgia Tech, Gonzaga University, Hong Kong University of Science and Technology, ICSEng Keynote, ICySSS keynote, IEEE Computing and Communication Workshop (CCWC), IEEE Electron Devices Conference (NVMETS), IEEE Workshop on Microelectronics and Electron Devices (WMED), Indian Institute of Science (Bangalore, India), Instituto de Informatica (Brazil), Instituto Tecnológico y de Estudios Superiores de Monterrey (ITESM, Mexico), Iowa State University, Lawrence Livermore National Laboratory, Lehigh University, Lockheed-Martin, Micron Technology, Nascentric, National Semiconductor, Princeton University, Rendition, Saintgits College (Kerala, India), Southern Methodist University, Sun Microsystems, Stanford University, ST Microelectronics (Delhi, India), Temple University, Texas A&M University, Tower Semiconductor (Israel), University of Alabama (Tuscaloosa), University of Arkansas, University of Buenos Aires (Argentina), University of Houston, University of Idaho, University of Illinois (Urbana-Champaign), Université Laval (Québec City, Québec), University of Macau, University of Maryland, Université de Montréal (École Polytechnique de Montréal), Xilinx (Ireland), University of Nevada (Las Vegas), University of Nevada (Reno), University of Toronto, University of Utah, Utah State University, and Yonsei University (Seoul, South Korea).

RESEARCH FUNDING (LAST 5 YEARS AS A PROFESSOR)

Recent funding listed below. In-kind, equipment, and other non-contract/grant funding [e.g., MOSIS support, money for travel for invited talks, etc.] not listed.

- Baker, R. Jacob, (2017-2023) "Tiled Silicon Photomultiplier Array Read-Out Integrated Circuit," NASA, \$29,999 (Phase I), \$225,238 (Phase II), and \$79,697 (Phase IIE)
- Goldman, J., Menezes, J., and Baker, R. J., (2021-2022) "Monitored Compression Therapy: Using Smart Technology to Optimize the Treatment of Lower Extremity Swelling," UNLV Sports Research & Innovation Initiative. Proof of Concept Grant Program, \$50,000
- Baker, R. Jacob, (2019-2021) "Dual-Mode, Extended Near-Infrared, Focal Plane Arrays Fabricated with CMOS Compatible GeSiSn Alloy Materials," DARPA, \$149,998
- Baker, R. Jacob, (2018-2020) "Geiger Mode SiGe Receiver for Long-Range Optical Communications," NASA, \$99,996
- Baker, R. Jacob, (2019) "Improved Quantum Efficiency Photo-Detector," Navy, \$29,999

- Baker, R. Jacob, (2018-2019) "Tiled Silicon Photomultiplier Array Read-Out Integrated Circuit – Phase I," NASA, \$29,999
- Baker, R. Jacob, (2017-2019) "Quantum Cryptography Detector Chip," Defense MicroElectronics Activity (DMEA), \$266,029
- Baker, R. Jacob, (2017-2019) "Advanced Printed Circuit Board Design Methods for Compact Optical Transceiver," U.S. Army/DOD, \$299,605
- Baker, R. Jacob, (2016-2018) "High-Sensitivity Monolithic Silicon APD and ROIC," U.S. Air Force/DOD, \$299,665
- Baker, R. Jacob, (2017-2018) "Transimpedance Amplifier Integrated Circuit Collaboration," Department of Energy, National Security Technologies, LLC, \$100,436
- Baker, R. Jacob, (2017) "Geiger Mode SiGe Receiver for Long-Range Optical Communications," NASA, \$30,000
- Baker, R. Jacob, (2016-2017) "Testing and development of BiCMOS photodetectors and diagnostic instrumentation," Department of Energy, National Security Technologies, LLC, \$181,605
- Baker, R. Jacob, (2016-2017) "Dual-Mode, Extended Near Infrared, Focal Plane Arrays fabricated with a Commercial SiGe BiCMOS Process," DARPA, \$41,892

DOCTORAL STUDENT SUPERVISION

11. Mario Valles Montenegro (underway)
10. Sachin Namboodiri – A Multi-channel MCP-PMT based Readout Integrated Circuit for LiDAR Applications (2020)
9. Wenlan Wu – High-Speed Radhard Mega-Pixel CIS Camera for High-Energy Physics (2019)
8. Kostas Moutafis – A Highly-Sensitive Global-Shutter CMOS Image Sensor with On-Chip Memory for Hundreds of kilo-frames per second Scientific Experiments (2019)
7. Yiyan Li – Portable High Throughput Digital Microfluidics and On-Chip Bacteria Cultures (2016)
6. Yacouba Moumouni – Designing, Building, and Testing a Solar Thermoelectric Generation, STEG, for Energy Delivery to Remote Residential Areas in Developing Regions (2015)
5. Qawi IbnZayd Harvard – Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design (2011)
4. Vishal Saxena – K-Delta-1-Sigma Modulators for Wideband Analog-to-Digital Conversion (2010)
3. Robert Russell Hay – Digitally-Tunable Surface Acoustic Wave Resonator (2009)
2. Xiangli Li (the first Boise State University College of Engineering PhD graduate) – MOSFET Modulated Dual Conversion Gain CMOS Image Sensors (2008)
1. Feng Lin, Research and Design of Low Jitter, Wide Locking-Range Phase-Locked and Delay-Locked Loops (2000)

MASTERS STUDENT SUPERVISION

93. Abraham Lopez (underway)
92. David Santiago (underway)
91. Khulan Tsogt (underway)
90. Jazmin Bolor (underway)
89. Chris Barr (underway)
88. Minsung Cho – Studies of Forward Projection Algorithms and Implementation on PC and FPGA (2023)
87. Armani Alvarez – A Control Integrated Circuit for a Hysteretic Flyback Power Converter (2022)
86. Francisco Mata-carlos – A Wearable Electronic Monitoring Device for Low Pressure Garment Applications and Temperature Analysis for Prevention of Ulceration and Infection (2022)
85. Daniel Senda – Designs and Outcomes of Transcranial Magnetic Stimulation (TMS) and Repetitive Transcranial Magnetic Stimulation (rTMS) Circuits (2021)
84. James Skelly – Monitored Compression Therapy: Using Smart Technology to Optimize the Treatment of Lower Extremity Swelling (2021)
83. Gonzalo Arteaga – Current-mode photon-counting circuit with SiGe BiCMOS input stage (2020)
82. Jason Silic – Design and Fabrication of a 6-bit Current-Mode ADC for Lidar and High-Speed Applications (2020)
81. Brandon Wade (2020)
80. Mario Valles Montenegro – Front-End CMOS Transimpedance Amplifiers on a Silicon Photomultiplier Resistant to Fast Neutron Fluence (2020)
79. Jonathan DeBoy (2018)
78. Dane Gentry – Design, Layout, and Testing of SiGe APDs Fabricated in a BiCMOS Process (2018)

77. James Mellot – Variable Transition Time Inverters in a Digital Delay Line with Analog Storage for Processing Fast Signals and Pulses (2018)
76. Eric Monahan – High Speed Fast Transient Digitizer Design and Simulation (2018)
75. Shada Sharif – Design and Analysis of First and Second Order K-Delta-1-Sigma Modulators in Multiple Fabrication Processes (2018)
74. Vikas Vinayaka – Analysis and Design of Analog Front-End Circuitry for Avalanche Photodiodes (APD) and Silicon Photo-Multipliers (SiPM) in Time-of-Flight Applications (2018)
73. Claire Tsagkari – Design, Fabrication and Testing of a Capacitive Sensor Using Delta-Sigma Modulation (2017)
72. Kevin Buck – Fast Transient Digitizer and PCB Interface (2015)
71. Marzieh Sharbat Maleki (2015)
70. Angsuman Roy – Design, Fabrication and Testing of Monolithic Low-Power Passive Sigma-Delta Analog-to-Digital Converters (2015)
69. Daniel Anderson – Design and Implementation of an Instruction Set Architecture and Instruction Execution Unit for the RZ9 Coprocessor System (2014)
68. Jared Gordon – Design and Fabrication of an Infrared Optical Pyrometer ASIC (2013)
67. Justin Butterfield (2012)
66. Adam Johnson – Methods and Considerations for Testing Resistive Memories (2012)
65. Ben Millemon – CMOS Characterization, Modeling, and Circuit Design in the Presence of Random Local Variation (2012)
64. Justin Wood (2012)
63. Chamunda Ndinawe Chamunda (2011)
62. Gary VanAckern – Design Guide for CMOS Process On-Chip 3D Inductors using Thru-Wafer Vias (2011)
61. Lucien Jan Bissey – High-Voltage Programmable Delta-Sigma Modulation Voltage-Control Circuit (2010)
60. Kaijun Li (2010)
59. Yingting Li (co-supervised with Maria Mitkova) (2010)
58. Lael Matthews (co-supervised with Said Ahmed-Zaid) (2010)
57. Priyanka Mukeshbhai Parikh (2010)
56. Todd Plum (co-supervised with Jeff Jessing) – Design and Fabrication of a Chemicapacitive Sensor for the Detection of Volatile Organic Compounds (2010)
55. Rahul Srikonda (2010)
54. Avani Falgun Trivedi (2010)
53. Kuang Ming Yap – Gain and Offset Error Correction for CMOS Image Sensors using Delta-Sigma Modulation (2010)
52. Mahesh Balasubramanian – Phase Change Memory - Array Development and Sensing Circuits using Delta-Sigma Modulation (2009)
51. Lincoln Bollschweiler (2009)
50. Shantanu Gupta (2009)
49. Qawi Harvard – Wide I_O DRAM Architecture Utilizing Proximity Communication (2009)
48. Avinash Rajagiri (2009)
47. Ramya Ramarapu (2009)
46. Harikrishna Rapole (2009)
45. Aruna Vadla (2009)
44. Hemanth Ande (2008)
43. Curtis Cahoon – Low-Voltage CMOS Temperature Sensor Design using Schottky Diode-Based References (2008)
42. Prashanth Busa (2008)
41. John McCoy III (2008)
40. Dennis Montierth – Using Delta-Sigma-Modulation for Sensing in a CMOS Imager (2008)
39. Rudi Rashwand (2008)
38. Barsha Shrestha (co-supervised with Zhu Han) – Wireless Access in Vehicular Environments using Bit Torrent and Bargaining (2008)
37. Eric Becker – Design of an Integrated Half-Cycle Delay Line Duty Cycle Corrector Delay Locked Loop (2007)

36. Matthew Leslie – Noise-Shaping Sense Amplifier for Cross-Point Arrays (2007)
35. Jose Monje (2007)
34. Sanghyun Park (2007)
33. Vishal Saxena – Indirect Feedback Compensation Techniques for Multi-Stage Operational Amplifiers (2007)
32. Meshack Appikarla (2006)
31. Eric Booth – Wide Range, Low Jitter Delay-Locked Loop Using a Graduated Digital Delay Line and Phase Interpolator (2006)
30. Sucheta Das (2006)
29. Krishna Duvvada – High Speed Digital CMOS Input Buffer Design (2006)
28. Krishnamraju Kurra (2006)
27. Soumya Narasimhan (2006)
26. Roger Porter (2006)
25. David Butler – Low-Voltage Bandgap Reference Design Utilizing Schottky Diodes (2005)
24. Dragos Dimitriu (2005)
23. Surendranath Eruvuru – Sensing Circuit Design for an Ion Mobility Spectrometer (2005)
22. Sandhya Sandireddy (2005)
21. Harish Singidi (2005)
20. Indira Vemula – Delta-Sigma Modulator Used in CMOS Imagers (2005)
19. Bhavana Kollimarla – A 1-Bit Analog-to-Digital Converter Using Delta Sigma Modulation for Sensing in CMOS Imagers (2004)
18. Sandeep Pemmaraju – High Voltage Charge Pump Circuit for an Ion Mobility Spectrometer (2004)
17. Ravindra Puthumbaka – Circuit Design for an Ion Mobility Spectrometer (2004)
16. Brandon Roth – Comparison of Asynchronous vs. Synchronous Design Technologies using a 16-bit Binary Adder (2004)
15. Jennifer Taylor – Reading and Writing Flash Memory Using Delta-Sigma Modulation (2004)
14. Jing Plaisted – Methods for Memory Testing (2003)
13. Murugesh Subramaniam – Flash Memory Sensing Using Averaging (2003)
12. Brian Johnson – Application of an Asynchronous FIFO in a DRAM Data Path (2002)
11. Scott Ward – Electrostatic Discharge (ESD) Protection in CMOS (2002)
10. Tyler Gomm – Design of a Delay-Locked Loop with a DAC-Controlled Analog Delay Line (2001)
9. Gexin Huang (2001)
8. Chris Atkins (2000)
7. Thaddeus Black (2000)
6. Zuxu Qin (2000)
5. Hao Chen (1999)
4. Doug Hackler (co-supervised with Steve Parke) – TMOS: A Novel Design for MOSFET Technology (1999)
3. Song Liu – Design of a CMOS 6-bit Folding and Interpolating Analog-to-Digital Converter (1999)
2. Ben Ba (1997)
1. Brent Keeth – A Novel Architecture for Advanced High Density Dynamic Random Access Memories (1996)

GRANTED US PATENTS

152. Baker, R. J., "Quantizing circuits having improved sensing," **10,658,018**, May 19, 2020.
151. Baker, R. J., "Quantizing circuits having improved sensing," **10,403,339**, September 3, 2019.
150. Baker, R. J., "Digital Filters with Memory," **10,366,744**, July 30, 2019.
149. Baker, R. J., "Quantizing circuits having improved sensing," **10,127,954**, November 13, 2018.
148. Baker, R. J. and Parkinson, W., "NMOS regulated voltage reference," **9,753,481**, September 5, 2017.
147. Baker, R. J., "Digital Filters with Memory," **9,734,894**, August 15, 2017.
146. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **9,697,883**, July 7, 2017
145. Baker, R. J., "Comparators for delta-sigma modulators," **9,641,193**, May 2, 2017.
144. Baker, R. J., "Quantizing circuits having improved sensing," **9,449,664**, September 20, 2016.
143. Baker, R. J., "Error detection for multi-bit memory," **9,336,084**, May 10, 2016.
142. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **9,299,423**, March 29, 2016.

141. Baker, R. J., "Methods for sensing memory elements in semiconductor devices," **9,299,405**, March 29, 2016.
140. Baker, R. J., "Comparators for delta-sigma modulators," **9,135,962**, September 15, 2015.
139. Baker, R. J., "Resistive memory element sensing using averaging," **9,081,042**, July 14, 2015.
138. Baker, R. J., "Digital Filters with Memory," **9,070,469**, June 30, 2015.
137. Baker, R. J., "Reference current sources," **8,879,327**, November 4, 2014.
136. Baker, R. J. and Beigel, K. D., "Multi-resistive integrated circuit memory," **8,878,274**, November 4, 2014.
135. Baker, R. J., "Methods for sensing memory elements in semiconductor devices," **8,854,899**, October 7, 2014.
134. Baker, R. J., "Quantizing circuits with variable parameters," **8,830,105**, September 9, 2014.
133. Baker, R. J., "Integrators for delta-sigma modulators," **8,754,795**, June 17, 2014.
132. Baker, R. J., "Methods of quantizing signals using variable reference signals," **8,717,220**, May 6, 2014.
131. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **8,712,249**, April 29, 2014.
130. Baker, R. J., "Resistive memory element sensing using averaging," **8,711,605**, April 29, 2014.
129. Baker, R. J., "Memory with correlated resistance," **8,681,557**, March 25, 2014.
128. Baker, R. J., "Reference current sources," **8,675,413**, March 18, 2014.
127. Baker, R. J., "Methods for sensing memory elements in semiconductor devices," **8,582,375**, November 12, 2013.
126. Linder, L. F., Renner, D., MacDougall, M., Geske, J., and Baker, R. J., "Dual well read-out integrated circuit (ROIC)," **8,581,168**, November 12, 2013.
125. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **8,516,292**, August 20, 2013.
124. Baker, R. Jacob, "Resistive memory element sensing using averaging," **8,441,834**, May 14, 2013.
123. Qawi, Q. I., Drost, R. J., and Baker, R. Jacob, "Increased DRAM-array throughput using inactive bitlines," **8,395,947**, March 12, 2013.
122. Baker, R. Jacob, "Memory with correlated resistance," **8,289,772**, October 16, 2012.
121. Lin, F. and Baker, R. Jacob, "Phase splitter using digital delay locked loops," **8,218,708**, July 10, 2012.
120. Baker, R. Jacob, "Subtraction circuits and digital-to-analog converters for semiconductor devices," **8,194,477**, June 5, 2012.
119. Baker, R. J., "Digital Filters for Semiconductor Devices," **8,149,646**, April 3, 2012.
118. Baker, R. J., "Error detection for multi-bit memory," **8,117,520**, February 14, 2012.
117. Baker, R. J., "Integrators for delta-sigma modulators," **8,102,295**, January 24, 2012.
116. Baker, R. J., "Devices including analog-to-digital converters for internal data storage locations," **8,098,180**, January 17, 2012.
115. Baker, R. J. and Beigel, K. D., "Multi-resistive integrated circuit memory," **8,093,643**, January 10, 2012.
114. Baker, R. J., "Quantizing circuits with variable parameters," **8,089,387**, January 3, 2012.
113. Baker, R. J., "Reference current sources," **8,068,367**, November 29, 2011.
112. Baker, R. J., "Methods of quantizing signals using variable reference signals," **8,068,046**, November 29, 2011.
111. Baker, R. J., "Systems and devices including memory with built-in self-test and methods of making using the same," **8,042,012**, October 18, 2011.
110. Baker, R. J., "Memory with correlated resistance," **7,969,783**, June 28, 2011.
109. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **7,941,056**, May 10, 2011.
108. Baker, R. J., "K-delta-1-sigma modulator," **7,916,054**, March 29, 2011.
107. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **7,877,623**, January 25, 2011.
106. Lin, F. and Baker, R. J., "Phase splitter using digital delay locked loops," **7,873,131**, January 18, 2011.
105. Hush, G. and Baker, R. J., "Complementary bit PCRAM sense amplifier and method of operation," **7,869,249**, January 11, 2011.
104. Baker, R. J., "Subtraction circuits and digital-to-analog converters for semiconductor devices," **7,839,703**, November 23, 2010.
103. Baker, R. J., "Digital Filters with Memory" **7,830,729**, November 9, 2010.
102. Baker, R. J., "Systems and devices including memory with built-in self test and methods of making using the same," **7,818,638**, October 19, 2010.
101. Baker, R. J., "Integrators for delta-sigma modulators," **7,817,073**, October 19, 2010.

100. Baker, R. J., "Digital filters for semiconductor devices," **7,768,868**, August 3, 2010.
99. Baker, R. J., "Quantizing circuits with variable reference signals," **7,733,262**, June 8, 2010.
98. Baker, R. J., "Quantizing circuits for semiconductor devices," **7,667,632**, February 23, 2010.
97. Baker, R. J., and Beigel, K. D., "Multi-resistive integrated circuit memory," **7,642,591**, January 5, 2010.
96. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **7,616,474**, November 10, 2009.
95. Baker, R. J., "Resistive memory element sensing using averaging," **7,577,044**, Aug. 18, 2009.
94. Baker, R. J., "Quantizing circuits with variable parameters," **7,538,702**, May 26, 2009.
93. Baker, R. J., "Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors," **7,528,877**, May 5, 2009.
92. Baker, R. J., "Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors," **7,515,188**, April 7, 2009.
91. Taylor, J. and Baker, R. J., "Method and apparatus for sensing flash memory using delta-sigma modulation," **7,495,964**, February 24, 2009.
90. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **7,489,575**, February 10, 2009.
89. Baker, R. J., "Per column one-bit ADC for image sensors," **7,456,885**, November 25, 2008.
88. Staples, T. and Baker, R. J., "Input buffer design using common-mode feedback," **7,449,953**, November 11, 2008.
87. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **7,421,607**, September 2, 2008.
86. Baker, R. J., "Methods for resistive memory element sensing using averaging," **7,372,717**, May 13, 2008.
85. Taylor, J. and Baker, R. J., "Method and apparatus for sensing flash memory using delta-sigma modulation," **7,366,021**, April 29, 2008.
84. Hush, G. and Baker, R. J., "Method of operating a complementary bit resistance memory sensor and method of operation," **7,366,003**, April 29, 2008.
83. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **7,330,390**, February 12, 2008.
82. Baker, R. J., "Input and output buffers having symmetrical operating characteristics and immunity from voltage variations," **7,319,620**, January 15, 2008.
81. Staples, T. and Baker, R. J., "Method and apparatus providing input buffer design using common-mode feedback," **7,310,018**, December 18, 2007.
80. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **7,286,428**, October 23, 2007.
79. Baker, R. J., and Cowles, T. B., "Method and apparatus for reducing duty cycle distortion of an output signal," **7,271,635**, September 18, 2007.
78. Baker, R. J., and Cowles, T. B., "Method and apparatus for reducing duty cycle distortion of an output signal," **7,268,603**, September 11, 2007.
77. Hush, G., Baker, R. J., and Moore, J., "Skewed sense AMP for variable resistance memory sensing," **7,251,177**, July 31, 2007.
76. Hush, G. and Baker, R. J., "Method of operating a complementary bit resistance memory sensor," **7,242,603**, July 10, 2007.
75. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **7,237,136**, June 26, 2007.
74. Moore, J. and Baker, R. J., "Rewrite prevention in a variable resistance memory," **7,224,632**, May 29, 2007.
73. Baker, R. J., "Integrated charge sensing scheme for resistive memories," **7,151,698**, December 19, 2006.
72. Baker, R. J., "Adjusting the frequency of an oscillator for use in a resistive sense amp," **7,151,689**, December 19, 2006.
71. Baker, R. J., "Resistive memory element sensing using averaging," **7,133,307**, Nov. 7, 2006.
70. Lin, F. and Baker, R. J., "Phase detector for all-digital phase locked and delay locked loops," **7,123,525**, October 17, 2006.
69. Baker, R. J., and Beigel, K. D., "Integrated circuit memory with offset capacitor," **7,109,545**, September 19, 2006.
68. Baker, R. J., "Input and output buffers having symmetrical operating characteristics and immunity from voltage variations," **7,102,932**, September 5, 2006.
67. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **7,095,667**, August 22, 2006.

66. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **7,082,045**, July 25, 2006.
65. Baker, R. J., "System and method for sensing data stored in a resistive memory element using one bit of a digital count," **7,009,901**, March 7, 2006.
64. Hush, G. and Baker, R. J., "Complementary bit resistance memory sensor and method of operation," **7,002,833**, February 21, 2006.
63. Lin, F. and Baker, R. J., "Phase detector for all-digital phase locked and delay locked loops," **6,987,701**, January 17, 2006.
62. Baker, R. J., "Adjusting the frequency of an oscillator for use in a resistive sense amp," **6,985,375**, January 10, 2006.
61. Baker, R. J., "Method for reducing power consumption when sensing a resistive memory," **6,954,392**, October 11, 2005.
60. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **6,954,391**, October 11, 2005.
59. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **6,954,390**, October 11, 2005.
58. Lin, F. and Baker, R. J., "Phase splitter using digital delay locked loops," **6,950,487**, September 27, 2005.
57. Baker, R. J., "Method and apparatus for measuring current as in sensing a memory cell," **6,930,942**, August 16, 2005.
56. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **6,917,534**, July 12, 2005.
55. Baker, R. J., "Dual loop sensing scheme for resistive memory elements," **6,914,838**, July 5, 2005.
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- Harvard, Q. I. and Baker, R. J., "Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design," a presentation covering semiconductor packaging, DRAM architectures, and I/O circuits. The goal of this work is to investigate replacing the currently used dual in-line memory modules (DIMMs) with a smaller and a lower power memory module, a "Nano-Module."
- Baker, R. J., and Campbell, K. A., "Reconfigurable Analog Electronics using the Memristor."
- Baker, R. J., and Saxena, V., "A K-Delta 1-Sigma Modulator for Wideband Analog-to-Digital Conversion."
- Li, K., Saxena, V., and Baker, R. J., "The Baker ADC: An Overview,"
- Saxena, V., and Baker, R. J., "High-Speed Op-Amp Design: Compensation and Topologies for Two and Three Stage Designs,"
- Baker, R. J., "Circuit Design for MLC Flash: Towards a Semiconductor Replacement for the Hard Disk Drive."

- Baker, R. J., Terman Award Acceptance Speech, given at the Frontiers in Education Conference (FIE 2007), Milwaukee, WI, October 11, 2007.
- Baker, R. J., "The One-Transistor, One-Capacitor (1T1C) Dynamic Random Access Memory (DRAM), and its Impact on Society," presented at the Franklin Institute, in the symposium honoring Dr. Robert H. Dennard and his receipt of the 2007 Benjamin Franklin Medal in Electrical Engineering, April 25, 2007.
- Baker, R. J. and Saxena, V., "Design of Bandpass Delta-Sigma Modulators: Avoiding Common Mistakes."
- Baker, R. J., "Sensing Circuits for Resistive Memory."
- Hadrick, M. and Baker, R. J., "Sensing in CMOS Imagers using Delta-Sigma Modulation."
- Baker, R. J., "Design of High-Speed CMOS Op-Amps for Signal Processing," IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED), April, 2005
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31. Loo, S. M., Cole, J., Youngberg, R., Baker, R. J., Gribb, M. M., "Field-programmable gate array in a miniature ion mobility spectrometer sensor system," *Proceedings of the 2006 International Conference on Embedded Systems & Applications*, June 26-29, 2006, Las Vegas, NV.
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29. Duvvada, K., Saxena, V., and Baker, R. J., High Speed Digital Input Buffer Circuits, *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 11-12, April, 2006.
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26. Sevier, D., Gribb, M., Plumlee, D., Moll, A. J., Hill, H. H., Hong, F., Baker, R. J., Loo, S. M., Walters, R. and Imonigie, J., "An In-Situ Ion Mobility Spectrometer Sensor System for Detecting Gaseous VOCs in the Vadose Zone," *Fourth International Conference on Unsaturated Soils (UNSAT '06) Conference, April 2-6, 2006, Carefree, AZ.*
25. Gribb, M., Hill, H. H., Baker, R. J., Loo, S. M., and Moll, A. J., "Ion Mobility Spectrometer (IMS) Sensor Project," presented at the *Environmental & Subsurface Science Symposium*, Inland Research Alliance, Sept. 19-21, 2005, Big Sky, Montana.
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22. Cheek, B. J., Southwick III, R. G., Ogas, M. L., Nagler, P. E., Whelchel, D., Kumar, S., Baker, R. J., and Knowlton, W. B., "Preliminary Soft Breakdown (SBD) Effects In CMOS Building Block Circuits," poster presentation at *2004 IEEE International Integrated Reliability Workshop*, Oct. 18-21, 2004.
21. Ogas, M., Southwick, R. G., Cheek, B. J., Lawrence, C. E., Kumar, S., Haggag, A., Baker, R. J., and Knowlton, W. B., "Multiple Waveform Pulse Voltage Stress Technique for Modeling Noise in Ultra-Thin Oxides," poster presentation at the *Workshop on Microelectronics and Electron Devices*, Boise, Idaho, April 16, 2004.
20. Ogas, M. L., Southwick III, R. G., Cheek, B. J., Baker, R. J., Bersuker, G., and Knowlton, W. B., "Survey of Oxide Degradation in Inverter Circuits Using 2.0nm MOS Devices," in *Proceedings of the 2004 IEEE International Integrated Reliability Workshop*, pp. 32-36.
19. Cheek, B. J., Stutzke, N., Santosh, K., Baker, R. J., Moll, A. J., and Knowlton, W. B., Investigation of Circuit-Level Oxide Degradation and its Effect on CMOS Inverter Operation Performance and MOSFET Characteristics, *2004 IEEE International Reliability Physics Symposium*, April, 25-29.

18. Stutzke, N., Cheek, B. J., Wiscombe, M., Lowman, T., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., *Effects of Circuit-Level Stress on Inverter Performance and MOSFET Characteristics*, 2003 IEEE International Integrated Reliability Workshop, Oct, 20-23.
17. Ogas, M. L., Southwick, R. G., Cheek, B. J., Lawrence, C. E., Kumar, S., Haggag, A., Baker, R. J., and Knowlton, W. B., *Investigation of Multiple Waveform Pulse Voltage Stress (MWPVS) Technique in Ultra-Thin Oxides*, poster presentation at the 2003 IEEE International Integrated Reliability Workshop Oct, 20-23.
16. Baker, R. J., *Mixed-Signal Design in the Microelectronics Curriculum*, IEEE University/Government/Industry Microelectronics (UGIM) Symposium, June 30 - July 2.
15. Hartman, J. A., Baker, R. J., Gribb, M., Hill, H. H., Jessing, J., Moll, A. J., Prouty, and Russell, D., *A Miniaturized Ion Mobility Spectrometer (IMS) Sensor for Wireless Operation*, FAME (Frontiers in Assessment Methods for the Environment) Symposium, Sponsored by NSF, Minneapolis, Minnesota, August 10-13, 2003.
14. Lawrence, C.E., Cheek, B. J., Lawrence, T. E., Kumar, S., Haggag, A., Baker, R. J., and Knowlton, W. B., *Gate Dielectric Degradation Effects on nMOS Devices Using a Noise Model Approach*, IEEE University/Government/Industry Microelectronics (UGIM) Symposium, June 30 - July 2, 2003.
13. Cheek, B., Lawrence, C., Lawrence, T., Gomez, J., Caldwell, T., Kiri, D., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., *Gate Dielectric Degradation Effects on nMOS Devices and Simple IC Building Blocks (SICBBs)*, IEEE Electron Devices Society Boise Meeting, Boise, ID Oct. 25, 2002.
12. Lawrence, C., Cheek, B., Caldwell, T., Lawrence, T., Kiri, D., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., *Pulse voltage stressing of ultrathin gate oxides in NMOS devices*, poster session at IEEE International Integrated Reliability Workshop, October 21-24, 2002.
11. Cheek, B., Lawrence, C., Lawrence, T., Caldwell, T., Kiri, D., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., *Circuit level reliability of ultrathin gate oxides for SICBBs: Preliminary study concentrated on the effect of stress on the NMOSFET of an inverter*, poster session at the IEEE International Integrated Reliability Workshop, October 21-24, 2002.
10. Baker, R. J., "Sensing Circuits for Resistive Memory," *IEEE Electron Devices Society Meeting*, Boise, Idaho October 25, 2002.
9. Rivera, B., Baker, R. J., Melngailis, J., "Design and Layout of Schottky Diodes in a Standard CMOS Process," 2001 International Semiconductor Device Research Symposium, Washington DC, Dec. 2001.
8. Hess, H. and Baker, R. J., "Easier Method to Simultaneously Trigger Series-Connected MOS Devices," *Power Systems World Conference 2000*, Boston, Massachusetts, September 2000.
7. Baker, R. J., and Hess, H., "Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices." *International Electric Machines and Drives Conference*, Seattle, Washington, May 1999, pp. 673-676.
6. Baker, R. J., "A windows based integrated circuit design tool for distance education," *International Conference on Simulation and Multimedia in Engineering Education*."
5. Chen, H. and Baker, R. J., "A CMOS Standard-Cell Library for the PC-based LASI Layout System," *Proceedings of the 41st International Midwest Symposium on Circuits and Systems*, August 9-12, 1998.
4. Liu, S. and Baker, R. J., "Process and temperature performance of a CMOS beta-multiplier voltage reference," *Proceedings of the 41st International Midwest Symposium on Circuits and Systems*, August 9-12, 1998.
3. Boyce, D.E. and Baker, R. J., "A Complete Layout System for the PC," *IEEE 40th International Midwest Symposium on Circuits and Systems*, 1997.
2. Baker, R. J., and Blair, J. J., "Step response considerations and the design of a suitable step generator for high speed digitizer testing," *LLNL's Third Annual Workshop on High Speed Digitizers*, April 3-4, Las Vegas, Nevada, 1991.
1. Baker, R. J., "Step-recovery diodes sharpen pulses," *Engineering Design News Magazine*, pp. 154-156, May 10, 1990.

EXPERT WITNESS EXPERIENCE (LAST 5 YEARS)

The law firms and clients (underlined) whom I have provided expert witness services in electrical and computer engineering are listed below. I have been deposed 93 times, given expert testimony at 12 trials (7 USITC, 2 D. Del., 1 Arbitr., 1 S.D. Cal., and 1 E.D. Tex.), and participated in 1 mediation.

McDermott Will & Emery LLP (Chicago, IL and Austin, TX)

Case – Xilinx, Inc. v. Polaris Innovations Limited

Case Numbers – IPR2023-00513 and IPR2023-00514. Petitions filed on February 6, 2023.

Case Subject Matter – Methods for terminating a memory chip with various termination resistances and output drivers for integrated circuits.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Norton Rose Fulbright LLP (Austin, TX and Dallas, TX)

Case – Current Lighting Solutions, LLC d/b/a GE Current v. Jiaying Super Lighting Electric Appliance Co., Ltd.

Case Number – IPR2023-00270. Petition filed on December 19, 2022.

Case Number – IPR2023-00271. Petition filed on December 14, 2022.

Case Subject Matter – LED lighting, lamps, tube lamps, assembly, and associated circuits and electronics.

Work Performed – Provided expert consulting services and wrote declarations for inter partes review.

Paul Hastings LLP (Washington, DC)

Case – Ex Parte Reexaminations

Case Numbers – 90/015155 and 90/015156. Requests filed on November 7, 2022.

Case Number – 90/015134. Request filed on October 14, 2022.

Case Number – 90/015130. Request filed on September 30, 2022.

Case Subject Matter – Packaging and fabrication of light emitting diodes (LEDs).

Work Performed – Provided expert consulting services and wrote declaration.

Sheppard, Mullin, Richter & Hampton LLP (Menlo Park, CA)

Case – Bell Semiconductor, LLC v. NXP, SMC, Micron, Nvidia, Advanced Micro Devices (AMD), Acer, Infineon, Qualcomm, Motorola Mobility, and Western Digital

Case Number – ITC Investigation No. 337-TA-1340. Complaint filed October 6, 2022.

Case Subject Matter – Electronic devices, semiconductor devices, and components.

Work Performed – Provided expert consulting services.

O'Melveny & Myers LLP (Los Angeles, CA)

Case – Daedalus Prime LLC v. Samsung Electronics and TSMC

Case Number – ITC Investigation No. 337-TA-1335. Complaint filed September 12, 2022.

Case Subject Matter – Semiconductor devices, mobile devices, and components.

Work Performed – Provided expert consulting services.

DLA Piper (Chicago, IL and Washington, DC)

Case – Ampt, LLC v. SolarEdge Technologies, Inc.

Case Number – ITC Investigation No. 337-TA-1327. Complaint filed July 28, 2022.

Case Subject Matter – Solar power optimizers, inverters, and components.

Work Performed – Provided expert consulting services including writing declarations for claim construction and expert reports.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – Samsung Electronics Co., Ltd. v. Scramoge Technology Ltd.

Case Numbers – IPR2022-01052, IPR2022-01053, and IPR2022-01058. Petitions filed on May 26, 2022.

Case Numbers – IPR2022-01054, IPR2022-01055, IPR2022-01056, and IPR2022-01057. Petitions filed on May 24, 2022.

Case Number – IPR2022-00939. Petition filed on April 29, 2022.

Case Subject Matter – An antenna that supports wireless charging.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – Ex Parte Reexaminations

Case Number – 90/015020. Request filed on May 2, 2022.

Case Number – 90/014906. Request filed on November 12, 2021.

Case Number – 90/014899. Request filed on November 10, 2021.

Case Number – 90/014888. Request filed on October 21, 2021.

Case Numbers – 90/014886 and 90/014887. Requests filed on October 20, 2021.

Case Number – 90/014885. Request filed on October 19, 2021.

Case Subject Matter – Universal Serial Bus (USB) for charging.

Work Performed – Provided expert consulting services and wrote declarations.

DLA Piper (Chicago, IL, Austin, TX, and Washington, DC)

Case – SolarEdge Technologies, Inc. v. Fronius International GMBH

Case Number – IPR2022-00849. Petition filed on April 14, 2022.

Case Subject Matter – Mechanical assembly and enclosure whereby an upper housing part is detached from a lower housing part using a “rotate-and-lift” feature.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Kirkland & Ellis LLP (New York, NY)

Case – Samsung Electronics Co. v. Sonrai Memory Ltd.

Case Numbers – IPR2022-00305 and IPR2022-00306. Petitions filed on December 10, 2021.

Case Subject Matter – USB devices and circuits for saving power.

Work Performed – Provided expert consulting services including writing declarations for inter partes reviews.

Haynes and Boone, LLP (Washington, DC)

Case – Unified Patents, LLC v. Arigna Technology Limited

Case Number – IPR2022-00285. Petition filed on December 9, 2021.

Case Subject Matter – High voltage driver circuit for driving power devices such as insulated gate bipolar transistors (IGBTs).

Work Performed – Provided expert consulting services, wrote declaration for inter partes review and was deposed.

Paul Hastings LLP (Washington, DC)

Case – Samsung Electronics Co., Ltd. v. Lynk Labs, Inc.

Case Numbers – IPR2022-00149 and IPR2022-00150. Petitions filed on November 12, 2021

Case Numbers – IPR2022-00100 and IPR2022-00101. Petitions filed on October 28, 2021.

Case Numbers – IPR2022-00051, IPR2022-00052, and IPR2022-00098. Petitions filed on October 27, 2021.

Case Numbers – IPR2021-01575 and IPR2021-01576. Petitions filed on October 1, 2021.

Case Numbers – IPR2021-01299, IPR2021-01300, IPR2021-01345, IPR2021-01346, and IPR2021-01347. Petitions filed on September 7, 2021.

Case Subject Matter – Circuit design, including switching power supply design, rectifiers, power factor correction, etc. for lighting and displays using light emitting diodes (LEDs).

Work Performed – Provided expert consulting services, wrote declarations, and was deposed ten times.

Haynes and Boone, LLP (Plano, TX)

Case – Pure Storage, Inc. v. Digital Cache, LLC

Case Number – IPR2022-00121. Petition filed on October 29, 2021.

Case Subject Matter – Non-volatile memory (NVM) devices capable of retaining stored data in case of a power failure.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Banner Witcoff (Washington, DC)

Case – SolarEdge Technologies Ltd. v. Koolbridge Solar, Inc.

Case Numbers – IPR2022-00007, IPR2022-00008, IPR2022-00009, IPR2022-00010, IPR2022-00011, and IPR2022-00012. Petitions filed on October 11, 2021.

Case Numbers – IPR2022-00013, IPR2022-00014, and IPR2022-00015. Petitions filed on October 8, 2021.

Case Subject Matter – DC-to-AC converters using full-bridges, multi-level conversion for power systems, and other electronics for harvesting solar energy.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – Samsung Electronics Co., Ltd. v. LED Wafer Solutions LLC

Case Number – IPR2021-01554. Petition filed on September 20, 2021.

Case Number – IPR2021-01526. Petition filed on September 10, 2021.

Case Number – IPR2021-01506. Petition filed on September 7, 2021.

Case Number – IPR2021-01491. Petition filed on September 3, 2021.

Case Subject Matter – Packaging of light emitting diodes (LEDs).

Work Performed – Provided expert consulting services and wrote declarations.

Paul Hastings, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/014,846. Request filed on August 30, 2021.

Case Subject Matter – Wireless power transmission and ways to wirelessly charge and/or discharge a battery.

Work Performed – Provided expert consulting services and wrote declaration.

Jones Day (San Diego, CA and Pittsburgh, PA)

Case – SOLiD, Inc. v. CommScope Technologies LLC

Case Numbers – IPR2021-01390, IPR2021-01391, IPR2021-01392, IPR2021-01393, and IPR2021-01394. Petitions filed on August 12, 2021.

Case Subject Matter – Digital antenna system that enables extension of radio frequency (RF) analog signals from base stations to areas (e.g., inside of buildings) where access to such signals is inhibited.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declaration.

Unified Patents, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/019,015. Request filed on July 20, 2021.

Case Subject Matter – Voltage-controlled oscillator (VCO) temperature compensation.

Work Performed – Provided expert consulting services and wrote declaration.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC v. Unification Technologies LLC

Case Numbers – IPR2021-00940, IPR2021-00941, and IPR2021-00942. Petitions filed on June 4, 2021.

Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declarations.

Hill, Kertscher & Wharton, LLP (Atlanta, GA)

Case – Kaijet Technology v. Sanho Corporation

Case Number – IPR2021-00886. Petition filed on April 30, 2021.

Case Subject Matter – Port extension apparatus for headphone jack, USB (Universal Serial Bus or Type-C ports), and video ports such as VGA (Video Graphics Array), DVI (Digital Visual Interface), HDMI (High-Definition Multimedia Interface), DP (Display Port), and mini-DP.

Work Performed – Provided expert consulting services for inter partes review, wrote declaration, was deposed.

O'Melveny & Myers LLP (Los Angeles, CA and New York, NY)

Case – Solas OLED LTD. v. Samsung Electronics Co. LTD.

Case Number – Texas, ED (Marshall) 2:21-cv-00105. Complaint filed March 22, 2021.

Case Subject Matter – Touch-sensors for gesture recognition and signal processing for capacitive touch displays.

Work Performed – Provided expert consulting services including writing declaration for claim construction.

O'Melveny & Myers LLP (San Francisco, CA)

Case – Super Interconnect Technologies LLC v. Google LLC

Case Number – Texas, ED (Marshall) 2:18-cv-00463 (complaint filed November 2, 2018) and Texas, WD (Waco) 6:21-cv-00259 (complaint filed March 15, 2021).

Case Subject Matter – Transmission of data and clock signals. Serial signals such as transition minimized differential signaling. Communications between processors and non-volatile storage such as Universal Flash Storage (UFS) and embedded MultiMedia Controller (eMMC).

Work Performed – Provided expert consulting services and wrote expert reports.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, and Irvine, CA)

Case – Fundamental Innovation Systems International LLC v. Anker Innovations and Fantasia Trading LLC d/b/a Ankerdirect

Case Number – Delaware, 1:21-cv-00339. Complaint filed on March 5, 2021.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – TCT Mobile Inc. and TCL Communication, Inc. v. Fundamental Innovation Systems International LLC

Case Numbers – IPR2021-00597, IPR2021-00598, and IPR2021-00599. Petitions filed on February 26, 2021.

Case Number – IPR2021-00428. Petition filed on January 13, 2021.

Case Number – IPR2021-00410. Petition filed on January 11, 2021.

Case Number – IPR2021-00395. Petition filed on December 31, 2020.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services including writing declarations for inter partes reviews. Was deposed twice.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – Samsung, Inc. v. Pictos Technologies, Inc.

Case Number – IPR2021-00557. Petition filed on February 18, 2021.

Case Number – IPR2021-00436. Petition filed on January 19, 2021.

Case Numbers – IPR2021-00437 and IPR2021-00438. Petitions filed on January 15, 2021.

Case Subject Matter – Solid-state imaging devices including red, green, and blue pixels, data conversion circuits, and interpolation circuits. CMOS imagers including fabrication and design, active pixels, and semiconductor physics.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

O'Melveny & Myers LLP (San Francisco, CA) and DLA Piper (New York, NY)

Case – Solas OLED Ltd. v. BOE Technology Group Co. Ltd. and Samsung Electronics

Case Number – ITC Investigation No. 337-TA-1243. Complaint filed January 5, 2021.

Case Subject Matter – Active matrix OLED display devices and components

Work Performed – Provided expert consulting services, wrote expert reports, was deposed, and testified at trial.

Paul Hastings LLP (Washington, DC)

Case – Samsung, Inc. v. Garrity Power Services LLC

Case Number – IPR2021-00389. Petition filed on December 31, 2020.

Case Subject Matter – Power electronics including full-bridge PWM modules for wireless power transmission using magnetic coupling via antennas and transformers. Design of inductors and coils.

Work Performed – Provided expert consulting services and wrote declaration for inter partes reviews.

Morgan, Lewis & Bockius LLP (Palo Alto, CA and Shanghai, CN)

Case – Monolithic Power Systems, Inc. v. Meraki Integrated Circuit Technology, Inc. and Promate Electronic Company, LTD.

Case Number – Texas, WD (Waco) 6:20-cv-00876. Complaint filed on December 24, 2020.

Case Subject Matter – Design of switching power supplies including synchronous rectification.

Work Performed – Provided expert consulting services including declaration for claim construction, trade secret analysis and declaration, and Markman tutorial.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC; Dell Technologies Inc.; Dell Inc.; and HP Inc. v. Unification Technologies LLC

Case Numbers – IPR2021-00343, IPR2021-00344, and IPR2021-00345. Petitions filed on December 22, 2020.

Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services for inter partes reviews, wrote declarations, and was deposed.

Jones Day (Chicago, IL and Dallas, TX)

Case – WSOU Investments, LLC d/b/a Brazos Licensing and Development v. Xilinx, Inc.

Case Numbers – Delaware, 1:20-cv-01231 and Delaware, 1:20-cv-01233. Complaints filed on November 23, 2020 and September 16, 2020.

Case Subject Matter – Controlling power cycles in communication devices and transferring multiple asynchronous clock signals.

Work Performed – Provided expert consulting services, wrote claim construction declaration, wrote expert reports, and was deposed.

O'Melveny & Myers LLP (Los Angeles, CA)

Case – Cosemi Technologies, Inc. v. EverPro Technologies, Fibbr Technologies, Logitech, Inc., and Facebook Technologies

Case Number – ITC Investigation No. 337-TA-1233. Complaint filed October 28, 2020.

Case Subject Matter – Data cables, including HDMI, Display Port, and USB Type A, USB Type C and USB Type A/C data cables.

Work Performed – Provided expert consulting services.

Kirkland & Ellis LLP (Boston, MA and New York, NY)

Case – Pictos Technologies, Inc. v. Samsung Electronics Co., LTD. and Samsung Semiconductor, Inc.

Case Number – ITC Investigation No. 337-TA-1231. Complaint filed September 25, 2020.

Case Subject Matter – Solid-state imaging devices including red, green, and blue pixels, correction of bad pixels, data conversion circuits, and interpolation circuits. CMOS imagers including fabrication and design, active pixels, and semiconductor physics.

Work Performed – Provided expert consulting services and wrote expert report.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – Fundamental Innovation Systems International LLC v. TCT Mobile Inc. and TCL Communication, Inc.

Case Number – Delaware, 1:20-cv-00552. Complaint filed on September 11, 2020.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services including writing declarations, expert report on invalidity, and was deposed.

Walters Wilson LLP (Redwood City, CA)

Case – Western Digital Corporation and SanDisk, LLC v. Martin Kuster

Case Numbers – IPR2020-01410 and IPR2020-01411. Petitions filed on August 3, 2020.

Case Subject Matter – Computer connectors such as universal serial bus (USB) that connect to peripheral devices such as mice, keyboards, displays, printers, external storage, etc.

Work Performed – Provided expert consulting services for inter partes review, wrote declarations and was deposed.

O'Melveny & Myers LLP (Los Angeles, CA)

Case – Advanced Micro Devices, Inc. v. Monterey Research, LLC

Case Number – IPR2020-01315. Petition filed on July 16, 2020.

Case Number – IPR2020-00985. Petition filed on May 26, 2020.

Case Subject Matter – Reading and writing to semiconductor memory such as SRAM and double data rate (DDR) DRAM. Buffer circuits with variable current supplies for controlling the rise and fall times of output signals.

Work Performed – Provided expert consulting services for inter partes review, wrote declarations and was deposed twice.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – Unification Technologies LLC v. Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC

Case Number – Texas, WD (Waco) 6:20-cv-00500. Complaint filed June 5, 2020.

Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services, wrote declaration for claim construction, and was deposed.

Ari Law, P.C. (Palo Alto, CA) and Hill, Kertscher & Wharton, LLP (Atlanta, GA)

Case – Sanho Corporation v. Kaijet Technology, Magic Control Technology, and Star View Global

Case Numbers – Georgia, ND (Atlanta) 1:18-cv-05385 (third amended complaint filed November 14, 2019) and Georgia, ND (Atlanta) 1:20-cv-02150 (filed May 19, 2020).

Case Subject Matter – Port extension apparatus for headphone jack, USB (Universal Serial Bus or Type-C ports), and video ports such as VGA (Video Graphics Array), DVI (Digital Visual Interface), HDMI (High-Definition Multimedia Interface), DP (Display Port), and mini-DP.

Work Performed – Provided expert consulting services, wrote declaration for claim construction, and expert reports. Was deposed.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – Fundamental Innovation Systems International LLC v. Coolpad Group Limited, Coolpad Technologies, Inc., and Yulong Computer Telecommunication Scientific Co. Ltd.

Case Number – Texas, ED (Marshall) 2:20-cv-00117. Complaint filed on April 23, 2020.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services including writing declaration for claim construction.

Pillsbury Winthrop Shaw Pittman LLP (San Francisco, CA and Shanghai, China)

Case – SMIC, Americas v. Innovative Foundry Technologies LLC

Case Numbers – IPR2020-00837 and IPR2020-00839. Petitions filed on April 14, 2020.

Case Subject Matter – Methods of manufacturing a semiconductor component, such as a short-channel MOS device, including forming graded-junctions using spacers along the sidewalls of a transistor's gate.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declarations.

Russ August & Kabat (Los Angeles, CA)

Case – Oyster Optics, LLC v. Ciena Corporation

Case Number – California, ND (Oakland) 3:20-cv-02354. Complaint filed on April 7, 2020.

Case Subject Matter – Fiber optic telecommunication systems.

Work Performed – Provided expert consulting services, wrote claim construction declaration, and was deposed.

Russ August & Kabat (Los Angeles, CA)

Case – Seoul Semiconductor Co., Ltd. v. Document Security Systems, Inc.

Case Number – IPR2020-00938. Petition filed on May 18, 2020.

Case – Nichia Corporation v. Document Security Systems, Inc.

Case Number – IPR2020-00908. Petition filed on May 18, 2020.

Case – Cree, Inc. v. Document Security Systems, Inc.

Case Number – IPR2020-00557. Petition filed on February 11, 2020.

Case Subject Matter – Light emitting diodes (LEDs) as a light source, extraction of light.

Work Performed – Provided expert consulting services, wrote declaration for inter partes reviews, and was deposed three times.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – Flex Logix Technologies, Inc. v. Konda Technologies Inc.

Case Numbers – IPR2020-00260, IPR2020-00261, and IPR2020-00260. Petitions filed on December 16, 2019.

Case Numbers – PGR2019-00037, PGR2019-00040, and PGR2019-00042. Petitions filed on March 18, 2019.

Case Subject Matter – FPGA layout routing for integrated circuits and networks, electrical and computer engineering.

Work Performed – Provided expert consulting services and wrote declarations for post grant and inter partes reviews.

DLA Piper (Chicago, IL, Houston, TX, and Washington, DC) and White & Case LLP (New York, NY and Washington, DC)

Case – M-Red Inc. v. Panasonic Corporation

Case Number – Texas, ED (Marshall) 2:19-cv-00251. Complaint filed on July 16, 2019.

Case Subject Matter – Integrated circuit electronics adjustment, such as ring oscillators, using auto calibration. Evaluating a known good die using both wire and flip-chip interconnects.

Work Performed – Provided expert consulting services and wrote declaration for claim construction.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – Samsung, Inc. v. NuCurrent, Inc.

Case Number – IPR2019-01217. Petition filed on June 19, 2019.

Case Numbers – PGR2019-00049 and PGR2019-00050. Petitions filed on May 28, 2019.

Case Numbers – IPR2019-00858, IPR2019-00859, IPR2019-00860, IPR2019-00861, IPR2019-00862, and IPR2019-00863. Petitions filed on March 22, 2019.

Case Subject Matter – Wireless power transmission using magnetic coupling via antennas and transformers. Design of inductors and coils.

Work Performed – Provided expert consulting services and wrote declarations for post grant and inter partes reviews. Was deposed five times.

DLA Piper (East Palo Alto, CA)

Case – Invensas Corporation and Tessera Advanced Technologies, Inc. v. NVIDIA Corporation

Case Number – Delaware, 1:19-cv-00861. Complaint filed on May 8, 2019.

Case Subject Matter – Reference voltage circuits (programmable bandgaps) having a substantially zero temperature coefficient using bipolar and MOS transistors.

Work Performed – Provided expert consulting services.

Irell & Manella LLP (Los Angeles, CA)

Case – VLSI Technology LLC v. Intel Corporation

Case Number – Texas, WD (Waco) 6:19-cv-00256. Complaint filed on April 11, 2019.

Case Subject Matter – Static Random Access Memory (SRAM) having a variable power supply using charge-sharing capacitors, methods for designing digital systems, and hardware managed interrupt control.

Work Performed – Provided expert consulting services, wrote expert reports, declaration, and was deposed.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – Samsung, Inc. v. ProMOS Technologies, Inc.

Case Numbers – IPR2019-00779, IPR2019-00780, IPR2019-00781, IPR2019-00784, and IPR2019-00785. Petitions filed on March 5, 2019.

Case Subject Matter – Programmable latches that include non-volatile programmable elements, digital delay elements, and decoders for memory chips.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed four times.

Pillsbury Winthrop Shaw Pittman LLP (San Francisco, CA)

Case – Kingston Technology Company, Inc. v. Memory Technologies, LLC

Case Numbers – IPR2019-00645, IPR2019-00648, IPR2019-00651, and IPR2019-00654. Petitions filed on January 31, 2019.

Case Numbers – IPR2019-00642, IPR2019-00643, and IPR2019-00644. Petitions filed on January 30, 2019.

Case Number – IPR2019-00638. Petition filed on January 29, 2019.

Case Subject Matter – Memory cards including PC cards, compact flash (“CF”) cards, secure digital (“SD”) cards, programmable credit cards, and embedded multimedia cards (“eMMC”). Uses of EEPROM and Flash memory in built-in operating system (BIOS).

Work Performed – Provided expert consulting services for inter partes reviews and wrote declarations.

Morrison & Foerster LLP (San Francisco, CA) and Schwabe, Williamson & Wyatt PC (Portland, OR)

Case – Steven A.W. de Jaray, Perienne de Jaray, and Darrell R. Oswald v. Lattice Semiconductor Corporation

Case Number – Oregon, Circuit Court (Multnomah), 3:19-cv-00086. Complaint filed on January 17, 2019.

Case Subject Matter – Export controlled integrated circuits in various packages. Programmable logic devices (PLDs).

Work Performed – Provided expert consulting services. wrote expert reports, and was deposed.

Russ August & Kabat (Los Angeles, CA)

Case – Ring LLC v. SkyBell Technologies, Inc.

Case Numbers – IPR2019-00443, IPR2019-00444, IPR2019-00445, IPR2019-00446, and IPR2019-00447. Petitions filed on December 17, 2018.

Case Subject Matter – Electronic doorbell system with digital chime, video, motion detection, wired and wireless communication, and control panel.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed three times.

Baker Botts LLP (Austin, TX)

Case – Semiconductor Components Industries, LLC d/b/a ON Semiconductor v. Power Integrations, Inc.

Case Numbers – IPR2018-01810, IPR2018-01812, IPR2018-01816, and IPR2018-01818. Petitions filed on September 28, 2018.

Case Subject Matter – Switched-mode power supplies (e.g., flyback, buck, boost), controllers, transformers, and sensing multiple voltage values.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Kirkland & Ellis LLP (Washington, DC) and Fish & Richardson P.C. (Washington, DC)

Case – Samsung Electronics Co., LTD. and SK hynix Inc. v. BiTMICRO, LLC

Case Number – IPR2018-01720. Petition filed on September 19, 2018.

Case Number – IPR2018-01545. Petition filed on August 23, 2018.

Case Subject Matter – Solid state storage drives, stacked consumer electronics components (3D packaging, solder balls, flip-chip, TSVs, etc.), and products.

Work Performed – Provided expert consulting services including writing declarations for inter partes reviews.

Knobbe, Martens, Olson, & Bear, LLP (Los Angeles, CA) and White & Case LLP (Palo Alto, CA and Washington, DC)

Case – Toshiba America Information Systems, Inc. and MSI Computer Corp. v. Wallelex Microelectronics Ltd.

Case Number – IPR2018-01538. Petition filed on August 10, 2018.

Case Subject Matter – Double-sided male USB and various card-shaped devices and connectors, electrical and computer engineering.

Work Performed – Provided expert consulting services including writing declarations for inter partes review and was deposed.

Jones Day (Cleveland, OH and Pittsburgh, PA)

Case – Intel Corp. v. Qualcomm, Inc.

Case Numbers – IPR2018-01344 and IPR2018-01346. Petitions filed on July 6, 2018.

Case Numbers – IPR2018-01261, IPR2018-01293, and IPR2018-01295. Petitions filed on June 29, 2018.

Case Subject Matter – Communications, e.g., PCI Express (PCIe), USB, Firewire (IEEE-1394), between two processing nodes within a computing device such as a cell phone, tablet, or computer.

Work Performed – Provided expert consulting services for inter partes reviews including writing declaration and was deposed.

Orrick, Herrington & Sutcliffe LLP (Menlo Park, CA) and Weil, Gotshal & Manges LLP (Redwood Shores, CA)

Case – Micron Technology, Inc. v. North Star Innovations, Inc.

Case Numbers – IPR2018-00998 and IPR2018-00999. Petitions filed on May 1, 2018.

Case Number – IPR2018-00989. Petition filed on April 27, 2018.

Case Subject Matter – Output circuits for memory integrated circuits and voltage boosting circuits.

Work Performed – Provided expert consulting services including writing declarations for inter partes reviews, and was deposed.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – Samsung, Inc. v. Red Rock Analytics, LLC

Case Numbers – IPR2018-00555, IPR2018-00556, and IPR2018-00557. Petitions filed on February 5, 2018.

Case Subject Matter – Calibration of IQ balance in transceivers in wireless communications (OFDM, 802.11, Bluetooth, 3G, 4G, etc.).

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Covington & Burling LLP (Palo Alto, CA and Washington, DC)

Case – Phenix (sic) Longhorn, LLC v. Texas Instruments, Inc.

Case Number - Texas, ED (Marshall) 2:18-cv-00020. Complaint filed January 22, 2018.

Case Subject Matter – Circuit with non-volatile memory for gamma correction in a display screen.

Work Performed – Provided expert consulting services, wrote declaration for claim construction, expert reports, and was deposed twice.

Kirkland & Ellis LLP (Washington, DC) and Fish & Richardson P.C. (Washington, DC)

Case – BitMICRO, LLC v. Samsung Electronics Co., LTD., SK hynix Inc., Dell Inc., Lenovo Group Inc., HP Inc., ASUSTek Computer Inc., ASUS Computer International, ACER Inc., VAIO Corporation, and Transcosmos America Inc.

Case Number – ITC Investigation No. 337-TA-1097. Complaint filed January 8, 2018.

Case Subject Matter – Solid state storage drives (SSDs), stacked electronics components (3D packaging, solder balls, flip-chip, TSVs, etc.), and products.

Work Performed – Provided expert consulting services including direct witness statement, deposition, and testified at trial for pilot 100-day ITC proceeding.