

COMPACT
disc
DIGITAL DATA

ELECTRICAL ENGINEERING

DICTIONARY

CRCnetBASE 2000

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three bits, for a total of four bits (i.e., a nibble), with every row access.

The typical organization of a DRAM includes a buffer to store a row of bits inside the DRAM for column access. Additional timing signals allow repeated accesses to the buffer without a row-access time. *See also* [two-dimensional memory organization](#).

NIC *See* [network interface card](#).

Nichols chart in control systems, a plot showing magnitude contours and phase contours of the return transfer function referred to ordinates of logarithmic loop gain and abscissae of loop phase angle.

night vision *See* [scotopic vision](#).

NMD connector *See* [network measurement division connector](#).

NMI *See* [nonmaskable interrupt](#).

NMR nuclear magnetic resonance. *See* [magnetic resonance imaging](#).

NMOS *See* [n-channel MOSFET](#).

no fetch on write strategy in the write-through cache policy where a line is not fetched from the main memory into the cache on a cache miss if the reference is a write reference. Also called non-allocate on write, as space is not allocated in the cache on write misses.

no load tap changer device that provides for changing the tap position on a tapped transformer when the transformer is de-energized. Different taps provide a different turns ratio for the transformer.

no voltage holding coil a holding coil that keeps the main-line contactor closed on zero voltage conditions. DC motor controllers that contain this feature are used in places where the motor is vital to the operation of a process. These controllers can maintain

control to the motor under momentary line power losses, by using the CEMF of the coasting armature to keep power to the main-line coil/contacter. If power to the motor controller is not restored within a short period of time, the motor coasts to a speed where it can no longer keep the main-line contactor closed. At this point, the m-coil drops out to insure starting resistors are placed back in the circuit.

no-load test measurement of input parameters of an induction motor while running at nearly synchronous speed, with zero output on the shaft. This test is used to determine the magnetizing reactance of the motor equivalent circuit. *See also* [open-circuit test](#).

no-op a computer instruction that performs no operation. It can be used to reserve a location in memory or to put a delay between other instruction execution.

no-write allocate part of a write policy that stipulates that if a copy of data being updated are not found in one level of the memory hierarchy, space for a copy of the updated data will not be allocated in that level. Most frequently used in conjunction with a write-through policy.

nodal cell cell with a radius of up to 300 m. Typically an isolated cell acting as a high capacity network node. *See also* [cell](#).

nodal system a secondary system of equations using nodal voltages as variables.

node a symbol representing a physical connection between two electrical components in a circuit. *See also* [graph](#).

node analysis a circuit analysis technique in which KCL is used to determine the node voltages in a network.

noise (1) any undesired disturbance, whether originating from the transmission medium or the electronics of the receiver it-