LDD structure, the organic electroluminescence display which can obtain the good luminescence brightness of repeatability is obtained.
The sectional view of the 1st TFT of EL display of this invention is shown in <gestalt of the 2nd operation> drawing 4 .
[0048] The 1st TFT is an n-type channel and the point that the gestalt of this operation differs from the gestalt of the 1st operation is a point of having double-gate structure and offset structure, as shown in drawing 4 .
[0049] As shown in drawing 4 , genuineness field 13OS is formed in the upper part of the gate electrode 11, and the both sides of the gate electrode 11 genuineness or substantially among the active layers which consist of p-Si which the 1st TFT carried out the laminating of the gate electrode 11 and the gate dielectric film 12, and was prepared upwards. This field is the so-called offset field. Furthermore, it is source 13s [when the impurity of n molds, such as Lynn, is doped by the field shown with the slash of drawing], and drain 13d. In this way, the 1st TFT is equipped with the so-called offset structure equipped with the offset field.
[0050] Thus, when the 1st TFT which has an n-type channel is equipped with double-gate structure and offset structure, the organic electroluminescence display which electric-field mobility can make leakage current small highly, it is few, and dispersion in the drain current over a drain electrical potential difference can improve [repeatability] it homogeneity by being referred to as TFT equipped with p mold channel still like the gestalt of the 1st operation of the 2nd TFT as for the luminescence brightness of an organic EL device, and can obtain a good gradation display is obtained.
In the gestalt of <gestalt of the 3rd operation> book operation, the case where the so-called top gate type with which 1st and 2nd TFT(s) 30 and 40 prepared the gate electrode on the active layer 13 of TFT is used is shown. In addition, the case where it is TFT whose gate electrode 11 is double-gate structure is shown.
[0051] The sectional view of the 1st TFT is shown in drawing 5 (a), and the sectional view of the 2nd TFT is shown in drawing 5 (b).
[0052] As shown in drawing 5 (a), channel 13c superimposed on two gate electrodes 11 which formed the active layer which consists of p-Si on the insulating substrate 10, and were formed in the active layer 13 through gate dielectric film 12, and low concentration field 13LD which doped the low concentration impurity of n molds, such as Lynn, on the both sides are formed. Furthermore, source 13s [of a high concentration field] and drain 13d which doped the impurity of n mold is formed.
[0053] In this way, the 1st TFT for switching which has LDD structure and top gate structure is formed.
[0054] As shown in drawing 5 (b), an active layer 43 is formed on the insulating substrate 10 at formation and coincidence of the active layer 13 of the 1st TFT. The impurity of p molds, such as boron (B), is doped on channel 43c superimposed on two gate electrodes 41 formed through gate dielectric film 12 like the 1st TFT, and its both sides, and source 43s and drain 43d is formed in this active layer 43. It connects with the anode plate 61 of an organic EL device source 43s. In addition, since the structure of an organic EL device is the same as that of the case of the gestalt of the 1st operation, explanation is omitted.
[0055] In this way, the 2nd TFT equipped with p mold channel for an organic EL device drive is formed.
[0056] Thus, since electric-field mobility is high, writing is quick and there is little leakage current similarly [in the 1st and 2nd TFT(s) which have top gate structure / of having the above-mentioned bottom gate structure], the 1st TFT with a sufficient electrical-potential-difference maintenance property and the 2nd TFT with small dispersion in a current value with sufficient saturation characteristics can be obtained.
[0057] Therefore, the maintenance property of a video signal is good and can obtain the organic electroluminescence display which can obtain a good gradation display.
[0058] In addition, in the gestalt of each above-mentioned operation, although the 1st TFT explained double-gate structure, this invention is not limited to it and a gate electrode can apply it also in three or more multi-gate structures.
[0059] Moreover, in the gestalt of each above-mentioned operation, although the p-Si film was used as an active layer, the microcrystal silicon film or amorphous silicon may be used.
[0060] Furthermore, in the gestalt of each above-mentioned operation, although the organic electroluminescence display was explained, this invention is not limited to it, and can be applied also to inorganic EL display with which a luminous layer consists of an inorganic material, and the same effectiveness is acquired.
[0061]
[Effect of the Invention] Since EL display of this invention is equipped with high-speed writing, the 1st TFT with a sufficient maintenance property, and the 2nd TFT with a sufficient current controllability, it can obtain EL display in which a good gradation display is possible.

[Translation done.]

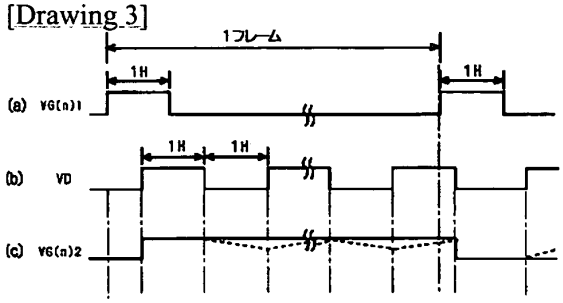
* NOTICES *

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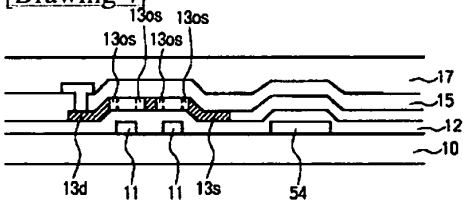
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

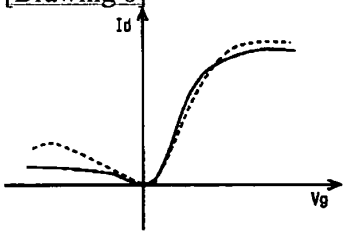
[Drawing 3]



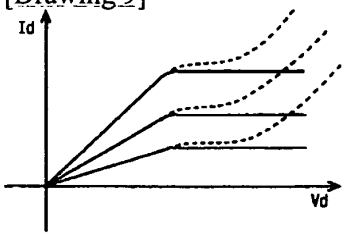
[Drawing 4]



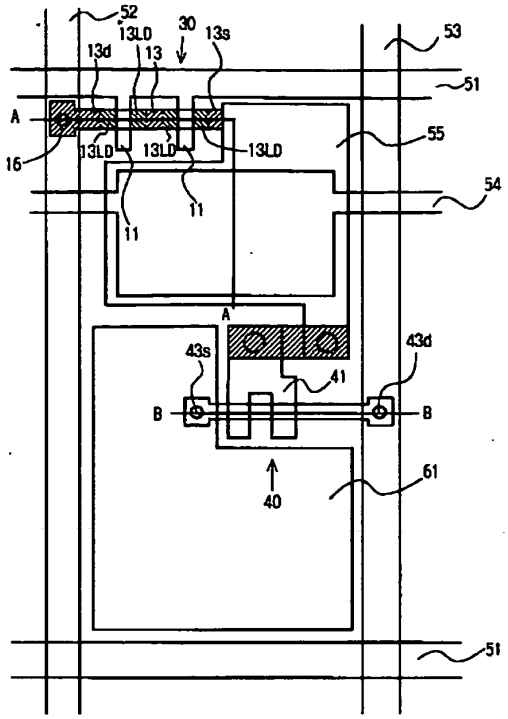
[Drawing 8]



[Drawing 9]

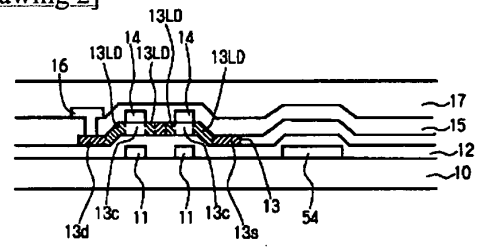


[Drawing 1]

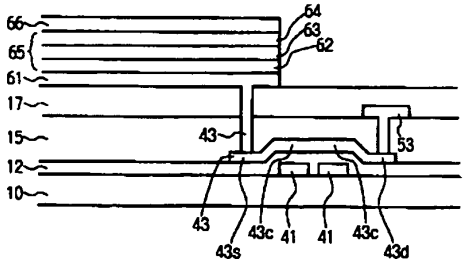


[Drawing 2]

(a)

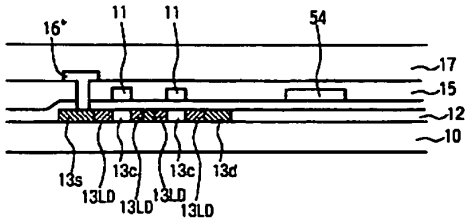


(b)

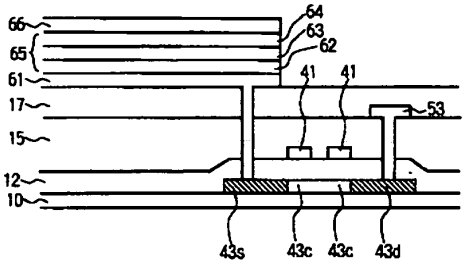


[Drawing 5]

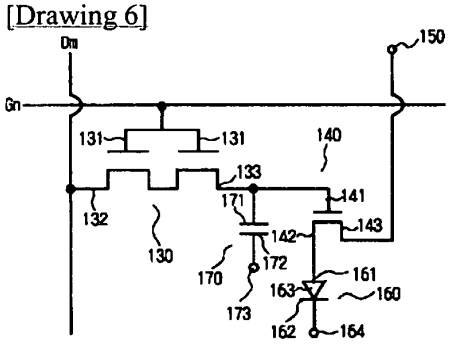
(a)



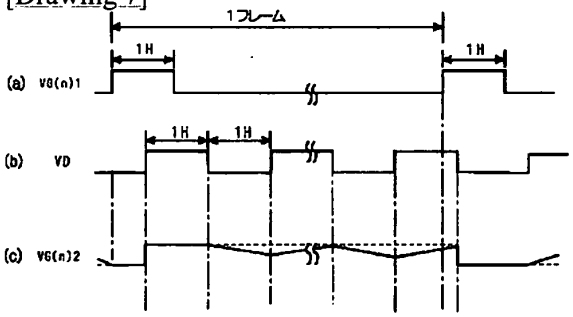
(b)



[Drawing 6]



[Drawing 7]



[Translation done.]

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Ｈ０５Ｂ	33/14		Ｈ０５Ｂ	33/14	Ａ	５Ｃ０９４
	33/26			33/26	Ｚ	

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(21)出願番号　特願平11－12280

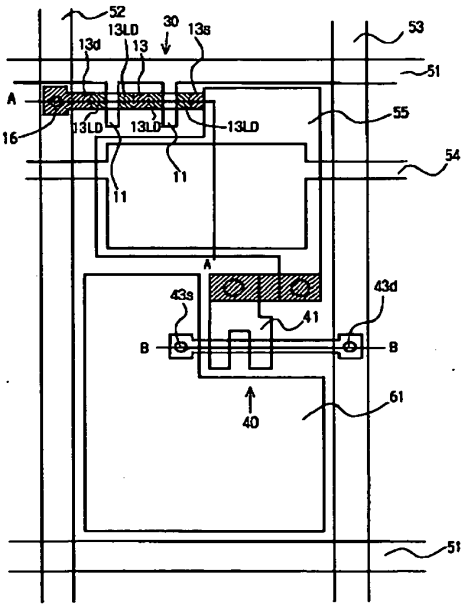
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5C094 AA02 AA25 AA53 BA03 BA29
CA25 GA10

(54)【発明の名称】　エレクトロルミネッセンス表示装置

(57)【要約】
【課題】　高速の書き込みと保持特性が良い第１のＴＦＴと、電流制御性が良い第２のＴＦＴとを備えているので、良好な階調表示が可能なＥＬ表示装置を提供する。
【解決手段】　スイッチング用の第１のＴＦＴ３０と、有機ＥＬ素子駆動用の第２のＴＦＴと、陽極６１、陰極６６及び該両電極の間に挟まれた発光素子層６５から成る有機ＥＬ素子６０とを備えた有機ＥＬ表示装置であって、第１のＴＦＴ３０はｎ型チャネルを有しＬＤＤ構造を備えており、第２のＴＦＴはｐ型チャネルを有している構造であるので、オン電流を高くリーク電流を小さくすることができるとともに、良好な階調表示を得ることができる。



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【特許請求の範囲】

【請求項１】　陽極と陰極との間に発光層を有するエレクトロルミネッセンス素子と、非単結晶半導体膜からなる能動層のソースが補助容量に、前記能動層のドレインがドレイン信号線に、前記能動層のチャネル上方に設けたゲート電極がゲート信号線にそれぞれ接続された第１の薄膜トランジスタと、非単結晶半導体膜からなる能動層のドレインが前記エレクトロルミネッセンス素子の駆動電源に、ゲートが前記第１の薄膜トランジスタのソースにそれぞれ接続された第２の薄膜トランジスタとを備えており、前記第１の薄膜トランジスタはｎ型チャネルを有するとともに、ＬＤＤ構造、マルチゲート構造またはオフセット構造のうちいずれか１つの構造を備えており、前記第２の薄膜トランジスタはｐ型チャネルを備えていることを特徴とするエレクトロルミネッセンス表示装置。

【請求項２】　陽極と陰極との間に発光層を有するエレクトロルミネッセンス素子と、非単結晶半導体膜からなる能動層のソースが補助容量に、前記能動層のドレインがドレイン信号線に、前記能動層のチャネル下方に設けたゲート電極がゲート信号線にそれぞれ接続された第１の薄膜トランジスタと、非単結晶半導体膜からなる能動層のドレインが前記エレクトロルミネッセンス素子の駆動電源に、ゲートが前記第１の薄膜トランジスタのソースにそれぞれ接続された第２の薄膜トランジスタとを備えており、前記第１の薄膜トランジスタはｎ型チャネルを有するとともに、ＬＤＤ構造、マルチゲート構造またはオフセット構造のうちいずれか１つの構造を備えており、前記第２の薄膜トランジスタはｐ型チャネルを備えていることを特徴とするエレクトロルミネッセンス表示装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、エレクトロルミネッセンス素子及び薄膜トランジスタを備えたエレクトロルミネッセンス表示装置に関する。

【０００２】

【従来の技術】近年、エレクトロルミネッセンス（Electro Luminescence：以下、「ＥＬ」と称する。）素子を用いたＥＬ表示装置が、ＣＲＴやＬＣＤに代わる表示装置として注目されており、例えば、そのＥＬ素子を駆動させるスイッチング素子として薄膜トランジスタ（Thin Film Transistor：以下、「ＴＦＴ」と称する。）を備えたＥＬ表示装置の研究開発も進められている。

【０００３】図６に、従来のＥＬ素子及びＴＦＴを備えたＥＬ表示装置の等価回路図を示す。

【０００４】同図は、第１のＴＦＴ１３０、第２のＴＦＴ１４０及び有機ＥＬ素子１６０からなるＥＬ表示装置の等価回路図であり、第ｎ行のゲート信号線Ｇｎと第ｍ列のドレイン信号線Ｄｍ付近を示している。

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【０００５】ゲート信号を供給するゲート信号線Ｇｎとドレイン信号を供給するドレイン信号線Ｄｍとが互いに直交しており、両信号線の交差点付近には、有機ＥＬ素子１６０及びこの有機ＥＬ素子１６０を駆動するＴＦＴ１３０，１４０が設けられている。

【０００６】スイッチング用のＴＦＴである第１のＴＦＴ１３０は、ゲート信号線Ｇｎに接続されておりゲート信号が供給されるゲート電極１３１と、ドレイン信号線Ｄｍに接続されておりドレイン信号が供給されるドレイン電極１３２と、第２のＴＦＴ１４０のゲート電極１４１に接続されているソース電極１３３とからなる。

【０００７】有機ＥＬ素子駆動用のＴＦＴである第２のＴＦＴ１４０は、第１のＴＦＴ１３０のソース電極１３３に接続されているゲート電極１４１と、有機ＥＬ素子１６０の陽極１６１に接続されたソース電極１４２と、有機ＥＬ素子１６０に供給される駆動電源１５０に接続されたドレイン電極１４３とから成る。

【０００８】また、有機ＥＬ素子１６０は、ソース電極１４２に接続された陽極１６１と、コモン電極１６４に接続された陰極１６２、及びこの陽極１６１と陰極１６２との間に挟まれた発光素子層１６３から成る。

【０００９】また、第１のＴＦＴ１３０のソース電極１３３と第２のＴＦＴ１４０のゲート電極１４１との間に一方の電極１７１が接続され他方の電極１７２がコモン電極１７３に接続された補助容量１７０を備えている。

【００１０】ここで、図６の等価回路図に示す回路の駆動方法について、図７に示す各信号のタイミングチャートに基づいて説明する。図７（ａ）は第ｎ行の第１のＴＦＴ１３０のゲート電極１３１に供給される信号ＶG(n)1の、同（ｂ）はドレイン信号線Ｄｍのドレイン信号ＶＤの、同（ｃ）は第ｎ行の第２のＴＦＴ１４０のゲート電極１４１に供給される信号ＶG(n)２のそれぞれのタイミングチャートを示す。

【００１１】図７（ａ）に示すゲート信号線Ｇｎからのゲート信号ＶG(n)1がゲート電極１３１に印加されると、第１のＴＦＴ１３０がオンになる。そのため、ドレイン信号線Ｄｍから図７（ｂ）に示すドレイン信号ＶＤがゲート電極１４１に供給され、ゲート電極１４１の電位がドレイン信号線Ｄｍの電位と同電位になる。そしてゲート電極１４１に供給された電流値に相当する電流が駆動電源１５０から有機ＥＬ素子１６０に供給される。それによって有機ＥＬ素子１６０は発光する。

【００１２】

【発明が解決しようとする課題】ここで、第１のＴＦＴ１３０がオンの期間には、ドレイン信号線Ｄｍの電位と同電位になるまで電流が流れてゲート電極１４１のゲート容量に電荷が蓄積される。そして、第１のＴＦＴ１３０がオフになると、そのゲート容量に蓄積された電荷はその状態を維持し、ゲート電位は、図７（ｃ）の点線で示すように保持される必要がある。

【００１３】しかしながら、上述の従来のＥＬ表示装置ではＴＦＴのオフ時にリーク電流が流れるため、ドレイン信号ＶＤが図６（ｂ）に示すように１水平期間（１Ｈ）毎に変化すると、ゲート電極１４１の電位ＶＧ(n)2は、図６（ｃ）の実線に示すように変化してしまい保持されない。

【００１４】即ち、図７（ｃ）の実線に示すように、（１）ドレイン信号線Ｄｍの電位がゲート電極１４１に供給された電位よりも低い場合には、第１のＴＦＴ１３０を介してドレイン信号線Ｄｍにリーク電流が流れてゲート電極１４１の電位が低下する。また、（２）ドレイン信号線Ｄｍの電位がゲート電極１４１に供給された電位よりも高い場合には第１のＴＦＴ１３０を介してゲート電極１４１にリーク電流が流れ、電荷が更に蓄積されてゲート電極１４１の電位が高くなる。

【００１５】そうすると、（１）の場合には、本来有機ＥＬ素子１６０に流れるべき電流よりも大きい電流が流れることになり有機ＥＬ素子の輝度が高くなってしまい、（２）の場合には、逆に輝度が低くなってしまう。

【００１６】これらいずれの場合にも、図７（ｃ）の点線で示すように、第１のＴＦＴ１３０のリーク電流が大きいと、発光する表示画素が発光すべき輝度で発光することが困難であるという欠点があった。

【００１７】また、第２のＴＦＴは、有機ＥＬを駆動する電源からの電流を、第２のＴＦＴのゲートに印加された電圧に応じて制御して有機ＥＬ素子に供給する機能を有しており、また、その能動層は、ゲートと重畳するチャネル領域は真性又は実質的に真性な領域と、その両側の領域に不純物をドーピングしたソース及びドレイン領域を備えている。

【００１８】ところが、図９の点線で示すように、第２のＴＦＴがｎ型チャネルの場合にはそのドレイン電流－ドレイン電圧（Ｉｄ－Ｖｄ）特性において、ドレイン電圧Ｖｄが増大しても一定のドレイン電流値Ｉｄになる、いわゆる飽和する領域が極めて狭い（飽和特性が悪い）ため、Ｖｄ値が大きくなると電流値Ｉｄが大きくなってしまい、電圧Ｖｄによって一定の電流が得られず電流の制御性が悪いという欠点があった。

【００１９】特にｎ型チャネルの多結晶シリコンＴＦＴでは結晶粒界が存在し、粒界にトラップされた電子によってポテンシャルバリアが形成され空乏層が広がる。このためドレイン電極エッジにおいて粒界に強い電界がかかり、これにより加速された電子が格子と衝突する衝突電離現象が発生するため、ドレイン電流は飽和せずに増加する。

【００２０】そこで本発明は、上記の従来の欠点に鑑みて為されたものであり、第１のＴＦＴ１３０のリーク電流を抑制して第２のＴＦＴ１４０のゲート電極１４１の電位を保持するとともに、第２のＴＦＴ１４０の電流制御性を良くすることにより、良好な階調表示が得られるＥＬ表示装置を提供することを目的とする。

【００２１】

【課題を解決するための手段】本発明のＥＬ表示装置は、陽極と陰極との間に発光層を有するエレクトロルミネッセンス素子と、非単結晶半導体膜からなる能動層のソースが補助容量に、前記能動層のドレインがドレイン信号線に、前記能動層のチャネル上方に設けたゲート電極がゲート信号線にそれぞれ接続された第１の薄膜トランジスタと、非単結晶半導体膜からなる能動層のドレインが前記エレクトロルミネッセンス素子の駆動電源に、ゲートが前記第１の薄膜トランジスタのソースにそれぞれ接続された第２の薄膜トランジスタとを備えており、前記第１の薄膜トランジスタはｎ型チャネルを有するとともに、ＬＤＤ構造、マルチゲート構造またはオフセット構造のうちいずれか１つの構造を備えており、前記第２の薄膜トランジスタはｐ型チャネルを備えているものである。

【００２２】また、本発明のＥＬ表示装置は、陽極と陰極との間に発光層を有するエレクトロルミネッセンス素子と、非単結晶半導体膜からなる能動層のソースが補助容量に、前記能動層のドレインがドレイン信号線に、前記能動層のチャネル下方に設けたゲート電極がゲート信号線にそれぞれ接続された第１の薄膜トランジスタと、非単結晶半導体膜からなる能動層のドレインが前記エレクトロルミネッセンス素子の駆動電源に、ゲートが前記第１の薄膜トランジスタのソースにそれぞれ接続された第２の薄膜トランジスタとを備えており、前記第１の薄膜トランジスタはｎ型チャネルを有するとともに、ＬＤＤ構造、マルチゲート構造またはオフセット構造のうちいずれか１つの構造を備えており、前記第２の薄膜トランジスタはｐ型チャネルを備えているものである。

【００２３】

【発明の実施の形態】本発明のＥＬ表示装置について以下に説明する。

＜第１の実施の形態＞図１に本発明を有機ＥＬ表示装置に適用した場合の１表示画素を示す平面図を示し、図２（ａ）に図１中のＡ－Ａ線に沿った断面図を示し、図２（ｂ）に図１中のＢ－Ｂ線に沿った断面図を示す。

【００２４】図１に示すように、ゲート信号線５１とドレイン信号線５２とに囲まれた領域に表示画素が形成されている。両信号線の交点付近には第１のＴＦＴ３０が備えられており、そのＴＦＴ３０のソース１３ｓは後述の補助容量電極線５４との間で補助容量をなす容量電極５５を兼ねるとともに、第２のＴＦＴ４０のゲート４１に接続されている。第２のＴＦＴのソース４３ｓは有機ＥＬの陽極６１に接続され、他方のドレイン４３ｄは有機ＥＬ素子を駆動する駆動電源線５３に接続されている。

【００２５】また、ＴＦＴの付近には、ゲート信号線５１と並行に補助容量電極線５４が配置されている。この

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補助容量電極線５４はクロム等から成っており、ゲート絶縁膜１２を介してＴＦＴのソース１３ｓと接続された容量電極５５との間で電荷を蓄積して補助容量を成している。この補助容量は、第２のＴＦＴ４０のゲート電極４１に印加される電圧を保持するために設けられている。

【００２６】図２に示すように、有機ＥＬ表示装置は、ガラスや合成樹脂などから成る基板又は導電性を有する基板あるいは半導体基板等の基板１０上に、ＴＦＴ及び有機ＥＬ素子を順に積層形成して成る。ただし、基板１０として導電性を有する基板及び半導体基板を用いる場合には、これらの基板１０上にSiO_2やＳｉＮなどの絶縁膜を形成した上にＴＦＴ及び有機ＥＬ表示装置を形成する。

【００２７】本実施の形態においては、第１及び第２のＴＦＴ３０，４０ともに、ゲート電極を能動層１３の下方に設けたいわゆるボトムゲート型のＴＦＴであり、能動層として多結晶シリコン（Poly-Silicon、以下、「ｐ－Ｓｉ」と称する。）膜を用いた場合を示す。またゲート電極１１がダブルゲート構造であるＴＦＴの場合を示す。

【００２８】まず、スイッチング用のＴＦＴである第１のＴＦＴ３０について説明する。

【００２９】図２（ａ）に示すように、石英ガラス、無アルカリガラス等からなる絶縁性基板１０上に、クロム（Ｃｒ）、モリブデン（Ｍｏ）などの高融点金属からなるゲート電極１１を兼ねたゲート信号線５１及びＡｌから成るドレイン信号線５２を形成する。そして有機ＥＬ素子の駆動電源であり駆動電源に接続されＡｌから成る駆動電源線５３を形成する。

【００３０】続いて、ゲート絶縁膜１２、及びｐ－Ｓｉ膜からなる能動層１３を順に形成する。

【００３１】その能動層１３には、いわゆるＬＤＤ（Lightly Doped Drain）構造が形成されている。即ち、ゲート電極１１上のチャネル１３ｃ上のストッパ絶縁膜１４をマスクにしてイオンドーピングし、更にゲート電極１１及びその両側のゲート電極１１から一定の距離までをレジストにてカバーしイオンドーピングしてゲート電極１１の両側に低濃度領域１３ＬＤ（図中左上方から右下方に向かう斜線で表示）とその外側に高濃度領域（図中右上方から左下方に向かう斜線で表示）のソース１３ｓ及びドレイン１３ｄが設けられている。

【００３２】そして、ゲート絶縁膜１２、能動層１３及びストッパ絶縁膜１４上の全面に、SiO_2膜、ＳｉＮ膜及びSiO_2膜の順に積層された層間絶縁膜１５を形成し、ドレイン１３ｄに対応して設けたコンタクトホールにＡｌ等の金属を充填してドレイン電極１６を形成する。更に全面に例えば有機樹脂から成り表面を平坦にする平坦化絶縁膜１７を形成する。

【００３３】次に、有機ＥＬ素子の駆動用のＴＦＴである第２のＴＦＴ４０について説明する。

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【００３４】図２（ｂ）に示すように、石英ガラス、無アルカリガラス等からなる絶縁性基板１０上に、Ｃｒ、Ｍｏなどの高融点金属からなるゲート電極４１を形成する。

【００３５】ゲート絶縁膜１２、及びｐ－Ｓｉ膜からなる能動層４３を順に形成する。

【００３６】その能動層４３には、ゲート電極４１上方に真性又は実質的に真性であるチャネル４３ｃと、このチャネル４３ｃの両側に、その両側をレジストにてカバーしてイオンドーピングしてソース１３ｓ及びドレイン１３ｄが設けられている。

【００３７】そして、ゲート絶縁膜１２及び能動層４３上の全面に、SiO_2膜、ＳｉＮ膜及びSiO_2膜の順に積層された層間絶縁膜１５を形成し、ドレイン４３ｄに対応して設けたコンタクトホールにＡｌ等の金属を充填して駆動電源５０に接続された駆動電源線５３を形成する。更に全面に例えば有機樹脂から成り表面を平坦にする平坦化絶縁膜１７を形成する。そして、その平坦化絶縁膜１７のソース４３ｓに対応した位置にコンタクトホールを形成し、このコンタクトホールを介してソース１３ｓとコンタクトしたＩＴＯから成る透明電極、即ち有機ＥＬ素子の陽極６１を平坦化絶縁膜１７上に形成する。

【００３８】有機ＥＬ素子６０は、一般的な構造であり、ＩＴＯ（Indium Thin Oxide）等の透明電極から成る陽極６１、ＭＴＤＡＴＡ（4,4-bis(3-methy lphenylphenylamino)biphenyl）から成る第１ホール輸送層６２、ＴＰＤ（4,4,4-tris(3-methylphenylphenylamino)triphenylanine）からなる第２ホール輸送層６３、キナクリドン（Quinacridone）誘導体を含むＢｅｂｑ２（10-ベンゾ〔ｈ〕キノリノール－ベリリウム錯体）から成る発光層６４及びＢｅｂｑ2から成る電子輸送層からなる発光素子層６５、マグネシウム・インジウム合金から成る陰極６６がこの順番で積層形成された構造である。

【００３９】また有機ＥＬ素子は、陽極から注入されたホールと、陰極から注入された電子とが発光層の内部で再結合し、発光層を形成する有機分子を励起して励起子が生じる。この励起子が放射失活する過程で発光層から光が放たれ、この光が透明な陽極から透明絶縁基板を介して外部へ放出されて発光する。

【００４０】図３に各信号のタイミングチャートを示す。なお、本実施の形態における有機ＥＬ表示装置の等価回路は前述の図６と同じである。

【００４１】図３において、図（ａ）は第ｎ行の第１のＴＦＴのゲート電極に供給される信号VG(n)1の、同（ｂ）は第ｍ列のドレイン信号ＶＤの、同（ｃ）は第ｎ行の第２のＴＦＴのゲート電極の信号VG(n)2のそれぞれのタイミングチャートを示す。

【００４２】図３（ａ）に示すようにゲート信号線Ｇｎ

に接続されたゲート１１にゲート信号が供給されると第１のＴＦＴ３０が１水平期間（１Ｈ）オン状態を保ちその後オフになる。そのオン状態になったとき図３（ｃ）に示すようにドレイン信号線Ｄｍから図３（ｂ）に示すドレイン信号がソース４３ｓを介してゲート電極４１に供給され、そのゲート電極４１の電位がドレイン信号線Ｄｍの電位と同電位になる。こうしてゲート電極４１に電位が供給されると第２のＴＦＴ４０がオン状態となり、ゲート電極４１の電流値に相当する電流が駆動電源５０からドレイン４３ｄ及びソース４３ｓを介して有機ＥＬ素子６０の陽極６１に供給される。そうして有機ＥＬ素子６０が発光する。

【００４３】このように構成された表示画素が基板１０上にマトリクス状に配置されることにより、有機ＥＬ表示装置が形成される。

【００４４】以上のように、本発明によれば、第１のＴＦＴ３０がｎ型を呈する不純物をドーピングしたソース及びドレインを備えた能動層１３を備えたＬＤＤ構造であるｎ型チャネルＴＦＴであるので、電界移動度が高く第１のＴＦＴ３０のリーク電流を抑制することができる。即ち高速で書き込みができるとともに電圧保持特性が良いため、図３（ｂ）に示すようにドレイン信号が１Ｈごとに変化する信号に追従して書き込みをすることができ、図３（ｃ）の点線で示す従来のようにゲート電極４１の電位が変化することなく、実線で示したように電位を保持することができるとともに、更に図８中の実線で示すように高いオン電流を得ることができるため、発光すべき電流を低下させることなく安定して有機ＥＬ素子に供給することができる。

【００４５】また、第２のＴＦＴ４０がｐ型を呈する不純物をドーピングしたソース及びドレインを備えた能動層を備えたｐ型チャネルＴＦＴであるので、図９中に実線で示すように、Ｉｄ－Ｖｄ特性において飽和する領域を広くすることができるため、Ｖｄに応じてＩｄが変化しにくくなる、即ちドレイン電圧の変化に応じたドレイン電流値のばらつきが少なくなるので有機ＥＬ素子の発光輝度が再現性良く均一にすることができることから良好な階調表示を容易に得ることができる。

【００４６】特に多結晶シリコンＴＦＴでは、従来の技術の欄で説明したように、結晶粒界が存在し、粒界にトラップされた電子によってポテンシャルバリアが形成され空乏層が広がる。このためドレイン電極エッジにおいて粒界に強い電界がかかり、これにより加速された電子が格子と衝突する衝突電離現象が発生するが、その現象はｎ型チャネルＴＦＴの場合に比べｐ型チャネルの場合の方が著しく小さいことから、ドレイン電流は飽和する領域を示し良好な飽和特性を得ることができることから、第２のＴＦＴとしてｐ型チャネルＴＦＴを用いる。

【００４７】以上のように、ｎ型チャネルを有しＬＤＤ構造を備えた第１のＴＦＴ及びｐ型チャネルを有する第２のＴＦＴを備えたことにより、高速の書き込みが可能でリーク電流を低減できるとともに、再現性の良い発光輝度を得ることができる有機ＥＬ表示装置が得られる。

＜第２の実施の形態＞図４に本発明のＥＬ表示装置の第１のＴＦＴの断面図を示す。

【００４８】本実施の形態が第１の実施の形態と異なる点は、図４に示すように、第１のＴＦＴがｎ型チャネルであってダブルゲート構造及びオフセット構造を有する点である。

【００４９】図４に示すように、第１のＴＦＴは、ゲート電極１１、ゲート絶縁膜１２を積層した上に設けたｐ－Ｓｉから成る能動層のうち、ゲート電極１１の上方及びゲート電極１１の両側に、真性又は実質的に真性な領域１３ＯＳが形成されている。この領域がいわゆるオフセット領域である。更に図の斜線で示す領域にはリン等のｎ型の不純物がドーピングされているソース１３ｓ及びドレイン１３ｄである。こうして、第１のＴＦＴはオフセット領域を備えたいわゆるオフセット構造を備えている。

【００５０】このように、ｎ型チャネルを有する第１のＴＦＴがダブルゲート構造及びオフセット構造とを備えることにより、電界移動度が高くリーク電流を小さくでき、更に第２のＴＦＴを第１の実施の形態と同様にｐ型チャネルを備えたＴＦＴとすることによりドレイン電圧に対するドレイン電流のばらつきが少なく有機ＥＬ素子の発光輝度が再現性良く均一にすることができ良好な階調表示を得ることができる有機ＥＬ表示装置が得られる。

＜第３の実施の形態＞本実施の形態においては、第１及び第２のＴＦＴ３０，４０ともに、ゲート電極を能動層１３の上に設けたいわゆるトップゲート型のＴＦＴを用いた場合を示す。なお、ゲート電極１１がダブルゲート構造であるＴＦＴの場合を示す。

【００５１】図５（ａ）に第１のＴＦＴの断面図を示し、図５（ｂ）に第２のＴＦＴの断面図を示す。

【００５２】図５（ａ）に示すように、絶縁性基板１０上に、ｐ－Ｓｉから成る能動層を形成し、その能動層１３には、ゲート絶縁膜１２を介して形成した２つのゲート電極１１と重畳するチャネル１３ｃと、その両側にリン等のｎ型の低濃度不純物をドーピングした低濃度領域１３ＬＤを形成している。更に、ｎ型の不純物をドーピングした高濃度領域のソース１３ｓ及びドレイン１３ｄを形成する。

【００５３】こうして、ＬＤＤ構造及びトップゲート構造を有するスイッチング用の第１のＴＦＴが形成される。

【００５４】図５（ｂ）に示すように、絶縁性基板１０上に、第１のＴＦＴの能動層１３の形成と同時に能動層４３を形成する。この能動層４３には、第１のＴＦＴと同様に、ゲート絶縁膜１２を介して形成した２つのゲー

ト電極４１と重畳するチャネル４３ｃと、その両側にボロン（Ｂ）等のｐ型の不純物をドーピングしてソース４３ｓ及びドレイン４３ｄを形成する。ソース４３ｓは有機ＥＬ素子の陽極６１に接続されている。なお、有機ＥＬ素子の構造は第１の実施の形態の場合と同様であるので説明は省略する。

【００５５】こうして、ｐ型チャネルを備えた有機ＥＬ素子駆動用の第２のＴＦＴが形成される。

【００５６】このように、トップゲート構造を有する第１及び第２のＴＦＴの場合も、前述のボトムゲート構造を有する場合と同様に、電界移動度が高いので書き込みが速くリーク電流が少ないので電圧保持特性が良い第１のＴＦＴ、及び飽和特性がよく電流値のばらつきの小さい第２のＴＦＴを得ることができる。

【００５７】そのため、映像信号の保持特性が良く、良好な階調表示を得ることができる有機ＥＬ表示装置を得ることができる。

【００５８】なお、上述の各実施の形態においては、第１のＴＦＴはダブルゲート構造について説明したが、本発明はそれに限定されるものではなく、ゲート電極が３つ以上のマルチゲート構造においても適用が可能である。

【００５９】また、上述の各実施の形態においては、能動層としてｐ－Ｓｉ膜を用いたが、微結晶シリコン膜又は非晶質シリコンを用いても良い。

【００６０】更に、上述の各実施の形態においては、有機ＥＬ表示装置について説明したが、本発明はそれに限定されるものではなく、発光層が無機材料から成る無機ＥＬ表示装置にも適用が可能であり、同様の効果が得られる。

【００６１】

【発明の効果】本発明のＥＬ表示装置は、高速の書き込みと保持特性が良い第１のＴＦＴと、電流制御性が良い第２のＴＦＴとを備えているので、良好な階調表示が可能なＥＬ表示装置を得ることができる。

【図面の簡単な説明】

【図１】本発明のＥＬ表示装置の平面図である。

【図２】本発明のＥＬ表示装置の断面図である。

【図３】本発明のＥＬ表示装置の各信号のタイミングチャートである。

【図４】本発明のＥＬ表示装置の断面図である。

【図５】本発明のＥＬ表示装置の断面図である。

【図６】ＥＬ表示装置の等価回路図である。

【図７】従来のＥＬ表示装置の各信号のタイミングチャートである。

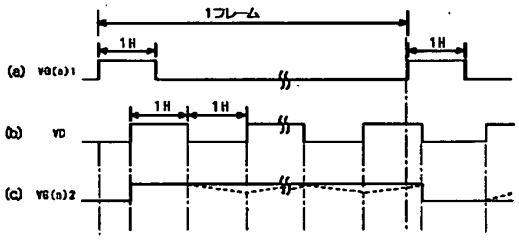
【図８】ＴＦＴの特性図である。

【図９】ＴＦＴの特性図である。

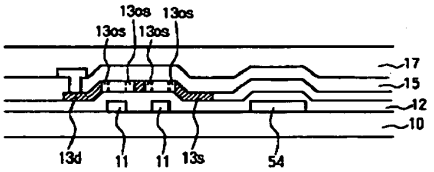
【符号の説明】

１１，４１	ゲート
１３ｓ、４３ｓ	ソース
１３ｄ、４３ｄ	ドレイン
１３ｃ、４３ｃ	チャネル
１３ｓ、４３ｓ	ＬＤＤ領域
３０	第１のＴＦＴ
４０	第２のＴＦＴ
５０	駆動電源
６０	有機ＥＬ素子

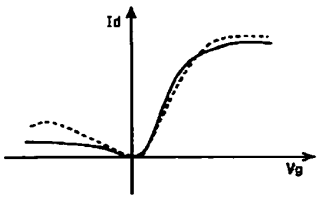
【図３】



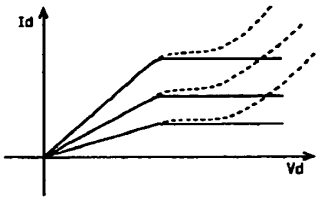
【図４】



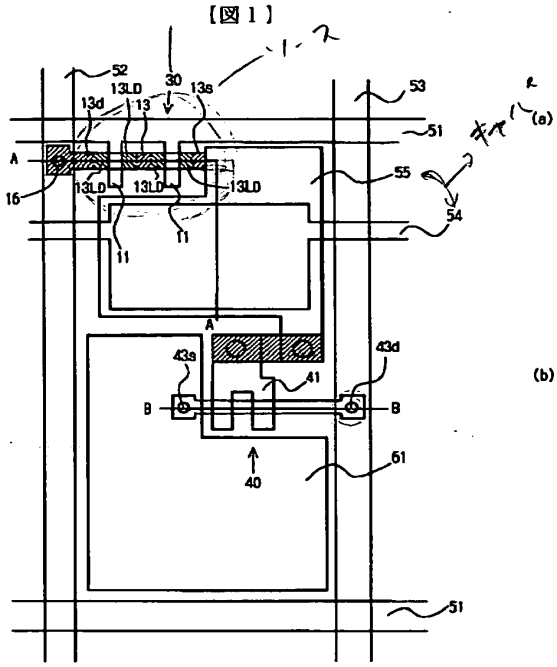
【図８】



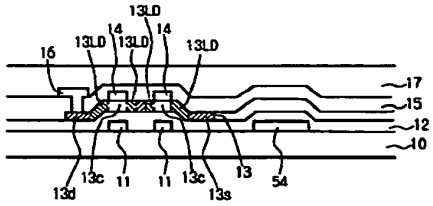
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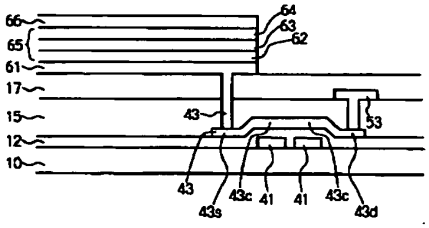


【図１】

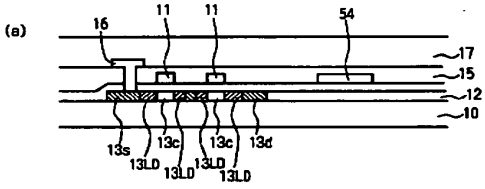

TFT
1-2
52
30
13s
53
13LD
13d
13
51
A
16
13LD
13LD
13LD
55
54
11
11
A
43s
43d
41
B
B
61
40
51

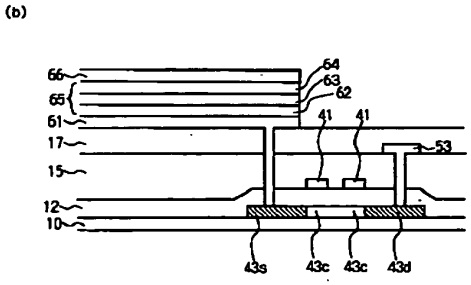
【図２】


13LD
14
13LD
14
13LD
13LD
16
17
15
12
10
13d
13c
11
11
13c
13s
13
54

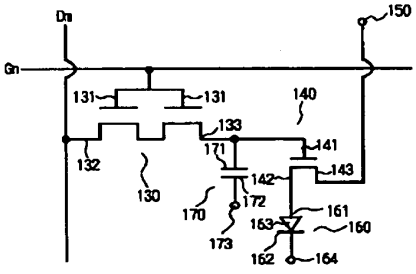

(b)
66
65
61
17
15
12
10
64
63
62
43
53
43
43s
43c
41
41
43c
43d

【図５】

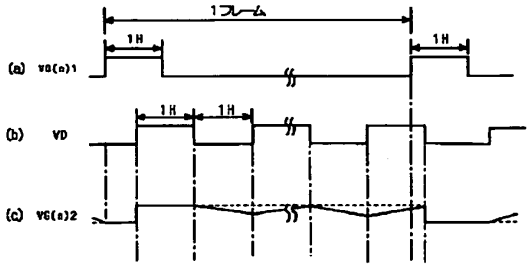

(a)
16
11
11
54
17
15
12
10
13s
13LD
13c
13LD
13c
13LD
13d
13LD


(b)
66
65
61
17
15
12
10
64
63
62
41
41
53
43s
43c
43c
43d

【図６】


Dn
150
Gn
131
131
140
133
171
141
132
130
142
143
170
172
161
163
160
173
162
164

【図７】


1フレーム
1H
1H
(a) VG(n)1
1H
1H
(b) VD
(c) VG(n)2

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PATENT ABSTRACTS OF JAPAN

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H01L 21/336
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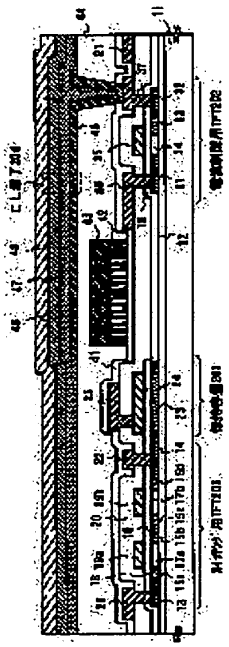
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FUKUNAGA KENJI

(30)Priority
Priority number : 11119466 Priority date : 27.04.1999 Priority country : JP

(54) ELECTRONIC DEVICE AND ELECTRIC APPLIANCE

(57)Abstract:
PROBLEM TO BE SOLVED: To obtain an EL display device with high operation performance and reliability.
SOLUTION: LDD areas 15a-15d of TFT 201 for switching formed in a pixel are formed so as not to overlap gate electrodes 19a, 19b, and structured placing importance on decrease in an off-current value. Moreover, an LDD area 33 of TFT 202 for current control is formed to partly overlap a gate electrode 35, and is structured placing importance on prevention of hot carrier injection and decrease in the off-current value. Thus, the operation performance and reliability are improved by properly structuring the TFT according to required functions.



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CLAIMS

[Claim(s)]
[Claim 1] In the electronic instrument which has the EL element connected to the 1st TFT, 2nd TFT, and said 2nd TFT in 1 pixel the LDD field of said 1st TFT It is the electronic instrument characterized by being formed so that it may not lap with the gate electrode of this 1st TFT on both sides of gate dielectric film, and forming the LDD field of said 2nd TFT so that a part or all may lap with the gate electrode of this 2nd TFT on both sides of gate dielectric film.
[Claim 2] In the electronic instrument which has the EL element connected to the 1st TFT, 2nd TFT, and said 2nd TFT in 1 pixel the LDD field of said 1st TFT It is the electronic instrument characterized by being formed so that a part may lap with the gate electrode of this 1st TFT on both sides of gate dielectric film, and forming the LDD field of said 2nd TFT so that a part or all may lap with the gate electrode of this 2nd TFT on both sides of gate dielectric film.
[Claim 3] In the electronic instrument which contains the pixel section and the drive circuit section on the same insulator said drive circuit section It has the n channel mold TFT formed so that some or all of a LDD field might lap with a gate electrode on both sides of gate dielectric film. Said pixel section It has a pixel containing the EL element connected to the 1st TFT, 2nd TFT, and said 2nd TFT. The LDD field of said 1st TFT It is the electronic instrument characterized by being formed so that it may not lap with the gate electrode of this 1st TFT on both sides of gate dielectric film, and forming the LDD field of said 2nd TFT so that a part or all may lap with the gate electrode of this 2nd TFT on both sides of gate dielectric film.
[Claim 4] In the electronic instrument which contains the pixel section and the drive circuit section on the same insulator said drive circuit section It has the n channel mold TFT formed so that some or all of a LDD field might lap with a gate electrode on both sides of gate dielectric film. Said pixel section It has a pixel containing the EL element connected to the 1st TFT, 2nd TFT, and said 2nd TFT. The LDD field of said 1st TFT It is the electronic instrument characterized by being formed so that a part may lap with the gate electrode of this 1st TFT on both sides of gate dielectric film, and forming the LDD field of said 2nd TFT so that a part or all may lap with the gate electrode of this 2nd TFT on both sides of gate dielectric film.
[Claim 5] It is the electronic instrument which said 1st TFT is a component for switching, and is characterized by said 2nd TFT being a component for current control in any 1 of claim 1 thru/or claims 4.
[Claim 6] The electronic instrument characterized by containing n mold impurity element by one 2 to 10 times the concentration of this compared with the LDD field of said 1st TFT in the LDD field of said 2nd TFT in any 1 of claim 1 thru/or claims 4.
[Claim 7] The electronic instrument characterized by containing n mold impurity element in the LDD field of said 2nd TFT by the density range of 2x1016 - 5x1019 atoms/cm3, and containing n mold impurity element in the LDD field of said 1st TFT in any 1 of claim 1 thru/or claims 4 by the density range of 1x1016 - 5x1018 atoms/cm3.
[Claim 8] It is the electronic instrument characterized by forming said EL element on the wrap flattening film in said the 1st TFT and said 2nd TFT in any 1 of claim 1 thru/or claims 4.
[Claim 9] The electric appliance characterized by using an electronic instrument according to claim 1 to 8 for a display.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] The invention in this application relates to the electronic instrument which made the semiconductor device (component using a semi-conductor thin film) on the substrate, and was formed, and the electric appliance using the electronic instrument as a display. Especially this invention is a technique with effective carrying out to EL (electroluminescence) display as an electronic instrument.
[0002]
[Description of the Prior Art] In recent years, on the substrate, the technique which forms TFT progresses sharply and application development to a active-matrix mold display is furthered. Since electric field effect mobility (it is also called mobility) is higher than TFT which used the conventional amorphous silicon film, high-speed operation is possible for especially TFT using the polish recon film. Therefore, it is possible to perform control of a pixel in the drive circuit besides a substrate conventionally in the drive circuit formed on the same substrate (insulator) as a pixel.
[0003] Such a active-matrix mold display attracts attention noting that various advantages, such as reduction of a manufacturing cost, a miniaturization of a display, a rise of the yield, and reduction of a throughput, are acquired by making various circuits and components on the same substrate.
[0004] However, on the substrate of a active-matrix mold display, the circuit and the component section which have various functions are formed. Therefore, in forming a circuit or a component by TFT, the engine performance of TFT which each circuit or component needs also differs. For example, the shift register which forms a timing signal is asked for TFT with an early working speed, and the switching element for a charge storage is asked for TFT of an OFF state current value (drain current value which flows when TFT is in off actuation) low enough.
[0005] In such a case, only by TFT of the same structure, it becomes difficult to secure the engine performance for which all circuits or components ask, and when raising the engine performance of a active-matrix mold display, it becomes serious evil.
[0006]
[Problem(s) to be Solved by the Invention] This invention makes it a technical problem to offer the engine performance of operation and a reliable electronic instrument using TFT of suitable structure according to the engine performance for which the circuit or component formed by TFT in the electronic instrument of the active-matrix mold which has the pixel section and the drive circuit section on the same insulator asks.
[0007] And let it be a technical problem to raise the quality of electronic equipment (electric appliance) using it as a display (display for a display) by raising the image quality of an electronic instrument (especially active-matrix mold EL indicating equipment).
[0008]
[Means for Solving the Problem] In order to solve the above-mentioned trouble, in this invention, it is making to assign TFT of the optimal structure into main point in view of the function for which the component contained in each pixel of EL display asks. That is, TFT of different structure in the same pixel will exist.
[0009] The components (component for switching etc.) which specifically make it to make an OFF state current value low enough a problem of the utmost importance have TFT structure more desirable than a working speed with emphasis on reducing an OFF state current value. Moreover, the components (component for current control etc.) which make it a problem of the utmost importance to pass a high current have TFT structure more desirable than reducing an OFF state current value with emphasis on controlling degradation by the hot carrier impregnation which poses passing a high current, and it and a problem remarkable in coincidence.
[0010] This invention enables improvement in the engine performance of EL display of operation, and improvement in

dependability by using the above TFT(s) properly on the same insulator. In addition, the thought of this invention is not what was restricted to the pixel section, and there is the description also in the point of attaining optimization of TFT structure including the drive circuit section which drives the pixel section and its pixel section.
[0011]
[Embodiment of the Invention] The gestalt of operation of this invention is explained using drawing 1 and drawing 2 . It is the sectional view of the pixel of EL display which is this invention which was shown in drawing 1 , and drawing 2 (A) is the plan and drawing 2 (B) is the circuitry. Two or more arrays of such a pixel are carried out in fact at the shape of a matrix, and the pixel section (image display section) is formed.
[0012] In addition, the sectional view of drawing 1 shows the cutting plane cut by A-A' in the plan shown in drawing 2 (A). Since the common sign is used by drawing 1 and drawing 2 here, it is good to refer to both drawings suitably. Moreover, both are the same structures although two pixels are illustrated in the plan of drawing 2 .
[0013] In drawing 1 , 11 is a substrate and 12 is the substrate film (insulator). As a substrate 11, a glass substrate, a crystallized glass substrate, a quartz substrate, a silicon substrate, a ceramic substrate, a metal substrate, or a plastic plate (plastic film is also included) can be used.
[0014] Moreover, although especially the substrate film 12 is effective when using the substrate containing movable ion, and the substrate which has conductivity, you may not prepare in a quartz substrate. What is necessary is just to prepare the insulator layer containing silicon (silicon) as substrate film 12. In addition, in this specification, "the insulator layer containing silicon" points out the insulator layer which specifically contains silicon, such as oxidation silicon film, a silicon nitride film, or nitriding oxidation silicon film (shown by SiOxNy), oxygen, or nitrogen at a predetermined rate.
[0015] Here, two TFT(s) are formed in a pixel. TFT (henceforth TFT for switching) on which 201 functions as a switching element, and 202 are TFT(s) (henceforth TFT for current control) which control the amount of currents passed to an EL element, and are formed by both with the n channel mold TFT.
[0016] TFT201 for switching has the drain wiring 22 in a barrier layer including the source field 13, the drain field 14, the LDD fields 15a-15d, the high concentration impurity range 16, and the channel formation fields 17a and 17b, gate dielectric film 18, gate electrode 19a, gate electrode 19b, the 1st interlayer insulation film 20, and source wiring 21 list, and is formed in them. In addition, as shown in drawing 2 , the gate electrodes 19a and 19b have double-gate structure which used the same gate wiring 211 as the trunk.
[0017] A barrier layer is formed by the semi-conductor film including the crystal structure. That is, the single crystal semiconductor film is sufficient and the polycrystal semi-conductor film and the microcrystal semi-conductor film are sufficient. Moreover, what is necessary is just to form gate dielectric film 18 by the insulator layer containing silicon. Moreover, all electric conduction film can be used as a gate electrode, source wiring, or drain wiring.
[0018] Moreover, retention volume (storage capacitor) 203 is connected to TFT201 for switching (refer to drawing 2). Retention volume 203 is formed with the semiconductor region 23 for capacity formation, the gate dielectric film 18 (in the field which forms retention volume 203, it functions as a dielectric for capacity formation), and the electrode 24 for capacity formation which were electrically connected with the drain field 14. In addition, the connection wiring 25 is wiring for giving fixed potential (here touch-down potential) to the electrode 24 for capacity formation, is formed in source wiring 21, the drain wiring 22, and coincidence, and is connected to the current supply source line 212.
[0019] At this time, in TFT201 for switching, the LDD fields 15a-15d are formed so that it may not lap with gate electrode 19a and gate electrode 19b on both sides of gate dielectric film 18. Generally such structure is called LDD structure.
[0020] TFT201 for switching accumulates the charge corresponding to a video signal (signal containing image information) to retention volume 203 at the time of selection. And since the charge must always be held at the time of un-choosing, the charge leakage by the OFF state current value must be prevented as much as possible. In such semantics, it must design that TFT201 for switching reduces an OFF state current value as a problem of the utmost importance.
[0021] In addition, it is still more desirable to prepare an offset field (field where it becomes in the semi-conductor layer of the same presentation as a channel formation field, and gate voltage is not impressed) between a channel formation field and a LDD field, when lowering an OFF state current value. Moreover, in the case of the multi-gate structure of having two or more gate electrodes, the high concentration impurity range prepared between channel formation fields is effective for reduction of an OFF state current value. In addition, although it is desirable to consider as multi-gate structure like this example, it can also consider as single gate structure.
[0022] Next, TFT202 for current control has the drain wiring 37 in a barrier layer including the source field 31, the drain field 32, the LDD field 33, and the channel formation field 34, gate dielectric film 18, the gate electrode 35, the 1st interlayer insulation film 20, and source wiring 36 list, and is formed in them. In addition, although the gate electrode 35

has single gate structure, you may be multi-gate structure.
[0023] As shown in drawing 2 , the gate electrode 35 is electrically connected through the drain field 14 of TFT201 for switching, and the drain wiring (said to be connection wiring) 22. Moreover, it is uniting with the connection wiring 25 and source wiring 36 is similarly connected to the current supply source line 212.
[0024] The description of this TFT202 for current control is the point of having the field where the LDD field 33 was formed between the drain field 32 and the channel formation field 34, and the LDD field 33 has lapped with the gate electrode 35 on both sides of gate dielectric film 18, and the field with which it has not lapped.
[0025] TFT202 for current control controls the amount of supply, and enables a gradation display at the same time it supplies the current for making EL element 204 emit light. Therefore, it is necessary to take the cure against degradation by hot carrier impregnation so that it may not deteriorate, even if it passes a high current. Moreover, in case black is displayed, TFT202 for current control is made into the OFF state, but in that case, if an OFF state current value is high, a beautiful black display will become impossible and the fall of contrast will be caused. Therefore, it is necessary to also hold down an OFF state current value.
[0026] About degradation by hot carrier impregnation, it is known that the structure with which the LDD field lapped to the gate electrode is very effective. However, since an OFF state current value will increase if the whole LDD field is kept in a gate electrode in piles, this invention persons have solved the cure against a hot carrier, and the cure against an OFF state current value to coincidence according to the new structure of preparing the LDD field which does not lap with a gate electrode.
[0027] What is necessary is just to set to 0.1-3 micrometers (preferably 0.3-1.5 micrometers) the die length of the LDD field which lapped with the gate electrode at this time. If too long, parasitic capacitance is enlarged, and if too short, the effectiveness of preventing a hot carrier will become weak. Moreover, what is necessary is just to set to 1.0-3.5 micrometers (preferably 1.5-2.0 micrometers) the die length of the LDD field which does not lap with a gate electrode. When too long, it becomes impossible to pass sufficient current, and if too short, the effectiveness of reducing an OFF state current value will become weak.
[0028] Moreover, it is more desirable not to prepare between the source field 31 and the channel formation field 34, since parasitic capacitance will be formed in the field with which the gate electrode and the LDD field lapped in the above-mentioned structure. Since TFT for current control always has the same direction where a carrier (here electron) flows, it is enough if the LDD field is established only in the drain field side.
[0029] As mentioned above, in the pixel, TFT of two kinds of different structures according to a function is arranged. In addition, in the example shown here, TFT201 for switching and TFT202 for current control are formed with the n channel mold TFT. Since the n channel mold TFT can do TFT size smaller than the p channel mold TFT, when enlarging effective luminescence area of an EL element, it is very advantageous.
[0030] Hot carrier impregnation hardly becomes a problem, but the p channel mold TFT has the advantage that an OFF state current value is low, and the example used as TFT for switching and the example used as TFT for current control are already reported. However, in the invention in this application, also in the n channel mold TFT, the problem of hot carrier impregnation and the problem of an OFF state current value are solved by considering as the structure where the location of a LDD field was changed, and the description is that it is using all TFT(s) in all pixels as the n channel mold TFT.
[0031] Moreover, 41 is the passivation film and uses a silicon nitride film or the nitriding oxidation silicon film. 42 is a color filter and 43 is a fluorescent substance (it is also called a fluorescence pigment layer). In the combination of the same color, both contain the coloring matter of red (R), green (G), or blue (B). It prepares, in order that a color filter 42 may raise color purity, and a fluorescent substance 42 is formed in order to perform color conversion.
[0032] In addition, the method which it roughly divides into EL display, and there are four colorization means of displaying, and forms three kinds of EL elements corresponding to RGB, the method which combined the EL element and color filter of white luminescence, the method which combined the EL element and fluorescent substance (the color conversion layer of fluorescence: CCM) of blue luminescence, the method which puts the EL element corresponding to RGB on cathode (counterelectrode) using a transparent electrode, ******.
[0033] The structure of drawing 1 is an example at the time of using the method which combined the EL element and fluorescent substance of blue luminescence. Here, light with the wavelength of the blue field which contains ultraviolet radiation, using the luminous layer of blue luminescence as EL element 204 is formed, by the light, a fluorescent substance 43 is excited and the light of red, green, or blue is generated. And color purity is raised and outputted with a color filter 42.
[0034] However, it is not concerned with a luminescence method, but the invention in this application can be carried out, and can use all the four above-mentioned methods for the invention in this application.

[0035] Moreover, after forming a color filter 42 and a fluorescent substance 42, the 2nd interlayer insulation film 43 performs flattening. As the 2nd interlayer insulation film 44, the organic resin film is desirable and it is good to use polyimide, acrylic resin, or BCB (benz-cyclo-butene). Of course, the inorganic film may be used as long as sufficient flattening is possible.
[0036] 45 is a pixel electrode (anode plate of an EL element) which becomes by the transparence electric conduction film, and after it opens a contact hole in the 2nd interlayer insulation film 44 and the passivation film 41, it is formed so that it may connect with the drain wiring 37 of TFT202 for current control.
[0037] On the pixel electrode 45, the EL layer (an organic material is desirable) 46, cathode 47, and the protection electrode 48 are formed one by one. Although the EL layer 46 can be used by the monolayer or the laminated structure, it uses by the laminated structure in many cases. This invention may be which structure although various laminated structures are proposed as an EL layer combining the electronic transportation layer or the electron hole transportation layer in addition to the luminous layer.
[0038] Moreover, the ingredient which contains the small magnesium (Mg), the lithium (Li), or calcium (calcium) of a work function as cathode 47 is used. What is necessary is just to use a MgAg electrode preferably. Moreover, it is the electrode prepared in order that the protection electrode 48 may carry out the protective coat of the cathode 47 from external moisture, and the ingredient containing aluminum (aluminum) or silver (Ag) is used.
[0039] In addition, as for the EL layer 46 and cathode 47, it is desirable to carry out continuation formation, without carrying out atmospheric-air release. Namely, no matter EL layer and cathode may be what laminated structures, it is desirable to carry out continuation formation altogether. When using an organic material as an EL layer, since it is very weak for moisture, this is for avoiding the moisture absorption when carrying out atmospheric-air release. Furthermore, even the EL layer 46 and not only the cathode 47 but the protection electrode 48 on it is still better to carry out continuation formation.
[0040] EL display of this invention has the pixel section which consists of a pixel of the above structures, and TFT from which structure differs according to a function in a pixel is arranged. TFT for switching of an OFF state current value low enough and TFT for current control strong against hot carrier impregnation can form in the same pixel by this, it has high dependability and EL display in which good image display is possible can be formed.
[0041] Moreover, it can say that this invention is the same also about the drive circuit section of the active-matrix mold EL indicating equipment in which not only the pixel section of EL indicating equipment but the drive circuit section and the pixel section were formed on the same substrate. That is, in all drive circuit sections and pixel sections, the point which arranges TFT of different structure according to the function for which a circuit or a component asks is one of the main point of this invention.
[0042] Moreover, this invention can be carried out also when also forming other digital disposal circuits in addition to the above-mentioned drive circuit section or the pixel section. As other digital disposal circuits, a signal dividing network, a D/A converter, a gamma correction circuit, a booster circuit, or a differential amplifying circuit is mentioned.

[0043] Suppose that still more detailed explanation is given about this invention which becomes with the above configuration as it is also at the example shown below.
[0044] [Example 1] The example of this invention is explained using drawing 3 - drawing 5 . Here, how to produce to coincidence TFT of the pixel section and the drive circuit section prepared around it is explained. However, in order to simplify explanation, suppose that the CMOS circuit which is a basic circuit is illustrated about a drive circuit.
[0045] First, as shown in drawing 3 (A), the substrate film 301 is formed on a glass substrate 300 at the thickness of 300nm. In this example, as substrate film 301, the laminating of the nitriding oxidation silicon film is carried out, and it is used. At this time, it is good to make into 10 - 25wt% nitrogen concentration of the direction which touches a glass substrate 300.
[0046] Next, the amorphous silicon film (not shown) with a thickness of 50nm is formed by the well-known forming-membranes method on the substrate film 301. In addition, what is necessary is just the semi-conductor film (the microcrystal semi-conductor film is included) which does not need to limit to the amorphous silicon film and includes amorphous structure. The compound semiconductor film which furthermore includes the amorphous structure of the amorphous silicon germanium film etc. is sufficient. Moreover, thickness should just be 20-100nm in thickness.
[0047] And the amorphous silicon film is crystallized with a well-known technique, and the crystalline substance silicon film (it is also called the polycrystalline silicon film or the polish recon film) 302 is formed. As the well-known crystallization approach, there are the heat crystallization approach which used the electric heat furnace, a laser annealing crystallizing method using laser light, and the lamp annealing crystallizing method using infrared light. In this example, it crystallizes using the excimer laser light which used XeCl gas.

[0048] In addition, although the excimer laser light of the pulse oscillation mold processed into the line is used in this example, you may be a rectangle and the argon laser light of a continuous-oscillation mold and the excimer laser light of a continuous-oscillation mold can also be used.
[0049] Next, as shown in drawing 3 (B), the protective coat 303 which becomes by the oxidation silicon film is formed on the crystalline substance silicon film 302 at the thickness of 130nm. What is necessary is just to choose this thickness in 100-200nm (preferably 130-170nm). Moreover, other film is sufficient as long as it is an insulator layer containing silicon. This protective coat 303 is formed in order to enable concentration control delicate in order not to put the crystalline substance silicon film to the direct plasma, in case an impurity is added.
[0050] And the resist masks 304a-304c are formed on it, and the impurity element (henceforth n mold impurity element) which gives n mold through a protective coat 303 is added. In addition, Lynn or arsenic can be used for the element and type target which belong to 15 groups typically as an n mold impurity element. In addition, in this example, Lynn is added by the concentration of 1x1018 atoms/cm3 using the plasma doping method which carried out plasma excitation without carrying out mass separation of the phosphoretted hydrogen (PH3). Of course, the ion implantation method for performing mass separation may be used.
[0051] In n mold impurity ranges 305-307 formed of this process, a dose is adjusted so that n mold impurity element may be contained by the concentration of 2x1016 - 5x1019 atoms/cm3 (typically 5x1017 - 5x1018 atoms/cm3). In addition, n mold impurity range 306 is equivalent to the semiconductor region 23 for capacity formation shown in drawing 1 .
[0052] Next, as shown in drawing 3 (C), the element which removes a protective coat 303 and belongs to 15 groups who added is activated. Although an activation means should just use a well-known technique, it is activated by the exposure of excimer laser light by this example. Of course, a pulse oscillation mold or a continuous-oscillation mold may be used, and it is not necessary to limit to excimer laser light. However, since activation of the added impurity element is the purpose, it is desirable to irradiate with the energy which is extent which the crystalline substance silicon film does not fuse. In addition, laser light may be irradiated, with the protective coat 303 attached.
[0053] In addition, on the occasion of activation of the impurity element by this laser light, activation by furnace annealing or lamp annealing may be used together. What is necessary is just to perform heat treatment of about 450-550 degrees C in consideration of the thermal resistance of a substrate, when performing activation by furnace annealing. Moreover, it may be activated only by furnace annealing or lamp annealing.
[0054] The boundary section (joint) with the field which has not added n mold impurity element which exists in the edge of n mold impurity ranges 305-307, i.e., the perimeter of n mold impurity ranges 305-307, according to this process becomes clear. This means that a LDD field and a channel formation field can form a very good joint, when TFT is completed behind.
[0055] Next, as shown in drawing 3 (D), the unnecessary part of the crystalline substance silicon film is removed, and the island-like semi-conductor film (henceforth a barrier layer) 308-311 is formed.
[0056] Next, as shown in drawing 3 (E), barrier layers 308-311 are covered and gate dielectric film 312 is formed. What is necessary is just to use 10-200nm of insulator layers which contain silicon with a thickness of 50-150nm preferably as gate dielectric film 312. Monolayer structure or a laminated structure is sufficient as this. In this example, the nitriding oxidation silicon film of 110nm thickness is used.
[0057] Next, patterning of the electric conduction film of 200-400nm thickness is formed and carried out, and the gate electrodes 313-317 and the electrode 318 for capacity formation are formed. In addition, although this specification may distinguish and explain a gate electrode and gate wiring, the part which functions as an electrode is only called the gate electrode, and you may think that the gate electrode is contained in gate wiring. What is necessary is for the same to be said of the electrode for capacity formation as for this, and just to call the part which is not functioning as an electrode wiring for capacity formation.
[0058] Moreover, although a gate electrode may be formed by the electric conduction film of a monolayer, it is desirable to consider as cascade screens, such as a bilayer and three layers, if needed. All electric conduction film well-known as an ingredient of a gate electrode can be used.
[0059] Specifically A tantalum (Ta), titanium (Ti), molybdenum (Mo), The thin film containing the silicon (Si) which has a tungsten (W), chromium (Cr), or conductivity, Or the thin film which nitrided them (typically the tantalum nitride film, nitriding tungsten film, or titanium nitride film), Or the alloy film (typically a Mo-W alloy or a Mo-Ta alloy) which combined the above-mentioned element, or the silicide film (typically tungsten silicide film or titanium silicide film) containing the above-mentioned element can be used. Of course, these may be used by the monolayer, or a laminating may be carried out and you may use.
[0060] In this example, the cascade screen which becomes by the tantalum nitride (TaN) film of 50nm thickness and Ta

film of 350nm thickness is used. What is necessary is just to form this by the spatter. Moreover, if inert gas, such as Xe and Ne, is added as sputtering gas, film peeling by stress can be prevented.
[0061] Moreover, at this time, the gate electrodes 314 and 317 are formed so that it may lap on both sides of gate dielectric film 312 with a part of n mold impurity ranges 305 and 307, respectively. This overlapping part serves as a LDD field which lapped with the gate electrode behind. In addition, although the gate electrodes 315 and 316 are visible to two in a cross section, they are formed from one pattern connected continuously in practice.
[0062] Moreover, on n mold impurity range 306, the electrode 318 for capacity formation is formed on both sides of gate dielectric film 312. At this time, the insulator layer prepared as gate dielectric film 312 is used as a dielectric of retention volume here, and the retention volume which consists of n mold impurity range (semiconductor region for capacity formation) 306, gate dielectric film 312, and an electrode 318 for capacity formation is formed.
[0063] Next, as shown in drawing 4 (A), n mold impurity element (this example Lynn) is added in self align by using the gate electrodes 313-317 and the electrode 318 for capacity formation as a mask. In this way, in the impurity ranges 319-325 formed, it adjusts so that Lynn may be added by the concentration of 1 / 2 - 1/10 of n mold impurity ranges 305-307 (typically 1 / 3 - 1/4). Specifically, the concentration of 1x1016 - 5x1018 atoms/cm3 (typically 3x1017 - 3x1018 atoms/cm3) is desirable.
[0064] Next, as shown in drawing 4 (B), the resist masks 326a-326c are formed for a gate electrode etc. in a wrap form, and the impurity ranges 327-334 which add n mold impurity element (this example Lynn), and include Lynn in high concentration are formed. It carries out by the ion doping method for having used phosphoretted hydrogen (PH3) also here, and the concentration of Lynn of this field is adjusted so that it may become 1x1020 - 1x1021 atoms/cm3 (typically 2x1020 - 5x1021 atoms/cm3).
[0065] Although the source field or drain field of the n channel mold TFT is formed of this process, TFT for switching leaves a part of n mold impurity ranges 322-324 formed at the process of drawing 4 (A). This left-behind field is equivalent to the LDD fields 15a-15d of TFT for switching in drawing 1 .
[0066] Next, as shown in drawing 4 (C), the resist masks 326a-326c are removed, and the resist mask 325 is newly formed. And p mold impurity element (this example boron) is added, and the impurity ranges 336 and 337 which contain boron in high concentration are formed. Here, boron is added so that it may become 3x1020 - 3x1021 atoms/cm3 (typically 5x1020 - 1x1021 atoms/cm3 NO) concentration by the ion doping method for having used diboron hexahydride (B-2 H6).
[0067] In addition, although Lynn is already added by impurity ranges 319 and 320 by the concentration of 1x1020 - 1x1021 atoms/cm3, the boron added here is added by the concentration of at least 3 times or more. Therefore, it is completely reversed to P type, and the impurity range of n mold currently formed beforehand functions as an impurity range of P type.
[0068] Next, as shown in drawing 4 (D), after removing the resist mask 335, the 1st interlayer insulation film 338 is formed. What is necessary is just to use the cascade screen which combined the insulator layer which uses the insulator layer containing silicon by the monolayer as the 1st interlayer insulation film 338, or contains silicon. Moreover, thickness is just 400nm - 1.5 micrometers. In this example, it considers as the structure which carried out the laminating of the oxidation silicon film of 800nm thickness on the nitriding oxidation silicon film of 200nm thickness.
[0069] Then, n mold or p mold impurity element added by each concentration is activated. As an activation means, it can carry out by the furnace annealing method, the laser annealing method, or the lamp annealing method. In this example, 550 degrees C and heat treatment of 4 hours are performed among nitrogen-gas-atmosphere mind in an electric heat furnace.
[0070] Furthermore, in the ambient atmosphere containing 3 - 100% of hydrogen, heat treatment of 1 - 12 hours is performed at 300-450 degrees C, and a hydrogen treating is performed. This process is a process which carries out hydrogen termination of the azygos joint hand of the semi-conductor film by the hydrogen excited thermally. As other means of hydrogenation, plasma hydrogenation (the hydrogen excited by the plasma is used) may be performed.
[0071] In addition, a hydrogen treating may be put in while forming the 1st interlayer insulation film 338. That is, after forming the nitriding oxidation silicon film of 200nm thickness, a hydrogen treating may be performed as mentioned above, and it may remain after that, and the oxidation silicon film of 800nm thickness may be formed.
[0072] Next, as shown in drawing 5 (A), a contact hole is formed to the 1st interlayer insulation film 338, and source wiring 339-342, the drain wiring 343-345, and the connection wiring 346 are formed. In addition, in this example, it considers as the cascade screen of the three-tiered structure which carried out the aluminum film which includes [Ti film] these wiring for 100nm and Ti by 300nm, and carried out continuation formation of the 150nm of the Ti film by the spatter. Of course, other electric conduction film may be used.
[0073] Next, the passivation film 347 is formed by the thickness of 50-500nm (typically 200-300nm). In this example,

the nitriding oxidation silicon film of 300nm thickness is used as passivation film 347. A silicon nitride film may be substituted for this.

[0074] At this time, it is effective to perform plasma treatment using the gas which contains H2 and NH3 grade hydrogen in advance of formation of the nitriding oxidation silicon film. The membraneous quality of the passivation film 347 is improved because the hydrogen excited by this pretreatment heat-treats by supplying the 1st interlayer insulation film 338. Since the hydrogen added by the 1st interlayer insulation film 338 at it and coincidence is spread in a lower layer side, a barrier layer can be hydrogenated effectively.

[0075] Next, as shown in drawing 5 (B), a color filter 348 and a fluorescent substance 349 are formed. These ingredients should just use a well-known thing. Moreover, patterning may be carried out separately and you may form, and these are formed continuously, and by package, patterning of them may be carried out and they may be formed. Each thickness is chosen in 0.5-5 micrometers (typically 1-2 micrometers). The optimal thickness changes with ingredients which use especially the fluorescent substance 349. That is, if too thin, color conversion efficiency will worsen, if too thick, a level difference turns large up and the amount of transmitted lights of light will fall off. Therefore, the optimal thickness must be determined on the balance of both properties.

[0076] In addition, although this example explains the light generated from EL layer taking the case of the colorization method which carries out color conversion, when adopting the method which produces EL layer corresponding to RGB according to an individual, a color filter and a fluorescent substance can also be omitted.

[0077] Next, the 2nd interlayer insulation film 350 which consists of organic resin is formed. As organic resin, polyimide, a polyamide, acrylic resin, or BCB (benz-cyclo-butene) can be used. Since especially the 2nd interlayer insulation film has the strong implications of flattening, its acrylic resin excellent in surface smoothness is desirable. At this example, acrylic resin is formed by the thickness which can carry out flattening of the level difference of a color filter 348 and a fluorescent substance 349.

[0078] Next, the contact hole which reaches the drain wiring 345 is formed in the 2nd interlayer insulation film 350 and the passivation film 347, and the pixel electrode 351 is formed. In this example, the electric conduction film (ITO film) which consists of a compound of indium oxide and the tin oxide is formed in the thickness of 110nm, patterning is performed, and it considers as a pixel electrode. This pixel electrode turns into an anode plate of an EL element.

[0079] Next, continuation formation is carried out without carrying out atmospheric-air release of the EL layer 352, cathode (MgAg electrode) 353, and the protection electrode 354, as shown in drawing 5 (C). However, an ingredient well-known as an EL layer 352 can be used. When the organic material is known and driver voltage is taken into consideration as a well-known ingredient, it is desirable to use an organic material. Let 4 layer structures which become in a hole-injection layer, an electron hole transportation layer, a luminous layer, and an electron injection layer be EL layers in this example. Moreover, although a MgAg electrode is used as cathode of an EL element in this example, you may be other well-known ingredients.

[0080] Moreover, the protection electrode 354 is formed in order to prevent degradation of the MgAg electrode 353, and the aluminum film (electric conduction film containing aluminum) is suitable for it. Of course, other ingredients are sufficient. Moreover, since the EL layer 352 and the MgAg electrode 353 are weak for moisture, it is desirable to form continuously without carrying out atmospheric-air release even of the protection electrode 354, and to protect EL layer from the open air.

[0081] In addition, what is necessary is just to set to 180-300nm (typically 200-250nm) thickness whose thickness of the EL layer 352 is 800-200nm (typically 100-120nm) and a MgAg electrode.

[0082] In this way, the active-matrix mold EL display of structure as shown in drawing 5 (C) is completed. In addition, in fact, when completing to drawing 5 (C), it is desirable to pack with airtight high protection films (laminate film etc.) so that it may not be further put to the open air. The dependability of EL layer improves by making the inside of a protection film into an inert atmosphere in that case.

[0083] Moreover, if packaging processing raises airtightness, the connector (flexible print circuit: FPC) for connecting the terminal and external signal terminal which were taken about from the component formed on the substrate or the circuit will be attached, and it will complete as a product. EL indicating equipment of such a condition is called EL module in this specification.

[0084] By the way, by arranging TFT of the optimal structure for the drive circuit section and the pixel section, the active-matrix mold EL display of this example shows very high dependability, and its operating characteristic may also improve.

[0085] First, TFT which has the structure of reducing hot carrier impregnation is used as an n channel mold TFT205 of the CMOS circuit which forms a drive circuit. In addition, as a drive circuit here, a shift register, a buffer, a level shifter, a sampling circuit (sample and hold circuit), etc. are included. In performing a digital drive, a D/A converter or a latch is

also included and it gets.
[0086] In the case of this example, as shown in drawing 5 (C), in the LDD field 357, the barrier layer of the n channel mold 205 has lapped with the gate electrode 314 on both sides of gate dielectric film 312 including the source field 355, the drain field 356, the LDD field 357, and the channel formation field 358.
[0087] The consideration for not reducing a working speed forms the LDD field only in a drain field side. Moreover, it is better for this n channel mold TFT205 to seldom have cared about the OFF state current value, and to attach greater importance than to it to a working speed. Therefore, as for the LDD field 357, it is desirable to keep in a gate electrode in piles completely, and to lessen a resistance component as much as possible. Namely, it is better to abolish the so-called offset.
[0088] Moreover, since degradation by hot carrier impregnation hardly worries the p channel mold TFT206 of a CMOS circuit, it is not necessary to prepare especially a LDD field. Therefore, a barrier layer includes the source field 359, the drain field 360, and the channel formation field 361. Of course, it is also possible to prepare a LDD field like the n channel mold TFT205, and to take the cure against a hot carrier.
[0089] In addition, also in a drive circuit, a sampling circuit is a particular for a while compared with other circuits, and a high current flows a channel formation field bidirectionally. That is, the role of a source field and a drain field interchanges. Furthermore, it is desirable to arrange TFT which needs to hold down an OFF state current value low as much as possible, and has the function of middle extent of TFT for switching and TFT for current control in such semantics.
[0090] Therefore, as for the n channel mold TFT which forms a sampling circuit, it is desirable to arrange TFT of structure as shown in drawing 8 . As shown in drawing 8 , a part of LDD fields 71a and 71b lap with the gate electrode 73 on both sides of gate dielectric film 72. This effectiveness is as explanation of TFT202 for current control having described, and, in the case of a sampling circuit, the points established in the form which faces across the channel formation field 74 differ.
[0091] Moreover, the pixel of structure as shown in drawing 1 is formed, and the pixel section is formed. About the structure of TFT for switching formed in a pixel, and TFT for current control, since drawing 1 already explained, explanation here is omitted.
[0092] [Example 2] This example explains the case where the pixel section of a active-matrix mold EL display is made into different structure from drawing 1 .
[0093] The example which changed the structure of TFT for switching with drawing 1 first is shown in drawing 6 (A). However, since it is the completely same structure as an example 1, TFT202 for current control and retention volume 203 which were shown in drawing 6 (A), and EL element 204 omit explanation. Moreover, a new sign is attached only to a need part also about TFT for switching, and other parts give explanation of drawing 1 to use as it is.
[0094] TFT(s)207 for switching shown in TFT201 for switching shown in drawing 1 and drawing 6 (A) differ in the formation location of a LDD field. The LDD fields 15a-15d of drawing 1 are formed so that it may not lap with the gate electrodes 19a and 19b, but by this example, they are formed so that a part may lap with a gate electrode.
[0095] That is, as shown in drawing 6 (A), the LDD fields [of TFT207 for switching / 50a-50d] part has lapped with the gate electrodes 51a and 51b on both sides of gate dielectric film. If it puts in another way, the LDD fields 50a-50d have the field which laps with the gate electrodes 51a and 51b on both sides of gate dielectric film.
[0096] Only by the ability to reduce an OFF state current value by this, it can lessen and degradation by hot carrier impregnation can also be prevented. However, since parasitic capacitance is formed between a gate electrode and a LDD field, compared with the structure of drawing 1 , a working speed may fall a little. However, if it designs based on the point, it is possible to form reliable TFT for switching.
[0097] Next, the example which changed the structure of TFT for current control with drawing 1 is shown in drawing 6 (B). However, since it is the completely same structure as an example 1, TFT201 for switching and retention volume 203 which were shown in drawing 6 (B), and EL element 204 omit explanation. Moreover, a new sign is attached only to a need part also about TFT for current control, and other parts give explanation of drawing 1 to use as it is.
[0098] TFT(s)208 for current control shown in TFT202 for current control shown in drawing 1 and drawing 6 (B) differ in the formation location of a LDD field. The LDD field 33 of drawing 1 is formed so that a part may lap with the gate electrode 35, but by this example, it is formed so that it may lap with a gate electrode completely.
[0099] That is, as shown in drawing 6 (B), the LDD field 52 of TFT208 for current control laps with the gate electrode 53 completely through gate dielectric film. If it puts in another way, the LDD field 52 does not have the field which does not lap with the gate electrode 53.
[0100] When the minimum electrical potential difference of a video (image) signal is impressed to the gate voltage of TFT for current control, if an OFF state current value is not fully low, an EL element emits light, and the fall of contrast

is caused. The structure of drawing 1 has prepared the LDD field which does not lap with a gate electrode, in order to lower the OFF state current value at that time.
[0101] However, in order to commit the LDD field which does not lap with a gate electrode as a resistance component, a working speed and an ON state current value will be lowered to some extent. Therefore, if it keeps as structure which is not established like this example, since such resistance components can be eliminated, it sink-comes to be easy of a bigger current. However, as mentioned above, when the minimum electrical potential difference of a video (image) signal is impressed to the gate voltage of TFT for current control, it is a premise to use TFT with a fully low OFF state current value.
[0102] In addition, it is also possible to use combining TFT207 for switching of drawing 6 (A) and TFT for current control of drawing 6 (B). Moreover, a production process should just refer to an example 1.
[0103] [Example 3] This example shows a different example from the configuration which showed the configuration of a pixel to drawing 2 (B) to drawing 7 .
[0104] In this example, two pixels shown in drawing 2 (B) are arranged so that it may become symmetrical about the current supply source line 212 for giving touch-down potential. That is, as shown in drawing 7 , the number of wiring which needs the current supply source line 213 by communalizing between two adjoining pixels is reduced. In addition, the TFT structure arranged in a pixel remains as it is, and is good.
[0105] It becomes possible to produce such a configuration, then the higher definition pixel section, and the quality of an image improves. In addition, according to the production process of an example 1, it can realize easily, and the configuration of this example may be combined with an example 2 about TFT structure.
[0106] [Example 4] This example explains the case where the pixel section of different structure from drawing 1 is formed, using drawing 9 . In addition, the process which forms the 2nd interlayer insulation film 44 should just follow an example 1. Moreover, since TFT201 for switching, TFT202 for current control, and retention volume 203 which were covered with the 2nd interlayer insulation film 44 are the same structure as drawing 1 , explanation is omitted.
[0107] If a contact hole is formed to the 2nd interlayer insulation film 44 in the case of this example, the pixel electrode 60, cathode 61, and the EL layer 62 will be formed. These carry out continuation formation without carrying out atmospheric-air release of each ingredient, they are etched by package, and should just perform pattern formation.
[0108] In this example, the aluminium alloy film (aluminum film containing 1wt% titanium) of 150nm thickness is prepared as a pixel electrode 60. In addition, although what kind of ingredient is sufficient as long as it is a metallic material as an ingredient of a pixel electrode, it is desirable that it is an ingredient with a high reflection factor.
[0109] Moreover, the thickness of the EL layer 62 may be 120nm, using the MgAg electrode of 230nm thickness as cathode 61. In addition, what is necessary is just to use the ingredient explained in the example 1 about formation of the EL layer 62.
[0110] Next, the insulator layer containing silicon is formed in the thickness of 200-500nm (typically 250-300nm), and the protective coat 63 which has opening by patterning is formed. And the anode plate 64 which consists of transparence electric conduction film (this example ITO film) is formed on it at the thickness of 110nm. As transparence electric conduction film, the compound of indium oxide and a zinc oxide, the tin oxide, indium oxide, or a zinc oxide can be used for others. Moreover, what added the gallium may be used for them.
[0111] Furthermore, a fluorescent substance 65 and a color filter 66 are formed on an anode plate 64, and the pixel section as shown in drawing 9 is completed.
[0112] When it considers as the structure of this example, outgoing radiation of the light of green or blue is carried out to the generated red and the substrate in which TFT was formed in the opposite side. Therefore, it can use as a luminescence field mostly, the whole region, i.e., the field in which TFT was formed, in a pixel. Consequently, the effective luminescence area of a pixel improves sharply and the brightness and contrast of an image improve.
[0113] In addition, the configuration of this example can be freely combined with any configuration of examples 2 and 3.
[0114] [Example 5] In the example 1, although laser crystallization is used as means forming of the crystalline substance silicon film 302, the case where a different crystallization means is used is explained in this example.
[0115] In this example, after forming the amorphous silicon film, it crystallizes using the technique indicated by JP,7-130652,A. The technique of considering as the catalyst element which promotes crystallization (promotion), and obtaining the crystalline high crystalline substance silicon film in this official report using nickel is indicated.
[0116] Moreover, after a crystallization process is completed, the process which removes the catalyst element used for crystallization may be performed. In that case, what is necessary is just to carry out gettering of the catalyst element with the technique indicated by JP,10-270363,A or JP,8-330602,A.
[0117] Moreover, TFT may be formed using the technique indicated by the specification of Japanese Patent Application

No. No. 076967 [11 to] by these people. What is necessary is just to refer to even the part which forms TFT, although different retention volume from drawing 1 is explained by the specification of Japanese Patent Application No. No. 076967 [11 to].

[0118] As mentioned above, it is making into main point for this invention to arrange TFT of suitable structure according to the function for which a component asks, as an example 1 and drawing 1 explained, and is not limited to the production approach. That is, the production process shown in the example 1 will be one example, and if the structure of drawing 5 (C) of drawing 1 or an example 1 is realizable, even if it uses other production processes, it will not be a problem.

[0119] In addition, in producing such structure also about the case where one configuration of the examples 2-4 is combined with the structure of drawing 1 or drawing 5 (C), it is possible to combine a production process as shown in this example.

[0120] [Example 6] In an example 1, the process which etches gate dielectric film 312 between the process of drawing 4 (A) and the process of drawing 4 (B) may be added. Namely, as shown in drawing 4 (A), after adding n mold impurity element, gate dielectric film 312 is etched in self align by using the gate electrodes 313-317 and the electrode 318 for capacity formation as a mask. This etching is performed until it is exposed of a barrier layer.

[0121] In this example, since the gate dielectric film used example 1 is nitriding oxidization silicon film, dry etching using CHF3 gas as etching gas is performed. Of course, other etching conditions are not limited to this.

[0122] And as shown in drawing 4 (B) to the exposed barrier layer, the addition process of n mold impurity element is performed. At this process, since direct Lynn will be added to a barrier layer, without letting gate dielectric film pass, it can process very much in a short time. Moreover, since the acceleration voltage at the time of addition is also low and ends, the damage to a barrier layer can also be reduced.

[0123] The rest should just complete EL display according to the process of an example 1. In addition, it combines with any configuration of examples 1-5 freely, and the configuration of this example can be carried out.

[0124] [Example 7] This example explains the active-matrix mold EL display in which the pixel of different structure from an example 1 was formed.

[0125] Although drawing 10 (A) is EL display of this example, the TFT structure of it is the same as an example 1 (refer to drawing 5 (C)). In this example, the pixel electrode 1001, cathode 1002, the EL layer 1003, and an anode plate 1004 are formed, and EL element 1000 is formed in cathode 1002, the EL layer 1003, and an anode plate 1004. At this time, the pixel electrode 1001 may use what kind of well-known electric conduction film. Moreover, in this example, the transparence electric conduction film which added the oxidation gallium to the zinc oxide as an anode plate 1004 is used, using the MgAg film as cathode 1002. In addition, what is necessary is just to form the EL layer 1003 combining a well-known ingredient.

[0126] In this example, the description is in the point that the crevice (hollow) formed in the contact section (part to which the pixel electrode 1001 and TFT202 for current control were connected) of the pixel electrode 1001 is embedded with an insulating material 1005, and the edge of the pixel electrode 1001 is further covered with the insulating material 1006.

[0127] The insulating material 1005 has prevented poor covering of EL layer by the level difference by embedding the above-mentioned crevice. the contact hole formed in the 2nd interlayer insulation film 350 -- being deep (a level difference being high) -- there is a possibility that poor covering of EL layer may arise and cathode 1002 and an anode plate 1004 may connect too hastily. Therefore, in this example, it is characterized by preventing poor covering of EL layer by embedding a crevice with an insulating material 1005.

[0128] Moreover, similarly, since the level difference for thickness of the pixel electrode 1001 has arisen, the edge of the pixel electrode 1001 forms an insulating material 1006 for the same reason as an insulating material 1005. Thereby in the edge of the pixel electrode 1001, the short circuit of cathode 1002 and an anode plate 1004 can be prevented certainly. Moreover, since electric-field concentration is caused and degradation of the EL layer 1003 tends to advance, the edge of the pixel electrode 1001 also has the purpose which is made not to carry out electric-field concentration in the EL layer 1003 by forming an insulating material 1006.

[0129] Moreover, drawing 10 (B) is an example at the time of considering as the structure which does not form a LDD field in the barrier layer of TFT for current control. When the electrical potential difference concerning an EL element becomes less than [5V] preferably below 10V, since degradation by the hot carrier hardly poses a problem, it can be considered as such structure. That is, with the structure of drawing 10 (B), the barrier layer of TFT for current control consists of the source field 1010, a drain field 1011, and a channel formation field 1012.

[0130] In addition, it combines with any configuration of examples 1-6 freely, and the configuration of this example can be carried out.

[0131] [Example 8] The analog drive for which the drive used the analog signal for EL display of this invention as a picture signal can also be performed, and the digital drive using a digital signal can also be performed.
[0132] When performing an analog drive, an analog signal is sent to the source wiring of TFT for switching, and an analog signal including the gradation information serves as gate voltage of TFT for current control. And the current which flows to an EL element is controlled by TFT for current control, the luminescence reinforcement of an EL element is controlled, and a gradation display is performed.
[0133] On the other hand, when performing a digital drive, unlike an analog gradation display, the gradation display called a time-sharing drive is performed. That is, by adjusting the die length of luminescence time amount, it shows as color gradation is changing visually.
[0134] Since the speed of response is very quick compared with a liquid crystal device, an EL element can be driven at high speed. Therefore, it can be said that it is a component suitable for the time-sharing drive which divides one frame into two or more subframes, and performs a gradation display.
[0135] Thus, since this invention is a technique about component structure, the drive approach may be what kind of thing.
[0136] [Example 9] Although [an example 1] it is desirable to use an organic electroluminescence ingredient as an EL layer, even if this invention uses inorganic EL ingredient, it can be carried out. However, since driver voltage is very high, the present inorganic EL ingredient must use TFT which has the proof-pressure property that such driver voltage can be borne, when performing an analog drive.
[0137] Or if inorganic EL ingredient with prospective still lower driver voltage is developed, applying to this invention is possible.
[0138] Moreover, the configuration of this example can be freely combined with any configuration of examples 1-7.
[0139] [Example 10] The external view of EL display of this invention is explained. In addition, drawing 11 (A) is the plan of EL display of this invention, and drawing 11 (B) is the sectional view.
[0140] In drawing 11 (A), for 4001, as for the pixel section and 4003, a substrate and 4002 are [a source side drive circuit and 4004] gate side drive circuits, and each drive circuit results in FPC (flexible print circuit)4006 through wiring 4005, and is connected to an external instrument.
[0141] At this time, as the pixel section 4002, the source side drive circuit 4003, and the gate side drive circuit 4004 are surrounded, the 1st sealant 4101, the covering material 4102, a filler 4103, and the 2nd sealant 4104 are formed.
[0142] Moreover, drawing 11 (B) is equivalent to the sectional view which cut drawing 11 (A) by A-A', and TFT4202 for current control contained in the drive TFT(however, n channel mold TFT and p channel mold TFT are illustrated here.) 4201 and the pixel section 4002 which are contained in the source side drive circuit 4003 is formed on the substrate 4001.
[0143] In this example, TFT of the same structure as the n channel mold TFT205 of drawing 5 (C) and the p channel mold TFT206 is used for drive TFT4201, and TFT of the same structure as the n channel mold TFT202 of drawing 1 is used for TFT4202 for current control. Moreover, the retention volume (not shown) connected to the gate of TFT4202 for current control is prepared in the pixel section 4002.
[0144] On drive TFT4201 and a pixel TFT4202, the interlayer insulation film (flattening film) 4301 which becomes with a resin ingredient is formed, and the pixel electrode (cathode) 4302 electrically connected with the drain of a pixel TFT4202 is formed on it. As a pixel electrode 4302, the small electric conduction film of a work function is used. The electric conduction film (electric conduction film which included alkali metals or an alkaline-earth-metal element in aluminum, copper, or silver typically) which contains the element belonging to one group of a periodic table or two groups as a metal membrane can be used.
[0145] And an insulator layer 4303 is formed on the pixel electrode 4302, and, as for the insulator layer 4303, opening is formed on the pixel electrode 4302. In this opening, the EL (electroluminescence) layer 4304 is formed on the pixel electrode 4302. The EL layer 4304 can use a well-known organic electroluminescence ingredient or inorganic EL ingredient. Moreover, whichever may be used although there are a low-molecular system (monomer system) ingredient and a macromolecule system (polymer system) ingredient as organic electroluminescence ingredient.
[0146] The formation approach of the EL layer 4304 should just use a well-known vacuum evaporationo technique or the applying method technique. Moreover, what is necessary is just to make structure of EL layer into a laminated structure or monolayer structure, combining freely a hole-injection layer, an electron hole transportation layer, a luminous layer, an electronic transportation layer, or an electron injection layer.
[0147] On the EL layer 4304, the anode plate 4305 which consists of transparence electric conduction film is formed. The electric conduction film which contains in the compound of indium oxide and the tin oxide, the compound of indium oxide and a zinc oxide, indium oxide, the tin oxide, a zinc oxide, or them the compound which added the

gallium as transparence electric conduction film can be used.
[0148] Moreover, as for the moisture which exists in the interface of an anode plate 4305 and the EL layer 4304, or oxygen, eliminating as much as possible is desirable. Therefore, the device of carrying out continuation membrane formation of both in a vacuum, or forming the EL layer 4304 in nitrogen or a rare-gas ambient atmosphere, and forming an anode plate 4305, making neither oxygen nor moisture touched is required. At this example, the above membrane formation is enabled by using the membrane formation equipment of a multi chamber method (cluster tool method).
[0149] And an anode plate 4305 is electrically connected to wiring 4005 in the field shown by 4306. Wiring 4005 is wiring for giving a predetermined electrical potential difference to an anode plate 4305, and is electrically connected to FPC4006 through the different direction conductivity film 4307.
[0150] The EL element which consists of the pixel electrode (cathode) 4302, an EL layer 4304, and an anode plate 4305 as mentioned above is formed. This EL element is surrounded by the covering material 4102 stuck on the substrate 4001 by the 1st sealant 4101 and the 1st sealant 4101, and is enclosed by the filler 4103.
[0151] As covering material 4102, glass material or plastics material (plastic film is also included) can be used. As plastics material, an FRP (Fiberglass-Reinforced Plastics) plate, a PVF (polyvinyl fluoride) film, a Mylar film, polyester film, or an acrylic resin film can be used.
[0152] Moreover, as a filler 4103, ultraviolet-rays hardening resin or heat-curing resin can be used, and PVC (polyvinyl chloride), an acrylic, polyimide, an epoxy resin, silicone resin, and PVB (polyvinyl BUCHIRARU) or EVA (ethylene vinyl acetate) can be used. If the hygroscopic matter (preferably barium oxide) is prepared in the interior of this filler 4103, degradation of an EL element can be controlled.
[0153] Moreover, a spacer may be made to contain in a filler 4103. At this time, if a spacer is formed with the barium oxide, it is possible to give hygroscopicity to the spacer itself. Moreover, when a spacer is formed, it is also effective to prepare the resin film on an anode plate 4305 as a buffer layer which eases the pressure from a spacer.
[0154] Moreover, wiring 4005 is electrically connected to FPC4006 through the different direction conductivity film 4307. Wiring 4005 tells the signal sent to the pixel section 4002, the source side drive circuit 4003, and the gate side drive circuit 4004 to FPC4006, and is electrically connected with an external instrument by FPC4006.
[0155] Moreover, in this example, the 2nd sealant 4104 is formed so that the disclosure section of the 1st sealant 4101 and a part of FPC4006 may be covered, and it has structure which intercepts an EL element from the open air thoroughly. In this way, it becomes EL display which has the cross-section structure of drawing 11 (B). In addition, EL display of this example may be produced combining which configuration of examples 1-9.
[0156] [Example 11] This example shows the example of the pixel structure of EL display of this invention to drawing 12 (A) - (C). in addition, this example -- setting -- 4601 -- in gate wiring of TFT4602 for switching, and 4604, a capacitor, and 4606 and 4608 make it as a current supply source line, and 4607 makes TFT for current control, and 4605 an EL element for the source wiring of TFT4602 for switching, and 4603.
[0157] Drawing 12 (A) is an example at the time of making the current supply source line 4606 common between two pixels. That is, the description is formed so that two pixels may serve as axial symmetry focusing on the current supply source line 4606. In this case, since the number of a current supply source line can be reduced, the pixel section can be further made highly minute.
[0158] Moreover, drawing 12 (B) is an example at the time of forming the current supply source line 4608 in parallel with the gate wiring 4603. In addition, although it has structure established so that the current supply source line 4608 and the gate wiring 4603 might not lap in drawing 12 (B), if it is wiring formed in the layer from which both differ, it can also prepare so that it may lap through an insulator layer. In this case, since the current supply source line 4608 and the gate wiring 4603 can be made to share monopoly area, the pixel section can be further made highly minute.
[0159] Moreover, drawing 12 (C) forms the current supply source line 4608 in parallel with the gate wiring 4603 like the structure of drawing 12 (B), and the description is that it forms two pixels further so that it may become axial symmetry focusing on the current supply source line 4608. Moreover, it is also effective to form the current supply source line 4608 so that it may lap with either of the gate wiring 4603. In this case, since the number of a current supply source line can be reduced, the pixel section can be further made highly minute.
[0160] In addition, the configuration of this example can be freely combined with any configuration of examples 1-10.
[0161] [Example 13] This example shows the example of the pixel structure of EL display of this invention to drawing 13 (A) and (B). in addition, this example -- setting -- 4701 -- the source wiring of TFT4702 for switching, and 4703 -- gate wiring of TFT4702 for switching, and 4704 -- in a capacitor (omitting is also possible) and 4706, TFT for power control and 4708 make it as gate wiring for power control, and 4709 makes a current supply source line and 4707 an EL element for TFT for current control, and 4705. About actuation of TFT4707 for power control, it is good to refer to Japanese Patent Application No. No. 341272 [11 to].

[0162] Moreover, although TFT4707 for power control is formed between TFT4704 for current control, and EL element 4708 in this example, it is good also as structure where TFT4704 for current control was formed between TFT4707 for power control, and EL element 4708. Moreover, as for TFT4707 for power control, it is desirable to consider as the same structure as TFT4704 for current control, or to carry out a serial by the same barrier layer, and to form.
[0163] Moreover, drawing 13 (A) is an example at the time of making the current supply source line 4706 common between two pixels. That is, the description is formed so that two pixels may serve as axial symmetry focusing on the current supply source line 4706. In this case, since the number of a current supply source line can be reduced, the pixel section can be further made highly minute.
[0164] Moreover, drawing 13 (B) is an example at the time of forming the current supply source line 4710 in parallel with the gate wiring 4703, and forming the gate wiring 4711 for power control in parallel with source wiring 4701. In addition, although it has structure established so that the current supply source line 4710 and the gate wiring 4703 might not lap in drawing 13 (B), if it is wiring formed in the layer from which both differ, it can also prepare so that it may lap through an insulator layer. In this case, since the current supply source line 4710 and the gate wiring 4703 can be made to share monopoly area, the pixel section can be further made highly minute.
[0165] In addition, the configuration of this example can be freely combined with any configuration of examples 1-10.
[0166] [Example 14] This example shows the example of the pixel structure of EL display of this invention to drawing 14 (A) and (B). in addition, this example -- setting -- 4801 -- the source wiring of TFT4802 for switching, and 4803 -- gate wiring of TFT4802 for switching, and 4804 -- in a capacitor (omitting is also possible) and 4806, TFT for elimination and 4808 make it as gate wiring for elimination, and 4809 makes a current supply source line and 4807 an EL element for TFT for current control, and 4805. About actuation of TFT4807 for elimination, it is good to refer to Japanese Patent Application No. No. 338786 [11 to].
[0167] It can connect with the gate of TFT4804 for current control, and the drain of TFT4807 for elimination can change now compulsorily the gate voltage of TFT4804 for current control. In addition, although TFT4807 for elimination is good also as a p channel mold TFT also as an n channel mold TFT, it is desirable to consider as the same structure as TFT4802 for switching so that the OFF state current can be made small.
[0168] Moreover, drawing 14 (A) is an example at the time of making the current supply source line 4806 common between two pixels. That is, the description is formed so that two pixels may serve as axial symmetry focusing on the current supply source line 4806. In this case, since the number of a current supply source line can be reduced, the pixel section can be further made highly minute.
[0169] Moreover, drawing 14 (B) is an example at the time of forming the current supply source line 4810 in parallel with the gate wiring 4803, and forming the gate wiring 4811 for elimination in parallel with source wiring 4801. In addition, although it has structure established so that the current supply source line 4810 and the gate wiring 4803 might not lap in drawing 14 (B), if it is wiring formed in the layer from which both differ, it can also prepare so that it may lap through an insulator layer. In this case, since the current supply source line 4810 and the gate wiring 4803 can be made to share monopoly area, the pixel section can be further made highly minute.
[0170] In addition, the configuration of this example can be freely combined with any configuration of examples 1-10.
[0171] [Example 15] EL display of this invention is good also as structure which prepared how many TFT(s) in the pixel. Although examples 13 and 14 show the example which prepared three TFT(s), four thru/or six TFT(s) may be prepared. This invention can be carried out without being limited to the pixel structure of EL display.
[0172] In addition, the configuration of this example can be freely combined with any configuration of examples 1-10.
[0173] [Example 16] EL display which carried out and formed this invention can be used as a display of various electric appliances. For example, it is good to use the display which built EL indicating equipment of this invention of 20-60 inches of vertical angles into the case for appreciating TV broadcast etc. In addition, all displays for information displays, such as a PC monitor, a display for TV broadcast reception, and a display for an advertising display, are included in the display which built EL indicating equipment into the case.
[0174] Moreover, as an electric appliance of other this inventions, a video camera, a digital camera, a goggles mold display (head mount display), a navigation system, music regenerative apparatus (a car audio, audio component stereo, etc.), a note type personal computer, a game device, a Personal Digital Assistant (a mobile computer, a cellular phone, a handheld game machine, or digital book), and picture reproducer (equipment equipped with the display which reproduces the image recorded on the record medium and displays the image) are mentioned. The example of these electric appliances is shown in drawing 15 and drawing 16 .
[0175] Drawing 15 (A) is the display which built EL indicating equipment into the case, and contains a case 2001, susceptor 2002, and a display 2003. EL display of this invention can be used for a display 2003. Since it is a spontaneous light type, such a display has an unnecessary back light, and it can be made into a display thinner than a

liquid crystal display.
[0176] Drawing 15 (B) is a video camera and contains a body 2101, a display 2102, the voice input section 2103, the actuation switch 2104, a dc-battery 2105, and the television section 2106. EL display of this invention can be used for a display 2102.
[0177] Drawing 15 (C) is a part of EL display (right one side) of a head installation mold, and contains a body 2201, a signal cable 2202, the head fixed band 2203, a display 2204, optical system 2205, and luminescence equipment 2206. This invention can be used for the EL display 2206.
[0178] drawing 15 -- (-- D --) -- a record medium -- having had -- picture reproducer (specifically DVD regenerative apparatus) -- it is -- a body -- 2301 -- record media (DVD etc.) -- 2302 -- actuation -- a switch -- 2303 -- a display -- (-- a --) -- 2304 -- a display -- (-- b --) -- 2305 -- containing . Although a display (a) mainly displays image information and a display (b) mainly displays text, EL display of this invention can be used for these displays (a) and (b). In addition, a home video game machine machine etc. is contained in the picture reproducer equipped with the record medium.
[0179] Drawing 15 (E) is a pocket mold (mobile) computer, and contains a body 2401, the camera section 2402, the television section 2403, the actuation switch 2404, and a display 2405. EL display of this invention can be used for a display 2405.
[0180] Drawing 15 (F) is a personal computer and contains a body 2501, a case 2502, a display 2503, and a keyboard 2504. EL display of this invention can be used for a display 2503.
[0181] In addition, if luminescence brightness will become still higher in the future, it will also become possible to carry out expansion projection of the light containing the outputted image information with a lens, an optical fiber, etc., and to use for the projector of a front mold or a rear mold.
[0182] Moreover, in order that the part which is emitting light may consume power, as for luminescence equipment, it is desirable to display information that the amount of light-emitting part decreases as much as possible. Therefore, when using luminescence equipment for the display which is mainly concerned with text like a Personal Digital Assistant, especially a cellular phone and a music regenerative apparatus, it is desirable to drive so that text may be formed by part for a light-emitting part by making a part for a non-light-emitting part into a background.
[0183] Drawing 16 (A) is a cellular phone and contains a body 2601, the voice output section 2602, the voice input section 2603, a display 2604, the actuation switch 2605, and an antenna 2606 here. EL display of this invention can be used for a display 2604. In addition, a display 2604 can stop the power consumption of a cellular phone by displaying a white alphabetic character on a black background.
[0184] Moreover, drawing 16 (B) is a car audio and includes a body 2701, a display 2702, and the actuation switches 2703 and 2704 in a music regenerative apparatus and a concrete target. EL display of this invention can be used for a display 2702. Moreover, although this example shows the car audio for mount, you may use for a pocket mold or a music regenerative apparatus for home use. In addition, a display 2704 can stop power consumption by displaying a white alphabetic character on a black background. Especially this is effective in the music regenerative apparatus of a pocket mold.
[0185] As mentioned above, the applicability of this invention is very wide, and using for the electric appliance of all fields is possible. Moreover, the electric appliance of this example may use EL display of which configuration shown in examples 1-15.
[0186]
[Effect of the Invention] By using this invention, it can become possible to arrange TFT of the suitable engine performance on the same insulator according to the specification which a component searches for, and the engine performance of operation and dependability of EL display can be raised sharply.
[0187] The TFT structure of specifically thinking as important it being the TFT structure and the low OFF state current value which think a working speed as important can be properly used on the same insulator. TFT for switching which this arranges to the pixel of EL indicating equipment can make an OFF state current value low enough, and TFT for current control can make an OFF state current value low enough while preventing degradation by hot carrier impregnation.
[0188] Moreover, by using such an EL indicating equipment as a display display, image quality is good and it becomes possible to produce a durable (for it to be reliable) application product (electric appliance).

[Translation done.]

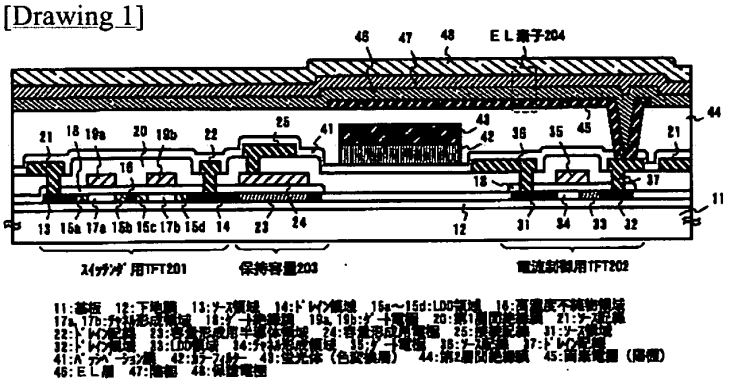
* NOTICES *

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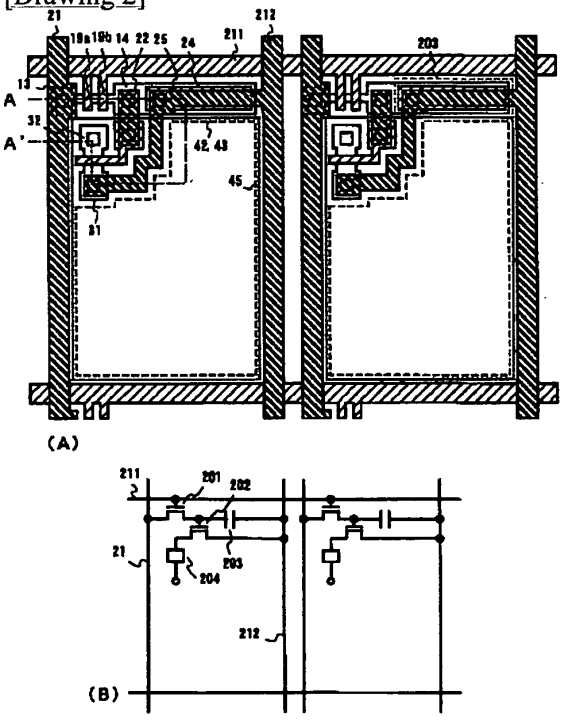
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

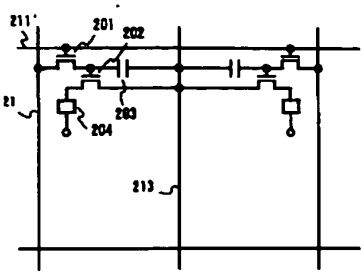
[Drawing 1]



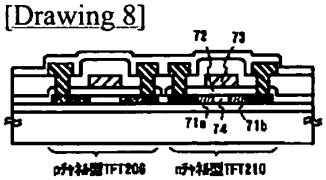
[Drawing 2]



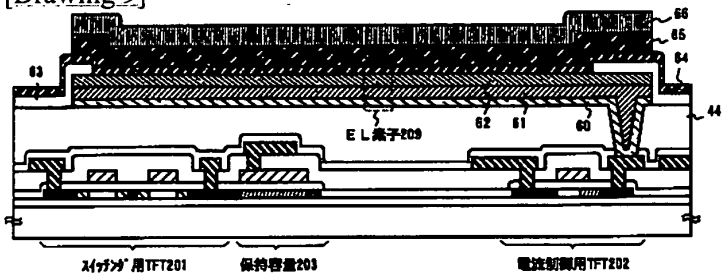
[Drawing 7]



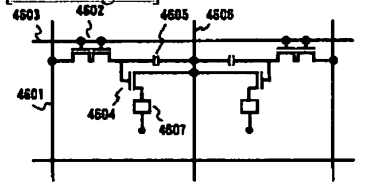
[Drawing 8]



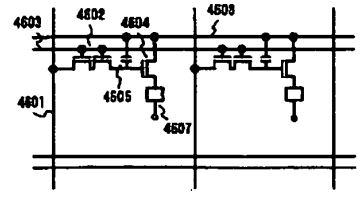
[Drawing 9]



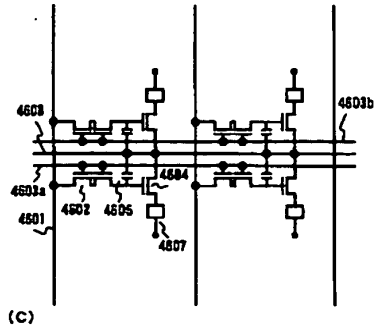
[Drawing 12]



(A)

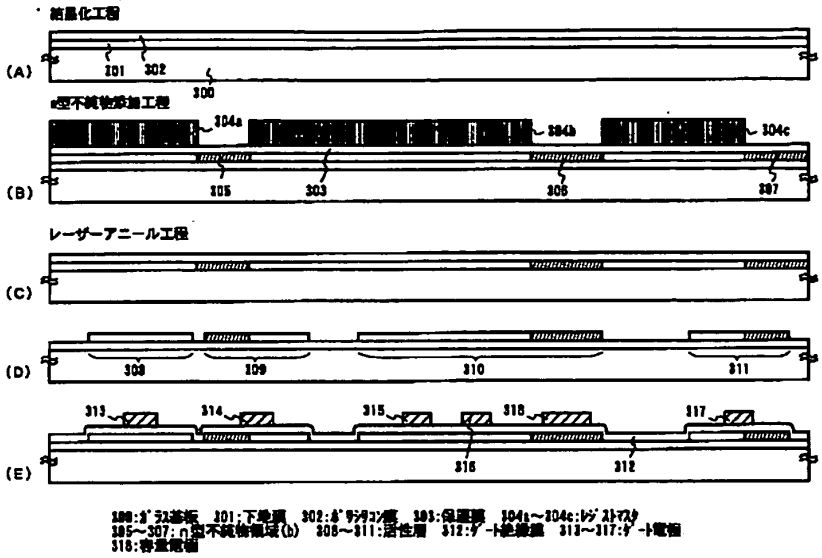


(B)

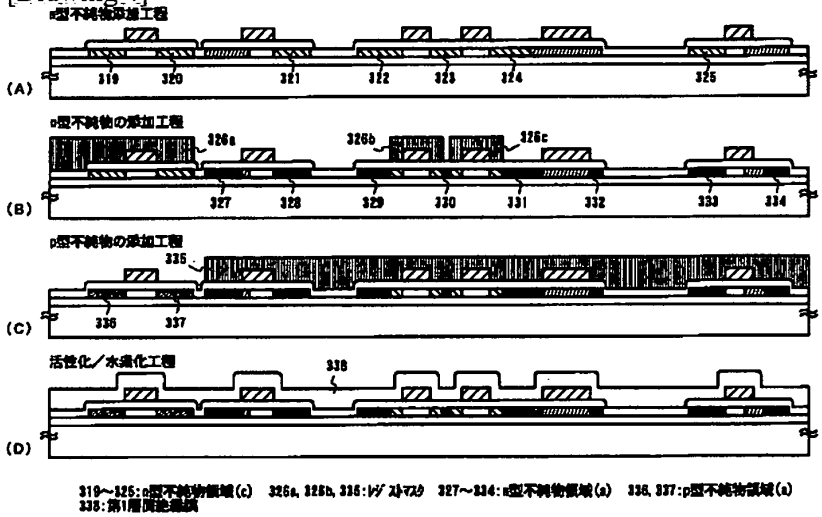


(C)

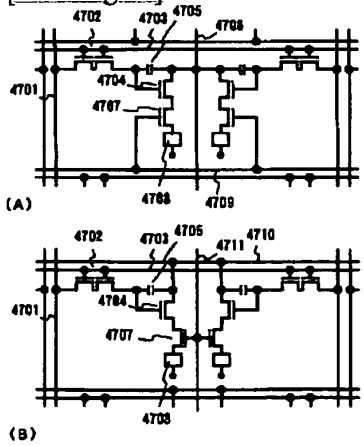
[Drawing 3]



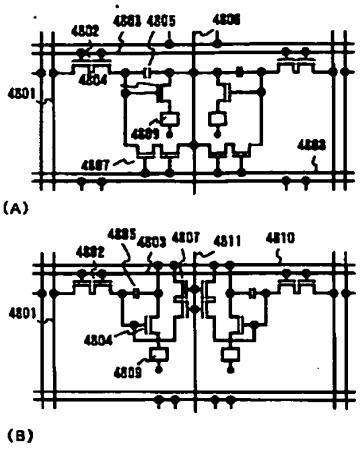
[Drawing 4]



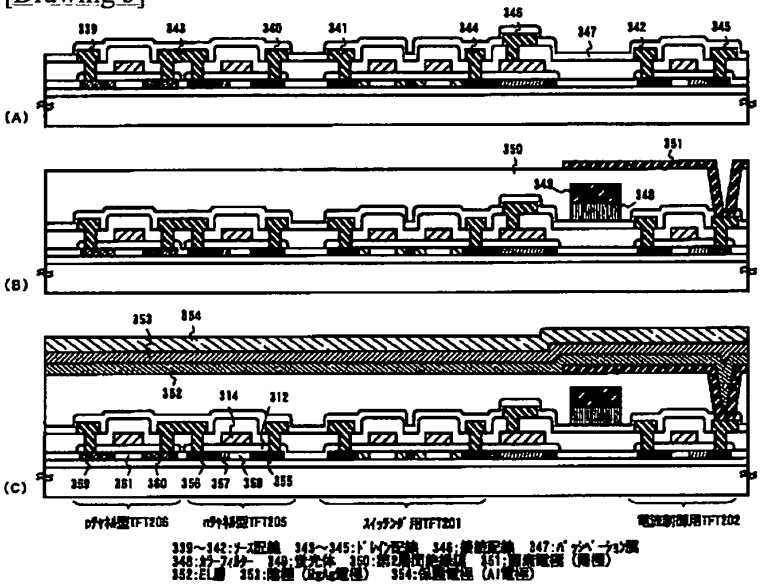
[Drawing 13]



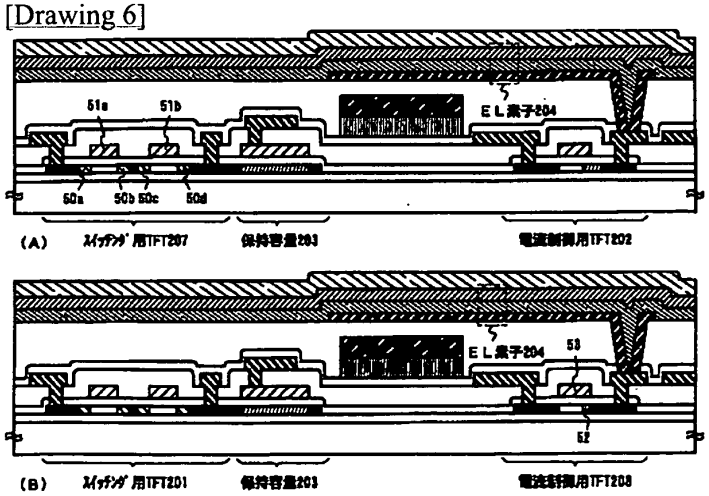
[Drawing 14]



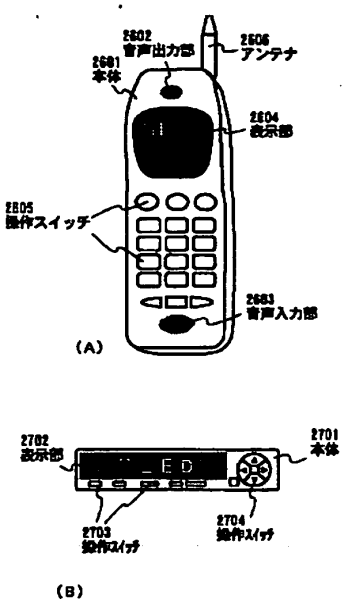
[Drawing 5]



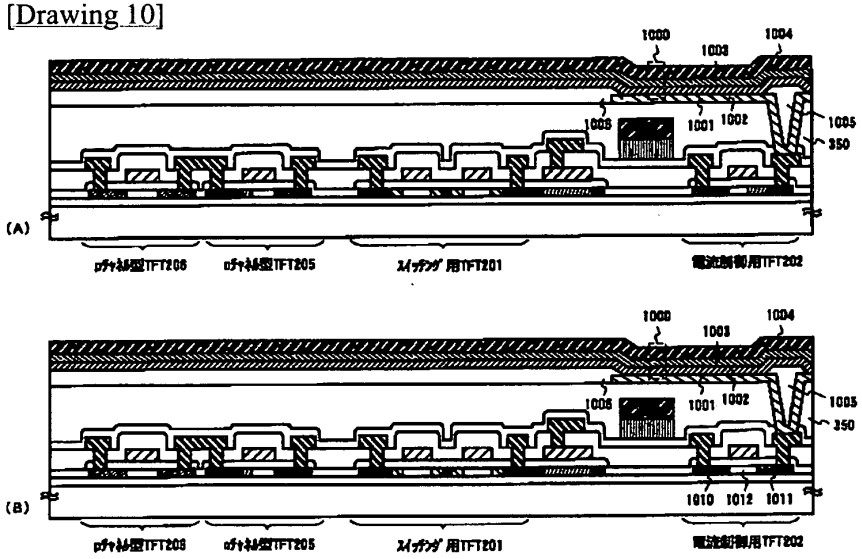
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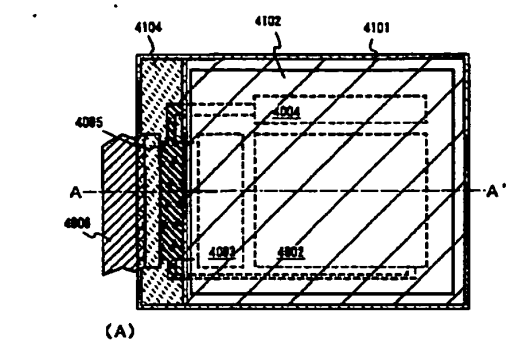
[Drawing 16]



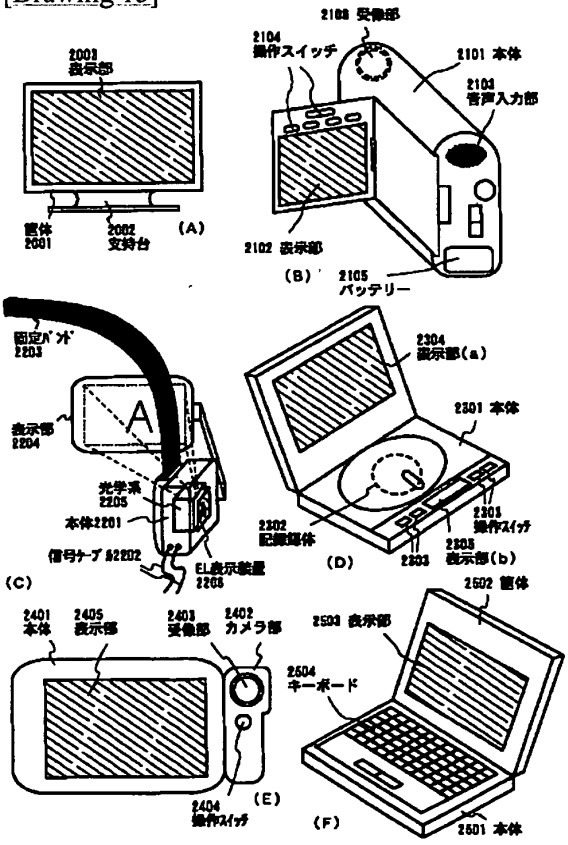
[Drawing 10]



[Drawing 11]



[Drawing 15]



[Translation done.]

* NOTICES *

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CORRECTION OR AMENDMENT

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G09F   9/30    338
365
H01L  29/786
21/336
// H05B  33/14
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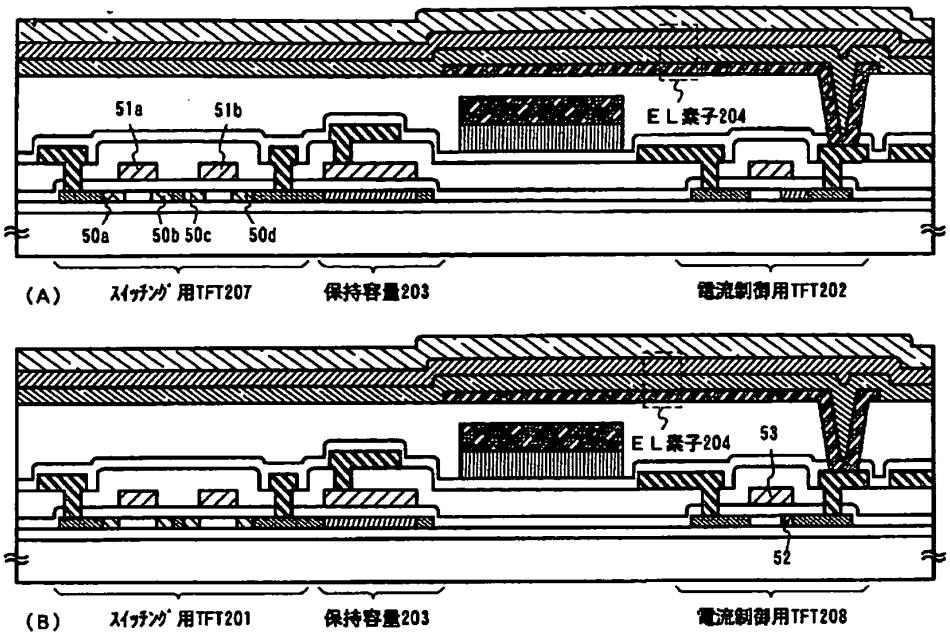
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G09F   9/30    338
365 Z
H05B  33/14        A
H01L  29/78    612 B
616 A
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[Procedure revision]
[Filing Date] February 4, Heisei 15 (2003. 2.4)
[Procedure amendment 1]
[Document to be Amended] Specification
[Item(s) to be Amended] Claim
[Method of Amendment] Modification
[Proposed Amendment]
[Claim(s)]
[Claim 1] In the electronic instrument which has the EL element connected to the 1st TFT for switching, the 2nd TFT for current control, and said 2nd TFT in 1 pixel,
The LDD field of said 1st TFT is formed so that it may not lap with the gate electrode of this 1st TFT on both sides of gate dielectric film,
The LDD field of said 2nd TFT is an electronic instrument characterized by being formed so that a part or all may lap with the gate electrode of this 2nd TFT on both sides of gate dielectric film.
[Claim 2] In the electronic instrument which has the EL element connected to the 1st TFT for switching, the 2nd TFT for current control, and said 2nd TFT in 1 pixel,
The LDD field of said 1st TFT is formed so that a part may lap with the gate electrode of this 1st TFT on both sides of gate dielectric film,
The LDD field of said 2nd TFT is an electronic instrument characterized by being formed so that a part or all may lap with the gate electrode of this 2nd TFT on both sides of gate dielectric film.

[Claim 3] In the electronic instrument which contains the pixel section and the drive circuit section on the same insulator,
Said drive circuit section has the n channel mold TFT formed so that some or all of a LDD field might lap with a gate electrode on both sides of gate dielectric film,
Said pixel section has a pixel containing the EL element connected to the 1st TFT for switching, the 2nd TFT for current control, and said 2nd TFT,
The LDD field of said 1st TFT is formed so that it may not lap with the gate electrode of this 1st TFT on both sides of gate dielectric film,
The LDD field of said 2nd TFT is an electronic instrument characterized by being formed so that a part or all may lap with the gate electrode of this 2nd TFT on both sides of gate dielectric film.
[Claim 4] In the electronic instrument which contains the pixel section and the drive circuit section on the same insulator,
Said drive circuit section has the n channel mold TFT formed so that some or all of a LDD field might lap with a gate electrode on both sides of gate dielectric film,
Said pixel section has a pixel containing the EL element connected to the 1st TFT for switching, the 2nd TFT for current control, and said 2nd TFT,
The LDD field of said 1st TFT is formed so that a part may lap with the gate electrode of this 1st TFT on both sides of gate dielectric film,
The LDD field of said 2nd TFT is an electronic instrument characterized by being formed so that a part or all may lap with the gate electrode of this 2nd TFT on both sides of gate dielectric film.
[Claim 5] In the electronic instrument which has the EL element connected to the 1st TFT for switching, the 2nd TFT for current control, and said 2nd TFT in 1 pixel,
It is the electronic instrument characterized by for said 1st TFT being the multi-gate structure of having two or more gate electrodes, forming a LDD field so that it may not lap with a gate electrode on both sides of gate dielectric film, and forming the LDD field of said 2nd TFT so that a part or all may lap with a gate electrode on both sides of gate dielectric film.
[Claim 6] In the electronic instrument which has the EL element connected to the 1st TFT for switching, the 2nd TFT for current control, and said 2nd TFT in 1 pixel,
Said 1st TFT is the multi-gate structure of having two or more gate electrodes, and a LDD field is formed so that a part may lap with a gate electrode on both sides of gate dielectric film,
The LDD field of said 2nd TFT is an electronic instrument characterized by being formed so that a part or all may lap with a gate electrode on both sides of gate dielectric film.
[Claim 7] In the electronic instrument which contains the pixel section and the drive circuit section on the same insulator,
Said drive circuit section has the n channel mold TFT formed so that some or all of a LDD field might lap with a gate electrode on both sides of gate dielectric film,
Said pixel section has a pixel containing the EL element connected to the 1st TFT for switching, the 2nd TFT for current control, and said 2nd TFT,
Said 1st TFT is the multi-gate structure of having two or more gate electrodes, and a LDD field is formed so that it may not lap with a gate electrode on both sides of gate dielectric film,
The LDD field of said 2nd TFT is an electronic instrument characterized by being formed so that a part or all may lap with a gate electrode on both sides of gate dielectric film.
[Claim 8] In the electronic instrument which contains the pixel section and the drive circuit section on the same insulator,
Said drive circuit section has the n channel mold TFT formed so that some or all of a LDD field might lap with a gate electrode on both sides of gate dielectric film,
Said pixel section has a pixel containing the EL element connected to the 1st TFT for switching, the 2nd TFT for current control, and said 2nd TFT,
Said 1st TFT is the multi-gate structure of having two or more gate electrodes, and a LDD field is formed so that a part may lap with a gate electrode on both sides of gate dielectric film,
The LDD field of said 2nd TFT is an electronic instrument characterized by being formed so that a part or all may lap with a gate electrode on both sides of gate dielectric film.
[Claim 9] The die length of the field which lapped with the gate electrode in the LDD field of said 2nd TFT in any 1 of claim 1 thru/or claims 8 is an electronic instrument characterized by being 0.1-3 micrometers.

[Claim 10] The electronic instrument characterized by containing n mold impurity element by one 2 to 10 times the concentration of this compared with the LDD field of said 1st TFT in the LDD field of said 2nd TFT in any 1 of claim 1 thru/or claims 9.
[Claim 11] The electronic instrument characterized by containing n mold impurity element in the LDD field of said 2nd TFT by the density range of 2x1016 - 5x1019 atoms/cm3, and containing n mold impurity element in the LDD field of said 1st TFT in any 1 of claim 1 thru/or claims 9 by the density range of 1x1016 - 5x1018 atoms/cm3.
[Claim 12] In the electronic instrument which has the EL element connected to the 1st TFT for switching, the 2nd TFT for current control, and said 2nd TFT in 1 pixel,
The LDD field of said 1st TFT is formed so that it may not lap with the gate electrode of this 1st TFT on both sides of gate dielectric film,
The electronic instrument characterized by not forming the LDD field in said 2nd TFT.
[Claim 13] In the electronic instrument which has the EL element connected to the 1st TFT for switching, the 2nd TFT for current control, and said 2nd TFT in 1 pixel,
The LDD field of said 1st TFT is formed so that a part may lap with the gate electrode of this 1st TFT on both sides of gate dielectric film,
The electronic instrument characterized by not forming the LDD field in said 2nd TFT.
[Claim 14] In the electronic instrument which has the EL element connected to the 1st TFT for switching, the 2nd TFT for current control, and said 2nd TFT in 1 pixel,
Said 1st TFT is an electronic instrument characterized by being the multi-gate structure of having two or more gate electrodes, and for a LDD field sandwiching gate dielectric film, being formed so that it may not lap with a gate electrode, and not forming the LDD field in said 2nd TFT.
[Claim 15] In the electronic instrument which has the EL element connected to the 1st TFT for switching, the 2nd TFT for current control, and said 2nd TFT in 1 pixel,
Said 1st TFT is the multi-gate structure of having two or more gate electrodes, and a LDD field is formed so that a part may lap with a gate electrode on both sides of gate dielectric film,
The electronic instrument characterized by not forming the LDD field in said 2nd TFT.
[Claim 16] It is the electronic instrument characterized by forming said EL element on the wrap flattening film in said the 1st TFT and said 2nd TFT in any 1 of claim 1 thru/or claims 15.
[Claim 17] The electronic instrument according to claim 1 to 16 characterized by being used for the display of the display for information displays, a video camera, a digital camera, a goggles mold display, a navigation system, a music regenerative apparatus, a note type personal computer, a game device, a Personal Digital Assistant, or picture reproducer.
[Claim 18] The electric appliance characterized by using an electronic instrument according to claim 1 to 16 for a display.
[Procedure amendment 2]
[Document to be Amended] DRAWINGS
[Item(s) to be Amended] drawing 6
[Method of Amendment] Modification
[Proposed Amendment]
[Drawing 6]



[Translation done.]

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Ｈ０１Ｌ　29/786		Ｈ０５Ｂ　33/14	Ａ	
21/336		Ｈ０１Ｌ　29/78	６１２Ｂ	
// Ｈ０５Ｂ　33/14			６１６Ａ	

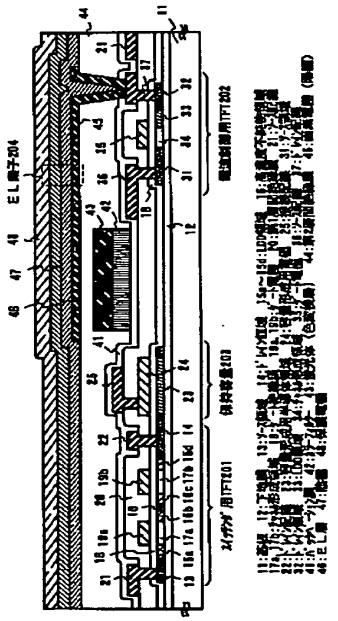
審査請求　未請求　請求項の数９　ＯＬ　（全 18 頁）

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(54)【発明の名称】　電子装置及び電気器具

(57)【要約】
【課題】　動作性能および信頼性の高いＥＬ表示装置を提供する。
【解決手段】　画素内に形成されるスイッチング用ＴＦＴ２０１のＬＤＤ領域１５a～１５dは、ゲート電極１９a、１９bに重ならないように形成され、オフ電流値の低減に重点をおいた構造となっている。また、電流制御用ＴＦＴ２０２のＬＤＤ領域３３は、ゲート電極３５に一部が重なるように形成され、ホットキャリア注入の防止とオフ電流値の低減に重点をおいた構造となっている。このように、求める機能に応じて適切なＴＦＴ構造とし、動作性能及び信頼性を高める。



【特許請求の範囲】
【請求項1】第1のTFT、第2のTFT及び前記第2のTFTに接続されたEL素子を一画素内に有する電子装置において、
前記第1のTFTのLDD領域は、該第1のTFTのゲート電極にゲート絶縁膜を挟んで重ならないように形成され、
前記第2のTFTのLDD領域は、該第2のTFTのゲート電極にゲート絶縁膜を挟んで一部若しくは全部が重なるように形成されていることを特徴とする電子装置。
【請求項2】第1のTFT、第2のTFT及び前記第2のTFTに接続されたEL素子を一画素内に有する電子装置において、
前記第1のTFTのLDD領域は、該第1のTFTのゲート電極にゲート絶縁膜を挟んで一部が重なるように形成され、
前記第2のTFTのLDD領域は、該第2のTFTのゲート電極にゲート絶縁膜を挟んで一部若しくは全部が重なるように形成されていることを特徴とする電子装置。
【請求項3】同一の絶縁体上に画素部および駆動回路部を含む電子装置において、
前記駆動回路部は、LDD領域の一部若しくは全部がゲート絶縁膜を挟んでゲート電極に重なるように形成されたnチャネル型TFTを有し、
前記画素部は、第1のTFT、第2のTFT及び前記第2のTFTに接続されたEL素子を含む画素を有し、
前記第1のTFTのLDD領域は、該第1のTFTのゲート電極にゲート絶縁膜を挟んで重ならないように形成され、
前記第2のTFTのLDD領域は、該第2のTFTのゲート電極にゲート絶縁膜を挟んで一部若しくは全部が重なるように形成されていることを特徴とする電子装置。
【請求項4】同一の絶縁体上に画素部および駆動回路部を含む電子装置において、
前記駆動回路部は、LDD領域の一部若しくは全部がゲート絶縁膜を挟んでゲート電極に重なるように形成されたnチャネル型TFTを有し、
前記画素部は、第1のTFT、第2のTFT及び前記第2のTFTに接続されたEL素子を含む画素を有し、
前記第1のTFTのLDD領域は、該第1のTFTのゲート電極にゲート絶縁膜を挟んで一部が重なるように形成され、
前記第2のTFTのLDD領域は、該第2のTFTのゲート電極にゲート絶縁膜を挟んで一部若しくは全部が重なるように形成されていることを特徴とする電子装置。
【請求項5】請求項1乃至請求項4のいずれか一において、前記第1のTFTはスイッチング用素子であり、前記第2のTFTは電流制御用素子であることを特徴とする電子装置。
【請求項6】請求項1乃至請求項4のいずれか一において、前記第2のTFTのLDD領域には、前記第1のTFTのLDD領域に比べて2～10倍の濃度でn型不純物元素が含まれることを特徴とする電子装置。
【請求項7】請求項1乃至請求項4のいずれか一において、前記第2のTFTのLDD領域には2×10^{16}～5×10^{19}atoms/cm^{3}の濃度範囲でn型不純物元素が含まれ、前記第1のTFTのLDD領域には1×10^{16}～5×10^{18}atoms/cm^{3}の濃度範囲でn型不純物元素が含まれていることを特徴とする電子装置。
【請求項8】請求項1乃至請求項4のいずれか一において、前記EL素子は前記第1のTFTおよび前記第2のTFTを覆う平坦化膜の上に形成されていることを特徴とする電子装置。
【請求項9】請求項1乃至請求項8のいずれか一に記載の電子装置を表示部に用いたことを特徴とする電気器具。
【発明の詳細な説明】
【0001】
【発明の属する技術分野】本願発明は半導体素子（半導体薄膜を用いた素子）を基板上に作り込んで形成された電子装置およびその電子装置を表示部として用いた電気器具に関する。特に、本発明は電子装置としてEL（エレクトロルミネッセンス）表示装置に実施することが有効な技術である。
【0002】
【従来の技術】近年、基板上にTFTを形成する技術が大幅に進歩し、アクティブマトリクス型表示装置への応用開発が進められている。特に、ポリシリコン膜を用いたTFTは、従来のアモルファスシリコン膜を用いたTFTよりも電界効果移動度（モビリティともいう）が高いので、高速動作が可能である。そのため、従来、基板外の駆動回路で行っていた画素の制御を、画素と同一の基板（絶縁体）上に形成した駆動回路で行うことが可能となっている。
【0003】このようなアクティブマトリクス型表示装置は、同一基板上に様々な回路や素子を作り込むことで製造コストの低減、表示装置の小型化、歩留まりの上昇、スループットの低減など、様々な利点が得られるとして注目されている。
【0004】しかし、アクティブマトリクス型表示装置の基板上には様々な機能を有する回路や素子部が形成される。従って、回路又は素子をTFTで形成するにあたって、それぞれの回路又は素子が必要とするTFTの性能も異なってくる。例えば、タイミング信号を形成するシフトレジスタなどには動作速度の早いTFTが求められ、電荷蓄積のためのスイッチング素子にはオフ電流値（TFTがオフ動作にある時に流れるドレイン電流値）の十分に低いTFTが求められる。
【0005】このような場合、同一構造のTFTだけでは全ての回路又は素子が求める性能を確保することが困

難となり、アクティブマトリクス型表示装置の性能を向上させる上で大きな弊害となる。

【0006】

【発明が解決しようとする課題】本発明は同一の絶縁体上に画素部と駆動回路部とを有するアクティブマトリクス型の電子装置において、ＴＦＴで形成される回路又は素子が求める性能に応じて適切な構造のＴＦＴを用い、動作性能及び信頼性の高い電子装置を提供することを課題とする。

【0007】そして、電子装置（特にアクティブマトリクス型ＥＬ表示装置）の画質を向上させることにより、それを表示部（表示用ディスプレイ）として用いた電子機器（電気器具）の品質を向上させることを課題とする。

【0008】

【課題を解決するための手段】上記問題点を解決するために本発明では、ＥＬ表示装置の各画素に含まれる素子が求める機能を鑑みて、最適な構造のＴＦＴを割り当てることを主旨としている。即ち、同一画素内に異なる構造のＴＦＴが存在することになる。

【0009】具体的には、オフ電流値を十分に低くさせることを最重要課題とする素子（スイッチング用素子など）は、動作速度よりもオフ電流値を低減させることに重点を置いたＴＦＴ構造が望ましい。また、大電流を流すことを最重要課題とする素子（電流制御用素子など）は、オフ電流値を低減させることよりも、大電流を流すこと及びそれと同時に顕著な問題となるホットキャリア注入による劣化を抑制することに重点を置いたＴＦＴ構造が望ましい。

【0010】本発明は、同一の絶縁体上で上記のようなＴＦＴの使い分けを行うことによって、ＥＬ表示装置の動作性能の向上と信頼性の向上とを可能とする。なお、本発明の思想は、画素部に限ったものではなく、画素部およびその画素部を駆動する駆動回路部を含めてＴＦＴ構造の最適化を図る点にも特徴がある。

【0011】

【発明の実施の形態】本発明の実施の形態について、図１、図２を用いて説明する。図１に示したのは本発明であるＥＬ表示装置の画素の断面図であり、図２（Ａ）はその上面図、図２（Ｂ）はその回路構成である。実際にはこのような画素がマトリクス状に複数配列されて画素部（画像表示部）が形成される。

【0012】なお、図１の断面図は図２（Ａ）に示した上面図においてＡ－Ａ’で切断した切断面を示している。ここでは図１及び図２で共通の符号を用いているので、適宜両図面を参照すると良い。また、図２の上面図では二つの画素を図示しているが、どちらも同じ構造である。

【0013】図１において、１１は基板、１２は下地膜（絶縁体）である。基板１１としてはガラス基板、ガラスセラミックス基板、石英基板、シリコン基板、セラミックス基板、金属基板若しくはプラスチック基板（プラスチックフィルムも含む）を用いることができる。

【0014】また、下地膜１２は特に可動イオンを含む基板や導電性を有する基板を用いる場合に有効であるが、石英基板には設けなくても構わない。下地膜１２としては、珪素（シリコン）を含む絶縁膜を設ければ良い。なお、本明細書において「珪素を含む絶縁膜」とは、具体的には酸化珪素膜、窒化珪素膜若しくは窒化酸化珪素膜（ＳｉＯｘＮｙで示される）など珪素、酸素若しくは窒素を所定の割合で含む絶縁膜を指す。

【0015】ここでは画素内に二つのＴＦＴを形成している。２０１はスイッチング素子として機能するＴＦＴ（以下、スイッチング用ＴＦＴという）、２０２はＥＬ素子へ流す電流量を制御するＴＦＴ（以下、電流制御用ＴＦＴという）であり、どちらもｎチャネル型ＴＦＴで形成されている。

【0016】スイッチング用ＴＦＴ２０１は、ソース領域１３、ドレイン領域１４、ＬＤＤ領域１５a～１５d、高濃度不純物領域１６及びチャネル形成領域１７a、１７bを含む活性層、ゲート絶縁膜１８、ゲート電極１９a、ゲート電極１９b、第１層間絶縁膜２０、ソース配線２１並びにドレイン配線２２を有して形成される。なお、図２に示すようにゲート電極１９a、１９bは同一のゲート配線２１１を幹としたダブルゲート構造となっている。

【0017】活性層は結晶構造を含む半導体膜で形成される。即ち、単結晶半導体膜でも良いし、多結晶半導体膜や微結晶半導体膜でも良い。また、ゲート絶縁膜１８は珪素を含む絶縁膜で形成すれば良い。また、ゲート電極、ソース配線若しくはドレイン配線としてはあらゆる導電膜を用いることができる。

【0018】また、スイッチング用ＴＦＴ２０１には保持容量（ｽﾄﾚｰｼﾞ ｷｬﾊﾟｼﾀ）２０３が接続されている（図２参照）。保持容量２０３は、ドレイン領域１４と電気的に接続された容量形成用半導体領域２３とゲート絶縁膜１８（保持容量２０３を形成する領域では容量形成用の誘電体として機能する）と容量形成用電極２４とで形成される。なお、接続配線２５は、容量形成用電極２４に固定電位（ここでは接地電位）を与えるための配線であり、ソース配線２１やドレイン配線２２と同時に形成され、電流供給線２１２に接続されている。

【0019】この時、スイッチング用ＴＦＴ２０１においては、ＬＤＤ領域１５a～１５dは、ゲート絶縁膜１８を挟んでゲート電極１９a、ゲート電極１９bに重ならないように設ける。このような構造は一般的にＬＤＤ構造と呼ばれている。

【0020】スイッチング用ＴＦＴ２０１は、選択時にビデオ信号（画像情報を含む信号）に対応する電荷を保持容量２０３へと蓄積する。そして非選択時は常にその

電荷を保持しなければならないので、オフ電流値による電荷漏れは極力防がなければならない。そういった意味で、スイッチング用ＴＦＴ２０１はオフ電流値を低減することを最重要課題として設計しなければならない。

【００２１】なお、チャネル形成領域とＬＤＤ領域との間にオフセット領域（チャネル形成領域と同一組成の半導体層でなり、ゲート電圧が印加されない領域）を設けることはオフ電流値を下げる上でさらに好ましい。また、二つ以上のゲート電極を有するマルチゲート構造の場合、チャネル形成領域の間に設けられた高濃度不純物領域がオフ電流値の低減に効果的である。なお、本実施例のようにマルチゲート構造とすることが望ましいが、シングルゲート構造とすることもできる。

【００２２】次に、電流制御用ＴＦＴ２０２は、ソース領域３１、ドレイン領域３２、ＬＤＤ領域３３及びチャネル形成領域３４を含む活性層、ゲート絶縁膜１８、ゲート電極３５、第１層間絶縁膜２０、ソース配線３６並びにドレイン配線３７を有して形成される。なお、ゲート電極３５はシングルゲート構造となっているが、マルチゲート構造であっても良い。

【００２３】図２に示すように、ゲート電極３５はスイッチング用ＴＦＴ２０１のドレイン領域１４とドレイン配線（接続配線とも言える）２２を介して電気的に接続されている。また、ソース配線３６は接続配線２５と一体化しており、同様にして電流供給線２１２に接続される。

【００２４】この電流制御用ＴＦＴ２０２の特徴は、ドレイン領域３２とチャネル形成領域３４との間にＬＤＤ領域３３が設けられ、且つ、ＬＤＤ領域３３がゲート絶縁膜１８を挟んでゲート電極３５に重なっている領域と重なっていない領域とを有する点である。

【００２５】電流制御用ＴＦＴ２０２は、ＥＬ素子２０４を発光させるための電流を供給すると同時に、その供給量を制御して階調表示を可能とする。そのため、大電流を流しても劣化しないようにホットキャリア注入による劣化対策を講じておく必要がある。また、黒色を表示する際は、電流制御用ＴＦＴ２０２をオフ状態にしておくが、その際、オフ電流値が高いときれいな黒色表示ができなくなり、コントラストの低下を招く。従って、オフ電流値も抑える必要がある。

【００２６】ホットキャリア注入による劣化に関しては、ゲート電極に対してＬＤＤ領域が重なった構造が非常に効果的であることが知られている。しかしながら、ＬＤＤ領域全体をゲート電極に重ねてしまうとオフ電流値が増加してしまうため、本発明者らはゲート電極に重ならないＬＤＤ領域を設けるという新規な構造によって、ホットキャリア対策とオフ電流値対策とを同時に解決している。

【００２７】この時、ゲート電極に重なったＬＤＤ領域の長さは０．１～３μm（好ましくは０．３～１．５μm）にすれば良い。長すぎては寄生容量を大きくしてしまい、短すぎてはホットキャリアを防止する効果が弱くなってしまう。また、ゲート電極に重ならないＬＤＤ領域の長さは１．０～３．５μｍ（好ましくは１．５～２．０μｍ）にすれば良い。長すぎると十分な電流を流せなくなり、短すぎるとオフ電流値を低減する効果が弱くなる。

【００２８】また、上記構造においてゲート電極とＬＤＤ領域とが重なった領域では寄生容量が形成されてしまうため、ソース領域３１とチャネル形成領域３４との間には設けない方が好ましい。電流制御用ＴＦＴはキャリア（ここでは電子）の流れる方向が常に同一であるので、ドレイン領域側のみにＬＤＤ領域を設けておけば十分である。

【００２９】以上のように、画素内には機能に応じて異なる二種類の構造のＴＦＴが配置されている。なお、ここで示した例では、スイッチング用ＴＦＴ２０１、電流制御用ＴＦＴ２０２共にｎチャネル型ＴＦＴで形成されている。ｎチャネル型ＴＦＴはＴＦＴサイズがｐチャネル型ＴＦＴよりも小さくできるので、ＥＬ素子の有効発光面積を大きくする上で非常に有利である。

【００３０】ｐチャネル型ＴＦＴはホットキャリア注入が殆ど問題にならず、オフ電流値が低いといった利点があって、スイッチング用ＴＦＴとして用いる例や電流制御用ＴＦＴとして用いる例が既に報告されている。しかしながら本願発明では、ＬＤＤ領域の位置を異ならせた構造とすることでｎチャネル型ＴＦＴにおいてもホットキャリア注入の問題とオフ電流値の問題を解決し、全ての画素内のＴＦＴ全てをｎチャネル型ＴＦＴとしている点にも特徴がある。

【００３１】また、４１はパッシベーション膜であり、窒化珪素膜若しくは窒化酸化珪素膜を用いる。４２はカラーフィルター、４３は蛍光体（蛍光色素層ともいう）である。どちらも同色の組み合わせで、赤（Ｒ）、緑（Ｇ）若しくは青（Ｂ）の色素を含む。カラーフィルター４２は色純度を向上させるために設け、蛍光体４２は色変換を行うために設けられる。

【００３２】なお、ＥＬ表示装置には大きく分けて四つのカラー化表示方式があり、ＲＧＢに対応した三種類のＥＬ素子を形成する方式、白色発光のＥＬ素子とカラーフィルターを組み合わせた方式、青色発光のＥＬ素子と蛍光体（蛍光性の色変換層：ＣＣＭ）とを組み合わせた方式、陰極（対向電極）に透明電極を使用してＲＧＢに対応したＥＬ素子を重ねる方式、がある。

【００３３】図１の構造は青色発光のＥＬ素子と蛍光体とを組み合わせた方式を用いた場合の例である。ここではＥＬ素子２０４として青色発光の発光層を用いて紫外光を含む青色領域の波長をもつ光を形成し、その光によって蛍光体４３を励起して赤、緑若しくは青の光を発生させる。そしてカラーフィルター４２で色純度を上げて

出力する。

【００３４】但し、本願発明は発光方式に関わらず実施することが可能であり、上記四つの全ての方式を本願発明に用いることができる。

【００３５】また、カラーフィルター４２、蛍光体４２を形成した後で、第２層間絶縁膜４３で平坦化を行う。第２層間絶縁膜４４としては、有機樹脂膜が好ましく、ポリイミド、アクリル樹脂もしくはＢＣＢ（ベンゾシクロブテン）を用いると良い。勿論、十分な平坦化が可能であれば、無機膜を用いても良い。

【００３６】４５は透明導電膜でなる画素電極（ＥＬ素子の陽極）であり、第２層間絶縁膜４４及びパッシベーション膜４１にコンタクトホールを開けた後、電流制御用ＴＦＴ２０２のドレイン配線３７に接続されるように形成される。

【００３７】画素電極４５の上には、順次ＥＬ層（有機材料が好ましい）４６、陰極４７、保護電極４８が形成される。ＥＬ層４６は単層又は積層構造で用いることができるが、積層構造で用いる場合が多い。ＥＬ層としては、発光層以外に電子輸送層や正孔輸送層を組み合わせて様々な積層構造が提案されているが、本発明はいずれの構造であっても良い。

【００３８】また、陰極４７としては、仕事関数の小さいマグネシウム（Ｍｇ）、リチウム（Ｌｉ）若しくはカルシウム（Ｃａ）を含む材料を用いる。好ましくはＭｇＡｇ電極を用いれば良い。また、保護電極４８は陰極４７を外部の湿気から保護膜するために設けられる電極であり、アルミニウム（Ａｌ）若しくは銀（Ａｇ）を含む材料が用いられる。

【００３９】なお、ＥＬ層４６及び陰極４７は大気解放せずに連続形成することが望ましい。即ち、ＥＬ層や陰極がどのような積層構造であっても全て連続形成することが望ましい。これはＥＬ層として有機材料を用いる場合、水分に非常に弱いため、大気解放した時の吸湿を避けるためである。さらに、ＥＬ層４６及び陰極４７だけでなく、その上の保護電極４８まで連続形成するとさらに良い。

【００４０】本発明のＥＬ表示装置は以上のような構造の画素からなる画素部を有し、画素内において機能に応じて構造の異なるＴＦＴが配置されている。これによりオフ電流値の十分に低いスイッチング用ＴＦＴと、ホットキャリア注入に強い電流制御用ＴＦＴとが同じ画素内に形成でき、高い信頼性を有し、良好な画像表示が可能なＥＬ表示装置が形成できる。

【００４１】また、本発明はＥＬ表示装置の画素部に限らず、駆動回路部と画素部とを同一基板上に形成したアクティブマトリクス型ＥＬ表示装置の駆動回路部についても同様のことが言える。即ち、駆動回路部と画素部すべてにおいて、回路若しくは素子が求める機能に応じて異なる構造のＴＦＴを配置する点は本発明の主旨の一つである。

【００４２】また、上記駆動回路部若しくは画素部以外に、その他の信号処理回路をも形成する場合にも本発明は実施しうる。その他の信号処理回路としては、信号分割回路、Ｄ／Ａコンバータ、γ補正回路、昇圧回路もしくは差動増幅回路が挙げられる。

【００４３】以上の構成でなる本発明について、以下に示す実施例でもってさらに詳細な説明を行うこととする。

【００４４】〔実施例１〕本発明の実施例について図３～図５を用いて説明する。ここでは、画素部とその周辺に設けられる駆動回路部のＴＦＴを同時に作製する方法について説明する。但し、説明を簡単にするために、駆動回路に関しては基本回路であるＣＭＯＳ回路を図示することとする。

【００４５】まず、図３（Ａ）に示すように、ガラス基板３００上に下地膜３０１を３００ｎｍの厚さに形成する。本実施例では下地膜３０１として窒化酸化珪素膜を積層して用いる。この時、ガラス基板３００に接する方の窒素濃度を１０～２５ｗｔ％としておくと良い。

【００４６】次に下地膜３０１の上に５０ｎｍの厚さの非晶質珪素膜（図示せず）を公知の成膜法で形成する。なお、非晶質珪素膜に限定する必要はなく、非晶質構造を含む半導体膜（微結晶半導体膜を含む）であれば良い。さらに非晶質シリコンゲルマニウム膜などの非晶質構造を含む化合物半導体膜でも良い。また、膜厚は２０～１００ｎｍの厚さであれば良い。

【００４７】そして、公知の技術により非晶質珪素膜を結晶化し、結晶質珪素膜（多結晶シリコン膜若しくはポリシリコン膜ともいう）３０２を形成する。公知の結晶化方法としては、電熱炉を使用した熱結晶化方法、レーザー光を用いたレーザーアニール結晶化法、赤外光を用いたランプアニール結晶化法がある。本実施例では、ＸｅＣｌガスを用いたエキシマレーザー光を用いて結晶化する。

【００４８】なお、本実施例では線状に加工したパルス発振型のエキシマレーザー光を用いるが、矩形であっても良いし、連続発振型のアルゴンレーザー光や連続発振型のエキシマレーザー光を用いることもできる。

【００４９】次に、図３（Ｂ）に示すように、結晶質珪素膜３０２上に酸化珪素膜でなる保護膜３０３を１３０ｎｍの厚さに形成する。この厚さは１００～２００ｎｍ（好ましくは１３０～１７０ｎｍ）の範囲で選べば良い。また、珪素を含む絶縁膜であれば他の膜でも良い。この保護膜３０３は不純物を添加する際に結晶質珪素膜が直接プラズマに曝されないようにするためと、微妙な濃度制御を可能にするために設ける。

【００５０】そして、その上にレジストマスク３０４ａ～３０４ｃを形成し、保護膜３０３を介してｎ型を付与する不純物元素（以下、ｎ型不純物元素という）を添加

する。なお、n型不純物元素としては、代表的には１５族に属する元素、典型的にはリン又は砒素を用いることができる。なお、本実施例ではフォスフィン（PH_3）を質量分離しないでプラズマ励起したプラズマドーピング法を用い、リンを1×10^{18}atoms/cm³の濃度で添加する。勿論、質量分離を行うイオンインプランテーション法を用いても良い。

【００５１】この工程により形成されるn型不純物領域３０５～３０７には、n型不純物元素が2×10^{16}～5×10^{19}atoms/cm³（代表的には5×10^{17}～5×10^{18}atoms/cm³）の濃度で含まれるようにドーズ量を調節する。なお、n型不純物領域３０６は図１に示した容量形成用半導体領域２３に相当する。

【００５２】次に、図３（Ｃ）に示すように、保護膜３０３を除去し、添加した１５族に属する元素の活性化を行う。活性化手段は公知の技術を用いれば良いが、本実施例ではエキシマレーザー光の照射により活性化する。勿論、パルス発振型でも連続発振型でも良いし、エキシマレーザー光に限定する必要はない。但し、添加された不純物元素の活性化が目的であるので、結晶質珪素膜が溶融しない程度のエネルギーで照射することが好ましい。なお、保護膜３０３をつけたままレーザー光を照射しても良い。

【００５３】なお、このレーザー光による不純物元素の活性化に際して、ファーネスアニールまたはランプアニールによる活性化を併用しても構わない。ファーネスアニールによる活性化を行う場合は、基板の耐熱性を考慮して４５０～５５０℃程度の熱処理を行えば良い。また、ファーネスアニールまたはランプアニールのみで活性化を行っても良い。

【００５４】この工程によりn型不純物領域３０５～３０７の端部、即ち、n型不純物領域３０５～３０７の周囲に存在するn型不純物元素を添加していない領域との境界部（接合部）が明確になる。このことは、後にＴＦＴが完成した時点において、ＬＤＤ領域とチャネル形成領域とが非常に良好な接合部を形成しうることを意味する。

【００５５】次に、図３（Ｄ）に示すように、結晶質珪素膜の不要な部分を除去して、島状の半導体膜（以下、活性層という）３０８～３１１を形成する。

【００５６】次に、図３（Ｅ）に示すように、活性層３０８～３１１を覆ってゲート絶縁膜３１２を形成する。ゲート絶縁膜３１２としては、１０～２００ｎｍ、好ましくは５０～１５０ｎｍの厚さの珪素を含む絶縁膜を用いれば良い。これは単層構造でも積層構造でも良い。本実施例では１１０ｎｍ厚の窒化酸化珪素膜を用いる。

【００５７】次に、２００～４００ｎｍ厚の導電膜を形成し、パターニングしてゲート電極３１３～３１７と容量形成用電極３１８を形成する。なお、本明細書ではゲート電極とゲート配線とを区別して説明する場合があるが、電極として機能する部分をゲート電極と呼んでいるだけであり、ゲート配線にゲート電極は含まれていると考えて良い。このことは容量形成用電極も同様であり、電極として機能していない部分は容量形成用配線と呼べば良い。

【００５８】また、ゲート電極は単層の導電膜で形成しても良いが、必要に応じて二層、三層といった積層膜とすることが好ましい。ゲート電極の材料としては公知のあらゆる導電膜を用いることができる。

【００５９】具体的には、タンタル（Ｔａ）、チタン（Ｔｉ）、モリブデン（Ｍｏ）、タングステン（Ｗ）、クロム（Ｃｒ）もしくは導電性を有するシリコン（Ｓｉ）を含む薄膜、またはそれらを窒化した薄膜（代表的には窒化タンタル膜、窒化タングステン膜もしくは窒化チタン膜）、または上記元素を組み合わせた合金膜（代表的にはＭｏ－Ｗ合金もしくはＭｏ－Ｔａ合金）、または上記元素を含むシリサイド膜（代表的にはタングステンシリサイド膜もしくはチタンシリサイド膜）を用いることができる。勿論、これらを単層で用いても積層して用いても良い。

【００６０】本実施例では、５０ｎｍ厚の窒化タンタル（ＴａＮ）膜と、３５０ｎｍ厚のＴａ膜とでなる積層膜を用いる。これはスパッタ法で形成すれば良い。また、スパッタガスとしてＸｅ、Ｎｅ等の不活性ガスを添加すると応力による膜はがれを防止することができる。

【００６１】またこの時、ゲート電極３１４、３１７はそれぞれn型不純物領域３０５、３０７の一部とゲート絶縁膜３１２を挟んで重なるように形成する。この重なった部分が後にゲート電極に重なったＬＤＤ領域となる。なお、ゲート電極３１５、３１６は断面では二つに見えるが、実際は連続的に繋がった一つのパターンから形成されている。

【００６２】また、n型不純物領域３０６の上にはゲート絶縁膜３１２を挟んで容量形成用電極３１８が形成される。この時、ゲート絶縁膜３１２として設けられた絶縁膜は、ここで保持容量の誘電体として用いられ、n型不純物領域（容量形成用半導体領域）３０６、ゲート絶縁膜３１２及び容量形成用電極３１８からなる保持容量が形成される。

【００６３】次に、図４（Ａ）に示すように、ゲート電極３１３～３１７及び容量形成用電極３１８をマスクとして自己整合的にn型不純物元素（本実施例ではリン）を添加する。こうして形成される不純物領域３１９～３２５にはn型不純物領域３０５～３０７の１／２～１／１０（代表的には１／３～１／４）の濃度でリンが添加されるように調節する。具体的には、1×10^{16}～5×10^{18}atoms/cm³（典型的には3×10^{17}～3×10^{18}atoms/cm³）の濃度が好ましい。

【００６４】次に、図４（Ｂ）に示すように、ゲート電極等を覆う形でレジストマスク３２６a～３２６cを形成

し、n型不純物元素（本実施例ではリン）を添加して高濃度にリンを含む不純物領域３２７～３３４を形成する。ここでもフォスフィン（PH_3）を用いたイオンドープ法で行い、この領域のリンの濃度は1×10^{20}～1×10^{21}atoms/cm³（代表的には2×10^{20}～5×10^{21}atoms/cm³）となるように調節する。

【００６５】この工程によってnチャネル型ＴＦＴのソース領域若しくはドレイン領域が形成されるが、スイッチング用ＴＦＴは、図４（Ａ）の工程で形成したn型不純物領域３２２～３２４の一部を残す。この残された領域が、図１におけるスイッチング用ＴＦＴのＬＤＤ領域１５a～１５dに対応する。

【００６６】次に、図４（Ｃ）に示すように、レジストマスク３２６a～３２６cを除去し、新たにレジストマスク３２５を形成する。そして、p型不純物元素（本実施例ではボロン）を添加し、高濃度にボロンを含む不純物領域３３６、３３７を形成する。ここではジボラン（B_2H_6）を用いたイオンドープ法により3×10^{20}～3×10^{21}atoms/cm³（代表的には5×10^{20}～1×10^{21}atoms/cm³）濃度となるようにボロンを添加する。

【００６７】なお、不純物領域３１９、３２０には既に1×10^{20}～1×10^{21}atoms/cm³の濃度でリンが添加されているが、ここで添加されるボロンはその少なくとも３倍以上の濃度で添加される。そのため、予め形成されていたn型の不純物領域は完全にＰ型に反転し、Ｐ型の不純物領域として機能する。

【００６８】次に、図４（Ｄ）に示すように、レジストマスク３３５を除去した後、第１層間絶縁膜３３８を形成する。第１層間絶縁膜３３８としては、珪素を含む絶縁膜を単層で用いるか、珪素を含む絶縁膜を組み合わせた積層膜を用いれば良い。また、膜厚は４００ｎｍ～１．５μmとすれば良い。本実施例では、２００ｎｍ厚の窒化酸化珪素膜の上に８００ｎｍ厚の酸化珪素膜を積層した構造とする。

【００６９】その後、それぞれの濃度で添加されたn型またはp型不純物元素を活性化する。活性化手段としては、ファーネスアニール法、レーザーアニール法、またはランプアニール法で行うことができる。本実施例では電熱炉において窒素雰囲気中、５５０℃、４時間の熱処理を行う。

【００７０】さらに、3～１００％の水素を含む雰囲気中で、３００～４５０℃で１～１２時間の熱処理を行い水素化処理を行う。この工程は熱的に励起された水素により半導体膜の不対結合手を水素終端する工程である。水素化の他の手段として、プラズマ水素化（プラズマにより励起された水素を用いる）を行っても良い。

【００７１】なお、水素化処理は第１層間絶縁膜３３８を形成する間に入れても良い。即ち、２００ｎｍ厚の窒化酸化珪素膜を形成した後で上記のように水素化処理を行い、その後で残り８００ｎｍ厚の酸化珪素膜を形成しても構わない。

【００７２】次に、図５（Ａ）に示すように、第１層間絶縁膜３３８に対してコンタクトホールを形成し、ソース配線３３９～３４２、ドレイン配線３４３～３４５および接続配線３４６を形成する。なお、本実施例ではこれらの配線を、Ｔｉ膜を１００ｎｍ、Ｔｉを含むアルミニウム膜を３００ｎｍ、Ｔｉ膜１５０ｎｍをスパッタ法で連続形成した３層構造の積層膜とする。勿論、他の導電膜を用いても良い。

【００７３】次に、５０～５００ｎｍ（代表的には２００～３００ｎｍ）の厚さでパッシベーション膜３４７を形成する。本実施例ではパッシベーション膜３４７として３００ｎｍ厚の窒化酸化珪素膜を用いる。これは窒化珪素膜で代用しても良い。

【００７４】この時、窒化酸化珪素膜の形成に先立ってH_2、NH_3等水素を含むガスを用いてプラズマ処理を行うことは有効である。この前処理により励起された水素が第１層間絶縁膜３３８に供給され、熱処理を行うことで、パッシベーション膜３４７の膜質が改善される。それと同時に、第１層間絶縁膜３３８に添加された水素が下層側に拡散するため、効果的に活性層を水素化することができる。

【００７５】次に、図５（Ｂ）に示すように、カラーフィルター３４８と蛍光体３４９を形成する。これらの材料は公知のものを用いれば良い。また、これらは別々にパターニングして形成しても良いし、連続的に形成して一括でパターニングして形成しても良い。それぞれの膜厚は０．５～５μm（典型的には１～２μm）の範囲で選択する。特に、蛍光体３４９は用いる材料によって最適な膜厚が異なる。即ち、薄すぎると色変換効率が悪くなり、厚すぎると段差が大きくなる上に光の透過光量が落ちてしまう。従って、両特性の兼ね合いで最適な膜厚を決定しなければならない。

【００７６】なお、本実施例ではＥＬ層から発生した光を色変換するカラー化方式を例にとって説明しているが、ＲＧＢに対応するＥＬ層を個別に作製する方式を採用する場合は、カラーフィルターや蛍光体を省略することもできる。

【００７７】次に、有機樹脂からなる第２層間絶縁膜３５０を形成する。有機樹脂としてはポリイミド、ポリアミド、アクリル樹脂もしくはＢＣＢ（ベンゾシクロブテン）を使用することができる。特に、第２層間絶縁膜は平坦化の意味合いが強いので、平坦性に優れたアクリル樹脂が好ましい。本実施例ではカラーフィルター３４８及び蛍光体３４９の段差を平坦化しうる膜厚でアクリル樹脂を形成する。

【００７８】次に、第２層間絶縁膜３５０、パッシベーション膜３４７にドレイン配線３４５に達するコンタクトホールを形成し、画素電極３５１を形成する。本実施例では酸化インジウムと酸化スズとの化合物からなる導

電膜（ＩＴＯ膜）を１１０ｎｍの厚さに形成し、パターニングを行って画素電極とする。この画素電極がＥＬ素子の陽極となる。

【００７９】次に、図５（Ｃ）に示すように、ＥＬ層３５２、陰極（ＭｇＡｇ電極）３５３、保護電極３５４を大気解放しないで連続形成する。但し、ＥＬ層３５２としては公知の材料を用いることができる。公知の材料としては、有機材料が知られており、駆動電圧を考慮すると有機材料を用いるのが好ましい。本実施例では正孔注入層、正孔輸送層、発光層及び電子注入層でなる４層構造をＥＬ層とする。また、本実施例ではＥＬ素子の陰極としてＭｇＡｇ電極を用いるが、公知の他の材料であっても良い。

【００８０】また、保護電極３５４はＭｇＡｇ電極３５３の劣化を防ぐために設けられ、アルミニウム膜（アルミニウムを含む導電膜）が好適である。勿論、他の材料でも良い。また、ＥＬ層３５２、ＭｇＡｇ電極３５３は水分に弱いので、保護電極３５４までを大気解放しないで連続的に形成し、外気からＥＬ層を保護することが望ましい。

【００８１】なお、ＥＬ層３５２の膜厚は８００～２００ｎｍ（典型的には１００～１２０ｎｍ）、ＭｇＡｇ電極の厚さは１８０～３００ｎｍ（典型的には２００～２５０ｎｍ）とすれば良い。

【００８２】こうして図５（Ｃ）に示すような構造のアクティブマトリクス型ＥＬ表示装置が完成する。なお、実際には、図５（Ｃ）まで完成したら、さらに外気に曝されないように気密性の高い保護フィルム（ラミネートフィルム等）でパッケージすることが好ましい。その際、保護フィルム内を不活性雰囲気にすることでＥＬ層の信頼性が向上する。

【００８３】また、パッケージング処理により気密性を高めたら、基板上に形成された素子又は回路から引き回された端子と外部信号端子とを接続するためのコネクター（フレキシブルプリントサーキット：ＦＰＣ）を取り付けて製品として完成する。このような状態のＥＬ表示装置を本明細書中ではＥＬモジュールという。

【００８４】ところで、本実施例のアクティブマトリクス型ＥＬ表示装置は、駆動回路部及び画素部に最適な構造のＴＦＴを配置することにより、非常に高い信頼性を示し、動作特性も向上しうる。

【００８５】まず、ホットキャリア注入を低減させる構造を有するＴＦＴを、駆動回路を形成するＣＭＯＳ回路のｎチャネル型ＴＦＴ２０５として用いる。なお、ここでいう駆動回路としては、シフトレジスタ、バッファ、レベルシフタ、サンプリング回路（サンプル及びホールド回路）などが含まれる。デジタル駆動を行う場合には、Ｄ／Ａコンバータもしくはラッチも含まれうる。

【００８６】本実施例の場合、図５（Ｃ）に示すように、ｎチャネル型２０５の活性層は、ソース領域３５５、ドレイン領域３５６、ＬＤＤ領域３５７及びチャネル形成領域３５８を含み、ＬＤＤ領域３５７はゲート絶縁膜３１２を挟んでゲート電極３１４に重なっている。

【００８７】ドレイン領域側のみにＬＤＤ領域を形成しているのは、動作速度を落とさないための配慮である。また、このｎチャネル型ＴＦＴ２０５はオフ電流値をあまり気にする必要はなく、それよりも動作速度を重視した方が良い。従って、ＬＤＤ領域３５７は完全にゲート電極に重ねてしまい、極力抵抗成分を少なくすることが望ましい。即ち、いわゆるオフセットはなくした方がよい。

【００８８】また、ＣＭＯＳ回路のｐチャネル型ＴＦＴ２０６は、ホットキャリア注入による劣化が殆ど気にならないので、特にＬＤＤ領域を設けなくても良い。従って、活性層はソース領域３５９、ドレイン領域３６０およびチャネル形成領域３６１を含む。勿論、ｎチャネル型ＴＦＴ２０５と同様にＬＤＤ領域を設け、ホットキャリア対策を講じることも可能である。

【００８９】なお、駆動回路の中でもサンプリング回路は他の回路と比べて少し特殊であり、チャネル形成領域を双方向に大電流が流れる。即ち、ソース領域とドレイン領域の役割が入れ替わるのである。さらに、オフ電流値を極力低く抑える必要があり、そういった意味でスイッチング用ＴＦＴと電流制御用ＴＦＴの中間程度の機能を有するＴＦＴを配置することが望ましい。

【００９０】従って、サンプリング回路を形成するｎチャネル型ＴＦＴは、図８に示すような構造のＴＦＴを配置することが望ましい。図８に示すように、ＬＤＤ領域７１ａ、７１ｂの一部がゲート絶縁膜７２を挟んでゲート電極７３に重なる。この効果は電流制御用ＴＦＴ２０２の説明で述べた通りであり、サンプリング回路の場合はチャネル形成領域７４を挟む形で設ける点が異なる。

【００９１】また、図１に示したような構造の画素を形成して画素部を形成している。画素内に形成されるスイッチング用ＴＦＴ及び電流制御用ＴＦＴの構造については、図１で既に説明したのでここでの説明は省略する。

【００９２】〔実施例２〕本実施例では、アクティブマトリクス型ＥＬ表示装置の画素部を図１とは異なる構造とした場合について説明する。

【００９３】まずスイッチング用ＴＦＴの構造を図１と異ならせた例を図６（Ａ）に示す。但し、図６（Ａ）に示した電流制御用ＴＦＴ２０２、保持容量２０３及びＥＬ素子２０４は実施例１と全く同じ構造であるので説明は省略する。また、スイッチング用ＴＦＴについても必要箇所のみに新たな符号をつけ、他の部分は図１の説明をそのまま用いることとする。

【００９４】図１に示したスイッチング用ＴＦＴ２０１と図６（Ａ）に示したスイッチング用ＴＦＴ２０７とは、ＬＤＤ領域の形成位置が異なる。図１のＬＤＤ領域１５ａ～１５ｄはゲート電極１９ａ、１９ｂに重ならないよ

うに形成されているが、本実施例では一部がゲート電極に重なるように形成する。

【0095】即ち、図6（A）に示すように、スイッチング用TFT207のLDD領域50a～50dの一部は、ゲート絶縁膜を挟んでゲート電極51a、51bに重なっている。換言すれば、LDD領域50a～50dはゲート絶縁膜を挟んでゲート電極51a、51bに重なる領域を有する。

【0096】これによりオフ電流値を低減できるだけで少なくし、ホットキャリア注入による劣化も防ぐことができる。但し、ゲート電極とLDD領域との間に寄生容量を形成してしまうので、図1の構造に比べて若干動作速度が落ちる場合がある。しかしながら、その点を踏まえて設計すれば信頼性の高いスイッチング用TFTを形成することが可能である。

【0097】次に、電流制御用TFTの構造を図1と異ならせた例を図6（B）に示す。但し、図6（B）に示したスイッチング用TFT201、保持容量203及びEL素子204は実施例1と全く同じ構造であるので説明は省略する。また、電流制御用TFTについても必要箇所のみに新たな符号をつけ、他の部分は図1の説明をそのまま用いることとする。

【0098】図1に示した電流制御用TFT202と図6（B）に示した電流制御用TFT208とは、LDD領域の形成位置が異なる。図1のLDD領域33はゲート電極35に一部が重なるように形成されているが、本実施例では完全にゲート電極に重なるように形成する。

【0099】即ち、図6（B）に示すように、電流制御用TFT208のLDD領域52は、ゲート絶縁膜を介して完全にゲート電極53に重なる。換言すれば、LDD領域52はゲート電極53に重ならない領域を有していない。

【0100】ビデオ（画像）信号の最低電圧が電流制御用TFTのゲート電圧に印加されたとき、十分にオフ電流値が低くなければEL素子が発光してしまい、コントラストの低下を招く。図1の構造はそのときのオフ電流値を下げるために、ゲート電極に重ならないLDD領域を設けている。

【0101】しかしながら、ゲート電極に重ならないLDD領域は抵抗成分として働くため、動作速度やオン電流値をある程度落とすことになってしまう。従って、本実施例のように設けない構造としてしまえば、そういった抵抗成分を排除できるので、より大きな電流を流しやすくなる。但し、前述のように、ビデオ（画像）信号の最低電圧が電流制御用TFTのゲート電圧に印加されたとき、十分にオフ電流値が低いTFTを用いることが前提である。

【0102】なお、図6（A）のスイッチング用TFT207と図6（B）の電流制御用TFTを組み合わせて用いることも可能である。また、作製工程は実施例1を参考にすれば良い。

【0103】〔実施例3〕本実施例では、画素の構成を図2（B）に示した構成と異なるものとした例を図7に示す。

【0104】本実施例では、図2（B）に示した二つの画素を、接地電位を与えるための電流供給線212について対称となるように配置する。即ち、図7に示すように、電流供給線213を隣接する二つの画素間で共通化することで、必要とする配線の本数を低減する。なお、画素内に配置されるTFT構造等はそのままで良い。

【0105】このような構成とすれば、より高精細な画素部を作製することが可能となり、画像の品質が向上する。なお、本実施例の構成は実施例1の作製工程に従って容易に実現可能であり、TFT構造に関しては実施例2と組み合わせても良い。

【0106】〔実施例4〕本実施例では、図1と異なる構造の画素部を形成する場合について図9を用いて説明する。なお、第2層間絶縁膜44を形成する工程までは実施例1に従えば良い。また、第2層間絶縁膜44で覆われたスイッチング用TFT201、電流制御用TFT202及び保持容量203は図1と同じ構造であるので、説明は省略する。

【0107】本実施例の場合、第2層間絶縁膜44に対してコンタクトホールを形成したら、画素電極60、陰極61及びEL層62を形成する。これらは、それぞれの材料を大気解放しないで連続形成し、一括でエッチングしてパターン形成を行えば良い。

【0108】本実施例では画素電極60として、150nm厚のアルミニウム合金膜（1wt%のチタンを含有したアルミニウム膜）を設ける。なお、画素電極の材料としては金属材料であれば如何なる材料でも良いが、反射率の高い材料であることが好ましい。

【0109】また、陰極61として230nm厚のMgAg電極を用い、EL層62の膜厚は120nmとする。なお、EL層62の形成に関しては、実施例1で説明した材料を用いれば良い。

【0110】次に、珪素を含む絶縁膜を200～500nm（典型的には250～300nm）の厚さに形成し、パターニングによって開口部を有する保護膜63を形成する。そして、その上に透明導電膜（本実施例ではITO膜）からなる陽極64を110nmの厚さに形成する。透明導電膜としては、他にも酸化インジウムと酸化亜鉛との化合物、酸化スズ、酸化インジウムもしくは酸化亜鉛を用いることができる。また、それらにガリウムを添加したものを用いても良い。

【0111】さらに、陽極64上に蛍光体65及びカラーフィルター66を形成して、図9に示すような画素部が完成する。

【0112】本実施例の構造とした場合、生成された赤、緑若しくは青の光はTFTが形成された基板とは反

対側に出射される。そのため、画素内のほぼ全域、即ちＴＦＴが形成された領域をも発光領域として用いることができる。その結果、画素の有効発光面積が大幅に向上し、画像の明るさやコントラストが向上する。

【０１１３】なお、本実施例の構成は、実施例２、３のいずれの構成とも自由に組み合わせることが可能である。

【０１１４】〔実施例５〕実施例１では、結晶質珪素膜３０２の形成手段としてレーザー結晶化を用いているが、本実施例では異なる結晶化手段を用いる場合について説明する。

【０１１５】本実施例では、非晶質珪素膜を形成した後、特開平７－１３０６５２号公報に記載された技術を用いて結晶化を行う。同公報には、結晶化を促進（助長）する触媒元素としてニッケルを用い、結晶性の高い結晶質珪素膜を得る技術が開示されている。

【０１１６】また、結晶化工程が終了した後で、結晶化に用いた触媒元素を除去する工程を行っても良い。その場合、特開平１０－２７０３６３号若しくは特開平８－３３０６０２号に記載された技術により触媒元素をゲッタリングすれば良い。

【０１１７】また、本出願人による特願平１１－０７６９６７号の明細書に記載された技術を用いてＴＦＴを形成しても良い。特願平１１－０７６９６７号の明細書では、図１とは異なる保持容量が説明されているが、ＴＦＴを形成する部分までを参照すれば良い。

【０１１８】以上のように、本発明は実施例１及び図１で説明したように、素子の求める機能に応じて適切な構造のＴＦＴを配置することを主旨としており、その作製方法に限定されるものではない。即ち、実施例１に示した作製工程は一実施例であって、図１若しくは実施例１の図５（Ｃ）の構造が実現できるのであれば、他の作製工程を用いても問題ではない。

【０１１９】なお、図１若しくは図５（Ｃ）の構造に実施例２～４のいずれかの構成を組み合わせた場合についても、そのような構造を作製するにあたって本実施例に示したような作製工程を組み合わせることは可能である。

【０１２０】〔実施例６〕実施例１において、図４（Ａ）の工程と図４（Ｂ）の工程との間に、ゲート絶縁膜３１２をエッチングする工程を加えても良い。即ち、図４（Ａ）に示すようにｎ型不純物元素を添加した後、ゲート電極３１３～３１７および容量形成用電極３１８をマスクとして自己整合的にゲート絶縁膜３１２をエッチングする。このエッチングは活性層が露呈するまで行う。

【０１２１】本実施例では、実施例１用いたゲート絶縁膜が窒化酸化珪素膜であるため、エッチングガスとしてCHF_3ガスを用いたドライエッチングを行う。勿論、他のエッチング条件はこれに限定されるものではない。

【０１２２】そして、露呈した活性層に対して図４（Ｂ）に示すようにｎ型不純物元素の添加工程を行う。この工程ではゲート絶縁膜を通さずに直接リンを活性層へ添加することになるため、非常に短時間で処理を行うことができる。また、添加時の加速電圧も低くて済むので、活性層へのダメージも低減しうる。

【０１２３】後は、実施例１の工程に従ってＥＬ表示装置を完成させれば良い。なお、本実施例の構成は実施例１～５のいずれの構成とも自由に組み合わせて実施することが可能である。

【０１２４】〔実施例７〕本実施例では、実施例１と異なる構造の画素を形成したアクティブマトリクス型ＥＬ表示装置について説明する。

【０１２５】図１０（Ａ）は本実施例のＥＬ表示装置であるが、ＴＦＴ構造は実施例１（図５（Ｃ）参照）と同様である。本実施例では画素電極１００１、陰極１００２、ＥＬ層１００３および陽極１００４を形成し、陰極１００２、ＥＬ層１００３および陽極１００４でＥＬ素子１０００を形成する。このとき、画素電極１００１は公知の如何なる導電膜を用いても良い。また、本実施例では陰極１００２としてＭｇＡｇ膜を用い、陽極１００４として酸化亜鉛に酸化ガリウムを添加した透明導電膜を用いる。なお、ＥＬ層１００３は公知の材料を組み合わせて形成すれば良い。

【０１２６】本実施例では、画素電極１００１のコンタクト部（画素電極１００１と電流制御用ＴＦＴ２０２とが接続された部分）に形成された凹部（窪み）が絶縁物１００５で埋め込まれ、さらに画素電極１００１の端部が絶縁物１００６で覆われている点に特徴がある。

【０１２７】絶縁物１００５は上記凹部を埋め込むことで段差によるＥＬ層の被覆不良を防止している。第２層間絶縁膜３５０に形成されたコンタクトホールが深い（段差が高い）とＥＬ層の被覆不良が生じて陰極１００２と陽極１００４が短絡する恐れがある。そのため、本実施例では凹部を絶縁物１００５で埋め込むことによりＥＬ層の被覆不良を防ぐことを特徴としている。

【０１２８】また、同様に画素電極１００１の端部は画素電極１００１の膜厚分の段差が生じているため、絶縁物１００５と同様の理由により絶縁物１００６を形成する。これにより画素電極１００１の端部において陰極１００２と陽極１００４の短絡を確実に防ぐことができる。また、画素電極１００１の端部は電界集中を起こしてＥＬ層１００３の劣化が進行しやすいため、絶縁物１００６を設けることでＥＬ層１００３に電界集中しないようにする目的もある。

【０１２９】また、図１０（Ｂ）は電流制御用ＴＦＴの活性層にＬＤＤ領域を形成しない構造とした場合の例である。ＥＬ素子にかかる電圧が１０Ｖ以下、好ましくは５Ｖ以下となった場合、ホットキャリアによる劣化は殆ど問題とならないため、このような構造とすることが可

能である。即ち、図１０（Ｂ）の構造では、電流制御用ＴＦＴの活性層がソース領域１０１０、ドレイン領域１０１１およびチャネル形成領域１０１２からなる。

【０１３０】なお、本実施例の構成は実施例１～６のいずれの構成とも自由に組み合わせて実施することが可能である。

【０１３１】〔実施例８〕本発明のＥＬ表示装置を駆動は、画像信号としてアナログ信号を用いたアナログ駆動を行うこともできるし、デジタル信号を用いたデジタル駆動を行うこともできる。

【０１３２】アナログ駆動を行う場合、スイッチング用ＴＦＴのソース配線にはアナログ信号が送られ、その階調情報を含んだアナログ信号が電流制御用ＴＦＴのゲート電圧となる。そして、電流制御用ＴＦＴでＥＬ素子に流れる電流を制御し、ＥＬ素子の発光強度を制御して階調表示を行う。

【０１３３】一方、デジタル駆動を行う場合、アナログ的な階調表示とは異なり、時分割駆動と呼ばれる階調表示を行う。即ち、発光時間の長さを調節することで、視覚的に色階調が変化しているように見せる。

【０１３４】ＥＬ素子は液晶素子に比べて非常に応答速度が速いため、高速で駆動することが可能である。そのため、１フレームを複数のサブフレームに分割して階調表示を行う時分割駆動に適した素子であると言える。

【０１３５】このように、本発明は素子構造に関する技術であるので、駆動方法は如何なるものであっても構わない。

【０１３６】〔実施例９〕実施例１ではＥＬ層として有機ＥＬ材料を用いることが好ましいとしたが、本発明は無機ＥＬ材料を用いても実施できる。但し、現在の無機ＥＬ材料は非常に駆動電圧が高いため、アナログ駆動を行う場合には、そのような駆動電圧に耐えうる耐圧特性を有するＴＦＴを用いなければならない。

【０１３７】または、将来的にさらに駆動電圧の低い無機ＥＬ材料が開発されれば、本発明に適用することは可能である。

【０１３８】また、本実施例の構成は、実施例１～７のいずれの構成とも自由に組み合わせることが可能である。

【０１３９】〔実施例１０〕本発明のＥＬ表示装置の外観図を説明する。なお、図１１（Ａ）は本発明のＥＬ表示装置の上面図であり、図１１（Ｂ）はその断面図である。

【０１４０】図１１（Ａ）において、４００１は基板、４００２は画素部、４００３はソース側駆動回路、４００４はゲート側駆動回路であり、それぞれの駆動回路は配線４００５を経てＦＰＣ（フレキシブルプリントサーキット）４００６に至り、外部機器へと接続される。

【０１４１】このとき、画素部４００２、ソース側駆動回路４００３及びゲート側駆動回路４００４を囲むようにして第１シール材４１０１、カバー材４１０２、充填材４１０３及び第２シール材４１０４が設けられている。

【０１４２】また、図１１（Ｂ）は図１１（Ａ）をＡ－Ａ'で切断した断面図に相当し、基板４００１の上にソース側駆動回路４００３に含まれる駆動ＴＦＴ（但し、ここではｎチャネル型ＴＦＴとｐチャネル型ＴＦＴを図示している。）４２０１及び画素部４００２に含まれる電流制御用ＴＦＴ４２０２が形成されている。

【０１４３】本実施例では、駆動ＴＦＴ４２０１には図５（Ｃ）のｎチャネル型ＴＦＴ２０５とｐチャネル型ＴＦＴ２０６と同じ構造のＴＦＴが用いられ、電流制御用ＴＦＴ４２０２には図１のｎチャネル型ＴＦＴ２０２と同じ構造のＴＦＴが用いられる。また、画素部４００２には電流制御用ＴＦＴ４２０２のゲートに接続された保持容量（図示せず）が設けられる。

【０１４４】駆動ＴＦＴ４２０１及び画素ＴＦＴ４２０２の上には樹脂材料でなる層間絶縁膜（平坦化膜）４３０１が形成され、その上に画素ＴＦＴ４２０２のドレインと電気的に接続する画素電極（陰極）４３０２が形成される。画素電極４３０２としては仕事関数の小さい導電膜が用いられる。金属膜としては、周期表の１族または２族に属する元素を含む導電膜（代表的にはアルミニウム、銅もしくは銀に、アルカリ金属元素もしくはアルカリ土類金属元素を含ませた導電膜）を用いることができる。

【０１４５】そして、画素電極４３０２の上には絶縁膜４３０３が形成され、絶縁膜４３０３は画素電極４３０２の上に開口部が形成されている。この開口部において、画素電極４３０２の上にはＥＬ（エレクトロルミネッセンス）層４３０４が形成される。ＥＬ層４３０４は公知の有機ＥＬ材料または無機ＥＬ材料を用いることができる。また、有機ＥＬ材料には低分子系（モノマー系）材料と高分子系（ポリマー系）材料があるがどちらを用いても良い。

【０１４６】ＥＬ層４３０４の形成方法は公知の蒸着技術もしくは塗布法技術を用いれば良い。また、ＥＬ層の構造は正孔注入層、正孔輸送層、発光層、電子輸送層または電子注入層を自由に組み合わせて積層構造または単層構造とすれば良い。

【０１４７】ＥＬ層４３０４の上には透明導電膜からなる陽極４３０５が形成される。透明導電膜としては、酸化インジウムと酸化スズとの化合物、酸化インジウムと酸化亜鉛との化合物、酸化インジウム、酸化スズ、酸化亜鉛もしくはそれらにガリウムを添加した化合物を含む導電膜を用いることができる。

【０１４８】また、陽極４３０５とＥＬ層４３０４の界面に存在する水分や酸素は極力排除しておくことが望ましい。従って、真空中で両者を連続成膜するか、ＥＬ層４３０４を窒素または希ガス雰囲気で形成し、酸素や水

分に触れさせないまま陽極４３０５を形成するといった工夫が必要である。本実施例ではマルチチャンバー方式（クラスターツール方式）の成膜装置を用いることで上述のような成膜を可能とする。

【０１４９】そして陽極４３０５は４３０６で示される領域において配線４００５に電気的に接続される。配線４００５は陽極４３０５に所定の電圧を与えるための配線であり、異方導電性フィルム４３０７を介してＦＰＣ４００６に電気的に接続される。

【０１５０】以上のようにして、画素電極（陰極）４３０２、ＥＬ層４３０４及び陽極４３０５からなるＥＬ素子が形成される。このＥＬ素子は、第１シール材４１０１及び第１シール材４１０１によって基板４００１に貼り合わされたカバー材４１０２で囲まれ、充填材４１０３により封入されている。

【０１５１】カバー材４１０２としては、ガラス材またはプラスチック材（プラスチックフィルムも含む）を用いることができる。プラスチック材としては、ＦＲＰ（Ｆｉｂｅｒｇｌａｓｓ－Ｒｅｉｎｆｏｒｃｅｄ Ｐｌａｓｔｉｃｓ）板、ＰＶＦ（ポリビニルフルオライド）フィルム、マイラーフィルム、ポリエステルフィルムまたはアクリル樹脂フィルムを用いることができる。

【０１５２】また、充填材４１０３としては紫外線硬化樹脂または熱硬化樹脂を用いることができ、ＰＶＣ（ポリビニルクロライド）、アクリル、ポリイミド、エポキシ樹脂、シリコーン樹脂、ＰＶＢ（ポリビニルブチラル）またはＥＶＡ（エチレンビニルアセテート）を用いることができる。この充填材４１０３の内部に吸湿性物質（好ましくは酸化バリウム）を設けておくとＥＬ素子の劣化を抑制できる。

【０１５３】また、充填材４１０３の中にスペーサを含有させてもよい。このとき、スペーサを酸化バリウムで形成すればスペーサ自体に吸湿性をもたせることが可能である。また、スペーサを設けた場合、スペーサからの圧力を緩和するバッファ層として陽極４３０５上に樹脂膜を設けることも有効である。

【０１５４】また、配線４００５は異方導電性フィルム４３０７を介してＦＰＣ４００６に電気的に接続される。配線４００５は画素部４００２、ソース側駆動回路４００３及びゲート側駆動回路４００４に送られる信号をＦＰＣ４００６に伝え、ＦＰＣ４００６により外部機器と電気的に接続される。

【０１５５】また、本実施例では第１シール材４１０１の露呈部及びＦＰＣ４００６の一部を覆うように第２シール材４１０４を設け、ＥＬ素子を徹底的に外気から遮断する構造となっている。こうして図１１（Ｂ）の断面構造を有するＥＬ表示装置となる。なお、本実施例のＥＬ表示装置は実施例１～９のいずれの構成を組み合わせて作製しても構わない。

【０１５６】〔実施例１１〕本実施例では、本発明のＥＬ表示装置の画素構造の例を図１２（Ａ）～（Ｃ）に示す。なお、本実施例において、４６０１はスイッチング用ＴＦＴ４６０２のソース配線、４６０３はスイッチング用ＴＦＴ４６０２のゲート配線、４６０４は電流制御用ＴＦＴ、４６０５はコンデンサ、４６０６、４６０８は電流供給線、４６０７はＥＬ素子とする。

【０１５７】図１２（Ａ）は、二つの画素間で電流供給線４６０６を共通とした場合の例である。即ち、二つの画素が電流供給線４６０６を中心に線対称となるように形成されている点に特徴がある。この場合、電流供給線の本数を減らすことができるため、画素部をさらに高精細化することができる。

【０１５８】また、図１２（Ｂ）は、電流供給線４６０８をゲート配線４６０３と平行に設けた場合の例である。なお、図１２（Ｂ）では電流供給線４６０８とゲート配線４６０３とが重ならないように設けた構造となっているが、両者が異なる層に形成される配線であれば、絶縁膜を介して重なるように設けることもできる。この場合、電流供給線４６０８とゲート配線４６０３とで専有面積を共有させることができるため、画素部をさらに高精細化することができる。

【０１５９】また、図１２（Ｃ）は、図１２（Ｂ）の構造と同様に電流供給線４６０８をゲート配線４６０３と平行に設け、さらに、二つの画素を電流供給線４６０８を中心に線対称となるように形成する点に特徴がある。また、電流供給線４６０８をゲート配線４６０３のいずれか一方と重なるように設けることも有効である。この場合、電流供給線の本数を減らすことができるため、画素部をさらに高精細化することができる。

【０１６０】なお、本実施例の構成は実施例１～１０のいずれの構成とも自由に組み合わせることが可能である。

【０１６１】〔実施例１３〕本実施例では、本発明のＥＬ表示装置の画素構造の例を図１３（Ａ）、（Ｂ）に示す。なお、本実施例において、４７０１はスイッチング用ＴＦＴ４７０２のソース配線、４７０３はスイッチング用ＴＦＴ４７０２のゲート配線、４７０４は電流制御用ＴＦＴ、４７０５はコンデンサ（省略することも可能）、４７０６は電流供給線、、４７０７は電源制御用ＴＦＴ、４７０８は電源制御用ゲート配線、４７０９はＥＬ素子とする。電源制御用ＴＦＴ４７０７の動作については特願平１１－３４１２７２号を参照すると良い。

【０１６２】また、本実施例では電源制御用ＴＦＴ４７０７を電流制御用ＴＦＴ４７０４とＥＬ素子４７０８との間に設けているが、電源制御用ＴＦＴ４７０７とＥＬ素子４７０８との間に電流制御用ＴＦＴ４７０４が設けられた構造としても良い。また、電源制御用ＴＦＴ４７０７は電流制御用ＴＦＴ４７０４と同一構造とするか、同一の活性層で直列させて形成するのが好ましい。

【０１６３】また、図１３（Ａ）は、二つの画素間で電

流供給線４７０６を共通とした場合の例である。即ち、二つの画素が電流供給線４７０６を中心に線対称となるように形成されている点に特徴がある。この場合、電流供給線の本数を減らすことができるため、画素部をさらに高精細化することができる。

【０１６４】また、図１３（Ｂ）は、ゲート配線４７０３と平行に電流供給線４７１０を設け、ソース配線４７０１と平行に電源制御用ゲート配線４７１１を設けた場合の例である。なお、図１３（Ｂ）では電流供給線４７１０とゲート配線４７０３とが重ならないように設けた構造となっているが、両者が異なる層に形成される配線であれば、絶縁膜を介して重なるように設けることもできる。この場合、電流供給線４７１０とゲート配線４７０３とで専有面積を共有させることができるため、画素部をさらに高精細化することができる。

【０１６５】なお、本実施例の構成は実施例１～１０のいずれの構成とも自由に組み合わせることが可能である。

【０１６６】〔実施例１４〕本実施例では、本発明のＥＬ表示装置の画素構造の例を図１４（Ａ）、（Ｂ）に示す。なお、本実施例において、４８０１はスイッチング用ＴＦＴ４８０２のソース配線、４８０３はスイッチング用ＴＦＴ４８０２のゲート配線、４８０４は電流制御用ＴＦＴ、４８０５はコンデンサ（省略することも可能）、４８０６は電流供給線、、４８０７は消去用ＴＦＴ、４８０８は消去用ゲート配線、４８０９はＥＬ素子とする。消去用ＴＦＴ４８０７の動作については特願平１１－３３８７８６号を参照すると良い。

【０１６７】消去用ＴＦＴ４８０７のドレインは電流制御用ＴＦＴ４８０４のゲートに接続され、電流制御用ＴＦＴ４８０４のゲート電圧を強制的に変化させることができるようになっている。なお、消去用ＴＦＴ４８０７はｎチャネル型ＴＦＴとしてもｐチャネル型ＴＦＴとしても良いが、オフ電流を小さくできるようにスイッチング用ＴＦＴ４８０２と同一構造とすることが好ましい。

【０１６８】また、図１４（Ａ）は、二つの画素間で電流供給線４８０６を共通とした場合の例である。即ち、二つの画素が電流供給線４８０６を中心に線対称となるように形成されている点に特徴がある。この場合、電流供給線の本数を減らすことができるため、画素部をさらに高精細化することができる。

【０１６９】また、図１４（Ｂ）は、ゲート配線４８０３と平行に電流供給線４８１０を設け、ソース配線４８０１と平行に消去用ゲート配線４８１１を設けた場合の例である。なお、図１４（Ｂ）では電流供給線４８１０とゲート配線４８０３とが重ならないように設けた構造となっているが、両者が異なる層に形成される配線であれば、絶縁膜を介して重なるように設けることもできる。この場合、電流供給線４８１０とゲート配線４８０３とで専有面積を共有させることができるため、画素部をさらに高精細化することができる。

【０１７０】なお、本実施例の構成は実施例１～１０のいずれの構成とも自由に組み合わせることが可能である。

【０１７１】〔実施例１５〕本発明のＥＬ表示装置は画素内にいくつのＴＦＴを設けた構造としても良い。実施例１３、１４ではＴＦＴを三つ設けた例を示しているが、四つ乃至六つのＴＦＴを設けても構わない。本発明はＥＬ表示装置の画素構造に限定されずに実施することが可能である。

【０１７２】なお、本実施例の構成は実施例１～１０のいずれの構成とも自由に組み合わせることが可能である。

【０１７３】〔実施例１６〕本発明を実施して形成したＥＬ表示装置は様々な電気器具の表示部として用いることができる。例えば、ＴＶ放送等を鑑賞するには対角２０～６０インチの本発明のＥＬ表示装置を筐体に組み込んだディスプレイを用いるとよい。なお、ＥＬ表示装置を筐体に組み込んだディスプレイには、パソコン用ディスプレイ、ＴＶ放送受信用ディスプレイ、広告表示用ディスプレイ等の全ての情報表示用ディスプレイが含まれる。

【０１７４】また、その他の本発明の電気器具としては、ビデオカメラ、デジタルカメラ、ゴーグル型ディスプレイ（ヘッドマウントディスプレイ）、ナビゲーションシステム、音楽再生装置（カーオーディオ、オーディオコンポ等）、ノート型パーソナルコンピュータ、ゲーム機器、携帯情報端末（モバイルコンピュータ、携帯電話、携帯型ゲーム機または電子書籍）、画像再生装置（記録媒体に記録された画像を再生し、その画像を表示する表示部を備えた装置）が挙げられる。それら電気器具の具体例を図１５、図１６に示す。

【０１７５】図１５（Ａ）はＥＬ表示装置を筐体に組み込んだディスプレイであり、筐体２００１、支持台２００２、表示部２００３を含む。本発明のＥＬ表示装置は表示部２００３に用いることができる。このようなディスプレイは自発光型であるためバックライトが必要なく、液晶ディスプレイよりも薄い表示部とすることができる。

【０１７６】図１５（Ｂ）はビデオカメラであり、本体２１０１、表示部２１０２、音声入力部２１０３、操作スイッチ２１０４、バッテリー２１０５、受像部２１０６を含む。本発明のＥＬ表示装置は表示部２１０２に用いることができる。

【０１７７】図１５（Ｃ）は頭部取り付け型のＥＬディスプレイの一部（右片側）であり、本体２２０１、信号ケーブル２２０２、頭部固定バンド２２０３、表示部２２０４、光学系２２０５、発光装置２２０６を含む。本発明はＥＬ表示装置２２０６に用いることができる。

【０１７８】図１５（Ｄ）は記録媒体を備えた画像再生

装置（具体的にはＤＶＤ再生装置）であり、本体２３０１、記録媒体（ＤＶＤ等）２３０２、操作スイッチ２３０３、表示部（ａ）２３０４、表示部（ｂ）２３０５を含む。表示部（ａ）は主として画像情報を表示し、表示部（ｂ）は主として文字情報を表示するが、本発明のＥＬ表示装置はこれら表示部（ａ）、（ｂ）に用いることができる。なお、記録媒体を備えた画像再生装置には家庭用ゲーム機器なども含まれる。

【０１７９】図１５（Ｅ）は携帯型（モバイル）コンピュータであり、本体２４０１、カメラ部２４０２、受像部２４０３、操作スイッチ２４０４、表示部２４０５を含む。本発明のＥＬ表示装置は表示部２４０５に用いることができる。

【０１８０】図１５（Ｆ）はパーソナルコンピュータであり、本体２５０１、筐体２５０２、表示部２５０３、キーボード２５０４を含む。本発明のＥＬ表示装置は表示部２５０３に用いることができる。

【０１８１】なお、将来的に発光輝度がさらに高くなれば、出力した画像情報を含む光をレンズや光ファイバー等で拡大投影してフロント型若しくはリア型のプロジェクターに用いることも可能となる。

【０１８２】また、発光装置は発光している部分が電力を消費するため、発光部分が極力少なくなるように情報を表示することが望ましい。従って、携帯情報端末、特に携帯電話や音楽再生装置のような文字情報を主とする表示部に発光装置を用いる場合には、非発光部分を背景として文字情報を発光部分で形成するように駆動することが望ましい。

【０１８３】ここで図１６（Ａ）は携帯電話であり、本体２６０１、音声出力部２６０２、音声入力部２６０３、表示部２６０４、操作スイッチ２６０５、アンテナ２６０６を含む。本発明のＥＬ表示装置は表示部２６０４に用いることができる。なお、表示部２６０４は黒色の背景に白色の文字を表示することで携帯電話の消費電力を抑えることができる。

【０１８４】また、図１６（Ｂ）は音楽再生装置、具体的にはカーオーディオであり、本体２７０１、表示部２７０２、操作スイッチ２７０３、２７０４を含む。本発明のＥＬ表示装置は表示部２７０２に用いることができる。また、本実施例では車載用のカーオーディオを示すが、携帯型や家庭用の音楽再生装置に用いても良い。なお、表示部２７０４は黒色の背景に白色の文字を表示することで消費電力を抑えられる。これは携帯型の音楽再生装置において特に有効である。

【０１８５】以上の様に、本発明の適用範囲は極めて広く、あらゆる分野の電気器具に用いることが可能である。また、本実施例の電気器具は実施例１～１５に示したいずれの構成のＥＬ表示装置を用いても良い。

【０１８６】

【発明の効果】本発明を用いることで、同一の絶縁体上に、素子の求める仕様に応じて適切な性能のＴＦＴを配置することが可能となり、ＥＬ表示装置の動作性能や信頼性を大幅に向上させることができる。

【０１８７】具体的には、動作速度を重視するＴＦＴ構造と低オフ電流値であることを重視するＴＦＴ構造とを同一の絶縁体上において、使い分けることができる。それによりＥＬ表示装置の画素に配置するスイッチング用ＴＦＴはオフ電流値を十分に低くさせることができ、電流制御用ＴＦＴはホットキャリア注入による劣化を防ぐと共にオフ電流値を十分に低くさせることができる。

【０１８８】また、そのようなＥＬ表示装置を表示ディスプレイとして用いることで、画像品質が良く、耐久性のある（信頼性の高い）応用製品（電気器具）を生産することが可能となる。

【図面の簡単な説明】

【図１】　ＥＬ表示装置の画素部の断面構造を示す図。

【図２】　ＥＬ表示装置の画素部の上面構造を示す図。

【図３】　アクティブマトリクス型ＥＬ表示装置の作製工程を示す図。

【図４】　アクティブマトリクス型ＥＬ表示装置の作製工程を示す図。

【図５】　アクティブマトリクス型ＥＬ表示装置の作製工程を示す図。

【図６】　ＥＬ表示装置の画素部の断面構造を示す図。

【図７】　ＥＬ表示装置の画素部の素子構成を示す図。

【図８】　ＥＬ表示装置のサンプリング回路の素子構成を示す図。

【図９】　ＥＬ表示装置の画素部の断面構造を示す図。

【図１０】　ＥＬ表示装置の画素部の断面構造を示す図。

【図１１】　ＥＬ表示装置の上面構造及び断面構造を示す図。

【図１２】　ＥＬ表示装置の画素部の回路構成を示す図。

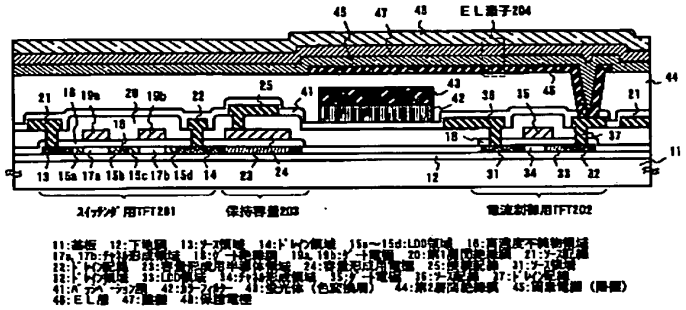
【図１３】　ＥＬ表示装置の画素部の回路構成を示す図。

【図１４】　ＥＬ表示装置の画素部の回路構成を示す図。

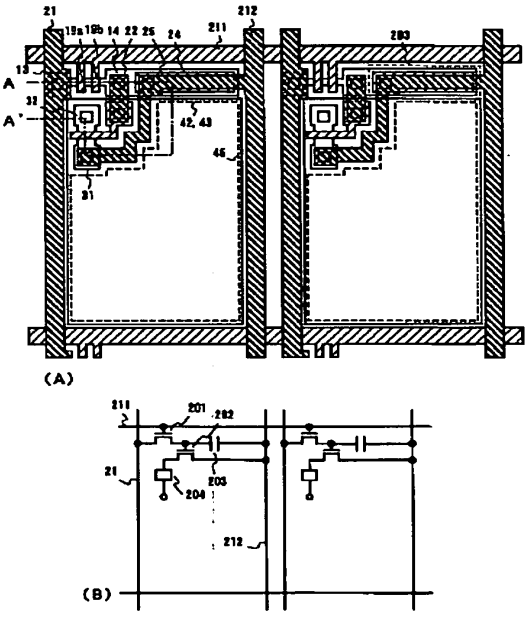
【図１５】　電気器具の具体例を示す図。

【図１６】　電気器具の具体例を示す図。

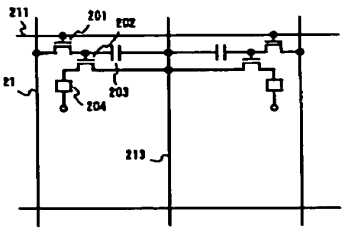
【図1】



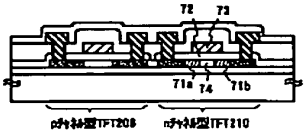
【図2】



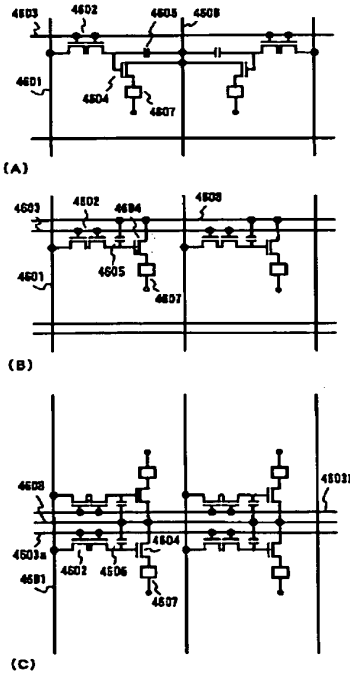
【図7】



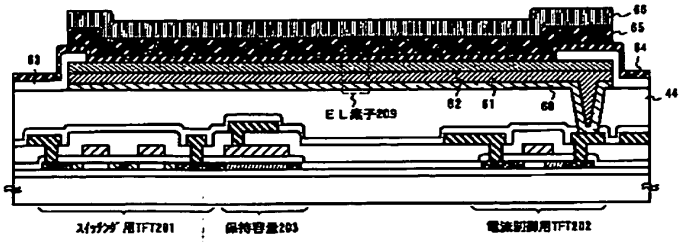
【図8】



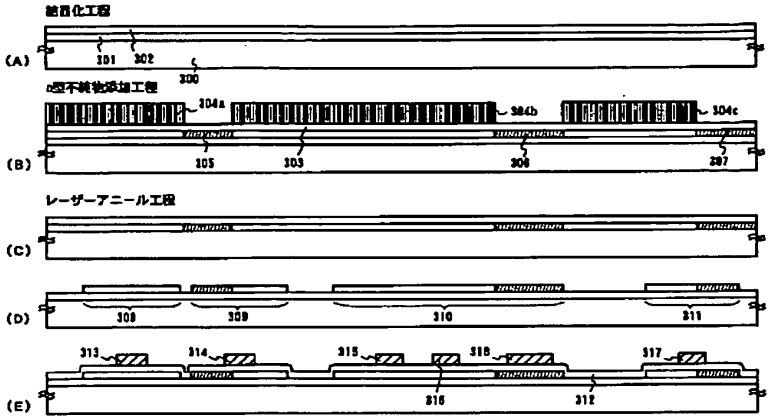
【図12】



【図9】

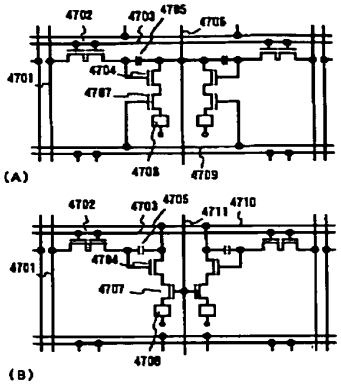


【図3】

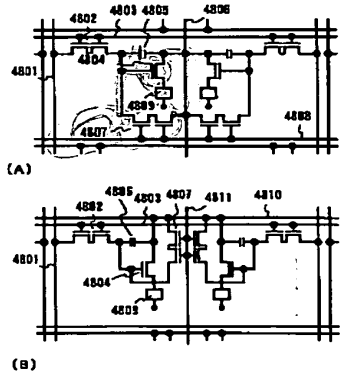


300:ｶﾞﾗｽ基板　301:下地膜　302:ｶﾞﾗｽｽﾃﾝ膜　303:保護膜　304a～304c:ﾚｼﾞｽﾄﾏｽｸ
305～307: n 型不純物領域(b)　308～311:活性層　312:ｹﾞｰﾄ絶縁膜　313～317:ｹﾞｰﾄ電極
316:容量電極

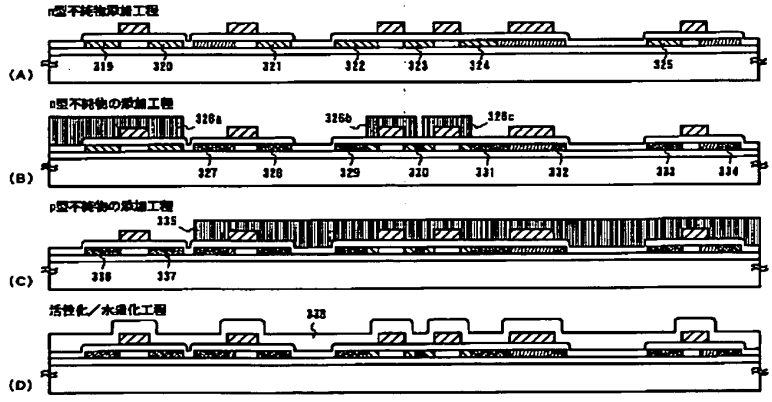
【図13】



【図14】

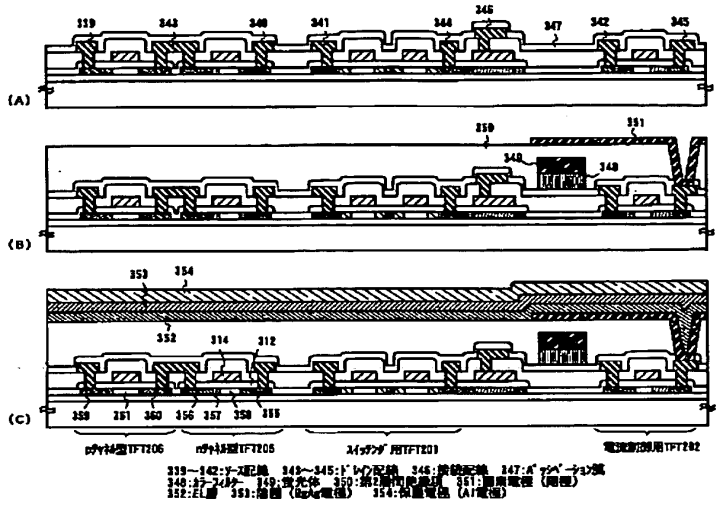


【図4】

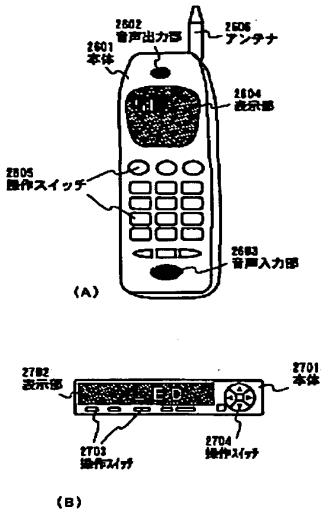


319～325:n型不純物領域(c)　326a, 326b, 326:ﾚｼﾞｽﾄﾏｽｸ　327～334:n型不純物領域(a)　336, 337:p型不純物領域(a)
338:第1層間絶縁膜

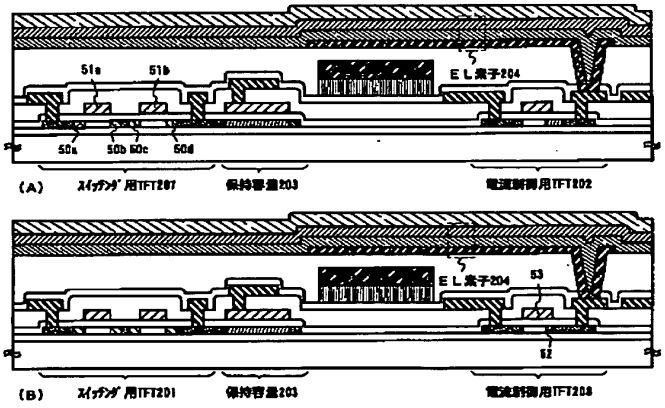
【図5】



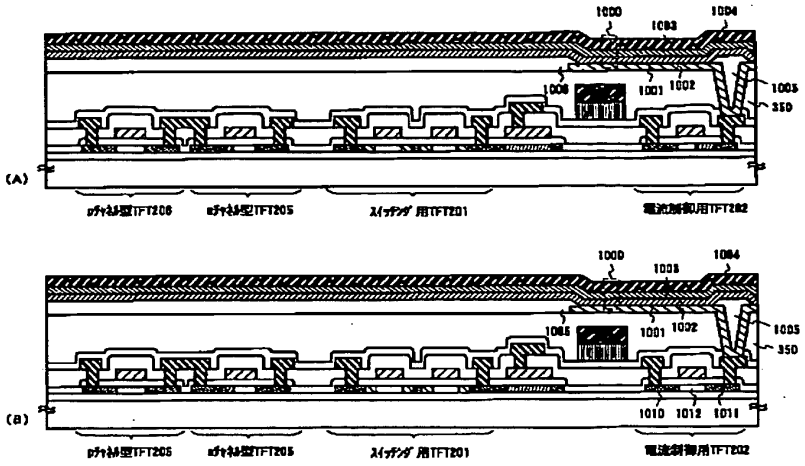
【図16】



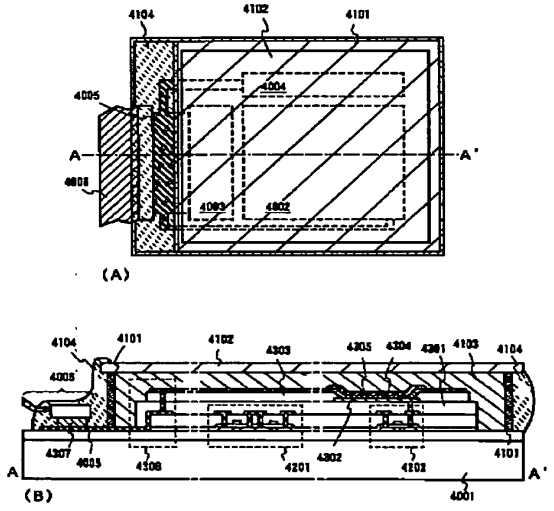
【図6】



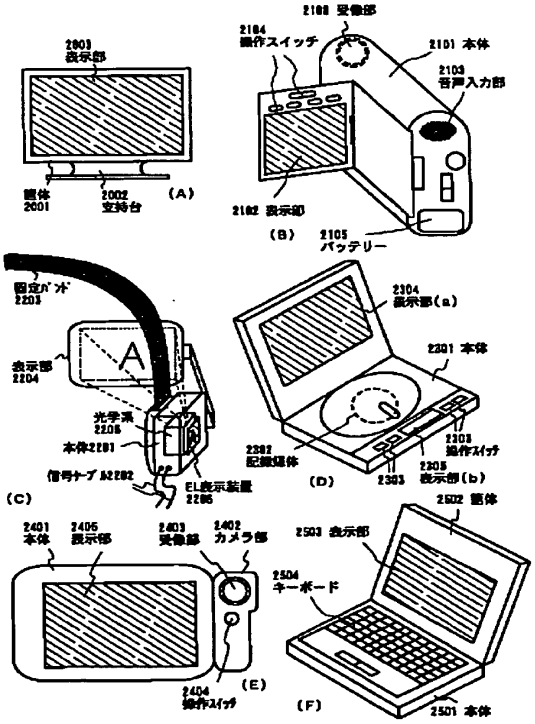
【図10】



【図11】



【図15】



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PATENT ABSTRACTS OF JAPAN

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G09G 3/30
H05B 33/12
H05B 33/14
H05B 33/26

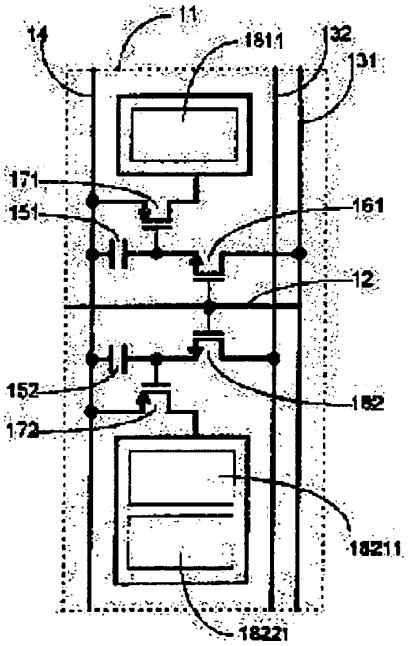
(21)Application number : 11-301448
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(71)Applicant : SEIKO EPSON CORP
(72)Inventor : KIMURA MUTSUMI

(30)Priority
Priority number : 11021623 Priority date : 29.01.1999 Priority country : JP

(54) DISPLAY DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide exact gradations by obtaining the exact ratio of light emitting parts by respectively forming equal plural electroluminescence elements (OELD) and controlling the number of OELD to be emitted.
SOLUTION: An OELD (low-order bit/rectangle) 1811, an OELD (high-order bit/first rectangle) 18211 and an OELD (high-order bit/second rectangule) 18221 are formed equal and the number of OELD to be emitted is controlled to be changed. Thus, it is difficult to obtain the absolute value of a light emitting area as desired but since the light emitting areas of the plural OELD are mutually equal, by controlling the number of these OELD, the ratio of light emitting areas can be made exact. Further, even when the OELD is cross-sectionally formed closer to the side face of a bank or away from the side face of the bank as a phenomenon peculiar for a liquid phase process, the light emitting parts of respective OELD are made into the same area and the exact gradations can be provided.



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CLAIMS

[Claim(s)]
[Claim 1] Two or more thin film transistor and two or more organic electroluminescent elements are formed in each pixel. Said thin film transistor and said organic electroluminescent element By controlling the area which it connects [area] with a serial, and the on-off condition of said thin film transistor is changed [area], and makes said organic electroluminescent element emit light It is the display which said two or more organic electroluminescent elements are the same configurations respectively in the display which realizes gradation, is controlling the number which makes said organic electroluminescent element emit light, and is characterized by realizing gradation.
[Claim 2] It is the display characterized by said two or more organic electroluminescent elements being circular in a display according to claim 1.
[Claim 3] It is the display characterized by arranging said two or more organic electroluminescent elements at equal intervals in a display according to claim 1 in the longitudinal direction or the lengthwise direction.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the thin film transistor drive organic electroluminescence display (it is described as TFT-OELD below) equipped with the indicating equipment and the organic electroluminescent element (it is described as Following OELD) of the macromolecule system which drives by the thin film transistor (it is described as Following TFT) especially, and is formed in a liquid phase process.
[0002]
[Description of the Prior Art] Promising ** of TFT-OELD will be carried out in the future as a display which realizes a light weight, a thin shape, small, a high definition, an extensive viewing angle, a low power, etc. Conventional TFT-OELD is shown in drawing 1 , and the sectional view is shown in drawing 2 . Here, although the account of drawing only of the one pixel 11 is carried out, many pixels 11 of a multi-line and two or more trains exist in fact. Here, OLED18 is a giant-molecule system and is formed of liquid phase processes, such as spin coat blade coating and an ink jet.
[0003] In order to realize gradation in the case of structure as shown in drawing 1 , it is necessary to control the current which flows OELD18 by changing the gate voltage of driving TFT17 and changing conductance. However, according to this method, especially in halftone, the variation in the transistor characteristics of driving TFT17 appears as brightness variation of OELD18, and the problem that a screen will become an ununiformity occurs.
[0004] Then, as shown in drawing 3 , the method which realizes gradation was invented by changing the luminescence area of OELD18 (Japanese Patent Application No. No. 233107 [nine to]). The drive approach of this method is shown in drawing 4 . The scan potential 31 is impressed to the scanning line 12, a signal line 13 consists of a signal line (lower bit) 131 and a signal line (high order bit) 132, and the signal potential (lower bit) 321 and the signal potential (high order bit) 322 are respectively impressed as signal potential 32. Driving TFT17 consists of driving TFT(lower bit) 171 and driving TFT(high order bit) 172, and OELD18 consists of OELD (lower bit)181 and OELD (high order bit)182. In this example, since 2-bit 4 gradation is considered, the surface ratio of OELD (lower bit)181 and OELD (high order bit) 182 is set to 1:2.
[0005] By this method, driving TFT17 takes either [two conditions] an ON state perfect in approximation, or an OFF state perfect in approximation. At an ON state, resistance of driving TFT17 is so small that it can be disregarded compared with resistance of OELD18, and the amount of currents which flows driving TFT17 and OELD18 is mostly decided only by resistance of OELD17. Therefore, the variation in the transistor characteristics of driving TFT17 does not appear as brightness variation of OELD18. Moreover, in an OFF state, since the electrical potential difference impressed to OELD18 turns into below a threshold electrical potential difference, OELD18 does not emit light at all and the variation in the transistor characteristics of driving TFT17 does not appear as brightness variation of OELD18 too.
[0006]
[Problem(s) to be Solved by the Invention] Drawing 5 is the sectional view of TFT-OELD which realizes a gradation display by changing the luminescence area of OELD18 shown in drawing 3 and drawing 4 . Drawing 5 (a) is the sectional view of OELD (lower bit)181, and drawing 5 (b) is the sectional view of OELD (high order bit)182. The ratio of the light-emitting part 25 of OELD (lower bit)181 and the light-emitting part 25 of OELD (high order bit)182 is wanted to be set to 1:2.
[0007] A luminous layer 22 is OELD of a macromolecule system, and is formed in a liquid phase process. Since the front face of bank 24 has liquid repellance and a luminous layer 22 does not remain, patterning of OELD18 is carried out and the area is determined. About the side face of bank 24, it is dependent on an ingredient and a process whether it becomes liquid repellance or it becomes lyophilic.

[0008] In drawing 5 , the side face of bank 24 assumes the lyophilic case. As a phenomenon peculiar to a liquid phase process, the luminous layer 22 serves as a cross-section configuration which was able to be drawn near to the side face of bank 24. In this case, in the thinner part of a luminous layer 22, a current flows and this part serves as a light-emitting part 25. The cross-section configuration of the luminous layer 22 which was described here is sensitive to the condition, the temperature, the ambient atmosphere, etc. of the initial valve position and substrate of the physical properties and liquid of the amount and liquid of a liquid, and it is difficult to control. That is, it is difficult to obtain the absolute value of the luminescence area as a wish. For this reason, it is difficult to set correctly the ratio of the light-emitting part 25 of OELD (lower bit)181, and the light-emitting part 25 of OELD (high order bit)182 to 1:2, and it difficult to obtain exact gradation after all.
[0009] Drawing 6 is the sectional view (drawing 6 (a)) of OELD (lower bit)181, and the sectional view (drawing 5 (b)) of OELD (high order bit)182 like drawing 5 . In drawing 6 , the side face of bank 24 assumes the liquid repellance case. As a phenomenon peculiar to a liquid phase process, the luminous layer 22 serves as a cross-section configuration which keeps away from the side face of bank 24. Also in this case, in the thinner part of a luminous layer 22, a current flows and this part serves as a light-emitting part 25. At this time as well as the case of drawing 5 , it is difficult to set correctly the ratio of the light-emitting part 25 of OELD (lower bit)181 and the light-emitting part 25 of OELD (high order bit)182 to 1:2, and it is difficult for obtaining exact gradation.
[0010] Then, the purpose of this invention is obtaining the ratio of the exact light-emitting part 25, and obtaining exact gradation.
[0011]
[Means for Solving the Problem] As for this invention according to claim 1, two or more TFT and two or more OELD (s) are formed in each pixel. (1) TFT and OELD In the display which is connected to a serial, changes the on-off condition of TFT, and realizes gradation by controlling the area which makes OELD emit light two or more OELD(s) It is the same configuration respectively and is the display characterized by realizing gradation by controlling the number which makes OELD emit light.
[0012] Even when OELD becomes the cross-section configuration which keeps away from the cross-section configuration which was able to be drawn near to the side face of a bank, or the side face of a bank as a phenomenon peculiar to a liquid phase process according to this configuration, the light-emitting part of each OELD is made into the same area, and it becomes possible to obtain exact gradation. Although this configuration is also difficult for obtaining the absolute value of the luminescence area as a wish, since the luminescence area of two or more OELD(s) becomes equal mutually, it is controlling these numbers and is because it is possible to make the ratio of luminescence area exact.

[0013] (2) This invention according to claim 2 is a display characterized by two or more OELD(s) being circular in a display according to claim 1.
[0014] According to this configuration, the light-emitting part of each OELD is made more into the same area at accuracy, and it becomes possible to obtain exact gradation. The reason is as follows. In the case of the configuration in which OELD has top-most vertices, such as a rectangle, the top-most-vertices section can be drawn near, or phenomena -- the top-most-vertices section is not filled -- may occur in it. This phenomenon is the same reason as the problem of the above-mentioned cross-section configuration, and becomes the hindrance for obtaining exact gradation. This phenomenon is still more sensitive to the condition, the temperature, the ambient atmosphere, etc. of the initial valve position and substrate of the physical properties and liquid of the amount and liquid of a liquid than the problem of the above-mentioned cross-section configuration, and it is difficult to control also between adjoining OELD(s). By making OELD circular, this phenomenon is avoidable.
[0015] (3) This invention according to claim 3 is a display characterized by arranging two or more OELD(s) at equal intervals in the longitudinal direction or the lengthwise direction in a display according to claim 1.
[0016] According to this configuration, the light-emitting part of each OELD is made more into the same area at accuracy, and it becomes possible to obtain exact gradation. The reason is as follows. When forming OELD by spin coat blade coating, the luminous layer once applied to the whole pixel flows into the crevice of nature and a bank for the liquid repellance on the front face of a bank. Also when an ink jet is caused, occasionally it becomes such. Since all the luminous layers applied to this part flow into a bank crevice at this time when the area of the heights around a bank crevice is large, a luminous layer becomes thick. A luminous layer becomes thin when the area of the heights around a bank crevice is narrow. After all, the variation in the thickness of a luminous layer occurs. This variation is avoidable by arranging two or more OELD(s) at equal intervals to a longitudinal direction or a lengthwise direction.
[0017] Moreover, since what is necessary is according to this configuration just to carry out the ink regurgitation at equal intervals when forming OELD according to an ink jet process, manufacture may become easy.

[0018]
[Embodiment of the Invention] Hereafter, the gestalt of desirable operation of this invention is explained based on a drawing.
[0019] (Example 1) Drawing 7 is drawing showing the pixel of TFT-OELD concerning the example 1 of this invention. Here, although the account of drawing only of the one pixel 11 is carried out, many pixels 11 of a multi-line and two or more trains exist in fact.
[0020] OELD (lower bit)181 consists of OELD (a lower bit and rectangle)1811, and OELD (high order bit)182 consists of OELD (the [a high order bit and] 1 and rectangle)18211 and OELD (the [a high order bit and] 2 and rectangle) 18221. Since OELD(lower bit and rectangle)1811, OELD(the [a high order bit and] 1 and rectangle)18211, and OELD (the [a high order bit and] 2 and rectangle)18221 are carrying out the same configuration as claim 1 showed, the same luminescence area is being obtained and changing the number of OELD18 which emits light, and becomes possible [obtaining exact gradation].
[0021] (Example 2) Drawing 8 is drawing showing the pixel of TFT-OELD concerning the example 2 of this invention. Here, although the account of drawing only of the one pixel 11 is carried out, many pixels 11 of a multi-line and two or more trains exist in fact.
[0022] OELD (lower bit)181 consists of OELD (a lower bit and round shape)1812, and OELD (high order bit)182 consists of OELD (the [a high order bit and] 1 and round shape)18212 and OELD (the [a high order bit and] 2 and round shape)18222. As claim 2 showed, since OELD(lower bit and round shape)1812, OELD(the [a high order bit and] 1 and round shape)18212, and OELD (the [a high order bit and] 2 and round shape)18222 are circular, it becomes possible [the more same luminescence area as accuracy being obtained, and obtaining exact gradation].
[0023] (Example 3) Drawing 9 is drawing showing the pixel of TFT-OELD concerning the example 3 of this invention. Here, although the account of drawing only of the one pixel 11 is carried out, many pixels 11 of a multi-line and two or more trains exist in fact.
[0024] OELD (lower bit)181 consists of OELD (a lower bit and round shape)1812, and OELD (high order bit)182 consists of OELD (the [a high order bit and] 1 and round shape)18212 and OELD (the [a high order bit and] 2 and round shape)18222. As claim 3 showed, OELD(lower bit and round shape)1812, OELD(the [a high order bit and] 1 and round shape)18212, and OELD (the [a high order bit and] 2 and round shape)18222 are arranged at equal intervals in the longitudinal direction and the lengthwise direction also not only to the interior of the pixel 11 but to the adjoining pixel 11. For this reason, the light-emitting part of each OELD is made more into the same area at accuracy, and it becomes possible to obtain exact gradation.
[0025] In addition, as an EL element formed in each pixel, by the example 1, although the rectangle-like component was shown as an example and examples 2 and 3 showed the component of a circle configuration, this invention is not limited to these and can obtain exact gradation also with a component the shape of a polygon, and elliptical. Since especially an elliptical component does not have the top-most-vertices section when considering as the shape of a rectangle like the case of a circle configuration, the problem that the top-most-vertices section is not filled by the luminous layer is absolutely none.
[Effect of the Invention] As stated above, according to this invention, exact gradation is realizable by controlling the light-emitting part area which an electroluminescent element makes emit light.

[Translation done.]

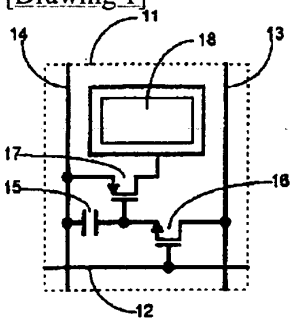
* NOTICES *

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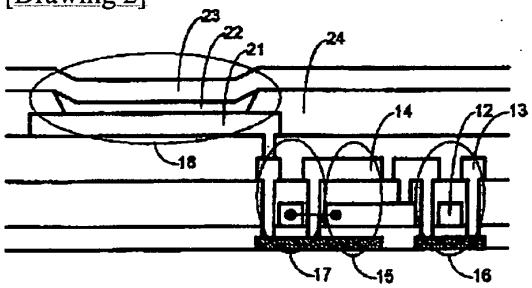
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

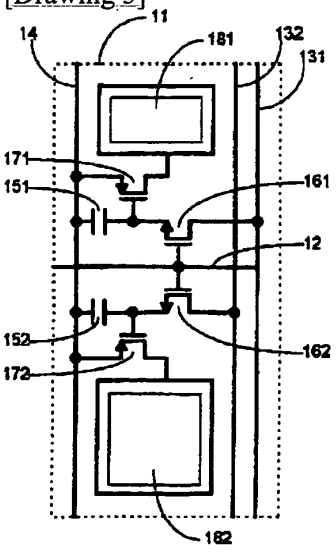
[Drawing 1]



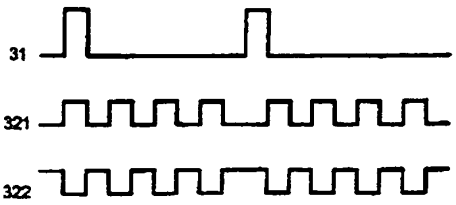
[Drawing 2]



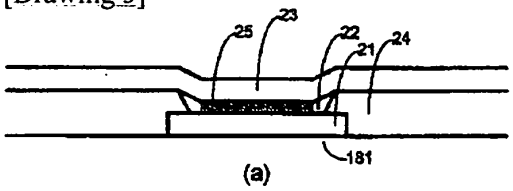
[Drawing 3]

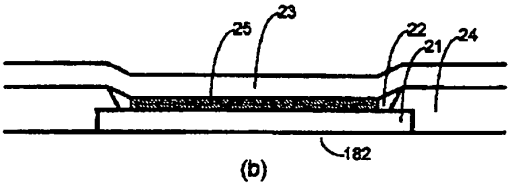


[Drawing 4]

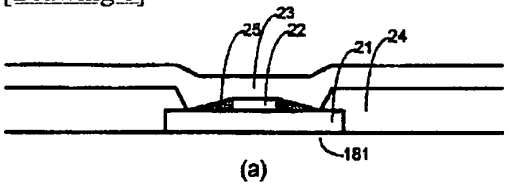


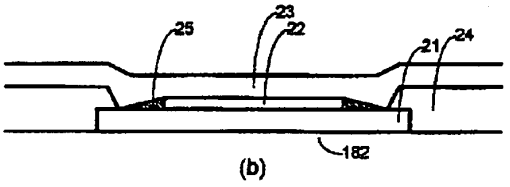
[Drawing 5]



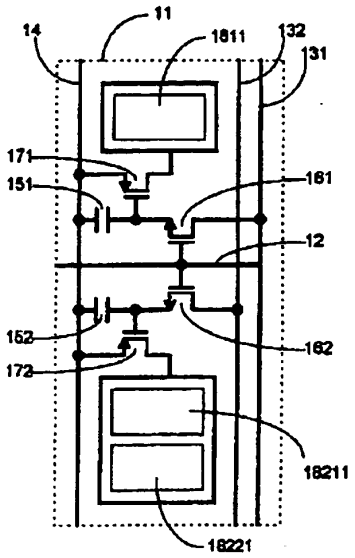


[Drawing 6]

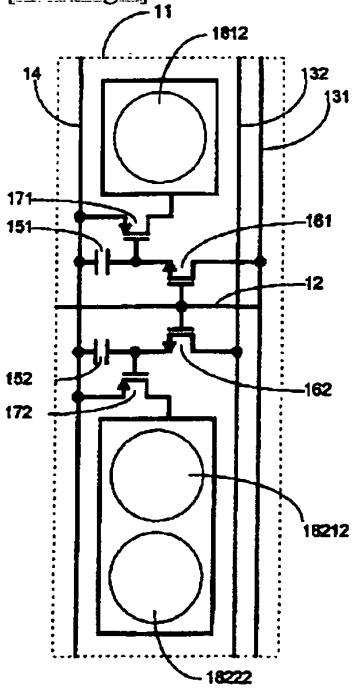




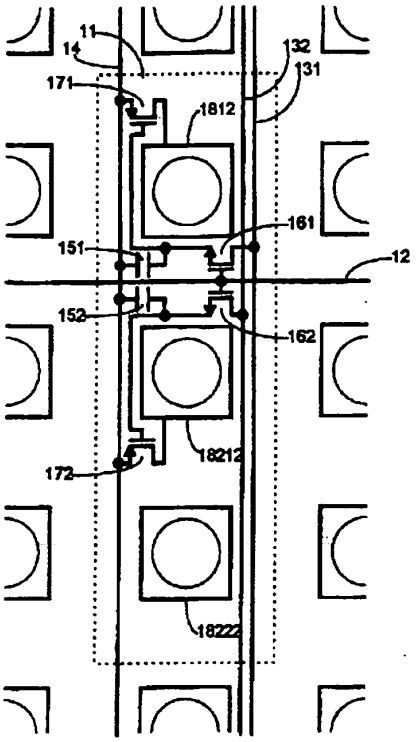
[Drawing 7]



[Drawing 8]



[Drawing 9]



[Translation done.]

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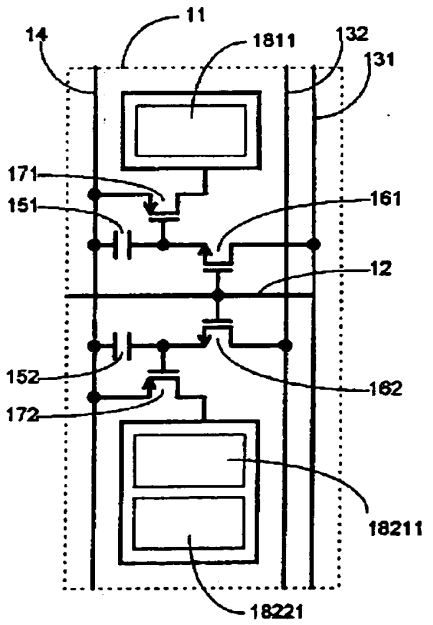
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(54)【発明の名称】　表示装置

(57)【要約】
【課題】　各画素に、複数のTFTおよび複数のOELDが形成され、TFTおよびOELDは、直列に接続され、TFTのオン・オフ状態を切り替え、OELDを発光させる面積を制御することで、階調を実現する、表示装置において、正確な発光部の比を得て、正確な階調を得ることを目的とする。
【解決手段】　複数のOELDは、各々同じ形状であり、OELDを発光させる個数を制御することで、階調を実現する。複数のOELDは、円形である。複数のOELDは、横方向あるいは縦方向に、等間隔に配置されている。これらの構成によれば、複数のOELDの発光面積は互いに等しくなるため、これらの個数を制御することで、発光面積の比を正確にすることが可能となる。



【特許請求の範囲】
【請求項１】 各画素に、複数の薄膜トランジスタおよび複数の有機エレクトロルミネッセンス素子が形成され、前記薄膜トランジスタおよび前記有機エレクトロルミネッセンス素子は、直列に接続され、前記薄膜トランジスタのオン･オフ状態を切り替え、前記有機エレクトロルミネッセンス素子を発光させる面積を制御することで、階調を実現する、表示装置において、
複数の前記有機エレクトロルミネッセンス素子は、各々同じ形状であり、前記有機エレクトロルミネッセンス素子を発光させる個数を制御することで、階調を実現することを特徴とする、表示装置。
【請求項２】 請求項１記載の、表示装置において、複数の前記有機エレクトロルミネッセンス素子は、円形であることを特徴とする、表示装置。
【請求項３】 請求項１記載の、表示装置において、複数の前記有機エレクトロルミネッセンス素子は、横方向あるいは縦方向に、等間隔に配置されていることを特徴とする、表示装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、表示装置、特に、薄膜トランジスタ(以下TFTと記す)により駆動され、液相プロセスにて形成される高分子系の有機エレクトロルミネッセンス素子(以下OELDと記す)を備えた、薄膜トランジスタ駆動有機エレクトロルミネッセンス表示装置(以下TFT-OELDと記す)に関する。
【０００２】
【従来の技術】TFT-OELDは、軽量･薄型･小型･高精細･広視角･低消費電力等を実現する表示装置として、将来的に有望視されている。図１に、従来のTFT-OELDを、図２に、その断面図を示す。ここでは、ひとつの画素11のみ図記しているが、実際には複数行･複数列の多数の画素11が存在する。ここでは、OLED18は高分子系であり、スピンコート･ブレード塗り･インクジェット等の液相プロセスにより形成される。
【０００３】図１に示したような構造の場合、階調を実現するためには、ドライビングTFT17のゲート電圧を変化させ、コンダクタンスを変化させることで、OELD18を流れる電流を制御する必要がある。しかしながら、この方式によれば、特に中間調において、ドライビングTFT17のトランジスタ特性のバラツキが、OELD18の輝度バラツキとして表れてしまい、画面が不均一となってしまうという問題が発生する。
【０００４】そこで、図３に示すように、OELD18の発光面積を変化させることで、階調を実現する方式が考え出された（特願平9-233107号）。図４に、この方式の駆動方法を示す。走査線12に走査電位31が印加され、信号線13は、信号線(下位ビット)131および信号線(上位ビット)132から成り、各々、信号電位32として、信号電位(下位ビット)321および信号電位(上位ビット)322が印加される。ドライビングTFT17は、ドライビングTFT(下位ビット)171およびドライビングTFT(上位ビット)172から成り、OELD18は、OELD(下位ビット)181およびOELD(上位ビット)182から成る。この例では、2ビット4階調について考えているため、OELD(下位ビット)181およびOELD(上位ビット)182の面積比は、1:2となる。
【０００５】この方式では、ドライビングTFT17は、近似的に完全なオン状態および近似的に完全なオフ状態の、2状態のどちらかをとる。オン状態では、ドライビングTFT17の抵抗は、OELD18の抵抗に比べて、無視できるほど小さく、ドライビングTFT17およびOELD18を流れる電流量は、ほぼOELD17の抵抗のみで決まる。故に、ドライビングTFT17のトランジスタ特性のバラツキが、OELD18の輝度バラツキとして表れることはない。また、オフ状態では、OELD18に印加される電圧が、しきい値電圧以下になるため、OELD18は全く発光せず、やはり、ドライビングTFT17のトランジスタ特性のバラツキが、OELD18の輝度バラツキとして表れることはない。
【０００６】
【発明が解決しようとする課題】図５は、図３および図４に示した、OELD18の発光面積を変化させることで階調表示を実現するTFT-OELDの、断面図である。図５(a)は、OELD(下位ビット)181の断面図で、図５(b)は、OELD(上位ビット)182の断面図である。OELD(下位ビット)181の発光部25と、OELD(上位ビット)182の発光部25との比は、1:2になることが望まれている。
【０００７】発光層22は、高分子系のOELDであり、液相プロセスにて形成される。バンク24の表面は、撥液性になっており、発光層22は残らないので、OELD18はパターニングされ、その面積が決定される。バンク24の側面については、撥液性になるか親液性になるかは、材料･プロセスに依存する。
【０００８】図５では、バンク24の側面が、親液性の場合を仮定している。液相プロセス特有の現象として、発光層22が、バンク24の側面に引き寄せられたような断面形状となっている。この場合、発光層22のより薄い部分を電流は流れ、この部分が発光部25となる。ここで述べたような、発光層22の断面形状は、液体の量･液体の物性･液体の初期位置･基板の状態･温度･雰囲気などに敏感で、制御するのは困難である。すなわち、望みどおりの発光面積の絶対値を得ることは、難しい。このため、OELD(下位ビット)181の発光部25と、OELD(上位ビット)182の発光部25との比を、正確に1:2にすることは困難で、結局、正確な階調を得ることは、難しい。
【０００９】図６は、図５と同様、OELD(下位ビット)181の断面図(図６(a))およびOELD(上位ビット)182の断面図(図５(b))である。図６では、バンク24の側面が、撥液性の場合を仮定している。液相プロセス特有の現象として、発光層22が、バンク24の側面から遠ざかるような

断面形状となっている。この場合も、発光層22のより薄い部分を電流は流れ、この部分が発光部25となる。このときも、図5の場合と同様に、OELD(下位ビット)181の発光部25と、OELD(上位ビット)182の発光部25との比を、正確に1:2にすることは困難で、正確な階調を得ることは、難しい。

【0010】そこで、本発明の目的は、正確な発光部25の比を得て、正確な階調を得ることである。

【0011】

【課題を解決するための手段】(1) 請求項1記載の本発明は、各画素に、複数のTFTおよび複数のOELDが形成され、TFTおよびOELDは、直列に接続され、TFTのオン・オフ状態を切り替え、OELDを発光させる面積を制御することで、階調を実現する、表示装置において、複数のOELDは、各々同じ形状であり、OELDを発光させる個数を制御することで、階調を実現することを特徴とする、表示装置である。

【0012】本構成によれば、OELDが、液相プロセス特有の現象として、バンクの側面に引き寄せられたような断面形状あるいはバンクの側面から遠ざかるような断面形状となった場合でも、各OELDの発光部を同一な面積とし、正確な階調を得ることが、可能となる。何故なら、本構成でも、望みどおりの発光面積の絶対値を得ることは、難しいが、複数のOELDの発光面積は互いに等しくなるため、これらの個数を制御することで、発光面積の比を正確にすることが可能だからである。

【0013】(2) 請求項2記載の本発明は、請求項1記載の、表示装置において、複数のOELDは、円形であることを特徴とする、表示装置である。

【0014】本構成によれば、より正確に各OELDの発光部を同一な面積とし、正確な階調を得ることが、可能となる。その理由は、次のとおりである。OELDが矩形等の頂点を持っている形状の場合には、その頂点部の引き寄せられる、あるいは、頂点部が満たされないなどの現象が発生する可能性がある。この現象は、上記した断面形状の問題と同じ理由で、正確な階調を得るための妨げになる。この現象は、上記した断面形状の問題よりも、さらに液体の量・液体の物性・液体の初期位置・基板の状態・温度・雰囲気などに敏感で、隣接するOELD間でも制御するのは困難である。OELDを円形にすることで、この現象を回避できる。

【0015】(3) 請求項3記載の本発明は、請求項1記載の、表示装置において、複数のOELDは、横方向あるいは縦方向に、等間隔に配置されていることを特徴とする、表示装置である。

【0016】本構成によれば、より正確に各OELDの発光部を同一な面積とし、正確な階調を得ることが、可能となる。その理由は、次のとおりである。スピンコート・ブレード塗りでOELDを形成するときは、一旦画素全体に塗布された発光層が、バンク表面の撥液性のために、自然とバンクの凹部に流れ込む。インクジェットのよる場合も、ときにはこのようになる。このとき、バンク凹部の周囲の凸部の面積が広いところでは、この部分に塗布された発光層が、すべてバンク凹部に流れ込むため、発光層は厚くなる。バンク凹部の周囲の凸部の面積が狭いところでは、発光層は薄くなる。結局、発光層の膜厚のバラツキが発生する。複数のOELDを、横方向あるいは縦方向に、等間隔に配置することで、このバラツキを回避できる。

【0017】また、本構成によれば、インクジェットプロセスによりOELDを形成する場合に、等間隔でインク吐出すればよいため、製造が簡単となる可能性がある。

【0018】

【発明の実施の形態】以下、本発明の好ましい実施の形態を、図面に基づいて説明する。

【0019】(実施例1) 図7は、本発明の実施例1に係るTFT-OELDの、画素を示す図である。ここでは、ひとつの画素11のみ図記しているが、実際には複数行・複数列の多数の画素11が存在する。

【0020】OELD(下位ビット)181は、OELD(下位ビット・矩形)1811から成り、OELD(上位ビット)182は、OELD(上位ビット・第1・矩形)18211とOELD(上位ビット・第2・矩形)18221から成っている。請求項1で示したように、OELD(下位ビット・矩形)1811・OELD(上位ビット・第1・矩形)18211・OELD(上位ビット・第2・矩形)18221は同じ形状をしているので、同じ発光面積が得られ、発光するOELD18の個数を変化させることで、正確な階調を得ることが可能となる。

【0021】(実施例2) 図8は、本発明の実施例2に係るTFT-OELDの、画素を示す図である。ここでは、ひとつの画素11のみ図記しているが、実際には複数行・複数列の多数の画素11が存在する。

【0022】OELD(下位ビット)181は、OELD(下位ビット・円形)1812から成り、OELD(上位ビット)182は、OELD(上位ビット・第1・円形)18212とOELD(上位ビット・第2・円形)18222から成っている。請求項2で示したように、OELD(下位ビット・円形)1812・OELD(上位ビット・第1・円形)18212・OELD(上位ビット・第2・円形)18222は、円形となっているので、より正確に同じ発光面積が得られ、正確な階調を得ることが可能となる。

【0023】(実施例3) 図9は、本発明の実施例3に係るTFT-OELDの、画素を示す図である。ここでは、ひとつの画素11のみ図記しているが、実際には複数行・複数列の多数の画素11が存在する。

【0024】OELD(下位ビット)181は、OELD(下位ビット・円形)1812から成り、OELD(上位ビット)182は、OELD(上位ビット・第1・円形)18212とOELD(上位ビット・第2・円形)18222から成っている。請求項3で示したように、OELD(下位ビット・円形)1812・OELD(上位ビット・第1・円形)18212・OELD(上位ビット・第2・円形)18222は、その画素11の

内部だけでなく、隣接する画素11に対しても、横方向および縦方向に、等間隔に配置されている。このため、より正確に各OELDの発光部を同一な面積とし、正確な階調を得ることが、可能となる。

【００２５】なお、各画素に形成されるＥＬ素子として、実施例１では、矩形状の素子を例として示し、実施例２，３では、円形状の素子を示したが、本発明は、これらに限定されるものではなく、多角形状や楕円形状の素子でも正確な階調を得る事ができる。特に、楕円形状の素子は、円形状の場合と同様に、矩形状としたときの頂点部がないので、頂点部が発光層により満たされないという問題は一切ない。

【発明の効果】以上述べたように、本発明によればエレクトロルミネッセンス素子の発光させる発光部面積を制御することにより、正確な階調を実現することができる。

【図面の簡単な説明】

【図１】従来の、TFTのコンダクタンスを変化させることで階調表示を実現するTFT-OELDの、画素を示す図。

【図２】TFT-OELDの、断面図。

【図３】従来の、OELDの発光面積を変化させることで階調表示を実現するTFT-OELDの、画素を示す図。

【図４】従来の、OELDの発光面積を変化させることで階調表示を実現するTFT-OELDの、駆動方法を示す図。

【図５】従来の、OELDの発光面積を変化させることで階調表示を実現するTFT-OELDにおける、OELDの断面図（バンク側面が親液性の場合）。(a)はOELD(下位ビット)の図、(b)はOELD(上位ビット)の図。

【図６】従来の、OELDの発光面積を変化させることで階調表示を実現するTFT-OELDにおける、OELDの断面図（バンク側面が撥液性の場合）。(a)はOELD(下位ビット)の図、(b)はOELD(上位ビット)の図。

【図７】本発明の実施例１に係るTFT-OELDの画素を示す図。

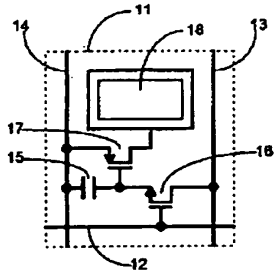
【図８】本発明の実施例２に係るTFT-OELDの画素を示す図。

【図９】本発明の実施例３に係るTFT-OELDの画素を示す図。

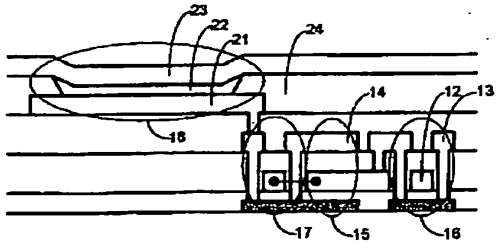
【符号の説明】

１１　画素
１２　走査線
１３　信号線
１３１　信号線(下位ビット)
１３２　信号線(上位ビット)
１４　電流供給線
１５　保持容量
１５１　保持容量(下位ビット)
１５２　保持容量(上位ビット)
１６　サンプリングTFT
１６１　サンプリングTFT(下位ビット)
１６２　サンプリングTFT(上位ビット)
１７　ドライビングTFT
１７１　ドライビングTFT(下位ビット)
１７２　ドライビングTFT(上位ビット)
１８　OELD
１８１　OELD(下位ビット)
１８１１　OELD(下位ビット･矩形)
１８１２　OELD(下位ビット･円形)
１８２　OELD(上位ビット)
１８２１１　OELD(上位ビット･第1･矩形)
１８２２１　OELD(上位ビット･第2･矩形)
１８２１２　OELD(上位ビット･第1･円形)
１８２２２　OELD(上位ビット･第2･円形)
２１　陽極
２２　発光層
２３　陰極
２４　バンク
２５　発光部
３１　走査電位
３２１　信号電位(下位ビット)
３２２　信号電位(上位ビット)

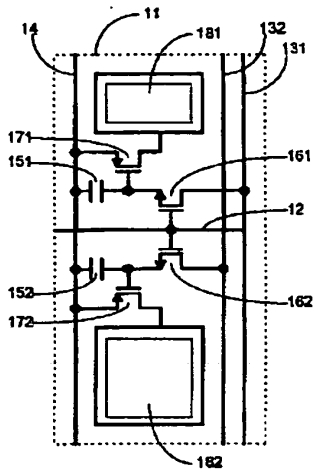
【図１】



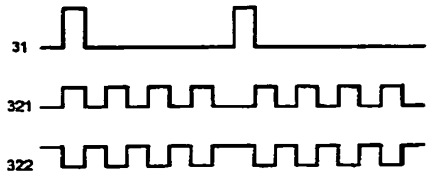
【図２】



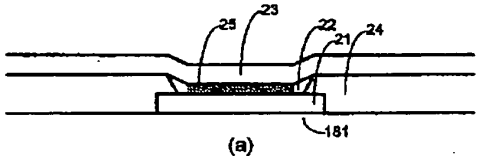
【図3】

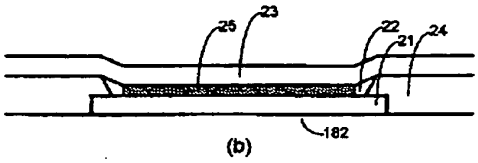


【図4】

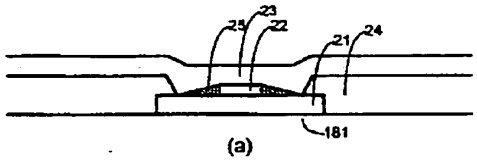


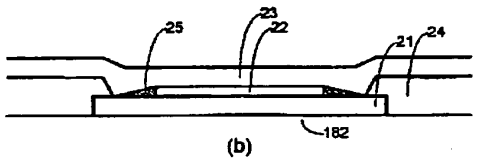
【図5】



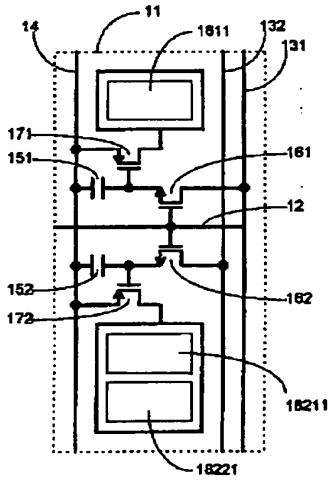


【図6】

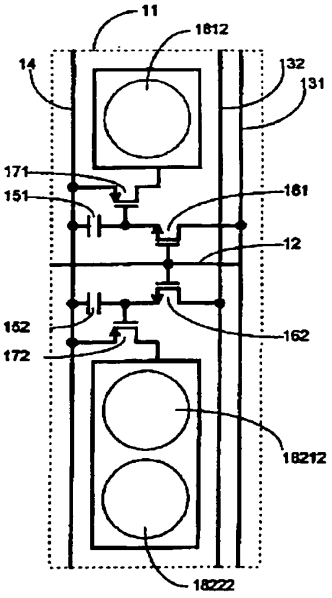




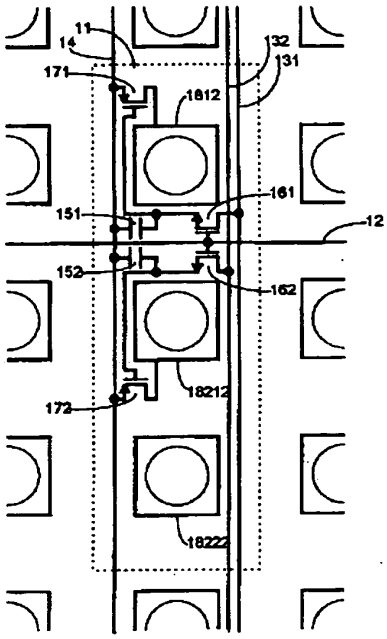
【図7】



【図8】



【図9】



フロントページの続き

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PATENT ABSTRACTS OF JAPAN

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(43)Date of publication of application : 05.03.1999

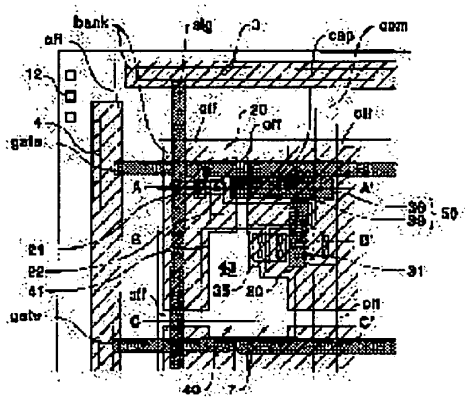
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G09F 9/30
H05B 33/22
H05B 33/26

(21)Application number : 09-225433
(22)Date of filing : 21.08.1997

(71)Applicant : SEIKO EPSON CORP
(72)Inventor : YUDASAKA KAZUO

(54) ACTIVE MATRIX TYPE DISPLAY DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To prevent the occurrence of discontinuity or the like in opposing electrodes formed on the upper layer of a thick insulation film by providing a broken part connecting counter electrode parts to each other of each pixel to an insulation film formed at the lower layer side of the counter electrodes more thickly than an organic semiconductor film through a flat part having no step caused by the insulation film, forming a thick insulation film around the organic semiconductor film and suppressing parasitic capacity.
SOLUTION: A thick insulation film (bank layer 'bank') is provided along a data line 'sig' a scanning line 'gate'. A broken part 'off' is formed on each end part in each extending direction of the data line 'sig' and the scanning line gate in this bank layer 'bank'. Thus, as a thick bank layer bank is interposed between them, the parasitic capacity of the data line 'sig' is extremely small. Moreover, as the thick bank layer 'bank' does not exist on the broken part 'off', it is a flat part having no step caused by the bank layer 'bank' and the counter electrodes formed on this part will not be disconnected.



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CLAIMS

[Claim(s)]
[Claim 1] Two or more data lines which intersect two or more scanning lines and these scanning lines on a substrate, It has the display which consists of two or more pixels formed in the shape of a matrix by this data line and said scanning line. Each of this pixel The flow control circuit containing the thin film transistor by which a scan signal is supplied to a gate electrode through said scanning line, The pixel electrode formed for every pixel, the luminescence thin film by which the laminating was carried out to the upper layer side of this pixel electrode, And it has a thin film light emitting device possessing the counterelectrode formed in the upper layer side of this luminescence thin film. In the active-matrix mold display with which said luminescence thin film emits light based on the picture signal supplied through said flow control circuit from said data line the formation field of said luminescence thin film While being divided by the insulator layer formed in the lower layer side of said counterelectrode more thickly than said luminescence thin film, this insulator layer The active-matrix mold display characterized by the thing to which the counterelectrode parts for every pixel are connected through a part for a flat part without the level difference resulting from the insulator layer concerned, and for which it broke off and has the part.
[Claim 2] The 1st thin film transistor by which, as for said flow control circuit, said scan signal is supplied to a gate electrode in claim 1, It has the 2nd thin film transistor which a gate electrode connects to said data line through this 1st thin film transistor. And this 2nd thin film transistor and said thin film light emitting device The active-matrix mold display characterized by having connected with a serial between the common feeder for the drive current supply sources constituted apart from said data line and scanning line, and said counterelectrode.
[Claim 3] It is the active-matrix mold display characterized by being the bank layer which prevents the flash of discharged liquid in case said luminescence thin film is formed by the ink jet method in the field where said insulator layer was divided by the insulator layer concerned in claims 1 or 2.
[Claim 4] Said insulator layer is a active-matrix mold display with which it is characterized by thickness being 1 micrometers or more in claim 3.
[Claim 5] It is the active-matrix mold display characterized by said thing [having broken off and having the part] at the part which corresponds between the pixels which are formed, become so that said insulator layer may surround the surroundings of the formation field of said luminescence thin film along with said data line and said scanning line in claim 1 thru/or either of 4, and adjoin each other in each installation direction of said data line and said scanning line.
[Claim 6] It is the active-matrix mold display characterized by said thing [having broken off and having the part] at the part which corresponds between the pixels which adjoin each other in the installation direction of said scanning line while having surrounded the surroundings of the formation field of said luminescence thin film by forming said insulator layer along with said data line and said scanning line in claim 1 thru/or either of 4.
[Claim 7] It is the active-matrix mold display characterized by said thing [having broken off and having the part] at the part which corresponds between the pixels which adjoin each other in the installation direction of said data line while having surrounded the surroundings of the formation field of said luminescence thin film by forming said insulator layer along with said data line and said scanning line in claim 1 thru/or either of 4.
[Claim 8] It is the active-matrix mold display which said insulator layer is formed in the shape of a stripe along with said data line in claim 1 thru/or either of 4, and is characterized by said thing [having broken off and having the part] at one [at least] edge of this formation direction.
[Claim 9] It is the active-matrix mold display characterized by covering the formation field of said flow control circuit, and the field with which it laps by said insulator layer among the formation fields of said pixel electrode in claim 5 thru/or either of 8.
[Claim 10] In claim 1 thru/or either of 9 around said display It has the data-line drive circuit which supplies a data signal through said data line, and the scanning-line drive circuit which supplies a scan signal through said scanning line. While

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the active-matrix mold display which carries out drive control of the thin film light emitting devices, such as EL (electroluminescence) component which emits light when a drive current flows to luminescence thin films, such as organic-semiconductor film, or an LED (light emitting diode) component, by the thin film transistor (henceforth TFT).
[0002]
[Description of the Prior Art] The display of the active-matrix mold using current control mold light emitting devices, such as an EL element or an LED component, is proposed. In order that each light emitting device used for this type of indicating equipment may carry out self-luminescence, unlike a liquid crystal display, it does not need a back light, and also has an advantage, like there are few angle-of-visibility dependencies.
[0003] Drawing 13 has shown the block diagram of the active-matrix mold indicating equipment which used the organic thin film EL element of such a charge impregnation mold. Two or more data lines sig installed in the direction which crosses on the transparence substrate 10 to the installation direction of two or more scanning lines gate and this scanning line gate, and two or more pixels 7 formed in the shape of a matrix by two or more common feeders com to which it stands in a row in this data line sig, the data line sig, and the scanning line gate consist of active-matrix mold display 1A shown in this drawing. To the data line sig and the scanning line gate, the data-line drive circuit 3 and the scanning-line drive circuit 4 are constituted. The flow control circuit 50 to which a scan signal is supplied through the scanning line gate, and the thin film light emitting device 40 which emits light based on the picture signal supplied from the data line sig through this flow control circuit 50 are constituted by each pixel 7. In the example shown here, the flow control circuit 50 consists of 1st TFT20 by which a scan signal is supplied to a gate electrode, retention volume cap holding the picture signal with which it is supplied from the data line sig through this 1st TFT20, and 2nd TFT30 by which the picture signal held with this retention volume cap is supplied to a gate electrode through the scanning line gate. The 2nd TFT30 and thin film light emitting device 40 are connected to a serial in detail between Counterelectrodes op and the common feeders com which are mentioned later. This luminescence condition is held for this thin film light emitting device 40 during the predetermined period with retention volume cap while a drive current flows in and emits light from the common feeder com, when 2nd TFT30 is turned on.
[0004] In such active-matrix mold display 1A of a configuration, as shown in drawing 14 and drawing 15 (A), and (B), also in which pixel 7, the 1st TFT20 and 2nd TFT30 are formed using the island-like semi-conductor film. As for 1st TFT20, the gate electrode 21 is constituted as a part of scanning line gate. The data line sig connected with one side of a source drain field electrically through the KONTAKU hole of the 1st interlayer insulation film 51, and the drain electrode 22 has connected 1st TFT20 to another side electrically. The drain electrode 22 is installed towards the formation field of 2nd TFT30, and the gate electrode 31 of 2nd TFT30 has connected it to this installation part electrically through the contact hole of the 1st interlayer insulation film 51. The junction electrode 35 connected with one side of the source drain field of 2nd TFT30 electrically through the contact hole of the 1st interlayer insulation film 51, and the pixel electrode 41 of the thin film light emitting device 40 has connected with this junction electrode 35 electrically through the contact hole of the 2nd interlayer insulation film 52 at it.
[0005] The pixel electrode 41 is formed independently every pixel 7 so that drawing 14 and drawing 15 (B), and (C) may show. The laminating of the organic-semiconductor film 43 and the counterelectrode op is carried out to this order at the upper layer side of the pixel electrode 41. Although the organic-semiconductor film 43 is formed every pixel 7, ranging over two or more pixels 7, it may be formed in the shape of a stripe. Counterelectrode op is formed all over the abbreviation not only for the display 11 but the transparence substrate 10 with which the pixel 7 is constituted so that

drawing 13 may show.
[0006] Again, in drawing 14 and drawing 15 (A), the common feeder com has connected with another side of the source drain field of 2nd TFT30 electrically through the contact hole of the 1st interlayer insulation film 51. To the installation part 36 of the gate electrode 31 of 2nd TFT30, the installation part 39 of the common feeder com counters on both sides of the 1st interlayer insulation film 51 as a dielectric film, and constitutes retention volume cap.
[0007]
[Problem(s) to be Solved by the Invention] However, in the aforementioned active-matrix mold indicating-equipment 1A, since the counterelectrode op which counters the pixel electrode 41 is different from a liquid crystal active-matrix mold indicating equipment and has only the 2nd interlayer insulation film 52 between the data lines sig on the same transparence substrate 10, a big capacity is parasitic on the data line sig, and its load of the data-line drive circuit 3 is large.
[0008] Then, as shown in drawing 13 , drawing 14 and drawing 16 (A), (B), and (C), an invention-in-this-application person prepares a thick insulator layer (field where bank layer bank / lower left attached the slash of ** in the large pitch) between Counterelectrode op, the data line sig, etc., and proposes reducing the capacity which is parasitic on the data line sig. By combining and surrounding the formation field of the organic-semiconductor film 43 by this insulator layer (bank layer bank), in case the organic-semiconductor film 43 is formed from the liquefied ingredient (discharged liquid) breathed out from the ink jet head, discharged liquid is dammed up in the bank layer bank, and it proposes preventing that discharged liquid overflows into the side. However, if this structure is adopted, it will be easy to disconnect the counterelectrode op which it originates in existence of the thick bank layer bank, and the big level difference bb is formed, and is formed in the upper layer of this bank layer bank in the part of the aforementioned level difference bb. If an open circuit arises in Counterelectrode op in such a level difference bb, the counterelectrode op of this part will be in an insulating condition from the surrounding counterelectrode op, and will generate the point defect or line defect of a display. Moreover, if an open circuit takes place to Counterelectrode op along the periphery edge of the wrap bank layer bank, between the counterelectrode op of a display 11 and terminals 12 will be in an insulating condition completely, and a display will completely become impossible [the front face of the data side drive circuit 3 or the scan side drive circuit 4].
[0009] Then, the technical problem of this invention is to offer the active-matrix mold display which an open circuit etc. does not generate in the counterelectrode which forms a thick insulator layer in the surroundings of the organic-semiconductor film, stops parasitic capacitance etc. and is formed in the upper layer of this thick insulator layer.
[0010]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, in this invention, on a substrate Two or more scanning lines, It has the display which consists of two or more pixels formed in the shape of a matrix by two or more data lines which intersect this scanning line, and this data line and said scanning line. Each of this pixel The flow control circuit containing TFT by which a scan signal is supplied to a gate electrode through said scanning line, The pixel electrode formed for every pixel, the luminescence thin film by which the laminating was carried out to the upper layer side of this pixel electrode, And it has a thin film light emitting device possessing the counterelectrode formed in the upper layer side of this luminescence thin film. In the active-matrix mold display with which said thin film light emitting device emits light based on the picture signal supplied through said flow control circuit from said data line While the formation field of said organic-semiconductor film is divided by the insulator layer formed in the lower layer side of said counterelectrode more thickly than said organic-semiconductor film, this insulator layer It is characterized by the thing to which the counterelectrode parts for every pixel are connected through a part for a flat part without the level difference resulting from the insulator layer concerned and for which it broke off and has the part.
[0011] In this invention, since it is in the condition of countering with the data line, the way things stand, a big capacity will be parasitic [it is formed in a counterelectrode display, and] to the data line. However, in this invention, since the thick insulator layer was made to intervene between the data line and a counterelectrode, it can prevent that capacity is parasitic on the data line. Consequently, since the load of a data-line drive circuit can be reduced, low-power-izing or improvement in the speed of a display action can be attained. Moreover, although this insulator layer has a possibility that an open circuit may generate the counterelectrode which forms a big level difference and is formed in that upper layer side when a thick insulator layer is formed, it breaks off to the position of a thick insulator layer, a part is constituted from this invention, and this part is made flat. Therefore, since it has connected electrically certainly through a part for the flat part which an insulator layer breaks off and is equivalent to a part even if it disconnects in this part with the level difference resulting from an insulator layer, since the counterelectrode for every field is electrically connected through the part formed in a part for a flat part, the fault of an open circuit of an opposite substrate does not

occur. So, in a active-matrix mold display, since an open circuit does not occur in the counterelectrode formed in the upper layer of an insulator layer even if it forms a thick insulator layer in the surroundings of the organic-semiconductor film and stops parasitic capacitance etc., the display quality and reliability of a active-matrix mold display can be improved.

[0012] Said flow control circuit is equipped with the 1st TFT by which said scan signal is supplied to a gate electrode, and the 2nd TFT which a gate electrode connects to said data line through this 1st TFT in this invention, and, as for said data line and scanning line, it is [this 2nd TFT and said thin film light emitting device] desirable to have connected with a serial between the common feeder for the drive current supply sources constituted independently and said counterelectrode. That is, although it is also possible to constitute a flow control circuit from one TFT and retention volume, if display grace is carried out from a viewpoint of making it high, it is desirable to constitute the flow control circuit of each pixel from two TFT(s) and retention volume.

[0013] In this invention, in case said insulator layer forms said luminescence thin film by the ink jet method in the field divided by the insulator layer concerned, it is desirable to use as a bank layer which prevents the flash of discharged liquid. As for said insulator layer, to it, it is desirable that thickness is 1 micrometers or more.

[0014] In this invention, said insulator layer constitutes the aforementioned way piece part into the part which corresponds between the pixels which adjoin each other in the direction between the pixels which adjoin each other in the installation direction of said scanning line, or of these both sides between the pixels which adjoin each other in the installation direction of said data line, when the surroundings of the formation field of said luminescence thin film are surrounded along with said data line and said scanning line.

[0015] Unlike the above-mentioned gestalt, said insulator layer may be installed in the shape of a stripe along with said data line, and may constitute the aforementioned way piece part at one [at least] edge of this installation direction in this case.

[0016] As for the formation field of said flow control circuit, and the field with which it laps, in this invention, being covered by said insulator layer is desirable among the formation fields of said pixel electrode. That is, it is desirable to carry out opening of the aforementioned thick insulator layer only by part for the flat part in which said flow control circuit is not formed among the formation fields of said pixel electrode, and to form the organic-semiconductor film only in this inside. Thus, if constituted, the display unevenness resulting from thickness dispersion of the organic-semiconductor film can be prevented. Moreover, in the field which laps with a flow control circuit even if the pixel electrode is formed, even if a drive current flows between counterelectrodes and the organic-semiconductor film emits light to it, this light will be interrupted by the flow control circuit and will not contribute to a display. The drive current which flows on the organic-semiconductor film in the part which does not contribute to this display can be called reactive current seen from the field of a display. So, in this invention, if it is the former, the aforementioned thick insulator layer is formed in the part into which such the reactive current should flow, and it prevents that a drive current flows there. Consequently, since the current which flows to a common feeder can make it small, if width of face of the part and a common feeder is narrowed, as the result, luminescence area can be increased and display engine performance, such as brightness and a contrast ratio, can be raised.

[0017] The data-line drive circuit which supplies a data signal to the perimeter of said display through said data line in this invention, And while having the scanning-line drive circuit which supplies a scan signal through said scanning line and forming said insulator layer also in the upper layer side of this scanning-line drive circuit and said data-line drive circuit The insulator layer concerned has the desirable thing which connect said counterelectrode to the location which corresponds between the formation field of said scanning-line drive circuit, and the formation field of said data-line drive circuit through a part for a flat part without the level difference which originates a said display and substrate periphery side in the insulator layer concerned and for which it broke off and has the part. Thus, if constituted, even if an open circuit occurs the front face of a data-line drive circuit or a scanning-line drive circuit in a counterelectrode along the periphery edge of a wrap insulator layer, the counterelectrode by the side of a display and the counterelectrode by the side of a substrate periphery are connected through a part for a flat part without the level difference resulting from this insulator layer, and the electrical installation between the counterelectrode by the side of a display and the counterelectrode by the side of a substrate periphery can be secured.

[0018] In this invention, when said insulator layer is constituted from organic materials, such as resist film, the thick film can be formed easily. On the other hand, when said insulator layer is constituted from an inorganic material, even if it is in the condition of having contacted the luminescence thin film, deterioration of a luminescence thin film can be prevented.

[0019]

[Embodiment of the Invention] The gestalt of operation of this invention is explained with reference to a drawing. In

addition, in the following explanation, the same sign is given to the part which is common to the element explaining drawing 13 thru/or drawing 16 .

[0020] [The gestalt 1 of operation]

(Whole configuration) Drawing 1 is the block diagram showing typically the layout of the whole active-matrix mold indicating equipment. The top view which drawing 2 extracts one of the pixels constituted by it, and is shown, drawing 3 (A), (B), and (C) are the A-A' sectional views, B-B' sectional views, and C-C' sectional views of drawing 2 , respectively.

[0021] Let the central part of the base slack transparence substrate 10 be a display 11 in the active-matrix mold display 1 shown in drawing 1 . The data side drive circuit 3 which outputs a picture signal to the edge of the data line sig among the periphery parts of the transparence substrate 10 is constituted, and the scan side drive circuit 4 which outputs a scan signal is constituted by the edge of the scanning line gate. A complementary type TFT is constituted by TFT of N type, and TFT of P type, and this complementary type TFT constitutes the shift register circuit, the level-shifter circuit, the analog switch circuit, etc. from these drive circuits 3 and 4 by them. Two or more data lines sig installed in the direction which crosses on the transparence substrate 10 to the installation direction of two or more scanning lines gate and this scanning line gate like the active-matrix substrate of a liquid crystal active-matrix mold indicating equipment, and two or more pixels 7 formed in the shape of a matrix by the data line sig and the scanning line gate consist of displays 11.

[0022] The flow control circuit 50 to which a scan signal is supplied through the scanning line gate, and the thin film light emitting device 40 which emits light based on the picture signal supplied from the data line sig through this flow control circuit 50 are constituted by each pixel 7. In the example shown here, the flow control circuit 50 consists of 1st TFT20 by which a scan signal is supplied to a gate electrode, retention volume cap holding the picture signal with which it is supplied from the data line sig through this 1st TFT20, and 2nd TFT30 by which the picture signal held with this retention volume cap is supplied to a gate electrode through the scanning line gate. The 2nd TFT30 and thin film light emitting device 40 are connected to a serial in detail between Counterelectrodes op and the common feeders com which are mentioned later.

[0023] With such a active-matrix mold display 1 of a configuration, they are drawing 2 and drawing 3 (as shown in (A) and (B), also in which pixel 7, the 1st TFT20 and 2nd TFT30 are formed using the island-like semi-conductor film (silicon film).).

[0024] As for 1st TFT20, the gate electrode 21 is constituted as a part of scanning line gate. The data line sig connected with one side of a source drain field electrically through the KONTAKU hole of the 1st interlayer insulation film 51, and the drain electrode 22 has connected 1st TFT20 to another side electrically. The drain electrode 22 is installed towards the formation field of 2nd TFT30, and the gate electrode 31 of 2nd TFT30 has connected it to this installation part electrically through the contact hole of the 1st interlayer insulation film 51.

[0025] The junction electrode 35 by which coincidence formation was carried out with the data line sig through the contact hole of the 1st interlayer insulation film 51 connected with one side of the source drain field of 2nd TFT30 electrically, and the transparent pixel electrode 41 which consists of ITO film of the thin film light emitting device 40 through the contact hole of the 2nd interlayer insulation film 52 has connected with this junction electrode 35 electrically.

[0026] The pixel electrode 41 is formed independently every pixel 7 so that drawing 2 and drawing 3 (B), and (C) may show. The laminating of the counterelectrode op which is from metal membranes, such as the organic-semiconductor film 43 which consists of those, such as polyphenylene vinylene (PPV), as a luminescence thin film and lithium content aluminum, and calcium, on the upper layer side of the pixel electrode 41 is carried out to this order, and the thin film light emitting device 40 is constituted. Although the organic-semiconductor film 43 is formed in each pixel 7, ranging over two or more pixels 7, it may be formed in the shape of a stripe. Counterelectrode op is formed in the display 11 whole and the field except the perimeter of a part in which the terminal 12 of the transparence substrate 10 is formed. This terminal 12 contains the terminal of the counterelectrode op linked to wiring (not shown) by which coincidence formation was carried out with Counterelectrode op.

[0027] In addition, the structure in which the both sides of the structure which prepared the hole-injection layer and raised luminous efficiency (rate of a hole injection) as a thin film light emitting device 40, the structure which prepared the electron injection layer and raised luminous efficiency (electron injection efficiency), a hole-injection layer, and an electron injection layer were formed is also employable.

[0028] Again, in drawing 2 and drawing 3 (A), the common feeder com has connected with another side of the source drain field of 2nd TFT30 electrically through the contact hole of the 1st interlayer insulation film 51. To the installation part 36 of the gate electrode 31 of 2nd TFT30, the installation part 39 of the common feeder com counters on both sides of the 1st interlayer insulation film 51 as a dielectric film, and constitutes retention volume cap.

[0029] Thus, in the active-matrix mold display 1, if it is chosen by the scan signal and 1st TFT20 is turned on, while the picture signal from the data line sig will be impressed to the gate electrode 31 of 2nd TFT30 through 1st TFT20, a picture signal is written in retention volume cap through 1st TFT20. Consequently, if 2nd TFT30 is turned on, an electrical potential difference will be impressed by using Counterelectrode op and the pixel electrode 41 as a negative electrode and a positive electrode, respectively, and the current (drive current) which flows on the organic-semiconductor film 43 in the field in which applied voltage exceeded the threshold electrical potential difference will increase rapidly. Therefore, a light emitting device 40 emits light as an electroluminescent element or an LED component, it is reflected by Counterelectrode op, and the light of a light emitting device 40 penetrates the transparent pixel electrode 41 and the transparence substrate 10, and outgoing radiation is carried out. The drive current for performing such luminescence will not flow, if 2nd TFT30 is turned off in order to flow Counterelectrode op, the organic-semiconductor film 43, the pixel electrode 41, 2nd TFT30, and the current path that consists of common feeders com. However, since the gate electrode of 2nd TFT30 is held at the potential which is equivalent to a picture signal with retention volume cap even if 1st TFT20 is turned off, 2nd TFT30 is still an ON state. So, a drive current continues flowing to a light emitting device 40, and this pixel is still a lighting condition. New image data is written in retention volume cap, and this condition is maintained until 2nd TFT30 is turned off.

[0030] In the active-matrix mold display 1 constituted in this way (Structure of a bank layer) With this gestalt In order to prevent that a big capacity is parasitic on the data line sig, as it is shown in drawing 1 , drawing 2 and drawing 3 (A), (B), and (C) Along with the data line sig and the scanning line gate, the thick insulator layer (field where bank layer bank / lower left attached the slash of ** in the large pitch) which consists of resist film or polyimide film is prepared, and Counterelectrode op is formed in the upper layer side of this bank layer bank. For this reason, since the 2nd interlayer insulation film 52 and the thick bank layer bank intervene between the data line sig and Counterelectrode op, the capacity which is parasitic on the data line sig is very small. So, the load of the drive circuits 3 and 4 can be reduced and low-power-izing or improvement in the speed of a display action can be attained.

[0031] Moreover, as shown in drawing 1 , the bank layer bank (the slash is given to the formation field.) is formed also in the boundary region (outside field of a display 11) of the transparence substrate 10. Therefore, the data side drive circuit 3 and the scan side drive circuit 4 are all covered with the bank layer bank. Counterelectrode op needs to be formed in a display 11 at least, and it is not necessary to form it in a drive circuit field. However, since Counterelectrode op is usually formed by the mask spatter method, doubling precision may be bad and Counterelectrode op and a drive circuit may lap. However, with this gestalt, even if it is in the condition that Counterelectrode op laps to the formation field of these drive circuits, the bank layer bank will intervene between the wiring layer of a drive circuit, and Counterelectrode op. So, since it can prevent that capacity is parasitic on the drive circuits 3 and 4, the load of the drive circuits 3 and 4 can be reduced and low-power-izing or improvement in the speed of a display action can be attained.

[0032] Furthermore, the bank layer bank is formed also in the field which laps with the junction electrode 35 of the flow control circuit 50 among the formation fields of the pixel electrode 41 with this gestalt. For this reason, the organic-semiconductor film 43 is not formed in the field which laps with the junction electrode 35. That is, since the organic-semiconductor film 43 is formed only in a flat part among the formation fields of the pixel electrode 41, the organic-semiconductor film 43 is formed by fixed thickness, and does not cause display unevenness. Moreover, if there is no bank layer bank in the field which laps with the junction electrode 35, also in this part, a drive current will flow between Counterelectrodes op and the organic-semiconductor film 43 will emit light to it. However, this light is inserted between the junction electrode 35 and Counterelectrode op, and outgoing radiation is not carried out outside, and it does not contribute to a display. The drive current which flows in the part which does not contribute to this display can be called reactive current seen from the field of a display. However, with this gestalt, since it prevents that form the bank layer bank in the part into which such the reactive current should flow, and a drive current flows there if it is the former, it can prevent that a useless current flows to the common feeder com. So, the width of face of the common feeder com may be narrow that much. As the result, luminescence area can be increased and display engine performance, such as brightness and a contrast ratio, can be raised.

[0033] By this gestalt, since the bank layer bank is formed along with the data line sig and the scanning line gate, any pixel 7 is surrounded in the thick bank layer bank further again. For this reason, the way things stand, the counterelectrode op of each pixel 7 will connect the bank layer bank with the counterelectrode op of the pixel 7 which gets over and adjoins. However, with this gestalt, it breaks off into the part which corresponds between the pixels 7 which adjoin each other in the installation direction of the data line sig, and Part off is formed in the bank layer bank. Moreover, it breaks off also into the part which corresponds between the pixels 7 which adjoin each other in the installation direction of the scanning line gate, and Part off is formed in the bank layer bank. Furthermore, it breaks off to each of the edge of each installation direction of the data line sig and the scanning line gate, and Part off is formed in

the bank layer bank.
[0034] Since it breaks off and Part off does not have the thick bank layer bank, the counterelectrode op which is a part for a flat part without such a big level difference resulting from the bank layer bank, and is formed in this part is not disconnected. Therefore, the counterelectrode 7 of each pixel 7 will be certainly connected through a part for a flat part without the level difference resulting from the bank layer bank. So, even if it forms a thick insulator layer (bank layer bank) in the surroundings of a pixel 7 and stops parasitic capacitance etc., an open circuit does not occur in the counterelectrode op formed in the upper layer of this thick insulator layer (bank layer bank).
[0035] And the bank layer bank formed in the upper layer side of the scan side drive circuit 4 and the data side drive circuit 3 breaks off in the location which corresponds between the formation field of the scan side drive circuit 4, and the formation field of the data side drive circuit 3, and Part off is formed. For this reason, the near counterelectrode op of a display 11 and the counterelectrode op by the side of a substrate periphery are parts for the flat part which the bank layer bank breaks off, connect through Part off, and do not have this level difference to which it breaks off and Part off originates in the bank layer bank. Therefore, since this counterelectrode op that breaks off and is formed in Part off is not disconnected, the bank layer bank broke off, it connected certainly through Part off, and the near counterelectrode op of a display 11 and the counterelectrode op by the side of a substrate periphery have connected certainly to the counterelectrode op by the side of this substrate periphery the terminal 12 by which wiring connection is made, and the counterelectrode op of a display 11.
[0036] In addition, if the bank layer bank is formed by the black resist, the bank layer bank will function as a black matrix, and its grace of displays, such as a contrast ratio, will improve. That is, in the active-matrix mold display 1 concerning this gestalt, since Counterelectrode op is formed in the front-face side of the transparence substrate 10 all over a pixel 7, the reflected light in Counterelectrode op reduces a contrast ratio. However, if the bank layer bank which bears the function to prevent parasitic capacitance is constituted from a black resist, since the bank layer bank will function also as a black matrix and the reflected light from Counterelectrode op will be interrupted, a contrast ratio improves.
[0037] (The manufacture approach of a active-matrix mold indicating equipment) Since the bank layer bank formed in this way is constituted so that the formation field of the organic-semiconductor film 43 may be surrounded, in the production process of a active-matrix mold indicating equipment, in case the organic-semiconductor film 43 is formed from the liquefied ingredient (discharged liquid) breathed out from the ink jet head, discharged liquid is dammed up, and it prevents that discharged liquid overflows into the side. In addition, in the manufacture approach of the active-matrix mold display 1 explained below, since the process until it manufactures the 1st TFT20 and 2nd TFT30 on the transparence substrate 10 is the same as that of the process and abbreviation which manufacture the active-matrix substrate of the liquid crystal active-matrix mold display 1, with reference to drawing 3 (A), (B), and (C), the outline is explained briefly.
[0038] First, after forming the substrate protective coat (not shown) which thickness becomes from the silicon oxide which is about 2000-5000A by the plasma-CVD method by making TEOS (tetra-ethoxy silane), oxygen gas, etc. into material gas to the transparence substrate 10 if needed, the semi-conductor film which thickness becomes from the amorphous silicon film which is about 300-700A by the plasma-CVD method is formed in the front face of a substrate protective coat. Next, to the semi-conductor film which consists of amorphous silicon film, crystallization processes, such as laser annealing or a solid phase grown method, are performed, and the semi-conductor film is crystallized on the polish recon film.
[0039] Next, the gate dielectric film 57 which patterning of the semi-conductor film is carried out, it considers as the island-like semi-conductor film, and thickness becomes from the silicon oxide or the nitride which is about 600-1500A by the plasma-CVD method to the front face by making TEOS (tetra-ethoxy silane), oxygen gas, etc. into material gas is formed.
[0040] Next, after forming the electric conduction film which consists of metal membranes, such as aluminum, a tantalum, molybdenum, titanium, and a tungsten, by the spatter, patterning is carried out and the installation parts 36 of the gate electrodes 21 and 31 and the gate electrode 31 are formed (gate electrode formation process). The scanning line gate is formed at this process.
[0041] In this condition, high-concentration phosphorus ion is driven in and a source drain field is formed in self align to the gate electrodes 21 and 31. In addition, the part into which an impurity was not introduced serves as a channel field.
[0042] Next, after forming the 1st interlayer insulation film 51, each contact hole is formed, next the installation parts 39 of data-line sig, the drain electrode 22, the common feeder com, and the common feeder com and the junction electrode 35 are formed. Consequently, 1st TFT20, 2nd TFT30, and retention volume cap are formed.

[0043] Next, the 2nd interlayer insulation film 52 is formed and contact hole formation is carried out at the part which is equivalent to this interlayer insulation film at the junction electrode 35. Next, after forming the ITO film in the whole front face of the 2nd interlayer insulation film 52, patterning is carried out and the pixel electrode 41 connected electrically is formed in the source drain field of 2nd TFT30 every pixel 7 through a contact hole.
[0044] Next, after forming a resist layer in the front-face side of the 2nd interlayer insulation film 52, patterning is carried out so that it may leave this resist along with the scanning line gate and the data line sig, and the bank layer bank is formed. Moreover, it breaks off into the predetermined part of the bank layer bank, and Part off is formed. At this time, the resist part which it leaves along with the data line sig presupposes that it is broad so that the common feeder com may be covered. Consequently, the field which should form the organic-semiconductor film 43 of a light emitting device 40 is surrounded by the bank layer bank.
[0045] Next, each organic-semiconductor film 43 corresponding to R, G, and B is formed using the ink jet method in the field divided in the shape of a matrix in the bank layer bank. To the inside field of the bank layer bank, from an ink jet head, the liquefied ingredient (precursor) for constituting the organic-semiconductor film 43 is fixed to it by discharge, it is fixed to it in the inside field of the bank layer bank, and the organic-semiconductor film 43 is formed in it. Here, since the bank layer bank consists of resists, it is water repellence. On the other hand, it does not overflow into the pixel 7 which it costs even if it breaks off in the bank layer bank which divides the formation field of the organic-semiconductor film 43 even if since the precursor of the organic-semiconductor film 43 uses the solvent of a hydrophilic property and there is a part off and which the spreading field of the organic-semiconductor film 43 is certainly prescribed by the bank layer bank, and adjoins since it breaks off and Part off is narrow. So, the organic-semiconductor film 43 etc. can be formed only in a predetermined field. In this process, in order that the precursor breathed out from the ink jet head may rise in thickness of about 2 micrometers thru/or about 4 micrometers under the effect of surface tension, the thickness of about 1 micrometer thru/or about 3 micrometers is required for the bank layer bank. In addition, the thickness of the organic-semiconductor film 43 after being established is about 0.05 micrometers to about 0.2 micrometers. In addition, if the septum which consists of a bank layer bank beforehand is 1 micrometers or more in height, even if the bank layer bank is not water repellence, the bank layer bank will fully function as a septum. If this thick bank layer bank is formed, it replaces with the ink jet method, and even when forming the organic-semiconductor film 43 by the applying method, the formation field can be specified.
[0046] Counterelectrode op is formed in after an appropriate time all over the abbreviation for the transparence substrate 10.
[0047] According to such a manufacture approach, since each organic-semiconductor film 43 corresponding to R, G, and B can be formed in the predetermined field using the ink jet method, the full color active-matrix mold display 1 can be manufactured for high productivity.
[0048] In addition, although TFT is formed also in the data side drive circuit 3 shown in drawing 1 , or the scan side drive circuit 4, these TFT(s) use all or a part of processes which forms TFT for the aforementioned pixel 7, and are performed. So, TFT which constitutes a drive circuit will also be formed between the same layers as TFT of a pixel 7. Moreover, about said 1st TFT20 and 2nd TFT30, since N type and both sides can form TFT by the well-known approach even if P type and one side are which such combination in N type, although any of P type are sufficient as another side, both sides omit the explanation.
[0049] [Modification 1 of gestalt 1 of operation] drawing 4 is the block diagram showing typically the layout of the whole active-matrix mold indicating equipment. The top view which drawing 5 extracts one of the pixels constituted by it, and is shown, drawing 6 (A), (B), and (C) are the A-A' sectional views, B-B' sectional views, and C-C' sectional views of drawing 5 , respectively. In addition, since a configuration with fundamental this gestalt and gestalt 1 of operation is identitas, the sign same into a common part is given to each drawing, and those detailed explanation is omitted.
[0050] As shown in drawing 4 , drawing 5 and drawing 6 (A), (B), and (C), the thick insulator layer (field where bank layer bank / lower left attached the slash of ** in the large pitch) which the active-matrix mold indicating equipment 1 of this gestalt also becomes from the resist film along with the data line sig and the scanning line gate is prepared, and Counterelectrode op is formed in the upper layer side of this bank layer bank. For this reason, since the 2nd interlayer insulation film 52 and the thick bank layer bank intervene between the data line sig and Counterelectrode op, the capacity which is parasitic on the data line sig is very small. So, the load of the drive circuits 3 and 4 can be reduced and low-power-izing or improvement in the speed of a display action can be attained.
[0051] Moreover, the bank layer bank (the slash is given to the formation field.) is formed also in the boundary region (outside field of a display 11) of the transparence substrate 10. Therefore, the data side drive circuit 3 and the scan side drive circuit 4 are all covered with the bank layer bank. For this reason, even if it is in the condition that

Counterelectrode op laps to the formation field of these drive circuits, the bank layer bank will intervene between the wiring layer of a drive circuit, and Counterelectrode op. So, since it can prevent that capacity is parasitic on the drive circuits 3 and 4, the load of the drive circuits 3 and 4 can be reduced and low-power-izing or improvement in the speed of a display action can be attained.

[0052] Furthermore, with this gestalt, since the bank layer bank is formed also in the field which laps with the junction electrode 35 of the flow control circuit 50 among the formation fields of the pixel electrode 41, it can prevent that the useless reactive current flows. So, the width of face of the common feeder com may be narrow that much.

[0053] By this gestalt, since the bank layer bank is formed along with the data line sig and the scanning line gate, any pixel 7 is surrounded in the bank layer bank further again. For this reason, since each organic-semiconductor film 43 corresponding to R, G, and B can be formed in the predetermined field using the ink jet method, the full color active-matrix mold display 1 can be manufactured for high productivity.

[0054] And it breaks off into the part which corresponds between the pixels 7 which adjoin each other in the installation direction of the scanning line gate, and Part off is formed in the bank layer bank. Moreover, it breaks off also to each of the edge of each installation direction of the data line sig and the scanning line gate, and Part off is formed in the bank layer bank. Furthermore, the bank layer bank formed in the upper layer side of the scan side drive circuit 4 and the data side drive circuit 3 breaks off in the location which corresponds between the formation field of the scan side drive circuit 4, and the formation field of the data side drive circuit 3, and Part off is formed. Therefore, through a part for a flat part without the level difference resulting from the bank layer bank (breaking off the part off), it connects certainly and Counterelectrode op is not disconnected.

[0055] [Modification 2 of gestalt 1 of operation] drawing 7 is the block diagram showing typically the layout of the whole active-matrix mold indicating equipment. The top view which drawing 8 extracts one of the pixels constituted by it, and is shown, drawing 9 (A), (B), and (C) are the A-A' sectional views, B-B' sectional views, and C-C' sectional views of drawing 8 , respectively. In addition, since a configuration with fundamental this gestalt and gestalt 1 of operation is identitas, the sign same into a common part is given to each drawing, and those detailed explanation is omitted.

[0056] As shown in drawing 7 , drawing 8 and drawing 9 (A), (B), and (C), the thick insulator layer (field where bank layer bank / lower left attached the slash of ** in the large pitch) which the active-matrix mold indicating equipment 1 of this gestalt also becomes from the resist film along with the data line sig and the scanning line gate is prepared, and Counterelectrode op is formed in the upper layer side of this bank layer bank. For this reason, since the 2nd interlayer insulation film 52 and the thick bank layer bank intervene between the data line sig and Counterelectrode op, the capacity which is parasitic on the data line sig is very small. So, the load of the drive circuits 3 and 4 can be reduced and low-power-izing or improvement in the speed of a display action can be attained.

[0057] Moreover, the bank layer bank (the slash is given to the formation field.) is formed also in the boundary region (outside field of a display 11) of the transparence substrate 10. Therefore, the data side drive circuit 3 and the scan side drive circuit 4 are all covered with the bank layer bank. For this reason, even if it is in the condition that Counterelectrode op laps to the formation field of these drive circuits, the bank layer bank will intervene between the wiring layer of a drive circuit, and Counterelectrode op. So, since it can prevent that capacity is parasitic on the drive circuits 3 and 4, the load of the drive circuits 3 and 4 can be reduced and low-power-izing or improvement in the speed of a display action can be attained.

[0058] Furthermore, with this gestalt, since the bank layer bank is formed also in the field which laps with the junction electrode 35 of the flow control circuit 50 among the formation fields of the pixel electrode 41, it can prevent that the useless reactive current flows. So, the width of face of the common feeder com may be narrow that much.

[0059] By this gestalt, since the bank layer bank is formed along with the data line sig and the scanning line gate, any pixel 7 is surrounded in the bank layer bank further again. For this reason, since each organic-semiconductor film 43 corresponding to R, G, and B can be formed in the predetermined field using the ink jet method, the full color active-matrix mold display 1 can be manufactured for high productivity.

[0060] And it breaks off into the part which corresponds between the pixels 7 which adjoin each other in the installation direction of the data line sig, and Part off is formed in the bank layer bank. Moreover, it breaks off also to each of the edge of each installation direction of the data line sig and the scanning line gate, and Part off is formed in the bank layer bank. Furthermore, the bank layer bank formed in the upper layer side of the scan side drive circuit 4 and the data side drive circuit 3 breaks off in the location which corresponds between the formation field of the scan side drive circuit 4, and the formation field of the data side drive circuit 3, and Part off is formed. Therefore, through a part for a flat part without the level difference resulting from the bank layer bank (breaking off the part off), it connects certainly and Counterelectrode op is not disconnected.

[0061] [Gestalt 2 of operation] drawing 10 is the block diagram showing typically the layout of the whole active-matrix mold indicating equipment. The top view which drawing 11 extracts one of the pixels constituted by it, and is shown, drawing 12 (A), (B), and (C) are the A-A' sectional views, B-B' sectional views, and C-C' sectional views of drawing 11 , respectively. In addition, since a configuration with fundamental this gestalt and gestalt 1 of operation is identitas, the sign same into a common part is given to each drawing, and those detailed explanation is omitted.
[0062] As shown in drawing 10 , drawing 11 and drawing 12 (A), (B), and (C), in the active-matrix mold indicating equipment 1 of this gestalt, along with the data line sig, the thick insulator layer (field where bank layer bank / lower left attached the slash of ** in the large pitch) which consists of resist film is formed in the shape of a stripe, and has formed Counterelectrode op in the upper layer side of this bank layer bank. For this reason, since the 2nd interlayer insulation film 52 and the thick bank layer bank intervene between the data line sig and Counterelectrode op, the capacity which is parasitic on the data line sig is very small. So, the load of the drive circuits 3 and 4 can be reduced and low-power-izing or improvement in the speed of a display action can be attained.
[0063] Moreover, the bank layer bank (the slash is given to the formation field.) is formed also in the boundary region (outside field of a display 11) of the transparence substrate 10. Therefore, since the data side drive circuit 3 and the scan side drive circuit 4 are covered with the bank layer bank, even if each is in the condition that Counterelectrode op laps to the formation field of these drive circuits, the bank layer bank will intervene between the wiring layer of a drive circuit, and Counterelectrode op. So, since it can prevent that capacity is parasitic on the drive circuits 3 and 4, the load of the drive circuits 3 and 4 can be reduced and low-power-izing or improvement in the speed of a display action can be attained.
[0064] Furthermore, in this gestalt, since the bank layer bank is formed along with the data line sig and each organic-semiconductor film 43 corresponding to R, G, and B can be formed in the shape of a stripe using the ink jet method in the field divided in the shape of a stripe in the bank layer bank, the full color active-matrix mold display 1 can be manufactured for high productivity.
[0065] And it breaks off at the edge of the installation direction of the data line sig, and Part off is formed in the bank layer bank. Therefore, in the installation direction of the scanning line gate, to the counterelectrode op of the adjoining pixel 7, the counterelectrode op of each pixel 7 overcame the thick bank layer bank, and has connected. If the installation direction of the data line sig is still followed, the counterelectrode op of each pixel 7 will break off at the edge of the data line sig, and it is Part off (a part for a flat part without the level difference resulting from the bank layer bank) (it minded and has connected with the train of the pixel 7 which adjoins in the installation direction of the scanning line gate.). So, it can say that the counterelectrode op of each pixel 7 is connected to the counterelectrode op of other pixels 7 through a part for a flat part without the level difference resulting from the bank layer bank, and neither of the counterelectrodes op of the pixels 7 will be in an open-circuit condition.
[0066] When [which is [the gestalt of other operations]] the bank layer bank (insulator layer) constitutes from organic materials, such as resist film and polyimide film, the thick film can be formed easily, but when the bank layer bank (insulator layer) is constituted from inorganic materials, such as silicon oxide which formed membranes by the CVD method or the SOG method, or a silicon nitride, even if it is in the condition of having contacted the organic-semiconductor film 43, deterioration of the organic-semiconductor film 43 can be prevented.
[0067] Moreover, about retention volume cap, you may form between the scanning line gate besides the structure formed between the common feeders com, and the capacity line formed in juxtaposition.
[0068]
[Effect of the Invention] As explained above, since the thick insulator layer was made to intervene between the data line and a counterelectrode, with the active-matrix mold indicating equipment concerning this invention, it can prevent that capacity is parasitic on the data line. So, since the load of a data-line drive circuit can be reduced, low-power-izing or improvement in the speed of a display action can be attained. Moreover, it breaks off to the position of a thick insulator layer, a part is constituted, and this part is made flat. Therefore, since the counterelectrode for every field is electrically connected through the part formed in a part for a flat part, even if it disconnects in this part with the level difference resulting from an insulator layer, it has connected electrically certainly through a part for the flat part which an insulator layer breaks off and is equivalent to a part. Therefore, since an open circuit does not occur in the counterelectrode formed in the upper layer of an insulator layer even if it forms a thick insulator layer in the surroundings of luminescence thin films, such as organic-semiconductor film, and stops parasitic capacitance etc., the display quality and reliability of a active-matrix mold display can be improved.

[Translation done.]

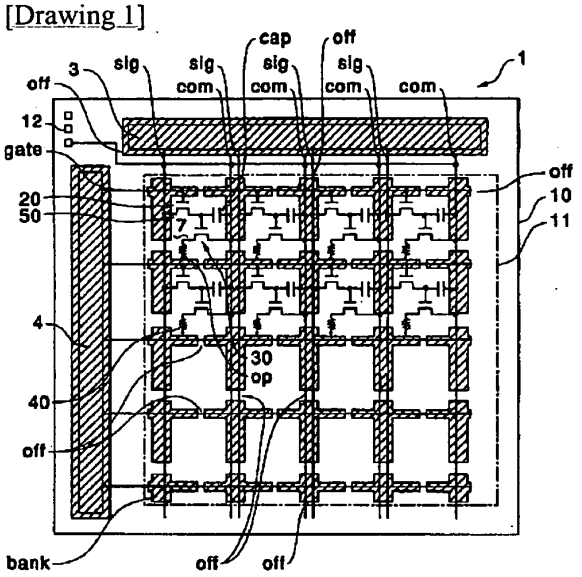
* NOTICES *

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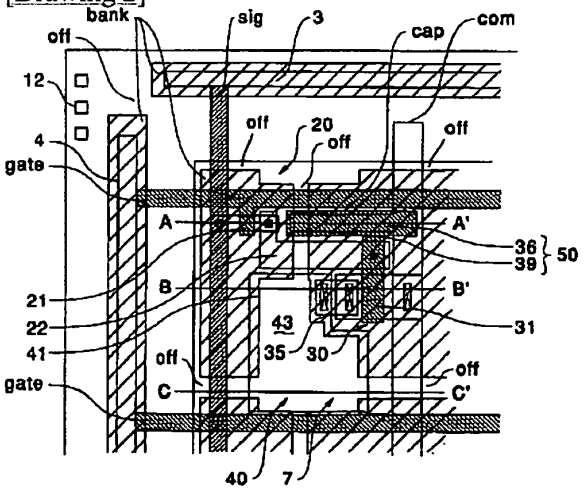
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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

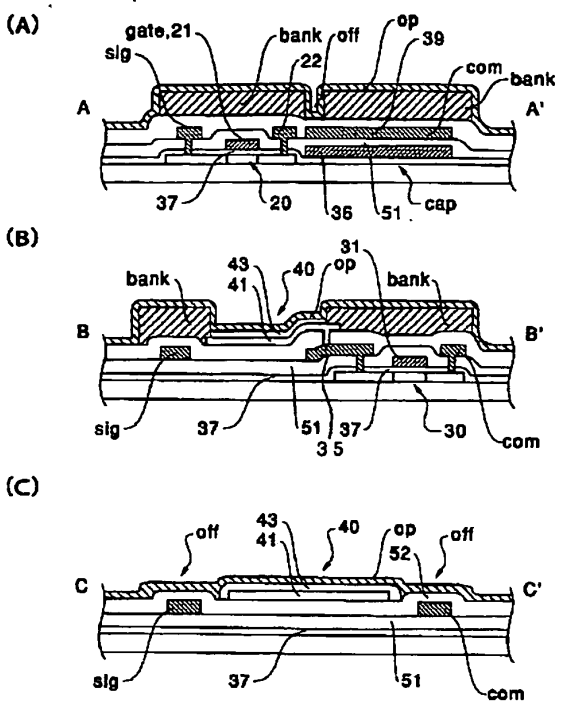
[Drawing 1]



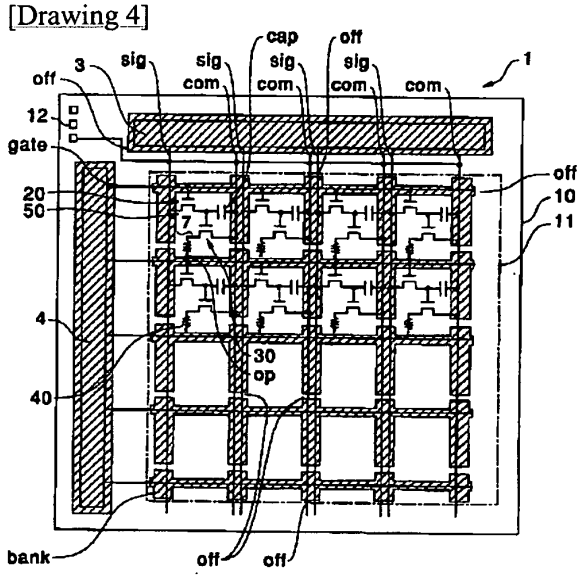
[Drawing 2]



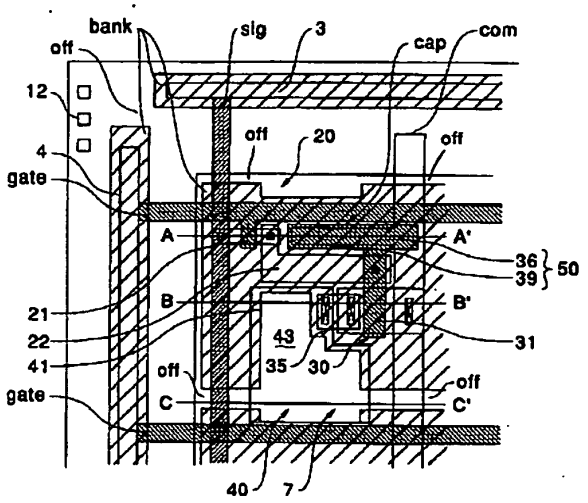
[Drawing 3]



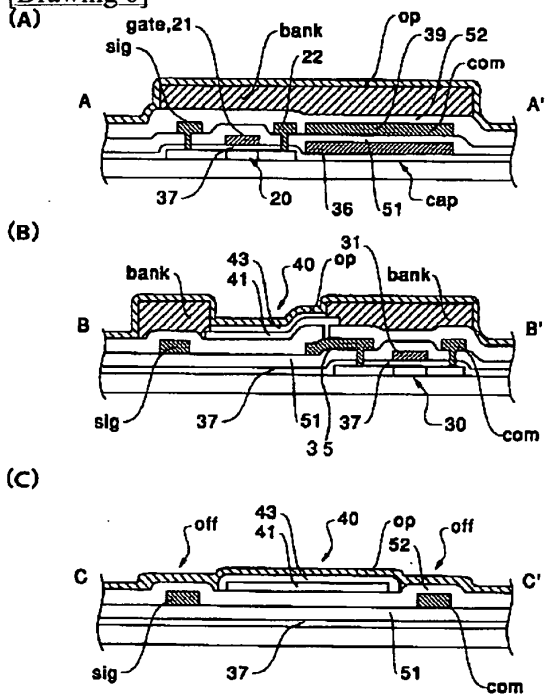
[Drawing 4]



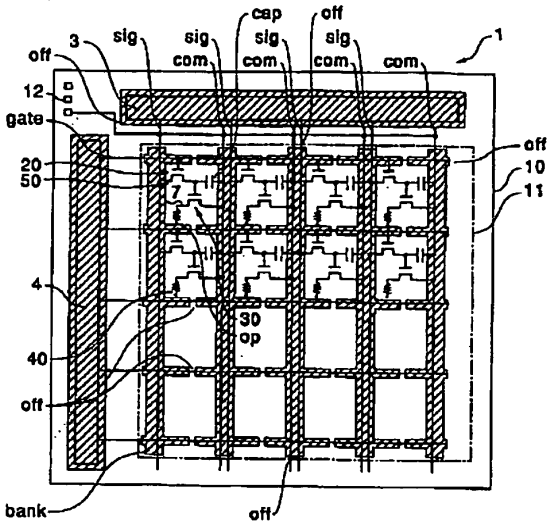
[Drawing 5]



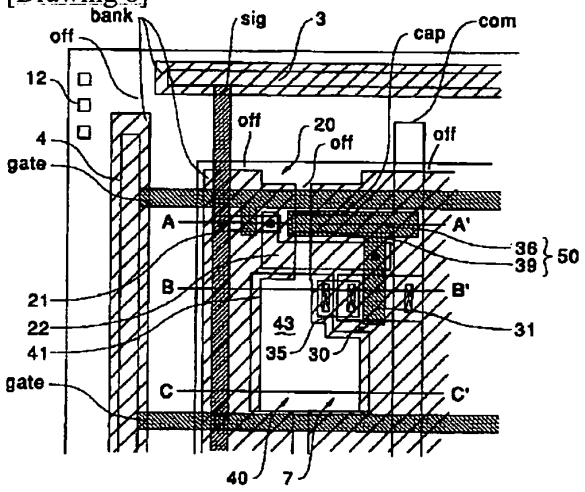
[Drawing 6]



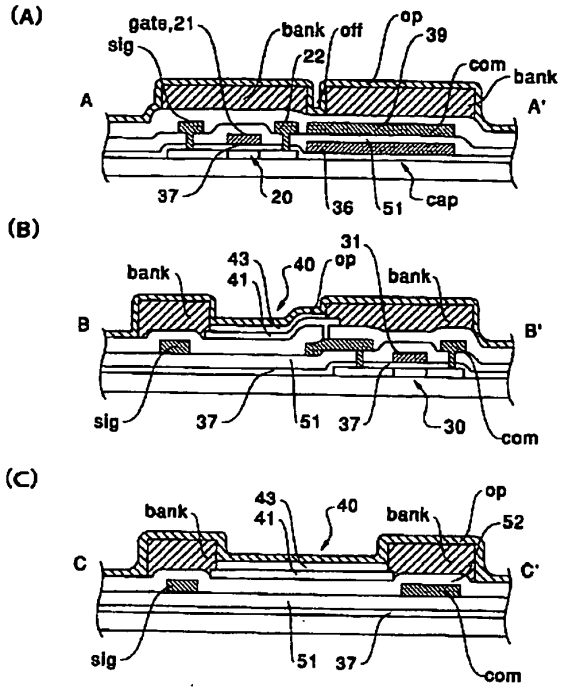
[Drawing 7]



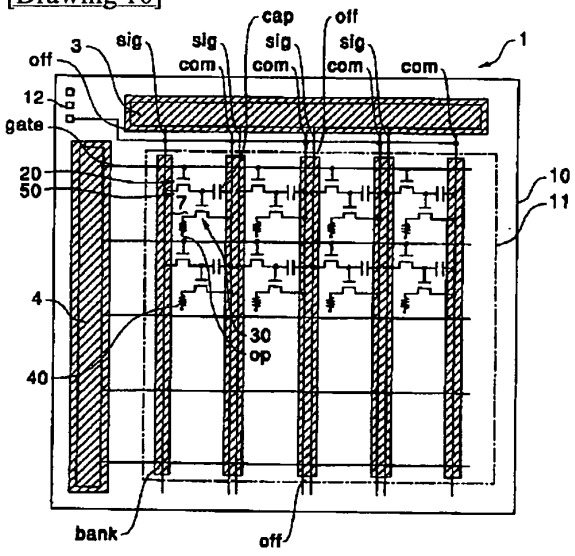
[Drawing 8]



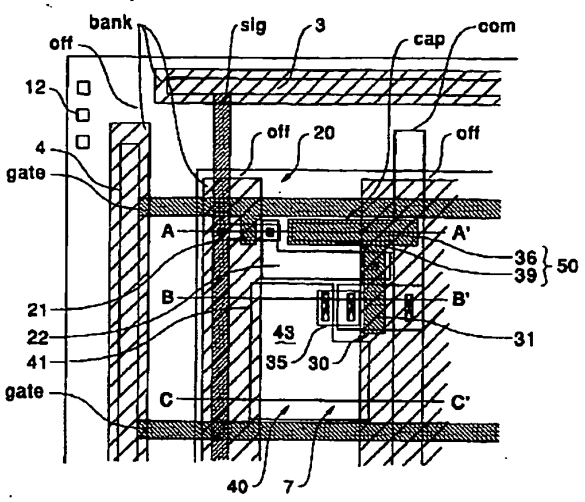
[Drawing 9]



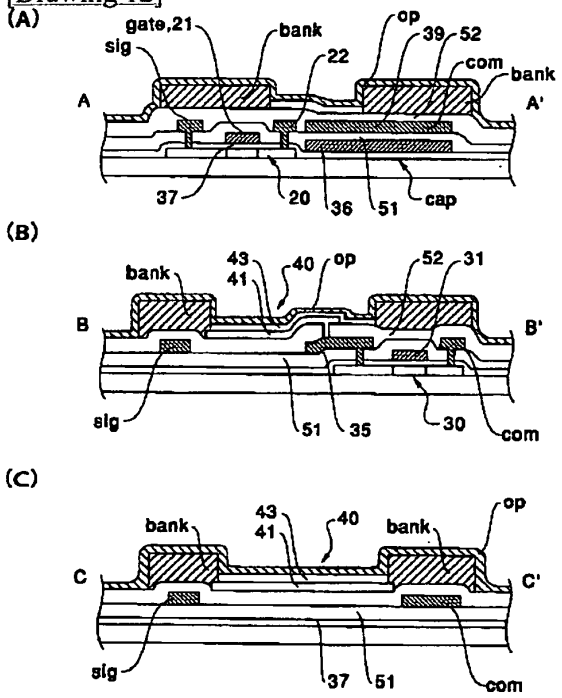
[Drawing 10]



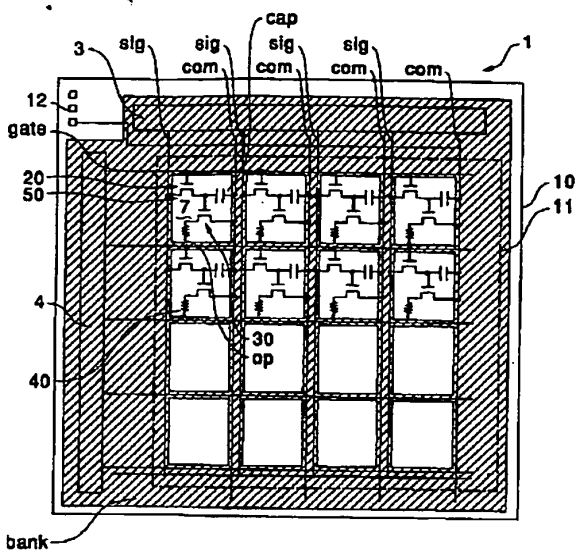
[Drawing 11]



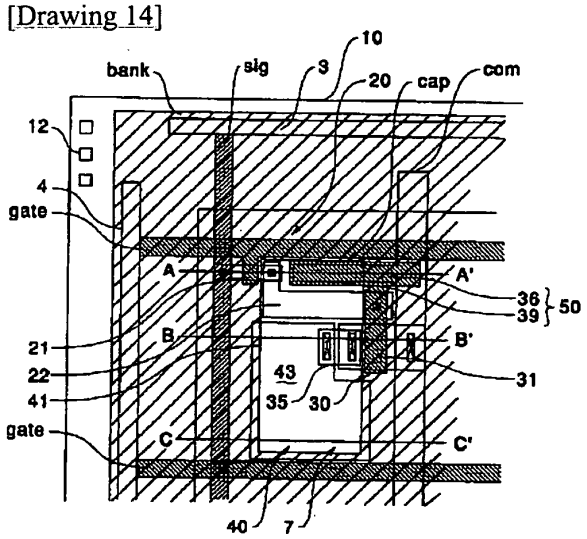
[Drawing 12]



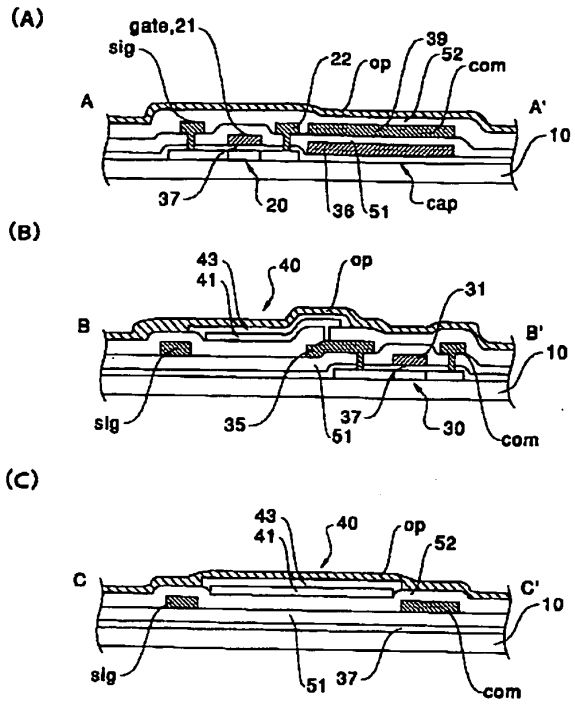
[Drawing 13]



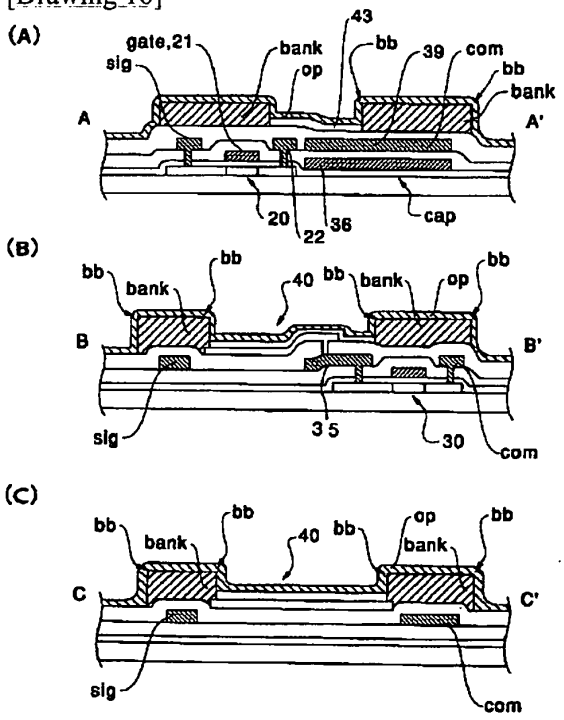
[Drawing 14]



[Drawing 15]



[Drawing 16]



[Translation done.]

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	9/30	３６５		9/30	３６５Ｄ
Ｈ０５Ｂ	33/22		Ｈ０５Ｂ	33/22	Ｚ
	33/26			33/26	Ｚ

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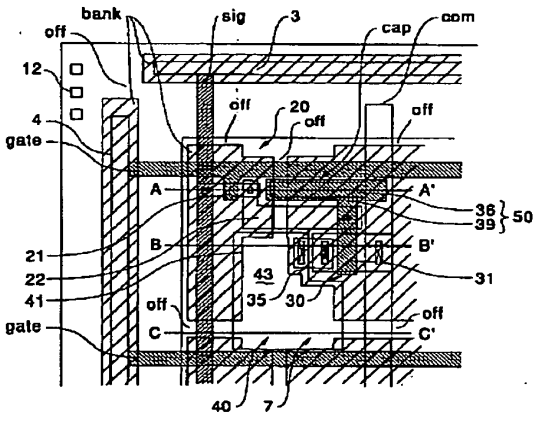
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(54)【発明の名称】　アクティブマトリクス型表示装置

(57)【要約】

【課題】　有機半導体膜の周りに厚い絶縁膜を形成して寄生容量などを抑え、かつ、絶縁膜の上層に形成する対向電極に断線などが発生しないアクティブマトリクス型表示装置を提供すること。

【解決手段】　アクティブマトリクス型表示装置１では、データ線ｓｉｇに寄生する容量を抑えるために、データ線ｓｉｇおよび走査線ｇａｔｅに沿ってレジスト膜からなるバンク層ｂａｎｋを設け、このバンク層ｂａｎｋの上層側に薄膜発光素子４０の対向電極ｏｐを積層する。バンク層ｂａｎｋには途切れ部分ｏｆｆが形成され、そこはバンク層ｂａｎｋに起因する大きな段差のない平坦部分であるので、この部分では対向電極ｏｐの断線がない。有機半導体膜４３をインクジェット法で形成する際にはインクジェットヘッドから吐出した液状の材料をバンク層ｂａｎｋでせき止める。



【特許請求の範囲】
【請求項１】　基板上に、複数の走査線と、該走査線に交差する複数のデータ線と、該データ線と前記走査線とによってマトリクス状に形成された複数の画素からなる表示部とを有し、該画素の各々は、前記走査線を介して走査信号がゲート電極に供給される薄膜トランジスタを含む導通制御回路と、画素毎に形成された画素電極、該画素電極の上層側に積層された発光薄膜、および該発光薄膜の上層側に形成された対向電極を具備する薄膜発光素子とを備え、前記データ線から前記導通制御回路を介して供給される画像信号に基づいて前記発光薄膜が発光するアクティブマトリクス型表示装置において、
前記発光薄膜の形成領域は、前記対向電極の下層側に前記発光薄膜よりも厚く形成された絶縁膜で区画されているとともに、
該絶縁膜は、各画素毎の対向電極部分同士を当該絶縁膜に起因する段差のない平坦部分を介して接続させる途切れ部分を備えていることを特徴とするアクティブマトリクス型表示装置。
【請求項２】　請求項１において、前記導通制御回路は、前記走査信号がゲート電極に供給される第１の薄膜トランジスタ、および該第１の薄膜トランジスタを介してゲート電極が前記データ線に接続する第２の薄膜トランジスタを備え、
該第２の薄膜トランジスタと前記薄膜発光素子は、前記データ線および走査線とは別に構成された駆動電流供給用の共通給電線と前記対向電極との間に直列に接続していることを特徴とするアクティブマトリクス型表示装置。
【請求項３】　請求項１または２において、前記絶縁膜は、当該絶縁膜で区画された領域内に前記発光薄膜をインクジェット法により形成する際に吐出液のはみ出しを防止するバンク層であることを特徴とするアクティブマトリクス型表示装置。
【請求項４】　請求項３において、前記絶縁膜は、膜厚が１μｍ以上であることを特徴とするアクティブマトリクス型表示装置。
【請求項５】　請求項１ないし４のいずれかにおいて、前記絶縁膜は、前記データ線および前記走査線に沿って前記発光薄膜の形成領域の周りを囲むように形成されてなり、前記データ線および前記走査線の各延設方向で隣り合う画素の間に相当する部分に前記途切れ部分を備えていることを特徴とするアクティブマトリクス型表示装置。
【請求項６】　請求項１ないし４のいずれかにおいて、前記絶縁膜は、前記データ線および前記走査線に沿って形成されていることにより前記発光薄膜の形成領域の周りを囲んでいるとともに、前記走査線の延設方向で隣り合う画素の間に相当する部分に前記途切れ部分を備えていることを特徴とするアクティブマトリクス型表示装置。
【請求項７】　請求項１ないし４のいずれかにおいて、前記絶縁膜は、前記データ線および前記走査線に沿って形成されていることにより前記発光薄膜の形成領域の周りを囲んでいるとともに、前記データ線の延設方向で隣り合う画素の間に相当する部分に前記途切れ部分を備えていることを特徴とするアクティブマトリクス型表示装置。
【請求項８】　請求項１ないし４のいずれかにおいて、前記絶縁膜は、前記データ線に沿ってストライプ状に形成され、該形成方向の少なくとも一方の端部に前記途切れ部分を備えていることを特徴とするアクティブマトリクス型表示装置。
【請求項９】　請求項５ないし８のいずれかにおいて、前記画素電極の形成領域のうち、前記導通制御回路の形成領域と重なる領域は前記絶縁膜で覆われていることを特徴とするアクティブマトリクス型表示装置。
【請求項１０】　請求項１ないし９のいずれかにおいて、前記表示部の周囲には、前記データ線を介してデータ信号を供給するデータ線駆動回路、および前記走査線を介して走査信号を供給する走査線駆動回路を有し、該走査線駆動回路および前記データ線側駆動回路の上層側にも前記絶縁膜が形成されているとともに、当該絶縁膜は、前記走査線駆動回路の形成領域と前記データ側駆動回路の形成領域との間に相当する位置には前記対向電極を前記表示部側と基板外周側とを当該絶縁膜に起因する段差のない平坦部分を介して接続させる途切れ部分を備えていることを特徴とするアクティブマトリクス型表示装置。
【請求項１１】　請求項１ないし１０のいずれかにおいて、前記絶縁膜は、有機材料からなることを特徴とするアクティブマトリクス型表示装置。
【請求項１２】　請求項１ないし１０のいずれかにおいて、前記絶縁膜は、無機材料からなることを特徴とするアクティブマトリクス型表示装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、有機半導体膜等の発光薄膜に駆動電流が流れることによって発光するＥＬ（エレクトロルミネッセンス）素子またはＬＥＤ（発光ダイオード）素子などの薄膜発光素子を薄膜トランジスタ（以下、ＴＦＴという。）で駆動制御するアクティブマトリクス型表示装置に関するものである。
【０００２】
【従来の技術】ＥＬ素子またはＬＥＤ素子などの電流制御型発光素子を用いたアクティブマトリクス型の表示装置が提案されている。このタイプの表示装置に用いられる発光素子はいずれも自己発光するため、液晶表示装置と違ってバックライトを必要とせず、また、視野角依存性が少ないなどの利点もある。

【０００３】図１３は、このような電荷注入型の有機薄膜ＥＬ素子を用いたアクティブマトリクス型表示装置のブロック図を示してある。この図に示すアクティブマトリクス型表示装置１Ａでは、透明基板１０上に、複数の走査線ｇａｔｅと、該走査線ｇａｔｅの延設方向に対して交差する方向に延設された複数のデータ線ｓｉｇと、該データ線ｓｉｇに並列する複数の共通給電線ｃｏｍと、データ線ｓｉｇと走査線ｇａｔｅとによってマトリクス状に形成された複数の画素７とが構成されている。データ線ｓｉｇおよび走査線ｇａｔｅに対してはデータ線駆動回路３および走査線駆動回路４が構成されている。各々の画素７には、走査線ｇａｔｅを介して走査信号が供給される導通制御回路５０と、この導通制御回路５０を介してデータ線ｓｉｇから供給される画像信号に基づいて発光する薄膜発光素子４０とが構成されている。ここに示す例において、導通制御回路５０は、走査線ｇａｔｅを介して走査信号がゲート電極に供給される第１のＴＦＴ２０と、この第１のＴＦＴ２０を介してデータ線ｓｉｇから供給される画像信号を保持する保持容量ｃａｐと、この保持容量ｃａｐによって保持された画像信号がゲート電極に供給される第２のＴＦＴ３０とから構成されている。第２のＴＦＴ３０と薄膜発光素子４０とは、詳しくは後述する対向電極ｏｐと共通給電線ｃｏｍとの間に直列に接続している。この薄膜発光素子４０は、第２のＴＦＴ３０がオン状態になったときには共通給電線ｃｏｍから駆動電流が流れ込んで発光するとともに、この発光状態は保持容量ｃａｐによって所定の期間、保持される。

【０００４】このような構成のアクティブマトリクス型表示装置１Ａでは、図１４および図１５（Ａ）、（Ｂ）に示すように、いずれの画素７においても、島状の半導体膜を利用して第１のＴＦＴ２０および第２のＴＦＴ３０が形成されている。第１のＴＦＴ２０は、ゲート電極２１が走査線ｇａｔｅの一部として構成されている。第１のＴＦＴ２０は、ソース・ドレイン領域の一方に第１層間絶縁膜５１のコンタクトホールを介してデータ線ｓｉｇが電気的に接続し、他方にはドレイン電極２２が電気的に接続している。ドレイン電極２２は、第２のＴＦＴ３０の形成領域に向けて延設されており、この延設部分には第２のＴＦＴ３０のゲート電極３１が第１の層間絶縁膜５１のコンタクトホールを介して電気的に接続している。第２のＴＦＴ３０のソース・ドレイン領域の一方には、第１の層間絶縁膜５１のコンタクトホールを介して中継電極３５が電気的に接続し、この中継電極３５には第２の層間絶縁膜５２のコンタクトホールを介して薄膜発光素子４０の画素電極４１が電気的に接続している。

【０００５】画素電極４１は、図１４および図１５（Ｂ）、（Ｃ）からわかるように各画素７毎に独立して形成されている。画素電極４１の上層側には、有機半導体膜４３および対向電極ｏｐがこの順に積層されている。有機半導体膜４３は画素７毎に形成されているが、複数の画素７に跨がってストライプ状に形成される場合もある。図１３からわかるように、対向電極ｏｐは、画素７が構成されている表示部１１だけでなく、透明基板１０の略全面に形成されている。

【０００６】再び、図１４および図１５（Ａ）において、第２のＴＦＴ３０のソース・ドレイン領域のもう一方には、第１の層間絶縁膜５１のコンタクトホールを介して共通給電線ｃｏｍが電気的に接続している。共通給電線ｃｏｍの延設部分３９は、第２のＴＦＴ３０のゲート電極３１の延設部分３６に対して、第１の層間絶縁膜５１を誘電体膜として挟んで対向し、保持容量ｃａｐを構成している。

【０００７】

【発明が解決しようとする課題】しかしながら、前記のアクティブマトリクス型表示装置１Ａにおいて、画素電極４１に対向する対向電極ｏｐは、液晶アクティブマトリクス型表示装置と相違して、同じ透明基板１０上においてデータ線ｓｉｇとの間に第２の層間絶縁膜５２しか有しないので、データ線ｓｉｇには大きな容量が寄生し、データ線駆動回路３の負荷が大きい。

【０００８】そこで、本願発明者は、図１３、図１４、および図１６（Ａ）、（Ｂ）、（Ｃ）に示すように、対向電極ｏｐとデータ線ｓｉｇなどとの間に厚い絶縁膜（バンク層ｂａｎｋ／左下がりの斜線を広いピッチで付した領域）を設け、データ線ｓｉｇに寄生する容量を低減することを提案する。併せて、この絶縁膜（バンク層ｂａｎｋ）で有機半導体膜４３の形成領域を囲むことによって、インクジェットヘッドから吐出した液状の材料（吐出液）から有機半導体膜４３を形成する際に吐出液をバンク層ｂａｎｋでせき止め、吐出液が側方にはみ出すことを防止することを提案する。しかし、かかる構造を採用すると、厚いバンク層ｂａｎｋの存在に起因して大きな段差ｂｂが形成され、このバンク層ｂａｎｋの上層に形成される対向電極ｏｐが前記の段差ｂｂの部分で断線しやすい。このような段差ｂｂで対向電極ｏｐに断線が生じると、この部分の対向電極ｏｐは周囲の対向電極ｏｐから絶縁状態になって表示の点欠陥あるいは線欠陥を発生させる。また、データ側駆動回路３や走査側駆動回路４の表面を覆うバンク層ｂａｎｋの外周縁に沿って対向電極ｏｐに断線が起こると、表示部１１の対向電極ｏｐと端子１２との間が完全に絶縁状態になって表示が全くできなくなる。

【０００９】そこで、本発明の課題は、有機半導体膜の周りに厚い絶縁膜を形成して寄生容量などを抑え、この厚い絶縁膜の上層に形成する対向電極に断線などが発生しないアクティブマトリクス型表示装置を提供することにある。

【００１０】

【課題を解決するための手段】上記課題を解決するため、本発明では、基板上に、複数の走査線と、該走査線に交差する複数のデータ線と、該データ線と前記走査線とによってマトリクス状に形成された複数の画素からなる表示部とを有し、該画素の各々は、前記走査線を介して走査信号がゲート電極に供給されるＴＦＴを含む導通制御回路と、画素毎に形成された画素電極、該画素電極の上層側に積層された発光薄膜、および該発光薄膜の上層側に形成された対向電極を具備する薄膜発光素子とを備え、前記データ線から前記導通制御回路を介して供給される画像信号に基づいて前記薄膜発光素子が発光するアクティブマトリクス型表示装置において、前記有機半導体膜の形成領域は、前記対向電極の下層側に前記有機半導体膜よりも厚く形成された絶縁膜で区画されているとともに、該絶縁膜は、各画素毎の対向電極部分同士を当該絶縁膜に起因する段差のない平坦部分を介して接続させる途切れ部分を備えていることを特徴とする。

【００１１】本発明において、対向電極表示部に形成され、データ線と対向する状態にあるため、このままではデータ線に対して大きな容量が寄生することになる。しかるに本発明では、データ線と対向電極との間に厚い絶縁膜を介在させたので、データ線に容量が寄生することを防止できる。その結果、データ線駆動回路の負荷を低減できるので、低消費電力化あるいは表示動作の高速化を図ることができる。また、厚い絶縁膜を形成すると、この絶縁膜は大きな段差を形成し、その上層側に形成される対向電極に断線が発生させるおそれがあるが、本発明では、厚い絶縁膜の所定の位置に途切れ部分を構成し、この部分を平坦にしてある。従って、各領域毎の対向電極は平坦部分に形成された部分を介して電気的に接続するので、たとえ、絶縁膜に起因する段差によってこの部分で断線しても、絶縁膜の途切れ部分に相当する平坦部分を介して確実に電気的に接続しているので、対向基板の断線という不具合が発生しない。それ故、アクティブマトリクス型表示装置において、有機半導体膜の周りに厚い絶縁膜を形成して寄生容量などを抑えたとしても、絶縁膜の上層に形成する対向電極に断線が発生しないので、アクティブマトリクス型表示装置の表示品質および信頼性を向上することができる。

【００１２】本発明では、前記導通制御回路は、前記走査信号がゲート電極に供給される第１のＴＦＴ、および該第１のＴＦＴを介してゲート電極が前記データ線に接続する第２のＴＦＴを備え、該第２のＴＦＴと前記薄膜発光素子は、前記データ線および走査線とは別に構成された駆動電流供給用の共通給電線と前記対向電極との間に直列に接続していることが好ましい。すなわち、導通制御回路を１つのＴＦＴと保持容量で構成することも可能ではあるが、表示品位を高くするという観点からすれば各画素の導通制御回路を２つのＴＦＴと保持容量で構成することが好ましい。

【００１３】本発明において、前記絶縁膜は、当該絶縁膜で区画された領域内に前記発光薄膜をインクジェット法により形成する際に吐出液のはみ出しを防止するバンク層として利用することが好ましい。それには、前記絶縁膜は、膜厚が１μｍ以上であることが好ましい。

【００１４】本発明においては、前記絶縁膜は、前記データ線および前記走査線に沿って前記発光薄膜の形成領域の周りを囲んでいる場合には、前記データ線の延設方向で隣り合う画素の間、前記走査線の延設方向で隣り合う画素の間、またはそれら双方の方向で隣り合う画素の間に相当する部分に前記途切れ部分を構成する。

【００１５】上記の形態と違って、前記絶縁膜は前記データ線に沿ってストライプ状に延設される場合があり、この場合には、該延設方向の少なくとも一方の端部に前記途切れ部分を構成してもよい。

【００１６】本発明において、前記画素電極の形成領域のうち、前記導通制御回路の形成領域と重なる領域は前記絶縁膜で覆われていることが好ましい。すなわち、前記画素電極の形成領域のうち、前記導通制御回路の形成されていない平坦部分のみで前記の厚い絶縁膜を開口し、この内側のみに有機半導体膜を形成することが好ましい。このように構成すると、有機半導体膜の膜厚ばらつきに起因する表示むらを防止できる。また、画素電極が形成されていても導通制御回路と重なる領域では、たとえ対向電極との間に駆動電流が流れて有機半導体膜が発光しても、この光は導通制御回路に遮られ、表示には寄与しない。かかる表示に寄与しない部分で有機半導体膜に流れる駆動電流は、表示という面からみて無効電流といえる。そこで、本発明では、従来ならこのような無効電流が流れるはずの部分に前記の厚い絶縁膜を形成し、そこに駆動電流が流れることを防止する。その結果、共通給電線に流れる電流が小さくすることができるので、その分、共通給電線の幅を狭くすれば、その結果として、発光面積を増すことができ、輝度、コントラスト比などの表示性能を向上させることができる。

【００１７】本発明では、前記表示部の周囲には、前記データ線を介してデータ信号を供給するデータ線駆動回路、および前記走査線を介して走査信号を供給する走査線駆動回路を有し、該走査線駆動回路および前記データ線駆動回路の上層側にも前記絶縁膜が形成されているとともに、当該絶縁膜は、前記走査線駆動回路の形成領域と前記データ線駆動回路の形成領域との間に相当する位置には前記対向電極を前記表示部側と基板外周側とを当該絶縁膜に起因する段差のない平坦部分を介して接続させる途切れ部分を備えていることが好ましい。このように構成すると、データ線駆動回路や走査線駆動回路の表面を覆う絶縁膜の外周縁に沿って対向電極に断線が起きても、表示部側の対向電極と基板外周側の対向電極とは該絶縁膜に起因する段差のない平坦部分を介して接続し、表示部側の対向電極と基板外周側の対向電極との間

の電気的接続を確保できる。

【００１８】本発明において、前記絶縁膜をレジスト膜などの有機材料から構成した場合には厚い膜を容易に形成できる。これに対して、前記絶縁膜を無機材料から構成した場合には、発光薄膜と接触した状態にあっても、発光薄膜の変質を防止することができる。

【００１９】

【発明の実施の形態】図面を参照して、本発明の実施の形態を説明する。なお、以下の説明において、図１３ないし図１６を説明した要素と共通する部分には同一の符号を付してある。

【００２０】［実施の形態１］

（全体構成）図１は、アクティブマトリクス型表示装置の全体のレイアウトを模式的に示すブロック図である。図２は、それに構成されている画素の１つを抜き出して示す平面図、図３（Ａ）、（Ｂ）、（Ｃ）はそれぞれ図２のＡ－Ａ′断面図、Ｂ－Ｂ′断面図、およびＣ－Ｃ′断面図である。

【００２１】図１に示すアクティブマトリクス型表示装置１では、その基体たる透明基板１０の中央部分が表示部１１とされている。透明基板１０の外周部分のうち、データ線ｓｉｇの端部には画像信号を出力するデータ側駆動回路３が構成され、走査線ｇａｔｅの端部には走査信号を出力する走査側駆動回路４が構成されている。これらの駆動回路３、４では、Ｎ型のＴＦＴとＰ型のＴＦＴとによって相補型ＴＦＴが構成され、この相補型ＴＦＴは、シフトレジスタ回路、レベルシフタ回路、アナログスイッチ回路などを構成している。表示部１１では、液晶アクティブマトリクス型表示装置のアクティブマトリクス基板と同様、透明基板１０上に、複数の走査線ｇａｔｅと、該走査線ｇａｔｅの延設方向に対して交差する方向に延設された複数のデータ線ｓｉｇと、データ線ｓｉｇと走査線ｇａｔｅとによってマトリクス状に形成された複数の画素７とが構成されている。

【００２２】各々の画素７には、走査線ｇａｔｅを介して走査信号が供給される導通制御回路５０と、この導通制御回路５０を介してデータ線ｓｉｇから供給される画像信号に基づいて発光する薄膜発光素子４０とが構成されている。ここに示す例においては、導通制御回路５０は、走査線ｇａｔｅを介して走査信号がゲート電極に供給される第１のＴＦＴ２０と、この第１のＴＦＴ２０を介してデータ線ｓｉｇから供給される画像信号を保持する保持容量ｃａｐと、この保持容量ｃａｐによって保持された画像信号がゲート電極に供給される第２のＴＦＴ３０とから構成されている。第２のＴＦＴ３０と薄膜発光素子４０とは、詳しくは後述する対向電極ｏｐと共通給電線ｃｏｍとの間に直列に接続している。

【００２３】このような構成のアクティブマトリクス型表示装置１では、図２および図３（（Ａ）、（Ｂ）に示すように、いずれの画素７においても、島状の半導体膜（シリコン膜）を利用して第１のＴＦＴ２０および第２のＴＦＴ３０が形成されている。

【００２４】第１のＴＦＴ２０は、ゲート電極２１が走査線ｇａｔｅの一部として構成されている。第１のＴＦＴ２０は、ソース・ドレイン領域の一方に第１層間絶縁膜５１のコンタクトホールを介してデータ線ｓｉｇが電気的に接続し、他方にはドレイン電極２２が電気的に接続している。ドレイン電極２２は、第２のＴＦＴ３０の形成領域に向けて延設されており、この延設部分には第２のＴＦＴ３０のゲート電極３１が第１の層間絶縁膜５１のコンタクトホールを介して電気的に接続している。

【００２５】第２のＴＦＴ３０のソース・ドレイン領域の一方には、第１の層間絶縁膜５１のコンタクトホールを介して、データ線ｓｉｇと同時形成された中継電極３５が電気的に接続し、この中継電極３５には第２の層間絶縁膜５２のコンタクトホールを介して薄膜発光素子４０のＩＴＯ膜からなる透明な画素電極４１が電気的に接続している。

【００２６】図２および図３（Ｂ）、（Ｃ）からわかるように、画素電極４１は各画素７毎に独立して形成されている。画素電極４１の上層側には、発光薄膜としてポリフェニレンビニレン（ＰＰＶ）などのからなる有機半導体膜４３、およびリチウム含有アルミニウム、カルシウムなどの金属膜からなる対向電極ｏｐがこの順に積層され、薄膜発光素子４０が構成されている。有機半導体膜４３は各画素７に形成されているが、複数の画素７に跨がってストライプ状に形成される場合もある。対向電極ｏｐは、表示部１１全体と、透明基板１０の端子１２が形成されている部分の周囲を除いた領域とに形成されている。この端子１２は、対向電極ｏｐと同時形成された配線（図示せず。）に接続する対向電極ｏｐの端子を含んでいる。

【００２７】なお、薄膜発光素子４０としては、正孔注入層を設けて発光効率（正孔注入率）を高めた構造、電子注入層を設けて発光効率（電子注入率）を高めた構造、正孔注入層および電子注入層の双方を形成した構造を採用することもできる。

【００２８】再び、図２および図３（Ａ）において、第２のＴＦＴ３０のソース・ドレイン領域のもう一方には、第１の層間絶縁膜５１のコンタクトホールを介して共通給電線ｃｏｍが電気的に接続している。共通給電線ｃｏｍの延設部分３９は、第２のＴＦＴ３０のゲート電極３１の延設部分３６に対して、第１の層間絶縁膜５１を誘電体膜として挟んで対向し、保持容量ｃａｐを構成している。

【００２９】このようにアクティブマトリクス型表示装置１において、走査信号によって選択されて第１のＴＦＴ２０がオン状態になると、データ線ｓｉｇからの画像信号が第１のＴＦＴ２０を介して第２のＴＦＴ３０のゲート電極３１に印加されるとともに、画像信号が第１の

ＴＦＴ２０を介して保持容量ｃａｐに書き込まれる。その結果、第２のＴＦＴ３０がオン状態になると、対向電極ｏｐおよび画素電極４１をそれぞれ負極および正極として電圧が印加され、印加電圧がしきい値電圧を越えた領域で有機半導体膜４３に流れる電流（駆動電流）が急激に増大する。従って、発光素子４０は、エレクトロルミネッセンス素子あるいはＬＥＤ素子として発光し、発光素子４０の光は、対向電極ｏｐに反射されて透明な画素電極４１および透明基板１０を透過して出射される。このような発光を行うための駆動電流は、対向電極ｏｐ、有機半導体膜４３、画素電極４１、第２のＴＦＴ３０、および共通給電線ｃｏｍから構成される電流経路を流れるため、第２のＴＦＴ３０がオフ状態になると、流れなくなる。但し、第２のＴＦＴ３０のゲート電極は、第１のＴＦＴ２０がオフ状態になっても、保持容量ｃａｐによって画像信号に相当する電位に保持されるので、第２のＴＦＴ３０はオン状態のままである。それ故、発光素子４０には駆動電流が流れ続け、この画素は点灯状態のままである。この状態は、新たな画像データが保持容量ｃａｐに書き込まれて、第２のＴＦＴ３０がオフ状態になるまで維持される。

【００３０】（バンク層の構造）このように構成したアクティブマトリクス型表示装置１において、本形態では、データ線ｓｉｇには大きな容量が寄生することを防止するため、図１、図２、および図３（Ａ）、（Ｂ）、（Ｃ）に示すように、データ線ｓｉｇおよび走査線ｇａｔｅに沿って、レジスト膜、あるいはポリイミド膜からなる厚い絶縁膜（バンク層ｂａｎｋ／左下がりの斜線を広いピッチで付した領域）を設け、このバンク層ｂａｎｋの上層側に対向電極ｏｐを形成してある。このため、データ線ｓｉｇと対向電極ｏｐとの間には、第２の層間絶縁膜５２と厚いバンク層ｂａｎｋが介在しているので、データ線ｓｉｇに寄生する容量が極めて小さい。それ故、駆動回路３、４の負荷を低減でき、低消費電力化あるいは表示動作の高速化を図ることができる。

【００３１】また、図１に示すように、透明基板１０の周辺領域（表示部１１の外側領域）にもバンク層ｂａｎｋ（形成領域に斜線を付してある。）を形成する。従って、データ側駆動回路３および走査側駆動回路４はいずれも、バンク層ｂａｎｋによって覆われている。対向電極ｏｐは、少なくとも表示部１１に形成される必要があり、駆動回路領域に形成する必要はない。しかし、対向電極ｏｐは、通常、マスクスパッタ法で形成されるため、合わせ精度が悪く、対向電極ｏｐと駆動回路とが重なることがある。しかるに本形態では、これらの駆動回路の形成領域に対して対向電極ｏｐが重なる状態にあっても、駆動回路の配線層と対向電極ｏｐとの間にバンク層ｂａｎｋが介在することになる。それ故、駆動回路３、４に容量が寄生することを防止できるため、駆動回路３、４の負荷を低減でき、低消費電力化あるいは表示動作の高速化を図ることができる。

【００３２】さらに、本形態では、画素電極４１の形成領域のうち、導通制御回路５０の中継電極３５と重なる領域にもバンク層ｂａｎｋが形成されている。このため、中継電極３５と重なる領域には有機半導体膜４３が形成されない。すなわち、画素電極４１の形成領域のうち、平坦な部分のみに有機半導体膜４３が形成されるので、有機半導体膜４３は一定の膜厚で形成され、表示むらを起こさない。また、中継電極３５と重なる領域にバンク層ｂａｎｋがないと、この部分でも対向電極ｏｐとの間に駆動電流が流れて有機半導体膜４３が発光する。しかし、この光は中継電極３５と対向電極ｏｐとの間に挟まれて外に出射されず、表示に寄与しない。かかる表示に寄与しない部分で流れる駆動電流は、表示という面からみて無効電流といえる。しかるに本形態では、従来ならこのような無効電流が流れるはずの部分にバンク層ｂａｎｋを形成し、そこに駆動電流が流れることを防止するので、共通給電線ｃｏｍに無駄な電流が流れることが防止できる。それ故、共通給電線ｃｏｍの幅はその分、狭くてよい。その結果として、発光面積を増すことができ、輝度、コントラスト比などの表示性能を向上させることができる。

【００３３】さらにまた、本形態では、データ線ｓｉｇおよび走査線ｇａｔｅに沿ってバンク層ｂａｎｋを形成してあるため、いずれの画素７も厚いバンク層ｂａｎｋで囲まれている。このため、このままでは、各画素７の対向電極ｏｐはバンク層ｂａｎｋを乗り越えて隣接する画素７の対向電極ｏｐと接続することになる。しかるに本形態では、バンク層ｂａｎｋには、データ線ｓｉｇの延設方向で隣り合う画素７の間に相当する部分に途切れ部分ｏｆｆが形成されている。また、バンク層ｂａｎｋには、走査線ｇａｔｅの延設方向で隣り合う画素７の間に相当する部分にも途切れ部分ｏｆｆが形成されている。さらに、バンク層ｂａｎｋには、データ線ｓｉｇおよび走査線ｇａｔｅの各延設方向の端部のそれぞれに途切れ部分ｏｆｆが形成されている。

【００３４】このような途切れ部分ｏｆｆは厚いバンク層ｂａｎｋがないので、バンク層ｂａｎｋに起因する大きな段差のない平坦部分であり、この部分に形成されている対向電極ｏｐは断線することがない。従って、各画素７の対向電極７は、バンク層ｂａｎｋに起因する段差のない平坦部分を介して確実に接続していることになる。それ故、画素７の周りに厚い絶縁膜（バンク層ｂａｎｋ）を形成して寄生容量などを抑えても、この厚い絶縁膜（バンク層ｂａｎｋ）の上層に形成する対向電極ｏｐに断線が発生しない。

【００３５】しかも、走査側駆動回路４およびデータ側駆動回路３の上層側に形成されたバンク層ｂａｎｋは、走査側駆動回路４の形成領域とデータ側駆動回路３の形成領域との間に相当する位置に途切れ部分ｏｆｆが形成

されている。このため、表示部１１の側の対向電極ｏｐと基板外周側の対向電極ｏｐとは、バンク層ｂａｎｋの途切れ部分ｏｆｆを介して接続し、この途切れ部分ｏｆｆもバンク層ｂａｎｋに起因する段差のない平坦部分である。従って、この途切れ部分ｏｆｆに形成されている対向電極ｏｐは断線することがないので、表示部１１の側の対向電極ｏｐと基板外周側の対向電極ｏｐとは、バンク層ｂａｎｋの途切れ部分ｏｆｆを介して確実に接続し、この基板外周側の対向電極ｏｐに配線接続されている端子１２と表示部１１の対向電極ｏｐとは確実に接続している。

【００３６】なお、バンク層ｂａｎｋを黒色のレジストによって形成すると、バンク層ｂａｎｋはブラックマトリクスとして機能し、コントラスト比などの表示の品位が向上する。すなわち、本形態に係るアクティブマトリクス型表示装置１では、対向電極ｏｐが透明基板１０の表面側において画素７の全面に形成されるため、対向電極ｏｐでの反射光がコントラスト比を低下させる。しかるに寄生容量を防止する機能を担うバンク層ｂａｎｋを黒色のレジストで構成すると、バンク層ｂａｎｋはブラックマトリクスとしても機能し、対向電極ｏｐからの反射光を遮るので、コントラスト比が向上する。

【００３７】（アクティブマトリクス型表示装置の製造方法）このように形成したバンク層ｂａｎｋは、有機半導体膜４３の形成領域を囲むように構成されているので、アクティブマトリクス型表示装置の製造工程では、インクジェットヘッドから吐出した液状の材料（吐出液）から有機半導体膜４３を形成する際に吐出液をせき止め、吐出液が側方にはみ出すことを防止する。なお、以下に説明するアクティブマトリクス型表示装置１の製造方法において、透明基板１０上に第１のＴＦＴ２０および第２のＴＦＴ３０を製造するまでの工程は、液晶アクティブマトリクス型表示装置１のアクティブマトリクス基板を製造する工程と略同様であるため、図３（Ａ）、（Ｂ）、（Ｃ）を参照してその概略を簡単に説明する。

【００３８】まず、透明基板１０に対して、必要に応じて、ＴＥＯＳ（テトラエトキシシラン）や酸素ガスなどを原料ガスとしてプラズマＣＶＤ法により厚さが約２０００～５０００オングストロームのシリコン酸化膜からなる下地保護膜（図示せず。）を形成した後、下地保護膜の表面にプラズマＣＶＤ法により厚さが約３００～７００オングストロームのアモルファスのシリコン膜からなる半導体膜を形成する。次にアモルファスのシリコン膜からなる半導体膜に対して、レーザアニールまたは固相成長法などの結晶化工程を行い、半導体膜をポリシリコン膜に結晶化する。

【００３９】次に、半導体膜をパターニングして島状の半導体膜とし、その表面に対して、ＴＥＯＳ（テトラエトキシシラン）や酸素ガスなどを原料ガスとしてプラズマＣＶＤ法により厚さが約６００～１５００オングストロームのシリコン酸化膜または窒化膜からなるゲート絶縁膜５７を形成する。

【００４０】次に、アルミニウム、タンタル、モリブデン、チタン、タングステンなどの金属膜からなる導電膜をスパッタ法により形成した後、パターニングし、ゲート電極２１、３１、およびゲート電極３１の延設部分３６を形成する（ゲート電極形成工程）。この工程では走査線ｇａｔｅも形成する。

【００４１】この状態で、高濃度のリンイオンを打ち込んで、ゲート電極２１、３１に対して自己整合的にソース・ドレイン領域を形成する。なお、不純物が導入されなかった部分がチャネル領域となる。

【００４２】次に、第１の層間絶縁膜５１を形成した後、各コンタクトホールを形成し、次に、データ線ｓｉｇ、ドレイン電極２２、共通給電線ｃｏｍ、共通給電線ｃｏｍの延設部分３９、および中継電極３５を形成する。その結果、第１のＴＦＴ２０、第２のＴＦＴ３０、および保持容量ｃａｐが形成される。

【００４３】次に、第２の層間絶縁膜５２を形成し、この層間絶縁膜には、中継電極３５に相当する部分にコンタクトホール形成する。次に、第２の層間絶縁膜５２の表面全体にＩＴＯ膜を形成した後、パターニングし、コンタクトホールを介して第２のＴＦＴ３０のソース・ドレイン領域に電気的に接続する画素電極４１を画素７毎に形成する。

【００４４】次に、第２の層間絶縁膜５２の表面側にレジスト層を形成した後、このレジストを走査線ｇａｔｅおよびデータ線ｓｉｇに沿って残すようにパターニングし、バンク層ｂａｎｋを形成する。また、バンク層ｂａｎｋの所定部分には途切れ部分ｏｆｆを形成しておく。このとき、データ線ｓｉｇに沿って残すレジスト部分は共通給電線ｃｏｍを覆うように幅広とする。その結果、発光素子４０の有機半導体膜４３を形成すべき領域はバンク層ｂａｎｋに囲まれる。

【００４５】次に、バンク層ｂａｎｋでマトリクス状に区画された領域内にインクジェット法を利用してＲ、Ｇ、Ｂに対応する各有機半導体膜４３を形成していく。それには、バンク層ｂａｎｋの内側領域に対してインクジェットヘッドから、有機半導体膜４３を構成するための液状の材料（前駆体）を吐出し、それをバンク層ｂａｎｋの内側領域で定着させて有機半導体膜４３を形成する。ここで、バンク層ｂａｎｋはレジストから構成されているため、撥水性である。これに対して、有機半導体膜４３の前駆体は親水性の溶媒を用いているため、たとえ有機半導体膜４３の形成領域を区画するバンク層ｂａｎｋに途切れ部分ｏｆｆがあったとしても、かかる途切れ部分ｏｆｆは狭いので、有機半導体膜４３の塗布領域はバンク層ｂａｎｋによって確実に規定され、隣接する画素７にはみ出ることがない。それ故、有機半導体膜４

３などを所定領域内だけに形成できる。この工程において、インクジェットヘッドから吐出した前駆体は表面張力の影響で約２μｍないし約４μｍの厚さに盛り上がるため、バンク層ｂａｎｋは約１μｍないし約３μｍの厚さが必要である。なお、定着した後の有機半導体膜４３の厚さは約０．０５μｍから約０．２μｍである。なお、予めバンク層ｂａｎｋからなる隔壁が１μｍ以上の高さであれば、バンク層ｂａｎｋが撥水性でなくても、バンク層ｂａｎｋは隔壁として十分に機能する。かかる厚いバンク層ｂａｎｋを形成しておけば、インクジェット法に代えて、塗布法で有機半導体膜４３を形成する場合でもその形成領域を規定できる。

【００４６】しかる後には、透明基板１０の略全面に対向電極ｏｐを形成する。

【００４７】このような製造方法によれば、インクジェット法を利用して所定の領域にＲ、Ｇ、Ｂに対応する各有機半導体膜４３を形成していけるので、フルカラーのアクティブマトリクス型表示装置１を高い生産性で製造できる。

【００４８】なお、図１に示すデータ側駆動回路３や走査側駆動回路４にもＴＦＴが形成されるが、これらのＴＦＴは前記の画素７にＴＦＴを形成していく工程の全部あるいは一部を援用して行われる。それ故、駆動回路を構成するＴＦＴも、画素７のＴＦＴと同一の層間に形成されることになる。また、前記第１のＴＦＴ２０、および第２のＴＦＴ３０については、双方がＮ型、双方がＰ型、一方がＮ型で他方がＰ型のいずれでもよいが、このようないずれの組合せであっても周知の方法でＴＦＴを形成していけるので、その説明を省略する。

【００４９】［実施の形態１の変形例１］図４は、アクティブマトリクス型表示装置の全体のレイアウトを模式的に示すブロック図である。図５は、それに構成されている画素の１つを抜き出して示す平面図、図６（Ａ）、（Ｂ）、（Ｃ）はそれぞれ図５のＡ－Ａ′断面図、Ｂ－Ｂ′断面図、およびＣ－Ｃ′断面図である。なお、本形態と実施の形態１とは基本的な構成が同一なので、共通する部分には同一の符号を各図に付してそれらの詳細な説明を省略する。

【００５０】図４、図５、および図６（Ａ）、（Ｂ）、（Ｃ）に示すように、本形態のアクティブマトリクス型表示装置１でも、データ線ｓｉｇおよび走査線ｇａｔｅに沿って、レジスト膜からなる厚い絶縁膜（バンク層ｂａｎｋ／左下がりの斜線を広いピッチで付した領域）を設け、このバンク層ｂａｎｋの上層側に対向電極ｏｐを形成してある。このため、データ線ｓｉｇと対向電極ｏｐとの間には、第２の層間絶縁膜５２と厚いバンク層ｂａｎｋが介在しているので、データ線ｓｉｇに寄生する容量が極めて小さい。それ故、駆動回路３、４の負荷を低減でき、低消費電力化あるいは表示動作の高速化を図ることができる。

【００５１】また、透明基板１０の周辺領域（表示部１１の外側領域）にもバンク層ｂａｎｋ（形成領域に斜線を付してある。）を形成する。従って、データ側駆動回路３および走査側駆動回路４はいずれも、バンク層ｂａｎｋによって覆われている。このため、これらの駆動回路の形成領域に対して対向電極ｏｐが重なる状態にあっても、駆動回路の配線層と対向電極ｏｐとの間にバンク層ｂａｎｋが介在することになる。それ故、駆動回路３、４に容量が寄生することを防止できるため、駆動回路３、４の負荷を低減でき、低消費電力化あるいは表示動作の高速化を図ることができる。

【００５２】さらに、本形態では、画素電極４１の形成領域のうち、導通制御回路５０の中継電極３５と重なる領域にもバンク層ｂａｎｋが形成されているため、無駄な無効電流が流れることを防止できる。それ故、共通給電線ｃｏｍの幅はその分、狭くてよい。

【００５３】さらにまた、本形態では、データ線ｓｉｇおよび走査線ｇａｔｅに沿ってバンク層ｂａｎｋを形成してあるため、いずれの画素７もバンク層ｂａｎｋで囲まれている。このため、インクジェット法を利用して所定の領域にＲ、Ｇ、Ｂに対応する各有機半導体膜４３を形成していけるので、フルカラーのアクティブマトリクス型表示装置１を高い生産性で製造できる。

【００５４】しかも、バンク層ｂａｎｋには、走査線ｇａｔｅの延設方向で隣り合う画素７の間に相当する部分に途切れ部分ｏｆｆが形成されている。また、バンク層ｂａｎｋには、データ線ｓｉｇおよび走査線ｇａｔｅの各延設方向の端部のそれぞれにも途切れ部分ｏｆｆが形成されている。さらに、走査側駆動回路４およびデータ側駆動回路３の上層側に形成されたバンク層ｂａｎｋは、走査側駆動回路４の形成領域とデータ側駆動回路３の形成領域との間に相当する位置に途切れ部分ｏｆｆが形成されている。従って、対向電極ｏｐは、バンク層ｂａｎｋに起因する段差のない平坦部分（途切れ部分ｏｆｆ）を介して確実に接続し、断線することがない。

【００５５】［実施の形態１の変形例２］図７は、アクティブマトリクス型表示装置の全体のレイアウトを模式的に示すブロック図である。図８は、それに構成されている画素の１つを抜き出して示す平面図、図９（Ａ）、（Ｂ）、（Ｃ）はそれぞれ図８のＡ－Ａ′断面図、Ｂ－Ｂ′断面図、およびＣ－Ｃ′断面図である。なお、本形態と実施の形態１とは基本的な構成が同一なので、共通する部分には同一の符号を各図に付してそれらの詳細な説明を省略する。

【００５６】図７、図８、および図９（Ａ）、（Ｂ）、（Ｃ）に示すように、本形態のアクティブマトリクス型表示装置１でも、データ線ｓｉｇおよび走査線ｇａｔｅに沿って、レジスト膜からなる厚い絶縁膜（バンク層ｂａｎｋ／左下がりの斜線を広いピッチで付した領域）を設け、このバンク層ｂａｎｋの上層側に対向電極ｏｐを

形成してある。このため、データ線ｓｉｇと対向電極ｏｐとの間には、第２の層間絶縁膜５２と厚いバンク層ｂａｎｋが介在しているので、データ線ｓｉｇに寄生する容量が極めて小さい。それ故、駆動回路３、４の負荷を低減でき、低消費電力化あるいは表示動作の高速化を図ることができる。

【００５７】また、透明基板１０の周辺領域（表示部１１の外側領域）にもバンク層ｂａｎｋ（形成領域に斜線を付してある。）を形成する。従って、データ側駆動回路３および走査側駆動回路４はいずれも、バンク層ｂａｎｋによって覆われている。このため、これらの駆動回路の形成領域に対して対向電極ｏｐが重なる状態にあっても、駆動回路の配線層と対向電極ｏｐとの間にバンク層ｂａｎｋが介在することになる。それ故、駆動回路３、４に容量が寄生することを防止できるため、駆動回路３、４の負荷を低減でき、低消費電力化あるいは表示動作の高速化を図ることができる。

【００５８】さらに、本形態では、画素電極４１の形成領域のうち、導通制御回路５０の中継電極３５と重なる領域にもバンク層ｂａｎｋが形成されているため、無駄な無効電流が流れることを防止できる。それ故、共通給電線ｃｏｍの幅はその分、狭くてよい。

【００５９】さらにまた、本形態では、データ線ｓｉｇおよび走査線ｇａｔｅに沿ってバンク層ｂａｎｋを形成してあるため、いずれの画素７もバンク層ｂａｎｋで囲まれている。このため、インクジェット法を利用して所定の領域にＲ、Ｇ、Ｂに対応する各有機半導体膜４３を形成していけるので、フルカラーのアクティブマトリクス型表示装置１を高い生産性で製造できる。

【００６０】しかも、バンク層ｂａｎｋには、データ線ｓｉｇの延設方向で隣り合う画素７の間に相当する部分に途切れ部分ｏｆｆが形成されている。また、バンク層ｂａｎｋには、データ線ｓｉｇおよび走査線ｇａｔｅの各延設方向の端部のそれぞれにも途切れ部分ｏｆｆが形成されている。さらに、走査側駆動回路４およびデータ側駆動回路３の上層側に形成されたバンク層ｂａｎｋは、走査側駆動回路４の形成領域とデータ側駆動回路３の形成領域との間に相当する位置に途切れ部分ｏｆｆが形成されている。従って、対向電極ｏｐは、バンク層ｂａｎｋに起因する段差のない平坦部分（途切れ部分ｏｆｆ）を介して確実に接続し、断線することがない。

【００６１】［実施の形態２］図１０は、アクティブマトリクス型表示装置の全体のレイアウトを模式的に示すブロック図である。図１１は、それに構成されている画素の１つを抜き出して示す平面図、図１２（Ａ）、（Ｂ）、（Ｃ）はそれぞれ図１１のＡ－Ａ′断面図、Ｂ－Ｂ′断面図、およびＣ－Ｃ′断面図である。なお、本形態と実施の形態１とは基本的な構成が同一なので、共通する部分には同一の符号を各図に付してそれらの詳細な説明を省略する。

【００６２】図１０、図１１、および図１２（Ａ）、（Ｂ）、（Ｃ）に示すように、本形態のアクティブマトリクス型表示装置１では、データ線ｓｉｇに沿って、レジスト膜からなる厚い絶縁膜（バンク層ｂａｎｋ／左下がりの斜線を広いピッチで付した領域）がストライプ状に形成され、このバンク層ｂａｎｋの上層側に対向電極ｏｐを形成してある。このため、データ線ｓｉｇと対向電極ｏｐとの間には、第２の層間絶縁膜５２と厚いバンク層ｂａｎｋが介在しているので、データ線ｓｉｇに寄生する容量が極めて小さい。それ故、駆動回路３、４の負荷を低減でき、低消費電力化あるいは表示動作の高速化を図ることができる。

【００６３】また、透明基板１０の周辺領域（表示部１１の外側領域）にもバンク層ｂａｎｋ（形成領域に斜線を付してある。）が形成されている。従って、データ側駆動回路３および走査側駆動回路４はいずれも、バンク層ｂａｎｋによって覆われているため、これらの駆動回路の形成領域に対して対向電極ｏｐが重なる状態にあっても、駆動回路の配線層と対向電極ｏｐとの間にバンク層ｂａｎｋが介在することになる。それ故、駆動回路３、４に容量が寄生することを防止できるため、駆動回路３、４の負荷を低減でき、低消費電力化あるいは表示動作の高速化を図ることができる。

【００６４】さらに、本形態では、データ線ｓｉｇに沿ってバンク層ｂａｎｋを形成してあるため、バンク層ｂａｎｋでストライプ状に区画された領域内にインクジェット法を利用してＲ、Ｇ、Ｂに対応する各有機半導体膜４３をストライプ状に形成していけるので、フルカラーのアクティブマトリクス型表示装置１を高い生産性で製造できる。

【００６５】しかも、バンク層ｂａｎｋには、データ線ｓｉｇの延設方向の端部に途切れ部分ｏｆｆが形成されている。従って、各画素７の対向電極ｏｐは、走査線ｇａｔｅの延設方向では、隣接する画素７の対向電極ｏｐに対して厚いバンク層ｂａｎｋを乗り越えて接続している。それでも、データ線ｓｉｇの延設方向を辿っていくと、各画素７の対向電極ｏｐは、データ線ｓｉｇの端部で途切れ部分ｏｆｆ（（バンク層ｂａｎｋに起因する段差のない平坦部分）を介して、走査線ｇａｔｅの延設方向で隣接する画素７の列と接続している。それ故、各画素７の対向電極ｏｐは、バンク層ｂａｎｋに起因する段差のない平坦部分を介して他の画素７の対向電極ｏｐに接続しているといえ、いずれの画素７の対向電極ｏｐも断線状態になることはない。

【００６６】［その他の実施の形態］なお、バンク層ｂａｎｋ（絶縁膜）についてはレジスト膜、ポリイミド膜などの有機材料から構成した場合には厚い膜を容易に形成できるが、バンク層ｂａｎｋ（絶縁膜）をＣＶＤ法あるいはＳＯＧ法で成膜したシリコン酸化膜あるいはシリコン窒化膜などの無機材料から構成した場合には、有機

半導体膜43と接触した状態にあっても有機半導体膜43の変質を防止することができる。

【0067】また、保持容量capについては共通給電線comとの間に形成した構造の他、走査線gateと並列に形成した容量線との間に形成してもよい。

【0068】

【発明の効果】以上説明したように、本発明に係るアクティブマトリクス型表示装置では、データ線と対向電極との間に厚い絶縁膜を介在させたので、データ線に容量が寄生することを防止できる。それ故、データ線駆動回路の負荷を低減できるので、低消費電力化あるいは表示動作の高速化を図ることができる。また、厚い絶縁膜の所定の位置に途切れ部分を構成し、この部分を平坦にしてある。従って、各領域毎の対向電極は平坦部分に形成された部分を介して電気的に接続するので、たとえ、絶縁膜に起因する段差によってこの部分で断線しても、絶縁膜の途切れ部分に相当する平坦部分を介して確実に電気的に接続している。よって、有機半導体膜等の発光薄膜の周りに厚い絶縁膜を形成して寄生容量などを抑えたとしても、絶縁膜の上層に形成する対向電極に断線が発生しないので、アクティブマトリクス型表示装置の表示品質および信頼性を向上することができる。

【図面の簡単な説明】

【図1】本発明の実施の形態1に係るアクティブマトリクス型表示装置の全体のレイアウトを模式的に示すブロック図である。

【図2】図1に示すアクティブマトリクス型表示装置に構成されている画素の1つを抜き出して示す平面図である。

【図3】（A）、（B）、（C）はそれぞれ図2のA－A′断面図、B－B′断面図、およびC－C′断面図である。

【図4】本発明の実施の形態1の変形例1に係るアクティブマトリクス型表示装置の全体のレイアウトを模式的に示すブロック図である。

【図5】図4に示すアクティブマトリクス型表示装置に構成されている画素の1つを抜き出して示す平面図である。

【図6】（A）、（B）、（C）はそれぞれ図5のA－A′断面図、B－B′断面図、およびC－C′断面図である。

【図7】本発明の実施の形態1の変形例2に係るアクティブマトリクス型表示装置の全体のレイアウトを模式的に示すブロック図である。

【図8】図7に示すアクティブマトリクス型表示装置に構成されている画素の1つを抜き出して示す平面図である。

【図9】（A）、（B）、（C）はそれぞれ図8のA－A′断面図、B－B′断面図、およびC－C′断面図である。

【図10】本発明の実施の形態2に係るアクティブマトリクス型表示装置の全体のレイアウトを模式的に示すブロック図である。

【図11】図10に示すアクティブマトリクス型表示装置に構成されている画素の1つを抜き出して示す平面図である。

【図12】（A）、（B）、（C）はそれぞれ図11のA－A′断面図、B－B′断面図、およびC－C′断面図である。

【図13】従来および本発明の比較例に係るアクティブマトリクス型表示装置の全体のレイアウトを模式的に示すブロック図である。

【図14】図13に示すアクティブマトリクス型表示装置に構成されている画素の1つを抜き出して示す平面図である。

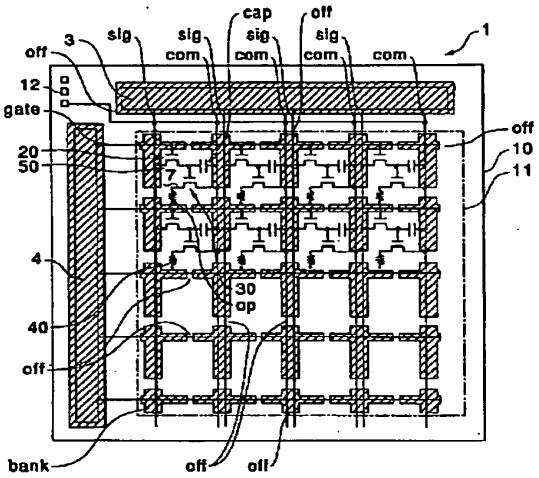
【図15】（A）、（B）、（C）はそれぞれ図14のA－A′断面図、B－B′断面図、およびC－C′断面図である。

【図16】（A）、（B）、（C）はそれぞれ図14の別のA－A′断面図、B－B′断面図、およびC－C′断面図である。

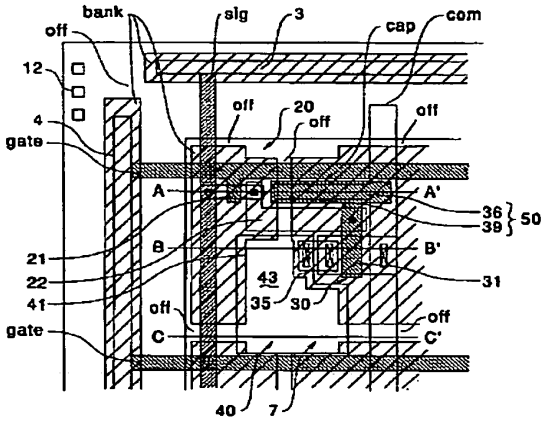
【符号の説明】

1	アクティブマトリクス型表示装置
2	表示部
3	データ側駆動回路
4	走査側駆動回路
7	画素
10	透明基板
12	端子
20	第1のTFT
21	第1のTFTのゲート電極
30	第2のTFT
31	第2のTFTのゲート電極
40	発光素子
41	画素電極
43	有機半導体
bank	バンク層（絶縁膜）
cap	保持容量
com	共通給電線
gate	走査線
op	対向電極
sig	データ線
off	バンク層の途切れ部分

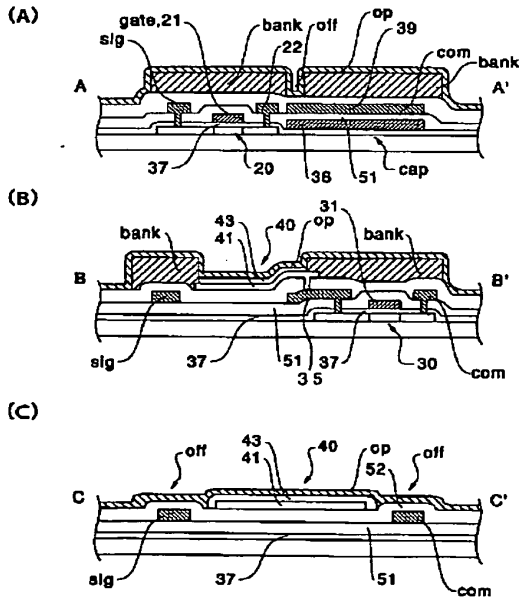
【図1】


off
3
sig
sig
com
cap
off
sig
com
sig
com
com
1
12
gate
20
50
4
40
off
bank
7
30
op
off
10
11

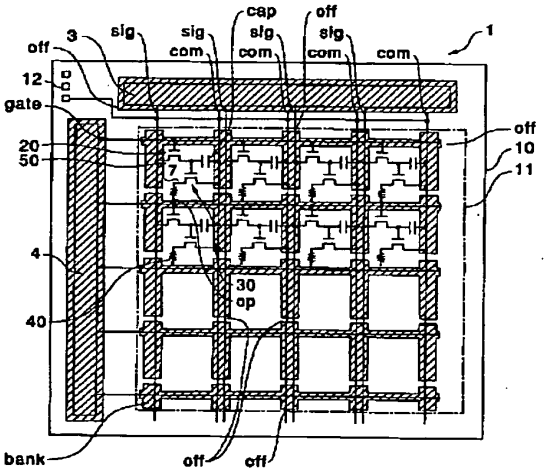
【図2】


bank
off
sig
3
cap
com
12
4
gate
off
20
off
off
A
A'
36
39
50
B
B'
21
22
41
43
35
30
31
off
gate
C
C'
off
40
7

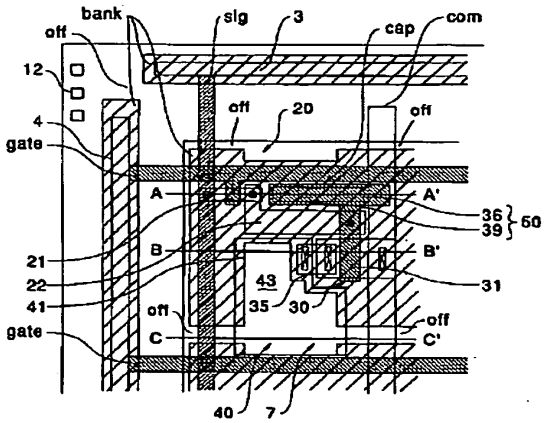
【図3】


(A)
gate,21
sig
bank
22
off
op
39
com
bank
A
A'
37
20
38
51
cap
(B)
31
op
43
41
40
bank
bank
B
B'
sig
37
51
37
35
30
com
(C)
43
41
40
off
op
52
off
C
C'
sig
37
51
com

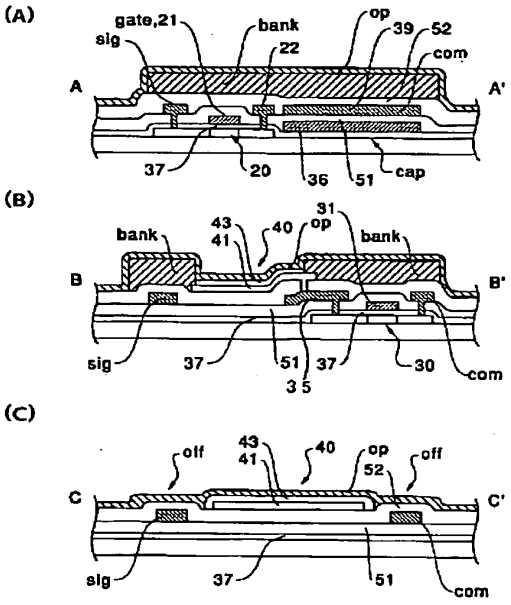
【図4】


off
3
sig
sig
com
cap
sig
com
off
sig
com
com
1
12
gate
20
50
7
off
10
11
4
40
30
op
bank
off
off

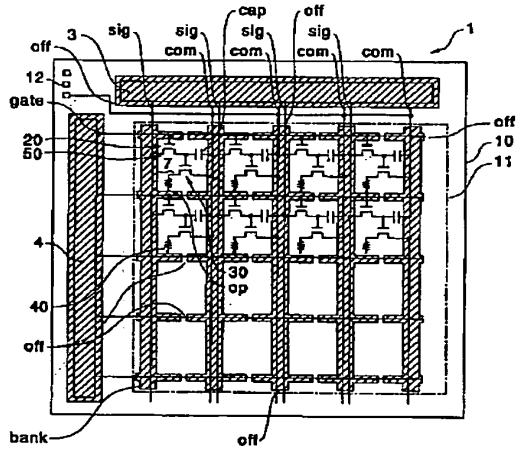
【図5】


bank
sig
3
cap
com
off
12
4
gate
off
20
off
A
A'
36
39
50
21
22
41
B
B'
43
31
35
30
off
gate
C
C'
off
40
7

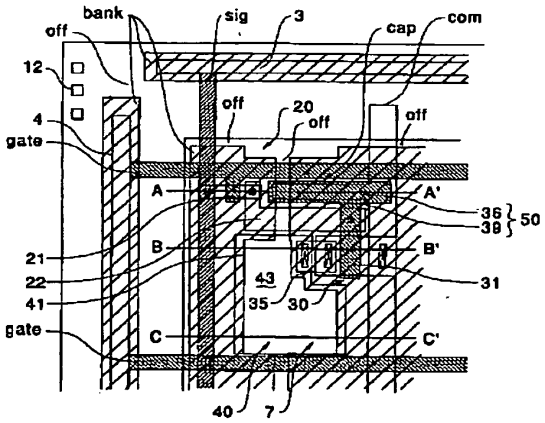
【図6】


(A)
gate,21
bank
op
39
52
sig
22
com
A
A'
37
20
36
51
cap
(B)
31
bank
43
41
40
op
bank
B
B'
sig
37
51
37
30
com
35
(C)
off
43
41
40
op
52
off
C
C'
sig
37
51
com

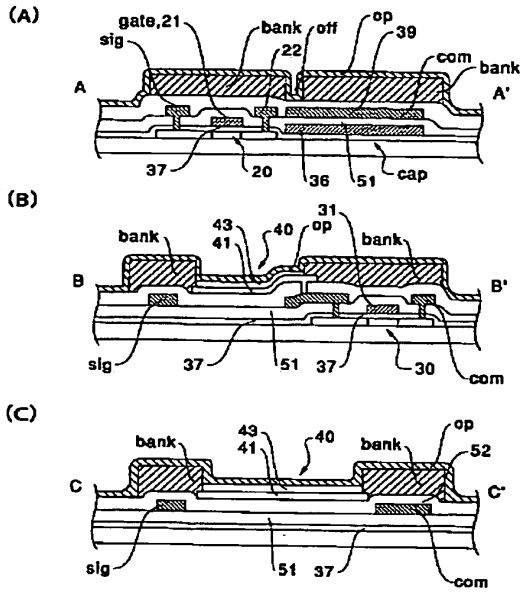
【図7】


cap
off
3
sig
sig
sig
sig
sig
1
off
com
com
com
com
com
12
gate
off
20
50
10
11
7
4
30
op
40
off
bank
off

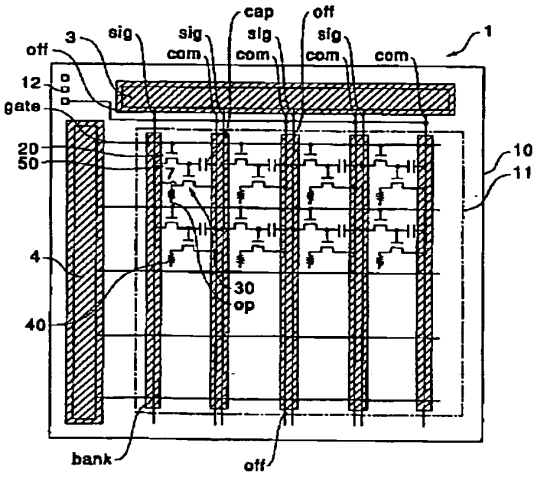
【図8】


bank
sig
3
cap
com
off
12
off
20
off
off
4
gate
A
A'
36
39
50
21
B
B'
22
43
31
41
35
30
gate
C
C'
40
7

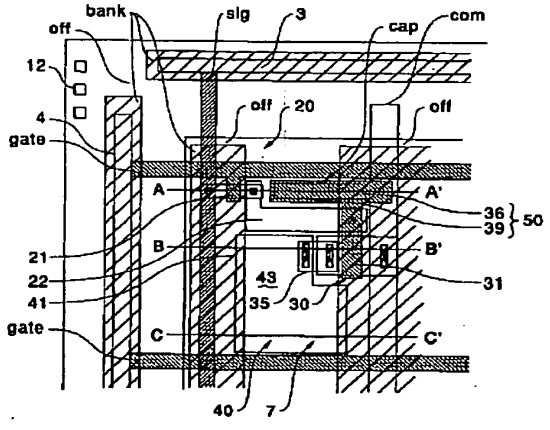
【図9】



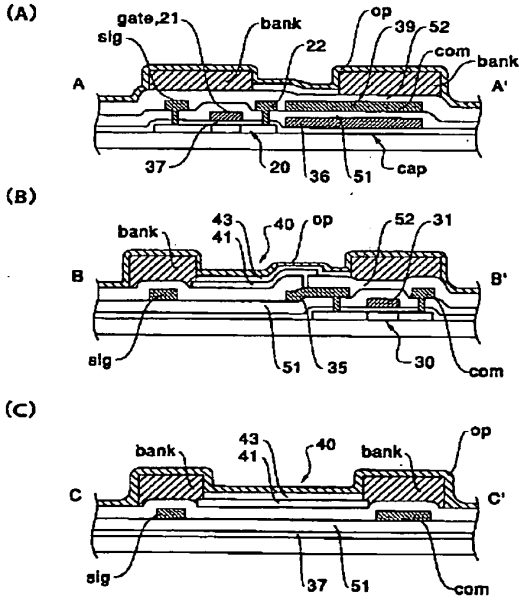
【図10】



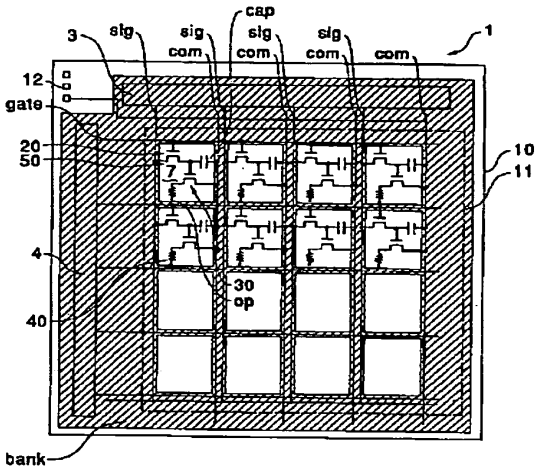
【図11】



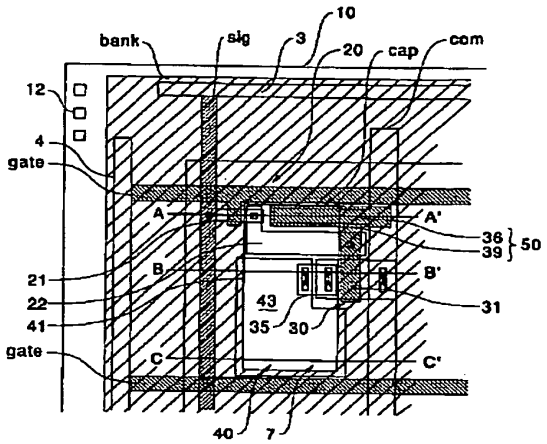
【図12】



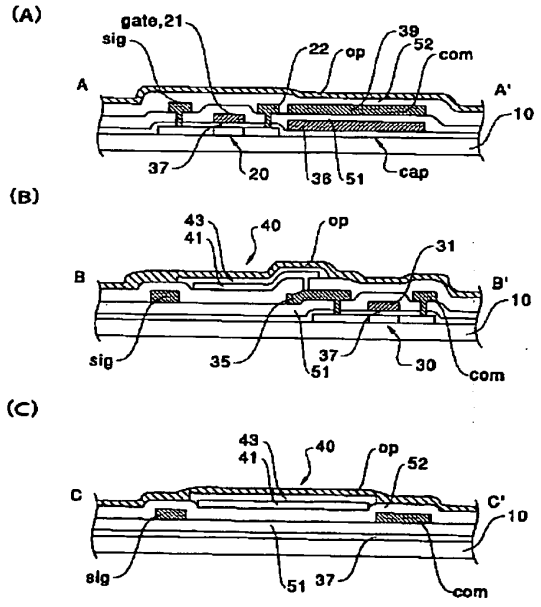
【図１３】



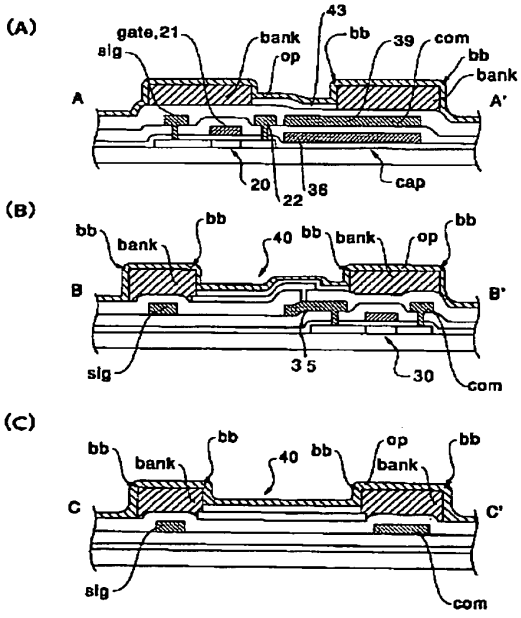
【図１４】



【図１５】



【図１６】



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⑫公開特許公報（A）　平1－101519

⑤1Int.Cl.⁴	識別記号	庁内整理番号	④3公開
G 02 F 1/133	327	7370－2H	平成1年(1989)4月19日

審査請求　未請求　発明の数 1　（全7頁）

⑤4発明の名称　アクティブマトリクス基板

⑦1特　願　昭62－258854

⑦2出　願　昭62(1987)10月14日

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⑦4代理人　弁理士　最上　務　外1名

明細書

1．発明の名称

アクティブマトリクス基板

2．特許請求の範囲

（1）薄膜トランジスタ、ソース配線、ゲート配線、画素電極、前記ソース配線と前記ゲート配線を絶縁する絶縁膜を具備するアクティブマトリクス基板において、前記ゲート配線と同じ材質で同時に形成された一部のソース配線、前記一部のソース配線を結合させる様に前記画素電極と同じ材質で同時に形成された架橋配線を具備することを特徴とするアクティブマトリクス基板。

（2）前記ソース配線と同じ材質で同時に形成された一部のゲート配線、前記一部のゲート配線を結合させる様に前記画素電極と同じ材質で同時に形成された架橋配線を具備することを特徴とする特許請求の範囲第1項に記載のアクティブマトリクス基板。

3．発明の詳細な説明

〔産業上の利用分野〕

本発明は、アクティブマトリクス方式の液晶ディスプレイやエレクトロクロミックディスプレイ等に用いられるアクティブマトリクス基板に関する。

〔従来の技術〕

従来のアクティブマトリクス基板は、例えば、JAPAN DISPLAY'86の196～199ページに見られる様に、配線材料としてITO、不純物を含む多結晶シリコン等が用いられている。

第3図（a）は、従来のアクティブマトリクス基板の上視図であり、第3図（b）は前記第3図（a）のBB'における断面図である。又、従来のアクティブマトリクス基板の製造工程の一部の上視図を第4図（a）～（d）に、断面図を第4図（a'）～（d'）に示した。

（a）、（a'）は下地絶縁膜411上に薄膜

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トランジスタのチャンネル領域４０５、ソース領域４０６、ドレイン領域４０７及びゲート絶縁膜４０９を形成した図である。（ｂ）、（ｂ′）はゲート電極、及びゲート配線４０１を形成した図であり、（ｃ）、（ｃ′）においてゲート配線４０１とソース配線４０２を絶縁する絶縁膜４１０を形成し、さらに薄膜トランジスタのソース領域４０６とソース配線４０１、及び薄膜トランジスタのドレイン領域４０７と画素電極４０４を接合するためのコンタクトホール４０８を所定の位置に形成する。さらに（ｄ）、（ｄ′）においてソース配線４０２と画素電極４０４を形成することによって、従来のアクティブマトリクス基板が作られる。

以上の工程を見れば明らかな様に、従来のアクティブマトリクス基板の配線方法では、２回の配線用の薄膜の形成と２回のフォトエッチング工程が必要である。

（発明が解決しようとする問題点）

前記の、従来の配線材料であるＩＴＯ等は、その比抵抗が３００μΩｃｍと大きく、信号遅延等の観点から、配線材料として用いることができるのは、約１０㎝程度の画面サイズが限界となり、それ以上の大型化は不可能である。したがって上記以上の画面サイズを実現するためには、より低抵抗の配線材料による配線が不可欠となる。しかし、従来の配線と構造のままで、配線の材料を変えると、ソース配線の材料と画素電極の材料が異なるために、薄膜形成とフォトエッチングの回数が１回づつ増え、製造工程を非常に複雑なものにする。

本発明は、この様な問題点を解決するもので、その目的とするところは、より大型で信頼性の高いアクティブマトリクス基板を提供することにある。

（問題点を解決するための手段）

薄膜トランジスタ、ソース配線、ゲート配線、画素電極、前記ソース配線と前記ゲート配線を絶縁する絶縁膜を具備するアクティブマトリクス基板において、本発明のアクティブマトリクス基板は、前記ゲート配線と同じ材質で同時に形成された一部のソース配線、前記一部のソース配線を結合させる様に前記画素電極と同じ材質で同時に形成された架橋配線を具備するか、又は前記ソース配線と同じ材質で同時に形成された一部のゲート配線、前記ゲート配線を結合させる様に前記画素電極と同じ材質で同時に形成された架橋配線を具備することを特徴とする。

（実施例）

以下、本発明について、実施例に基づき詳細に説明する。

実施例１

第１図は本発明によるアクティブマトリクス基板の一例の上視図である。１０３の架橋配線により、ソース配線１０２とゲート配線１０１の交差部を架橋しているのが特徴である。第２図に第１図のＡＡ′における断面図を示した。

本発明の、実施例を第５図の、上視図（ａ）～（ｄ）、断面図（ａ′）～（ｄ′）を用いて、工程順に、さらに詳しく説明する。まず、（ａ）、（ａ′）の如く、ガラス、石英、サファイア等の絶縁性基板上に、二酸化硅素、窒化硅素等から成る清浄な下地絶縁膜５１１を形成する。その上に１５００Å～３０００Å程度のドナー、あるいはアクセプタとなる不純物を含む、多結晶シリコン膜、若しくは非晶質シリコン膜を所定の形状に形成する。さらにその上に１００Å～５００Å程度の故不純物を含まない多結晶シリコン、又は非晶質シリコンからなる薄膜を、所定の形状に形成する。この工程により薄膜トランジスタのチャンネル領域５０５、ソース領域５０６、ドレイン領域５０７が形成される。その上に５００Å～３０００Å程度の二酸化硅素、窒化硅素等の絶縁膜を形成し、ゲート絶縁膜５０９とする。

次に、（ｂ）、（ｂ′）に示す様にアルミニウム、モリブデン、タングステン、タンタル、ニオブ、チタンおよびその硅化物、各種合金、超電導物質等の低抵抗材料を用いて１０００Å～７０００Å程度の薄膜を所定の形状に形成し、ゲート配線５０１およびソース配線５０２とする。ここで

注目すべきことは、該ゲート配線と該ソース配線の交差部においては、ソース配線が形成されていないことである。この構造を採用することによって、ゲート配線とソース配線の大部分を同時に形成することが可能となる。

次に（ｃ）、（ｃ′）に示されるようにソース配線とゲート配線を絶縁する絶縁膜と薄膜トランジスタを保護するパッシベーション膜をかねた二酸化硅素、窒化硅素等からなる絶縁膜５１０を３０００Å～１００００Å程度形成し、図に示した様に所定の形状にコンタクトホール５０８を形成する。

次に（ｄ）、（ｄ′）に示される様にＩＴＯ膜を所定の形状に形成し、画素透明電極５０４、および該ゲート配線とソース配線の交差部においてソース配線を架橋する５０３の架橋配線を得る。又、この工程によりソース配線５０１とソース領域５０６、画素電極５０４とドレイン領域５０７のコンタクトがとられる。

以上の工程を経て、本発明によるアクティブマトリクスの１例が製造される。

実施例２

前実施例では、ソース配線を架橋したが、ゲート配線を、架橋することも可能であり、第６図（ａ）～（ｃ）に示した。

薄膜トランジスタの、チャンネル領域６０５、ソース領域６０６、ドレイン領域６０７を形成した後、絶縁膜を形成し、前実施例と同様な低低抗材料を用いてソース配線６０２とゲート配線６０１の大部分を形成する。この時、該ソース配線とゲート配線の交差部のゲート配線を形成せず、絶縁膜を形成し、コンタクトホール６０８を形成した後で、この交差部のゲート配線６０３を画素電極６０４及び薄膜トランジスタのソース領域６０８とソース配線６０２を結ぶ配線６１３と同時に形成する。

（発明の効果）

以上に述べたように本発明によれば、従来より工程数をまったく増やすことなく、ゲート配線、ソース配線の低低抗化が可能となる。これにより以下のような効果が得られる。

ａ．ゲート配線の低低抗化により、薄膜トランジスタのスイッチング時間を短縮できるため、画素数を増やすことができ、画面の大型化が可能となる。

ｂ．ソース配線の低低抗化により、画素に対する書き込み時間を短縮できるため、ａと同様な効果がある。

ｃ．配線を細くすることが可能となるために、ゲート配線とソース配線の間の容量等の寄生容量を小さくできる。これらの寄生容量はトランジスタのスイッチング速度を低下させる原因の１つであるため、本発明によって該寄生容量を小さくすることが可能となると、トランジスタの高速化が可能となり、その結果ａと同様な効果がある。

ｄ．配線を細くすることが可能となるために、画素の開口率を大きくすることができ、より明るい画像が得られる。

ｅ．単純に配線を金属等の、低低抗材料にすると、膜形成工程、フォトエッチング工程が、それぞれ１回増え、信頼性および歩留りの低下を招くが、本発明の工程数は従来の技術の工程数とかわりないため、これを回避することが可能である。

したがって本発明によれば、信頼性および歩留りの低下を招くことなく、アクティブマトリクス基板の大型化および高精細化、高開口率化による高画像品質化が可能となる。

４．図面の簡単な説明

第１図は、本発明の実施例の上視図である。第２図は、第１図のＡＡ′の断面図である。第３図（ａ）は従来のアクティブマトリクス基板の１例の上視図、（ｂ）はＢＢ′の断面図である。第４図（ａ）～（ｄ）、（ａ′）～（ｄ′）は従来例の製造工程を示したもので、（ａ）～（ｄ）は上視図、（ａ′）～（ｄ′）は断面図である。第５図（ａ）～（ｄ）、（ａ′）～（ｄ′）は、本発明の実施例の製造工程を示したもので、（ａ）～（ｄ）は、上視図、（ａ′）～（ｄ′）は断面図である。第６図（ａ）～（ｃ）は実施例の製造工

程を示した上視図である。

１０１、２０１、３０１、４０１、５０１、６０１…ゲート配線

１０２、２０２、３０２、４０２、５０２、６０２…ソース配線

１０３、２０３、５０３、６０３…架橋配線

１０４、４０４、５０４、６０４…画素電極

１０５、４０５、５０５、６０５…チャンネル領域

１０６、４０６、５０６、６０６…ソース領域

１０７、４０７、５０７、６０７…ドレイン領域

１０８、４０８、５０８、６０８…コンタクトホール

２０９、３０９、４０９、５０９…ゲート絶縁膜

２１０、３１０、４１０、５１０…ソース配線、ゲート配線間絶縁膜

２１１、３１１、４１１、５１１…下地絶縁膜

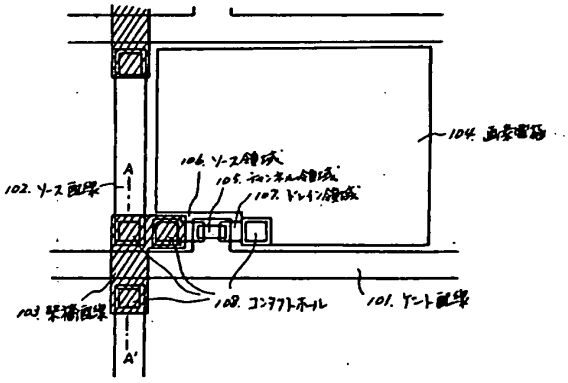
４１２、３１２、４１２、５１２…絶縁性基板

６１３…ソース領域、ソース配線間配線

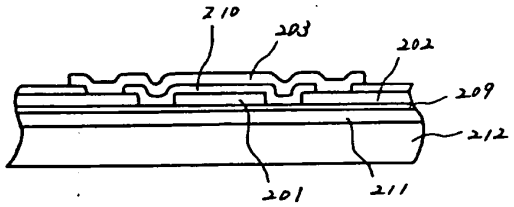
以　上

出願人　セイコーエプソン株式会社

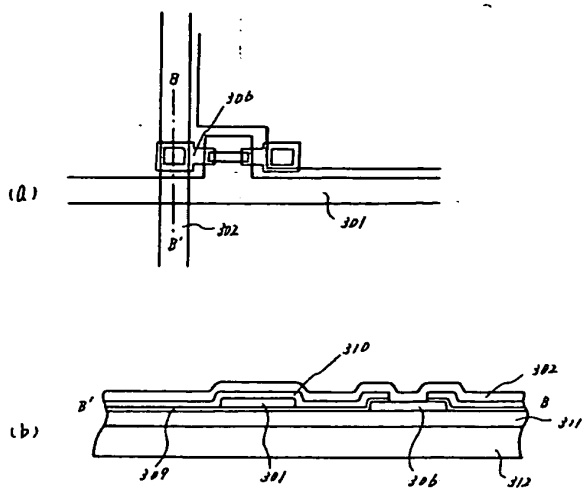
代理人　弁理士　最　上　務　他１名



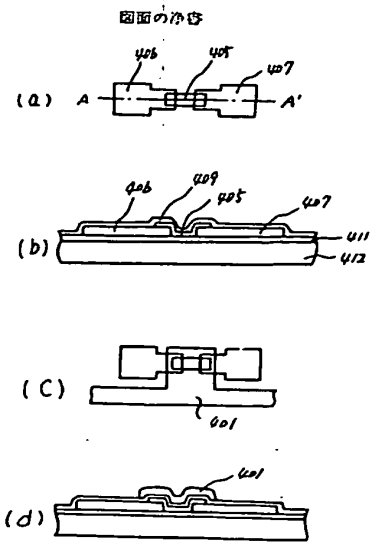
第１図



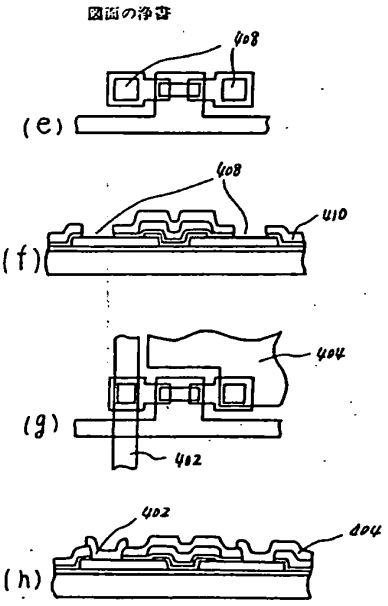
第２図



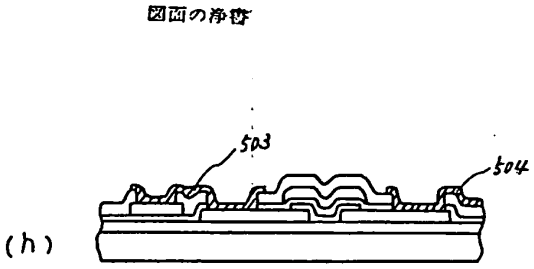
第3図



第4図



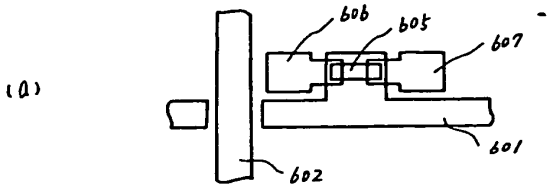
第4図

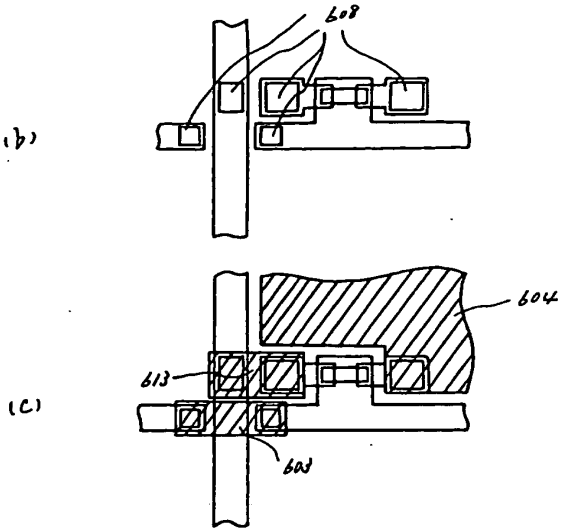


第5図

第5図

第5図





第6図

第6図

手続補正書（方式）

昭和63年2月18日

特許庁長官 小川邦夫 殿

1．事件の表示

昭和62年 特許願 第258854号

2．発明の名称

アクティブマトリクス基板

3．補正する者

事件との関係 出願人

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(4664) 弁理士 最上務 (他1名)

連絡先 563-2111 内線 631～635 担当 林

5．補正命令の日付

昭和63年 1月26日

6．補正の対象

明細書 (図面の簡単な説明)

図面 (第4図、第5図)

7．補正の内容

別紙の通り

手続補正書

1．明細書第10頁第12行目、「第4図」から最終行「である。」を以下の如く補正する。

「第4図(a)～(h)は従来例の製造工程を示したもので(a)、(c)、(e)、(g)は上視図、(b)、(d)、(f)、(h)は断面図である。第5図(a)～(h)は、本発明の実施例1の製造工程を示したもので(a)、(c)、(e)、(g)は上視図(b)、(d)、(f)は断面図である。」

2．第4図、第5図を別紙の如く補正する。

以上

代理人 最上務他1名

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⑬公開　平成2年(1990)6月29日

審査請求　未請求　請求項の数 1　(全8頁)

⑤④発明の名称　薄膜電界効果型トランジスタ素子アレイ

⑳特　願　昭63−326841

㉒出　願　昭63(1988)12月23日

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⑦④代理人　弁理士　内原　晋

明　細　書

1. 発明の名称

薄膜電界効果型トランジスタ素子アレイ

2. 特許請求の範囲

透光性絶縁基板上にゲートバスラインとドレインバスラインとがマトリックス状に形成され、前記ゲートバスラインと前記ドレインバスラインとの各交差部付近に薄膜電界効果型トランジスタが形成され、各々の前記薄膜電界効果型トランジスタには画素電極が接続された薄膜電界効果型トランジスタ素子アレイにおいて、

ゲート電極、前記ゲートバスライン、前記ドレインバスラインは同一の金属膜で形成され、

前記金属膜により形成された前記ドレインバスラインは前記ゲートバスラインとの各交差部付近で分離されて島状化され、

透明導電膜により、前記画素電極、前記薄膜電界効果型トランジスタのドレイン、ソース電極、及び前記島状化された各ドレインバスラインの接続配線部が形成されていることを特徴とする薄膜電界効果型トランジスタ素子アレイ。

3. 発明の詳細な説明

(産業上の利用分野)

本発明は、特にアクティブマトリックス型液晶ディスプレイに用いる薄膜電界効果型トランジスタ素子アレイに関するものである。

(従来の技術)

携帯型コンピュータや壁掛けテレビ用のフラットパネルディスプレイとして液晶ディスプレイが注目されている。その中でもガラス基板上にアレイ化した薄膜電界効果型トランジスタを形成し、各画素のスイッチとして用いたアクティブマトリックス方式はフルカラー表示が可能であることからテレビなどへの応用が期待され、各機関で活発に開発が行なわれている。このアクティブマトリックス型液晶ディスプレイの実用化のためには低コスト化が重要な課題であり、その対策として構

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造及びプロセスの簡略化がある。薄膜電界効果型トランジスタのゲート電極をソースドレイン電極よりもガラス基板側に形成する逆スタガード方式においては、従来の技術としては、３枚のマスクを用いた製造方法がある（例えば、特開 昭６２－２８６２７１）。

第３図(a)ないし(g)は従来の方法を基本にした薄膜電界効果型トランジスタ素子アレイを形成する一工程図であり、(a)、(c)、(e)は上部から見た平面図であり、(b)、(d)、(f)、(g)はそれぞれ各平面図のA—A′、B—B′、C—C′、D—D′の断面図である。第３図において、１は透光性絶縁基板であるガラス基板であり、２ａ及び６ａはそれぞれクロム（Cr）ゲート電極及びクロム画素電極である。また２ｂ及び６ｂは透明導電膜から構成される透明ゲート電極及び透明画素電極である。また７は窒化シリコン（SiN_x）、８は水素化アモルファスシリコン（a-Si:H）、９は燐をドープしたｎ型水素化アモルファスシリコン（n^+-a-Si:H）である。さらに４はドレイン電極、５ａはクロムドレインバスライン

であり、同一の工程で形成され一体化されている。薄膜電界効果型トランジスタ１０（第３図(e)）のチャネル部をはさんでドレイン電極４の反対側に配置されたソース電極１４はクロム画素電極６ａを介して透明画素電極６ｂに接続されている。

ゲート電極及びドレイン電極としてクロム、ゲート絶縁膜としてSiN_x、半導体膜としてa-Si:H、ｎ型半導体膜として燐をドープしたn^+-a-Si:H、透明導電膜としてインジウム、錫の酸化物（Indium Tin Oxide：ITO）を使用して、従来の薄膜電界効果型トランジスタアレイを作製する工程を第３図を用いて説明する。まず、ガラス基板１上にＩＴＯ及び第１の金属としてクロムを積層し、第１のマスクパターンを用いてフォトリソグラフィ法によりクロムゲート電極２ａ、クロム画素電極６ａ、透明ゲート電極２ｂ及び透明画素電極６ｂを形成する（第３図(a)、(b)）。次にSiN_x７、a-Si:H８、n^+-a-Si:H９を順次積層し、第２のマスクを用いてフォトリソグラフィ法により、薄膜電界効果型トランジスタ１０及び

クロムドレインバスライン５ａ付近の積層膜を残して、それ以外の部分のSiN_x７、a-Si:H８、n^+-a-Si:H９を除去する（第３図(c)、(d)）。そして、さらに第２の金属としてクロムを成膜した後、第３のマスクを用いてフォトリソグラフィ法により、第２のクロムのエッチングを行ない、クロムドレインバスライン５ａ、ドレイン電極４、ソース電極１４を形成し、さらにエッチングを進めて透明画素電極６ｂ上の第１のクロムからなるクロム画素電極６ａを除去する。このとき同時に、薄膜トランジスタ１０及びクロムドレインバスライン５ａとの交差部以外の、透明ゲート電極６ｂ上の第１のクロムからなるクロムゲート電極も除去される。そして、同一のレジストパターンを使用してn^+-a-Si:H９をエッチングすることにより、ドレイン電極４とソース電極１４間のｎ型アモルファスシリコンを除去し、薄膜電界効果型トランジスタ１０のチャネル部を形成する（第３図(e)、(f)）。この場合には、ゲートバスライン３は薄膜トランジスタ１０及びドレインバスライン

５との交差部では第１のクロムとＩＴＯの積層構造であるが、それ以外の部分ではＩＴＯのみから構成される（第３図(g)）。

通常、逆スタガード型薄膜トランジスタアレイを作製するためには５～７枚のマスクパターンが必要とされるが、前述の方法によれば、マスク数３枚で薄膜電界効果型トランジスタアレイを形成できる。

（発明が解決しようとする課題）

さて、ディスプレイの表示サイズの大型化にともない配線長が増大し、高精細化にともない配線幅は減少する。したがって、配線抵抗が増加するので、ゲートバスライン及びドレインバスラインに印加された電圧は、配線容量との作用で伝搬遅延を生ずる。この伝搬遅延によって、各薄膜トランジスタへの電圧の印加が不十分となるので、信号電圧の各画素へ書き込みが不十分となり、表示品質の低下をもたらす。特に、ゲートバスラインの場合、ディスプレイにおいて横方向に配置されるので配線長が長く、配線抵抗が高い。さらにド

レインバスラインとの交差部における容量や薄膜トランジスタのチャネル容量など、配線容量が大きいので、伝搬遅延の影響がドレインバスラインよりも大きい。そして、第３図(e)の平面図からわかるように、ゲートバスラインの一部は金属と比較して比抵抗が数十倍から数百倍高い透明導電膜から形成されているので、配線抵抗は高く、影響はさらに大きい。また、第３図(e)の薄膜電界効果型トランジスタ１０付近にはａ－Ｓｉ：Ｈ８層が存在するために薄膜電界効果型トランジスタ１０のチャネル長及びチャネル幅の規定が困難であった。

本発明は、マスクパターンを３枚より増加させることなく、ゲートバスラインを金属から形成し、さらに成膜プロセスを減少させることが可能な薄膜電果効果型トランジスタ素子アレイを提供することを目的としている。

（課題を解決するための手段）

本発明は、透光性絶縁基板上にゲートバスラインとドレインバスラインとがマトリックス状に形成され、前記ゲートバスラインと前記ドレインバ

スラインとの各交差部付近に薄膜電界効果型トランジスタが形成され、各々の前記薄膜電界効果型トランジスタには画素電極が接続された薄膜電界効果型トランジスタ素子アレイにおいて、ゲート電極、前記ゲートバスライン、前記ドレインバスラインは同一の金属膜で形成され、前記金属膜により形成された前記ドレインバスラインは前記ゲートバスラインとの各交差部付近で分離されて島状化され、透明導電膜により、前記画素電極、前記薄膜電界効果型トランジスタのドレイン、ソース電極、及び前記島状化された各ドレインバスラインの接続配線部が形成されていることを特徴としている。

（作用）

本発明の薄膜電界効果型トランジスタ素子アレイによれば、配線抵抗の影響が大きいゲートバスラインの全部分を金属から構成できる。また、トランジスタのチャネル長及びチャネル幅の規定が確実である。さらに、従来は、透明導電膜、第１の金属、ゲート絶縁膜、半導体膜、ｎ型半導体膜、

第２の金属の計６回の成膜が必要であったが、本発明の構造によれば、第２の金属の成膜は必要ないので、プロセスが簡略化できる。

（実施例）

第１図(a)ないし(g)は、本発明による構造を持つ薄膜電界効果型トランジスタ素子アレイの製造方法の一実施例を示す工程図であり、(a)、(c)、(e)は上部から見た平面図であり、(b)、(d)、(f)、(g)はそれぞれ各平面図のＡ—Ａ′、Ｂ—Ｂ′、Ｃ—Ｃ′、Ｄ—Ｄ′の断面図である。第１図において、１は透光性絶縁基板であるガラス基板であり、２ａ及び３ａは金属としてクロムを使用したクロムゲート電極及びクロムゲートバスラインである。そして５ａは同じくクロムから形成したクロムドレインバスラインで島状に形成されている。また７は窒化シリコン（SiN_x）、８は水素化アモルファスシリコン（ａ－Ｓｉ：Ｈ）、９は燐をドープしたｎ型水素化アモルファスシリコン（n^+－ａ－Ｓｉ：Ｈ）である。そして、５ｂ、６ｂはそれぞれＩＴＯから形成された、透明ドレインバスライン、透明画素電極である。

る。さらに、４及び１４はそれぞれ、ドレイン電極、ソース電極である。

第１図を用いて本発明の構造を持つ薄膜電界効果型トランジスタ素子アレイの製造方法を説明する。まず、ガラス基板１上にスパッタ法により１０００Åのクロムを成膜し、第１のマスクパターンを用いてフォトリソグラフィ法により、クロムゲート電極２ａ、クロムドレインバスライン３ａ、クロムドレインバスライン５ａを形成する（第１図(a)、(b)）。具体的には、第１のマスクパターンをフォトレジストで形成し、ウエットエッチング法によりフォトレジストに覆われていない部分のクロムを除去する。このクロムのエッチングは、CCl_4 を用いたドライエッチング法でもよい。そして、エッチング後、フォトレジストを剥離することにより第１のマスクパターンを用いたフォトリソグラフィが終了する。マスクパターンの特徴としては、ドレインバスラインがゲートバスラインとの交差部付近において、分離されて島状化されていることである。次に、プラズマＣＶＤ

(Chcmical Vapor Deposition) 法により、SiN_x 7、a-Si:H 8、n^+-a-Si:H 9を順次成膜、積層する。なお、SiN_x 7、a-Si:H 膜8、n^+-a-Si:H 9の膜厚はそれぞれ、3000Å、2000Å、500Åである。その後、第2のマスクパターンを用いてフォトリソグラフィ法により、クロムゲート電極2a及びクロムゲートバスライン3a上にSiN_x 7、a-Si:H 8、n^+-a-Si:H 9の島を形成する（第1図(c)、(d)）。具体的には、フォトレジストで第2のマスクパターンの形状を形成する。そして、CF_4ガスを用いたドライエッチング法によりレジストに覆われていない部分のSiN_x 7、a-Si:H 8、n^+-a-Si:H 9を除去し、さらにフォトレジストを剥離する。その次に、スパッタ法によりITOを500Å成膜した後に第3のマスクパターンを用いてフォトリソグラフィ法により透明画素電極6b、ドレイン電極4、ソース電極14及び島状化されたドレインバスラインをそれぞれ接続するための透明ドレインバスライン5bを形成する。具体的には、

フォトレジストで第3のマスクパターンの形状を形成し、ウエットエッチング法によりレジストのない部分のITOを除去する。そして、同一のレジストパターンを使用してn^+-a-Si:H 9をエッチングすることにより、ドレイン電極4とソース電極14間のn^+-a-Si:Hを除去し、薄膜電界効果型トランジスタ10のチャネル部を形成する（第1図(e)、(f)、(g)）。最後にフォトレジストを除去することにより、薄膜電界効果型トランジスタ素子アレイが完成する。

以上の製造方法に述べたように、本実施例による薄膜電界効果型トランジスタアレイは、第1図(f)の平面図及び(g)の断面図に示すように、ゲートバスライン3は全部分をクロムから形成できる。クロムの抵抗はITOの1／20程度であるので、従来の一部ITOから構成されていたゲートバスラインと比較して、1桁程度低い配線抵抗のゲートバスラインが実現できた。なお、本実施例の場合にはドレインバスラインが一部ITOから構成されるが、ドレインバスラインにおいてはディス

プレイの縦方向に配置されるのでゲートバスラインより長さが短いこと、薄膜電界効果型トランジスタの容量についてはドレイン電極側のみ考慮すればよいことから、配線抵抗、配線容量による信号の伝搬遅延は短い（参考、昭和62年電子情報通信学会秋期大会半導体・材料部門予稿集185ページ）。したがって、信号電圧の書き込み不足による表示品質の低下をもたらすことのない、より大きなディスプレイが実現できる。

また、従来は、透明導電膜、第1の金属、ゲート絶縁膜、半導体膜、n型半導体膜、第2の金属の計6回の成膜が必要であったが、本発明の構造を持つ薄膜電界効果型トランジスタアレイの作製には、クロム膜、SiN_x膜、a-Si:H、n^+-a-Si:H 膜、ITO膜と5回しか成膜を行なわないので、製造プロセスの短縮が可能となる。

本実施例においては、透明導電膜としてITOを用いたが、In_2O_3 や SnO_2も使用できる。また、ゲート絶縁膜として、SiN_xのかわりにSiO_2を用いてもよい。さらに、ゲートバスライ

ンのクロムのかわりに、タンタル、アルミニウム、モリブデン等の他の金属を用いることも可能である。

本発明による他の薄膜電界効果型トランジスタ素子アレイの平面図を第2図に示す。この場合には、ITOをクロムゲートバスライン3a上にも配置することにより、ゲートバスラインの2重配線を行ない、断線を防止している。また、ドレインバスラインにおいても、ITOから形成された透明ドレインバスライン5b延長してドレイン電極4に接続し、さらに隣の透明バスラインとも接続することにより、ドレインバスラインの低抵抗化と、2重配線による断線防止策が施している。この他は前述の実施例と同じである。

（発明の効果）

以上述べてきたように、本発明の薄膜電界効果型トランジスタアレイによれば、ゲートバスラインの低抵抗化が可能となり、信号パルスの伝搬遅延を原因とした信号電圧の書き込み不足による表示品質の低下をもたらすことのない、より大きな

ディスプレイが実現できる。さらに、本発明の薄膜電界効果型トランジスタの製造に際しては、従来と比較して成膜工程が1回減少し、ディスプレイの製造コスト、歩留まりの点から有利であるので、実用上有効である。

4. 図面の簡単な説明

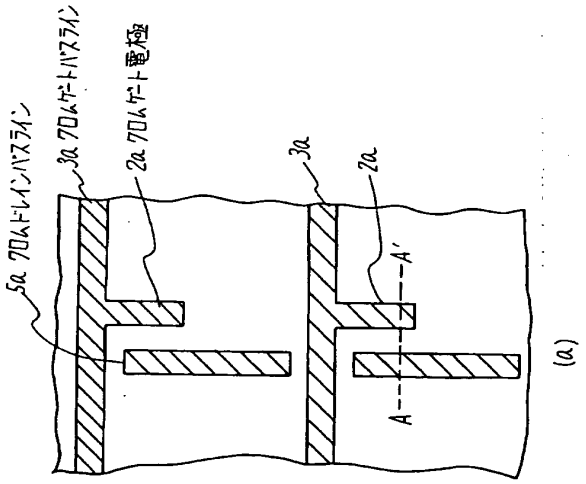
第1図(a)ないし(g)は、本発明による薄膜電界効果型トランジスタ素子アレイの一実施例の製造工程を説明する平面図及び断面図、第2図は他の実施例の平面図、第3図(a)ないし(g)は、従来の薄膜電界効果型トランジスタ素子アレイの製造工程を説明する平面図及び断面図である。

図において

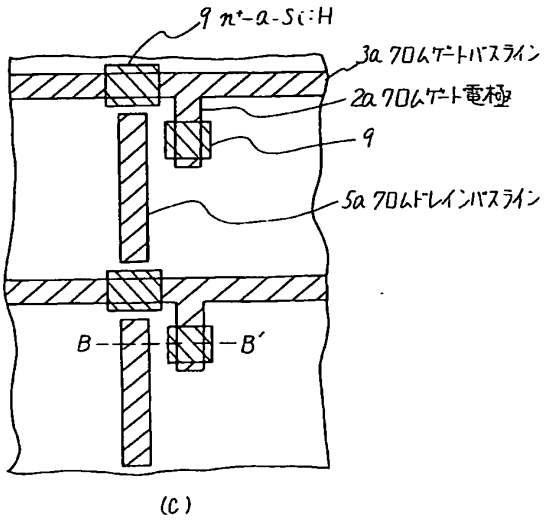
1……ガラス基板、2a……クロムゲート電極、2b……透明ゲート電極、3a……クロムゲートバスライン、4……ドレイン電極、5a……クロムドレインバスライン、5b……透明ドレインバスライン、6a……クロム画素電極、6b……透明画素電極、7……SiN_x、8……a-Si:H、9……n^+a-Si:H、10……薄膜電界効果型トランジスタ、14……ソース電極。

代理人　弁理士　　内　原　　晋

第1図

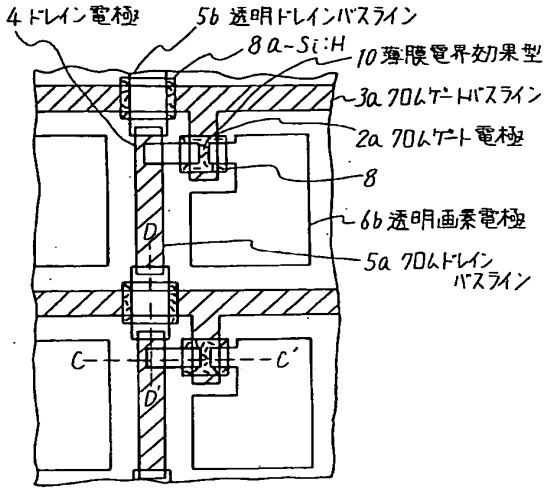


第 1 図

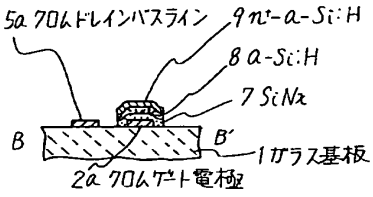


(c)

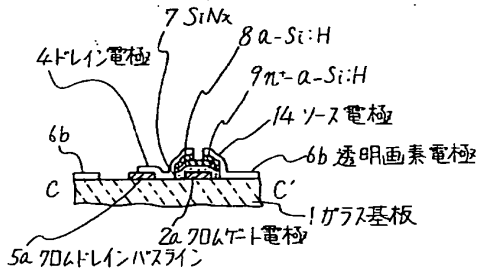
第 1 図



(e)

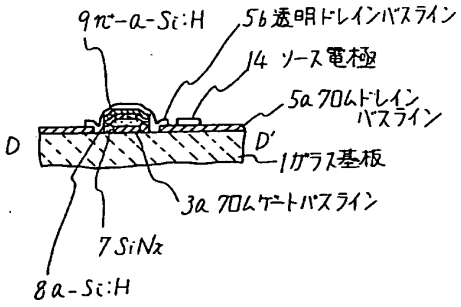


(d)



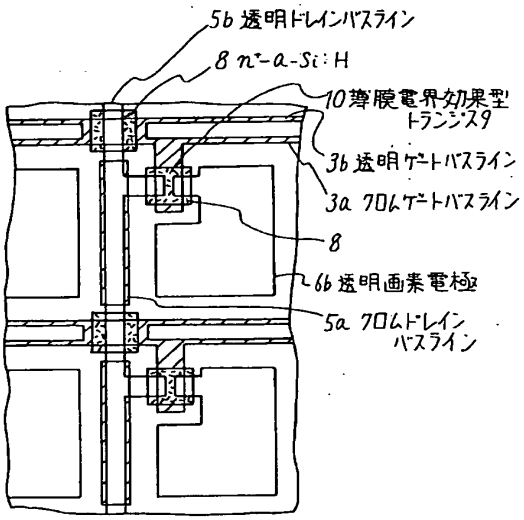
(f)

第 1 図

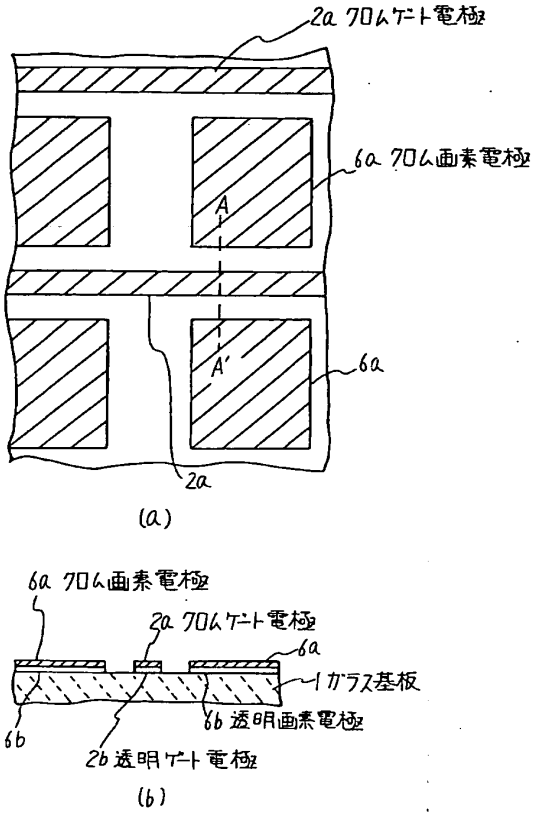


(g)

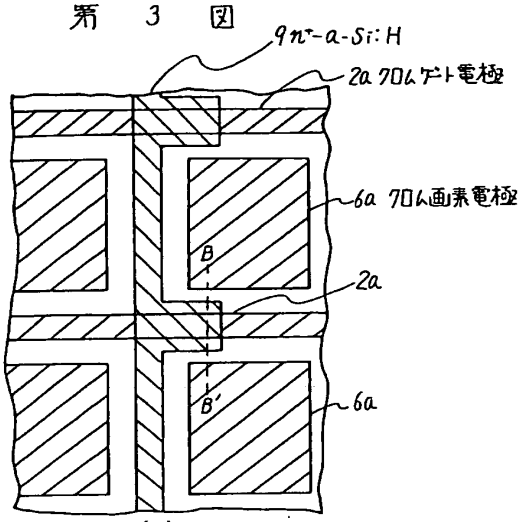
第 2 図


5b 透明ドレインバスライン
8 n⁺-a-Si:H
10 薄膜電界効果型トランジスタ
3b 透明ゲートバスライン
3a クロムゲートバスライン
8
6b 透明画素電極
5a クロムドレインバスライン

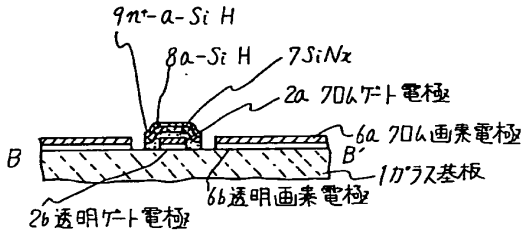
第 3 図


2a クロムゲート電極
6a クロム画素電極
A
A'
6a
2a
(a)
6a クロム画素電極
2a クロムゲート電極
6a
1 ガラス基板
6b
6b 透明画素電極
2b 透明ゲート電極
(b)

第 3 図

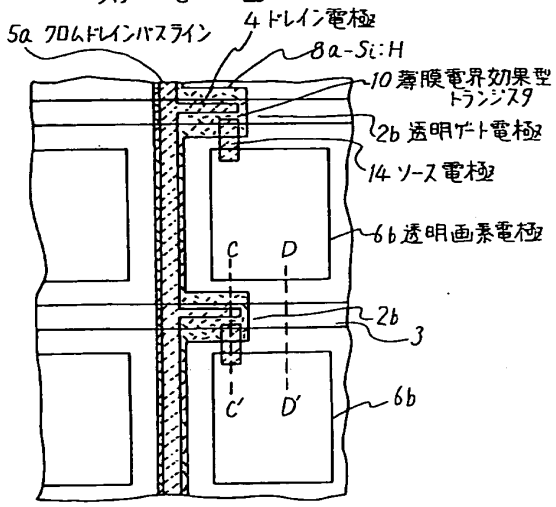


(c)

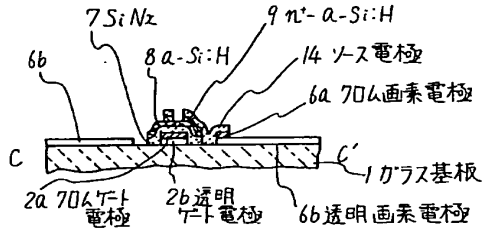


(d)

第 3 図

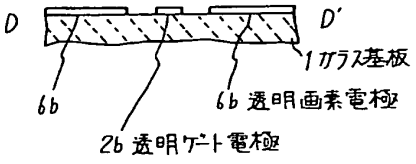


(e)



(f)

第 3 図



(g)

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30

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA	Group Art Unit: 2675
Application No.: 10/299,861	Examiner: E. V. Woods
Filed: November 20, 2002	Docket No.: 114251

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE

CONFIRMATION OF TELEPHONE ELECTION

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Technology Center 2600

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

A telephone requirement for restriction was made in connection with the above-identified patent application on October 25, 2004. The oral Restriction Requirement restricts claims 1-39 under 35 U.S.C. §121 as Group I, claims 1-15 and 34-39, drawn to an active matrix substrate; Group II, claims 16-22, drawn to an electro-optical device; and Group III, claims 23-33 drawn to an electro-optical device.

The undersigned confirms that in response to the telephone requirement, a provisional election was made on October 28, 2004 to prosecute Group I, claims 1-15 and 34-59.

Said provisional election was specifically made with traverse because no basis therefor has been set forth in the written record.

RECEIVED
DEC 13 2004
TC 1700

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Gerhard W. Thielman
Registration No. 43,186

JAO:GWT/gwt

Date: October 29, 2004

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	986	capacitor same portion same (power with supply with line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/02 08:10
L2	160	capacitor same portion with (power near supply near line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/02 08:10
L3	86	capacitor with portion with (power near supply near line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/02 08:11
L4	9	capacitor with portion near (power near supply near line) not seiko.as. not epson.as.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/02 08:11
L5	9	capacitor with portion near (power near supply near line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/02 09:36
L6	182	laser near anneal$5 same recrystal$10 and polysilicon and TFT$	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/02 09:37
L7	7	6 and layer and OLED	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/02 09:38
S1	15870	LDD	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:19
S2	45103	"electro-optical" electrooptical	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:19
S3	3757098	element	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:20

S4	2	"6781155".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:21
S5	2	"6777255".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:20
S6	171475	Sanyo.as.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:20
S7	2	"6277679".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:34
S8	10578	DDD	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:34
S9	254	GDD	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:34
S10	1	S1 and S8 and S9 and "active matrix"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:34
S11	4	S1 and S8 and S9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:16
S12	35797	"active matrix"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:34
S13	1855360	substrate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:34

S14	39920	"first transistor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:16
S15	43582	"second transistor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:16
S16	18297	"third transistor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:16
S17	289209	"pixel" "unit cell" "unit circuit"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:17
S18	694	S14 and S15 and S16 and S17	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:18
S19	4	S14 and S15 and S16 and S18 and "1217"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:27
S20	512	S18 and "pixel"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:27
S21	205	S20 and "active matrix"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:28
S22	27	S21 and S2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:17
S23	151	"21" and (gate same metal same (scan with line))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18

S24	39920	"first transistor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18
S25	43582	"second transistor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18
S26	18297	"third transistor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18
S27	289209	"pixel" "unit cell" "unit circuit"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18
S28	694	S24 and S25 and S26 and S27	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18
S29	512	S28 and "pixel"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18
S30	205	S29 and "active matrix"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18
S31	1	S30 and (gate same metal same (scan with line))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:23
S32	6	S30 and ((gate same metal) and (scan with line))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:30
S33	152	(gate with metal) same ((scan with line) "scan line" "scan lines") same form$7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:31

S34	45103	"electro-optical" electrooptical	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:31
S35	35797	"active matrix"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:31
S36	10	S33 and S34 and S35	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:36

Office Action Summary	Application No.	Applicant(s)	
	10/299,861	MATSUEDA, YOJIRO	
	Examiner	Art Unit	
	Eric V Woods	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) *16-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 34-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-39* are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/19/2004*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *10/19/2004* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-15 and 34-39, drawn to active matrix substrates, classified in class 345, subclass 84.

   II. Claims 16-22, drawn to electro-optical devices and their shape, classified in class 345, subclass 43.

   III. Claims 23-33, drawn to individual electro-optical devices, classified in class 345, subclass 33.

Inventions in Group I and Groups II and III are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because an active matrix substrate can be formed of many different kinds of circuitry, not only the "electro-optical devices" claimed in Group II and described in the specification or the "electro-optical device" claimed in Group III. The subcombinations have separate utility such as pixels in different kinds of display, means for forming and control circuitry of other individual single- and multi-element systems requiring light emission (e.g. semiconductor quantum-dot laser arrays, for instance), and similar applications. The claimed invention (the use of polygonal configurations for organic LED applications) that

is embodied here is tangibly separate from the focus of the other claims, which describe how to form an active matrix substrate with fewer process steps. Claim 16 is an evidence claim – e.g. "An electro-optical device" that has "electro-optical elements" where "said electro-optical elements are formed such that a boundary of the electro-optical elements has, at least, a prescribed curvature." These claims are directed to the properties of individual electro-optical devices, not the substrate as a whole.

Inventions Group II and Group III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group III has separate utility from Group II such as individual pixels and discrete devices, for example discrete light-emitting elements for indicator signals. Invention Group II has separate utility from Group III such as formation of electrodes for microelectronic processes, such as CMOS, MEMS, microfluidics, and other applications. Group II can be practiced without Group III and Group III can be practiced without Group II, and both can be practiced without Group I. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, the search required for Group II is not required for Group III, and the search for Group I is not required for Group III, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

Further, the international search report for this application, which is part of the record for this application, disclosed that during preliminary PCT examination, the claims failed the unity of invention test, and were judged to have dozens of separate, patentable inventions being claimed. For this reason as well, restriction for examination purposes as indicated is proper.

2. During a telephone conversation with applicant's attorney Jerry Thielman on October 28, 2004 at 2:35 p.m., a provisional election was made with traverse to prosecute the invention of Group I, claims 1-15 and 34-39. Affirmation of this election must be made by applicant in replying to this Office action. Claims 16-33 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Fig. 2 does not have element 102, semiconductor layer, described as being present in the specification on pg. 17, lines 15-16. This element must be labeled and shown. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate

prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because in Fig. 3C reference character "C" has been used to designate both the cut line "C-C'" and the holding capacitor (both noted on pg. 19 of the specification). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The disclosure is objected to because of the following informalities:

Page 16 – in the 'Brief Listing of Figures' section – lines 6-7, applicant refers to Fig. 11 on line 6, but then refers to Figs. 10A and 10B on line 7; these should be Figs. 11A and 11B, as they are so listed in the drawing section;

Page 19 – lines 25 and 26, two ratios are given – (SiO_X: $0<x\leq2$) and (Si_3N_X: $0<x\leq4$) – these numbers obviously refer to the refractive or optical index of the material, but x is never explicitly labeled or defined, and so must be correctly defined. Also, the wavelength at which the index is measured and referred to above must be provided, e.g. λ =633nm, 1550nm, etc. must be provided.

Appropriate correction is required.

6. The disclosure is objected to because of the following nonstandard language and use of terminology not standard in the art: applicant states on line 11, pg. 19, that a semiconductor layer consisting of a complex compound such as silicon germanium gallium arsenide ($Si_XGe_YGa_ZAs_Z$; x+y+z=1) can be employed. This statement is objected to by the examiner, as combinations of Group IV and Group III-V material systems are not standard, not known to exist within the art, and are mutually exclusive and incompatible due to problems with defect formation, crystal lattice spacing differences, and various other problems [usually, Group III or V are used as dopants, as acknowledged by applicant on lines 25-27, pg. 19]. Applicant is required to submit documentation proving that such material systems have in fact been integrated successfully and used for this application or to amend the disclosure and cancel that statement.

7. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

8. Claims 8-10 and 14 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim cannot depend from any other multiple dependent claims. See MPEP § 608.01(n).

9. Claims 10 and 12 are objected to because of the following informalities: the terminology "which is closer to said semiconductor layer." The correct, idiomatic English usage would be "that is closer to said semiconductor layer." Appropriate correction is required.

10. Examiner respectfully suggests to applicant that the terminology " ... at least a portion of one scan line ... " that is used in claim 8 and onward be clarified, since in the specification applicant discloses that multiple scan lines would be formed separately and that is not entirely clear from the claim language. Further, the nature of the fabrication techniques used would make it extremely difficult if not impossible to form only one scan line in such a manner. The evaporation and/or sputtering techniques used are fundamentally batch-processing methodologies that would not allow for fabrication of a single line; even with extremely effective shadow masking techniques, such an approach would be both economically and practically infeasible. Applicant discusses these techniques in the specification. Therefore, changing the wording to " ... at least a portion of the plurality of scan lines ... " would be more appropriate and accurate.

Claim Rejections - 35 USC § 112

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 1, 2, 14, and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "said electro-optical elements" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim. Applicant refers to 'electro-optical element of each pixel' preceding that limitation, but it is unclear which electro-optical elements applicant is referring to.

The term "type" in claim 2 is a relative term that renders the claim indefinite. The term "type" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention [see MPEP 2173.02]. Also, the word "type" renders the claim indefinite by definition – see MPEP 2173.02, and *Ex parte Cocenhaver*, 109 USPQ 118 (Bd. App. 1955).

In claim 14 applicant recites "electro-optical elements" in claim 1 and then recites "electro-optical elements" in claim 14 without using "said" or "the" or another modifier. As such and given that claim 14 is a multiple dependent claim, it is unclear which electro-optical elements applicant is referring to.

Claim 15 recites the limitation "said electro-optical elements" in lines 2-3 of that claim. There is insufficient antecedent basis for this claim. Applicant refers to 'electro-optical element of each pixel' preceding that limitation, but it is unclear which electro-optical elements applicant is referring to.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

14. Claims 1,2 and 4 are rejected under 35 U.S.C. 102(e) as being unpatentable over Yamada (US 6,781,155 B1)('Yamada')[valid under 102(e)(2)]. [Reference data provided in column: line format]

As to claim 1,

An active matrix substrate (see Yamada Fig. 1, etc.), comprising peripheral circuits to supply current to an electro-optical element of each pixel corresponding to said electro-optical elements (assumed for purposes of examination to be the element in each pixel, as per 112 objection above), wherein each of said peripheral circuits comprises:

-A holding element (170, Fig. 1, Yamada (1:50-60)) to hold a control voltage;

-A first active element, connected to said holding element, to supply a current based on said control voltage to said electro-optical element (140, Fig. 1, Yamada (1:40-45)); and,

-A second active element, connected to said holding element, which controls the charging and discharging of said holding element (130, Fig. 1, Yamada (1:35-48)); and

-Wherein said active element comprises a structure to prevent leakage currents during shutoff (Yamada 3:5-15, 3:26-40).

Reference Yamada teaches all the limitations of the claim, as shown in Yamada Fig. 1 and discussed in the parenthetical documentation.

As to claim 2,

The active matrix substrate according to claim 1, wherein said second active element is configured as a multi-gate type active element. (Yamada 3:26-40 for multigate structure, and Fig. 1 with the second active element (130) having two gates (both labeled as 131)).

As to claim 4,

An active matrix substrate, comprising a plurality of unit circuits arranged corresponding to intersections of a plurality of data lines and a plurality of scan lines, wherein each of said plurality of unit circuits comprises (see Fig. 1 for illustration of this; 3:53-65; all transistors have number of terminals shown in cited figures)(see Fig. 1 and Fig. 4 that illustrate that the intended use is for a matrix display with multiple unit cells, which *prima facie* must have multiple data and scan lines to support multiple pixels)[note 5:35-45, where Fig. 4 is discussed – lines 51 and 52 are two different signal lines – drain and gate signal lines, thus fulfilling the recited "data line" and "scan line" requirements – scan lines are discussed in 3:62-65]:

-A first transistor, comprising a first control terminal, a first terminal, and a second terminal (140, Fig. 1, Yamada (1:40-45));

-A holding element, connected to said first control terminal, and comprising a first electrode and a second electrode (170, Fig. 1, Yamada (1:50-60)); and,

-A second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal and said fourth terminal being respectively connected to said first terminal and said first electrode (140, Fig. 1, Yamada (1:40-45)); and

-Wherein said second transistor has a multi-gate structure (see Fig. 1, element 130, 2 gates (131) are shown, and Yamada 3:26-40 for multigate structure).

Reference Yamada discloses the entirety of this invention in Fig. 1 with the appropriate connections as described above.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as unpatentable over Yamada in view of Gualandris *et al* (US Re. 35,827)('Gualandris').

As to claim 3,

The active matrix substrate according to claim 1, wherein at least said second active element is a transistor comprising a structure selected from the group consisting of an LDD structure, GDD structure, and DDD structure.

Yamada teaches in Fig. 5 that elements 13 and 13LD – discussed in 6:15-25 – have the LDD structure in the active transistor, and it is discussed as being the active layer *per se*, that is on top of the gate oxide, so it would work for any transistor as

specified there. However, Yamada does not explicitly teach the use of GDD and DDD structures where Gualandris teaches DDD in 1:55-65, GDD in 2:25-30, and LDD in 2:25-30. Gualandris teaches that these are all methods of doping transistors, although one (the LDD) is preferred to work for 'ULSI' applications. Given that 'ULSI' applications at the time the patent was issued were mainly for deep sub-micron processes and that current TFT / liquid crystal display processes have much larger dimensions, e.g. still larger than one micron minimum channel length for silicon-on-glass technology, these techniques would be perfectly valid for use in TFT / silicon-on-glass technology.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix substrates of Yamada with the transistors of Gualandris, since Yamada uses transistors, which *prima facie* have a source and a drain and different drain doping techniques are well-known in the art.

As to claim 5,

An active matrix substrate, comprising a plurality of unit circuits arranged corresponding to intersections of a plurality of data lines and a plurality of scan lines, wherein each of said plurality of unit circuits comprises (see Fig. 1 for illustration of this; 3:53-65; all transistors have number of terminals shown in cited figures))[note 5:35-45, where Fig. 4 is discussed – lines 51 and 52 are two different signal lines – drain and gate signal lines, thus fulfilling the recited "data line" and "scan line" requirements – scan lines are discussed in 3:62-65]:

-A first transistor, comprising a first control terminal, a first terminal, and a second terminal (140, Fig. 1, Yamada (1:40-45));

-A holding element, connected to said first control terminal, and comprising a first electrode and a second electrode (170, Fig. 1, Yamada (1:50-60)); and,

-A second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal and said fourth terminal being respectively connected to said first terminal and said first electrode (140, Fig. 1, Yamada (1:40-45)); and

-Wherein said second transistor has a multi-gate structure (see Fig. 1, element 130, 2 gates (131) are shown, and Yamada 3:26-40 for multigate structure).

Reference Yamada discloses the entirety of this invention in Fig. 1 with the LDD structure as cited above; however, the GDD and DDD structures are not taught by this reference. As discussed in claim 3 above, reference Gualandris discloses these structures for use with transistors and discusses them as being well known in the art in the first two columns. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix substrates of Yamada with the transistors of Gualandris, since Yamada uses transistors, which *prima facie* have a source and a drain and different drain doping techniques are well-known in the art.

17. Claims 6, 7, and 15 are rejected under 35 U.S.C. 103(a) as unpatentable over Yamada in view of Yumoto (US PGPub 2004/0207615)('Yumoto')[valid under 102(e)].

As to claim 6,

The active matrix substrate according to claim 4 or claim 5, further comprising a third transistor comprising a fifth terminal, a sixth terminal, and a third control terminal (third transistor disclosed in Fig. 5 Yumoto in unit pixel cell, 0064),

-Wherein said third control terminal is connected to one scan line among said plurality of scan lines (Yumoto 0064, Fig. 5: TFT4 is connected to scanB and TFT3 is connected to scanA; let TFT3 be the third transistor), and

-Said fifth terminal is connected to one data line among said plurality of data lines (Yumoto 0064, Fig. 5: TFT3 connected to data line).

Reference Yamada teaches all the limitations of the claim except the use of a third transistor and its connections. Reference Yumoto teaches the use of additional transistors with the standard two-transistor TFT cells with the recited connections.

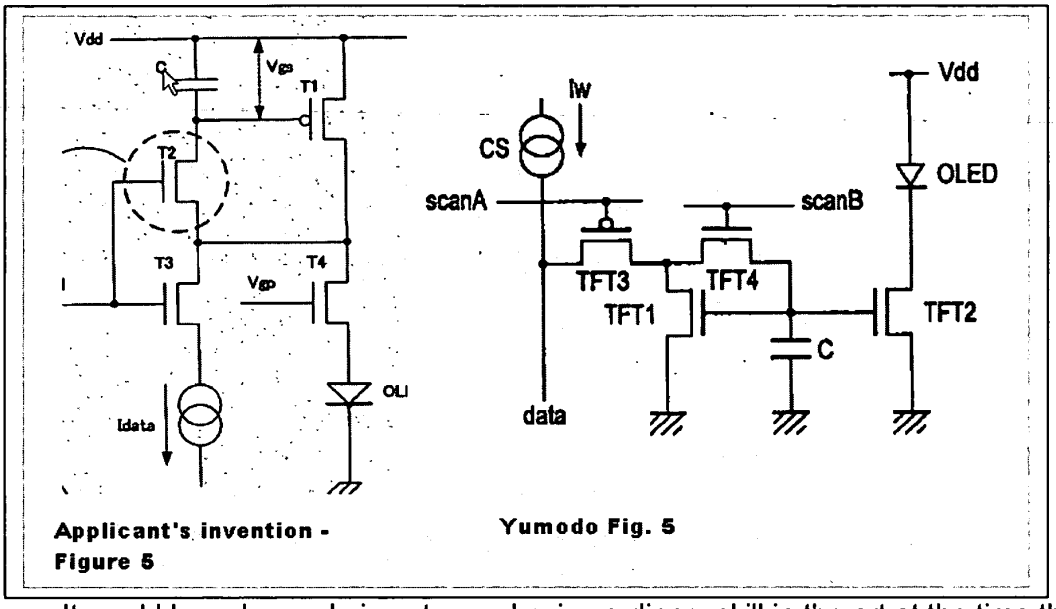
It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the two-transistor cell of Yamada with the multiple transistors of Yumoto, since both are aimed at active matrix panel applications (Yamada Fig. 1, Yumoto Fig. 2, etc.) and to prevent variation due to device parameters in cells similar to that of Yamada (Yumoto 0017).

As to claim 7,

The active matrix substrate according to claim 6, wherein said sixth terminal is connected to said third terminal and to said first terminal.

Reference Yamada does not teach the third transistor. Yumoto discloses in Figure 5 the use of a four-transistor cell. If transistor TFT1 is removed, then the claimed invention is precisely the same as applicant recites in claim 7, with the same connections. As both the multigate variant and the single gate variants of the second transistor are claimed, both will be briefly addressed. If the multigate transistor of Yamada – shown in Fig. 1 and discussed in the rejection to claim 5, is used in place of

TFT4 shown in Yumoto Fig. 5, the result will be exactly the invention recited by applicant. If only one gate is used on the second transistor, then no modification is necessary and again the invention recited in claim 7 is obtained. See images below.



Applicant's invention - Figure 5 **Yumodo Fig. 5**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the two-transistor cell of Yamada with the multiple transistors of Yumoto, since both are aimed at active matrix panel applications (Yamada Fig. 1, Yumoto Fig. 2, etc.) and to prevent variation due to device parameters in cells similar to that of Yamada (Yumoto 0017).

As to claim 15,

An electro-optical device (see Yamada Fig. 1 and 4, etc.), comprising peripheral circuits (see Yamada Fig. 4 and Yumoto Figs. 7 and 11) to supply current to an electro-optical

element of each pixel corresponding to said electro-optical elements, wherein each of said peripheral circuits comprises:

-A light-emission control active element to supply a current to said electro-optical element during a light emission period (function served by recited first-active element; driving circuit can perform both tasks; see also TFT1 in Fig. 13, or in Fig. 12 the alternate structure, with TFT7, as a separate element);

-A holding element to hold a control voltage (170, Fig. 1, Yamada (1:50-60); Capacitor C in any of Figs. 11-15, Yumoto);

-A first active element, a gate terminal of which is connected to said holding element, which supplies a current, based on said control voltage applied to the gate terminal, to said electro-optical element via said light-emission control active element (140, Fig. 1, Yamada (1:40-45); see also TFT1, in Figs. 11 and 12 in Yumoto or TFT5 in Fig. 11);

-A current-controlling active element, which passes data current via said first active element during a selection period (TFT4 or TFT3 in Yumoto Fig. 13); and,

-A second active element, connected between said current-controlling active element and said holding element, which, during said selection period, charges said holding element and causes said control voltage to be stored (130, Fig. 1, Yamada (1:35-48); Yumoto – TFT1); and

-Wherein said active element contains a structure to prevent leakage current during shutoff (Yamada 3:5-15, 3:26-40).

Reference Yamada teaches the general two-transistor structure along with current-controlling elements and structures to prevent leakage current during shutoff.

Reference Yamada does not explicitly teach the other recited details of the claim. Yumoto teaches several different embodiments of peripheral structure for each pixel or unit circuit that contain all the recited elements as identified previously.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the two-transistor cell of Yamada with the multiple transistors of Yumoto, since both are aimed at active matrix panel applications (Yamada Fig. 1, Yumoto Fig. 2, etc.) and to prevent variation due to device parameters in cells similar to that of Yamada (Yumoto 0017). Furthermore, certain functionality that is split off in this claim, e.g. making the light-emission control active element separable from the driving TFT, and splitting off the current-controlling active elements, are obvious and not patentable under *Nerwin v. Erlichman*, 168 USPQ 177, 179 (PTO Bd. Of Int. 1969), since applicant is merely making separable items which are claimed as integral functions in earlier claims (For example, claims 1 and 4 used as evidence claims for this justification). Secondly, if the adjustable argument is made by applicant (that adding elements making those features adjustable), under *In re Stevens*, 101 USPQ 284 (CCPA 1954) that doctrine will not hold, in "that the provision of adjustability, when needed, is not a patentable advance."

18. Claims 8-12, 37, and 39 are rejected under 35 U.S.C. 103(a) as unpatentable over Yamada as applied to claim 4 above, and further in view of Maeda *et al* (US 2002/0008822 A1)('Maeda')[valid under 102(e)](claim 4 operative here – any of the other claims would be subject to the same rejection).

As to claim 8,

The active matrix substrate according to any of claims 4 through 7, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yamada 6:1-45 for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yamada 6:5-25); and

-A gate metal layer comprising said second control terminal (Yamada 6:40-45) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one scan line among said plurality of scan lines is formed in said gate metal layer (Maeda 0121).

Reference Yamada teaches all the limitations of this claim except the formation of a scan line in the gate metal layer. Reference Maeda teaches the formation of scan lines and gate electrodes in the same metal film layer for TFT / LCD monitor fabrication (e.g. 0162, 0121). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yamada with the single metal layer of Maeda since Maeda performs in one step what Yamada does in several steps (note Yamada fabrication process in 6:1-67 and 7:1-50), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination, e.g. common sense is sufficient to justify the combination. See also *In re Karlson*, 136 USPQ 184 (CCPA 1963), for the doctrine that eliminating components is an obvious expedient – in this, eliminating fabrication steps.

As to claim 9,

The active matrix substrate according to any of claims 4 through 7, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yamada 6:1-45 for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yamada 6:5-25); and

-A gate metal layer comprising said second control terminal (Yamada 6:40-45) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in said gate metal layer (Maeda 0121 and 0113 and 0125).

Reference Yamada teaches all the limitations of this claim except the formation of a data line in the gate metal layer. Reference Maeda teaches the formation of data lines and source and drain electrodes in the same metal film layer for TFT / LCD monitor fabrication (e.g. 0113, 0125). It would be *prima facie* obvious to choose to form gate electrodes and data lines simultaneously rather than gate electrodes and scan lines, for example. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yamada with the single metal layer of Maeda since Maeda performs in one step what Yamada does in several steps (note Yamada fabrication process in 6:1-67 and 7:1-50), which is *prima facie*

more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

As to claim 10,

The active matrix substrate according to any of claims 4 through 7, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yamada 6:1-45 for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yamada 6:5-25); and

-A gate metal layer comprising said second control terminal (Yamada 6:40-45) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-A source metal layer comprising a source electrode or drain electrode connected to the source or drain of said second transistor (Maeda 0113, 0125); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in the layer (Maeda 0121 and 0113 and 0125), among said source metal layer and said gate metal layer, which is closer to said semiconductor layer.

References Maeda and Yamada teach all the limitations of this claim, and this is merely a recitation of the dual limitations of claims 8 and 9 above. As such, the combination and motivation from claim 8 is used here and no further comment is necessary, as this claim is only a nominal variation of the parent.

As to claim 11,

An active matrix substrate, comprising a circuit with transistors, scan lines, and data lines, and having a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yamada 6:1-45 for example)[Yamada established to have transistors (1:10-15), scan lines (3:60-65), and signal lines (the data lines of applicant)(3:60-65)];

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yamada 6:5-25); and

-A gate metal layer having gate terminals of said transistors formed therein (Yamada 6:40-45); and

-Wherein at least one portion of either said scan lines or said data lines, or both, is formed in said gate metal layer (Maeda 0121 and 0113 and 0125).

References Maeda and Yamada teach all the limitations of this claim, and this is merely a recitation of the dual limitations of claims 8 and 9 above, e.g. forming the scan or data lines in the gate metal layer, and clearly in claim 8 the formation of scan lines in the gate metal, and thusly for the data lines in claim 9. As such, the combination and motivation from claim 8 is used here and no further comment is necessary, as this claim is only a nominal variation of the parent, e.g. the combination is obvious under *In re Karlson* and common sense as recited above. Further, in view of *In re Hubbell*, 76 USPQ 105 (CCPA 1947) and *In re Japikse*, 86 USPQ 70 (CCPA 1950), all applicant is doing is moving parts (fabrication steps for portions of the display) around among locations in the fabrication process. Reference Maeda very clearly teaches that scan

and data lines can be formed in metal layers wherever in the fabrication process such a metal layer is deposited if it would be favorable to do so.

As to claim 12,

An active matrix substrate, comprising a circuit with transistors, scan lines, and data lines, and having a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yamada 6:1-45 for example)[Yamada established to have transistors (1:10-15), scan lines (3:60-65), and signal lines (the data lines of applicant)(3:60-65)];

Wherein said plurality of layers comprise:

-A semiconductor layer, in which a semiconductor film constituting transistors is formed (Yamada 6:5-25); and

-A gate metal layer having gate terminals of said transistors formed therein (Yamada 6:40-45); and

-A source metal layer in which source electrodes or gate electrodes connected to sources or drains of said transistors are formed; and

-Wherein at least one portion of either said scan lines or said data lines, or both, is formed in the layer, among said gate metal layer and said source metal layer, which is closer to said semiconductor layer (Maeda 0121 and 0113 and 0125).

References Maeda and Yamada teach all the limitations of this claim, and this is merely a restating of the limitations of claim 11 with a bit of shuffling. These variations have been covered exhaustively in the rejections for claims 8-11 as above. The

combination and motivation are that of claim 11, as this is only a nominal variation and the shifting of parts as attributed above in claim 11.

As to claim 37,

An active matrix substrate, comprising unit circuits comprising transistors, arranged corresponding to intersections of data lines and scan lines (Yamada Figs. 1 and 4 for example) wherein

-A semiconductor layer constituting such transistors is formed in a semiconductor layer (Yamada 6:5-25);

-Either said scan lines or said data lines are formed in a first conducting layer at the intersections of said scan lines and said data lines (Maeda 0113, 0121, and 0125); and,

-A portion of said scan lines and said data lines outside said intersections are formed in a second conducting layer (Maeda 0113, 0121, and 0125).

Reference Yamada does not explicitly teach the formation of scan or data lines formed in a conducting layer at the intersections of such lines. Reference Maeda describes forming gate metal and scan lines, etc. simultaneously. As such, the scan lines would be formed everywhere not masked with a shadow mask, e.g. both in the scan lines and in the intersections. No matter what portions of the lines are claimed, any such configuration could be made using shadow masking and formed using either evaporation or sputtering. Any set of contacts could be created using correctly etched contact holes; electrically contiguous metal formed in the same layer is *prima facie* the same from an electrical and an engineering perspective. Further, forming scan lines or data lines or portions thereof (as claimed) in the same layer as other things would

simply be making a component integral by eliminating unnecessary metal, and under *In re Larson*, 144 USPQ 347 (CCPA 1965), making a component integral is obvious and not patentable. Therefore, under either methodology, the recited limitations of the claim have been met.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yamada with the single metal layer of Maeda since Maeda performs in one step what Yamada does in several steps (note Yamada fabrication process in 6:1-67 and 7:1-50), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

As to claim 39,

An electro-optical device, comprising electro-optical elements corresponding to intersections of scan lines and data lines (Yamada Figs. 1 and 4, element 60 for example (OLED)), wherein:

-A pair of electrodes is provided to supply power to electro-optical elements (Maeda Fig. 11C, elements 19 and 15 are opposing and pixel electrodes (see 0006-0008));

-At the intersections of said scan lines and said data lines, either said scan lines or said data lines are formed in a first conducting layer (Maeda 0113, 0118, 0121, 0125 – again, gate metal as discussed in rejections to claims 8-12);

-Portions of said scan lines and said data lines outside said intersections are formed in a second conducting layer (source metal layer, 0113, 0118, 0121, 0125 as discussed in rejections to claims 8-12); and,

-Said second conducting layer is positioned at a greater distance than said first conducting layer from one of said pair of electrodes (design choice issue, see Maeda Fig. 11C).

Reference Yamada does not recite details of the fabrication process claimed above. Reference Maeda teaches the fabrication of such substrates and teaches contact holes (0044, 0047). Logically, such contact holes would fill on conducting layer deposition, thus meeting the recited limitation concerning intersections of data and scan lines. The positioning of a layer or its size is *prima facie* obvious and is not patentable (*In re Japikse* for order of parts and further under *In re Reese*, anyone of ordinary skill in the art would know that there would be an optimal spacing of electrodes from each other to minimize cross-talk that would also occupy the minimum aspect ratio required on the shadow mask).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yamada with the single metal layer of Maeda since Maeda performs in one step what Yamada does in several steps (note Yamada fabrication process in 6:1-67 and 7:1-50), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

19. Claim 13 is rejected under 35 U.S.C. 103(a) as unpatentable over Yamada in view of Maeda as applied to claims 11 and 12 above, and further in view of Gualandris.

As to claim 13,

The active matrix substrate according to claim 11 or claim 12, wherein said unit circuit comprises:

-A first transistor, comprising a first control terminal, a first terminal, and a second terminal (140, Fig. 1, Yamada (1:40-45));

-A holding element, connected to said first control terminal, and comprising a first electrode and a second electrode (170, Fig. 1, Yamada (1:50-60)); and,

-A second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal and said fourth terminal being respectively connected to said first terminal and said first electrode (140, Fig. 1, Yamada (1:40-45)); and

-Wherein said second transistor is a transistor comprising a structure selected from the group consisting of an LDD structure, GDD structure, and DDD structure.

Yamada teaches in Fig. 5 that elements 13 and 13LD – discussed in 6:15-25 – have the LDD structure in the active transistor, and it is discussed as being the active layer *per se*, that is on top of the gate oxide, so it would work for any transistor as specified there. However, Yamada does not explicitly teach the use of GDD and DDD structures where Gualandris teaches DDD in 1:55-65, GDD in 2:25-30, and LDD in 2:25-30. Gualandris teaches that these are all methods of doping transistors, although one (the LDD) is preferred to work for 'ULSI' applications. Given that 'ULSI' applications at the time the patent was issued were mainly for deep sub-micron processes and that current TFT / liquid crystal display processes have much larger dimensions, e.g. still larger than one micron minimum channel length for silicon-on-glass technology, these techniques would be perfectly valid for use in TFT / silicon-on-glass technology.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix substrates of Yamada and Maeda with the transistors of Gualandris, since Yamada [and Maeda] uses silicon transistors, which *prima facie* have a source and a drain and different drain doping techniques are well-known in the art. Further, since only the primary reference is utilized (e.g. no Maeda), a separate motivation is not required for Maeda and Yamada. Further, the gates in Gualandris utilize (5:10-20) a silicon layer as their base, as the substrates for Maeda and Yamada are silicon as well.

As to claim 14,

An electro-optical device comprising an active matrix substrate according to any of the claims 1 through 13, and electro-optical elements. (Yamada Fig. 4, element 60 – an OLED, which is *prima facie* an electro-optical device with an anode 61 (see 5:35-60)). Since only the primary reference is used, no motivation or combination is necessary. That of claim 13 is used if were to be necessary for this rejection.

20. Claim 34 is rejected under 35 U.S.C. 103(a) as unpatentable over Yamada in view of Koyama (US PGPub 2001/0040565 A1)('Koyama')(valid under 102(e)).

As to claim 34,

An active matrix substrate, comprising pixel electrodes and path arranged corresponding to intersections of data lines and scan lines (Yamada Figs. 1 and 4; Koyama Fig. 1), wherein:

-Said pixel electrodes are connected to a power supply line via one or more transistors (Koyama, element 9106, Fig. 1 (0055); Yamada element 140, Fig. 1, connected to 150 power supply line);

-A holding element is provided, connected to a gate of said one or more transistors (Yamada capacitor C, element 170, Fig. 1; Koyama, element 9107 (0055)); and

-A first electrode constituting said holding element is connected to said power supply line (*prima facie* the capacitor of Koyama that is connected to the power supply line, would constitute two electrodes (capacitors have two electrodes by definition)).

Reference Yamada teaches all the limitations except a capacitor directly connected to the power supply line. Reference Koyama teaches the use of a capacitor directly connected to the power supply line. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the circuitry of Yamada with the capacitor of Koyama, as the structures claim are almost the same (e.g. multi-gate (see Fig. 1 and 0055-0057)) and the addition of the capacitor makes it easier to test for defects in manufacturing (see 0034-0037). Also, the position of the relevant capacitor is a design choice issue (positioning of parts, *In re Japikse* as discussed in other portions of the rejection).

21. Claims 35 and 36 are rejected under 35 U.S.C. 103(a) as unpatentable over Yamada in view of Koyama as applied to claim 34 above, and further in view of Maeda [Even though this is an independent claim, the variation is extremely nominal].

As to claim 35,

-An active matrix substrate, comprising pixel electrodes and path arranged corresponding to intersections of data lines and scan lines (Yamada Figs. 1 and 4; Koyama Fig. 1), wherein:

-Said pixel electrodes are connected to a power supply line via one or more transistor (Koyama, element 9106, Fig. 1 (0055); Yamada element 140, Fig. 1, connected to 150 power supply line);

-A holding element is provided, connected to a gate of said one or more transistor (Yamada capacitor C, element 170, Fig. 1; Koyama, element 9107 (0055)); and

-A first electrode constituting said holding element is a portion of said power supply line (*prima facie* the capacitor of Koyama that is connected to the power supply line, would constitute two electrodes (capacitors have two electrodes by definition) and (Maeda 0121 and 0113 and 0125).

References Yamada and Koyama teach all of the limitations except explicitly stating that such an electrode could be a portion of said power supply line. In the rejections to claims 8-12, the formation of data and scan lines in either gate metal or source metal layers is discussed and the formation of such lines in those layers is claimed (those arguments are incorporated here by reference). Reference Maeda teaches the formation of multiple sets of lines (e.g. gates, scan lines, etc. (Maeda 0121 and 0113 and 0125) simultaneously during metal deposition steps. It would be obvious to combine power supply line formation with the deposition of the electrodes to form the capacitors (in TFT processes, capacitors are often MIM (metal-insulator-metal)). As

such, the power supply line would in fact be the electrode of such a capacitor, as they were formed simultaneously and are electrically contiguous.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the TFT circuitry of Yamada and Koyama with the single metal layer of Maeda since Maeda performs in one step what Yamada does in several steps (note Yamada fabrication process in 6:1-67 and 7:1-50), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination, e.g. common sense is sufficient to justify the combination. See also *In re Karlson*, 136 USPQ 184 (CCPA 1963), for the doctrine that eliminating components is an obvious expedient – in this, eliminating fabrication steps.

As to claim 36,

The active matrix substrate of claim 34 or claim 35, wherein a second electrode constituting said holding element is the gate of one or more said transistors.

References Yamada and Koyama do not explicitly teach this limitation. Reference Maeda describes forming gate metal and scan lines, etc. simultaneously. As such, the top electrode of the capacitor would be simultaneously formed with the gate. Electrically contiguous metal formed in the same layer is *prima facie* the same from an electrical and an engineering perspective. Further, making the capacitor top electrode and the gate electrode the same thing (as claimed) would simply be making a component integral by eliminating unnecessary metal, and under *In re Larson*, 144 USPQ 347 (CCPA 1965), making a component integral is obvious and not patentable. Therefore, under either methodology, the recited limitations of the claim have been met.

This claim is only a nominal variation of the parent (e.g. claim 35) and as such the rejection uses the same combination and motivation without need to repeat it.

21. Claim 38 is rejected over Yamada in view of Maeda as applied to claim 37, and further in view of Tanaka (US PGPub 2001/0026835 A1)('Tanaka')(valid under 102(e)).

As to claim 38,

The active matrix substrate according to claim 37, wherein said second conducting layer is positioned between said first conducting layer and said semiconductor layer.

Reference Yamada does not explicitly teach this limitation. In Fig. 10B, Maeda shows that the bottom gate – element 56, which is metal (a niobium alloy) is put down first, then various insulating materials, then element 13 (source and drain electrodes) are formed on the same level and slightly covering the semiconductor layer 54. Under the doctrine of *In re Japikse*, switching the two layers would be *prima facie* obvious, and only minor alternations in the shadow masks for the process would be necessary (additive vs. subtractive processing in semiconductors, for example, switching the process would not be difficult for one of ordinary skill in the semiconductor / TFT art). Again, given that Maeda teaches many different embodiments (see Figs. 10-13, etc.), such a switch would be a design choice issue, and it would allow low-temperature processing of the substrate throughout the process, particularly allowing for newer techniques such as laser annealing and recrystallization of the semiconductor layer taught by Tanaka, and treatment of the semiconductor layer towards the end of processing.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the TFT circuits of Yamada and Maeda with the laser annealing processing of polysilicon for TFT applications of Tanaka (see 0002-0015), as both Yamada (2:61-67) and Maeda (0008, 0121, etc.) utilize polysilicon as the semiconductor material, and laser annealing is now a well-known, standard process in the art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric V Woods whose telephone number is 703-305-0263. The examiner can normally be reached on M-F 7:30-5:00 alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on 703-305-4713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JEFFERY BRIER
PRIMARY EXAMINER

Eric Woods 11/2/2004

Notice of References Cited	Application/Control No. 10/299,861	Applicant(s)/Patent Under Reexamination MATSUEDA, YOJIRO	
	Examiner Eric V Woods	Art Unit 2672	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-RE35,827	06-1998	Gualandris et al.	257/285
	B	US-6,781,155 B1	08-2004	Yamada, Tsutomu	257/72
	C	US-2001/0026835	10-2001	Tanaka, Koichiro	427/96
	D	US-2001/0040565	11-2001	Koyama, Jun	345/204
	E	US-2002/0008822	01-2002	Maeda, Akitoshi	349/139
	F	US-2004/0207615	10-2004	Yumoto, Akira	345/211
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

PE JC177 JUN 2 9 2004 PATENT & TRADEMARK OFFICE

Sheet 1 of 1

Form PTO-1449 (REV. 8-83)	U.S. Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 114251	APPLICATION NO. 10/299,861
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT Yojiro MATSUEDA	
		FILING DATE November 20, 2002	GROUP 1775

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS

RECEIVED JUL 0 2 2004 TC 1700

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
EW	1)	WO 98/36407 w/ abst	08/20/1998	WIPO		
EW	2)	JP A 2000-214800 w/ abst. & trans	08/04/2000	JAPAN		
EW	3)	JP A 2001-13893 w/ abst. & trans	01/19/2001	JAPAN		
EW	4)	JP A 2000-284727 w/ abst. & trans	10/13/2000	JAPAN		
EW	5)	JP A 11-65487 w/ abst. & trans	03/05/1999	JAPAN		
EW	6)	JP A 1-101519	04/19/1989	JAPAN		
EW	7)	JP A 2-170135	06/29/1990	JAPAN		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED
[signature]	10/28/2004

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Examiner-Initiated Interview Summary	Application No.	Applicant(s)	
	10/299,861	MATSUEDA, YOJIRO	
	Examiner	Art Unit	
	Eric V Woods	2672	

All Participants:

(1) *Eric V Woods*.

(2) *JerryThielman*.

Status of Application: *Pending*

(3) _____.

(4) _____.

Date of Interview: *28 October 2004*

Time: *2:35 p.m.*

Type of Interview:
☒ Telephonic
☐ Video Conference
☐ Personal (Copy given to: ☐ Applicant ☐ Applicant's representative)

Exhibit Shown or Demonstrated: ☐ Yes ☒ No
If Yes, provide a brief description:

Part I.

Rejection(s) discussed:
N/A - Restriction / election only

Claims discussed:
1-39

Prior art documents discussed:
N/A

Part II.

SUBSTANCE OF INTERVIEW DESCRIBING THE GENERAL NATURE OF WHAT WAS DISCUSSED:
See Continuation Sheet

Part III.

☐ It is not necessary for applicant to provide a separate record of the substance of the interview, since the interview directly resulted in the allowance of the application. The examiner will provide a written summary of the substance of the interview in the Notice of Allowability.

☒ It is not necessary for applicant to provide a separate record of the substance of the interview, since the interview did not result in resolution of all issues. A brief summary by the examiner appears in Part II above.

(Examiner/SPE Signature) (Applicant/Applicant's Representative Signature – if appropriate)

Continuation of Substance of Interview including description of the general nature of what was discussed: Applicant's attorney of record stated that applicant is electing Group I, that is claims 1-15 and 34-39, with traverse. This was in response to a phone call from examiner to applicant's attorney of record informing him of a restriction requirement with three groups of claims. .

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/299,861	11/20/2002	Yojiro Matsueda	114251	5800

25944 7590 01/13/2005

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
WOODS, ERIC V	
ART UNIT	**PAPER NUMBER**
2672	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/299,861	MATSUEDA, YOJIRO	
	Examiner	Art Unit	
	Eric V Woods	2672	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) *16-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 34-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-39* are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/19/2004*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *10/19/2004*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-15 and 34-39, drawn to active matrix substrates, classified in class 345, subclass 84.

   II. Claims 16-22, drawn to electro-optical devices and their shape, classified in class 345, subclass 43.

   III. Claims 23-33, drawn to individual electro-optical devices, classified in class 345, subclass 33.

Inventions in Group I and Groups II and III are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because an active matrix substrate can be formed of many different kinds of circuitry, not only the "electro-optical devices" claimed in Group II and described in the specification or the "electro-optical device" claimed in Group III. The subcombinations have separate utility such as pixels in different kinds of display, means for forming and control circuitry of other individual single- and multi-element systems requiring light emission (e.g. semiconductor quantum-dot laser arrays, for instance), and similar applications. The claimed invention (the use of polygonal configurations for organic LED applications) that

is embodied here is tangibly separate from the focus of the other claims, which describe how to form an active matrix substrate with fewer process steps. Claim 16 is an evidence claim – e.g. "An electro-optical device" that has "electro-optical elements" where "said electro-optical elements are formed such that a boundary of the electro-optical elements has, at least, a prescribed curvature." These claims are directed to the properties of individual electro-optical devices, not the substrate as a whole.

Inventions Group II and Group III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group III has separate utility from Group II such as individual pixels and discrete devices, for example discrete light-emitting elements for indicator signals. Invention Group II has separate utility from Group III such as formation of electrodes for microelectronic processes, such as CMOS, MEMS, microfluidics, and other applications. Group II can be practiced without Group III and Group III can be practiced without Group II, and both can be practiced without Group I. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, the search required for Group II is not required for Group III, and the search for Group I is not required for Group III, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

Further, the international search report for this application, which is part of the record for this application, disclosed that during preliminary PCT examination, the claims failed the unity of invention test, and were judged to have dozens of separate, patentable inventions being claimed. For this reason as well, restriction for examination purposes as indicated is proper.

2. During a telephone conversation with applicant's attorney Jerry Thielman on October 28, 2004 at 2:35 p.m., a provisional election was made with traverse to prosecute the invention of Group I, claims 1-15 and 34-39. Affirmation of this election must be made by applicant in replying to this Office action. Claims 16-33 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Fig. 2 does not have element 102, semiconductor layer, described as being present in the specification on pg. 17, lines 15-16. This element must be labeled and shown. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate

prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because in Fig. 3C reference character "C" has been used to designate both the cut line "C-C'" and the holding capacitor (both noted on pg. 19 of the specification). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The disclosure is objected to because of the following informalities:

Page 16 – in the 'Brief Listing of Figures' section – lines 6-7, applicant refers to Fig. 11 on line 6, but then refers to Figs. 10A and 10B on line 7; these should be Figs. 11A and 11B, as they are so listed in the drawing section;

Page 19 – lines 25 and 26, two ratios are given – (SiO_X: $0<x\leq2$) and (Si_3N_X: $0<x\leq4$) – these numbers obviously refer to the refractive or optical index of the material, but x is never explicitly labeled or defined, and so must be correctly defined. Also, the wavelength at which the index is measured and referred to above must be provided, e.g. λ =633nm, 1550nm, etc. must be provided.

Appropriate correction is required.

6. The disclosure is objected to because of the following nonstandard language and use of terminology not standard in the art: applicant states on line 11, pg. 19, that a semiconductor layer consisting of a complex compound such as silicon germanium gallium arsenide ($Si_XGe_YGa_ZAs_Z$; x+y+z=1) can be employed. This statement is objected to by the examiner, as combinations of Group IV and Group III-V material systems are not standard, not known to exist within the art, and are mutually exclusive and incompatible due to problems with defect formation, crystal lattice spacing differences, and various other problems [usually, Group III or V are used as dopants, as acknowledged by applicant on lines 25-27, pg. 19]. Applicant is required to submit documentation proving that such material systems have in fact been integrated successfully and used for this application or to amend the disclosure and cancel that statement.

7. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

8. Claims 8-10 and 14 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim cannot depend from any other multiple dependent claims. See MPEP § 608.01(n).

9. Claims 10 and 12 are objected to because of the following informalities: the terminology "which is closer to said semiconductor layer." The correct, idiomatic English usage would be "that is closer to said semiconductor layer." Appropriate correction is required.

10. Examiner respectfully suggests to applicant that the terminology " ... at least a portion of one scan line ... " that is used in claim 8 and onward be clarified, since in the specification applicant discloses that multiple scan lines would be formed separately and that is not entirely clear from the claim language. Further, the nature of the fabrication techniques used would make it extremely difficult if not impossible to form only one scan line in such a manner. The evaporation and/or sputtering techniques used are fundamentally batch-processing methodologies that would not allow for fabrication of a single line; even with extremely effective shadow masking techniques, such an approach would be both economically and practically infeasible. Applicant discusses these techniques in the specification. Therefore, changing the wording to " ... at least a portion of the plurality of scan lines ... " would be more appropriate and accurate.

Claim Rejections - 35 USC § 112

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 1, 2, 14, and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "said electro-optical elements" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim. Applicant refers to 'electro-optical element of each pixel' preceding that limitation, but it is unclear which electro-optical elements applicant is referring to.

The term "type" in claim 2 is a relative term that renders the claim indefinite. The term "type" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention [see MPEP 2173.02]. Also, the word "type" renders the claim indefinite by definition – see MPEP 2173.02, and *Ex parte Cocenhaver*, 109 USPQ 118 (Bd. App. 1955).

In claim 14 applicant recites "electro-optical elements" in claim 1 and then recites "electro-optical elements" in claim 14 without using "said" or "the" or another modifier. As such and given that claim 14 is a multiple dependent claim, it is unclear which electro-optical elements applicant is referring to.

Claim 15 recites the limitation "said electro-optical elements" in lines 2-3 of that claim. There is insufficient antecedent basis for this claim. Applicant refers to 'electro-optical element of each pixel' preceding that limitation, but it is unclear which electro-optical elements applicant is referring to.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

14. Claims 1,2 and 4 are rejected under 35 U.S.C. 102(e) as being unpatentable over Yamada (US 6,781,155 B1)('Yamada')[valid under 102(e)(2)]. [Reference data provided in column: line format]

As to claim 1,

An active matrix substrate (see Yamada Fig. 1, etc.), comprising peripheral circuits to supply current to an electro-optical element of each pixel corresponding to said electro-optical elements (assumed for purposes of examination to be the element in each pixel, as per 112 objection above), wherein each of said peripheral circuits comprises:

-A holding element (170, Fig. 1, Yamada (1:50-60)) to hold a control voltage;

-A first active element, connected to said holding element, to supply a current based on said control voltage to said electro-optical element (140, Fig. 1, Yamada (1:40-45)); and,

-A second active element, connected to said holding element, which controls the charging and discharging of said holding element (130, Fig. 1, Yamada (1:35-48)); and

-Wherein said active element comprises a structure to prevent leakage currents during shutoff (Yamada 3:5-15, 3:26-40).

Reference Yamada teaches all the limitations of the claim, as shown in Yamada Fig. 1 and discussed in the parenthetical documentation.

As to claim 2,

The active matrix substrate according to claim 1, wherein said second active element is configured as a multi-gate type active element. (Yamada 3:26-40 for multigate structure, and Fig. 1 with the second active element (130) having two gates (both labeled as 131)).

As to claim 4,

An active matrix substrate, comprising a plurality of unit circuits arranged corresponding to intersections of a plurality of data lines and a plurality of scan lines, wherein each of said plurality of unit circuits comprises (see Fig. 1 for illustration of this; 3:53-65; all transistors have number of terminals shown in cited figures)(see Fig. 1 and Fig. 4 that illustrate that the intended use is for a matrix display with multiple unit cells, which *prima facie* must have multiple data and scan lines to support multiple pixels)[note 5:35-45, where Fig. 4 is discussed – lines 51 and 52 are two different signal lines – drain and gate signal lines, thus fulfilling the recited "data line" and "scan line" requirements – scan lines are discussed in 3:62-65]:

-A first transistor, comprising a first control terminal, a first terminal, and a second terminal (140, Fig. 1, Yamada (1:40-45));

-A holding element, connected to said first control terminal, and comprising a first electrode and a second electrode (170, Fig. 1, Yamada (1:50-60)); and,

-A second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal and said fourth terminal being respectively connected to said first terminal and said first electrode (140, Fig. 1, Yamada (1:40-45)); and

-Wherein said second transistor has a multi-gate structure (see Fig. 1, element 130, 2 gates (131) are shown, and Yamada 3:26-40 for multigate structure).

Reference Yamada discloses the entirety of this invention in Fig. 1 with the appropriate connections as described above.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as unpatentable over Yamada in view of Gualandris *et al* (US Re. 35,827)('Gualandris').

As to claim 3,

The active matrix substrate according to claim 1, wherein at least said second active element is a transistor comprising a structure selected from the group consisting of an LDD structure, GDD structure, and DDD structure.

Yamada teaches in Fig. 5 that elements 13 and 13LD – discussed in 6:15-25 – have the LDD structure in the active transistor, and it is discussed as being the active layer *per se*, that is on top of the gate oxide, so it would work for any transistor as

specified there. However, Yamada does not explicitly teach the use of GDD and DDD structures where Gualandris teaches DDD in 1:55-65, GDD in 2:25-30, and LDD in 2:25-30. Gualandris teaches that these are all methods of doping transistors, although one (the LDD) is preferred to work for 'ULSI' applications. Given that 'ULSI' applications at the time the patent was issued were mainly for deep sub-micron processes and that current TFT / liquid crystal display processes have much larger dimensions, e.g. still larger than one micron minimum channel length for silicon-on-glass technology, these techniques would be perfectly valid for use in TFT / silicon-on-glass technology.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix substrates of Yamada with the transistors of Gualandris, since Yamada uses transistors, which *prima facie* have a source and a drain and different drain doping techniques are well-known in the art.

As to claim 5,

An active matrix substrate, comprising a plurality of unit circuits arranged corresponding to intersections of a plurality of data lines and a plurality of scan lines, wherein each of said plurality of unit circuits comprises (see Fig. 1 for illustration of this; 3:53-65; all transistors have number of terminals shown in cited figures))[note 5:35-45, where Fig. 4 is discussed – lines 51 and 52 are two different signal lines – drain and gate signal lines, thus fulfilling the recited "data line" and "scan line" requirements – scan lines are discussed in 3:62-65]:

-A first transistor, comprising a first control terminal, a first terminal, and a second terminal (140, Fig. 1, Yamada (1:40-45));

-A holding element, connected to said first control terminal, and comprising a first electrode and a second electrode (170, Fig. 1, Yamada (1:50-60)); and,

-A second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal and said fourth terminal being respectively connected to said first terminal and said first electrode (140, Fig. 1, Yamada (1:40-45)); and

-Wherein said second transistor has a multi-gate structure (see Fig. 1, element 130, 2 gates (131) are shown, and Yamada 3:26-40 for multigate structure).

Reference Yamada discloses the entirety of this invention in Fig. 1 with the LDD structure as cited above; however, the GDD and DDD structures are not taught by this reference. As discussed in claim 3 above, reference Gualandris discloses these structures for use with transistors and discusses them as being well known in the art in the first two columns. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix substrates of Yamada with the transistors of Gualandris, since Yamada uses transistors, which *prima facie* have a source and a drain and different drain doping techniques are well-known in the art.

17. Claims 6, 7, and 15 are rejected under 35 U.S.C. 103(a) as unpatentable over Yamada in view of Yumoto (US PGPub 2004/0207615)('Yumoto')[valid under 102(e)].

As to claim 6,

The active matrix substrate according to claim 4 or claim 5, further comprising a third transistor comprising a fifth terminal, a sixth terminal, and a third control terminal (third transistor disclosed in Fig. 5 Yumoto in unit pixel cell, 0064),

-Wherein said third control terminal is connected to one scan line among said plurality of scan lines (Yumoto 0064, Fig. 5: TFT4 is connected to scanB and TFT3 is connected to scanA; let TFT3 be the third transistor), and

-Said fifth terminal is connected to one data line among said plurality of data lines (Yumoto 0064, Fig. 5: TFT3 connected to data line).

Reference Yamada teaches all the limitations of the claim except the use of a third transistor and its connections. Reference Yumoto teaches the use of additional transistors with the standard two-transistor TFT cells with the recited connections.

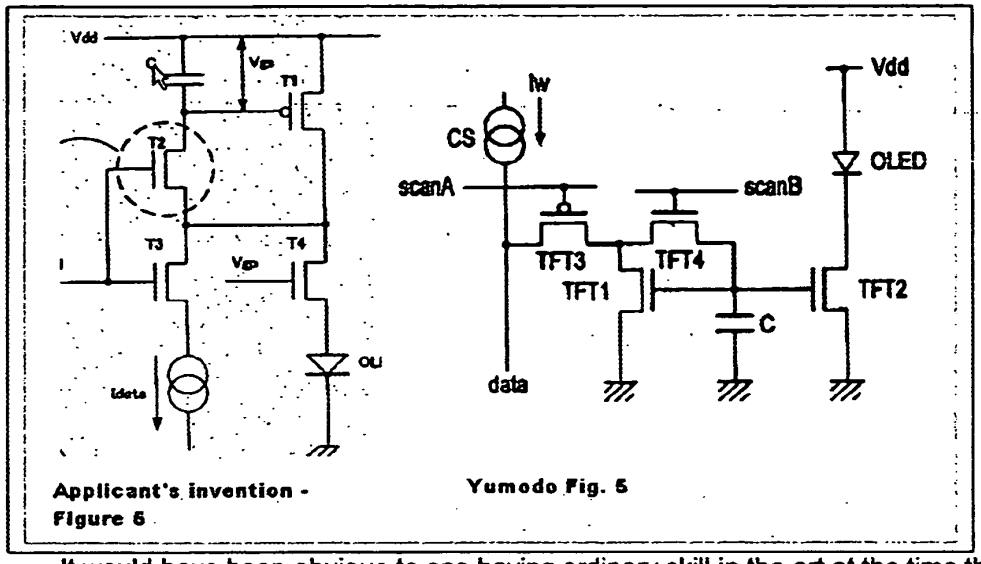
It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the two-transistor cell of Yamada with the multiple transistors of Yumoto, since both are aimed at active matrix panel applications (Yamada Fig. 1, Yumoto Fig. 2, etc.) and to prevent variation due to device parameters in cells similar to that of Yamada (Yumoto 0017).

As to claim 7,

The active matrix substrate according to claim 6, wherein said sixth terminal is connected to said third terminal and to said first terminal.

Reference Yamada does not teach the third transistor. Yumoto discloses in Figure 5 the use of a four-transistor cell. If transistor TFT1 is removed, then the claimed invention is precisely the same as applicant recites in claim 7, with the same connections. As both the multigate variant and the single gate variants of the second transistor are claimed, both will be briefly addressed. If the multigate transistor of Yamada – shown in Fig. 1 and discussed in the rejection to claim 5, is used in place of

TFT4 shown in Yumoto Fig. 5, the result will be exactly the invention recited by applicant. If only one gate is used on the second transistor, then no modification is necessary and again the invention recited in claim 7 is obtained. See images below.



Applicant's invention - Figure 6

Yumodo Fig. 5

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the two-transistor cell of Yamada with the multiple transistors of Yumoto, since both are aimed at active matrix panel applications (Yamada Fig. 1, Yumoto Fig. 2, etc.) and to prevent variation due to device parameters in cells similar to that of Yamada (Yumoto 0017).

As to claim 15,

An electro-optical device (see Yamada Fig. 1 and 4, etc.), comprising peripheral circuits (see Yamada Fig. 4 and Yumoto Figs. 7 and 11) to supply current to an electro-optical

element of each pixel corresponding to said electro-optical elements, wherein each of said peripheral circuits comprises:

-A light-emission control active element to supply a current to said electro-optical element during a light emission period (function served by recited first-active element; driving circuit can perform both tasks; see also TFT1 in Fig. 13, or in Fig. 12 the alternate structure, with TFT7, as a separate element);

-A holding element to hold a control voltage (170, Fig. 1, Yamada (1:50-60); Capacitor C in any of Figs. 11-15, Yumoto);

-A first active element, a gate terminal of which is connected to said holding element, which supplies a current, based on said control voltage applied to the gate terminal, to said electro-optical element via said light-emission control active element (140, Fig. 1, Yamada (1:40-45); see also TFT1, in Figs. 11 and 12 in Yumoto or TFT5 in Fig. 11);

-A current-controlling active element, which passes data current via said first active element during a selection period (TFT4 or TFT3 in Yumoto Fig. 13); and,

-A second active element, connected between said current-controlling active element and said holding element, which, during said selection period, charges said holding element and causes said control voltage to be stored (130, Fig. 1, Yamada (1:35-48); Yumoto – TFT1); and

-Wherein said active element contains a structure to prevent leakage current during shutoff (Yamada 3:5-15, 3:26-40).

Reference Yamada teaches the general two-transistor structure along with current-controlling elements and structures to prevent leakage current during shutoff.

Reference Yamada does not explicitly teach the other recited details of the claim. Yumoto teaches several different embodiments of peripheral structure for each pixel or unit circuit that contain all the recited elements as identified previously.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the two-transistor cell of Yamada with the multiple transistors of Yumoto, since both are aimed at active matrix panel applications (Yamada Fig. 1, Yumoto Fig. 2, etc.) and to prevent variation due to device parameters in cells similar to that of Yamada (Yumoto 0017). Furthermore, certain functionality that is split off in this claim, e.g. making the light-emission control active element separable from the driving TFT, and splitting off the current-controlling active elements, are obvious and not patentable under *Nerwin v. Erlichman*, 168 USPQ 177, 179 (PTO Bd. Of Int. 1969), since applicant is merely making separable items which are claimed as integral functions in earlier claims (For example, claims 1 and 4 used as evidence claims for this justification). Secondly, if the adjustable argument is made by applicant (that adding elements making those features adjustable), under *In re Stevens*, 101 USPQ 284 (CCPA 1954) that doctrine will not hold, in "that the provision of adjustability, when needed, is not a patentable advance."

18. Claims 8-12, 37, and 39 are rejected under 35 U.S.C. 103(a) as unpatentable over Yamada as applied to claim 4 above, and further in view of Maeda *et al* (US 2002/0008822 A1)('Maeda')[valid under 102(e)](claim 4 operative here – any of the other claims would be subject to the same rejection).

As to claim 8,

The active matrix substrate according to any of claims 4 through 7, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yamada 6:1-45 for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yamada 6:5-25); and

-A gate metal layer comprising said second control terminal (Yamada 6:40-45) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one scan line among said plurality of scan lines is formed in said gate metal layer (Maeda 0121).

Reference Yamada teaches all the limitations of this claim except the formation of a scan line in the gate metal layer. Reference Maeda teaches the formation of scan lines and gate electrodes in the same metal film layer for TFT / LCD monitor fabrication (e.g. 0162, 0121). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yamada with the single metal layer of Maeda since Maeda performs in one step what Yamada does in several steps (note Yamada fabrication process in 6:1-67 and 7:1-50), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination, e.g. common sense is sufficient to justify the combination. See also *In re Karlson*, 136 USPQ 184 (CCPA 1963), for the doctrine that eliminating components is an obvious expedient – in this, eliminating fabrication steps.

As to claim 9,

The active matrix substrate according to any of claims 4 through 7, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yamada 6:1-45 for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yamada 6:5-25); and

-A gate metal layer comprising said second control terminal (Yamada 6:40-45) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in said gate metal layer (Maeda 0121 and 0113 and 0125).

Reference Yamada teaches all the limitations of this claim except the formation of a data line in the gate metal layer. Reference Maeda teaches the formation of data lines and source and drain electrodes in the same metal film layer for TFT / LCD monitor fabrication (e.g. 0113, 0125). It would be *prima facie* obvious to choose to form gate electrodes and data lines simultaneously rather than gate electrodes and scan lines, for example. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yamada with the single metal layer of Maeda since Maeda performs in one step what Yamada does in several steps (note Yamada fabrication process in 6:1-67 and 7:1-50), which is *prima facie*

more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

As to claim 10,

The active matrix substrate according to any of claims 4 through 7, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yamada 6:1-45 for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yamada 6:5-25); and

-A gate metal layer comprising said second control terminal (Yamada 6:40-45) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-A source metal layer comprising a source electrode or drain electrode connected to the source or drain of said second transistor (Maeda 0113, 0125); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in the layer (Maeda 0121 and 0113 and 0125), among said source metal layer and said gate metal layer, which is closer to said semiconductor layer.

References Maeda and Yamada teach all the limitations of this claim, and this is merely a recitation of the dual limitations of claims 8 and 9 above. As such, the combination and motivation from claim 8 is used here and no further comment is necessary, as this claim is only a nominal variation of the parent.

As to claim 11,

An active matrix substrate, comprising a circuit with transistors, scan lines, and data lines, and having a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yamada 6:1-45 for example)[Yamada established to have transistors (1:10-15), scan lines (3:60-65), and signal lines (the data lines of applicant)(3:60-65)];

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yamada 6:5-25); and

-A gate metal layer having gate terminals of said transistors formed therein (Yamada 6:40-45); and

-Wherein at least one portion of either said scan lines or said data lines, or both, is formed in said gate metal layer (Maeda 0121 and 0113 and 0125).

References Maeda and Yamada teach all the limitations of this claim, and this is merely a recitation of the dual limitations of claims 8 and 9 above, e.g. forming the scan or data lines in the gate metal layer, and clearly in claim 8 the formation of scan lines in the gate metal, and thusly for the data lines in claim 9. As such, the combination and motivation from claim 8 is used here and no further comment is necessary, as this claim is only a nominal variation of the parent, e.g. the combination is obvious under *In re Karlson* and common sense as recited above. Further, in view of *In re Hubbell*, 76 USPQ 105 (CCPA 1947) and *In re Japikse*, 86 USPQ 70 (CCPA 1950), all applicant is doing is moving parts (fabrication steps for portions of the display) around among locations in the fabrication process. Reference Maeda very clearly teaches that scan

and data lines can be formed in metal layers wherever in the fabrication process such a metal layer is deposited if it would be favorable to do so.

As to claim 12,

An active matrix substrate, comprising a circuit with transistors, scan lines, and data lines, and having a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yamada 6:1-45 for example)[Yamada established to have transistors (1:10-15), scan lines (3:60-65), and signal lines (the data lines of applicant)(3:60-65)];

Wherein said plurality of layers comprise:

-A semiconductor layer, in which a semiconductor film constituting transistors is formed (Yamada 6:5-25); and

-A gate metal layer having gate terminals of said transistors formed therein (Yamada 6:40-45); and

-A source metal layer in which source electrodes or gate electrodes connected to sources or drains of said transistors are formed; and

-Wherein at least one portion of either said scan lines or said data lines, or both, is formed in the layer, among said gate metal layer and said source metal layer, which is closer to said semiconductor layer (Maeda 0121 and 0113 and 0125).

References Maeda and Yamada teach all the limitations of this claim, and this is merely a restating of the limitations of claim 11 with a bit of shuffling. These variations have been covered exhaustively in the rejections for claims 8-11 as above. The

combination and motivation are that of claim 11, as this is only a nominal variation and the shifting of parts as attributed above in claim 11.

As to claim 37,

An active matrix substrate, comprising unit circuits comprising transistors, arranged corresponding to intersections of data lines and scan lines (Yamada Figs. 1 and 4 for example) wherein

-A semiconductor layer constituting such transistors is formed in a semiconductor layer (Yamada 6:5-25);

-Either said scan lines or said data lines are formed in a first conducting layer at the intersections of said scan lines and said data lines (Maeda 0113, 0121, and 0125); and,

-A portion of said scan lines and said data lines outside said intersections are formed in a second conducting layer (Maeda 0113, 0121, and 0125).

Reference Yamada does not explicitly teach the formation of scan or data lines formed in a conducting layer at the intersections of such lines. Reference Maeda describes forming gate metal and scan lines, etc. simultaneously. As such, the scan lines would be formed everywhere not masked with a shadow mask, e.g. both in the scan lines and in the intersections. No matter what portions of the lines are claimed, any such configuration could be made using shadow masking and formed using either evaporation or sputtering. Any set of contacts could be created using correctly etched contact holes; electrically contiguous metal formed in the same layer is *prima facie* the same from an electrical and an engineering perspective. Further, forming scan lines or data lines or portions thereof (as claimed) in the same layer as other things would

simply be making a component integral by eliminating unnecessary metal, and under *In re Larson*, 144 USPQ 347 (CCPA 1965), making a component integral is obvious and not patentable. Therefore, under either methodology, the recited limitations of the claim have been met.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yamada with the single metal layer of Maeda since Maeda performs in one step what Yamada does in several steps (note Yamada fabrication process in 6:1-67 and 7:1-50), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

As to claim 39,

An electro-optical device, comprising electro-optical elements corresponding to intersections of scan lines and data lines (Yamada Figs. 1 and 4, element 60 for example (OLED)), wherein:

-A pair of electrodes is provided to supply power to electro-optical elements (Maeda Fig. 11C, elements 19 and 15 are opposing and pixel electrodes (see 0006-0008));

-At the intersections of said scan lines and said data lines, either said scan lines or said data lines are formed in a first conducting layer (Maeda 0113, 0118, 0121, 0125 – again, gate metal as discussed in rejections to claims 8-12);

-Portions of said scan lines and said data lines outside said intersections are formed in a second conducting layer (source metal layer, 0113, 0118, 0121, 0125 as discussed in rejections to claims 8-12); and,

-Said second conducting layer is positioned at a greater distance than said first conducting layer from one of said pair of electrodes (design choice issue, see Maeda Fig. 11C).

Reference Yamada does not recite details of the fabrication process claimed above. Reference Maeda teaches the fabrication of such substrates and teaches contact holes (0044, 0047). Logically, such contact holes would fill on conducting layer deposition, thus meeting the recited limitation concerning intersections of data and scan lines. The positioning of a layer or its size is *prima facie* obvious and is not patentable (*In re Japikse* for order of parts and further under *In re Reese*, anyone of ordinary skill in the art would know that there would be an optimal spacing of electrodes from each other to minimize cross-talk that would also occupy the minimum aspect ratio required on the shadow mask).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yamada with the single metal layer of Maeda since Maeda performs in one step what Yamada does in several steps (note Yamada fabrication process in 6:1-67 and 7:1-50), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

19. Claim 13 is rejected under 35 U.S.C. 103(a) as unpatentable over Yamada in view of Maeda as applied to claims 11 and 12 above, and further in view of Gualandris.

As to claim 13,

The active matrix substrate according to claim 11 or claim 12, wherein said unit circuit comprises:

-A first transistor, comprising a first control terminal, a first terminal, and a second terminal (140, Fig. 1, Yamada (1:40-45));

-A holding element, connected to said first control terminal, and comprising a first electrode and a second electrode (170, Fig. 1, Yamada (1:50-60)); and,

-A second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal and said fourth terminal being respectively connected to said first terminal and said first electrode (140, Fig. 1, Yamada (1:40-45)); and

-Wherein said second transistor is a transistor comprising a structure selected from the group consisting of an LDD structure, GDD structure, and DDD structure.

Yamada teaches in Fig. 5 that elements 13 and 13LD – discussed in 6:15-25 – have the LDD structure in the active transistor, and it is discussed as being the active layer *per se*, that is on top of the gate oxide, so it would work for any transistor as specified there. However, Yamada does not explicitly teach the use of GDD and DDD structures where Gualandris teaches DDD in 1:55-65, GDD in 2:25-30, and LDD in 2:25-30. Gualandris teaches that these are all methods of doping transistors, although one (the LDD) is preferred to work for 'ULSI' applications. Given that 'ULSI' applications at the time the patent was issued were mainly for deep sub-micron processes and that current TFT / liquid crystal display processes have much larger dimensions, e.g. still larger than one micron minimum channel length for silicon-on-glass technology, these techniques would be perfectly valid for use in TFT / silicon-on-glass technology.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix substrates of Yamada and Maeda with the transistors of Gualandris, since Yamada [and Maeda] uses silicon transistors, which *prima facie* have a source and a drain and different drain doping techniques are well-known in the art. Further, since only the primary reference is utilized (e.g. no Maeda), a separate motivation is not required for Maeda and Yamada. Further, the gates in Gualandris utilize (5:10-20) a silicon layer as their base, as the substrates for Maeda and Yamada are silicon as well.

As to claim 14,

An electro-optical device comprising an active matrix substrate according to any of the claims 1 through 13, and electro-optical elements. (Yamada Fig. 4, element 60 – an OLED, which is *prima facie* an electro-optical device with an anode 61 (see 5:35-60)). Since only the primary reference is used, no motivation or combination is necessary. That of claim 13 is used if were to be necessary for this rejection.

20. Claim 34 is rejected under 35 U.S.C. 103(a) as unpatentable over Yamada in view of Koyama (US PGPub 2001/0040565 A1)('Koyama')(valid under 102(e)).

As to claim 34,

An active matrix substrate, comprising pixel electrodes and path arranged corresponding to intersections of data lines and scan lines (Yamada Figs. 1 and 4; Koyama Fig. 1), wherein:

-Said pixel electrodes are connected to a power supply line via one or more transistors (Koyama,.element 9106, Fig. 1 (0055); Yamada element 140, Fig. 1, connected to 150 power supply line);

-A holding element is provided, connected to a gate of said one or more transistors (Yamada capacitor C, element 170, Fig. 1; Koyama, element 9107 (0055)); and

-A first electrode constituting said holding element is connected to said power supply line (*prima facie* the capacitor of Koyama that is connected to the power supply line, would constitute two electrodes (capacitors have two electrodes by definition)).

Reference Yamada teaches all the limitations except a capacitor directly connected to the power supply line. Reference Koyama teaches the use of a capacitor directly connected to the power supply line. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the circuitry of Yamada with the capacitor of Koyama, as the structures claim are almost the same (e.g. multi-gate (see Fig. 1 and 0055-0057)) and the addition of the capacitor makes it easier to test for defects in manufacturing (see 0034-0037). Also, the position of the relevant capacitor is a design choice issue (positioning of parts, *In re Japikse* as discussed in other portions of the rejection).

21. Claims 35 and 36 are rejected under 35 U.S.C. 103(a) as unpatentable over Yamada in view of Koyama as applied to claim 34 above, and further in view of Maeda [Even though this is an independent claim, the variation is extremely nominal].

As to claim 35,

-An active matrix substrate, comprising pixel electrodes and path arranged corresponding to intersections of data lines and scan lines (Yamada Figs. 1 and 4; Koyama Fig. 1), wherein:

-Said pixel electrodes are connected to a power supply line via one or more transistor (Koyama, element 9106, Fig. 1 (0055); Yamada element 140, Fig. 1, connected to 150 power supply line);

-A holding element is provided, connected to a gate of said one or more transistor (Yamada capacitor C, element 170, Fig. 1; Koyama, element 9107 (0055)); and

-A first electrode constituting said holding element is a portion of said power supply line (*prima facie* the capacitor of Koyama that is connected to the power supply line, would constitute two electrodes (capacitors have two electrodes by definition) and (Maeda 0121 and 0113 and 0125).

References Yamada and Koyama teach all of the limitations except explicitly stating that such an electrode could be a portion of said power supply line. In the rejections to claims 8-12, the formation of data and scan lines in either gate metal or source metal layers is discussed and the formation of such lines in those layers is claimed (those arguments are incorporated here by reference). Reference Maeda teaches the formation of multiple sets of lines (e.g. gates, scan lines, etc. (Maeda 0121 and 0113 and 0125) simultaneously during metal deposition steps. It would be obvious to combine power supply line formation with the deposition of the electrodes to form the capacitors (in TFT processes, capacitors are often MIM (metal-insulator-metal)). As

such, the power supply line would in fact be the electrode of such a capacitor, as they were formed simultaneously and are electrically contiguous.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the TFT circuitry of Yamada and Koyama with the single metal layer of Maeda since Maeda performs in one step what Yamada does in several steps (note Yamada fabrication process in 6:1-67 and 7:1-50), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination, e.g. common sense is sufficient to justify the combination. See also *In re Karlson*, 136 USPQ 184 (CCPA 1963), for the doctrine that eliminating components is an obvious expedient – in this, eliminating fabrication steps.

As to claim 36,

The active matrix substrate of claim 34 or claim 35, wherein a second electrode constituting said holding element is the gate of one or more said transistors.

References Yamada and Koyama do not explicitly teach this limitation. Reference Maeda describes forming gate metal and scan lines, etc. simultaneously. As such, the top electrode of the capacitor would be simultaneously formed with the gate. Electrically contiguous metal formed in the same layer is *prima facie* the same from an electrical and an engineering perspective. Further, making the capacitor top electrode and the gate electrode the same thing (as claimed) would simply be making a component integral by eliminating unnecessary metal, and under *In re Larson*, 144 USPQ 347 (CCPA 1965), making a component integral is obvious and not patentable. Therefore, under either methodology, the recited limitations of the claim have been met.

This claim is only a nominal variation of the parent (e.g. claim 35) and as such the rejection uses the same combination and motivation without need to repeat it.

21. Claim 38 is rejected over Yamada in view of Maeda as applied to claim 37, and further in view of Tanaka (US PGPub 2001/0026835 A1)('Tanaka')(valid under 102(e)).

As to claim 38,

The active matrix substrate according to claim 37, wherein said second conducting layer is positioned between said first conducting layer and said semiconductor layer.

Reference Yamada does not explicitly teach this limitation. In Fig. 10B, Maeda shows that the bottom gate – element 56, which is metal (a niobium alloy) is put down first, then various insulating materials, then element 13 (source and drain electrodes) are formed on the same level and slightly covering the semiconductor layer 54. Under the doctrine of *In re Japikse*, switching the two layers would be *prima facie* obvious, and only minor alternations in the shadow masks for the process would be necessary (additive vs. subtractive processing in semiconductors, for example, switching the process would not be difficult for one of ordinary skill in the semiconductor / TFT art). Again, given that Maeda teaches many different embodiments (see Figs. 10-13, etc.), such a switch would be a design choice issue, and it would allow low-temperature processing of the substrate throughout the process, particularly allowing for newer techniques such as laser annealing and recrystallization of the semiconductor layer taught by Tanaka, and treatment of the semiconductor layer towards the end of processing.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the TFT circuits of Yamada and Maeda with the laser annealing processing of polysilicon for TFT applications of Tanaka (see 0002-0015), as both Yamada (2:61-67) and Maeda (0008, 0121, etc.) utilize polysilicon as the semiconductor material, and laser annealing is now a well-known, standard process in the art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric V Woods whose telephone number is 703-305-0263. The examiner can normally be reached on M-F 7:30-5:00 alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on 703-305-4713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JEFFERY BRIER
PRIMARY EXAMINER

Eric Woods 11/2/2004

Notice of References Cited	Application/Control No. 10/299,861	Applicant(s)/Patent Under Reexamination MATSUEDA, YOJIRO	
	Examiner Eric V Woods	Art Unit 2672	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-RE35,827	06-1998	Gualandris et al.	257/285
	B	US-6,781,155 B1	08-2004	Yamada, Tsutomu	257/72
	C	US-2001/0026835	10-2001	Tanaka, Koichiro	427/96
	D	US-2001/0040565	11-2001	Koyama, Jun	345/204
	E	US-2002/0008822	01-2002	Maeda, Akitoshi	349/139
	F	US-2004/0207615	10-2004	Yumoto, Akira	345/211
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Sheet 1 of 1

*Form PTO-1449 (REV. 8-83) U.S. Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 114251	APPLICATION NO. 10/299,861
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANT Yojiro MATSUEDA	
	FILING DATE November 20, 2002	GROUP 1775

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS

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JUL 02 2004
TC 1700

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
EW	1)	WO 98/36407 w/ abst	08/20/1998	WIPO		
EW	2)	JP A 2000-214800 w/ abst. & trans	08/04/2000	JAPAN		
EW	3)	JP A 2001-13893 w/ abst. & trans	01/19/2001	JAPAN		
EW	4)	JP A 2000-284727 w/ abst. & trans	10/13/2000	JAPAN		
EW	5)	JP A 11-65487 w/ abst. & trans	03/05/1999	JAPAN		
EW	6)	JP A 1-101519	04/19/1989	JAPAN		
EW	7)	JP A 2-170135	06/29/1990	JAPAN		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED
[signature]	10/28/2004

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Examiner-Initiated Interview Summary	Application No.	Applicant(s)	
	10/299,861	MATSUEDA, YOJIRO	
	Examiner	Art Unit	
	Eric V Woods	2672	

All Participants:

(1) *Eric V Woods*.

(2) *JerryThielman*.

Status of Application: *Pending*

(3) _____.

(4) _____.

Date of Interview: *28 October 2004*

Time: *2:35 p.m.*

Type of Interview:
- ☒ Telephonic
- ☐ Video Conference
- ☐ Personal (Copy given to: ☐ Applicant ☐ Applicant's representative)

Exhibit Shown or Demonstrated: ☐ Yes ☒ No
If Yes, provide a brief description:

Part I.

Rejection(s) discussed:
N/A - Restriction / election only

Claims discussed:
1-39

Prior art documents discussed:
N/A

Part II.

SUBSTANCE OF INTERVIEW DESCRIBING THE GENERAL NATURE OF WHAT WAS DISCUSSED:
See Continuation Sheet

Part III.

☐ It is not necessary for applicant to provide a separate record of the substance of the interview, since the interview directly resulted in the allowance of the application. The examiner will provide a written summary of the substance of the interview in the Notice of Allowability.

☒ It is not necessary for applicant to provide a separate record of the substance of the interview, since the interview did not result in resolution of all issues. A brief summary by the examiner appears in Part II above.

(Examiner/SPE Signature) (Applicant/Applicant's Representative Signature – if appropriate)

Continuation of Substance of Interview including description of the general nature of what was discussed: Applicant's attorney of record stated that applicant is electing Group I, that is claims 1-15 and 34-39, with traverse. This was in response to a phone call from examiner to applicant's attorney of record informing him of a restriction requirement with three groups of claims. .

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2672

Application No.: 10/299,861

Examiner: E. V. Woods

Filed: November 20, 2002

Docket No.: 114251

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE

AMENDMENT UNDER 37 CFR §1.111

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the January 13, 2005 Office Action, please consider the following:

Amendments to the Specification;

Amendments to the Claims are reflected in the listing of claims;

Amendments to the Drawings include attached replacement sheets; and

Remarks.

Amendments to the Specification:

Please replace the paragraph at page 15, line 17 – page 16, line 18 with the following rewritten paragraph:

Fig. 1 is an overall drawing of a display panel of this embodiment;

Fig. 2 is a plane view of a pixel region in embodiment 1;

Fig. 3 shows plane views of a pixel region in embodiment 1; Fig. 3A is a cross-section along A-A in Fig. 2, Fig. 3B is a cross-section along B-B in Fig. 2, and Fig. 3C is a cross-section along ~~C-C~~ D-D in Fig. 2;

Fig. 4 shows examples of modification of the boundary shape of the light-emitting portion; Fig. 4A shows the case of a circular light-emitting portion, Fig. 4B shows the case of a light-emitting portion having a curved portion symmetrical about a center line, and Fig. 4C shows the case of a light-emitting region having a curved portion asymmetrical about a center line;

Fig. 5 is a circuit diagram of a pixel region in embodiment 1;

Fig. 6 is a drawing explaining the alignment of a metal layer in embodiment 1;

Fig. 7 is a drawing explaining processing to separate gate metal in embodiment 1;

Fig. 8 is a plane view of a pixel region in embodiment 2;

Fig. 9 shows cross-sectional views of a pixel region in embodiment 2; Fig. 9A is a cross-section along A-A in Fig. 8, Fig. 9B is a cross-section along B-B in Fig. 8, and Fig. 9C is a cross-section along ~~C-C~~ D-D in Fig. 8;

Fig. 10 is a plane view of a pixel region in embodiment 3;

Fig. 11 shows cross-sectional views of a pixel region in embodiment 3; Fig. ~~10A~~ 11A is a cross-section along A-A in Fig. 10, and Fig. ~~10B~~ 11B is a cross-section along B-B in Fig. 10;

Fig. 12 is a plane view of a pixel region in embodiment 4;

Fig. 13 shows cross-sectional views of a pixel region in embodiment 4; Fig. 13A is a cross-section along A-A in Fig. 12, and Fig. 13B is a cross-section along B-B in Fig. 12;

Fig. 14 is a connection diagram for a display panel in embodiment 5; and,

Fig. 15 shows examples of electronic device in embodiment 5, showing examples of application of a display panel of this invention to a portable telephone in Fig. 15A, to a camcorder in Fig. 15B, to a portable personal computer in Fig. 15C, to a head-mounted display in Fig. 15D, to a rear projector in Fig. 15E, and to a front projector in Fig. 15F.

Please replace the paragraph at page 18, lines 5-8 with the following rewritten paragraph:

Fig. 3 shows cross-sections to explain the layer structure in each of the cross-sectional planes shown in Fig. 2. Fig. 3A, Fig. 3B, and Fig. 3C show the layer structure in the A-A cross-sectional plane, B-B cross-sectional plane, and ~~C-C~~ D-D cross-sectional plane, respectively.

Please replace the paragraph at page 18, lines 25-29 with the following rewritten paragraph:

As the underlayer protective film 101, silicon oxide film (SiO_x: $0<x\leq2$), silicon nitride film (Si_3N_x: $0<x\leq4$), and other insulating materials can be used, where x represents the number of atoms in the associated formula. The underlayer protective film is formed in order to prevent sodium (Na) and other mobile ions contained in the glass substrate from penetrating into the semiconductor layer and exerting adverse effects on impurity control in the semiconductor layer.

Please replace the paragraph at page 19, lines 4-11 with the following rewritten paragraph:

As the semiconductor layer 102, in addition to a group IV single-element semiconductor layer of silicon (Si), germanium (Ge) or similar, a complex with a group IV element, such as silicon germanium (Si_xGe_{1-x}: $0<x<1$), silicon carbide (Si_xC_{1-x}: $0<x<1$), or germanium carbide (Ge_xC_{1-x}: $0<x<1$), as well as a compound of group III and group V elements such as gallium arsenide (GaAs) and indium antimonide (InSb), a compound of group II and group VI elements such as cadmium selenide (CdSe), or other different complex compounds such as silicon germanium gallium arsenide ($Si_xGe_yGa_zAs_z$: $x+y+z=1$), can be employed, where x, y and z represent integer values (two of which are "0" and the remainder is "1") of the atom in the formula.

Please replace the paragraph at page 21, lines 7-10 with the following rewritten paragraph:

As the hole transport layer 111, for example, N, N'-diphenyl-N,N'-bis-(3-methylphenyl)-(1,1'-biphenyl)-4,4'-diamine (TPDA) is used. The hole transport layer is

deposited in the aperture portion provided in the bank layer ~~109~~ 108, using a metal mask or similar.

Please replace the paragraph at page 26, line 30 – page 27, line 10 with the following rewritten paragraph:

Hence in this embodiment, the wiring pattern formed by the gate metal layer is positioned with a separation of at least a prescribed distance from at least one among the electrodes of the light-emitting layer. A problem due to low impedance arises due to the distance between the cathode layer 109, which is the common electrode, and the gate metal layer 104. Also, the cathode layer 109 is a small distance from the lower side in the light-emitting portion OLED, so that the distance from the gate metal layer in the vicinity of the light-emitting portion poses a problem. Hence in this embodiment, as shown in Fig. 7 (equivalent to the ~~C-C~~ D-D cross-section in Fig. 2), patterns are formed such that, near the light-emitting portion, the distance d1 in the depth direction between the cathode layer 109 and the gate metal layer 104 and the distance d2 in the plane are both equal to or greater than a prescribed distance.

Please replace the paragraph at page 30, lines 11-18 with the following rewritten paragraph:

Fig. 8 shows a plane view explaining one pixel region and the wiring pattern in the vicinity thereof for an EL element of embodiment 2 of this invention. Fig. 9 shows cross-sectional views which explain the layer structure in cross-sections of Fig. 8. Fig. 9A shows the layer structure in a cross-section along the A-A plane, Fig. 9B is a cross-section along B-B, and Fig. 9C is a cross-section along ~~C-C~~ D-D. In these drawings, similarly to embodiment 1, the patterns of the principal semiconductor layer 102, gate metal layer 104, source metal layer 106, and anode layer 110 are shown.

Please replace the paragraph at page 30, line 25 – page 31, line 6 with the following rewritten paragraph:

As shown in Fig. 9C, the light-emitting portion OLED in embodiment 2 comprises an affinity-controlling layer 113, between the second interlaminar insulating film 107 and the bank layer 108. This affinity-controlling layer 113 need not be formed over the entire pixel region, but when forming a light-emitting portion OLED using a liquid material, should preferably be provided at least near the boundaries of the light-emitting portion. The affinity-

controlling layer 113 must have an affinity for the liquid material used in forming the light-emitting portion. In this embodiment, the bank layer 108 forms a wall near the boundary of the light-emitting portion; a material is selected which exhibits no affinity for the liquid material used when forming the light-emitting layer ~~110~~ 112, and ~~[the bank layer]~~ the bank layer 108 is stacked on top of the affinity-controlling layer 113. Consequently the affinity-controlling layer 113 forms a step shape Step on the inside of the light-emitting portion in the wall formed by the bank layer, as shown in Fig. 8 and Fig. 9C.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An active matrix substrate including a plurality of electro-optical elements, comprising peripheral circuits to supply current to an electro-optical element of each pixel corresponding to said electro-optical elements, wherein each of said peripheral circuits comprises:

a holding element to hold a control voltage;

a first active element, comprising a control terminal and a terminal, said control terminal being connected to said holding element, and said terminal being connected in series to said ~~holding~~ electro-optical element, to supply a current based on said control voltage to said electro-optical element; ~~and,~~ and

a second active element, connected ~~to~~ between said ~~holding~~ control terminal and said terminal of said first active element, ~~which controls the charging and discharging of said holding element; and~~

wherein said second active element comprises a structure to prevent leakage currents during shutoff.

2. (Currently Amended) The active matrix substrate according to claim 1, wherein said second active element is configured as a multi-gate ~~type~~ active element.

3. (Currently Amended) The active matrix substrate according to claim 1, wherein at least said second active element is a transistor comprising a structure selected from the group consisting of an LDD structure, a GDD structure, and a DDD structure.

4. (Currently Amended) An active matrix substrate, comprising a plurality of unit circuits arranged corresponding to intersections of a plurality of data lines and a plurality of scan lines, wherein each of said plurality of unit circuits comprises:

a first transistor, comprising a first control terminal, a first terminal, and a second terminal, said first terminal connected in series to an electro-optical element;

a holding element, connected to said first control terminal, and comprising a first electrode connected to said first control terminal and a second electrode connected to said second terminal; ~~and,~~ and

a second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal being connected to one of said first terminal and

said second terminal, and said fourth terminal being ~~respectively~~ connected to said first control terminal ~~and said first electrode~~; ~~and~~

wherein said second transistor has a multi-gate structure.

5. (Currently Amended) An active matrix substrate, comprising a plurality of unit circuits arranged corresponding to intersections of a plurality of data lines and a plurality of scan lines, wherein each of said plurality of unit circuits comprises:

a first transistor, comprising a first control terminal, a first terminal, and a second terminal, said first terminal connected in series to an electro-optical element;

a holding element, connected to said first control terminal, and comprising a first electrode connected to said first control terminal and a second electrode connected to said second terminal; ~~and,~~ and

a second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal being connected to one of said first terminal and said second terminal, and said fourth terminal being ~~respectively~~ connected to said first control terminal ~~and said first electrode~~; ~~and~~

wherein said second transistor is a transistor comprising a structure selected from the group consisting of an LDD structure, a GDD structure, and a DDD structure.

6-7. (Cancelled)

8. (Currently Amended) The active matrix substrate according to claim 4, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed; and

a gate metal layer comprising said second control terminal, and

wherein at least a portion of ~~one scan line among~~ said plurality of scan lines is formed in said gate metal layer.

9. (Previously Presented) The active matrix substrate according to claim 4, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed; and

a gate metal layer comprising said second control terminal; and

wherein at least a portion of one data line among said plurality of data lines is formed in said gate metal layer.

10. (Currently Amended) The active matrix substrate according to claim 4, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed;

a gate metal layer comprising said second control terminal; and

a source metal layer comprising a source electrode or drain electrode connected to the source or drain of said second transistor; ~~and~~

wherein at least one portion of at least one data line among said plurality of data lines is formed in the layer, among said source metal layer and said gate metal layer, ~~which~~ that is closer to said semiconductor layer.

11-13. (Cancelled)

14. (Currently Amended) An electro-optical device comprising an active matrix substrate according to claim 1, and said electro-optical elements.

15. (Currently Amended) An electro-optical device including a plurality of electro-optical elements, comprising peripheral circuits to supply current to an electro-optical element of each pixel corresponding to said electro-optical elements,

wherein each of said peripheral circuits comprises:

a light-emission control active element to supply ~~a current~~ said current to said electro-optical element during a light emission period;

a holding element to hold a control voltage;

a first active element comprising a gate terminal and a terminal, ~~a~~ said gate terminal ~~of which is~~ being connected to said holding element, ~~which~~ that supplies a current, based on said control voltage applied to the gate terminal, and said terminal being connected in series to said electro-optical element via said light-emission control active element;

a current-controlling active element, ~~which~~ that passes data current via said first active element during a selection period; ~~and,~~ and

a second active element, connected between a first terminal to said current-controlling active element and said terminal and a second terminal to said holding element and said control terminal, ~~which~~ that, during said selection period, charges said holding element and causes said control voltage to be stored; ~~and,~~

wherein said second active element comprises a structure to prevent leakage currents during shutoff.

16. (Withdrawn - Currently Amended) An electro-optical device, comprising electro-optical elements and peripheral circuitry ~~which~~ that drives said electro-optical elements,

wherein said electro-optical elements are formed such that a boundary of the electro-optical elements has, at least, a prescribed curvature; and

at least one portion of said peripheral circuitry is formed in the region surrounded by the boundary having the specified curvature and by the boundaries of a polygon circumscribing the electro-optical element.

17. (Withdrawn) The electro-optical device according to claim 16, wherein a plurality of boundary portions having said prescribed curvature are formed.

18. (Withdrawn) The electro-optical device according to claim 16, wherein said plurality of formed boundary portions are arranged substantially symmetrically with respect to a center line passing through the geometric center of said electro-optical element.

19. (Withdrawn - Currently Amended) An electro-optical device, comprising a light-emitting portion and a peripheral circuit ~~which~~ that controls the current supplied to said light-emitting portion, by means of a pixel electrode, wherein:

the area of said light-emitting portion is smaller than the area of said pixel electrode; and,

the shape of said light-emitting portion and the shape of said pixel electrode are different.

20. (Withdrawn - Currently Amended) An electro-optical device, comprising a light-emitting portion and a peripheral circuit ~~which~~ that controls the current supplied to said light-emitting portion, by means of a pixel electrode, wherein:

the area of said light-emitting portion is smaller than the area of said pixel electrode; ~~and,~~ and

the shape of said light-emitting portion is a shape having a curvature, and the shape of said pixel electrode is a polygonal shape.

21. (Withdrawn - Currently Amended) An electro-optical device, comprising a light-emitting portion and a peripheral circuit ~~which~~ that controls the current supplied to said light-emitting portion, by means of a pixel electrode, wherein:

the area of said light-emitting portion is smaller than the area of said pixel electrode;

said light-emitting portion has a polygonal shape having n vertices (where n is an integer greater than or equal to 4);

said pixel electrode has a polygonal shape having m vertices (where m is an integer greater than or equal to 3); ~~and,~~ and

the relation n>m obtains.

22. (Withdrawn) The electro-optical device according to claim 19, wherein the entire region of said light-emitting portion is formed on said pixel electrode, and a contact region for connection of said peripheral circuit and said pixel electrode is provided in a portion of said pixel electrode in which said light-emitting portion is not formed.

23. (Withdrawn - Currently Amended) An electro-optical device, comprising:

an electro-optical element;

a holding capacitance, constituted by a plurality of layers including electrodes, ~~which~~ that regulates a current supplied to said electro-optical element; ~~and,~~ and

an active element ~~which~~ that supplies current to said electro-optical element according to the electric charge amount held in said holding capacitance;

wherein a first electrode constituting said holding capacitance is formed by patterning a portion of a metal layer comprising a power supply line ~~which~~ that supplies current to said electro-optical element.

24. (Withdrawn) The electro-optical device according to claim 23, wherein a second electrode constituting said holding capacitance is formed by patterning a portion of a metal layer comprising a control terminal of said active element.

25. (Withdrawn) The electro-optical device according to claim 23, wherein said first electrode is a portion of said power supply line, and a portion of a metal layer forming a control terminal of said active element is superposed on a portion of said power supply line and patterned to form said second electrode.

26. (Withdrawn) The electro-optical device according to claim 23, comprising a semiconductor layer below said first electrode and said second electrode.

27. (Withdrawn) The electro-optical device according to claim 25, wherein the region occupied by a layer positioned on the lower side among the layers constituting electrodes of said holding capacitance is formed to be larger than the region occupied by a layer positioned on the upper side.

28. (Withdrawn) The electro-optical device according to claim 27, wherein the region occupied by said layer positioned on the lower side is pattern-formed in a shape such that, even if the maximum possible position shift occurs at the time of formation of said layer

positioned on the upper side, the region of the layer positioned on the upper side is contained within the region of said layer positioned on the lower side.

29. (Withdrawn - Currently Amended) An electro-optical device, comprising a plurality of layers including electrodes, configured such that a current can be supplied by an active element according to a voltage stored in a holding capacitance to an electro-optical element ~~which~~ that emits light through the application of an electric field between the electrodes, comprising:

a first metal layer, constituting a power supply line; ~~and,~~ and

a second metal layer, formed in a pattern including a portion of a control terminal of said active element; and

wherein one electrode constituting said holding capacitance is formed by patterning one portion of said first metal layer.

30. (Withdrawn) The electro-optical device according to claim 29, wherein the other electrode constituting said holding capacitance is formed by patterning one portion of said second metal layer.

31. (Withdrawn) The electro-optical device according to claim 29, wherein one electrode constituting said holding capacitance is one portion of said power supply line, and said other electrode is formed by superposing a portion of said second metal layer on a portion of the power supply line and patterning.

32. (Withdrawn) The electro-optical device according to claim 29, wherein the region occupied by a layer positioned on the lower side among the layers comprising said holding capacitance electrodes is formed to be larger than the region occupied by a layer positioned on the upper side.

33. (Withdrawn) The electro-optical device according to claim 32, wherein the region occupied by said layer positioned on the lower side is pattern-formed in a shape such that, even if the maximum possible position shift occurs at the time of formation of said layer positioned on the upper side, the region of the layer positioned on the upper side is contained within the region of said layer positioned on the lower side.

34-36. (Cancelled)

37. (Currently Amended) ~~An~~ The active matrix substrate in accordance with claim 4, comprising unit circuits comprising transistors, arranged corresponding to intersections of data lines and scan lines; wherein

a semiconductor film constituting said transistors is formed in a semiconductor layer;

either said scan lines or said data lines are formed in a first conducting layer at the intersections of said scan lines and said data lines; ~~and,~~ and

a portion of said scan lines and said data lines outside said intersections are formed in a second conducting layer.

38. (Original) The active matrix substrate according to claim 37, wherein said second conducting layer is positioned between said first conducting layer and said semiconductor layer.

39. (Currently Amended) ~~An~~ The electro-optical device according to claim 4, comprising electro-optical elements corresponding to intersections of scan lines and data lines, wherein:

a pair of electrodes is provided to supply power to said electro-optical elements;

at the intersections of said scan lines and said data lines, either said scan lines or said data lines are formed in a first conducting layer;

portions of said scan lines and said data lines outside said intersections are formed in a second conducting layer; ~~and,~~ and

said second conducting layer is positioned at a greater distance than said first conducting layer from one of said pair of electrodes.

40. (New) The active matrix substrate in accordance with claim 1, wherein said first and second active elements have opposite polarities.

41. (New) An active matrix substrate, comprising a plurality of unit circuits arranged corresponding to intersections of a plurality of data lines and a plurality of scan lines, wherein each of said plurality of unit circuits comprises:

a first transistor, comprising a first control terminal, a first terminal, and a second terminal, said first terminal connected in series to an electro-optical element;

a holding element, connected to said first control terminal, and comprising a first electrode connected to said first control terminal and a second electrode connected to said second terminal;

a second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal being connected to one of said first terminal and said second terminal, and said fourth terminal being connected to said first control terminal; and

a third transistor comprising a fifth terminal, a sixth terminal, and a third control terminal, wherein

said second transistor has a multi-gate structure,

said third control terminal is connected to one scan line among said plurality of scan lines,

said fifth terminal is connected to one data line among said plurality of data lines, and

said sixth terminal is connected to said third terminal and to said first terminal.

42. (New) The active matrix substrate according to claim 41, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed; and

a gate metal layer comprising said second control terminal, and

wherein at least a portion of said plurality of scan lines is formed in said gate metal layer.

43. (New) The active matrix substrate according to claim 41, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed; and

a gate metal layer comprising said second control terminal; and

wherein at least a portion of one data line among said plurality of data lines is formed in said gate metal layer.

44. (New) The active matrix substrate according to claim 41, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed;

a gate metal layer comprising said second control terminal; and

a source metal layer comprising a source electrode or drain electrode connected to the source or drain of said second transistor; and

wherein at least one portion of at least one data line among said plurality of data lines is formed in the layer, among said source metal layer and said gate metal layer, that is closer to said semiconductor layer.

45. (New) An active matrix substrate, comprising a plurality of unit circuits arranged corresponding to intersections of a plurality of data lines and a plurality of scan lines, wherein each of said plurality of unit circuits comprises:

a first transistor, comprising a first control terminal, a first terminal, and a second terminal, said first terminal connected in series to an electro-optical element;

a holding element, connected to said first control terminal, and comprising a first electrode connected to said first control terminal and a second electrode connected to said second terminal;

a second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal being connected to one of said first terminal and said second terminal, and said fourth terminal being connected to said first control terminal; and

a third transistor comprising a fifth terminal, a sixth terminal, and a third control terminal,

wherein said second transistor is a transistor comprising a structure selected from the group consisting of an LDD structure, a GDD structure, and a DDD structure;

said second transistor has a multi-gate structure,

said third control terminal is connected to one scan line among said plurality of scan lines,

said fifth terminal is connected to one data line among said plurality of data lines, and

said sixth terminal is connected to said third terminal and to said first terminal.

Amendments to the Drawings:

The attached sheets of drawings includes changes and additions to Figs 2 and 8.

These sheets, which include Figs. 2 and 8, replace the original sheets including Figs. 2 and 8.

Attachment: Replacement Sheets: Figs. 2 and 8

REMARKS

Claims 1-5, 8-10, 14-33 and 37-45 are pending in this application. Claims 16-33 are withdrawn from consideration as being drawn to non-elected Groups. Rejoinder of claims 16-33 is respectfully requested.

By this Amendment, Figs. 2 and 8 are replaced pursuant to the attached drawing sheets, claims 6, 7, 11-13 and 34-36 are cancelled without prejudice to or disclaimer of the subject matter contained therein, the specification and claims 1-5, 8, 10, 14-16, 19, 23, 29, 37 and 39 are amended, and claims 40-45 are added.

Claims 1, 4, 5 and 15 are amended to recite features supported in the specification at, for example, page 28, lines 5-22 and Fig. 5. Claims 2, 3, 8, 10, 14, 16, 19, 23 and 29 are amended to correct minor informalities. Claims 37 and 39 are amended to depend from claim 4. Claim 40 is added to recite features supported in the specification at, for example, page 29, lines 19-23. Claims 41 and 45 are added to incorporate features from claims 4 and 5, respectively, and to both include features from claims 6 and 7. Claims 42-44 are added to correspond to features recited in claims 8-10, and to depend from new claim 41. No new matter is added by any of these amendments.

Reconsideration based on the following remarks is respectfully requested.

I. The Drawings Satisfy All Formal Requirements

The Office Action objects to the drawings based on informalities. Figures 2 and 8 are replaced pursuant to the attached drawing sheets. In particular, Applicant adds label 102, and replaces the cross-section legend "C-C" with substitute legend --D-D-- in Figs. 2 and 8, as requested by the Examiner.

In addition, Applicant corrects label "OLED" in Fig. 2. Withdrawal of the objection to the drawings is respectfully requested.

II. The Specification Satisfies All Formal Requirements

The Office Action objects to the specification based on informalities. The specification has been amended to obviate the objection. Regarding the objection for the values "x", "y" and "z" at page 19, line 11, Applicant respectfully asserts that these values represent numbers of atoms in the associated chemical formula, and are not associated with wavelengths.

Further, Applicant asserts that the relation x+y+z=1 is a reasonable representation of semiconductor materials for the formula $Si_xGe_yGa_zAs_z$, such as Si (x=1), Ge (y=1), and GaAs (z=1). The Office Action asserts that combinations of Group IV (*e.g.*, Si, Ge) and Group III-V (*e.g.*, Ga and As, respectively) are mutually exclusive. Applicant responds that such alleged incompatibility is not dispositive, because the values x, y and z include integer values, thereby restricting the formula to either Group IV elements or a Group III-IV pair. Thus, Applicant submits that documentation of the above-described material configurations is unnecessary, as these characteristics are well understood by artisans skilled in the art.

Moreover, the specification has been corrected for other informalities, not identified by the Examiner. Withdrawal of the objection to the specification is respectfully requested.

III. The Claims Satisfy All Formal Requirements

The Office Action objects to claims 8-10 and 14 based on informalities. Claims 6, 8-10, 13, 14, 18, 22 and 36 were amended in the February 13, 2003 Preliminary Amendment to remove multiple claim dependencies. Withdrawal of the claim objection is respectfully requested.

IV. The Claims Satisfy the Requirements under 35 U.S.C. §112, second paragraph

The Office Action rejects claims 1, 2, 14 and 15 under 35 U.S.C. §112, second paragraph, as being indefinite. Claims 1, 2, 14 and 15 have been amended to obviate this rejection in view of the Examiner's helpful comments. Withdrawal of the rejection under 35 U.S.C. §112, second paragraph is respectfully requested.

V. Claims 1-15 and 34-39 Define Patentable Subject Matter

The Office Action rejects claims 1, 2 and 4 under 35 U.S.C. §102(e) over U.S. Patent 6,781,155 to Yamada. This rejection is respectfully traversed.

Yamada does not teach or suggest an active matrix substrate including a plurality of electro-optical elements, comprising peripheral circuits to supply current to an electro-optical element of each pixel corresponding to the electro-optical elements, wherein each of the peripheral circuits comprises a holding element to hold a control voltage, a first active element, comprising a control terminal and a terminal, the control terminal being connected to the holding element, and the terminal being connected in series to the electro-optical element, to supply a current based on the control voltage to the electro-optical element, and a second active element, connected between the control terminal and the terminal of the first active element, wherein the second active element comprises a structure to prevent leakage currents during shutoff, as recited in claim 1, and similarly recited, *inter alia*, in claim 15. These reasons apply by extension to claim 2 based on its dependence from claim 1.

Further, Yamada fails to teach or suggest an active matrix substrate including a plurality of unit circuits arranged corresponding to intersections of a plurality of data lines and a plurality of scan lines, wherein each of the plurality of unit circuits comprises a first transistor, comprising a first control terminal, a first terminal, and a second terminal, the first terminal connected in series to an electro-optical element, a holding element comprising a first electrode connected to the first control terminal and a second electrode connected to the second terminal, and a second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, the third terminal being connected to one of the first terminal and the second terminal, and the fourth terminal being connected to the first control terminal, wherein the second transistor has a multi-gate structure, as recited in claim 4 and similarly recited in claim 5.

For example, the specification discloses various exemplary aspects of active element or transistors T1, T2, T3 and T4, a holding element or capacitor C, a data line Idata and a electro-optical light emitting element OLED shown, for example, in Fig. 5 and described, for example, at pages 28-29. The first (p) transistor T1 includes a source terminal connected to a power supply Vdd together with the capacitor C, a gate (or control terminal) connected to a source terminal of second (n) transistor T2 and to the capacitor C, and a drain terminal connected to a source terminal of the fourth (n) transistor T4 and to a drain terminal of the second (n) transistor T2, which is connected in series to the element OLED. The second (n) transistor T2 includes a gate connected to a write control line Vsel together with a gate of the third (n) transistor T3, which includes a source terminal connected to the data line Idata. The second (n) transistor T2 may incorporate a multigate structure.

Instead, Yamada discloses an organic EL display with a double-gate TFT. In particular, Yamada teaches first and second TFTs 130, 140, an organic EL element 160, and a storage capacitor 170. The EL element 160 includes an emissive layer (diode 163) sandwiched between an anode 161 and a cathode 162 that is connected to a common electrode 164. Yamada further teaches that the first TFT 130 has a double-gate structure and includes a gate electrode 131 connected to a gate signal line Gn, a drain electrode 132 connected to a drain signal line Dm and a source electrode 133. The second TFT 140 includes a gate electrode 141 connected to the source electrode 133, a source electrode 142 connected to the anode 161 and a drain electrode 143 connected to a driving power supply 150. The storage capacitor includes an electrode 171 connected between the (first) source electrode 133 and the (second) gate electrode 141, and another electrode 172 connected to another common electrode 173 (col. 1, lines 21-55 and Fig. 1 of Yamada).

Applicant asserts that Yamada fails to teach or suggest a first active element or transistor connected in series at a terminal to the electro-optical element, and a second active element connected between the first control terminal and the first terminal of the first active

element, as recited in claim 1. Similarly, Yamada fails to teach or suggest a first transistor having first and second terminals and a first control terminal, a holding element including a first electrode connected to the first control terminal and a second electrode connected to the second terminal, and a second transistor including third and fourth terminals and a second control terminal, the third terminal connected to either the first or second terminal, and the fourth terminal connected to the first control terminal, as recited in claim 4.

A claim must be literally disclosed for a proper rejection under §102. This requirement is satisfied "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference" (MPEP §2131). Applicant asserts that the Office Action fails to satisfy this requirement with Yamada.

The Office Action further rejects claims 3 and 5 under 35 U.S.C. §103(a) over Yamada in view of U.S. Patent Re 35,827 to Gualandris *et al.* (hereinafter "Gualandris"); claims 6, 7 and 15 under 35 U.S.C. §103(a) over Yamada in view of U.S. Patent Publication 2004-0207615 to Yumoto; claims 8-12, 37 and 39 under 35 U.S.C. §103(a) over Yamada in view of U.S. Patent Publication 2002-0008822 to Maeda; claims 13 and 14 under 35 U.S.C. §103(a) over Yamada in view of Maeda and further in view of Gualandris (with claim 14 included at page 27); claim 34 under 35 U.S.C. §103(a) over Yamada in view of U.S. Patent Publication 2001-0040565 to Koyama; claims 35 and 36 under 35 U.S.C. §103(a) over Yamada in view of Koyama and further in view of Maeda; and claim 38 under 35 U.S.C. §103(a) over Yamada in view of Maeda and further in view of U.S. Patent Publication 2001-0026835 to Tanaka. These rejections are rendered moot with respect to claims 6, 7, 11-13 and 34-36, and are respectfully traversed with respect to the remaining claims.

Gualandris, Yumoto, Maeda, Koyama, and Tanaka do not compensate for the deficiencies of Yamada outlined above for claims 1, 2 and 4. Nor do Gualandris, Yumoto, Maeda, Koyama and Tanaka teach, disclose or suggest the additional features recited in claims 3, 5-10, 14 and 15.

Instead, Gualandris discloses a surface field effect transistor. In particular, Gualandris teaches a MOSFET structure including a gate electrode 1 isolated by a gate oxide layer 2 on a silicon substrate 5 and flanked by source and drain areas 3 (col. 4, lines 7-24 and Fig. 1 of Gualandris). Thus, Gualandris fails to teach a terminal being connected in series to an electro-optical element, as provided in Applicant's claim 1 from which claim 3 depends. Nor does Gualandris teach a third terminal of a second transistor connected to either first or second terminals of a first transistor, and a fourth terminal of the second transistor connected to the first control terminal of the first transistor, as provided in Applicant's claim 5.

Yumoto discloses a current drive circuit. In particular, Yumoto teaches a pixel circuit including transistors TFT1 and TFT2 both having gates connected to each other and to a capacitor C, and transistors TFT3 and TFT4 both having gates connected to scan-A and scan-B lines respectively. Terminals of TFT1, TFT3 and TFT4 are connected together, while a terminal of TFT2 is connected to a light emitting element OLED (paragraphs [0064] – [0066] and Fig. 5 of Yumoto). Thus, Yumoto fails to teach a terminal being connected in series to an electro-optical element, as provided in Applicant's claim 15.

Maeda discloses a liquid crystal display panel. In particular, Maeda teaches an active matrix substrate 11 having a TFT 14 that includes a gate electrode 56 connected to a scan line 12, a source electrode 52 connected to a signal line 13, and a drain electrode 53 connected to a pixel electrode 15. Maeda further teaches forming the electrodes 52, 53 and the signal line 13 by successively sputtering and patterning films (paragraphs [0111] – [0014], [0125] and Figs. 10(a)-10(c) of Maeda). Thus, Maeda fails to teach a third terminal of a second transistor connected to either a first or second terminal of a first transistor, and a fourth terminal of the second transistor connected to the first control terminal of the first transistor, as provided in claim 4, from which claims 8-10, 37 and 39 depend. Maeda also does not teach a terminal being connected in series to an electro-optical element, as provided in Applicant's claim 15, as well as claim 1 from which claim 14 depends.

Tanaka discloses a semiconductor device manufacturing method. In particular, Tanaka teaches using an excimer laser for crystallizing and annealing a silicon film (paragraph [0053] and Figs. 1A and 1B of Tanaka). Thus, Tanaka lacks any teaching that compensates for the deficiencies of Yamada regarding the features of claim 4, from which claim 38 depends.

Further, there is no motivation to combine features related to the sandwiched EL layer of Yamada with the flanked MOSFET of Gualandris, the TFT gates connected to scan lines of Yumoto, the film sputtering method of Maeda and/or the laser processing method of Tanaka, nor has the Office Action established sufficient motivation for a *prima facie* case of obviousness. Even assuming that motivation to combine the applied references is established, the combination fails to teach or suggest Applicant's claimed features.

A *prima facie* case of obviousness for a §103 rejection requires satisfaction of three basic criteria: there must be some suggestion or motivation either in the references or knowledge generally available to modify the references or combine reference teachings, a reasonable expectation of success, and the references must teach or suggest all the claim limitations (MPEP §706.02(j)). Applicant asserts that the Office Action fails to satisfy these requirements with Yamada, Gualandris, Yumoto, Maeda and Tanaka.

For at least these reasons, Applicant respectfully asserts that the independent claims are now patentable over the applied references. The dependent claims are likewise patentable over the applied references for at least the reasons discussed, as well as for the additional features they recite. Consequently, all the claims are in condition for allowance. Thus, Applicant respectfully requests that the rejections under 35 U.S.C. §§102 and 103 be withdrawn.

VI. Conclusion

In view of the foregoing amendments and remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Gerhard W. Thielman
Registration No. 43,186

JAO:GWT/gwt

Attachment:
Replacement Drawing Sheets (Figs. 2 and 8)

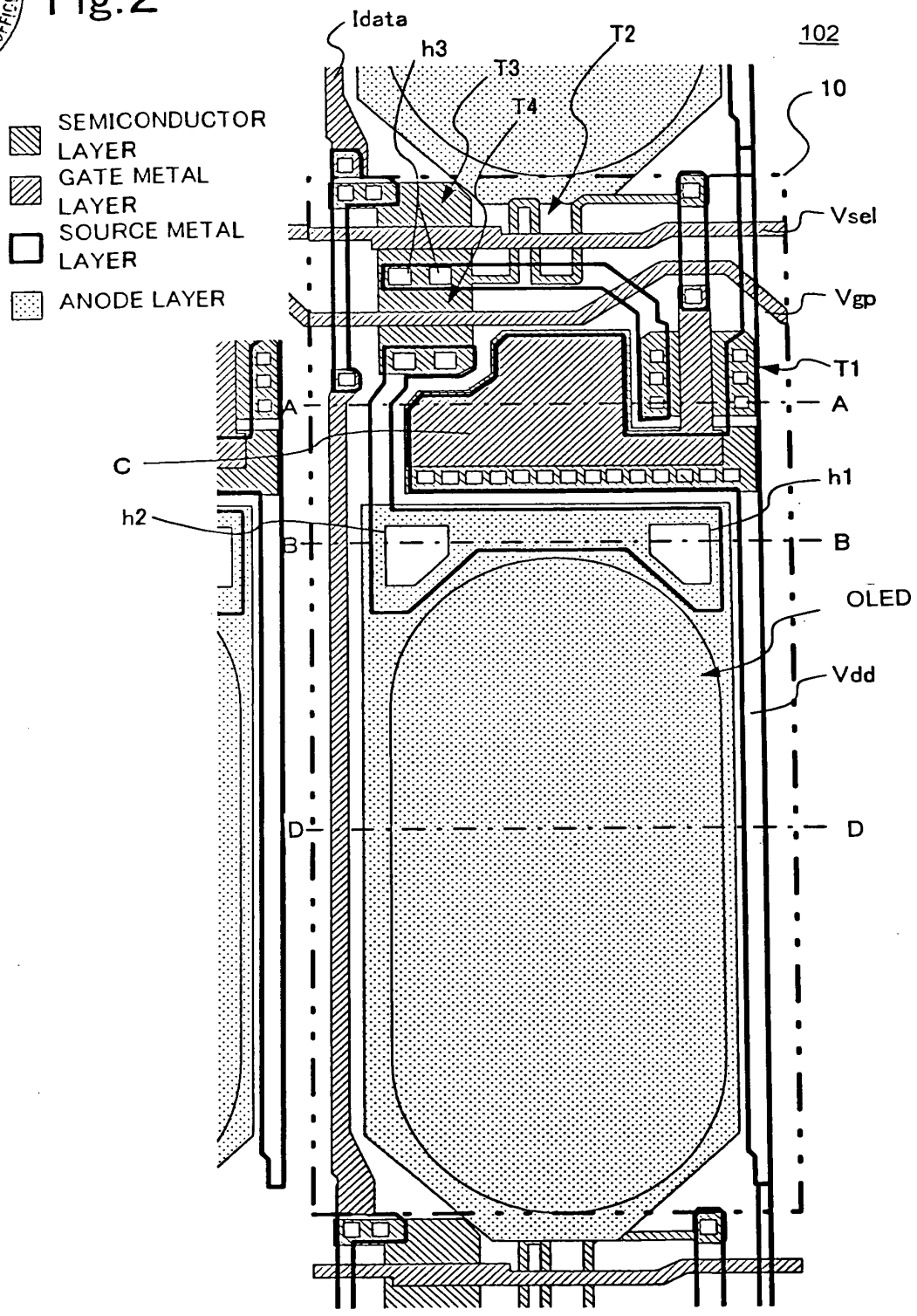
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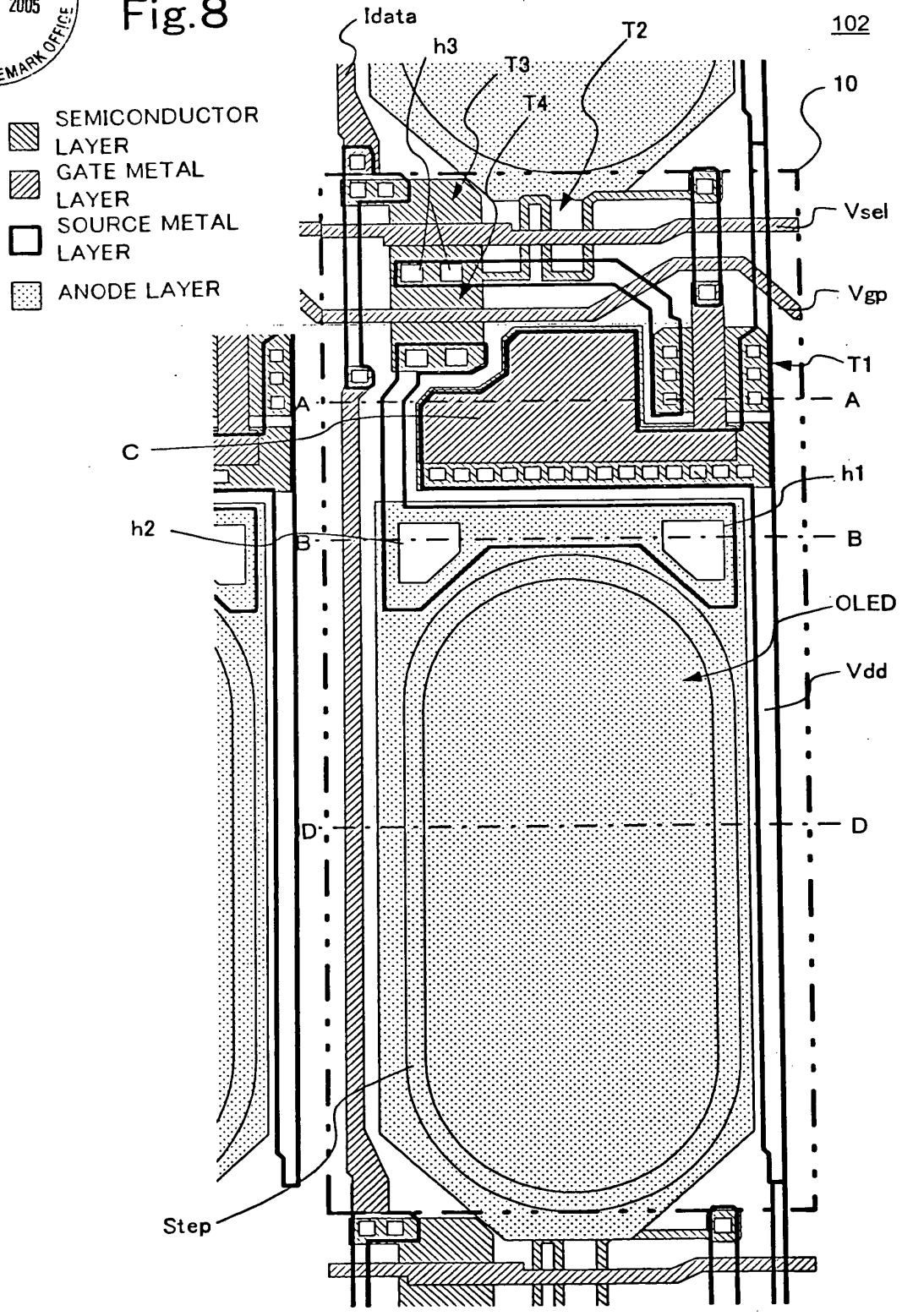
OIPE
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Fig.2



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Fig.8



Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	15870	LDD	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:19
S2	45103	"electro-optical" electrooptical	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:19
S3	3757098	element	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:20
S4	2	"6781155".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:21
S5	2	"6777255".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:20
S6	171475	Sanyo.as.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:20
S7	2	"6277679".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:34
S8	10578	DDD	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:34
S9	254	GDD	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:34
S10	1	S1 and S8 and S9 and "active matrix"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:34

S11	4	S1 and S8 and S9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:16
S12	35797	"active matrix"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:34
S13	1855360	substrate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:34
S14	39920	"first transistor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:16
S15	43582	"second transistor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:16
S16	18297	"third transistor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:16
S17	289209	"pixel" "unit cell" "unit circuit"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:17
S18	694	S14 and S15 and S16 and S17	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:18
S19	4	S14 and S15 and S16 and S18 and "1217"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:27
S20	512	S18 and "pixel"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:27

S21	205	S20 and "active matrix"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:28
S22	27	S21 and S2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:17
S23	151	"21" and (gate same metal same (scan with line))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18
S24	39920	"first transistor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18
S25	43582	"second transistor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18
S26	18297	"third transistor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18
S27	289209	"pixel" "unit cell" "unit circuit"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18
S28	694	S24 and S25 and S26 and S27	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18
S29	512	S28 and "pixel"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18
S30	205	S29 and "active matrix"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18

S31	1	S30 and (gate same metal same (scan with line))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:23
S32	6	S30 and ((gate same metal) and (scan with line))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:30
S33	152	(gate with metal) same ((scan with line) "scan line" "scan lines") same form$7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:31
S34	45103	"electro-optical" electrooptical	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:31
S35	35797	"active matrix"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:31
S36	10	S33 and S34 and S35	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:36
S37	986	capacitor same portion same (power with supply with line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/02 08:10
S38	160	capacitor same portion with (power near supply near line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/02 08:10
S39	86	capacitor with portion with (power near supply near line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/02 08:11
S40	9	capacitor with portion near (power near supply near line) not seiko.as. not epson.as.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/02 08:11

S41	9	capacitor with portion near (power near supply near line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/02 09:36
S42	182	laser near anneal$5 same recrystal$10 and polysilicon and TFT$	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/02 09:37
S43	7	S42 and layer and OLED	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/02 09:38
S44	1334	(345/76 345/77 345/78 345/79).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/12 17:26
S45	12373	(345/8? 345/9? 345/100 345/101 345/102 345/103 345/104 345/105).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/12 17:26

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/299,861	11/20/2002	Yojiro Matsueda	114251	5800

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EXAMINER	
WOODS, ERIC V	
ART UNIT	**PAPER NUMBER**
2672	

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/299,861	MATSUEDA, YOJIRO	
	Examiner	Art Unit	
	Eric V Woods	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,8-10,14,15 and 37-45* is/are pending in the application.

4a) Of the above claim(s) *16-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-10,14,15 and 37-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I (claims 1-15 and 34-39) in the reply filed on 25 March 2005 is acknowledged. The traversal is on the ground(s) that examiner is mistaken, but provides no arguments or evidence to support this conclusion. This is not found persuasive because there is no evidence or arguments to justify the request for rejoinder.

The requirement is still deemed proper and is therefore made **FINAL**.

Drawings

2. Examiner accepts the new drawing sheets and withdraws the previous objections to the drawings.

Specification

3. Examiner accepts the changes to the specification and withdraws the previous objections to the specification.

Response to Arguments

4. Applicant's arguments, see Page 3, filed 25 March 2005, with respect to the objections to the drawings and the specification have been fully considered and are persuasive.

The objections to the specification and drawings have accordingly been withdrawn.

The objections to claims 6, 8-10, 13, 14, 18, 22, and 36 have been withdrawn.

The rejections of claims 1, 2, 14, and 15 under 35 U.S.C. 112, second paragraph, are withdrawn.

The rejection of claims 1, 2, and 4 under 35 U.S.C. 102(e) under reference Yamada has been withdrawn due to applicant's amendment.

All rejections under 35 U.S.C. 103(a) have been withdrawn.

Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1-2, 4, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bird et al (US PGPub 2002/0067323 A1) in view of Yamada (US 6,781,155 B1).

7. As to claim 1, Bird shows in Fig. 5 a large, multi-pixel display [0019, 0042] with a plurality of electro-optical elements (LCD elements, see Fig. 5, element 84, and [0084-0089]) and support circuitry (Figs. 2 and 3) in active matrix format [0011] with driving capability, which inherently requires sending current to an electro-optical elements. Each peripheral circuit is shown in Figures 2 and 3, particularly the case of Fig. 3, where there is a holding element (capacitor) 36 that holds a control voltage (capacitors inherently hold voltage), with a first transistor (active element) 16 having a terminal that is connected in series with LCD element 18 (electro-optical element). The control terminal of first transistor 16 is connected through second transistor 28 to the other terminal, and second transistor 28 is between the two terminals, as recited in the claim.

The transistor is known to supply current to electro-optical element 18, as the electro-optical element is connected to either the source or drain, through which current prima facie passes [0041-0043, particularly 0042].

Yamada teaches an active matrix substrate (see Yamada Fig. 1, etc.), comprising peripheral circuits to supply current to an electro-optical element of each pixel corresponding to said electro-optical elements (assumed for purposes of examination to be the element in each pixel, as per 112 objection above), wherein each of said peripheral circuits comprises:

-A holding element (170, Fig. 1, Yamada (1:50-60)) to hold a control voltage;

-A first active element, connected to said holding element, to supply a current based on said control voltage to said electro-optical element (140, Fig. 1, Yamada (1:40-45)); and,

-A second active element, connected to said holding element, which controls the charging and discharging of said holding element (130, Fig. 1, Yamada (1:35-48)); and

-Wherein said active element comprises a structure to prevent leakage currents during shutoff (Yamada 3:5-15, 3:26-40).

Reference Bird teaches all the limitations above but does not expressly teach the use of a structure at the second active element to prevent leakage. Reference Yamada teaches most of the above limitations, including the use of a structure to prevent leakage as recited above. The references are analogous art and are directed to the same problem solving area, as they both are driving circuitry for electro-optical elements. Motivation for combination comes from the fact that preventing leakage current during shutoff is that leakage current causes increased power consumption and

prevents the display from switching in a rapid manner (e.g. various problems, see Yamada 2:15-32) where Yamada's structure solves that problem; thusly, the structure of Yamada would reduce the leakage current of Bird, which is silent on the subject.

8. As to claim 2, reference Bird does not expressly teach this limitation whilst reference Yamada does. Yamada in 3:26-40 shows a multi-gate structure in Fig. 1 with the second active element (130) having two gates (both labeled as 131)). Motivation is taken from the parent claim.

9. As to claim 4,

The rejection to claims 1 and 2 are herein incorporated by reference in their entirety.

References Bird and Yamada both teach an active matrix substrate with unit circuits (as discussed in the rejection to claim 1 above). Bird shows a plurality of scan lines in Figure 5, with one column connector 88 shown. Yamada shows these features (see Fig. 1 for illustration of this; 3:53-65; all transistors have number of terminals shown in cited figures)(see Fig. 1 and Fig. 4 that illustrate that the intended use is for a matrix display with multiple unit cells, which *prima facie* must have multiple data and scan lines to support multiple pixels)[note 5:35-45, where Fig. 4 is discussed – lines 51 and 52 are two different signal lines – drain and gate signal lines, thus fulfilling the recited "data line" and "scan line" requirements – scan lines are discussed in 3:62-65].

As discussed in claim 1, Bird and Yamada both teach a first transistor (which inherently has a source and a drain (those being first and second terminals) as well as a gate (first control terminal), with one terminal connected in series with an electro-optical

element. They are both connected in series with an electro-optical element at the first terminal.

Yamada teaches the recited multi-gate transistor structure, and in both cases the fourth terminal of the second transistor is connected to the first control terminal of the first transistor, while the other (third) terminal is connected to a terminal of the first transistor, even if through a holding element.

A capacitor inherently has two terminals, and a transistor inherently has three as shown in the various figures.

Now, the only substantial difference is that the Bird reference has the holding element connected to the first control terminal of the first transistor and to the first terminal through the second transistor, rather than through the second terminal of the first transistor. Yamada teaches a capacitor (holding element) with two terminals with one of them attached to the second terminal of the first transistor, and not the configuration of the Bird reference. As shown by the other patents that were cited or referenced in the first patent, the connection of the holding element to the second terminal of the first transistor is the conventional mechanism of connecting the capacitor. Further, applicant's own claim 1 is silent on this particular point – in that it would clearly allows for a holding element (capacitor) to be connected to either other terminal of the active device (transistor) in question and such a device would function. That being said, it is obvious that the choice of which terminal (first or second of the first transistor) to connect the second terminal of the holding element (capacitor) to are

obviously functionally equivalent (see MPEP 2144.03, case law, *In re Japikse,* 181 F.2d 1019, 86 USPQ 70 (CCPA 1950), and *In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975)) and thusly the placement of the second contact of the capacitor would be an issue of design choice. Further, the capacitor merely serves to hold charge and its placement on either side of the transistor does not change its function, and the fact remains that a transistor – either the first or second transistor (if the capacitor is connected as shown in Fig. 1 and Bird, then the second transistor; if connected as in Yamada, the first) must be turned on in order for current to pass through it, e.g. the first control terminal must have a voltage applied to it greater than the threshold voltage of the transistor, in order for the charge of the capacitor to actually be used. In both cases, the capacitor is still connected to the first control terminal of the transistor.

As such, while the capacitor is necessary, its placement (e.g. connection) on either side of the transistor does not change the leakage current, as the leakage current is regulated by the second transistor as applicant claims and recites. Thusly, the second connection of the transistor is design choice under both logic and common sense to one of ordinary skill in the field and under legal precedent, as rearranging the location of the parts does not change the function of the device, and finally as shown by applicant's own first claim (evidence claim and admission by applicant).

Motivation and combination, besides the above, are taken from claim 1.

10. As to claim 14, an electro-optical device comprising an active matrix substrate according to claim 1, and said electro-optical elements. (Yamada Fig. 4, element 60 – an OLED, which is *prima facie* an electro-optical device with an anode 61 (see 5:35-

60)). Since only the primary reference is used, no motivation or combination is necessary.

11. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as unpatentable over Bird in view of Yamada as applied to claim 1 above, and further in view of Gualandris *et al* (US Re. 35,827)('Gualandris').

12. As to claim 3,

The active matrix substrate according to claim 1, wherein at least said second active element is a transistor comprising a structure selected from the group consisting of an LDD structure, GDD structure, and DDD structure.

Yamada teaches in Fig. 5 that elements 13 and 13LD – discussed in 6:15-25 – have the LDD structure in the active transistor, and it is discussed as being the active layer *per se*, that is on top of the gate oxide, so it would work for any transistor as specified there. However, Yamada does not explicitly teach the use of GDD and DDD structures where Gualandris teaches DDD in 1:55-65, GDD in 2:25-30, and LDD in 2:25-30. Gualandris teaches that these are all methods of doping transistors, although one (the LDD) is preferred to work for 'ULSI' applications. Given that 'ULSI' applications at the time the patent was issued were mainly for deep sub-micron processes and that current TFT / liquid crystal display processes have much larger dimensions, e.g. still larger than one micron minimum channel length for silicon-on-glass technology, these techniques would be perfectly valid for use in TFT / silicon-on-glass technology.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix substrates of Yamada with the

transistors of Gualandris, since Yamada uses transistors, which *prima facie* have a source and a drain and different drain doping techniques are well-known in the art, and Yamada also teaches LDD mechanisms of doping, and the others would be obvious to a worker of ordinary skill in the art.

13. As to claim 5,

An active matrix substrate, comprising a plurality of unit circuits arranged corresponding to intersections of a plurality of data lines and a plurality of scan lines, wherein each of said plurality of unit circuits comprises (see Fig. 1 for illustration of this; 3:53-65; all transistors have number of terminals shown in cited figures))[note 5:35-45, where Fig. 4 is discussed – lines 51 and 52 are two different signal lines – drain and gate signal lines, thus fulfilling the recited "data line" and "scan line" requirements – scan lines are discussed in 3:62-65]:

-A first transistor, comprising a first control terminal, a first terminal, and a second terminal (140, Fig. 1, Yamada (1:40-45));

-A holding element, connected to said first control terminal, and comprising a first electrode and a second electrode (170, Fig. 1, Yamada (1:50-60)); and,

-A second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal and said fourth terminal being respectively connected to said first terminal and said first electrode (140, Fig. 1, Yamada (1:40-45)); and

-Wherein said second transistor has a multi-gate structure (see Fig. 1, element 130, 2 gates (131) are shown, and Yamada 3:26-40 for multi-gate structure).

Reference Yamada discloses the entirety of this invention in Fig. 1 with the LDD structure as cited above; however, the GDD and DDD structures are not taught by this reference. As discussed in claim 3 above, reference Gualandris discloses these structures for use with transistors and discusses them as being well known in the art in the first two columns. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix substrates of Yamada with the transistors of Gualandris, since Yamada uses transistors, which *prima facie* have a source and a drain and different drain doping techniques are well-known in the art.

14. Claims 8-10, 37, and 39-40 are rejected under 35 U.S.C. 103(a) as unpatentable over Bird in view of Yamada as applied to claim 4 above, and further in view of Maeda *et al* (US 2002/0008822 A1)('Maeda')[valid under 102(e)](claim 4 operative here – any of the other claims would be subject to the same rejection).

15. As to claim 8,

The active matrix substrate according to any of claims 4 through 7, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yamada 6:1-45 for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yamada 6:5-25); and

-A gate metal layer comprising said second control terminal (Yamada 6:40-45) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one scan line among said plurality of scan lines is formed in said gate metal layer (Maeda 0121).

References Yamada and Bird teach all the limitations of this claim except the formation of a scan line in the gate metal layer. Reference Maeda teaches the formation of scan lines and gate electrodes in the same metal film layer for TFT / LCD monitor fabrication (e.g. 0162, 0121). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yamada with the single metal layer of Maeda since Maeda performs in one step what Yamada does in several steps (note Yamada fabrication process in 6:1-67 and 7:1-50), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination, e.g. common sense is sufficient to justify the combination. See also *In re Karlson*, 136 USPQ 184 (CCPA 1963), for the doctrine that eliminating components is an obvious expedient – in this, eliminating fabrication steps.

16. As to claim 9,

The active matrix substrate according to any of claims 4 through 7, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yamada 6:1-45 for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yamada 6:5-25); and

-A gate metal layer comprising said second control terminal (Yamada 6:40-45) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in said gate metal layer (Maeda 0121 and 0113 and 0125).

References Yamada and Bird teach all the limitations of this claim except the formation of a data line in the gate metal layer. Reference Maeda teaches the formation of data lines and source and drain electrodes in the same metal film layer for TFT / LCD monitor fabrication (e.g. 0113, 0125). It would be *prima facie* obvious to choose to form gate electrodes and data lines simultaneously rather than gate electrodes and scan lines, for example. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yamada with the single metal layer of Maeda since Maeda performs in one step what Yamada does in several steps (note Yamada fabrication process in 6:1-67 and 7:1-50), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

17. As to claim 10,

The active matrix substrate according to any of claims 4 through 7, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yamada 6:1-45 for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yamada 6:5-25); and

-A gate metal layer comprising said second control terminal (Yamada 6:40-45) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-A source metal layer comprising a source electrode or drain electrode connected to the source or drain of said second transistor (Maeda 0113, 0125); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in the layer (Maeda 0121 and 0113 and 0125), among said source metal layer and said gate metal layer, which is closer to said semiconductor layer.

References Maeda and Bird in combination with Yamada teach all the limitations of this claim, and this is merely a recitation of the dual limitations of claims 8 and 9 above. As such, the combination and motivation from claim 8 is used here and no further comment is necessary, as this claim is only a nominal variation of the parent.

18. As to claim 37,

An active matrix substrate according to claim 4, comprising unit circuits comprising transistors, arranged corresponding to intersections of data lines and scan lines (Yamada Figs. 1 and 4 for example) wherein

-A semiconductor layer constituting such transistors is formed in a semiconductor layer (Yamada 6:5-25);

-Either said scan lines or said data lines are formed in a first conducting layer at the intersections of said scan lines and said data lines (Maeda 0113, 0121, and 0125); and,

-A portion of said scan lines and said data lines outside said intersections are formed in a second conducting layer (Maeda 0113, 0121, and 0125).

References Yamada and Bird do not explicitly teach the formation of scan or data lines formed in a conducting layer at the intersections of such lines. Reference Maeda describes forming gate metal and scan lines, etc. simultaneously. As such, the scan lines would be formed everywhere not masked with a shadow mask, e.g. both in the scan lines and in the intersections. No matter what portions of the lines are claimed, any such configuration could be made using shadow masking and formed using either evaporation or sputtering. Any set of contacts could be created using correctly etched contact holes; electrically contiguous metal formed in the same layer is *prima facie* the same from an electrical and an engineering perspective. Further, forming scan lines or data lines or portions thereof (as claimed) in the same layer as other things would simply be making a component integral by eliminating unnecessary metal, and under *In re Larson*, 144 USPQ 347 (CCPA 1965), making a component integral is obvious and not patentable. Therefore, under either methodology, the recited limitations of the claim have been met.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yamada with the single metal layer of Maeda since Maeda performs in one step what Yamada does in several steps (note Yamada fabrication process in 6:1-67 and 7:1-50), which is *prima facie* more efficient

and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

19. As to claim 39,

An electro-optical device according to claim 4, comprising electro-optical elements corresponding to intersections of scan lines and data lines (Yamada Figs. 1 and 4, element 60 for example (OLED)), wherein:

-A pair of electrodes is provided to supply power to electro-optical elements (Maeda Fig. 11C, elements 19 and 15 are opposing and pixel electrodes (see 0006-0008));

-At the intersections of said scan lines and said data lines, either said scan lines or said data lines are formed in a first conducting layer (Maeda 0113, 0118, 0121, 0125 – again, gate metal as discussed in rejections to claims 8-12);

-Portions of said scan lines and said data lines outside said intersections are formed in a second conducting layer (source metal layer, 0113, 0118, 0121, 0125 as discussed in rejections to claims 8-12); and,

-Said second conducting layer is positioned at a greater distance than said first conducting layer from one of said pair of electrodes (design choice issue, see Maeda Fig. 11C).

Reference Yamada does not recite details of the fabrication process claimed above. Reference Maeda teaches the fabrication of such substrates and teaches contact holes (0044, 0047). Logically, such contact holes would fill on conducting layer deposition, thus meeting the recited limitation concerning intersections of data and scan lines. The positioning of a layer or its size is *prima facie* obvious and is not patentable

(*In re Japikse* for order of parts and further under *In re Reese*, anyone of ordinary skill in the art would know that there would be an optimal spacing of electrodes from each other to minimize cross-talk that would also occupy the minimum aspect ratio required on the shadow mask).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yamada with the single metal layer of Maeda since Maeda performs in one step what Yamada does in several steps (note Yamada fabrication process in 6:1-67 and 7:1-50), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

20. As to claim 40, reference Yamada clearly teaches in 3:12-27 that the first transistor has a n-channel and that the second transistor has a p-channel, which are prima facie opposite polarities. Motivation and combination are taken from claim 39.

21. Claims 15 and 41 are rejected under 35 U.S.C. 103(a) as unpatentable over Bird in view of Yamada as applied to claim 4 above, and further in view of Yumoto (US PGPub 2004/0207615)('Yumoto')[valid under 102(e)]. The rejection to claim 1 is herein incorporated by reference in its entirety.

22. As to claim 15,

An electro-optical device including a plurality of electro-optical elements (see Yamada Fig. 1 and 4, Bird Fig. 2, the rejection to claim 1, etc.), comprising peripheral circuits (see Yamada Fig. 4 and Yumoto Figs. 7 and 11) to supply current to an electro-optical

element of each pixel corresponding to said electro-optical elements, wherein each of said peripheral circuits comprises:

-A light-emission control active element to supply said current to said electro-optical element during a light emission period (function served by recited first-active element; driving circuit can perform both tasks; see also TFT1 in Fig. 13, or in Fig. 12 the alternate structure, with TFT7, as a separate element);

-A holding element to hold a control voltage (170, Fig. 1, Yamada (1:50-60); Capacitor C in any of Figs. 11-15, Yumoto);

-A first active element, comprising a gate terminal and a terminal, a gate terminal of which is connected to said holding element, which supplies a current, based on said control voltage applied to the gate terminal, and said terminal being connected in series to said electro-optical element via said light-emission control active element (140, Fig. 1, Yamada (1:40-45); see also TFT1, in Figs. 11 and 12 in Yumoto or TFT5 in Fig. 11)(see also the rejection to claim 1, where the recited connections are shown to be present in the recited form, and it is prima facie obvious that the electro-optical element is in series with the transistor);

-A current-controlling active element, that passes data current via said first active element during a selection period (TFT4 or TFT3 in Yumoto Fig. 13); and,

-A second active element, connected between a first terminal to said current-controlling active element and said terminal and a second terminal to said holding element, which, during said selection period, charges said holding element and causes said control voltage to be stored (130, Fig. 1, Yamada (1:35-48); Yumoto – TFT1)(see the rejection

to claim 1, where this is shown to be in the combination of Yamada and Bird, and the connections between the elements are shown there in the format listed);

-Wherein said active element contains a structure to prevent leakage current during shutoff (Yamada 3:5-15, 3:26-40).

Reference Yamada teaches the general two-transistor structure along with current-controlling elements and structures to prevent leakage current during shutoff. Reference Yamada does not explicitly teach the other recited details of the claim. Yumoto teaches several different embodiments of peripheral structure for each pixel or unit circuit that contain all the recited elements as identified previously.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the two-transistor cell of Yamada with the multiple transistors of Yumoto, since both are aimed at active matrix panel applications (Yamada Fig. 1, Yumoto Fig. 2, etc.) and to prevent variation due to device parameters in cells similar to that of Yamada (Yumoto 0017). Furthermore, certain functionality that is split off in this claim, e.g. making the light-emission control active element separable from the driving TFT, and splitting off the current-controlling active elements, are obvious and not patentable under *Nerwin v. Erlichman*, 168 USPQ 177, 179 (PTO Bd. Of Int. 1969), since applicant is merely making separable items which are claimed as integral functions in earlier claims (For example, claims 1 and 4 used as evidence claims for this justification). Secondly, if the adjustable argument is made by applicant (that adding elements making those features adjustable), under *In re Stevens*, 101 USPQ 284

(CCPA 1954) that doctrine will not hold, in "that the provision of adjustability, when needed, is not a patentable advance."

23. As to claim 41, the rejection to claim 4 is incorporated by reference in its entirety, as this claim is a substantial duplicate. The only differences are discussed below.

A third transistor comprising a fifth terminal, a sixth terminal, and a third control terminal (third transistor disclosed in Fig. 5 Yumoto in unit pixel cell, 0064),

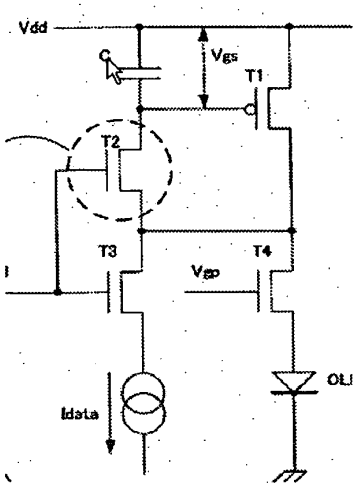
-Wherein said third control terminal is connected to one scan line among said plurality of scan lines (Yumoto 0064, Fig. 5: TFT4 is connected to scanB and TFT3 is connected to scanA; let TFT3 be the third transistor), and

-Said fifth terminal is connected to one data line among said plurality of data lines (Yumoto 0064, Fig. 5: TFT3 connected to data line).

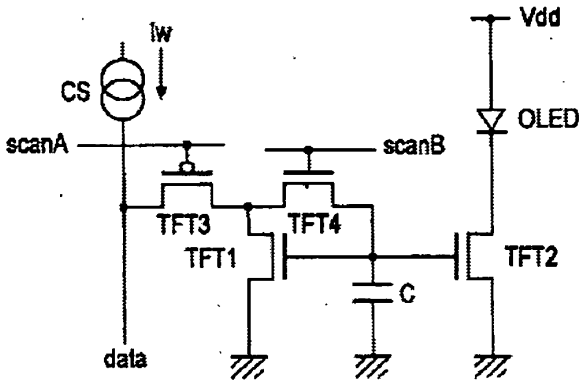
Wherein said sixth terminal is connected to said third terminal and to said first terminal.

Reference Yamada does not teach the third transistor. Yumoto discloses in Figure 5 the use of a four-transistor cell. If transistor TFT1 is removed, then the claimed invention is precisely the same as applicant recites in claim 7, with the same connections. As both the multi-gate variant and the single gate variants of the second transistor are claimed, both will be briefly addressed. If the multi-gate transistor of Yamada – shown in Fig. 1 and discussed in the rejection to claim 5, is used in place of TFT4 shown in Yumoto Fig. 5, the result will be exactly the invention recited by applicant. If only one gate is used on the second transistor, then no modification is necessary and again the invention recited in claim 7 is obtained. See images below.

Reference Yamada teaches all the limitations of the claim except the use of a third transistor and its connections. Reference Yumoto teaches the use of additional transistors with the standard two-transistor TFT cells with the recited connections.



Applicant's invention - Figure 5



Yumodo Fig. 5

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the two-transistor cell of Yamada with the multiple transistors of Yumoto, since both are aimed at active matrix panel applications (Yamada Fig. 1, Yumoto Fig. 2, etc.) and to prevent variation due to device parameters in cells similar to that of Yamada (Yumoto 0017).

24. Claim 38 is rejected over Bird in view of Yamada and Maeda as applied to claim 37 above, and further in view of Tanaka (US PGPub 2001/0026835 A1)('Tanaka')(valid under 102(e)).

25. As to claim 38,

The active matrix substrate according to claim 37, wherein said second conducting layer is positioned between said first conducting layer and said semiconductor layer.

Reference Yamada does not explicitly teach this limitation. In Fig. 10B, Maeda shows that the bottom gate – element 56, which is metal (a niobium alloy) is put down first, then various insulating materials, then element 13 (source and drain electrodes) are formed on the same level and slightly covering the semiconductor layer 54. Under the doctrine of *In re Japikse*, switching the two layers would be *prima facie* obvious, and only minor alternations in the shadow masks for the process would be necessary (additive vs. subtractive processing in semiconductors, for example, switching the process would not be difficult for one of ordinary skill in the semiconductor / TFT art). Again, given that Maeda teaches many different embodiments (see Figs. 10-13, etc.), such a switch would be a design choice issue, and it would allow low-temperature processing of the substrate throughout the process, particularly allowing for newer techniques such as laser annealing and recrystallization of the semiconductor layer taught by Tanaka, and treatment of the semiconductor layer towards the end of processing.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the TFT circuits of Yamada and Maeda with the laser annealing processing of polysilicon for TFT applications of Tanaka (see 0002-0015), as both Yamada (2:61-67) and Maeda (0008, 0121, etc.) utilize polysilicon as the semiconductor material, and laser annealing is now a well-known, standard process in the art.

26. Claims 42-44 are rejected under 35 U.S.C. 103(a) as unpatentable over Bird in view of Yamada and Yumoto as applied to claim 41 above, and further in view of Maeda *et al* (US 2002/0008822 A1)('Maeda')[valid under 102(e)](claim 4 operative here – any of the other claims would be subject to the same rejection).

27. As to claim 42,

The active matrix substrate according to claim 41, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yamada 6:1-45 for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yamada 6:5-25); and

-A gate metal layer comprising said second control terminal (Yamada 6:40-45) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one scan line among said plurality of scan lines is formed in said gate metal layer (Maeda 0121).

References Yamada and Bird teach all the limitations of this claim except the formation of a scan line in the gate metal layer. Reference Maeda teaches the formation of scan lines and gate electrodes in the same metal film layer for TFT / LCD monitor fabrication (e.g. 0162, 0121). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yamada with the single metal layer of Maeda since Maeda performs in one step what

Yamada does in several steps (note Yamada fabrication process in 6:1-67 and 7:1-50), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination, e.g. common sense is sufficient to justify the combination. See also *In re Karlson*, 136 USPQ 184 (CCPA 1963), for the doctrine that eliminating components is an obvious expedient – in this, eliminating fabrication steps.

28. As to claim 43,

The active matrix substrate according to claim 41, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yamada 6:1-45 for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yamada 6:5-25); and

-A gate metal layer comprising said second control terminal (Yamada 6:40-45) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in said gate metal layer (Maeda 0121 and 0113 and 0125).

References Yamada, Yumoto, and Bird teach all the limitations of this claim except the formation of a data line in the gate metal layer. Reference Maeda teaches the formation of data lines and source and drain electrodes in the same metal film layer for TFT / LCD monitor fabrication (e.g. 0113, 0125). It would be *prima facie* obvious to choose to form gate electrodes and data lines simultaneously rather than gate

electrodes and scan lines, for example. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yamada with the single metal layer of Maeda since Maeda performs in one step what Yamada does in several steps (note Yamada fabrication process in 6:1-67 and 7:1-50), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

29. As to claim 44,

The active matrix substrate according to claim 41, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yamada 6:1-45 for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yamada 6:5-25); and

-A gate metal layer comprising said second control terminal (Yamada 6:40-45) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-A source metal layer comprising a source electrode or drain electrode connected to the source or drain of said second transistor (Maeda 0113, 0125); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in the layer (Maeda 0121 and 0113 and 0125), among said source metal layer and said gate metal layer, which is closer to said semiconductor layer.

References Maeda and Bird in combination with Yamada teach all the limitations of this claim, and this is merely a recitation of the dual limitations of claims 42 and 43 above. As such, the combination and motivation from claim 42 is used here and no further comment is necessary, as this claim is only a nominal variation of the parent.

30. Claim 45 is rejected under 35 U.S.C. 103(a) as unpatentable over Bird in view of Yamada and Yumoto as applied to claim 41 above, and further in view of Gualandris *et al* (US Re. 35,827)('Gualandris'). The rejection to claim 41 is herein incorporated by reference in its entirety.

31. Claim 45 is a substantial duplicate of claim 41, with the only difference being the addition of the limitation from claim 3:

Wherein at least said second active element is a transistor comprising a structure selected from the group consisting of an LDD structure, GDD structure, and DDD structure.

Yamada teaches in Fig. 5 that elements 13 and 13LD – discussed in 6:15-25 – have the LDD structure in the active transistor, and it is discussed as being the active layer *per se*, that is on top of the gate oxide, so it would work for any transistor as specified there. However, Yamada does not explicitly teach the use of GDD and DDD structures where Gualandris teaches DDD in 1:55-65, GDD in 2:25-30, and LDD in 2:25-30. Gualandris teaches that these are all methods of doping transistors, although one (the LDD) is preferred to work for 'ULSI' applications. Given that 'ULSI' applications at the time the patent was issued were mainly for deep sub-micron processes and that current TFT / liquid crystal display processes have much larger dimensions, e.g. still

larger than one micron minimum channel length for silicon-on-glass technology, these techniques would be perfectly valid for use in TFT / silicon-on-glass technology.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix substrates of Yamada, Bird, and Yumoto with the transistors of Gualandris, since Yamada uses transistors, which *prima facie* have a source and a drain and different drain doping techniques are well-known in the art, and Yamada teaches at least one variant (LDD) of this technology.

Conclusion

32. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric V Woods whose telephone number is 571-272-7775. The examiner can normally be reached on M-F 7:30-4:30 alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on 571-272-7664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eric Woods

April 13, 2005

JEFFERY BRIER
PRIMARY EXAMINER

Notice of References Cited	Application/Control No. 10/299,861	Applicant(s)/Patent Under Reexamination MATSUEDA, YOJIRO	
	Examiner Eric V Woods	Art Unit 2672	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-RE35,827	06-1998	Gualandris et al.	257/285
	B	US-6,781,155 B1	08-2004	Yamada, Tsutomu	257/72
	C	US-2001/0026835	10-2001	Tanaka, Koichiro	427/96
	D	US-2001/0040565	11-2001	Koyama, Jun	345/204
	E	US-2002/0008822	01-2002	Maeda, Akitoshi	349/139
	F	US-2002/0067323	06-2002	Bird et al.	345/87
	G	US-2004/0207615	10-2004	Yumoto, Akira	345/211
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims

Application No.	Applicant(s)
10/299,861	MATSUEDA, YOJIRO
Examiner	**Art Unit**
Eric V Woods	2672

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	4/13/05
	1	√
	2	√
	3	√
	4	√
	5	√
	6	–
	7	–
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	9	√
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Claim		Date
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BIBDATASHEET

Bib Data Sheet

CONFIRMATION NO. 5800

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/299,861	11/20/2002 RULE	345	2672	114251

APPLICANTS

Yojiro Matsueda, Chino-shi, JAPAN;

** CONTINUING DATA **********

** FOREIGN APPLICATIONS **********

JAPAN 2001-356007 11/21/2001 EW
JAPAN 2001-371403 12/05/2001 EW
JAPAN 2001-371410 12/05/2001 EW

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 02/10/2003

Foreign Priority claimed	STATE OR	SHEETS	TOTAL	INDEPENDENT
☑ yes ☐ no				
35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance				
Verified and Acknowledged Examiner's Signature Initials	COUNTRY	DRAWING	CLAIMS	CLAIMS
	JAPAN	15	39	16

ADDRESS
25944
OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA , VA
22320

TITLE
Active matrix substrate, electro-optical device, and electronic device

FILING FEE RECEIVED	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue)

Search Notes

Application No.	Applicant(s)	
10/299,861	MATSUEDA, YOJIRO	
Examiner	**Art Unit**	
Eric V Woods	2672	

SEARCHED

Class	Subclass	Date	Examiner
345	76-105	4/12/2005	EW

INTERFERENCE SEARCHED

Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)

	DATE	EXMR
EAST (see attached)	4/12/2005	EW

Interview Summary	Application No.	Applicant(s)	
	10/299,861	MATSUEDA, YOJIRO	
	Examiner	Art Unit	
	Eric V. Woods	2672	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Eric V. Woods*. (3)*Almis Jankus*.

(2) *Jerry Tillman (43,186)*. (4)_____.

Date of Interview: *26 June 2005*.

Type: a)☐ Telephonic b)☐ Video Conference
c)☒ Personal [copy given to: 1)☐ applicant 2)☒ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____.

Claim(s) discussed: *1,4,5 and 15*.

Identification of prior art discussed: *Yamada, Bird, Maeda*.

Agreement with respect to the claims f)☐ was reached. g)☒ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *See Continuation Sheet*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN ONE MONTH FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

ALMIS R. JANKUS
PRIMARY EXAMINER

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

_____
Examiner's signature, if required

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)
In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Continuation of Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: Applicant's representative proposed claim amendments to independent claims 1, 4, and 15 primarily focused on claim 4, with respect to the configuration of the transistors shown in Fig. 5 of the drawings of the instant application, primarily focused on adding the third transistor in series, which examiner noted would overcome the prior art of record and clarified issues concerning electro-optical elements. Additional embodiments were also discussed, including T3 (the second, non multi-gate transistor on the left in Fig. 5. Any new amendments to that effect are likely to introduce new issues and require new search, and thusly would likely not be entered after final.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/299,861	11/20/2002	Yojiro Matsueda	114251	5800

25944 7590 07/12/2005

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
WOODS, ERIC V	
ART UNIT	**PAPER NUMBER**
2672	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Interview Summary	Application No.	Applicant(s)	
	10/299,861	MATSUEDA, YOJIRO	
	Examiner	Art Unit	
	Eric V. Woods	2672	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Eric V. Woods*. (3)_____.

(2) *Jerry Tillman (43,186)*. (4)_____.

Date of Interview: *30 June 2005*.

Type: a)☒ Telephonic b)☐ Video Conference
c)☐ Personal [copy given to: 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____.

Claim(s) discussed: *4,15 and 41*.

Identification of prior art discussed: *Yumoto, Yamada, Maeda, Bird*.

Agreement with respect to the claims f)☐ was reached. g)☒ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *Applicant wanted examiner's input to clarify certain questions concerning the prior art of record, e.g. what combinations of amended limitations would overcome the prior art of record, particularly with respect to various combinations of the third active element or current-controlling element and changing the electro-optical element limitation to be an OLED*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN ONE MONTH FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

Jeffrey A. Brier

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

Examiner's signature, if required

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)
In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

OIPE JC104 JUL 13 2005 PATENT & TRADEMARK OFFICE

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA	Group Art Unit: 2672
Application No.: 10/299,861	Examiner: E. WOODS
Filed: November 20, 2002	Docket No.: 114251
For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE	**MAIL STOP RCE**

LARGE ENTITY REQUEST FOR CONTINUED EXAMINATION UNDER 37 CFR §1.114

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 CFR §1.114, Applicant hereby requests continued examination.

☒ Applicant further requests entry and consideration of the attached submission.

The above-identified application was filed on or after June 8, 1995. Thus, entry is proper under 37 CFR §1.114(d).

Attached hereto is our check no. 168659 in the amount of ☒ $790.00 as payment of the fees set forth in 37 CFR §1.17(e). The Commissioner is hereby authorized to charge any additional fees or credit any overpayment associated with this communication to Deposit Account No. 15-0461. Two duplicate copies of this page are enclosed.

Respectfully submitted,

07/14/2005 SZEWDIE1 00000058 10299861
01 FC:1801 790.00 OP

James A. Oliff
Registration No. 27,075

Gerhard W. Thielman
Registration No. 43,186

JAO:GWT/gwt

Date: July 13, 2005

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461



PATENT APPLICATION

RESPONSE UNDER 37 CFR §1.114
EXPEDITED PROCEDURE
TECHNOLOGY CENTER ART UNIT 2672

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA — Group Art Unit: 2672

Application No.: 10/299,861 — Examiner: E. WOODS

Filed: November 20, 2002 — Docket No.: 114251

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE

AMENDMENT SUBMISSION UNDER 37 CFR §1.114

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the April 19, 2005 Final Office Action, and further to the June 27, 2005 personal interview between Applicant's representative and Examiners Woods and Jankus, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An active matrix substrate including a plurality of electro-optical elements, comprising peripheral circuits to supply current to an electro-optical element of each pixel corresponding to said electro-optical elements, wherein each of said peripheral circuits comprises:

a holding element to hold a control voltage;

a first active element, comprising a control terminal and a terminal, said control terminal being connected to said holding element, and said terminal being connected in series to said electro-optical element, to supply a current based on said control voltage to said electro-optical element; ~~and~~

a second active element, connected between said control terminal and said terminal of said first active element; and

a third active element, connected between said terminal of said first active element and a data line,

wherein said second active element comprises a structure to prevent leakage currents during shutoff, and said electro-optical element is an electroluminescence element.

2. (Previously Presented) The active matrix substrate according to claim 1, wherein said second active element is configured as a multi-gate active element.

3. (Previously Presented) The active matrix substrate according to claim 1, wherein at least said second active element is a transistor comprising a structure selected from the group consisting of an LDD structure, a GDD structure, and a DDD structure.

4. (Currently Amended) An active matrix substrate, comprising a plurality of unit circuits arranged corresponding to intersections of a plurality of data lines and a plurality of scan lines, wherein each of said plurality of unit circuits comprises:

a first transistor, comprising a first control terminal, a first terminal, and a second terminal, said first terminal connected in series to an electro-optical element;

a holding element, connected to said first control terminal, and comprising a first electrode connected to said first control terminal and a second electrode connected to said second terminal; ~~and~~

a second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal being connected to one of said first terminal and said second terminal, and said fourth terminal being connected to said first control terminal; and

a third transistor, comprising a fifth terminal, a sixth terminal, and a third control terminal, said fifth terminal being connected to a data line of said plurality of data lines, and said sixth terminal being connected to said third terminal;

wherein said second transistor has a multi-gate structure, and said electro-optical element is an electroluminescence element.

5. (Currently Amended) An active matrix substrate, comprising a plurality of unit circuits arranged corresponding to intersections of a plurality of data lines and a plurality of scan lines, wherein each of said plurality of unit circuits comprises:

a first transistor, comprising a first control terminal, a first terminal, and a second terminal, said first terminal connected in series to an electro-optical element;

a holding element, connected to said first control terminal, and comprising a first electrode connected to said first control terminal and a second electrode connected to said second terminal; ~~and~~

a second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal being connected to one of said first terminal and said second terminal, and said fourth terminal being connected to said first control terminal; and

a third transistor, comprising a fifth terminal, a sixth terminal, and a third control terminal, said fifth terminal being connected to a data line of said plurality of data lines, and said sixth terminal being connected to said third terminal;

wherein said second transistor is a transistor comprising a structure selected from the group consisting of an LDD structure, a GDD structure, and a DDD structure, and said electro-optical element is an electroluminescence element.

6-7. (Cancelled)

8. (Previously Presented) The active matrix substrate according to claim 4, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed; and

a gate metal layer comprising said second control terminal, and

wherein at least a portion of said plurality of scan lines is formed in said gate metal layer.

9. (Previously Presented) The active matrix substrate according to claim 4, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed; and

a gate metal layer comprising said second control terminal; and

wherein at least a portion of one data line among said plurality of data lines is formed in said gate metal layer.

10. (Previously Presented) The active matrix substrate according to claim 4, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed;

a gate metal layer comprising said second control terminal; and

a source metal layer comprising a source electrode or drain electrode connected to the source or drain of said second transistor;

wherein at least one portion of at least one data line among said plurality of data lines is formed in the layer, among said source metal layer and said gate metal layer, that is closer to said semiconductor layer.

11-13. (Cancelled)

14. (Previously Presented) An electro-optical device comprising an active matrix substrate according to claim 1, and said electro-optical elements.

15. (Currently Amended) An electro-optical device including a plurality of electro-optical elements, comprising peripheral circuits to supply current to an electro-optical element of each pixel corresponding to said electro-optical elements,

wherein each of said peripheral circuits comprises:

a light-emission control active element to supply said current to said electro-optical element during a light emission period;

a holding element to hold a control voltage;

a first active element comprising a gate terminal and a terminal, said gate terminal being connected to said holding element that supplies a current, based on said control voltage applied to the gate terminal, and said terminal being connected in series to said electro-optical element via said light-emission control active element;

a current-controlling active element, that passes data current via said first active element during a selection period, said current-controlling element being connected between said terminal of said first active element and a data line; and

a second active element, connected between a first terminal to said current-controlling active element and said terminal and a second terminal to said holding element and said control terminal, that, during said selection period, charges said holding element and causes said control voltage to be stored,

wherein said second active element comprises a structure to prevent leakage currents during shutoff, and said electro-optical element is an electroluminescence element.

16. (Withdrawn) An electro-optical device, comprising electro-optical elements and peripheral circuitry that drives said electro-optical elements,

wherein said electro-optical elements are formed such that a boundary of the electro-optical elements has, at least, a prescribed curvature; and

at least one portion of said peripheral circuitry is formed in the region surrounded by the boundary having the specified curvature and by the boundaries of a polygon circumscribing the electro-optical element.

17. (Withdrawn) The electro-optical device according to claim 16, wherein a plurality of boundary portions having said prescribed curvature are formed.

18. (Withdrawn) The electro-optical device according to claim 16, wherein said plurality of formed boundary portions are arranged substantially symmetrically with respect to a center line passing through the geometric center of said electro-optical element.

19. (Withdrawn) An electro-optical device, comprising a light-emitting portion and a peripheral circuit that controls the current supplied to said light-emitting portion, by means of a pixel electrode, wherein:

the area of said light-emitting portion is smaller than the area of said pixel electrode; and,

the shape of said light-emitting portion and the shape of said pixel electrode are different.

20. (Withdrawn) An electro-optical device, comprising a light-emitting portion and a peripheral circuit that controls the current supplied to said light-emitting portion, by means of a pixel electrode, wherein:

the area of said light-emitting portion is smaller than the area of said pixel electrode; and

the shape of said light-emitting portion is a shape having a curvature, and the shape of said pixel electrode is a polygonal shape.

21. (Withdrawn) An electro-optical device, comprising a light-emitting portion and a peripheral circuit that controls the current supplied to said light-emitting portion, by means of a pixel electrode, wherein:

the area of said light-emitting portion is smaller than the area of said pixel electrode;

said light-emitting portion has a polygonal shape having n vertices (where n is an integer greater than or equal to 4);

said pixel electrode has a polygonal shape having m vertices (where m is an integer greater than or equal to 3); and

the relation n>m obtains.

22. (Withdrawn) The electro-optical device according to claim 19, wherein the entire region of said light-emitting portion is formed on said pixel electrode, and a contact region for connection of said peripheral circuit and said pixel electrode is provided in a portion of said pixel electrode in which said light-emitting portion is not formed.

23. (Withdrawn) An electro-optical device, comprising:

an electro-optical element;

a holding capacitance, constituted by a plurality of layers including electrodes, that regulates a current supplied to said electro-optical element; and

an active element that supplies current to said electro-optical element according to the electric charge amount held in said holding capacitance;

wherein a first electrode constituting said holding capacitance is formed by patterning a portion of a metal layer comprising a power supply line that supplies current to said electro-optical element.

24. (Withdrawn) The electro-optical device according to claim 23, wherein a second electrode constituting said holding capacitance is formed by patterning a portion of a metal layer comprising a control terminal of said active element.

25. (Withdrawn) The electro-optical device according to claim 23, wherein said first electrode is a portion of said power supply line, and a portion of a metal layer forming a control terminal of said active element is superposed on a portion of said power supply line and patterned to form said second electrode.

26. (Withdrawn) The electro-optical device according to claim 23, comprising a semiconductor layer below said first electrode and said second electrode.

27. (Withdrawn) The electro-optical device according to claim 25, wherein the region occupied by a layer positioned on the lower side among the layers constituting electrodes of said holding capacitance is formed to be larger than the region occupied by a layer positioned on the upper side.

28. (Withdrawn) The electro-optical device according to claim 27, wherein the region occupied by said layer positioned on the lower side is pattern-formed in a shape such that, even if the maximum possible position shift occurs at the time of formation of said layer positioned on the upper side, the region of the layer positioned on the upper side is contained within the region of said layer positioned on the lower side.

29. (Withdrawn) An electro-optical device, comprising a plurality of layers including electrodes, configured such that a current can be supplied by an active element according to a voltage stored in a holding capacitance to an electro-optical element that emits light through the application of an electric field between the electrodes, comprising:

a first metal layer, constituting a power supply line; and

a second metal layer, formed in a pattern including a portion of a control terminal of said active element; and

wherein one electrode constituting said holding capacitance is formed by patterning one portion of said first metal layer.

30. (Withdrawn) The electro-optical device according to claim 29, wherein the other electrode constituting said holding capacitance is formed by patterning one portion of said second metal layer.

31. (Withdrawn) The electro-optical device according to claim 29, wherein one electrode constituting said holding capacitance is one portion of said power supply line, and

said other electrode is formed by superposing a portion of said second metal layer on a portion of the power supply line and patterning.

32. (Withdrawn) The electro-optical device according to claim 29, wherein the region occupied by a layer positioned on the lower side among the layers comprising said holding capacitance electrodes is formed to be larger than the region occupied by a layer positioned on the upper side.

33. (Withdrawn) The electro-optical device according to claim 32, wherein the region occupied by said layer positioned on the lower side is pattern-formed in a shape such that, even if the maximum possible position shift occurs at the time of formation of said layer positioned on the upper side, the region of the layer positioned on the upper side is contained within the region of said layer positioned on the lower side.

34-36. (Cancelled)

37. (Previously Presented) The active matrix substrate in accordance with claim 4, comprising unit circuits comprising transistors, arranged corresponding to intersections of data lines and scan lines; wherein

a semiconductor film constituting said transistors is formed in a semiconductor layer;

either said scan lines or said data lines are formed in a first conducting layer at the intersections of said scan lines and said data lines; and

a portion of said scan lines and said data lines outside said intersections are formed in a second conducting layer.

38. (Original) The active matrix substrate according to claim 37, wherein said second conducting layer is positioned between said first conducting layer and said semiconductor layer.

39. (Previously Presented) The electro-optical device according to claim 4, comprising electro-optical elements corresponding to intersections of scan lines and data lines, wherein:

a pair of electrodes is provided to supply power to said electro-optical elements;

at the intersections of said scan lines and said data lines, either said scan lines or said data lines are formed in a first conducting layer;

portions of said scan lines and said data lines outside said intersections are formed in a second conducting layer; and

said second conducting layer is positioned at a greater distance than said first conducting layer from one of said pair of electrodes.

40. (Previously Presented) The active matrix substrate in accordance with claim 1, wherein said first and second active elements have opposite polarities.

41. (Currently Amended) An active matrix substrate, comprising a plurality of unit circuits arranged corresponding to intersections of a plurality of data lines and a plurality of scan lines, wherein each of said plurality of unit circuits comprises:

a first transistor, comprising a first control terminal, a first terminal, and a second terminal, said first terminal connected in series to an electro-optical element;

a holding element, connected to said first control terminal, and comprising a first electrode connected to said first control terminal and a second electrode connected to said second terminal;

a second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal being connected to one of said first terminal and said second terminal, and said fourth terminal being connected to said first control terminal; and

a third transistor to control current to the holding element, the third transistor comprising a fifth terminal, a sixth terminal, and a third control terminal, wherein

said second transistor has a multi-gate structure,

said third control terminal is connected to one scan line among said plurality of scan lines,

said fifth terminal is connected to one data line among said plurality of data lines, ~~and~~

said sixth terminal is connected to said third terminal and to said first terminal, and

said electro-optical element is an electroluminescence element.

42. (Previously Presented) The active matrix substrate according to claim 41, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed; and

a gate metal layer comprising said second control terminal, and

wherein at least a portion of said plurality of scan lines is formed in said gate metal layer.

43. (Previously Presented) The active matrix substrate according to claim 41, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed; and

a gate metal layer comprising said second control terminal; and

wherein at least a portion of one data line among said plurality of data lines is formed in said gate metal layer.

44. (Previously Presented) The active matrix substrate according to claim 41, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed;

a gate metal layer comprising said second control terminal; and

a source metal layer comprising a source electrode or drain electrode connected to the source or drain of said second transistor; and

wherein at least one portion of at least one data line among said plurality of data lines is formed in the layer, among said source metal layer and said gate metal layer, that is closer to said semiconductor layer.

45. (Currently Amended) An active matrix substrate, comprising a plurality of unit circuits arranged corresponding to intersections of a plurality of data lines and a plurality of scan lines, wherein each of said plurality of unit circuits comprises:

a first transistor, comprising a first control terminal, a first terminal, and a second terminal, said first terminal connected in series to an electro-optical element;

a holding element, connected to said first control terminal, and comprising a first electrode connected to said first control terminal and a second electrode connected to said second terminal;

a second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal being connected to one of said first terminal and

said second terminal, and said fourth terminal being connected to said first control terminal; and

a third transistor to control current to the holding element, the third transistor comprising a fifth terminal, a sixth terminal, and a third control terminal,

wherein said second transistor is a transistor comprising a structure selected from the group consisting of an LDD structure, a GDD structure, and a DDD structure;

said second transistor has a multi-gate structure,

said third control terminal is connected to one scan line among said plurality of scan lines,

said fifth terminal is connected to one data line among said plurality of data lines, ~~and~~

said sixth terminal is connected to said third terminal and to said first terminal, and

said electro-optical element is an electroluminescence element.

REMARKS

Claims 1-5, 8-10, 14-33 and 37-45 are pending in this application. Claims 16-33 are withdrawn from consideration as being drawn to non-elected Groups. Rejoinder of claims 16-33 is respectfully requested.

By this Amendment, claims 1, 4, 5, 15, 41 and 45 are amended to recite features supported in the specification at, for example, page 14, lines 27-28; 17, line 14 – page 18, line 3 and Fig. 5. No new matter is added by any of these amendments.

Applicant appreciates the courtesies extended to Applicant's representative by Examiners Woods and Jankus during the June 27, 2005 personal interview. In accordance with MPEP §713.04, the points discussed during the interview are incorporated in the remarks below and constitute Applicant's record of the interview.

Reconsideration based on the following remarks is respectfully requested.

I. Amendment Entry with Request for Continued Examination

Entry of this amendment is proper under 37 CFR §1.114 because this Submission is filed in conjunction with a Request for Continued Examination.

II. Claims 1-5, 8-10, 14-33 and 37-45 Define Patentable Subject Matter

The Final Office Action rejects claims 1, 2, 4 and 14 under 35 U.S.C. §103(a) over U.S. Patent Application Publication 2002/0067323 to Bird *et al.* ("Bird") in view of U.S. Patent 6,781,155 to Yamada; claims 3 and 5 under 35 U.S.C. §103(a) over Bird in view of Yamada and further in view of U.S. Reissue Patent Re 35,827 to Gualandris *et al.* ("Gualandris"); claims 8-10, 37, 39 and 40 under 35 U.S.C. §103(a) over Bird in view of Yamada and further in view of U.S. Patent Application Publication 2002/0008822 to Maeda *et al.* ("Maeda"); claims 15 and 41 under 35 U.S.C. §103(a) over Bird in view of Yamada and Maeda and further in view of U.S. Patent Application Publication 2004/0207615 to Yumoto; claim 38 under 35 U.S.C. §103(a) over Bird in view of Yamada and further in view of U.S.

Patent Application Publication 2001/0026835 to Tanaka; claims 42-44 under 35 U.S.C. §103(a) over Bird in view of Yamada and Yumoto and further in view of Maeda; and claim 45 under 35 U.S.C. §103(a) over Bird in view of Yamada and Yumoto and further in view of Gualandris. These rejections are respectfully traversed.

As implicitly agreed during the interview, the applied references fail to teach or suggest an active matrix substrate directed to an electroluminescence element, and further do not teach or suggest a third active element connected between the first active element and a data line, as recited in claims 1 and 15. Nor do the applied references teach or suggest a third transistor having a fifth terminal, a sixth terminal, and a third control terminal, the fifth terminal being connected to a data line, and the sixth terminal being connected to the third terminal of the first transistor, as recited in claims 4 and 5, or else a third transistor to control current to the holding element, as recited in claims 41 and 45.

For at least these reasons, Applicant respectfully asserts that the independent claims are patentable over the applied references. The dependent claims are likewise patentable over the applied references for at least the reasons discussed, as well as for the additional features they recite. Consequently, all the claims are in condition for allowance. Thus, Applicant respectfully requests that the rejections under 35 U.S.C. §103 be withdrawn.

III. Conclusion

In view of the foregoing amendments and remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Gerhard W. Thielman
Registration No. 43,186

JAO:GWT/gwt

Attachment:
Request for Continued Examination

Date: July 13, 2005

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

PATENT APPLICATION FEE DETERMINATION RECORD

R.C.E.

Application or Docket Number 10/299861

CLAIMS AS FILED - PART I

AMSB

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	39 minus 39 =	* 0
INDEPENDENT CLAIMS	16 minus 16 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		☐

7-13-05

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE		OR	BASIC FEE	790.
X$ =		OR	X$ =	
X =		OR	X =	
+ =		OR	+ =	
TOTAL		OR	TOTAL	790.

CLAIMS AS AMENDED - PART II

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ =		OR	X$ =	
X =		OR	X =	
+ =		OR	+ =	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ =		OR	X$ =	
X =		OR	X =	
+ =		OR	+ =	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ =		OR	X$ =	
X =		OR	X =	
+ =		OR	+ =	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

PTO/SB/06 (12-04)
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 10/299861

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))							
SEARCH FEE (37 CFR 1.16(k), (i), or (m))							
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X =		OR	X =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X =			X =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
			TOTAL			TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

2-13-05

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 39	Minus	** 39	= 0	X =		OR	X =	
Independent (37 CFR 1.16(h))	* 16	Minus	*** 16	= 0	X =		OR	X =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

3-25-05

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 37	Minus	** 39	= 0	X =		OR	X =	
Independent (37 CFR 1.16(h))	* 12	Minus	*** 16	= 0	X =		OR	X =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/06 (12-04)
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 10/299861

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))							
SEARCH FEE (37 CFR 1.16(k), (i), or (m))							
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X =		OR	X =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X =			X =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

7-13-05

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
AMENDMENT A	Total (37 CFR 1.16(i))	* 37	Minus	** 39	= 0	X =		OR	X =	
	Independent (37 CFR 1.16(h))	* 13	Minus	*** 16	= 0	X =		OR	X =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	15870	LDD	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:19
S2	45103	"electro-optical" electrooptical	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:19
S3	3757098	element	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:20
S4	2	"6781155".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:21
S5	2	"6777255".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:20
S6	171475	Sanyo.as.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:20
S7	2	"6277679".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:34
S8	10578	DDD	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:34
S9	254	GDD	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:34

S10	1	S1 and S8 and S9 and "active matrix"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:34
S11	4	S1 and S8 and S9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:16
S12	35797	"active matrix"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:34
S13	1855360	substrate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 12:34
S14	39920	"first transistor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:16
S15	43582	"second transistor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:16
S16	18297	"third transistor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:16
S17	289209	"pixel" "unit cell" "unit circuit"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:17
S18	694	S14 and S15 and S16 and S17	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:18
S19	4	S14 and S15 and S16 and S18 and "1217"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:27

S20	512	S18 and "pixel"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:27
S21	205	S20 and "active matrix"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 13:28
S22	27	S21 and S2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:17
S23	151	"21" and (gate same metal same (scan with line))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18
S24	39920	"first transistor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18
S25	43582	"second transistor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18
S26	18297	"third transistor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18
S27	289209	"pixel" "unit cell" "unit circuit"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18
S28	694	S24 and S25 and S26 and S27	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18
S29	512	S28 and "pixel"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18

S30	205	S29 and "active matrix"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:18
S31	1	S30 and (gate same metal same (scan with line))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:23
S32	6	S30 and ((gate same metal) and (scan with line))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:30
S33	152	(gate with metal) same ((scan with line) "scan line" "scan lines") same form$7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:31
S34	45103	"electro-optical" electrooptical	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:31
S35	35797	"active matrix"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:31
S36	10	S33 and S34 and S35	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/01 15:36
S37	986	capacitor same portion same (power with supply with line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/02 08:10
S38	160	capacitor same portion with (power near supply near line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/02 08:10
S39	86	capacitor with portion with (power near supply near line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/02 08:11

S40	9	capacitor with portion near (power near supply near line) not seiko. as. not epson.as.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/02 08:11
S41	9	capacitor with portion near (power near supply near line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/02 09:36
S42	182	laser near anneal$5 same recrystal$10 and polysilicon and TFT$	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/02 09:37
S43	7	S42 and layer and OLED	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/11/02 09:38
S44	1334	(345/76 345/77 345/78 345/79).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/12 17:26
S45	12373	(345/8? 345/9? 345/100 345/101 345/102 345/103 345/104 345/105).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/12 17:26
S46	1526	(345/76 345/77 345/78 345/79).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/21 13:12
S48	13083	(345/8? 345/9? 345/100 345/101 345/102 345/103 345/104 345/105).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/21 13:12
S49	2	"20020067323".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/21 16:10

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/299,861	11/20/2002	Yojiro Matsueda	114251	5800

25944 7590 10/13/2005

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
WOODS, ERIC V	
ART UNIT	**PAPER NUMBER**
2672	

DATE MAILED: 10/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/299,861	MATSUEDA, YOJIRO	
	Examiner	Art Unit	
	Eric V. Woods	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,8-10,14-33 and 37-45* is/are pending in the application.

4a) Of the above claim(s) *16-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-10,14,15 and 37-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 13 July 2005 has been entered.

Election/Restrictions

Applicant's request for rejoinder is inapposite because the restriction requirement was made **final** in the last Office Action, and no arguments other than a general request for rejoinder were put forward. Applicant has not provided any new evidence; therefore, if rejoinder is desired, a petition under 37 CFR 1.129(b) or otherwise is required. No further communication will be made on this topic. Claims 16-33 are withdrawn from consideration, and will be canceled if the case is passed to issue.

Status of Claims

Applicant has claims 1-5, 8-10, 14-33, and 37-45 pending. As noted above, claims 16-33 have been withdrawn on a final restriction requirement, and as such are no longer under consideration, nor can they be under further circumstances.

The relevant remaining claims under examination are 1-5, 8-10, 14-15, and 37-45.

Response to Arguments

Applicant's arguments, see Remarks pages 1-3, filed 13 July 2005, with respect to the rejections of all pending claims have been fully considered and are persuasive.

The rejections of claims 1-5, 8-10, 14-15, and 37-45 under 35 U.S.C. 103(a) have been withdrawn in view of applicant's amendment to the claims. As noted in the interviews of 26 June and 12 July, the changes made in the amendments are sufficient to overcome the rejections used in the previous Office Action.

However, after further consideration, examiner provides new ground(s) of rejection against claims 1-5, 8-10, 14-15, and 37-45 below.

Definitions

The term "electroluminescence element" will be taken to mean, as per the specification page 1 and previous interviews with applicant's representative, to include LEDs and organic light-emitting diodes (OLEDs) among other items. That is, the definition is taken to require active emission of light by application of an electrical signal or field.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yumoto (US 2004/0207615 A1). Claim 1 is slightly broader than claim 4; the additional limitations will be discussed at the end of the claim.

As to claim 4,

An active matrix substrate, comprising a plurality of unit circuits arranged corresponding to intersections of a plurality of data lines and a plurality of scan lines, wherein each of said plurality of unit circuits comprises: (Yumoto Figure 2 shows an array of unit circuits on a substrate with a plurality of data lines and scan lines)

-A first transistor, comprising a first control terminal, a first terminal, and a second terminal, said first terminal connected in series to an electro-optical element; (Yumoto Figure 9, TFT one has a first terminal (upper one) connected in series with an electro-optical element (OLED))

-A holding element, connected to said first control terminal, and comprising a first electrode connected to said first control terminal and a second electrode connected to said second terminal; (Yumoto Figure 9, the holding element is capacitor C with one electrode connected to the control terminal (gate) of transistor TFT1; the second electrode is connected to ground, while the second terminal is also connected ground, which therefore are electrically contiguous and are connected together)

-A second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal being connected to one of said first terminal and said second terminal, and said fourth terminal being connected to said first control terminal; and (Yumoto, Figure 9, TFT4 has two terminals, with the third terminal (the one on the left) being connected to the first terminal of TFT1; fourth terminal is connected to the first control terminal (gate) of TFT1)

-A third transistor, comprising a fifth terminal, a sixth terminal, and a third control terminal, said fifth terminal being connected to a data line of said plurality of data lines,

and said sixth terminal being connected to said third terminal; (Yumoto Figure 9, TFT3 has two terminals and a control terminal, with the fifth terminal (the left one) clearly attached to a line labeled '**data**', and the sixth terminal on the right is clearly attached to the third terminal (the left one) of TFT4)

-Wherein said second transistor has a multi-gate structure, and said electro-optical element is an electroluminescence element. (Yumoto shows in Figure 8 an implementation where TFT2 and TFT4 both consist of dual-gate devices, and the electro-optical element of Yumoto is an OLED, which as noted in the above definitions sections is clearly an EL element)

It would have been obvious to modify the implementation of Yumoto in Figure 9 to use the dual-gate transistors of Figure 8 (as in TFT 4a/4b and TFT 2a/2b) because such structures suppress and lower leakage current [0073], and such a second transistor is explicitly shown having a dual-gate structure in Figure 8.

As to claim 1,

This claim is a broader version of claim 4, the rejection to which is incorporated by reference. As stated above, Yumoto teaches in [0073] that the dual-gate structure on TFT2 in Figure 8 serves to suppress leakage "during the off time" (e.g. during shutoff), and all the other limitations are taught in the rejection to claim 4 above. Claims 1 and 4 will stand and fall together.

As to claim 2, as noted above, Yumoto in [0073] teaches the multi-gate structure.

As to claim 15,

An electro-optical device including a plurality of electro-optical elements (see Yumoto Figure 2, the rejection to claim 1, etc.), comprising peripheral circuits (see Yumoto Figs. 7 and 11) to supply current to an electro-optical element of each pixel corresponding to said electro-optical elements, wherein each of said peripheral circuits comprises:

-A light-emission control active element to supply said current to said electro-optical element during a light emission period (function served by recited first-active element; driving circuit can perform both tasks; see also TFT1 in Fig. 13, or in Fig. 12 the alternate structure, with TFT7, as a separate element);

-A holding element to hold a control voltage (Capacitor C in any of Figs. 11-15, Yumoto);

-A first active element, comprising a gate terminal and a terminal, a gate terminal of which is connected to said holding element, which supplies a current, based on said control voltage applied to the gate terminal, and said terminal being connected in series to said electro-optical element via said light-emission control active element (Yumoto, see also TFT1, in Figs. 11 and 12 in Yumoto or TFT5 in Fig. 11)(see also the rejection to claim 4, where the recited connections are shown to be present in the recited form, and it is prima facie obvious that the electro-optical element is in series with the transistor);

-A current-controlling active element, that passes data current via said first active element during a selection period (TFT4 in Yumoto Fig. 13, 9); and,

-A second active element, connected between a first terminal to said current-controlling active element and said terminal and a second terminal to said holding element, which,

during said selection period, charges said holding element and causes said control voltage to be stored (see the rejection to claim 4, where this is the second transistor, TFT3 and the connections between the elements are shown there in the format listed); -Wherein said active element contains a structure to prevent leakage current during shutoff (Yumoto teaches in [0073] that the dual-gate structure on TFT2 in Figure 8 serves to suppress leakage "during the off time" (e.g. during shutoff)).

Reference Yamada teaches the general two-transistor structure along with current-controlling elements and structures to prevent leakage current during shutoff. Reference Yamada does not explicitly teach the other recited details of the claim. Yumoto teaches several different embodiments of peripheral structure for each pixel or unit circuit that contain all the recited elements as identified previously.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the unit pixel cells of Yumoto Figures 9, 11-13, with the multi-gate structures of Figure 8 to prevent leakage, as noted in [0073] for transistors of Yumoto, since both are aimed at active matrix panel applications (Yumoto Fig. 2, etc.) and to prevent variation due to device parameters (Yumoto 0017). Furthermore, certain functionality that is split off in this claim, e.g. making the light-emission control active element separable from the driving TFT, and splitting off the current-controlling active elements, are obvious and not patentable under *Nerwin v. Erlichman*, 168 USPQ 177, 179 (PTO Bd. Of Int. 1969), since applicant is merely making separable items which are claimed as integral functions in earlier claims (For example, claims 1 and 4 used as evidence claims for this justification). Secondly, if the adjustable argument is made by

applicant (that adding elements making those features adjustable), under *In re Stevens*, 101 USPQ 284 (CCPA 1954) that doctrine will not hold, in "that the provision of adjustability, when needed, is not a patentable advance."

As to claim 41, the rejection to claim 4 is incorporated by reference. The only difference is that the third transistor's purpose is to control current to the holding element, where it is prima facie obvious that any transistor that has a current-controlling terminal (e.g. first or second terminal in the terminology of the claims, source or drain to those of ordinary skill in the art) that is connected to a capacitor will prima facie control the current to the holding element; in this case, the third transistor is connected to the holding element and thusly will effect the current to it in some manner; further, the entire purpose of the capacitor is to retain charge from the data line, which therefore means that it will intrinsically be used for that purpose.

Take Yumoto Figure 9 – the control terminal of TFT4 (the third transistor) is connected to scanA, which is clearly a scan line. The other connections are as in the rejection to Figure 4. The EO element is clearly an OLED, which clearly qualifies as an EL element according to applicant's specification.

Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as unpatentable over Yumoto as applied to claim 1 above, and further in view of Gualandris.

As to claim 3,

The active matrix substrate according to claim 1, wherein at least said second active element is a transistor comprising a structure selected from the group consisting of an LDD structure, GDD structure, and DDD structure.

Yumoto teaches in [0113] to have the LDD structure in the active transistor, and it is discussed as being the active layer *per se*, that is on top of the gate oxide, so it would work for any transistor as specified there. However, Yumoto does not explicitly teach the use of GDD and DDD structures where Gualandris teaches DDD in 1:55-65, GDD in 2:25-30, and LDD in 2:25-30. Gualandris teaches that these are all methods of doping transistors, although one (the LDD) is preferred to work for 'ULSI' applications. Given that 'ULSI' applications at the time the patent was issued were mainly for deep sub-micron processes and that current TFT / liquid crystal display processes have much larger dimensions, e.g. still larger than one micron minimum channel length for silicon-on-glass technology, these techniques would be perfectly valid for use in TFT / silicon-on-glass technology.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix substrates of Yumoto with the transistors of Gualandris, since Yamada uses transistors, which *prima facie* have a source and a drain and different drain doping techniques are well-known in the art, and Yumoto also teaches LDD mechanisms of doping, and the others would be obvious to a worker of ordinary skill in the art.

As to claim 5,

The rejection to claim 4 is incorporated by reference. This claim is substantially similar, with the only exception that the required 'multi-gate' structure for the second transistor has been replaced by one of a group of LDD, GDD, and DDD structures. The additional

limitation is taught above in the rejection of claim 3, which is incorporated by reference. Claims 3 and 5 stand and fall together.

Claims 8-10 and 37-44 are rejected under 35 U.S.C. 103(a) as unpatentable over Yumoto as applied to claim 4 above, and further in view of Maeda.

As to claim 8,

The active matrix substrate according to any of claims 4 through 7, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yumoto Figure 3 and [0010] for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yumoto [0011], semiconductor thin film 4); and

-A gate metal layer comprising said second control terminal (Yumoto [0011], gate electrode 2)(forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one scan line among said plurality of scan lines is formed in said gate metal layer (Maeda 0121).

References Yumoto teaches all the limitations of this claim except the formation of a scan line in the gate metal layer. Reference Maeda teaches the formation of scan lines and gate electrodes in the same metal film layer for TFT / LCD monitor fabrication (e.g. 0162, 0121). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single

metal layer of Maeda since Maeda performs in one step what Yumoto does in several steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode goes down first and then the scan lines go down after the semiconductor layer, which clearly is a different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination, e.g. common sense is sufficient to justify the combination. See also *In re Karlson*, 136 USPQ 184 (CCPA 1963), for the doctrine that eliminating components is an obvious expedient – in this, eliminating fabrication steps.

As to claim 9,

The active matrix substrate according to any of claims 4 through 7, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yumoto Figure 3 and [0010] for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yumoto [0011], semiconductor thin film 4); and

-A gate metal layer comprising said second control terminal (Yumoto [0012]) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in said gate metal layer (Maeda 0121 and 0113 and 0125).

Reference Yumoto teaches all the limitations of this claim except the formation of a data line in the gate metal layer. Reference Maeda teaches the formation of data lines and source and drain electrodes in the same metal film layer for TFT / LCD

monitor fabrication (e.g. 0113, 0125). It would be *prima facie* obvious to choose to form gate electrodes and data lines simultaneously rather than gate electrodes and scan lines, for example. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single metal layer of Maeda since Maeda performs in one step what Yumoto does in several steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode goes down first and then the scan lines go down after the semiconductor layer, which clearly is a different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

As to claim 10,

The active matrix substrate according to any of claims 4 through 7, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yumoto Figure 3 and [0010] for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yumoto [0011], semiconductor thin film 4); and

-A gate metal layer comprising said second control terminal (Yumoto [0012]) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-A source metal layer comprising a source electrode or drain electrode connected to the source or drain of said second transistor (Maeda 0113, 0125); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in the layer (Maeda 0121 and 0113 and 0125), among said source metal layer and said gate metal layer, which is closer to said semiconductor layer.

Reference Maeda in combination with Yumoto teaches all the limitations of this claim, and this is merely a recitation of the dual limitations of claims 8 and 9 above. As such, the combination and motivation from claim 8 is used here and no further comment is necessary, as this claim is only a nominal variation of the parent.

As to claim 37,

An active matrix substrate according to claim 4, comprising unit circuits comprising transistors, arranged corresponding to intersections of data lines and scan lines (Yumoto Figure 2, and the transistor picture layouts in Figures 5, 8, 9, etc) wherein

-A semiconductor layer constituting such transistors is formed in a semiconductor layer (Yumoto [0011], semiconductor thin film 4);

-Either said scan lines or said data lines are formed in a first conducting layer at the intersections of said scan lines and said data lines (Maeda 0113, 0121, and 0125); and,

-A portion of said scan lines and said data lines outside said intersections are formed in a second conducting layer (Maeda 0113, 0121, and 0125).

Reference Yumoto does not explicitly teach the formation of scan or data lines formed in a conducting layer at the intersections of such lines. Reference Maeda describes forming gate metal and scan lines, etc. simultaneously. As such, the scan lines would be formed everywhere not masked with a shadow mask, e.g. both in the scan lines and in the intersections. No matter what portions of the lines are claimed,

any such configuration could be made using shadow masking and formed using either evaporation or sputtering. Any set of contacts could be created using correctly etched contact holes; electrically contiguous metal formed in the same layer is *prima facie* the same from an electrical and an engineering perspective. Further, forming scan lines or data lines or portions thereof (as claimed) in the same layer as other things would simply be making a component integral by eliminating unnecessary metal, and under *In re Larson*, 144 USPQ 347 (CCPA 1965), making a component integral is obvious and not patentable. Therefore, under either methodology, the recited limitations of the claim have been met.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single metal layer of Maeda since Maeda performs in one step what Yumoto does in several steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode goes down first and then the scan lines go down after the semiconductor layer, which clearly is a different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

As to claim 39,

An electro-optical device according to claim 4, comprising electro-optical elements corresponding to intersections of scan lines and data lines (Yumoto, element OLED in various figures, such as 5, 8, 9, etc), wherein:

-A pair of electrodes is provided to supply power to electro-optical elements (Maeda Fig. 11C, elements 19 and 15 are opposing and pixel electrodes (see 0006-0008));

-At the intersections of said scan lines and said data lines, either said scan lines or said data lines are formed in a first conducting layer (Maeda 0113, 0118, 0121, 0125 – again, gate metal as discussed in rejections to claims 8-12);

-Portions of said scan lines and said data lines outside said intersections are formed in a second conducting layer (source metal layer, 0113, 0118, 0121, 0125 as discussed in rejections to claims 8-12); and,

-Said second conducting layer is positioned at a greater distance than said first conducting layer from one of said pair of electrodes (design choice issue, see Maeda Fig. 11C).

Reference Yumoto does not recite details of the fabrication process claimed above. Reference Maeda teaches the fabrication of such substrates and teaches contact holes (0044, 0047). Logically, such contact holes would fill on conducting layer deposition, thus meeting the recited limitation concerning intersections of data and scan lines. The positioning of a layer or its size is *prima facie* obvious and is not patentable (*In re Japikse* for order of parts and further under *In re Reese*, anyone of ordinary skill in the art would know that there would be an optimal spacing of electrodes from each other to minimize cross-talk that would also occupy the minimum aspect ratio required on the shadow mask).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single metal layer of Maeda since Maeda performs in one step what Yumoto does in several steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode goes down

first and then the scan lines go down after the semiconductor layer, which clearly is a different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

As to claim 40, reference Yumoto clearly teaches in [0098] that the first transistor (TFT1) is an n-channel type and that the second transistor (TFT3, but as noted in [0100-0101, particularly [0101], TFT4 has the same conductivity type as TFT3) has a p-channel, which are prima facie opposite polarities. Motivation and combination are taken from claim 39.

Claim 38 is rejected over Yumoto and Maeda as applied to claim 37 above, and further in view of Tanaka.

As to claim 38,

The active matrix substrate according to claim 37, wherein said second conducting layer is positioned between said first conducting layer and said semiconductor layer.

Reference Yumoto does not explicitly teach this limitation. In Fig. 10B, Maeda shows that the bottom gate – element 56, which is metal (a niobium alloy) is put down first, then various insulating materials, then element 13 (source and drain electrodes) are formed on the same level and slightly covering the semiconductor layer 54. Under the doctrine of *In re Japikse*, switching the two layers would be *prima facie* obvious, and only minor alternations in the shadow masks for the process would be necessary (additive vs. subtractive processing in semiconductors, for example, switching the process would not be difficult for one of ordinary skill in the semiconductor / TFT art).

Again, given that Maeda teaches many different embodiments (see Figs. 10-13, etc.), such a switch would be a design choice issue, and it would allow low-temperature processing of the substrate throughout the process, particularly allowing for newer techniques such as laser annealing and recrystallization of the semiconductor layer taught by Tanaka, and treatment of the semiconductor layer towards the end of processing.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the TFT circuits of Yumoto and Maeda with the laser annealing processing of polysilicon for TFT applications of Tanaka (see 0002-0015), as both Yumoto ([0011-0013]) and Maeda (0008, 0121, etc.) utilize polysilicon as the semiconductor material, and laser annealing is now a well-known, standard process in the art.

Claims 42-44 are rejected under 35 U.S.C. 103(a) as unpatentable over Yumoto as applied to claim 41 above, and further in view of Maeda (claim 4 operative here – any of the other claims would be subject to the same rejection).

As to claim 42,

The active matrix substrate according to claim 41, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yumoto Figure 3 and [0010] for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yumoto [0011], semiconductor thin film 4); and

-A gate metal layer comprising said second control terminal (Yumoto [0012]) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one scan line among said plurality of scan lines is formed in said gate metal layer (Maeda 0121).

References Yumoto teach all the limitations of this claim except the formation of a scan line in the gate metal layer. Reference Maeda teaches the formation of scan lines and gate electrodes in the same metal film layer for TFT / LCD monitor fabrication (e.g. 0162, 0121). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single metal layer of Maeda since Maeda performs in one step what Yumoto does in several steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode goes down first and then the scan lines go down after the semiconductor layer, which clearly is a different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination, e.g. common sense is sufficient to justify the combination. See also *In re Karlson*, 136 USPQ 184 (CCPA 1963), for the doctrine that eliminating components is an obvious expedient – in this, eliminating fabrication steps.

As to claim 43,

The active matrix substrate according to claim 41, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yumoto Figure 3 and [0010] for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yumoto [0011], semiconductor thin film 4); and

-A gate metal layer comprising said second control terminal (Yumoto [0012]) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in said gate metal layer (Maeda 0121 and 0113 and 0125).

Reference Yumoto teaches all the limitations of this claim except the formation of a data line in the gate metal layer. Reference Maeda teaches the formation of data lines and source and drain electrodes in the same metal film layer for TFT / LCD monitor fabrication (e.g. 0113, 0125). It would be *prima facie* obvious to choose to form gate electrodes and data lines simultaneously rather than gate electrodes and scan lines, for example. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single metal layer of Maeda since Maeda performs in one step what Yumoto does in several steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode goes down first and then the scan lines go down after the semiconductor layer, which clearly is a different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

As to claim 44,

The active matrix substrate according to claim 41, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yumoto Figure 3 and [0010] for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yumoto [0011], semiconductor thin film 4); and

-A gate metal layer comprising said second control terminal (Yumoto [0012]) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-A source metal layer comprising a source electrode or drain electrode connected to the source or drain of said second transistor (Maeda 0113, 0125); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in the layer (Maeda 0121 and 0113 and 0125), among said source metal layer and said gate metal layer, which is closer to said semiconductor layer.

Reference Maeda in combination with Yumoto teaches all the limitations of this claim, and this is merely a recitation of the dual limitations of claims 42 and 43 above. As such, the combination and motivation from claim 42 is used here and no further comment is necessary, as this claim is only a nominal variation of the parent.

Claim 45 is rejected under 35 U.S.C. 103(a) as unpatentable over Yumoto as applied to claim 41 above, and further in view of Gualandris. The rejection to claim 41 is herein incorporated by reference in its entirety.

Claim 45 is a substantial duplicate of claim 41, with the only difference being the addition of the limitation from claim 3:

Wherein at least said second active element is a transistor comprising a structure selected from the group consisting of an LDD structure, GDD structure, and DDD structure.

Yumoto teaches in [0113] to have the LDD structure in the active transistor, and it is discussed as being the active layer *per se*, that is on top of the gate oxide, so it would work for any transistor as specified there. However, Yumoto does not explicitly teach the use of GDD and DDD structures where Gualandris teaches DDD in 1:55-65, GDD in 2:25-30, and LDD in 2:25-30. Gualandris teaches that these are all methods of doping transistors, although one (the LDD) is preferred to work for 'ULSI' applications. Given that 'ULSI' applications at the time the patent was issued were mainly for deep sub-micron processes and that current TFT / liquid crystal display processes have much larger dimensions, e.g. still larger than one micron minimum channel length for silicon-on-glass technology, these techniques would be perfectly valid for use in TFT / silicon-on-glass technology.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix substrates of Yumoto with the transistors of Gualandris, since Yamada uses transistors, which *prima facie* have a source and a drain and different drain doping techniques are well-known in the art, and Yumoto also teaches LDD mechanisms of doping, and the others would be obvious to a worker of ordinary skill in the art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric V. Woods whose telephone number is 571-272-7775. The examiner can normally be reached on M-F 7:30-4:30 alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on 571-272-7664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eric Woods

PRIMARY EXAMINER

September 22, 2005

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/299,861	MATSUEDA, YOJIRO
Examiner	**Art Unit**
Eric V. Woods	2672

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	9/21/05
	1	√
	2	√
	3	√
	4	√
	5	√
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	9	√
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Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
10/299,861	MATSUEDA, YOJIRO	
Examiner	**Art Unit**	
Eric V. Woods	2672	

SEARCHED			
Class	Subclass	Date	Examiner
345	76-79, 80-105	9/21/2005	EW

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST (USPT,USPGPUB,USOCR, DERWENT,EPO,JPO,IBM_TDB) -- see attached search history	9/21/2005	EW



IFW

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2672

Application No.: 10/299,861

Examiner: E. WOODS

Filed: November 20, 2002

Docket No.: 114251

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE

AMENDMENT UNDER 37 C.F.R. §1.111

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the October 13, 2005 Office Action, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An active matrix substrate including a plurality of electro-optical elements, comprising peripheral circuits to supply current to an electro-optical element of each pixel corresponding to said electro-optical elements, wherein each of said peripheral circuits comprises:

a holding element to hold a control voltage;

a first active element, comprising a first control terminal and a terminal, said control terminal being connected to said holding element, and said terminal being connected in series to said electro-optical element, to supply a current based on said control voltage to said electro-optical element;

a scan line;

a second active element, connected between said first control terminal and said terminal of said first active ~~element;~~ element, and including a second control terminal connected to the scan line; and

a third active element, connected between said terminal of said first active element and a data line, and including a third control terminal connected to the scan line,

wherein said second active element comprises a structure to prevent leakage currents during shutoff, and said electro-optical element is an electroluminescence element.

2. (Previously Presented) The active matrix substrate according to claim 1, wherein said second active element is configured as a multi-gate active element.

3. (Previously Presented) The active matrix substrate according to claim 1, wherein at least said second active element is a transistor comprising a structure selected from the group consisting of an LDD structure, a GDD structure, and a DDD structure.

4. (Currently Amended) An active matrix substrate, comprising a plurality of unit circuits arranged corresponding to intersections of a plurality of data lines and a plurality of scan lines, wherein each of said plurality of unit circuits comprises:

a first transistor, comprising a first control terminal, a first terminal, and a second terminal, said first terminal connected in series to an electro-optical element;

a holding element, connected to said first control terminal, and comprising a first electrode connected to said first control terminal and a second electrode connected to said second terminal;

a second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal being connected to one of said first terminal and said second terminal, ~~and~~ said fourth terminal being connected to said first control ~~terminal;~~ terminal and said second control terminal being connected to one of said scan lines; and

a third transistor, comprising a fifth terminal, a sixth terminal, and a third control terminal, said fifth terminal being connected to a data line of said plurality of data lines, ~~and~~ said sixth terminal being connected to said third ~~terminal;~~ terminal and said third control terminal being connected to said one of said scan lines;

wherein said second transistor has a multi-gate structure, and said electro-optical element is an electroluminescence element.

5. (Currently Amended) An active matrix substrate, comprising a plurality of unit circuits arranged corresponding to intersections of a plurality of data lines and a plurality of scan lines, wherein each of said plurality of unit circuits comprises:

a first transistor, comprising a first control terminal, a first terminal, and a second terminal, said first terminal connected in series to an electro-optical element;

a holding element, connected to said first control terminal, and comprising a first electrode connected to said first control terminal and a second electrode connected to said second terminal;

a second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal being connected to one of said first terminal and said second terminal, ~~and~~ said fourth terminal being connected to said first control ~~terminal;~~ terminal and said second control terminal being connected to one of said scan lines; and

a third transistor, comprising a fifth terminal, a sixth terminal, and a third control terminal, said fifth terminal being connected to a data line of said plurality of data lines, ~~and~~ said sixth terminal being connected to said third ~~terminal;~~ terminal and said third control terminal being connected to said one of said scan lines;

wherein said second transistor is a transistor comprising a structure selected from the group consisting of an LDD structure, a GDD structure, and a DDD structure, and said electro-optical element is an electroluminescence element.

6-7. (Canceled)

8. (Previously Presented) The active matrix substrate according to claim 4, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed; and

a gate metal layer comprising said second control terminal, and

wherein at least a portion of said plurality of scan lines is formed in said gate metal layer.

9. (Previously Presented) The active matrix substrate according to claim 4, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed; and

a gate metal layer comprising said second control terminal; and

wherein at least a portion of one data line among said plurality of data lines is formed in said gate metal layer.

10. (Previously Presented) The active matrix substrate according to claim 4, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed;

a gate metal layer comprising said second control terminal; and

a source metal layer comprising a source electrode or drain electrode connected to the source or drain of said second transistor;

wherein at least one portion of at least one data line among said plurality of data lines is formed in the layer, among said source metal layer and said gate metal layer, that is closer to said semiconductor layer.

11-13. (Canceled)

14. (Previously Presented) An electro-optical device comprising an active matrix substrate according to claim 1, and said electro-optical elements.

15. (Currently Amended) An electro-optical device including a plurality of electro-optical elements, comprising peripheral circuits to supply current to an electro-optical element of each pixel corresponding to said electro-optical elements,

wherein each of said peripheral circuits comprises:

a light-emission control active element to supply said current to said electro-optical element during a light emission period;

a holding element to hold a control voltage;

a scan line;

a first active element comprising a gate terminal and a terminal, said gate terminal being connected to said holding element that supplies a ~~current,~~ current and said scan line, based on said control voltage applied to the gate terminal, and said terminal being connected in series to said electro-optical element via said light-emission control active element;

a current-controlling active element, that passes data current via said first active element during a selection period, said current-controlling element being connected between said terminal of said first active element and a data line; and

a second active element, connected between a first terminal to said current-controlling active element and said terminal and a second terminal to said holding element and said control terminal, that, during said selection period, charges said holding element and causes said control voltage to be stored, said second active element including a gate terminal connected to said scan line,

wherein said second active element comprises a structure to prevent leakage currents during shutoff, and said electro-optical element is an electroluminescence element.

16. (Withdrawn) An electro-optical device, comprising electro-optical elements and peripheral circuitry that drives said electro-optical elements,

wherein said electro-optical elements are formed such that a boundary of the electro-optical elements has, at least, a prescribed curvature; and

at least one portion of said peripheral circuitry is formed in the region surrounded by the boundary having the specified curvature and by the boundaries of a polygon circumscribing the electro-optical element.

17. (Withdrawn) The electro-optical device according to claim 16, wherein a plurality of boundary portions having said prescribed curvature are formed.

18. (Withdrawn) The electro-optical device according to claim 16, wherein said plurality of formed boundary portions are arranged substantially symmetrically with respect to a center line passing through the geometric center of said electro-optical element.

19. (Withdrawn) An electro-optical device, comprising a light-emitting portion and a peripheral circuit that controls the current supplied to said light-emitting portion, by means of a pixel electrode, wherein:

the area of said light-emitting portion is smaller than the area of said pixel electrode; and,

the shape of said light-emitting portion and the shape of said pixel electrode are different.

20. (Withdrawn) An electro-optical device, comprising a light-emitting portion and a peripheral circuit that controls the current supplied to said light-emitting portion, by means of a pixel electrode, wherein:

the area of said light-emitting portion is smaller than the area of said pixel electrode; and

the shape of said light-emitting portion is a shape having a curvature, and the shape of said pixel electrode is a polygonal shape.

21. (Withdrawn) An electro-optical device, comprising a light-emitting portion and a peripheral circuit that controls the current supplied to said light-emitting portion, by means of a pixel electrode, wherein:

the area of said light-emitting portion is smaller than the area of said pixel electrode;

said light-emitting portion has a polygonal shape having n vertices (where n is an integer greater than or equal to 4);

said pixel electrode has a polygonal shape having m vertices (where m is an integer greater than or equal to 3); and

the relation n>m obtains.

22. (Withdrawn) The electro-optical device according to claim 19, wherein the entire region of said light-emitting portion is formed on said pixel electrode, and a contact region for connection of said peripheral circuit and said pixel electrode is provided in a portion of said pixel electrode in which said light-emitting portion is not formed.

23. (Withdrawn) An electro-optical device, comprising:

an electro-optical element;

a holding capacitance, constituted by a plurality of layers including electrodes, that regulates a current supplied to said electro-optical element; and

an active element that supplies current to said electro-optical element according to the electric charge amount held in said holding capacitance;

wherein a first electrode constituting said holding capacitance is formed by patterning a portion of a metal layer comprising a power supply line that supplies current to said electro-optical element.

24. (Withdrawn) The electro-optical device according to claim 23, wherein a second electrode constituting said holding capacitance is formed by patterning a portion of a metal layer comprising a control terminal of said active element.

25. (Withdrawn) The electro-optical device according to claim 23, wherein said first electrode is a portion of said power supply line, and a portion of a metal layer forming a control terminal of said active element is superposed on a portion of said power supply line and patterned to form said second electrode.

26. (Withdrawn) The electro-optical device according to claim 23, comprising a semiconductor layer below said first electrode and said second electrode.

27. (Withdrawn) The electro-optical device according to claim 25, wherein the region occupied by a layer positioned on the lower side among the layers constituting electrodes of said holding capacitance is formed to be larger than the region occupied by a layer positioned on the upper side.

28. (Withdrawn) The electro-optical device according to claim 27, wherein the region occupied by said layer positioned on the lower side is pattern-formed in a shape such that, even if the maximum possible position shift occurs at the time of formation of said layer positioned on the upper side, the region of the layer positioned on the upper side is contained within the region of said layer positioned on the lower side.

29. (Withdrawn) An electro-optical device, comprising a plurality of layers including electrodes, configured such that a current can be supplied by an active element according to a voltage stored in a holding capacitance to an electro-optical element that emits light through the application of an electric field between the electrodes, comprising:

a first metal layer, constituting a power supply line; and

a second metal layer, formed in a pattern including a portion of a control terminal of said active element; and

wherein one electrode constituting said holding capacitance is formed by patterning one portion of said first metal layer.

30. (Withdrawn) The electro-optical device according to claim 29, wherein the other electrode constituting said holding capacitance is formed by patterning one portion of said second metal layer.

31. (Withdrawn) The electro-optical device according to claim 29, wherein one electrode constituting said holding capacitance is one portion of said power supply line, and said other electrode is formed by superposing a portion of said second metal layer on a portion of the power supply line and patterning.

32. (Withdrawn) The electro-optical device according to claim 29, wherein the region occupied by a layer positioned on the lower side among the layers comprising said holding capacitance electrodes is formed to be larger than the region occupied by a layer positioned on the upper side.

33. (Withdrawn) The electro-optical device according to claim 32, wherein the region occupied by said layer positioned on the lower side is pattern-formed in a shape such that, even if the maximum possible position shift occurs at the time of formation of said layer positioned on the upper side, the region of the layer positioned on the upper side is contained within the region of said layer positioned on the lower side.

34-36. (Canceled)

37. (Previously Presented) The active matrix substrate in accordance with claim 4, comprising unit circuits comprising transistors, arranged corresponding to intersections of data lines and scan lines; wherein

a semiconductor film constituting said transistors is formed in a semiconductor layer;

either said scan lines or said data lines are formed in a first conducting layer at the intersections of said scan lines and said data lines; and

a portion of said scan lines and said data lines outside said intersections are formed in a second conducting layer.

38. (Original) The active matrix substrate according to claim 37, wherein said second conducting layer is positioned between said first conducting layer and said semiconductor layer.

39. (Previously Presented) The electro-optical device according to claim 4, comprising electro-optical elements corresponding to intersections of scan lines and data lines, wherein:

a pair of electrodes is provided to supply power to said electro-optical elements;

at the intersections of said scan lines and said data lines, either said scan lines or said data lines are formed in a first conducting layer;

portions of said scan lines and said data lines outside said intersections are formed in a second conducting layer; and

said second conducting layer is positioned at a greater distance than said first conducting layer from one of said pair of electrodes.

40. (Previously Presented) The active matrix substrate in accordance with claim 1, wherein said first and second active elements have opposite polarities.

41. (Currently Amended) An active matrix substrate, comprising a plurality of unit circuits arranged corresponding to intersections of a plurality of data lines and a plurality of scan lines, wherein each of said plurality of unit circuits comprises:

a first transistor, comprising a first control terminal, a first terminal, and a second terminal, said first terminal connected in series to an electro-optical element;

a holding element, connected to said first control terminal, and comprising a first electrode connected to said first control terminal and a second electrode connected to said second terminal;

a second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal being connected to one of said first terminal and said second terminal, and said fourth terminal being connected to said first control ~~terminal;~~ terminal and said second control terminal being connected to one of said scan lines; and

a third transistor to control current to the holding element, the third transistor comprising a fifth terminal, a sixth terminal, and a third control terminal, wherein

said second transistor has a multi-gate structure,

said third control terminal is connected to said one scan line among said plurality of scan lines,

said fifth terminal is connected to one data line among said plurality of data lines,

said sixth terminal is connected to said third terminal and to said first terminal, and

said electro-optical element is an electroluminescence element.

42. (Previously Presented) The active matrix substrate according to claim 41, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed; and

a gate metal layer comprising said second control terminal, and

wherein at least a portion of said plurality of scan lines is formed in said gate metal layer.

43. (Previously Presented) The active matrix substrate according to claim 41, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed; and

a gate metal layer comprising said second control terminal; and

wherein at least a portion of one data line among said plurality of data lines is formed in said gate metal layer.

44. (Previously Presented) The active matrix substrate according to claim 41, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed;

a gate metal layer comprising said second control terminal; and

a source metal layer comprising a source electrode or drain electrode connected to the source or drain of said second transistor; and

wherein at least one portion of at least one data line among said plurality of data lines is formed in the layer, among said source metal layer and said gate metal layer, that is closer to said semiconductor layer.

45. (Currently Amended) An active matrix substrate, comprising a plurality of unit circuits arranged corresponding to intersections of a plurality of data lines and a plurality of scan lines, wherein each of said plurality of unit circuits comprises:

a first transistor, comprising a first control terminal, a first terminal, and a second terminal, said first terminal connected in series to an electro-optical element;

a holding element, connected to said first control terminal, and comprising a first electrode connected to said first control terminal and a second electrode connected to said second terminal;

a second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal being connected to one of said first terminal and said second terminal, and said fourth terminal being connected to said first control ~~terminal;~~ terminal and said second control terminal being connected to one of said scan lines; and

a third transistor to control current to the holding element, the third transistor comprising a fifth terminal, a sixth terminal, and a third control terminal,

wherein said second transistor is a transistor comprising a structure selected from the group consisting of an LDD structure, a GDD structure, and a DDD structure;

said second transistor has a multi-gate structure,

said third control terminal is connected to said one scan line among said plurality of scan lines,

said fifth terminal is connected to one data line among said plurality of data lines,

said sixth terminal is connected to said third terminal and to said first terminal, and

said electro-optical element is an electroluminescence element.

REMARKS

Claims 1-5, 8-10, 14-33 and 37-45 are pending in this application. Claims 16-33 are withdrawn from consideration as being directed to non-elected subject matter. By this Amendment, claims 1, 4, 5, 15, 41 and 45 are amended.

On pages 4-9, the Office Action rejects claims 1 and 4 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Publication No. 2004/0207615 to Yumoto. On pages 9-11, the Office Action rejects claims 3 and 5 under 35 U.S.C. §103(a) as being unpatentable over Yumoto in view of Gualandris. On pages 11-17, the Office Action rejects claims 8-10 and 37-44 under 35 U.S.C. §103(a) as being unpatentable over Yumoto in view of Maeda. On pages 17-18, the Office Action rejects claim 38, presumably as being unpatentable under 35 U.S.C. §103(a), over Yumoto and Maeda further in view of Tanaka.[1] On pages 18-21, the Office Action rejects claims 42-44 under 35 U.S.C. §103(a) as being unpatentable over Yumoto in view of Maeda. On pages 21-22, the Office Action rejects claim 45 under 35 U.S.C. §103(a) as being unpatentable over Yumoto in view of Gualandris. These rejections are respectfully traversed.

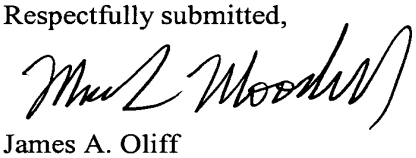
Independent claims 1, 4, 5, 15, 41 and 45 are amended to specify that at least two of the active elements recited in each claim include control terminals connected to a single scan line. It is respectfully submitted that none of the prior art of record discloses, teaches or suggests at least two active elements including control terminals connected to a single scan line, in combination with the other subject matter respectively recited in independent claims 1, 4, 5, 15, 41 and 45. Claims 2, 3, 8-10, 14, 37-40 and 42-44 are allowable based at least on their dependence from independent claims 1, 4 and 41 for the reasons stated above in connection with independent claims 1, 4 and 41.

[1] If the rejection of claim 38 on pages 17-18 is not a rejection as being unpatentable under 35 U.S.C. §103(a), Applicant requests clarification of the nature of this rejection.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-5, 8-10, 14-33 and 37-45 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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JAO:MRW/jth

Date: January 13, 2006

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PATENT APPLICATION FEE DETERMINATION RECORD

R.C.E.

plication or Docket Number

10/299861

CLAIMS AS FILED - PART I

AMSB

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	39 minus 39 =	0
INDEPENDENT CLAIMS	16 minus 16 =	
MULTIPLE DEPENDENT CLAIM PRESENT		☐

7-13-05

SMALL ENTITY TYPE ☐	RATE	FEE	OR	OTHER THAN SMALL ENTITY	RATE	FEE
	BASIC FEE		OR		BASIC FEE	790.
	X$ =		OR		X$ =	
	X =		OR		X =	1
	+ =		OR		+ =	
	TOTAL		OR		TOTAL	790.

CLAIMS AS AMENDED - PART II

1-13-06

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
AMENDMENT Total	* 37	Minus	** 17	=
AMENDMENT Independent	* 12	Minus	*** 9	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY	RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY	RATE	ADDITIONAL FEE
	X$ =		OR		X$ =	
	X =		OR		X =	
	+ =		OR		+ =	-
	TOTAL ADDIT. FEE		OR		TOTAL ADDIT. FEE	

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

	RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
	X$ =		OR	X$ =	
	X =		OR	X =	
	+ =		OR	+ =	
	TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

	RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
	X$ =		OR	X$ =	
	X =		OR	X =	
	+ =		OR	+ =	
	TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S50	9	(US-20040207615-$ or US-20020067323-$ or US-20030058212-$ or US-20020008822-$ or US-20010026835-$ or US-20010040565-$).did. or (US-RE35827-$ or US-6777255-$ or US-6781155-$).did.	US-PGPUB; USPAT	OR	ON	2006/03/22 17:17
S51	2	(precharg$4 pre-charg$4 (pre adj charg$4)) and S50	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/22 17:18
S52	1795	(345/76 345/77 345/78 345/79).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/04 20:13
S54	13905	(345/8? 345/9? 345/100 345/101 345/102 345/103 345/104 345/105).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/04 20:13
S56	1795	(345/76 345/77 345/78 345/79).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/04 20:13
S59	44942	"first transistor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/04 20:42
S60	48748	"second transistor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/04 20:42
S61	20458	"third transistor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/04 20:42

EAST Search History

S62	365775	"pixel" "unit cell" "unit circuit"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/04 20:42
S63	1082	S59 and S60 and S61 and S62	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/04 20:42
S64	1082	S63	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/04 20:42
S65	54	(plural$4 pluralit$4 many several multipl$4 multiplic$4 three two) near2 transistor with (connect$4 attach$5 link$4 join$3) with (scanline scan-line scan?line (scan adj line))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/04 22:03
S66	33	S65 same (pixel pel "unit circuit" "unit pixel")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/04 21:58
S67	21	S65 not S66	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/04 21:58
S68	16	(plural$4 pluralit$4 many several multipl$4 multiplic$4 three two) near2 transistor same transistor near2 (connect$4 attach$5 link$4 join$3) with (scanline scan-line scan?line (scan adj line)) not S65	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/04 22:02
S69	27	(plural$4 pluralit$4 many several multipl$4 multiplic$4 three two) near2 (transistor TFT (EL adj (element))) same (transistor TFT (EL adj (element))) near2 (connect$4 attach$5 link$4 join$3) with (scanline scan-line scan?line (scan adj line)) not (S65 S68)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/04 22:04

EAST Search History

S70	16	(plural$4 pluralit$4 many several multipl$4 multiplic$4 three two some few couple) near2 (transistor TFT (EL adj (element))) with (connect$4 attach$5 link$4 join$3) with (scanline scan-line scan?line (scan adj line)) not (S65 S68 S69)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/04 22:04

OIPE IAP13 APR 07 2006 PATENT & TRADEMARK OFFICE

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2672

Application No.: 10/299,861

Examiner: E. WOODS

Filed: November 20, 2002

Docket No.: 114251

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, Notice of Allowance or other action that closes prosecution (e.g., Quayle Action).

☒ a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

☒ 2. In accordance with 37 CFR §1.98(a)(2)(ii), copies of any U.S. patents and patent application publications are not attached.

☒ 3. Reference 1 corresponds to Reference 2 cited in the foreign Office Action.

Respectfully submitted,

Dinnatia Doster-Greene

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JAO:DJG/sqb

Date: April 7, 2006

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Form PTO-1449 (REV. 1/06)	US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 114251	APPLICATION NO. 10/299,861
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT Yojiro MATSUEDA	
		FILING DATE November 20, 2002	GROUP 2672

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Name
	1	6,794,675	09/21/2004	Koji SUZUKI et al.

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
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요약

TFT의 능동층의 소스와 유기 EL 소자의 양극과의 콘택트를 확실하게 하여 안정된 표시를 얻을 수 있는 유기 EL 표시 장치를 제공한다.

유리 기판으로 미루어지는 절연성 기판(10) 상에, TFT(40) 및 유기 EL 소자(60)를 형성한 유기 EL 표시 장치에 있어서, TFT(40)의 능동층(43)의 소스(43s)와 유기 EL 소자(60) 콘택트가, 소스(43s)의 n-Si, Mo, Al, Mo, 및 양극(61)의 ITO의 적층체로 이루어져 있으므로, 소스(43s)와 양극(61)과의 콘택트를 확실하게 행할 수 있어, 발기가 변동되거나 TFT(40) 및 유기 EL 소자(60)의 열화가 빨라지는 것을 방지할 수 있다.

대표도

도1

색인어

TFT 능동층, 유기 EL 소자, 절연성 기판, 발광 소자층, 스위칭 소자

명세서

도면의 간단한 설명

도 1은 본 발명의 EL 표시 장치의 평면도.
도 2는 본 발명의 EL 표시 장치의 단면도.
도 3은 종래의 EL 표시 장치의 평면도.
도 4는 종래의 EL 표시 장치의 단면도.
<도면의 주요 부분에 대한 부호의 설명>
10 : 절연성 기판
14 : 소도피 절연막
15 : 층간 절연막
15a, 15b : 콘택트 홀

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12 : 평탄화 절연막
17a : 콘택트 홀
41 : 게이트 전극
43 : 능동층
43s : 소스
43d : 드레인
43c : 채널
61 : 양극
62 : 발광 수전층
63 : 음극
64 : 절연막

발명의 상세한 설명

발명의 목적

발명이 속하는 기술분야 및 그 분야의 종래기술

본 발명은 박막 트랜지스터(Thin Film Transistor : 이하, TFT 라고 칭함) 및 유기 EL(Electro Luminescence) 소자를 구비하고 있고, 그 TFT를 스위칭 소자로서 이용한 유기 EL 표시 장치에 관한 것이다.

도 3에 종래의 EL 표시 장치의 표시 화소부의 평면도를 도시하고, 도 4a에 도 3의 A-A' 선에 따른 EL 표시 장치의 단면도를 도시하고, 도 4b에 도 3의 B-B선에 따른 단면도를 도시한다.

도 3에 도시된 바와 같이, 게이트 신호선(51)과 드레인 신호선(52)으로 둘러싸인 영역에 표시 화소가 형성되어 있다. 상 신호선의 교점 부근에는 제1 TFT(30)가 구비되어 있고, 그 TFT(30)의 소스(43s)는 유지 용량 전극선(54) 사이에서 용량을 이루는 용량 전극(55)를 겸함과 함께 제2 TFT(40)의 게이트(41)에 접속되어 있다. 제2 TFT의 소스(43s)는 유기 EL 소자(60)의 양극(61)에 접속되고, 다른 드레인(43d)는 유기 EL 소자를 구동하는 구동 전원선(53)에 접속되어 있다.

또한, TFT의 부근에는 게이트 신호선(51)과 평행하게 유지 용량 전극선(54)이 배치되어 있다. 이 유지 용량 전극선(54)은 크롬 등으로 이루어져 있고, 게이트 절연막(42)를 통해 TFT의 소스(43s)와 일체 형성된 용량 전극(55) 사이에서 전하를 축적하여 용량을 이루고 있다. 이 유지 용량은, 제2 TFT(40)의 게이트 전극(41)에 인가되는 전압을 유지하기 위해 설치되어 있다.

이와 같이 유기 EL 소자(60), 및 TFT(30), TFT(40)를 구비한 표시 화소가 기판(10) 상에 매트릭스형으로 배치됨에 따라 유기 EL 표시 장치가 형성된다.

도 4에 도시된 바와 같이, 유기 EL 표시 장치는, 유리나 합성 수지 등으로 이루어지는 기판 또는 도전성을 갖는 기판 또는 반도체 기판 등의 기판(10) 상에, TFT 및 유기 EL 소자를 순서대로 적층 형성하여 이루어진다. 단, 기판(10)으로서 도전성을 갖는 기판 및 반도체 기판을 이용하는 경우에는, 이들 기판(10) 상에 SiO2나 SiN 등의 절연막을 형성한 위에 TFT(30), TFT(40) 및 유기 EL 표시 소자(60)를 형성한다.

우선, 스위칭용의 TFT인 제1 TFT(30)에 대해 설명한다.

도 4a에 도시된 바와 같이, 석영 유리, 무알칼리 유리 등으로 이루어지는 절연성 기판(10) 상에, 크롬(Cr), 몰리브덴(Mo) 등의 고융점 금속으로 이루어지는 게이트 전극(41)을 겸한 게이트 신호선(51), 및 이로 이루어진 드레인 신호선(52)을 구비하고 있고, 유기 EL 소자의 구동 전원으로 이루어지는 구동 전원선(53)을 배치한다.

계속해서, 게이트 절연막(42), 및 다결정 실리콘(이하, p-Si 라고 칭함)막으로 이루어지는 능동층(43)을 순서대로 형성하고, 그 능동층(43)에는, 소위 LDD(Lightly Doped Drain) 구조가 설치되어 있다. 그 왼쪽에 소스(43s), 및 드레인(43d)이 설치되어 있다.

그리고, 게이트 절연막(42), 능동층(43) 및 스토퍼 절연막(44) 상의 전면에는, SiO2막, SiN막 및 SiO2막의 순서대로 적층된 층간 절연막(45)을 설치하고, 드레인(43d)에 대응하여 설치한 콘택트 홀에 Al 등의 금속을 충전하여 드레인 전극(46)을 설치한다. 또한 전면에 예를 들면 유기 수지로 이루어져 표면을 평탄하게 하는 평탄화 절연막(47)을 설치한다.

이어서, 유기 EL 소자(60)의 구동용의 TFT인 제2 TFT(40)에 대해 설명한다.

도 4b에 도시된 바와 같이, 석영 유리, 무알칼리 유리 등으로 이루어지는 절연성 기판(10) 상에, Cr, Mo 등의 고융점 금속으로 이루어지고, 제1 TFT(30)의 게이트 전극(41)과 동시에 이 게이트 전극(41)은 용량 전극(55)과 접속되어 있는 게이트 전극(41)을 형성한다. 게이트 절연막(12), 및 p-Si막으로 이루어지는 능동층(43)을 순서대로 형성한다.

그 능동층(43)에는, 게이트 전극(41) 상측에 진성 또는 실질적으로 진성인 채널(43c)과, 이 채널(43c)의 양측에, 그 양측에 이온 도핑하여 소스(43s) 및 드레인(43d)이 설치되어 있다.

그리고, 게이트 절연막(12) 및 능동층(43) 상의 전면에, SiO막, SiN막 및 SiO막의 순서대로 적층된 층간 절연막(15)을 형성하고, 드레인(43d)에 대응하여 설치한 콘택트 홀에 Al등의 금속을 충전하여 구동 전원(50)에 접속된 구동 전원선(53)을 형성한다. 또한, 전면에 예를 들면, 유기 수지로 이루어진 표면을 평탄하게 하는 평탄화 절연막(17)을 형성한다. 그리고, 그 평탄화 절연막(17) 및 층간 절연막(15)의 소스(43s)에 대응한 위치에 콘택트 홀을 형성하고, 이 콘택트 홀을 통해 소스(43s)와 콘택트한 ITO(Indium Tin Oxide)로 이루어지는 투명 전극, 즉 유기 EL 소자의 양극(61)을 평탄화 절연막(17) 상에 형성한다.

유기 EL 소자(60)는, ITO 등의 투명 전극으로 이루어지는 양극(61), MTDATA(4,4',4''-tris(3-methylphenylphenylamino)triphenylamine: TPD)로 이루어지는 제1 홀 수송층, TPD(N,N'-diphenyl-N,N'-di(3-methylphenyl)-1,1'-biphenyl-4,4'-diamine)로 이루어지는 제2 홀 수송층, 퀴나크리돈(Quinacridone) 유도체를 포함하는 BeBq(bis(10-hydroxybenzo[h]quinolinato)beryllium)로 이루어지는 발광층 및 BeBq로 이루어지는 전자 수송층으로 이루어지는 발광 소자층(62), 마그네슘 인듐 합금으로 이루어지는 음극(63)의 미 순서로 적층 형성한 구조이다. 또한 홀 주입층을 갖는 표시장치로 발광시키는 색을 달리하게 할 경우에는 도 2에 도시한 바와 같이 양극(61)에 대응하여 상 형성으로 형성된다. 이 다른 발광 소자층(62) 및 음극(63)은, 또 2에 도시된 유기 EL 표시 장치를 형성하는 기판(10)의 전면, 즉 지면의 전면에 설치되어 있다.

또한, 유기 EL 소자는, 양극으로부터 주입된 홀과, 음극으로부터 주입된 전자가 발광층의 내부에서 재결합하고, 발광층을 형성하는 유기 분자를 여기하여 여기자(励起子)가 생긴다. 이 여기자가 발산 실활(失活)하는 과정에서, 발광층으로부터 빛이 방해지고, 이 빛이 투명한 양극으로부터, 투명 절연 기판을 통해 외부로 방출되어 발광한다.

그리고, 양극의 두께에 따른 스치에 기인하는 발광층의 절단에 의해 발생하는 음극(63)과 양극(61)과의 단락을 방지하기 위해, 양극(61)을 형성한 후, 그 양극(61)의 주변부에 절연막(64)(점선으로 둘러싸인 영역 외)을 형성한다. 그 후, 발광 소자층(62) 및 음극(63)을 형성한다. 그리고, 발광 소자층(62)에서 발광된 빛은 절연성 기판(10)을 투과하여 출사한다.

발명이 이루고자 하는 기술적 과제

그런데, 유기 EL 소자(60)는 상술된 바와 같이 제2 TFT(40)의 게이트 전극(41)에 인가된 전압에 따라 구동 전원선(53)으로부터의 전류를 유기 EL 소자로 공급함으로써 발광하는 소자이고, 양극으로부터 주입된 홀과, 음극으로부터 주입된 전자가 발광층의 내부에서 재결합하여 발광층으로부터 빛이 발해지는 것하 주입형의 발광이기 때문에 전류 제어 구동이다. 그 때문에, 예를 들면 100cd/㎡의 휘도를 얻기 위해서는 전류 밀도는 1mA/㎠이고, 10000cd/㎡의 휘도를 얻기 위해서는 전류 밀도는 약 100mA/㎠이다.

이와 같이 유기 EL 소자를 구동시키기 위해서는, 고전류가 필요하기 때문에, 양호한 표시를 얻기 위해서는, 직접 콘택트하는 반도체막인 소스(43s)와 ITO가 확실하게 도통하고 있을 필요가 있었다.

그러나, p-Si막인 소스(43s)와 ITO와의 콘택트부에서, p-Si막 표면이 산화하여 절연체인 SiO막이 형성되기 때문에 콘택트가 양호하며 양호한 표시를 얻을 수 없다고 하는 결점이 있었다.

또한, 소스(43s)와 ITO 사이에 p-Si 막보다도 저저항의 Al을 설치한 경우라도 Al막 표면에 절연막인 알루미늄 산화막(Al2O3막)이 형성되어, 안정된 콘택트를 얻을 수 없다는 결점이 있었다.

그래서 본 발명은, 상기한 종래의 결점을 감안하여 이루어진 것으로, 소스와 양극의 콘택트를 확실하게 확보하고, 양호한 표시를 얻을 수 있는 유기 EL 표시 장치를 제공하는 것을 목적으로 한다.

본 발명의 유기 EL 표시 장치는, 절연성 기판 상에, 소스를 갖는 반도체막을 구비한 박막 트랜지스터와, 상기 소스에 접속된 양극, 유기 재료로 이루어지는 발광층 및 음극이 순서대로 적층된 일렉트로 루미네센스 소자를 구비한 유기 일렉트로 루미네센스 표시 장치로서, 상기 소스와 상기 양극은, 상기 소스측의 도전 재료, 및 상기 양극측의 제1 고융점 금속을 통해 접속되어 있는 것이다.

또한, 본 발명의 유기 EL 표시 장치는, 상기 소스와 상기 양극은, 상기 소스측으로부터 순서대로 제2 고융점 금속, 도전 재료 및 제1 고융점 금속이 적층되어 접속되는 유기 EL 표시 장치이다.

또한, 본 발명의 유기 EL 표시 장치는, 상기 제1 또는 제2 고융점 금속은, 크롬(Cr), 몰리브덴(Mo), 탄탈(Ta), 티탄(Ti) 중 어느 하나를 포함한 재료로 이루어져 있고, 상기 도전 재료는 알루미늄(Al)을 포함한 재료로 이루어지는 유기 EL 표시 장치이다.

또한, 본 발명의 유기 EL 표시 장치는, 상기 양극은 산화인듐 주석 또는 산화인듐 아연으로 이루어지고, 상기 반도체막은 다결정 실리콘막으로 이루어지는 유기 EL 표시 장치이다.

발명의 구성 및 작용

이하에, 본 발명의 유기 EL 표시 장치에 대해 설명한다.

도 1에 본 발명의 유기 EL 표시 장치의 표시 화소부의 평면도를 나타내고, 도 2에 도 1의 B-B선에 따른 단면도를 도시한다. 또, 도 1의 A-A선에 따른 단면도는 상술된 도 4a와 동일하므로 생략한다.

도 1에 도시된 바와 같이, 게이트 신호선(51)과 드레인 신호선(52)으로 둘러싸인 영역에 유기 EL 소자 등으로 이루어지는 표시 화소가 형성되어 있다. 양 신호선의 교점 부근에는 제1 TFT(30)가 구비되어 있고, 그 TFT(30)의 소스(43s)는 유지 용량 전극선(54)상에서 용량 을 이루는 용량 전극(55)을 경합과 함께, 제2 TFT(40)의 게이트(41)에 접속되어 있다. 제2 TFT의 소스(43s)는 유기 EL 소자(60)의 양극(61)에 접속되고, 다른 드레인(43d)은 유기 EL 소자를 구동하는 구동 전원선(53)에 접속되어 있다.

표한, 표시 화소 부분에는, 게이트 신호선(51)과 평행하게 유지 용량 전극선(54)이 패치되어 있다. 이 유지 용량 전극선(54)은 알루 등으로 이루어져 있고, 게이트절연막(12)을 통해 TFT의 소스(43s)와 일체 형성된 용량 전극(55) 사이에서 전하를 축적하여 용량을 가지고 있다. 이 유지 용량은, 제2 TFT(40)의 게이트 전극(41)에 인가되는 전압을 유지하기 위해 설치되어 있다.

이와 같이 유기 EL 소자(60), 및 TFT(30), TFT(40)를 구비한 표시 화소가 기판(10) 상에 매트릭스형으로 배치됨에 따라 유기 EL 표시 장치가 형성된다.

도 2에 도시한 바와 같이, 유기 EL 표시 장치는, 유리나 합성 수지 등으로 이루어지는 기판 또는 도전성을 갖는 기판 또는 반도체 기판 등의 기판(10) 상에, TFT 및 유기 EL 소자를 순서대로 적층 형성하여 이루어진다. 또는 기판(10)으로서 도전성을 갖는 기판 및 반도체 기판을 이용하는 경우에는, 이들 기판(10) 상에 SiO2나 SiN 등의 절연막을 형성한 후에 TFT 및 유기 EL 표시 소자를 형성한다.

본 실시의 형태에서는, 제1 TFT(30) 및 제2 TFT(40) 모두, 게이트 전극(41, 41)을 능동층(43, 43)의 하측에 설치한 소위 하부 게이트형의 TFT이고, 반도체막을 강등층으로서 다결정 실리콘(Poly-Silicon, 이하, 「p-Si」라고 칭함)막을 이용한 경우를 도시한다. 또한, 게이트 전극(41, 41)이 더블 게이트 구조인 TFT의 경우를 나타낸다.

스위칭용의 TFT인 제1 TFT(30)에 대해서는 상세의 구조와 동일하므로 설명을 생략한다.

여기서, 유기 EL 소자(60)의 구동용의 TFT인 제2 TFT(40)에 대해 설명한다.

도 1 및 도 2에 도시한 바와 같이, 산화 유리, 무알칼리 유리 등으로 이루어지는 절연성 기판(10) 상에 Cr, Mo 등의 고융점 금속으로 이루어지고, 제1 TFT(30)의 게이트 전극(11)과 동시에 게이트 전극(41)을 형성한다. 게이트절연막(12), 및 p-Si 막으로 이루어지는 능동층(43)을 순서대로 형성한다.

또 능동층(43)에는, 게이트 전극(41) 상측에 진성 또는 실질적으로 진성인 채널(43c)과, 이 채널(43c)의 양측에 그 양측에 마운 도핑하여 소스(43s) 및 드레인(43d)이 설치되어 있다.

그리고, 게이트 절연막(12) 및 능동층(43) 상의 전면에, 예를 들면 SiO막, SiN 막 및 SiO막의 순서대로 적층된 층간 절연막(15)을 형성한다. 또한, 그 층간 절연막(15)에 소스(43s) 및 드레인(43d)에 각각 대응한 위치에 콘택트 홀(15s, 15d)을 형성한다. 그 콘택트 홀에 의해 노출된 능동층(43)을 포함하는 층간 절연막(15)의 전면에 제1 고융점 금속(21) 인, 예를 들면 Mo을 스퍼터법 등에 따라 퇴적하고, 연속하여 스퍼터법 등에 따라 도전 재료인 Al, 및 제2 고융점 금속(22)인, 예를 들면 Mo을 퇴적한다. 이렇게 하여 콘택트 홀 형성에 따라 노출한 능동층(43) 상에는, 능동층(43)측으로부터 Mo, Al, Mo가 적층된다. 그리고 포토리소 기술을 이용하여, 드레인(43d)에 대응한 콘택트 홀(15d) 및 층간 절연막(15) 상에는 Mo 및 Al로 이루어지는 구동 전원선(53)이 형성된다. 다른 소스(43s)에 대응한 콘택트 홀(15s) 및 층간 절연막(15) 상에는 소스 전극(45)이 형성된다. 이렇게 하여 형성된 소스 전극(45), 구동 전원선(53) 및 층간 절연막(15) 상에, 유기 수지로 이루어져 표면을 평탄하게 하는 평탄화 절연막(17)을 형성한다. 그리고, 그 평탄화 절연막(17)의 소스(43s)에 대응한 위치에 콘택트 홀(17s)을 형성한다. 그후, 콘택트 홀(17s) 및 평탄화 절연막(17)의 전면에 ITO를 퇴적하고, 포토리소 기술을 이용하여 투명 전극, 즉 유기 EL 소자의 양극(61)을 평탄화 절연막(17) 상에 형성한다.

유기 EL 소자(60)는, ITO 등의 투명 전극으로 이루어지는 양극(61), MTDATA(4,4',4''-tris(3-methylphenylphenylamino)triphenylamine, TPD)로 이루어지는 제1 홀 수송층, TPD(N,N'-diphenyl-N,N'-di(3-methylphenyl)-1,1'-biphenyl-4,4'-diamine)로 이루어지는 제2 홀 수송층, 퀴나크리돈(Quinacridone) 유도체를 포함하는 Bebq(bis(10-hydroxybenzo[h]quinolinato)beryllium)로 이루어지는 발광층, 및 Bebq로 이루어지는 전자 수송층으로 이루어지는 발광 소자층(62), 마그네슘 인듐 합금으로 이루어지는 음극(63)의 이 순서로 적층 형성된 구조이다. 이 음극(63)은, 도 1에 도시한 유기 EL 표시 장치를 형성하는 커패(10)의 전면, 즉 지면의 전면에 설치되어 있다.

또한 유기 EL 소자는, 양극으로부터 주입된 홀과, 음극으로부터 주입된 전자가 발광층의 내부에서 재결합하고, 발광층을 형성하는 유기 분자를 여기하여 여기자가 생긴다. 이 여기자가 방사실활하는 과정에서 발광층으로부터 빛이 발해지고, 이 빛이 투명한 양극으로부터 투명 절연 기판을 통해 외부로 방출되어 발광한다.

양극(61)의 주변에 절연막(54)(점선으로 나타내는 영역의 외측)을 형성한다. 이것은, 양극(61)의 두께에 따른 단차에 기인하는 발광층의 단절에 의해 생기는 음극(65)과 양극(61)과의 단락을 방지하기 위해 설치한다. 그리고, 양극(61) 상에 정공원 각 상(相)의 재료를 퇴적하여 발광층(62)을 형성한다. 또한 그 위에는, 들듯명 재료인, 마그네슘(Mg)과 인듐(In)과의, 합금으로 이루어지는 각 유기 EL 소자에 공통의 음극(63)을 TFT(40)의 상측을 포함하는 기판(10)의 전면에 형성한다.

이상과 같이, 본 발명의 유기 EL 표시 장치에 따르면, 구동 전원으로부터의 전류가 유기 EL 소자의 양극과 TFT의 소스사이에 흐르더도, p-Si 막보다도 저저항이고, 또한 표면에 산화막이 형성되기 어려운 고융점 금속을 이용함에 따라, 양자의 콘택트가 확실하게 확해져으로, 안정적으로 전류를 유기 EL 소자로 공급할 수 있고, 발기의 변동되거나 빠른 시간에 열화하는 것을 방지할 수 있다.

또, 본 실시예에서는, 제1 및 제2 고융점 금속으로서 Mo을 이용한 경우를 나타냈지만, 크롬(Cr), 탄탈(Ta), 텅스텐(W), 티탄(Ti) 중 어느 하나의 금속을 포함하면 되고, 이들 금속 중에서 하나를 선택하여 이용하는 것이 가능하고, 또한 이들 금속의 합금을 이용하는 것도 가능하다. 그 합금으로는 예를 들면 AlSi(알루미늄 실리콘) 합금, AlSiCu(알루미늄 실리콘 구리) 합금, AlNd (알루미늄 네오지움) 합금, MoW(몰리브 텅스텐) 합금, TiW(티탄텅스텐) 합금, TiN(티탄 텅스텐) 합금을 이용해도 좋다.

또한 본 실시예에서는, 양극의 재료로서 산화인듐 주석을 이용한 경우에 대해 설명했지만, 산화인듐 아연(In2O3-ZnO)을 이용해도 좋다.

또한, 제1 고융점 금속과 제2 고융점 금속은 서로 고융점 금속이라는 점 외에는 특별히 한정되지 않는다.

또한, 본 실시예에서는 도전 재료로서, 금을 이용한 경우에 대해 설명하였지만, 상기의 합금, 예를 들면 Al-Si(알루미늄 실리콘) 합금, Al-Si-Cu(알루미늄-실리콘-구리) 합금, Al-Ni(알루미늄-니오지움) 합금을 이용해도 된다.

효과의 요약

본 발명에 따르면, 기판의 능동층과 유기 FET 소자의 양극과의 콘택트가 확실하게 행해지므로, 안정된 표시를 얻을 수 있는 유기 FET 표시 장치를 얻을 수 있다.

도면의 간단한 설명

청구항 1

절연성 기판 상에, 소스를 갖는 반도체막을 구비한 보텀 트렌치 스타일, 상기 소스에 접속된 양극, 유기 재료로 이루어지는 발광층 및 음극이 순서대로 적층된 일렉트로 루미네센스 소자를 구비한 유기 일렉트로 루미네센스 표시 장치로서,

상기 소스와 상기 양극은, 상기 소스층의 도장 재료 및 상기 양극층의 제1 고융점 금속을 통해 접속되어 있는 것을 특징으로 하는 유기 일렉트로 루미네센스 표시 장치.

청구항 2

제1항에 있어서, 상기 소스와 상기 양극은, 상기 소스층으로부터 순서대로 제2 고융점 금속, 도전 재료 및 제1 고융점 금속이 적층되어 접속되는 것을 특징으로 하는 유기 일렉트로 루미네센스 표시 장치.

청구항 3

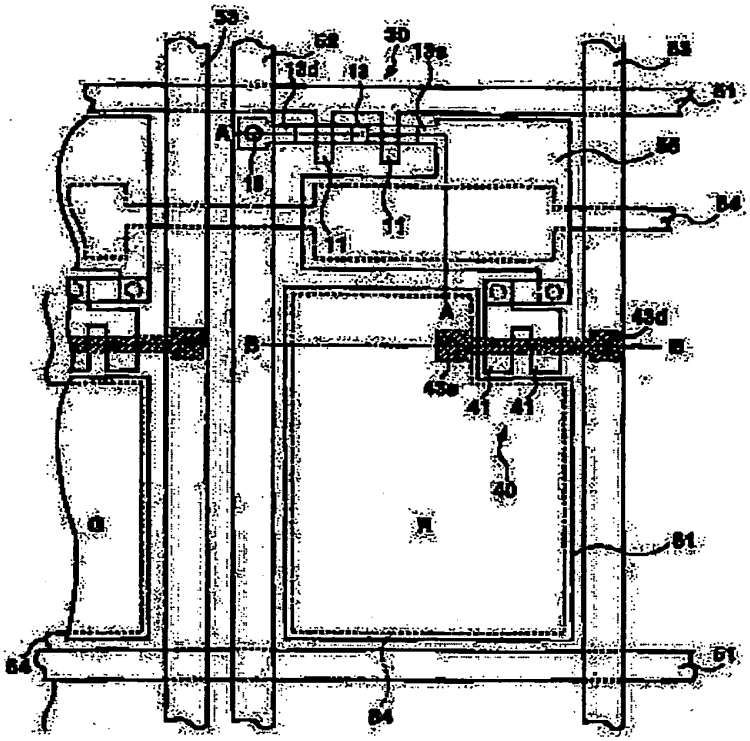
제1항 또는 제2항에 있어서, 상기 제1 또는 제2 고융점 금속은, 크롬(Cr), 몰리브덴(Mo), 텅스텐(W), 티탄(Ti) 중 어느 하나를 포함한 재료로 이루어져 있고, 상기 도전 재료는 알루미늄(Al)을 포함한 재료로 이루어지는 것을 특징으로 하는 유기 일렉트로 루미네센스 표시 장치.

청구항 4

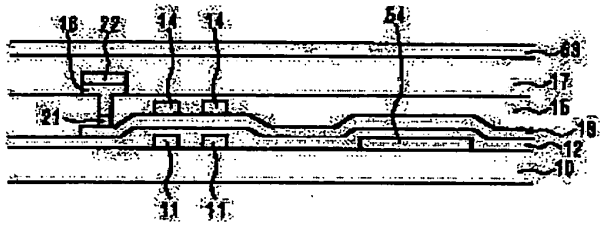
제1항 내지 제3항 중 어느 한 항에 있어서, 상기 양극은 산화인듐 주석 또는 산화인듐 아연으로 이루어지고, 상기 반도체막은 다결정 실리콘막으로 이루어지는 것을 특징으로 하는 유기 일렉트로 루미네센스 표시 장치.

도면

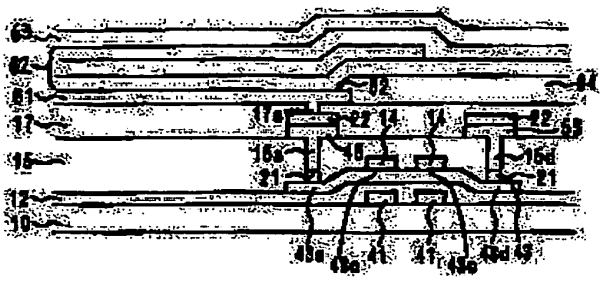
도면1


53
62
30
13a
13d
13
51
A
18
11
52
54
B
45d
45a
41
41
40
61
64
63
64

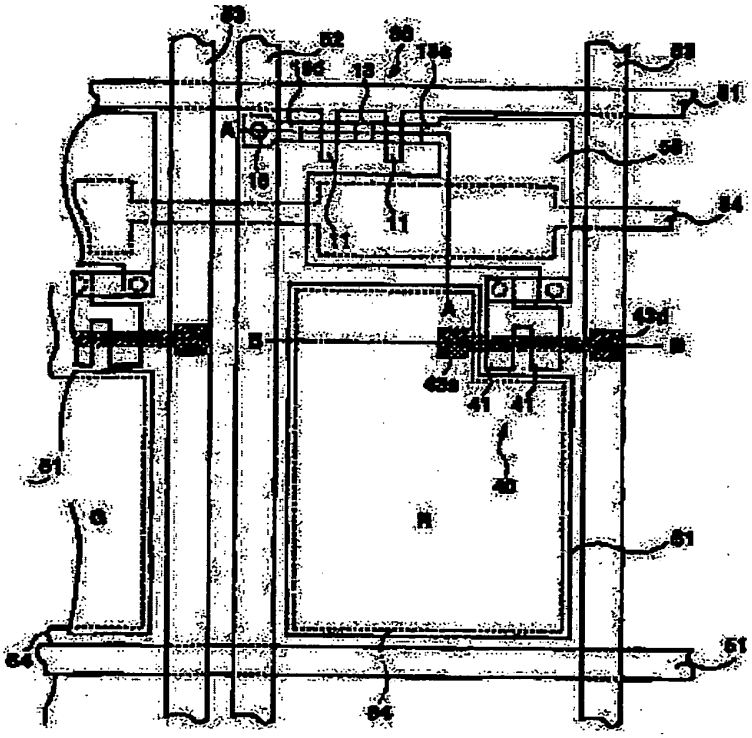
도면2


18
22
14
14
54
63
17
16
21
18
12
10
11
11

도면2b

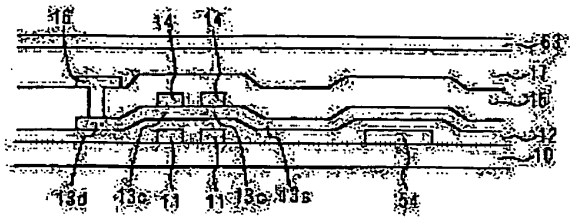


도면3

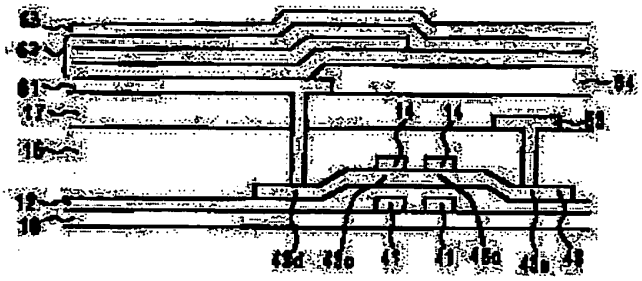


#7

도면4a



도면4b



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	Examiner	Art Unit	
	Eric Woods	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,8-10,14-33 and 37-45* is/are pending in the application.

4a) Of the above claim(s) *16-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-10,14,15 and 37-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments, see Remarks pages 1-2 and amendments to the claims, filed 13 January 2006, with respect to the rejection(s) of claim(s) 1-15 and 37-45 under various statutes have been fully considered and are persuasive.

Therefore, the rejections of claims 1-15 and 37-45 under 35 USC 103(a) has been withdrawn in view of applicant's amendments to the independent claims.

However, upon further consideration, a new ground(s) of rejection is made in view of various references as below.

Applicant has not contested examiner's statement (OA 10/13/2005 page 6) that claim 1 is merely a broader version of claim 4, and that they stand and fall together. It is additionally noted that the various other sections where examiner has designated claims as standing and falling together, applicant has not contested this assertion. Therefore, since this action closes prosecution, applicant has acquiesced in the grouping of these claims as set forth for purposes of appeal.

Priority

Applicant is kindly requested to specify which of claims 1-15 and 37-45 should receive which foreign priority date (since there are three Japanese applications from which priority has been claimed that have different dates, and no translations have been provided), as it is completely unclear which claims should receive the benefit of the 11/21/01, 12/05/01, and 11/20/02 dates.

Election/Restrictions

Claims 16-33 were withdrawn from consideration several Office Actions ago as per the restriction requirement, where the restriction requirement was not successfully traversed before the close of prosecution. Those claims have been withdrawn from consideration as drawn to a non-elected group, and must be canceled if the case were to be passed to issue.

Definitions

The term "electroluminescence element" will be taken to mean, as per the specification page 1 and previous interviews with applicant's representative, to include LEDs and organic light-emitting diodes (OLEDs) among other items. That is, the definition is taken to require active emission of light by application of an electrical signal or field. Applicant has not disputed this definition, which therefore will control for the duration of prosecution (should it be reopened) and/or on appeal.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 15 recites the limitation "said active element" in the last ('wherein') clause, where it is **exceptionally** unclear **which** active element is being referenced. There is insufficient antecedent basis for this limitation in the claim, and it is indefinite.

This rejection was necessitated by applicant's amendments.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-2, 4, 15, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yumoto et al (US 2004/0207615 A1). (Bolded segments added via amendment in last response).

As to claim 4,

An active matrix substrate, comprising a plurality of unit circuits arranged corresponding to intersections of a plurality of data lines and a plurality of scan lines, wherein each of said plurality of unit circuits comprises: (Yumoto Figure 2 shows an array of unit circuits on a substrate with a plurality of data lines and scan lines. Further, it is noted that any matrix display with greater than one pixel in both directions will inherently have multiple scan lines)

-A first transistor, comprising a first control terminal, a first terminal, and a second terminal, said first terminal connected in series to an electro-optical element; (Yumoto Figure 9, TFT one has a first terminal (upper one) connected in series with an electro-optical element (OLED))

-A holding element, connected to said first control terminal, and comprising a first electrode connected to said first control terminal and a second electrode connected to said second terminal; (Yumoto Figure 9, the holding element is capacitor C with one electrode connected to the control terminal (gate) of transistor TFT1; the second electrode is connected to ground, while the second terminal is also connected ground, which therefore are electrically contiguous and are connected together)

-A second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal being connected to one of said first terminal and said second terminal, said fourth terminal being connected to said first control terminal **and said second control terminal being connected to one of said scan lines** (Yumoto, Figure 9, TFT4 has two terminals, with the third terminal (the one on the left) being connected to the first terminal of TFT1; fourth terminal is connected to the first control terminal (gate) of TFT1. Yumoto clearly discloses that the second control terminal (of TFT4) is attached to a scan line (scanB). Yumoto Figure 18 clearly discloses an embodiment where TFT3 and TFT4 are both attached to **one** scan line, that is, where both the second and third control terminals are attached to a single scan line)

-A third transistor, comprising a fifth terminal, a sixth terminal, and a third control terminal, said fifth terminal being connected to a data line of said plurality of data lines,

said sixth terminal being connected to said third terminal and **said third control terminal being connected to said one of said scan lines**; (Yumoto Figure 9, TFT3 has two terminals and a control terminal, with the fifth terminal (the left one) clearly attached to a line labeled '**data**', and the sixth terminal on the right is clearly attached to the third terminal (the left one) of TFT4). Yumoto clearly discloses that TFT3 is attached to scanA. Yumoto Figure 18 clearly discloses an embodiment where TFT3 and TFT4 are both attached to **one** scan line, that is, where both the second and third control terminals are attached to a single scan line.)

-Wherein said second transistor has a multi-gate structure, and said electro-optical element is an electroluminescence element. (Yumoto shows in Figure 8 an implementation where TFT2 and TFT4 both consist of dual-gate devices, and the electro-optical element of Yumoto is an OLED, which as noted in the above definitions sections is clearly an EL element. It would have been obvious to modify the implementation of Yumoto in Figure 9 to use the dual-gate transistors of Figure 8 (as in TFT 4a/4b and TFT 2a/2b) because such structures suppress and lower leakage current [0073], and such a second transistor is explicitly shown having a dual-gate structure in Figure 8.)

Yumoto teaches all of the above limitations without expressly teaching that the second and third transistors have their control terminals (second and third) attached to the **same** scan line in the specified example (Figures 5-6 and 8-9), but does teach that limitation in Figure 18. In the shown embodiments, scanA and scanB are separate scan lines, but carry nearly identical information (see Figure 6, where scanB essentially only

carries an inverted version of the signal on scanA). This fact and exemplary configuration clearly illustrates that the scan lines could be combined as in Figure 18, where this only involves changing the type of one transistor (e.g. clearing of charge from certain transistors, e.g. erasure effect – [0064-0071]). This would be an obvious expedient in fabrication of the overall system, since it would reduce the number of overall parts (number of scan lines), and would be in keeping with the CCPA holding of *In re Karlson* (CCPA) 136 USPQ 184 (1963). Yumoto further teaches that such an arrangement is advantageous as it allows the removal of a driver circuit from the overall circuit [0090]. Therefore, such a modification would be an obvious expedient as above.

This is precisely the arrangement contemplated by the instant claim (see for example Figure 5 of the instant specification).

As to claim 1,

This claim is a broader version of claim 4, the rejection to which is incorporated by reference. As stated above, Yumoto teaches in [0073] that the dual-gate structure on TFT2 in Figure 8 serves to suppress leakage "during the off time" (e.g. during shutoff), and all the other limitations are taught in the rejection to claim 4 above. Claims 1 and 4 will stand and fall together. Yumoto provides scan lines (as scanA and scanB) in Figure 9.

As to claim 2, as noted above, Yumoto in [0073] teaches the multi-gate structure.

As to claim 15,

An electro-optical device including a plurality of electro-optical elements (see Yumoto Figure 2, the rejection to claim 1, etc.), comprising peripheral circuits (see Yumoto Figs.

7 and 11) to supply current to an electro-optical element of each pixel corresponding to said electro-optical elements, wherein each of said peripheral circuits comprises:

-A light-emission control active element to supply said current to said electro-optical element during a light emission period (Yumoto – this function can be served by recited first-active element; driving circuit can perform both tasks; see TFT5 in Fig. 13, or in Fig. 11. More specifically, see TFT2 in Figures 15-16);

-A holding element to hold a control voltage (Capacitor C in any of Figs. 11-16, Yumoto);

-A scan line (Yumoto shows elements scanA and scanB in Figures 9 and/or 11-16, and a plurality of scan lines in Figure 2, scan line SCAN in Figure 18)

-A first active element, comprising a gate terminal and a terminal, said gate terminal of which is connected to said holding element, which supplies a current and said scan line, based on said control voltage applied to the gate terminal, and said terminal being connected in series to said electro-optical element via said light-emission control active element (Yumoto --one example: TFT1, in Figs. 11-13 in Yumoto. Yumoto Figures 11 and 13 both clearly illustrate how the terminals are in series with the light-emission control active element. More specifically, see Figure 16 **only for the scan line and the holding element (with gate terminal) all connected to the scan line**, where a similar configuration is presented, where TFT4 is the active element, which has the gate terminal connected to scanB, which is connected through capacitor or holding element C2 to the scan line scanB, and also to the second or main holding element C, where as below such elements inherently supply a current. Clearly the terminal is connected to

TFT2, which constitutes the 'light –emission control active element' recited in the first part of the claim. It is prima facie obvious that the electro-optical element is in series with the transistor. A capacitor will inherently generate a current – any charge stored in a capacitor will be released as a current rather than a voltage, since the controlling equations for a capacitor are (simple parallel plate example only):

$C = \frac{Q}{V}$ $E_{stored} = 0.5 * C * V^2$ $I = \frac{dQ}{dt} = C\frac{dV}{dt} = C\frac{dV(t)}{dt}$ Where it is quite clear that such a holding element automatically generates a current with the shift in voltage, where the voltage across such a capacitor changes with the shifts in the scan line voltage, and thus always generates a changing current.);

-A current-controlling active element, that passes data current via said first active element during a selection period (TFT3 in Yumoto Figs. 11,13, 9); and,

-A second active element, connected between a first terminal to said current-controlling active element and said terminal and a second terminal to said holding element, which, during said selection period, charges said holding element and causes said control voltage to be stored, said second active element including a gate terminal including a gate terminal connected to said scan line (Yumoto -- see the rejection to claim 4, where this is the second transistor, TFT4, in Figures 11, 13-14, and 16 and the connections between the elements are shown there in the format listed. Specifically, note how TFT4 is connected between the scan line (that is, the gate terminal is connected to the scan line); the first terminal is connected to the 'current controlling active element (e.g. TFT5 in Figure 11, for example); and the second terminal is connected to the holding element C);

-Wherein said active element contains a structure to prevent leakage current during shutoff (Yumoto teaches in [0073] that the dual-gate structure on TFT2 in Figure 8 serves to suppress leakage "during the off time" (e.g. during shutoff)).

Reference Yumoto teaches the general two-transistor structure (Yumoto Figure 8, elements TFT 4a/4b instead of TFT4 by itself, elements TFT 2a/2b instead of TFT2 by itself (as in Figures 11-15) along with current-controlling elements and structures to prevent leakage current during shutoff. Yumoto teaches several different embodiments of peripheral structure for each pixel or unit circuit that contain all the recited elements as identified previously.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the unit pixel cells of Yumoto Figures 9, 11-13, with the multi-gate structures of Figure 8 to prevent leakage, as noted in [0073] for transistors of Yumoto, since both are aimed at active matrix panel applications (Yumoto Fig. 2, etc.) and to prevent variation due to device parameters (Yumoto 0017). Furthermore, certain functionality that is split off in this claim, e.g. making the light-emission control active element separable from the driving TFT, and splitting off the current-controlling active elements, are obvious and not patentable under *Nerwin v. Erlichman*, 168 USPQ 177, 179 (PTO Bd. Of Int. 1969), since applicant is merely making separable items which are claimed as integral functions in earlier claims (For example, claims 1 and 4 used as evidence claims for this justification). Secondly, if the adjustable argument is made by applicant (that adding elements making those features adjustable), under *In re Stevens*,

101 USPQ 284 (CCPA 1954) that doctrine will not hold, in "that the provision of adjustability, when needed, is not a patentable advance."

Additionally, it would have been obvious to have the connections through the secondary capacitance C2 as in Figure 16, since this [0088] effectively downwardly adjusts (slightly) the gate potential of the light-controlling active element (e.g. TFT2 in Figure 8 and Figure 16), which assists in better controlling that gate.

Finally, as noted above, it would have been obvious to use the same scan line (as in Figure 18). Yumoto teaches all of the above limitations without expressly teaching that the second and third transistors have their control terminals (second and third) attached to the **same** scan line in the specified example (Figures 5-6 and 8-9), but does teach that limitation in Figure 18. In the shown embodiments, scanA and scanB are separate scan lines, but carry nearly identical information (see Figure 6, where scanB essentially only carries an inverted version of the signal on scanA). This fact and exemplary configuration clearly illustrates that the scan lines could be combined as in Figure 18, where this only involves changing the type of one transistor (e.g. clearing of charge from certain transistors, e.g. erasure effect – [0064-0071]). This would be an obvious expedient in fabrication of the overall system, since it would reduce the number of overall parts (number of scan lines), and would be in keeping with the CCPA holding of *In re Karlson* (CCPA) 136 USPQ 184 (1963). Yumoto further teaches that such an arrangement is advantageous as it allows the removal of a driver circuit from the overall circuit [0090]. Therefore, such a modification would be an obvious expedient as above.

As to claim 41, the rejection to claim 4 is incorporated by reference; claim 4 is virtually identical to claim 4. The only difference is that the third transistor's purpose is to control current to the holding element, where it is prima facie obvious that any transistor that has a current-controlling terminal (e.g. first or second terminal in the terminology of the claims, source or drain to those of ordinary skill in the art) that is connected to a capacitor will prima facie control the current to the holding element; in this case, the third transistor is connected to the holding element and thusly will effect the current to it in some manner; further, the entire purpose of the capacitor is to retain charge from the data line, which therefore means that it will intrinsically be used for that purpose.

Take Yumoto Figure 9 – the control terminal of TFT4 (the third transistor) is connected to scanA, which is clearly a scan line. The other connections are as in the rejection to Figure 4. The EO element is clearly an OLED, which clearly qualifies as an EL element according to applicant's specification.

Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as unpatentable over Yumoto as applied to claim 1 above, and further in view of Gualandris.

As to claim 3,

The active matrix substrate according to claim 1, wherein at least said second active element is a transistor comprising a structure selected from the group consisting of an LDD structure, GDD structure, and DDD structure.

Yumoto teaches in [0113] to have the LDD structure in the active transistor, and it is discussed as being the active layer *per se*, that is on top of the gate oxide, so it would work for any transistor as specified there. However, Yumoto does not explicitly teach the use of GDD and DDD structures where Gualandris teaches DDD in 1:55-65, GDD in 2:25-30, and LDD in 2:25-30. Gualandris teaches that these are all methods of doping transistors, although one (the LDD) is preferred to work for 'ULSI' applications. Given that 'ULSI' applications at the time the patent was issued were mainly for deep sub-micron processes and that current TFT / liquid crystal display processes have much larger dimensions, e.g. still larger than one micron minimum channel length for silicon-on-glass technology, these techniques would be perfectly valid for use in TFT / silicon-on-glass technology.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix substrates of Yumoto with the transistors of Gualandris, since Yamada uses transistors, which *prima facie* have a source and a drain and different drain doping techniques are well-known in the art, and Yumoto also teaches LDD mechanisms of doping, and the others would be obvious to a worker of ordinary skill in the art.

As to claim 5,

The rejection to claim 4 is incorporated by reference. This claim is substantially similar, with the only exception that the required 'multi-gate' structure for the second transistor has been replaced by one of a group of LDD, GDD, and DDD structures. The additional

limitation is taught above in the rejection of claim 3, which is incorporated by reference. Claims 3 and 5 stand and fall together.

Claims 8-10 and 37-44 are rejected under 35 U.S.C. 103(a) as unpatentable over Yumoto as applied to claim 4 above, and further in view of Maeda.

As to claim 8,

The active matrix substrate according to any of claims 4 through 7, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yumoto Figure 3 and [0010] for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yumoto [0011], semiconductor thin film 4); and

-A gate metal layer comprising said second control terminal (Yumoto [0011], gate electrode 2)(forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one scan line among said plurality of scan lines is formed in said gate metal layer (Maeda 0121).

References Yumoto teaches all the limitations of this claim except the formation of a scan line in the gate metal layer. Reference Maeda teaches the formation of scan lines and gate electrodes in the same metal film layer for TFT / LCD monitor fabrication (e.g. 0162, 0121). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single

metal layer of Maeda since Maeda performs in one step what Yumoto does in several steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode goes down first and then the scan lines go down after the semiconductor layer, which clearly is a different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination, e.g. common sense is sufficient to justify the combination. See also *In re Karlson*, 136 USPQ 184 (CCPA 1963), for the doctrine that eliminating components is an obvious expedient – in this, eliminating fabrication steps.

As to claim 9,

The active matrix substrate according to any of claims 4 through 7, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yumoto Figure 3 and [0010] for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yumoto [0011], semiconductor thin film 4); and

-A gate metal layer comprising said second control terminal (Yumoto [0012]) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in said gate metal layer (Maeda 0121 and 0113 and 0125).

Reference Yumoto teaches all the limitations of this claim except the formation of a data line in the gate metal layer. Reference Maeda teaches the formation of data lines and source and drain electrodes in the same metal film layer for TFT / LCD

monitor fabrication (e.g. 0113, 0125). It would be *prima facie* obvious to choose to form gate electrodes and data lines simultaneously rather than gate electrodes and scan lines, for example. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single metal layer of Maeda since Maeda performs in one step what Yumoto does in several steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode goes down first and then the scan lines go down after the semiconductor layer, which clearly is a different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

As to claim 10,

The active matrix substrate according to any of claims 4 through 7, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yumoto Figure 3 and [0010] for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yumoto [0011], semiconductor thin film 4); and

-A gate metal layer comprising said second control terminal (Yumoto [0012]) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-A source metal layer comprising a source electrode or drain electrode connected to the source or drain of said second transistor (Maeda 0113, 0125); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in the layer (Maeda 0121 and 0113 and 0125), among said source metal layer and said gate metal layer, which is closer to said semiconductor layer.

Reference Maeda in combination with Yumoto teaches all the limitations of this claim, and this is merely a recitation of the dual limitations of claims 8 and 9 above. As such, the combination and motivation from claim 8 is used here and no further comment is necessary, as this claim is only a nominal variation of the parent.

As to claim 37,

An active matrix substrate according to claim 4, comprising unit circuits comprising transistors, arranged corresponding to intersections of data lines and scan lines (Yumoto Figure 2, and the transistor picture layouts in Figures 5, 8, 9, etc) wherein

-A semiconductor layer constituting such transistors is formed in a semiconductor layer (Yumoto [0011], semiconductor thin film 4);

-Either said scan lines or said data lines are formed in a first conducting layer at the intersections of said scan lines and said data lines (Maeda 0113, 0121, and 0125); and,

-A portion of said scan lines and said data lines outside said intersections are formed in a second conducting layer (Maeda 0113, 0121, and 0125).

Reference Yumoto does not explicitly teach the formation of scan or data lines formed in a conducting layer at the intersections of such lines. Reference Maeda describes forming gate metal and scan lines, etc. simultaneously. As such, the scan lines would be formed everywhere not masked with a shadow mask, e.g. both in the scan lines and in the intersections. No matter what portions of the lines are claimed,

any such configuration could be made using shadow masking and formed using either evaporation or sputtering. Any set of contacts could be created using correctly etched contact holes; electrically contiguous metal formed in the same layer is *prima facie* the same from an electrical and an engineering perspective. Further, forming scan lines or data lines or portions thereof (as claimed) in the same layer as other things would simply be making a component integral by eliminating unnecessary metal, and under *In re Larson*, 144 USPQ 347 (CCPA 1965), making a component integral is obvious and not patentable. Therefore, under either methodology, the recited limitations of the claim have been met.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single metal layer of Maeda since Maeda performs in one step what Yumoto does in several steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode goes down first and then the scan lines go down after the semiconductor layer, which clearly is a different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

As to claim 39,

An electro-optical device according to claim 4, comprising electro-optical elements corresponding to intersections of scan lines and data lines (Yumoto, element OLED in various figures, such as 5, 8, 9, etc), wherein:

-A pair of electrodes is provided to supply power to electro-optical elements (Maeda Fig. 11C, elements 19 and 15 are opposing and pixel electrodes (see 0006-0008));

-At the intersections of said scan lines and said data lines, either said scan lines or said data lines are formed in a first conducting layer (Maeda 0113, 0118, 0121, 0125 – again, gate metal as discussed in rejections to claims 8-12);

-Portions of said scan lines and said data lines outside said intersections are formed in a second conducting layer (source metal layer, 0113, 0118, 0121, 0125 as discussed in rejections to claims 8-12); and,

-Said second conducting layer is positioned at a greater distance than said first conducting layer from one of said pair of electrodes (design choice issue, see Maeda Fig. 11C).

Reference Yumoto does not recite details of the fabrication process claimed above. Reference Maeda teaches the fabrication of such substrates and teaches contact holes (0044, 0047). Logically, such contact holes would fill on conducting layer deposition, thus meeting the recited limitation concerning intersections of data and scan lines. The positioning of a layer or its size is *prima facie* obvious and is not patentable (*In re Japikse* for order of parts and further under *In re Reese*, anyone of ordinary skill in the art would know that there would be an optimal spacing of electrodes from each other to minimize cross-talk that would also occupy the minimum aspect ratio required on the shadow mask).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single metal layer of Maeda since Maeda performs in one step what Yumoto does in several steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode goes down

first and then the scan lines go down after the semiconductor layer, which clearly is a different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

As to claim 40, reference Yumoto clearly teaches in [0098] that the first transistor (TFT1) is an n-channel type and that the second transistor (TFT3, but as noted in [0100-0101, particularly [0101], TFT4 has the same conductivity type as TFT3) has a p-channel, which are prima facie opposite polarities. Motivation and combination are taken from claim 39.

Claim 38 is rejected over Yumoto and Maeda as applied to claim 37 above, and further in view of Tanaka.

As to claim 38,

The active matrix substrate according to claim 37, wherein said second conducting layer is positioned between said first conducting layer and said semiconductor layer.

Reference Yumoto does not explicitly teach this limitation. In Fig. 10B, Maeda shows that the bottom gate – element 56, which is metal (a niobium alloy) is put down first, then various insulating materials, then element 13 (source and drain electrodes) are formed on the same level and slightly covering the semiconductor layer 54. Under the doctrine of *In re Japikse*, switching the two layers would be *prima facie* obvious, and only minor alternations in the shadow masks for the process would be necessary (additive vs. subtractive processing in semiconductors, for example, switching the process would not be difficult for one of ordinary skill in the semiconductor / TFT art).

Again, given that Maeda teaches many different embodiments (see Figs. 10-13, etc.), such a switch would be a design choice issue, and it would allow low-temperature processing of the substrate throughout the process, particularly allowing for newer techniques such as laser annealing and recrystallization of the semiconductor layer taught by Tanaka, and treatment of the semiconductor layer towards the end of processing.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the TFT circuits of Yumoto and Maeda with the laser annealing processing of polysilicon for TFT applications of Tanaka (see 0002-0015), as both Yumoto ([0011-0013]) and Maeda (0008, 0121, etc.) utilize polysilicon as the semiconductor material, and laser annealing is now a well-known, standard process in the art.

Claims 42-44 are rejected under 35 U.S.C. 103(a) as unpatentable over Yumoto as applied to claim 41 above, and further in view of Maeda (claim 4 operative here – any of the other claims would be subject to the same rejection).

As to claim 42,

The active matrix substrate according to claim 41, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yumoto Figure 3 and [0010] for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yumoto [0011], semiconductor thin film 4); and

-A gate metal layer comprising said second control terminal (Yumoto [0012]) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one scan line among said plurality of scan lines is formed in said gate metal layer (Maeda 0121).

References Yumoto teach all the limitations of this claim except the formation of a scan line in the gate metal layer. Reference Maeda teaches the formation of scan lines and gate electrodes in the same metal film layer for TFT / LCD monitor fabrication (e.g. 0162, 0121). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single metal layer of Maeda since Maeda performs in one step what Yumoto does in several steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode goes down first and then the scan lines go down after the semiconductor layer, which clearly is a different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination, e.g. common sense is sufficient to justify the combination. See also *In re Karlson*, 136 USPQ 184 (CCPA 1963), for the doctrine that eliminating components is an obvious expedient – in this, eliminating fabrication steps.

As to claim 43,

The active matrix substrate according to claim 41, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yumoto Figure 3 and [0010] for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yumoto [0011], semiconductor thin film 4); and

-A gate metal layer comprising said second control terminal (Yumoto [0012]) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in said gate metal layer (Maeda 0121 and 0113 and 0125).

Reference Yumoto teaches all the limitations of this claim except the formation of a data line in the gate metal layer. Reference Maeda teaches the formation of data lines and source and drain electrodes in the same metal film layer for TFT / LCD monitor fabrication (e.g. 0113, 0125). It would be *prima facie* obvious to choose to form gate electrodes and data lines simultaneously rather than gate electrodes and scan lines, for example. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single metal layer of Maeda since Maeda performs in one step what Yumoto does in several steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode goes down first and then the scan lines go down after the semiconductor layer, which clearly is a different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

As to claim 44,

The active matrix substrate according to claim 41, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yumoto Figure 3 and [0010] for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yumoto [0011], semiconductor thin film 4); and

-A gate metal layer comprising said second control terminal (Yumoto [0012]) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-A source metal layer comprising a source electrode or drain electrode connected to the source or drain of said second transistor (Maeda 0113, 0125); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in the layer (Maeda 0121 and 0113 and 0125), among said source metal layer and said gate metal layer, which is closer to said semiconductor layer.

Reference Maeda in combination with Yumoto teaches all the limitations of this claim, and this is merely a recitation of the dual limitations of claims 42 and 43 above. As such, the combination and motivation from claim 42 is used here and no further comment is necessary, as this claim is only a nominal variation of the parent.

Claim 45 is rejected under 35 U.S.C. 103(a) as unpatentable over Yumoto as applied to claim 41 above, and further in view of Gualandris. The rejection to claim 41 is herein incorporated by reference in its entirety.

Claim 45 is a substantial duplicate of claim 41, with the only difference being the addition of the limitation from claim 3:

Wherein at least said second active element is a transistor comprising a structure selected from the group consisting of an LDD structure, GDD structure, and DDD structure.

Yumoto teaches in [0113] to have the LDD structure in the active transistor, and it is discussed as being the active layer *per se*, that is on top of the gate oxide, so it would work for any transistor as specified there. However, Yumoto does not explicitly teach the use of GDD and DDD structures where Gualandris teaches DDD in 1:55-65, GDD in 2:25-30, and LDD in 2:25-30. Gualandris teaches that these are all methods of doping transistors, although one (the LDD) is preferred to work for 'ULSI' applications. Given that 'ULSI' applications at the time the patent was issued were mainly for deep sub-micron processes and that current TFT / liquid crystal display processes have much larger dimensions, e.g. still larger than one micron minimum channel length for silicon-on-glass technology, these techniques would be perfectly valid for use in TFT / silicon-on-glass technology.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix substrates of Yumoto with the transistors of Gualandris, since Yamada uses transistors, which *prima facie* have a source and a drain and different drain doping techniques are well-known in the art, and Yumoto also teaches LDD mechanisms of doping, and the others would be obvious to a worker of ordinary skill in the art.

Claims 1-2, 4, 15, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yumoto et al (US 2004/0207615 A1) in view of Kim et al (US PGPub 2001/0019327). (Bolded segments added via amendment in last response).

As to claim 4,

An active matrix substrate, comprising a plurality of unit circuits arranged corresponding to intersections of a plurality of data lines and a plurality of scan lines, wherein each of said plurality of unit circuits comprises: (Yumoto Figure 2 shows an array of unit circuits on a substrate with a plurality of data lines and scan lines. Further, it is noted that any matrix display with greater than one pixel in both directions will inherently have multiple scan lines)

-A first transistor, comprising a first control terminal, a first terminal, and a second terminal, said first terminal connected in series to an electro-optical element; (Yumoto Figure 9, TFT one has a first terminal (upper one) connected in series with an electro-optical element (OLED))

-A holding element, connected to said first control terminal, and comprising a first electrode connected to said first control terminal and a second electrode connected to said second terminal; (Yumoto Figure 9, the holding element is capacitor C with one electrode connected to the control terminal (gate) of transistor TFT1; the second

electrode is connected to ground, while the second terminal is also connected ground, which therefore are electrically contiguous and are connected together)

-A second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, said third terminal being connected to one of said first terminal and said second terminal, said fourth terminal being connected to said first control terminal **and said second control terminal being connected to one of said scan lines** (Yumoto, Figure 9, TFT4 has two terminals, with the third terminal (the one on the left) being connected to the first terminal of TFT1; fourth terminal is connected to the first control terminal (gate) of TFT1. Yumoto clearly discloses that the second control terminal (of TFT4) is attached to a scan line (scanB).)

-A third transistor, comprising a fifth terminal, a sixth terminal, and a third control terminal, said fifth terminal being connected to a data line of said plurality of data lines, said sixth terminal being connected to said third terminal and **said third control terminal being connected to said one of said scan lines**; (Yumoto Figure 9, TFT3 has two terminals and a control terminal, with the fifth terminal (the left one) clearly attached to a line labeled '**data**', and the sixth terminal on the right is clearly attached to the third terminal (the left one) of TFT4). Yumoto clearly discloses that TFT3 is attached to scanA)

-Wherein said second transistor has a multi-gate structure, and said electro-optical element is an electroluminescence element. (Yumoto shows in Figure 8 an implementation where TFT2 and TFT4 both consist of dual-gate devices, and the electro-optical element of Yumoto is an OLED, which as noted in the above definitions

sections is clearly an EL element. It would have been obvious to modify the implementation of Yumoto in Figure 9 to use the dual-gate transistors of Figure 8 (as in TFT 4a/4b and TFT 2a/2b) because such structures suppress and lower leakage current [0073], and such a second transistor is explicitly shown having a dual-gate structure in Figure 8.)

Yumoto teaches all of the above limitations except expressly teaching that the second and third transistors have their control terminals (second and third) attached to the **same** scan line, but at least suggests it in Figure 18, where a single scan line is shown. In the shown embodiments, scanA and scanB are separate scan lines, but carry nearly identical information (see Figure 6, where scanB essentially only carries an inverted version of the signal on scanA). This fact and exemplary configuration clearly illustrates that the scan lines could probably be combined if the transistor type were inverted (e.g. PMOS v. NMOS) or the circuit slightly reconfigured such that the purpose of having different scanlines (e.g. clearing of charge from certain transistors, e.g. erasure effect – [0064-0071]). This would be an obvious expedient in fabrication of the overall system, since it would reduce the number of overall parts, and would be in keeping with the CCPA holding of *In re Karlson* (CCPA) 136 USPQ 184 (1963).

As noted above, Kim clearly shows in Figure 3 a case where comparable transistors use the same scan line – that is, elements Q3 and Q4 share the same scan line. This is precisely the arrangement contemplated by the instant claim (see for example Figure 5 of the instant specification). Kim clearly has transistors in a configuration that is comparable to that shown in Yumoto Figures 5, 8, and 9 wherein

the scan lines are configured in a similar manner and they shared (as in Kim Figures 2A, 3, and 4). Motivation for having such a scan line shared between elements Q3 and Q4 as in Kim Figures 2A, 3, and 4 can be found in [0046-0048]. Such transistors can be PMOS entirely, thusly not requiring the separate and inverted control signals found in Yumoto, and further evidenced by the fact that this configuration is found to be the system emulates a current mirror only when engaged, thusly providing additional benefits over the system of Yumoto [0051-0055], which acts as a current mirror at all times, which requires additional design steps and consideration that the system of Kim addresses. Finally, since the system of Kim allows the same level of control as that of Yumoto (in, for example, Figure 9), it therefore is more compact and efficient for at least all of the above reasons and the logic put forth by the CAFC in their opinion given as *In re Karlson*.

As to claim 1,

This claim is a broader version of claim 4, the rejection to which is incorporated by reference. As stated above, Yumoto teaches in [0073] that the dual-gate structure on TFT2 in Figure 8 serves to suppress leakage "during the off time" (e.g. during shutoff), and all the other limitations are taught in the rejection to claim 4 above. Claims 1 and 4 will stand and fall together. Yumoto provides scan lines (as scanA and scanB) in Figure 9.

As to claim 2, as noted above, Yumoto in [0073] teaches the multi-gate structure.

As to claim 15,

An electro-optical device including a plurality of electro-optical elements (see Yumoto Figure 2, the rejection to claim 1, etc.), comprising peripheral circuits (see Yumoto Figs. 7 and 11) to supply current to an electro-optical element of each pixel corresponding to said electro-optical elements, wherein each of said peripheral circuits comprises:

-A light-emission control active element to supply said current to said electro-optical element during a light emission period (Yumoto – this function can be served by recited first-active element; driving circuit can perform both tasks; see TFT5 in Fig. 13, or in Fig. 11. More specifically, see TFT2 in Figures 15-16);

-A holding element to hold a control voltage (Capacitor C in any of Figs. 11-16, Yumoto);

-A scan line (Yumoto shows elements scanA and scanB in Figures 9 and/or 11-16, and a plurality of scan lines in Figure 2, scan line SCAN in Figure 18)

-A first active element, comprising a gate terminal and a terminal, said gate terminal of which is connected to said holding element, which supplies a current and said scan line, based on said control voltage applied to the gate terminal, and said terminal being connected in series to said electro-optical element via said light-emission control active element (Yumoto --one example: TFT1, in Figs. 11-13 in Yumoto. Yumoto Figures 11 and 13 both clearly illustrate how the terminals are in series with the light-emission control active element. More specifically, see Figure 16 **only for the scan line and the holding element (with gate terminal) all connected to the scan line**, where a similar configuration is presented, where TFT4 is the active element, which has the gate terminal connected to scanB, which is connected through capacitor or holding element

C2 to the scan line scanB, and also to the second or main holding element C, where as below such elements inherently supply a current. Clearly the terminal is connected to TFT2, which constitutes the 'light –emission control active element' recited in the first part of the claim. It is prima facie obvious that the electro-optical element is in series with the transistor. A capacitor will inherently generate a current – any charge stored in a capacitor will be released as a current rather than a voltage, since the controlling equations for a capacitor are (simple parallel plate example only):

$C = \frac{Q}{V}$ $E_{stored} = 0.5 * C * V^2$ $I = \frac{dQ}{dt} = C\frac{dV}{dt} = C\frac{dV(t)}{dt}$ Where it is quite clear that such a holding element automatically generates a current with the shift in voltage, where the voltage across such a capacitor changes with the shifts in the scan line voltage, and thus always generates a changing current.);

-A current-controlling active element, that passes data current via said first active element during a selection period (TFT3 in Yumoto Figs. 11,13, 9); and,

-A second active element, connected between a first terminal to said current-controlling active element and said terminal and a second terminal to said holding element, which, during said selection period, charges said holding element and causes said control voltage to be stored, said second active element including a gate terminal including a gate terminal connected to said scan line (Yumoto -- see the rejection to claim 4, where this is the second transistor, TFT4, in Figures 11, 13-14, and 16 and the connections between the elements are shown there in the format listed. Specifically, note how TFT4 is connected between the scan line (that is, the gate terminal is connected to the scan line); the first terminal is connected to the 'current controlling active element (e.g. TFT5

in Figure 11, for example); and the second terminal is connected to the holding element C);

-Wherein said active element contains a structure to prevent leakage current during shutoff (Yumoto teaches in [0073] that the dual-gate structure on TFT2 in Figure 8 serves to suppress leakage "during the off time" (e.g. during shutoff)).

Reference Yumoto teaches the general two-transistor structure (Yumoto Figure 8, elements TFT 4a/4b instead of TFT4 by itself, elements TFT 2a/2b instead of TFT2 by itself (as in Figures 11-15) along with current-controlling elements and structures to prevent leakage current during shutoff. Yumoto teaches several different embodiments of peripheral structure for each pixel or unit circuit that contain all the recited elements as identified previously.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the unit pixel cells of Yumoto Figures 9, 11-13, with the multi-gate structures of Figure 8 to prevent leakage, as noted in [0073] for transistors of Yumoto, since both are aimed at active matrix panel applications (Yumoto Fig. 2, etc.) and to prevent variation due to device parameters (Yumoto 0017). Furthermore, certain functionality that is split off in this claim, e.g. making the light-emission control active element separable from the driving TFT, and splitting off the current-controlling active elements, are obvious and not patentable under *Nerwin v. Erlichman*, 168 USPQ 177, 179 (PTO Bd. Of Int. 1969), since applicant is merely making separable items which are claimed as integral functions in earlier claims (For example, claims 1 and 4 used as evidence claims for this justification). Secondly, if the adjustable argument is made by

applicant (that adding elements making those features adjustable), under *In re Stevens*, 101 USPQ 284 (CCPA 1954) that doctrine will not hold, in "that the provision of adjustability, when needed, is not a patentable advance."

Additionally, it would have been obvious to have the connections through the secondary capacitance C2 as in Figure 16, since this [0088] effectively downwardly adjusts (slightly) the gate potential of the light-controlling active element (e.g. TFT2 in Figure 8 and Figure 16), which assists in better controlling that gate.

Finally, as noted above, it would have been obvious to use the same scan line (as in Figure 18). Yumoto teaches all of the above limitations without expressly teaching that the second and third transistors have their control terminals (second and third) attached to the **same** scan line in the specified example (Figures 5-6 and 8-9), but does teach that limitation in Figure 18. In the shown embodiments, scanA and scanB are separate scan lines, but carry nearly identical information (see Figure 6, where scanB essentially only carries an inverted version of the signal on scanA). This fact and exemplary configuration clearly illustrates that the scan lines could be combined as in Figure 18, where this only involves changing the type of one transistor (e.g. clearing of charge from certain transistors, e.g. erasure effect – [0064-0071]). This would be an obvious expedient in fabrication of the overall system, since it would reduce the number of overall parts (number of scan lines), and would be in keeping with the CCPA holding of *In re Karlson* (CCPA) 136 USPQ 184 (1963). Yumoto further teaches that such an arrangement is advantageous as it allows the removal of a driver circuit from the overall circuit [0090]. Therefore, such a modification would be an obvious expedient as above.

Finally, motivation and rationale for having both transistors connected to the scan line and other details are incorporated by reference along with the entirety of the rejection of claim 4 above.

As to claim 41, the rejection to claim 4 is incorporated by reference; claim 4 is virtually identical to claim 4. The only difference is that the third transistor's purpose is to control current to the holding element, where it is prima facie obvious that any transistor that has a current-controlling terminal (e.g. first or second terminal in the terminology of the claims, source or drain to those of ordinary skill in the art) that is connected to a capacitor will prima facie control the current to the holding element; in this case, the third transistor is connected to the holding element and thusly will effect the current to it in some manner; further, the entire purpose of the capacitor is to retain charge from the data line, which therefore means that it will intrinsically be used for that purpose.

Take Yumoto Figure 9 – the control terminal of TFT4 (the third transistor) is connected to scanA, which is clearly a scan line. The other connections are as in the rejection to Figure 4. The EO element is clearly an OLED, which clearly qualifies as an EL element according to applicant's specification.

Finally, motivation and rationale for having both transistors connected to the scan line and other details are incorporated by reference along with the entirety of the rejection of claim 4 above.

Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as unpatentable over Yumoto and Kim as applied to claim 1 above, and further in view of Gualandris.

As to claim 3,

The active matrix substrate according to claim 1, wherein at least said second active element is a transistor comprising a structure selected from the group consisting of an LDD structure, GDD structure, and DDD structure.

Yumoto teaches in [0113] to have the LDD structure in the active transistor, and it is discussed as being the active layer *per se*, that is on top of the gate oxide, so it would work for any transistor as specified there. However, Yumoto does not explicitly teach the use of GDD and DDD structures where Gualandris teaches DDD in 1:55-65, GDD in 2:25-30, and LDD in 2:25-30. Gualandris teaches that these are all methods of doping transistors, although one (the LDD) is preferred to work for 'ULSI' applications. Given that 'ULSI' applications at the time the patent was issued were mainly for deep sub-micron processes and that current TFT / liquid crystal display processes have much larger dimensions, e.g. still larger than one micron minimum channel length for silicon-on-glass technology, these techniques would be perfectly valid for use in TFT / silicon-on-glass technology.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix substrates of Yumoto with the transistors of Gualandris, since Yamada uses transistors, which *prima facie* have a source and a drain and different drain doping techniques are well-known in the art, and

Yumoto also teaches LDD mechanisms of doping, and the others would be obvious to a worker of ordinary skill in the art.

As to claim 5,

The rejection to claim 4 is incorporated by reference. This claim is substantially similar, with the only exception that the required 'multi-gate' structure for the second transistor has been replaced by one of a group of LDD, GDD, and DDD structures. The additional limitation is taught above in the rejection of claim 3, which is incorporated by reference. Claims 3 and 5 stand and fall together.

Claims 8-10 and 37-44 are rejected under 35 U.S.C. 103(a) as unpatentable over Yumoto and Kim as applied to claim 4 above, and further in view of Maeda.

As to claim 8,

The active matrix substrate according to any of claims 4 through 7, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yumoto Figure 3 and [0010] for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yumoto [0011], semiconductor thin film 4); and

-A gate metal layer comprising said second control terminal (Yumoto [0011], gate electrode 2)(forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one scan line among said plurality of scan lines is formed in said gate metal layer (Maeda 0121).

References Yumoto teaches all the limitations of this claim except the formation of a scan line in the gate metal layer. Reference Maeda teaches the formation of scan lines and gate electrodes in the same metal film layer for TFT / LCD monitor fabrication (e.g. 0162, 0121). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single metal layer of Maeda since Maeda performs in one step what Yumoto does in several steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode goes down first and then the scan lines go down after the semiconductor layer, which clearly is a different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination, e.g. common sense is sufficient to justify the combination. See also *In re Karlson*, 136 USPQ 184 (CCPA 1963), for the doctrine that eliminating components is an obvious expedient – in this, eliminating fabrication steps.

As to claim 9,

The active matrix substrate according to any of claims 4 through 7, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yumoto Figure 3 and [0010] for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yumoto [0011], semiconductor thin film 4); and

-A gate metal layer comprising said second control terminal (Yumoto [0012]) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in said gate metal layer (Maeda 0121 and 0113 and 0125).

Reference Yumoto teaches all the limitations of this claim except the formation of a data line in the gate metal layer. Reference Maeda teaches the formation of data lines and source and drain electrodes in the same metal film layer for TFT / LCD monitor fabrication (e.g. 0113, 0125). It would be *prima facie* obvious to choose to form gate electrodes and data lines simultaneously rather than gate electrodes and scan lines, for example. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single metal layer of Maeda since Maeda performs in one step what Yumoto does in several steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode goes down first and then the scan lines go down after the semiconductor layer, which clearly is a different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

As to claim 10,

The active matrix substrate according to any of claims 4 through 7, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yumoto Figure 3 and [0010] for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yumoto [0011], semiconductor thin film 4); and

-A gate metal layer comprising said second control terminal (Yumoto [0012]) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-A source metal layer comprising a source electrode or drain electrode connected to the source or drain of said second transistor (Maeda 0113, 0125); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in the layer (Maeda 0121 and 0113 and 0125), among said source metal layer and said gate metal layer, which is closer to said semiconductor layer.

Reference Maeda in combination with Yumoto teaches all the limitations of this claim, and this is merely a recitation of the dual limitations of claims 8 and 9 above. As such, the combination and motivation from claim 8 is used here and no further comment is necessary, as this claim is only a nominal variation of the parent.

As to claim 37,

An active matrix substrate according to claim 4, comprising unit circuits comprising transistors, arranged corresponding to intersections of data lines and scan lines (Yumoto Figure 2, and the transistor picture layouts in Figures 5, 8, 9, etc) wherein

-A semiconductor layer constituting such transistors is formed in a semiconductor layer (Yumoto [0011], semiconductor thin film 4);

-Either said scan lines or said data lines are formed in a first conducting layer at the intersections of said scan lines and said data lines (Maeda 0113, 0121, and 0125); and,

-A portion of said scan lines and said data lines outside said intersections are formed in a second conducting layer (Maeda 0113, 0121, and 0125).

Reference Yumoto does not explicitly teach the formation of scan or data lines formed in a conducting layer at the intersections of such lines. Reference Maeda describes forming gate metal and scan lines, etc. simultaneously. As such, the scan lines would be formed everywhere not masked with a shadow mask, e.g. both in the scan lines and in the intersections. No matter what portions of the lines are claimed, any such configuration could be made using shadow masking and formed using either evaporation or sputtering. Any set of contacts could be created using correctly etched contact holes; electrically contiguous metal formed in the same layer is *prima facie* the same from an electrical and an engineering perspective. Further, forming scan lines or data lines or portions thereof (as claimed) in the same layer as other things would simply be making a component integral by eliminating unnecessary metal, and under *In re Larson*, 144 USPQ 347 (CCPA 1965), making a component integral is obvious and not patentable. Therefore, under either methodology, the recited limitations of the claim have been met.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single metal layer of Maeda since Maeda performs in one step what Yumoto does in several steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode goes down first and then the scan lines go down after the semiconductor layer, which clearly is a

different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

As to claim 39,

An electro-optical device according to claim 4, comprising electro-optical elements corresponding to intersections of scan lines and data lines (Yumoto, element OLED in various figures, such as 5, 8, 9, etc), wherein:

-A pair of electrodes is provided to supply power to electro-optical elements (Maeda Fig. 11C, elements 19 and 15 are opposing and pixel electrodes (see 0006-0008));

-At the intersections of said scan lines and said data lines, either said scan lines or said data lines are formed in a first conducting layer (Maeda 0113, 0118, 0121, 0125 – again, gate metal as discussed in rejections to claims 8-12);

-Portions of said scan lines and said data lines outside said intersections are formed in a second conducting layer (source metal layer, 0113, 0118, 0121, 0125 as discussed in rejections to claims 8-12); and,

-Said second conducting layer is positioned at a greater distance than said first conducting layer from one of said pair of electrodes (design choice issue, see Maeda Fig. 11C).

Reference Yumoto does not recite details of the fabrication process claimed above. Reference Maeda teaches the fabrication of such substrates and teaches contact holes (0044, 0047). Logically, such contact holes would fill on conducting layer deposition, thus meeting the recited limitation concerning intersections of data and scan lines. The positioning of a layer or its size is *prima facie* obvious and is not patentable

(*In re Japikse* for order of parts and further under *In re Reese*, anyone of ordinary skill in the art would know that there would be an optimal spacing of electrodes from each other to minimize cross-talk that would also occupy the minimum aspect ratio required on the shadow mask).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single metal layer of Maeda since Maeda performs in one step what Yumoto does in several steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode goes down first and then the scan lines go down after the semiconductor layer, which clearly is a different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

As to claim 40, reference Yumoto clearly teaches in [0098] that the first transistor (TFT1) is an n-channel type and that the second transistor (TFT3, but as noted in [0100-0101, particularly [0101], TFT4 has the same conductivity type as TFT3) has a p-channel, which are prima facie opposite polarities. Motivation and combination are taken from claim 39.

Claim 38 is rejected over Yumoto, Kim, and Maeda as applied to claim 37 above, and further in view of Tanaka.

As to claim 38,

The active matrix substrate according to claim 37, wherein said second conducting layer is positioned between said first conducting layer and said semiconductor layer.

Reference Yumoto does not explicitly teach this limitation. In Fig. 10B, Maeda shows that the bottom gate – element 56, which is metal (a niobium alloy) is put down first, then various insulating materials, then element 13 (source and drain electrodes) are formed on the same level and slightly covering the semiconductor layer 54. Under the doctrine of *In re Japikse*, switching the two layers would be *prima facie* obvious, and only minor alternations in the shadow masks for the process would be necessary (additive vs. subtractive processing in semiconductors, for example, switching the process would not be difficult for one of ordinary skill in the semiconductor / TFT art). Again, given that Maeda teaches many different embodiments (see Figs. 10-13, etc.), such a switch would be a design choice issue, and it would allow low-temperature processing of the substrate throughout the process, particularly allowing for newer techniques such as laser annealing and recrystallization of the semiconductor layer taught by Tanaka, and treatment of the semiconductor layer towards the end of processing.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the TFT circuits of Yumoto and Maeda with the laser annealing processing of polysilicon for TFT applications of Tanaka (see 0002-0015), as both Yumoto ([0011-0013]) and Maeda (0008, 0121, etc.) utilize polysilicon as the semiconductor material, and laser annealing is now a well-known, standard process in the art.

Claims 42-44 are rejected under 35 U.S.C. 103(a) as unpatentable over Yumoto as applied to claim 41 above, and further in view of Maeda (claim 4 operative here – any of the other claims would be subject to the same rejection).

As to claim 42,

The active matrix substrate according to claim 41, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yumoto Figure 3 and [0010] for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yumoto [0011], semiconductor thin film 4); and

-A gate metal layer comprising said second control terminal (Yumoto [0012]) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one scan line among said plurality of scan lines is formed in said gate metal layer (Maeda 0121).

References Yumoto teach all the limitations of this claim except the formation of a scan line in the gate metal layer. Reference Maeda teaches the formation of scan lines and gate electrodes in the same metal film layer for TFT / LCD monitor fabrication (e.g. 0162, 0121). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single metal layer of Maeda since Maeda performs in one step what Yumoto does in several steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode

goes down first and then the scan lines go down after the semiconductor layer, which clearly is a different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination, e.g. common sense is sufficient to justify the combination. See also *In re Karlson*, 136 USPQ 184 (CCPA 1963), for the doctrine that eliminating components is an obvious expedient – in this, eliminating fabrication steps.

As to claim 43,

The active matrix substrate according to claim 41, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yumoto Figure 3 and [0010] for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yumoto [0011], semiconductor thin film 4); and

-A gate metal layer comprising said second control terminal (Yumoto [0012]) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in said gate metal layer (Maeda 0121 and 0113 and 0125).

Reference Yumoto teaches all the limitations of this claim except the formation of a data line in the gate metal layer. Reference Maeda teaches the formation of data lines and source and drain electrodes in the same metal film layer for TFT / LCD monitor fabrication (e.g. 0113, 0125). It would be *prima facie* obvious to choose to form gate electrodes and data lines simultaneously rather than gate electrodes and scan

lines, for example. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single metal layer of Maeda since Maeda performs in one step what Yumoto does in several steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode goes down first and then the scan lines go down after the semiconductor layer, which clearly is a different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

As to claim 44,

The active matrix substrate according to claim 41, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yumoto Figure 3 and [0010] for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yumoto [0011], semiconductor thin film 4); and

-A gate metal layer comprising said second control terminal (Yumoto [0012]) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-A source metal layer comprising a source electrode or drain electrode connected to the source or drain of said second transistor (Maeda 0113, 0125); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in the layer (Maeda 0121 and 0113 and 0125), among said source metal layer and said gate metal layer, which is closer to said semiconductor layer.

Reference Maeda in combination with Yumoto teaches all the limitations of this claim, and this is merely a recitation of the dual limitations of claims 42 and 43 above. As such, the combination and motivation from claim 42 is used here and no further comment is necessary, as this claim is only a nominal variation of the parent.

Claim 45 is rejected under 35 U.S.C. 103(a) as unpatentable over Yumoto and Kim as applied to claim 41 above, and further in view of Gualandris. The rejection to claim 41 is herein incorporated by reference in its entirety.

Claim 45 is a substantial duplicate of claim 41, with the only difference being the addition of the limitation from claim 3:

Wherein at least said second active element is a transistor comprising a structure selected from the group consisting of an LDD structure, GDD structure, and DDD structure.

Yumoto teaches in [0113] to have the LDD structure in the active transistor, and it is discussed as being the active layer *per se*, that is on top of the gate oxide, so it would work for any transistor as specified there. However, Yumoto does not explicitly teach the use of GDD and DDD structures where Gualandris teaches DDD in 1:55-65, GDD in 2:25-30, and LDD in 2:25-30. Gualandris teaches that these are all methods of doping transistors, although one (the LDD) is preferred to work for 'ULSI' applications. Given that 'ULSI' applications at the time the patent was issued were mainly for deep sub-micron processes and that current TFT / liquid crystal display processes have much larger dimensions, e.g. still larger than one micron minimum channel length for silicon-

on-glass technology, these techniques would be perfectly valid for use in TFT / silicon-on-glass technology.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix substrates of Yumoto with the transistors of Gualandris, since Yamada uses transistors, which *prima facie* have a source and a drain and different drain doping techniques are well-known in the art, and Yumoto also teaches LDD mechanisms of doping, and the others would be obvious to a worker of ordinary skill in the art.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Woods whose telephone number is 571-272-7775. The examiner can normally be reached on M-F 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eric Woods April 5, 2006

Kee M. Tung
Primary Examiner

Notice of References Cited	Application/Control No. 10/299,861	Applicant(s)/Patent Under Reexamination MATSUEDA, YOJIRO	
	Examiner Eric Woods	Art Unit 2628	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2001/0019327	09-2001	Kim et al.	345/204
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
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	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/299,861	MATSUEDA, YOJIRO
Examiner	**Art Unit**
Eric Woods	2628

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
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Claim		Date
Final	Original	4/4/06
	1	√
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	4	√
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	11	–
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Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/299,861	MATSUEDA, YOJIRO	
	Examiner	Art Unit	
	Eric Woods	2628	

SEARCHED			
Class	Subclass	Date	Examiner
345	76-79,80-105	4/3/2006	EW

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST (USPT,USPGPUB,USOCR, DERWENT,EPO,JPO,IBM_TDB)--see attached search histories	4/3/2006	EW

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PATENT & TRADEMARK OFFICE

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2628

Application No.: 10/299,861

Examiner: E. WOODS

Filed: November 20, 2002

Docket No.: 114251

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection, Notice of Allowance, or other action that closes prosecution (e.g., Quayle Action), but before payment of the Issue Fee. Attached is our Check No. 179237 in the amount of $180.00 in payment of the fee under 37 CFR §1.17(p). Please credit or debit Deposit Account No. 15-0461 as needed to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached.

☒ a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

04/27/2006 SFELEKE1 00000101 10299861
01 FC:1806 180.00 OP

☒ 2. An English translation of the non-English language reference is attached hereto. See Reference 1.

Respectfully submitted,

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JAO:DJG/sqb

Date: April 26, 2006

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OIPE TAP40 APR 26 2006 PATENT & TRADEMARK OFFICE

Form PTO-1449 (REV. 1/06)	US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 114251	APPLICATION NO. 10/299,861
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT Yojiro MATSUEDA	
		FILING DATE November 20, 2002	GROUP 2628

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Name

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
	1	KR 1994-0009134	10/01/1994	Korea	X	X

OTHER DOCUMENTS

Examiner Initials	Cite No.	(Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: April 26, 2006

(19) Korean Intellectual Property Office (KR)
(12) Patent Publication (B1)

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(11) Publication Number:	1994-0009134
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(21) Application Number:	10-1992-0000101
(22) Application Date:	January 7, 1992
(73) Patentee:	Kim, Kwang-Ho Samsung Electronics Co., Ltd. 416, Maetan-dong, Gwonseon-gu, Suwon-shi, Gyonggi-do, Korea
(72) Inventor:	Bae, Byung-Seong # 110-205, Jugong Apt., Godeok-dong, Gangdong-gu, Seoul, Korea
(74) Agents:	Lee, Young-Pil; Choi, Deok-Yong

(54) Title: Liquid Crystal Flat Panel Display Device and Fabrication Method Thereof

ABSTRACT

The present invention relates to an active-matrix liquid crystal flat panel display device and a fabrication method thereof using thin-film transistor (TFT). In an arranged substrate in which a gate electrode line and a signal electrode line for transmitting a signal are separately formed by interposing an insulation film therebetween, and a thin-film transistor is formed adjacent to an intersection region of the gate electrode line and the signal electrode line, it is characterized in that the gate electrode line and the signal electrode line are formed on the same plane on an insulative substrate, or by penetrating into a predetermined depth below the surface of an insulative substrate. According to the present invention, a wiring resistance can be reduced without failure in the coverage in accordance with the height of a metal wiring.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a draw illustrating a prior art using a reverse stagger type TFT.

FIG. 2 is a draw illustrating a fabrication process according to a first embodiment of the

present invention.

FIG. 3 is a cross-sectional view illustrating a display substrate fabricated by a second embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention relates to an active matrix liquid crystal display using a thin film transistor (TFT), and more particularly, to a display substrate and a fabrication method thereof in which electrode lines and TFTs are formed.

An active matrix type liquid crystal display substrate using a TFT is being actively studied and developed due to providing a larger screen and higher definition compared to a simple passive matrix type display, and is a potential display device capable of realizing high-definition OA or high-vision displays in the future. As a TFT semiconductor material which has been used in this application, cadmium selenide (CdSe) was used in the early stage, and then amorphous silicon (a-Si), poly-crystal silicon (Poly-Si), or the like has been gradually used, and even in the structure of a TFT it has been diversified into a forward stagger type, a reverse stagger type, a co-planar type, and the like. A fabrication process of an active matrix type display substrate using a forward stagger TFT is disclosed in Japanese Laid-Open No. Sho 59 - 501562, but it is a recent trend that a reverse stagger type TFT capable of providing a better quality of TFT is widely used.

In general, a fabrication process of an active matrix display substrate using a reverse stagger type TFT is described below with reference to FIG. 1. FIG. 1a is a plan view illustrating a display substrate in which a reverse stagger type TFT is formed adjacent to an intersection of a gate electrode line 17 and a source electrode 18, and FIG. 1b is a cross-sectional view as seen through the line A-A' in FIG. 1a, and FIG. 1c is a cross-sectional view as seen through the line B-B' in FIG. 1a.

A gate electrode 12 and a gate electrode line 17 are patterned on a glass substrate 11 as ① in FIG. 1a, and a silicon nitride insulating layer 13 and an a-Si layer 14 are deposited and then patterned as ② in FIG. 1a to form a semiconductor layer 14. Subsequently, a metal film is deposited and then patterned as ③ in FIG. 1a to form a source electrode 15, a drain electrode 16, and a source electrode 18.

In the aforementioned fabrication method, a p-doped n^+ a-Si layer is typically formed to

make an ohmic contact between the source/drain electrodes 15 and 16 and the a-Si layer 14, and pixel electrodes made of ITO (Indium Tin Oxide) can be formed in an appropriate order according to the process condition.

For an active matrix type display substrate fabricated as described above, a method of forming a gate electrode line and a pixel electrode with the same mask for reducing the complexity of the process was invented by Japanese Takeda Etsuya, Kawaguchi Takao, and others, and disclosed in Korean Patent Publication No. 1990-0004732. However, the object of our concern is a problem of achieving the large screen size and high definition for a display portion.

In pursuit of the large screen size and high definition for a display portion, pixel density per unit area will be increased, and also the number of electrodes will be increased. Accordingly, the length of a electrode line will be increased, and as a result the wiring resistance will be increased significantly. In a RC circuit in which a pixel electrode acts as a capacitor, therefore, time constant will be increased, thereby resulting in an effect of delaying the propagation time of an image signal. This is against the request for a high definition, so it is a main cause that a lot of research and investment are currently being done in order to reduce the wiring resistance. The development of wiring materials having low resistance has been actively progressed to reduce the wiring resistance, and a great deal of research has been accomplished to improve a wiring structure.

In particular, for the wiring structure, in order to reduce the wiring resistance inversely proportional to the cross-sectional area of wire, it is typical of increasing the thickness of wiring. However, raising it more than a predetermined thickness will create a step height between the metal wiring and the substrate to a great extent, and the step coverage will be degraded at a step portion in the subsequent processes, thereby reducing the reliability and yield of a semiconductor device.

As illustrated in FIG. 1, in the prior art, a gate electrode line, a insulating layer, and a signal electrode line are formed with a vertically layered structure on the substrate, thereby causing a defect that the thickness of metal wiring is restricted to a certain extent in consideration of the step coverage in the subsequent processes.

Accordingly, it is an object of the invention to form metal wiring having greater than a predetermined thickness while not causing a step defect by metal wiring in order to reduce the wiring resistance of the signal electrode line and gate electrode line on a display substrate of a liquid crystal display formed with thin film transistors.

In order to achieve the foregoing object, a gate electrode line and a signal electrode line for transmitting a signal are separately formed by interposing an insulation film therebetween, and a thin-film transistor is formed adjacent to an intersection region of the gate electrode line and signal electrode line, wherein the gate electrode line and signal electrode line are formed on the same plane on an insulative substrate, or formed by penetrating into a predetermined depth below the surface of an insulative substrate.

Hereinafter, preferred embodiments 1 and 2 according to the principle of the invention will be described in detail with reference to the accompanying drawings.

[Embodiment 1]

According to an embodiment 1, a gate electrode line 12 and a source electrode line 13 are formed on the same plane on a glass substrate 11, thereby allowing to overcome a restriction on the thickness of metal wiring in the prior art in which the gate electrode line, the insulating layer, and the signal electrode line are formed with a vertically layered structure.

Hereinafter, a fabrication process according to an embodiment 1 is described below with reference to FIGS. 2a through 2e. Referring to FIG. 2a, a metal is formed with a predetermined thickness on the entire surface of a glass substrate 11 made of a vitreous insulating material by a method of physical vapor deposition, CVD, or the like, and then the gate electrode line 2 and the source electrode line 3 are patterned as illustrated in FIG 2a. At this time, the thickness of the first metal layer can be maintained at about 500 or less to improve the step coverage in the subsequent processes for a thin film transistor. Subsequently, an insulating layer 6 such as silicon nitrite, an a-Si:H (hydrogenated amorphous silicon) 4, and an n^+a-Si layer 4 are successively deposited on the entire surface of the substrate, and then patterned as illustrated in FIG. 2b to form a semiconductor film 4. At this time, the insulating layer 6 remains on the entire surface other than the semiconductor film 4.

Subsequently, as illustrated in FIG. 2c, the insulating layer 6 remaining inside a dotted region of the gate electrode line 2 and the source electrode line 3 is removed by etching.

Subsequently, a metal is deposited on the entire surface of the substrate, and a second metal layer 5 is patterned on the gate electrode line 2 and the source electrode line 3 as illustrated in FIG. 2d. At this time, the source electrode and drain electrode are formed together.

When the second metal layer is patterned on the gate electrode line 2 and the source electrode line 3, the connection or disconnection of an electrode line can be chosen in the

reverse manner at an intersection of electrode lines. That is, in case where the source electrode 3 is connected and the gate electrode line 2 is disconnected as illustrated in FIG. 2a, the gate electrode line should be connected and the source electrode line should be disconnected as illustrated in FIG. 2d by changing a pattern of the second metal layer 5. The thickness of the second metal layer can be sufficiently increased in consideration of the wiring resistance of metal wire in a different way from the first metal layer.

FIG. 2e is a cross-sectional view as seen through the line of A- A' in FIG. 2d.

[Embodiment 2]

According to an embodiment 2, the gate electrode line 22 and the source electrode line 23 are formed by penetrating into a predetermined depth below the surface of a vitreous insulating substrate 21 as illustrated in FIG. 3, thereby providing a potential means to overcome a restriction on the thickness of metal wiring in the prior art.

A method of forming planarized metal wiring into a glass substrate is described in detail in Korean Patent Application No. 1991-10069 entitled "Method of Fabricating Metal Wiring" by the inventor of this invention as a representative.

The previously filed invention is a method of fabricating metal wiring comprising: a first process of forming a photoresist pattern on a glass substrate, a second process of removing the glass substrates exposed through the photoresist pattern at a predetermined thickness to form an opening portion, a third process of coating a metal layer on the entire surface having the above structure to fill the opening portion of the glass substrate, and a fourth process of removing the metal layer and the photoresist pattern other than the opening portion having the above structure.

Accordingly, according to an embodiment 2, a fabrication method of the previously filed Korean Patent Application No. 1991-10069 will be applied, thereby allowing to form the gate electrode line 22 and the signal electrode line 23 by penetrating into a predetermined depth below the surface of the glass substrate 21, and the subsequent process will be performed by a fabrication method as described in the embodiment 1.

As a result, according to an embodiment 2, a restriction on the thickness of metal wiring can be further relieved by the depth of penetrated metal wiring.

According to the foregoing fabrication process, first metal layers 22 and 23 are formed by penetrating into a glass substrates at a predetermined depth, and then an anodized film is formed on the first metal layers, and then the surface of the glass substrate is planarized,

thereby reducing the leakage current of an insulating layer in the subsequent process.

As described above, embodiments 1 and 2 in an active matrix type liquid crystal display substrate becoming a large size and high definition, as an invention in which electrode lines are formed on the same plane to reduce the wiring resistance of metal wiring, thin film transistors can be applied on an insulative substrate in a wide range to reduce the wiring resistance down to a desired level.

(57) What is claimed is:

1. A liquid crystal flat panel display device in which a gate electrode line and a signal electrode line for transmitting a signal are separately formed by interposing an insulation film therebetween, and a thin-film transistor is formed adjacent to an intersection region of the gate electrode line and signal electrode line, wherein the gate electrode line and signal electrode line are formed on the same plane on an insulative substrate.

2. The liquid crystal flat panel display device according to claim 1, wherein the thin-film transistor is a reverse stagger type.

3. The liquid crystal flat panel display device according to claim 1, wherein the gate electrode line and signal electrode line are formed by interposing an insulating film therebetween in a layered structure at the intersection of the gate electrode line and signal electrode line.

4. A liquid crystal flat panel display device in which a gate electrode line and a signal electrode line for transmitting a signal are separately formed by interposing an insulation film therebetween, and a thin-film transistor is formed adjacent to an intersection region of the gate electrode line and signal electrode line, wherein the gate electrode line and signal electrode line are formed by penetrating into a predetermined length below the surface of an insulative substrate.

5. The liquid crystal flat panel display device according to claim 4, wherein the gate electrode line and signal electrode line are formed by interposing an insulating film therebetween in a layered structure at the intersection of the gate electrode line and signal electrode line.

6. The liquid crystal flat panel display device according to claim 4, wherein the thin-film transistor is a reverse stagger type.

7. The liquid crystal flat panel display device according to claim 4, wherein an anodized film is formed between a surface of the gate electrode line and signal electrode line penetrated

below the surface of an insulative substrate and the insulation film.

8. A fabrication method of a liquid crystal flat panel display device in which a gate electrode line and a signal electrode line are separately formed by interposing an insulation film therebetween, and a thin-film transistor is formed adjacent to an intersection region of the gate electrode line and signal electrode line, comprising the steps of:

a first process of patterning the gate electrode line and signal electrode line on the same plane of an insulative substrate so as not to contact to each other;

a second process of depositing an insulation film and a semiconductor film on the substrate, and then patterning the semiconductor layer;

a third process of removing part of the insulation film on a surface of the gate electrode line and signal electrode line; and

a fourth process of patterning a second metal layer on the gate electrode line and signal electrode line so as not to contact to each other.

9. The fabrication method of a liquid crystal flat panel display device according to claim 8, wherein a pattern type at the intersection of the electrode lines in the fourth process is reversed to a pattern type in the first process so as not to disconnect the gate electrode line and signal electrode line.

10. The fabrication method of a liquid crystal flat panel display device according to claim 8, wherein the gate electrode line and signal electrode line in the first process are formed with the thickness of about 500 Å or below.

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심사청구 : 있음

(54) 액정평판 표시장치와 그 제조방법

요약

본 발명은 박막트랜지스터(TFT)를 사용한 액티브 매트릭스형 액정표시기판과 그 제조방법에 관한 것으로써, 게이트전극과 신호를 전달하는 신호전극선이 절연막을 사이에 두고 분리형성되어 있으며, 상기 게이트 전극선과 신호전극선의 교차지역 부근에 박막트랜지스터가 형성되어 있는 배열기판에 있어서, 상기 게이트전극선과 신호전극선을 절연성기판상의 동일평면상에 형성시켜 주거나, 절연성기판 표면아래로 소정의 깊이 만큼 침입시켜 형성시켜 주는 것을 특징으로 한다. 따라서 본 발명에 의하면 금속배선의 높이에 따른 피복성의 불량없이 배선저항을 낮출 수 있다.

대표도

도1

명세서

[발명의 명칭]

액정평판 표시장치와 그 제조방법

[도면의 간단한 설명]

제1도는 역스태거형 TFT를 사용한 종래 기술을 나타낸 도면, 제2도는 본 발명의 실시예 1의 제조공정을 설명하기 위한 도면, 제3도는 본 발명의 실시예 2에 의해 제조된 표시기판의 단면도.

본 내용은 요부공개 건이므로 전문내용을 수록하지 않았음

(57) 청구의 범위

청구항 1

게이트전극선과 신호를 전달하는 신호전극선이 절연막을 사이에 두고 분리 형성되어 있으며, 상기 게이트전극선과 신호전극선의 교차지역부근에 박막트랜지스터가 형성되어 있는 액정평판 표시장치에 있어서, 상기 게이트전극선과 신호전극선이절연성 기판상의 동일 평면상에 형성되어 있는 것을 특징으로 하는 액정평판 표시장치.

청구항 2

제1항에 있어서, 상기 박막트랜지스터는 역스태거형인 것을 특징으로 하는 액정평판 표시장치.

청구항 3

제1항에 있어서, 상기 게이트전극선과 신호전극선의 교차부에 있어서는 게이트전극선과 신호전극선이 절연막을 사이에 두고 적층구조로 형성되어 있는 것을 특징으로 하는 액정평판 표시장치.

청구항 4

게이트전극선과 신호를 전달하는 신호전극선이 절연막을 사이에 두고 분리 형성되어 있으며, 상기 게이트전극선과 신호전극선의 교차지역부근에 박막트랜지스터가 형성되어 있는 액정평판 표시장치에 있어서, 상기 게이트전극선과 신호전극선이절연성기판 표면아래로 소정의 길이만큼 침입되어 형성되어 있는 것을 특징으로 하는 액정평판 표시장치.

청구항 5

제4항에 있어서, 상기 게이트전극선과 신호전극선의 교차부에 있어서는 게이트전극선과 신호전극선이 절연막을 사이에 두고 적층구조로 형성되어 있는 것을 특징으로 하는 액정평판 표시장치.

청구항 6

제4항에 있어서, 상기 박막트랜지스터는 역스태거형인 것을 특징으로 하는 액정평판 표시장치.

청구항 7

제4항에 있어서, 상기 절연성기판 표면 아래를 침입되어 있는 게이트전극선, 신호전극선, 표면과 상기 절연막 사이에 양극 산화막이 형성되어 있는 것을 특징으로 하는 액정평판 표시장치.

청구항 8

게이트전극선과 신호전극선이 절연막을 사이에 두고 분리형성되어 있으며, 상기 게이트전극선과 신호전극선의 교차지역부근에 박막트랜지스터가 형성되어 있는 액정평판 표시장치의 제조방법에 있어서, 상기 게이트전극선과 신호전극선을 절연기판상의 동일 평면상에 서로 접촉되지 않게 패턴형성시키는 제1공정과, 상기 기판상에 절연막, 반도체막을 증착시킨후 반도체층을 패턴 형성시키는 제2공정과, 상기 게이트전극선, 신호전극선 표면의 절연막을 일부 제거시키는 제3공정과,상기 게이트전극선, 신호전극선상에 제2금속층은 서로 접촉되지 않게 패턴형성시키는 제4공정은 구비하여 이루어진 것을특징으로 하는 액정평판 표시장치의 제조방법.

청구항 9

제8항에 있어서, 상기 제4공정에 있어서 전극선의 교차부에서의 패턴형태는 상기 제1공정에서의 패턴형태와 반대로 하여게이트전극선, 신호전극선이 단절되지 않도록 형성시키는 것을 특징으로 하는 액정평판 표시장치의 제조방법.

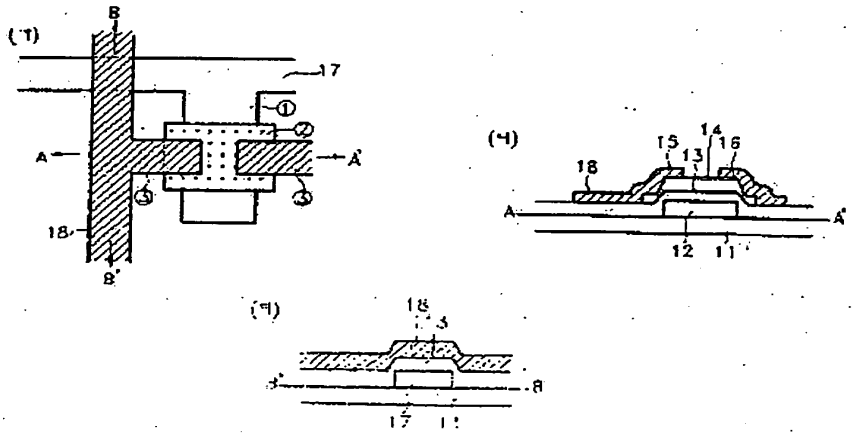
청구항 10

제8항에 있어서, 상기 제1공정에서의 게이트전극선, 신호전극선의 두께는 500Å정도나 그 이하로 형성시키는 것을 특징으로 하는 액정평판 표시장치의 제조방법.

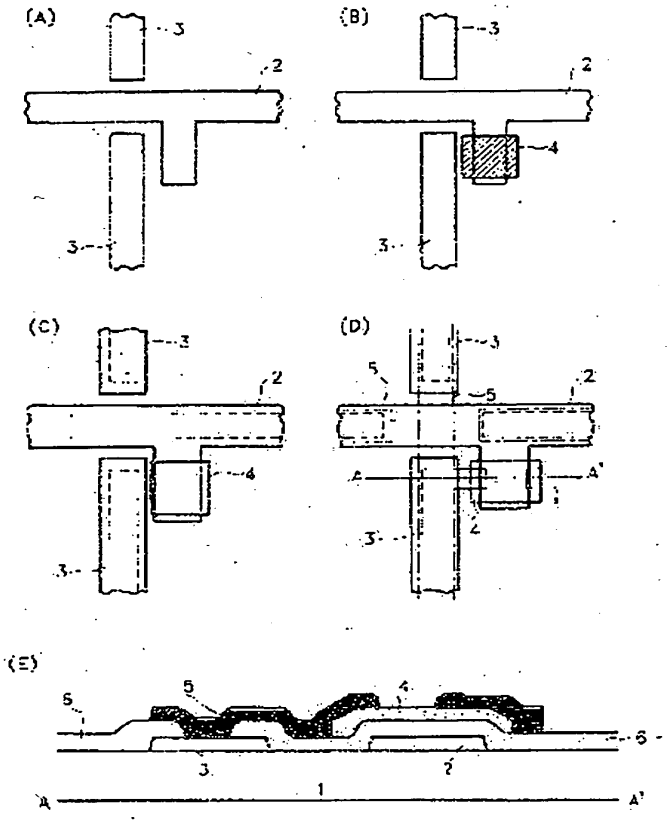
※ 참고사항 : 최초출원 내용에 의하여 공개하는 것임.

도면

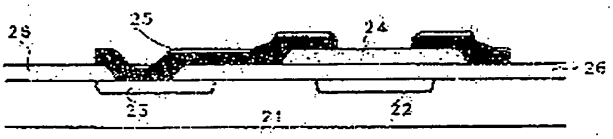
도면1



도면2



도면3



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PATENT APPLICATION

RESPONSE UNDER 37 CFR §1.116
EXPEDITED PROCEDURE
TECHNOLOGY CENTER ART UNIT 2628

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2628

Application No.: 10/299,861

Examiner: E. WOODS

Filed: November 20, 2002

Docket No.: 114251

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE

AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR §1.116

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the April 12, 2006 Office Action, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1-7. (Canceled)

8. (Currently Amended) The ~~active matrix substrate~~electro-optical device according to ~~claim 4,~~claim 46, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed; and

a gate metal layer comprising said second control terminal, and

wherein at least a portion of said plurality of scan lines is formed in said gate metal layer.

9. (Currently Amended) The ~~active matrix substrate~~electro-optical device according to ~~claim 4,~~claim 46, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed; and

a gate metal layer comprising said second control terminal; and

wherein at least a portion of one data line among said plurality of data lines is formed in said gate metal layer.

10. (Currently Amended) The ~~active matrix substrate~~electro-optical device according to ~~claim 4,~~claim 46, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed;

a gate metal layer comprising said second control terminal; and

a source metal layer comprising a source electrode or drain electrode connected to the source or drain of said second transistor;

wherein at least one portion of at least one data line among said plurality of data lines is formed in the layer, among said source metal layer and said gate metal layer, that is closer to said semiconductor layer.

11-36. (Canceled)

37. (Currently Amended) The ~~active matrix substrate~~electro-optical device in accordance with ~~claim 4,~~claim 46, comprising unit circuits comprising transistors, arranged corresponding to intersections of data lines and scan lines; wherein

a semiconductor film constituting said transistors is formed in a semiconductor layer;

either said scan lines or said data lines are formed in a first conducting layer at the intersections of said scan lines and said data lines; and

a portion of said scan lines and said data lines outside said intersections are formed in a second conducting layer.

38. (Currently Amended) The ~~active matrix substrate~~electro-optical device according to claim 37, wherein said second conducting layer is positioned between said first conducting layer and said semiconductor layer.

39. (Currently Amended) The electro-optical device according to ~~claim 4,~~claim 46, comprising electro-optical elements corresponding to intersections of scan lines and data lines, wherein:

a pair of electrodes is provided to supply power to said electro-optical elements;

at the intersections of said scan lines and said data lines, either said scan lines or said data lines are formed in a first conducting layer;

portions of said scan lines and said data lines outside said intersections are formed in a second conducting layer; and

said second conducting layer is positioned at a greater distance than said first conducting layer from one of said pair of electrodes.

40-45. (Canceled)

46. (New) An electro-optical device comprising:

a plurality of data lines;

a plurality of scan lines;

a plurality of unit circuits arranged corresponding to intersections of the plurality of data lines and the plurality of scan lines, each of the unit circuits including:

a first transistor;

an electroluminescence element being connected in series to one of a source and a drain of the first transistor;

a second transistor arranged between a gate of the first transistor and one of the source and the drain of the first transistor, the second transistor having a structure to prevent leakage currents during shutoff, and the polarity of the second transistor being opposite to the polarity of the first transistor; and

a holding element coupled to the gate of the first transistor, the holding element holding a control voltage, the first transistor supplying a current based on the control voltage to the electroluminescence element.

47. (New) The electro-optical device according to claim 46, wherein the second transistor is configured as a multi-gate transistor.

48. (New) The electro-optical device according to claim 46, wherein the second transistor has a structure selected from the group consisting of an LDD structure, a GDD structure, and a DDD structure.

49. (New) The electro-optical device according to claim 46, wherein the second transistor is arranged between the gate of the first transistor and one of the source and the drain of the first transistor which is coupled to the electroluminescence element.

50. (New) The electro-optical device according to claim 46, wherein the first transistor has a p-type polarity.

51. (New) The electro-optical device according to claim 46, each of the unit circuits including a third transistor coupled in series to the first and the second transistor, a gate of the second transistor and a gate of the third transistor being connected to a same corresponding scan line.

52. (New) The electro-optical device according to claim 46, each of the unit circuits including a fourth transistor coupled in series to the first transistor, the fourth transistor supplying the current to the electroluminescence element during a light emission period.

53. (New) The electro-optical device according to claim 46, further comprising a plurality of power supply lines, one electrode of the holding element is connected to a corresponding power supply line of the plurality of power supply lines, or the one electrode of the holding element is a portion of the corresponding power supply line of the plurality of power supply lines.

REMARKS

Claims 8-10, 37-39 and 46-53 are pending in this application. By this amendment, claims 8-10 and 37-39 are amended. Claims 1-5, 14-33 and 40-45 are canceled without prejudice or disclaimer of the subject matter found therein. Claims 46-53 are added. No new matter has been added.

Entry of the amendments is proper under 37 CFR §1.116 since the amendments: (a) place the application in condition for allowance for the reasons discussed herein; (b) do not raise any new issue requiring further search and/or consideration as the amendments amplify issues previously discussed throughout prosecution; (c) do not present any additional claims without canceling a corresponding number of finally rejected claims; and (d) place the application in better form for appeal, should an appeal be necessary. The amendments are necessary and were not earlier presented because they are made in response to arguments raised in the final rejection. Entry of the amendments is thus respectfully requested.

I. Response to Arguments

On page 2 of the Office Action, the Office Action states that Applicant has not contested Examiner's statement in the Office Action of October 13, 2005 on page 6 that claim 1 is merely a broader version of claim 4, and that the claims stand and fall together. Applicant respectfully traverses the Office Action's grouping of the claims. Furthermore, in view of the cancellation of claims 1 and 6, the Office Action's grouping is moot.

II. Priority

On page 2, the Office Action requests that Applicant specify which of claims 1-15 and 37-45 correspond to the three Japanese applications from which priority has been claimed. Applicant respectfully points that there is no requirement that translations be provided to the Patent Office unless Applicant is attempting to overcome the date of an applied reference. Because this is not the case in the present application, Applicant is neither required to provide

translation nor is Applicant required to specify any particular date of priority. In sum, the claimed invention is entitled to the priority dates for each application indicated on the declaration and the subject matter contained therein.

III. Election/Restrictions

On page 3, the Office Action indicates that claims 16-33 were withdrawn from consideration and must be canceled if the case were to pass to issue.

In view of this Amendment, the claims have been canceled. Therefore, this issue is moot.

IV. Definitions

On page 3, the Office Action states that the term "electroluminescence element" will be taken to mean, as per the specification page 1 and the previous interviews with Applicant's representative, to include LED's and organic light-emitting diodes (OLEDs) among other things. Applicant respectfully traverses the definition assigned to the term "electroluminescence elements" by the Office Action.

Applicant respectfully points out that the invention is entitled to the definition as defined by the specification and any equivalent thereof. The invention is not limited by the definition which the Office Action has allegedly defined.

V. Claim Rejections Under 35 U.S.C. §112

On page 3, claim 15 was rejected under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim this subject matter which Applicant regards as the invention.

In view of the cancellation of claim 15, this rejection is moot. Withdrawal of the rejection is requested.

VI. Claim Rejection Under 35 U.S.C. §103

On pages 4-12, the Office Action rejected claims 1, 2, 4, 15 and 41 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Publication No. 2004/0207615 to Yumoto et al. (hereinafter "Yumoto"). On pages 12-14, the Office Action rejected claims 3 and 5 under 35 U.S.C. §103(a) as being unpatentable over Yumoto as applied to claim 1 and further in view of Gualandris. On pages 14-20, the Office Action rejected claims 8-10 and 37-44 under 35 U.S.C. §103(a) as being unpatentable over Yumoto as applied to claim 4 and further in view of Maeda. On pages 20 and 21, the Office Action rejected claim 38, presumably as being unpatentable under 35 U.S.C. §103(a), over Yumoto and Maeda as applied to claim 37 and further in view of Tanaka.[1] On pages 21-24, the Office Action rejected claims 42-44 under 35 U.S.C. §103(a) as being unpatentable over Yumoto as applied to claim 41 and further in view of Maeda. On pages 24-25, the Office Action rejected claim 45 under 35 U.S.C. §103(a) as being unpatentable over Yumoto as applied to claim 41 and further in view of Gualandris. On pages 26-36, the Office Action rejected claims 1, 2, 4, 15 and 41 under 35 U.S.C. §103(a) as being unpatentable over Yumoto in view of U.S. Patent Application Publication No. 2001/0019327 to Kim. On pages 36-42, the Office Action rejected claims 8-10 and 37-44 under 35 U.S.C. §103(a) as being unpatentable over Yumoto and Kim as applied to claim 4 and further in view of Maeda. On pages 42-43, the Office Action rejected claim 38 under 35 U.S.C. §103(a) as being unpatentable over Yumoto, Kim and Maeda as applied to claim 37 and further in view of Tanaka. On pages 44-47, the Office Action rejected claims 42-44 under 35 U.S.C. §103(a) as being unpatentable over Yumoto as applied to claim 41 and further in view of Maeda. On page 47-48, the Office Action rejected claim

[1] If the rejection of claim 38 on pages 20-21 is not a rejection as being unpatentable under 35 U.S.C. §103(a), Applicant requests clarification of the nature of this rejection.

45 under 35 U.S.C. §103(a) as being unpatentable over Yumoto and Kim as applied to claim 41 and further in view of Gualandris. These rejections are respectfully traversed.

The rejection of claims 1-5, 8-10, 14, 15 and 37-45 over the above identified applied references is moot in view of the cancellation of claims 1-5, 14, 15 and 40-45 in view of the amendment of claims 8-10 and 37-39.

New claim 46 recites, among other features, "a second transistor arranged between a gate of the first transistor and one of the source and the drain of the first transistor, the second transistor having a structure to prevent leakage currents during shutoff, and the polarity of the second transistor being opposite to the polarity of the first transistor."

Therefore, according to the invention in comparison to the Yumoto reference, the second transistor (TFT2), which has a structure to prevent leakage current during shutoff, is arranged between the gate of the first transistor (drive transistor TFT1) and either the source or the drain of the first transistor, as illustrated in Fig. 5. Another feature of the invention is that the first and second transistors have polarities that are opposite each other.

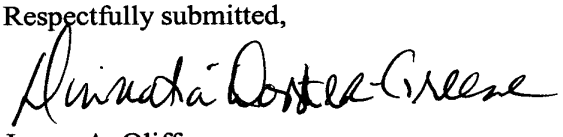
In Yumoto, there is no disclosure or suggestion that TFT4 in Figs. 9 and 11 should have a structure to prevent leakage current during shutoff. Although the Office Action states that it is obvious that the double-gate structure in Fig. 8 is applied to the circuit in Fig. 9 or 11, the double-gate transistor in Fig. 8 is not connected between a gate and source (drain) of a driving transistor. Thus, no suggestion is made in Yumoto that a control transistor connected between a gate and a source (drain) of a drive transistor should have a structure to prevent leakage current. Accordingly, there is no motivation to combine the double-gate transistor in Fig. 8 with the circuits in Figs. 9 and 11.

Claims 8-10, 37-39 and 47-49 are allowable based at least on their dependence from independent claim 46 for the reasons stated above in connection with independent claim 46.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 8-10, 37-39 and 46-53 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

Dinnatia J. Doster-Greene
Registration No. 45,268

JAO:DJG/gck

Date: July 12, 2006

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

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EFS ID:	1110448
Application Number:	10299861
Confirmation Number:	5800
Title of Invention:	Active matrix substrate, electro-optical device, and electronic device
First Named Inventor:	Yojiro Matsueda
Customer Number:	25944
Filer:	Eric Dean Morehouse/Cyndi Racine
Filer Authorized By:	Eric Dean Morehouse
Attorney Docket Number:	114251
Receipt Date:	12-JUL-2006
Filing Date:	20-NOV-2002
Time Stamp:	15:58:15
Application Type:	Utility
International Application Number:	

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part	Pages
1		114251AAFR_07-12-06.pdf	360293	yes	10

	Multipart Description		
	Doc Desc	**Start**	**End**
	Amendment After Final	1	1
	Claims	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	10
Warnings:			
Information:			
	Total Files Size (in bytes):	360293	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

PTO/SB/06 (12-04)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

Application or Docket Number: 10/279861

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))							
SEARCH FEE (37 CFR 1.16(k), (i), or (m))							
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 = *	*	X =		OR	X =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 = *	*	X =			X =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

7-13-06

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 13	Minus	** 37	= 0	X =		OR	X =	
Independent (37 CFR 1.16(h))	* 1	Minus	*** 12	=	X =		OR	X =	
Application Size Fee (37 CFR 1.16(s))							OR		
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/299,861	11/20/2002	Yojiro Matsueda	114251	5800

25944 7590 07/31/2006

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
WOODS, ERIC V	
ART UNIT	**PAPER NUMBER**
2628	

DATE MAILED: 07/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Advisory Action Before the Filing of an Appeal Brief	Application No.	Applicant(s)	
	10/299,861	MATSUEDA, YOJIRO	
	Examiner	Art Unit	
	Eric Woods	2628	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 12 July 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☒ They raise the issue of new matter (see NOTE below);
   (c) ☒ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: *See Continuation Sheet.* (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-5, 8-10, 14, 15, and 37-45*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.
12. ☒ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☐ Other: _____.

ULKA CHAUHAN
SUPERVISORY PATENT EXAM

Continuation of 3. NOTE: Firstly, the amendments cancel all independent claims and replace them with new sets of claims, which would clearly require a new search and raises new issues. As an example, the introduction of a transistor having a different polarity is a new object that was never in the canceled claims. Examiner does not find a specific example of the this structure in the originally filed claims, and applicant did not clearly point out support. Next, this cancellation does *not* materially reduce or simplify the claims for appeal, because the new claims are both broader and more narrow than the old ones. As such, entry of the amendment would *not* be proper..

OIPE 1A213
APR 07 2006
PATENT & TRADEMARK OFFICE

Form PTO-1449 (REV. 1/06) US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 114251	APPLICATION NO. 10/299,861
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANT Yojiro MATSUEDA	
	FILING DATE November 20, 2002	GROUP 2672

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Name
EW	1	6,794,675	09/21/2004	Koji SUZUKI et al.

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
	1	KR 2001-0014528 A (Corresponds to U.S. 6,794,675)	02/26/2001	Korea		

OTHER DOCUMENTS

Examiner Initials	Cite No.	(Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	/Eric Woods/ (07/17/2006)	DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: April 7, 2006

OIPE TAP40 APR 26 2006 PATENT & TRADEMARK OFFICE

Form PTO-1449 (REV. 1/06)	US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 114251	APPLICATION NO. 10/299,861
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT Yojiro MATSUEDA	
		FILING DATE November 20, 2002	GROUP 2628

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Name

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
EW	1	KR 1994-0009134	10/01/1994	Korea	X	X

OTHER DOCUMENTS

Examiner Initials	Cite No.	(Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	/Eric Woods/ (07/17/2006)	DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: April 26, 2006

DO NOT ENTER
EW 7/17/06

PATENT APPLICATION

RESPONSE UNDER 37 CFR §1.116
EXPEDITED PROCEDURE
TECHNOLOGY CENTER ART UNIT 2628

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2628

Application No.: 10/299,861

Examiner: E. WOODS

Filed: November 20, 2002

Docket No.: 114251

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE

AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR §1.116

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the April 12, 2006 Office Action, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

AUG 11 2006
PATENT & TRADEMARK OFFICE

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2628

Application No.: 10/299,861

Examiner: E. WOODS

Filed: November 20, 2002

Docket No.: 114251

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE

MAIL STOP RCE

LARGE ENTITY REQUEST FOR CONTINUED EXAMINATION UNDER 37 C.F.R. §1.114

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. §1.114, Applicant(s) hereby request(s) continued examination.

☒ Applicant further requests entry and consideration of the submission filed July 12, 2006.

The above-identified application was filed on or after June 8, 1995. Thus, entry is proper under 37 C.F.R. §1.114(d).

Attached hereto is our check no. 183010 in the amount of ☒ $790.00 as payment of the fees set forth in 37 C.F.R. §1.17(e). The Commissioner is hereby authorized to charge any additional fees or credit any overpayment associated with this communication to Deposit Account No. 15-0461. Two duplicate copies of this page are enclosed.

Respectfully submitted,

Dinnatia Doster-Greene

James A. Oliff
Registration No. 27,075

Dinnatia J. Doster-Greene
Registration No. 45,268

JAO:DJG/sqb

Date: August 11, 2006

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461



PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Date August 11, 2006

In re the Application of

Yojiro MATSUEDA	Group Art Unit: 2628
Application No.: 10/299,861	Examiner: E. WOODS
Filed: November 20, 2002	Docket No.: 114251

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE

LARGE ENTITY PETITION FOR 1st - 3rd EXTENSION OF TIME UNDER 37 C.F.R. §1.136(a) AND TRANSMITTAL OF FEE UNDER 37 C.F.R. §1.17

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is a response to the outstanding Official Action in the above-identified patent application. The shortened statutory period having expired July 12, 2006, an extension of time for a period of one (1) month is hereby requested. Attached hereto is our Check No. 183011 in the amount of $120.00 in payment for:

X	Extension fee for response within first month pursuant to §1.136(a) ($120.00)
	Extension fee for response within second month pursuant to §1.136(a) ($450.00)
	Extension fee for response within third or subsequent month pursuant to §1.136(a) ($1020.00)

The Commissioner is hereby authorized to charge any additional fee or credit any overpayment associated with this communication to Deposit Account No. 15-0461. Two copies of this petition are enclosed.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Dinnatia J. Doster-Greene
Registration No. 45,268

JAO:DJG/sqb

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

PTO/SB/06 (12-04)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-876

Application or Docket Number: 10/299861

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))							
SEARCH FEE (37 CFR 1.16(k), (l), or (m))							
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 = *	*	x =		OR	x =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 = *	*	x =			x =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
			TOTAL			TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

7-13-05

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 13	Minus	** 37	= 0	x =		OR	x =	
Independent (37 CFR 1.16(h))	* 1	Minus	*** 12	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

8/11/05

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 14	Minus	** 37	= 1	x =		OR	x =	
Independent (37 CFR 1.16(h))	* 1	Minus	*** 12	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S71	2030	(345/76 345/77 345/78 345/79).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/19 18:06
S72	14867	(345/8? 345/9? 345/100 345/101 345/102 345/103 345/104 345/105).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/19 18:06
S73	2030	(345/76 345/77 345/78 345/79).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/19 18:06
S74	14867	(345/8? 345/9? 345/100 345/101 345/102 345/103 345/104 345/105).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/19 18:06
S75	2	"20020067323".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/19 18:06
S76	304	drive near transistor with polarit$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 09:33
S77	147	driver near transistor with (polarity polarities)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:31
S78	38	S77 with (opposite different)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:32
S79	0	S78 and pixel	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:32

EAST Search History

S80	18	S77 and pixel	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 13:30
S81	2	"6092107".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 13:55
S82	4	Steele.in. and SVG	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 14:24
S83	1	Itoh.in. and SVG and VRML	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 13:56
S84	675	driv$3 near transistor with polarity	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 14:24
S85	43688	("n type" n-type) same ("p type" p-type) same transistor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 14:24
S86	91	S84 and pixel	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 14:24
S87	35	S84 same pixel	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 14:24
S88	40	(opposite different other) near (polarity type) and S86	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 14:25

EAST Search History

S89	314	(opposite different other) near (polarity type) and S84	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 14:25
S90	91	S86 and S86	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 14:25
S91	37	S89 and S85	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 14:25
S92	13	S88 and S85	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 14:25

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/299,861	11/20/2002	Yojiro Matsueda	114251	5800

25944 7590 09/29/2006

OLIFF & BERRIDGE, PLC
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EXAMINER	
WOODS, ERIC V	

ART UNIT	PAPER NUMBER
2628	

DATE MAILED: 09/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/299,861	MATSUEDA, YOJIRO	
	Examiner	Art Unit	
	Eric Woods	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-10,37-39 and 46-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-10,37-39 and 46-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/11/2006 has been entered.

Response to Arguments

Applicant has canceled claims 1-5, 14-33, and 40-45. Therefore, since all the grounds of rejection against the remaining claims were based on canceled independent claims, the remaining grounds of rejection are vacated.

Claims 46-53 have been added

Applicant's arguments, see Remarks pages 1-5 and claim amendments, filed 7/12/2006, with respect to the rejection(s) of claim(s) 1-15 and 37-45 under 35 USC 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn as above. However, upon further consideration, a new ground(s) of rejection is made in view of various references as below.

Examiner duly notes applicant's statements with respect to priority and notes that the request for clarification of priority dates was only a request and was in no manner, shape, or form a requirement.

Examiner thanks applicant for canceling the non-elected claims.

Examiner's definition of the term "electroluminescent element" was only to point out illustrative embodiments that the current claims have focused upon in order to clarify the issue with respect to the prior art only and was meant to be inclusive rather than exclusive.

The rejection of claim 15 under 35 USC 112, second paragraph, stands withdrawn in view of applicant's amendments.

As noted above, the rejection of claims 8-10 and 37-39 under 35 USC 103(a) stands withdrawn in view of the claim amendments.

With respect to the newly added claims, examiner has provided numerous references to show that the state of the art at the time the invention was made would have led a PHOSITA to utilize multi-gate structures because they were known to minimize leakage, which lowers overall system power consumption and increases efficiencies.

Claim Objections

Claim 52 is objected to because of the following informalities: it recites a fourth transistor without ever reciting a third transistor in any of the claims in the dependency chain. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 10 stands rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 recites the limitation "said active matrix substrate" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 51 is rejected as not clearly describing the metes and bounds of the claim. It is unclear how such a third transistor is to be "coupled in series" to a first and second transistor when these transistors are themselves not necessarily directly connected. It is unclear how the claim should be read.

The following is a quotation of the fourth paragraph of 35 U.S.C. 112:

> Subject to the following paragraph, a claim in dependent form shall contain a reference to a claim previously set forth and then specify a further limitation of the subject matter claimed. A claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers.

Claim 49 is rejected under 35 U.S.C. 112, fourth paragraph, as failing to further limit the subject matter of the parent claim. See CAFC 06-1179, *Pfizer Inc. v. Ranbaxy Labs Ltd.* (79 USPQ2d 1583).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 46 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Knapp et al (US 6,373,454 B1) in view of Yumoto (US PGPub 2004/0207615 A1).

As to claim 46,

An electro-optical device comprising:

-A plurality of data lines; (Knapp Figure 1, column, data, driver circuit 18 with data lines 14, 5:24-38)

-A plurality of scan lines; (Knapp Figure 1, row scanning driving circuit 16 and row scan lines 12, 5:24-38)

-A plurality of unit circuits arranged corresponding to intersections of the plurality of data lines and the plurality of scan lines, each of the unit circuits including: (Knapp has pixels 10 that are regularly spaced and the like, as shown in Figure 1, 5:24-38.)

-A first transistor; (Knapp Figure 3, element 30, first transistor being a n-channel device, 7:25-48)

-An electroluminescence element being connected in series to one of a source and a drain of the first transistor; (Knapp Figure 3, display element 20, comprising an OLED – 5:40-55, 6:10-15, connected in series to one of the source or drain of transistor 30.

The claim is written using comprising language, which is open-ended and allows there to be elements (e.g. other transistors) between the source / drain of the first transistor and the OLED element itself)

-An second transistor arranged between a gate of the first transistor and one of the source and the drain of the first transistor, the second transistor having a structure to prevent leakage currents during shutoff, and the polarity of the second transistor being opposite to the polarity of the first transistor; and (Knapp Figure 3, transistor 33 is arranged between the gate of transistor 30 and the source / drain of transistor 30 through a contiguous path via conducting line 12 and transistor 32. Applicant used a different term – "arranged" instead of "connected" which would reasonably be construed as only requiring a contiguous path rather than a per se connection. As such, "arranged" is very broad and the path pointed out by examiner would be "arranged")(Yumoto clearly shows in Figure 8 multi-gate elements that are used to block leakage – e.g. TFT4a/b and TFT2a/b [0073], where these are used to suppress the leakage current with the double gate structure.)

-A holding element coupled to the gate of the first transistor, the holding element holding a control voltage, the first transistor supplying a current based on the control voltage to the electroluminescence element. (Knapp Figure 3, holding element 38, described in 7:25-8:10, where clearly it is connected to the gate of the first transistor, and transistor 30 is the drive transistor for the circuit – 2:20-35, 3:5-17, 6:20-35, etc)

Knapp teaches most of the limitations of the above claim, except that it does not teach the use of a structure to prevent leakage currents. In Yumoto Figure 8, a circuit with is show that utilizes such a structure. The merits of using such structure are stated in [0073], which drastically reduces leakage. For at least the above reasons, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the structure of Knapp to use the double gate transistors in Yumoto Figure 8 to prevent leakage.

As to claim 53, Knapp clearly shows that the holding element 38 is attached to the drive line (supply line) 31, where clearly each (row/column) has its own supply line as discussed above.

Claims 46-47, 49, and 51-52 are rejected under 35 USC 103(a) as unpatentable over Yumoto.

As to claim 46,

An electro-optical device comprising:

-A plurality of data lines; (Yumoto Figure 7, data line driving circuit 22 and the plurality of data lines shown therein)

-A plurality of scan lines; (Yumoto Figure 7, scan line driving circuit 21 and the plurality of data lines shown therein)

-A plurality of unit circuits arranged corresponding to intersections of the plurality of data lines and the plurality of scan lines, each of the unit circuits including: (Yumoto has

pixels 25 that are arranged at the intersection of data lines and scan lines as shown in Figure 7)

-A first transistor; (Yumoto Figure 27, TFT2, n-type)

-An electroluminescence element being connected in series to one of a source and a drain of the first transistor; (Yumoto OLED Figure 27)

-An second transistor arranged between a gate of the first transistor and one of the source and the drain of the first transistor, the second transistor having a structure to prevent leakage currents during shutoff, and the polarity of the second transistor being opposite to the polarity of the first transistor; and (Yumoto Figure 27, TFT4 has opposite polarity – p-type, and it is directly connected to the gate of transistor TFT2, and it is connected to ground via TFT1, which is directly linked back to the drain/source of TFT2 since that is tied to ground. Therefore, as noted above, since the term "arranged" is very broadly, clearly it means something other than 'connected', which therefore means that as long as it is in a path between the two the limitation is met. Yumoto clearly shows in Figure 8 multi-gate elements that are used to block leakage – e.g. TFT4a/b and TFT2a/b [0073], where these are used to suppress the leakage current with the double gate structure.)

-A holding element coupled to the gate of the first transistor, the holding element holding a control voltage, the first transistor supplying a current based on the control voltage to the electroluminescence element. (Yumoto capacitor / holding element C in Figure 27. Clearly, the first transistor is the drive transistor for the OLED because it is the only transistor connected to it, and clearly the holding element holds a control

voltage, since it is connected to the gate of the transistor which only accepts voltage and not current, where clearly the transistor will provide current to the serially connected OLED based on the voltage applied to the gate)

Yumoto teaches all of the limitations in the circuit of Figure 27 as described above but does not expressly teach 'a structure to prevent leakage currents during shutoff.' However, in Figure 8, a circuit with a transistor in a similar position (e.g. TFT4a/b in Figure 8, comparable to TFT4 in Figure 27) utilizes such a structure. The merits of using such a structure are stated in [0073] as noted above, particularly in the case of the circuit of Figure 27 since this is the only transistor controlling the gate voltage of the drive transistor and it would especially desirous to prevent leakage. For at least the above reasons, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the structure in Figure 27 to use the double gate transistors in Figure 8 to prevent leakage.

As to claim 47, clearly a double-gate transistor is a multi-gate transistor, as describe above.

As to claim 49, this claim is a duplicate of the parent claim and recites the limitations found therein in the above rejection.

As to claim 51, Figure 22 meets most of the limitations of claim 46. There is a first transistor TFT2 with a holding element C coupled to the gate, with a second transistor TFT3 connected to the gate of TFT2, and TFT3 is "arranged in a path" via the data line, which is connected to ground, which is connected to the source/drain of TFT2,

thusly linking TFT2 and TFT3 in the required manner. Finally, TFT3 is of the opposite polarity of TFT2.

Additionally, there is a third transistor (TFT4) coupled in series to the first and second transistors, where it is not specified how the series connection is made (e.g. gate to source, source to drain, etc), nor is it specified that the series connections must be contiguous, and 'comprising' language is used)(where TFT4 could be regarded as being connected in series via the holding element C to ground which is in series with that terminal of TFT2). Both TFT3 and TFT4 are connected to scan lines.

Yumoto does not expressly teach that TFT4 and TFT3 are connected to the same scan line. However, in Figure 18, a similar circuit to that shown in Figure 22 is shown, and it is exactly comparable except the fact that the data line is connected to ground. The reasons for this are stated in [0090], in that it allows the omission of another scanning line drive circuit (e.g. two separate drive circuits are not needed). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Figure 22 to have TFT4 and TFT3 both connect to the same scan line.

As to claim 52, it is well known to have a separate drive transistor as in Figure 11 because it is beneficial to do so [0077-0079].

Claims 8-10 and 37-39 are rejected under 35 U.S.C. 103(a) as unpatentable over Yumoto as applied to claim 4 above, and further in view of Maeda.

As to claim 8,

The electro-optical device according to claim 46, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yumoto Figure 3 and [0010] for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yumoto [0011], semiconductor thin film 4); and

-A gate metal layer comprising said second control terminal (Yumoto [0011], gate electrode 2)(forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one scan line among said plurality of scan lines is formed in said gate metal layer (Maeda 0121).

References Yumoto teaches all the limitations of this claim except the formation of a scan line in the gate metal layer. Reference Maeda teaches the formation of scan lines and gate electrodes in the same metal film layer for TFT / LCD monitor fabrication (e.g. 0162, 0121). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single metal layer of Maeda since Maeda performs in one step what Yumoto does in several steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode goes down first and then the scan lines go down after the semiconductor layer, which clearly is a different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination, e.g. common sense is sufficient to justify the

combination. See also *In re Karlson*, 136 USPQ 184 (CCPA 1963), for the doctrine that eliminating components is an obvious expedient – in this, eliminating fabrication steps.

As to claim 9,

The electro-optical device according to claim 46, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yumoto Figure 3 and [0010] for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yumoto [0011], semiconductor thin film 4); and

-A gate metal layer comprising said second control terminal (Yumoto [0012]) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in said gate metal layer (Maeda 0121 and 0113 and 0125).

Reference Yumoto teaches all the limitations of this claim except the formation of a data line in the gate metal layer. Reference Maeda teaches the formation of data lines and source and drain electrodes in the same metal film layer for TFT / LCD monitor fabrication (e.g. 0113, 0125). It would be *prima facie* obvious to choose to form gate electrodes and data lines simultaneously rather than gate electrodes and scan lines, for example. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single metal layer of Maeda since Maeda performs in one step what Yumoto does in several

steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode goes down first and then the scan lines go down after the semiconductor layer, which clearly is a different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

As to claim 10,

The electro-optical device according to claim 46, wherein said active matrix substrate has a stacked-layer structure comprising a plurality of layers (stacked-layer structure established in Yumoto Figure 3 and [0010] for example);

Said plurality of layers comprising:

-A semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed (Yumoto [0011], semiconductor thin film 4); and

-A gate metal layer comprising said second control terminal (Yumoto [0012]) (forming second gate metal is *prima facie* obvious, given that the layer is for the "gate electrode"); and

-A source metal layer comprising a source electrode or drain electrode connected to the source or drain of said second transistor (Maeda 0113, 0125); and

-Wherein at least a portion of one data line among said plurality of data lines is formed in the layer (Maeda 0121 and 0113 and 0125), among said source metal layer and said gate metal layer, which is closer to said semiconductor layer.

Reference Maeda in combination with Yumoto teaches all the limitations of this claim, and this is merely a recitation of the dual limitations of claims 8 and 9 above. As

such, the combination and motivation from claim 8 is used here and no further comment is necessary, as this claim is only a nominal variation of the parent.

As to claim 37,

An electro-optical device according to claim 46, comprising unit circuits comprising transistors, arranged corresponding to intersections of data lines and scan lines (Yumoto Figure 2, and the transistor picture layouts in Figures 5, 8, 9, etc) wherein

-A semiconductor layer constituting such transistors is formed in a semiconductor layer (Yumoto [0011], semiconductor thin film 4);

-Either said scan lines or said data lines are formed in a first conducting layer at the intersections of said scan lines and said data lines (Maeda 0113, 0121, and 0125); and,

-A portion of said scan lines and said data lines outside said intersections are formed in a second conducting layer (Maeda 0113, 0121, and 0125).

Reference Yumoto does not explicitly teach the formation of scan or data lines formed in a conducting layer at the intersections of such lines. Reference Maeda describes forming gate metal and scan lines, etc. simultaneously. As such, the scan lines would be formed everywhere not masked with a shadow mask, e.g. both in the scan lines and in the intersections. No matter what portions of the lines are claimed, any such configuration could be made using shadow masking and formed using either evaporation or sputtering. Any set of contacts could be created using correctly etched contact holes; electrically contiguous metal formed in the same layer is *prima facie* the same from an electrical and an engineering perspective. Further, forming scan lines or data lines or portions thereof (as claimed) in the same layer as other things would

simply be making a component integral by eliminating unnecessary metal, and under *In re Larson*, 144 USPQ 347 (CCPA 1965), making a component integral is obvious and not patentable. Therefore, under either methodology, the recited limitations of the claim have been met.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single metal layer of Maeda since Maeda performs in one step what Yumoto does in several steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode goes down first and then the scan lines go down after the semiconductor layer, which clearly is a different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

As to claim 39,

An electro-optical device according to claim 46, comprising electro-optical elements corresponding to intersections of scan lines and data lines (Yumoto, element OLED in various figures, such as 5, 8, 9, etc), wherein:

-A pair of electrodes is provided to supply power to electro-optical elements (Maeda Fig. 11C, elements 19 and 15 are opposing and pixel electrodes (see 0006-0008));

-At the intersections of said scan lines and said data lines, either said scan lines or said data lines are formed in a first conducting layer (Maeda 0113, 0118, 0121, 0125 – again, gate metal as discussed in rejections to claims 8-12);

-Portions of said scan lines and said data lines outside said intersections are formed in a second conducting layer (source metal layer, 0113, 0118, 0121, 0125 as discussed in rejections to claims 8-12); and,

-Said second conducting layer is positioned at a greater distance than said first conducting layer from one of said pair of electrodes (design choice issue, see Maeda Fig. 11C).

Reference Yumoto does not recite details of the fabrication process claimed above. Reference Maeda teaches the fabrication of such substrates and teaches contact holes (0044, 0047). Logically, such contact holes would fill on conducting layer deposition, thus meeting the recited limitation concerning intersections of data and scan lines. The positioning of a layer or its size is *prima facie* obvious and is not patentable (*In re Japikse* for order of parts and further under *In re Reese*, anyone of ordinary skill in the art would know that there would be an optimal spacing of electrodes from each other to minimize cross-talk that would also occupy the minimum aspect ratio required on the shadow mask).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix of Yumoto with the single metal layer of Maeda since Maeda performs in one step what Yumoto does in several steps (note Yumoto fabrication process in [0011-0013], where the metal gate electrode goes down first and then the scan lines go down after the semiconductor layer, which clearly is a different level), which is *prima facie* more efficient and sufficient motivation in its own right to justify the combination under *In re Karlson* as discussed above.

Claim 38 is rejected over Yumoto and Maeda as applied to claim 37 above, and further in view of Tanaka.

As to claim 38,

The active matrix substrate according to claim 37, wherein said second conducting layer is positioned between said first conducting layer and said semiconductor layer.

Reference Yumoto does not explicitly teach this limitation. In Fig. 10B, Maeda shows that the bottom gate – element 56, which is metal (a niobium alloy) is put down first, then various insulating materials, then element 13 (source and drain electrodes) are formed on the same level and slightly covering the semiconductor layer 54. Under the doctrine of *In re Japikse*, switching the two layers would be *prima facie* obvious, and only minor alternations in the shadow masks for the process would be necessary (additive vs. subtractive processing in semiconductors, for example, switching the process would not be difficult for one of ordinary skill in the semiconductor / TFT art). Again, given that Maeda teaches many different embodiments (see Figs. 10-13, etc.), such a switch would be a design choice issue, and it would allow low-temperature processing of the substrate throughout the process, particularly allowing for newer techniques such as laser annealing and recrystallization of the semiconductor layer taught by Tanaka, and treatment of the semiconductor layer towards the end of processing.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the TFT circuits of Yumoto and Maeda with the laser

annealing processing of polysilicon for TFT applications of Tanaka (see 0002-0015), as both Yumoto ([0011-0013]) and Maeda (0008, 0121, etc.) utilize polysilicon as the semiconductor material, and laser annealing is now a well-known, standard process in the art.

Claim 48 is rejected under 35 U.S.C. 103(a) as unpatentable over Yumoto as applied to claim 46 above, and further in view of Gualandris. The rejection to claim 46 is herein incorporated by reference in its entirety.

Wherein at least said second active element is a transistor comprising a structure selected from the group consisting of an LDD structure, GDD structure, and DDD structure.

Yumoto teaches in [0113] to have the LDD structure in the active transistor, and it is discussed as being the active layer *per se*, that is on top of the gate oxide, so it would work for any transistor as specified there. However, Yumoto does not explicitly teach the use of GDD and DDD structures where Gualandris teaches DDD in 1:55-65, GDD in 2:25-30, and LDD in 2:25-30. Gualandris teaches that these are all methods of doping transistors, although one (the LDD) is preferred to work for 'ULSI' applications. Given that 'ULSI' applications at the time the patent was issued were mainly for deep sub-micron processes and that current TFT / liquid crystal display processes have much larger dimensions, e.g. still larger than one micron minimum channel length for silicon-on-glass technology, these techniques would be perfectly valid for use in TFT / silicon-on-glass technology.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the active matrix substrates of Yumoto with the transistors of Gualandris, since Yamada uses transistors, which *prima facie* have a source and a drain and different drain doping techniques are well-known in the art, and Yumoto also teaches LDD mechanisms of doping, and the others would be obvious to a worker of ordinary skill in the art.

Claim 50 is rejected under 35 USC 103(a) as unpatentable over Yumoto as applied to claim 46, and further in view of Knopp.

Yumoto does not expressly show an example where the first transistor is p-type. Knopp clearly states that the polarity of the transistor is a matter of design choice, see 4:40-45. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a p-type transistor for when the polarity of the waveform was reversed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Woods whose telephone number is 571-272-7775. The examiner can normally be reached on M-F 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Eric Woods

September 21, 2006

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER

Notice of References Cited	Application/Control No. 10/299,861	Applicant(s)/Patent Under Reexamination MATSUEDA, YOJIRO	
	Examiner Eric Woods	Art Unit 2628	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,373,454	04-2002	Knapp et al.	345/76
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/299,861	MATSUEDA, YOJIRO
Examiner	**Art Unit**
Eric Woods	2628

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	+	Restricted	I	Interference	O	Objected

Claim		Date								
Final	Original	9/19/06								
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Claim		Date								
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Search Notes

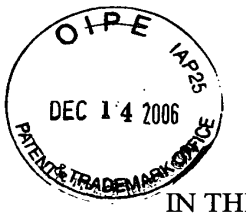
Application/Control No.	Applicant(s)/Patent under Reexamination
10/299,861	MATSUEDA, YOJIRO
Examiner	**Art Unit**
Eric Woods	2628

SEARCHED			
Class	Subclass	Date	Examiner
345	76-79,80-105	9/19/2006	EW

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST (USPT,USPGPUB, DERWENT,EPO,JPO,IBM_TDB)–see attached search histories	9/19/2006	EW

TFW 2628



PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2628

Application No.: 10/299,861

Examiner: E. WOODS

Filed: November 20, 2002

Docket No.: 114251

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE

AMENDMENT UNDER 37 C.F.R. §1.111

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the September 29, 2006 Office Action, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1-7. (Canceled)

8. (Currently Amended) The electro-optical device according to claim 46, wherein said ~~active matrix substrate~~ electro-optical device has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed; and

a gate metal layer comprising said second control terminal, and

wherein at least a portion of said plurality of scan lines is formed in said gate metal layer.

9. (Currently Amended) The electro-optical device according to claim 46, wherein said ~~active matrix substrate~~ electro-optical device has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed; and

a gate metal layer comprising said second control terminal; and

wherein at least a portion of one data line among said plurality of data lines is formed in said gate metal layer.

10. (Currently Amended) The electro-optical device according to claim 46, wherein said ~~active matrix substrate~~ electro-optical device has a stacked-layer structure comprising a plurality of layers;

said plurality of layers comprising:

a semiconductor layer, in which a semiconductor film constituting said first transistor and said second transistor is formed;

a gate metal layer comprising said second control terminal; and

a source metal layer comprising a source electrode or drain electrode connected to the source or drain of said second transistor;

wherein at least one portion of at least one data line among said plurality of data lines is formed in the layer, among said source metal layer and said gate metal layer, that is closer to said semiconductor layer.

11-36. (Canceled)

37. (Previously Presented) The electro-optical device in accordance with claim 46, comprising unit circuits comprising transistors, arranged corresponding to intersections of data lines and scan lines; wherein

a semiconductor film constituting said transistors is formed in a semiconductor layer;

either said scan lines or said data lines are formed in a first conducting layer at the intersections of said scan lines and said data lines; and

a portion of said scan lines and said data lines outside said intersections are formed in a second conducting layer.

38. (Previously Presented) The electro-optical device according to claim 37, wherein said second conducting layer is positioned between said first conducting layer and said semiconductor layer.

39. (Previously Presented) The electro-optical device according to claim 46, comprising electro-optical elements corresponding to intersections of scan lines and data lines, wherein:

a pair of electrodes is provided to supply power to said electro-optical elements;

at the intersections of said scan lines and said data lines, either said scan lines or said data lines are formed in a first conducting layer;

portions of said scan lines and said data lines outside said intersections are formed in a second conducting layer; and

said second conducting layer is positioned at a greater distance than said first conducting layer from one of said pair of electrodes.

40-45. (Canceled)

46. (Currently Amended) An electro-optical device comprising:

a plurality of data lines;

a plurality of scan lines;

a plurality of unit circuits arranged corresponding to intersections of the plurality of data lines and the plurality of scan lines, each of the unit circuits including:

a first transistor;

an electroluminescence element being connected in series to one of a source and a drain of the first transistor;

a second transistor arranged between a gate of the first transistor and one of the source and the drain of the first transistor, the second transistor having a structure to prevent leakage currents during shutoff, and the polarity of the second transistor being opposite to the polarity of the first transistor; and

a holding element coupled to the gate of the first transistor, the holding element holding a control voltage, the first transistor supplying a current based on the control voltage to the electroluminescence ~~element.~~element; and

at least a part of a wiring connecting between the first and second transistors being formed in a metal layer other than a semiconductor layer in which the first and second transistors are formed.

47. (Previously Presented) The electro-optical device according to claim 46, wherein the second transistor is configured as a multi-gate transistor.

48. (Previously Presented) The electro-optical device according to claim 46, wherein the second transistor has a structure selected from the group consisting of an LDD structure, a GDD structure, and a DDD structure.

49. (Canceled)

50. (Previously Presented) The electro-optical device according to claim 46, wherein the first transistor has a p-type polarity.

51. (Currently Amended) The electro-optical device according to claim 46, each of the unit circuits including a third transistor coupled in series to the first and the second transistor, a source and a drain of the third transistor connecting each respectively to one of the first and the second transistors and a gate of the second transistor and a gate of the third transistor being connected to a same corresponding scan line.

52. (Currently Amended) The electro-optical device according to claim ~~46~~51, each of the unit circuits including a fourth transistor coupled in series to the first transistor, the fourth transistor supplying the current to the electroluminescence element during a light emission period.

53. (Previously Presented) The electro-optical device according to claim 46, further comprising a plurality of power supply lines, one electrode of the holding element is connected to a corresponding power supply line of the plurality of power supply lines, or the one electrode of the holding element is a portion of the corresponding power supply line of the plurality of power supply lines.

REMARKS

Claims 8-10, 37-39, 46-48 and 50-53 are pending in this application. By this Amendment, claims 8-10, 46, 51 and 52 are amended. Claim 49 is canceled without prejudice to, or disclaimer of, the subject matter recited in this claim. Reconsideration of the application in view of the foregoing amendments and the following remarks is respectfully requested.

The Office Action objects to claim 52 because of an informality. Claim 52 is amended in response to the claim objection. Accordingly, reconsideration and withdrawal of the objection to claim 52 are respectfully requested.

The Office Action rejects claims 10 and 51 under 35 U.S.C. §112, second paragraph and claim 49 under 35 U.S.C. §112, fourth paragraph.

Claims 10 and 51 are amended, and claim 49 is canceled, in response to the claim rejections. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. §112, second paragraph, and fourth paragraph, are respectfully requested.

The Office Action rejects claims 46 and 53 under 35 U.S.C. §103(a) over U.S. Patent No. 6,373,454 to Knapp et al. (Knapp) in view of U.S. Patent Application Publication No. 2004/0207615 to Yumoto et al. (Yumoto); rejects claims 46, 47, 49, 51 and 52 over Yumoto; rejects claims 8-10 and 37-39 over Yumoto in view of U.S. Patent Application Publication No. 2002/0008822 to Maeda; rejects claim 38 over Yumoto and Maeda and further in view of U.S. Patent Application Publication No. 2001/0026835 to Tanaka; rejects claim 48 over Yumoto and further in view of U.S. Patent No. Re. 35,827 to Gualandris et al. (Gualandris); and rejects claim 50 over Yumoto and further in view of Knapp. The rejection of claim 49 is moot in view of the cancellation of claim 49. The rejections are respectfully traversed with respect to claims 8-10, 37-39, 46-48 and 50-53.

Claim 46, recites, among other features, a second transistor arranged between a gate of the first transistor and one of the source and the drain of the first transistor, the second transistor having a structure to prevent leakage currents during shutoff; and at least a part of a wiring connecting between the first and second transistors, being formed in a metal layer other than a semiconductor layer in which the first and second transistors are formed. Support for the added feature can be found, for example, in Fig. 2. None of the applied references taken alone, or in combination, teach, or reasonably would have suggested, this feature.

The Office Action acknowledges that Knapp does not teach that its structure can be used to prevent leakage currents, as claim 46 recites. Knapp also does not teach or suggest that at least a part of a wiring connection between the first and second transistors being formed in a metal layer other than a semiconductor layer in which the first and second transistors are formed. Rather, Knapp merely teaches that its electroluminescent display element 20 comprises an organic light emitting diode (LED) and comprising a pair of electrodes between which one or more active layers of organic electroluminescence material is sandwiched (col. 5, lines 40 - 66). Knapp also mentions that the matrix structure of its array may comprise thin film transistors (TFTs), the sets of address lines, the storage capacitors (if provided as discrete components), the display element electrodes and their interconnections, formed using standard thin film processing technology similar to that used in active matrix LCDs which basically involves the deposition and patterning of various thin film layers of conductive, insulating and semiconductive materials on the surface of an insulating support such as glass or plastics material by CVD deposition and photolithographic patterning techniques. Nevertheless, Knapp does not teach or suggest the features positively recited in claim 46.

On page 7, the Office Action relies upon Yumoto to teach "the use of preventing leakage currents." On page 9, the Office Action admits that Yumoto does not teach the feature of "a structure to prevent leakage currents during shutoff", but indicates that Yumoto suggests such a feature. However, Yumoto does not cure the above-discussed deficiency of Knapp because Yumoto also does not teach or suggest the positively recited combination of features of a second transistor having a structure to prevent leakage current during shutoff and at least a part of a wiring connecting between the first and second transistors, being formed in a metal layer other than a semiconductor layer in which the first and second transistors are formed. According to the wiring configuration as recited in claim 46, this wiring construction may require through holes for implementation, but such a connection through another layer other than a semiconductor layer more than likely may cause current leakage. Thus, having the structure and capability to prevent current leakage during shutoff can be an important factor when the control (first) transistor and the drive (second) transistor are connected via a wiring which is partially formed in a metal layer other than the semiconductor layer, as claim 46 recites. Yumoto does not teach or suggest this feature of claim 46.

Rather, Yumoto discloses a display device that uses a pixel circuit. The pixel comprises a light emitting element OLED, a first thin transistor TFT1, a second thin film transistor TFT2 and a holding capacitor. Fig. 3 illustrates a sectional structure of the pixel, where only the OLED and TFT2 are represented. The OLED is configured by successively superposing a transparent electrode 10, an organic EL layer 11, and a metal electrode 12. The TFT2 comprises a gate electrode 2 formed on a substrate 1 made of glass or the like, the gate insulating film 3 superimposed on the top surface thereof, and a semiconductor thin film 4 superimposed above the gate 2 via the gate insulating film 3. The TFT2 is provided with a source S, a channel Ch, and a drain D which acts as a passage of the current supplied to the OLED. As Yumoto discusses in paragraph [0031], the first gate electrode 2, the gate

insulating film 3, and the semiconductor thin film 4 are successively stacked and patterned on the glass substrate 1 to form the TFT2. However, nowhere does Yumoto teach or disclose that at least part of the wiring connecting the first and second transistors being formed in a metal layer other than the semiconductor layer in which the first and second transistors are formed.

Furthermore, with respect to combining the prior art references, Maeda is relied upon for allegedly teaching wherein at least a portion of a plurality of scan lines is formed in a gate metal layer. As the Office Action admits, Maeda only discloses a single metal layer. Maeda does not teach or suggest at least a part of the wiring connecting between the first and second transistors, being formed in a metal layer other than a semiconductor layer in which the first and second transistors are formed. The Office Action relies on Tanaka for allegedly teaching wherein the second conducting layer is positioned between the first conducting layer and the semiconductor layer; and Gualandris is relied upon for allegedly teaching wherein the second active element is a transistor comprising a structure selected from the group consisting of an LDD structure, GDD structure and DDD structure. Thus, these prior art references do not overcome the above-referenced shortfall in the application of Knapp in combination with Yumoto or Yumoto alone with respect to the features positively recited in claim 46.

In view of the above, the prior art references, taken alone or in any permissible combination, do not teach, nor can they reasonably be considered to have suggested the combination of all of the features positively recited in claim 46. Further, claims 8-10, 37-39, 47, 48 and 50-53 also would not have been suggested by the applied prior art references for at least their respective dependence directly or indirectly on allowable base claim 46, as well as for the separately patentable matter that each of these claims recites.

Accordingly, reconsideration and withdrawal of the rejections of the pending claims over any permissible combination of the applied prior references are respectfully requested.

Further, the alleged motivations to combine presented in the abbreviated conclusory form, for example, "[t]o prevent leakage", "common sense... that the eliminating components is an obvious expedient", "electrically contiguous metal formed in the same layer is *prima facie* the same from an electrical and an engineering perspective" "the positioning of the layer and its size is *prima facie* obviousness", "where the metal gate electrode goes down first and then the scan line go down after the semiconductor layer, . . . which is *prima facie* more efficient and sufficient motivation" or "a matter of design choice" are not enough to prove that there is a teaching, suggesting or motivation in the prior art to combine the references in the manner suggested by the Office Action. The Federal Circuit recently reaffirmed its prior holdings asserting that "rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, Appeal No. 04-1616, March 22, 2006 (Fed. Cir.) (quoting *In re Lee*" 277 F.3d 1338,1343 46 (Fed. Cir. 2002)). This standard is not met here as no articulated reasoning with some rational underpinning is provided.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 8-10, 37-39, 46-48 and 51-53 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

Dinnatia Doster-Greene

James A. Oliff
Registration No. 27,075

Dinnatia J. Doster-Greene
Registration No. 45,268

JAO/DJG:mab

Date: December 14, 2006

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

PATENT APPLICATION FEE DETERMINATION RECORD
Effective December 8, 2004

10/299861

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	minus 20=	*
INDEPENDENT CLAIMS	minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐ OR OTHER THAN SMALL ENTITY

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BASIC FEE		OR	BASIC FEE	
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL		OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A

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Total	* 13	Minus	** 14	=
Independent	* 1	Minus	*** 1	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY OR OTHER THAN SMALL ENTITY

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X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
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X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
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Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
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X100=		OR	X200=	
+180=		OR	+360=	

PLUS Search Results for S/N 10299861, Searched Tue Mar 06 08:27:45 EST 2007

The Patent Linguistics Utility System (PLUS) is a USPTO automated search system for U.S. Patents from 1971 to the present PLUS is a query-by-example search system which produces a list of patents that are most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

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OIPE
MAR 06 2007
PATENT & TRADEMARK OFFICE

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2628

Application No.: 10/299,861

Examiner: E. WOODS

Filed: November 20, 2002

Docket No.: 114251

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, Notice of Allowance or other action that closes prosecution (e.g., Quayle Action).

☒ a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

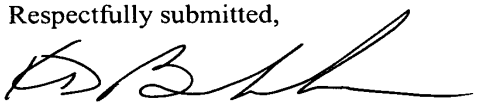
☒ 2. One or more reference cited herein was cited in a counterpart foreign application. See References 1 and 2.

☒ 3. An English language Abstract of one or more non-English language reference is attached hereto. See References 3 and 4.

☒ 4. A computer-generated English language translation of one or more Japanese Patent Publication cited herein has been obtained from the website of the Japanese Patent Office ([http://www.jpo.go.jp]), and is attached, but has not been reviewed for accuracy. See References 3 and 4.

☒ 5. References 1 and 2 correspond to references 3 and 4, respectively.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

Kirk D. Berkhimer
Registration No. 59,874

JAO:KDB/jam

Date: March 6, 2007

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P.O. Box 19928
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Form PTO-1449 (REV. 1/06)	US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 114251	APPLICATION NO. 10/299,861
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT(S) Yojiro MATSUEDA	
		FILING DATE November 20, 2002	GROUP 2628

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Name

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
	1	CN 1291786A	04/18/2001	CHINA		
	2	CN 1242924A	01/26/2000	CHINA		
	3	JP-A-2001-185354	07/06/2001	JAPAN	XX	XX
	4	JP-A-11-074073	03/16/1999	JAPAN	XX	XX

OTHER DOCUMENTS

Examiner Initials	Cite No.	(Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: March 6, 2007

[19]中华人民共和国国家知识产权局

[51]Int. Cl⁷
H01L 21/00
H01L 31/12 H01L 27/15

[12]发明专利申请公开说明书

[21]申请号 00130499.2

[43]公开日 2001年4月18日 ✓

[11]公开号 CN 1291786A ✓

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[30]优先权
[32]1999.10.12 [33]JP [31]290314/1999
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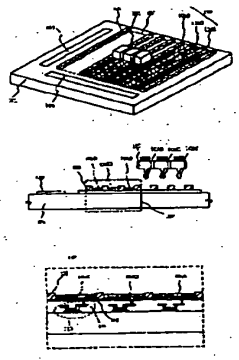
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[54]发明名称 电光器件及其制作方法

[57]摘要

本发明目的是提供简单、高速的,用喷墨方法形成EL层的加工技术。一种制作具有良好操作性能和高可靠性的电光器件的方法,和特别是,提供一种制作EL显示器件的方法。当EL层用喷墨方法制作时,本发明形成连续横过多个电极的EL层。特别地,对于排列成矩阵状态的m列和n行像素电极,EL层形成对应于一个特定行或列的条形。对于每一个像素电极,EL层也可以被形成具有长圆形或矩形形状。



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说　明　书

电光器件及其制作方法

本发明涉及电光器件，典型地为EL（电致发光）显示器件，通过在基底表面上加工半导体元件（使用半导体薄膜的元件）形成，以及包括该电光器件作为显示器件的电子器件．特别地，本发明涉及上述器件的制作方法．

近年来，在基底上形成薄膜晶体管（以下称为“TFT”）的技术已经取得相当大的进步，并且已开始开展它的应用和开发成有源矩阵类型显示器件．特别地，由于TFT使用具有晶体结构的半导体薄膜（例如多晶硅膜），比使用非晶硅膜的传统的TFT具有更高的场效应迁移率，所以可以获得高速操作性能．因此，有可能形成连接像素点和TFT的驱动电路，和在同一基底上形成驱动电路．

由于各种优点，如制作成本的降低，显示器件的小型化和变薄，合格率和产量的提高，这样的有源矩阵类型显示器件已经被注意，并能通过在同一基底上制作各种电路和元件获得．

在有源矩阵类型EL显示器件中，为每一个像素提供TFT组成的开关元件，并且由开关元件操作进行电流控制的驱动元件，以使EL层（光发射层）发光．例如，已有EL显示器件公开于美国专利No.5684365中（见日本专利申请公开平No. 8-234683），或日本专利申请公开平No. 10-189252中．

在这些EL显示器件的彩色显示方法中，已经有试验布置EL层，在每一个像素点发出的光为三原色红（R）、绿（G）和蓝（B）．然而，几乎所有一般用于EL层的材料都是有机材料，难于应用微加工中使用的光刻技术．原因是EL材料本身对潮湿极其脆弱，并且它们的加工是困难的，因为它们甚至易于溶解于显影溶液中．

通过喷墨方法形成EL层的技术已经被建议作为解决这类问题的技术．例如，在日本专利申请公开平No.10-012377中，公开了有源矩阵类型EL显示器件中的EL层是用喷墨方法形成的．进而，类似的技术也公开于Shimada，T.，et al.“通过喷墨印刷对发光聚合物进行多彩色象素构图（Multicolor Pixel Patterning of Light-Emitting Polymers by Ink-jet Printing），”SID 99 DIGEST，pp.376-379.