

inputted from the outside is changed into n bit digital video data for gradation voltage, Both a circuit which supplies said n bit digital video data to said source driver, and (m and n are two or more positive numbers and $m > n$) display devices which it has, and said source driver, It has a D/A conversion circuit which changes said n bit digital video data into analog gradation voltage, A display device performing a time gradation display and obtaining a gradation display of a passage ($2^m - (2^{m-n} - 1)$) by forming an image of one frame by a subframe of a 2^{m-n} individual.

[Claim 7]An active matrix circuit where two or more pixels TFT have been arranged at matrix form, A source driver and a gate driver which drive said active matrix circuit, a circuit (m.) which changes into n bit digital video data for gradation voltage m bit digital video data inputted from the outside A D/A conversion circuit which both n changes two or more positive numbers, $m > n$, and said n bit digital video data into an analog video data, and is inputted into said source driver and to carry out, A display device which is a display device which **** and is characterized by performing a time gradation display by forming an image of one frame by a subframe of a 2^{m-n} individual.

[Claim 8]An active matrix circuit where two or more pixels TFT have been arranged at matrix form, A source driver and a gate driver which drive said active matrix circuit, a circuit (m.) which changes into n bit digital video data for gradation voltage m bit digital video data inputted from the outside A D/A conversion circuit which both n changes two or more positive numbers, $m > n$, and said n bit digital video data into an analog video data, and is inputted into said source driver and to carry out, A display device being a display device which ****, performing a time gradation display by forming an image of one frame by a subframe of a 2^{m-n} individual, and obtaining a gradation display of a passage ($2^m - (2^{m-n} - 1)$).

[Claim 9]The display device according to any one of claims 1 to 8, wherein said m is 8 and said n is 2.

[Claim 10]The display device according to any one of claims 1 to 8, wherein said m is 10 and said n is 2.

[Claim 11]The display device according to any one of claims 1 to 8, wherein said m is 12 and said n is 4.

[Claim 12]A rear projector provided with the three display devices according to any one of claims 1 to 11.

[Claim 13]A front projector provided with the three display devices according to any one of claims 1 to 11.

[Claim 14]A single plate type rear projector provided with the one display device according to any one of claims 1 to 11.

[Claim 15]A goggles type display provided with the display device according to any one of claims 1 to 11 two.

[Translation done.]

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1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

[0002]This invention relates to a display device. It is related with the display device which performs a gradation display by both gradation voltage and time gradation especially.

[0003]

[Description of the Prior Art]

[0004]The semiconductor device which formed semiconductor membrane on the inexpensive glass substrate recently, for example, the technology which produces a thin film transistor (TFT), is progressing quickly. The Reason is because the demand of active matrix type displays has increased.

[0005]The pixel TFT is arranged in tens arranged at matrix form - the picture element region of 1 million numbers, respectively, and an active matrix type display controls the electric charge which frequents the picture element electrode connected to each pixel TFT by the switching function of the pixel TFT.

[0006]In recent years, the multi-gradation display which can perform a full color display desirably is called for with highly-minute-izing of a picture, and high resolution-ization.

[0007]The active matrix type display of the digital drive system in which a high speed drive is possible has attracted attention with highly-minute-izing of a display device, and high-resolution-izing also in an active matrix type display.

[0008]

[Problem to be solved by the invention]

[0009]The D/A conversion circuit (DAC) which changes into analog data (gradation voltage) the digital video data inputted from the outside is required for the active matrix type display of a digital drive system. Various kinds of things exist in a D/A conversion circuit.

[0010]The capability of this D/A conversion circuit, i.e., a D/A conversion circuit, depends for the multi-tone display ability of an active matrix type display on whether the digital video data which what bit is is convertible for analog data. For example, if it is a display device which generally has a D/A conversion circuit which processes a 2-bit digital video data, a $2^2=4$ gradation display can be performed, if 8 bits becomes, a $2^8=256$ gradation display can be performed, and if it is n bit, a 2^n gradation display can be performed.

[0011]However, in order to improve the capability of a D/A conversion circuit, the circuitry of a D/A conversion circuit becomes complicated, and a layout area becomes large. These days, the display device which forms a D/A conversion circuit by poly-Si TFT on the same substrate as an active matrix circuit has been reported. However, if the circuitry of a D/A conversion circuit becomes complicated in this case, the yield of a D/A conversion circuit will fall and the yield of a display device will also fall. If the layout area of a D/A conversion circuit becomes large, it will become

difficult to realize a small display device.

[0012]

[Means for solving problem]

[0013]Then, this invention is made in view of an above-mentioned problem, and provides the display device which can realize the display of multi-tone.

[0014]First, drawing 1 is referred to. The outline block diagram of the display device of this invention is shown in drawing 1. 101 is a display panel which has a digital driver. 101-1 is a source driver, 101-2 and 101-3 are gate drivers, and 101-4 is an active matrix circuit where two or more pixels TFT have been arranged at matrix form. The source driver 101-1, the gate driver 101-2, and 101-3 drive an active matrix circuit. 102 is a digital video data time gradation processing circuit.

[0015]The digital video data time gradation processing circuit 102 changes the digital video data of n bit into the digital video data for the gradation voltage of n bit among m bit digital video datas inputted from the outside. The gradation information of a low rank (m-n) bit is expressed by time gradation among the digital video datas of m bit.

[0016]n bit digital video data changed by the digital video data time gradation processing circuit 102 is inputted into the display panel 101. n bit digital video data inputted into the display panel 101 is inputted into a source driver, is changed into analog gradation data in the D/A conversion circuit in a source driver, and is supplied to each source signal line.

[0017]Next, another example of the display device of this invention is shown in drawing 2. In drawing 2, 201 is a display panel which has an analog driver. 201-1 is a source driver, 201-2 and 201-3 are gate drivers, and 201-4 is an active matrix circuit where two or more pixels TFT have been arranged at matrix form. The source driver 201-1, the gate driver 201-2, and 201-3 drive an active matrix circuit. 202 is an A/D conversion circuit and changes into m bit digital video data the analog video data supplied from the outside. 203 is a digital video data time gradation processing circuit. The digital video data time gradation processing circuit 203 changes the digital video data of n bit into the digital video data for the gradation voltage of n bit among m bit digital video datas inputted. The gradation information of a low rank (m-n) bit is expressed by time gradation among the digital video datas of m bit inputted. n bit digital video data changed by the digital video data time gradation processing circuit 203 is inputted into the D/A conversion circuit 204, and is changed into an analog video data. The analog video data changed by the D/A conversion circuit 204 is inputted into the display panel 201. The analog video data inputted into the display panel 201 is inputted into a source driver, is sampled by the sampling circuit in a source driver, and is supplied to each source signal line.

[0018]The details of operation of the display device of this invention will be later mentioned using an embodiment.

[0019]The composition of this invention is described below.

[0020]The active matrix circuit where two or more pixels TFT have been arranged at matrix form according to this invention, The source driver and gate driver which drive said active matrix circuit, It is a display device which ****, and top n bits of m bit digital video data inputted from the outside are used as information on gradation voltage, a low rank (m-n) bit is used as information on time gradation, and a display device, wherein both m and n are two or more positive numbers and $m > n$ is provided. .

[0021]The active matrix circuit where two or more pixels TFT have been arranged at matrix form according to this invention, The source driver and gate driver which drive said active matrix circuit, m bit digital video data inputted from the outside is changed into n bit digital video data for gradation voltage, the circuit (m.) which supplies said n bit digital video data to said source driver Both n is two or more positive numbers and a display device which has $m > n$, and the display device performing a time gradation display is provided by forming the image of one frame by the subframe of a 2^{m-n} individual.

[0022]The active matrix circuit where two or more pixels TFT have been arranged at matrix form

according to this invention, The source driver and gate driver which drive said active matrix circuit, m bit digital video data inputted from the outside is changed into n bit digital video data for gradation voltage, the circuit (m.) which supplies said n bit digital video data to said source driver Both n is two or more positive numbers and a display device which has $m > n$, a time gradation display is performed by forming the image of one frame by the subframe of a 2^{m-n} individual, and the display device obtaining the gradation display of a passage ($2^m - (2^{m-n} - 1)$) is provided.

[0023]The active matrix circuit where two or more pixels TFT have been arranged at matrix form according to this invention, The source driver and gate driver which drive said active matrix circuit, Top n bits of m bit digital video data which is a display device which **** and is inputted from the outside as information on gradation voltage, And a display device, wherein said source driver has a D/A conversion circuit which changes said n bit digital video data into analog gradation voltage is provided, using a low rank (m-n) bit as information on time gradation (both m and n are two or more positive numbers and $m > n$).

[0024]The active matrix circuit where two or more pixels TFT have been arranged at matrix form according to this invention, The source driver and gate driver which drive said active matrix circuit, m bit digital video data inputted from the outside is changed into n bit digital video data for gradation voltage, Both the circuit which supplies said n bit digital video data to said source driver, and (m and n are two or more positive numbers and $m > n$) display devices which it has, and said source driver, It has a D/A conversion circuit which changes said n bit digital video data into analog gradation voltage, and the display device performing a time gradation display is provided by forming the image of one frame by the subframe of a 2^{m-n} individual.

[0025]The active matrix circuit where two or more pixels TFT have been arranged at matrix form according to this invention, The source driver and gate driver which drive said active matrix circuit, m bit digital video data inputted from the outside is changed into n bit digital video data for gradation voltage, Both the circuit which supplies said n bit digital video data to said source driver, and (m and n are two or more positive numbers and $m > n$) display devices which it has, and said source driver, It has a D/A conversion circuit which changes said n bit digital video data into analog gradation voltage, By forming the image of one frame by the subframe of a 2^{m-n} individual, a time gradation display is performed and the display device obtaining the gradation display of a passage ($2^m - (2^{m-n} - 1)$) is provided.

[0026]The active matrix circuit where two or more pixels TFT have been arranged at matrix form according to this invention, The source driver and gate driver which drive said active matrix circuit, the circuit (m.) which changes into n bit digital video data for gradation voltage m bit digital video data inputted from the outside The D/A conversion circuit which both n changes two or more positive numbers, $m > n$, and said n bit digital video data into an analog video data, and is inputted into said source driver and to carry out, It is a display device which **** and the display device performing a time gradation display is provided by forming the image of one frame by the subframe of a 2^{m-n} individual.

[0027]The active matrix circuit where two or more pixels TFT have been arranged at matrix form according to this invention, The source driver and gate driver which drive said active matrix circuit, the circuit (m.) which changes into n bit digital video data for gradation voltage m bit digital video data inputted from the outside The D/A conversion circuit which both n changes two or more positive numbers, $m > n$, and said n bit digital video data into an analog video data, and is inputted into said source driver and to carry out, It is a display device which ****, and by forming the image of one frame by the subframe of a 2^{m-n} individual, a time gradation display is performed and the display device obtaining the gradation display of a passage ($2^m - (2^{m-n} - 1)$) is provided.

[0028]Said m may be 8 and said n may be 2.

[0029]Said m may be 10 and said n may be 2.

[0030] Said m may be 12 and said n may be 4.

[0031]

[Mode for carrying out the invention]

[0032] The display device of this invention is explained with an embodiment below. However, the display device of this invention is not necessarily limited to following embodiments.

[0033] (Embodiment 1)

[0034] The outline block diagram of the display device of this embodiment is shown in drawing 3. In this embodiment, since explanation is simple, the display device in which a 4-bit digital video data is supplied from the exterior is taken for an example.

[0035] 301 is a display panel which has a digital driver. 301-1 is a source driver, 301-2 and 301-3 are gate drivers, and 301-4 is an active matrix circuit where two or more pixels TFT have been arranged at matrix form.

[0036] The digital video data time gradation processing circuit 302 changes the digital video data of 2 bits of higher ranks into the digital video data for the gradation voltage of 2 bits among the 4-bit digital video datas inputted from the outside. The gradation information of 2 bits of low ranks is expressed by time gradation among 4-bit digital video datas.

[0037] The top 2-bit digital video data changed by the digital video data time gradation processing circuit 302 is inputted into the display panel 301. The 2-bit digital video data inputted into the display panel 301 is inputted into a source driver, is changed into analog gradation data in the D/A conversion circuit (not shown) in a source driver, and is supplied to each source signal line. The D/A conversion circuit built in the display panel of this embodiment changes a 2-bit digital video data into analog gradation voltage.

[0038] Here, the case where the display panel of this embodiment is a liquid crystal panel using the liquid crystal as an expression medium is explained. The circuitry of the display panel 301, especially the active matrix circuit 301-4 are explained using drawing 4.

[0039] The active matrix circuit 301-4 has a pixel of an individual (xxy). Marks, such as the expedient top of explanation, P1, 1, P2, 1, ..., Py, and x, are attached to each pixel. Each pixel has pixel TFT 301-4-1 and retention volume 301-4-3. The liquid crystal is inserted between the active matrix substrate and counter substrate in which the source driver 301-1, the gate driver 301-2, 301-3, and the active matrix circuit 301-4 are formed. The liquid crystal 3006 shows the liquid crystal corresponding to each pixel typically.

[0040] The digital driver display panel of this embodiment performs what is called a line sequential drive that drives simultaneously the pixel for one line (for example, P1, 1, P1, 2, ..., P1, x). In other words, analog gradation voltage is simultaneously written in the pixel for one line. The time taken to write analog gradation voltage in all the pixels (P1, 1 - Py, x) will be called 1 frame period (Tf). The period which quadrisectioned 1 frame period (Tf) will be called a subframe period (Tsf). The time taken to write analog gradation voltage in the pixel for one line (for example, P1, 1, P1, 2, ..., P1, x) will be called 1 line period (Tsfl).

[0041] The gradation display of the display device of this embodiment is explained. The digital video data supplied to the display device of this embodiment from the outside is 4 bits, and has the information on 16 gradation. Here, drawing 5 is referred to. The gradation display level of the display device of this embodiment is shown in drawing 5. Voltage-level VL is the minimum voltage level inputted into a D/A conversion circuit, and the voltage level VH is the highest voltage level inputted into a D/A conversion circuit.

[0042] In this embodiment, in order to realize the voltage level of 4 gradation, between the voltage level VH and voltage-level VLs was mostly divided into equal voltage level, and the step of the voltage level was set to alpha. It is $\alpha = (VH - VL) / 4$. Therefore, the gradation voltage level which the D/A conversion circuit of this embodiment outputs, When the address of a digital video data is (00), it is set to VL, when the address of a digital video data is (01), it becomes VL+alpha, when the address of a digital video data is (10), it is set to VL+2alpha, and it is set to VL+3alpha when the

address of a digital video data is (11).

[0043]The gradation voltage level which can output the D/A conversion circuit of this embodiment is four kinds, VL, VL+alpha, VL+2alpha, and VL+3alpha, as mentioned above. Then, in this invention, the number of the gradation display levels of a display device can be raised by combining a time gradation display. In this embodiment, the gradation display level equivalent to the gradation voltage level which divided Step alpha of the voltage level into about four equally is realizable by having information for 2 bits of the 4-bit digital video datas in a time gradation display, and being. The display device of this embodiment That is, VL, VL+alpha/4, VL+2alpha/4, VL+3alpha/4, VL+alpha, VL+2alpha, VL+3alpha, VL+4alpha, VL+5alpha/4, VL+6alpha/4, VL+7alpha/4, VL+2alpha, VL+9alpha/4, VL+10alpha/4, VL+11alpha/4, and VL+3alpha is realizable.

[0044]Here, correspondence with the 4-bit digital video data address inputted from the outside, the digital video data address after time gradation processing and the gradation voltage level corresponding to it, and the gradation display level which combined time gradation is shown in the following table 1.

[0045]

[Table 1]

デジタルビデオ データアドレス		時間階調処理後 デジタルビデオデータアドレス (階調電圧 レベル)				時間階調を 組み合わせた 階調表示レベル
上位	下位	1st Tsfl	2nd Tsfl	3rd Tsfl	4th Tsfl	
00	00	00 (VL)	00 (VL)	00 (VL)	00 (VL)	VL
	01	00 (VL)	00 (VL)	00 (VL)	01 (VL+ α)	VL+ $\alpha/4$
	10	00 (VL)	00 (VL)	01 (VL+ α)	01 (VL+ α)	VL+2 $\alpha/4$
	11	00 (VL)	01 (VL+ α)	01 (VL+ α)	01 (VL+ α)	VL+3 $\alpha/4$
01	00	01 (VL+ α)	01 (VL+ α)	01 (VL+ α)	01 (VL+ α)	VL+ α
	01	01 (VL+ α)	01 (VL+ α)	01 (VL+ α)	10 (VL+2 α)	VL+5 $\alpha/4$
	10	01 (VL+ α)	01 (VL+ α)	10 (VL+2 α)	10 (VL+2 α)	VL+6 $\alpha/4$
	11	01 (VL+ α)	10 (VL+2 α)	10 (VL+2 α)	10 (VL+2 α)	VL+7 $\alpha/4$
10	00	10 (VL+2 α)	10 (VL+2 α)	10 (VL+2 α)	10 (VL+2 α)	VL+2 α
	01	10 (VL+2 α)	10 (VL+2 α)	10 (VL+2 α)	11 (VL+3 α)	VL+9 $\alpha/4$
	10	10 (VL+2 α)	10 (VL+2 α)	11 (VL+3 α)	11 (VL+3 α)	VL+10 $\alpha/4$
	11	10 (VL+2 α)	11 (VL+3 α)	11 (VL+3 α)	11 (VL+3 α)	VL+11 $\alpha/4$
11	00	11 (VL+3 α)	11 (VL+3 α)	11 (VL+3 α)	11 (VL+3 α)	VL+3 α
	01	11 (VL+3 α)	11 (VL+3 α)	11 (VL+3 α)	11 (VL+3 α)	VL+3 α
	10	11 (VL+3 α)	11 (VL+3 α)	11 (VL+3 α)	11 (VL+3 α)	VL+3 α
	11	11 (VL+3 α)	11 (VL+3 α)	11 (VL+3 α)	11 (VL+3 α)	VL+3 α

[0046]The display device of this embodiment shows by dividing the 1 frame period T_f during [four] the subframe (1st Tsf, 2nd Tsf, 3rd Tsf, and 4th Tsf). Since the display device of this embodiment performs a line sequential drive, gradation voltage is written during 1 line period (Tsfl) in each pixel. Therefore, each subframe period (3rd Tsf 2nd Tsf 1stTsfl) And each subframe line period corresponding to 4th Tsf (1st Tsfl) The address of the 2-bit digital video data after time gradation processing is inputted into a D/A conversion circuit, and gradation voltage is outputted to 2nd Tsfl, 3rd Tsfl, and 4th Tsfl from a D/A conversion circuit. Four subframe line periods (2nd Tsfl 1st Tsfl) Four displays of a subframe will be performed at high speed by the gradation voltage written in 3rd Tsfl and 4th Tsfl, and the gradation display of one frame will be what carried out the time average of the total of the gradation voltage level of each subframe line period as a result.

[0047]As shown in Table 1, in this embodiment, the gradation voltage level (VL+3 α) in which the address of - (1100) (1111) of a 4-bit digital video data is the same is outputted.

[0048]Therefore, in the display device of this embodiment, even when the D/A conversion circuit treating a 2-bit digital video data is carried out, the gradation level of $3 = 2^4 - 13$ gradation can be displayed.

[0049]The drive timing chart of the display device of this embodiment is shown in drawing 6. The pixel P1, 1 – the pixel Py, and 1 take for an example, and they are shown in drawing 6.

[0050]When it explains taking the case of the pixel P1 and 1, to the pixel P1 and 1. The digital video data 1, 1-1, 1, 1-2, 1, 1-3 and 1, and 1-4 are written in each subframe line period (1st Tsfl, 2nd Tsfl, 3rd Tsfl, and 4th Tsfl), respectively. These digital video datas 1, 1-1, 1, 1-2, 1, 1-3 and 1, and 1-4 are the 2-bit digital video datas which carried out time gradation processing of the 4-bit digital video datas 1 and 1.

[0051]Such operation is performed about all the pixels.

[0052]Here, drawing 7 is referred to. Drawing 7 shows the relation between the gradation voltage level written in a certain pixel (for example, the pixel P1, 1), and a subframe period and a frame period.

[0053]First, if its attention is paid to 1 frame-period eye, the gradation voltage of VL+alpha will be written in the 1st subframe line period (1stTsfl), and the picture corresponding to gradation voltage VL+alpha will be displayed on the 1st subframe period (1st Tsf). Next, the gradation voltage of VL+2alpha is written in the 2nd subframe line period (2nd Tsfl), and the picture corresponding to gradation voltage VL+2alpha is displayed on the 2nd subframe period (2nd Tsf). Next, the gradation voltage of VL+2alpha is written in the 3rd subframe line period (3rd Tsfl), and the picture corresponding to gradation voltage VL+2alpha is displayed on the 3rd subframe period (3rdTsfl). Next, the gradation voltage of VL+2alpha is written in the 4th subframe line period (4th Tsfl), and the picture corresponding to gradation voltage VL+2alpha is displayed on the 4th subframe period (4th Tsf). Therefore, the gradation display level of the 1st frame serves as a gradation display corresponding to the gradation voltage level of VL+7alpha/4.

[0054]Next, if its attention is paid to 2 frame-period eye, the gradation voltage of VL+2alpha will be written in the 1st subframe line period (1stTsfl), and the picture corresponding to gradation voltage VL+2alpha will be displayed on the 1st subframe period (1stTsf). Next, the gradation voltage of VL+2alpha is written in the 2nd subframe line period (2nd Tsfl), and the picture corresponding to gradation voltage VL+2alpha is displayed on the 2nd subframe period (2nd Tsf). Next, the gradation voltage of VL+3alpha is written in the 3rd subframe line period (3rd Tsfl), and the picture corresponding to gradation voltage VL+3alpha is displayed on the 3rd subframe period (3rd Tsf). Next, the gradation voltage of VL+3alpha is written in the 4th subframe line period (4thTsfl), and the picture corresponding to gradation voltage VL+3alpha is displayed on the 4th subframe period (4thTsf). Therefore, the gradation display level of the 2nd frame serves as a gradation display corresponding to the gradation voltage level of VL+10alpha/4.

[0055]Thus, it is understood that 13 kinds of gradation displays are performed.

[0056]In this embodiment, in order to realize the voltage level of 4 gradation, divided mostly between the voltage level VH and voltage-level VLs into equal voltage level, and set the step of the voltage level to alpha, but. Even when between the voltage level VH and voltage-level VLs is not divided into equal voltage level but is set up arbitrarily, there is an effect of this invention.

[0057]The gradation voltage level written in each subframe line period was set up as shown in Table 1, but it may be made for this embodiment to be shown in the following table 2.

[0058]

[Table 2]

デジタルビデオ データアドレス		時間階調処理後 デジタルビデオデータ アドレス (階調電圧) レベル				時間階調を 組み合わせた 階調表示レベル
上位	下位	1st Tsfl	2nd Tsfl	3rd Tsfl	4th Tsfl	
00	00	00 (V_L)	00 (V_L)	00 (V_L)	00 (V_L)	V_L
	01	01 ($V_L + \alpha$)	00 (V_L)	00 (V_L)	00 (V_L)	$V_L + \alpha / 4$
	10	01 ($V_L + \alpha$)	01 ($V_L + \alpha$)	00 (V_L)	00 (V_L)	$V_L + 2\alpha / 4$
	11	01 ($V_L + \alpha$)	01 ($V_L + \alpha$)	01 ($V_L + \alpha$)	00 (V_L)	$V_L + 3\alpha / 4$
01	00	01 ($V_L + \alpha$)	01 ($V_L + \alpha$)	01 ($V_L + \alpha$)	01 ($V_L + \alpha$)	$V_L + \alpha$
	01	10 ($V_L + 2\alpha$)	01 ($V_L + \alpha$)	01 ($V_L + \alpha$)	01 ($V_L + \alpha$)	$V_L + 5\alpha / 4$
	10	10 ($V_L + 2\alpha$)	10 ($V_L + 2\alpha$)	01 ($V_L + \alpha$)	01 ($V_L + \alpha$)	$V_L + 6\alpha / 4$
	11	10 ($V_L + 2\alpha$)	10 ($V_L + 2\alpha$)	10 ($V_L + 2\alpha$)	01 ($V_L + \alpha$)	$V_L + 7\alpha / 4$
10	00	10 ($V_L + 2\alpha$)	10 ($V_L + 2\alpha$)	10 ($V_L + 2\alpha$)	10 ($V_L + 2\alpha$)	$V_L + 2\alpha$
	01	11 ($V_L + 3\alpha$)	10 ($V_L + 2\alpha$)	10 ($V_L + 2\alpha$)	10 ($V_L + 2\alpha$)	$V_L + 9\alpha / 4$
	10	11 ($V_L + 3\alpha$)	11 ($V_L + 3\alpha$)	10 ($V_L + 2\alpha$)	10 ($V_L + 2\alpha$)	$V_L + 10\alpha / 4$
	11	11 ($V_L + 3\alpha$)	11 ($V_L + 3\alpha$)	11 ($V_L + 3\alpha$)	10 ($V_L + 2\alpha$)	$V_L + 11\alpha / 4$
11	00	11 ($V_L + 3\alpha$)	11 ($V_L + 3\alpha$)	11 ($V_L + 3\alpha$)	11 ($V_L + 3\alpha$)	$V_L + 3\alpha$
	01	11 ($V_L + 3\alpha$)	11 ($V_L + 3\alpha$)	11 ($V_L + 3\alpha$)	11 ($V_L + 3\alpha$)	$V_L + 3\alpha$
	10	11 ($V_L + 3\alpha$)	11 ($V_L + 3\alpha$)	11 ($V_L + 3\alpha$)	11 ($V_L + 3\alpha$)	$V_L + 3\alpha$
	11	11 ($V_L + 3\alpha$)	11 ($V_L + 3\alpha$)	11 ($V_L + 3\alpha$)	11 ($V_L + 3\alpha$)	$V_L + 3\alpha$

[0059]The address (or gradation voltage level) of the digital video data written in each subframe line period (1st Tsfl, 2nd Tsfl, 3rd Tsfl, and 4th Tsfl) may be set up also with combination other than Table 1 or table 2.

[0060]In this embodiment, among the 4-bit digital video datas inputted from the outside, the digital video data of 2 bits of higher ranks, It changes into the digital video data for the gradation voltage of 2 bits, and the gradation information of 2 bits of low ranks was expressed by time gradation among 4-bit digital video datas. Here, generally, a top n bit digital video data is changed into the digital video data for gradation voltage for the digital video data of m bit from the exterior by the time gradation processing circuit, and the gradation information of a low rank (m-n) bit considers the case where it is expressed by time gradation. Both m and n are two or more integers, and are taken as $m > n$.

[0061]In this case, the relation between a frame period (T_f) and a subframe period (T_{sf}) serves as

$Tf=2^{m-n}$ and Tsf , and can perform the gradation display of a passage ($2^m - (2^{m-n} - 1)$).

[0062] $m=12$ and $n=4$ may be sufficient.

[0063] (Embodiment 2)

[0064] In this embodiment, the display device into which an 8-bit digital video data is inputted is explained. Drawing 8 is referred to. The outline block diagram of the display device of this embodiment is shown in drawing 8. 801 is a panel which has a digital driver. 801-1 and 801-2 are source drivers, 801-3 is a gate driver, 801-4 is an active matrix circuit where two or more pixels TFT have been arranged at matrix form, and 801-5 is a digital video data time gradation processing circuit.

[0065] The digital video data time gradation processing circuit 801-5 changes a 6-bit digital video data into the digital video data for the gradation voltage of 6 bits among the 8-bit digital video datas inputted from the outside. 2-bit gradation information is expressed by time gradation among 8-bit digital video datas.

[0066] The 6-bit digital video data changed by the digital video data time gradation processing circuit 801-5, it is inputted into the source driver 801-1 and 801-2, and is changed into analog gradation voltage in the D/A conversion circuit (not shown) in a source driver, and each source signal line is supplied. The D/A conversion circuit built in the display device of this embodiment changes a 6-bit digital video data into analog gradation voltage.

[0067] In the display device of this embodiment, the source driver 801-1 and 801-2, the gate driver 801-3, the active matrix circuit 801-4, and the digital video data time gradation processing circuit 801-5 are really formed on the same substrate.

[0068] Here, drawing 9 is referred to. The circuitry of the display device of this embodiment is shown in drawing 9 in more detail. The source driver 801-1 has shift-register-circuit 801-1-1, the latch circuitry 1 (801-1-2), the latch circuitry 2 (801-1-3), and a D/A conversion circuit (801-1-4). In addition, it has a buffer circuit and a level shifter circuit (neither is illustrated). The level shifter circuit is included in expedient top [of explanation], and D/A conversion circuit 801-1-4.

[0069] The source driver 801-2 has the same composition as the source driver 801-1. The source driver 801-1 supplies a picture signal (gradation voltage) to the odd-numbered source signal line, and the source driver 801-2 supplies a picture signal to the even-numbered source signal line.

[0070] In the active matrix type display of this embodiment, provided the two source drivers 801-1 and 801-2 so that the upper and lower sides of an active matrix circuit might be inserted on account of a circuit layout, but. As long as it is possible, it may be made to form only one source driver on a circuit layout.

[0071] 801-3 is a gate driver and has a shift register circuit, a buffer circuit, a level shifter circuit (neither is illustrated), etc.

[0072] The active matrix circuit 801-4 has a pixel of 1920×1080 (horizontal x length). The composition of each pixel is the same as that of what was explained by the above-mentioned Embodiment 1.

[0073] The display device of this embodiment has D/A conversion circuit 801-1-4 treating a 6-bit digital video data. Among the 8-bit digital video datas supplied from the outside, the information for 2 bits of low ranks is used in order to perform time gradation. About time gradation, it is the same as that of above-mentioned Embodiment 1.

[0074] Therefore, the display device of this embodiment can perform the gradation display of $2^8 - 3 = 253$ kind.

[0075] (Embodiment 3)

[0076] In drawing 10, 1001 is a display panel which has an analog driver. 1001-1 is a source driver, 1001-2 and 1001-3 are gate drivers, and 1001-4 is an active matrix circuit where two or more pixels TFT have been arranged at matrix form.

[0077] The digital video data time gradation processing circuit 1002 changes the digital video data of

2 bits of higher ranks into the digital video data for the gradation voltage of 2 bits among the 4-bit digital video datas inputted from the outside. The gradation information of 2 bits of low ranks is expressed by time gradation among 4-bit digital video datas.

[0078]The top 2-bit digital video data changed by the digital video data time gradation processing circuit 1002 is inputted into the D/A conversion circuit 1003, and is changed into an analog video data. It pushes and this analog video data is inputted into the panel 1001.

[0079]Here, the case where used the liquid office for the display panel 1001 of this embodiment as an expression medium, and it is considered as a liquid crystal panel is explained. The circuit circuitry of the display panel 1001 of this embodiment, especially the active matrix circuit 1001-4 are explained using drawing 11.

[0080]The active matrix circuit 1001-4 has a pixel of an individual (xxy). Marks, such as the expedient top of explanation, P1, 1, P2, 1, ..., Py, and x, are attached to each pixel. Each pixel has pixel TFT1001-4-1 and retention volume 1001-4-3. The liquid crystal is inserted between the active matrix substrate and counter substrate in which the source driver 1001-1, the gate driver 1001-2, 1001-3, and the active matrix circuit 1001-4 are formed. Liquid crystal 1001-4-2 shows the liquid crystal corresponding to each pixel typically.

[0081]The analog driver liquid crystal panel of this embodiment performs what is called the dot order following drive that drives one pixel in order. The time taken to write analog gradation voltage in all the pixels (P1, 1 - Py, x) will be called 1 frame period (Tf). The period which quadrisectioned 1 frame period (Tf) will be called a subframe period (Tsf). The time taken to write analog gradation voltage in the pixel for one (for example, P1, 1, P1, 2, ..., P1, x) will be called 1 subframe dot period (Tsfd).

[0082]The gradation display of the display device of this embodiment is explained. The digital video data supplied to the display device of this embodiment from the outside is 4 bits, and has the information on 16 gradation. Since the gradation display level of the display device of this embodiment is the same as that of what was shown in drawing 5, drawing 5 is referred to.

[0083]The drive timing chart of the display device of this embodiment is shown in drawing 12. The pixel P1, 1, P1, 2, P1, 3 and the pixel Py, and x take for an example, and are shown in drawing 12.

[0084]When it explains taking the case of the pixel P1 and 1, to the pixel P1 and 1. The digital video data 1, 1-1, 1, 1-2, 1, 1-3 and 1, and 1-4 are written in each subframe dot period (1st Tsfd, 2nd Tsfd, 3rd Tsfd, and 4th Tsfd). These digital video datas 1, 1-1, 1, 1-2, 1, 1-3 and 1, and 1-4 are the analog video datas which carried out analogue conversion of the 2-bit digital video data which carried out time gradation processing of the 4-bit digital video datas 1 and 1.

[0085]Such operation is performed about all the pixels.

[0086]Therefore, also in the display device of this embodiment, the gradation display of 13 gradation can be performed like above-mentioned Embodiment 1.

[0087]What is necessary is to carry out digital video data conversion of the analog video data inputted, and just to make it input into the digital video data time gradation processing circuit 1002, when an analog video data is inputted into the display device of this embodiment from the exterior.

[0088]Generally also in this embodiment, the digital video data of m bit from the exterior by a time gradation processing circuit. A top n bit digital video data is changed into the digital video data for gradation voltage, and the gradation information of a low rank (m-n) bit considers the case where it is expressed by time gradation. Both m and n are two or more integers, and are taken as $m > n$.

[0089]In this case, the relation between a frame period (Tf) and a subframe period (Tsf) serves as $Tf = 2^{m-n}$ and Tsf, and can perform the gradation display of a passage ($2^m - (2^{m-n} - 1)$).

[0090](Embodiment 4)

[0091]This embodiment explains below the example of a making process of the display device (or liquid crystal panel) of this invention explained by above-mentioned Embodiments 1-3. This embodiment shows the example which forms two or more TFT(s) on the substrate which has an insulation surface, and forms an active matrix circuit, a source driver, a gate driver, other peripheral circuits, etc. on the same board to drawing 13 - drawing 16. The following examples show signs that

the one pixel TFT of an active matrix circuit and the CMOS circuit which is basic circuits of other circuits (a source driver, a gate driver, and other peripheral circuits) are formed simultaneously. Although the following examples explain the making process about the case where P channel type TFT and N channel type TFT are provided with one gate electrode in the CMOS circuit, respectively, The CMOS circuit by TFT provided with two or more gate electrodes like a double-gate mold or a triple gate type is producible similarly. In the following examples, the pixel TFT is good also as TFT(s), such as a single gate, a triple gate, etc. which are N channel type TFT of DABURUGEITO. It may be made to form simultaneously a digital video data time gradation processing circuit like the display device of the above-mentioned Embodiment 2.

[0092]Drawing 13 (A) is referred to. First, the quartz substrate 5000 is prepared as a substrate which has an insulation surface. The silicon substrate which formed the oxidizing film instead of the quartz substrate can also be used. It is very good in a method which once forms an amorphous silicon film on a quartz substrate, oxidizes it thermally thoroughly, and is used as an insulator layer. The quartz substrate, the ceramic board, or the silicon substrate in which the silicon nitride film was formed may be used as an insulator layer. Next, the ground film 5001 is formed. According to this embodiment, silicon oxide (SiO_2) was used for the ground film 5001. Next, the amorphous silicon film 5003 is formed. The amorphous silicon film 5003 is adjusted so that final thickness (thickness in consideration of the film decrease after thermal oxidation) may be set to 10–75 nm (preferably 15–45 nm).

[0093]It is important to manage the impurity concentration in a film thoroughly when forming the amorphous silicon film 5003. In the case of this embodiment, in the amorphous silicon film 5003, Each concentration of C (carbon) and N (nitrogen) which are the impurities which check next crystallization is less than 5×10^{18} atoms/cm³ (below 5×10^{17} atoms/cm³ typically.). Preferably, below 2×10^{17} atoms/cm³ manages O (oxygen) so that less than 1.5×10^{19} atoms/cm³ (typically below 1×10^{18} atoms/cm³ preferably below 5×10^{17} atoms/cm³) may become. It is because it will become the cause of having an adverse effect in the case of next crystallization, and reducing the membraneous quality after crystallization if each impurity exists by the concentration beyond this. The above-mentioned impurity element concentration in a film is defined [be / it / under / this / Description / setting] by the minimum in the measurement result of SIMS (secondary mass ion analysis).

[0094]As for the decompression heat CVD furnace used by this embodiment, in order to obtain the above-mentioned composition, it is desirable to perform dry cleaning periodically and to attain defecation of a membrane formation room. Dry cleaning passes the ClF_3 (chlorine fluoride) gas of 100 – 300sccm in the furnace heated at about 200–400 **, and should just clean a membrane formation room with the fluoride generated by the pyrolysis.

[0095]When according to these people's knowledge it is considered as the degree of furnace temperature of 300 ** and the flow of ClF_3 gas is set to 300sccm, the affix (the main ingredients of the silicon are mainly carried out) of about 2–micrometer thickness can be removed thoroughly in 4 hours.

[0096]It seems that the hydrogen concentration in the amorphous silicon film 5003 is also a very important parameter, and the film it is [crystallinity] better to stop a hydrogen content low is obtained. Therefore, as for membrane formation of the amorphous silicon film 5003, it is preferred that it is a decompression heat CVD method. It is also possible to use plasma CVD method by optimizing a film formation condition.

[0097]Next, the crystallization stage of the amorphous silicon film 5003 is performed. Technology given in JP,H7–130652,A is used as a means of crystallization. Although which means of the working example 1 of the gazette and Embodiment 2 may be used, in this embodiment, it is preferred to use the technical contents (detailed to JP,H8–78329,A) indicated in the working example 2 of the gazette.

[0098]Technology given in JP,H8-78329,A forms in 150 nm the mask insulator layer 4004 which chooses the addition field of a catalyst element first. The mask insulator layer 4004 has two or more openings, in order to add a catalyst element. The position of this opening can determine the position of a crystalline region (drawing 13 (B)).

[0099]And the solution (nickel acetate ethanol solution) 5005 which contained nickel (nickel) as a catalyst element which promotes crystallization of the amorphous silicon film 5003 is applied with a spin coat method. As a catalyst element, cobalt (Co), iron (Fe), palladium (Pd), germanium (germanium), platinum (Pt), copper (Cu), gold (Au), etc. can be used besides nickel (drawing 13 (B)).

[0100]The ion implantation or the plasma doping method for having used the resist mask can also be used for the addition process of the above-mentioned catalyst element. In this case, since reduction of the occupation area of an addition field and control of the growth distance of the lateral growth region mentioned later become easy, it becomes effective technology when the miniaturized bottom constitutes a circuit.

[0101]If the addition process of a catalyst element is completed next, into after hydrogen **** of about 1 hour, an inert atmosphere, a hydrogen atmosphere, or oxygen environment, heat-treatment of 4 to 24 hours will be added at 450 ** at the temperature of 500-960 ** (typically 550-650 **), and the amorphous silicon film 5003 will be crystallized. At this embodiment, a nitrogen atmosphere performs heat-treatment of 14 hours at 570 **.

[0102]At this time, crystallization of the amorphous silicon film 5003 advances preferentially from the core generated in the field 4006 which added nickel, and the crystalline region 5007 which consists of a polycrystalline silicon film grown-up almost in parallel to the substrate face of the substrate 5000 is formed. This crystalline region 5007 is called a lateral growth region. Since each crystals have gathered in the state where it gathered comparatively, a lateral growth region has the advantage of excelling in overall crystallinity.

[0103]nickel acetic acid solution can be applied to the front face of an amorphous silicon film, and it can also be made to crystallize without using the mask insulator layer 5004.

[0104]Drawing 13 (D) is referred to. Next, the gettering process of a catalyst element is performed. First, phosphorous ion is doped selectively. A phosphorus is doped where the mask insulator layer 5004 is formed. Then, a phosphorus is doped by only the portion 5008 which is not covered with the mask insulator layer 5004 of the polycrystalline silicon film (the field of these is called the phosphorus addition field 5008). The accelerating voltage of doping and the thickness of the mask which changes with an oxide film are optimized, and a phosphorus is kept from running through the mask insulator layer 5004 at this time. Although this mask insulator layer 5004 may not necessarily be an oxide film, since an oxide film does not cause contamination even if it touches an active layer directly, it is convenient.

[0105]The dose of a phosphorus is good to consider it as a 1×10^{15} from 1×10^{14} ions/cm² grade.

According to this embodiment, the dose of 5×10^{14} ions/cm² was performed using ion doping equipment.

[0106]Accelerating voltage in the case of an ion dope was set to 10keV. If it is the accelerating voltage of 10keV, the phosphorus can hardly pass a 150-nm mask insulator layer.

[0107]Drawing 13 (E) is referred to. Next, thermal annealing was carried out in a 600 ** nitrogen atmosphere for 1 to 12 hours (this embodiment 12 hours), and gettering of the nickel element was performed. By carrying out like this, as drawing 13 (E) is shown by the arrow, nickel will be drawn close by the phosphorus. Although a phosphorus atom hardly moves under 600 ** temperature in a film, the nickel atom can move about several 100 micrometers or the distance beyond it. He can understand from this that a phosphorus is one of the elements which fitted the gettering of nickel most.

[0108]Next, the process of patterning a polycrystalline silicon film is explained with reference to drawing 14 (A). The addition field 5008 of a phosphorus, i.e., the field where gettering of the nickel

was carried out, is kept from remaining at this time. Thus, the active layers 5009-5011 of the polycrystalline silicon film which hardly contains a nickel element were obtained. The active layers 5009-5011 of the obtained polycrystalline silicon film turn into an active layer of TFT behind.

[0109]Drawing 14 (B) is referred to. If the active layers 5009-5011 are formed, the gate dielectric film 5012 which comes on it with the insulator layer containing silicon will be formed to 70 nm. And in an oxidizing atmosphere, it heat-treats at 800-1100 ** (preferably 950-1050 **), and an oxidizing film (not shown) is formed in the interface of the active layers 5009-5011 and the gate dielectric film 5012.

[0110]Heat-treatment (gettering process of a catalyst element) for carrying out gettering of the catalyst element may be performed in this stage. In that case, heat-treatment includes a halogen in a treatment atmosphere, and uses the gettering effect of the catalyst element by a halogen. In order to fully acquire the gettering effect by a halogen, it is preferred to perform the above-mentioned heat-treatment at the temperature over 700 **. Below at this temperature, disassembly of the halogenated compound in a treatment atmosphere becomes difficult, and there is a possibility that a gettering effect may no longer be acquired. A kind or two or more sorts of things chosen from the compound which contains halogen, such as HCl, HF, NF₃, HBr, Cl₂, ClF₃, BCl₂, F₂, and Br₂, typically can be used as gas which contains a halogen in this case. In this process, when HCl is used, for example, gettering is carried out by operation of chlorine, and nickel in an active layer turns into volatile nickel chloride, and is considered to be broken away and removed into the atmosphere. When performing the gettering process of a catalyst element using a halogen, after removing the mask insulator layer 5004 for the gettering process of a catalyst element, it may carry out, before carrying out the patterning of the active layer. The gettering process of a catalyst element may be performed after carrying out the patterning of the active layer. It may carry out combining which gettering process.

[0111]Next, the metal membrane which uses as the main ingredients the aluminum which is not illustrated is formed, and the prototype of a next gate electrode is formed by patterning. In this embodiment, the aluminum film containing 2wt% of a scandium is used.

[0112]A gate electrode may be formed with the polycrystalline silicon film which added the impurity for giving conductivity.

[0113]Next, the porous anode oxide films 5013-5020, the imperforation oxide films on anode 5021-5024, and the gate electrodes 5025-5028 are formed by technology given in JP,H7-135318,A (drawing 14 (B)).

[0114]In this way, if the state of drawing 14 (B) is acquired, the gate dielectric film 5012 will be etched next by using the gate electrodes 5025-5028 and the porous anode oxide films 5013-5020 as a mask. And the porous anode oxide films 5013-5020 are removed, and the state of drawing 14 (C) is acquired. It is gate dielectric film after processing that drawing 14 (C) is shown by 5029-5031.

[0115]Drawing 15 (A) is referred to. Next, the addition process of the impurity element which gives 1 conductivity is performed. What is necessary is just to use B (boron) or Ga (gallium), if it is an N channel type as an impurity element and is P (phosphorus) or As (arsenic), and P type.

[0116]According to this embodiment, the impurity addition for forming N channel type and P channel type TFT is divided into 2 times of processes, respectively, and is performed.

[0117]First, impurity addition for forming N channel type TFT is performed. First, 1st impurity addition (P (phosphorus) is used in this embodiment) is performed with about 80 keV of high acceleration voltages, and an n⁻ field is formed. This n⁻ field is adjusted so that P ion concentration may become 1x10¹⁸atoms/cm³ - 1x10¹⁹atoms/cm³.

[0118]2nd impurity addition is performed with about 10 keV of low acceleration voltage, and an n⁺ field is formed. Since accelerating voltage is low at this time, gate dielectric film functions as a mask. This n⁺ field is adjusted so that sheet resistance may be set to 500ohms or less (preferably 300ohms or less).

[0119]The source region of N channel type TFT and the drain areas 5033 and 5033, the low concentration impurity region 5037, and the channel forming region 5040 which constitute a CMOS circuit are formed through the above process. The source region of N channel type TFT and the drain areas 5035 and 5036, the low concentration impurity regions 5038 and 5039, and the channel forming regions 5041 and 5042 which constitute the pixel TFT are decided (drawing 15 (A)).

[0120]The active layer of P channel type TFT which constitutes a CMOS circuit from a state which shows in drawing 15 (A) has the same composition as the active layer of N channel type TFT.

[0121]Next, as shown in drawing 15 (B), N channel type TFT is covered, the resist mask 5043 is formed, and the impurity ion (boron is used in this embodiment) which gives P type is added.

[0122]Although this process as well as the above-mentioned impurity addition process is performed in 2 steps, in order to make a P channel type reverse an N channel type, B (boron) ion of the concentration which is about several times the addition concentration of the above-mentioned P ion is added.

[0123]In this way, the source region of P channel type TFT and the drain areas 5044 and 5045, the low concentration impurity region 5046, and the channel forming region 5047 which constitute a CMOS circuit are formed (drawing 15 (B)).

[0124]What is necessary is just to use a publicly known sidewall structure for formation of a low concentration impurity, when a gate electrode is formed with the polycrystalline silicon film which added the impurity for giving conductivity.

[0125]Next, impurity ion is activated with combination, such as a furnace annealing, laser annealing, and lamp annealing. The damage to an active layer received at the addition process simultaneously with it is also restored.

[0126]Drawing 15 (C) is referred to. Next, after forming the cascade screen of a silicon oxide film and a silicon nitride film as the 1st interlayer insulation film 5048 and forming a contact hole, a source electrode and the drain electrodes 5049-5053 are formed. An organic nature resin layer can also be used as the 1st interlayer insulation film 5048.

[0127]Drawing 16 is referred to. Next, the 2nd interlayer insulation film 5054 is formed with a silicon nitride film. And next, the 3rd interlayer insulation film 5056 that consists of an organic nature resin layer is formed in a thickness of 0.5-3 micrometers. Polyimide, an acrylic, polyimidoamide, etc. are used as an organic nature resin layer. Since the point for a method for film deposition that the advantage of an organic nature resin layer is simple, the point which can thicken thickness easily, and specific inductive capacity are low, the point that parasitic capacitance can be reduced, a point excellent in surface smoothness, etc. are mentioned. The organic nature resin layer except having mentioned above can also be used.

[0128]Next, a part of 3rd interlayer insulation film 5056 is etched, and the black matrix 5055 is formed in the upper part of the drain electrode 5052 of the pixel TFT on both sides of the 2nd interlayer insulation film. According to this embodiment, Ti (titanium) was used for the black matrix 5055. In this embodiment, retention volume is formed between the pixel TFT and a black matrix.

[0129]Next, a contact hole is formed in the 2nd interlayer insulation film 5054 and the 3rd interlayer insulation film 5056, and the picture element electrode 5057 is formed in a thickness of 120 nm. Since this embodiment is an example of a transmission type active matrix display device, it uses transparent conducting films, such as ITO, as a conducting film which constitutes the picture element electrode 5057.

[0130]Next, the whole substrate is heated by a 350 °C hydrogen atmosphere for 1 to 2 hours, and the dangling bond (azygos joint hand) in a film (especially inside of an active layer) is compensated with hydrogenating the whole element. This hydrogen treatment may be performed from the hydrogen made by making it plasma-ize.

[0131]The active matrix substrate which has a CMOS circuit and a picture-element-matrix circuit on the same substrate through the above process is completed.

[0132]Next, the process of producing an active matrix type display is explained based on the active

matrix substrate produced by the above-mentioned process.

[0133]The orienting film 5059 is formed in the active matrix substrate of the state of drawing 16 (C). According to this embodiment, polyimide was used for the orienting film 5059. Next, a counter substrate is prepared. A counter substrate comprises the counterelectrode 5061 and the orienting film 5062 which comprise the glass substrate 5060 and a transparent conducting film.

[0134]The polyimide film was used for the orienting film in this embodiment. Rubbing treatment was performed after orienting film formation. In this embodiment, polyimide which has a comparatively big pre chill angle in an orienting film was used.

[0135]Next, the active matrix substrate and counter substrate which passed through the above-mentioned process are pasted together via a sealant, a spacer (not shown [both]), etc. by a publicly known cell **** process. Then, the liquid crystal 5063 is poured in among both boards, and it closes thoroughly with encapsulant (not shown). According to this embodiment, the nematic liquid crystal was used for the liquid crystal 5063.

[0136]Therefore, a transmission type active matrix type display as shown in drawing 16 (C) is completed.

[0137]An amorphous silicon film may be crystallized by a laser beam (typically excimer laser beam) instead of the method of crystallization of the amorphous silicon film explained by this embodiment.

[0138]Instead of using a polycrystalline silicon film, the SOI structure (SOI substrate) of a smart cut, SIMOX, EI Tran, etc. may be used, and other processes may be performed.

[0139](Embodiment 5)

[0140]This embodiment explains another manufacturing method of the display device of this invention. Here, how to produce simultaneously TFT of an active matrix circuit and the drive circuit provided around it is explained.

[0141][Process:drawing 17 (A) of an island like semiconductor layer and gate-dielectric-film formation] In drawing 17 (A), it is desirable to use an alkali-free-glass board and a quartz substrate for the substrate 7001. In addition, it is good also considering the thing in which the insulator layer was formed on the surface of a silicon substrate or a metallic base, as a substrate.

[0142]And the ground film 7002 which consists of a silicon oxide film, a silicon nitride film, or a nitriding silicon oxide film was formed in the surface in which TFT of the substrate 7001 is formed by plasma CVD method or a sputtering method at a thickness of 100–400 nm. For example, as the ground film 7002, it is good to form the silicon nitride film 7002 with the two-layer structure which set the silicon oxide film 7003 to 50–300 nm 25–100 nm and here, and was made into a thickness of 150 nm here at a thickness of 50 nm. The ground film 7002 is formed in order to prevent the impurity contamination from a substrate, and when a quartz substrate is used, it is not necessary to necessarily provide it.

[0143]Next, the 20–100-nm-thick amorphous silicon film was formed by the publicly known forming-membranes method on the ground film 7002. Although an amorphous silicon film is based also on a water content quantum, it is desirable to heat at 400–550 ** preferably for several hours, to perform dehydrogenation treatment, to make a water content quantum less than 5atom%, and to perform the process of crystallization. Although an amorphous silicon film may be formed with other manufacturing methods, such as a sputtering method and vacuum deposition, it is desirable to reduce enough impurity elements contained in a film, such as oxygen and nitrogen. Here, since a ground film and an amorphous silicon film can be formed by the same forming-membranes method, they may carry out continuously forming of both. After forming a ground film, by making it not once exposed to atmospheric air, it can become possible to prevent surface contamination and the characteristic variation of TFT produced can be reduced.

[0144]Publicly known laser crystallization technology or the technology of thermal crystallization should just be used for the process of forming a crystalline silicon film from an amorphous silicon film. A crystalline silicon film may be produced by the method of thermal crystallization using the catalyst element which promotes crystallization of silicon. In addition, a microcrystal silicon film may

be used and deposition membrane formation of the crystalline silicon film may be carried out directly. A crystalline silicon film may be formed using the known art of SOI (SiliconOn Insulators) which pastes single crystal silicon together on a substrate.

[0145]In this way, etching removal of the unnecessary portion of the formed crystalline silicon film was carried out, and the island like semiconductor layers 7004–7006 were formed. In the field to which n channel type TFT of a crystalline silicon film is produced, in order to control threshold voltage, boron (B) may be beforehand added by the concentration about $1 \times 10^{15} - 5 \times 10^{17} \text{ cm}^{-3}$.

[0146]Next, the island like semiconductor layers 7004–7006 were covered, and the gate dielectric film 7007 which uses silicon oxide or silicon nitride as the main ingredients was formed. What is necessary is just to form preferably 10–200 nm of gate dielectric film 7007 in a thickness of 50–150 nm. For example, it is good also as 115-nm gate dielectric film to form 75 nm of nitriding silicon oxide films which used N_2O and SiH_4 as the raw material with plasma CVD method, and oxidize thermally at 800–1000 ** among oxygen environment or the mixed atmosphere of oxygen and chloride after that. (Drawing 17 (A))

[0147][-- formation [of an n^- field]: -- drawing 17 (B)] -- with the whole surface of the field which forms the island like semiconductor layers 7004 and 7006 and wiring. The resist masks 7008–7011 were formed in a part of island like semiconductor layer 7005 (the field used as a channel forming region is included), the impurity element which gives a n type was added and the low concentration impurity region 7012 was formed. The LDD region where this low concentration impurity region 7012 laps with a gate electrode via gate dielectric film at n channel type TFT of a CMOS circuit behind (in this Description, it is called a Lov field.) It is a meaning of overlap in ov. It is an impurity range for forming. Suppose that the concentration of the impurity element which gives the n type contained in the low concentration impurity region formed here is expressed with (n^-). Therefore, in this Description, the low concentration impurity region 7012 can be put in another way as an n^- field.

[0148]Here, the phosphorus was added by the ion doping method which carried out plasma excitation without carrying out mass separation of the phosphoretted hydrogen (PH_3). Of course, the ion implantation method for performing mass separation may be used. In this process, the phosphorus was added to the semiconductor layer under it through the gate dielectric film 7007. As for the phosphorus concentration to add, it was preferred to use the range of $5 \times 10^{17} - 5 \times 10^{18} \text{ atoms/cm}^3$, and it made it $1 \times 10^{18} \text{ atoms/cm}^3$ here.

[0149]Then, the resist masks 7008–7011 were removed, in a nitrogen atmosphere, heat treatment of 1 to 12 hours was preferably performed at 550–800 **, and 400–900 ** of processes of activating the phosphorus added at this process were performed.

[0150][-- formation [of the object for gate electrodes, and the conducting film for wiring]: -- drawing 17 (C)] -- the element or either which was chosen from tantalum (Ta), titanium (Ti), molybdenum (Mo), and tungsten (W) in the 1st conducting film 7013 was formed in a thickness of 10–100 nm with the conductive material used as the main ingredients. As the 1st conducting film 7013, it is desirable to use tantalum nitride (TaN) and tungsten nitride (WN), for example. The element or either which was chosen from Ta, Ti, Mo, and W in the 2nd conducting film 7014 on the 1st conducting film 7013 was formed in a thickness of 100–400 nm with the conductive material used as the main ingredients. For example, what is necessary is just to form Ta in a thickness of 200 nm. Although not illustrated, it is effective to form a silicone film by a thickness of about 2–20 nm under the 1st conducting film 7013 for antioxidizing of the conducting films 7013 and 7014 (especially conducting film 7014).

[0151][Formation: drawing 18 (A) of formation of a p-ch gate electrode and a wiring electrode, and a p^+ field] Form the resist masks 7015–7018 and the 1st conducting film and 2nd conducting film (it is hereafter dealt with as a cascade screen) are etched, The gate electrode 7019 of p channel type

TFT and the gate wires 7020 and 7021 were formed. On the field used as n channel type TFT, it left the conducting films 7022 and 7023 so that the whole surface might be covered.

[0152]And it left the resist masks 7015-7018 as they were, and was considered as the mask, and the process of adding the impurity element which gives a p type to a part of semiconductor layer 7004 in which p channel type TFT is formed was performed. Here, it added by using boron as the impurity element using diborane (B_2H_6) by the ion doping method (of course, the ion implantation

method may be used). Here, boron was added to the concentration of $5 \times 10^{20} - 3 \times 10^{21}$ atoms/cm³. Suppose that the concentration of the impurity element which gives the p type contained in the impurity range formed here is expressed with (p^{++}). Therefore, in this Description, the impurity ranges 7024 and 7025 can be put in another way as a p^{++} field.

[0153]In this process, after carrying out etching removal of the gate dielectric film 7007 using the resist masks 7015-7018 and exposing a part of island like semiconductor layer 7004, the process of adding the impurity element which gives a p type may be performed. In that case, since accelerating voltage is low and ends, there are few damages given to island-shape semiconductor membrane, and a throughput also improves.

[0154][-- formation [of a n-ch gate electrode]: -- drawing 18 (B)] -- next, after removing the resist masks 7015-7018, they formed the resist masks 7026-7029, and formed the gate electrodes 7030 and 7031 of n channel type TFT. At this time, the gate electrode 7030 was formed so that it might lap with the n^- field 7012 via gate dielectric film.

[0155][-- formation [of an n^+ field]: -- drawing 18 (C)] -- next, the resist masks 7026-7029 were removed and the resist masks 7032-7034 were formed. And in n channel type TFT, the process of forming the impurity range which functions as the source region or a drain area was performed. The resist mask 7034 formed the gate electrode 7031 of n channel type TFT with the wrap form. This is for forming an LDD region so that it may not lap with a gate electrode in a next process at n channel type TFT of a picture-element-matrix circuit.

[0156]And the impurity element which gives a n type was added and the impurity ranges 7035-7039 were formed. Here, it carried out by the ion doping method (of course, the ion implantation method may be used) for having used phosphoretted hydrogen (PH_3), and concentration of the phosphorus of this field was made into $1 \times 10^{20} - 1 \times 10^{21}$ atoms/cm³. Suppose that the concentration of the impurity element which gives the n type contained in the impurity ranges 7037-7039 formed here is expressed with (n^+). Therefore, in this Description, the impurity ranges 7037-7039 can be put in another way as an n^+ field. Since the n^- field was already formed, the impurity ranges 7035 and 7036 contain a phosphorus strictly by concentration a little higher than the impurity ranges 7037-7039.

[0157]In this process, after etching the gate dielectric film 7007 by having used the resist masks 7032-7034 and the gate electrode 7030 as the mask and exposing a part of island-shape semiconductor membrane 7005 and 7006, the process of adding the impurity element which gives a n type may be performed. In that case, since accelerating voltage is low and ends, there are few damages given to island-shape semiconductor membrane, and a throughput also improves.

[0158][-- n^- formation [of field]: -- drawing 19 (A)] -- next, the resist masks 7032-7034 were removed and the process of adding the impurity element which gives a n type to the island like semiconductor layer 7006 used as n channel type TFT of a picture-element-matrix circuit was performed. In this way, comparable as said n^- field in the formed impurity ranges 7040-7043 or the phosphorus of concentration (specifically $5 \times 10^{16} - 1 \times 10^{18}$ atoms/cm³) less than it was added. Suppose that the concentration of the impurity element which gives the n type contained in the impurity ranges 7040-7043 formed here is expressed with (n^{--}). Therefore, in this Description, they

are the impurity ranges 7040–7043 n⁺ It can be put in another way as field. Although the phosphorus is added by all the impurity ranges by the concentration of n⁺ except for the impurity range 7067 hidden with the gate electrode in this process, since it is very low concentration, it does not ignore and interfere.

[0159][-- process [of thermal activation]: -- drawing 19 (B)] -- next, the supplementary insulation film 7044 which turns into a part of 1st interlayer insulation film was formed in behind. What is necessary is just to form the supplementary insulation film 7044 by the cascade screen which combined a silicon nitride film, a silicon oxide film, a nitriding silicon oxide film, or them. The thickness is just 100–400 nm.

[0160]Then, in order to activate the impurity element which gives the n type or p type added by each concentration, the heat treatment process was performed. This process can be performed by the furnace annealing method, the laser annealing method, or the rapid thermal annealing method (the RTA method). Here, the activation process was performed by the furnace annealing method. Into a nitrogen atmosphere, heat-treatment performed 300–650 °C of 450 °C and heat treatments of 2 hours preferably 400–550 °C and here.

[0161]In the atmosphere containing 3 to 100% of hydrogen, heat treatment of 1 to 12 hours was performed at 300–450 °C, and the process of hydrogenating an island like semiconductor layer was performed. This process is a process of carrying out the termination of the dangling bond of a semiconductor layer by the hydrogen excited thermally. As other means of hydrogenation, plasma hydrogenation (the hydrogen excited by plasma is used) may be performed.

[0162][Formation:drawing 19 (C) of an interlayer insulation film, a source/drain electrode, a light-shielding film, a picture element electrode, and retention volume] When finishing the activation process, the interlayer insulation film 7045 of 0.5 – 1.5-micrometer thickness was formed on the supplementary insulation film 7044. The cascade screen which becomes with said supplementary insulation film 7044 and the interlayer insulation film 7045 was used as the 1st interlayer insulation film.

[0163]Then, the contact hole which arrives at the source region or the drain area of each TFT was formed, and the source electrodes 7046–7048 and the drain electrodes 7049 and 7050 were formed. Although not illustrated, in this embodiment, it was considered as the cascade screen of the three-tiered structure which formed continuously 300 nm of aluminum films which contain [this electrode] 100 nm and Ti for a Ti film, and 150 nm of Ti films by the sputtering method.

[0164]Next, it formed as the passivation film 7051 by a thickness of 50–500 nm (typically 200–300 nm) with the silicon nitride film, the silicon oxide film, or the nitriding silicon oxide film. Then, when hydrogen treatment was performed in this state, the desirable result was obtained the improvement [for] in the characteristic of TFT. For example, the same effect was acquired, even if it was good to have performed heat treatment of 1 to 12 hours at 300–450 °C or it used the plasma hydrogenating method in the atmosphere containing 3 to 100% of hydrogen. An opening may be formed in the passivation film 7051 in the position which forms the contact hole for connecting a picture element electrode and a drain electrode behind here.

[0165]Then, the 2nd interlayer insulation film 7052 that consists of organic resin was formed in a thickness of about 1 micrometer. As organic resin, polyimide, an acrylic, polyamide, polyimidoamide, BCB (benz-cyclo-butene), etc. can be used. The point for a method for film deposition that the advantage of using an organic resin film is simple, the point that parasitic capacitance can be reduced since specific inductive capacity is low, the point of excelling in surface smoothness, etc. are got. An organic resin film, an organic system SiO compound, etc. except having mentioned above can also be used. Here, it calcinated and formed at 300 °C after applying to a substrate using polyimide of the type which carries out thermal polymerization.

[0166]Next, in the field used as a picture-element-matrix circuit, the light-shielding film 7053 was formed on the 2nd interlayer insulation film 7052. The light-shielding film 7053 formed in a thickness

of 100–300 nm the element or either which was chosen from aluminum (aluminum), titanium (Ti), and tantalum (Ta) by the film used as the main ingredients. And the 30–150 nm (preferably 50–75 nm)–thick oxide film 7054 was formed in the surface of the light-shielding film 7053 by the anode oxidation method or the plasma oxidation method. Here, the aluminum oxide film (alumina membrane) was used as the oxide film 7054 using the film which uses an aluminum film or aluminum as the main ingredients as the light-shielding film 7053.

[0167]Although it had composition which provides an insulator layer only in the light-shielding film surface here, an insulator layer may be formed by gaseous phase methods, such as plasma CVD method, a heat CVD method, or a sputtering method. It is preferred that thickness sets to 30–150 nm (preferably 50–75 nm) also in that case. A silicon oxide film, a silicon nitride film, a nitriding silicon oxide film, a DLC (Diamond like carbon) film, or an organic resin film may be used. The cascade screen which combined these may be used.

[0168]Next, the contact hole which reaches the drain electrode 7050 was formed in the 2nd interlayer insulation film 7052, and the picture element electrode 7055 was formed. The picture element electrodes 7056 and 7057 are picture element electrodes of another pixel which adjoins, respectively. A metal membrane should just be used for the picture element electrodes 7055–7057 when making it into a reflection type liquid crystal display using a transparent conducting film, in making it into a transmission type liquid crystal display. Here, in order to consider it as a transmission type liquid crystal display, the indium–tin–oxide (ITO) film was formed in a thickness of 100 nm by the sputtering method.

[0169]At this time, the field 7058 with which the picture element electrode 7055 and the light-shielding film 7053 lapped via the oxide film 7054 formed retention volume.

[0170]In this way, on the same substrate, the active matrix substrate with the CMOS circuit and picture-element-matrix circuit used as a driver line was completed. P channel type TFT7081 and n channel type TFT7082 were formed in the CMOS circuit used as a driver line, and pixel TFT7083 which becomes by n channel type TFT was formed in the picture-element-matrix circuit.

[0171]The channel forming region 7061, the source region 7062, and the drain area 7063 were formed in p channel type TFT7081 of a CMOS circuit in the p^+ field, respectively. The LDD region which lapped with the gate electrode via the channel forming region 7064, the source region 7065, the drain area 7066, and gate dielectric film in n channel type TFT7082 (henceforth a Lov field) It is the mind of overlap in ov. 7067 was formed. At this time, the source region 7065 and the drain area 7066 were formed in the field, respectively ($n^- + n^+$), and the Lov field 7067 was formed in the n^- field.

[0172]The LDD region which does not lap with a gate electrode via the channel forming regions 7068 and 7069, the source region 7070, the drain area 7071, and gate dielectric film in pixel TFT7083 (henceforth a Loff field) off is the mind of offset. The n^+ field 7076 adjacent to 7072–7075, and the Loff fields 7073 and 7074 was formed. At this time, it is formed in an n^+ field, respectively and, in the Loff fields 7072–7075, the source region 7070 and the drain area 7071 are n^- It was formed in field.

[0173]Here, the structure of TFT which forms each circuit according to the circuit specifications which **, a picture-element-matrix circuit, and a driver line require was able to be optimized, and the performance of operation and reliability of the semiconductor device were able to be raised. Specifically, n channel type TFT realized TFT structure which thought as important high-speed operation or the measure against hot carriers on the same board, and TFT structure which thought low OFF state current operation as important by changing arrangement of an LDD region according to circuit specifications, and using a Lov field or a Loff field properly.

[0174]For example, in the case of the active matrix type liquid crystal display device, n channel type TFT7082 is suitable for logical circuits which think high-speed operation as important, such as a shift register circuit, a subharmonics circuit, a signal dividing network, a level shifter circuit, and a

buffer circuit. N channel type TFT7083 is suitable for the picture-element-matrix circuit and sampling circuit (sample hold circuit) which thought low OFF state current operation as important. [0175]What is necessary is for 0.5–3.0 micrometers of the length (width) of a Lov field just to be 1.0–1.5 micrometers typically to 3–7 micrometers of channel length. What is necessary is for 0.5–3.5 micrometers of the length (width) of the Loff fields 7072–7075 established in pixel TFT7083 just to be 2.0–2.5 micrometers typically.

[0176](Embodiment 6)

[0177]This embodiment explains another manufacturing method of the liquid crystal display of this invention. Here, how to produce simultaneously TFT of an active matrix circuit and the drive circuit provided around it is explained.

[0178][Process:drawing 20 (A) of an island like semiconductor layer and gate-dielectric-film formation] In drawing 20 (A), it is desirable to use an alkali-free-glass board and a quartz substrate for the substrate 6001. In addition, it is good also considering the thing in which the insulator layer was formed on the surface of a silicon substrate or a metallic base, as a substrate.

[0179]And the ground film 6002 which consists of a silicon oxide film, a silicon nitride film, or a nitriding silicon oxide film was formed in the surface in which TFT of the substrate 6001 is formed by plasma CVD method or a sputtering method at a thickness of 100–400 nm. For example, as the ground film 6002, it is good to form the silicon nitride film 6002 with the two-layer structure which set the silicon oxide film 6003 to 50–300 nm 25–100 nm and here, and was made into a thickness of 150 nm here at a thickness of 50 nm. The ground film 6002 is formed in order to prevent the impurity contamination from a substrate, and when a quartz substrate is used, it is not necessary to necessarily provide it.

[0180]Next, the 20–100-nm-thick amorphous silicon film was formed by the publicly known forming-membranes method on the ground film 6002. Although an amorphous silicon film is based also on a water content quantum, it is desirable to heat at 400–550 °C preferably for several hours, to perform dehydrogenation treatment, to make a water content quantum less than 5atom%, and to perform the process of crystallization. Although an amorphous silicon film may be formed with other manufacturing methods, such as a sputtering method and vacuum deposition, it is desirable to reduce enough impurity elements contained in a film, such as oxygen and nitrogen. Here, since a ground film and an amorphous silicon film can be formed by the same forming-membranes method, they may carry out continuously forming of both. After forming a ground film, by making it not once exposed to atmospheric air, it can become possible to prevent surface contamination and the characteristic variation of TFT produced can be reduced.

[0181]Publicly known laser crystallization technology or the technology of thermal crystallization should just be used for the process of forming a crystalline silicon film from an amorphous silicon film. A crystalline silicon film may be produced by the method of thermal crystallization using the catalyst element which promotes crystallization of silicon. In addition, a microcrystal silicon film may be used and deposition membrane formation of the crystalline silicon film may be carried out directly. A crystalline silicon film may be formed using the known art of SOI (SiliconOn Insulators) which pastes single crystal silicon together on a substrate.

[0182]In this way, etching removal of the unnecessary portion of the formed crystalline silicon film was carried out, and the island like semiconductor layers 6004–6006 were formed. In the field to which n channel type TFT of a crystalline silicon film is produced, in order to control threshold voltage, boron (B) may be beforehand added by the concentration about $1 \times 10^{15} - 5 \times 10^{17} \text{ cm}^{-3}$.

[0183]Next, the island like semiconductor layers 6004–6006 were covered, and the gate dielectric film 6007 which uses silicon oxide or silicon nitride as the main ingredients was formed. What is necessary is just to form preferably 10–200 nm of gate dielectric film 6007 in a thickness of 50–150 nm. For example, it is good also as 115-nm gate dielectric film to form 75 nm of nitriding silicon oxide films which used N_2O and SiH_4 as the raw material with plasma CVD method, and oxidize

thermally at 800–1000 ** among oxygen environment or the mixed atmosphere of oxygen and chloride after that. (Drawing 20 (A))

[0184][-- formation [of an n^- field]: -- drawing 20 (B)] -- with the whole surface of the field which forms the island like semiconductor layers 6004 and 6006 and wiring. The resist masks 6008–6011 were formed in a part of island like semiconductor layer 6005 (the field used as a channel forming region is included), the impurity element which gives a n type was added and the low concentration impurity regions 6012 and 6013 were formed. The LDD region where these low concentration impurity regions 6012 and 6013 lap with a gate electrode via gate dielectric film at n channel type TFT of a CMOS circuit behind (in this Description, it is called a Lov field.) It is a meaning of overlap in ov. It is an impurity range for forming. Suppose that the concentration of the impurity element which gives the n type contained in the low concentration impurity region formed here is expressed with (n^-). Therefore, in this Description, the low concentration impurity regions 6012 and 6013 can be put in another way as an n^- field.

[0185]Here, the phosphorus was added by the ion doping method which carried out plasma excitation without carrying out mass separation of the phosphoretted hydrogen (PH_3). Of course, the ion implantation method for performing mass separation may be used. In this process, the phosphorus was added to the semiconductor layer under it through the gate dielectric film 6007. As for the phosphorus concentration to add, it was preferred to use the range of 5×10^{17} – 5×10^{18} atoms/cm³, and it made it 1×10^{18} atoms/cm³ here.

[0186]Then, the resist masks 6008–6011 were removed, in a nitrogen atmosphere, heat treatment of 1 to 12 hours was preferably performed at 550–800 **, and 400–900 ** of processes of activating the phosphorus added at this process were performed.

[0187][-- formation [of the object for gate electrodes, and the conducting film for wiring]: -- drawing 20 (C)] -- the element or either which was chosen from tantalum (Ta), titanium (Ti), molybdenum (Mo), and tungsten (W) in the 1st conducting film 6014 was formed in a thickness of 10–100 nm with the conductive material used as the main ingredients. As the 1st conducting film 6014, it is desirable to use tantalum nitride (Ta₂N₃) and tungsten nitride (W₂N₃), for example. The element or either which was chosen from Ta, Ti, Mo, and W in the 2nd conducting film 6015 on the 1st conducting film 6014 was formed in a thickness of 100–400 nm with the conductive material used as the main ingredients. For example, what is necessary is just to form Ta in a thickness of 200 nm. Although not illustrated, it is effective to form a silicone film by a thickness of about 2–20 nm under the 1st conducting film 6014 for antioxidizing of the conducting films 6014 and 6015 (especially conducting film 6015).

[0188][Formation:drawing 21 (A) of formation of a p-ch gate electrode and a wiring electrode, and a p^+ field] Form the resist masks 6016–6019 and the 1st conducting film and 2nd conducting film (it is hereafter dealt with as a cascade screen) are etched, The gate electrode 6020 of p channel type TFT and the gate wires 6021 and 6022 were formed. On the field used as n channel type TFT, it left the conducting films 6023 and 6024 so that the whole surface might be covered.

[0189]And it left the resist masks 6016–6019 as they were, and was considered as the mask, and the process of adding the impurity element which gives a p type to a part of semiconductor layer 6004 in which p channel type TFT is formed was performed. Here, it added by using boron as the impurity element using diborane (B_2H_6) by the ion doping method (of course, the ion implantation method may be used). Here, boron was added to the concentration of 5×10^{20} – 3×10^{21} atoms/cm³. Suppose that the concentration of the impurity element which gives the p type contained in the impurity range formed here is expressed with (p^{++}). Therefore, in this Description, the impurity ranges 6025 and 6026 can be put in another way as a p^{++} field.

[0190]In this process, after carrying out etching removal of the gate dielectric film 6007 using the

resist masks 6016-6019 and exposing a part of island like semiconductor layer 6004, the process of adding the impurity element which gives a p type may be performed. In that case, since accelerating voltage is low and ends, there are few damages given to island-shape semiconductor membrane, and a throughput also improves.

[0191][-- formation [of a n⁻ch gate electrode]: -- drawing 21 (B)] -- next, after removing the resist masks 6016-6019, they formed the resist masks 6027-6030, and formed the gate electrodes 6031 and 6032 of n channel type TFT. At this time, the gate electrode 6031 was formed so that it might lap with the n⁻ fields 6012 and 6013 via gate dielectric film.

[0192][-- formation [of an n⁺ field]: -- drawing 21 (C)] -- next, the resist masks 6027-6030 were removed and the resist masks 6033-6035 were formed. And in n channel type TFT, the process of forming the impurity range which functions as the source region or a drain area was performed. The resist mask 6035 formed the gate electrode 6032 of n channel type TFT with the wrap form. This is for forming an LDD region so that it may not lap with a gate electrode in a next process at n channel type TFT of a picture-element-matrix circuit.

[0193]And the impurity element which gives a n type was added and the impurity ranges 6036-6040 were formed. Here, it carried out by the ion doping method (of course, the ion implantation method may be used) for having used phosphoretted hydrogen (PH₃), and concentration of the phosphorus of this field was made into $1 \times 10^{20} - 1 \times 10^{21}$ atoms/cm³. Suppose that the concentration of the impurity element which gives the n type contained in the impurity ranges 6038-6040 formed here is expressed with (n⁺). Therefore, in this Description, the impurity ranges 6038-6040 can be put in another way as an n⁺ field. Since the n⁻ field was already formed, the impurity ranges 6036 and 6037 contain a phosphorus strictly by concentration a little higher than the impurity ranges 6038-6040.

[0194]In this process, after etching the gate dielectric film 6007 by having used the resist masks 6033-6035 and the gate electrode 6031 as the mask and exposing a part of island-shape semiconductor membrane 6005 and 6006, the process of adding the impurity element which gives a n type may be performed. In that case, since accelerating voltage is low and ends, there are few damages given to island-shape semiconductor membrane, and a throughput also improves.

[0195][-- n⁻ formation [of field]: -- drawing 22 (A)] -- next, the resist masks 6033-6035 were removed and the process of adding the impurity element which gives a n type to the island like semiconductor layer 6006 used as n channel type TFT of a picture-element-matrix circuit was performed. In this way, comparable as said n⁻ field in the formed impurity ranges 6074-6077 or the phosphorus of concentration (specifically $5 \times 10^{16} - 1 \times 10^{18}$ atoms/cm³) less than it was added. Suppose that the concentration of the impurity element which gives the n type contained in the impurity ranges 6074-6077 formed here is expressed with (n⁻). Therefore, in this Description, they are the impurity ranges 6074-6077 n⁻. It can be put in another way as field. Although the phosphorus is added in this process by the concentration which is in all the impurity ranges except for the impurity ranges 6068 and 6069 hidden with the gate electrode, since it is very low concentration, it does not ignore and interfere.

[0196][-- process [of thermal activation]: -- drawing 22 (B)] -- next, the supplementary insulation film 6045 which turns into a part of 1st interlayer insulation film was formed in behind. What is necessary is just to form the supplementary insulation film 6045 by the cascade screen which combined a silicon nitride film, a silicon oxide film, a nitriding silicon oxide film, or them. The thickness is just 100-400 nm.

[0197]Then, in order to activate the impurity element which gives the n type or p type added by each concentration, the heat treatment process was performed. This process can be performed by the furnace annealing method, the laser annealing method, or the rapid thermal annealing method

(the RTA method). Here, the activation process was performed by the furnace annealing method. Into a nitrogen atmosphere, heat-treatment performed 300–650 °C of 450 °C and heat treatments of 2 hours preferably 400–550 °C and here.

[0198]In the atmosphere containing 3 to 100% of hydrogen, heat treatment of 1 to 12 hours was performed at 300–450 °C, and the process of hydrogenating an island like semiconductor layer was performed. This process is a process of carrying out the termination of the dangling bond of a semiconductor layer by the hydrogen excited thermally. As other means of hydrogenation, plasma hydrogenation (the hydrogen excited by plasma is used) may be performed.

[0199][Formation: drawing 22 (C) of an interlayer insulation film, a source/drain electrode, a light-shielding film, a picture element electrode, and retention volume] When finishing the activation process, the interlayer insulation film 6046 of 0.5 – 1.5-micrometer thickness was formed on the supplementary insulation film 6045. The cascade screen which becomes with said supplementary insulation film 6045 and the interlayer insulation film 6046 was used as the 1st interlayer insulation film.

[0200]Then, the contact hole which arrives at the source region or the drain area of each TFT was formed, and the source electrodes 6047–6049 and the drain electrodes 6050 and 6051 were formed. Although not illustrated, in this embodiment, it was considered as the cascade screen of the three-tiered structure which formed continuously 300 nm of aluminum films which contain [this electrode] 100 nm and Ti for a Ti film, and 150 nm of Ti films by the sputtering method.

[0201]Next, it formed as the passivation film 6052 by a thickness of 50–500 nm (typically 200–300 nm) with the silicon nitride film, the silicon oxide film, or the nitriding silicon oxide film. Then, when hydrogen treatment was performed in this state, the desirable result was obtained the improvement [for] in the characteristic of TFT. For example, the same effect was acquired, even if it was good to have performed heat treatment of 1 to 12 hours at 300–450 °C or it used the plasma hydrogenating method in the atmosphere containing 3 to 100% of hydrogen. An opening may be formed in the passivation film 6052 in the position which forms the contact hole for connecting a picture element electrode and a drain electrode behind here.

[0202]Then, the 2nd interlayer insulation film 6053 that consists of organic resin was formed in a thickness of about 1 micrometer. As organic resin, polyimide, an acrylic, polyamide, polyimidoamide, BCB (benz-cyclo-butene), etc. can be used. The point for a method for film deposition that the advantage of using an organic resin film is simple, the point that parasitic capacitance can be reduced since specific inductive capacity is low, the point of excelling in surface smoothness, etc. are got. An organic resin film, an organic system SiO compound, etc. except having mentioned above can also be used. Here, it calcinated and formed at 300 °C after applying to a substrate using polyimide of the type which carries out thermal polymerization.

[0203]Next, in the field used as a picture-element-matrix circuit, the light-shielding film 6054 was formed on the 2nd interlayer insulation film 6053. The light-shielding film 6054 formed in a thickness of 100–300 nm the element or either which was chosen from aluminum (aluminum), titanium (Ti), and tantalum (Ta) by the film used as the main ingredients. And the 30–150 nm (preferably 50–75 nm)-thick oxide film 6055 was formed in the surface of the light-shielding film 6054 by the anode oxidation method or the plasma oxidation method. Here, the aluminum oxide film (alumina membrane) was used as the oxide film 6055 using the film which uses an aluminum film or aluminum as the main ingredients as the light-shielding film 6054.

[0204]Although it had composition which provides an insulator layer only in the light-shielding film surface here, an insulator layer may be formed by gaseous phase methods, such as plasma CVD method, a heat CVD method, or a sputtering method. It is preferred that thickness sets to 30–150 nm (preferably 50–75 nm) also in that case. A silicon oxide film, a silicon nitride film, a nitriding silicon oxide film, a DLC (Diamond like carbon) film, or an organic resin film may be used. The cascade screen which combined these may be used.

[0205]Next, the contact hole which reaches the drain electrode 6051 was formed in the 2nd

interlayer insulation film 6053, and the picture element electrode 6056 was formed. The picture element electrodes 6057 and 6058 are picture element electrodes of another pixel which adjoins, respectively. A metal membrane should just be used for the picture element electrodes 6056-6058 when making it into a reflection type liquid crystal display using a transparent conducting film, in making it into a transmission type liquid crystal display. Here, in order to consider it as a transmission type liquid crystal display, the indium-tin-oxide (ITO) film was formed in a thickness of 100 nm by the sputtering method.

[0206]At this time, the field 6059 with which the picture element electrode 6056 and the light-shielding film 6054 lapped via the oxide film 6055 formed retention volume.

[0207]In this way, on the same substrate, the active matrix substrate with the CMOS circuit and picture-element-matrix circuit used as a driver line was completed. P channel type TFT6081 and n channel type TFT6082 were formed in the CMOS circuit used as a driver line, and pixel TFT6083 which becomes by n channel type TFT was formed in the picture-element-matrix circuit.

[0208]The channel forming region 6062, the source region 6063, and the drain area 6064 were formed in p channel type TFT6081 of a CMOS circuit in the p^+ field, respectively. The LDD region which lapped with the gate electrode via the channel forming region 6065, the source region 6066, the drain area 6067, and gate dielectric film in n channel type TFT6082 (henceforth a Lov field) It is the mind of overlap in ov. 6068 and 6069 were formed. At this time, the source region 6066 and the drain area 6067 were formed in the field, respectively ($n^- + n^+$), and the Lov fields 6068 and 6069 were formed in the n^- field.

[0209]The LDD region which does not lap with a gate electrode via the channel forming regions 6070 and 6071, the source region 6072, the drain area 6073, and gate dielectric film in pixel TFT6083 (henceforth a Loff field) off is the mind of offset. The n^+ field 6078 adjacent to 6074-6077, and the Loff fields 6075 and 6076 was formed. At this time, it is formed in an n^+ field, respectively and, in the Loff fields 6074-6077, the source region 6072 and the drain area 6073 are n^- -- It was formed in field.

[0210]Here, the structure of TFT which forms each circuit according to the circuit specifications which a picture-element-matrix circuit and a driver line require was able to be optimized, and the performance of operation and reliability of the semiconductor device were able to be raised. Specifically, n channel type TFT realized TFT structure which thought as important high-speed operation or the measure against hot carriers on the same board, and TFT structure which thought low OFF state current operation as important by changing arrangement of an LDD region according to circuit specifications, and using a Lov field or a Loff field properly.

[0211]For example, in the case of the active matrix type liquid crystal display device, n channel type TFT6082 is suitable for logical circuits which think high-speed operation as important, such as a shift register circuit, a subharmonics circuit, a signal dividing network, a level shifter circuit, and a buffer circuit. N channel type TFT6083 is suitable for the picture-element-matrix circuit and sampling circuit (sample hold circuit) which thought low OFF state current operation as important.

[0212]What is necessary is for 0.5-3.0 micrometers of the length (width) of a Lov field just to be 1.0-1.5 micrometers typically to 3-7 micrometers of channel length. What is necessary is for 0.5-3.5 micrometers of the length (width) of the Loff fields 6074-6077 established in pixel TFT6083 just to be 2.0-2.5 micrometers typically.

[0213](Embodiment 7)

[0214]It is possible to use various liquid crystal materials besides a TN liquid crystal for the liquid crystal display produced by the above-mentioned Embodiments 4-6. For example, 1998, SID, "Characteristics and Driving Scheme of Polymer-Stabilized Monostable FLCDC Exhibiting Fast Response Time and High Contrast Ratio with Gray-Scale Capability" by H. Furueet al., 1997, SID DIGEST, 841, "A Full-Color Thresholdless Antiferroelectric LCD Exhibiting Wide Viewing Angle with

Fast Response It is possible to use the liquid crystal material indicated by Time" by T. Yoshida et al. or U.S. Pat. No. 5594569.

[0215]In particular, in the non-threshold antiferroelectricity liquid crystal mixture which is the liquid crystal mixture material of a non-threshold antiferroelectricity liquid crystal material, and ferroelectric liquid crystal material and an antiferroelectricity liquid crystal material, that in which the driver voltage is about $\pm 2.5\text{V}$ is also found out. When the non-threshold antiferroelectricity liquid crystal mixture of such a low voltage drive is used, It is effective, when becoming possible to suppress the power supply voltage of the sampling circuit of a picture signal to about 5V-8V and using TFT (for example, 0 nm - 500 nm, or 0 nm - 200 nm) with comparatively small width of an LDD region (low concentration impurity region).

[0216]The graph which shows the characteristic of light transmittance to the impressed electromotive force of non-threshold antiferroelectricity liquid crystal mixture here is shown in a figure. The transmission axis of the polarizing plate by the side of incidence of a liquid crystal display is set as the rubbing direction of a liquid crystal display almost in parallel with the normal line direction of the smectic layer of non-threshold antiferroelectricity liquid crystal mixture mostly in agreement. The transmission axis of the polarizing plate by the side of outgoing radiation is mostly set as the right angle (cross Nicol) to the polarization axis of the polarizing plate by the side of incidence. Thus, when non-threshold antiferroelectricity liquid crystal mixture is used, it turns out that it is possible to perform the gradation display which shows an impressed-electromotive-force-transmissivity characteristic as shown in a figure.

[0217]Generally, non-threshold antiferroelectricity liquid crystal mixture has large spontaneous polarization, and its dielectric constant of the liquid crystal itself is high. For this reason, in using non-threshold antiferroelectricity liquid crystal mixture for a liquid crystal display, comparatively big retention volume is needed for a pixel. Therefore, it is preferred to use non-threshold antiferroelectricity liquid crystal mixture with small spontaneous polarization. By considering the drive method of a liquid crystal display as a line sequential drive, the write-in period (pixel feeding period) of the gradation voltage to a pixel can be lengthened, and retention volume can also compensate small **** with it.

[0218]Since a low voltage drive is realized by using a non-threshold antiferroelectricity liquid crystal, low power consumption of a liquid crystal display is realized.

[0219](Embodiment 8)

[0220]The display device of this invention explained by above-mentioned Embodiments 1-3 can be used for the projector of 3 board types as shown in drawing 24.

[0221]As for a dichroic mirror, 2406, and 2407, in drawing 24, 2401 is [the display device of this invention and 2411] projection lenses a total reflection mirror, and 2408-2410 a white light source, and 2402-2405.

[0222](Embodiment 9)

[0223]The liquid crystal display of this invention explained by above-mentioned Embodiments 1-3 can also be used for the projector of 3 board types as shown in drawing 25.

[0224]As for a total reflection mirror, and 2507-2509, in drawing 25, a white light source, 2502, and 2503 are [a dichroic prism and 2511] projection lenses a dichroic mirror, and 2504-2506 the liquid crystal panel of this invention, and 2510 2501.

[0225](Embodiment 10)

[0226]The liquid crystal display using the liquid crystal as an expression medium of the display device of this invention explained by above-mentioned Embodiments 1-3 can also be used for the projector of a single plate type as shown in drawing 26.

[0227]In drawing 26, 2601 is a white light source which comprises a lamp and a reflector. 2602, 2603, and 2604 are dichroic mirrors, and reflect the light of blue, red, and a green wavelength zone selectively, respectively. 2605 is a microlens array and is constituted by two or more micro lenses. 2606 is a liquid crystal panel of this invention. As for 2607, a projection lens and 2609 are screens a

field lens and 2608.

[0228](Embodiment 11)

[0229]The projector of the above-mentioned Embodiments 8-10 has a rear projector and a front projector with the projection method.

[0230]Drawing 27 (A) is a front type projector, and comprises the main part 10001, the liquid crystal display 10002 of this invention, the light source 10003, the optical system 10004, and the screen 10005. in addition -- constructing three liquid crystal displays (it is made to correspond to the light of R, G, and B, respectively), although the front projector incorporating one liquid crystal display is shown in drawing 27 (A) -- **** -- high resolution and a high definition front type projector are more realizable by things.

[0231]Drawing 27 (B) is a rear mold projector, 10006 is a main part, 10007 is a liquid crystal display, 10008 is a light source, 10009 is a reflector and 10010 is a screen. The rear mold projector incorporating three active-matrix type semiconductor displays (it is made to correspond to the light of R, G, and B, respectively) is shown in drawing 27 (B).

[0232](Embodiment 12)

[0233]This embodiment shows the example which used the display device of this invention for the goggles type display.

[0234]Drawing 28 is referred to. 2801 is a goggles type display body. 2802-R and 2802-L are the display devices of this invention, 2803-R and 2803-L are LED back lights, and 2804-R and 2804-L are optical elements.

[0235](Embodiment 13)

[0236]In this embodiment, LED is used for the back light of the display device of this invention, and a field sequential drive is performed.

[0237]the start signal (Vsync signal) of the picture signal writing to the timing chart of the field sequential drive method shown in drawing 29, red (R), and green -- (G) and blue -- the lighting timing signal (R, G, and B) of LED of (B) and the video signal (VIDEO) are shown. Tf is a frame period. TR, TG, and TB are the LED lighting periods of red (R) green (G) blue (B), respectively.

[0238]The picture signal supplied to a display device, for example, R1, is a signal with which the video data of the origin corresponding to the red inputted from the outside was compressed into one third by the time base direction. The picture signal supplied to a liquid crystal panel, for example, G1, is a signal with which the video data of the origin corresponding green inputted from the outside was compressed into one third by the time base direction. The picture signal supplied to a liquid crystal panel, for example, B1, is a signal with which the video data of the origin corresponding to the blue inputted from the outside was compressed into one third by the time base direction.

[0239]In a field sequential drive method, LED of R, G, and B lights up in order an LED lighting period TR period, TG period, and during the TB, respectively. During the lighting (TR) of red LED, the video signal (R1) corresponding to red is supplied to a liquid crystal panel, and a part for picture 1 red screen is written in a liquid crystal panel. During the green lighting (TG) of LED, the video data (G1) corresponding green is supplied to a liquid crystal panel, and a part for picture 1 green screen is written in a liquid crystal panel. During the lighting (TB) of blue LED, the video data (B1) corresponding to blue is supplied to a display device, and a part for picture 1 blue screen is written in a display device. One frame is formed by these three writing of a picture. A liquid crystal can be used for the expression medium of the display device of this embodiment.

[0240](Embodiment 14)

[0241]In this embodiment, the example which used the display device of this invention for the notebook type personal computer is shown in drawing 30.

[0242]3001 is a notebook type personal computer body, and 3002 is a display device of this invention. a liquid crystal can be used for the expression medium of the display device of this embodiment, and a back light is used for a case. the back light concerned -- being alike -- LED is used. A cathode-ray tube may be used for a back light like before.

[0243](Embodiment 15)

[0244]Uses various otherwise are shown in the display device of this invention. This embodiment explains the semiconductor device incorporating the display device of this invention.

[0245]A video camera, a still camera, car navigation, a personal computer, Personal Digital Assistants (a mobile computer, a cellular phone, etc.), etc. are mentioned to such a semiconductor device. Those examples are shown in drawing 31.

[0246]Drawing 31 (A) is a cellular phone and comprises the main part 11001, the voice output part 11002, the voice input part 11003, the display device 11004 of this invention, the operation switch 11005, and the antenna 11006.

[0247]Drawing 31 (B) is a video camera and comprises the main part 12001, the display device 12002 of this invention, the voice input part 12003, the operation switch 12004, the battery 12005, and the television part 12006.

[0248]Drawing 31 (C) is a mobile computer and comprises the main part 13001, the camera part 13002, the television part 13003, the operation switch 13004, and the display device 13005 of this invention.

[0249]Drawing 31 (D) is portable books (digital book), and comprises the main part 14001, the liquid crystal displays 14002 and 14003 of this invention, the storage 14004, the operation switch 14005, and the antenna 14006.

[0250](Embodiment 16)

[0251]This embodiment explains the example which used for EL (electroluminescence) display device the drive method used for the display device of the invention in this application.

[0252]Drawing 32 (A) is a plan of the EL display of this embodiment. In drawing 32 (A), as for a substrate and 24011, the source side drive circuit and 24013 are the gate side drive circuits a picture element part and 24012 24010, and each drive circuit results in FPC24017 through the wiring 24014-24016, and is connected to an external instrument.

[0253]Drawing 32 (B) is the section structure of the EL display of this embodiment. this time -- at least -- a picture element part -- as a drive circuit and a picture element part are surrounded preferably, the cover material 26000, the sealant 27000, and the sealant (the 2nd sealant) 27001 are formed.

[0254]On the substrate 24010 and the ground film 24021, TFT for drive circuits. (However, the CMOS circuit which combined n channel type TFT and p channel type TFT here is illustrated.) 24022 and TFT24023 (however, only TFT which controls the current to an EL element here is illustrated.) for picture element parts are formed.

[0255]If TFT24022 for drive circuits and TFT24023 for picture element parts are completed, the picture element electrode 24027 which becomes with the transparent conducting film electrically connected with the drain of TFT24023 for picture element parts will be formed on the interlayer insulation film (flattening film) 24026 which becomes with a resin material. As a transparent conducting film, the compound (referred to as ITO) of indium oxide and the tin oxide or the compound of indium oxide and a zinc oxide can be used. And if the picture element electrode 24027 is formed, the insulator layer 24028 will be formed and an opening will be formed on the picture element electrode 24027.

[0256]Next, EL layer 24029 is formed. EL layer 24029 should just be taken as a laminated structure or layer structure, combining freely a publicly known EL material (a hole injection layer, an electron hole transporting bed, a luminous layer, an electron transport layer, or an electronic injection layer). As what kind of structure it is considered should just use publicly known technology. There are low molecule system material and polymer system (polymer system) material in an EL material. When using low molecule system material, vacuum deposition is used, but when using polymer system material, it is possible to use simple methods, such as a spin coat method, print processes, or the ink jet method.

[0257]According to this embodiment, an EL layer is formed with vacuum deposition using a shadow

mask. By forming the luminous layer (a red light layer, a green emission layer, and a blue light layer) in which luminescence from which wavelength differs for every pixel using a shadow mask is possible, a colored presentation becomes possible. In addition, which method may be used although there are a system which combined the color conversion layer (CCM) and the light filter, and a system which combined the white light layer and the light filter. Of course, it can also be considered as the EL display of monochrome luminescence.

[0258]If EL layer 24029 is formed, the anode 24030 will be formed on it. As for the moisture which exists in the interface of the anode 24030 and EL layer 24029, or oxygen, eliminating as much as possible is desirable. Therefore, the device of forming the anode 24030 without carrying out continuation membrane formation of EL layer 24029 and the anode 24030 in a vacuum, or forming EL layer 24029 by an inert atmosphere and carrying out air release is required. At this embodiment, the above membrane formation is enabled by using the film deposition system of a multi chamber system (cluster tool system).

[0259]In this embodiment, the laminated structure of a LiF (lithium fluoride) film and aluminum (aluminum) film is used as the anode 24030. The LiF (lithium fluoride) film of 1-nm thickness is specifically formed with vacuum deposition on EL layer 24029, and the aluminum film of 300-nm thickness is formed on it. Of course, the MgAg electrode which is a publicly known cathode material may be used. And the anode 24030 is connected to the wiring 24016 in the field shown by 24031. The wiring 24016 is a power supply line for giving predetermined voltage to the anode 24030, and is connected to FPC24017 via the conductive paste material 24032.

[0260]In order to electrically connect the anode 24030 and the wiring 24016 in the field shown in 24031, it is necessary to form a contact hole in the interlayer insulation film 24026 and the insulator layer 24028. What is necessary is just to form these at the time of etching of the interlayer insulation film 24026, and etching of the insulator layer 24028 (at the time of formation of the contact hole for picture element electrodes) (at the time of formation of the opening before EL layer formation). When etching the insulator layer 24028, even the interlayer insulation film 24026 may etch by package. In this case, if the interlayer insulation film 24026 and the insulator layer 24028 are the same resin materials, form of a contact hole can be made good.

[0261]Thus, the surface of the formed EL element is covered and the passivation film 26003, the filler 26004, and the cover material 26000 are formed.

[0262]As an EL element part is surrounded, the sealant 27000 is formed inside the cover material 26000 and the substrate 24010, and the sealant (the 2nd sealant) 27001 is further formed in the outside of the sealant 27000.

[0263]At this time, this filler 26004 functions also as adhesives for pasting up the cover material 26000. As the filler 26004, PVC (polyvinyl chloride), an epoxy resin, silicone resin, and PVB (polyvinyl BUCHIRARU) or EVA (ethylene vinyl acetate) can be used. If the drier is provided in the inside of this filler 26004, since a moisture absorption effect can be held, it is desirable.

[0264]A spacer may be made to contain in the filler 26004. At this time, a spacer may be used as the particulate matter which consists of BaO(s) etc., and hygroscopicity may be given to the spacer itself.

[0265]When a spacer is formed, the passivation film 26003 can ease spacer pressure. The resin layer etc. which ease spacer pressure may be provided apart from a passivation film.

[0266]As the cover material 26000, a glass plate, an aluminum plate, a stainless plate, An FRP (Fiberglass-Reinforced Plastics) board, a PVF (polyvinyl fluoride) film, a miler film, polyester film, or an acrylic film can be used. When using PVB and EVA as the filler 26004, it is preferred to use the sheet of the structure which sandwiched tens of micrometers aluminium foil with the PVF film or the miler film.

[0267]However, depending on the light-emitting direction (the direction of a light emission) from an EL element, the cover material 26000 needs to have translucency.

[0268]The wiring 24016 is electrically connected to FPC24017 through the crevice between the

sealant 27000 and the sealant 27001, and the substrate 24010. Although the wiring 24016 was explained here, other wiring 24014 and 24015 is electrically connected to FPC24017 through the bottom of the sealant 27000 and the sealant 27001 in a similar manner.

[0269](Embodiment 17) This embodiment explains the example which produced the EL display of a form which is different in Embodiment 16 using drawing 33 (A) and 33 (B). Since the thing of the same number as drawing 32 (A) and 32 (B) has pointed out the same portion, explanation is omitted.

[0270]Drawing 33 (A) is a plan of the EL display of this embodiment, and shows drawing 33 (B) the sectional view which cut drawing 33 (A) by A-A'.

[0271]According to Embodiment 16, the surface of an EL element is covered and even the passivation film 26003 is formed.

[0272]The filler 6004 is formed as an EL element is covered. This filler 26004 functions also as adhesives for pasting up the cover material 26000. As the filler 26004, PVC (polyvinyl chloride), an epoxy resin, silicone resin, and PVB (polyvinyl BUCHIRARU) or EVA (ethylene vinyl acetate) can be used. If the drier is provided in the inside of this filler 26004, since a moisture absorption effect can be held, it is desirable.

[0273]A spacer may be made to contain in the filler 26004. At this time, a spacer may be used as the particulate matter which consists of BaO(s) etc., and hygroscopicity may be given to the spacer itself.

[0274]When a spacer is formed, the passivation film 26003 can ease spacer pressure. The resin layer etc. which ease spacer pressure may be provided apart from a passivation film.

[0275]As the cover material 26000, a glass plate, an aluminum plate, a stainless plate, An FRP (Fiberglass-Reinforced Plastics) board, a PVF (polyvinyl fluoride) film, a miler film, polyester film, or an acrylic film can be used. When using PVB and EVA as the filler 26004, it is preferred to use the sheet of the structure which sandwiched tens of micrometers aluminium foil with the PVF film or the miler film.

[0276]However, depending on the light-emitting direction (the direction of a light emission) from an EL element, the cover material 6000 needs to have translucency.

[0277]next, the side (disclosure side) of the filler 26004 after pasting up the cover material 26000 using the filler 26004 -- a wrap -- the frame material 26001 is attached like. The frame material 26001 is pasted up by the sealant (it functions as adhesives) 26002. Although it is preferred at this time to use a photo-setting resin as the sealant 26002, thermosetting resin may be used as long as the heat resistance of an EL layer allows. As for the sealant 26002, it is desirable that it is the material which penetrates neither moisture nor oxygen as much as possible. The drier may be added inside the sealant 26002.

[0278]The wiring 24016 is electrically connected to FPC24017 through the crevice between the sealant 26002 and the substrate 24010. Although the wiring 24016 was explained here, other wiring 24014 and 24015 is electrically connected to FPC24017 through the bottom of the sealant 26002 in a similar manner.

[0279](Embodiment 18) Upper surface structure is shown in drawing 35 (A), and this true form voice shows a circuit diagram for the still more detailed section structure of the picture element part in an EL display panel to drawing 34 at drawing 35 (B). What is necessary is just to refer to it mutually in drawing 34, drawing 35 (A), and drawing 35 (B), since a common mark is used.

[0280]In drawing 34, TFT23002 for switching provided on the substrate 23001 may use the TFT structure of Embodiment 4, and may use the structure of publicly known TFT. Although it is considered as double gated structure in this embodiment, since there is no big difference in structure and production processes, explanation is omitted. However, it becomes the structure where the series of the two TFT(s) were substantially carried out by considering it as double gated structure, and there is an advantage that an OFF state current value can be reduced. Although it is considered as double gated structure in this embodiment, a single gate structure may be sufficient and multi-gate structure with triple gate structure or the gate number beyond it may be sufficient.

[0281]TFT23003 for current control is formed using NTFT. At this time, the drain wiring 23035 of TFT23002 for switching is electrically connected to the gate electrode 23037 of TFT for current control by the wiring 23036. The wiring shown by 23038 is a gate wire which electrically connects the gate electrodes 23039a and 23039b of TFT23002 for switching.

[0282]Since TFT for current control is an element for controlling the current amount which flows through an EL element, much current flows and it is also an element with the high danger of degradation by heat, or degradation by hot carriers. Therefore, the structure of the invention in this application which provides an LDD region so that it may lap with a gate electrode via gate dielectric film at the drain side of TFT for current control is very effective.

[0283]Although the single gate structure is illustrating TFT23003 for current control in this embodiment, it is good also as multi-gate structure which connected two or more TFT(s) in series. It is good also as a structure which connects two or more TFT(s) in parallel, divides a channel forming region into plurality substantially, and enabled it to emit heat at high efficiency. Such a structure is effective as a measure against degradation by heat.

[0284]As shown in drawing 35 A, the wiring used as the gate electrode 23037 of TFT23003 for current control laps via the drain wiring 23040 and the insulator layer of TFT23003 for current control in the field shown by 23004. At this time, a capacitor is formed in the field shown by 23004. This capacitor 23004 functions as a capacitor for holding the voltage concerning the gate of TFT23003 for current control. The drain wiring 23040 is connected to the current supply source line (power source wire) 23006, and fixed voltage is always applied.

[0285]The 1st passivation film 23041 is formed on TFT23002 for switching, and TFT23003 for current control, and the flattening film 23042 which becomes with a resin insulator layer is formed on it. It is dramatically important to carry out the flattening of the level difference by TFT using the flattening film 23042. Since the EL layer formed behind is very thin, when a level difference exists, it may cause poor luminescence. Therefore, before forming a picture element electrode so that an EL layer can be formed as much as possible in a flat surface, it is desirable to carry out a flattening.

[0286]23043 is a picture element electrode (anode of an EL element) which becomes with a reflexible high conducting film, and is electrically connected to the drain of TFT23003 for current control. It is preferred to use low resistance conducting films, such as an aluminum alloy film, a copper alloy film, or a silver alloy film, or those cascade screens as the picture element electrode 23043. Of course, it is good also as a laminated structure with other conducting films.

[0287]The luminous layer 23045 is formed into the slot (it is equivalent to a pixel) formed by the banks 23044a and 23044b formed with the insulator layer (preferably resin). Although only stroke matter is illustrated here, the luminous layer corresponding to each color of R (red), G (green), and B (blue) may be made and divided. pi conjugated polymer system material is used as an organic electroluminescence material made into a luminous layer. As a typical polymer system material, a poly para-phenylene vinylene (PPV) system, a polyvinyl-carbazole (PVK) system, the Polyful Oren system, etc. are mentioned.

[0288]Although there is a thing of various molds as a PPV system organic electroluminescence material, For example, "H. Shenk, H.Becker, O.Gelsen, E.Kluge, W.Kreuder, and H.Spreitzer, "Polymers forLight Emitting Diodes", and Euro. What is necessary is just to use material which was indicated to Display, Proceedings, 1999, and p.33-37" and JP,H10-92576,A.

[0289]What is necessary is to use cyano polyphenylene vinylene for the luminous layer which emits light in red as a concrete luminous layer, to use polyphenylene vinylene for the luminous layer which emits light green, and just to use polyphenylene vinylene or poly alkyl phenylene for the luminous layer which emits light blue. The thickness is just 30-150 nm (preferably 40-100 nm).

[0290]However, the above example is an example of the organic electroluminescence material which can be used as a luminous layer, and there is no necessity of limiting to this. What is necessary is just to form an EL layer (layer for moving luminescence and the carrier for it), combining freely a luminous layer, a charge transport layer, or an electric charge pouring layer.

[0291]For example, although this embodiment showed the example which uses polymer system material as a luminous layer, low molecule system organic electroluminescence material may be used. It is also possible to use inorganic materials, such as silicon carbide, as a charge transport layer or an electric charge pouring layer. These organic electroluminescence materials and inorganic materials can use a publicly known material.

[0292]In this embodiment, it is considered as the EL layer of the laminated structure which formed the hole injection layer 3046 which becomes by PEDOT (polythiophene) or PANi (poly aniline) on the luminous layer 23045. And on the hole injection layer 23046, the cathode 23047 which becomes with a transparent conducting film is formed. Since the light generated by the luminous layer 23045 is emitted toward the upper surface side in the case of this embodiment (going above TFT), the cathode must be translucency. Although the compound of indium oxide and the tin oxide and the compound of indium oxide and a zinc oxide can be used as a transparent conducting film, in order to form after forming a heat-resistant low luminous layer and hole injection layer, what can form membranes at low temperature as much as possible is preferred.

[0293]When formed to the cathode 23047, EL element 23005 is completed. EL element 23005 here points out the capacitor formed by the picture element electrode (anode) 23043, the luminous layer 23045, the hole injection layer 23046, and the cathode 23047. Since the picture element electrode 23043 is mostly in agreement with the area of a pixel as shown in drawing 22 A, the whole pixel functions as an EL element. Therefore, bright image display becomes the utilization efficiency of luminescence is dramatically high and possible.

[0294]By the way, in this embodiment, the 2nd passivation film 23048 is further formed on the cathode 23047. As the 2nd passivation film 23048, a silicon nitride film or a nitriding oxidized silicon film is preferred. The purpose is to intercept the exterior and an EL element, and has both a meaning which prevents degradation by oxidation of organic electroluminescence material, and a meaning which stops degasifying from organic electroluminescence material. Thereby, the reliability of an EL display is improved.

[0295]As mentioned above, the EL display panel of this embodiment has a picture element part which consists of a pixel of structure like drawing 34, and has TFT for switching of an OFF state current value low enough, and TFT for current control strong against hot carrier injection. Therefore, it has high reliability and the EL display panel in which good image display is possible is obtained.

[0296](Embodiment 19) In the picture element part shown in Embodiment 18, this embodiment explains the structure where the structure of EL element 23005 was reversed. Drawing 23 is used for explanation. Since a different point from the structure of drawing 34 is only the portion and TFT for current control of an EL element, other explanation is given to omit.

[0297]In drawing 36, TFT23103 for current control is formed using PTFT.

[0298]According to this embodiment, a transparent conducting film is used as the picture element electrode (cathode) 23050. The conducting film which specifically becomes with the compound of indium oxide and a zinc oxide is used. Of course, the conducting film which becomes with the compound of indium oxide and the tin oxide may be used.

[0299]And after the banks 23051a and 23051b which become with an insulator layer are formed, the luminous layer 23052 which becomes by a polyvinyl carbazole by solution spreading is formed. The electronic injection layer 23053 which becomes by potassium acetylacetonate on it, and the anode 23054 which becomes with an aluminum alloy are formed. In this case, the anode 23054 functions also as a passivation film. In this way, EL element 23101 is formed.

[0300]In the case of this embodiment, the light generated in the luminous layer 23052 is emitted toward the direction of the substrate with which TFT was formed as shown by the arrow.

[0301](Embodiment 20) This embodiment shows the example at the time of considering it as a different pixel of structure from the circuit diagram shown in drawing 35 (B) to drawing 37 (A) - (C). 23201 in this embodiment The source wiring of TFT23202 for switching, A capacitor and 23208

consider it as a current supply source line by TFT for current control and 23205 setting to 23206, and the gate wire of TFT23202 for switching and 23204 make 23203 an EL element 23207.

[0302]Drawing 37 (A) is an example at the time of making the current supply source line 23206 common between two pixels. That is, the feature is formed so that two pixels may serve as axial symmetry focusing on the current supply source line 23206. In this case, since the number of a power supply line can be reduced, a picture element part can be further made highly minute.

[0303]Drawing 37 (B) is an example at the time of forming the current supply source line 23208 in parallel with the gate wire 23203. Although it has structure established so that the current supply source line 23208 and the gate wire 23203 might not lap in drawing 37 (B), if it is the wiring formed in the layer from which both differ, it can also provide so that it may lap via an insulator layer. In this case, since the power supply line 23208 and the gate wire 23203 can be made to share the area of exclusive use, a picture element part can be further made highly minute.

[0304]Drawing 37 (C) forms the current supply source line 23208 in parallel with the gate wire 23203 like the structure of drawing 37 (B), and the feature is that it forms two pixels further so that it may become axial symmetry focusing on the current supply source line 23208. It is also effective to form the current supply source line 23208 so that it may lap with either of the gate wires 23203. In this case, since the number of a power supply line can be reduced, a picture element part can be further made highly minute.

[0305]It combines with the composition and freedom of Embodiments 1-9, and composition of this embodiment can be carried out. It is effective to use the EL display panel which has the pixel structure of this embodiment as a display of the electronic device of Embodiment 10.

[0306](Embodiment 21) In drawing 35 (A) shown in Embodiment 20, and 35 (B), in order to hold the voltage concerning the gate of TFT23003 for current control, it is considered as the structure of forming the capacitor 23004, but it is also possible to omit the capacitor 23004. In the case of Embodiment 11, TFT which has the LDD region provided so that it might lap with a gate electrode via gate dielectric film is used as TFT23003 for current control. Although the parasitic capacitance generally called gate capacitance is formed in these overlapping fields, in this embodiment, the feature is at the point of using this parasitic capacitance positively as a substitute of the capacitor 23004.

[0307]Since the capacitance of this parasitic capacitance changes with the area which the above-mentioned gate electrode and the LDD region overlapped, it is decided by the length of the LDD region included to those overlapping fields.

[0308]In the structure of drawing 37 (A) shown in Embodiment 13, (B), and (C), it is possible similarly to omit the capacitor 23205.

[0309]

[Effect of the Invention]

[0310]According to the liquid crystal display of this invention, the multi-gradation display more than the capability of a D/A conversion circuit can be performed. Therefore, it becomes possible to realize a small liquid crystal display.

[Translation done.]

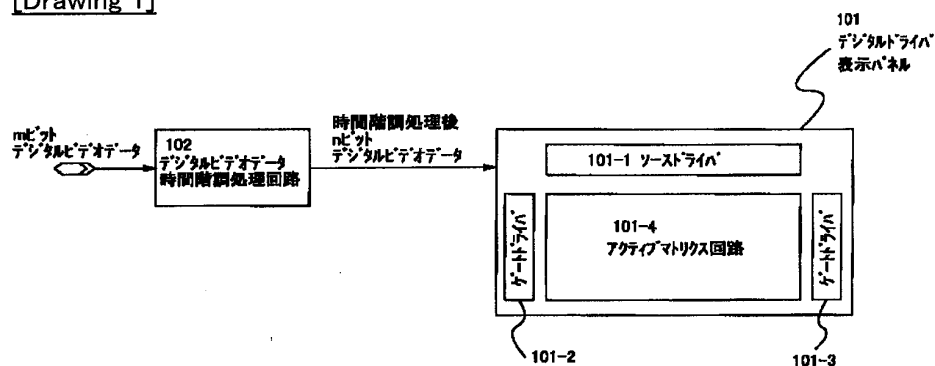
* NOTICES *

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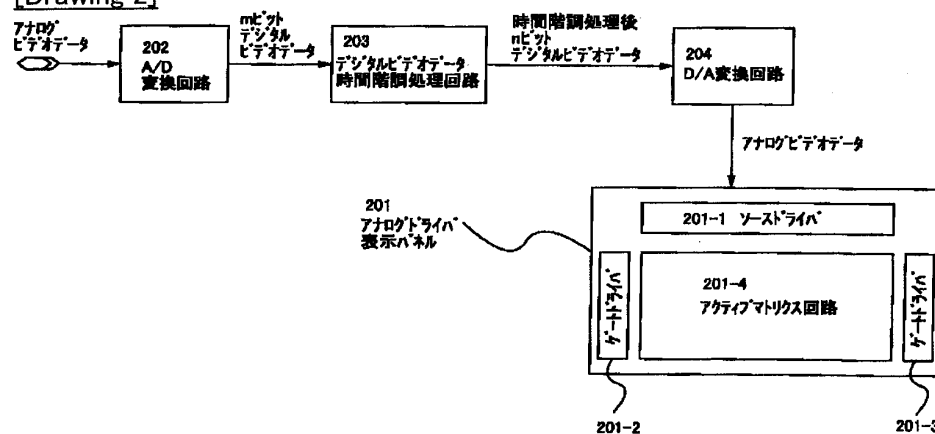
1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DRAWINGS

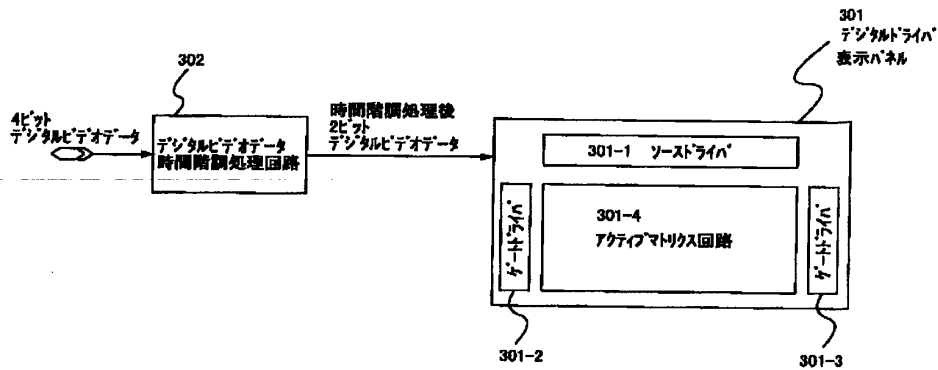
[Drawing 1]



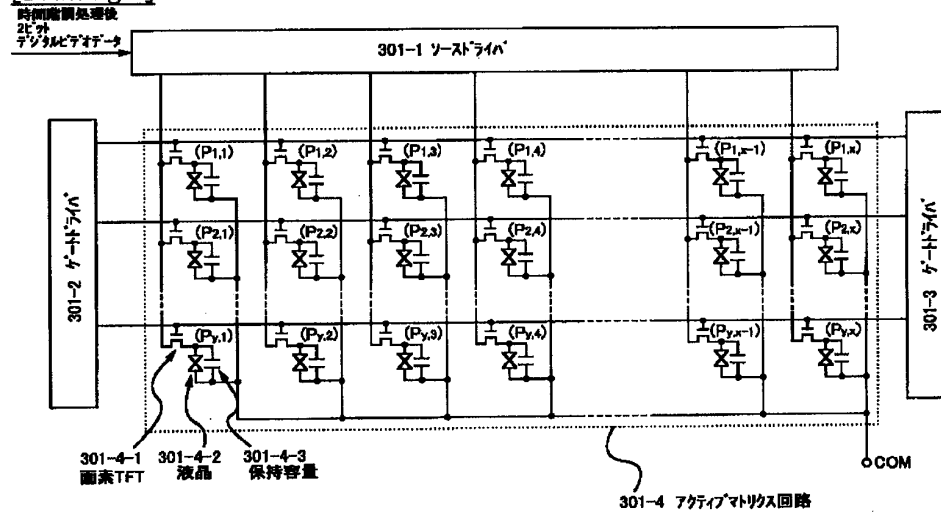
[Drawing 2]



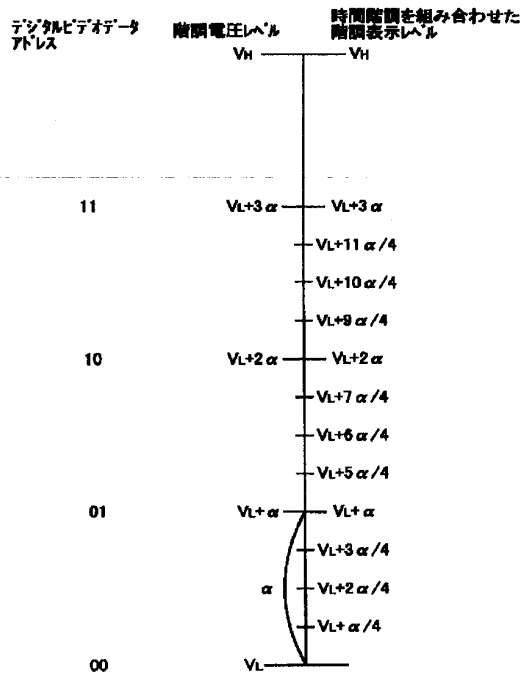
[Drawing 3]



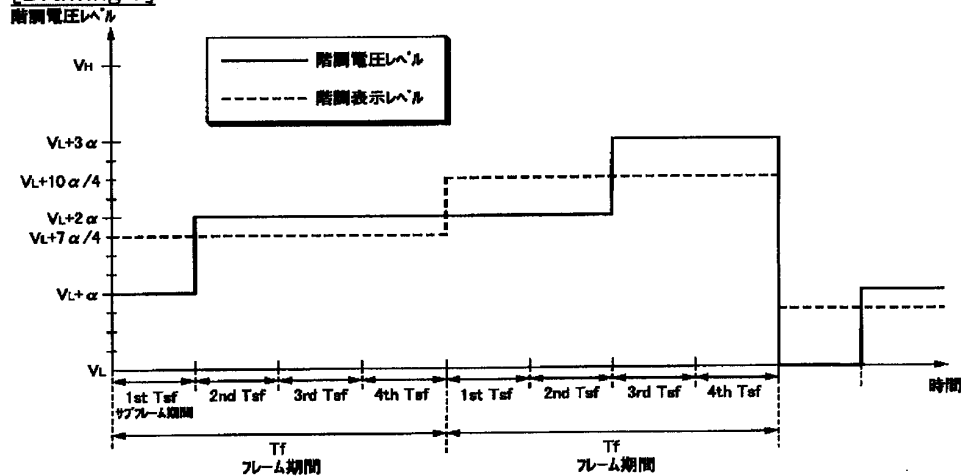
[Drawing 4]



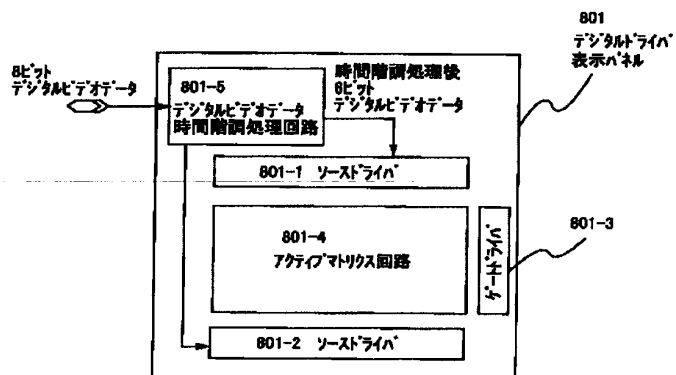
[Drawing 5]



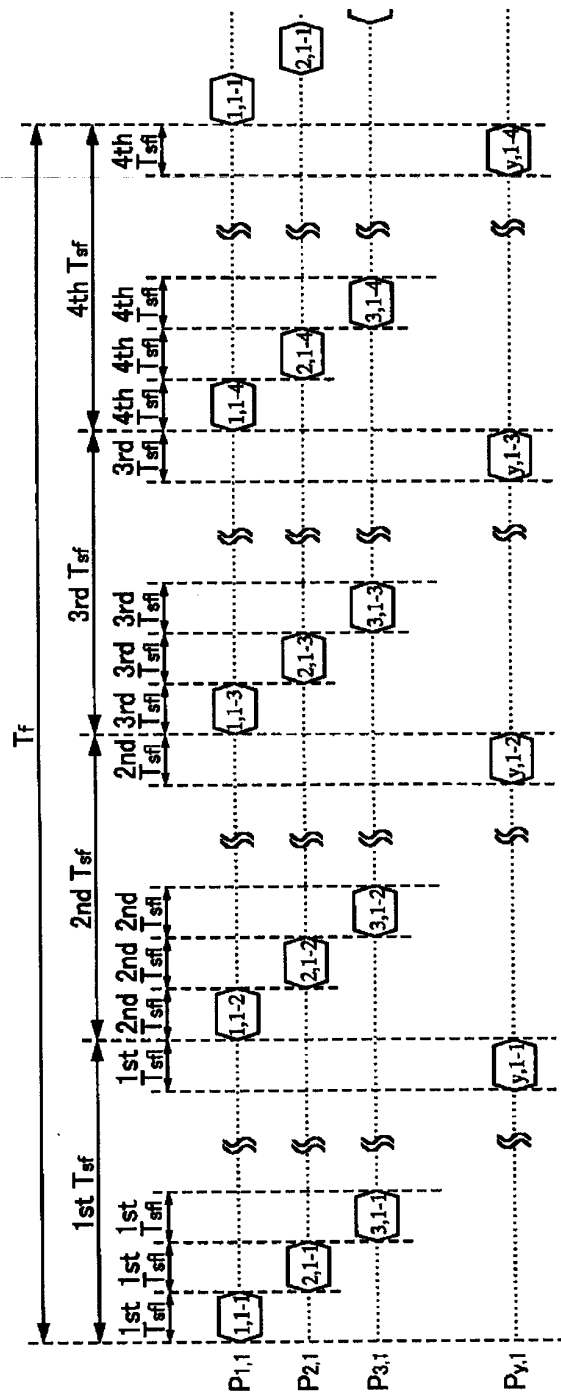
[Drawing 7]



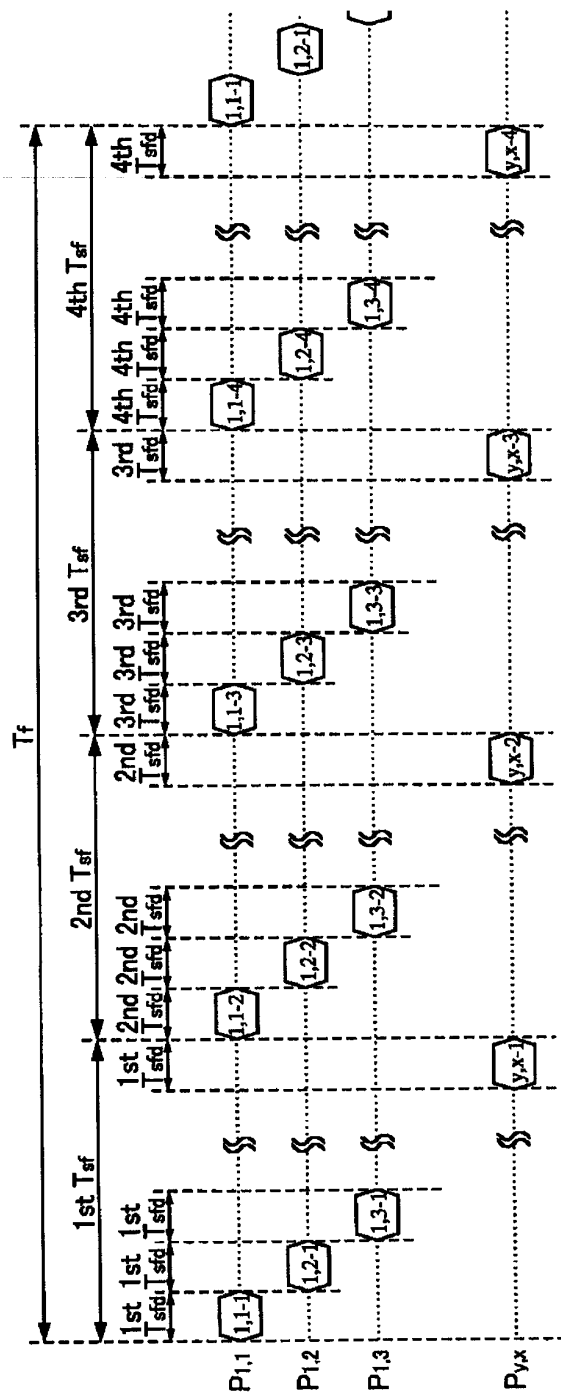
[Drawing 8]



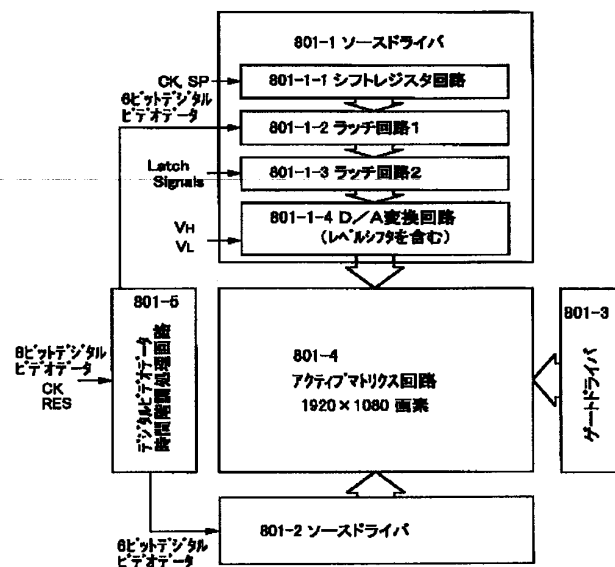
[Drawing 6]



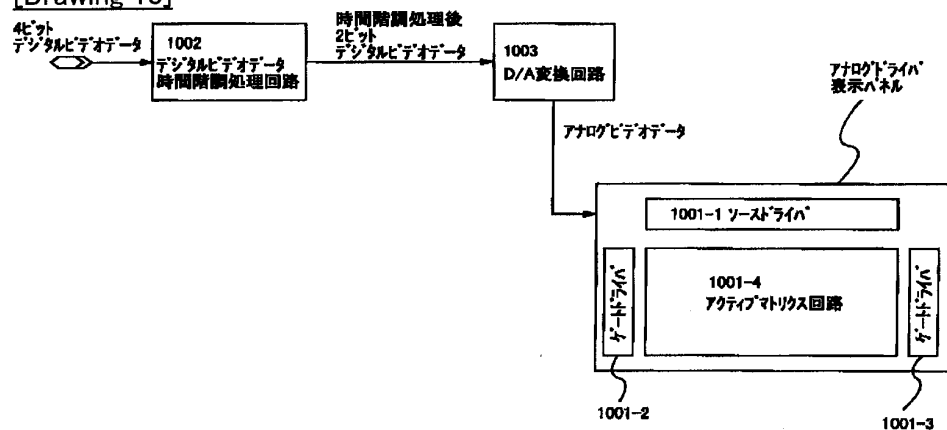
[Drawing 12]



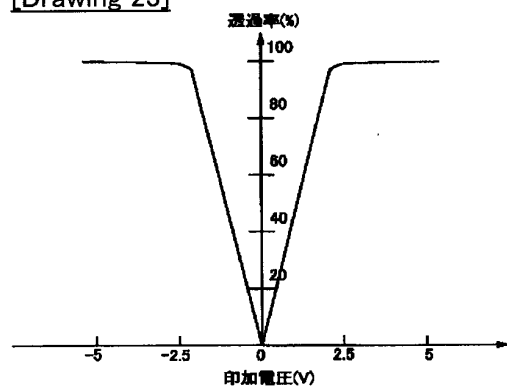
[Drawing 9]



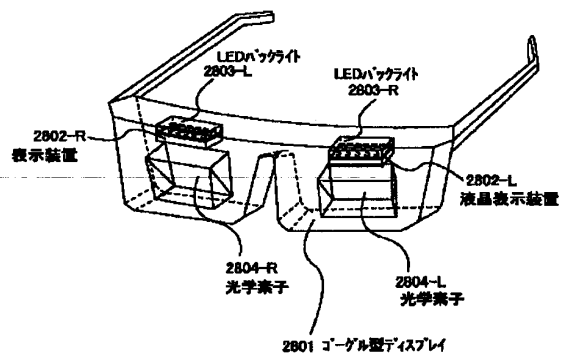
[Drawing 10]



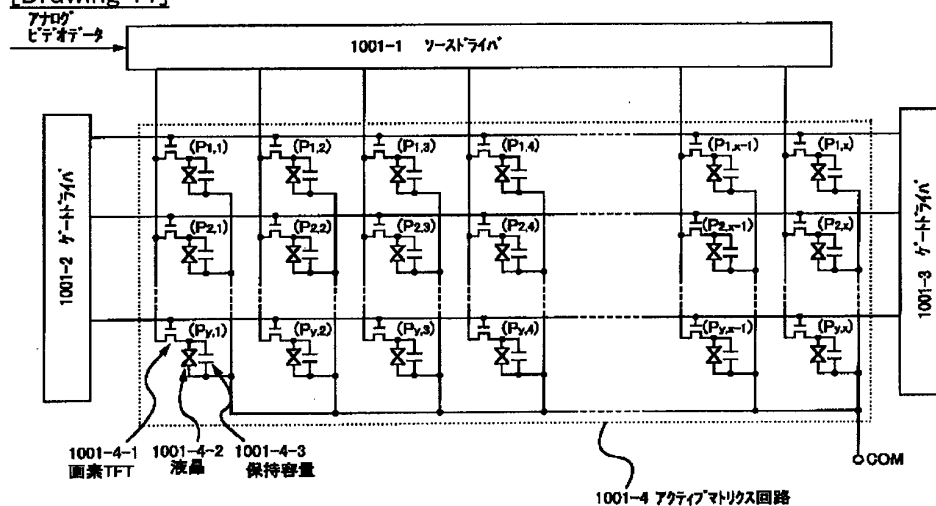
[Drawing 23]



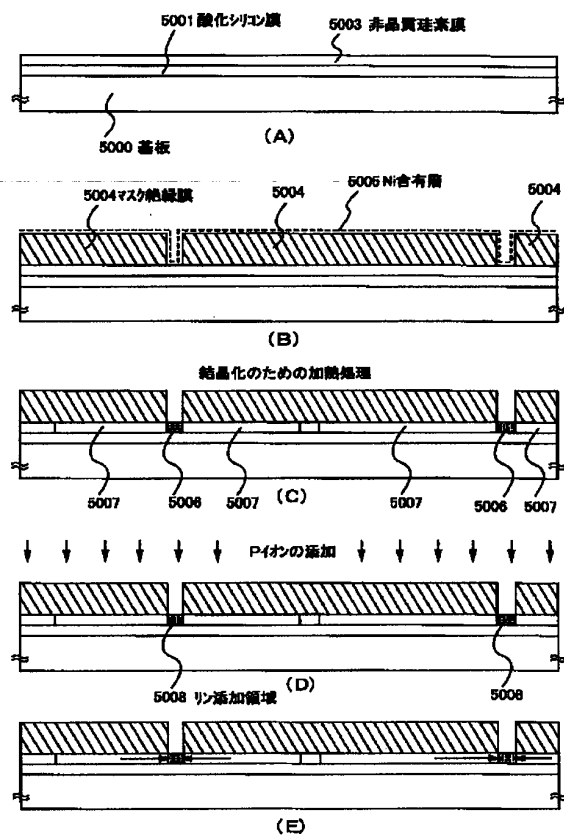
[Drawing 28]



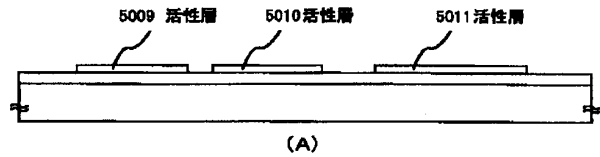
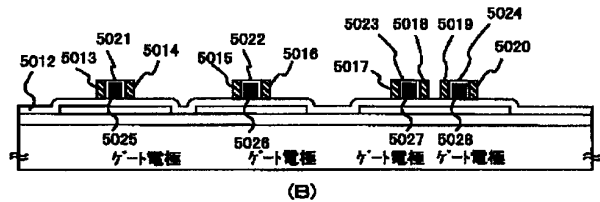
[Drawing 11]



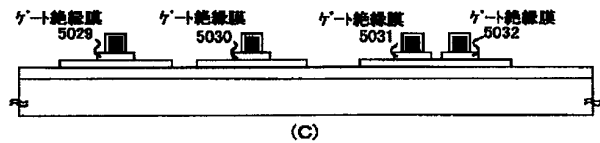
[Drawing 13]



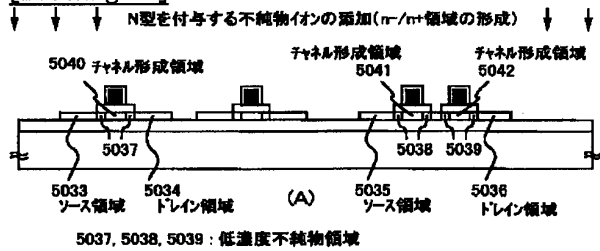
[Drawing 14]



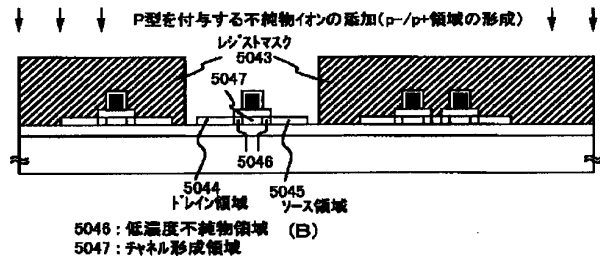
5013~5020 : 多孔性層酸化膜 5021~5024 : 無孔性層酸化膜



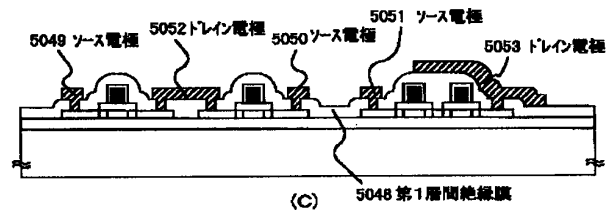
[Drawing 15]



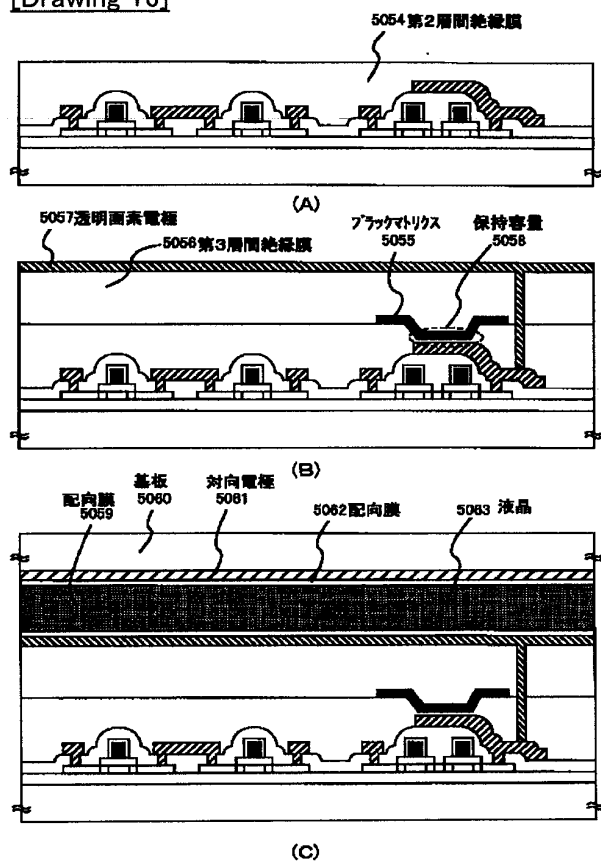
5037, 5038, 5039 : 低温度不純物領域



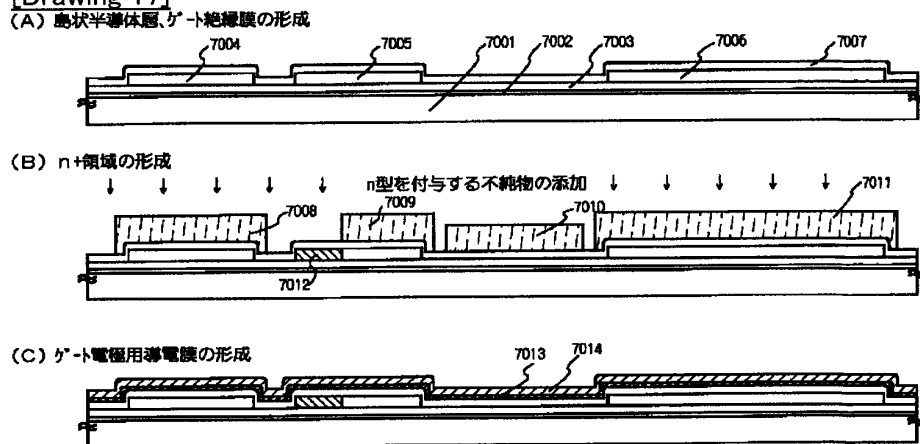
5046 : 低温度不純物領域
5047 : チャネル形成領域



[Drawing 16]

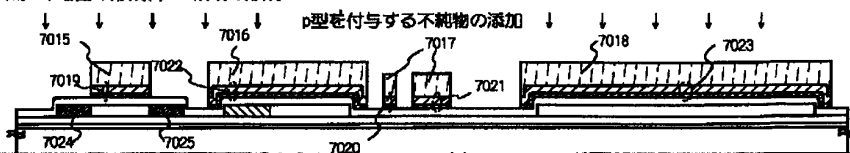


[Drawing 17]



[Drawing 18]

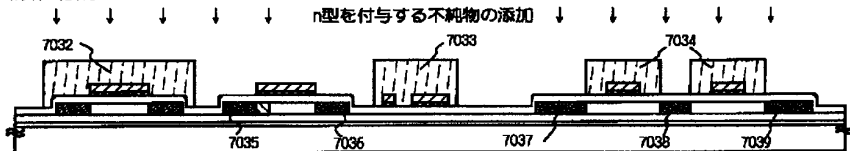
(A) p-チャネル電極の形成、p++領域の形成



(B) n-チャネル電極の形成

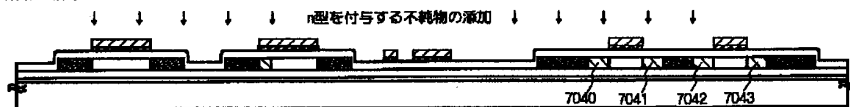


(C) n+領域の形成

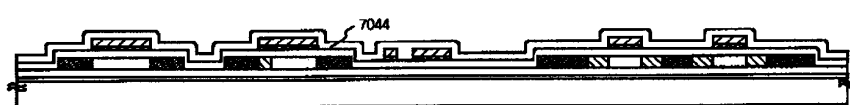


[Drawing 19]

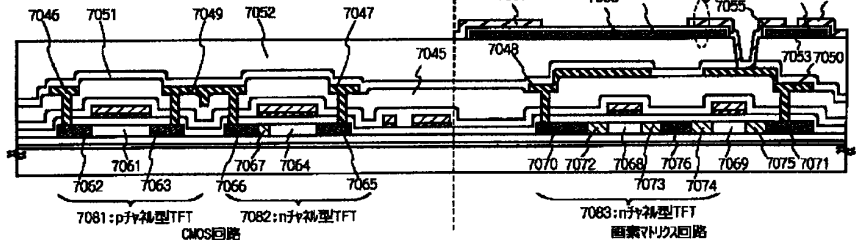
(A) n+領域の形成



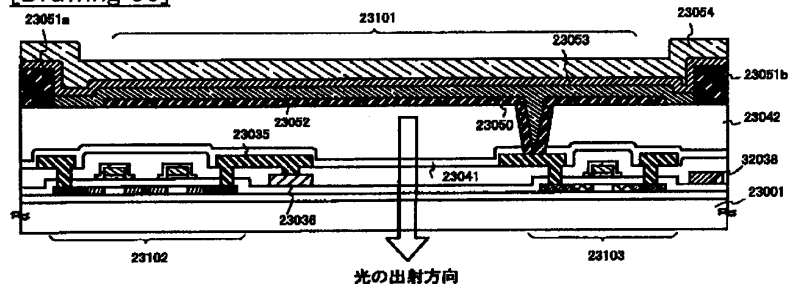
(B) 熱活性化



(C) 層間絶縁膜、ソース/ドレイン電極、画素電極、保持容量の形成

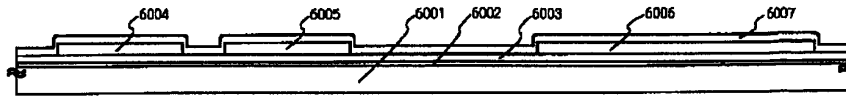
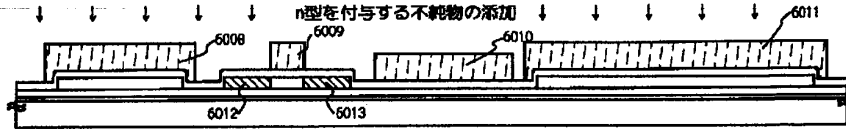


[Drawing 36]



[Drawing 20]

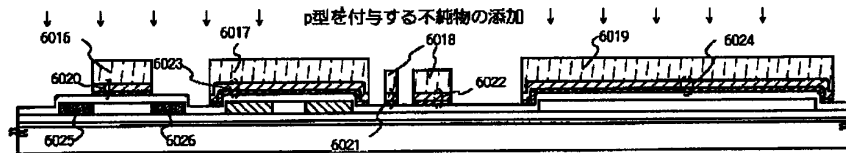
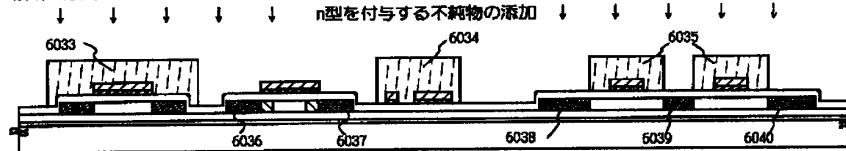
(A) 島状半導体層、ゲート絶縁膜の形成

(B) n⁺領域の形成

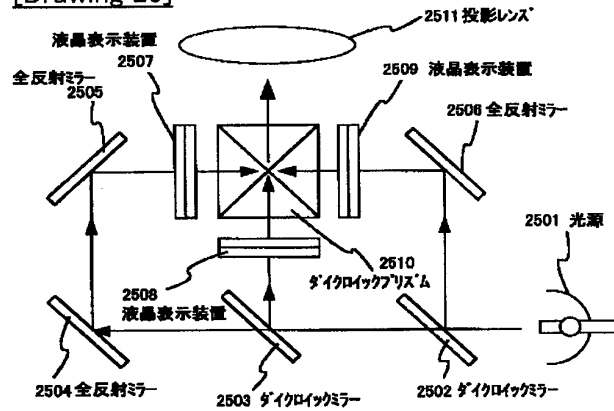
(C) ゲート電極用導電膜の形成



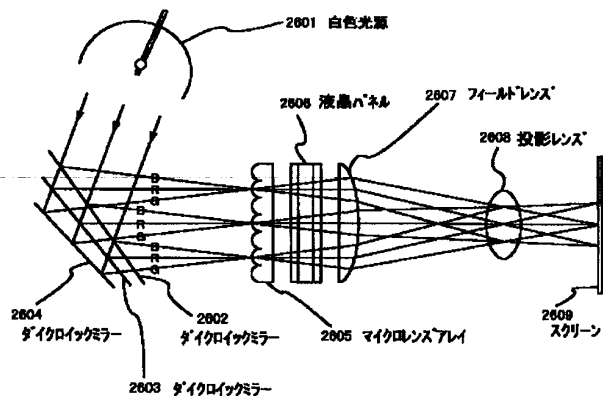
[Drawing 21]

(A) p-ch⁺ゲート電極の形成、p⁺⁺領域の形成(B) n-ch⁺ゲート電極の形成(C) n⁺領域の形成

[Drawing 25]



[Drawing 26]

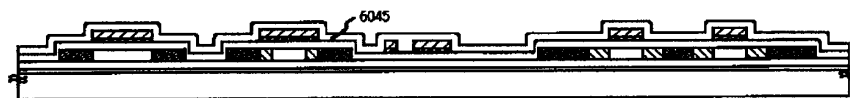


[Drawing 22]

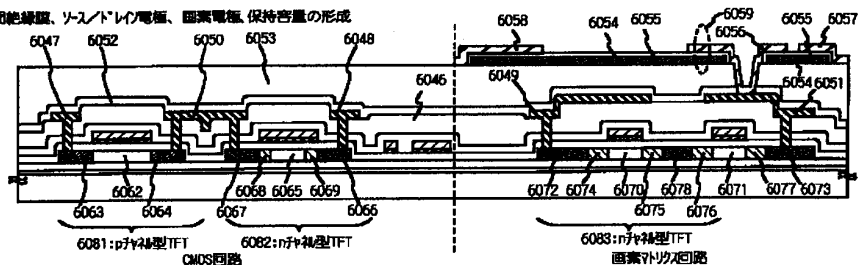
(A) n-領域の形成



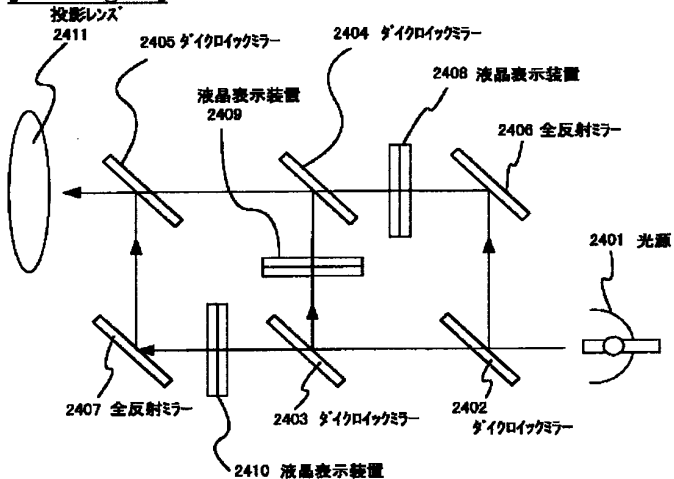
(B) 熱活性化



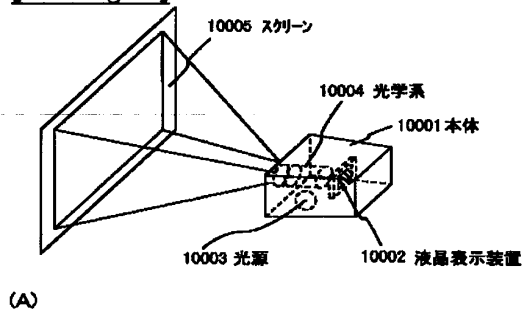
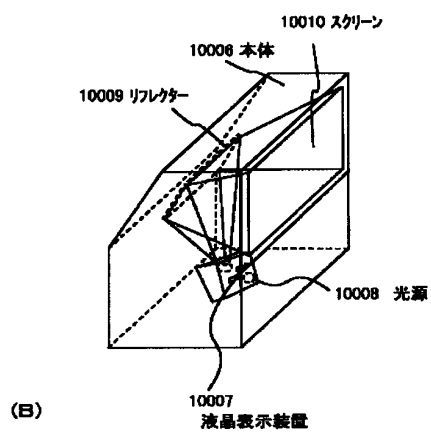
(C) 層間絶縁膜、ソース/ドレイン電極、画素電極、保持容量の形成



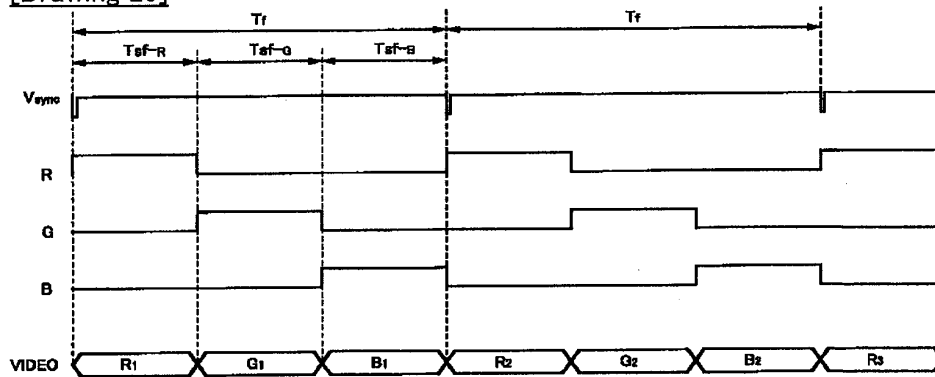
[Drawing 24]



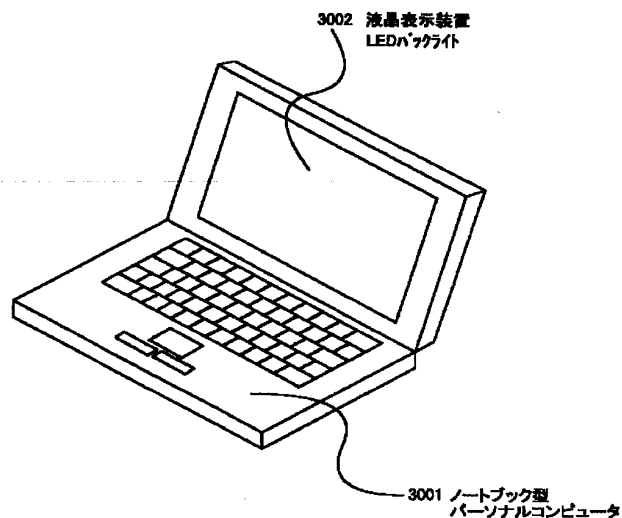
[Drawing 27]



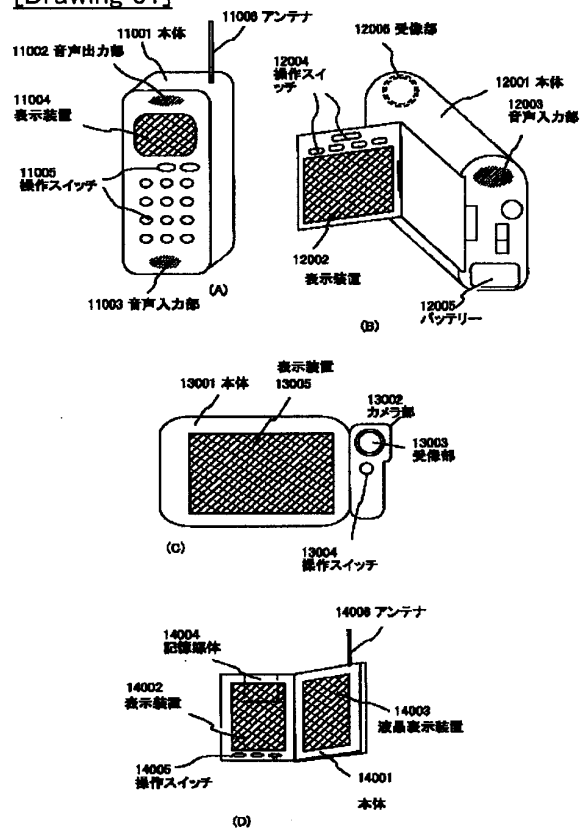
[Drawing 29]



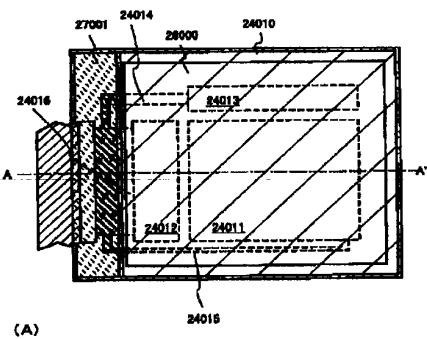
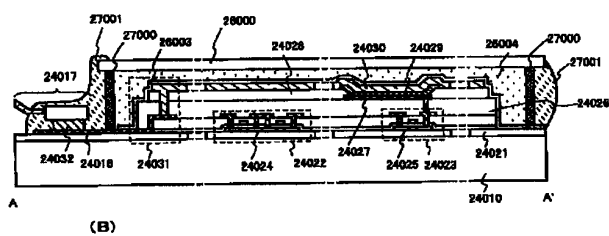
[Drawing 30]



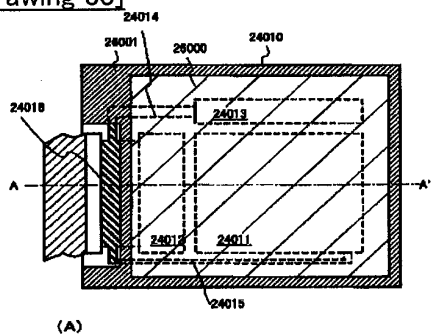
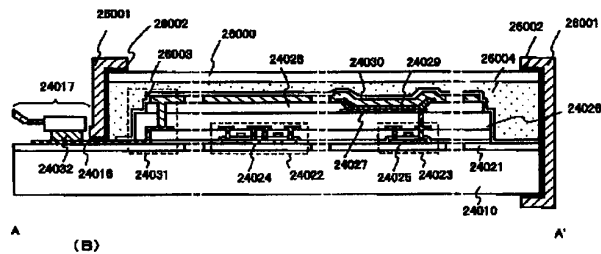
[Drawing 31]



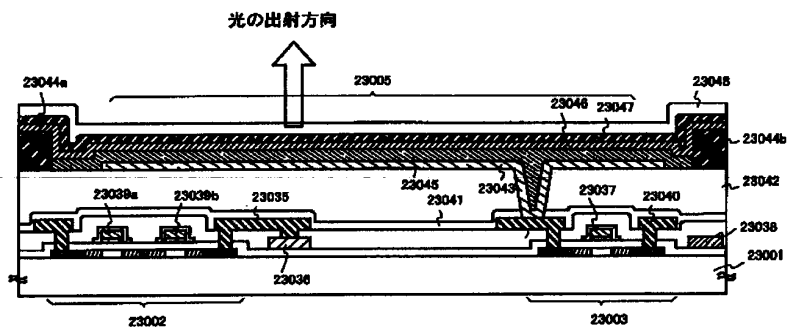
[Drawing 32]



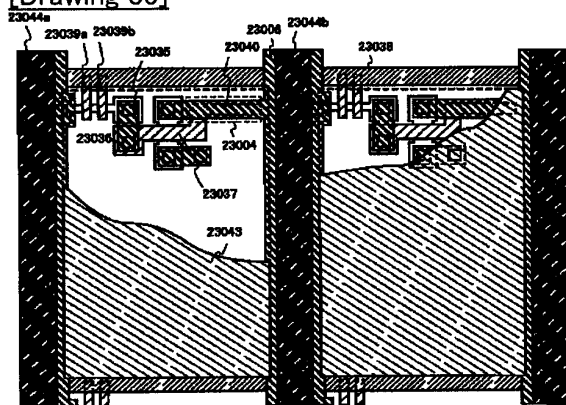
[Drawing 33]



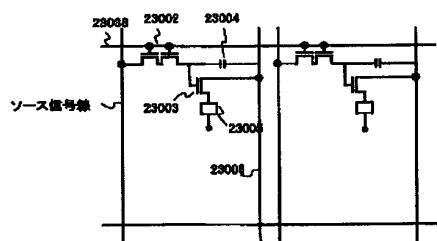
[Drawing 34]



[Drawing 35]

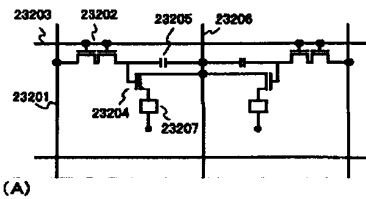


(A)

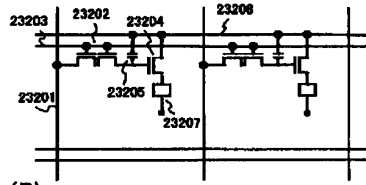


(B)

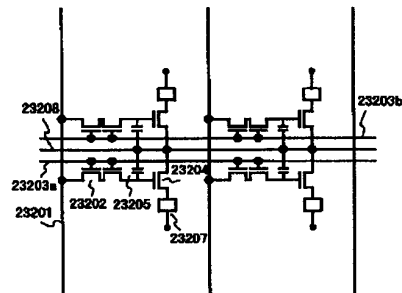
[Drawing 37]



(A)



(B)



(C)

[Translation done.]

*** NOTICES ***

JPO and INPIT are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

CORRECTION OR AMENDMENT

[Kind of official gazette] Printing of amendment by regulation of Patent Law Article 17 of 2
[Section Type] The 2nd Type of the part VI gate
[Publication date] Heisei 19(2007) April 5 (2007.4.5)

[Publication No.] JP,2000-310980,A (P2000-310980A)
[Date of Publication] Heisei 12(2000) November 7 (2000.11.7)
[Application number] Application for patent 2000-39258 (P2000-39258)
[International Patent Classification]

G09G 3/36 (2006. 01)

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G09F 9/30 (2006. 01)

G09G 3/20 (2006. 01)

G02F 1/1368 (2006. 01)

[FI]

G09G 3/36

G02F 1/133 550

G02F 1/133 575

G09F 9/30 338

G09G 3/20 641 K

G09G 3/20 641 A

G09G 3/20 641 C

G09G 3/20 641 E

G02F 1/1368

[Written Amendment]

[Filing date] Heisei 19(2007) February 9 (2007.2.9)

http://www4.ipdl.inpit.go.jp/cgi-bin/tran_web.cgi_ejje?atw_u=http%3A%2F%2Fwww4.i... 10/17/2011

[Amendment 1]

[Document to be Amended]Description

[Item(s) to be Amended]Claims

[Method of Amendment]Change

[The contents of amendment]

[Claim(s)]

[Claim 1]

An active matrix circuit where two or more picture element transistors have been arranged at matrix form,

It is a display device which has a source driver and a gate driver which drive said active matrix circuit,

Top n bits of a digital video data of m bit inputted from the outside are used as information on gradation voltage, a low rank $(m-n)$ bit is used as information on time gradation, and an image of one frame is formed,

A display device, wherein both m and n are two or more positive numbers and are $m > n$.

[Claim 2]

An active matrix circuit where two or more picture element transistors have been arranged at matrix form,

A source driver and a gate driver which drive said active matrix circuit,

It has a processing circuit,

Said processing circuit is a circuit (both m and n are two or more positive numbers and $m > n$) which changes n bit into a digital video data of n bit for gradation voltage among digital video datas of m bit inputted from the outside, and supplies a digital video data of the n bit concerned to said source driver,

A display device, wherein an image of one frame is formed using a digital video data of the n bit concerned, and a time gradation display by a subframe of a 2^{m-n} individual.

[Claim 3]

An active matrix circuit where two or more picture element transistors have been arranged at matrix form,

A source driver and a gate driver which drive said active matrix circuit,

It has a processing circuit,

Said processing circuit is a circuit (both m and n are two or more positive numbers and $m > n$) which changes n bit into a digital video data of n bit for gradation voltage among digital video datas of m bit inputted from the outside, and supplies a digital video data of the n bit concerned to said source driver,

A display device forming an image of one frame using a digital video data of the n bit concerned, and a time gradation display by a subframe of a 2^{m-n} individual, and obtaining a gradation display of a passage ($2^m - (2^{m-n} - 1)$).

[Claim 4]

An active matrix circuit where two or more picture element transistors have been arranged at matrix form,

It is a display device which has a source driver and a gate driver which drive said active matrix circuit,

Top n bits of a digital video data of m bit inputted from the outside are used as information on gradation voltage, a low rank $(m-n)$ bit is used as information on time gradation (both m and n are two or more positive numbers and $m > n$), and an image of one frame is formed,

A display device, wherein said source driver has a D/A conversion circuit which changes a digital video data of said n bit into analog gradation voltage.

[Claim 5]

An active matrix circuit where two or more picture element transistors have been arranged at

matrix form,

A source driver and a gate driver which drive said active matrix circuit,

It has a processing circuit,

Said processing circuit is a circuit (both m and n are two or more positive numbers and $m > n$) which changes n bit into a digital video data of n bit for gradation voltage among digital video datas of m bit inputted from the outside, and supplies a digital video data of the n bit concerned to said source driver,

Said source driver has a D/A conversion circuit which changes a digital video data of the n bit concerned into analog gradation voltage,

A display device, wherein an image of one frame is formed using said analog gradation voltage and a time gradation display by a subframe of a 2^{m-n} individual.

[Claim 6]

An active matrix circuit where two or more picture element transistors have been arranged at matrix form,

A source driver and a gate driver which drive said active matrix circuit,

It has a processing circuit,

Said processing circuit is a circuit (both m and n are two or more positive numbers and $m > n$) which changes n bit into a digital video data of n bit for gradation voltage among digital video datas of m bit inputted from the outside, and supplies a digital video data of the n bit concerned to said source driver,

Said source driver has a D/A conversion circuit which changes a digital video data of the n bit concerned into analog gradation voltage,

A display device forming an image of one frame using said analog gradation voltage and a time gradation display by a subframe of a 2^{m-n} individual, and obtaining a gradation display of a passage ($2^m - (2^{m-n} - 1)$).

[Claim 7]

An active matrix circuit where two or more picture element transistors have been arranged at matrix form,

A source driver and a gate driver which drive said active matrix circuit,

It has a processing circuit and a D/A conversion circuit,

Said processing circuit changes n bit into a digital video data of n bit for gradation voltage among digital video datas of m bit inputted from the outside (both m and n are two or more positive numbers and $m > n$),

Said D/A conversion circuit changes a digital video data of the n bit concerned into an analog video data, and inputs said analog video data into said source driver,

A display device, wherein an image of one frame is formed using the analog video data concerned and a time gradation display by a subframe of a 2^{m-n} individual.

[Claim 8]

An active matrix circuit where two or more picture element transistors have been arranged at matrix form,

A source driver and a gate driver which drive said active matrix circuit,

It has a processing circuit and a D/A conversion circuit,

Said processing circuit changes n bit into a digital video data of n bit for gradation voltage among digital video datas of m bit inputted from the outside (both m and n are two or more positive numbers and $m > n$),

Said D/A conversion circuit changes a digital video data of the n bit concerned into an analog video data, and inputs said analog video data into said source driver,

A display device forming an image of one frame using the analog video data concerned and a time gradation display by a subframe of a 2^{m-n} individual, and obtaining a gradation display of a passage

$$(2^m - (2^{m-n} - 1)).$$

[Translation done.]

Electronic Patent Application Fee Transmittal				
Application Number:	12917885			
Filing Date:	02-Nov-2010			
Title of Invention:	ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE			
First Named Inventor/Applicant Name:	Yojiro MATSUEDA			
Filer:	James Albert Oliff/Sheri Michals			
Attorney Docket Number:	114251.03			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with \$0 paid	1251	1	150	150

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for continued examination	1801	1	930	930
Total in USD (\$)				1080

Electronic Acknowledgement Receipt	
EFS ID:	11222724
Application Number:	12917885
International Application Number:	
Confirmation Number:	2374
Title of Invention:	ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE
First Named Inventor/Applicant Name:	Yojiro MATSUEDA
Customer Number:	25944
Filer:	James Albert Oliff/Sheri Michals
Filer Authorized By:	James Albert Oliff
Attorney Docket Number:	114251.03
Receipt Date:	19-OCT-2011
Filing Date:	02-NOV-2010
Time Stamp:	17:21:40
Application Type:	Utility under 35 USC 111(a)

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Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1080
RAM confirmation Number	3978
Deposit Account	150461
Authorized User	
<p>The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:</p> <p>Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)</p> <p>Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)</p>	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		11425103_RCE_Amend_PEOT.pdf	240578	yes	8
			17884e0f097b9ac5124f556fe1c035cfdb4520d0		
	Multipart Description/PDF files in .zip description				
	Document Description		Start		End
	Request for Continued Examination (RCE)		1		1
	Extension of Time		2		2
	Amendment Submitted/Entered with Filing of CPA/RCE		3		3
	Claims		4		5
	Applicant Arguments/Remarks Made in an Amendment		6		8
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	11425103_IDS.pdf	93207	no	3
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Information:					
Total Files Size (in bytes):			13592477		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2629

Application No.: 12/917,885

Examiner: D. BOLOTIN

Filed: November 2, 2010

Docket No.: 114251.03

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-
OPTICAL DEVICE, AND ELECTRONIC
DEVICE

MAIL STOP RCE

**LARGE ENTITY REQUEST FOR
CONTINUED EXAMINATION UNDER 37 C.F.R. §1.114**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. §1.114, Applicants hereby request continued examination.

☒ Applicants further request entry and consideration of the submission filed herewith.

The above-identified application was filed on or after June 8, 1995. Thus, entry is proper under 37 C.F.R. §1.114(d).

The fees associated with this filing are being paid electronically with this filing. The Commissioner is hereby authorized to charge any additional fee (or credit any overpayment) for this filing to Deposit Account No. 15-0461.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

John A. Radi
Registration No. 59,345

JAO:JAR/sam

Date: October 19, 2011

OLIFF & BERRIDGE, PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION Please grant any extension necessary for entry; Charge any fee due to our Deposit Account No. 15-0461
--

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Date October 19, 2011

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2629

Application No.: 12/917,885

Examiner: D. BOLOTIN

Filed: November 2, 2010

Docket No.: 114251.03

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC
DEVICE

**LARGE ENTITY PETITION FOR 1st - 3rd EXTENSION
OF TIME UNDER 37 C.F.R. §1.136(a) AND
TRANSMITTAL OF FEE UNDER 37 C.F.R. §1.17**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is a response to the outstanding Official Action in the above-identified patent application. The shortened statutory period having expired September 21, 2011, an extension of time for a period of one month is hereby requested.

The fees associated with this filing under 37 C.F.R. §1.136(a) are being paid electronically with this filing. The Commissioner is hereby authorized to charge any additional fee (or credit any overpayment) associated for this filing to Deposit Account No. 15-0461.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

John A. Radi
Registration No. 59,345

JAO:JAR/sam

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Telephone: (703) 836-6400

<p>DEPOSIT ACCOUNT USE AUTHORIZATION Please grant any extension necessary for entry; Charge any fee due to our Deposit Account No. 15-0461</p>
--

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2629

Application No.: 12/917,885

Examiner: D. BOLOTIN

Filed: November 2, 2010

Docket No.: 114251.03

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND
ELECTRONIC DEVICE

AMENDMENT WITH REQUEST FOR CONTINUED EXAMINATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the June 21, 2011 Office Action, and upon entry of the attached Petition for
Extension of Time and Request for Continued Examination, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An electro-optical device comprising:
 - a data line;
 - a control line; and
 - a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit comprising:
 - a first transistor;
 - an electro-optical element electrically connected to one of a source or a drain of the first transistor;
 - a second transistor connected between the one of the source or the drain and a gate of the first transistor; ~~and;~~
 - a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor according to a data signal; and
 - a wiring connected between a gate of the first transistor and the second transistor;
 - the first transistor supplying a current based on the gate voltage to the electro-optical element; ~~;~~
 - the wiring being formed in a layer which is different from a semiconductor layer in which the first transistor and the second transistor are formed; and
 - the wiring being formed in a layer different from a gate layer in which a gate of the first transistor formed.
 - ~~the first transistor having a single gate structure, and~~
 - ~~the second transistor having a multi-gate structure.~~

2. (Previously Presented) The electro-optical device according to claim 1, wherein the first transistor and the second transistor have opposite polarities.

3-10. (Cancelled)

11. (New) The electro-optical device according to claim 1, wherein the control line supplies a control signal to a gate of the second transistor, and the control line crosses the wiring.

12. (New) The electro-optical device according to claim 11, wherein the unit circuit further comprises a third transistor connected between the holding element and the data line, and wherein the second transistor and the third transistor are controlled according to the control signal.

13. (New) An electric device comprising an electro-optical device according to claim 1.

14. (New) An electric device comprising an electro-optical device according to claim 2.

15. (New) An electric device comprising an electro-optical device according to claim 11.

16. (New) An electric device comprising an electro-optical device according to claim 12.

REMARKS

Claims 1, 2 and 11-16 are pending in this application. By this Amendment, claim 1 is amended, claims 3-10 are cancelled without surrender or disclaimer of the subject matter recited therein, and claims 11-16 are added. No new matter is added.

An Information Disclosure Statement is being submitted concurrent with this Amendment. The Examiner is requested to consider the references cited therein and return a signed and initialed PTO-1449 indicated the same.

The Office Action rejects claims 1, 2 and 5-10 under 35 U.S.C. 103(a) as being obvious in view of Dawson et al. (U.S. Patent No. 6,229,506) in view of Yumoto (U.S. Patent No. 6,859,193); and claims 3 and 4 were rejected under 35 U.S.C. §103(a) as being obvious over Dawson in view of Yumoto and Koyama (U.S. Patent No. 7,277,070). Claims 3-10 have been canceled and the rejection of these claims is moot.

With regard to independent claim 1, the combination of Dawson, Yumoto and Koyama does not disclose or render obvious "a wiring connected between a gate of the first transistor and the second transistor ... the wiring being formed in a layer which is different from a semiconductor layer in which the first transistor and the second transistor are formed; and the wiring being formed in a layer different from a gate layer in which a gate of the first transistor formed." Dawson discloses in Fig. 2, a unit driving circuit for an organic EL element. In Dawson, a transistor (P2) 260, of which a gate is connected to a holding capacitor (Cs) 280 and a transistor (P1) 250, which is connected to a signal line 230, respectively, correspond to the first transistor and the second transistor. However, Dawson is silent as towards the layers on which the wiring is formed.

Fig. 8 of Yumoto discloses a unit driving circuit for an organic EL element. Yumoto is relied upon for teaching multi-gate structures, for example, TFT 2a/2b connected to the

organic EL element OLED and TFT 4a/4b connected to a holding capacitor C. Fig. 20 of Koyama, discloses a drive circuit that an organic EL element can be found that: (i) a wiring connecting the first transistor and the second transistor is formed on a layer other than the semiconductor layer; (ii) the wiring is formed on a layer different from a gate metal layer of the second transistor; and (iii) the first transistor and the second transistor are connected via a contact hole.

However, none of the above references teach or render obvious "a layer which is different from a semiconductor layer in which the first transistor and the second transistor are formed" and "a layer which is different from a gate layer in which a gate of the first transistor is formed."

Accordingly, because the applied references do not disclose or render obvious the features of amended claim 1, Applicant respectfully request that the rejection over these references should be withdrawn.

The newly added claims are patentable at least for their dependence on an allowable claim, as well as for the additional features recited therein.

CONCLUSION

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

John A. Radi
Registration No. 59,345

JAO:JAR/sam

Attachments:

Petition for Extension of Time
Request for Continued Examination
Information Disclosure Statement with References

Date: October 19, 2011

OLIFF & BERRIDGE, PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/917,885		Filing Date 11/02/2010		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.										
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	10/19/2011	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
Total (37 CFR 1.16(i))	*	8	Minus	** 20	=	0	OR	X \$60=	0	
Independent (37 CFR 1.16(h))	*	1	Minus	*** 3	=	0	OR	X \$250=	0	
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0	
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)		
Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =	OR	X \$ =			
Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =	OR	X \$ =			
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
/DAVINA G. BUTLER/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2629

Application No.: 12/917,885

Examiner: D. BOLOTIN

Filed: November 2, 2010

Docket No.: 114251.03

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC
DEVICE

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Further to an Information Disclosure Statement filed October 19, 2011 and pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

- ☒ 1. This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits after the filing of a Request for Continued Examination under 37 CFR §1.114. No certification or fee is required.
- ☒ 2. In accordance with 37 CFR §1.98(a)(2)(ii), copies of any U.S. patents and patent application publications are not attached.

- ☒ 3. Reference 1 corresponds to JP-A-2000-310980, which was previously disclosed in an Information Disclosure Statement on October 19, 2011.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

John A. Radi
Registration No. 59,345

JAO:JAR/mlh

Date: October 25, 2011

OLIFF & BERRIDGE, PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

<p>DEPOSIT ACCOUNT USE AUTHORIZATION Please grant any extension necessary for entry of this filing; Charge any fee due to our Deposit Account No. 15-0461</p>

Form PTO-1449 (REV. 5/11)	PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 114251.03	APPLICATION NO. 12/917,885
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT(S) Yojiro MATSUEDA	
		FILING DATE November 2, 2010	GROUP 2629

U.S. PATENT DOCUMENTS				
Examiner Initials	Cite No.	Document Number	Date	Name
	1	7,233,342 B1	6-19-2007	Yamazaki et al.

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation

OTHER DOCUMENTS		
Examiner Initials	Cite No.	Including name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.

EXAMINER	DATE CONSIDERED
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

Date: October 25, 2011

Electronic Acknowledgement Receipt	
EFS ID:	11259714
Application Number:	12917885
International Application Number:	
Confirmation Number:	2374
Title of Invention:	ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE
First Named Inventor/Applicant Name:	Yojiro MATSUEDA
Customer Number:	25944
Filer:	James Albert Oliff/Morgan Haugh
Filer Authorized By:	James Albert Oliff
Attorney Docket Number:	114251.03
Receipt Date:	25-OCT-2011
Filing Date:	02-NOV-2010
Time Stamp:	14:22:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	11425103_SupplIDS.pdf	77971 8bac3ee8db8e82ab182647e3f70913c4d89e0553	no	3

Warnings:

Information:

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Total Files Size (in bytes):

77971

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/917,885	11/02/2010	Yojiro MATSUEDA	114251.03	2374
25944 7590 11/02/2011 OLIFF & BERRIDGE, PLC P.O. BOX 320850 ALEXANDRIA, VA 22320-4850			EXAMINER BOLOTIN, DMITRIY	
			ART UNIT 2629	PAPER NUMBER
			NOTIFICATION DATE 11/02/2011	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OfficeAction25944@oliff.com
jarmstrong@oliff.com

DETAILED ACTION

It would be of great assistance to the Office if all incoming papers pertaining to a filed application carried the following items:

1. Application number (checked for accuracy, including series code and serial no.).
2. Group art unit number (copied from most recent Office communication).
3. Filing date.
4. Name of the examiner who prepared the most recent Office action.
5. Title of invention.
6. Confirmation number (See MPEP § 503).

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/19/2011 has been entered.

Status of Claims

2. **Claims 1, 2** have been amended, **claims 3 – 10** have been canceled, new **claims 11 – 16** have been added; and **claims 1, 2 and 11 – 16** are pending.

Terminal Disclaimer

3. The terminal disclaimer filed on 05/09/2011 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 7,483,001 has been reviewed and is approved.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1, 2, 13 and 14** are rejected under 35 U.S.C. 102(e) as being anticipated by Koyama (US 7,277,070).

As to **claim 1**, Koyama discloses an electro-optical device comprising: a data line (signal line Si of fig. 20); a control line (gate signal line Gaj of fig. 20); and a unit circuit arranged corresponding to an intersection of the data line and the control line (fig. 20), the unit circuit comprising: a first transistor (transistor 104 of fig. 20); an electro-optical element (pixel electrode 181 of fig. 20) electrically connected to one of a source or a drain of the first transistor (181 is electrically connected to 104 through transistor 105 of fig. 20); a second transistor connected between the one of the source or the drain and a gate of the first transistor (transistor 103 of fig. 20); and a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor

according to a data signal (capacitor 107 of fig. 20), and a wiring (184 of fig. 20) connected between a gate of the first transistor (185 of fig. 20) and the second transistor (103 of fig. 20) the first transistor supplying a current based on the gate voltage (TFT 104 is current controlling TFT (col. 27, line 60 – col. 28, line 20), inherently, TFT 104 is on based on voltage at the gate, inducing current through OLED) to the electro-optical element (181 of fig. 22), the wiring being formed in a layer which is different from a semiconductor layer in which the first transistor and the second transistor are formed (as shown in fig. 20, the wiring is not in semiconductor areas of either TFT 103 or TFT 104); and the wiring being formed in a layer different from a gate layer in which a gate of the first transistor formed (as shown in fig. 20, the wiring 184 and gate layer 185 are in different layers (col. 27, line 60 – col. 28, line 20)).

As to **claim 2** (dependent on 1), Koyama discloses the electro-optical device, wherein the first transistor and the second transistor have opposite polarities (second switching transistor TFT 103 may be n-channel and current controlling TFT may be p-channel, col. 9, lines 45 – 50).

As to **claim 13** (dependent on 1) and **claim 14** (dependent on 2), Koyama discloses an electric device comprising an electro-optic device (television of fig. 24A).

Allowable Subject Matter

6. **Claims 11, 12, 15 and 16** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

The Prior Art of record discloses the electro-optical device wherein the control line (gate line Gaj of fig. 20) supplies a control signal to a gate of the second transistor (103 of fig. 20), but fails to disclose that “*control line crosses the wiring*”.

Response to Arguments

8. Applicant's arguments with respect to **claims 1, 2 and 11 – 16** have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DMITRIY BOLOTIN whose telephone number is (571)270-5873. The examiner can normally be reached on Monday-Friday, 7:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571)272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DMITRIY BOLOTIN/
Examiner, Art Unit 2629

Notice of References Cited	Application/Control No. 12/917,885	Applicant(s)/Patent Under Reexamination MATSUEDA, YOJIRO	
	Examiner DMITRIY BOLOTIN	Art Unit 2629	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,277,070	10-2007	Koyama, Jun	345/76
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 12917885	Applicant(s)/Patent Under Reexamination MATSUEDA, YOJIRO
	Examiner DMITRIY BOLOTIN	Art Unit 2629

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant					☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE								
Final	Original	01/28/2011	06/07/2011	10/25/2011						
	1	✓	✓	✓						
	2	✓	✓	✓						
	3	✓	✓	-						
	4	✓	✓	-						
	5	✓	✓	-						
	6	✓	✓	-						
	7	✓	✓	-						
	8	✓	✓	-						
	9	✓	✓	-						
	10	✓	✓	-						
	11			O						
	12			O						
	13			✓						
	14			✓						
	15			O						
	16			O						

Receipt date: 10/19/2011

12917885 - GAU: 2629
Sheet 1 of 1

Form PTO-1449 (REV. 5/11) PATENT & TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY DOCKET NO. 114251.03	APPLICATION NO. 12/917,885
	APPLICANT(S) Yojiro MATSUEDA	
	FILING DATE November 2, 2010	GROUP 2629

U.S. PATENT DOCUMENTS				
Examiner Initials	Cite No.	Document Number	Date	Name
	1	6,118,506	09-12-2000	Yamazaki et al.
	2	5,815,226	09-29-1998	Yamazaki et al.
	3	2002/0070385 A1	06-13-2002	Yamagata
	4	2002/0030770 A1	03-14-2002	Tsutsui et al.
	5	6,271,543 B1	08-07-2001	Ohtani et al.

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
	6	EP 1 093 166 A2	04-18-2001	Europe		
	7	EP 1 093 156 A2	04-18-2001	Europe		
	8	EP 1 128 436 A1	08-29-2001	Europe		
	9	EP 1 096 579 A2	05-02-2001	Europe		
	10	JP-A-2000-310980	11-07-2000	Japan	X	X

OTHER DOCUMENTS		
Examiner Initials	Cite No.	Including name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
	11	
	12	
	13	
	14	
	15	
	16	

EXAMINER	/Dmitriy Bolotin/	DATE CONSIDERED	10/25/2011
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

Date: October 19, 2011

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.B./

Search Notes 	Application/Control No. 12917885	Applicant(s)/Patent Under Reexamination MATSUEDA, YOJIRO
	Examiner DMITRIY BOLOTIN	Art Unit 2629

SEARCHED			
Class	Subclass	Date	Examiner
345	76-83	1/28/2011	DB
315	169.1-169.4	1/28/2011	DB
	Updated Search	06/07/2011	DB
	Updated Search	10/25/2011	DB
349	42,43,46	10/25/2011	DB

SEARCH NOTES			
Search Notes		Date	Examiner
Google		1/28/2011	DB
EAST		1/28/2011	DB
Updated Search		06/07/2011	DB
Updated Search		10/25/2011	DB

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

/DMITRIY BOLOTIN/ Examiner.Art Unit 2629	
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Receipt date: 10/25/2011

12917885 - GAU: 2629

Sheet 1 of 1

Form PTO-1449 (REV. 5/11) PATENT & TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY DOCKET NO. 114251.03	APPLICATION NO. 12/917,885
	APPLICANT(S) Yojiro MATSUEDA	
	FILING DATE November 2, 2010	GROUP 2629

U.S. PATENT DOCUMENTS				
Examiner Initials	Cite No.	Document Number	Date	Name
	1	7,233,342 B1	6-19-2007	Yamazaki et al.

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation

OTHER DOCUMENTS		
Examiner Initials	Cite No.	Including name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.

EXAMINER /Dmitriy Bolotin/	DATE CONSIDERED 10/26/2011
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

Date: October 25, 2011 REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.B./

Receipt date: 08/04/2011

12917885 - GAU: 2629
Sheet 1 of 1

Form PTO-1449 (REV. 5/11) PATENT & TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY DOCKET NO. 114251.03	APPLICATION NO. 12/917,885
	APPLICANT(S) Yojiro MATSUEDA	
	FILING DATE November 2, 2010	GROUP 2629

U.S. PATENT DOCUMENTS				
Examiner Initials	Cite No.	Document Number	Date	Name
	1	2001/0017517	08/30/2001	Yamazaki

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation

OTHER DOCUMENTS		
Examiner Initials	Cite No.	Including name of the author (in CAPITAL LETTERS), title of the article (where appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume/issue number(s), publisher, city and/or country where published.
	2	July 11, 2011 Office Action issued in U.S. Patent Application No. 11/483,087.
	3	U.S. Patent Application No. 11/483,087.

EXAMINER	/Dmitriy Bolotin/	DATE CONSIDERED	10/25/2011
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

Date: August 4, 2011

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.B./

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2629

Application No.: 12/917,885

Examiner: D. BOLOTIN

Filed: November 2, 2010

Docket No.: 114251.03

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC
DEVICE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

- ☒ 1. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, Notice of Allowance or other action that closes prosecution (e.g., Quayle Action).
- ☒ a. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to my knowledge after making reasonable inquiry, no item of information in this Information Disclosure Statement was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(2).

- ☒ 2. An Office Action was issued in U.S. application No. 11/483,087. A copy of the Office Action is submitted for the Examiner's consideration as Reference 1. The references cited therein have already been made of record in this application.

Respectfully submitted,

Shahid Khan

James A. Oliff
Registration No. 27,075

Shahid K. Khan
Registration No. 60,984

JAO:SZK/amw

Date: December 9, 2011

OLIFF & BERRIDGE, PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

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Form PTO-1449 (REV. 1/06)		US Dept. of Commerce PATENT & TRADEMARK OFFICE		ATTY DOCKET NO. 114251.03		APPLICATION NO. 12/917,885	
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)				APPLICANT(S) Yojiro MATSUEDA			
				FILING DATE November 2, 2010		GROUP 2629	
U.S. PATENT DOCUMENTS							
Examiner Initials	Cite No.	Document Number	Date	Name			
FOREIGN PATENT DOCUMENTS							
Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation	
OTHER DOCUMENTS							
Examiner Initials	Cite No.	Including name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume/issue number(s), publisher, city and/or country where published.					
	1	Office Action issued in U.S. Patent Application No. 11/483,087 mailed November 10, 2011.					
EXAMINER					DATE CONSIDERED		
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

Date: December 9, 2011

Electronic Acknowledgement Receipt	
EFS ID:	11584293
Application Number:	12917885
International Application Number:	
Confirmation Number:	2374
Title of Invention:	ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE
First Named Inventor/Applicant Name:	Yojiro MATSUEDA
Customer Number:	25944
Filer:	James Albert Oliff/Amanda White
Filer Authorized By:	James Albert Oliff
Attorney Docket Number:	114251.03
Receipt Date:	09-DEC-2011
Filing Date:	02-NOV-2010
Time Stamp:	15:29:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	11425103_IDS12911.pdf	90166 07ec50290d33bc546744e0914af16259f5ff1e2f	no	3

Warnings:

Information:

This is not an USPTO supplied IDS fillable form					
2	Non Patent Literature	11425103_REF1.pdf	333549	no	9
			70d9b3be72d24a43f4a0bd70e7efe87f5b3dd250		
Warnings:					
Information:					
Total Files Size (in bytes):				423715	
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2629

Application No.: 12/917,885

Examiner: D. BOLOTIN

Filed: November 2, 2010

Docket No.: 114251.03

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND
ELECTRONIC DEVICE

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the November 2, 2011 Office Action, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An electro-optical device comprising:

a data line;

a control line; and

a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit ~~including~~ comprising:

_____ a first transistor ~~that includes a first semiconductor film;~~

_____ an electro-optical element electrically connected to one of a source or a drain of the first transistor;

_____ a second transistor ~~that includes a second semiconductor film, the second transistor~~ connected between the one of the source or the drain and a gate of the first transistor;

_____ a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor according to a data signal; and

_____ a wiring connected between ~~a gate of the first transistor and the second transistor and the gate of the first transistor;~~

the first transistor supplying a current based on the gate voltage to the electro-optical element;

the wiring being formed in a layer which is different from a ~~semiconductor layer in which the first semiconductor film and the second semiconductor film the first transistor and the second transistor are formed;~~ and

the wiring being formed in a layer different from a gate layer in which ~~a the~~ gate of the first transistor is formed.

2. (Currently Amended) The electro-optical device according to claim 1, wherein the first transistor has a conduction type different from a conduction film the second transistor has and the second transistor have opposite polarities.

11. (Currently Amended) The electro-optical device according to claim 1, wherein the control line supplies a control signal to a gate of the second transistor, and the control line ~~crosses~~ intersecting the wiring.

12. (Currently Amended) The electro-optical device according to claim 11, wherein the unit circuit further includes ~~comprises~~ a third transistor ~~connected~~ coupled between the holding element and the data line, and wherein the second transistor and the third transistor are controlled according to the control signal.

13. (Previously Presented) An electric device comprising an electro-optical device according to claim 1.

14. (Previously Presented) An electric device comprising an electro-optical device according to claim 2.

15. (Previously Presented) An electric device comprising an electro-optical device according to claim 11.

16. (Previously Presented) An electric device comprising an electro-optical device according to claim 12.

17. (New) An electro-optical device comprising:
a data line;
a control line
a power line; and
a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit including:

a first transistor that includes a first semiconductor film;
an electro-optical element electrically connected to one of a source or a drain of the first transistor;
a second transistor that includes a second semiconductor film, the second transistor connected between the one of the source or the drain and a gate electrode of the first transistor;
a holding element that is connected to the gate electrode of the first transistor and holds a gate voltage of the first transistor according to a data signal; and
a wiring connected between the gate electrode of the first transistor and the second transistor,
the first transistor supplying a current based on the gate voltage to the electro-optical element,
the wiring being formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film are formed, and
the wiring being formed in a layer different from a gate layer in which the gate electrode of the first transistor formed.

18. (New) An electro-optical device comprising:

a data line;
a control line
a power line; and
a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit including:
a first transistor that includes a first semiconductor film;
an electro-optical element electrically connected to one of a source or a drain of the first transistor;

a second transistor that includes a second semiconductor film, the second transistor connected between the one of a source or the drain and a gate electrode of the first transistor;

a holding element that is connected to the gate electrode of the first transistor and holds a gate voltage of the first transistor according to a data signal; and

a wiring connected between the gate electrode of the first transistor and the second transistor,

the first transistor supplying a current based on the gate voltage to the electro-optical element, and

the wiring being formed in a layer in which the data line and the power line are formed.

19. (New) The electro-optical device according to claim 17,

wherein the first transistor has a first terminal, a second terminal, and a channel region disposed between the first terminal and the second terminal, the first terminal being disposed between the power line and the second terminal, and

the first transistor controlling an electrical connection between the first terminal and the second terminal.

20. (New) The electro-optical device according to claim 18,

wherein the first transistor has a first terminal, a second terminal, and a channel region disposed between the first terminal and the second terminal, the first terminal being disposed between the power line and the second terminal, and

the first transistor controlling an electrical connection between the first terminal and the second terminal.

REMARKS

Claims 1, 2 and 11-20 are pending in this application. By this Amendment, claims 1, 2, 11 and 12 are amended and new claims 17-20 are added. Support for the amendments to claim 1 can be found in, for example, Figs. 3A, 6 and 9A of Applicant's specification. Support for the amendments to claim 2 can be found in, for example, page 25, lines 5-7, of Applicant's specification. Support for the amendments to claim 11 can be found in, for example, Fig. 2 of Applicant's specification. Support for the amendments to claim 12 can be found in, for example, Fig. 2 of Applicant's specification. No new matter is added. Entry of the amendments is thus respectfully requested.

I. Claim Rejections Under 35 U.S.C. §102(e)

The Office Action rejects claims 1, 2, 13 and 14 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 7,277,070 to Koyama. The rejection is respectfully traversed.

Koyama does not disclose "the wiring being formed in a layer different from a gate layer in which the gate of the first transistor is formed," as recited in claim 1. Specifically, the Examiner asserts that the wiring 184 and the gate layer 185 are illustrated in Koyama's Fig. 20 as being in different layers. Koyama describes Fig. 20 as disclosing "[t]he second switching TFT 103 has a source region and a drain region one of which is connected to the drain region of the current controlling TFT 104 through the connection wiring line 183 and the other of which is connected to a connection wiring line 184 and to a gate wiring line 185." See, Koyama, col. 27, line 65-col. 28, line 2. However, this description alone does not provide sufficient detail to determine whether the wiring connecting TFT 103 and the gate of the TFT 104 is either the connection wiring 184, the gate wiring line 185, or both the connection wiring 184 and the gate wiring line 185.

Fig. 20 indicates that the wiring connecting TFT 103 and the gate of the TFT 104 is the gate wiring line 185. Because Fig. 20 only illustrates a top view, we have to rely on the hatched layer markings to determine which layer the wiring lines are located in. To one of ordinary skill in the art, the square region pointed to by label 184 indicates a contact hole. This square region has hatching lines identical to those indicating the connection wiring line 103 and the power supply line V_i . Thus, Fig. 20 would indicate to one of ordinary skill in the art that the connection wiring line 184 is formed with the same metallic layer that forms the connection wiring 183 and the power supply line V_i and serves only to cover the contact hole. Therefore, Fig. 20 discloses that the wiring between TFT 103 and the gate of TFT 104 is the **gate wiring line 185**. Thus, Koyama does not anticipate "the wiring being formed in a layer different from a gate layer in which the gate of the first transistor is formed," as recited in claim 1.

Accordingly, the applied reference does not disclose all the features recited in claim 1. Therefore, Applicant respectfully requests withdrawal of the rejection.

Applicant does not concede that Koyama teaches or discloses the features of the other dependent claims. However, it is unnecessary to separately discuss the other dependent claims given the existence of clear distinguishing features in independent claim 1. Thus, Applicant respectfully requests withdrawal of the rejection with respect to the other dependent claims.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

Shahid Khan

James A. Oliff
Registration No. 27,075

Shahid K. Khan
Registration No. 60,984

JAO:SZK/rmh

Date: February 2, 2012

OLIFF & BERRIDGE, PLC
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Telephone: (703) 836-6400

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Electronic Acknowledgement Receipt	
EFS ID:	11987994
Application Number:	12917885
International Application Number:	
Confirmation Number:	2374
Title of Invention:	ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE
First Named Inventor/Applicant Name:	Yojiro MATSUEDA
Customer Number:	25944
Filer:	James Albert Oliff/Rockelle Hamilton
Filer Authorized By:	James Albert Oliff
Attorney Docket Number:	114251.03
Receipt Date:	02-FEB-2012
Filing Date:	02-NOV-2010
Time Stamp:	16:58:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		11425103_Amendment.pdf	258042 d737db	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	8
Warnings:			
Information:			
Total Files Size (in bytes):		258042	
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>			



UNITED STATES PATENT AND TRADEMARK OFFICE

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25944 e 2012-02-09

OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

Paper No.

Application No.:	12/917,885	Date Mailed:	2012-02-09
			
First Named Inventor:	MATSUEDA, Yojiro,	Examiner:	BOLOTIN, DMITRIY
Attorney Docket No.:	114251.03	Art Unit:	2629
Confirmation No.:	2374	Filing Date:	2010-11-02

Please find attached an Office communication concerning this application or proceeding.

Commissioner for Patents

Notice of Non-Compliant Amendment (37 CFR 1.121)	Application No. 12/917,885	Applicant(s) MATSUEDA, YOJIRO
		Art Unit 2800

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

The amendment document filed on _____ is considered non-compliant because it has failed to meet the requirements of 37 CFR 1.121 or 1.4. In order for the amendment document to be compliant, correction of the following item(s) is required.

THE FOLLOWING MARKED (X) ITEM(S) CAUSE THE AMENDMENT DOCUMENT TO BE NON-COMPLIANT:

- ☐ 1. Amendments to the specification:
 - ☐ A. Amended paragraph(s) do not include markings.
 - ☐ B. New paragraph(s) should not be underlined.
 - ☐ C. Other _____.
- ☐ 2. Abstract:
 - ☐ A. Not presented on a separate sheet. 37 CFR 1.72.
 - ☐ B. Other _____.
- ☐ 3. Amendments to the drawings:
 - ☐ A. The drawings are not properly identified in the top margin as "Replacement Sheet," "New Sheet," or "Annotated Sheet" as required by 37 CFR 1.121(d).
 - ☐ B. The practice of submitting proposed drawing correction has been eliminated. Replacement drawings showing amended figures, without markings, in compliance with 37 CFR 1.84 are required.
 - ☐ C. Other _____.
- ☐ 4. Amendments to the claims:
 - ☐ A. A complete listing of all of the claims is not present.
 - ☐ B. The listing of claims does not include the text of all pending claims (including withdrawn claims)
 - ☐ C. Each claim has not been provided with the proper status identifier, and as such, the individual status of each claim cannot be identified. Note: the status of every claim must be indicated after its claim number by using one of the following status identifiers: (Original), (Currently amended), (Canceled), (Previously presented), (New), (Not entered), (Withdrawn) and (Withdrawn-currently amended).
 - ☐ D. The claims of this amendment paper have not been presented in ascending numerical order.
 - ☐ E. Other: _____.
- ☐ 5. Other (e.g., the amendment is unsigned or not signed in accordance with 37 CFR 1.4): For further explanation of the amendment format required by 37 CFR 1.121, see MPEP § 714.

TIME PERIODS FOR FILING A REPLY TO THIS NOTICE:

1. Applicant is given **no new time period if the non-compliant amendment is an** after-final amendment or an amendment filed after allowance, or a drawing submission (only) If applicant wishes to resubmit the non-compliant after-final amendment with corrections, the **entire corrected amendment** must be resubmitted.
2. Applicant is given **one month**, or thirty (30) days, whichever is longer, from the mail date of this notice to supply the correction, if the non-compliant amendment is one of the following: a preliminary amendment, a non-final amendment (including a submission for a request for continued examination (RCE) under 37 CFR 1.114), a supplemental amendment filed within a suspension period under 37 CFR 1.103(a) or (c), and an amendment filed in response to a Quayle action. If any of above boxes 1 to 4 are checked, the correction required is only the corrected section of the non-compliant amendment in compliance with 37 CFR 1.121.

Extensions of time are available under 37 CFR 1.136(a) only if the non-compliant amendment is a non-final amendment or an amendment filed in response to a *Quayle* action.

Failure to timely respond to this notice will result in:

Abandonment of the application if the non-compliant amendment is a non-final amendment or an amendment filed in response to a *Quayle* action; or

Non-entry of the amendment if the non-compliant amendment is a preliminary amendment or supplemental amendment.

Legal Instruments Examiner (LIE), if applicable /Theresa Dawkins/

Telephone No: (571)272-1567

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/917,885		Filing Date 11/02/2010		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)		RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.										
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	02/02/2012	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 12	Minus	** 20	= 0	X \$ =		OR	X \$60=	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X \$ =		OR	X \$250=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
	TOTAL ADD'L FEE									
OR										
TOTAL ADD'L FEE										
0										
AMENDMENT										
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
	TOTAL ADD'L FEE									
OR										
TOTAL ADD'L FEE										
Legal Instrument Examiner: /Theresa Dawkins/										
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.										
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".										
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".										
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2629

Application No.: 12/917,885

Examiner: D. BOLOTIN

Filed: November 2, 2010

Docket No.: 114251.03

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND
ELECTRONIC DEVICE

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the November 2, 2011 Office Action, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An electro-optical device comprising:
 - a data line;
 - a control line; and
 - a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit including:
 - a first transistor that includes a first semiconductor film;
 - an electro-optical element electrically connected to one of a source or a drain of the first transistor;
 - a second transistor that includes a second semiconductor film, the second transistor connected between the one of the source or the drain and a gate of the first transistor;
 - a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor according to a data signal; and
 - a wiring connected between the second transistor and the gate of the first transistor,
 - the first transistor supplying a current based on the gate voltage to the electro-optical element,
 - the wiring being formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film are formed, and
 - the wiring being formed in a layer different from a gate layer in which the gate of the first transistor is formed.

2. (Currently Amended) The electro-optical device according to claim 1, wherein the first transistor has a conduction type different from a conduction film the second transistor has.

3-10. (Canceled)

11. (Currently Amended) The electro-optical device according to claim 1, wherein the control line supplies a control signal to a gate of the second transistor, the control line intersecting the wiring.

12. (Currently Amended) The electro-optical device according to claim 11, wherein the unit circuit further includes a third transistor coupled between the holding element and the data line, and wherein the second transistor and the third transistor are controlled according to the control signal.

13. (Previously Presented) An electric device comprising an electro-optical device according to claim 1.

14. (Previously Presented) An electric device comprising an electro-optical device according to claim 2.

15. (Previously Presented) An electric device comprising an electro-optical device according to claim 11.

16. (Previously Presented) An electric device comprising an electro-optical device according to claim 12.

17. (New) An electro-optical device comprising:

a data line;

a control line;

a power line; and

a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit including:

a first transistor that includes a first semiconductor film;

an electro-optical element electrically connected to one of a source or a drain of the first transistor;

a second transistor that includes a second semiconductor film, the second transistor connected between the one of the source or the drain and a gate electrode of the first transistor;

a holding element that is connected to the gate electrode of the first transistor and holds a gate voltage of the first transistor according to a data signal; and

a wiring connected between the gate electrode of the first transistor and the second transistor,

the first transistor supplying a current based on the gate voltage to the electro-optical element,

the wiring being formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film are formed, and

the wiring being formed in a layer different from a gate layer in which the gate electrode of the first transistor formed.

18. (New) An electro-optical device comprising:

a data line;

a control line;

a power line; and

a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit including:

a first transistor that includes a first semiconductor film;

an electro-optical element electrically connected to one of a source or a drain of the first transistor;

a second transistor that includes a second semiconductor film, the second transistor connected between the one of a source or the drain and a gate electrode of the first transistor;

a holding element that is connected to the gate electrode of the first transistor and holds a gate voltage of the first transistor according to a data signal; and

a wiring connected between the gate electrode of the first transistor and the second transistor,

the first transistor supplying a current based on the gate voltage to the electro-optical element, and

the wiring being formed in a layer in which the data line and the power line are formed.

19. (New) The electro-optical device according to claim 17,

wherein the first transistor has a first terminal, a second terminal, and a channel region disposed between the first terminal and the second terminal, the first terminal being disposed between the power line and the second terminal, and

the first transistor controlling an electrical connection between the first terminal and the second terminal.

20. (New) The electro-optical device according to claim 18,

wherein the first transistor has a first terminal, a second terminal, and a channel region disposed between the first terminal and the second terminal, the first terminal being disposed between the power line and the second terminal, and

the first transistor controlling an electrical connection between the first terminal and the second terminal.

REMARKS

Claims 1, 2 and 11-20 are pending in this application. By this Amendment, claims 1, 2, 11 and 12 are amended and new claims 17-20 are added. Support for the amendments to claim 1 can be found in, for example, Figs. 3A, 6 and 9A of Applicant's specification. Support for the amendments to claim 2 can be found in, for example, page 25, lines 5-7, of Applicant's specification. Support for the amendments to claim 11 can be found in, for example, Fig. 2 of Applicant's specification. Support for the amendments to claim 12 can be found in, for example, Fig. 2 of Applicant's specification. No new matter is added. Entry of the amendments is thus respectfully requested.

I. Claim Rejections Under 35 U.S.C. §102(e)

The Office Action rejects claims 1, 2, 13 and 14 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 7,277,070 to Koyama. The rejection is respectfully traversed.

Koyama does not disclose "the wiring being formed in a layer different from a gate layer in which the gate of the first transistor is formed," as recited in claim 1. Specifically, the Examiner asserts that the wiring 184 and the gate layer 185 are illustrated in Koyama's Fig. 20 as being in different layers. Koyama describes Fig. 20 as disclosing "[t]he second switching TFT 103 has a source region and a drain region one of which is connected to the drain region of the current controlling TFT 104 through the connection wiring line 183 and the other of which is connected to a connection wiring line 184 and to a gate wiring line 185." See, Koyama, col. 27, line 65-col. 28, line 2. However, this description alone does not provide sufficient detail to determine whether the wiring connecting TFT 103 and the gate of the TFT 104 is either the connection wiring 184, the gate wiring line 185, or both the connection wiring 184 and the gate wiring line 185.

Fig. 20 indicates that the wiring connecting TFT 103 and the gate of the TFT 104 is the gate wiring line 185. Because Fig. 20 only illustrates a top view, we have to rely on the hatched layer markings to determine which layer the wiring lines are located in. To one of ordinary skill in the art, the square region pointed to by label 184 indicates a contact hole. This square region has hatching lines identical to those indicating the connection wiring line 103 and the power supply line V_i . Thus, Fig. 20 would indicate to one of ordinary skill in the art that the connection wiring line 184 is formed with the same metallic layer that forms the connection wiring 183 and the power supply line V_i and serves only to cover the contact hole. Therefore, Fig. 20 discloses that the wiring between TFT 103 and the gate of TFT 104 is the **gate wiring line 185**. Thus, Koyama does not anticipate "the wiring being formed in a layer different from a gate layer in which the gate of the first transistor is formed," as recited in claim 1.

Accordingly, the applied reference does not disclose all the features recited in claim 1. Therefore, Applicant respectfully requests withdrawal of the rejection.

Applicant does not concede that Koyama teaches or discloses the features of the other dependent claims. However, it is unnecessary to separately discuss the other dependent claims given the existence of clear distinguishing features in independent claim 1. Thus, Applicant respectfully requests withdrawal of the rejection with respect to the other dependent claims.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

Shahid K. Khan
Registration No. 60,984

JAO:SZK/mjb

Date: March 9, 2012

OLIFF & BERRIDGE, PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

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Electronic Acknowledgement Receipt	
EFS ID:	12271487
Application Number:	12917885
International Application Number:	
Confirmation Number:	2374
Title of Invention:	ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE
First Named Inventor/Applicant Name:	Yojiro MATSUEDA
Customer Number:	25944
Filer:	James Albert Oliff/Megan Bowers
Filer Authorized By:	James Albert Oliff
Attorney Docket Number:	114251.03
Receipt Date:	09-MAR-2012
Filing Date:	02-NOV-2010
Time Stamp:	16:54:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Amendment_030912.pdf	247373 f049cf5d193bb5c4dab9c1a58ca4e2deb97a6499	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	8
Warnings:			
Information:			
Total Files Size (in bytes):		247373	
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>			



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/917,885	11/02/2010	Yojiro MATSUEDA	114251.03	2374
25944 7590 03/27/2012 OLIFF & BERRIDGE, PLC P.O. BOX 320850 ALEXANDRIA, VA 22320-4850			EXAMINER BOLOTIN, DMITRIY	
			ART UNIT 2629	PAPER NUMBER
			NOTIFICATION DATE 03/27/2012	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OfficeAction25944@oliff.com
jarmstrong@oliff.com

Notice of Non-Compliant Amendment (37 CFR 1.121)	Application No.	Applicant(s)
	12/917,885	MATSUEDA, YOJIRO
	Examiner	Art Unit
	DMITRIY BOLOTIN	2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

The amendment document filed on 09 March 2012 is considered non-compliant because it has failed to meet the requirements of 37 CFR 1.121 or 1.4. In order for the amendment document to be compliant, correction of the following item(s) is required.

THE FOLLOWING MARKED (X) ITEM(S) CAUSE THE AMENDMENT DOCUMENT TO BE NON-COMPLIANT:

- ☐ 1. Amendments to the specification:
 - ☐ A. Amended paragraph(s) do not include markings.
 - ☐ B. New paragraph(s) should not be underlined.
 - ☐ C. Other _____.
- ☐ 2. Abstract:
 - ☐ A. Not presented on a separate sheet. 37 CFR 1.72.
 - ☐ B. Other _____.
- ☐ 3. Amendments to the drawings:
 - ☐ A. The drawings are not properly identified in the top margin as "Replacement Sheet," "New Sheet," or "Annotated Sheet" as required by 37 CFR 1.121(d).
 - ☐ B. The practice of submitting proposed drawing correction has been eliminated. Replacement drawings showing amended figures, without markings, in compliance with 37 CFR 1.84 are required.
 - ☐ C. Other _____.
- ☒ 4. Amendments to the claims:
 - ☐ A. A complete listing of all of the claims is not present.
 - ☐ B. The listing of claims does not include the text of all pending claims (including withdrawn claims)
 - ☒ C. Each claim has not been provided with the proper status identifier, and as such, the individual status of each claim cannot be identified. Note: the status of every claim must be indicated after its claim number by using one of the following status identifiers: (Original), (Currently amended), (Canceled), (Previously presented), (New), (Not entered), (Withdrawn) and (Withdrawn-currently amended).
 - ☐ D. The claims of this amendment paper have not been presented in ascending numerical order.
 - ☐ E. Other: _____.
- ☒ 5. Other (e.g., the amendment is unsigned or not signed in accordance with 37 CFR 1.4):
 Claims 1, 2, 11 and 12 indicate that they were amended, however no underlined amended portion is present.

For further explanation of the amendment format required by 37 CFR 1.121, see MPEP § 714.

TIME PERIODS FOR FILING A REPLY TO THIS NOTICE:

1. Applicant is given **no new time period** if the non-compliant amendment is an after-final amendment or an amendment filed after allowance. If applicant wishes to resubmit the non-compliant after-final amendment with corrections, the **entire corrected amendment** must be resubmitted.
2. Applicant is given **one month**, or thirty (30) days, whichever is longer, from the mail date of this notice to supply the correction, if the non-compliant amendment is one of the following: a preliminary amendment, a non-final amendment (including a submission for a request for continued examination (RCE) under 37 CFR 1.114), a supplemental amendment filed within a suspension period under 37 CFR 1.103(a) or (c), and an amendment filed in response to a *Quayle* action. If any of above boxes 1. to 4. are checked, the correction required is only the **corrected section** of the non-compliant amendment in compliance with 37 CFR 1.121.

Extensions of time are available under 37 CFR 1.136(a) only if the non-compliant amendment is a non-final amendment or an amendment filed in response to a *Quayle* action.

Failure to timely respond to this notice will result in:

- Abandonment** of the application if the non-compliant amendment is a non-final amendment or an amendment filed in response to a *Quayle* action; or
- Non-entry** of the amendment if the non-compliant amendment is a preliminary amendment or supplemental amendment.

/ABBAS ABDULSELAM/ Primary Examiner, Art Unit 2629	
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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2629

Application No.: 12/917,885

Examiner: D. BOLOTIN

Filed: November 2, 2010

Docket No.: 114251.03

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND
ELECTRONIC DEVICE

RESPONSE TO NOTICE OF NON-COMPLIANT AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Notice of Non-Compliant Amendment mailed March 27, 2012

(copy attached), please consider the following:

Remarks.

REMARKS

The Notice of Non-Compliant Amendment mailed on March 27, 2012, indicated that the amendment document filed on March 9, 2012 was non-compliant because claims 1, 2, 11 and 12 were indicated as amended, but the claims were not marked up. In response to the Notice, attached hereto is an Amendment in accordance with 37 C.F.R. 1.4. Applicant earnestly solicits favorable consideration and prompt allowance of the pending claims.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, Applicant invites the Examiner to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

Shahid Khan

James A. Oliff
Registration No. 27,075

Shahid K. Khan
Registration No. 60,984

JAO:SZK/mdl

Attachments:

Notice of Non-Compliant Amendment
Amendment

Date: April 26, 2012

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/91 7,885	11/02/2010	Yojiro MATSUEDA	114251.03	2374

25944	7590	03/27/2012
OLIFF & BERRIDGE, PLC P.O. BOX 320850 ALEXANDRIA, VA 22320-4850		

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MAR 27 2012

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EXAMINER	
BOLOTIN, DMITRIY	
ART UNIT	PAPER NUMBER
2629	
NOTIFICATION DATE	DELIVERY MODE
03/27/2012	ELECTRONIC

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OfficeAction25944@oliff.com
jarnstrong@oliff.com

DUE DATE

APR 27 2012

DOCKETED
By BSM on 03/22/2012
and
By W/O on 3/27/2012
Oliff & Berridge

Notice of Non-Compliant Amendment (37 CFR 1.121)	Application No.	Applicant(s)
	12/917,885	MATSUEDA, YOJIRO
	Examiner	Art Unit
	DMITRIY BOLOTIN	2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

The amendment document filed on 09 March 2012 is considered non-compliant because it has failed to meet the requirements of 37 CFR 1.121 or 1.4. In order for the amendment document to be compliant, correction of the following item(s) is required.

THE FOLLOWING MARKED (X) ITEM(S) CAUSE THE AMENDMENT DOCUMENT TO BE NON-COMPLIANT:

- ☐ 1. Amendments to the specification:
 - ☐ A. Amended paragraph(s) do not include markings.
 - ☐ B. New paragraph(s) should not be underlined.
 - ☐ C. Other _____.
- ☐ 2. Abstract:
 - ☐ A. Not presented on a separate sheet. 37 CFR 1.72.
 - ☐ B. Other _____.
- ☐ 3. Amendments to the drawings:
 - ☐ A. The drawings are not properly identified in the top margin as "Replacement Sheet," "New Sheet," or "Annotated Sheet" as required by 37 CFR 1.121(d).
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 - ☐ C. Other _____.
- ☒ 4. Amendments to the claims:
 - ☐ A. A complete listing of all of the claims is not present.
 - ☐ B. The listing of claims does not include the text of all pending claims (including withdrawn claims)
 - ☒ C. Each claim has not been provided with the proper status identifier, and as such, the individual status of each claim cannot be identified. Note: the status of every claim must be indicated after its claim number by using one of the following status identifiers: (Original), (Currently amended), (Canceled), (Previously presented), (New), (Not entered), (Withdrawn) and (Withdrawn-currently amended).
 - ☐ D. The claims of this amendment paper have not been presented in ascending numerical order.
 - ☐ E. Other: _____.
- ☒ 5. Other (e.g., the amendment is unsigned or not signed in accordance with 37 CFR 1.4):
 Claims 1, 2, 11 and 12 indicate that they were amended, however no underlined amended portion is present.

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Failure to timely respond to this notice will result in:

- Abandonment** of the application if the non-compliant amendment is a non-final amendment or an amendment filed in response to a *Quayle* action; or
- Non-entry** of the amendment if the non-compliant amendment is a preliminary amendment or supplemental amendment.

/ABBAS ABDULSELAM/ Primary Examiner, Art Unit 2629	
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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2629

Application No.: 12/917,885

Examiner: D. BOLOTIN

Filed: November 2, 2010

Docket No.: 114251.03

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND
ELECTRONIC DEVICE

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the November 2, 2011 Office Action, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An electro-optical device comprising:
 - a data line;
 - a control line; and
 - a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit ~~including~~ comprising:
 - _____ a first transistor that includes a first semiconductor film;
 - _____ an electro-optical element electrically connected to one of a source or a drain of the first transistor;
 - _____ a second transistor that includes a second semiconductor film, the second transistor connected between the one of the source or the drain and a gate of the first transistor;
 - _____ a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor according to a data signal; and
 - _____ a wiring connected between ~~a gate of the first transistor and the second transistor and the gate of the first transistor;~~
 - the first transistor supplying a current based on the gate voltage to the electro-optical element,;
 - the wiring being formed in a layer which is different from a ~~semiconductor~~ layer in which the first semiconductor film and the second semiconductor film ~~the first transistor and the second transistor~~ are formed,; and
 - the wiring being formed in a layer different from a gate layer in which ~~a the~~ gate of the first transistor is formed.

2. (Currently Amended) The electro-optical device according to claim 1, wherein the first transistor has a conduction type different from a conduction film the second transistor has~~and the second transistor have opposite polarities.~~

3-10. (Canceled)

11. (Currently Amended) The electro-optical device according to claim 1, wherein the control line supplies a control signal to a gate of the second transistor, ~~and the control line crosses~~intersecting the wiring.

12. (Currently Amended) The electro-optical device according to claim 11, wherein the unit circuit further includes~~comprises~~ a third transistor ~~connected~~coupled between the holding element and the data line, and wherein the second transistor and the third transistor are controlled according to the control signal.

13. (Previously Presented) An electric device comprising an electro-optical device according to claim 1.

14. (Previously Presented) An electric device comprising an electro-optical device according to claim 2.

15. (Previously Presented) An electric device comprising an electro-optical device according to claim 11.

16. (Previously Presented) An electric device comprising an electro-optical device according to claim 12.

17. (New) An electro-optical device comprising:

a data line;

a control line;

a power line; and

a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit including:

a first transistor that includes a first semiconductor film;

an electro-optical element electrically connected to one of a source or a drain of the first transistor;

a second transistor that includes a second semiconductor film, the second transistor connected between the one of the source or the drain and a gate electrode of the first transistor;

a holding element that is connected to the gate electrode of the first transistor and holds a gate voltage of the first transistor according to a data signal; and

a wiring connected between the gate electrode of the first transistor and the second transistor,

the first transistor supplying a current based on the gate voltage to the electro-optical element,

the wiring being formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film are formed, and

the wiring being formed in a layer different from a gate layer in which the gate electrode of the first transistor formed.

18. (New) An electro-optical device comprising:

a data line;

a control line;

a power line; and

a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit including:

a first transistor that includes a first semiconductor film;

an electro-optical element electrically connected to one of a source or a drain of the first transistor;

a second transistor that includes a second semiconductor film, the second transistor connected between the one of a source or the drain and a gate electrode of the first transistor;

a holding element that is connected to the gate electrode of the first transistor and holds a gate voltage of the first transistor according to a data signal; and

a wiring connected between the gate electrode of the first transistor and the second transistor,

the first transistor supplying a current based on the gate voltage to the electro-optical element, and

the wiring being formed in a layer in which the data line and the power line are formed.

19. (New) The electro-optical device according to claim 17,

wherein the first transistor has a first terminal, a second terminal, and a channel region disposed between the first terminal and the second terminal, the first terminal being disposed between the power line and the second terminal, and

the first transistor controlling an electrical connection between the first terminal and the second terminal.

20. (New) The electro-optical device according to claim 18,

wherein the first transistor has a first terminal, a second terminal, and a channel region disposed between the first terminal and the second terminal, the first terminal being disposed between the power line and the second terminal, and

the first transistor controlling an electrical connection between the first terminal and the second terminal.

REMARKS

Claims 1, 2 and 11-20 are pending in this application. By this Amendment, claims 1, 2, 11 and 12 are amended and new claims 17-20 are added. Support for the amendments to claim 1 can be found in, for example, Figs. 3A, 6 and 9A of Applicant's specification. Support for the amendments to claim 2 can be found in, for example, page 25, lines 5-7, of Applicant's specification. Support for the amendments to claim 11 can be found in, for example, Fig. 2 of Applicant's specification. Support for the amendments to claim 12 can be found in, for example, Fig. 2 of Applicant's specification. No new matter is added. Entry of the amendments is thus respectfully requested.

I. Claim Rejections Under 35 U.S.C. §102(e)

The Office Action rejects claims 1, 2, 13 and 14 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 7,277,070 to Koyama. The rejection is respectfully traversed.

Koyama does not disclose "the wiring being formed in a layer different from a gate layer in which the gate of the first transistor is formed," as recited in claim 1. Specifically, the Examiner asserts that the wiring 184 and the gate layer 185 are illustrated in Koyama's Fig. 20 as being in different layers. Koyama describes Fig. 20 as disclosing "[t]he second switching TFT 103 has a source region and a drain region one of which is connected to the drain region of the current controlling TFT 104 through the connection wiring line 183 and the other of which is connected to a connection wiring line 184 and to a gate wiring line 185." See, Koyama, col. 27, line 65-col. 28, line 2. However, this description alone does not provide sufficient detail to determine whether the wiring connecting TFT 103 and the gate of the TFT 104 is either the connection wiring 184, the gate wiring line 185, or both the connection wiring 184 and the gate wiring line 185.

Fig. 20 indicates that the wiring connecting TFT 103 and the gate of the TFT 104 is the gate wiring line 185. Because Fig. 20 only illustrates a top view, we have to rely on the hatched layer markings to determine which layer the wiring lines are located in. To one of ordinary skill in the art, the square region pointed to by label 184 indicates a contact hole. This square region has hatching lines identical to those indicating the connection wiring line 103 and the power supply line V_i . Thus, Fig. 20 would indicate to one of ordinary skill in the art that the connection wiring line 184 is formed with the same metallic layer that forms the connection wiring 183 and the power supply line V_i and serves only to cover the contact hole. Therefore, Fig. 20 discloses that the wiring between TFT 103 and the gate of TFT 104 is the gate wiring line 185. Thus, Koyama does not anticipate "the wiring being formed in a layer different from a gate layer in which the gate of the first transistor is formed," as recited in claim 1.

Accordingly, the applied reference does not disclose all the features recited in claim 1. Therefore, Applicant respectfully requests withdrawal of the rejection.

Applicant does not concede that Koyama teaches or discloses the features of the other dependent claims. However, it is unnecessary to separately discuss the other dependent claims given the existence of clear distinguishing features in independent claim 1. Thus, Applicant respectfully requests withdrawal of the rejection with respect to the other dependent claims.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

Shahid Khan

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JAO:SZK/mdl

Date: April 26, 2012

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PATENT APPLICATION

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DEVICE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

- ☒ 1. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, Notice of Allowance or other action that closes prosecution (e.g., Quayle Action).
- ☒ a. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to my knowledge after making reasonable inquiry, no item of information in this Information Disclosure Statement was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(2).
- ☒ 2. Each item of information contained in this Information Disclosure Statement was either first cited in a communication from a patent office in a counterpart foreign or international application or from the USPTO, or is a communication that was issued by a patent office in a counterpart foreign or international application or by the USPTO, and this communication was not received by any individual designated in §1.56(c) more than thirty days prior to the filing of this Information Disclosure Statement.
- ☒ 3. One or more reference cited herein was cited in a counterpart foreign application. An English language version of the foreign search report is attached for the Examiner's

information as Reference. See reference 8

- ☒ 4. In accordance with 37 CFR §1.98(a)(2)(ii), copies of any U.S. patents and patent application publications are not attached.
- ☒ 5. An English language Abstract of one or more non-English language reference is included. See References 6 and 7.
- ☒ 6. A computer-generated English language translation of one or more Japanese Patent Publication cited herein has been obtained from the website of the Japanese Patent Office (<http://www.jpo.go.jp>), and is attached, but has not been reviewed for accuracy. See References 6 and 7.
- ☒ 7. References 1 and 2 correspond to references 3 and 4, respectively.
- ☒ 8. JP-A-2000-214800, U.S. 6,307,528 and U.S. 6,781,155 were previously cited in an Information Disclosure Statement filed November 2, 2010.
- ☒ 9. Reference 5 corresponds to U.S. 6,225,750, which was previously cited in an Information Disclosure Statement filed November 2, 2010.

Respectfully submitted,

Shahid Khan

James A. Oliff
Registration No. 27,075

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JAO:SZK/mdl

Date: April 26, 2012

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Modified Form PTO-1449 (REV. 5/11) PATENT & TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY DOCKET NO. 114251.03	APPLICATION NO. 12/917,885
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	FILING DATE November 2, 2010	GROUP 2629

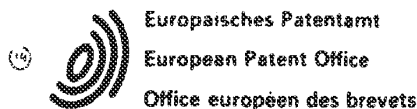
U.S. PATENT DOCUMENTS				
Examiner Initials	Cite No.	Document Number	Date	Name
	1	5,144,288 A	09/01/1992	Hamada et al.
	2	7,368,868 B2	05/06/2008	Sakamoto

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
	3	EP 0158366 A2	10/16/1985	Europe		
	4	EP 1594347 A1	11/09/2005	Europe		
	5	EP 1024472	08/02/2000	Europe		
	6	JP-A-10-12377	01/16/1998	Japan	X	X
	7	JP-A-2001-85162	03/30/2001	Japan	X	X

OTHER DOCUMENTS		
Examiner Initials	Cite No.	Including name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
	8	March 28, 2012 Search Report issued in European Patent Application No. 10191880.3
	9	Lungu G. Et al.: "Thin Film Active Matrix Organic Electroluminescent Display Development", University/Government/Industry Microelectronics Symposium, 1997 IEEE; pages 165-168

EXAMINER	DATE CONSIDERED
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

Date: April 26, 2011



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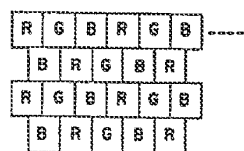
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(54) Color liquid-crystal display apparatus.

(57) The present invention relates to picture elements of a color liquid-crystal display apparatus, color arrangements of coloring means, and the electric control. The arrangement patterns of picture-element electrodes are provided which may be driven by a simple driving circuit and may obtain the regenerative images of high quality. In the color liquid-crystal display apparatus, the delta arrangement is adopted, thus improving the image resolution and the display quality.

Fig. 1(A)



EP 0 158 366 A2

COLOR LIQUID-CRYSTAL DISPLAY APPARATUSBACKGROUND OF THE INVENTION

The present invention relates to picture elements of a color liquid-crystal display apparatus, color arrangements of coloring means, and electric control.

5 The color liquid-crystal display apparatus is provided with many picture elements arranged in dot-matrix shape and a coloring means arranged corresponding to each picture element. Each picture element is controlled through application of a picture signal corresponding to a color
10 corresponding to each picture element so that colors are additively mixed in accordance with the same principle as that of a color CRT, with the result that an arbitrary color picture including a half tone color image may be displayed. Read "Liquid-Crystal Electronics Base And Application" (Ohm
15 Company, 1979) or the like edited by Sasaki for details on the liquid crystal.

 Many modes such as twisted-nematic (TN), guest-host (GH), dynamic-scattering-mode (DSM), phase transfer, etc. are available as an operation mode of a liquid crystal
20 display apparatus. Particularly the TN and GH provide favorable results. In the guest-host, black die is used and is operated as a so-called black shutter.

Normally additive three primary colors are selected as the colors of the coloring means. An interference filter, a color filter made of inorganic or organic dye or pigment are used in the coloring means. The coloring means may be provided on the outer face of a substrate which constitutes a liquid crystal display apparatus or on the inner face thereof. In the case of the latter, the coloring means may be provided on or below a signal electrode, a scanning electrode, a picture element electrode or a common electrode.

In the color liquid crystal display apparatus, only the spectrum region of one color of three primary colors among the spectra of the incident light can be used and the remaining region are absorbed by the coloring means. In the case of a liquid crystal operation mode using a polarizer, the light intensity to be used is further reduced by half so that it is very dark in a reflection type mode with no illuminating means in it. Thus, a light source such as incandescent lamp, fluorescent lamp, EL (Electro-luminescence) panel or the like is provided or a means for guiding ambient lights to the rear face of the liquid crystal display apparatus are provided as the illuminating means. For application into a portable appliance, it is important to improve the radiation efficiency of the light source because of the severe restriction in power capacity. To faithfully reproduce

picture signals, many picture element, i.e., many scanning lines are required. For example, a liquid crystal panel for color television use will be considered. In the NTSC system of a television broadcasting, the band width of luminance signal (Y signal) is 4MH_z , while the band widths of I signal and Q signal which are color phase signals are respectively 1.5MH_z , 5.0MH_z . As the sine waves of the 0.5MH_z includes 26.5 cycle waves in the 1 effective horizontal scanning period (53 microseconds), the horizontal resolution is equivalent to 53 lines or 26.5 line pair of bright line and dark line. According to the theorem of Shanon, the loss of the information to be contained in the original signal cannot be caused if the sampling operation is performed with a frequency twice the highest frequency of the original signal. However, it is difficult to say that the images provided when the signals sampled in that manner have been reproduced as they are are visually faithful to the original signal under the influences of aliasing. As the result of our experiment the visual satisfaction is provided when the sampling has been performed with a frequency higher than three times the highest frequency. Accordingly, to reproduce the color signal of 0.5MH_z , the information having the original signal can be reproduced almost faithfully if the number of the picture elements of the same color on the same horizontal line is 80 and more.

In a liquid crystal display apparatus provided with many picture element, one of the following three methods is used to individually control the respective picture elements.

5 (1) SIMPLE MATRIX

As shown graphically in Fig. 7 (a), a stripe shaped electrode group is provided respectively on the two opposite substrate. They are sealed each other so that they become normal to each other so as to constitute a liquid
10 crystal display. Row selection signals are sequentially applied upon the row electrodes (scanning electrodes) SL, SL disposed on one substrate. An image signal is applied in synchronous relation with a row selection signal upon the column electrodes (signal electrodes) DL, DL disposed on the
15 other substrate. The overlap regions (which are shown by oblique lines) between the row electrodes SL and the column electrodes DL become picture elements and the liquid crystal sandwiched between both the electrodes responses to the potential difference between them.

20 As the liquid crystal responses to the effective value in this method, the number of the scanning lines cannot be rendered large because of crosstalk, dynamic range.

To overcome such restriction as described
25 hereinabove, multiple matrix is devised. This is a method of increasing the number of the picture elements in a

scanning electrode direction instead of increasing the number of the scanning electrodes, by deformation of the signal electrode of the simple matrix. (Read "Liquid-Crystal Electronics Base And Application" (Ohm Company, 1979) edited by Sasaki).

Liquid crystal apparatuses of duplex matrix and quadruplex matrix are now put on the market or being manufactured for trial. In the duplex matrix graphically shown in Fig. 7 (B), the number of the scanning electrodes SE is kept the same as before, the number of the signal electrodes DL is rendered twice, the number of the picture elements (which are shown by oblique lines), and the adjacent two rows of picture elements are simultaneously scanned.

As the shape of the signal electrode becomes complicated to produce the narrow wiring-width portion in the multiplex matrix, the wiring resistance is likely to become high. When the wiring resistance of transparent conductive film only cannot be made sufficiently low, metallic wirings are jointly used. When the metallic wirings are used, effective picture element area reduces to make the picture face dark. Also, once the multiplex degree increases, the area of the wiring portion becomes relatively large to reduce the effective picture-element area.

25

Also, the following two systems which are effective when the number of the picture elements is many are developed.

(2) ADDITION OF NONLINEAR ELEMENT

5 There is a method of adding to each picture element a nonlinear element, such as varister, back-to-back diode, MIM (metal / insulator / metal) or the like, as an element to surpress the crosstalk. As shown graphically in Fig. 7 (C), picture element electrodes PE corresponding to
10 the respective picture elements are provided and are connected respectively with the signal electrodes DL through the nonlinear elements NL. The scanning electrodes SL, SL are disposed, on the opposite substrate, in a direction normal to the signal electrode DL. As shown in oblique
15 lines, the picture element is located in the overlapped portion between the picture element PE and the scanning electrode SL.

(3) ADDITION OF SWITCHING ELEMENT

 This is a method of adding a switching transistor,
20 as an active element, to each picture element to individually drive it. As shown graphically in Fig. 7 (D), a picture element electrode PE corresponding to each picture element is provided and is connected with a signal electrode DL through a switching element SW. Scanning electrodes SL,
25 SL are provided in a direction normal to the signal electrode DL and are connected with the gate of the

switching element SW. On the other hand, a common electrode
CE is provided on its opposite substrate. The picture
element is provided on an overlapped portion between the
picture electrode PE and the common electrode CE as shown in
5 oblique lines. A storage capacitor is added when necessary.
A driving voltage is applied and the capacity is charged
during a selection period, and the applied voltage is held
by the capacitor even during a non-selection period. As the
liquid crystal itself is also capacitive load and its time
10 constant of discharge is sufficiently larger than a repeated
period of the driving, the storage capacitor can be omitted.
A thin film transistor, a MOS-FET formed on silicon wafer or
the like is used as a switching transistor.

Although not shown concretely in the
15 above-description, a color filter is disposed corresponding
to each picture element in a color liquid-crystal display
apparatus.

The present invention is applied even to any one
of the above-described ways.

20 The color arrangement which is the subject of the
present invention will be described hereinafter. A color
liquid-crystal display apparatus using the liquid crystal is
already disclosed in such as Japanese Patent Publication
Tokkaisho No. 49-57726 and U.S. Patent No. 3,840,695. A XY
25 matrix display apparatus using three primary colors of
stripe-shaped color-filter is disclosed in the former and a

matrix display apparatus with a thin film transistor (TFT) being provided per picture element electrode is disclosed in the latter. In these examples, described only the use of the three primary colors of stripe-shaped or mosaic-shaped color filter is described without any concrete mention of the three primary colors of arrangement method in the color arrangement. Also, in the conventional TFT matrix display substrate, the signal electrode and the scanning electrode which are connected with the column of the picture element and the row thereof were rectilinear, and all the picture-element electrodes were arranged on the same side of an intersecting point between the corresponding signal electrode and scanning electrode.

The conventional color arrangement (see Fig. 8) is largely divided into a stripe shape and a mosaic shape. In the stripe-shaped color arrangement of the former, picture elements are arranged in parallel like longitudinal stripe (Fig. 8 (A)) and lateral stripe (Fig. 8 (B)). In the mosaic-shaped color arrangement of the latter, square or rectangular picture elements are arranged in checkers shape. Nine picture-element staircase shape (Fig. 8 (C)), longitudinal six picture-element type (Fig. 8 (D)), lateral six picture-element type (Fig. 8 (E)), four picture-element type (Fig. 8 (F)), etc. and their modifications are taken into consideration. Referring to Fig. 8, reference characters R, G, B respectively show the red, green, blue of

additive three primary colors, and a parenthesis { shows a basic period of the arrangement pattern of three colors (R, G, B). The six picture-element type and the four picture-element type are proposed by the present inventors
5 (Patent Application, No. 58-242548, etc.).

When the picture elements sufficient enough to faithfully reproduce the picture signals are provided in number, the color arrangement of the picture elements does not give influences to the quality of the reproduced images.
10 But when the number of the picture elements is not sufficiently large, the quality of the reproduced images is badly affected by the color arrangement. In the case of the stripe-shaped color arrangement, the color switching of the driving signal is not necessary in the longitudinal stripe
15 and all you have to do in the lateral stripe is to switch the color for each of the scanning lines before the analog line memory, but the spatial resolution in a direction normal to the stripe is inferior as many as three picture element pitch thus causing Moire stripes easily. Also, in a
20 condition where the white balance is filled, the brightness of the blue is so low in terms of the visibility characteristics that the blue looks extremely dark. Thus, blue lines look like black stripe patterns, thus spoiling the picture quality. On the other hand, in the case of
25 mosaic-shaped color arrangement, in the nine picture-element staircase type, the same color of picture elements are

obliquely connected in the staircase. The spatial resolution in a direction normal to its connection direction becomes $3/\sqrt{2}$ picture elements pitch, thus reducing the above-described disadvantage somewhat, but the color switching of the picture signal is required for each of the signal electrodes and each of scanning electrodes.

To improve such disadvantages as described hereinabove, the inventors of this case have proposed the color arrangement of the six picture-element type and four picture-element type. In the six picture-element type, the blue lines become zigzag, which makes the stripe patterns less conspicuous. In the four picture-element type, the green picture-elements are arranged in chequered patterns, and the spatial resolution becomes one picture-element pitch both longitudinally and laterally, and becomes $\sqrt{2}$ picture-element pitch even in the worst oblique direction, thus resulting in considerably small anisotropy. As the blue pictures are arranged separately, no dark lines are produced. The vision has characteristics that the spatial resolution with respect to brilliance (brightness) is high, but the spatial resolution with respect to the color difference is not so high. In the contribution towards the brilliance, the green among the red, green, blue is largest. Accordingly, if the green picture element faithfully reproduces a brilliance signal (Y signal), the image quality

is not deteriorated even if the space resolution is half as much as the green in the red and blue picture elements.

However, in the mosaic-shaped color arrangement, the resolution and the reproduced image quality are improved, but the driving circuit of the picture element is complicated. Namely, as described hereinabove, the colors of the picture element to be driven by the same signal electrode are two or three, thus requiring the color switching of the picture signal.

Fig. 9 (A), (B) are connection diagrams in a case where the liquid crystal is driven with a thin film transistor (TFT) of the conventional mosaic-shaped picture element arrangement. All the picture-element electrodes are arranged on the same side of an intersecting point between the corresponding signal electrode and the scanning electrode. Drain electrode of TFT 1, 1, ... and the storage capacitors which are provided when necessary are connected with the picture element electrodes arranged in mosaic shape (not shown). In the drawing, the capacitors 2, 2, ... are equivalent circuits showing the capacity of the liquid crystal and the point of each arrow is connected commonly to a common electrode. Each scanning electrode (gate line) 3 is connected with the gates of the TFT 1, 1, ... arranged laterally. Also, each of the signal electrodes (data line) 4 is connected with the source electrodes of the TFT 1, 1, ... arranged longitudinally. A gate driver 5 composed of a

shift register sequentially scans the scanning electrodes 3, 3 periodically with scanning pulses (horizontal synchronizing signal H) to turn on the TFT 1, 1, ... connected with the selected scanning electrode 3. Picture
5 signals applied upon the signal electrodes in synchronous relation to it are applied upon the picture-element electrodes (not shown) and the capacitors 2, 2, ... through the TFT 1, 1, ..., whereby the liquid crystal is driven. The capacitors 2, 2 maintains the voltage to be applied upon
10 the liquid crystal during a time period with the TFT 1, 1, ... off. When the time constant of the liquid crystal is sufficiently large as compared with the scanning period, the storage capacitor is not required to be provided in particular.

15 In the conventional mosaic-shaped color arrangement, picture elements of two colors or three colors are connected to the same signal electrode 4 to apply a signal (red, green, blue) corresponding to each color to a signal electrode 4. Each picture element selects only the
20 corresponding signal through the periodic scanning operation of the scanning electrodes 3, 3, As a result, a circuit which periodically switches the signals (red, green, blue) is required. In Fig. 8 (A). each picture signal of the Red, Green, Blue is respectively inputted into analog
25 line memories so that the picture signal of each color sampled is inputted into a color switching circuit 7

provided for each of the signal electrodes 4, thereby selecting a signal corresponding to the color arrangement. Here, the analog line memory 6 samples a color picture-signal R, G or B to output a signal in synchronous relation to the scanning electrode. In Fig. 8 (B), before the picture signal is inputted to an analog line memory 6, each picture signal of the R, G, B is time-shared in accordance with the color arrangement by a color switching circuit 7, is converted into a serial signal and is sent into an analog line memory 6.

SUMMARY OF THE INVENTION

An object of the present invention is to provide arrangement patterns of picture-element electrodes which may be driven by a simple driving circuit and may obtain the regenerative images of high quality.

The present inventors have found out that this object can be achieved by the adoption of delta arrangement.

The color liquid crystal display apparatus of the present invention is provided with picture elements corresponding to the intersecting points between the respective signal elements and scanning electrodes, and a coloring means of three colors, red, green, blue disposed corresponding to each of the above-described picture elements so that a picture element corresponding to the red, green or blue and a coloring means corresponding to it are so arranged that rectilinear arrangements each having three

colors of red, green, blue periodically arranged as one period may be rendered adjacent in parallel and shifted by half a period.

And each picture element which is composed of the
5 above-described one line of rectilinear arrangement
corresponding to the arrangement of the picture element is
controlled by one scanning electrode and the same color of
picture elements composing the adjacent two lines from among
the lines of the same color of picture elements arranged in
10 a direction vertical to the rectilinear arrangement are
connected directly or through the non-linear element or the
switching element to the same signal electrode. Or each
picture element constituting the above-described one line of
rectilinear arrangement is connected to the same signal
15 electrode, and the same color of picture elements
constituting the adjacent two lines among the lines of the
same color of picture elements arranged at a 1.5
picture-element pitch in a direction vertical to this
rectilinear arrangement are controlled by one scanning
20 electrode.

Or each one line or each two lines of the
respective picture-elements constituting the above-described
rectilinear arrangement are controlled by the same scanning
electrodes, and the same color of picture-element electrodes
25 are connected every other line directly to the same signal

electrode or through the non-linear element or a switching element.

BRIEF DESCRIPTION OF THE DRAWINGS

5 This object and other objects and features of the present invention will become apparent from the following description taken in conjunction with the preferred embodiment thereof with reference to the accompanying drawings, in which;

10 Fig. 1 (A), (B) are views each showing an example of the delta arrangement to be used in the present invention,

Fig. 1 (C) is a view showing the relationship between the electrodes and the delta arrangement,

Fig. 2 (A) is a plan view of TFT,

15 Fig. 2 (B) is a cross-sectional view taken along a line A - A,

Fig. 3 (A), (B) are plan views of TFT,

Fig. 4 is a driving circuit diagram of picture-element electrodes of the color arrangement in the embodiment of a color liquid-crystal display apparatus with
20 TFT added thereto,

Fig. 5 (A), (B) are views each showing graphically the embodiment of the present invention with respect to simple matrix and double matrix,

25 Fig. 6 (A), (B), (C) are views respectively graphically showing embodiments of simple matrix, double

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matrix, double matrix with non-linear elements added thereto,

Fig. 7 (A), (B), (C), (D) are views graphically showing a system of displaying various matrixes, wherein (A) shows simple matrix, (B) double matrix, (C) double matrix with non-linear elements added thereto, (D) double matrix with switching elements added thereto,

Fig. 8 (A), (B), (C), (D), (E), (F) are views showing the conventional color arrangements, wherein (A) shows a longitudinal stripe type, (B) a lateral stripe type, (C) a nine picture-element staircase type, (D) a longitudinal six picture-element type, (E) a lateral six picture-element type, (F) a four picture-element type, and

Fig. 9 (A), (B) are respectively connection diagrams in the case where the liquid crystal is driven by the thin film transistor (TFT) panel of the conventional mosaic-shaped picture-element arrangement.

DETAILED DESCRIPTION OF THE INVENTION

Before the description of the present invention proceeds, it is to be noted that like parts are designated by like reference numerals throughout the accompanying drawings.

(EMBODIMENT)

In the present invention, a delta arrangement is adopted as the color arrangement. It is known that the delta arrangement is least in the direction dependency

property of the spatial resolution. Namely, the regenerative images of high quality can be realized through adoption of the delta arrangement. The color arrangement of the color filter and the arrangement of the picture elements corresponding to it are provided in delta arrangement. In the delta arrangement, three colors of red, green, blue are periodically arranged rectilinearly and the adjacent rectilinear arrangements are shifted by half a period in a parallel direction to each other. In Fig. 1 (A) and Fig. 1 (B), the shape of the picture element is rectangular and hexagonal respectively. The gravity center of each color is arranged in an equilateral triangle. Assume that the ratio between the height of the triangle and the base thereof is $\sqrt{3}/2$ and the position of the gravity center of each picture element is in an equilateral triangle. The same color of picture elements are arranged symmetrically in six faces when the same color of picture elements only are taken into consideration. Also, the line of the same color of picture element is arranged every other line in a direction vertical to the rectilinear arrangement and the line of the same color of picture elements in this vertical direction has a space of 1.5 pitch (half a period) in the lateral direction and is shifted by one picture-element portion in the longitudinal direction.

In the present embodiment, to simplify the driving circuit of the picture elements, the signal electrodes are

caused to meander in the crank shape or in the curve shape so that the amplitude may become one half of the picture element pitch as shown in Fig. 1 (C), and the picture elements (B in Fig. 1 (C)) to be driven by the same scanning electrode are arranged right and left alternately. Namely, the picture elements are arranged right and left alternately by 1.5 picture-element pitch (half a period) for each one line in the position of the gravity center of the picture element to be supplied with picture signals by the same signal electrode. Under such construction as described hereinabove, all the necessary things are to apply only the same color of picture signals to the same signal electrode. Thus, the color picture signals of the analog line memory are not required to be switched, with the result that the driving circuit becomes extremely simplified.

It is to be noted that the delta arrangement was initially adopted in the color CRT belonging to the other art field than the present invention. It followed as a logical consequence, because an electron gun of caliber as large as possible was required to be arranged in a narrow neck. The present invention was adopted from the other art demand. It is rare to be used in the color TV for home use, because a highly efficient electron gun is available.

A color liquid crystal display apparatus with switching elements added thereto will be described hereinafter in an embodiment. Fig. 2 (A) is a plan view

showing one example of a thin film transistor (TFT), which is a switching element. Fig. 2 (B) is a cross-sectional view taken along a line A - A. The TFT has a scanning electrode 11, a gate insulating film 12, a semiconductor film 13, a signal electrode 14 and a drain electrode 15 sequentially patterned and laminated on a transparent insulating substrate 10 of glass or the like. A picture-element electrode 16 and a storage capacitor (not shown) which is provided at need are connected with the drain electrode 15. A vacuum evaporating method, a sputtering method, a CVD method, a plasma CVD method, a low pressure CVD method or the like is used as a thin film forming method, and the patterning is performed by the art of shadow mask or photo-lithography. To drive the liquid crystal by a substrate with this TFT being formed thereon, optical shield and orientation layer are further provided. If a positive voltage is applied upon the scanning electrode 11 when an n type semiconductor has been used as a semiconductor film 13, an accumulation layer of electrons is formed on the surface on the side of the gate insulating film 12 of the semiconductor film 13 to modulate the resistance between the signal electrode (source electrode) 14 and the drain electrode 15.

One of the characteristics of the present invention is to cause the signal electrode to meander right and left and the picture elements, which are driven by the

same signal electrode, to be synchronized with the meandering to put them right and left alternately to shift the picture-element arrangement by 1.5 picture-element pitch for each of scanning lines so as to realize the delta arrangement. The color of the picture elements to be driven by the same signal electrode under such construction as described hereinabove becomes the same, thus rendering the color switching unnecessary. One example of the connection patterns is shown in Fig. 3 (A), (B). Fig. 3 (A) shows an example wherein the shape of the picture elements is rectangular and Fig. 3 (B) shows an example of the hexangle. It is to be noted that for simplification, the semiconductor film 13 and the insulating film 12 of the cross portion between the signal electrode 14 and the scanning electrode 11 are omitted.

The aim of the present invention is that the position of the gravity center of each picture element is delta shaped and the shape of the picture element is not restricted to the rectangle and hexangle. Also, the patterns shown in Fig. 3 (A), (B) show one example of the patterns in a case where the scanning electrodes only are branched to constitute the transistor. Only the scanning electrodes or both the signal electrodes and the scanning electrodes can be branched to constitute a transistor. Also, they show one example in a case where the scanning electrode is provided first, the signal electrode and the

drain electrode is provided later, but they may be provided in the opposite order.

In the present invention, the same color of picture elements are driven by the same signal electrode, but the images to be regenerated are shifted by 1.5 picture element right and left for each of scanning electrodes, with the sampling timing of the analog line memory being fixed in the delta arrangement of the picture elements, thus lowering the resolution. This inconvenience is settled through shifting of the sampling timing by time equivalent to $1.5 P$ (P =effective horizontal scanning time / number of horizontal picture elements) with odd lines and even lines. To shift the timing of the sampling, a signal for driving the signal electrode only in the case of one of them in accordance with the odd number or the even number the selected scanning electrode is located in is required to be delayed by $1.5 P$.

Fig. 4 shows an example of a driving circuit of a liquid crystal display panel of the present invention. A gate driver 20 composed of a shift register scans the scanning electrodes $11, 11, \dots$ sequentially by a horizontal synchronizing signal H to turn on the transistors $2, 2, \dots$ connected with the selected scanning electrode 11 . The time width of the gate pulse is not always necessary to be $1H$ (horizontal scanning time) and pulses to be applied upon each scanning electrode may be overlapped on each other. To make the width of the gate pulse larger than $1H$ is applied

for by the inventors of this case. The aim of that invention is to turn on the scanning electrode 11 prior to the original timing to preliminarily charge the liquid crystal and the storage capacitor. For use in the
5 embodiment, the same color of picture signals are normally applied upon the same signal electrode 14 and the correlation of the signals between the adjacent scanning lines is high in the normal picture signal so that the effect of the preliminary charging is large to render the
10 crosstalk between the colors difficult to cause.

An analog line memory 21 for driving the signal electrode is composed of a shift register 22 and sample hold circuits 23, 23, The shift register 22 sequentially transfers start pulses ST by a clock pulse CK of a period
15 $\frac{1}{2} P$ to generate sampling pulses. The sample hold circuits 23, 23, ... receive the sampling pulses to sample the color picture signals R, G, B to drive the signal electrodes 14, 14, ... in synchronous relation to the gate signal H. The picture elements to be driven by the same signal electrode
20 14 are the same in color in the arrangement of the picture elements of the present embodiment so that the color switching operation of the picture signals to be inputted to the sample hold circuits 23, 23, ... is not required.

A start pulse delay circuit 24 shifts the sampling
25 timing of the odd scanning lines and the even scanning lines. In an example of Fig. 4, the sampling timing is

delayed by 3 clock pulses, which are $1.5 P$ when the scanning electrode is in an even number. In such a sampling method, a period $= 1/2 P$ clock pulse is required, but substitution can be made by the clock pulse of a period of $1 P$ or $1.5 P$ when the short clock period is necessary to be avoided.

In the former, the positional shift of the $1/2$ picture element is caused between the odd line and the even line. In the latter, the picture signals of the G may be sampled at the original timing and the R and B may be simultaneously sampled at a timing corresponding to a central position where they are connected with each other. In this manner, the picture quality is hardly deteriorated because of the following reason. The vision is high in the spatial resolution with respect to the brilliance (brightness), but is not so high in the spatial resolution with respect to the color difference. As the contribution towards the brilliance is largest in G among the R, G, B, influences are hardly given in vision even if the positional shift of $1/2$ picture element is cause in the R and B when the G is faithfully reproduced.

Then, a substrate on a common electrode side with transparent conductive film and color filter provided on the transparent substrate of glass or the like is made by a known method although not shown. Interference filter, organic or inorganic dye or pigment are used as the color filter. In the color filter, three primary colors are

arranged in delta to suit the delta arrangement of the above-described picture element electrodes by a photo-lithography or a printing method. Transparent conductive film composed of ITO is provided thereon by a method of ion plating or the like. An orientation layer for orientating the liquid crystal is provided thereon.

A substrate with picture-element electrodes disposed in delta arrangement and a substrate with common electrodes disposed thereon are sealed each other through a spacer, and liquid crystal is impregnated into the gap between the substrate to complete the color liquid crystal panel. When an operation mode of the liquid crystal is TN, a polarizer is provided on both faces of the liquid crystal panel.

When the images have been reproduced by the color liquid-crystal display panel compiled in this manner, the resolution and display quality have been proved to be better, and the Moire stripes have been hard to cause.

The above description applies to a case where the picture elements which cause the signal electrodes to meander and drive them by the same signal electrode are arranged right and left alternately. Needless to say, the similar effect is caused even when the picture elements are arranged with the scanning electrodes being meandered and the same scanning electrodes being provided up and down alternately. It is necessary to retain a picture signal

located on a scanning line but one scanning line or two by a delay element such as surface acoustic-wave (SAW) element or the like or an analog line memory.

Needless to say, the present invention is
5 applicable even to a liquid crystal display apparatus (simple matrix system, adding system with nonlinear elements thereon, or the like) with switching elements added thereto.

Fig. 5 (A) is a view graphically showing the embodiment of the present invention with respect to the
10 simple matrix. The picture-element electrodes 31, 31, ... of the delta arrangement are directly connected to the signal electrodes 32, 32, Each of the signal electrodes 32 is caused to meander so that the amplitude may become $\frac{1}{4}$ of the picture-element pitch, and is directly
15 connected with the same color of picture elements 31, 31,... which are arranged right and left alternately by 1.5 picture element pitch (half a period). The scanning electrodes 33, 33, ... are provided corresponding to the lateral arrangements of the picture-element electrodes 31, 31, ...
20 in parallel laterally to the opposite substrate.

Fig. 5 (B) is a view graphically showing the embodiment of the present invention with respect to the double matrix. The scanning electrodes 37, 37, ... provided
in parallel on the opposite substrate with respect to the
25 picture-element electrodes 36, 36, ... of the delta arrangement are arranged to correspond to two lines in the

lateral direction of the arrangements of the picture elements. In the connection between each signal electrode 38 and the picture-element electrodes 36, 36, ... , one signal electrode 38 is connected only to the same color of picture-element electrodes existing every other line in the longitudinal direction, which is different from the above embodiment.

Fig. 6 (A), (B), (C) show embodiments of a color liquid crystal display apparatus with nonlinear elements being added thereto.

In Fig. 6 (A), the picture-element electrodes 41, 41, ... of the delta arrangement are respectively connected with the signal electrodes 43, 43, ... through the nonlinear elements 42, 42, Each of the signal electrodes 43 is caused to meander so that the amplitude may become $\frac{1}{2}$ of the picture-element pitch, and is connected to the same color of picture-element electrodes 41, 41, ... arranged right and left alternately by 1.5 picture-element pitch (half a period) for each one line. The scanning electrodes 44, 44, ... are provided corresponding to the lateral arrangement of the picture-element electrodes 41, 41, ... in parallel laterally on the substrate.

Fig. 6 (B) is a view graphically showing an example of a color liquid-crystal display apparatus with nonlinear elements added thereto with respect to the double matrix. The scanning electrodes 47, 47, ... provided on the

opposite substrate are arranged so that one may correspond to two lines of the lateral direction of the arrangements of the picture elements with respect to the picture-element electrodes 46, 46, ... in delta arrangement. Each of the signal electrodes 48, 48, ... grade separation the picture-element electrodes 46, 46, ... through insulating film not shown. In the connection between each signal electrode 48 and the picture-element electrodes 46, 46, ..., one signal electrode 38 is connected through nonlinear elements 49, 49, ... only to the same color of picture-element electrodes 46, 46, ... existing every other line in the longitudinal direction as in the embodiment shown in Fig. 5 (B).

Fig. 6 (C) is the modification of an example shown in Fig. 6 (B). Each picture-element electrode is divided into two portions 46', 46', arranged on both sides of a signal electrode 48 and respectively connected with the same signal electrode 48 through the nonlinear elements 49, 49. In this case, the signal electrodes 48, 48, ... are not required to grade separation the picture-element electrodes 46', 46',

Even in a color liquid crystal display apparatus with switching elements added thereto, the picture elements and each electrode can be arranged in accordance with the same aim shown in Fig. 6 (B), (C).

Normally the picture elements are driven by a voltage averaging method (see the book described before) in a simple matrix system and an adding system with nonlinear elements added thereto. To produce a half tone, the width of the selection pulse width to be applied upon a signal electrode is modulated in accordance with gradation (see Television Society Journal 31, 940 (in 1977)). To apply the present invention to this case, a pulse width modulation circuit is provided between a signal electrode 14 and a sample hold circuit 23 of an analog line memory 21 of Fig. 4. This circuit is adapted to modulate the width of the selection pulse to be applied upon the signal electrode in accordance with a picture signal sample-held by a sample hold circuit 23.

Also, a digital line memory, instead of an analog line memory 21, may be used. In this case, the picture signals are converted into a digital signal by an AD converter and sequentially store in the digital line memory. Then, the width of the selection pulse to be applied upon the signal electrode is controlled by a digital picture signal stored in the digital line memory. In this case, a method is used of generating a series of pulses each being different in the pulse width in accordance with the number of the bits of the AD conversion and selecting by a multiplexer a pulse of the pulse width corresponding to the level of the picture signal.

Even when the analog line memory or the digital line memory is used, the color switching is required in the conventional construction, but in the present invention, the color switching becomes unnecessary as in a case where the switching element has been added.

As is clear from the foregoing description, according to the present invention, in the color liquid-crystal display apparatus, the delta arrangement is adopted, thus improving the image resolution and the display quality.

Although the present invention has been fully described by way of example with reference to the accompanying drawings, it is to be noted here that various changes and modifications will be apparent to those skilled in the art. Therefore, unless otherwise such changes and modifications depart from the scope of the present invention, they should be construed as included therein.

What is claimed is:

1. A color liquid-crystal display apparatus provided with picture elements corresponding to the intersecting points between signal electrodes and scanning electrodes, and a coloring means of three colors, red, green, blue
5 disposed corresponding to each of the picture elements, wherein rectilinear arrangements, each having a picture element corresponding to red, green or blue and a coloring means corresponding to it, being arranged periodically with three colors of red, green, blue as one period are arranged
10 -- in parallel to each other and in adjacent relation, shifted by half a period.
2. A color liquid-crystal display apparatus in accordance with claim 1, wherein each of the picture elements constituting the above-described one line of linear arrangement is controlled by one scanning electrode,
5 adjacent two lines among the lines of the same color of picture elements arranged in a direction vertical to the rectilinear arrangement are connected directly or through a nonlinear element or a switching element to the same signal electrode.
3. A color liquid-crystal display apparatus in accordance with claim 1, wherein each of the picture-element electrodes constituting the above-described one line of rectilinear arrangement is connected directly or through a
5 nonlinear element or a switching element, the adjacent two

lines of the lines of the same color of picture elements arranged in a direction vertical to the rectilinear arrangement are controlled by the same scanning electrode.

4. A color liquid-crystal display apparatus in accordance with claim 1, wherein every one line or every two lines of the respective picture elements constituting the above-described rectilinear arrangement are controlled by the same scanning electrode, and the same color of picture-element electrodes are connected every other line directly or through a nonlinear element or a switching element to the same signal electrode.
- 5

Fig. 1(A)

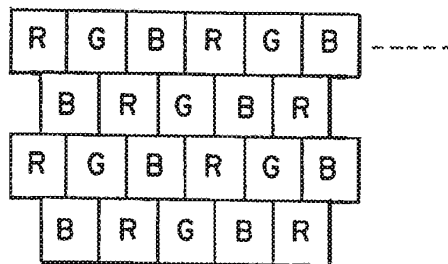


Fig. 1(B)

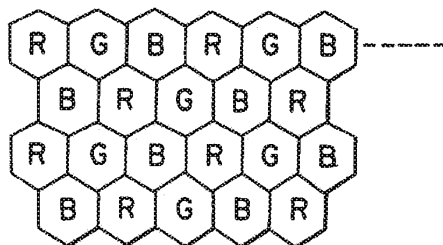
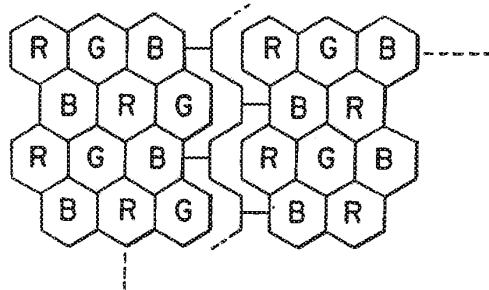


Fig. 1(C)



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Fig. 2(A)

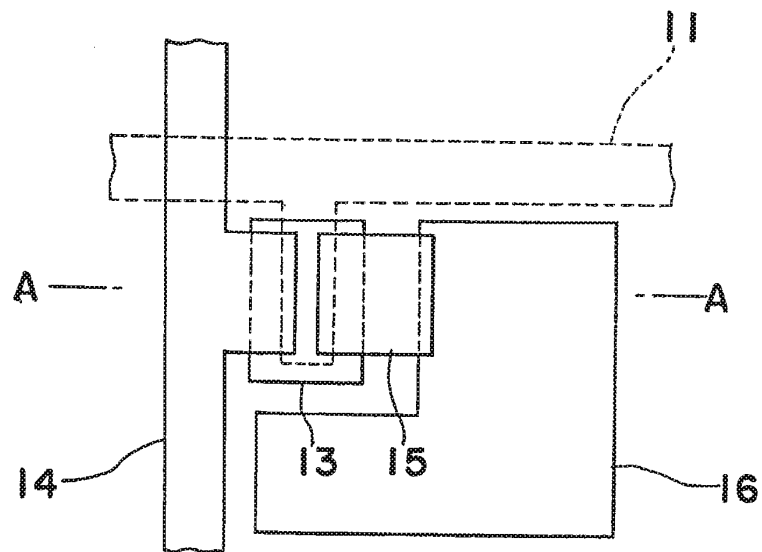


Fig. 2(B)

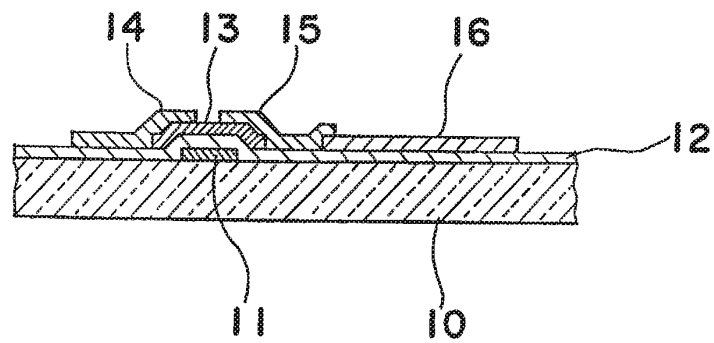


Fig. 3(B)

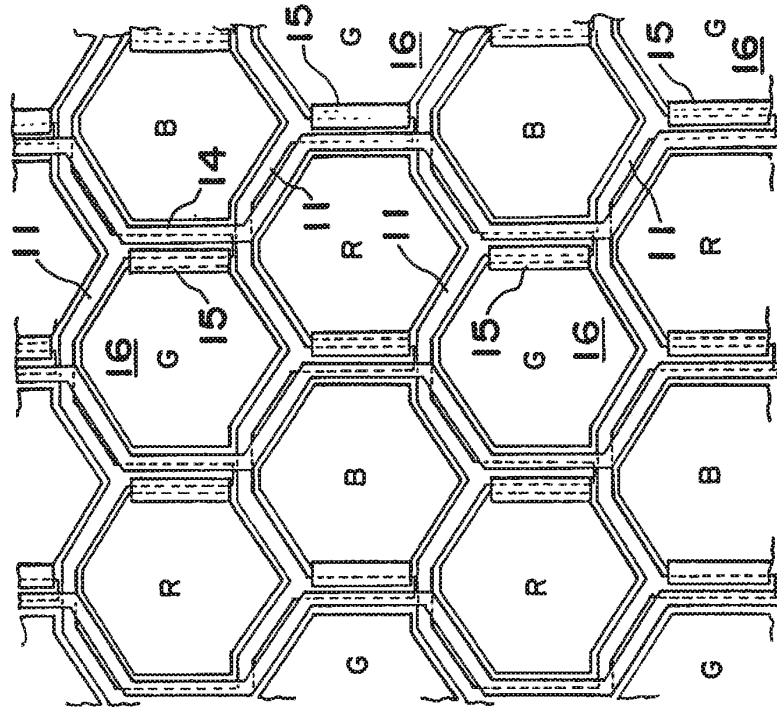


Fig. 3(A)

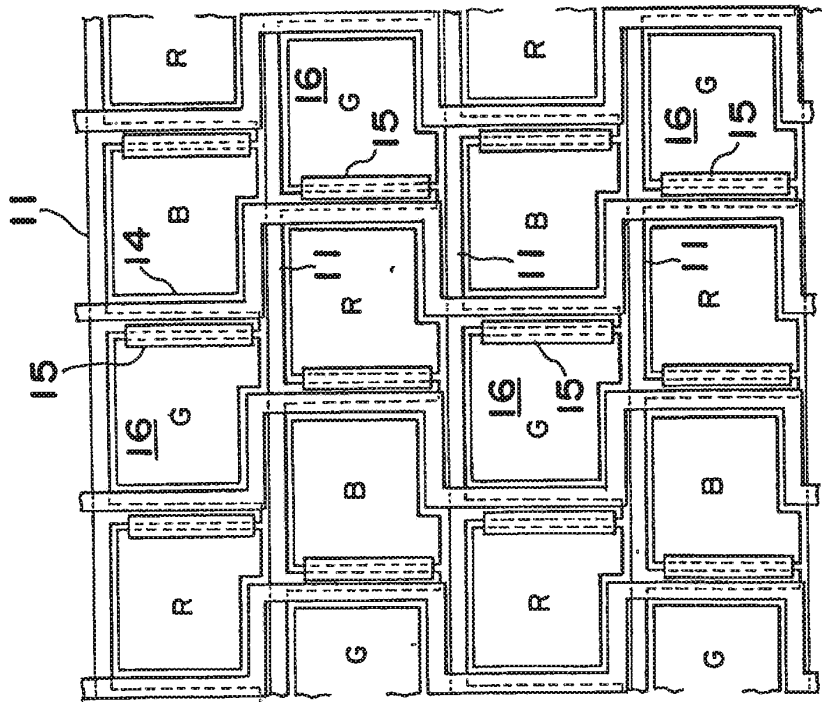


Fig. 5(A)

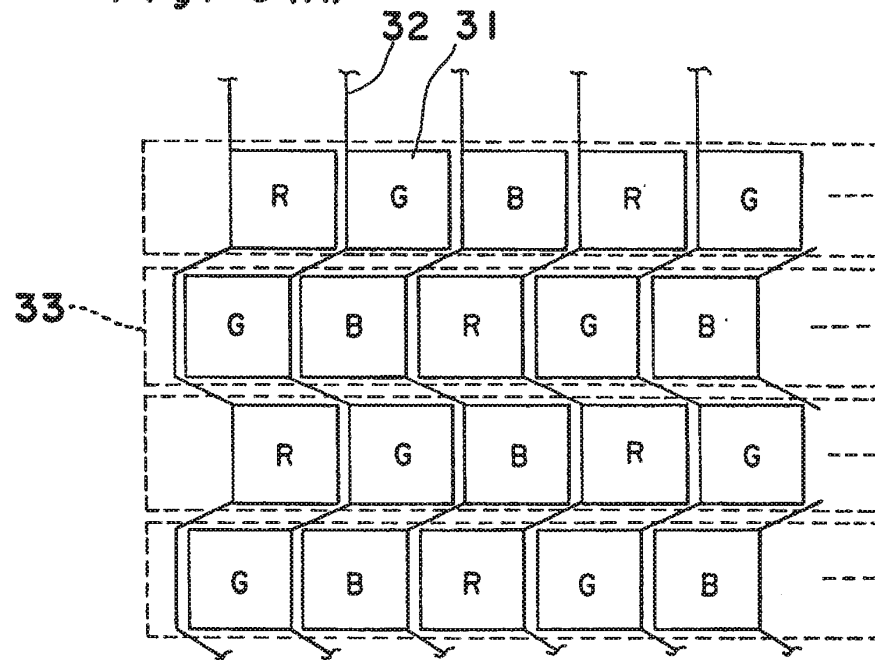
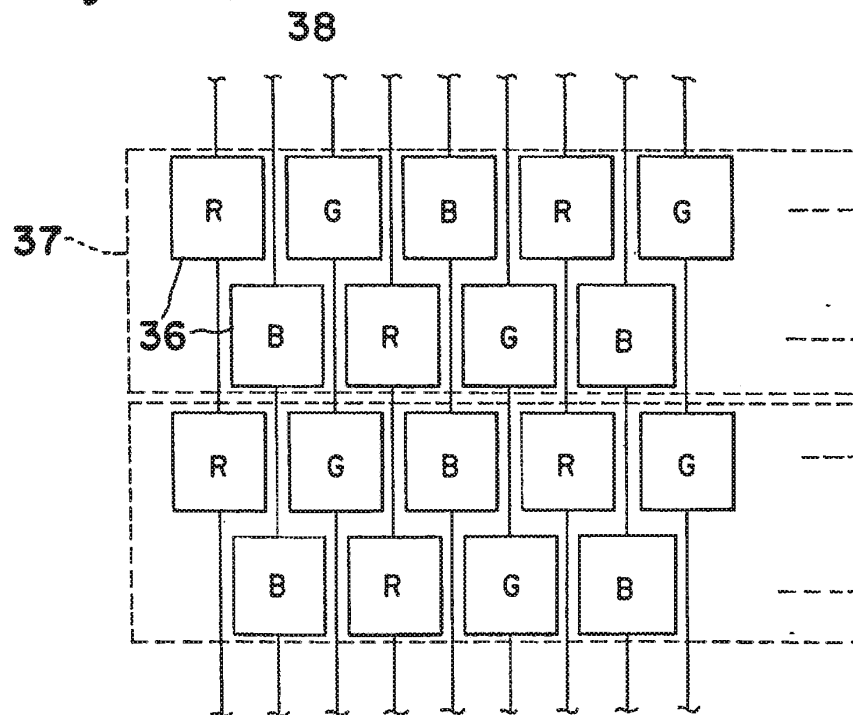


Fig. 5(B)



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Fig. 6(A)

Fig. 6(B)

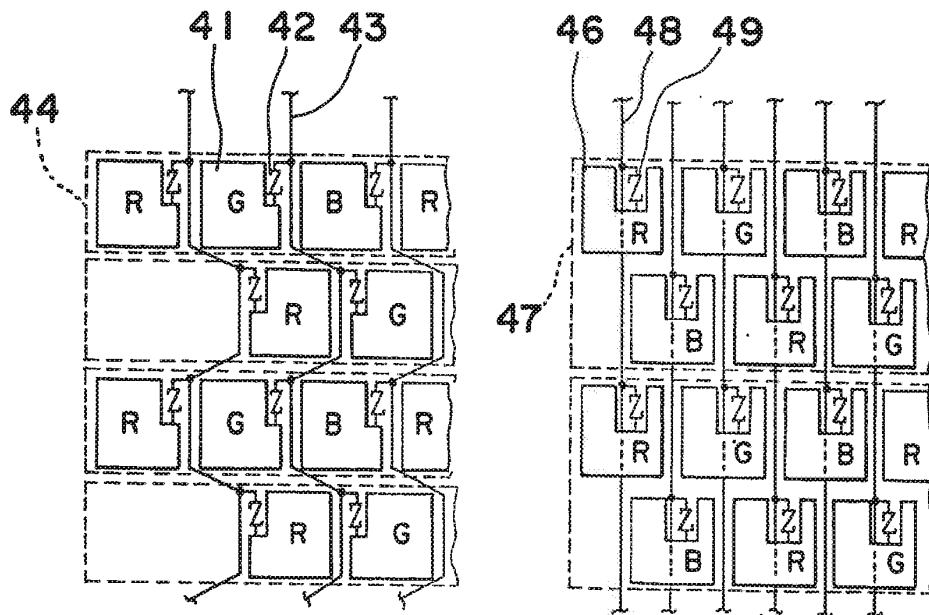


Fig. 6(C)

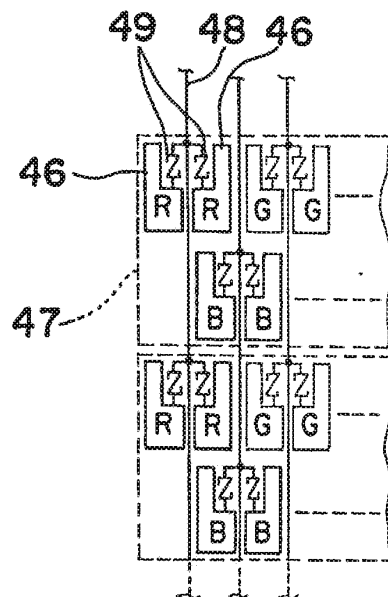


Fig. 7(A)

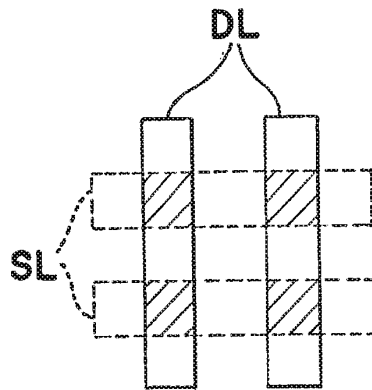


Fig. 7(B)

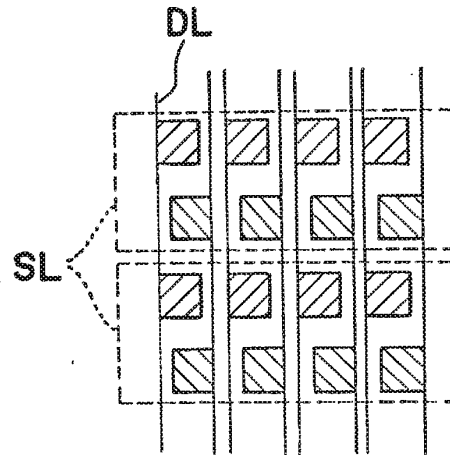


Fig. 7(C)

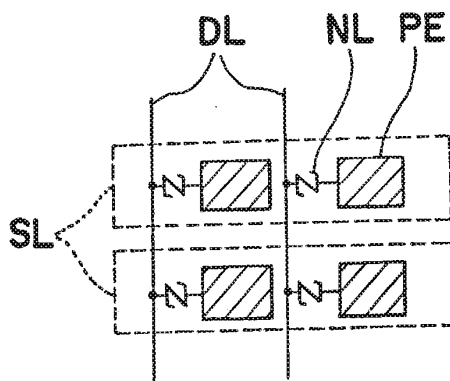


Fig. 7(D)

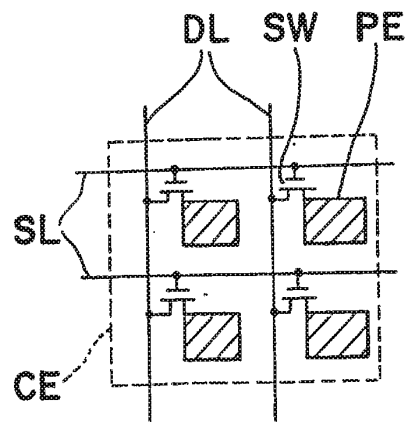


Fig. 8(A)

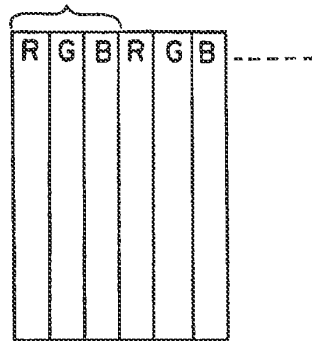


Fig. 8(B)

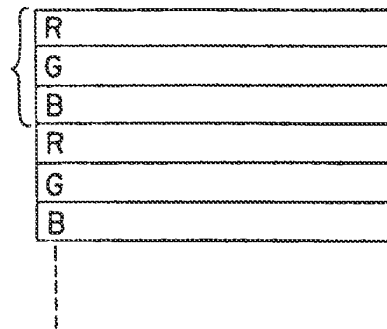


Fig. 8(C)

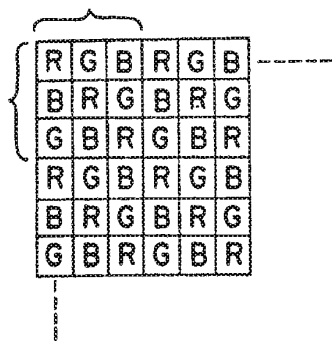


Fig. 8(D)

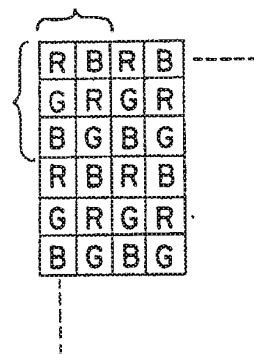


Fig. 8(E)

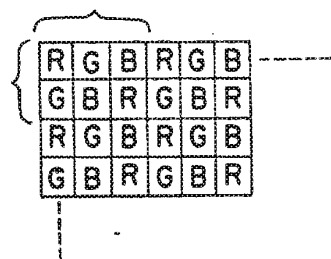
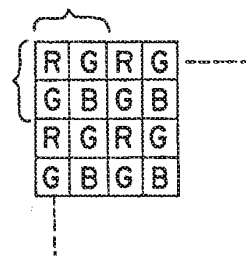
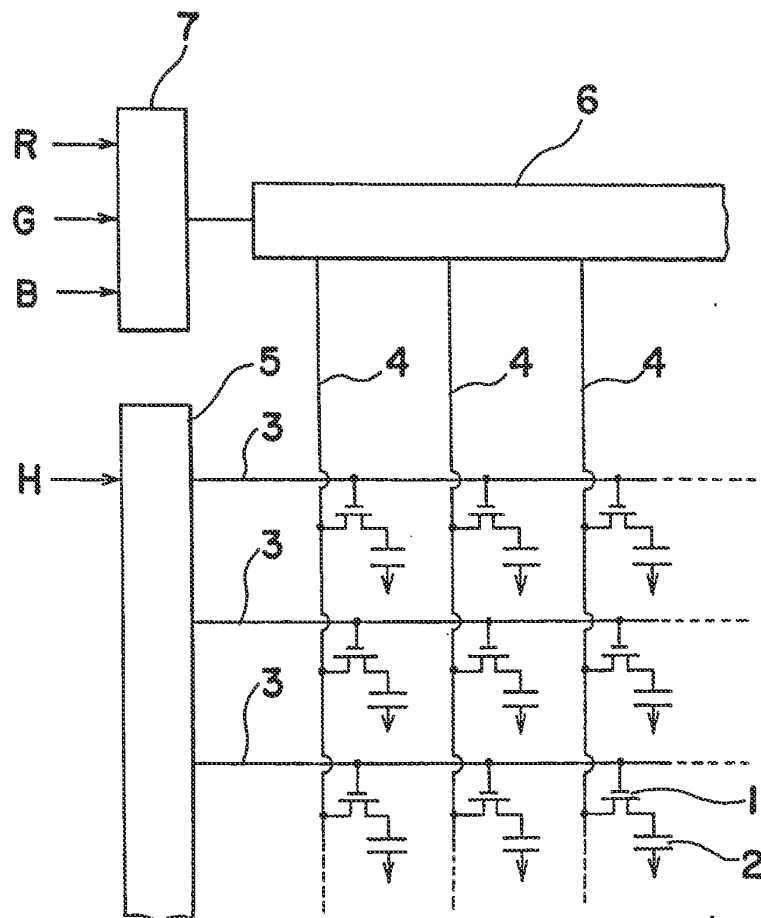


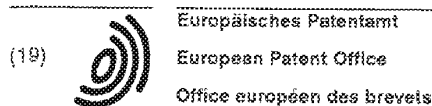
Fig. 8(F)



[illegible]

Fig. 9 (B)





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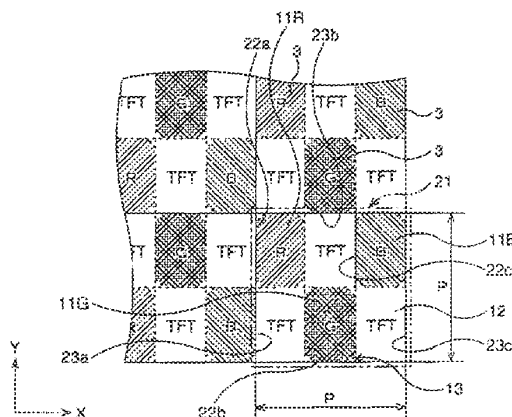
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(54) **DISPLAY APPARATUS AND MANUFACTURING METHOD THEREOF**

(57) Each pixel (21) includes a plurality of light emitting regions (11R, 11G, and 11B) corresponding R, G, and B each having an organic EL layer (3), and a plurality of TFT elements (12) provided corresponding to the light emitting regions to control light emission in the respective light emitting regions. The light emitting regions are provided in a zigzag manner and adjacent light emitting regions are kept from contacting one another. Each pixel (21) is divided into six segments (22a to 22c

and 23a to 23c), and the light emitting regions are arranged in three segments (22a to 22c) in a zigzag manner. In this way, in a bottom emission type, active matrix organic EL display, a sufficient aperture ratio can efficiently be secured, and pixels can be arranged so that the aperture ratio is hardly a trade off for higher resolution. Therefore, power consumption for obtaining necessary luminance can be reduced, and this can contribute to downsizing of the driving circuit and the device as a whole.

FIG. 2



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Description

Technical Field

[0001] The present invention relates to display devices that use organic EL (Electro-Luminescence), and more particularly, is applied to a bottom emission type, active matrix organic EL panel.

Background Art

[0002] In recent years, organic EL displays that employ an organic EL system in which carriers are injected into an organic solid from an electrode to emit light from a flat surface have actively been developed as light-emitting type displays. The organic EL displays can be divided into passive matrix type and active matrix type, for example, depending on how the displays are driven. The former type display allows pixels arranged in a matrix to emit light by line-at-a-time driving method. The latter type has a switching element for each of pixels arranged in a matrix and the switching elements are controlled to drive the pixels so that they emit light individually.

[0003] According to the driving method by the active matrix type organic EL display, the switching circuits control light emission of the pixels on a pixel basis, and therefore the display has attracted attention particularly as an optimum display for moving picture. There are bottom emission type displays that extract emitted light toward the glass substrate and the top emission type displays that extract emitted light to the opposite side to the glass substrate.

[0004] A bottom emission type, active matrix organic EL panel is provided with a switching circuit on a pixel basis, and light is emitted toward the glass substrate. Therefore, the part of the switching circuits that occupies half the area of the pixel inevitably becomes a non-light emitting region. In addition, three light emitting regions for three colors R (red), G (green), and B (blue) that are necessary for full color display are produced by coloring the organic EL light emitting layer discretely corresponding to the colors. Therefore, a registration margin (dm) for discrete coloring between adjacent light emitting regions in different colors is necessary, and this dm portion constitutes a non-light emitting region.

[0005] In a conventional display, the three light emitting regions for R, G, and B and the switching circuit portions are arranged continuously based on the colors (see Fig. 4 for the arrangement in the horizontal (X-) direction). As the registration margin (dm) depends on the registration precision by the pixel film deposition device and the processing precision of the patterning mask, how much the registration margin (dm) can be reduced is limited, and the minimum value for the margin dm is generally 20 μm (corresponding to $\pm 10 \mu\text{m}$). In this case, the width of each light emitting region is smaller as the resolution increases. However, the minimum value for

dm is fixed, and therefore the ratio of dm occupied in the pixel increases, which lowers the ratio of the light emitting regions (aperture ratio) if higher resolution is to be achieved. With a smaller aperture ratio, the luminance is lowered, and therefore the amount of current that contributes to the light emission should be increased to keep the luminance in a necessary level. This gives rise to increase in power consumption.

[0006] The present invention was devised in view of the above described problems, and it is an object of the present invention to provide a display device having a bottom emission type, active matrix organic EL panel that efficiently secures a sufficient aperture ratio, has pixel arrangement in which the aperture ratio is hardly a trade off for higher resolution, and can operate with reduced power consumption for obtaining necessary luminance and contribute to downsizing of the driving circuit and the device as a whole, and a manufacturing method that allows the configuration of such a display device to be readily provided with reliability.

Summary of the Invention

[0007] A display device according to the invention includes an active matrix organic EL panel having first and second electrodes provided on a substrate and an organic EL light emitting layer provided between the first and second electrodes. The organic EL light emitting layer includes a light emitting region, a plurality of the light emitting regions are arranged in a zigzag manner, and adjacent ones of the light emitting regions are kept from contacting each other.

[0008] By a method of manufacturing a display device according to the invention, a display device is produced that includes an active matrix organic EL panel having first and second electrodes provided on a substrate and an organic EL light emitting layer provided between the first and second electrodes. The organic EL light emitting layer includes a light emitting region. At the time of forming a plurality of the light emitting regions, the organic EL light emitting layers corresponding to the respective light emitting regions are formed by mask vapor deposition so that they are arranged in a zigzag manner and adjacent ones of the light emitting regions are kept from contacting each other.

Brief Description of the Drawings

[0009]

Fig. 1 is a schematic sectional view of an organic EL layer in an organic EL display according to an embodiment of the invention.

Fig. 2 is a schematic plan view of an organic EL light emitting layer, a main part of the organic EL display according to the embodiment, showing its surface as being enlarged.

Fig. 3 is a schematic plan view of the pixel unit in Fig. 2 as being enlarged.

Fig. 4 is a schematic plan view of an example of pixel arrangement in a conventional bottom emission type, active matrix organic EL display.

Fig. 5 is a graph showing a result of examining the relation between increase in the pixel resolution and the aperture ratio in comparison with the conventional example (comparative example).

Figs. 6A to 6G are schematic sectional views showing main steps in the process of manufacturing the organic EL display according to the embodiment in the order of the steps.

Fig. 7 is a schematic plan view of an organic EL light emitting layer, a main part of an organic EL display according to Modification 1, showing its surface as being enlarged.

Fig. 8 is a schematic plan view of an organic EL light emitting layer, a main part of an organic EL display according to Modification 2.

Detailed Description of the Preferred Embodiments

[0010] Hereinafter, specific embodiments of the invention will be described in detail with reference to the accompanying drawings.

[0011] Now, a preferred embodiment of the invention will be described in detail with reference to the accompanying drawings. The embodiment is mainly directed to a display device including a bottom emission type, active matrix organic EL panel (bottom emission type, active matrix organic EL display).

- Specific Configuration of Organic EL Display -

[0012] Fig. 1 is a schematic sectional view of the configuration of the panel of the organic EL display according to the embodiment, Fig. 2 is a schematic plan view of an organic EL light emitting layer, a main component of the organic EL display according to the embodiment, showing its surface as being enlarged, and Fig. 3 is a schematic plan view of pixels in Fig. 2 as being enlarged. Here, Fig. 1 shows a section taken along the line I-I' in Fig. 3.

[0013] As shown in Fig. 1, the organic EL display includes a TFT (Thin Film Transistor) element 12 as a switching circuit that controls light emission, for example, on a glass substrate 1 as a transparent substrate. The TFT element 12 and the interconnection lines are protected and insulated by a flattening film 10 that forms a flat surface on which an organic EL element is to be stacked. A plurality of first electrodes 2 made of a material containing, for example, an indium tin oxide (ITO)

alloy as transparent electrodes, a plurality of organic EL layers 3 corresponding to the respective first electrodes 2, and a second electrode 4 made of a material containing aluminum or the like and covering the entire surface are stacked on the flat surface. The organic EL layers 3 are held between the associated first electrodes 2 and the second electrode 4, and the first electrode 2 and the TFT element 12 are connected by a through hole provided at part of the flattening film 10. In this case, the area of the organic EL layer 3 is formed to be larger than the area of the first electrode 2. At the time of driving, light is emitted from the organic EL layer 3 through the first electrode 2 and the glass substrate 1.

[0014] As shown in Fig. 2, a plurality of pixels 21 are arranged in a matrix, and the pixels 21 each include a plurality of light emitting regions 11R, 11G, and 11B corresponding to R, G, and B, and a plurality of TFT elements 12 provided corresponding to the light emitting regions and serving as switching circuits that control light emission from the respective light emitting regions. Here, the overlapping parts between the first electrodes 2 and the organic EL layers 3 are the light emitting regions 11R, 11G, and 11B. The light emitting regions 11R, 11G, and 11B are arranged in a zigzag manner, and non-light emitting regions 13 provided at corners of the light emitting regions prevent adjacent ones among the light emitting regions 11R, 11G, and 11B from contacting each other. One pixel 21 is in the shape of a regular square of $P \times P$. The pixels 21 are each divided in two in the vertical direction and three in the horizontal direction into six segments 22a to 22c and 23a to 23c. The light emitting regions 11R, 11G, and 11B are provided in the three zigzagged segments 22a to 22c, and the TFT elements 12 are in the remaining three segments 23a to 23c. Herein, the light emitting regions in the same color are aligned in the vertical direction (Y-direction) with each TFT element 12 interposed therebetween.

[0015] Now, as a comparative example to the embodiment, pixel arrangement in a conventional bottom emission type, active matrix organic EL display is shown in Fig. 4.

[0016] As can be seen, in the conventional example, the light emitting regions 101R, 101G, and 101B constituting the pixel 111 are aligned in the horizontal direction (X-direction), and therefore adjacent light emitting regions are separated by the non-light emitting regions 103 provided at vertical sides of the light emitting regions and the TFT elements 102. Therefore, how much the area of the non-light emitting regions 103 can be reduced is necessarily limited.

[0017] In comparison, according to the embodiment, the light emitting regions 11R, 11G, and 11B are provided with notches, in C-chamfer shape in this example (though they may be rounded), as the non-light emitting regions 13 at their respective four corners. The non-light emitting regions 13 and the TFT circuits 12 keep adjacent light emitting regions from contacting one another. The non-light emitting regions 13 formed at the corners

of the light emitting regions occupy only an extremely small area, and the aperture ratio can be improved significantly over that of the example in Fig. 4.

[0018] Based on this pixel arrangement, a size for a resolution of 160 ppi will be described with reference to Fig. 3. It is understood that the size is simply by way of example and the invention is not limited thereto.

[0019] When the resolution is 160 ppi, $P = 159 \mu\text{m}$, and therefore the regions occupied by the colors R, G, and B are each $159 \mu\text{m} \times 53 \mu\text{m}$, half the area, $79.5 \mu\text{m} \times 53 \mu\text{m}$ is the area occupied by a TFT element 12, and the remaining $79.5 \mu\text{m} \times 53 \mu\text{m}$ is the area occupied by each light emitting region. So-called C-chamfers are provided as non-light emitting regions 13 at the corners of the light emitting regions in order to secure registration margins necessary for discrete coloring in three colors and a space for various interconnection lines for switching circuits. The registration margin dm necessary for discrete coloring is $20 \mu\text{m}$ ($\pm 5 \mu\text{m}$ for the registration margin by the pixel film deposition device plus $\pm 5 \mu\text{m}$ for the processing precision for the R, G, and B patterning mask). The necessary interconnection lines include a data line 31, a scanning line 32, a power supply line 33, and a storage capacitor line 34, and these lines each have a width in the range of from $5 \mu\text{m}$ to $15 \mu\text{m}$. The data line 31 is provided in the Y-direction, and the scanning line 32, the power supply line 33, and the storage capacitor line 34 are provided in the X-direction. These interconnection lines in the TFT element 12 are formed in different layers formed as multiple film layers and connected with each other by a through hole 35 provided in interlayer insulating films. Therefore, a chamfer of $C15 \mu\text{m}$ provided at the corner of each light emitting region allows the registration margin and the space for the interconnection lines to be secured.

[0020] In order to form the light emitting regions, the first electrode 2 as the transparent electrode on the glass substrate has a rectangular shape of $79.5 \mu\text{m} \times 53 \mu\text{m}$, and each corner is chamfered by $C15 \mu\text{m}$. Consequently, the segment for each color has an area of $159 \mu\text{m} \times 53 \mu\text{m} = 8427 \mu\text{m}^2$, while the area of the effective light emitting region is $79.5 \mu\text{m} \times 53 \mu\text{m} - C15 \mu\text{m} \times 4 = 3753.5 \mu\text{m}^2$. The aperture ratio is $(3753.5/8427) \times 100 = 44.7\%$.

[0021] In contrast, in the comparative example of Fig. 4, the segment width of each of the R, G, and B light emitting regions is $P/3$ relative to the pixel pitch P , and if the registration margin dm for discrete coloring is secured, the width of the light emitting region is $P/3 - dm$. If the lower limit for the registration margin dm for discrete coloring is applied to design higher resolution arrangement, the ratio of reduction in the width of the light emitting region by dm increases as the pitch P is reduced, and the aperture ratio is reduced.

[0022] When, for example, $P = 318 \mu\text{m}$ (for a resolution of 80 ppi), and $dm = 20 \mu\text{m}$, the size of the light emitting region $L \times W = 159 \mu\text{m} \times 86 \mu\text{m}$, and the aperture ratio is 40.5%. When $P = 159 \mu\text{m}$ (for a resolution

of 160 ppi), and $dm = 20 \mu\text{m}$, $L \times W = 79.5 \mu\text{m} \times 33 \mu\text{m}$ and the aperture ratio is 31.1%. This means that the aperture ratio is greatly reduced by the registration margin dm if higher resolution is to be obtained.

[0023] The organic EL display according to the embodiment having the above-described configuration was compared to the conventional example (the comparative example described above) regarding the relation between increase in the pixel resolution and the aperture ratio. The result is given in Fig. 5. As can be seen, when the registration margin dm necessary for discrete coloring is $20 \mu\text{m}$, the aperture ratio in the configuration according to the present embodiment is significantly greater than that of the conventional example regardless of the value of the resolution. It has been found that the configuration according to the embodiment considerably, effectively improves the aperture ratio in the bottom emission type, active matrix organic EL panel.

[0024] In this way, the present embodiment can improve the aperture ratio by 13.6% over the comparative example. Therefore, according to the embodiment, a display having a bottom emission type, active matrix organic EL panel that efficiently secures a sufficient aperture ratio, has pixel arrangement in which the aperture ratio is hardly a trade off for higher resolution, and can operate with reduced power consumption for obtaining necessary luminance and contribute to downsizing of the driving circuit and the device as a whole can be provided.

- Specific Example of Method of Manufacturing Organic EL Display -

[0025] Figs. 6A to 6G are schematic sectional views showing main steps in the process of manufacturing the organic EL display according to the embodiment in the order of the steps. In Figs. 6A to 6G, the left side on the surface of the sheet corresponds to a section taken along the line II-II' in Fig. 3, and the right side corresponds to a section taken along line III-III' in Fig. 3.

[0026] Now, as shown in Fig. 6A, on the surface of, for example, a glass substrate 1 as a transparent substrate, a TFT element 12 serving as a switching circuit, and various interconnection lines such as a data line 31, a scanning line 32, a power supply line 33, and a storage capacitor line 34 are formed, and then a flattening film 10 made of a transparent resin is formed to cover them. Here, the TFT elements 12 are formed in the parts corresponding to the segments 23a to 23c of the pixel 21 as described above.

[0027] Then, as shown in Fig. 6B, a film of an indium tin oxide (ITO) alloy as a transparent electrode is deposited at the effective light emitting portion described above, and thus first electrodes 2 are formed.

[0028] Then, light emitting regions 11R, 11G, and 11B forming the pixels 21 are sequentially formed.

[0029] More specifically, as shown in Fig. 6C, a vapor deposition mask 5 with an opening 5a corresponding to

a region to form a light emitting region is used. The vapor deposition mask 5 is placed on the surface of the glass substrate 1 so that the opening 5a is placed only in the position of the organic EL layer 3 corresponding to the light emitting region 11R, and the organic EL layer 3 corresponding to the light emitting region 11R is formed in the segment 22a by vapor deposition. At the time, the first electrode 2 is completely covered with the organic EL layer 3 for the light emitting region 11R, and the organic EL layer 3 does not overlap the first electrodes 2 for the other colors.

[0030] Then, as shown in Fig. 6D, using the same vapor deposition mask 5, the mask 5 is moved and placed on the surface of the glass substrate 1 so that the opening 5a is placed only in the position to form an organic EL layer 3 corresponding to the light emitting region 11G and the organic EL layer 3 corresponding to the light emitting region 11G is formed in the segment 22b by vapor deposition. At the time, the first electrode 2 is completely covered with the organic EL layer 3 for the light emitting region 11G, and the organic EL layer 3 does not overlap the first electrodes 2 for the other colors.

[0031] Then, as shown in Fig. 6E, using the same vapor deposition mask 5, the mask 5 is moved and placed on the surface of the glass substrate 1 so that the opening 5a is placed only in the position to form the organic EL layer 3 corresponding to the light emitting region 11B and the organic EL layer 3 corresponding to the light emitting region 11B is formed in the segment 22c by vapor deposition. At the time, the first electrode 2 is completely covered with the organic EL layer 3 for the light emitting region 11B, and the organic EL layer 3 does not overlap the first electrodes 2 for the other colors.

[0032] In this way, through the process steps in Figs. 6C to 6E, C-chamfer shaped (or rounded) non-light emitting regions 13 are formed at the four corners of the light emitting regions 11R, 11G, and 11B. These non-light emitting regions 13 as well as the segments 23a to 23c for the TFT elements 12 are non-light emitting regions, the organic EL layers 3 are formed so that adjacent light emitting regions are kept from contacting one another in a pixel 21 and a plurality of such pixels 21 are provided in a matrix. The organic EL layers 3 corresponding to the light emitting regions 11R, 11G, and 11B are each formed to have an area greater than the corresponding first electrode 2 and cover the same, so that the registration margins for forming the light emitting regions can be secured. In addition, the TFT element region can be used for securing the registration margin necessary for achieving higher resolution. In this way, the aperture ratio can be improved.

[0033] The light emitting regions for the same colors are aligned with each TFT element 12 interposed therebetween so that the light emitting regions 11R, 11G, and 11B are evenly provided in a plane without contacting one another.

[0034] Then, as shown in Fig. 6F, a vapor deposition mask 6 with openings 6a to expose all the light emitting

regions is used and placed on the surface of the glass substrate 1, and an aluminum alloy film is deposited by vapor deposition, thereby forming a second electrode 4 to cover all the light emitting regions.

[0035] As shown in Fig. 6G, a plate 7 made of glass or the like that prevents moisture penetration is adhesively fixed, for example, with an adhesive 8 to cover the second electrode 4, so that the organic EL layers 3 are prevented from deteriorating by moisture and the like. Various conductive members formed on the glass substrate 1 are connected to a driving circuit (not shown) through the interconnection line 9 of an FPC (Flexible Printed Circuit).

[0036] Then, after various post-processing steps, a bottom emission type, active matrix organic EL display, for example, with a resolution of 160 ppi and an aperture ratio of 44.7% is produced.

[0037] As in the foregoing, according to the embodiment, at the time of manufacturing the organic EL display having the above-described configuration, mask vapor deposition technique is applied to form the organic EL layers 3 corresponding to the respective light emitting regions 11R, 11G, and 11B, and the same vapor deposition mask 5 is sequentially moved to form these light emitting regions. Therefore, the single vapor deposition mask 5 can readily be formed using a single film deposition chamber, low molecular organic EL can be deposited by vapor deposition, and an organic EL display having the above-described configuration can readily be provided with reliability.

- Modifications of Embodiment -

[0038] Now, modifications of the embodiment will be described.

(Modification 1)

[0039] Fig. 7 is a schematic plan view of an organic EL light emitting layer, a main part of an organic EL display according to Modification 1, showing its surface as being enlarged.

[0040] In the organic EL display, the areas of the light emitting regions 11R, 11G, and 11B in the pixel 21 are each greater than the area of the TFT element 12. In this case, the registration margins necessary for discrete coloring into the three colors can be included in the segments of the TFT elements 12, so that the aperture ratio can be increased.

(Modification 2)

[0041] Fig. 8 is a schematic plan view of an organic EL light emitting layer, a main part of an organic EL display according to Modification 2, showing its surface as being enlarged.

[0042] In this organic EL display, the areas of the light emitting regions 11R, 11G, and 11B in the pixel 21 are

each smaller than the area of the TFT element 12. In this case, adjacent TFT elements 12 separate adjacent light emitting regions, and therefore there is no necessity for providing non-light emitting regions in association with the light emitting regions, so that the aperture ratio can be increased (in the shown example, the segments for the TFT elements 12 are in contact with each other).

Industrial Applicability

[0043] According to the invention, a display device having a bottom emission type, active matrix organic EL panel that efficiently secures a sufficient aperture ratio, has pixel arrangement in which the aperture ratio is hardly a trade off for higher resolution, and can operate with reduced power consumption for obtaining necessary luminance and contribute to downsizing of the driving circuit and the device as a whole, and a manufacturing method that allows the configuration of such a device to be readily provided can be provided with reliability.

Claims

1. A display device having an active matrix organic EL panel comprising:
 - first and second electrodes provided on a substrate, and
 - an organic EL light emitting layer provided between said first and second electrodes, wherein
 - said organic EL light emitting layer includes light emitting regions, arranged in a zigzag manner, and adjacent ones of said light emitting regions are kept from contacting each other.
2. The display device according to claim 1, wherein,
 - three kinds of said light emitting regions corresponding to R, G, and B and three switching circuits corresponding to the three kinds of said light emitting regions are arranged in a matrix, and
 - in six segments arranged in two rows and three columns, said light emitting regions are arranged in three of said segments positioned in a zigzag manner and said three switching circuits are arranged in the three remaining segments.
3. The display device according to claim 2, wherein said light emitting regions for the same color are aligned with said switching circuit interposed therebetween.
4. The display device according to claim 1, wherein the area of said organic EL light emitting layer is greater than the area of said first electrode.
5. The display device according to claim 1, wherein a non-light emitting region is formed at a corner of said light emitting region, and adjacent ones of said light emitting regions are separated by said non-light emitting region.
6. The display device according to claim 1, wherein the area of said light emitting region is greater than the area of said switching circuit.
7. The display device according to claim 1, wherein said light emitting region has an area smaller than the area of said switching circuit and is separated from adjacent one of said light emitting regions with said switching circuit interposed therebetween.
8. A method of manufacturing a display device having an active matrix organic EL panel comprising first and second electrodes provided on a substrate and an organic EL light emitting layer provided between said first and second electrodes, wherein said organic EL light emitting layer includes a light emitting region, the method comprising the step of forming a plurality of said light emitting regions by mask vapor deposition, wherein said organic EL light emitting layers corresponding to each of said light emitting regions are arranged in a zigzag manner and adjacent ones of said light emitting regions are kept from contacting each other.
9. The method of manufacturing a display device according to claim 8, wherein the same mask is sequentially moved to form said organic EL light emitting layers corresponding to each of said light emitting regions.
10. The method of manufacturing a display device according to claim 8, wherein:
 - three kinds of said light emitting regions corresponding to R, G, and B and said three switching circuits corresponding to the three kinds of said light emitting regions are arranged in a matrix;
 - in six segments arranged in two rows and three columns, said light emitting regions are arranged in three of said segments positioned in a zigzag manner and said three switching circuits are arranged in the three remaining segments.
11. The method of manufacturing a display device according to claim 10, wherein said light emitting regions for the same color are aligned with said switching circuit interposed therebetween.

12. The method of manufacturing a display device according to claim 6, wherein
said organic EL light emitting layer is formed
to have a greater area than the area of said first
electrode. 5
13. The method of manufacturing a display device according to claim 8, wherein
said light emitting region is formed to have a
corner part serving as a non-light emitting region. 10
14. The method of manufacturing a display device according to claim 8, wherein
said light emitting region is formed to have a
greater area than the area of said switching circuit. 15
15. The method of manufacturing a display device according to claim 8, wherein
said light emitting region has an area smaller
than the area of said switching circuit and is separated from adjacent one of said light emitting regions with said switching circuit interposed therebetween. 20

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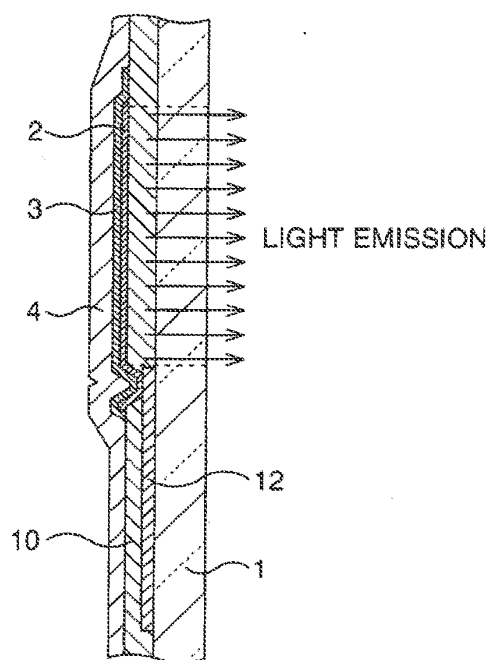
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FIG. 1



I - I' SECTION

FIG. 2

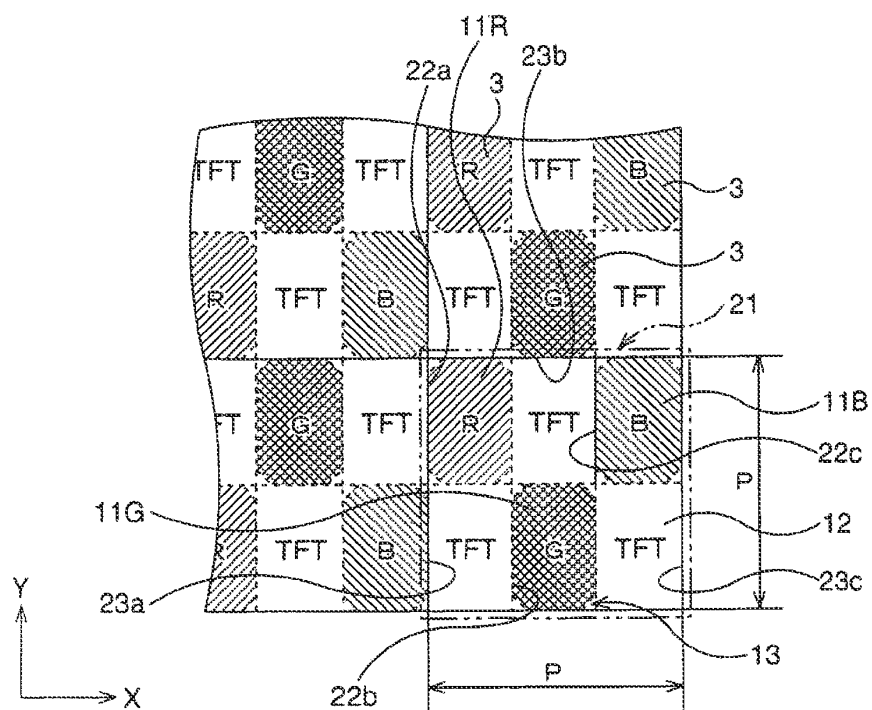


FIG. 3

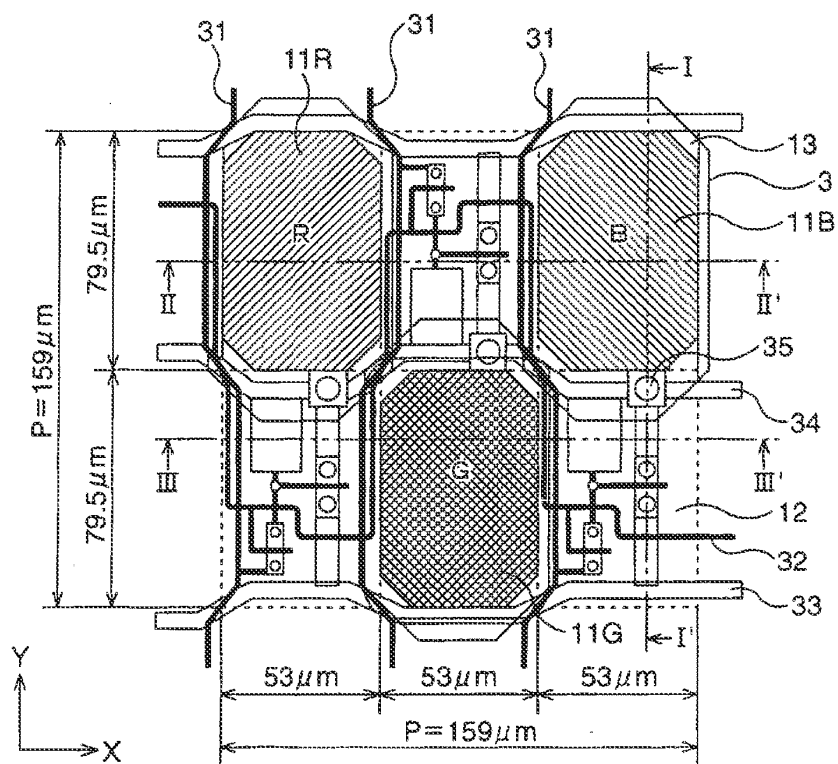


FIG. 4

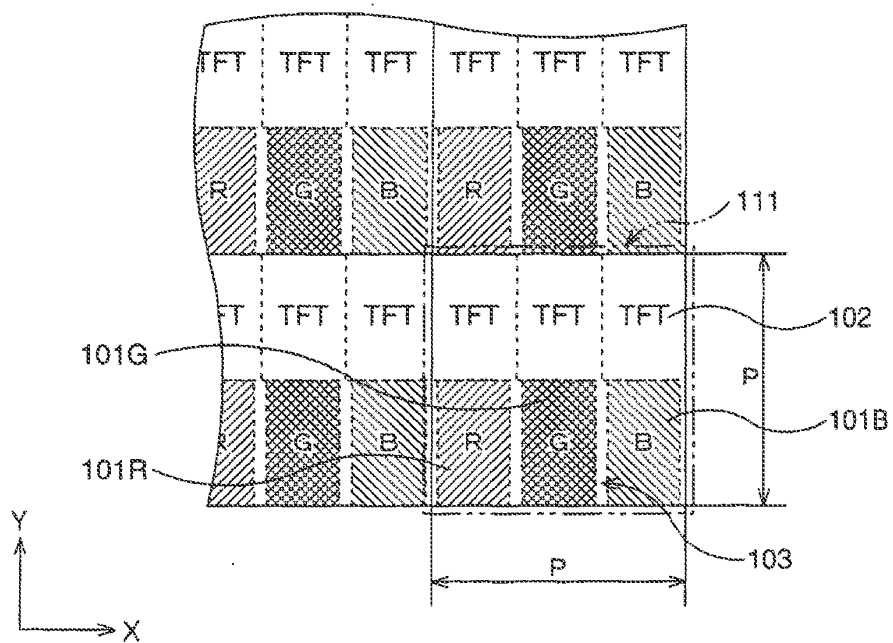
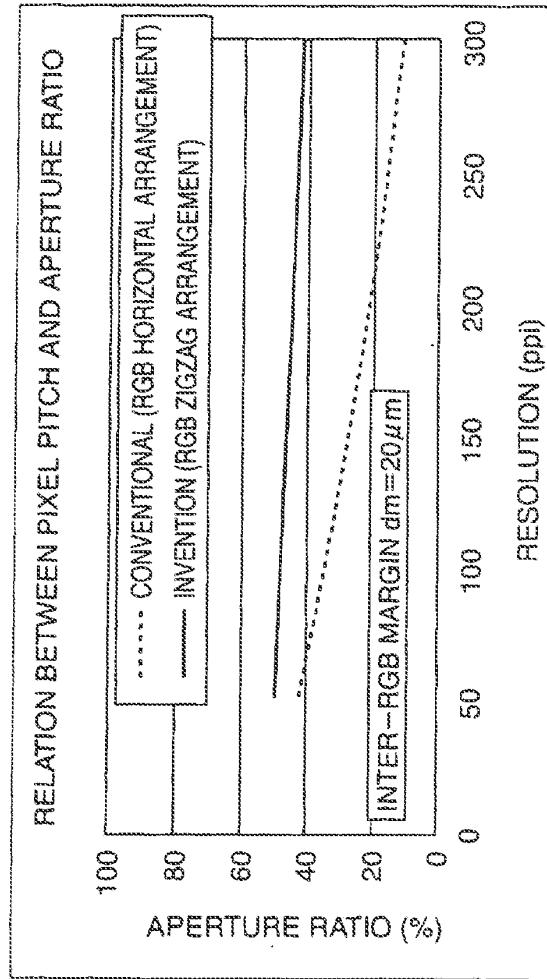


FIG. 5



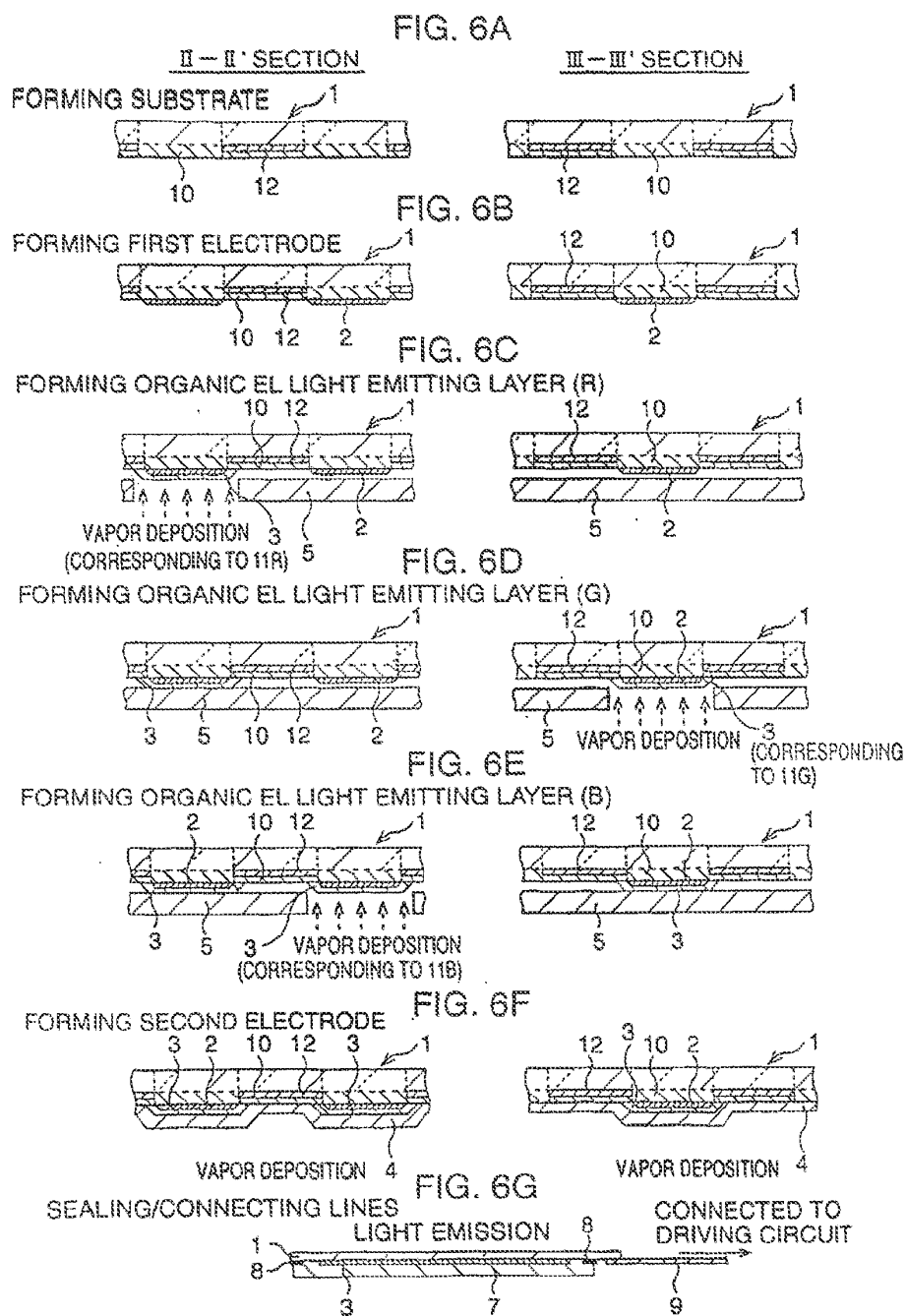


FIG. 7

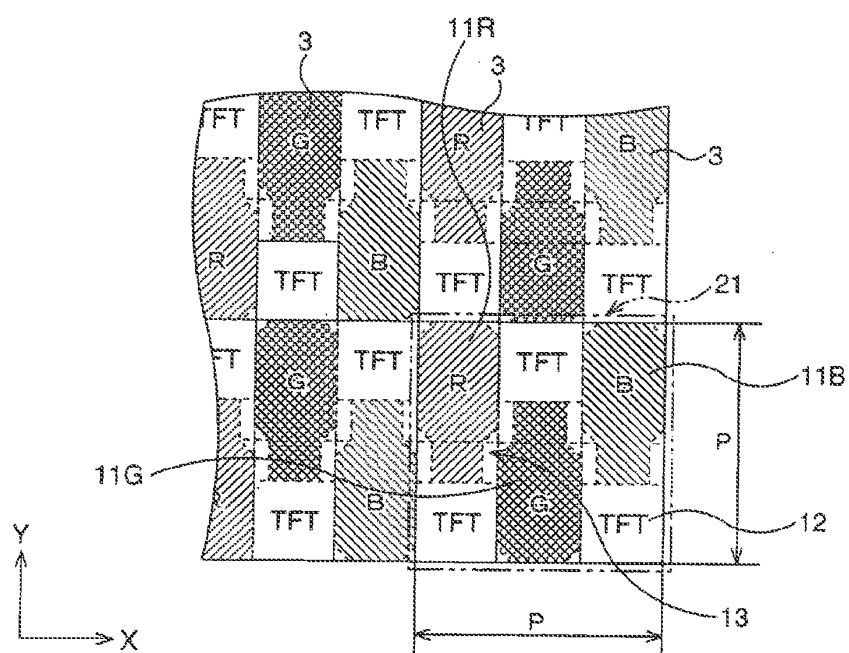
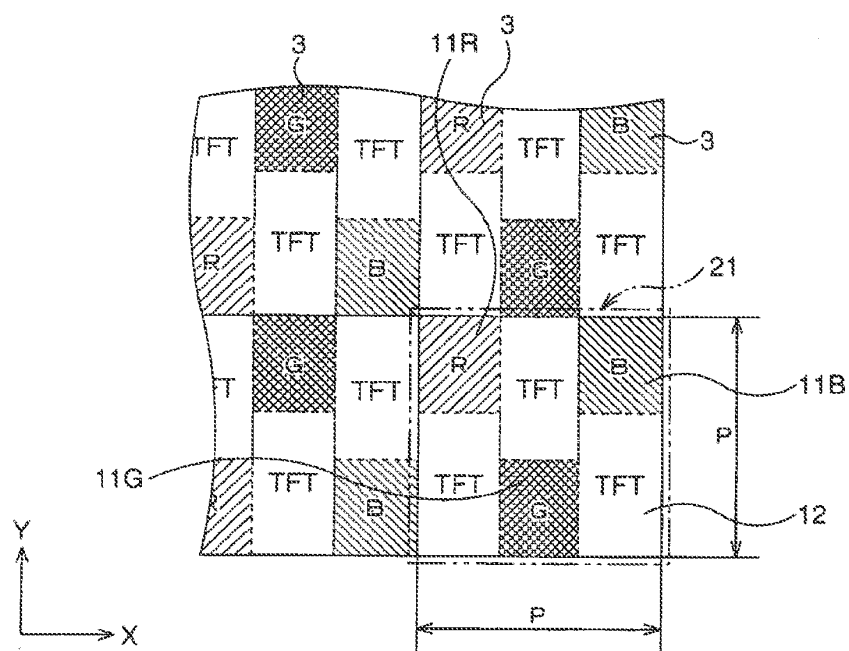


FIG. 8



INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP03/01464

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl.⁷ H05B33/12, H05B33/26, G09F9/30

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl.⁷ H05B33/00-33/28, G09F9/30

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1922-1996	Jitsuyo Shinan Toroku Koho	1996-2003
Kokai Jitsuyo Shinan Koho	1971-2003	Toroku Jitsuyo Shinan Koho	1994-2003

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2001-85162 A (Sharp Corp.), 30 March, 2001 (30.03.01), Page 5, column 8, line 29 to page 6, column 9, line 15; Fig. 3 (Family: none)	1, 6 8-9, 14 2-5, 7, 10-13, 15
Y	WO 99/20080 A1 (Toray Industries, Inc.), 22 April, 1999 (22.04.99), Full text & EP 955791 A	8-9, 14
A	JP 2002-215063 A (Sony Corp.), 31 July, 2002 (31.07.02), (Family: none)	1

☒ Further documents are listed in the continuation of Box C.☐ See patent family annex.

* Special categories of cited documents:

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document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art document member of the same patent family

"&"

Date of the actual completion of the international search

03 April, 2003 (03.04.03)

Date of mailing of the international search report

15 April, 2003 (15.04.03)

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Facsimile No.

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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2002-221917 A (Sony Corp.), 09 August, 2002 (09.08.02), # US 2002/0070909 A1	1
A	JP 60-218626 A (Sharp Corp.), 01 November, 1985 (01.11.85), (Family: none)	1

Form PCT/ISA/210 (continuation of second sheet) (July 1998)

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(19)  **Europäisches Patentamt**
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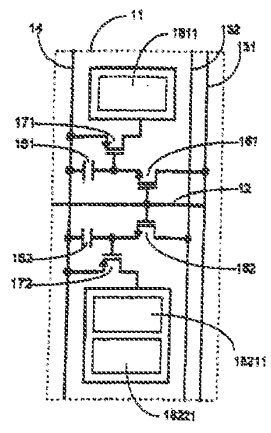
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 (30) Priority: 29.01.1999 JP 2162399
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(54) **Organic electroluminescent display device**

(57) The invention provides a method and apparatus to obtain accurate gradation by obtaining an accurate ratio of light emitting parts in a display device which implements gradation by forming a plurality of TFTs and a plurality of OLEDs in each pixel, interconnecting the TFTs and OLEDs, and switching an on and off state of the TFTs, and controlling a light emitting area of the OLEDs. A plurality of OLEDs have the same shape, and gradation can be implemented by controlling the number of OLEDs that emit light at a given time. Preferably a plurality of OLEDs have a round shape. Also preferably plurality of OLEDs are ranged at the same interval in a vertical and/or horizontal direction. According to this structure, because the light emitting areas of the plurality of OLEDs become equal to each other, by controlling the number of OLEDs, a ratio of the light emitting areas can be accurately obtained.

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Description

[0001] This invention relates to a display device, particularly a thin film transistor driven organic electro-luminescent display device (hereafter referred to as TFT-OELD) which is driven by a thin film transistor (hereafter referred to as TFT) and provided with an organic electro-luminescent element (hereafter referred to as OELD) preferably of a high polymer system formed in a liquid phase process.

[0002] TFT-OELD is promising because it is a display device which realizes light-weightness, thinness, smallness, higher accuracy, wider view angle, lower electric consumption, and the like. Fig. 1 shows a conventional TFT-OELD. Fig. 2 shows a cross-sectional view of a conventional TFT-OELD. Here, there is only one pixel 11 depicted, but there are actually many pixels 11 in plural rows and lines. Here, OELD 18 is a high polymer system, formed by a liquid phase process, such as spin coating, blade coating, ink jet, or the like.

[0003] In order to implement gradation, in the case of the structure shown in Fig. 1, a gate voltage of a driving TFT 17 is made to change and conductance is changed, so electric current which flows in the OELD 18 needs to be controlled. However, according to this method, particularly in half tone, irregularity of transistor characteristics of the driving TFT 17 appears as brightness irregularity of the OELD 18, and there is a problem such that the screen becomes non-uniform.

[0004] Therefore, as shown in Fig. 3, a method is considered which implements gradation by changing a light emitting area of the OELD 18 (Japanese Patent Application 9-233107). Fig. 4 shows a driving method of this display. A scanning electric potential 31 is applied to a scanning line 12, and a signal line 13 is formed of a signal line (lower bit) 131 and a signal line (upper bit) 132. A signal electric potential (lower bit) 321 and signal electric potential (upper bit) 322 are respectively applied as a signal electric potential 32. A driving TFT 17 is formed of a driving TFT (lower bit) 171 and a driving TFT (upper bit) 172, and the OELD 18 is formed of an OELD (lower bit) 181 and an OELD (upper bit) 182. In this example, 2-bit 4 gradation is considered, so an area ratio between OELD (lower bit) 181 and OELD (upper bit) 182 is 1:2.

[0005] In this method, the driving TFT 17 takes either a substantially completely on state or a substantially completely off state. In the on state, the resistance of the driving TFT 17 is small enough to be ignored, compared to the resistance of OELD 18, and the electric current amount which flows in the driving TFT 17 and OELD 18 is substantially determined by only the resistance of the OELD 18.

[0006] Therefore, irregularity of transistor characteristics of the driving TFT 17 does not appear as brightness irregularity of the OELD 18. Furthermore, in the off state, voltage applied to the OELD 18 becomes less than a threshold voltage, so the OELD 18 does not emit

light at all, and, needless to say, irregularity of transistor characteristics of the driving TFT 17 does not appear as brightness irregularity of the OELD 18.

[0007] Fig. 5 is a cross-sectional view of TFT-OELD which implements gradation display by changing a light emitting area of the OELD 18 shown in Figs. 3 and 4. Fig. 5(a) is a cross-sectional view of the OELD (lower bit) 181, and Fig. 5(b) is a cross-sectional view of the OELD (upper bit) 182. The ratio between the light emitting part 25 of the OELD (lower bit) 181 and the light emitting part 25 of the OELD (upper bit) 182 is preferably 1:2.

[0008] A light emitting layer 22 is an OELD of a high polymer system and formed in a liquid phase process. A surface of a bank 24 is lyophobic and the light emitting layer 22 does not remain. Therefore, the area of the OELD 18 is determined by patterning. With respect to a side surface of the bank 24, the materials and processing determine whether the side surface of the bank 24 becomes lyophobic or lyophilic.

[0009] Fig. 5 shows the case of a lyophilic side surface of the bank 24. As a phenomenon that is characteristic of a liquid phase process, the light emitting layer 22 has a cross-sectional shape which is pulled toward the side surface of the bank 24. In this case, electric current flows into a thinner part of the light emitting layer 22, and this part becomes a light emitting part 25. The cross-sectional shape of the light emitting layer 22 described here is sensitive to liquid amount, liquid material, an initial position of the liquid, and a state, temperature, atmosphere, or the like of a substrate, and which are difficult to control. That is, it is difficult to obtain an absolute value of a desired light emitting area. Because of this, it is difficult to obtain an accurate ratio of 1:2 between the light emitting part 25 of the OELD (lower bit) 181 and the light emitting part 25 of the OELD (upper bit) 182, and ultimately, it is difficult to obtain accurate gradation.

[0010] Fig. 6 is a cross-sectional view of OELD (lower bit) 181 (Fig. 6(a)) and a cross-sectional view of OELD (upper bit) 182 (Fig. 6(b)) in the same manner as in Fig. 5. In Fig. 6, the side surface of the bank 24 is lyophobic. As a phenomenon that is characteristic of a liquid phase process, the light emitting layer 22 has a cross-sectional shape which is distant from the side surface of the bank 24. In this case as well, electric current flows into the thinner part of the light emitting layer 22, and this part becomes the light emitting part 25. In this case as well, in the same manner as in the case of Fig. 5, it is difficult to obtain an accurate ratio of 1:2 between the light emitting part 25 of the OELD (lower bit) 181 and the light emitting part 25 of the OELD (upper bit) 182, so it is difficult to obtain accurate gradation.

[0011] Therefore, one aspect of this invention is to obtain an accurate ratio of the light emitting parts, and accurate gradation. Therefore, the invention may provide a display device in which gradation is implemented by forming a plurality of TFTs and a plurality of OELDs

in each pixel, directly connecting the TFTs and OLEDs, switching an on and off state of the TFTs, and controlling an area of the OLEDs, that emits light, wherein the plurality of OLEDs have the same shape, and gradation is implemented by controlling the number of OLEDs that are created to emit light.

[0012] According to this structure, as a characteristic phenomenon of a liquid phase process, even if an OLED becomes a cross-sectional shape which is pulled in to a side surface of a bank or is distant from the side surface of the bank, the light emitting part of each OLED is the same area, and accurate gradation can be obtained. In this structure as well, it is difficult to obtain an absolute value of a desired light emitting area, but the light emitting area of a plurality of OLEDs becomes equal, so the ratio of the light emitting areas can be accurate by controlling the number of OLEDs.

[0013] The display device may also include a plurality of OLEDs that have a round shape. According to this structure, the light emitting part of each OLED can reliably be the same area, and accurate gradation can be obtained. The reasons are as follows. When an OLED has a shape with a rectangular vertex (or vertices), there is a possibility that a phenomenon may occur, for example, that the vertex becomes pulled in or the vertex cannot be filled. This phenomenon prevents a user from obtaining accurate gradation for the same reason as in the problems of a cross-sectional shape as described above. This phenomenon is more sensitive to the liquid amount, liquid material, initial position of liquid, and the state, temperature, and atmosphere of a substrate, more so than the problems in a cross-sectional shape described above, and it is difficult to control this phenomenon between adjacent OLEDs. By making the OLED round shaped, this phenomenon can be avoided.

[0014] The display device may also include a plurality of OLEDs arranged at the same interval in a horizontal and/or vertical direction. According to this structure, the light emitting part of each OLED is made to be more reliably the same area, and accurate gradation can be obtained. The reasons are as follows. When an OLED is formed by spin coating or blade coating, the light emitting layer which is coated over all the pixels, due to the lyophobicity of a surface of the bank, the light emitting layer naturally flows into a convex part of the bank. In the case of ink jet as well, this may sometimes happen. At this time, when a concave area surrounded by a bank convex part is large, the light emitting layer coated over this part flows into a convex bank portion, so the light emitting layer becomes thick. When the convex area surrounded by the bank concave part is small, the light emitting layer becomes thin. Ultimately, irregularity of film thickness of the light emitting layer is generated. This irregularity can be avoided by arranging a plurality of OLEDs at the same interval in a horizontal or vertical direction.

[0015] Additionally, according to this structure, when the OLEDs are formed by an ink jet process, ink

jetting can be performed at the same interval, so fabrication can be simplified.

[0016] Embodiments of the present invention will now be described, by way of further example only and with reference to the accompanying drawings, in which:-

Fig. 1 is a diagram showing a pixel of a conventional TFT-OLED which implements a gradation display by changing a TFT conductance;

Fig. 2 is a cross-sectional view of a TFT-OLED;

Fig. 3 is a diagram showing one pixel of a TFT-OLED which implements a gradation display by changing a conventional OLED light emitting area;

Fig. 4 is a diagram showing a TFT-OLED driving method which implements a gradation display by changing a conventional OLED light emitting area;

Figs. 5(a) and 5(b) are cross-sectional views of an OLED in a TFT-OLED which implements a gradation display by changing a conventional OLED light emitting area (when the side surface of the bank is lyophilic), where Fig. 5(a) is a diagram of an OLED (lower bit) and Fig. 5(b) is a diagram of an OLED (upper bit);

Figs. 6(a) and 6(b) are cross-sectional views of an OLED in a TFT-OLED which implements a gradation display by changing a conventional OLED light emitting area (when the side surface of the bank is lyophobic), where Fig. 6(a) is a diagram of an OLED (lower bit), and Fig. 6(b) is a diagram of an OLED (upper bit);

Fig. 7 is a diagram showing one pixel of a TFT-OLED related to embodiment 1 of this invention;

Fig. 8 is a diagram showing one pixel of a TFT-OLED related to embodiment 2 of this invention; and

Fig. 9 is a diagram showing one pixel of a TFT-OLED related to embodiment 3 of this invention.

[0017] The following explains preferred embodiments of this invention, based upon the drawings.

[0018] Fig. 7 is a diagram showing a pixel of a TFT-OLED related to a first embodiment of this invention. Here, only one pixel 11 is depicted, but many pixels 11 actually exist in a plurality of rows and a plurality of lines.

[0019] An OLED (lower bit) 181 is formed of OLED (lower bit • rectangular) 1811, and an OLED (upper bit) 182 is formed of OLED (upper bit • first • rectangular) 18211 and an OLED (upper bit • second • rectangular) 18221. The OLED (lower bit • rectangular) 1811, the OLED (upper bit • first • rectangular) 18211, and the OLED (upper bit • second • rectangular) 18221 have the same shape, so the same light emitting area can be obtained, and accurate gradation can be obtained by changing the number of OLEDs that are caused to emit light.

[0020] Fig. 8 is a diagram showing a pixel of a TFT-OLED related to another embodiment of this invention. Here, only one pixel 11 is depicted, but many pixels 11

actually exist in a plurality of lines and a plurality of rows.

[0021] An OELD (lower bit) 181 is formed of an OELD (lower bit·round shape) 1812, and an OELD (upper bit) 182 is formed of OELD (upper bit·first·round shape) 18212 and OELD (upper bit·second·round shape) 18222. The OELD (lower bit·round shape) 1812, the OELD (upper bit·first·round shape) 18212, and the OELD (upper bit·second·round shape) 18222 have the same round shape, so the same light emitting area can be reliably obtained, and accurate gradation can be obtained.

[0022] Fig. 9 is a diagram showing a pixel of a TFT-OELD related to another embodiment of this invention. Here, only one pixel 11 is depicted, but many pixels 11 actually exist in a plurality of lines and a plurality of rows.

[0023] An OELD (lower bit) 181 is formed of an OELD (lower bit·round shape) 1812, and an OELD (upper bit) 182 is formed of an OELD (upper bit·first·round shape) 18212 and an OELD (upper bit·second·round shape) 18222. The OELD (lower bit·round shape) 1812, the OELD (upper bit·first·round shape) 18212, and the OELD (upper bit·second·round shape) 18222 are arranged at the same interval in horizontal and vertical directions within the pixel 11, and also with respect to the adjacent pixel 11. Because of this, the light emitting part of each OELD can more reliably have the same area, and accurate gradation can be obtained.

[0024] Furthermore, as an EL element formed in each pixel, in the first embodiment (Fig. 7), a rectangular element is shown as an example, and in the second and third embodiments (Figs. 8 and 9, respectively), a round-shaped element is shown, but this invention is not limited to these. Accurate gradation can also be obtained in a polygonal or elliptic-shaped element. In particular, an elliptic element, as in the case of a round shape, does not have a vertex such as is present in the case of a rectangular shape, so there is no problem such that the vertex cannot be filled by the light emitting layer.

[0025] As described above, according to this invention, by controlling the area of an electroluminescent element that emits light, accurate gradation can be realized.

Claims

1. A display device, comprising:

a plurality of thin film transistors formed in each pixel; and
a plurality of organic electro-luminescent elements formed in each pixel, the thin film transistors being connected to the organic electro-luminescent elements, the display device switching an on and off state of the thin film transistors and controlling the area which emits electro-luminescent light, each of the plurality

of organic electro-luminescent elements having the same shape, and the display device implementing gradation by controlling the number of organic electro-luminescent elements that emit light at any given time.

2. The display device as set forth in claim 1, wherein the plurality of organic electro-luminescent elements are round in shape.
3. The display device as set forth in claim 1, wherein the plurality of organic electro-luminescent elements are arranged in horizontal and vertical directions at equal intervals.
4. The display device as set forth in claim 1, wherein the plurality of organic electro-luminescent elements are arranged in a horizontal direction at equal intervals.
5. The display device as set forth in claim 1, wherein the plurality of organic electro-luminescent elements are arranged in a vertical direction at equal intervals.
6. A method of forming a display device, comprising:

forming a plurality of thin film transistors and a plurality of organic electro-luminescent elements in each pixel;
inter-connecting the thin film transistors and the organic electro-luminescent elements;
switching an on and off state of the thin film transistors;
controlling the area which emits electro-luminescent light, each of the plurality of organic electro-luminescent elements being formed to have the same shape; and
controlling the number of organic electro-luminescent elements that emit light to implement gradation.

7. The method as set forth in claim 6, comprising the step of forming the plurality of organic electro-luminescent elements to be round in shape.
8. The method as set forth in claim 6, comprising the step of forming the plurality of organic electro-luminescent elements in horizontal and vertical directions at equal intervals.
9. The method as set forth in claim 6, comprising the step of forming the plurality of organic electro-luminescent elements in a horizontal direction at equal intervals.
10. The method as set forth in claim 6, comprising the step of forming the plurality of organic electro-lumi-

nescent elements in a vertical direction at equal intervals.

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Fig. 1

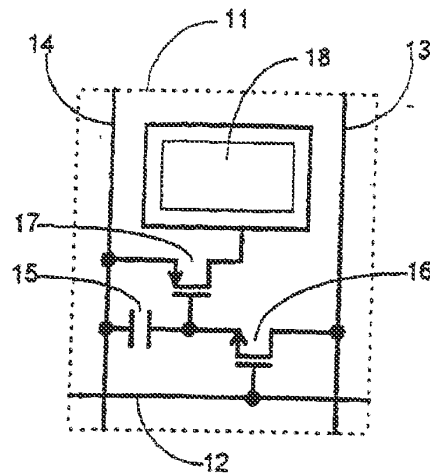


Fig. 2

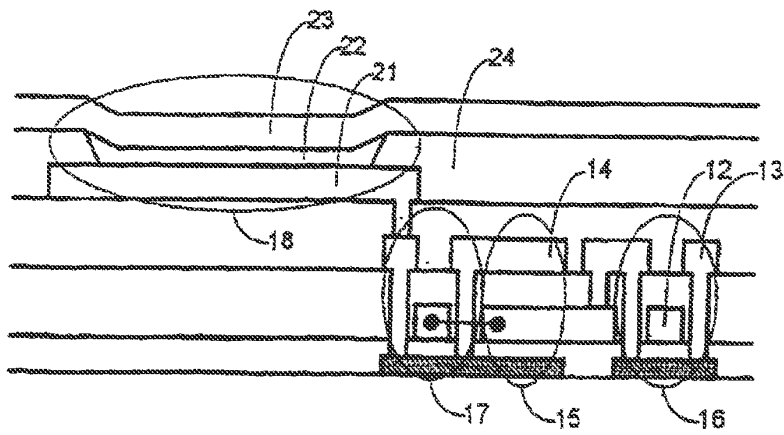


Fig. 3

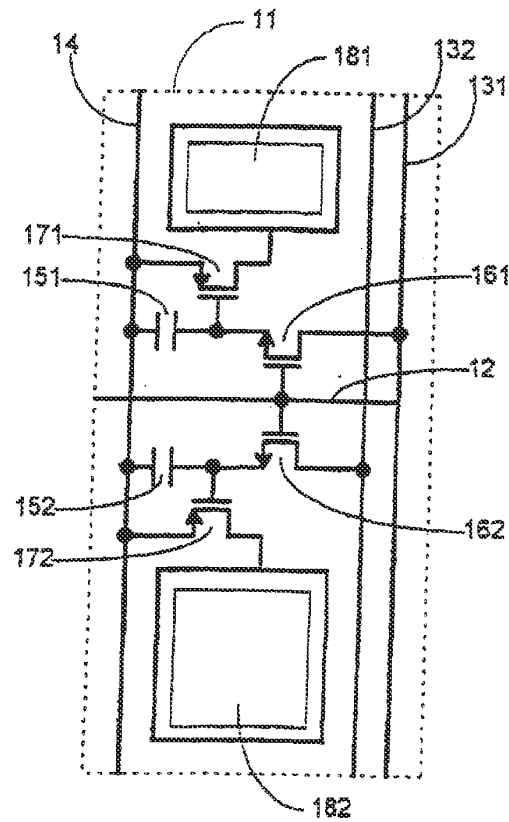


Fig. 4

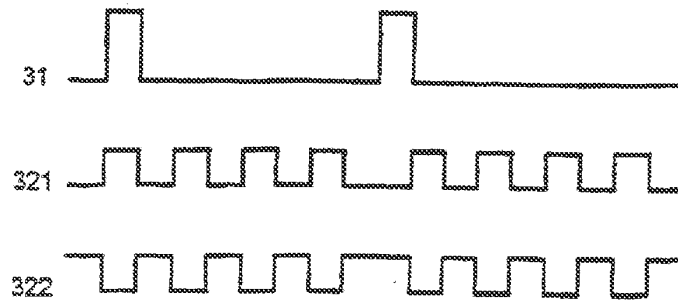


Fig. 5

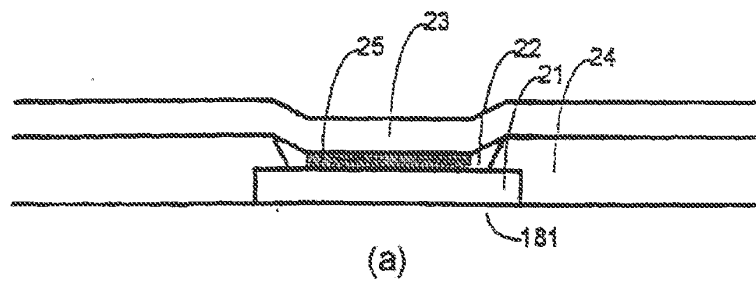
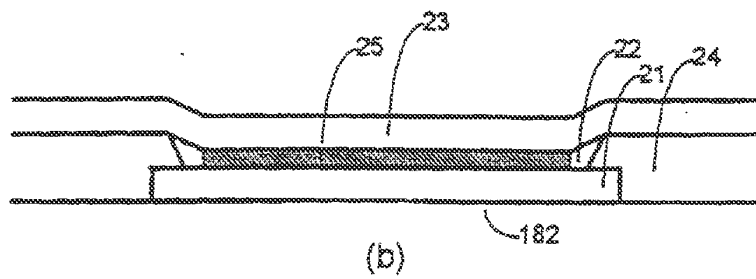


Fig. 6

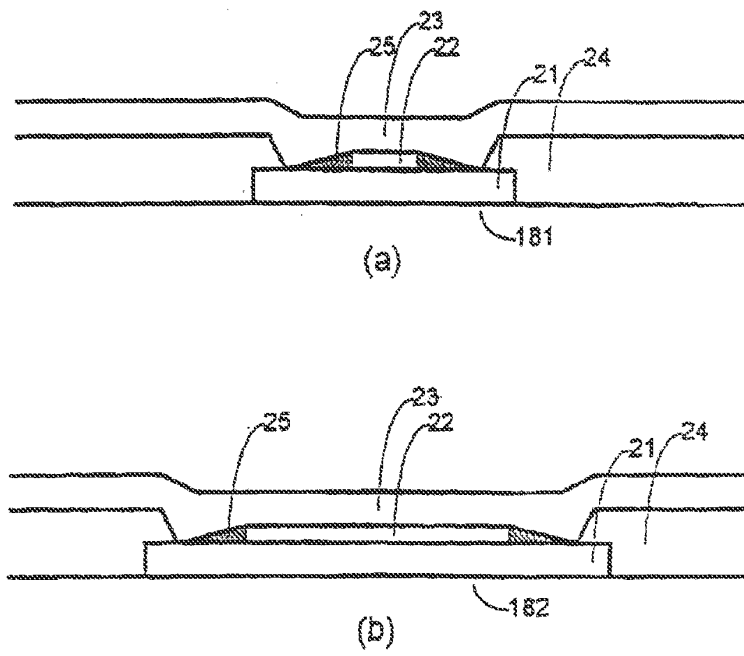


Fig. 7

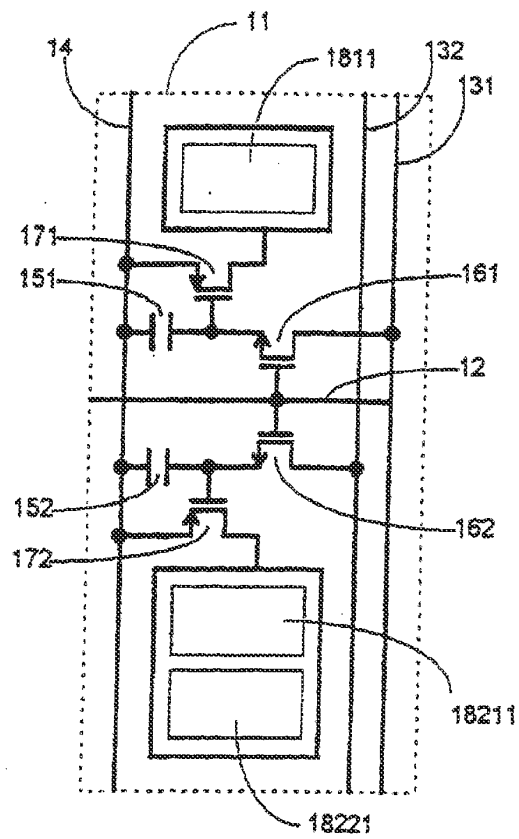
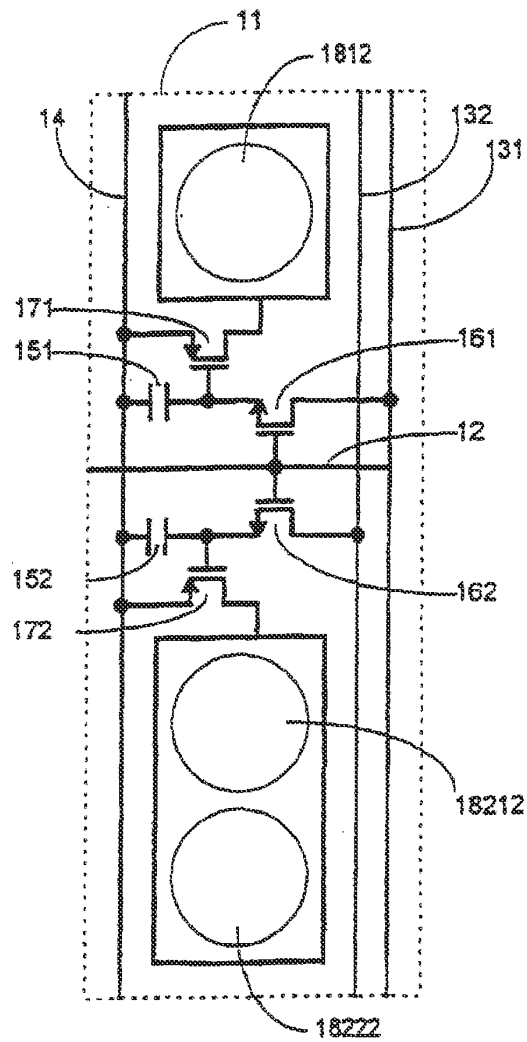
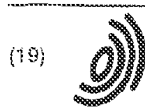


Fig. 8





(19)

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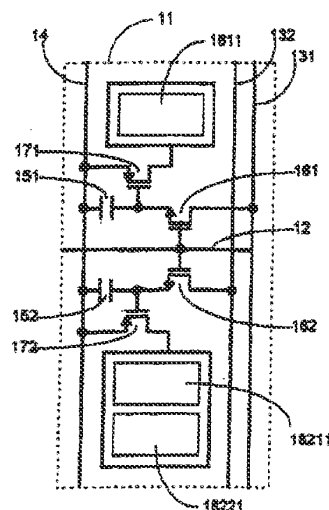
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(54) Organic electroluminescent display device

(57) The invention provides a method and apparatus to obtain accurate gradation by obtaining an accurate ratio of light emitting parts in a display device which implements gradation by forming a plurality of TFTs and a plurality of OLEDs in each pixel, interconnecting the TFTs and OLEDs, and switching an on and off state of the TFTs, and controlling a light emitting area of the OLEDs. A plurality of OLEDs have the same shape, and gradation can be implemented by controlling the number of OLEDs that emit light at a given time. Preferably a plurality of OLEDs have a round shape. Also preferably plurality of OLEDs are ranged at the same interval in a vertical and/or horizontal direction. According to this structure, because the light emitting areas of the plurality of OLEDs become equal to each other, by controlling the number of OLEDs, a ratio of the light emitting areas can be accurately obtained.

Fig. 7



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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	SARMA K R ET AL: "ACTIVE-MATRIX LCDS USING GRAY SCALE IN HALFTONE METHODS" PROCEEDINGS OF THE SID,US,SOCIETY FOR INFORMATION DISPLAY. PLAYA DEL REY, CA, vol. 31, no. 1, 1990, pages 7-11, XP000115902 * page 7, right-hand column, paragraph 2 - page 9, left-hand column, paragraph 1 * * figures 2-5 *	1,6	G09G3/32
P,A, D	EP 0 949 603 A (SEIKO EPSON CORP) 13 October 1999 (1999-10-13) * column 6, line 5 - line 44 * * figures 1.2 *	1,6	
A	US 5 585 695 A (KITAI ADRIAN H) 17 December 1996 (1996-12-17) * abstract *	2,7	
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			G09G
The present search report has been drawn up for all claims			
Place of search		Date of completion of the search	Examiner
THE HAGUE		22 September 2000	Farricella, L
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

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**ANNEX TO THE EUROPEAN SEARCH REPORT
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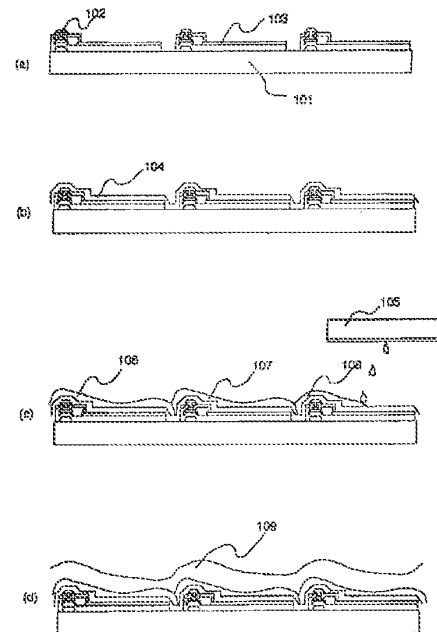
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(54) 【発明の名称】 アクティブマトリックス型有機EL表示体の製造方法

(57) 【要約】

【解決手段】 従来、パターニングができないとされた有機EL材料をインクジェット方式により形成および配列することで、赤、緑、青の発光色を備える有機発光層を画素毎に任意にパターニングすることが可能となった。これにより、フルカラー表示のアクティブマトリックス型有機EL表示体を実現した。

【効果】 安価で大画面のフルカラー表示体が製造可能となり、効果は大である。



【特許請求の範囲】

【請求項1】 薄膜トランジスタを有するガラス基板に形成された透明画素電極上層に正孔注入層が形成され、この上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層が形成され、更にこの上層に反射電極が形成されるアクティブマトリックス型有機EL表示体の製造方法において、前記有機発光層の形成および配列がインクジェット方式によりなされることを特徴とするアクティブマトリックス型有機EL表示体の製造方法。

【請求項2】 薄膜トランジスタを有するガラス基板に形成された透明画素電極上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層が形成され、更にこの上層に反射電極が形成されるアクティブマトリックス型有機EL表示体の製造方法において、前記有機発光層の形成および配列がインクジェット方式によりなされることを特徴とするアクティブマトリックス型有機EL表示体の製造方法。

【請求項3】 薄膜トランジスタを有するガラス基板に形成された反射画素電極上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層が形成され、この上層に正孔注入層が形成され、更にこの上層に透明電極が形成されるアクティブマトリックス型有機EL表示体の製造方法において、前記有機発光層の形成および配列がインクジェット方式によりなされることを特徴とするアクティブマトリックス型有機EL表示体の製造方法。

【請求項4】 薄膜トランジスタを有するガラス基板に形成された反射画素電極上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層が形成され、更にこの上層に透明電極が形成されるアクティブマトリックス型有機EL表示体の製造方法において、前記有機発光層の形成および配列がインクジェット方式によりなされることを特徴とするアクティブマトリックス型有機EL表示体の製造方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】 本発明は、薄膜トランジスタを用いたアクティブマトリックス型のEL表示体のインクジェット方式を用いた製造方法に関する。

【0002】

【従来の技術】 有機EL素子は、蛍光性有機化合物を含む薄膜を、陰極と陽極とで挟んだ構成を有し、前記薄膜に電子および正孔（ホール）を注入して再結合させることにより励起子（エキシトン）を生成させ、このエキシトンが失活する際の光の放出（蛍光・燐光）を利用して発光させる素子である。

【0003】 この有機EL素子の特徴は、10V以下の低電圧で100～100000 cd/m² 程度の高輝度の面発光が可能であり、また蛍光物質の種類を選択するこ

とにより青色から赤色までの発光が可能なことである。

【0004】 有機EL素子は、安価な大面積フルカラー表示素子を実現するものとして注目を集めている（電子情報通信学会技術報告、第89巻、NO. 106、49ページ、1989年）。報告によると、強い蛍光を発する有機色素を発光層に使用し、青、緑、赤色の明るい発光を得ている。これは、薄膜状で強い蛍光を発し、ピンホール欠陥の少ない有機色素を用いたことで、高輝度なフルカラー表示を実現できたと考えられている。

10 【0005】 更に特開平5-78655号公報には、有機発光層の成分が有機電荷材料と有機発光材料の混合物からなる薄膜層を設け、濃度消光を防止して発光材料の選択幅を広げ、高輝度なフルカラー素子とする旨が提案されている。

【0006】 しかし、いずれの報告にも、実際のフルカラー表示パネルの構成や製造方法については言及されていない。

【0007】

20 【発明が解決しようとする課題】 前述の有機色素を用いた有機薄膜EL素子は、青、緑、赤の発光を示す。しかし、よく知られているように、フルカラー表示体を実現するためには、3原色を発光する有機発光層を画素毎に配置する必要がある。従来、有機発光層をパターンニングする技術は非常に困難とされていた。原因は、一つは反射電極材の金属表面が不安定であり、蒸着のパターンニング精度が出ないという点である。2つめは、正孔注入層および有機発光層を形成するポリマーや前駆体がフォトリソグラフィ等のパターンニング工程に対して耐性が無いという点である。

30 【0008】 本発明は、上述したような課題を解決するものであり、その目的は、有機発光層をインクジェット方式により画素毎にパターンニングしたアクティブマトリックス型EL表示体の製造方法を提供することにある。

【0009】

【課題を解決するための手段】 本発明に関わるアクティブマトリックス型有機EL表示体の製造方法は、薄膜トランジスタを有するガラス基板に形成された透明画素電極上層に正孔注入層が形成され、この上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層が形成され、更にこの上層に反射電極が形成されるアクティブマトリックス型有機EL表示体の製造方法において、前記有機発光層の形成および配列がインクジェット方式によりなされることを特徴とし、また、薄膜トランジスタを有するガラス基板に形成された透明画素電極上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層が形成され、更にこの上層に反射電極が形成されるアクティブマトリックス型有機EL表示体の製造方法において、前記有機発光層の形成および配列がインクジェット方式によりなされることを特徴とする。

【0010】更に、薄膜トランジスタを有するガラス基板上に形成された反射画素電極上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層が形成され、この上層に正孔注入層が形成され、更にこの上層に透明電極が形成されるアクティブマトリックス型有機EL表示体の製造方法において、前記有機発光層の形成および配列がインクジェット方式によりなされることを特徴とし、また、薄膜トランジスタを有するガラス基板上に形成された反射画素電極上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層が形成され、更にこの上層に透明電極が形成されるアクティブマトリックス型有機EL表示体の製造方法において、前記有機発光層の形成および配列がインクジェット方式によりなされることを特徴とする。

【0011】本発明は、要するに図3に示すように、基板上に形成された信号線301、ゲート線302、画素電極303および薄膜トランジスタ304上に、インクジェット法により、赤、緑、青色の有機発光材料をパターンニング塗布することで、フルカラー表示を実現するのである。

【0012】

【発明の実施の形態】以下、本発明の好適な実施形態について図面を参照して説明する。

【0013】（実施例1）図1に示すように、ガラス基板101上に薄膜トランジスタ102を形成してから、ITO透明画素電極103を形成する。

【0014】正孔注入材料としてポリマー前駆体であるポリテトラヒドロチオフェニルフェニレンをコーティングする。加熱により、前駆体はポリフェニレンビニレンとなり、厚さ0.05ミクロンの正孔注入層104が形成される。

【0015】次に、インクジェットプリント装置105により赤、緑、青色を発色する発光材料をパターンニング塗布し、厚さ0.05ミクロンの発光層106、107、108を形成する。赤色発光材料にはシアノポリフェニレンビニレン、緑色発光材料にはポリフェニレンビニレン、青色発光材料にはポリフェニレンビニレンおよびポリアルキルフェニレンを使用する。これらの有機EL材料はケンブリッジ・ディスプレイ・テクノロジー社製であり、液状で入手可能である。

【0016】最後に、厚さ0.1~0.2ミクロンのMgAg反射電極109を蒸着法により形成する。

【0017】これにより、直視型のフルカラー有機EL表示体が完成する。

【0018】（実施例2）図2に示すように、ガラス基板201上に薄膜トランジスタ202を形成してから、AlLi反射画素電極203を形成する。

【0019】次に、インクジェットプリント装置207により赤、緑、青色を発色する発光材料をパターンニング塗布し、発光層204、205、206を形成する。赤

色発光材料にはシアノポリフェニレンビニレン、緑色発光材料にはポリフェニレンビニレン、青色発光材料にはポリフェニレンビニレンおよびポリアルキルフェニレンを使用する。これらの有機EL材料はケンブリッジ・ディスプレイ・テクノロジー社製であり、液状で入手可能である。

【0020】正孔注入材料としてポリマー前駆体であるポリテトラヒドロチオフェニルフェニレンをキャスト法により形成する。加熱により、前駆体はポリフェニレンビニレンとなり、正孔注入層208が形成される。

【0021】最後に、ITO透明電極209を蒸着法により形成する。

【0022】これにより、反射型のフルカラー有機EL表示体が完成する。

【0023】（実施例3）有機発光層の有機発光材料として2,3,6,7-テトラヒドロ-11-オキソ-1H,5H,11H-(1)ベンゾピラノ[6,7,8-ij]-キノリジン-10-カルボン酸を用い、有機正孔注入層材料として1,1-ビス-(4-N,N-ジトリルアミノフェニル)シクロヘキサンを用い、両者を混合することで緑色の発光材料とする。

【0024】同様に、赤色の有機発光材料として、2-1,3',4'-ジヒドロキシフェニル)-3,5,7-トリヒドロキシ-1-ベンゾピリリウムパークロレートを用いて正孔注入層材料と混合する。

【0025】更に、青色発光層には有機正孔注入材料としてトリス(8-ヒドロキシキノリノール)アルミニウムを用い、有機発光材料として、2,3,6,7-テトラヒドロ-9-メチル-11-オキソ-1H,5H,11H-(1)ベンゾピラノ[6,7,8-ij]-キノリジンを混合し、発光材料を作成する。

【0026】実施例1または実施例2と同様な工程で、各々の発光層をインクジェットプリント装置により局所パターンニングし、アクティブマトリックス型有機EL表示体を作成する。

【0027】なお、本実施例で使用した有機EL材料以外にも、アロマティックジアミン誘導体(TDP)、オキシアゾールダイマー(OXD)、オキシアゾール誘導体(PBD)、ジスチルアリーレン誘導体(DSA)、キノリノール系金属錯体、ベリリウム-ベンゾキノリノール錯体(Be bq)、トリフェニルアミン誘導体(MTDATA)、ジスチル誘導体、ピラゾリンダイマー、ルブレン、キナクリドン、トリアゾール誘導体、ポリフェニレン、ポリアルキルフルオレン、ポリアルキルチオフェン、アゾメチン亜鉛錯体、ポリフィリン亜鉛錯体、ベンゾオキサゾール亜鉛錯体、フェナントロリンユウロピウム錯体を使用できるが、これに限られる物ではない。

【0028】

【発明の効果】従来、パターンニングができないとされた有機EL材料をインクジェット方式により形成および配列することでパターンニングが可能となり、フルカラー表

示のアクティブマトリクス型有機EL表示体を実現した。これにより、安価で大画面のフルカラー表示体が製造可能となり、効果は大である。

【図面の簡単な説明】

【図1】本発明の第1の実施形態におけるアクティブマトリクス型有機EL表示体の工程を示す図である。

【図2】本発明の第2の実施形態におけるアクティブマトリクス型有機EL表示体の工程を示す図である。

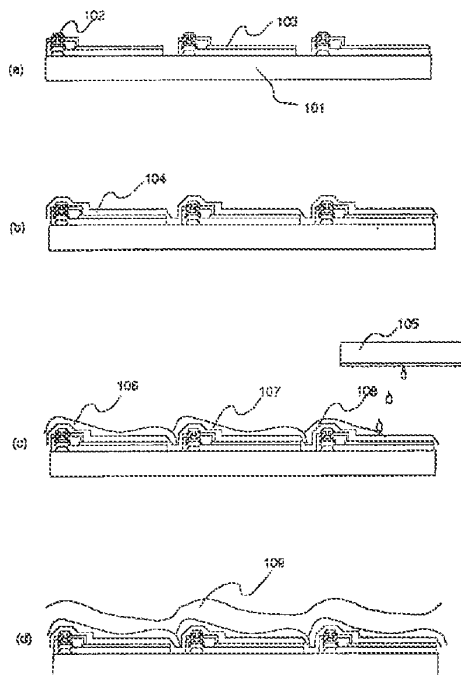
【図3】本発明の薄膜トランジスタ上にインクジェット法により形成された発色層を示す図である。

【符号の説明】

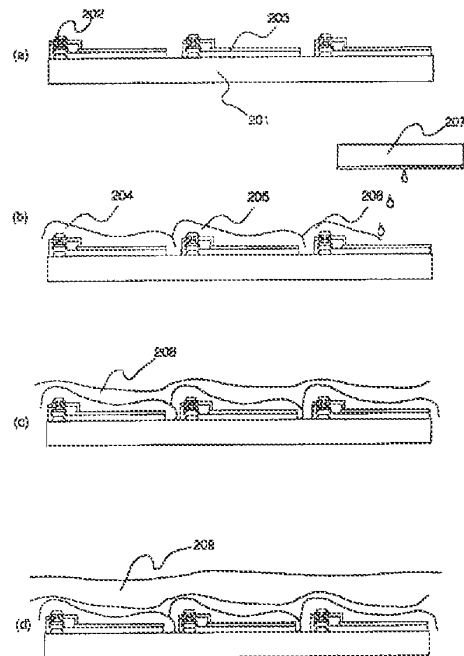
101 ガラス基板
102 薄膜トランジスタ
103 透明画素電極
104 正孔注入層
105 インクジェットプリンタヘッド
106 有機発光層（第1色）
107 有機発光層（第2色）

* 108 有機発光層（第3色）
109 反射電極
201 ガラス基板
202 薄膜トランジスタ
203 反射画素電極
204 有機発光層（第1色）
205 有機発光層（第2色）
206 有機発光層（第3色）
207 インクジェットプリンタヘッド
208 正孔注入層
209 透明電極
301 信号線
302 ゲート線
303 画素電極
304 薄膜トランジスタ
305 有機発光層（第1色）
306 有機発光層（第2色）
* 307 有機発光層（第3色）

【図1】



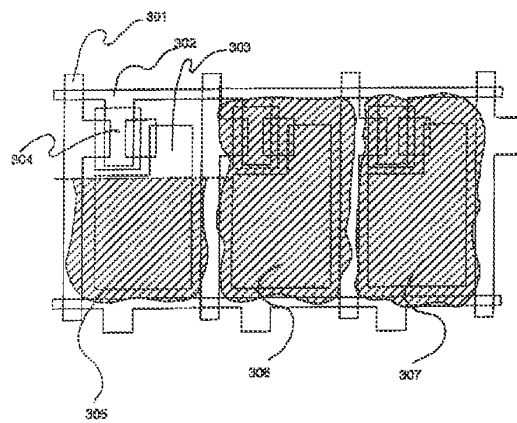
【図2】



(5)

特開平10-12377

【図3】



【公報種別】特許法第17条の2の規定による補正の掲載
【部門区分】第7部門第1区分
【発行日】平成13年3月16日(2001. 3. 16)

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【出願番号】特願平8-158671
【国際特許分類第7版】

H05B 33/10

B41J 2/01

【F1】

H05B 33/10

B41J 3/04 101 2

【手続補正書】

【提出日】平成11年10月29日(1999. 10. 29)

【手続補正1】

【補正対象書類名】明細書

【補正対象項目名】特許請求の範囲

【補正方法】変更

【補正内容】

【特許請求の範囲】

【請求項1】 薄膜トランジスタを有するガラス基板に形成された透明画素電極上層に正孔注入層が形成され、この上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層が形成され、更にこの上層に反射電極が形成されるアクティブマトリックス型有機EL表示体の製造方法において、前記有機発光層の形成および配列がインクジェット方式によりなされることを特徴とするアクティブマトリックス型有機EL表示体の製造方法。

【請求項2】 薄膜トランジスタを有するガラス基板に形成された透明画素電極上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層が形成され、更にこの上層に反射電極が形成されるアクティブマトリックス型有機EL表示体の製造方法において、前記有機発光層の形成および配列がインクジェット方式によりなされることを特徴とするアクティブマトリックス型有機EL表示体の製造方法。

【請求項3】 薄膜トランジスタを有するガラス基板に形成された反射画素電極上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層が形成され、この上層に正孔注入層が形成され、更にこの上層に透明電極が形成されるアクティブマトリックス型有機EL表示体の製造方法において、前記有機発光層の形成および配列がインクジェット方式によりなされることを特徴とするアクティブマトリックス型有機EL表示体の製造方法。

【請求項4】 薄膜トランジスタを有するガラス基板に形成された反射画素電極上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層が形成され、更にこの上層に透明電極が形成されるアクティブマトリックス型有機EL表示体の製造方法において、前記有機発光層の形成および配列がインクジェット方式によりなされることを特徴とするアクティブマトリックス型有機EL表示体の製造方法。

【請求項5】 前記インクジェット方式でポリマーまたはその前駆体を供給して、前記有機発光層を形成する請求項1ないし4のいずれかに記載のアクティブマトリックス型有機EL表示体の製造方法。

【請求項6】 シアノポリフェニレンにより、赤色の発光色を有する前記有機発光層を形成する請求項1ないし5のいずれかに記載のアクティブマトリックス型有機EL表示体の製造方法。

【請求項7】 ポリフェニレンにより、緑色の発光色を有する前記有機発光層を形成する請求項1ないし6のいずれかに記載のアクティブマトリックス型有機EL表示体の製造方法。

【請求項8】 ポリフェニレンおよびポリアルキルフェニレンにより、青色の発光色を有する前記有機発光層を形成する請求項1ないし7のいずれかに記載のアクティブマトリックス型有機EL表示体の製造方法。

【請求項9】 前記有機発光層をポリアルキルフルオレンで構成する請求項1ないし8のいずれかに記載のアクティブマトリックス型有機EL表示体の製造方法。

【手続補正2】

【補正対象書類名】明細書

【補正対象項目名】0009

【補正方法】変更

【補正内容】

【0009】

【課題を解決するための手段】本発明に関わるアクティ

ブマトリックス型有機EL表示体の製造方法は、薄膜トランジスタを有するガラス基板に形成された透明画素電極上層に正孔注入層が形成され、この上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層（特にポリマーまたはその前駆体よりなる発光材料で構成された有機発光層）が形成され、更にこの上層に反射電極が形成されるアクティブマトリックス型有機EL表示体の製造方法において、前記有機発光層の形*

*成および配列がインクジェット方式によりなされることを特徴とする。また、薄膜トランジスタを有するガラス基板に形成された透明画素電極上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層が形成され、更にこの上層に反射電極が形成されるアクティブマトリックス型有機EL表示体の製造方法において、前記有機発光層の形成および配列がインクジェット方式によりなされることを特徴とする。

【手続補正書】

【提出日】平成11年11月25日（1999. 11. 25）

【手続補正1】

【補正対象書類名】明細書

【補正対象項目名】特許請求の範囲

【補正方法】変更

【補正内容】

【特許請求の範囲】

【請求項1】 薄膜トランジスタを有するガラス基板に形成された透明画素電極上層に正孔注入層が形成され、この上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層が形成され、更にこの上層に反射電極が形成されるアクティブマトリックス型有機EL表示体の製造方法において、前記有機発光層をその形状および配列が最終パターンとなるようインクジェット方式により形成することを特徴とするアクティブマトリックス型有機EL表示体の製造方法。

【請求項2】 薄膜トランジスタを有するガラス基板に形成された透明画素電極上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層が形成され、更にこの上層に反射電極が形成されるアクティブマトリックス型有機EL表示体の製造方法において、前記有機発光層をその形状および配列が最終パターンとなるようインクジェット方式により形成することを特徴とするアクティブマトリックス型有機EL表示体の製造方法。

【請求項3】 薄膜トランジスタを有するガラス基板に形成された反射画素電極上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層が形成され、この上層に正孔注入層が形成され、更にこの上層に透明電極が形成されるアクティブマトリックス型有機EL表示体の製造方法において、前記有機発光層をその形状および配列が最終パターンとなるようインクジェット方式により形成することを特徴とするアクティブマトリックス型有機EL表示体の製造方法。

【請求項4】 薄膜トランジスタを有するガラス基板に形成された反射画素電極上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層が形成され、更にこの上層に透明電極が形成されるアクテ

ィブマトリックス型有機EL表示体の製造方法において、前記有機発光層をその形状および配列が最終パターンとなるようインクジェット方式により形成することを特徴とするアクティブマトリックス型有機EL表示体の製造方法。

【請求項5】 前記インクジェット方式でポリマーまたはその前駆体を供給して、前記有機発光層を形成する請求項1ないし4のいずれかに記載のアクティブマトリックス型有機EL表示体の製造方法。

【請求項6】 シアノポリフェニレンビニレンにより、赤色の発光色を有する前記有機発光層を形成する請求項1ないし5のいずれかに記載のアクティブマトリックス型有機EL表示体の製造方法。

【請求項7】 ポリフェニレンビニレンにより、緑色の発光色を有する前記有機発光層を形成する請求項1ないし6のいずれかに記載のアクティブマトリックス型有機EL表示体の製造方法。

【請求項8】 ポリフェニレンビニレンおよびポリアルキルフェニレンにより、青色の発光色を有する前記有機発光層を形成する請求項1ないし7のいずれかに記載のアクティブマトリックス型有機EL表示体の製造方法。

【請求項9】 前記有機発光層をポリアルキルフルオレンで構成する請求項1ないし8のいずれかに記載のアクティブマトリックス型有機EL表示体の製造方法。

【手続補正2】

【補正対象書類名】明細書

【補正対象項目名】0009

【補正方法】変更

【補正内容】

【0009】

【課題を解決するための手段】本発明に関わるアクティブマトリックス型有機EL表示体の製造方法は、薄膜トランジスタを有するガラス基板に形成された透明画素電極上層に正孔注入層が形成され、この上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層（特にポリマーまたはその前駆体よりなる発光材料で構成された有機発光層）が形成され、更にこの上層に反射電極が形成されるアクティブマトリックス型有機EL表示体の製造方法において、前記有機発光層をそ

の形状および配列が最終パターンとなるようインクジェット方式により形成することを特徴とする。また、薄膜トランジスタを有するガラス基板に形成された透明画素電極上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層が形成され、更にこの上層に反射電極が形成されるアクティブマトリックス型有機EL表示体の製造方法において、前記有機発光層をその形状および配列が最終パターンとなるようインクジェット方式により形成することを特徴とする。

【手続補正3】

【補正対象書類名】明細書

【補正対象項目名】0010

【補正方法】変更

【補正内容】

【0010】更に、薄膜トランジスタを有するガラス基

板に形成された反射画素電極上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層が形成され、この上層に正孔注入層が形成され、更にこの上層に透明電極が形成されるアクティブマトリックス型有機EL表示体の製造方法において、前記有機発光層をその形状および配列が最終パターンとなるようインクジェット方式により形成することを特徴とし、また、薄膜トランジスタを有するガラス基板に形成された反射画素電極上層に少なくとも各画素毎に赤、緑、青より選択された発光色を有する有機発光層が形成され、更にこの上層に透明電極が形成されるアクティブマトリックス型有機EL表示体の製造方法において、前記有機発光層をその形状および配列が最終パターンとなるようインクジェット方式により形成することを特徴とする。

PATENT ABSTRACTS OF JAPAN

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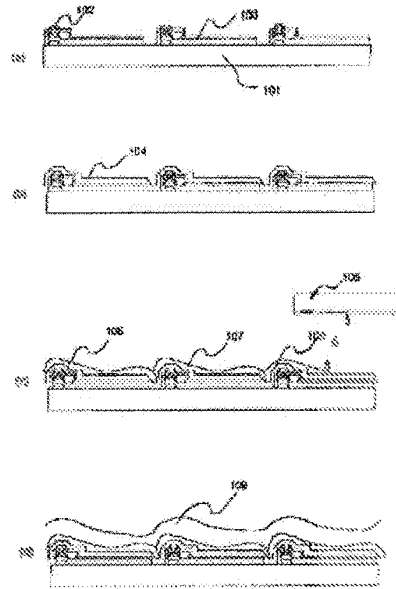
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(54) MANUFACTURE OF ACTIVE MATRIX TYPE ORGANIC EL DISPLAY BODY

(57)Abstract:

PROBLEM TO BE SOLVED: To manufacture an active matrix type organic EL display body at low cost by pattern-applying organic light emitting materials of red, green and blue on a base having a thin film transistor by means of ink jet.

SOLUTION: On a glass base 101, an ITO transparent picture element electrode 103 is formed after a thin film transistor 102 is formed thereon. A positive hole injection layer 104 of polyphenylene vinylene or the like is further formed thereon. This positive hole injection layer 104 is obtained by applying polytetrahydrothiophenyl phenylene of precursor followed by heating and polymerization. Organic light emitting layers 106-108 of red, green and blue are formed thereon every picture element. The organic light emitting layers are color-arranged and formed according to the pattern of each color every picture element by an ink jet printer 105. Further, A reflecting electrode 109 such as Mg, Ag or the like is formed thereon by evaporation.



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CLAIMS

[Claim(s)]

[Claim 1]A hole injection layer is formed in the transparent pixel electrode upper layer formed in a glass substrate which has a thin film transistor, In a manufacturing method of an active-matrix type organic electroluminescence display object with which an organic luminous layer which has the luminescent color besides chosen as a layer from red, green, and blue for every pixel at least is formed, and also a reflector is formed in this upper layer, A manufacturing method of an active-matrix type organic electroluminescence display object, wherein formation and arrangement of the aforementioned organic luminous layer are made by an ink jet system.

[Claim 2]In the transparent pixel electrode upper layer formed in a glass substrate which has a thin film transistor, for every pixel at least Red, In a manufacturing method of an active-matrix type organic electroluminescence display object with which an organic luminous layer which has the luminescent color chosen from green and blue is formed, and also a reflector is formed in this upper layer, A manufacturing method of an active-matrix type organic electroluminescence display object, wherein formation and arrangement of the aforementioned organic luminous layer are made by an ink jet system.

[Claim 3]In the reflection pixel electrode upper layer formed in a glass substrate which has a thin film transistor, for every pixel at least Red, In a manufacturing method of an active-matrix type organic electroluminescence display object with which an organic luminous layer which has the luminescent color chosen from green and blue is formed, and a hole injection layer is formed in this upper layer, and also a transparent electrode is formed in this upper layer, A manufacturing method of an active-matrix type organic electroluminescence display object, wherein formation and arrangement of the aforementioned organic luminous layer are made by an ink jet system.

[Claim 4]In the reflection pixel electrode upper layer formed in a glass substrate which has a thin film transistor, for every pixel at least Red, In a manufacturing method of an active-matrix type organic electroluminescence display object with which an organic luminous layer which has the luminescent color chosen from green and blue is formed, and also a transparent electrode is formed in this upper layer, A manufacturing method of an active-matrix type organic electroluminescence display object, wherein formation and arrangement of the aforementioned organic luminous layer are made by an ink jet system.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]This invention relates to the manufacturing method using the ink jet system of active-matrix type EL display object which used the thin film transistor.

[0002]

[Description of the Prior Art]An organic EL device has the composition which sandwiched the thin film containing a fluorescence organic compound by the anode and the cathode. It is an element which makes an exciton (exciton) generate and is made to emit light using discharge (fluorescence and phosphorescence) of the light at the time of this exciton being deactivated by making an electron and an electron hole (hole) pour in and recombine with the aforementioned thin film.

[0003]The feature of this organic EL device is 100 – 100000 cd/m² at the low voltage not more than 10V. It is that the high-intensity surface light of a grade is possible, and luminescence from blue to red is possible by choosing the kind of fluorescent substance.

[0004]The organic EL device attracts attention as what realizes an inexpensive large area full color display device (the Institute of Electronics, Information and Communication Engineers technical report, the 89th volume, NO.106, 49 pages, 1989). According to the report, the organic coloring matter which shows a strong fluorescence was used for the luminous layer, and blue, green, and bright red luminescence have been obtained. This shows a filmy and strong fluorescence, is having used organic coloring matter with few pin hole defects, and is considered that it has realized the high-intensity full color display.

[0005]The thin film layer which consists of a mixture of an organic electric charge material and an organic luminescent material is provided, in JP,H5-78655,A, the ingredient of an organic luminous layer prevents concentration quenching, and expands the range of choice of a luminescent material to it, and making it into a high-intensity full color element is proposed.

[0006]However, reference is made by neither of the reports about the composition and the manufacturing method of the actual full color display panel.

[0007]

[Problem to be solved by the invention]The organic thin film EL element using the above-mentioned organic coloring matter shows luminescence of blue, green, and red. However, in order to realize a full color display object as known well, it is necessary to arrange the organic luminous layer which emits light in the three primary colors for every pixel. Conventionally, technology which patterns an organic luminous layer was made very difficult. A cause is the point that the surface of metal of one of reflector material is unstable, and the patterning accuracy of vacuum evaporation does not come out. The 2nd is the point that polymer or the precursor which form a hole injection layer and an organic luminous layer do not have tolerance to pattern processes, such as photo lithography.

[0008]This invention solves problem which was mentioned above. The purpose is to provide a manufacturing method of an active-matrix type EL display object which patterned an organic luminous layer for every pixel with an ink jet system.

[0009]

[Means for solving problem]The manufacturing method of the active-matrix type organic electroluminescence display object in connection with this invention, A hole injection layer is formed in the transparent pixel electrode upper layer formed in the glass substrate which has a thin film transistor. In the manufacturing method of an active-matrix type organic electroluminescence display object with which the organic luminous layer which has the luminescent color besides chosen as the layer from red, green, and blue for every pixel at least is formed, and also a reflector is formed in this upper layer, It is characterized by making formation and arrangement of the aforementioned organic

luminous layer by an ink jet system, In the transparent pixel electrode upper layer formed in the glass substrate which has a thin film transistor, for every pixel at least Red, In the manufacturing method of an active-matrix type organic electroluminescence display object with which the organic luminous layer which has the luminescent color chosen from green and blue is formed, and also a reflector is formed in this upper layer, formation and arrangement of the aforementioned organic luminous layer are made by an ink jet system.

[0010]In the reflection pixel electrode upper layer formed in the glass substrate which has a thin film transistor, for every pixel at least Red, In the manufacturing method of an active-matrix type organic electroluminescence display object with which the organic luminous layer which has the luminescent color chosen from green and blue is formed, and a hole injection layer is formed in this upper layer, and also a transparent electrode is formed in this upper layer, It is characterized by making formation and arrangement of the aforementioned organic luminous layer by an ink jet system, In the reflection pixel electrode upper layer formed in the glass substrate which has a thin film transistor, for every pixel at least Red, In the manufacturing method of an active-matrix type organic electroluminescence display object with which the organic luminous layer which has the luminescent color chosen from green and blue is formed, and also a transparent electrode is formed in this upper layer, formation and arrangement of the aforementioned organic luminous layer are made by an ink jet system.

[0011]As shown in drawing 3 in short, on the signal wire 301 formed on the substrate, the gate line 302, the picture element electrode 303, and the thin film transistor 304, by the ink jet method, this invention is carrying out patterning spreading of red and the green and blue organic luminescent material, and realizes a full color display.

[0012]

[Mode for carrying out the invention]Hereafter, the suitable embodiment of this invention is described with reference to Drawings.

[0013](Working example 1) As shown in drawing 1, after forming the thin film transistor 102 on the glass substrate 101, the ITO transparent pixel electrode 103 is formed.

[0014]Polytetrahydro thiophenyl phenylene which is a polymer precursor as a hole injection material is coated. By heating, a precursor serves as polyphenylene vinylene and the 0.05-micron-thick hole injection layer 104 is formed.

[0015]Next, patterning spreading of the luminescent material which colors in red, green, and blue with the ink jet printing equipment 105 is carried out, and the 0.05-micron-thick layers colors 106, 107, and 108 are formed. Into red light material, polyphenylene vinylene and poly alkyl phenylene are used for polyphenylene vinylene and blue light material at cyano polyphenylene vinylene and green emission material. It is the Cambridge Display Technologies make, and such organic electroluminescence materials are liquefied and available.

[0016]Finally, the 0.1-0.2-micron-thick MgAg reflector 109 is formed with vacuum deposition.

[0017]Thereby, the full color organic electroluminescence display object of a direct viewing type is completed.

[0018](Working example 2) As shown in drawing 2, after forming the thin film transistor 202 on the glass substrate 201, the AlLi reflection pixel electrode 203 is formed.

[0019]Next, patterning spreading of the luminescent material which colors in red, green, and blue with the ink jet printing equipment 207 is carried out, and the layers colors 204, 205, and 206 are formed. Into red light material, polyphenylene vinylene and poly alkyl phenylene are used for polyphenylene vinylene and blue light material at cyano polyphenylene vinylene and green emission material. It is the Cambridge Display Technologies make, and such organic electroluminescence materials are liquefied and available.

[0020]Polytetrahydro thiophenyl phenylene which is a polymer precursor as a hole injection material is formed by the cast method. By heating, a precursor serves as polyphenylene vinylene and the hole injection layer 208 is formed.

[0021]Finally, the ITO transparent electrode 209 is formed with vacuum deposition.

[0022]Thereby, a reflection type full color organic electroluminescence display object is completed.

[0023](Working example 3) 2,3,6,7-tetrahydro 11-oxo 1 H,5 H,11H-(1) benzo PIRANO [6,7,8-] [ij]-kino lysine 10-carboxylic acid is used as an organic luminescent material of an organic luminous layer, It is considered as a green luminescent material by mixing both, using 1,1-bis-(4-N,N-ditolylamino phenyl) cyclohexane as an organic hole injection layer material.

[0024]Similarly, it mixes with hole injection layer material, using 2-13',4'-dihydroxyphenyl-3,5,7-trihydroxy 1-benzo pyrylium perchlorate as a red organic luminescent material.

[0025]In a blue light layer, using tris(8-hydroxyquinolinol) aluminum as an organic hole injection material as an organic luminescent material, 2,3,6,7-tetrahydro 9-methyl-11-oxo 1 H,5 H,11H-(1)

benzo PIRANO [6, 7, and 8--] [ii]-kino lysine is mixed, and a luminescent material is created.
[0026]At the same process as the working example 1 or the working example 2, partial patterning of each luminous layer is carried out with an ink jet printer apparatus, and an active-matrix type organic electroluminescence display object is created.

[0027]Besides the organic electroluminescence material used by this example, an aromatic diamine derivative (TDP), An oxydi azole dimer (OXD), an oxydi azole derivative (PBD), A JISUCHIRU arylene derivative (DSA), a quinolinol system metal complex, a beryllium benzo quinolinol complex (Bebq), A triphenylamine derivative (MTDATA), a distyryl derivative, a pyrazoline dimer, Although rubrene, Quinacridone, a triazole derivative, polyphenylene, a poly alkyl fluorene, polyalkylthio Foehn, an azomethine zinc complex, the Pori Phi Lynne zinc complex, a benzooxazol zinc complex, and a phenanthroline europium complex can be used, It is not a thing restricted to this.

[0028]

[Effect of the Invention]Patterning became possible in forming and arranging the organic electroluminescence material it was presupposed that patterning was impossible of material conventionally with an ink jet system, and the active-matrix type organic electroluminescence display object of the full color display was realized. Manufacture of the full color display object of a big screen is attained [that it is inexpensive and] by this, and an effect is size.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1]It is a figure showing the process of the active-matrix type organic electroluminescence display object in a 1st embodiment of this invention.

[Drawing 2]It is a figure showing the process of the active-matrix type organic electroluminescence display object in a 2nd embodiment of this invention.

[Drawing 3]It is a figure showing the layers color formed by the ink jet method on the thin film transistor of this invention.

[Explanations of letters or numerals]

101 Glass substrate

102 Thin film transistor

103 Transparent pixel electrode

104 Hole injection layer

105 Inkjet printer head

106 Organic luminous layer (the 1st color)

107 Organic luminous layer (the 2nd color)

108 Organic luminous layer (the 3rd color)

109 Reflector

201 Glass substrate

202 Thin film transistor

203 Reflection pixel electrode

204 Organic luminous layer (the 1st color)

205 Organic luminous layer (the 2nd color)

206 Organic luminous layer (the 3rd color)

207 Inkjet printer head

208 Hole injection layer

209 Transparent electrode

301 Signal wire

302 Gate line

303 Picture element electrode

304 Thin film transistor

305 Organic luminous layer (the 1st color)

306 Organic luminous layer (the 2nd color)

307 Organic luminous layer (the 3rd color)

[Translation done.]

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CORRECTION OR AMENDMENT

[Kind of official gazette]Printing of amendment by regulation of Patent Law Article 17 of 2

[Section Type] The 1st Type of the part VII gate

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B41J 3/04 101 Z

[Written Amendment]

[Filing date]Heisei 11(1999) October 29 (1999.10.29)

[Amendment 1]

[Document to be Amended]Description

[Item(s) to be Amended]Claims

[Method of Amendment]Change

[Proposed Amendment]

[Claim(s)]

[Claim 1]A hole injection layer is formed in the transparent pixel electrode upper layer formed in a glass substrate which has a thin film transistor. In a manufacturing method of an active-matrix type organic electroluminescence display object with which an organic luminous layer which has the luminescent color besides chosen as a layer from red, green, and blue for every pixel at least is formed, and also a reflector is formed in this upper layer. A manufacturing method of an active-matrix type organic electroluminescence display object, wherein formation and arrangement of the aforementioned organic luminous layer are made by an ink jet system.

[Claim 2]In the transparent pixel electrode upper layer formed in a glass substrate which has a thin film transistor, for every pixel at least Red. In a manufacturing method of an active-matrix type organic electroluminescence display object with which an organic luminous layer which has the luminescent color chosen from green and blue is formed, and also a reflector is formed in this upper layer. A manufacturing method of an active-matrix type organic electroluminescence display object, wherein formation and arrangement of the aforementioned organic luminous layer are made by an ink jet system.

[Claim 3]In the reflection pixel electrode upper layer formed in a glass substrate which has a thin film transistor, for every pixel at least Red. In a manufacturing method of an active-matrix type organic electroluminescence display object with which an organic luminous layer which has the luminescent color chosen from green and blue is formed, and a hole injection layer is formed in this upper layer, and also a transparent electrode is formed in this upper layer. A manufacturing method of an active-matrix type organic electroluminescence display object, wherein formation and arrangement of the aforementioned organic luminous layer are made by an ink jet system.

[Claim 4]In the reflection pixel electrode upper layer formed in a glass substrate which has a thin film

transistor, for every pixel at least Red. In a manufacturing method of an active-matrix type organic electroluminescence display object with which an organic luminous layer which has the luminescent color chosen from green and blue is formed, and also a transparent electrode is formed in this upper layer, A manufacturing method of an active-matrix type organic electroluminescence display object, wherein formation and arrangement of the aforementioned organic luminous layer are made by an ink jet system.

[Claim 5]A manufacturing method of the active-matrix type organic electroluminescence display object according to any one of claims 1 to 4 which supplies polymer or its precursor with the aforementioned ink jet system, and forms the aforementioned organic luminous layer.

[Claim 6]A manufacturing method of the active-matrix type organic electroluminescence display object according to any one of claims 1 to 5 which forms the aforementioned organic luminous layer which has the red luminescent color by cyano polyphenylene vinylene.

[Claim 7]A manufacturing method of the active-matrix type organic electroluminescence display object according to any one of claims 1 to 6 which forms the aforementioned organic luminous layer which has the green luminescent color by polyphenylene vinylene.

[Claim 8]A manufacturing method of the active-matrix type organic electroluminescence display object according to any one of claims 1 to 7 which forms the aforementioned organic luminous layer which has the blue luminescent color by polyphenylene vinylene and poly alkyl phenylene.

[Claim 9]A manufacturing method of the active-matrix type organic electroluminescence display object according to any one of claims 1 to 8 which constitutes the aforementioned organic luminous layer from a poly alkyl fluorene.

[Amendment 2]

[Document to be Amended]Description

[Item(s) to be Amended]0009

[Method of Amendment]Change

[Proposed Amendment]

[0009]

[Means for solving problem]The manufacturing method of the active-matrix type organic electroluminescence display object in connection with this invention, A hole injection layer is formed in the transparent pixel electrode upper layer formed in the glass substrate which has a thin film transistor, The organic luminous layer (organic luminous layer which comprised a luminescent material consisting of especially polymer or its precursor) which has the luminescent color besides chosen as the layer from red, green, and blue for every pixel at least is formed, In the manufacturing method of an active-matrix type organic electroluminescence display object with which a reflector is formed in this upper layer, formation and arrangement of the aforementioned organic luminous layer are made by an ink jet system. In the transparent pixel electrode upper layer formed in the glass substrate which has a thin film transistor, for every pixel at least Red, In the manufacturing method of an active-matrix type organic electroluminescence display object with which the organic luminous layer which has the luminescent color chosen from green and blue is formed, and also a reflector is formed in this upper layer, formation and arrangement of the aforementioned organic luminous layer are made by an ink jet system.

[Written Amendment]

[Filing date]Heisei 11(1999) November 25 (1999.11.25)

[Amendment 1]

[Document to be Amended]Description

[Item(s) to be Amended]Claims

[Method of Amendment]Change

[Proposed Amendment]

[Claim(s)]

[Claim 1]A hole injection layer is formed in the transparent pixel electrode upper layer formed in a glass substrate which has a thin film transistor, In a manufacturing method of an active-matrix type organic electroluminescence display object with which an organic luminous layer which has the luminescent color besides chosen as a layer from red, green, and blue for every pixel at least is formed, and also a reflector is formed in this upper layer, A manufacturing method of an active-matrix type organic electroluminescence display object forming the aforementioned organic luminous layer with an ink jet system so that the form and arrangement may serve as the last pattern.

[Claim 2]In the transparent pixel electrode upper layer formed in a glass substrate which has a thin film transistor, for every pixel at least Red, In a manufacturing method of an active-matrix type organic electroluminescence display object with which an organic luminous layer which has the

luminescent color chosen from green and blue is formed, and also a reflector is formed in this upper layer. A manufacturing method of an active-matrix type organic electroluminescence display object forming the aforementioned organic luminous layer with an ink jet system so that the form and arrangement may serve as the last pattern.

[Claim 3] In the reflection pixel electrode upper layer formed in a glass substrate which has a thin film transistor, for every pixel at least Red. In a manufacturing method of an active-matrix type organic electroluminescence display object with which an organic luminous layer which has the luminescent color chosen from green and blue is formed, and a hole injection layer is formed in this upper layer, and also a transparent electrode is formed in this upper layer. A manufacturing method of an active-matrix type organic electroluminescence display object forming the aforementioned organic luminous layer with an ink jet system so that the form and arrangement may serve as the last pattern.

[Claim 4] In the reflection pixel electrode upper layer formed in a glass substrate which has a thin film transistor, for every pixel at least Red. In a manufacturing method of an active-matrix type organic electroluminescence display object with which an organic luminous layer which has the luminescent color chosen from green and blue is formed, and also a transparent electrode is formed in this upper layer. A manufacturing method of an active-matrix type organic electroluminescence display object forming the aforementioned organic luminous layer with an ink jet system so that the form and arrangement may serve as the last pattern.

[Claim 5] A manufacturing method of the active-matrix type organic electroluminescence display object according to any one of claims 1 to 4 which supplies polymer or its precursor with the aforementioned ink jet system, and forms the aforementioned organic luminous layer.

[Claim 6] A manufacturing method of the active-matrix type organic electroluminescence display object according to any one of claims 1 to 5 which forms the aforementioned organic luminous layer which has the red luminescent color by cyano polyphenylene vinylene.

[Claim 7] A manufacturing method of the active-matrix type organic electroluminescence display object according to any one of claims 1 to 6 which forms the aforementioned organic luminous layer which has the green luminescent color by polyphenylene vinylene.

[Claim 8] A manufacturing method of the active-matrix type organic electroluminescence display object according to any one of claims 1 to 7 which forms the aforementioned organic luminous layer which has the blue luminescent color by polyphenylene vinylene and poly alkyl phenylene.

[Claim 9] A manufacturing method of the active-matrix type organic electroluminescence display object according to any one of claims 1 to 8 which constitutes the aforementioned organic luminous layer from a poly alkyl fluorene.

[Amendment 2]

[Document to be Amended] Description

[Item(s) to be Amended] 0009

[Method of Amendment] Change

[Proposed Amendment]

[0009]

[Means for solving problem] The manufacturing method of the active-matrix type organic electroluminescence display object in connection with this invention. A hole injection layer is formed in the transparent pixel electrode upper layer formed in the glass substrate which has a thin film transistor. The organic luminous layer (organic luminous layer which comprised a luminescent material consisting of especially polymer or its precursor) which has the luminescent color besides chosen as the layer from red, green, and blue for every pixel at least is formed. In the manufacturing method of an active-matrix type organic electroluminescence display object with which a reflector is formed in this upper layer, the aforementioned organic luminous layer is formed with an ink jet system so that that form and arrangement may serve as the last pattern. In the transparent pixel electrode upper layer formed in the glass substrate which has a thin film transistor, for every pixel at least Red. In the manufacturing method of an active-matrix type organic electroluminescence display object with which the organic luminous layer which has the luminescent color chosen from green and blue is formed, and also a reflector is formed in this upper layer. The aforementioned organic luminous layer is formed with an ink jet system so that the form and arrangement may serve as the last pattern.

[Amendment 3]

[Document to be Amended] Description

[Item(s) to be Amended] 0010

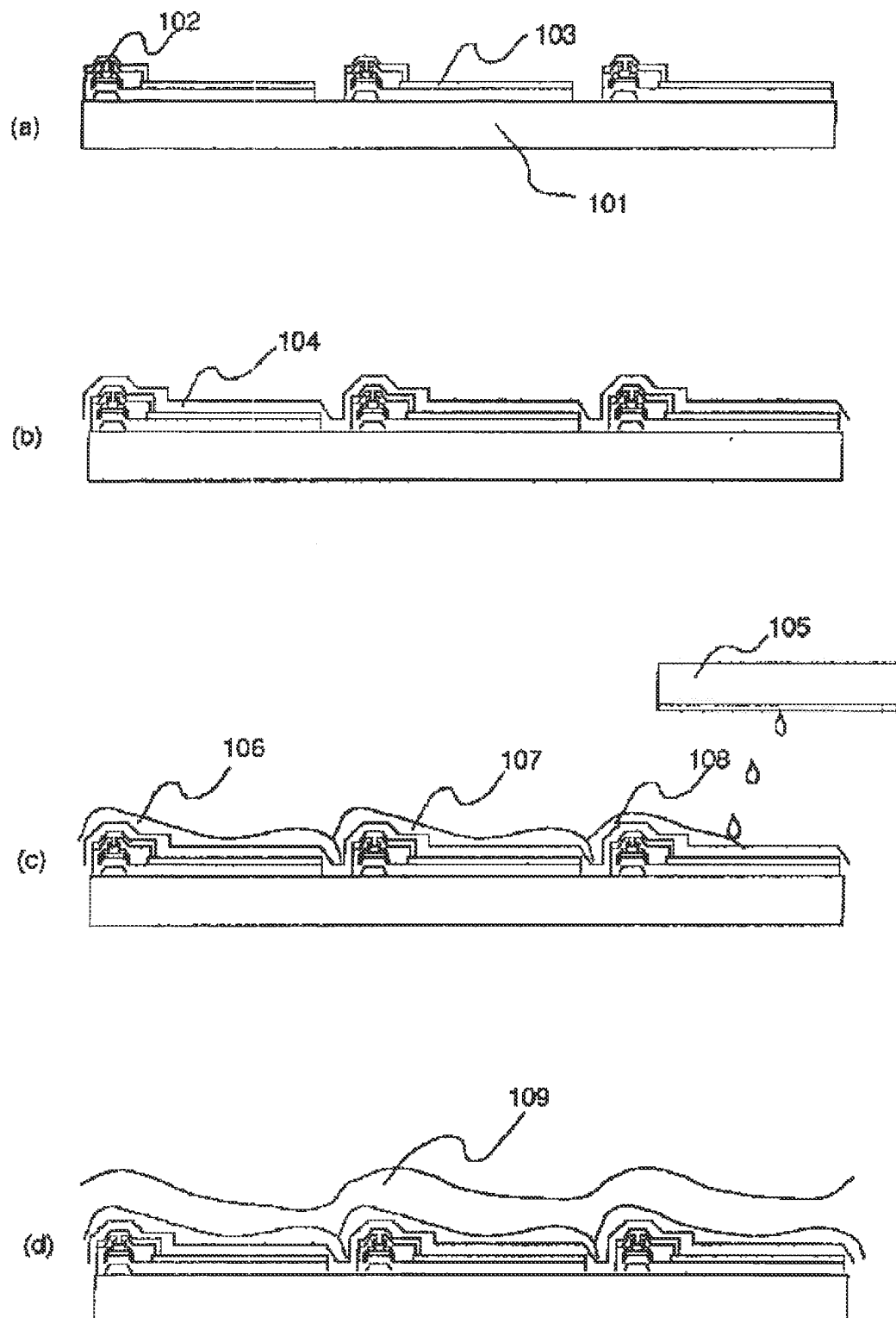
[Method of Amendment] Change

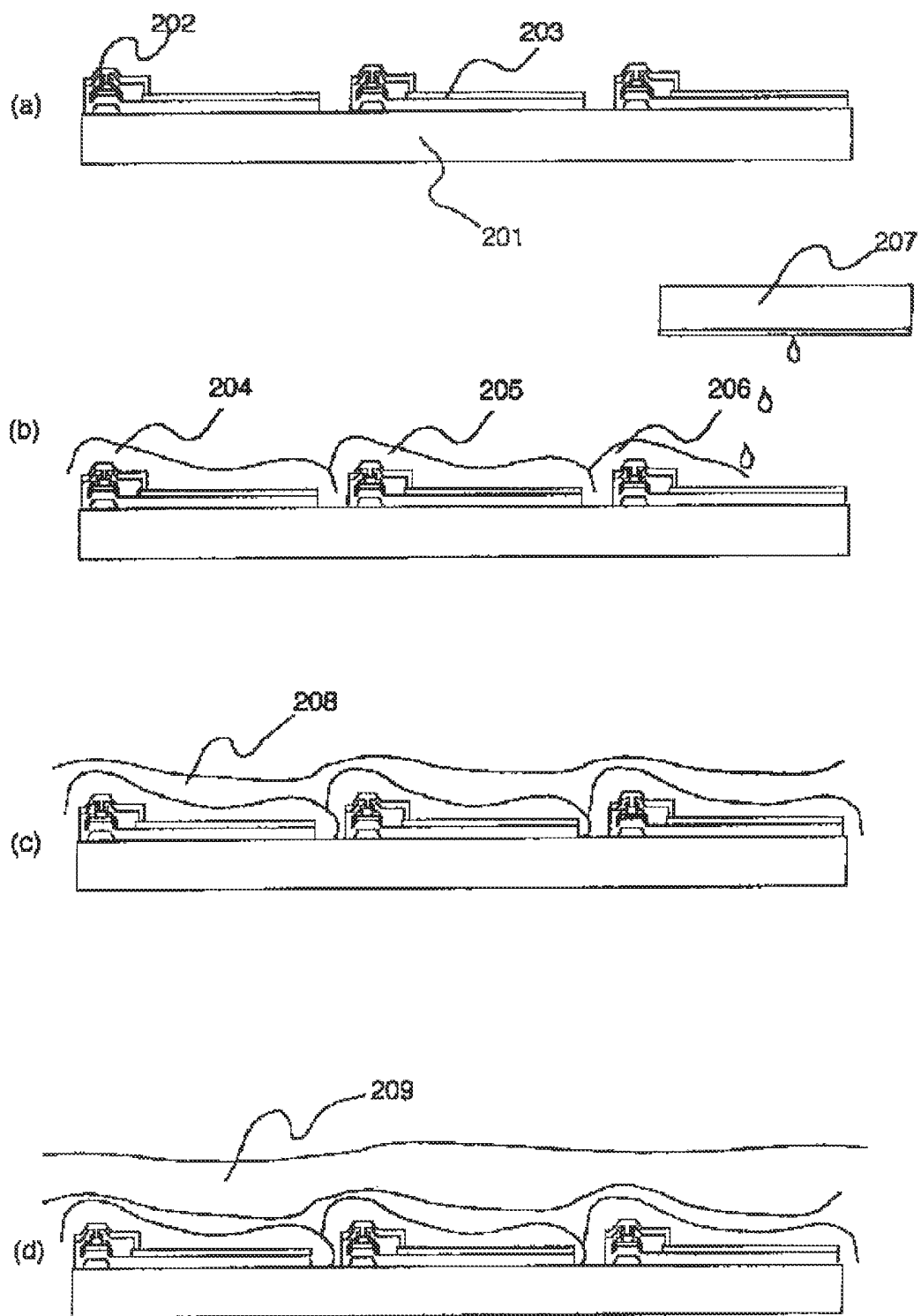
[Proposed Amendment]

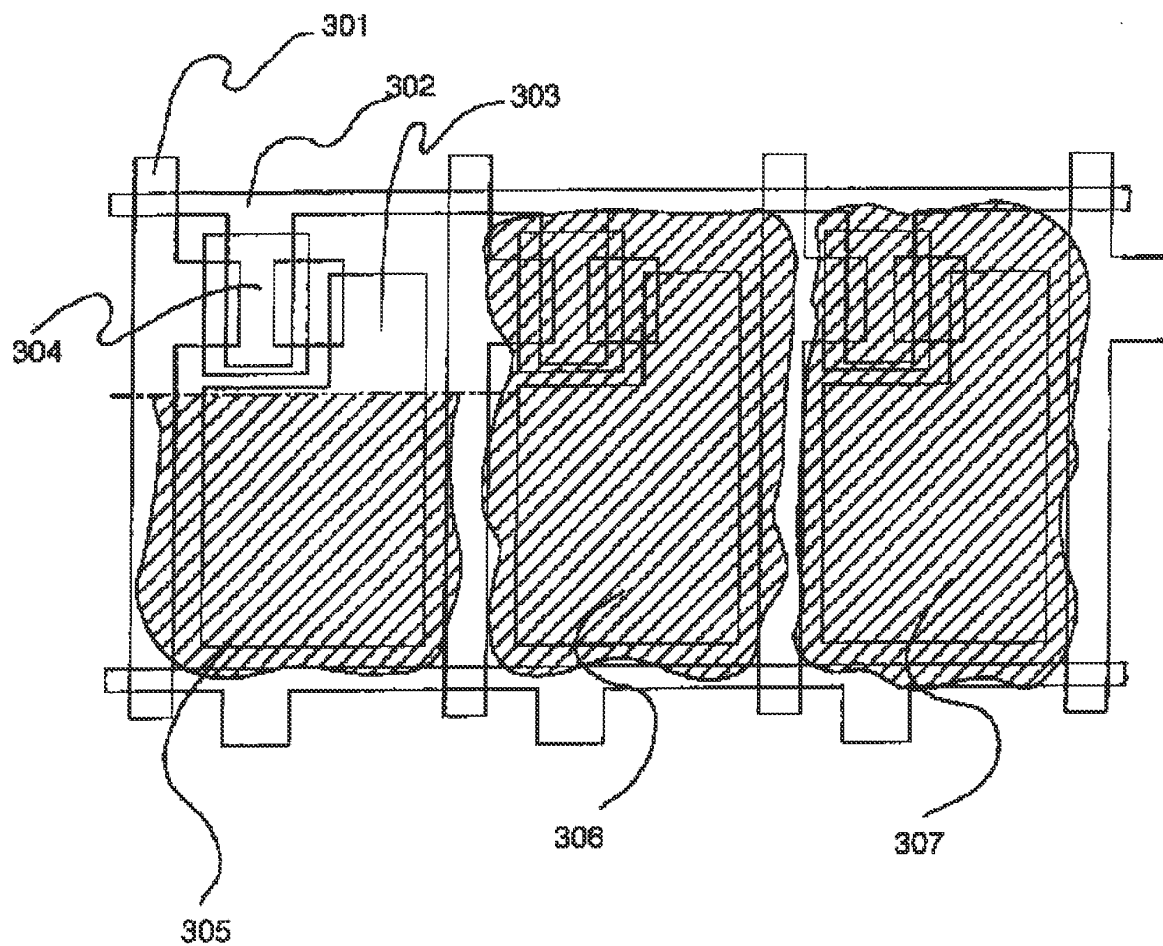
[0010] In the reflection pixel electrode upper layer formed in the glass substrate which has a thin film transistor, for every pixel at least Red. In the manufacturing method of an active-matrix type organic

electroluminescence display object with which the organic luminous layer which has the luminescent color chosen from green and blue is formed, and a hole injection layer is formed in this upper layer, and also a transparent electrode is formed in this upper layer, It is characterized by forming the aforementioned organic luminous layer with an ink jet system so that the form and arrangement may serve as the last pattern, In the reflection pixel electrode upper layer formed in the glass substrate which has a thin film transistor, for every pixel at least Red, In the manufacturing method of an active-matrix type organic electroluminescence display object with which the organic luminous layer which has the luminescent color chosen from green and blue is formed, and also a transparent electrode is formed in this upper layer, The aforementioned organic luminous layer is formed with an ink jet system so that the form and arrangement may serve as the last pattern.

[Translation done.]







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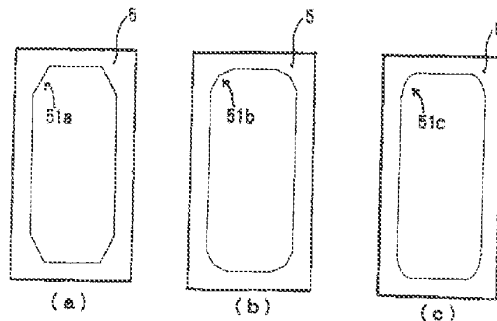
FA01

(54) 【発明の名称】 有機発光素子及びその製造方法

(57) 【要約】

【課題】 電極膜間の短絡を防止し、各画素の角部を含めた有機層全体が均一に発光する有機発光素子及びその製造方法を提供する。

【解決手段】 有機発光素子は、基板と、第1電極と、それぞれの画素の四周を囲む枠壁と、電極の上に形成された有機層と、有機層の上に形成された第2電極とを有し、有機層のうち少なくとも1層は、枠壁の内側に注入された有機材料を含む溶液または分散液が固化して形成され、枠壁は、注入された有機材料を含む溶液または分散液で枠壁内側の角部が充塞されるよう前記角部が角を取られてなる。



【特許請求の範囲】

【請求項1】 基板と、第1電極と、それぞれの画素の四周を囲む枠壁と、電極の上に形成された有機層と、有機層の上に形成された第2電極とを有する有機発光素子において、

有機層のうち少なくとも1層は、枠壁の内側に注入された有機材料を含む溶液または分散液が固化して形成され、枠壁は、注入された有機材料を含む溶液または分散液で枠壁内側の角部が充塞されるよう前記角部が角を取られてなることを特徴とする有機発光素子。

【請求項2】 有機層が、角を取られた枠壁内側の角部を充塞することにより枠壁の内側に密接して第2電極と第1電極の短絡を防止する請求項1に記載の有機発光素子。

【請求項3】 基板の表面に第1電極を縦横に列設し、それぞれの電極膜の四周を枠壁で囲み、電極膜の上に有機材料を含む溶液または分散液を注入して有機層を少なくとも1層形成し、次いで第2電極を形成する工程を有する有機発光素子の製造方法において、

枠壁は、その内側の角部が、有機材料を含む溶液または分散液によって充塞されるよう角を取られてなることを特徴とする有機発光素子の製造方法。

【請求項4】 枠壁の臨界面面張力が、枠壁の内側に注入する有機材料を含む溶液または分散液の表面張力よりも小さいことを特徴とする請求項3に記載の有機発光素子の製造方法。

【請求項5】 第1電極の臨界面面張力が、有機材料を含む溶液または分散液の表面張力よりも大きい請求項3または4に記載の有機発光素子の製造方法。

【請求項6】 枠壁を形成する際、基板の表面にレジスト膜を形成し、次いで、角取りがなされた角部を有する枠壁のフォトリソを用いて前記レジスト膜のエッチングを行い、角取りがなされた枠壁を得る請求項3から5のいずれか一つに記載の有機発光素子の製造方法。

【請求項7】 有機層が、有機材料を含む溶液または分散液からスピンコート法、インクジェット法およびノズル噴射法から選択されるいずれかの注入方法を用いて形成される請求項3から6のいずれか一つに記載の有機発光素子の製造方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、ディスプレイの画素として使用される有機発光素子及びその製造方法に関する。

【0002】

【従来の技術】従来、湿式法による有機LED素子の作製には、スピンコート法、ディップ法、ドクターブレード法等の塗布法が用いられていたが、これらの方法では、発光層のパターンニングによって画素をカラー化するのは困難であった。しかし、近年、この問題に対する一

つの解決法として、発光層を、インクジェット法によりパターン化して形成する方法が提案されている（特開平10-12377号公報、Appl. Phys. Lett. No. 72, 519頁, 1998年）。

【0003】また、透明基板上に形成された陽極をパターンニングして陽極群とした後に、前記陽極群にバンクを形成し、前記バンク間に電荷注入輸送層および／または発光層を液相にて形成し、その上に陰極を形成した構造の電界発光素子が開示されている（特開平11-87062号公報）。この電界発光素子では、バンクの構成材料の臨界面面張力 γ_c が、前記液相の表面張力 γ よりも小さいので、バンクが撥水・撥油性を有する。したがって、これらの層を形成する物質が画素間にまたがることのないので、画素間における漏電が防止される。また、発光層を形成する材料液をインクジェットヘッドを用いて吐出しても、これらの溶媒の表面張力 γ は、通常、30 dyne/cm以上でありバンクに対する濡れが小さいので、画素内に収まり、隣接する画素を汚染することがない。そのため、各画素の確実な発光により、鮮やかなカラー表示が可能となる。

【0004】

【発明が解決しようとする課題】しかし、バンクの構成材料の臨界面面張力 γ_c を、電荷注入輸送層および／または発光層を形成する液相の表面張力 γ よりも小さくすることにより、バンクで画素を囲った場合に、画素を区画するバンク内の角部まで発光層を形成する液が浸透せず、第1電極膜が剥き出しになる。よって、発光層を形成する液が固化して形成された有機層上に第2電極膜を形成した際、第1電極膜と第2電極膜との間で短絡が生じやすい。この問題を解決するには、有機層が形成されている部分のみに第2電極膜を形成する方法や、真空蒸着法等のドライプロセスで有機層を形成するプロセスと湿式法とを組み合わせる方法も可能であるが、これらの方法を用いた場合には、有機層の開口率が著しく低下する。

【0005】本発明は、上記の問題点に鑑みてなされたものであり、電極膜間の短絡を防止し、各画素の角部を含めた有機層全体が均一に発光する有機発光素子及びその製造方法を提供する。

【0006】

【課題を解決するための手段】この発明によれば、基板と、その表面に縦横に列設された第1電極（膜）と、それぞれの画素の四周を囲む枠壁と、電極膜の上に形成された有機層と、有機層の上に形成された第2電極膜群とを有する有機発光素子において、少なくとも1層の有機層は、枠壁の内側に注入された有機材料を含む溶液または分散液が固化して形成され、枠壁は、注入された有機材料を含む溶液または分散液で枠壁内側の角部が充塞されるよう前記角部が角を取られてなることを特徴とする有機発光素子が提供される。

【0007】すなわち、本発明者らは、有機層と枠壁の内側の角部との間に隙間を生じさせないために、枠壁内側の角部の形状について鋭意検討を行った。その結果、枠壁の内側の角部を取ることによって、有機材料を含む溶液または分散液（以下、「有機材料液」と略称する）を枠壁の内側に注入した際に、有機材料液が枠壁内側の角部を充塞し、有機材料液が固化した際に枠壁内側の角部との間に隙間のない有機層が形成される。したがって、第2電極膜が、枠壁と有機層との間の隙間に浸入して第1電極膜と短絡するのを防止することができる。さらに、優れた表示品質を有するとともに開口率の高い有機発光素子を湿式法により容易にかつ安価に製造することが可能となる。

【0008】この発明の別の観点によれば、基板の表面に第1電極膜群を縦横に列設し、それぞれの画素の四周を枠壁で囲み、電極膜の上に有機材料液を注入して少なくとも1層の有機層を形成し、次いで第2電極膜群を形成する工程を有する有機発光素子の製造方法において、枠壁は、その内側の角部が、有機材料液によって充塞されるよう角を取られてなることを特徴とする有機発光素子の製造方法が提供される。

【0009】この発明における臨界面張力とは、固体の表面における液体の「ヌレ」の度合を規定する「ジスマン（Zisman）の臨界面張力」を意味する。すなわち、低エネルギー表面をもつ大部分の有機高分子や有機化合物等の固体の表面上に、種々の表面張力をもつ極性の有機液体や飽和炭化水素、水等を滴下し、それらの接触角 θ を測定し、これらの $\cos \theta$ をそれぞれの液体の表面張力 γ [dyne/cm] に対してプロットし、得られた近似直線が接触角 $\theta = 0^\circ$ の水平線と交わる点の表面張力の値 γ_c [dyne/cm] が、この発明における臨界面張力となる。この発明における有機材料液の表面張力とは、液体が単位面積 [cm²] の表面をつくるための仕事 [erg] として表示される表面張力の値 γ [dyne/cm] を意味する。

【0010】枠壁の臨界面張力が、枠壁の内側に注入する有機材料液の表面張力よりも小さくなるように、有機材料液及び枠壁材質の双方を選択することにより、有機材料液を枠壁の内側に注入する際に、枠壁の内側壁面が有機材料液に対して撥水性または撥油性となるので、すなわち、有機材料液が枠壁の上部内側をぬらさないもので、有機材料液が枠壁を伝って隣接する画素にまたがることなく、画素間における短絡を防止できる。

【0011】また、隣接する画素の有機材料液による汚染が防止されるので、混色等の問題も回避でき、有機層全体を均一に発光させることができる。枠壁の内側壁面の20℃における臨界面張力と有機材料液の20℃における表面張力の差は、5 dyne/cm 以上であることが好ましい。この範囲にあれば、有機材料液の枠壁に対する付着力が小さいので、凸状のメニスカスを形成する。

【0012】他方、第1電極膜の臨界面張力が、有機材料液の表面張力よりも大きくなるよう第1電極膜および有機材料液の材質を選択することで、電極膜に対する有機材料液のヌレ性が向上し、枠壁の内側角部の下部隅部にまで有機材料液を満たすことができる。その結果、高開口率を有したままで、画素間および電極膜間の短絡を防止でき、かつ、極めて鮮やかなカラー表示が可能となる。第1電極膜の20℃における臨界面張力と有機材料液の20℃における表面張力の差は、5 dyne/cm 以上であることが好ましい。

【0013】この発明における画素とは、単色またはゾーンカラーのディスプレイの場合にはピクセルを意味し、マルチカラー、フルカラーディスプレイの場合にはサブピクセルを意味する。画素の形状は特に限定されないが、多角形状、円形状、楕円形状が例示される。画素の角部まで均一な膜を形成するためには、俯瞰したときに、画素の角部が中心に向かって凹状をなす円弧状のものが好ましい。

【0014】有機材料液を枠壁の内側へ注入する方法としては、スピコート法、インクジェットヘッドから有機材料液を吐出させるインクジェット法あるいはノズルまたはニードルから有機材料液を吐出させるノズル噴射法等、公知の方法を採用できる。

【0015】

【発明の実施の形態】以下、図1から図6を参照して、本発明の有機発光素子及びその製造方法の実施の形態を説明するが、これによって本発明は限定されない。

【0016】図1に、本発明の有機発光素子としての有機LED素子の基本的な構造を示す。図1において、有機LED素子10は、偏向板7、基板1、第1電極膜2、有機層3、第2電極膜4及び封止膜6が、この順に積層されてなり、枠壁5が有機層3の周囲を取り囲み、1つの画素（ピクセル）を形成する。有機層3は、有機材料液を注入した際の凸状のメニスカスが固化されて形成される。基板1としては、石英基板、ガラス基板、プラスチック基板等が使用される。

【0017】第1電極膜2及び第2電極膜4は、陽陰両極を形成する電極対であり、複数の有機LED素子10からなるディスプレイを形成したとき、基板1及び第1電極膜2が透明である場合は、有機層3からの発光が基板1側から出射されるので、発光効率を高めるためには、第2電極膜4が反射電極であること、あるいは第2電極膜4の有機層3と隣接しない側に反射膜を有することが好ましい。逆に、第2電極膜4を透明材料で構成して、有機層3からの発光を第2電極膜4側から出射させることもできる。この場合には、第1電極膜2が反射電極であること、基板1が反射基板であること、あるいは第1電極膜2と基板1との間に反射膜を有することが好ましい。

【0018】透明電極としては、CuI、ITO、Sn

O_2 、 ZnO 、 CuAlO_2 等の透明電極が使用される。また、反射電極としては、アルミニウム、カルシウム等の金属、マグネシウム-銀、リチウム-アルミニウム等の合金、マグネシウム/銀等の金属同士の積層膜、フッ化リチウム/アルミニウム等の絶縁体と金属との積層膜等が使用される。偏向板7は、ディスプレイにおける良好なコントラストを得るために基板1の外側に設けられる。封止膜6(または封止基板)は、第2電極膜4の損傷あるいは劣化を防止するために設けられる。

【0019】枠壁5は、その内側の角部が、後述する有機材料液によって充塞されるような角を取られてなり、有機材料液が枠壁5の内側の形状に従って固化し、有機層3を形成するので、画素は枠壁5の形状によって決定される。図2の(a)~(c)は、各画素を形成する枠壁5内側の角部51の形状の一例を示す(51a~51c)水平断面図である。角部51の形状としては、51a及び51bのように、1本または複数の直線で「角取り」されたものでもよいし、51cのように、中心に向かって凹状をなす曲線で「角取り」されたものでもよい。さらに、四隅の角部51の「角取り」を異なる大きさにしてもよいし、異なる形状にしてもよい。

【0020】枠壁5は、フォトリソグラフィにより作製することができる。この場合、所望の形状の角部51を有する枠壁5のフォトマスクを準備し、レジスト膜を形成した後、このフォトマスクを用いてエッチングを行い、所望の「角取り」がなされた枠壁5を形成することができる。枠壁5は、枠壁5の内側に注入される有機材料液の表面張力よりも小さい臨界面張力を有する材質からなり、有機材料液と枠壁5の内側との「濡れ」を抑えることによって、有機材料液の上面に凸状のメニスカスが形成されるような有機材料で形成される。したがって、枠壁5は、有機材料液の表面張力との関係でその材料が選択される。

【0021】枠壁5を形成するための好ましい材料を以下に列挙する。なお()内は、20℃における枠壁材料の臨界面張力の値 γ_c [dyne/cm]を示す。枠壁5の好ましい材料としては、例えば、パーフロオクチルエチルメタクリレート(15dyne/cm)、ポリ六フッ化プロピレン(16dyne/cm)、ポリ四フッ化エチレン(18dyne/cm)、ポリ三フッ化エチレン(22dyne/cm)、ポリジメチルシロキサン(24dyne/cm)、ポリフッ化ビニリデン(25dyne/cm)、ポリエチレン(31dyne/cm)、ポリスチレン(33dyne/cm)、旭硝子製サイトップ(商標)(19dyne/cm)等が挙げられる。また、ポジ型レジストをホストとして用い、信越化学製KBM7103(20dyne/cm)、7803(15dyne/cm)KP801M(8dyne/cm)をゲストとして混合したものも好ましい材料として挙げられる。

【0022】枠壁5は、少なくとも画素間の一部に形成されていればよく、枠壁5の構造は、単層構造であって

もよいし、薄膜を重畳してなる多層構造であってもよく、有機材料液の溶媒に対しては不溶もしくは難溶であることが好ましい。また、ディスプレイとしての表示品質を上げるために、ブラックマトリックス用の材料を用いることも好ましい。あるいは、これらの材料を用いて枠壁5を形成した後、プラズマ処理、UV処理、ガス処理等を行うことにより、枠壁5の表面の臨界面張力 γ_c の値を制御してもよい。

【0023】枠壁5は、上記のような材料を使用すること、あるいは上記のような処理を施すことにより、枠壁5の内側の壁面部分が構成されるが、より有効な凸状のメニスカスを形成するには、枠壁5の材料の臨界面張力 γ_c と、後述する有機層3となる有機材料液の表面張力 γ の差が、少なくとも5dyne/cm以上であることが好ましい。なお、枠壁5は、さらに、シャドウマスクを用いて第2電極膜4を形成した際に、シャドウマスクの密着による有機層3へのダメージを防止することができ、枠壁5の形状を適切な形、例えば、逆テーパ状とすることにより、シャドウマスクを用いなくても、第2電極膜4のパターニングが可能となる。

【0024】有機層3は、少なくとも一層の有機層を有する構造であって、有機層のみからなる単層構造、あるいは、電荷輸送層と有機層との多層構造であってもよい。また、必要に応じて、バフアー層を挿入してもよい。電荷輸送層と有機層との多層構造とする場合には、電荷輸送層及び有機層を各一層ずつとしてもよいし、上記の各層を複数ずつ用いてもよい。また、有機層3を、複数層の有機層からなる多層構造とする場合には、有機層の少なくとも一層が湿式法により形成されていることが必要である。このとき、他の有機層は湿式法により形成されていてもよいし、真空蒸着法等のドライプロセスにより形成されていてもよい。

【0025】有機層3は、塗液(有機材料液)の状態から薄膜を形成できる湿式法によるものであれば、材料は特に限定されない。湿式法としては、例えば、スピンコート法、ディップ法、ドクターブレード法、印刷法、電着法またはインクジェットヘッド、ノズルもしくはニードルから有機材料液を吐出する方法等、各種の薄膜形成方法があるが、インクジェットヘッド、ノズルまたはニードルから塗液を吐出する方法が特に好ましい。採用する方法によって適する材料(有機材料液)は若干異なるが、有機材料液の表面張力 γ は、枠壁5の臨界面張力 γ_c より大きく、さらには電極膜2及び電極膜4の臨界面張力 γ_c より小さいことが条件となる。

【0026】湿式法で用いられる有機材料液は、発光層形成用塗液と、電荷輸送層形成用塗液とに分けることができる。発光層形成用塗液としては、有機LED用の公知の高分子発光材料、例えば、ポリ[2-デシルオキシー-1,4-フェニレン](DO-PPP)、ポリ[2,5-ビス[2-(N,N-ネオトリエチルアンモニウ

ム)エトキシ]-1, 4-フェニレン-アルト-1, 4-フェニレン]ジプロマイド (PPP-NEt₃)、ポリ〔2-(2'-エチルヘキシルオキシ)-5-メトキシ-1, 4-フェニレンビニレン〕(MEH-PPV)、ポリ〔5-メトキシ-(2-プロパノキシサルフォニド)-1, 4-フェニレンビニレン〕(MPS-PPV)、ポリ〔2, 5-ビス(ヘキシルオキシ)-1, 4-フェニレン-(1-シアノビニレン)〕(CN-PPV)等を公知の溶媒に溶解あるいは分散させた塗液、もしくは、有機LED用の公知の低分子発光材料、例えば、テトラフェニルブタジエン(TPB)、クマリン、ナイルレッド、オキサジアゾール誘導体等と、公知の高分子材料、例えばポリカーボネート(PC)、ポリメタクリル酸メチル(PMMA)、ポリビニルカルバゾール(PVCz)等を公知の溶媒に溶解もしくは分散させた塗液を用いることができる。また、これらの塗液には、必要に応じてpH調整用、粘度調整用、浸透促進用、レベリング用等の添加剤、有機LED用及び有機光導電体用の公知のホール輸送材料(例えば、前記N, N'-ビス(3-メチルフェニル)-N, N'-ビス(フェニル)-ベンジジン(TPD)、N, N'-ジ(ナフタレン-1-イル)-N, N'-ジフェニル-ベンジジン(NPD)等)、電子輸送材料(例えば、3-(4-ビフェニルイル)-4-4'-フェニレン-5-tert-ブチルフェニル-1, 2, 4-トリアゾール(TAZ)、トリス(8-ヒドロキシキノリンナト)アルミニウム(Alq₃)等)等の電荷輸送材料、アクセプター、ドナー等のドーパント等を添加してもよい。

【0027】電荷輸送層形成用塗液としては、有機LED用、有機光導電体用の公知の高分子電荷輸送材料(例えば、ポリアニリン(PANI)、3, 4-エチレンジオキシチオフェン(PEDT)、ポリ〔トリフェニルアミン誘導体〕(Poly-TPD)、ポリ〔オキサジアゾール誘導体〕(Poly-OXZ等)、前記PVCz等を公知の溶媒に溶解もしくは分散させた塗液、もしくは、有機LED用、有機光導電体用の公知の低分子電荷輸送材料(例えば、前記のTPD、NPD、オキサジアゾール誘導体等)と公知の高分子材料(例えば、前記のPC、PMMA、PVCz等)を公知の溶媒に溶解もしくは分散させた塗液を用いることができる。また、これらの液に、必要に応じてpH調整用、粘度調整用、

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コールモノエチルエーテル、トリエチレングリコールモノメチルエーテル、トリエチレングリコールモノエチルエーテル、グリセリン、ホルムアミド、N-メチル-2-ピロリドン、シクロヘキサン、1-プロパノール、オクタン、ノナン、デカン等が含まれることが好ましい。発光層形成用塗液および電荷輸送層形成用塗液における固形分と溶媒の組成割合は、塗液の20℃における粘度が10mPa・s以下になるように調整することが好ましく、また、表面張力 γ を少なくとも40dyne/cmとなるように調整することが好ましい。

【0029】また、従来のドライプロセス、例えば、抵抗加熱蒸着法、EB蒸着法、イオンプレーティング法等で有機層3を電極膜2及び電極膜4の間に形成することもできる。ドライプロセスで使用できる有機材料としては、有機LED用の公知の発光材料が使用可能であり、有機層は有機材料のみから構成されてもよいし、添加剤等を含有していてもよい。また、電荷輸送材料としては、有機LED用、有機光導電体用の公知の材料が使用可能であり、電荷輸送層は、電荷輸送材料のみから構成されてもよいし、添加剤等を含有していてもよい。

【0030】次に、図3の平面図を参照しながら有機LED素子を複数配置して有機LEDディスプレイを形成するための有機層3の配置について説明する。有機層3には、赤色(R)発光素子11、緑色(G)発光素子12及び青色(B)発光素子13の3種類があり、本発明の有機LEDディスプレイ20は、これら3種類の有機層3を所定の配置パターンで、あるいはランダムパターンで、マトリックス状に配置して構成される。

【0031】図3(a)は、上記した各色の発光素子が枠壁5の短辺で隣接したストライプ状に配列されてなる「ストライプ配列」。図3(b)は、上記した各色の発光素子が枠壁5の角で隣接してモザイク状に配列されてなる「モザイク配列」。図3(c)は、有機層3(枠壁5)が蛇行し、かつ上記した各色の発光素子が千鳥状に配列されてなる「デルタ配列」。さらに、有機LEDディスプレイ20は、図3(d)に示すように、上記した各色の発光素子が規則的に配列されたもの(スクウェア配列)が例示される。これらの発光素子の配列において、赤色(R)発光素子11、緑色(G)発光素子12及び青色(B)発光素子13の配列数は、必ずしも、1:1:1の比でなくともよい。また、各画素の面積は、同一であってもよいし、各画素で異なってもよい。また、3種類(3色)でなく、1種類(1色)であってもよい。

【0032】上記の画素の形状は、枠壁作製時に枠壁を所望の形に形成することで形成可能であり、この枠壁の形成方法は、特に限定されないが、例えば、フォトリソグラフィ法により枠壁を形成する際に、露光条件、フォトマスクの形状、ベーク温度、ベーク時間等の条件を適切に制御して作製することが可能であり、また、所望

の枠壁の形状の溝が掘られた型を基板に密着させ、形成された空間に枠壁形成用の液状の原料を染み込ませ、充填した後に固定化させることで作製することも可能である。

【0033】次に、図4及び図5の平面図を参照しながら各画素に対応した第1電極膜2どうしと第2電極膜4どうしの接続方法について説明する。本発明の有機LEDディスプレイは、図4に示すように、有機層3を挟持する第1電極膜2と第2電極膜4が共通の基板1上で互いに直交する斜行ストライプ状の電極構成としてもよい。また、図5に示すように、第1電極膜2あるいは第2電極膜4が、所定のソースバスライン22及びゲートバスライン23で接続される薄膜トランジスタ21(TFT)を介して第2電極膜4あるいは第1電極膜2に接続していてもよい。

【0034】

【実施例】以下、実施の形態の具体例を示す。

実施例1

まず、130nmの膜厚をもつITO付きガラス基板1を、フォトリソグラフィ法により第1電極膜2として240μmピッチで200μm幅のITO透明ストライプ電極を作製する。次に、ITO付きガラス基板1を、例えばイソプロピルアルコール、アセトン、純水を用いた従来のウェットプロセスによる洗浄法及びUVオゾン処理、プラズマ処理等の従来のドライプロセスにより洗浄する。このとき、ITO表面の20℃における臨界面張力 γ_c は56dyne/cmであった。

【0035】次に、この基板1上に、20℃における臨界面張力 γ_c が20dyne/cmのポジ型レジストをスピンコート法により塗布し、膜厚30μmのレジスト膜を形成した。次に、露光用のマスクを用いて枠壁5を作製した。露光用のマスクは、枠壁5の内側の角部が、前述した図2(c)に示したように、その中心に向かって凹状をなす曲線からなる角部51cの形状のものを用いた。次いで、レジストの残渣を洗い流し、ITOと平行の方向には540μmピッチ、ITOと直行する方向には230μmピッチで、40μm幅の枠壁5を作製した。

【0036】次に、市販のスピンコーターにより、表面張力が20℃において43dyne/cmの3,4-ポリエチレンジオキシチオフェン水溶液を用い、厚さ50nmの正孔注入層を形成した。次に、市販のディスペンサーにより、赤、緑、青色に発光する発光材料をパターンニング塗布し、厚さ50nmの発光層を形成した。ここで、赤色発光材料としてシアノポリフェニレンピニレン前駆体、緑色発光材料としてポリフェニレンピニレン前駆体、青色発光材料としてポリパラフェニレンをそれぞれ使用した。このとき、すべての塗液の20℃における表面張力 γ は、48dyne/cmであった。ただし、シアノポリフェニレンピニレン前駆体とポリフェニレン

ピニレン前駆体に関しては、膜を形成後、Ar雰囲気下で150℃、6時間の加熱処理を行って、シアノポリフェニレンピニレンとポリフェニレンピニレンにそれぞれ変換した。なお、発光層の配置パターンは、図3(a)のストライプ配列を用いた。

【0037】次に、厚さ0.2μm、幅510μm、ピッチ540μmのシャドウマスクを用いて、AlとLiを共蒸着することにより、第2電極膜4としてのAlLi合金電極を形成した。最後にエポキシ樹脂を用いて封止を行った。以上のようにして作製した有機LEDディスプレイは、第1電極膜2と第2電極膜4との間、第1電極膜2どうし及び第2電極膜4どうしでの短絡は発生せず、また、発光層及び電荷輸送層の膜厚の不均一に伴う画素部のエッジからの不均一な発光は見られなかった。また、このディスプレイに30Vのパルス電圧を印加することで、すべての画素から均一な発光が得られた。

【0038】実施例2

有機材料液の吐出方法として、ディスペンサーの代わりに、市販のインクジェットプリンターを用いたこと以外は、実施例1と同様にして有機LEDディスプレイを作製した。インクジェットプリンターによる有機材料液の吐出は、図6に示すように、所定の配置パターンでマトリックス状に形成された枠壁5の間隔に対応して3つのインクジェットヘッド24を配置し、これらのインクジェットヘッド24から赤色(R)発光画素11、緑色(G)発光画素12及び青色(B)発光画素13を枠壁5の内側の第1電極2上に吐出させ、さらにこれらのインクジェットヘッド24を平行移動させて前記した発光画素の吐出を繰り返して発光層を形成した。

【0039】形成された有機LEDディスプレイは、第1電極膜2と第2電極膜4との間、第1電極膜2どうし及び第2電極膜4どうしでの短絡は発生せず、また、発光層及び電荷輸送層の膜厚の不均一に伴う画素部のエッジからの不均一な発光は見られなかった。また、このディスプレイに30Vのパルス電圧を印加することで、すべての画素から均一な発光が得られた。

【0040】実施例3

まず、ガラス基板1上に、薄膜トランジスタを形成した後、第1電極膜2として、長辺が500μmで、短辺が220μmとなるようにITO透明電極を形成した。このとき、ITO表面の20℃における臨界面張力 γ_c は56dyne/cmであった。

【0041】次に、この基板1上に、20℃における臨界面張力 γ_c が20dyne/cmのポジ型レジストを用いてスピンコート法により膜厚30μmのレジスト膜を形成した。次に、露光用のマスクを用いて枠壁5を作製した。露光用のマスクは、枠壁5の内側角部が、前述した図2(c)に示したように、その中心に向かって凸状をなす角部51cの形状のものを用いた。次いで、

レジストの残渣を洗い流し、ITOと平行の方向には540 μ mピッチ、ITOと直行する方向には230 μ mピッチで、40 μ m幅の枠壁5を作製した。次に、実施例2と同様にして有機体を形成した。次に、AlとLiを共蒸着することにより、第2電極膜4としてのAlLi合金電極を形成した。最後にエポキシ樹脂を用いて封止を行った。

【0042】形成された有機LEDディスプレイは、第1電極膜2と第2電極膜4との間、第1電極膜2どうし及び第2電極膜4どうしでの短絡は発生せず、また、発光層及び電荷輸送層の膜厚の不均一に伴う画素部のエッジからの不均一な発光は見られなかった。また、このディスプレイに30Vのパルス電圧を印加することで、すべての画素から均一な発光が得られた。

【0043】

【発明の効果】本発明では、枠壁の内側の角を取ることで、有機材料液を枠壁の内側に注入した際に、有機材料液が枠壁内側の角部を充塞し、有機材料液が固化した際に枠壁内側の角部との間に隙間のない有機層が形成される。したがって、第2電極膜が、枠壁と有機層との間の隙間に浸入して第1電極膜と短絡するのを防止することができる。

【0044】枠壁の臨界面張力が、枠壁の内側に注入する有機材料液の表面張力よりも小さくなるように、有機材料液及び枠壁材質の双方を選択することにより、有機材料液の上面に凸状のメニスカスが形成され、隣接する画素に有機材料液がまたがることなく枠壁の内側に収まり、有機層全体を均一に発光させることができる。さらに、第1電極膜の臨界面張力が、有機材料液の表面張力よりも大きくなるよう両者を選択することで、枠壁の内側角部の下部隅部にまで有機材料液を満たすことができる。その結果、高開口率を有したままで、画素間および電極膜間の短絡を防止でき、かつ極めて鮮やかなカラー表示が可能となる。

【0045】また、有機層の混じり合いによる混色、または有機層の混じり合いにより発光材料間に起こるエネルギー移動に伴うエネルギーの高い発光色の発光を抑え、表示品質の著しい低下を防止できる。さらに、シャドウマスクを用いて第2電極膜を形成した際に、シャドウマスクの密着による有機層へのダメージを防止するこ

とができる。この場合、枠壁の形状を適切な形、例えば、逆テーパー状とすることにより、シャドウマスクを用いなくても、第2電極膜のパターニングが可能となる。

【0046】したがって、この発明の製造方法により、電極膜間および画素間での短絡を防止し、かつ優れた表示品質を有するとともに開口率の高い有機発光素子を湿式法により容易にかつ安価に製造することが可能となる。

【図面の簡単な説明】

【図1】本発明による有機LEDディスプレイの拡大縦断面図。

【図2】図1の枠壁内側の角部の形状を説明する有機LEDディスプレイの水平断面図。

【図3】本発明による有機LEDディスプレイの発光層の配置例を示す概略部分平面図。

【図4】本発明による有機LEDディスプレイの電極膜の構成例を示す概略部分平面図。

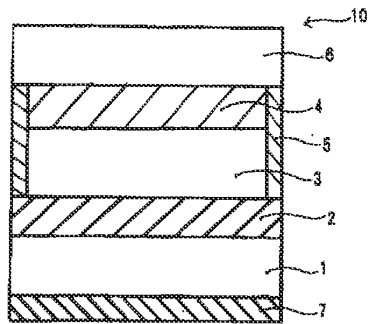
【図5】図4に対応する、本発明による有機LEDディスプレイの電極膜の他の構成例を示す概略部分平面図。

【図6】本発明の有機層の形成方法の一例を説明する概念図。

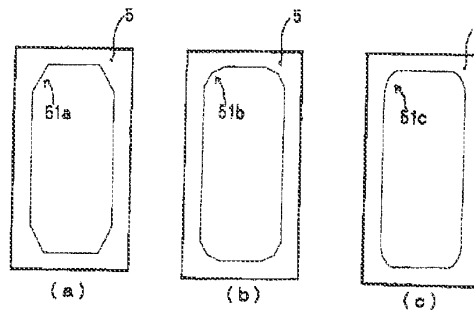
【符号の説明】

- 1 基板
- 2 第1電極膜
- 3 有機層
- 4 第2電極膜
- 5 枠壁
- 6 封止膜
- 7 偏向板
- 10 有機LED素子（有機発光素子）
- 11 赤色発光画素
- 12 緑色発光画素
- 13 青色発光画素
- 20 有機LEDディスプレイ
- 21 薄膜トランジスタ（TFT）
- 22 ソースバスライン
- 23 ゲートバスライン
- 24 インクジェットヘッド
- 40 51 角部

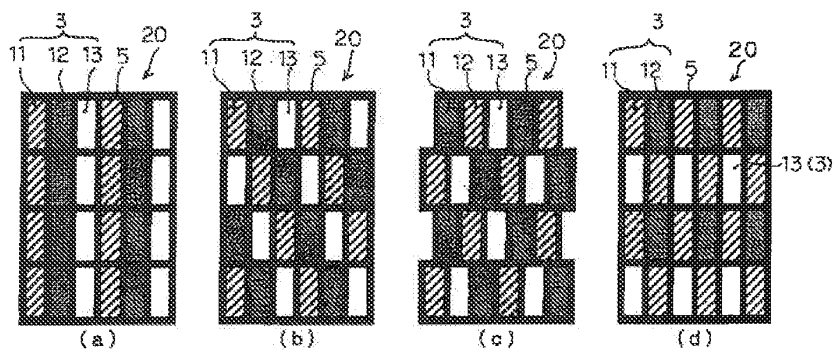
【図1】



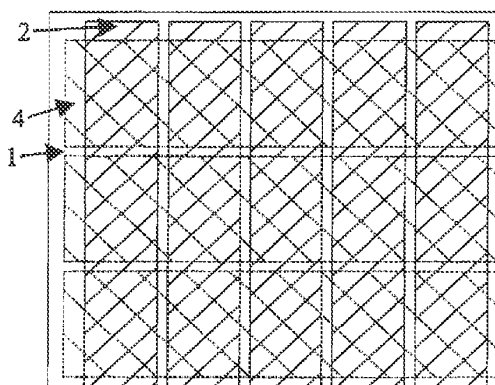
【図2】



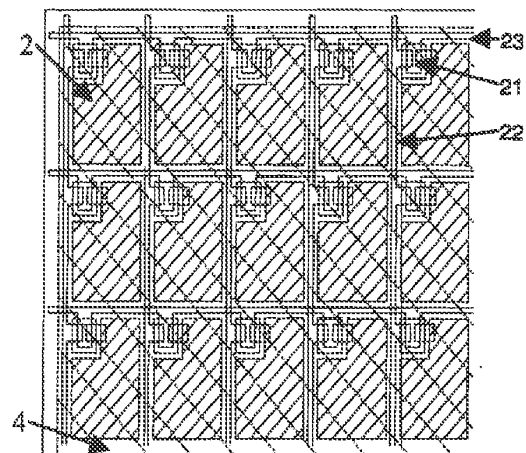
【図3】



【図4】



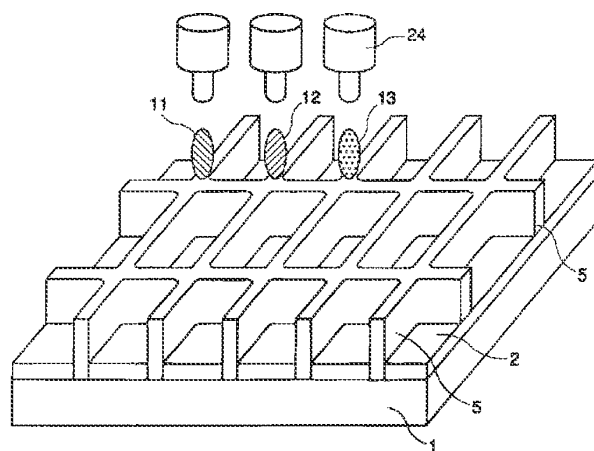
【図5】



(9)

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【図 6】



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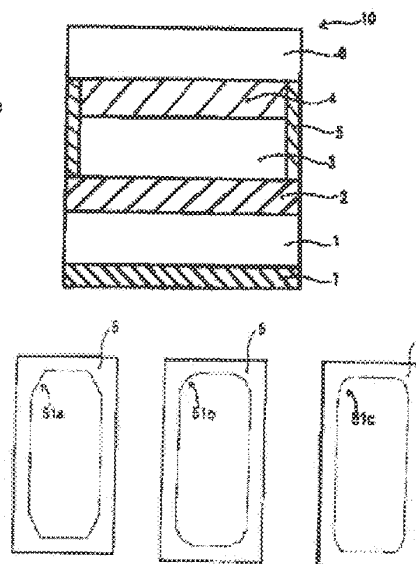
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(54) ORGANIC LIGHT EMITTING ELEMENT AND ITS MANUFACTURING METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To provide an organic light emitting element preventing a short circuit between electrode films and causing entire organic layers including the corners of each pixel to emit light uniformly, and a method for manufacturing it.

SOLUTION: This organic light emitting element has a substrate 1, a first electrode 2, a framing wall 5 surrounding the four sides of each pixel, organic layers 3 formed on the electrode, and a second electrode 4 formed on the organic layers. At least one of the electrode layers is formed by solidification of a solution or dispersion containing an organic material and injected inside the framing wall, and the inside corners of the framing wall are rounded so that the inside corners of the framing wall are filled with the injected solution or dispersion containing the organic material.



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CLAIMS

[Claim(s)]

[Claim 1]A substrate.

The 1st electrode.

A frame wall surrounding 4 rounds of each pixel.

An organic layer formed on an electrode.

The 2nd electrode formed on an organic layer.

In an organic light emitting element provided with the above,

An organic light emitting element which a solution or dispersion liquid containing an organic material poured in inside a frame wall solidifies, and at least one layer in an organic layer is formed, and is characterized by the aforementioned corner's having an angle taken and a frame wall becoming so that a corner of the frame wall inside may be full of a solution or dispersion liquid containing a poured-in organic material.

[Claim 2]The organic light emitting element according to claim 1 which is close inside a frame wall and prevents a short circuit of the 2nd electrode and the 1st electrode when an organic layer is filled with a corner of the frame wall inside which had an angle taken.

[Claim 3]Install the 1st electrodes successively in all directions on the surface of a substrate, and 4 rounds of each electrode layer are surrounded with a frame wall, In a manufacturing method of an organic light emitting element which it has, a process of pouring in a solution or dispersion liquid containing an organic material, carrying out an organic layer at least 1 stratification, and subsequently forming the 2nd electrode on an electrode layer a frame wall, A manufacturing method of an organic light emitting element, wherein an angle is taken and a corner of the inside becomes so that it may be full with a solution or dispersion liquid containing an organic material.

[Claim 4]A manufacturing method of the organic light emitting element according to claim 3, wherein critical surface tension of a frame wall is smaller than surface tension of a solution or dispersion liquid containing an organic material poured in inside a frame wall.

[Claim 5]A manufacturing method of the organic light emitting element according to claim 3 or 4 with larger critical surface tension of the 1st electrode than surface tension of a solution or dispersion liquid containing an organic material.

[Claim 6]A manufacturing method of an organic light emitting element of any one description of five from Claim 3 which acquires a frame wall which formed a resist film on the surface of a substrate, ranked second and etched the aforementioned resist film using a photo mask of a frame wall which has the corner by which chamfering was made, and in which chamfering was made when forming a frame wall.

[Claim 7]A manufacturing method of an organic light emitting element of any one description of six from Claim 3 formed using one which is chosen from a spin coat method, the ink jet method, and a nozzle spray method of injection methods from a solution or dispersion liquid in which an organic layer includes an organic material.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to an organic light emitting element used as a pixel of a display, and a manufacturing method for the same.

[0002]

[Description of the Prior Art] Although the applying methods, such as a spin coat method, a dip method, and a doctor blade method, were conventionally used for production of the organic LED device by wet process, it was difficult to colorize a pixel by patterning of a luminous layer in these methods. However, the method of patternizing a luminous layer by the ink jet method, and forming it as one solution over this problem, is proposed in recent years (JP, H10-12377, A, Appl. Phys. Lett. No. 72, 519 pages, and 1998 year).

[0003] After patterning the cathode formed on the transparent base and considering it as an anode group, the electroluminescence devices of the structure which formed the bank between the aforementioned cathodes, formed the electric charge pouring transporting bed and/or the luminous layer in the liquid phase between the aforementioned banks, and formed the anode on it are indicated (JP, H11-87062, A). In these electroluminescence devices, since critical-surface-tension γ_{cs} of the component of a bank is smaller than the surface tension γ of the aforementioned liquid phase, a bank has water and oil repellency. Therefore, since the substance which forms these layers does not straddle between pixels, fault current between pixels is prevented. Even if it breathes out the material liquids which form a luminous layer using an ink jet head, the surface tension γ of these solvents is 30 or more dyne/cm, and since γ_{cs} to a bank is small, it is settled in a pixel and it does not usually pollute the adjoining pixel. Therefore, a skillful colored presentation becomes possible by positive luminescence of each pixel.

[0004]

[Problem to be solved by the invention] However, by making critical-surface-tension γ_{cs} of the component of a bank smaller than the surface tension γ of the liquid phase which forms an electric charge pouring transporting bed and/or a luminous layer, when a pixel is enclosed on a bank, the liquid which forms a luminous layer to the corner within the bank which divides a pixel does not permeate, but the 1st electrode layer becomes unreserved. Therefore, when the liquid which forms a luminous layer forms the 2nd electrode layer on the organic layer solidified and formed, it is easy to produce a short circuit between the 1st electrode layer and the 2nd electrode layer. In order to solve this problem, the method of combining the method of forming the 2nd electrode layer, and the process of forming an organic layer by dry processes, such as a vacuum deposition method, and wet process only with the portion in which the organic layer is formed is also possible, but when these methods are used, the numerical aperture of an organic layer falls remarkably.

[0005] This invention is made in view of the above-mentioned problem, the short circuit between electrode layers is prevented, and the whole organic layer including the corner of each pixel provides an organic light emitting element which emits light uniformly, and a manufacturing method for the same.

[0006]

[Means for solving problem] In the organic light emitting element which has a substrate, the 1st electrode (film) installed in all directions successively by that surface, a frame wall surrounding 4 rounds of each pixel, the organic layer formed on the electrode layer, and the 2nd electrode layer group formed on the organic layer according to this invention, the solution or dispersion liquid containing the organic material poured in inside the frame wall solidifies the organic layer of at least one layer, it is formed, and an organic light emitting element, wherein the aforementioned corner has an angle taken and a frame wall becomes so that the corner of the frame wall inside may be full of

the solution or dispersion liquid containing the poured-in organic material is provided.

[0007] That is, since this invention persons did not produce a crevice between an organic layer and the corner inside a frame wall, they examined the form of the corner of the frame wall inside wholeheartedly. As a result, when the solution or dispersion liquid (it is hereafter called the "organic material liquid" for short) which includes an organic material by taking the angle inside a frame wall is poured in inside a frame wall, organic material liquid is filled with the corner of the frame wall inside, and when organic material liquid solidifies, an organic layer without a crevice is formed between the corners of the frame wall inside. Therefore, it can be prevented from the 2nd electrode layer infiltrating into the crevice between a frame wall and an organic layer, and connecting with the 1st electrode layer too hastily. While having the outstanding display quality, it becomes possible to manufacture easily and inexpensive an organic light emitting element with a high numerical aperture with wet process.

[0008] According to another viewpoint of this invention, the 1st electrode layer groups are installed successively in all directions on the surface of a substrate. In the manufacturing method of the organic light emitting element which has the process of surrounding 4 rounds of each pixel with a frame wall, pouring in organic material liquid on an electrode layer, forming the organic layer of at least one layer, and subsequently forming the 2nd electrode layer group. The manufacturing method of an organic light emitting element, wherein an angle is taken and a frame wall becomes so that the corner of the inside may be full with organic material liquid is provided.

[0009] The critical surface tension in this invention means "the critical surface tension of JISUMAN (Zisman)" which specifies the degree of "NURE" of the liquid in the solid surface. Namely, on the surface of solids, such as an organic high polymer of most with the low energy surface, and an organic compound, A polar organic liquid, saturated hydrocarbon, water with various surface tension, etc. are dropped, Value γ_{cm} of the surface tension of the point that the approximation straight lines obtained by measuring those angles of contact θ and plotting these $\cos\theta$ to the surface tension γ [dyne/cm] of each liquid cross the horizon which is $\theta = 0$ degree of angles of contact [dyne/cm] serves as critical surface tension in this invention. The surface tension of the organic material liquid in this invention means the value γ [dyne/cm] of the surface tension displayed as work [erg] for a liquid to build the surface of an unit area [cm^2].

[0010] So that the critical surface tension of a frame wall may become smaller than the surface tension of the organic material liquid poured in inside a frame wall. Since the paries-medialis-orbitae side of a frame wall serves as water repellence or oil repellency to organic material liquid when pouring in organic material liquid inside a frame wall by choosing the both sides of organic material liquid and frame wall construction material, That is, since organic material liquid does not soak the top inside of a frame wall, the pixel which organic material liquid is transmitted to a frame wall, and adjoins is not straddled, and the short circuit between pixels can be prevented.

[0011] Since contamination with the organic material liquid of the adjoining pixel is prevented, problems, such as mixed colors, can also be avoided and the whole organic layer can be made to emit light uniformly. As for the difference of the critical surface tension at 20 ** of the paries-medialis-orbitae side of a frame wall, and the surface tension at 20 ** of organic material liquid, it is preferred that they are 5 or more dyne/cm. Since the adhesion force to the frame wall of organic material liquid is small if it is in this range, a convex meniscus is formed.

[0012] On the other hand, the NURE nature of organic material liquid to an electrode layer can improve, and organic material liquid can be filled with choosing the construction material of the 1st electrode layer and organic material liquid so that the critical surface tension of the 1st electrode layer may become larger than the surface tension of organic material liquid even to the lower corner of the inside corner of a frame wall. As a result, with a high numerical aperture having, the short circuit between pixels and between electrode layers can be prevented, and a very skillful colored presentation becomes possible. As for the difference of the critical surface tension at 20 ** of the 1st electrode layer, and the surface tension at 20 ** of organic material liquid, it is preferred that they are 5 or more dyne/cm.

[0013] In the display of monochrome or a zone color, the pixel in this invention means a pixel, and, in the case of multicolor and a full color display, means subpixel. Although the form in particular of a pixel is not limited, polygonal shape, a circle configuration, and elliptical are illustrated. In order to form a film uniform to the corner of a pixel, when it looks down, the circular thing in which the corner of a pixel makes a concave toward a center is preferred.

[0014] As a method of pouring in organic material liquid to the inside of a frame wall, publicly known methods of making organic material liquid breathe out, such as a nozzle spray method, are employable from a spin coat method, the ink jet method make organic material liquid breathe out from an ink jet

head, a nozzle, or a needle.

[0015]

[Mode for carrying out the invention] Hereafter, this invention is not limited by this although the organic light emitting element of this invention and the embodiment of the manufacturing method are described with reference to drawing 6 from drawing 1.

[0016] A fundamental structure of the organic LED device as an organic light emitting element of this invention is shown in drawing 1. In drawing 1, this order comes to laminate the deflection plate 7, the substrate 1, the 1st electrode layer 2, the organic layer 3, the 2nd electrode layer 4, and the sealing film 6, the frame wall 5 encloses the circumference of the organic layer 3, and the organic LED device 10 forms one pixel (pixel). The convex meniscus at the time of pouring in organic material liquid is solidified, and the organic layer 3 is formed. As the substrate 1, a quartz substrate, a glass substrate, a plastic plate, etc. are used.

[0017] When the display which the 1st electrode layer 2 and the 2nd electrode layer 4 are electrode pairs which form positive-negative two poles, and consists of two or more organic LED devices 10 is formed, Since luminescence from the organic layer 3 is emitted from the substrate 1 side when the substrate 1 and the 1st electrode layer 2 are transparent, in order to raise luminous efficiency, it is preferred to have a reflecting film in the side which does not adjoin the organic layer 3 of that the 2nd electrode layer 4 is a reflector or the 2nd electrode layer 4. On the contrary, the 2nd electrode layer 4 can be constituted from a transparent material, and luminescence from the organic layer 3 can also be made to emit from the 2nd electrode layer 4 side. In this case, it is preferred that the 1st electrode layer 2 is a reflector, that the substrate 1 is a reflective substrate, or to have a reflecting film between the 1st electrode layer 2 and the substrate 1.

[0018] As a transparent electrode, transparent electrodes, such as CuI, ITO, SnO₂, ZnO, and CuAlO₂, are used. As a reflector, the cascade screen of metal, such as alloys, such as metal, such as aluminum and calcium, magnesium silver, and lithium aluminum, magnesium/silver, the cascade screen of insulators, such as lithium fluoride/aluminum, and metal, etc. are used. The deflection plate 7 is formed in the outside of the substrate 1, in order to acquire the good contrast in a display. The sealing film 6 (or sealing substrate) is formed in order to prevent damage or degradation of the 2nd electrode layer 4.

[0019] Since an angle is taken, the corner of the inside becomes so that it may be full with the organic material liquid mentioned later, organic material liquid solidifies the frame wall 5 according to the form inside the frame wall 5 and the organic layer 3 is formed, a pixel is determined by the form of the frame wall 5. (a) - (c) of drawing 2 is a horizontal sectional view showing an example of the form of the corner 51 of the frame wall 5 inside which forms each pixel (51a-51c). As form of the corner 51, like 51a and 51b, "chamfering" could be carried out in 1 or two or more straight lines, and "chamfering" could be carried out like 51c with the curve which makes a concave toward a center. "Chamfering" of the corner 51 of four corners may be made into a different size, and it may be made different form.

[0020] The frame wall 5 is producible by a photolithography. In this case, after preparing the photo mask of the frame wall 5 which has the corner 51 of desired form and forming a resist film, it can etch using this photo mask and the frame wall 5 in which desired "chamfering" was made can be formed. The frame wall 5 consists of construction material which has critical surface tension smaller than the surface tension of the organic material liquid poured in inside the frame wall 5, and is formed with the organic material that a convex meniscus is formed in the upper surface of organic material liquid, by stopping "NURE" organic material liquid and inside the frame wall 5. Therefore, as for the frame wall 5, the material is chosen by a relation with the surface tension of organic material liquid.

[0021] The desirable materials for forming the frame wall 5 are enumerated below. Value γ_{cm} of the critical surface tension of frame wall material [in / in the inside of () / 20 **] [dyne/cm] is shown. As a desirable material of the frame wall 5, for example Perphloro octylethylmethacrylate (15 dyne/cm), Polypropylene hexafluoride (16 dyne/cm), polytetrafluoroethylene (18 dyne/cm), Polyethylene trifluoride (22 dyne/cm), polydimethylsiloxane (24 dynes/(cm)), Polyvinylidene fluoride (25 dyne/cm), polyethylene (31 dyne/cm), polystyrene (33 dyne/cm), Asahi Glass SAITOPPU [trademark] (19 dyne/cm), etc. are mentioned. What mixed KBM7103 made from the Shin-etsu chemistry (20 dyne/cm) and 7803(15 dynes/(cm)) KP801M (8 dynes/(cm)) as a guest is mentioned as a desirable material, using a positive resist as a host.

[0022] The frame wall 5 should just be formed in the part between pixels at least, it may be layer structure, and may be the multilayer structure which superimposes a thin film, and, as for the structure of the frame wall 5, it is preferred that it is insoluble or refractory to the solvent of organic material liquid. In order to raise the display quality as a display, it is also preferred to use the material

for black matrices. Or after forming the frame wall 5 using such materials, the value of critical-surface-tension γ_{mac} of the surface of the frame wall 5 may be controlled by performing plasma treatment, UV processing, gassing, etc.

[0023] Although the wall surface portion inside the frame wall 5 is constituted using the above materials or by performing the above processings, the frame wall 5, in order to form a more effective convex meniscus, it is preferred that the difference of critical-surface-tension γ_{mac} of the material of the frame wall 5 and the surface tension γ of the organic material liquid used as the organic layer 3 mentioned later is at least 5 or more dyne/cm. When the frame wall 5 forms the 2nd electrode layer 4 further using a shadow mask, the damage to the organic layer 3 by adhesion of a shadow mask can be prevented, and even if it does not use a shadow mask by making form of the frame wall 5 into a suitable form, for example, reverse tapered shape, patterning of the 2nd electrode layer 4 is attained.

[0024] The organic layer 3 may be the structure of having an organic layer of at least one layer, and may be the layer structure which consists only of organic layers, or the multilayer structure of a charge transport layer and an organic layer. A buffer layer may be inserted if needed. When considering it as the multilayer structure of a charge transport layer and an organic layer, it is good also considering a charge transport layer and an organic layer as every one layer each, and two or more above-mentioned each layers may be used every. To make the organic layer 3 into the multilayer structure which consists of an organic layer of two or more layers, it is required to form at least one layer of an organic layer by wet process. At this time, other organic layers may be formed by wet process, and may be formed of dry processes, such as a vacuum deposition method.

[0025] If the organic layer 3 is based on the wet process which can form a thin film from the state of coating liquid (organic material liquid), material in particular will not be limited. Although there are various kinds of methods for forming thin film, such as the method of carrying out the regurgitation of the organic material liquid from a spin coat method, a dip method, a doctor blade method, print processes, an electrodeposition process or an ink jet head, a nozzle, or a needle, as wet process, for example, Especially the method of carrying out the regurgitation of the coating liquid from an ink jet head, a nozzle, or a needle is preferred. Although the materials (organic material liquid) which are suitable by the method of adopting differ a little, it becomes conditions that the surface tension γ of organic material liquid is larger than critical-surface-tension γ_{mac} of the frame wall 5, and it is still smaller than critical-surface-tension γ_{mac} of the electrode layer 2 and the electrode layer 4.

[0026] The organic material liquid used with wet process can be divided into the coating liquid for luminous layer formation, and the coating liquid for charge transport layer formation. A high polymer luminescent material publicly known [for organic LED] as coating liquid for luminous layer formation, For example, the poly [2-decyloxy 1,4-phenylene] (DO-PPP). Poly[2,5-screw [2-(N,N,N-triethyl ammonium) ethoxy]-1,4-phenylene-alto 1,4-phenylene] dibromide (PPP-NEt₃⁺). The poly [2-(2'-ethylhexyloxy)-5-methoxy- 1, the 4-phenylenevinylene] (MEH-PPV). The poly [5-methoxy-(2-pro PANOKI sisal FONIDO)-1,4-phenylenevinylene] (MPS-PPV). the coating liquid which made the publicly known solvent dissolve or distribute poly[2,5-bis(hexyloxy)-1,4-phenylene-(1-cyanovinylene)] (CN-PPV) etc. — or, The publicly known low molecule luminescent material for organic LED, for example, tetraphenylbutadiene, (TPB), a coumarin, the Nile red, an oxadiazole derivative, etc., The coating liquid which made the publicly known solvent dissolve or distribute a publicly known polymer material (PC), for example, polycarbonate, poly methyl methacrylate (PMMA), a polyvinyl carbazole (PVCz), etc. can be used. To these coating liquid, if needed The object for pH adjustments, the object for viscosity control, for osmosis promotion, The additive agents for leveling etc., the object for organic LED, and the publicly known hole carrying material for organic photo conductors. for example, the aforementioned N,N'-bis-(3-methylphenyl)-N,N'-bis-(phenyl)-benzidine (TPD) — N,N'-JI (naphthalene-1-yl)-N,N'-diphenyl-benzidine (NPD) etc., an electron transport material (for example, 3-(4-biphenyl) 4-4-phenylene-5-t-buthylphenyl 1,2,4-triazole (TAZ) —) tris (8-hydroxy kino RINONATO) aluminum (Alq₃) etc. — etc. — dopants, such as a charge transporting material, an acceptor, and a donor, etc. may be added.

[0027] A polymer charge transporting material publicly known [for organic LED and for organic photo conductors] as coating liquid for charge transport layer formation. for example, poly aniline (PANI) and 3,4-polyethylene dioxythiophene (PEDT) — The poly [triphenylamine derivative] (Poly-TPD) poly [oxadiazole derivative] (Poly-OXZ etc.). the coating liquid which made the publicly known solvent dissolve or distribute the aforementioned PVCz etc. — or, The coating liquid which made the publicly known solvent dissolve or distribute the object for organic LED, the publicly known low molecule charge transporting materials for organic photo conductors (for example, above TPD, NPD, an

oxadiazole derivative, etc.), and publicly known polymer materials (for example, the aforementioned PC, PMMA, PVCz, etc.) can be used. Dopants, such as additive agents the object for pH adjustments, the object for viscosity control, the object for fullness promotion, the object for leveling, for surface tension adjustment, etc., an acceptor, and a donor, etc. may be added in these liquid if needed.

[0028]When using the ink jet method, can use the conventional solvent by using the aforementioned polymer material as the solvent dissolved or distributed, but. The solvent of low steam pressure [inside / of these solvents], for example, ethylene glycol, Propylene glycol, triethylene glycol, ethylene glycol monomethyl ether, Ethylene glycol monoethyl ether, triethylene glycol monomethyl ether, It is preferred that triethylene glycol monoethyl ether, glycerin, a formamide, N-methyl-2-pyrrolidone, cyclohexane, 1-propanol, octane, nonane, Deccan, etc. are included. As for the presentation rate of solid content and a solvent in the coating liquid for luminous layer formation, and the coating liquid for charge transport layer formation, adjusting is preferred so that the viscosity at 20 °C of coating liquid may be 10 or less mPa·s, and it is preferred to adjust the surface tension gamma so that it may become at least 40 dyne/cm.

[0029]The organic layer 3 can also be formed between the electrode layer 2 and the electrode layer 4 by the conventional dry process, for example, resistance heating vacuum deposition, EB vacuum deposition, the ion plating method, etc. As an organic material which can be used by a dry process, the publicly known luminescent material for organic LED is usable, and an organic layer may comprise only an organic material and may contain the additive agent etc. As a charge transporting material, the object for organic LED and a publicly known material for organic photo conductors are usable, and a charge transport layer may comprise only a charge transporting material, and may contain the additive agent etc.

[0030]Next, arrangement of the organic layer 3 for arranging two or more organic LED devices, and forming an organic LED display is explained, referring to the top view of drawing 3. There are three kinds of the organic layers 3, the red (R) emission pixel 11, the green (G) emission pixel 12, and the blue (B) emission pixel 13, and the organic LED display 20 of this invention. It is a predetermined arrangement pattern, or these three kinds of organic layers 3 are arranged to matrix form, and it constitutes them from a random pattern.

[0031]The stripe shape which the emission pixel of each above-mentioned color adjoined by the shorter side of the frame wall 5 comes to arrange drawing 3 (a) [stripe arrangement]. The emission pixel of each above-mentioned color adjoins on the square of the frame wall 5, and mosaic shape comes to arrange drawing 3 (b) [a mosaic array]. It comes alternately to arrange the emission pixel of each color which the organic layer 3 (frame wall 5) moved in a zigzag direction, and described drawing 3 (c) above [a delta array]. As the organic LED display 20 is shown in drawing 3 (d), that [Square arrangement] by which the emission pixel of each above-mentioned color was arranged regularly is illustrated. As for the number of arrangement of the red (R) emission pixel 11, the green (G) emission pixel 12, and the blue (B) emission pixel 13, in the arrangement of these emission pixels, it is not necessarily good to be no match for 1:1:1. The area of each pixel may be the same and may differ by each pixel. It may be not three kinds (3 colors) but one kind (1 color).

[0032]Can form the form of the above-mentioned pixel by forming in the form of a request of a frame wall at the time of frame wall production, and the formation method of this frame wall, Although not limited in particular, when forming a frame wall with the photolithographic method, for example, It is possible to control appropriately conditions, such as an exposing condition, form of a photo mask, baking temperature, and bake time, and to produce them, It is also possible to produce by making it fix, after the slot of the form of a desired frame wall sticks the **** type, ditches, to a substrate, infiltrates the liquefied raw material for frame wall formation into formed space and is filled up.

[0033]Next, the connection method of 1st electrode layer 2 corresponding to each pixel and 2nd electrode layer 4 is explained, referring to the top view of drawing 4 and drawing 5. The organic LED display of this invention has good 1st electrode layer 2 and 2nd electrode layer 4 which pinch the organic layer 3 also as an electrode configuration of the bias stripe shape which intersects perpendicularly mutually on the common substrate 1, as shown in drawing 4. As shown in drawing 5, the 1st electrode layer 2 or the 2nd electrode layer 4 may connect with the 2nd electrode layer 4 or the 1st electrode layer 2 via the thin film transistor 21 (TFT) connected by the predetermined source bus line 22 and the gate bus line 23.

[0034]

[Working example]Hereafter, the example of an embodiment is shown.

the working example 1 --- the ITO transparent stripe electrode of 200-micrometer width is first produced for the glass substrate 1 with ITO with 130-nm thickness in a 240-micrometer pitch as the 1st electrode layer 2 with photolithography method. Next, the conventional dry processes, such as a

cleaning method by the conventional wet process using isopropyl alcohol, acetone, and pure water and UV ozonization, and plasma treatment, wash the glass substrate 1 with ITO, for example. At this time, critical-surface-tension γ_{mac} at 20 °C on the surface of ITO was 56 dyne/cm.

[0035]Next, on this substrate 1, critical-surface-tension γ_{mac} at 20 °C applied the positive resist of 20 dyne/cm with the spin coat method, and formed the resist film of 30 micrometers of thickness. Next, the frame wall 5 was produced using the mask for exposure. As shown in drawing 2 (c) which the corner inside the frame wall 5 mentioned above, the thing of the form of the corner 51c which consists of a curve which makes a concave toward the center was used for the mask for exposure. Subsequently, the residue of the resist was flushed and the frame wall 5 of 40-micrometer width was produced in a 230-micrometer pitch in the direction which goes in the direction parallel to ITO direct with a 540-micrometer pitch and ITO.

[0036]Next, surface tension formed the 50-nm-thick hole injection layer by the commercial spin coater using 43 dynes/cm 3,4-polyethylene dioxythiophene solution in 20 °C. Next, with the commercial dispenser, patterning spreading of red and the luminescent material that emits light green and blue was carried out, and the 50-nm-thick luminous layer was formed. Here, poly para-phenylene was used as a polyphenylene vinylene precursor and a blue light material as a cyano polyphenylene vinylene precursor and a green emission material as a red light material, respectively. At this time, the surface tension γ at 20 °C of all the coating liquid was 48 dyne/cm. However, about the cyano polyphenylene vinylene precursor and the polyphenylene vinylene precursor, 150 °C and heat-treatment for 6 hours were performed under Ar atmosphere after forming a film, and it changed into cyano polyphenylene vinylene and polyphenylene vinylene, respectively. The stripe arrangement of drawing 3 (a) was used for the arrangement pattern of a luminous layer.

[0037]Next, the AlLi alloy electrode as the 2nd electrode layer 4 was formed by carrying out vapor codeposition of aluminum and the Li using the 0.2-micrometer [in thickness], 510-micrometer [in width], and pitch 540micrometer shadow mask. Finally the epoxy resin was used and sealing was performed. the organic LED display produced as mentioned above --- between the 1st electrode layer 2 and the 2nd electrode layer 4 and the 1st electrode layer 2 --- doing what --- and the 2nd electrode layer 4 --- the short circuit which does what and comes out was not generated, and uneven luminescence from the edge of the picture element part accompanying the unevenness of the thickness of a luminous layer and a charge transport layer was not seen. Uniform luminescence was obtained from all the pixels by impressing the pulse voltage of 30V to this display.

[0038]As a discharging method of working-example 2 organic-material liquid, the organic LED display was produced like the working example 1 instead of the dispenser except having used the commercial ink jet printer. The regurgitation of the organic material liquid by an ink jet printer, As shown in drawing 6, corresponding to the interval of the frame wall 5 formed in matrix form, the three ink jet heads 24 are arranged with a predetermined arrangement pattern, The red (R) emission pixel 11, the green (G) emission pixel 12, and the blue (B) emission pixel 13 are made to breathe out on the 1st electrode 2 inside the frame wall 5 from these ink jet heads 24. The regurgitation of the emission pixel which carried out parallel translation of these ink jet heads 24, and furthermore described them above was repeated, and the luminous layer was formed.

[0039]the formed organic LED display --- between the 1st electrode layer 2 and the 2nd electrode layer 4 and the 1st electrode layer 2 --- doing what --- and the 2nd electrode layer 4 --- the short circuit which does what and comes out was not generated, and uneven luminescence from the edge of the picture element part accompanying the unevenness of the thickness of a luminous layer and a charge transport layer was not seen. Uniform luminescence was obtained from all the pixels by impressing the pulse voltage of 30V to this display.

[0040]the working example 3 --- first, after forming a thin film transistor on the glass substrate 1, the long side formed the ITO transparent electrode at 500 micrometers as the 1st electrode layer 2, so that a shorter side might be set to 220 micrometers. At this time, critical-surface-tension γ_{mac} at 20 °C on the surface of ITO was 56 dyne/cm.

[0041]Next, critical-surface-tension γ_{mac} at 20 °C formed the resist film of 30 micrometers of thickness with the spin coat method on this substrate 1 using the positive resist of 20 dyne/cm. Next, the frame wall 5 was produced using the mask for exposure. As shown in drawing 2 (c) which the inside corner of the frame wall 5 mentioned above, the thing of the form of the corner 51c which makes convex toward the center was used for the mask for exposure. Subsequently, the residue of the resist was flushed and the frame wall 5 of 40-micrometer width was produced in a 230-micrometer pitch in the direction which goes in the direction parallel to ITO direct with a 540-micrometer pitch and ITO. Next, the organism was formed like the working example 2. Next, the AlLi alloy electrode as the 2nd electrode layer 4 was formed by carrying out vapor codeposition of

aluminum and the Li. Finally the epoxy resin was used and sealing was performed.

[0042]the formed organic LED display — between the 1st electrode layer 2 and the 2nd electrode layer 4 and the 1st electrode layer 2 — doing what — and the 2nd electrode layer 4 — the short circuit which does what and comes out was not generated, and uneven luminescence from the edge of the picture element part accompanying the unevenness of the thickness of a luminous layer and a charge transport layer was not seen. Uniform luminescence was obtained from all the pixels by impressing the pulse voltage of 30V to this display.

[0043]

[Effect of the Invention]In this invention, when organic material liquid is poured in inside a frame wall by taking the angle inside a frame wall, organic material liquid is filled with the corner of the frame wall inside, and when organic material liquid solidifies, an organic layer without a crevice is formed between the corners of the frame wall inside. Therefore, it can be prevented from the 2nd electrode layer infiltrating into the crevice between a frame wall and an organic layer, and connecting with the 1st electrode layer too hastily.

[0044]So that the critical surface tension of a frame wall may become smaller than the surface tension of the organic material liquid poured in inside a frame wall. A convex meniscus can be formed in the upper surface of organic material liquid, and it can be settled inside a frame wall, without organic material liquid straddling the adjoining pixel, and the whole organic layer can be made to emit light uniformly by choosing the both sides of organic material liquid and frame wall construction material. Organic material liquid can be filled with choosing both so that the critical surface tension of the 1st electrode layer may become larger than the surface tension of organic material liquid even to the lower corner of the inside corner of a frame wall. As a result, with a high numerical aperture having, the short circuit between pixels and between electrode layers can be prevented, and a very skillful colored presentation becomes possible.

[0045]the mixed colors depended to mix an organic layer or an organic layer — being mixed — luminescence of the luminescent color with high energy accompanying the energy transfer which happens between luminescent materials is suppressed, and remarkable deterioration of display quality can be prevented. When the 2nd electrode layer is formed using a shadow mask, the damage to the organic layer by adhesion of a shadow mask can be prevented. In this case, even if it does not use a shadow mask by making form of a frame wall into a suitable form, for example, reverse tapered shape, patterning of the 2nd electrode layer is attained.

[0046]Therefore, while having the display quality which prevented the short circuit between electrode layers and between pixels, and was excellent with the manufacturing method of this invention, it becomes possible to manufacture easily and inexpensive an organic light emitting element with a high numerical aperture with wet process.

[Translation done.]

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2.*** shows the word which can not be translated.

3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1]The enlarged vertical longitudinal sectional view of the organic LED display by this invention.

[Drawing 2]The horizontal sectional view explaining the form of the corner inside [frame wall] drawing 1 of an organic LED display.

[Drawing 3]The outline part plan showing the example of arrangement of the luminous layer of the organic LED display by this invention.

[Drawing 4]The outline part plan showing the example of composition of the electrode layer of the organic LED display by this invention.

[Drawing 5]The outline part plan showing other examples of composition of the electrode layer of the organic LED display by this invention corresponding to drawing 4.

[Drawing 6]The key map explaining an example of the formation method of the organic layer of this invention.

[Explanations of letters or numerals]

1 Substrate

2 The 1st electrode layer

3 Organic layer

4 The 2nd electrode layer

5 Frame wall

6 Sealing film

7 Deflection plate

10 Organic LED device (organic light emitting element)

11 Red light pixel

12 Green emission pixel

13 Blue light pixel

20 Organic LED display

21 Thin film transistor (TFT)

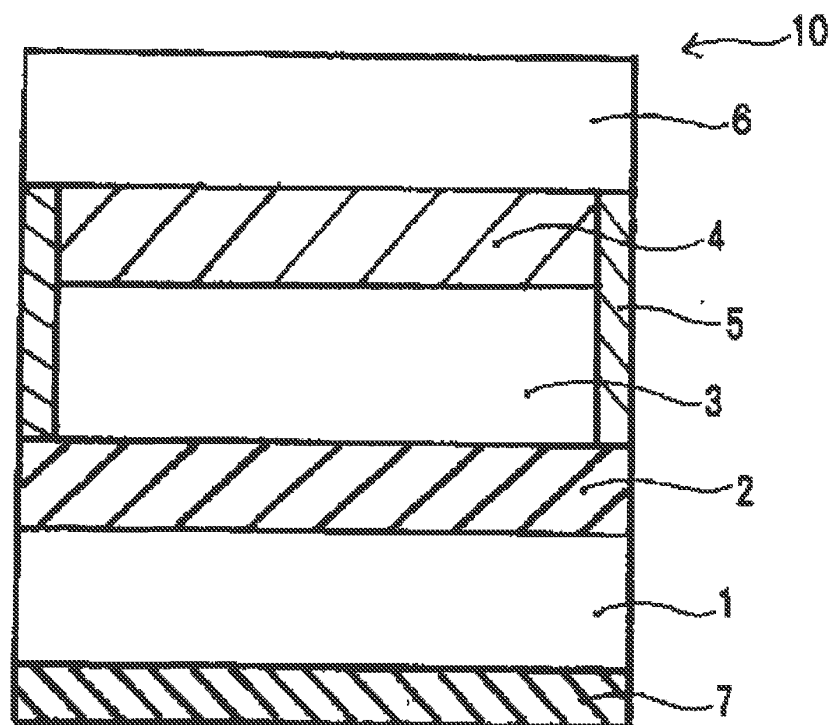
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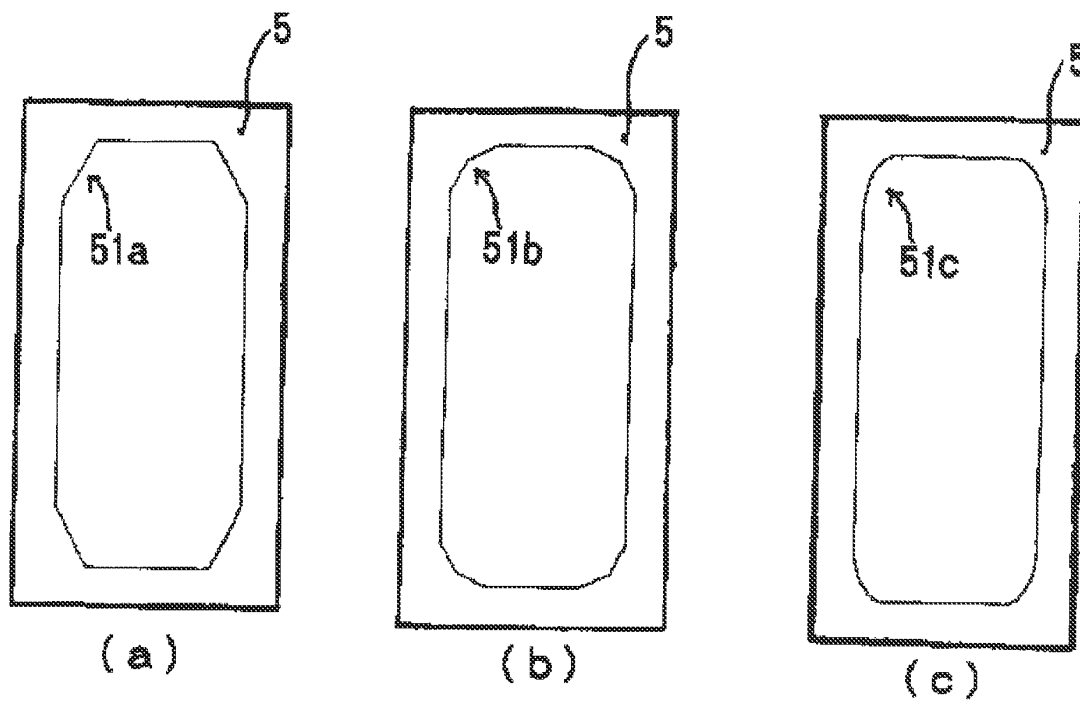
23 Gate bus line

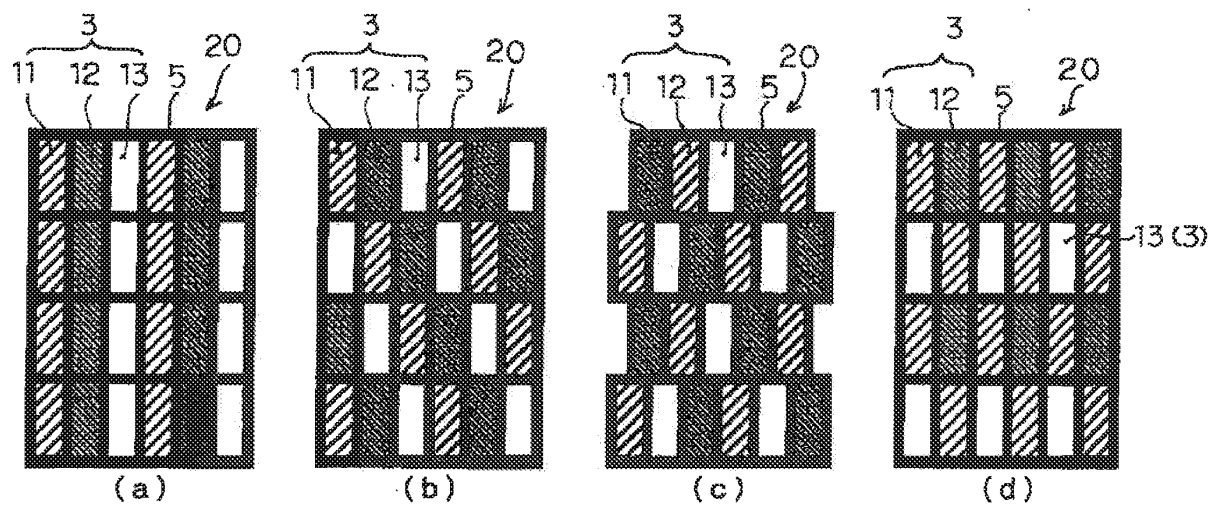
24 Ink jet head

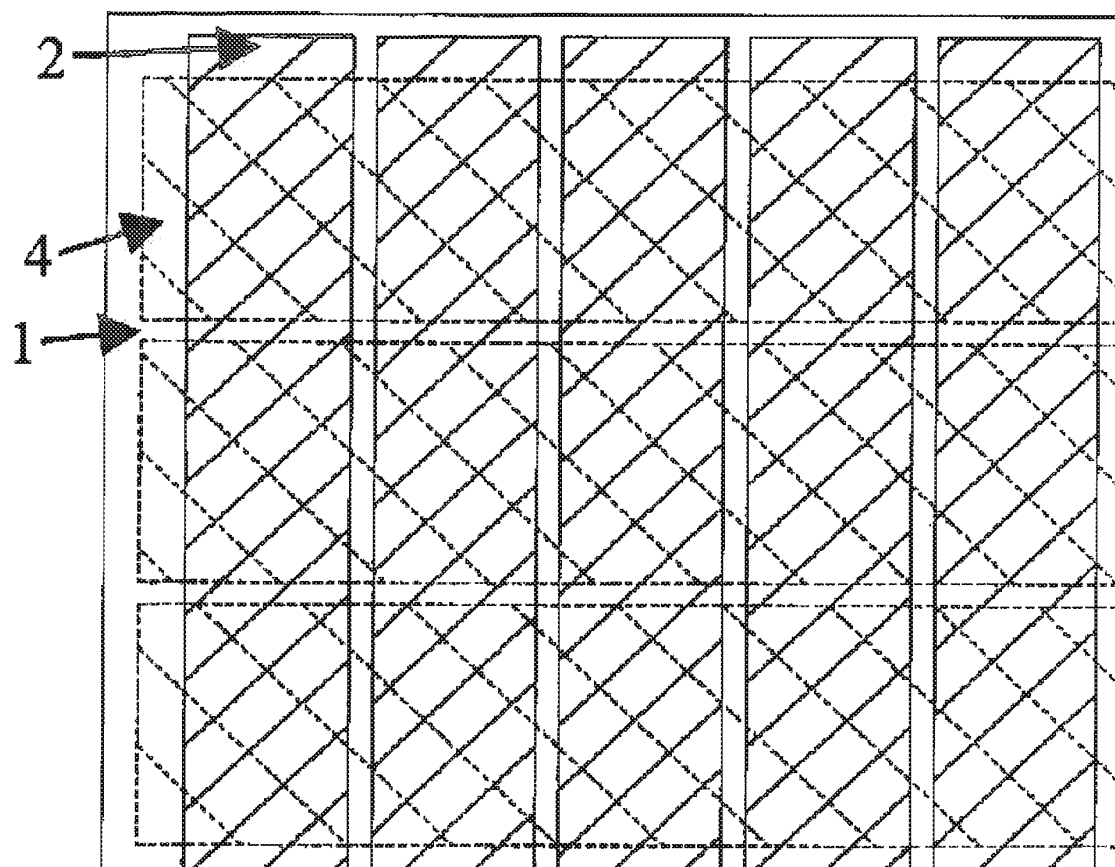
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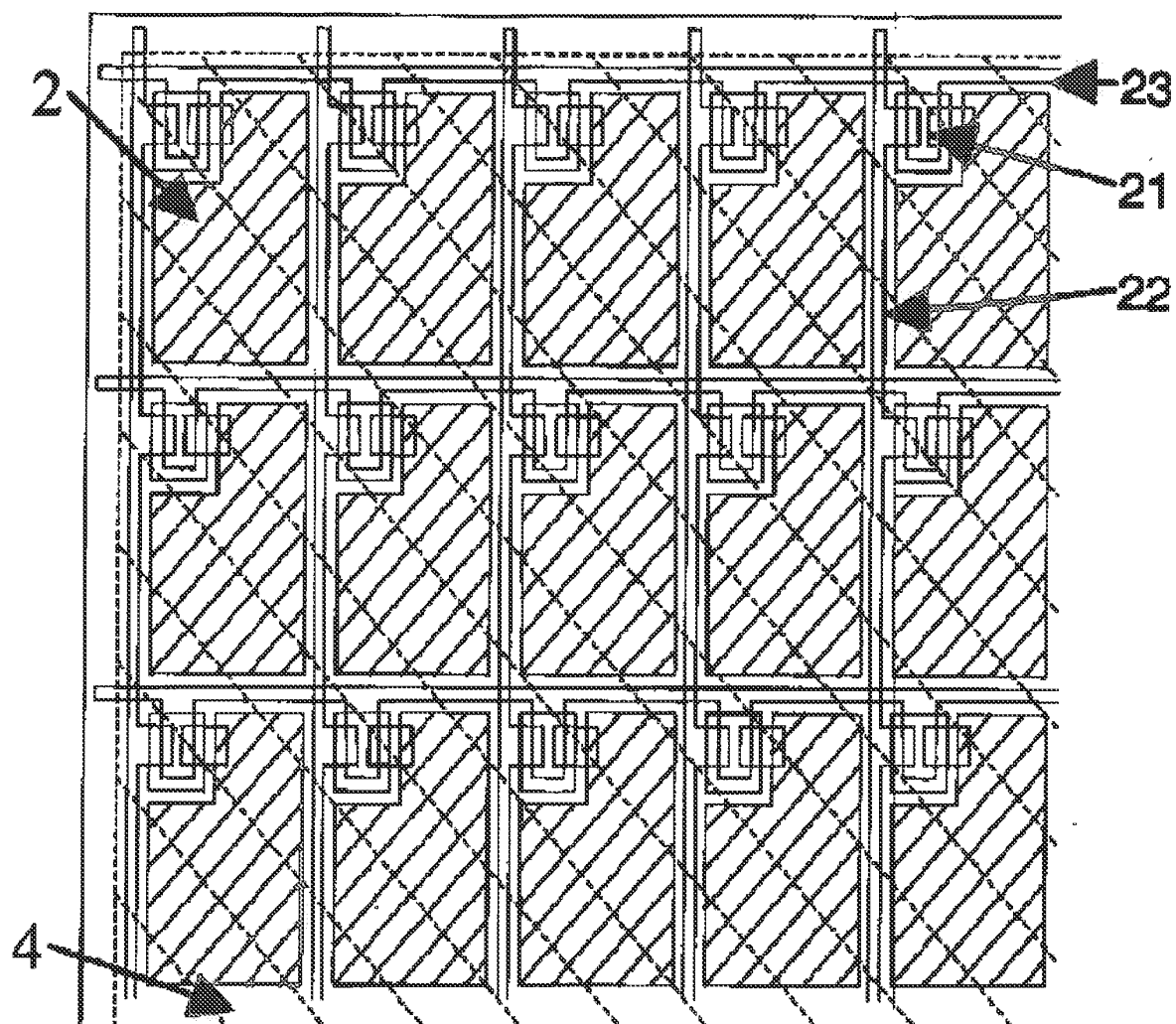
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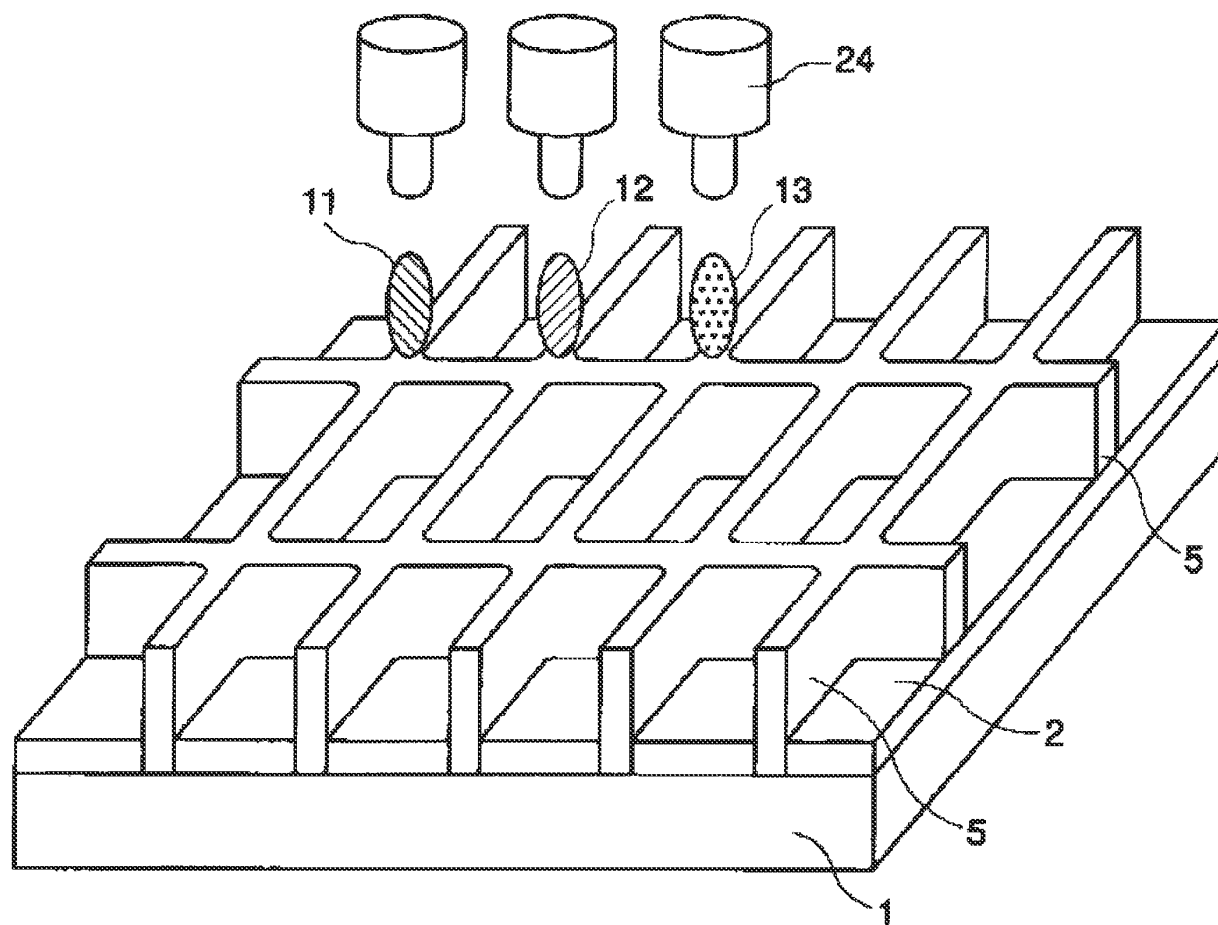












Electronic Acknowledgement Receipt	
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Supplemental Response or Supplemental Amendment	11425103_Response_NonCompliant.pdf	289412 f2cc1c66620b5e3e6083b6019eae6db4a9114ee2	no	5

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	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/917,885		Filing Date 11/02/2010		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =				
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APPLICATION AS AMENDED – PART II										
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	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
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AMENDMENT	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2629

Application No.: 12/917,885

Examiner: D. BOLOTIN

Filed: November 2, 2010

Docket No.: 114251.03

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND
ELECTRONIC DEVICE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

- ☒ 1. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, Notice of Allowance or other action that closes prosecution (e.g., Quayle Action).
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- ☒ 3. In accordance with 37 CFR §1.98(a)(2)(ii), copies of any U.S. patents and patent application publications are not attached.
- ☒ 4. One or more reference cited herein was cited in an Office Action in U.S. Application No. 11/483,087. See Reference 1. A copy of the Office Action is submitted for the Examiner's consideration as Reference 2.

Respectfully submitted,

Shahid Khan

James A. Oliff
Registration No. 27,075

Shahid K. Khan
Registration No. 60,984

JAO:SZK/szk

Date: June 7, 2012

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	APPLICANT(S) Yojiro MATSUEDA	
	FILING DATE November 2, 2010	GROUP 2629

U.S. PATENT DOCUMENTS				
Examiner Initials	Cite No.	Document Number	Date	Name
	1	2001/0049881 A1	12/13/2001	LOOK et al.
	2			
	3			
	4			

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
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	12	Office Action issued in U.S. Patent Application No. 11/483,087; mailed March 7, 2012.
	13	
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	17	

EXAMINER	DATE CONSIDERED
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

Date: June 7, 2012

Electronic Acknowledgement Receipt	
EFS ID:	12962860
Application Number:	12917885
International Application Number:	
Confirmation Number:	2374
Title of Invention:	ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE
First Named Inventor/Applicant Name:	Yojiro MATSUEDA
Customer Number:	25944
Filer:	James Albert Oliff/Clay Sellers
Filer Authorized By:	James Albert Oliff
Attorney Docket Number:	114251.03
Receipt Date:	07-JUN-2012
Filing Date:	02-NOV-2010
Time Stamp:	17:29:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	11425103_IDS_06-07-12.pdf	201473 2e63519820e9c0f6e270d0ce1e48413d08369d65	no	3

Warnings:

Information:

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2	Non Patent Literature	11425103_Ref1_06-07-12.pdf	792732	no	12
			821da3033e42c194e1402721e77bed7cf3aac3f5		
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Information:					
Total Files Size (in bytes):			994205		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/917,885	11/02/2010	Yojiro MATSUEDA	114251.03	2374
25944 7590 06/28/2012 OLIFF & BERRIDGE, PLC P.O. BOX 320850 ALEXANDRIA, VA 22320-4850			EXAMINER BOLOTIN, DMITRIY	
			ART UNIT 2629	PAPER NUMBER
			NOTIFICATION DATE 06/28/2012	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OfficeAction25944@oliff.com
jarmstrong@oliff.com

DETAILED ACTION

It would be of great assistance to the Office if all incoming papers pertaining to a filed application carried the following items:

1. Application number (checked for accuracy, including series code and serial no.).
2. Group art unit number (copied from most recent Office communication).
3. Filing date.
4. Name of the examiner who prepared the most recent Office action.
5. Title of invention.
6. Confirmation number (See MPEP § 503).

Status of Claims

1. **Claims 1, 2, 11 and 12** have been amended, **claims 3 – 10** have been canceled, new **claims 17 – 20** have been added; and **claims 1, 2 and 11 – 20** are pending.

Terminal Disclaimer

2. The terminal disclaimer filed on 05/09/2011 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 7,483,001 has been reviewed and is approved.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1, 2, 13, 14 and 17 – 20** are rejected under 35 U.S.C. 102(e) as being anticipated by Koyama (US 7,277,070).

As to **claim 1**, Koyama discloses an electro-optical device comprising: a data line (signal line Si of fig. 20); a control line (gate signal line Gaj of fig. 20); and a unit circuit arranged corresponding to an intersection of the data line and the control line (fig. 20), the unit circuit including: a first transistor (transistor 104 of fig. 20) that includes a first semiconductor film (semiconductor film 5005 of fig. 21A); an electro-optical element (pixel electrode 181 of fig. 20) electrically connected to one of a source or a drain of the first transistor (181 is electrically connected to 104 through transistor 105 of fig. 20); a second transistor (transistor 103 of fig. 20) that includes a second semiconductor film (semiconductor film 5004 of fig. 21A), the second transistor connected between the one of the source or the drain and a gate of the first transistor (transistor 103 of fig. 20); and a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor according to a data signal (capacitor 107 of fig. 20), and a wiring (184 of fig. 20) connected between the second transistor (103 of fig. 20) and the gate of the first transistor (104 of fig. 20); and the first transistor supplying a current based on the gate voltage (TFT 104 is current controlling TFT (col. 27, line 60 – col. 28, line 20), inherently, TFT 104 is on based on voltage at the gate, inducing current through OLED) to the electro-optical element (181 of fig. 22), the wiring being formed in

a layer which is different from a layer in which the first semiconductor film and the second semiconductor film

are formed (as shown in fig. 20, the wiring is not in semiconductor areas of either TFT 103 or TFT 104, the wiring is formed in layer 5059 of figs. 22 and 23); and the wiring being formed in a layer different from a gate layer in which the gate of the first transistor is formed (as shown in fig. 20, the wiring 184 and gate layer 185 are in different layers (col. 27, line 60 – col. 28, line 20)).

As to **claim 2** (dependent on 1), Koyama discloses the electro-optical device, wherein the first transistor has a conduction type different from a conduction film the second transistor has (second switching transistor TFT 103 may be n-channel and current controlling TFT may be p-channel, col. 9, lines 45 – 50).

As to **claim 13** (dependent on 1) and **claim 14** (dependent on 2), Koyama discloses an electric device comprising an electro-optic device (television of fig. 24A).

As to **claim 17**, Koyama discloses an electro-optical device comprising: a data line (signal line Si of fig. 20); a control line (gate signal line Gaj of fig. 20); a power line (power line Vi of fig. 20); and a unit circuit arranged corresponding to an intersection of the data line and the control line (fig. 20), the unit circuit including: a first transistor (transistor 104 of fig. 20) that includes a first semiconductor film (semiconductor film 5005 of fig. 21A); an electro-optical element (pixel electrode 181 of fig. 20) electrically connected to one of a source or a drain of the first transistor (181 is electrically connected to 104 through transistor 105 of fig. 20); a second transistor (transistor 103 of

fig. 20) that includes a second semiconductor film (semiconductor film 5004 of fig. 21A), the second transistor connected between the one of the source or the drain and a gate electrode of the first transistor (transistor 104 of fig. 20); a holding element that is connected to the gate electrode of the first transistor and holds a gate voltage of the first transistor according to a data signal (capacitor 107 of fig. 20); and a wiring connected between the gate electrode of the first transistor and the second transistor (184 of fig. 20), the first transistor supplying a current, based on the gate voltage to the electro-optical element (TFT 104 is current controlling TFT (col. 27, line 60 – col. 28, line 20), inherently, TFT 104 is on based on voltage at the gate, inducing current through OLED), the wiring being formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film are formed (as shown in fig. 20, the wiring is not in semiconductor areas of either TFT 103 or TFT 104, the wiring is formed in layer 5059 of figs. 22 and 23), and the wiring being formed in a layer different from a gate layer in which the gate electrode of the first transistor formed (as shown in fig. 20, the wiring 184 and gate layer 185 are in different layers (col. 27, line 60 – col. 28, line 20)).

As to **claim 18**, Koyama discloses an electro-optical device comprising: a data line (signal line Si of fig. 20); a control line (gate signal line Gaj of fig. 20); a power line (power line Vi of fig. 20); and a unit circuit arranged corresponding to an intersection of the data line and the control line (fig. 20), the unit circuit including: a first transistor (transistor 104 of fig. 20) that includes a first semiconductor film (semiconductor film

5005 of fig. 21A); an electro-optical element (pixel electrode 181 of fig. 20) electrically connected to one of a source or a drain of the first transistor (181 is electrically connected to 104 through transistor 105 of fig. 20); a second transistor (transistor 103 of fig. 20) that includes a second semiconductor film (semiconductor film 5004 of fig. 21A), the second transistor connected between the one of a source or the drain and a gate electrode of the first transistor (transistor 104 of fig. 20); a holding element that is connected to the gate electrode of the first transistor and holds a gate voltage of the first transistor according to a data signal (capacitor 107 of fig. 20); and a wiring connected between the gate electrode of the first transistor and the second transistor (184 of fig. 20), the first transistor supplying a current based on the gate voltage to the electro-optical element (TFT 104 is current controlling TFT (col. 27, line 60 – col. 28, line 20), inherently, TFT 104 is on based on voltage at the gate, inducing current through OLED), and the wiring being (184 of fig. 20) formed in a layer in which the data line (182 of fig. 20) and the power line (Vi of fig. 20) are formed.

As to **claim 19** (dependent on 17), Koyama discloses the electro-optical device, wherein the first transistor (104 of fig. 20) has a first terminal and a second terminal (source and drain shown in fig. 20), and a channel region disposed between the first terminal and the second terminal (channel region of 104 of fig. 20 corresponding to layer 5005 of fig. 21A), the first terminal (terminal connected to Vi of fig. 20) being disposed between the power line (Vi of fig. 20) and the second terminal (terminal connected to 186 of fig. 20), and the first transistor controlling an electrical connection

between the first terminal and the second terminal (via gate 185 of fig. 21).

As to **claim 20** (dependent on 18), Koyama discloses the electro-optical device, wherein the first transistor (104 of fig. 20) has a first terminal, a second terminal (source and drain shown in fig. 20), and a channel region disposed between the first terminal and the second terminal (channel region of 104 of fig. 20 corresponding to layer 5005 of fig. 21A), the first terminal (terminal connected to Vi of fig. 20) being disposed between the power line (Vi of fig. 20) and the second terminal (terminal connected to 186 of fig. 20), and the first transistor controlling an electrical connection between the first terminal and the second terminal (via gate 185 of fig. 21).

Allowable Subject Matter

5. **Claims 11, 12, 15 and 16** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
6. The following is a statement of reasons for the indication of allowable subject matter:

The Prior Art of record discloses the electro-optical device wherein the control line (gate line Gaj of fig. 20) supplies a control signal to a gate of the second transistor (103 of fig. 20), but fails to disclose that “*the control line intersecting the wiring*”.

Response to Arguments

7. Applicant's arguments filed 04/26/2012 have been fully considered but they are not persuasive.

8. As to Applicant's argument that “Koyama does not disclose that the wiring being formed in a layer different from a gate layer in which the gate of the first transistor is formed,” the Examiner respectfully disagrees. Koyama discloses “connection wiring line 184” (col. 27, line 65 – col. 28, line 2). As shown in fig. 20, the connection wiring 184 and gate 185 are in different layers.

9. As to Applicant's argument that “description alone does not provide sufficient detail to determine whether the wiring connecting TFT 103 and the gate of the TFT 104 is either the connection wiring 184, the gate wiring line 185, or both the connection wiring 184 and the gate wiring line 185,” the Examiner respectfully disagrees. As shown in fig. 20, wiring 184 connecting source region of transistor 103 and the gate 185 of transistor 104.

10. As to Applicant's argument that “Koyama does not anticipate that the wiring being formed in a layer different from a gate layer in which the gate of the first transistor

is formed,” the Examiner respectfully disagrees. As shown in fig. 20, “connection wiring line 184” and the gate 185 of transistor 184 are in different layers.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DMITRIY BOLOTIN whose telephone number is (571)270-5873. The examiner can normally be reached on Monday-Friday, 7:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571)272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DMITRIY BOLOTIN/
Examiner, Art Unit 2629

/Amare Mengistu/
Supervisory Patent Examiner, Art Unit 2629

<i>Index of Claims</i> 	Application/Control No. 12917885	Applicant(s)/Patent Under Reexamination MATSUEDA, YOJIRO
	Examiner DMITRIY BOLOTIN	Art Unit 2629

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant
 ☐ CPA
 ☐ T.D.
 ☐ R.1.47

CLAIM		DATE							
Final	Original	01/28/2011	06/07/2011	10/25/2011	06/08/2012				
	1	✓	✓	✓	✓				
	2	✓	✓	✓	✓				
	3	✓	✓	-	-				
	4	✓	✓	-	-				
	5	✓	✓	-	-				
	6	✓	✓	-	-				
	7	✓	✓	-	-				
	8	✓	✓	-	-				
	9	✓	✓	-	-				
	10	✓	✓	-	-				
	11			○	○				
	12			○	○				
	13			✓	✓				
	14			✓	✓				
	15			○	○				
	16			○	○				
	17				✓				
	18				✓				
	19				✓				
	20				✓				

<i>Search Notes</i> 	Application/Control No. 12917885	Applicant(s)/Patent Under Reexamination MATSUEDA, YOJIRO
	Examiner DMITRIY BOLOTIN	Art Unit 2629

SEARCHED			
Class	Subclass	Date	Examiner
345	76-83	1/28/2011	DB
315	169.1-169.4	1/28/2011	DB
	Updated Search	06/07/2011	DB
	Updated Search	10/25/2011	DB
349	42,43,46	10/25/2011	DB
	Updated Search	06/08/2012	DB

SEARCH NOTES			
Search Notes		Date	Examiner
Google		1/28/2011	DB
EAST		1/28/2011	DB
Updated Search		06/07/2011	DB
Updated Search		10/25/2011	DB
Updated Search		06/08/2012	DB

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

/DMITRIY BOLOTIN/ Examiner, Art Unit 2629	
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Receipt date: 12/09/2011

12917885 - GAU: 2629

Sheet 1 of 1

Form PTO-1449 (REV. 1/06)		US Dept. of Commerce PATENT & TRADEMARK OFFICE		ATTY DOCKET NO. 114251.03		APPLICATION NO. 12/917,885	
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)				APPLICANT(S) Yojiro MATSUEDA			
				FILING DATE November 2, 2010		GROUP 2629	
U.S. PATENT DOCUMENTS							
Examiner Initials	Cite No.	Document Number	Date	Name			
FOREIGN PATENT DOCUMENTS							
Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation	
OTHER DOCUMENTS							
Examiner Initials	Cite No.	Including name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume/issue number(s), publisher, city and/or country where published.					
/D.B./	1	Office Action issued in U.S. Patent Application No. 11/483,087 mailed November 10, 2011.					
EXAMINER				DATE CONSIDERED			
/Dmitriy Bolotin/				06/08/2012			
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

Date: December 9, 2011

Receipt date: 04/26/2012

12917885 - GAU; 2629

Modified Form PTO-1449 (REV. 5/11) PATENT & TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY DOCKET NO. 114251.03	APPLICATION NO. 12/917,885
	APPLICANT(S) Yojiro MATSUEDA	
	FILING DATE November 2, 2010	GROUP 2629

U.S. PATENT DOCUMENTS				
Examiner Initials	Cite No.	Document Number	Date	Name
	1	5,144,288 A	09/01/1992	Hamada et al.
	2	7,368,868 B2	05/06/2008	Sakamoto

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
	3	EP 0158366 A2	10/16/1985	Europe		
	4	EP 1594347 A1	11/09/2005	Europe		
	5	EP 1024472	08/02/2000	Europe		
	6	JP-A-10-12377	01/16/1998	Japan	X	X
	7	JP-A-2001-85162	03/30/2001	Japan	X	X

OTHER DOCUMENTS		
Examiner Initials	Cite No.	Including name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
	8	March 28, 2012 Search Report issued in European Patent Application No. 10191880.3
	9	Lungu G. Et al.: "Thin Film Active Matrix Organic Electroluminescent Display Development", University/Government/Industry Microelectronics Symposium, 1997 IEEE; pages 165-168

EXAMINER /Dmitriy Bolotin/	DATE CONSIDERED 06/08/2012
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

Date: April 26, 2014

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.B./

Receipt date: 06/07/2012

12917885 - GAU; 2629

Modified Form PTO-1449 (REV. 5/11) PATENT & TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY DOCKET NO. 114251.03	APPLICATION NO. 12/917,885
	APPLICANT(S) Yojiro MATSUEDA	
	FILING DATE November 2, 2010	GROUP 2629

U.S. PATENT DOCUMENTS				
Examiner Initials	Cite No.	Document Number	Date	Name
/D.B./	1	2001/0049881 A1	12/13/2001	LOOK et al.
	2			
	3			
	4			

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
	5					
	6					
	7					
	8					
	9					
	10					
	11					

OTHER DOCUMENTS		
Examiner Initials	Cite No.	Including name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
/D.B./	12	Office Action issued in U.S. Patent Application No. 11/483,087; mailed March 7, 2012.
	13	
	14	
	15	
	16	
	17	

EXAMINER /Dmitriy Bolotin/	DATE CONSIDERED 06/08/2012
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

Date: June 7, 2012

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2629

Application No.: 12/917,885

Examiner: D. BOLOTIN

Filed: November 2, 2010

Docket No.: 114251.03

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND
ELECTRONIC DEVICE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

- ☒ 1. This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection, Notice of Allowance, or other action that closes prosecution (e.g., Quayle Action), but on or before payment of the Issue Fee. The fees associated with this filing under 37 C.F.R. §1.17(p) are being paid electronically with this filing. The Commissioner is hereby authorized to charge any additional fee (or credit any overpayment) associated for this filing to Deposit Account No. 15-0461.
- ☒ a. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this Information Disclosure Statement.
37 CFR §1.97(e)(2).

- ☒ 2. Each item of information contained in this Information Disclosure Statement was either first cited in a communication from a patent office in a counterpart foreign or international application or from the USPTO, or is a communication that was issued by a patent office in a counterpart foreign or international application or by the USPTO, and this communication was not received by any individual designated in §1.56(c) more than thirty days prior to the filing of this Information Disclosure Statement.
- ☒ 3. In accordance with 37 CFR §1.98(a)(2)(ii), copies of any U.S. patents and patent application publications are not attached.

Respectfully submitted,

Shahid Khan

James A. Oliff
Registration No. 27,075

Shahid K. Khan
Registration No. 60,984

JAO:SZK/bbc

Date: July 16, 2012

OLIFF & BERRIDGE, PLC
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Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

<p>DEPOSIT ACCOUNT USE AUTHORIZATION Please grant any extension necessary for entry of this filing; Charge any fee due to our Deposit Account No. 15-0461</p>

Modified Form PTO-1449 (REV. 5/11) PATENT & TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY DOCKET NO. 114251.03	APPLICATION NO. 12/917,885
	APPLICANT(S) Yojiro MATSUEDA	
	FILING DATE November 2, 2010	GROUP 2629

U.S. PATENT DOCUMENTS				
Examiner Initials	Cite No.	Document Number	Date	Name
	1	2005/0231122 A1	10/20/2005	Osame et al.
	2	7,483,001 B2	01/27/2009	Matsueda

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation

OTHER DOCUMENTS		
Examiner Initials	Cite No.	Including name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.

EXAMINER	DATE CONSIDERED
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

Date: July 16, 2012

Electronic Patent Application Fee Transmittal				
Application Number:		12917885		
Filing Date:		02-Nov-2010		
Title of Invention:		ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE		
First Named Inventor/Applicant Name:		Yojiro MATSUEDA		
Filer:		James Albert Oliff/Becky Campbell		
Attorney Docket Number:		114251.03		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
Total in USD (\$)				180

Electronic Acknowledgement Receipt	
EFS ID:	13256397
Application Number:	12917885
International Application Number:	
Confirmation Number:	2374
Title of Invention:	ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE
First Named Inventor/Applicant Name:	Yojiro MATSUEDA
Customer Number:	25944
Filer:	James Albert Oliff/Becky Campbell
Filer Authorized By:	James Albert Oliff
Attorney Docket Number:	114251.03
Receipt Date:	16-JUL-2012
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Application Type:	Utility under 35 USC 111(a)

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RAM confirmation Number	9894
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Authorized User	
<p>The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:</p> <p>Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)</p> <p>Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)</p>	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	11425103_ids_7_16_12.pdf	111111	no	3
			f92a4091587e6ef753ffb7b20e3a3fdc8e013b52		
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
2	Fee Worksheet (SB06)	fee-info.pdf	30784	no	2
			15b84c0f04f39674fd59a7d114d682cd3e63af31		
Warnings:					
Information:					
Total Files Size (in bytes):			141895		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

PATENT APPLICATION

*Recd
1/18*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Application No.: 12/917,885

Filed: November 2, 2010

For: ACTIVE MATRIX SUBSTRATE,
ELECTRO-OPTICAL DEVICE, AND
ELECTRONIC DEVICE



Group Art Unit: 2629

Examiner: D. BOLOTIN

Docket No.: 114251.03

MAIL STOP RCE

**LARGE ENTITY REQUEST FOR
CONTINUED EXAMINATION UNDER 37 C.F.R. §1.114**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. §1.114, Applicant hereby requests continued examination.

☒ Applicant further requests entry and consideration of the attached submission.

The above-identified application was filed on or after June 8, 1995. Thus, entry is proper under 37 C.F.R. §1.114(d).

Attached hereto is our check no. 247989 in the amount of \$930.00 as payment of the fees set forth in 37 C.F.R. §1.17(e). The Commissioner is hereby authorized to charge any additional fees or credit any overpayment associated for this filing to Deposit Account No. 15-0461.

Respectfully submitted,

H. Yamashita

James A. Oliff
Registration No. 27,075

Hirotsuna Yamashita
Registration No. L0563

JAO:HQY/prg

Date: September 28, 2012

OLIFF & BERRIDGE, PLC
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Telephone: (703) 836-6400

<p>DEPOSIT ACCOUNT USE AUTHORIZATION</p> <p>Please grant any extension necessary for entry of this filing; Charge any fee due to our Deposit Account No. 15-0461</p>
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10/01/2012 HVUONG1 00000004 12917885

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2629

Application No.: 12/917,885

Examiner: D. BOLOTIN

Filed: November 2, 2010

Docket No.: 114251.03

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND
ELECTRONIC DEVICE

AMENDMENT WITH REQUEST FOR CONTINUED EXAMINATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the June 28, 2012 Office Action, and upon entry of the attached Request
for Continued Examination, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An electro-optical device comprising:

a data line;

a control line; and

a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit including:

a first transistor that includes a first semiconductor film;

an electro-optical element electrically connected to one of a source or a drain of the first transistor;

a second transistor that includes a second semiconductor film, the second transistor connected between the one of the source or the drain and a gate of the first transistor;

a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor according to a data signal; and

a wiring connected between the second transistor and the gate of the first transistor,

the first transistor supplying a current based on the gate voltage to the electro-optical element,

the wiring being formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film are formed, and

the wiring being formed in athe layer different from a gate layer in which the gate of the first transistor is ~~formed~~formed, and

the wiring having a portion formed in the layer, the portion extending in a direction in which the data line extends.

2. (Previously Presented) The electro-optical device according to claim 1, wherein the first transistor has a conduction type different from a conduction film the second transistor has.

3-10. (Canceled)

11. (Previously Presented) The electro-optical device according to claim 1, wherein the control line supplies a control signal to a gate of the second transistor, the control line intersecting the wiring.

12. (Previously Presented) The electro-optical device according to claim 11, wherein the unit circuit further includes a third transistor coupled between the holding element and the data line, and

wherein the second transistor and the third transistor are controlled according to the control signal.

13. (Previously Presented) An electric device comprising an electro-optical device according to claim 1.

14. (Previously Presented) An electric device comprising an electro-optical device according to claim 2.

15. (Previously Presented) An electric device comprising an electro-optical device according to claim 11.

16. (Previously Presented) An electric device comprising an electro-optical device according to claim 12.

17. (Currently Amended) An electro-optical device comprising:
a data line;
a control line;

a power line; and

a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit including:

a first transistor that includes a first semiconductor film;

an electro-optical element electrically connected to one of a source or a drain of the first transistor;

a second transistor that includes a second semiconductor film, the second transistor connected between the one of the source or the drain and a gate electrode of the first transistor;

a holding element that is connected to the gate electrode of the first transistor and holds a gate voltage of the first transistor according to a data signal; and

a wiring connected between the gate electrode of the first transistor and the second transistor,

the first transistor supplying a current based on the gate voltage to the electro-optical element,

the wiring being formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film are formed, and

the wiring being formed in at the layer different from a gate layer in which the gate electrode of the first transistor ~~formed.~~ formed, and

the wiring having a portion formed in the layer, the portion extending in a direction in which the data line extends.

18. (Currently Amended) An electro-optical device comprising:

a data line;

a control line;

a power line; and

a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit including:

a first transistor that includes a first semiconductor film;

an electro-optical element electrically connected to one of a source or a drain of the first transistor;

a second transistor that includes a second semiconductor film, the second transistor connected between the one of a source or the drain and a gate electrode of the first transistor;

a holding element that is connected to the gate electrode of the first transistor and holds a gate voltage of the first transistor according to a data signal; and

a wiring connected between the gate electrode of the first transistor and the second transistor,

the first transistor supplying a current based on the gate voltage to the electro-optical element, and

the wiring being formed in the layer in which the data line and the power line are ~~formed~~formed, and

the wiring having a portion formed in the layer, the portion extending in a direction in which the data line extends.

19. (Previously Presented) The electro-optical device according to claim 17, wherein the first transistor has a first terminal, a second terminal, and a channel region disposed between the first terminal and the second terminal, the first terminal being disposed between the power line and the second terminal, and the first transistor controlling an electrical connection between the first terminal and the second terminal.

20. (Previously Presented) The electro-optical device according to claim 18,

wherein the first transistor has a first terminal, a second terminal, and a channel region disposed between the first terminal and the second terminal, the first terminal being disposed between the power line and the second terminal, and the first transistor controlling an electrical connection between the first terminal and the second terminal.

REMARKS

Claims 1, 2 and 11-20 are pending in this application. By this Amendment, claims 1, 17 and 18 are amended. Support for the amendments may be found in at least Figs. 2, 8 and 10. No new matter is added. Applicant respectfully requests reconsideration and prompt allowance of the pending claims at least in light of the following remarks.

I. Allowable Claims

Applicant gratefully acknowledges the Office Action's indication that claims 11, 12, 15 and 16 recite allowable subject matter.

II. 35 U.S.C. §102(e) Rejection

Claims 1, 2, 13, 14 and 17-20 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 7,277,070 (Koyama). Applicant respectfully traverses the rejection for the following two reasons.

A. Koyama Fails To Disclose A Wiring Connected Between The Second Transistor And The Gate Of The First Transistor

Koyama fails to disclose "a wiring connected between the second transistor and the gate of the first transistor," as recited in claim 1, and "a wiring connected between the gate electrode of the first transistor and the second transistor," as recited in claims 17 and 18.

The Office Action asserts that a connection wiring line 184 of Koyama corresponds to the claimed wiring. The Office Action also asserts that Fig. 20 of Koyama discloses that the connection wiring line 184 is connected between a second switching TFT 103 (i.e., the asserted claimed second transistor) and a gate of a current controlling TFT 104 (i.e., the asserted claimed first transistor). This assertion is unreasonable for the following three reasons.

i. It Is Improper To Rely On Fig. 20

It is improper for the Office Action to rely on Fig. 20 of Koyama for the above feature. Fig. 20 of Koyama is a top view of a pixel of a light emitting device. However, Fig.

20 does not clearly show how the connection wiring line 184 is connected. It is improper for the Patent Office to rely on a drawing of the cited reference if the drawing is not clearly described as disclosing the claimed feature. "A drawing can be used as prior art and anticipate claim only if the drawing clearly shows the structure which is claimed." *In re Mraz*, 455 F.2d 1069, 173 USPQ 25 (CCPA 1972); MPEP §2125. Thus, it is improper that the Office Action relies on Fig. 20 of Koyama for the above feature.

Further, as discussed below, it is reasonably interpreted that Fig. 20 of Koyama fails to disclose that the connection wiring line 184 is connected between the second switching TFT 103 (i.e., the asserted claimed second transistor) and the gate of the current controlling TFT 104 (i.e., the asserted claimed first transistor).

ii. Fig. 20 of Koyama Fails To Disclose The Above Feature

As shown in the attached enlarged Fig. 20 of Koyama, the configuration of the connection wiring line 184 is unclear. Thus, the Office Action's assertion (i.e., the connection wiring line 184 is connected between the second switching TFT 103 and the gate of a current controlling TFT 104) is groundless. Further, as discussed below, it is reasonably interpreted that Fig. 20 of Koyama fails to disclose that the connection wiring line 184 is connected between the second switching TFT 103 and the gate of a current controlling TFT 104.

As shown in the attached enlarged Fig. 20 of Koyama, because hatching lines in a region depicted as 184 are the same as those in Vi, it is reasonably understood that the connection wiring line 184 is formed in the same layer as a power supply line Vi. Accordingly, two possible cross-sectional structures can be derived from Figure 20 as shown in Cross-sections I and II (see attached Enlarged Fig. 20 of Koyama).

Cross-section I shows the connecting wiring line 184 extending parallel to a gate wiring line 185 and connected to the power supply line Vi. However, this cross-sectional

structure appears to be impossible, because a part of the gate wiring line 185 should form, as one of two electrodes, a capacitor 107 in combination with a part of the power supply line Vi, as the other of the two electrodes. However, as shown in Cross-section I, if the connection wiring line 184 were connected to the power supply line Vi, no capacitor could be formed between the wiring lines 184 and 185 because no potential difference exists. Therefore, possible structure should be Cross-section II.

In Cross-section II, the connection wiring line 184 is formed on contact holes, but it cannot be extended parallel to the gate wiring line 185 towards the gate of the transistor 104 for the following reasons. First, because the gate wiring line 185 is already connected to the gate of the transistor 104, there is no need for the connection wiring line 184 to be further connected to the gate of the transistor 104. Secondly, if the connection wiring line 184 were to extend towards the gate of the transistor 104, it should overlap with the gate wiring line 185. However, there is no indication in Figure 20 that the connection wiring line 184 overlaps with the gate wiring line 185 and the gate wiring line 185 alone is depicted as a line to connect the contact hole with the gate of the transistor 104. Accordingly, it is reasonably concluded that the connection wiring line 184 in Figure 20 is merely formed on the contact holes, and thus Fig. 20 of Koyama fails to disclose that the connection wiring line 184 is connected between the second switching TFT 103 and the gate of a current controlling TFT 104. Thus, Fig. 20 of Koyama fails to disclose the above feature of claims 1, 17 and 18.

iii. Koyama Fails To inherently Disclose The Above Feature

Koyama fails to inherently disclose the above feature of claims 1, 17 and 18. As discussed above, Fig. 20 of Koyama fails to disclose the above feature. Further, the specification of Koyama fails to disclose the above feature (see, e.g., column 27, line 65-column 28, line 2). Thus, the Office Action appears to assert that Koyama inherently disclose the above feature. However, Koyama fails to inherently disclose the above claimed feature.

To establish inherency, it must be clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill (MPEP §2112). Inherency may not be established by probabilities or possibilities (*Id.*). The mere fact that a certain thing may result from a given set of circumstances is not sufficient (*Id.*). In the present case, as discussed above, it is reasonably interpreted that Koyama fails to disclose that the connection wiring line 184 is connected between the second switching TFT 103 and the gate of a current controlling TFT 104. In addition, the Examiner does not provide any extrinsic evidence proving that the above claimed feature is necessarily present in Fig. 20. Because the Examiner does not provide the extrinsic evidence that must make clear that the above claimed feature is necessary present (i.e., the connection wiring line 184 is necessary connected between the second switching TFT 103 and a gate of a current controlling TFT 104), Fig. 20 does not inherently disclose the above claimed feature. Thus, Koyama fails to disclose the above feature of claims 1, 17 and 18.

B. Koyama Fails To Disclose The Claimed Features of The Wiring

Koyama fails to disclose "the wiring being formed in the layer different from a gate layer in which the gate of the first transistor is formed, and the wiring having a portion formed in the layer, the portion extending in a direction in which the data line extends," as recited in claims 1, 17 and 18.

First, Koyama fails to disclose that the asserted connection wiring line 184 extends in a direction a data line extends (see Fig. 20). Thus, Koyama fails to disclose i) the wiring having a portion formed in the layer, the portion extending in a direction in which the data line extends, as recited in claims 1, 17 and 18.

Second, Koyama fails to disclose ii) the wiring being formed in the layer different from a gate layer in which the gate of the first transistor is formed. The Office Action asserts

that Fig. 20 of Koyama discloses that the connection wiring line 184 and the gate wiring line 185 are different layers. This assertion is unreasonable.

That, it is improper for the Office Action to rely on Fig. 20 of Koyama for the above feature because Fig. 20 does not clearly show how the connection wiring line 184 and the gate wiring line 185 are formed. "A drawing can be used as prior art and anticipate claim only if the drawing clearly shows the structure which is claimed." *In re Mraz*, 455 F.2d 1069, 173 USPQ 25 (CCPA 1972); MPEP §2125.

Further, Koyama discloses that the second switching TFT 103 has a source region and a drain region one of which is connected to the drain region of the current controlling TFT 104 through the connection wiring line 183 and the other of which is connected to a connection wiring line 184 and to a gate wiring line 185 (see, column 27, line 65-column 28, line 2). However, Koyama fails to disclose that the wiring 184 and a gate wiring line 185 are different layers.

In addition, Koyama fails to inherently disclose this feature. To establish inherency, it must be clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill (MPEP §2112). Inherency may not be established by probabilities or possibilities (*Id.*). The mere fact that a certain thing may result from a given set of circumstances is not sufficient (*Id.*). In the present case, the Examiner does not provide any extrinsic evidence proving that the above claimed feature is necessarily present in Koyama (i.e., the connection wiring line 184 and the gate wiring line 185 are different layers). Because the Examiner does not provide the extrinsic evidence that must make clear that the above claimed feature is necessarily present, Koyama does not inherently disclose the above claimed feature.

Thus, Koyama fails to disclose ii) the wiring being formed in the layer different from a gate layer in which the gate of the first transistor is formed. Accordingly, Koyama fails to disclose the above feature of claims 1, 17 and 18.

C. Conclusion

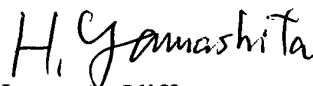
Thus, claims 1, 17 and 18 are patentable over Koyama. Further, claims 2, 13, 14, 19 and 20 are patentable for at least the same reasons as claims 1, 17 and 18, as well as for the additional features they recite. Applicant respectfully requests withdrawal of the rejection.

* * * * *

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



James A. Oliff

Registration No. 27,075

Hirotsuna Yamashita

Registration No. L0563

JAO:HQY/prg

Attachment:

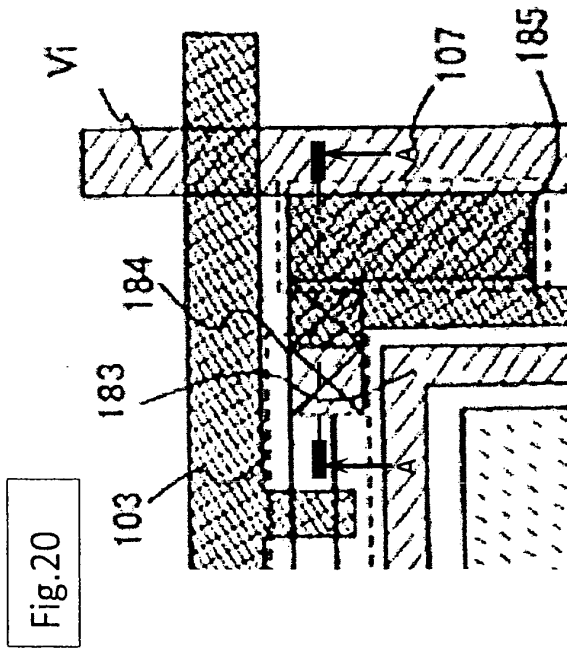
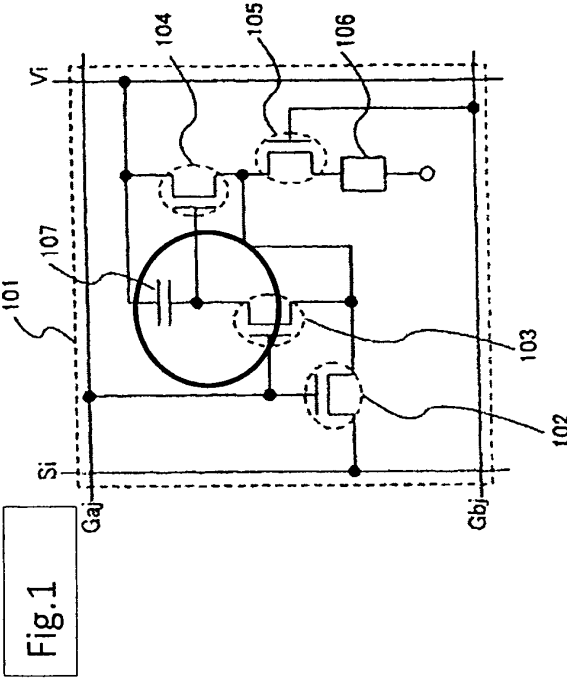
Request for Continued Examination
Enlarged Fig. 20 of Koyama

Date: September 28, 2012

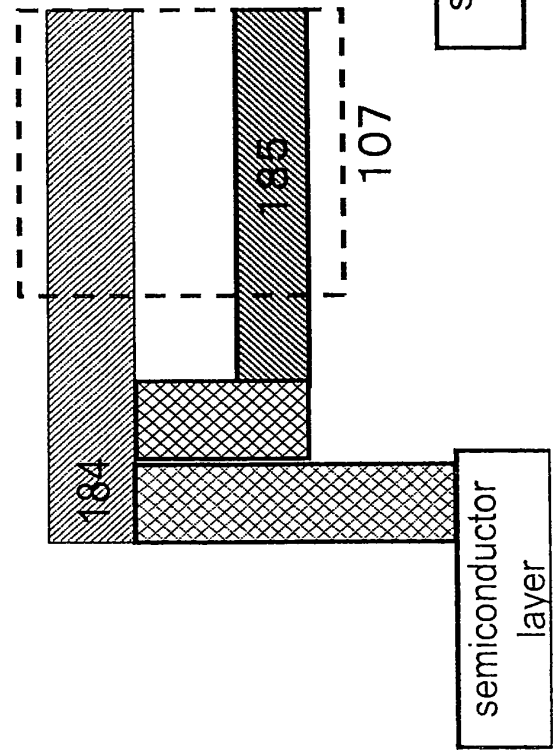
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Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

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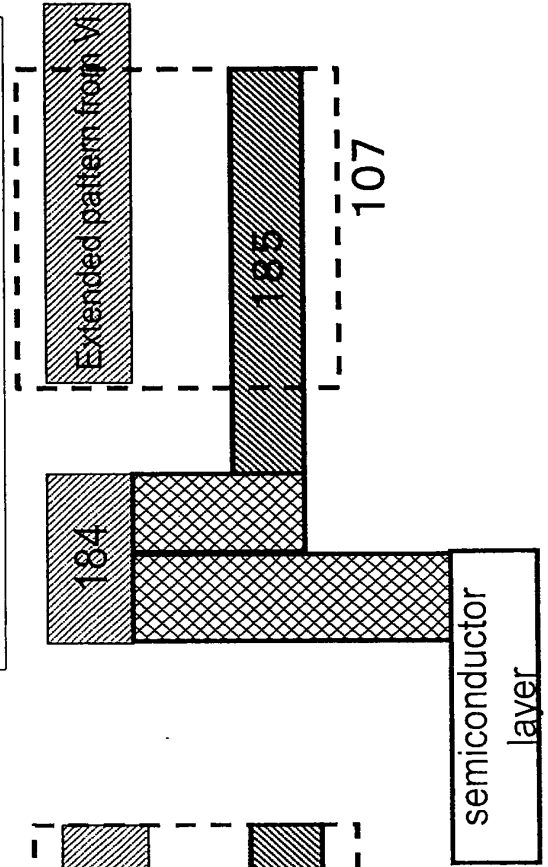
Enlarged Fig. 20 of Koyama



Possible Cross-section I -> impossible



Possible Cross-section II -> possible





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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/917,885	11/02/2010	Yojiro MATSUEDA	114251.03	2374
25944 7590 10/18/2012 OLIFF & BERRIDGE, PLC P.O. BOX 320850 ALEXANDRIA, VA 22320-4850			EXAMINER BOLOTIN, DMITRIY	
			ART UNIT 2695	PAPER NUMBER
			NOTIFICATION DATE 10/18/2012	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OfficeAction25944@oliff.com
jarmstrong@oliff.com

Office Action Summary	Application No.	Applicant(s)	
	12/917,885	MATSUEDA, YOJIRO	
	Examiner	Art Unit	
	DMITRIY BOLOTIN	2695	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 28 September 2012.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5) ☒ Claim(s) 1,2 and 11-20 is/are pending in the application.

5a) Of the above claim(s) ____ is/are withdrawn from consideration.

6) ☐ Claim(s) ____ is/are allowed.

7) ☒ Claim(s) 1,2,13,14,17-20 is/are rejected.

8) ☒ Claim(s) 11,12,15 and 16 is/are objected to.

9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

10) ☐ The specification is objected to by the Examiner.

11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. ____.
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) ☐ Notice of Informal Patent Application
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>7/16/2012</u> .	6) ☐ Other: ____.

DETAILED ACTION

It would be of great assistance to the Office if all incoming papers pertaining to a filed application carried the following items:

1. Application number (checked for accuracy, including series code and serial no.).
2. Group art unit number (copied from most recent Office communication).
3. Filing date.
4. Name of the examiner who prepared the most recent Office action.
5. Title of invention.
6. Confirmation number (See MPEP § 503).

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/28/2012 has been entered.

Status of Claims

2. **Claims 1, 17 and 18** have been amended, **claims 3 – 10** have been canceled; and **claims 1, 2 and 11 – 20** are pending.

Terminal Disclaimer

3. The terminal disclaimer filed on 05/09/2011 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 7,483,001 has been reviewed and is approved.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1, 2, 13, 14 and 17 – 20** are rejected under 35 U.S.C. 102(e) as being anticipated by Koyama (US 7,277,070).

As to **claim 1**, Koyama discloses an electro-optical device comprising: a data line (signal line Si comprising wiring 190 supplying signal to transistor 102 of fig. 20); a control line (gate signal line Gaj of fig. 20); and a unit circuit arranged corresponding to an intersection of the data line and the control line (fig. 20), the unit circuit including: a first transistor (transistor 104 of fig. 20) that includes a first semiconductor film (semiconductor film 5005 of fig. 21A); an electro-optical element (pixel electrode 181 of fig. 20) electrically connected to one of a source or a drain of the first transistor (181 is electrically connected to 104 through transistor 105 of fig. 20); a second transistor (transistor 103 of fig. 20) that includes a second semiconductor film (semiconductor film

5004 of fig. 21A), the second transistor connected between the one of the source or the drain and a gate of the first transistor (transistor 103 of fig. 20); and a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor according to a data signal (capacitor 107 of fig. 20), and

a wiring (184 of fig. 20) connected between the second transistor (103 of fig. 20) and the gate of the first transistor (104 of fig. 20); and the first transistor supplying a current based on the gate voltage (TFT 104 is current controlling TFT (col. 27, line 60 – col. 28, line 20), inherently, TFT 104 is on based on voltage at the gate, inducing current through OLED) to the electro-optical element (181 of fig. 22), the wiring being formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film

are formed (as shown in fig. 20, the wiring is not in semiconductor areas of either TFT 103 or TFT 104, the wiring is formed in layer 5059 of figs. 22 and 23);

the wiring being formed in the layer different from a gate layer in which the gate of the first transistor is formed (as shown in fig. 20, the wiring 184 and gate layer 185 are in different layers (col. 27, line 60 – col. 28, line 20)), and

the wiring having a portion formed in the layer (wiring 184 of fig. 20), the portion extending in a direction in which the data line extends (as shown in fig. 20, the wiring extends in the direction corresponding to the wiring 190).

As to **claim 2** (dependent on 1), Koyama discloses the electro-optical device, wherein the first transistor has a conduction type different from a conduction film the

second transistor has (second switching transistor TFT 103 may be n-channel and current controlling TFT may be p-channel, col. 9, lines 45 – 50).

As to **claim 13** (dependent on 1) and **claim 14** (dependent on 2), Koyama discloses an electric device comprising an electro-optic device (television of fig. 24A).

As to **claim 17**, Koyama discloses an electro-optical device comprising: a data line (signal line Si comprising wiring 190 supplying signal to transistor 102 of fig. 20); a control line (gate signal line Gaj of fig. 20); a power line (power line Vi of fig. 20); and a unit circuit arranged corresponding to an intersection of the data line and the control line (fig. 20), the unit circuit including: a first transistor (transistor 104 of fig. 20) that includes a first semiconductor film (semiconductor film 5005 of fig. 21A); an electro-optical element (pixel electrode 181 of fig. 20) electrically connected to one of a source or a drain of the first transistor (181 is electrically connected to 104 through transistor 105 of fig. 20); a second transistor (transistor 103 of fig. 20) that includes a second semiconductor film (semiconductor film 5004 of fig. 21A), the second transistor connected between the one of the source or the drain and a gate electrode of the first transistor (transistor 104 of fig. 20); a holding element that is connected to the gate electrode of the first transistor and holds a gate voltage of the first transistor according to a data signal (capacitor 107 of fig. 20); and a wiring connected between the gate electrode of the first transistor and the second transistor (184 of fig. 20), the first transistor supplying a current, based on the gate voltage to the electro-optical element (TFT 104 is current controlling TFT (col. 27, line 60 – col. 28, line 20), inherently, TFT

104 is on based on voltage at the gate, inducing current through OLED), the wiring being formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film are formed (as shown in fig. 20, the wiring is not in semiconductor areas of either TFT 103 or TFT 104, the wiring is formed in layer 5059 of figs. 22 and 23), the wiring being formed in the layer different from a gate layer in which the gate electrode of the first transistor formed (as shown in fig. 20, the wiring 184 and gate layer 185 are in different layers (col. 27, line 60 – col. 28, line 20)), and the wiring having a portion formed in the layer (wiring 184 of fig. 20), the portion extending in a direction in which the data line extends (as shown in fig. 20, the wiring extends in the direction corresponding to the wiring 190).

As to **claim 18**, Koyama discloses an electro-optical device comprising: a data line (signal line Si comprising wiring 190 supplying signal to transistor 102 of fig. 20); a control line (gate signal line Gaj of fig. 20); a power line (power line Vi of fig. 20); and a unit circuit arranged corresponding to an intersection of the data line and the control line (fig. 20), the unit circuit including: a first transistor (transistor 104 of fig. 20) that includes a first semiconductor film (semiconductor film 5005 of fig. 21A); an electro-optical element (pixel electrode 181 of fig. 20) electrically connected to one of a source or a drain of the first transistor (181 is electrically connected to 104 through transistor 105 of fig. 20); a second transistor (transistor 103 of fig. 20) that includes a second semiconductor film (semiconductor film 5004 of fig. 21A), the second transistor connected between the one of a source or the drain and a gate electrode of the first

transistor (transistor 104 of fig. 20); a holding element that is connected to the gate electrode of the first transistor and holds a gate voltage of the first transistor according to a data signal (capacitor 107 of fig. 20); and a wiring connected between the gate electrode of the first transistor and the second transistor (184 of fig. 20), the first transistor supplying a current based on the gate voltage to the electro-optical element (TFT 104 is current controlling TFT (col. 27, line 60 – col. 28, line 20), inherently, TFT 104 is on based on voltage at the gate, inducing current through OLED), the wiring being (184 of fig. 20) formed in the layer in which the data line (182 of fig. 20) and the power line (Vi of fig. 20) are formed, and the wiring having a portion formed in the layer (wiring 184 of fig. 20), the portion extending in a direction in which the data line extends (as shown in fig. 20, the wiring extends in the direction corresponding to the wiring 190).

As to **claim 19** (dependent on 17), Koyama discloses the electro-optical device, wherein the first transistor (104 of fig. 20) has a first terminal and a second terminal (source and drain shown in fig. 20), and a channel region disposed between the first terminal and the second terminal (channel region of 104 of fig. 20 corresponding to layer 5005 of fig. 21A), the first terminal (terminal connected to Vi of fig. 20) being disposed between the power line (Vi of fig. 20) and the second terminal (terminal connected to 186 of fig. 20), and the first transistor controlling an electrical connection between the first terminal and the second terminal (via gate 185 of fig. 21).

As to **claim 20** (dependent on 18), Koyama discloses the electro-optical device, wherein the first transistor (104 of fig. 20) has a first terminal, a second terminal (source

an drain shown in fig. 20), and a channel region disposed between the first terminal and the second terminal (channel region of 104 of fig. 20 corresponding to layer 5005 of fig. 21A), the first terminal (terminal connected to Vi of fig. 20) being disposed between the power line (Vi of fig. 20) and the second terminal (terminal connected to 186 of fig. 20), and the first transistor controlling an electrical connection between the first terminal and the second terminal (via gate 185 of fig. 21).

Allowable Subject Matter

6. **Claims 11, 12, 15 and 16** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

The Prior Art of record discloses the electro-optical device wherein the control line (gate line Gaj of fig. 20) supplies a control signal to a gate of the second transistor (103 of fig. 20), but fails to disclose that “*the control line intersecting the wiring*”.

Response to Arguments

8. Applicant's arguments filed 09/28/2012 have been fully considered but they are not persuasive.

9. As to Applicant's argument that Koyama fails to disclose "a wiring connected between the second transistor and the gate of the first transistor," as recited in claim 1, and "a wiring connected between the gate electrode of the first transistor and the second transistor," as recited in claims 17 and 18, the Examiner respectfully disagrees. Koyama discloses a wiring 184 of fig. 20 connected between the second transistor 103 of fig. 20 and the gate 185 of fig. 20 of the first transistor 104 of fig. 20 and Koyama discloses a wiring 184 of fig. 20 connected between the gate electrode 185 of fig. 20 of the first transistor 104 of fig. 20 and the second transistor 103 of fig. 20.

10. As to Applicant's argument that figure 20 of Koyama does not clearly show how the connection wiring line 184 is connected, the Examiner respectfully disagrees. First, Koyama discloses that source or drain of transistor 103 is connected to the connection wiring 184 and a gate wiring 185, col. 28, lines 1 - 5, therefore connection wiring 184 and a gate wiring 185 are indeed connected to each other. Second, as can be seen from fig. 20, connection wiring 184 is connected to the source or drain of TFT 103 through a via represented by "X" (the profile can be seen from fig. 23A, where connection wiring 184 is represented by element 5059) and connection wiring 184 is extended to be connected to gate wiring 185 that another via represented by "X". Therefore, Koyama clearly show how the connection wiring line 184 is connected.

11. As to Applicant's argument that Koyama fails to disclose that the connection wiring line 184 is connected between the second switching transistor TFT 103 and the gate of current controlling TFT 104, the Examiner respectfully disagrees. Koyama discloses that source or drain of transistor 103 is connected to the connection wiring

184 and a gate wiring 185, col. 28, lines 1 – 5, as show in fig. 20, the gate wiring 185 is not directly connected to the source or drain of transistor 103 (this can also be seen from fig. 23A, where the gate of current controlling TFT 5055 is not directly connected to the source or drain of the second switching TFT, but instead the source or drain of the second switching TFT is connected to connection wiring 5059). Therefore Koyama discloses that the connection wiring line 184 is connected between the second switching transistor TFT 103 and the gate 185 of current controlling TFT 104.

12. As to Applicant's argument that "because the gate wiring line 185 is already connected to the gate of the transistor 104, there is no need for the connection wiring line 184 to be further connected to the gate of the transistor 104," the Examiner respectfully disagrees. Just because the gate wiring line 185 is already connected to the gate of the transistor 104 does not mean that the gate wiring is connected to the source or drain of transistor 103 and Koyama discloses that source or drain of transistor 103 is connected to the connection wiring 184 and a gate wiring 185, col. 28, lines 1 – 5.

13. As to Applicant's argument that "connection wiring 184 (according to cross-section II) cannot be extended parallel to the gate wiring line 185," the Examiner respectfully disagrees. The Examiner generally agrees with applicants Cross-section II except for one important part, in order for layer 184 and 185 to be connected as shown by the applicant, layers 184 and 185 must overlap. There cannot be a connection between two layers unless the layers overlap so a via can be formed. Therefore, connection wiring 184 must be extended parallel to the gate wiring line 185 at least enough to form an interlayer connecting via.

14. As to Applicant's argument that "if the connection wiring line 184 were to extend towards the gate of the transistor 104, it should overlap with the gate wiring line 185. However, there is no indication in Figure 20 that the connection wiring line 184 overlaps with the gate wiring line 185 and the gate wiring line 185 alone is depicted as a line to connect the contact hole with the gate of the transistor 104," the Examiner respectfully disagrees. Below are figures 1, 2 and 3; figure 1 corresponds to fig. 20 showing the semiconductor film layers of transistors 103 and 104, figure 2 corresponds to fig. 20 showing the layer corresponding to the connection wiring 184 and fig. 3, corresponds to fig. 20 showing the layer corresponding to the gate wiring 185. As shown below in figures 2 and 3, the gate wiring 185 overlaps the connection wiring 184. The gate line 185 cannot be directly connected to the source or drain region of transistor 103, because as shown in fig. 20, the semiconductor film layers of transistors 103 ends before gate wiring 185 begins and therefore, gate wiring 185 and semiconductor film layers of transistors 103 do not overlap, connection wiring 184 serves as a bridge connecting semiconductor film layers of transistors 103 and gate wiring 185.

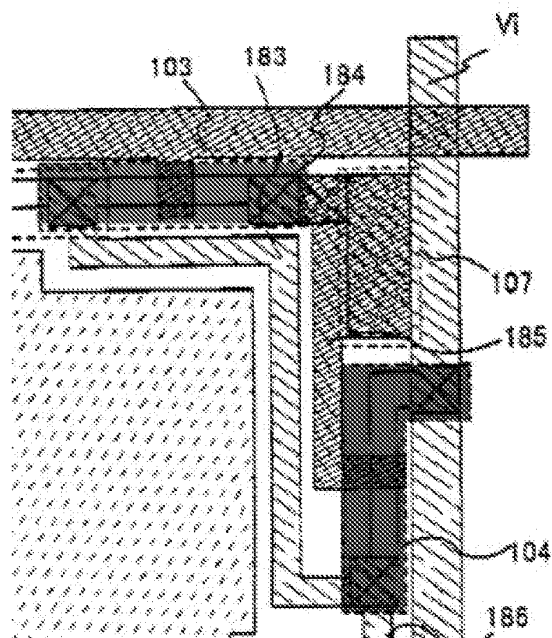


Figure 1

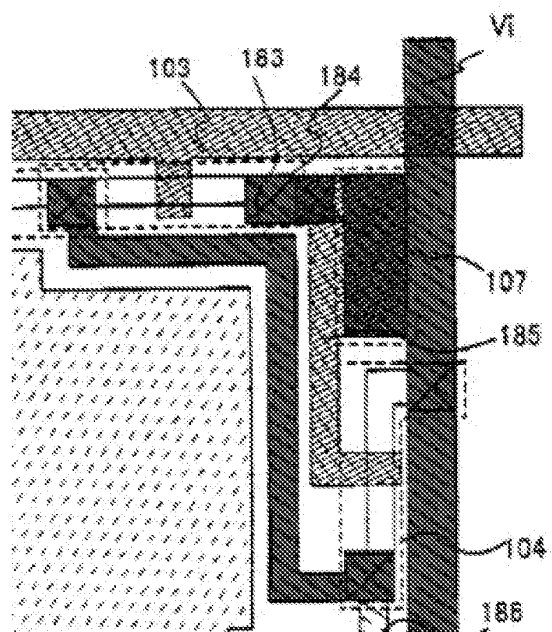


Figure 2

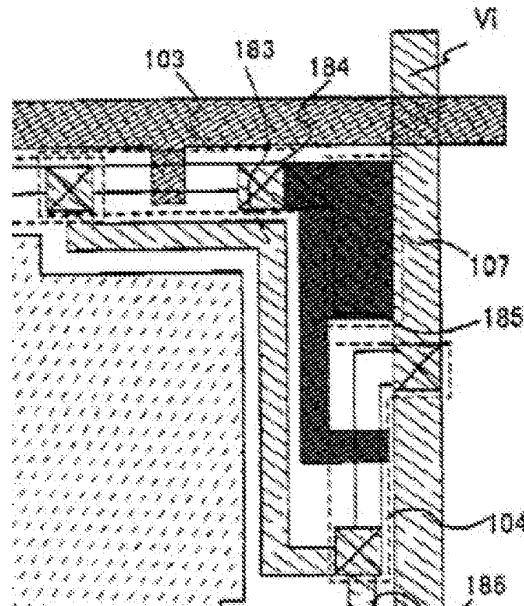


Figure 3

15. As to Applicant's argument that "Koyama fails to disclose "the wiring being formed in the layer different from a gate layer in which the gate of the first transistor is formed, and the wiring having a portion formed in the layer, the portion extending in a direction in which the data line extends," as recited in claims 1, 17 and 18," the Examiner respectfully disagrees. Koyama discloses the wiring 184 corresponding to 5059 of fig. 23A being formed in the layer corresponding to figure 2 above different from a gate layer of figure 3 above in which the gate 185 corresponding to element 5055 of fig. 23A of the first transistor 104 is formed. Koyama also discloses that the wiring 184 of fig. 20 having a portion formed in the layer, the portion extending in a direction in which the data line extends as shown in fig. 20, 184 extends in the direction of data line 190.

16. As to Applicant's argument that "Koyama fails to disclose ii) the wiring being formed in the layer different from a gate layer in which the gate of the first transistor is formed," as recited in claims 1, 17 and 18," the Examiner respectfully disagrees. Koyama discloses the wiring 184 of fig. 20 being formed in the layer corresponding to 5059 of fig. 23A and figure 2 above different from a gate layer corresponding to 5055 of fig. 23A and figure 3 above in which the gate 185 of the first transistor 104 is formed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DMITRIY BOLOTIN whose telephone number is (571)270-5873. The examiner can normally be reached on Monday-Friday, 7:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571)272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DMITRIY BOLOTIN/
Examiner, Art Unit 2695

Receipt date: 07/16/2012

12917885 - GAU: 2695

Modified Form PTO-1449 (REV. 5/11) PATENT & TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY DOCKET NO. 114251.03	APPLICATION NO. 12/917,885
	APPLICANT(S) Yojiro MATSUEDA	
	FILING DATE November 2, 2010	GROUP 2629

U.S. PATENT DOCUMENTS				
Examiner Initials	Cite No.	Document Number	Date	Name
	1	2005/0231122 A1	10/20/2005	Osame et al.
	2	7,483,001 B2	01/27/2009	Matsueda

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation

OTHER DOCUMENTS		
Examiner Initials	Cite No.	Including name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.

EXAMINER	/Dmitriy Bolotin/	DATE CONSIDERED 10/13/2012
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.		

Date: July 16, 2012 ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.B./

<i>Index of Claims</i> 	Application/Control No. 12917885	Applicant(s)/Patent Under Reexamination MATSUEDA, YOJIRO
	Examiner DMITRIY BOLOTIN	Art Unit 2629

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant
 ☐ CPA
 ☐ T.D.
 ☐ R.1.47

CLAIM		DATE							
Final	Original	01/28/2011	06/07/2011	10/25/2011	06/08/2012	10/13/2012			
	1	✓	✓	✓	✓	✓			
	2	✓	✓	✓	✓	✓			
	3	✓	✓	-	-	-			
	4	✓	✓	-	-	-			
	5	✓	✓	-	-	-			
	6	✓	✓	-	-	-			
	7	✓	✓	-	-	-			
	8	✓	✓	-	-	-			
	9	✓	✓	-	-	-			
	10	✓	✓	-	-	-			
	11			○	○	○			
	12			○	○	○			
	13			✓	✓	✓			
	14			✓	✓	✓			
	15			○	○	○			
	16			○	○	○			
	17				✓	✓			
	18				✓	✓			
	19				✓	✓			
	20				✓	✓			

<i>Search Notes</i> 	Application/Control No. 12917885	Applicant(s)/Patent Under Reexamination MATSUEDA, YOJIRO
	Examiner DMITRIY BOLOTIN	Art Unit 2629

SEARCHED			
Class	Subclass	Date	Examiner
345	76-83	1/28/2011	DB
315	169.1-169.4	1/28/2011	DB
	Updated Search	06/07/2011	DB
	Updated Search	10/25/2011	DB
349	42,43,46	10/25/2011	DB
	Updated Search	06/08/2012	DB
	Updated Search	10/13/2012	DB

SEARCH NOTES			
Search Notes		Date	Examiner
Google		1/28/2011	DB
EAST		1/28/2011	DB
Updated Search		06/07/2011	DB
Updated Search		10/25/2011	DB
Updated Search		06/08/2012	DB
Updated Search		10/13/2012	DB

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

/DMITRIY BOLOTIN/ Examiner.Art Unit 2695	
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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2695

Application No.: 12/917,885

Examiner: D. BOLOTIN

Filed: November 2, 2010

Docket No.: 114251.03

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND
ELECTRONIC DEVICE

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the October 18, 2012 Office Action, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

01/22/2013 LNGUYEN1 00000025 12917885
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250.00 OP

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An electro-optical device comprising:

a data line;

a control line; and

a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit including:

a first transistor that includes a first semiconductor film;

an electro-optical element electrically connected to one of a source or a drain of the first transistor;

a second transistor that includes a second semiconductor film, the second transistor connected between the one of the source or the drain and a gate of the first transistor;

a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor according to a data signal; and

a wiring connected between the second transistor and the gate of the first transistor,

the first transistor supplying a current based on the gate voltage to the electro-optical element,

the wiring being formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film are formed,

the wiring ~~being~~ having a portion formed in the layer different from a gate layer in which the gate of the first transistor is formed, ~~and~~ the portion crossing another wiring formed in the gate layer.

~~the wiring having a portion formed in the layer, the portion extending in a direction in which the data line extends.~~

2. (Previously Presented) The electro-optical device according to claim 1, wherein the first transistor has a conduction type different from a conduction film the second transistor has.

3-10. (Canceled)

11. (Previously Presented) The electro-optical device according to claim 1, wherein the control line supplies a control signal to a gate of the second transistor, the control line intersecting the wiring.

12. (Previously Presented) The electro-optical device according to claim 11, wherein the unit circuit further includes a third transistor coupled between the holding element and the data line, and

wherein the second transistor and the third transistor are controlled according to the control signal.

13. (Previously Presented) An electric device comprising an electro-optical device according to claim 1.

14. (Previously Presented) An electric device comprising an electro-optical device according to claim 2.

15. (Previously Presented) An electric device comprising an electro-optical device according to claim 11.

16. (Previously Presented) An electric device comprising an electro-optical device according to claim 12.

17. (Currently Amended) An electro-optical device comprising:

a data line;

a control line;

a power line; and

a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit including:

- a first transistor that includes a first semiconductor film;
- an electro-optical element electrically connected to one of a source or a drain of the first transistor;
- a second transistor that includes a second semiconductor film, the second transistor connected between the one of the source or the drain and a gate electrode of the first transistor;
- a holding element that is connected to the gate electrode of the first transistor and holds a gate voltage of the first transistor according to a data signal; and
- a wiring connected between the gate electrode of the first transistor and the second transistor,

the first transistor supplying a current based on the gate voltage to the electro-optical element,

the wiring being formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film are formed,

the wiring ~~being~~ having a portion formed in the layer different from a gate layer in which the gate electrode of the first transistor formed, ~~and~~ the portion crossing another wiring formed in the gate layer.

~~the wiring having a portion formed in the layer, the portion extending in a direction in which the data line extends.~~

18. (Currently Amended) An electro-optical device comprising:

- a data line;
- a control line;

a power line; and

a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit including:

- a first transistor that includes a first semiconductor film;
- an electro-optical element electrically connected to one of a source or a drain of the first transistor;
- a second transistor that includes a second semiconductor film, the second transistor connected between the one of a source or the drain and a gate electrode of the first transistor;
- a holding element that is connected to the gate electrode of the first transistor and holds a gate voltage of the first transistor according to a data signal; and
- a wiring connected between the gate electrode of the first transistor and the second transistor,

the first transistor supplying a current based on the gate voltage to the electro-optical element,

the wiring ~~being~~ having a portion formed in the layer in which the data line and the power line are formed, and the portion crossing another wiring formed in the gate layer.

~~the wiring having a portion formed in the layer, the portion extending in a direction in which the data line extends.~~

19. (Previously Presented) The electro-optical device according to claim 17,

wherein the first transistor has a first terminal, a second terminal, and a channel region disposed between the first terminal and the second terminal, the first terminal being disposed between the power line and the second terminal, and

the first transistor controlling an electrical connection between the first terminal and the second terminal.

20. (Previously Presented) The electro-optical device according to claim 18,
wherein the first transistor has a first terminal, a second terminal, and a
channel region disposed between the first terminal and the second terminal, the first terminal
being disposed between the power line and the second terminal, and
the first transistor controlling an electrical connection between the first terminal and
the second terminal.
21. (New) An electro-optical device comprising:
a data line;
a control line; and
a unit circuit arranged corresponding to an intersection of the data line and the
control line, the unit circuit including:
a first transistor that includes a first semiconductor film;
an electro-optical element electrically connected to one of a source or a
drain of the first transistor;
a second transistor that includes a second semiconductor film, the
second transistor connected between the one of the source or the drain and a gate of the first
transistor;
a holding element that is connected to the gate of the first transistor
and holds a gate voltage of the first transistor according to a data signal; and
a wiring connected between the second transistor and the gate of the
first transistor,
the first transistor supplying a current based on the gate voltage to the electro-
optical element,
the wiring being formed in a layer which is different from a layer in which the
first semiconductor film and the second semiconductor film are formed,

the wiring having a portion formed in the layer different from a gate layer in which the gate of the first transistor is formed, the portion crossing the control line.

REMARKS

Claims 1, 2 and 11-21 are pending in this application. By this Amendment, claims 1, 17 and 18 are amended. Claim 21 is added. Support for the amendments may be found in at least Figs. 2, 8 and 10. No new matter is added. Applicant respectfully requests reconsideration and prompt allowance of the pending claims at least in light of the following remarks.

I. Allowable Claims

Applicant gratefully acknowledges the Office Action's indication that claims 11, 12, 15 and 16 recite allowable subject matter.

II. 35 U.S.C. §102(e) Rejection

Claims 1, 2, 13, 14 and 17-20 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 7,277,070 (Koyama). Applicant respectfully traverses the rejection.

A. Claims 1 and 17

Koyama fails to disclose "a wiring connected between the second transistor and the gate of the first transistor...the wiring having a portion formed in the layer different from a gate layer in which the gate of the first transistor is formed, the portion crossing another wiring formed in the gate layer," as recited in claims 1 and 17 for the following three reasons.

First, Koyama fails to disclose a wiring that connects between the second transistor and the gate of the first transistor, and has a portion formed in the layer different from a gate layer in which the gate of the first transistor is formed. The Office Action asserts a wiring 184 and a gate wiring line 185, of Koyama, correspond to the claimed wiring and the gate of the first transistor, respectively. The Office Action also asserts Fig. 20 and column 27, line 60-column 28, line 20, of Koyama disclose this feature (Office Action on page 4). This assertion is unreasonable. Koyama discloses that a second switching TFT 103 has a source

region and a drain region one of which is connected to a drain region of the current controlling TFT 104 through a connection wiring line 183 and the other of which is connected to a connection wiring line 184 and to a gate wiring line 185 (see, column 27, line 65-column 28, line 2). However, the asserted section of Koyama is silent about layers where the wiring 184 (i.e., the asserted claimed wiring) and the gate wiring line 185 (i.e., the asserted claimed gate of the first transistor) are formed (see also Fig. 20). Specifically, Koyama fails to disclose that the wiring 184 is formed in a layer which is different from a layer the gate wiring line 185 is formed. Thus, Koyama fails to disclose i) a wiring that connects between the second transistor and the gate of the first transistor the wiring and has a portion formed in the layer different from a gate layer in which the gate of the first transistor is formed.

Further, Koyama fails to inherently disclose this feature. To establish inherency, it must be clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill (MPEP §2112). Inherency may not be established by probabilities or possibilities (*Id.*). The mere fact that a certain thing may result from a given set of circumstances is not sufficient (*Id.*). In the present case, as discussed above, Koyama is silent about layers where the wiring 184 and the gate wiring line 185 are formed. Further, the Examiner does not provide any extrinsic evidence proving that the above feature is necessarily present in Koyama. Because the Examiner does not provide the extrinsic evidence that must make clear that the above feature is necessary present (i.e., the wiring 184 is formed in a layer which is different from a layer the gate wiring line 185 is formed), Koyama does not inherently disclose the above feature. Thus, Koyama fails to disclose the above feature.

Second, Koyama fails to disclose that the portion of the wiring crosses another wiring formed in the gate layer. As shown in Fig. 20, Koyama fails to disclose that the connection

wiring line 184 has a portion that crosses another wiring formed in a gate layer (i.e., a layer where the gate wiring line 185 is formed) (see Fig. 20). Further, as discussed above, Koyama is silent about a layer where the gate wiring line 185 is formed. Thus, Koyama fails to disclose ii) the portion of the wiring which crosses another wiring formed in the gate layer.

Third, Applicant stresses that it is improper for the Office Action's continued reliance on Fig. 20 of Koyama for the claimed feature. Fig. 20 of Koyama is a top view of a pixel of a light emitting device. However, Fig. 20 does not clearly show how the connection wiring line 184 is connected. For example, the Office Action asserts that the connection wiring line 184 is connected to the source or drain of TFT103 at an "X" (the Office Action on page 9). However, this is mere a conclusive statement without factual support (i.e., the specification does not disclose that the connection wiring line 184 is connected to the source or drain of TFT103 through an "X"). It is improper for the Patent Office to rely on a drawing of the cited reference if the drawing is not clearly described as disclosing the claimed feature. "A drawing can be used as prior art and anticipate claim only if the drawing clearly shows the structure which is claimed." *In re Mraz*, 455 F.2d 1069, 173 USPQ 25 (CCPA 1972); MPEP §2125. Thus, it is improper that the Office Action relies on Fig. 20 of Koyama for the above features.

B. Claim 18

Similar to the above, analysis, Koyama fails to disclose "a wiring connected between the gate electrode of the first transistor and the second transistor...the wiring having a portion formed in the layer in which the data line and the power line are formed, the portion crossing a line formed in the gate layer," as recited in claim 18. In addition, Koyama fails to disclose that the connection wiring line 184 has a portion formed in a layer in which a data line and a power line are formed (see Fig. 20).

C. Conclusion

Thus, claims 1, 17 and 18 are patentable over Koyama. Further, claims 2, 13, 14, 19 and 20 are patentable for at least the same reasons as claims 1, 17 and 18, as well as for the additional features they recite. Applicant respectfully requests withdrawal of the rejection.

III. New Claim

Similar to the above analysis, Koyama fails to disclose "a wiring connected between the second transistor and the gate of the first transistor...the wiring having a portion formed in the layer different from a gate layer in which the gate of the first transistor is formed, the portion crossing the control line," as recited in claim 21. In addition, Koyama fails to disclose that the connection wiring line 184 has a portion that crosses a control line (see Fig. 20). Thus, claim 21 is patentable over Koyama.

* * * * *

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

Hirotsuna Yamashita
Registration No. L0563

JAO:HQY/sxl

Attachment:
Amendment Transmittal

Date: January 18, 2013

OLIFF & BERRIDGE, PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

<p>DEPOSIT ACCOUNT USE AUTHORIZATION Please grant any extension necessary for entry of this filing; Charge any fee due to our Deposit Account No. 15-0461</p>



OLIFF & BERRIDGE, PLC
Telephone: (703) 836-6400
Facsimile: (703) 836-2787

PATENT APPLICATION

Attorney Docket No.: 114251.03

CUSTOMER NUMBER 25944

In re the Application of

Yojiro MATSUEDA

Application No.: 12/917,885

Filed: November 2, 2010

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is an Amendment in the above-identified application.

- ☐ Entitlement to small entity status is hereby asserted.
☐ Small entity status of this application has been established.

Any additional claim fees have been calculated as shown below:

	(Column 1)	(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA
TOTAL CLAIMS	*13 MINUS	**20	=0
INDEP CLAIMS	*4 MINUS	***3	=1
☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM			

SMALL ENTITY	
RATE	ADD'L FEE
x 31	\$
x 125	\$
+ 230	\$
	\$

OTHER THAN A SMALL ENTITY	
RATE	ADD'L FEE
x 62	\$
x 250	\$250.00
+ 460	\$
	\$250.00

* If the entry in Column 1 is less than the entry in Column 2, write "0" in Column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space.

The "Highest Number Previously Paid For" in this space (Total or Independent) is the highest number found from the equivalent box in Column 1 of a prior Amendment or the number of claims originally filed.

- ☒ Check No. 250014 in the amount of \$250.00 is attached. The Commissioner is hereby authorized to charge any other fees that may be required to complete this filing, or to credit any overpayment, to Deposit Account No. 15-0461.

Respectfully submitted,

H. Yamashita

James A. Oliff
Registration No. 27,075

Hirotsuna Yamashita
Registration No. L0563

JAO:HQY/sxl

Date: January 18, 2013

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/917,885		Filing Date 11/02/2010		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.										
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	01/18/2013	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 13	Minus	** 20	= 0	X \$ =		OR	X \$62=	0
	Independent (37 CFR 1.16(h))	* 4	Minus	*** 3	= 1	X \$ =		OR	X \$250=	250
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE	OR	TOTAL ADD'L FEE	250	
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =	
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE	OR	TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.										
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".										
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".										
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
/ROSALIND BALL/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/917,885	11/02/2010	Yojiro MATSUEDA	114251.03	2374

25944	7590	02/13/2013
OLIFF & BERRIDGE, PLC		
P.O. BOX 320850		
ALEXANDRIA, VA 22320-4850		

EXAMINER	
BOLOTIN, DMITRIY	

ART UNIT	PAPER NUMBER
2695	

NOTIFICATION DATE	DELIVERY MODE
02/13/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

OfficeAction25944@oliff.com
jarmstrong@oliff.com

Office Action Summary	Application No.	Applicant(s)	
	12/917,885	MATSUEDA, YOJIRO	
	Examiner	Art Unit	
	DMITRIY BOLOTIN	2695	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 18 January 2013.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5) ☒ Claim(s) 1,2 and 11-21 is/are pending in the application.

5a) Of the above claim(s) ____ is/are withdrawn from consideration.

6) ☒ Claim(s) 21 is/are allowed.

7) ☒ Claim(s) 1,2,13,14 and 17-20 is/are rejected.

8) ☒ Claim(s) 11,12,15 and 16 is/are objected to.

9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10) ☐ The specification is objected to by the Examiner.

11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. ____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date ____.

3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.

4) ☐ Other: ____.

DETAILED ACTION

It would be of great assistance to the Office if all incoming papers pertaining to a filed application carried the following items:

1. Application number (checked for accuracy, including series code and serial no.).
2. Group art unit number (copied from most recent Office communication).
3. Filing date.
4. Name of the examiner who prepared the most recent Office action.
5. Title of invention.
6. Confirmation number (See MPEP § 503).

Status of Claims

1. **Claims 1, 17 and 18** have been amended, **claims 3 – 10** have been canceled, new **claim 21** has been added; and **claims 1, 2 and 11 – 21** are pending.

Terminal Disclaimer

2. The terminal disclaimer filed on 05/09/2011 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 7,483,001 has been reviewed and is approved.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1, 2, 13, 14 and 17 – 20** are rejected under 35 U.S.C. 102(e) as being anticipated by Koyama (US 7,277,070).

As to **claim 1**, Koyama discloses an electro-optical device comprising: a data line (signal line Si comprising wiring 190 supplying signal to transistor 102 of fig. 20); a control line (gate signal line Gaj of fig. 20); and a unit circuit arranged corresponding to an intersection of the data line and the control line (fig. 20), the unit circuit including: a first transistor (transistor 104 of fig. 20) that includes a first semiconductor film (semiconductor film 5005 of fig. 21A); an electro-optical element (pixel electrode 181 of fig. 20) electrically connected to one of a source or a drain of the first transistor (181 is electrically connected to 104 through transistor 105 of fig. 20); a second transistor (transistor 103 of fig. 20) that includes a second semiconductor film (semiconductor film 5004 of fig. 21A), the second transistor connected between the one of the source or the drain and a gate of the first transistor (transistor 103 of fig. 20); and a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor according to a data signal (capacitor 107 of fig. 20), and

a wiring (184 of fig. 20) connected between the second transistor (103 of fig. 20) and the gate of the first transistor (104 of fig. 20); and the first transistor supplying a current based on the gate voltage (TFT 104 is current controlling TFT (col. 27, line 60 –

col. 28, line 20), inherently, TFT 104 is on based on voltage at the gate, inducing current through OLED) to the electro-optical element (181 of fig. 22),

the wiring being formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film are formed (as shown in fig. 20, the wiring is not in semiconductor areas of either TFT 103 or TFT 104, the wiring is formed in layer 5059 of figs. 22 and 23);

the wiring having a portion formed in the layer different from a gate layer in which the gate of the first transistor is formed (as shown in fig. 20, the wiring 184 and gate layer 185 are in different layers (col. 27, line 60 – col. 28, line 20)), and the portion (wiring 184 of fig. 20) crossing another wiring formed in the gate layer (as shown in fig. 20 (corresponding to Figure 1 bellow), the wiring 184 crosses gate wiring 185 to form a junction such that wiring 184 and 185 may be connected: “the other of which [drain or source] is connected to a connection wiring line 184 and to a gate wiring line 185”, col. 27, line 60 – col. 28, line 20. It is absolutely necessary when connecting two wirings disposed in two different layers to overlap and since 184 and 185 are connected they necessarily overlap).

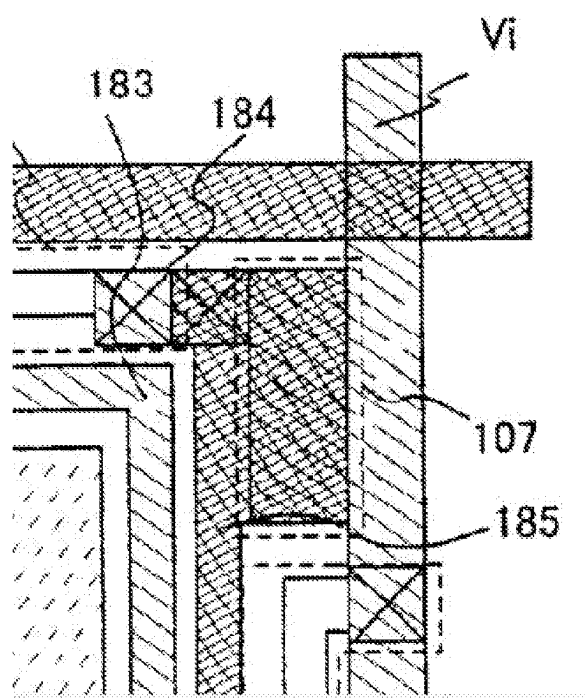


Figure 1

As to **claim 2** (dependent on 1), Koyama discloses the electro-optical device, wherein the first transistor has a conduction type different from a conduction film the second transistor has (second switching transistor TFT 103 may be n-channel and current controlling TFT may be p-channel, col. 9, lines 45 – 50).

As to **claim 13** (dependent on 1) and **claim 14** (dependent on 2), Koyama discloses an electric device comprising an electro-optic device (television of fig. 24A).

As to **claim 17**, Koyama discloses an electro-optical device comprising: a data line (signal line Si comprising wiring 190 supplying signal to transistor 102 of fig. 20); a control line (gate signal line Gaj of fig. 20); a power line (power line Vi of fig. 20); and a

unit circuit arranged corresponding to an intersection of the data line and the control line (fig. 20), the malt circuit including: a first transistor (transistor 104 of fig. 20) that includes a first semiconductor film (semiconductor film 5005 of fig. 21A); an electro-optical element (pixel electrode 181 of fig. 20) electrically connected to one of a source or a drain of the first transistor (181 is electrically connected to 104 through transistor 105 of fig. 20); a second transistor (transistor 103 of fig. 20) that includes a second semiconductor film (semiconductor film 5004 of fig. 21A), the second transistor connected between the one of the source or the drain and a gate electrode of the first transistor (transistor 104 of fig. 20); a holding element that is connected to the gate electrode of the first transistor and holds a gate voltage of the first transistor according to a data signal (capacitor 107 of fig. 20); and a wiring connected between the gate electrode of the first transistor and the second transistor (184 of fig. 20), the first transistor supplying a current, based on the gate voltage to the electro-optical element (TFT 104 is current controlling TFT (col. 27, line 60 – col. 28, line 20), inherently, TFT 104 is on based on voltage at the gate, inducing current through OLED), the wiring being formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film are formed (as shown in fig. 20, the wiring is not in semiconductor areas of either TFT 103 or TFT 104, the wiring is formed in layer 5059 of figs. 22 and 23), the wiring having a portion formed in the layer different from a gate layer in which the gate electrode of the first transistor formed (as shown in fig. 20, the wiring 184 and gate layer 185 are in different layers (col. 27, line 60 – col. 28, line 20)), and the portion (wiring 184 of fig. 20) crossing another wiring formed in the gate layer

(as shown in fig. 20 (corresponding to Figure 2 bellow), the wiring 184 crosses gate wiring 185 to form a junction such that wiring 184 and 185 may be connected: "the other of which [drain or source] is connected to a connection wiring line 184 and to a gate wiring line 185", col. 27, line 60 – col. 28, line 20. It is absolutely necessary when connecting two wirings disposed in two different layers to overlap and since 184 and 185 are connected they necessarily overlap).

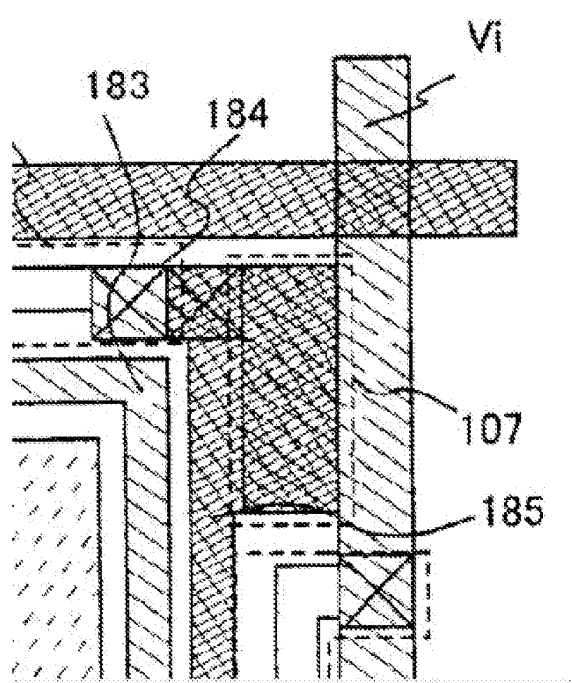


Figure 2

As to **claim 18**, Koyama discloses an electro-optical device comprising: a data line (signal line Si comprising wiring 190 supplying signal to transistor 102 of fig. 20); a control line (gate signal line Gaj of fig. 20); a power line (power line Vi of fig. 20); and a

unit circuit arranged corresponding to an intersection of the data line and the control line (fig. 20), the unit circuit including: a first transistor (transistor 104 of fig. 20) that includes a first semiconductor film (semiconductor film 5005 of fig. 21A); an electro-optical element (pixel electrode 181 of fig. 20) electrically connected to one of a source or a drain of the first transistor (181 is electrically connected to 104 through transistor 105 of fig. 20); a second transistor (transistor 103 of fig. 20) that includes a second semiconductor film (semiconductor film 5004 of fig. 21A), the second transistor connected between the one of a source or the drain and a gate electrode of the first transistor (transistor 104 of fig. 20); a holding element that is connected to the gate electrode of the first transistor and holds a gate voltage of the first transistor according to a data signal (capacitor 107 of fig. 20); and a wiring connected between the gate electrode of the first transistor and the second transistor (184 of fig. 20), the first transistor supplying a current based on the gate voltage to the electro-optical element (TFT 104 is current controlling TFT (col. 27, line 60 – col. 28, line 20), inherently, TFT 104 is on based on voltage at the gate, inducing current through OLED), the wiring having a portion (184 of fig. 20) formed in the layer in which the data line (182 of fig. 20) and the power line (Vi of fig. 20) are formed, the portion (wiring 184 of fig. 20) crossing another wiring formed in the gate layer (as shown in fig. 20 (corresponding to Figure 3 bellow), the wiring 184 crosses gate wiring 185 to form a junction such that wiring 184 and 185 may be connected: “the other of which [drain or source] is connected to a connection wiring line 184 and to a gate wiring line 185”, col. 27, line 60 – col. 28, line

20. It is absolutely necessary when connecting two wirings disposed in two different layers to overlap and since 184 and 185 are connected they necessarily overlap).

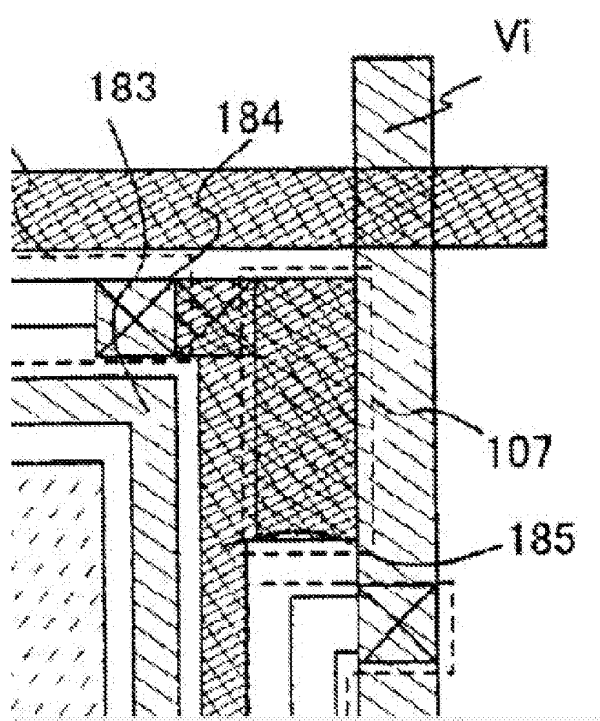


Figure 3

As to **claim 19** (dependent on 17), Koyama discloses the electro-optical device, wherein the first transistor (104 of fig. 20) has a first terminal and a second terminal (source and drain shown in fig. 20), and a channel region disposed between the first terminal and the second terminal (channel region of 104 of fig. 20 corresponding to layer 5005 of fig. 21A), the first terminal (terminal connected to Vi of fig. 20) being disposed between the power line (Vi of fig. 20) and the second terminal (terminal connected to 186 of fig. 20), and the first transistor controlling an electrical connection

between the first terminal and the second terminal (via gate 185 of fig. 21).

As to **claim 20** (dependent on 18), Koyama discloses the electro-optical device, wherein the first transistor (104 of fig. 20) has a first terminal, a second terminal (source and drain shown in fig. 20), and a channel region disposed between the first terminal and the second terminal (channel region of 104 of fig. 20 corresponding to layer 5005 of fig. 21A), the first terminal (terminal connected to Vi of fig. 20) being disposed between the power line (Vi of fig. 20) and the second terminal (terminal connected to 186 of fig. 20), and the first transistor controlling an electrical connection between the first terminal and the second terminal (via gate 185 of fig. 21).

Allowable Subject Matter

5. **Claims 11, 12, 15 and 16** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

The Prior Art of record discloses the electro-optical device wherein the control line (gate line Gaj of fig. 20) supplies a control signal to a gate of the second transistor (103 of fig. 20), but fails to disclose that “*the control line intersecting the wiring*”.

7. **Claim 21** is allowed.

8. The following is an examiner's statement of reasons for allowance: Koyama discloses electro-optical device as claimed in claim 21, but does not disclose that a wiring connecting the second transistor and the gate of the first transistor comprises a portion formed in a layer other than semiconductor layer or the gate layer of the first transistor, and said portion crossing the control line of the electro-optical device.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

9. Applicant's arguments filed 01/18/2013 have been fully considered but they are not persuasive.

10. As to Applicant's argument that Koyama fails to disclose "a wiring connected between the second transistor and the gate of the first transistor...the wiring having a portion formed in the layer different from a gate layer in which the gate of the first transistor is formed, the portion crossing the wiring formed in the gate layer," the Examiner respectfully disagrees. Koyama discloses a wiring 184 of fig. 20 connected between the second transistor 103 of fig. 20 and the gate 185 of fig. 20 of the first

transistor 104 of fig. 20. In particular, Koyama discloses a wiring (184 of fig. 20) connected between the gate electrode of the first transistor (185 of fig. 20) and the second transistor (103 of fig. 20), the wiring having a portion (184 of fig. 20) formed in the layer different from a gate layer (185 of fig. 20) in which the gate of the first transistor is formed, the portion (wiring 184 of fig. 20) crossing another wiring formed in the gate layer (as shown in fig. 20 (corresponding to Figure 4 bellow), the wiring 184 crosses gate wiring 185 to form a junction such that wiring 184 and 185 may be connected. As stated by Koyama: "the other of which [drain or source] is connected to a connection wiring line 184 and to a gate wiring line 185", col. 27, line 60 – col. 28, line 20. Specially, as shown in fig. 23A, the only connection to the transistor 103 is the wiring 5059 which does not correspond to the gate layer, therefore, it is absolutely necessary when connecting two wirings disposed in two different layers to overlap and since 184 and 185 are connected they necessarily overlap).

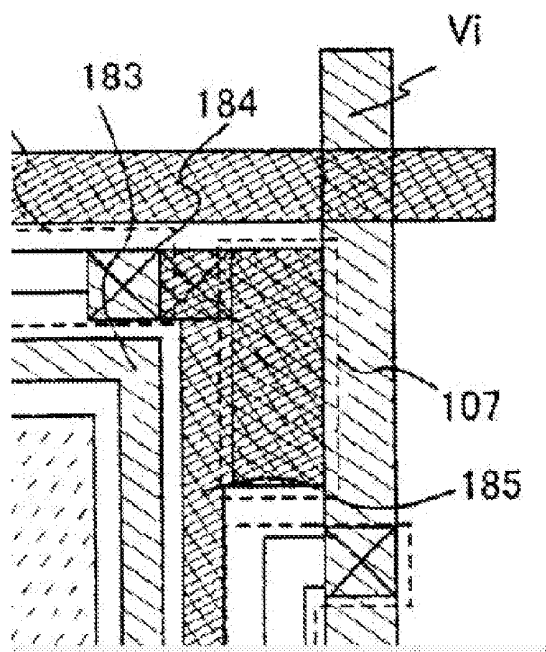


Figure 4

11. As to Applicant's argument that Koyama fails to disclose "Koyama fails to disclose a wiring that connects the second transistor and the gate of the first transistor, and has a portion formed in a layer different from a gate layer in which the gate of the first transistor is formed," the Examiner respectfully disagrees. Koyama discloses a wiring (184 of fig. 20, corresponding to 5059 of fig. 23A) that connects the second transistor (103 of fig. 20) and the gate of the first transistor (185 of fig. 20), and has a portion formed in a layer different from a gate layer in which the gate of the first transistor is formed (as shown in fig. 20 and 23A, the wiring 184 is formed in a layer other than the gate layer of the first transistor).

12. As to Applicant's argument that: "the Examiner does not provide any extrinsic evidence proving that the above features are necessarily present," the Examiner respectfully disagrees. No extrinsic evidence is necessary since all of the evidence may be found in the Koyama reference. Koyama discloses that second transistor 103 is connected to the wiring 184 and gate line 185 (col. 28, lines 1 - 5), further Koyama discloses that the only thing connected to the source/drain of the second transistor are wiring 5058 and wiring 5059 of fig. 23A which as shown in the figure 23A are not formed of a gate layer of any of the transistors. Therefore, in order to establish connection between transistor 103 and the gate wiring 185 (col. 28, lines 1 - 5), as shown in fig. 20, the wirings 184 and 185 must overlap and that is shown in fig. 20.

13. As to Applicant's argument that Koyama fails to disclose that the connection wiring line 184 is connected between the second switching transistor TFT 103 and the gate of current controlling TFT 104, the Examiner respectfully disagrees. Koyama discloses that source or drain of transistor 103 is connected to the connection wiring 184 and a gate wiring 185, col. 28, lines 1 - 5, as shown in fig. 20, the gate wiring 185 is not directly connected to the source or drain of transistor 103 (this can also be seen from fig. 23A, where the gate of current controlling TFT 5055 is not directly connected to the source or drain of the second switching TFT, but instead the source or drain of the second switching TFT is connected to connection wiring 5059). Therefore Koyama discloses that the connection wiring line 184 is connected between the second switching transistor TFT 103 and the gate 185 of current controlling TFT 104.

14. As to Applicant's argument that "because the gate wiring line 185 is already connected to the gate of the transistor 104, there is no need for the connection wiring line 184 to be further connected to the gate of the transistor 104," the Examiner respectfully disagrees. Just because the gate wiring line 185 is already connected to the gate of the transistor 104 does not mean that the gate wiring is connected to the source or drain of transistor 103 and Koyama discloses that source or drain of transistor 103 is connected to the connection wiring 184 and a gate wiring 185, col. 28, lines 1 – 5.

15. As to Applicant's argument that "connection wiring 184 (according to cross-section II) cannot be extended parallel to the gate wiring line 185," the Examiner respectfully disagrees. The Examiner generally agrees with applicants Cross-section II except for one important part, in order for layer 184 and 185 to be connected as shown by the applicant, layers 184 and 185 must overlap. There cannot be a connection between two layers unless the layers overlap so a via can be formed. Therefore, connection wiring 184 must be extended parallel to the gate wiring line 185 at least enough to form an interlayer connecting via.

16. As to Applicant's argument that "if the connection wiring line 184 were to extend towards the gate of the transistor 104, it should overlap with the gate wiring line 185. However, there is no indication in Figure 20 that the connection wiring line 184 overlaps with the gate wiring line 185 and the gate wiring line 185 alone is depicted as a line to connect the contact hole with the gate of the transistor 104," the Examiner respectfully disagrees. Below are figures 5, 6 and 7; figure 5 corresponds to fig. 20 showing the semiconductor film layers of transistors 103 and 104, figure 6 corresponds to fig. 20

showing the layer corresponding to the connection wiring 184 and fig. 7, corresponds to fig. 20 showing the layer corresponding to the gate wiring 185. As shown below in figures 2 and 3, the gate wiring 185 overlaps the connection wiring 184. The gate line 185 cannot be directly connected to the source or drain region of transistor 103, because as shown in fig. 20, the semiconductor film layers of transistors 103 ends before gate wiring 185 begins and therefore, gate wiring 185 and semiconductor film layers of transistors 103 do not overlap, connection wiring 184 serves as a bridge connecting semiconductor film layers of transistors 103 and gate wiring 185.

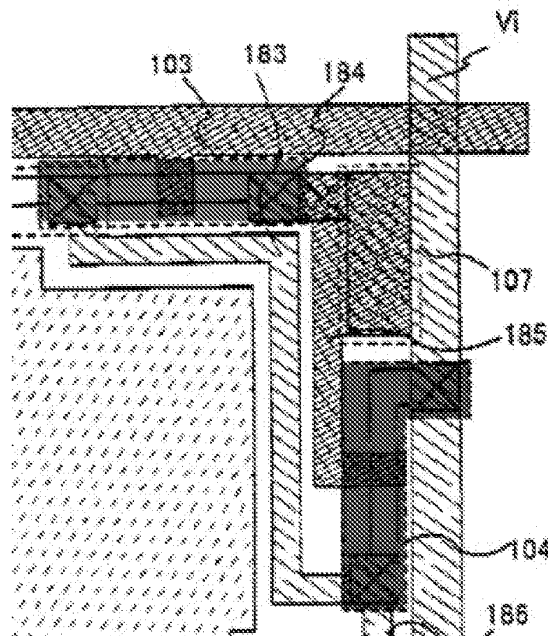


Figure 5

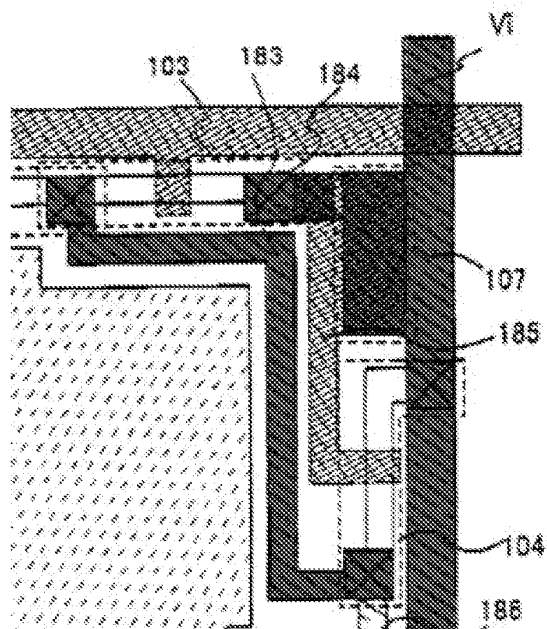


Figure 6

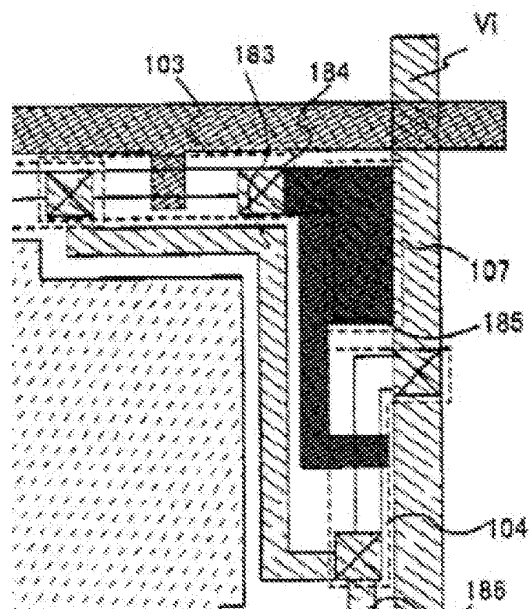


Figure 7

17. As to Applicant's argument that "Koyama fails to disclose "the wiring being formed in the layer different from a gate layer in which the gate of the first transistor is formed, and the wiring having a portion formed in the layer, the portion extending in a direction in which the data line extends," as recited in claims 1, 17 and 18," the Examiner respectfully disagrees. Koyama discloses the wiring 184 corresponding to 5059 of fig. 23A being formed in the layer corresponding to figure 6 above different from a gate layer of figure 7 above in which the gate 185 corresponding to element 5055 of fig. 23A of the first transistor 104 is formed. Koyama also discloses that the wiring 184 of fig. 20 having a portion formed in the layer, the portion extending in a direction in which the data line extends as shown in fig. 20, 184 extends in the direction of data line 190.

18. As to Applicant's argument that "Koyama fails to disclose ii) the wiring being formed in the layer different from a gate layer in which the gate of the first transistor is formed," as recited in claims 1, 17 and 18," the Examiner respectfully disagrees. Koyama discloses the wiring 184 of fig. 20 being formed in the layer corresponding to 5059 of fig. 23A and figure 6 above different from a gate layer corresponding to 5055 of fig. 23A and figure 7 above in which the gate 185 of the first transistor 104 is formed.

19. As to Applicant's arguments that: "Koyama fails to disclose that the portion of the wiring crosses another wiring formed in the gate layer," the examiner respectfully disagrees. As shown in fig. 20 and explained in the remarks above, the wirings 184 of fig. 20 and 185 overlap so they may be connected by a via, therefore portion of the

wiring 184 of fig. 20 crosses another wiring 185 of fig. 20 formed in the gate layer of the first transistor.

20. As to Applicant's argument that figure 20 of Koyama does not clearly show how the connection wiring line 184 is connected, the Examiner respectfully disagrees. First, Koyama discloses that source or drain of transistor 103 is connected to the connection wiring 184 and a gate wiring 185, col. 28, lines 1 - 5, therefore connection wiring 184 and a gate wiring 185 are indeed connected to each other. Second, as can be seen from fig. 20, connection wiring 184 is connected to the source or drain of TFT 103 through a via represented by "X" (the profile can be seen from fig. 23A, where connection wiring 184 is represented by element 5059) and connection wiring 184 is extended to be connected to gate wiring 185 that another via represented by "X". Therefore, Koyama clearly show how the connection wiring line 184 is connected.

Conclusion

21. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DMITRIY BOLOTIN whose telephone number is (571)270-5873. The examiner can normally be reached on Monday-Friday, 7:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571)272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DMITRIY BOLOTIN/
Examiner, Art Unit 2695

Application/Control Number: 12/917,885
Art Unit: 2695

Page 21

<i>Index of Claims</i> 	Application/Control No. 12917885	Applicant(s)/Patent Under Reexamination MATSUEDA, YOJIRO
	Examiner DMITRIY BOLOTIN	Art Unit 2629

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47				
CLAIM		DATE								
Final	Original	01/28/2011	06/07/2011	10/25/2011	06/08/2012	10/13/2012	02/07/2013			
	1	✓	✓	✓	✓	✓	✓			
	2	✓	✓	✓	✓	✓	✓			
	3	✓	✓	-	-	-	-			
	4	✓	✓	-	-	-	-			
	5	✓	✓	-	-	-	-			
	6	✓	✓	-	-	-	-			
	7	✓	✓	-	-	-	-			
	8	✓	✓	-	-	-	-			
	9	✓	✓	-	-	-	-			
	10	✓	✓	-	-	-	-			
	11			○	○	○	○			
	12			○	○	○	○			
	13			✓	✓	✓	✓			
	14			✓	✓	✓	✓			
	15			○	○	○	○			
	16			○	○	○	○			
	17				✓	✓	✓			
	18				✓	✓	✓			
	19				✓	✓	✓			
	20				✓	✓	✓			
	21						=			

Search Notes 	Application/Control No. 12917885	Applicant(s)/Patent Under Reexamination MATSUEDA, YOJIRO
	Examiner DMITRIY BOLOTIN	Art Unit 2629

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
345	76-83	1/28/2011	DB
315	169.1-169.4	1/28/2011	DB
	Updated Search	06/07/2011	DB
	Updated Search	10/25/2011	DB
349	42,43,46	10/25/2011	DB
	Updated Search	06/08/2012	DB
	Updated Search	10/13/2012	DB
	Updated Search	02/07/2013	DB

SEARCH NOTES		
Search Notes	Date	Examiner
Google	1/28/2011	DB
EAST	1/28/2011	DB
Updated Search	06/07/2011	DB
Updated Search	10/25/2011	DB
Updated Search	06/08/2012	DB
Updated Search	10/13/2012	DB
Updated Search	02/07/2013	DB

INTERFERENCE SEARCH

/DMITRIY BOLOTIN/ Examiner.Art Unit 2695	
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US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/DMITRIY BOLOTIN/
Examiner.Art Unit 2695

PATENT APPLICATION

**RESPONSE UNDER 37 CFR §1.116
EXPEDITED PROCEDURE
TECHNOLOGY CENTER ART UNIT 2695**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yojiro MATSUEDA

Group Art Unit: 2695

Application No.: 12/917,885

Examiner: D. BOLOTIN

Filed: November 2, 2010

Docket No.: 114251.03

For: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND
ELECTRONIC DEVICE

AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR §1.116

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the February 13, 2013 Office Action, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Canceled)
2. (Currently Amended) The electro-optical device according to ~~claim 1~~claim 21, wherein the first transistor has a conduction type different from a conduction ~~film~~type the second transistor has.
- 3-10. (Canceled)
11. (Currently Amended) The electro-optical device according to ~~claim 1~~claim 21, wherein the control line supplies a control signal to a gate of the second transistor, ~~the control line intersecting the wiring.~~
12. (Previously Presented) The electro-optical device according to claim 11, wherein the unit circuit further includes a third transistor coupled between the holding element and the data line, and wherein the second transistor and the third transistor are controlled according to the control signal.
13. (Currently Amended) An electric device comprising an electro-optical device according to ~~claim 1~~claim 21.
14. (Previously Presented) An electric device comprising an electro-optical device according to claim 2.
15. (Previously Presented) An electric device comprising an electro-optical device according to claim 11.
16. (Previously Presented) An electric device comprising an electro-optical device according to claim 12.
17. (Canceled)

18. (Currently Amended) ~~An~~The electro-optical device according to claim 21,
further comprising:comprising a power line, the power line being formed in a layer in which
the data line and the wiring are formed.

- ~~_____~~ a data line;
- ~~_____~~ a control line;
- ~~_____~~ a power line; and
- ~~_____~~ a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit including:
 - ~~_____~~ a first transistor that includes a first semiconductor film;
 - ~~_____~~ an electro-optical element electrically connected to one of a source or a drain of the first transistor;
 - ~~_____~~ a second transistor that includes a second semiconductor film, the second transistor connected between the one of a source or the drain and a gate electrode of the first transistor;
 - ~~_____~~ a holding element that is connected to the gate electrode of the first transistor and holds a gate voltage of the first transistor according to a data signal; and
 - ~~_____~~ a wiring connected between the gate electrode of the first transistor and the second transistor;
 - ~~_____~~ the first transistor supplying a current based on the gate voltage to the electro-optical element;
 - ~~_____~~ the wiring having a portion formed in the layer in which the data line and the power line are formed, the portion crossing another wiring formed in the gate layer.

19. (Currently Amended) The electro-optical device according to ~~claim 17~~claim 18,

wherein the first transistor has a first terminal, a second terminal, and a channel region disposed between the first terminal and the second terminal, the first terminal being disposed between the power line and the second terminal, and the first transistor controlling an electrical connection between the first terminal and the second terminal.

20. (Previously Presented) The electro-optical device according to claim 18, wherein the first transistor has a first terminal, a second terminal, and a channel region disposed between the first terminal and the second terminal, the first terminal being disposed between the power line and the second terminal, and the first transistor controlling an electrical connection between the first terminal and the second terminal.

21. (Previously Presented) An electro-optical device comprising:
a data line;
a control line; and
a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit including:
a first transistor that includes a first semiconductor film;
an electro-optical element electrically connected to one of a source or a drain of the first transistor;
a second transistor that includes a second semiconductor film, the second transistor connected between the one of the source or the drain and a gate of the first transistor;
a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor according to a data signal; and

a wiring connected between the second transistor and the gate of the first transistor,

the first transistor supplying a current based on the gate voltage to the electro-optical element,

the wiring being formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film are formed,

the wiring having a portion formed in the layer different from a gate layer in which the gate of the first transistor is formed, the portion crossing the control line.

REMARKS

Claims 2, 11-16 and 18-21 are pending in this application. By this Amendment, claims 2, 11, 13, 18 and 19 are amended. Claims 1 and 17 are canceled without surrender or disclaimer of the subject matter recited therein. Support for the amendments may be found in at least the original claims. No new matter is added. Applicant respectfully requests reconsideration and prompt allowance of the pending claims at least in light of the following remarks.

I. Allowed Claim and Allowable Claims

Applicant gratefully acknowledges the Office Action's indication that i) claim 21 is allowed and ii) claims 11, 12, 15 and 16 recite allowable subject matter.

II. Entry of the Amendments is Proper under 37 CFR §1.116

Entry of the amendments is proper under 37 C.F.R. §1.116 because the amendments: (a) place the application in condition for allowance for the reasons discussed herein; (b) do not raise any new issue requiring further search and/or consideration; (c) satisfy a requirement of form asserted in the previous Office Action; (d) do not present any additional claims without canceling a corresponding number of finally rejected claims; and (e) place the application in better form for appeal, should an appeal be necessary.

Alternatively, entry of the amendments is proper under 37 C.F.R. §1.116 in view of the Patent Office's After Final Consideration Pilot (AFCP) because the amendments can be determined to place the application in condition for allowance by changing form and/or new dependent claims, which require only a limited amount of further consideration or search.

Entry of the amendments is thus respectfully requested.

III. 35 U.S.C. §102(a)

Claims 1, 2, 13 14 and 17-20 are rejected under 35 U.S.C. §102(a) over U.S. Patent No. 7,277,070 (Koyama). Applicant respectfully traverses the rejection.

By this Amendment, claims 1 and 17 are canceled. Claims 2, 13 and 18-20 are amended to depend from claim 21. Claim 21 is allowed. Thus, claims 2, 13 and 18-20 are also patentable. Applicant respectfully requests withdrawal of the rejection.

* * * * *

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,


James A. Oliff
Registration No. 27,075

Hirotsuna Yamashita
Registration No. L0563

JAO:HQY/prg

Date: April 11, 2013

OLIFF & BERRIDGE, PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

<p>DEPOSIT ACCOUNT USE AUTHORIZATION Please grant any extension necessary for entry of this filing; Charge any fee due to our Deposit Account No. 15-0461</p>

Electronic Acknowledgement Receipt	
EFS ID:	15496246
Application Number:	12917885
International Application Number:	
Confirmation Number:	2374
Title of Invention:	ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE
First Named Inventor/Applicant Name:	Yojiro MATSUEDA
Customer Number:	25944
Filer:	William P. Berridge/Portia Gordon
Filer Authorized By:	William P. Berridge
Attorney Docket Number:	114251.03
Receipt Date:	11-APR-2013
Filing Date:	02-NOV-2010
Time Stamp:	16:40:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		11425103_AAFR.pdf	119343	yes	7
			50b8039f6ebae7c85317ef0b1f7a93b3b5f649ab		

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment After Final	1	1
	Claims	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	7
Warnings:			
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<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 12/917,885		Filing Date 11/02/2010		☒ To be Mailed		
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO										
APPLICATION AS FILED – PART I										
		(Column 1)		(Column 2)						
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)		
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))		N/A		N/A		N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A				
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =		*		X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =		*		X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL				
APPLICATION AS AMENDED – PART II										
		(Column 1)		(Column 2)		(Column 3)				
AMENDMENT	04/11/2013		CLAIMS REMAINING AFTER AMENDMENT			HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))		* 11		Minus	** 20	= 0	X \$80 =	0	
	Independent (37 CFR 1.16(h))		* 1		Minus	***4	= 0	X \$420 =	0	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
	TOTAL ADD'L FEE								0	
		(Column 1)		(Column 2)		(Column 3)				
AMENDMENT			CLAIMS REMAINING AFTER AMENDMENT			HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))		*		Minus	**	=	X \$ =		
	Independent (37 CFR 1.16(h))		*		Minus	***	=	X \$ =		
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
	TOTAL ADD'L FEE									
<p>* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.</p> <p>** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".</p> <p>*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".</p> <p>The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.</p>										

LIE
/NICHELE PETERSON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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ALEXANDRIA, VA 22320-4850

EXAMINER

BOLOTIN, DMITRIY

ART UNIT

PAPER NUMBER

2695

DATE MAILED: 04/26/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/917,885	11/02/2010	Yojiro MATSUEDA	114251.03	2374

TITLE OF INVENTION: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$300	\$0	\$2080	07/26/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25944 7590 04/26/2013
OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/917,885	11/02/2010	Yojiro MATSUEDA	114251.03	2374

TITLE OF INVENTION: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$300	\$0	\$2080	07/26/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
BOLOTIN, DMITRIY	2695	345-076000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/917,885	11/02/2010	Yojiro MATSUEDA	114251.03	2374
25944 7590 04/26/2013 OLIFF & BERRIDGE, PLC P.O. BOX 320850 ALEXANDRIA, VA 22320-4850			EXAMINER BOLOTIN, DMITRIY	
			ART UNIT 2695	PAPER NUMBER

DATE MAILED: 04/26/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 12/917,885	Applicant(s) MATSUEDA, YOJIRO	
	Examiner DMITRIY BOLOTIN	Art Unit 2695	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Remarks and Amendment filed on 04/11/2013.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 2,11-16 and 18-21. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☒ All b) ☐ Some *c) ☐ None of the:

1. ☒ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Interim copies:

a) ☐ All b) ☐ Some c) ☐ None of the: Interim copies of the priority documents have been received.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____	6. ☐ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	

/DMITRIY BOLOTIN/ Examiner, Art Unit 2695	
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BIB DATA SHEET

CONFIRMATION NO. 2374

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
12/917,885	11/02/2010	345	2695	114251.03		
RULE						
APPLICANTS Yojiro MATSUEDA, Chino-shi, JAPAN;						
** CONTINUING DATA ***** This application is a CON of 11/483,109 07/10/2006 PAT 7982692 which is a DIV of 10/299,861 11/20/2002 PAT 7483001						
** FOREIGN APPLICATIONS ***** JAPAN 2001-356007 11/21/2001 JAPAN 2001-371410 12/05/2001 JAPAN 2001-371403 12/05/2001						
** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 11/15/2010						
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and Acknowledged <u>/DMITRIY BOLOTIN/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY JAPAN	SHEETS DRAWINGS 15	TOTAL CLAIMS 10	INDEPENDENT CLAIMS 1
ADDRESS OLIFF & BERRIDGE, PLC P.O. BOX 320850 ALEXANDRIA, VA 22320-4850 UNITED STATES						
TITLE ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE						
FILING FEE RECEIVED 1340	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Search Notes 	Application/Control No. 12917885	Applicant(s)/Patent Under Reexamination MATSUEDA, YOJIRO
	Examiner DMITRIY BOLOTIN	Art Unit 2629

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
345	76-83	1/28/2011	DB
315	169.1-169.4	1/28/2011	DB
	Updated Search	06/07/2011	DB
	Updated Search	10/25/2011	DB
349	42,43,46	10/25/2011	DB
	Updated Search	06/08/2012	DB
	Updated Search	10/13/2012	DB
	Updated Search	02/07/2013	DB
	Updated Search	04/12/2013	DB

SEARCH NOTES		
Search Notes	Date	Examiner
Google	1/28/2011	DB
EAST	1/28/2011	DB
Updated Search	06/07/2011	DB
Updated Search	10/25/2011	DB
Updated Search	06/08/2012	DB
Updated Search	10/13/2012	DB
Updated Search	02/07/2013	DB
Updated Search	04/12/2013	DB
Inventor Search	04/12/2013	DB
Interference Search Printout	04/12/2013	DB

/DMITRIY BOLOTIN/ Examiner, Art Unit 2695	
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INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	PGPub Search, See Interference Search Printout	04/12/2013	DB
	Searched all class/subclass above	04/12/2013	DB

/DMITRIY BOLOTIN/
Examiner.Art Unit 2695

<i>Index of Claims</i> 	Application/Control No. 12917885	Applicant(s)/Patent Under Reexamination MATSUEDA, YOJIRO
	Examiner DMITRIY BOLOTIN	Art Unit 2695

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant										☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE													
Final	Original	01/28/2011	06/07/2011	10/25/2011	06/08/2012	10/13/2012	02/07/2013	04/12/2013							
-	1	✓	✓	✓	✓	✓	✓	-							
2	2	✓	✓	✓	✓	✓	✓	=							
-	3	✓	✓	-	-	-	-	-							
-	4	✓	✓	-	-	-	-	-							
-	5	✓	✓	-	-	-	-	-							
-	6	✓	✓	-	-	-	-	-							
-	7	✓	✓	-	-	-	-	-							
-	8	✓	✓	-	-	-	-	-							
-	9	✓	✓	-	-	-	-	-							
-	10	✓	✓	-	-	-	-	-							
4	11			○	○	○	○	=							
5	12			○	○	○	○	=							
8	13			✓	✓	✓	✓	=							
3	14			✓	✓	✓	✓	=							
7	15			○	○	○	○	=							
6	16			○	○	○	○	=							
-	17				✓	✓	✓	-							
9	18				✓	✓	✓	=							
10	19				✓	✓	✓	=							
11	20				✓	✓	✓	=							
1	21						=	=							

Issue Classification 	Application/Control No. 12917885	Applicant(s)/Patent Under Reexamination MATSUEDA, YOJIRO
	Examiner DMITRIY BOLOTIN	Art Unit 2695

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
-	1	-	17												
2	2	9	18												
-	3	10	19												
-	4	11	20												
-	5	1	21												
-	6														
-	7														
-	8														
-	9														
-	10														
4	11														
5	12														
8	13														
3	14														
7	15														
6	16														

/DMITRIY BOLOTIN/ Examiner.Art Unit 2695		Total Claims Allowed: 11	
(Assistant Examiner)	(Date)		
/DMITRIY BOLOTIN/ Examiner.Art Unit 2695		04/12/2013	
(Primary Examiner)	(Date)	O.G. Print Claim(s) 21	O.G. Print Figure 1

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	82	((YOJI RO) near2 (MATSUEDA)).INV.	US-PGPUB; USPAT; USOCR	ADJ	ON	2013/04/12 23:25
L2	192	((YOJI RO) near2 (MATSUEDA)).INV.	EPO; JPO; DERWENT	ADJ	ON	2013/04/12 23:25
S1	0	"12917885"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/27 17:37
S2	2	"7483001".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/27 17:49
S3	1	(10/299861).APP.	US-PGPUB; USOCR	ADJ	ON	2011/01/27 17:49
S4	2	"6781155".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 11:04
S5	3	"20040207615"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 11:16
S6	0	"12917885" and (opposite polarities)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 11:19
S7	0	"12917885" and (opposite)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 11:19
S8	3	"10299861" and (opposite)	US-PGPUB;	ADJ	ON	2011/01/28;

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			11:20
S9	3	"10299861" and (opposite polarities)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 11:20
S10	2	"20020067323"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 11:42
S11	2	"20100295820"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 11:49
S12	3	"20040207615"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 12:08
S13	1807	oled and @ad<"20011121"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 13:14
S14	69	S13 and 345/76.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 13:15
S15	262	S13 and "345"/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 13:17
S16	6	"09787036"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	ADJ	ON	2011/01/28 13:43

			IBM_TDB			
S17	2	"6859913".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 13:44
S18	2	"6859193".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 13:44
S19	2	"20020008822"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 13:59
S20	286	("3590156" "3761617" "4006383" "4114070" "4482841" "4528480" "4532506" "4554539" "4613793" "4652872" "4736137" "4797667" "4957747" "4958105" "4962374" "4963861" "4975691" "5003302" "5028916" "5063378" "5079483" "5095248" "5172032" "5302966" "5463279" "5670979" "5684365" "5952789").PN. OR ("6229506").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/01/28 14:58
S21	28	("3590156" "3761617" "4006383" "4114070" "4482841" "4528480" "4532506" "4554539" "4613793" "4652872" "4736137" "4797667" "4957747" "4958105" "4962374" "4963861" "4975691" "5003302" "5028916" "5063378" "5079483" "5095248" "5172032" "5302966" "5463279" "5670979" "5684365" "5952789").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/01/28 14:59
S22	1	"6194837".pn.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/01/28 15:03
S23	10	("20010019327" "20010026835" "20010040565" "20020008822" "20020067323" "20040207615" "6194837" "6781155" "6794675" "RE35827").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/01/28 15:04
S24	1745	((oled or amoled or el or electroluminescent) and (second transistor) and layer and (via or (contact hole)))	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/01/28 16:19
S25	1747	((oled or amoled or el or electroluminescent) and (second transistor) and layer and (via or (contact hole)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:20

S26	182	S25 and @ad<"20011121"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:20
S27	845	((oled or amoled or el or electroluminescent) and (third transistor) and layer and (via or (contact hole)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:22
S28	63	S27 and @ad<"20011121"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:23
S29	6782	345/76-83.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:27
S30	738	S29 and (third transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:28
S31	35	S30 and @ad<"20011121"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:28
S32	4	FETlington	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:33
S33	56	paired fet	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:33
S34	39	S33 and @ad<"20011121"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	ADJ	ON	2011/01/28 16:34

			DERWENT; IBM_TDB			
S35	2245	315/169.1-169.4.ccls. and @ad< "20011121"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:36
S36	45	S35 and (third transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:37
S37	51	S35 and (third (transistor or TFT))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:37
S38	3054	349/139.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:39
S39	34	349/139.ccls. and (third (transistor or TFT))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:39
S40	2	"20070188453"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:44
S41	5	"7208942".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:44
S42	0	"200900096750"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:44
S43	2	"20090079711"	US-PGPUB; USPAT; USOCR;	ADJ	ON	2011/01/28 16:44

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S44	2	"20090096750"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:45
S45	11	S40 or S41 or S43 or S44	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:45
S46	214	(first (transistor or TFT)) with (second (transistor or TFT)) with (contact hole)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:52
S47	109	(first (transistor or TFT)) with (second (transistor or TFT)) with (contact hole) with layer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:52
S48	25	S47 and @ad<"20011121"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:52
S49	8	((transistor or TFT)) with (contact hole) with (gate layer) with (metal layer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:56
S50	2	gate with source with drain	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:58
S51	281354	gate with source with drain	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 16:58
S52	5800	cascade and S51	US-PGPUB;	ADJ	ON	2011/01/28;

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			17:00
S53	2521	S52 and @ad<"20011121"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 17:00
S54	2	(S29 or S35) and S53	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 17:00
S55	1985	pixel layout	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 17:01
S56	652	S51 and S55	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 17:01
S57	98	S56 and @ad<"20011121"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 17:01
S58	10	("20010019327" "20010026835" "20010040565" "20020008822" "20020067323" "20040207615" "6194837" "6781155" "6794675" "RE35827").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/01/28 17:52
S59	10	(US-20040207615-\$ or US- 20020021266-\$ or US-20020186188-\$ or US-20020044111-\$ or US- 20010043173-\$).did. or (US-6781155-\$ or US-7277070-\$ or US-6859193-\$ or US-6501448-\$ or US-6958740-\$).did.	US-PGPUB; USPAT	ADJ	ON	2011/01/28 17:52
S60	8	S59 not S58	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/01/28 17:52
S61	2	S59 not S60	US-PGPUB; USPAT;	ADJ	ON	2011/01/28 17:52

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S62	2	"6229506".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/10/24 15:55
S63	28	"3590156" "3761617" "4006383" "4114070" "4482841" "4528480" "4532506" "4554539" "4613793" "4652872" "4736137" "4797667" "4957747" "4958105" "4962374" "4963861" "4975691" "5003302" "5028916" "5063378" "5079483" "5095248" "5172032" "5302966" "5463279" "5670979" "5684365" "5952789").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/10/24 16:03
S64	290	("6229506").URPN.	USPAT	ADJ	ON	2011/10/24 16:04
S65	1467	315/169.1,163.3.ccls.	USPAT	ADJ	ON	2011/10/24 16:40
S66	209903	"257".clas.	USPAT	ADJ	ON	2011/10/24 16:45
S67	95	S65 and S66	USPAT	ADJ	ON	2011/10/24 16:46
S68	1467	315/169.1,163.3.ccls.	USPAT	ADJ	ON	2011/10/24 22:17
S69	115337	gate near4 source	USPAT	ADJ	ON	2011/10/24 22:17
S70	323	S68 and S69	USPAT	ADJ	ON	2011/10/24 22:19
S71	117	S70 and @ad<"20011121"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/10/24 22:20
S72	225592	gate near3 source	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/10/24 22:37
S73	6604	oled and S72	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/10/24 22:38
S74	1020	S73 and 345/76.ccls.	US-PGPUB; USPAT;	ADJ	ON	2011/10/24 22:38

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S75	702	S74 and layer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/10/24 22:38
S76	39	S75 and @ad<"20011121"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/10/24 22:39
S77	26293	(gate near2 transistor) near5 (source near2 transistor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/10/24 22:46
S78	990	S77 and OLED	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/10/24 22:47
S79	701	S78 and layer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/10/24 22:47
S80	14	S79 and @ad<"20011121"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/10/24 22:47
S81	48	("20040207615" "6794675" "6958740" "6271543" "20020008822" "20020067323" "6118506" "20010026835" "20010040565" "20010017517" "20020030770" "6501448" "20020186188" "RE35827" "20010043173" "6859193" "6882102" "20020070385" "5815226" "20010019327" "6194837" "7277070" "6781155" "20020021266" "20020044111").FN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/10/25 11:57
S82	40	("20010017618" "20010035863" "20010052606" "20020014852"	US-PGPUB; USPAT;	ADJ	ON	2011/10/25 12:01

		"20020075208" "20020135309" "20020163514" "20020195968" "20030020335" "20030098708" "20040036664" "20040113873" "20040165003" "20040183791" "20040246241" "20040256617" "20050140610" "20050219168" "20060119552" "20060214890" "5680149" "6023259" "6091382" "6166714" "6229506" "6373454" "6377235" "6522315" "6577302" "6650060" "6661180" "6667580" "6734636" "6744414" "6750833" "6788003" "6859193" "6900784" "6943759" "6947019").PN.	USOCR			
S83	90	(Shirasaki near2 Tomoyuki).in.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/10/25 12:04
S84	8	S83 and @ad<"20011121"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/10/25 12:04
S85	666090	"67" and @ad<"20011121"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/10/25 12:07
S86	1472	315/169.1,163.3.ccls.	USPAT	ADJ	ON	2011/10/25 12:07
S87	210155	"257".clas.	USPAT	ADJ	ON	2011/10/25 12:07
S88	95	S86 and S87	USPAT	ADJ	ON	2011/10/25 12:07
S89	43	S88 and @ad<"20011121"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/10/25 12:07
S90	82	("6229506" "6023259" "6788003" "6900784" "6377235" "20040036664" "20010017618" "20010052606" "20020163514" "20030020335" "20050219168" "6091382" "6373454" "6734636" "6744414" "6667580" "6960680" "20040246241" "6859193" "6947019" "20010035863" "20020014852" "20040113873" "6943759" "6661180" "6947019" "20030098708" "20040256617" "20060214890" "6667580" "6522315" "20020075208" "20040183791" "6166714" "20050140610" "6577302"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/10/25 12:21

		"6750833" "20020135309" "20040165003" "6650060" "20020195968" "5680149" "6873174").PN.				
S91	166	"0120591"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/10/25 12:29
S92	1	"10472423"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/10/25 12:31
S93	42	("20010017618" "20010035863" "20010052606" "20020014852" "20020075208" "20020135309" "20020163514" "20020195968" "20030020335" "20030098708" "20030103022" "20030112205" "20040036664" "20040165003" "20040183791" "20040236443" "20040246241" "20040256617" "20050140610" "20050157581" "20050219168" "20060214890" "5680149" "6023259" "6091382" "6166714" "6229506" "6373454" "6522315" "6577302" "6650060" "6661180" "6667580" "6734636" "6744414" "6750833" "6788003" "6859193" "6900784" "6930680" "6943759" "6947019").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/10/25 12:31
S94	16	(oled and (third transistor)) and @ad< "20011121"	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/10/25 12:34
S95	1	"7483001".pn.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/10/25 14:26
S96	1	"12917885"	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/10/25 14:26
S97	5	"10299861"	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/10/25 14:27
S98	25	("20010014493" "20010019327" "20010026835" "20010040565" "20020000614" "20020008822" "20020067323" "20020154253" "20040012548" "20040207615" "20070007527" "5867233" "6100119" "6153893" "6373454" "6468839" "6515428" "6661180" "6781155" "6794675" "6859193" "6914390" "6952244" "7106006" "RE35827").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/10/25 14:28
S99	2	"7277070".pn.	US-PGPUB; USPAT;	ADJ	ON	2011/10/25 15:46

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S100	8	"10299861"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/10/25 15:50
S133	2	"7277070".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/06/08 10:42
S134	5	"20050231122" or "7483001".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/10/10 12:23
S135	1	"13217982" and record	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/10/10 12:28
S136	2	"6510207".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/10/11 14:51
S137	1	"12917885"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2013/02/07 18:23

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S101	2209	349/ 139.ccls.	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 14:33
S102	672	S101 and @ad< "20011121"	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 14:33

S103	5	S102 and oled	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 14:34
S104	1715	315/169.1,163.3.ccls.	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 14:34
S105	6782	345/76-83.ccls.	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 14:34
S106	8124	S104 or S105	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 14:34
S107	214896	(oled or amoled or el or electroluminescent)	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 14:35
S108	5481	S106 and S107	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 14:35
S109	875	S108 and @ad<"20011121"	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 14:36
S110	164	S109 and (layer with gate)	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 14:36
S111	23	("20020196206" "20030098827" "20040150591" "20040233143" "3659159" "5235253" "5610628" "5990629" "6023259" "6091203" "6229506" "6246180" "6304304" "6373454" "6462722" "6509690" "6522315" "6542138" "6577302" "6580408" "6734836" "6750833" "6839045").PN.	US-PGPUB; USPAT	ADJ	ON	2011/10/25 14:48
S112	3626	349/42,43,46.ccls.	US-PGPUB; USPAT	ADJ	ON	2011/10/25 14:55
S113	569	S107 and S112	US-PGPUB; USPAT	ADJ	ON	2011/10/25 14:58
S114	130	S113 and @ad<"20011121"	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 14:58
S115	16	(oled and (third transistor)) and @ad<"20011121"	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 15:04
S116	239	(S107 and (third transistor)) and @ad<"20011121"	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 15:04

S117	222182	gate with source with drain	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 15:04
S118	128	S116 and S117	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 15:05
S119	28	S116 and (plan view)	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 15:10
S120	221474	gate near5 source	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 15:12
S121	124	S116 and S120	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 15:12
S122	16	S121 and (plan view)	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 15:13
S123	23	S121 and (layout)	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 15:13
S124	106	(first (transistor or TFT)) with (second (transistor or TFT)) with (contact hole) with layer	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 15:16
S125	22	S124 and @ad< "20011121"	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 15:17
S126	3465	315/169.2,169.3.cds.	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 15:18
S127	230	S126 and (third transistor)	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 15:18
S128	31	S127 and @ad< "20011121"	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 15:18
S129	1	"7277070".pn.	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 15:24
S130	1	"7277070".pn.	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/10/25 15:46
S131	9	"7233342"	US-PGPUB; USPAT	ADJ	ON	2011/10/25 16:58

EAST Search History

S132	1	"7233342".pn.	US- PGPUB; USPAT	ADJ	ON	2011/10/25 16:58
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4/ 12/ 2013 11:44:12 PM
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PART B - FEE(S) TRANSMITTAL

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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25944 7590 04/26/2013
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Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/917,885	11/02/2010	Yojiro MATSUEDA	114251.03	2374

TITLE OF INVENTION: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$300	\$0	\$2080	07/26/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
BOLOTIN, DMITRIY	2695	345-076000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 OLIFF & BERRIDGE, PLC
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

SEIKO EPSON CORPORATION

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

TOKYO, JAPAN

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☒ A check is enclosed. Check No. 253804 (\$2080)
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 15-0461 (enclose an extra copy of this form).

07/26/2013 LNGUYEN2 00000049 12917885

01 FC:1501
02 FC:1504

1788.00 OP
300.00 OP

5. **Change in Entity Status** (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature

H. Yamashita

Date July 25, 2013

Typed or printed name

Hirotsuna Yamashita

Registration No. L0563

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Receipt date: 11/02/2010

Sheet 3 of 3
12917885 - GAU 2629

Form PTO-1449 (REV. 1/06)	US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 114251.03	APPLICATION NO. New U.S. Patent Application
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT Yojiro MATSUEDA	
		FILING DATE November 2, 2010	GROUP

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Name
	42	2001/0026125 A1	10/04/2001	Yamazaki et al.
	43	6,094,248	07/25/2000	Hayashi
	44	5,684,365	11/04/1997	Tang et al.
	45	6,509,688 B1	01/21/2003	Bae et al.
	46	6,657,230	12/2003	Murade
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Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
	61	JP-A-2001-242827	09/07/2001	Japan		
	62	JP-A-2001-318628	11/16/2001	Japan		

OTHER DOCUMENTS

Examiner Initials	Cite No.	Including name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
	63	Shang-Li Chen et al.; "Current Programmed Pixel Structures for OLED"; Electronics Research & Service Organization; Hsinchu, Taiwan; October 2001, pp. 399-402.
	64	Eiji Takeda et al.; "An As-P(n ⁺ -n ⁻) Double Diffused Drain MOSFET for VLSI's"; IEEE Transactions on Electron Devices, IEEE Service Center; Piscataway, NJ; vol. 30; no. 6; June 1983; pp. 652-657.

EXAMINER

/Dmitriy Bolotin/

DATE CONSIDERED
07/28/2011

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: November 2, 2010

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.B./

Receipt date: 11/02/2010

12917885 - GAU: 2629
Sheet 2 of 3

Form PTO-1449 (REV. 1/06)		US Dept. of Commerce PATENT & TRADEMARK OFFICE		ATTY DOCKET NO. 114251.03		APPLICATION NO. New U.S. Patent Application	
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)				APPLICANT Yojiro MATSUEDA			
				FILING DATE November 2, 2010		GROUP	
U.S. PATENT DOCUMENTS							
Examiner Initials	Cite No.	Document Number	Date	Name			
	19	6,859,193 B1	02/22/2005	Yumoto			
	20	2004/012548	01/22/2004	Anzai			
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Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation	
	28	CN 1291786A	04/18/2001	China			
	29	CN 1242924A	01/26/2000	China			
	30	JP-A-2001-185354	07/06/2001	Japan	X	X	
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	35	JP-A-2000-137241	05/16/2000	Japan	X	X	
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	41	EP 1 003 223 A2	05/24/2000	Europe			
EXAMINER /Dmitriy Bolotin/					DATE CONSIDERED 01/28/2011		
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

Change(s) applied
to document,
/MHE/
6/7/2013

Date: November 2, 2010

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.B./

Notice of References Cited	Application/Control No. 12/917,885	Applicant(s)/Patent Under Reexamination MATSUEDA, YOJIRO	
	Examiner DMITRIY BOLOTIN	Art Unit 2629	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2001/0043173 A1	11-2001	TROUTMAN, RONALD ROY	345/82
*	B	US-2002/0021266 A1	02-2002	Koyama et al.	345/76
*	C	US-2002/0044111 A1	04-2002	Yamazaki et al.	345/83
*	D	US-2002/0186188 A1	12-2002	Cok, Ronald S.	345/82
*	E	US-6,501,448 B1	12-2002	Komiya et al.	345/80
*	F	US-7,277,070 B2	06-2004	Yamada, Tsutomu Koyama October 2, 2007	257/72
*	G	US-6,958,740 B1	10-2004	Yumoto, Akira Nishikawa October 25, 2005	345/211
*	H	US-6,859,193 B1	02-2005	Yumoto, Akira	345/82
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/917,885	09/03/2013	8525760	114251.03	2374

25944 7590 08/14/2013
OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Yojiro MATSUEDA, Chino-shi, JAPAN;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court _____ for the Eastern District of Texas, Marshall Division _____ on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO. 2:22-cv-00118	DATE FILED 4/18/2022	U.S. DISTRICT COURT for the Eastern District of Texas, Marshall Division
PLAINTIFF Element Capital Commercial Company PTE. LTD		DEFENDANT BOE Technology Group Co., Ltd; Beijing BOE Display technology Co., Ltd; and Motorola (Wuhan) Mobility Technologies Communication Co., Ltd.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,259,736	8/21/2007	Element Capital Commercial Company PTE. LTD
2 8,164,267	4/24/2012	Element Capital Commercial Company PTE. LTD
3 8,525,760	9/3/2013	Element Capital Commercial Company PTE. LTD
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy