

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Yojiro Matsueda
U.S. Patent No.: 8,525,760 Attorney Docket No.: 54108-0001IP3
Issue Date: September 3, 2013
Appl. Serial No.: 12/917,885
Filing Date: November 2, 2010
Title: ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE,
AND ELECTRONIC DEVICE

Mail Stop Patent Board

Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

**DECLARATION OF DAVID K. LIU IN SUPPORT OF PETITION FOR *IN-TER PARTES* REVIEW OF UNITED STATES PATENT NO. 8,525,760
PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

TABLE OF CONTENTS

I.	ASSIGNMENT	1
II.	QUALIFICATIONS AND BACKGROUND INFORMATION	2
	A. Educational Background.....	2
	B. Professional Experience.....	3
III.	OVERVIEW OF CONCLUSIONS FORMED	5
IV.	LEVEL OF ORDINARY SKILL IN THE ART	8
V.	LEGAL STANDARDS	8
	A. Claim Construction.....	8
	B. Legal Standards for Anticipation.....	9
	C. Legal Standards for Obviousness	10
VI.	TECHNOLOGY BACKGROUND	14
VII.	THE '760 PATENT	19
	A. Overview of the '760 Patent.....	19
	B. United States Patent Office Proceedings	28
VIII.	SUMMARY OF THE CITED PRIOR ART	35
IX.	GROUND 1A	45
X.	GROUND 1B	68
XI.	GROUND 2A	72
XII.	GROUND 2B	84
XIII.	CONCLUSION	87

EXHIBITS

EX-1001	U.S. Patent No. 8,525,760 to Yojiro Matsueda (“the ’760 patent”)
EX-1002	The Prosecution History of U.S. Application No. 10/299,861
EX-1003	The Prosecution History of U.S. Application No. 11/483,109
EX-1004	The Prosecution History of U.S. Application No. 12/917,885
EX-1005	P.C.T. Published Application No. WO98/36407 (“Ozawa”)
EX-1006	Declaration of Dr. David K. Liu
EX-1007	U.S. Pub. No. 2002/0000576 to Kazutaka Inukai (“Inukai 576”)
EX-1008	European Pub. No. EP1111574A2 (“Inukai 574”)
EX-1009	U.S. Patent No. 7,277,070 to Jun Koyama (“Koyama”)
EX-1010	U.S. Patent No. 5,498,579 to Yan A. Borodovsky et al (“Borodovsky”)
EX-1011	U.S. Pub. Patent No. 2001/0025959 to Shunpei Yamazaki et al (“Yamazaki”)
EX-1012	Fabrice Caignet et al, The Challenge of Signal Integrity of Deep-Submicrometer CMOS Technology, 89 Proceedings of the IEEE, No. 4 (April 2001) (“Caignet”)
EX-1013	Flat Panel Displays for Portable Systems by Kalluri R. Sarma and Tayo Akinwande, Journal of VLSI Signal Processing Systems 13, 165-190 (1996) (“Sarma”)

EX-1014 Complaint, *Element Capital Commercial Company PTE. Ltd. v. BOE Technology Group Co., Ltd. et al.*, Case No. 2:22-cv-0118-JRG (EDTEX)

EX-1015 Joint Agreed Scheduling Order, *Element Capital Commercial Company PTE. Ltd. v. BOE Technology Group Co., Ltd. et al.*, Case No. 2:22-cv-0118-JRG (EDTEX)

I, David K. Liu, Ph.D., do hereby declare as follows:

I. ASSIGNMENT

1. I have been retained as a technical expert by counsel on behalf of BOE Technology Group Co., Ltd., Beijing BOE Display Technology Co., Ltd., and Motorola (Wuhan) Mobility Technologies Communication Co., Ltd. (“Petitioner”). I understand that Petitioner is requesting that the Patent Trial and Appeal Board institute an *inter partes* review (“IPR”) proceeding with respect to U.S. Patent No. 8,525,760 (“the ’760 patent”).

2. I have been asked to provide my independent analysis of the ’760 patent in light of certain prior art references.

3. I am not, and never have been, an employee of Petitioner. I received no compensation for this Declaration beyond my normal hourly compensation based on my time actually spent analyzing the ’760 patent, the prior art cited below, and issues related thereto, and I will not receive any added compensation based on the outcome of any IPR or other proceeding involving the ’760 patent.

4. My analysis here is based on my years of education, research and experience, as well as my investigation and study of relevant materials, including those cited here. I may rely upon these materials, my knowledge and experience, and/or additional materials to rebut arguments raised by the Patent Owner. Further,

I may also consider additional documents and information in forming any necessary opinions, including documents that may not yet have been provided to me.

5. My analysis of the materials produced in this proceeding is ongoing and I will continue to review any new material as it is provided. This declaration represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated here based on new information and on my continuing analysis of the materials already provided.

II. QUALIFICATIONS AND BACKGROUND INFORMATION

6. I have personal knowledge or have developed knowledge of these technologies based upon education, training, or experience, of the matters set forth herein.

7. A detailed description of my professional qualifications, including a listing of my specialties/expertise and professional activities, is contained in my curriculum vitae, a copy of which is provided as Appendix A. Below is a short summary of my professional qualifications.

A. Educational Background

8. I received a Bachelor of Science degree in Electrical Engineering from the University of California, Berkeley, in 1983. I received Master of Science and Ph.D. degrees in Electrical Engineering from Stanford University in 1985 and 1989, respectively.

B. Professional Experience

9. From 1989 to 1992, I was a member of technical staff at Texas Instruments, Inc. At Texas Instruments, my job responsibilities included process integration, device modeling, high-voltage CMOS process integration, and investigating novel source-side injection mechanisms for Flash EPROM channel hot-electron programming.

10. From 1992 to 1995, I was a member of the technical staff at Advanced Micro Devices, Inc. (AMD) where I was a key contributor in optimizing Flash cell and periphery devices in AMD's CMOS-based 0.5um and 0.35um Flash EPROM technology. My job responsibilities at AMD also included process integration, device modeling, and development of triple-well process technology for accommodate x-decoder transistors and high voltage transistors for negative gate erase operation. While at AMD, I was awarded a Spotlight Award for developing a method of manufacturing a self-aligned source (SAS) etch for a NOR flash memory.

11. I spent the next five years of my career in managerial and director roles at several California-based semiconductor companies. I was responsible for increasing yield and for leading teams of engineers working to develop next-generation memory devices.

12. In 2000, I co-founded Progressant Technologies in Fremont, California. Progressant Technologies developed IP for negative differential resistance

transistor technology and was eventually acquired by Synopsys, Inc.

13. From 2000 to 2004, I was a Senior Manager at Xilinx, Incorporated, where I was responsible for developing nonvolatile memory process technology for flash and CPLD product applications, as well as advanced CMOS process technology (specifically 75nm CMOS technology node, a half node version between 90nm and 65nm). The flash memory products I developed at Xilinx are used as the configuration memory for the FPGA, with the configuration interface between them being the JTAG interface.

14. From 2004 to 2007, I was a Senior Scientist at Maxim Integrated Products where I was responsible for developing Embedded Non-volatile Memory process technology for Power Management product applications.

15. Since 2007, I have served as a technical consultant where I have provided expert advice regarding Flash memory technology, CMOS process technology, and semiconductor device physics.

16. I have 20 years of experience as an engineer and engineering manager/director of Complementary Metal Oxide Semiconductor (CMOS) technology development. During my career, I have worked at some of the leading technology companies in the world, such as Texas Instruments, Advanced Micro Devices, Altera Corporation (now a subsidiary of Intel Corp.), and Xilinx. At these companies, my work focused on various aspects of CMOS and semiconductor technology.

17. I hold over 95 U.S. patents, a large number of which are directed to logic CMOS processes technology and high voltage CMOS process technology. The vast majority of my patents are in the area of CMOS process technology and memory architecture. As such, I am intimately familiar with the implementation of integrated process flows that essentially are repetitive sequences of modules, each composed of a layer patterning step followed by selective deposition and etching of various semiconductor materials, with the area of selectivity dictated by the layer patterning.

III. OVERVIEW OF CONCLUSIONS FORMED

18. The analysis and conclusions set forth in this Declaration are informed by my educational background and experiences in the field (see Section II).

19. Additionally, as part of my independent analysis for this Declaration, I have considered the following: the background knowledge/technologies that were commonly known to a person of ordinary skill in the art at the time of alleged invention (“POSITA”) before the earliest claimed priority date for the ’760 patent (11/21/2001); my own knowledge and experiences gained from my work experience in the field and related disciplines; and my experience in working with others involved in this field and related disciplines.

20. In addition, I have reviewed the ’760 patent (EX-1001), relevant ex-

cerpts of the prosecution history of the '760 patent (EX-1004), and relevant excerpts of applications related to the '760 patent (EX-1002, EX-1003). I have also reviewed at least the following prior art references:

- U.S. Pub. Patent No. 2002/0000576A1 (“Inukai 576”) (EX-1007)
- European Published Patent Application No. 1 111 574A2 (“Inukai 574”) (EX- 1008)
- U.S. Pub. Patent No. 2001/0025959 (“Yamazaki”) (EX-1011)

21. I have also reviewed some cited supporting references and documentation including:

- P.C.T. Published Application No. WO98/36407 (“Ozawa”) (EX-1005)
- U.S. Patent No. 7,277,070 to Jun Koyama (“Koyama”) (EX-1009)
- U.S. Patent No. 5,498,579 to Yan A. Borodovsky et al (“Borodovsky”) (EX-1010)
- Fabrice Caignet et al, The Challenge of Signal Integrity of Deep-Submicrometer CMOS Technology, 89 Proceedings of the IEEE, No. 4 (April 2001) (“Caignet”) (EX-1012)
- Sarma et al., “Flat Panel Displays for Portable Systems,” 13 Journal of VLSI Signal Processing Systems 165-190 (1996) (EX-1013)

22. Counsel has informed me that I should consider these materials through the lens of one of ordinary skill in the art related to the '760 patent at the

time of the earliest possible priority date of the '760 patent, and I have done so during my review of these materials. Counsel has informed me that the earliest possible priority date to which the challenged claims of '760 patent are entitled is November 21, 2001 ("Critical Date"), and I have therefore used that Critical Date in my analysis below.

23. Any figures that appear within this document have been prepared with the assistance of Counsel and reflect my understanding of the '760 patent and the prior art discussed below.

24. Although this Declaration refers to certain portions of the cited references for the sake of brevity, it should be understood that these citations are examples, and that one of ordinary skill in the art would have viewed the references cited herein in their entirety and, for reasons detailed later, in combination with other references cited herein or cited within those references themselves. The references used in this Declaration, therefore, should be viewed as being cited and analyzed herein in their entirety.

25. This declaration explains the conclusions that I have formed based on my analysis. To summarize those conclusions, based upon my knowledge and experience and my review of the prior art publications listed above, I believe that:

- Claim 1 is anticipated by, and obvious over Inukai 576 (Ground 1a)
- Claim 1 is obvious over Inukai 576 in view of Yamazaki (Ground 1b)

- Claim 1 is anticipated by, and obvious over Inukai 574 (Ground 2a)
- Claim 1 is obvious over Inukai 574 in view of Yamazaki (Ground 2b)

IV. LEVEL OF ORDINARY SKILL IN THE ART

26. Based on my knowledge and experience in the field and my review of the '760 patent and its file history, I believe that a person of ordinary skill in the art at the time of alleged invention ("POSITA") would have had at least a Master's degree in electrical engineering, physics, or a related field, and at least two years of relevant work experience in the field of integrated circuit design and manufacturing. Additional education can remedy lack of work experience and vice versa.

27. Based on my experience, I have a good understanding of the capabilities of one of ordinary skill. Furthermore, I possess those capabilities myself.

V. LEGAL STANDARDS

28. I have been informed by counsel of certain legal principles applicable to a patentability analysis and I have applied these principles as listed below.

A. Claim Construction

29. I have been informed by Counsel and understand that the best indicator of claim meaning is its usage in the context of the patent specification as understood by one of ordinary skill. I further understand that the words of the claims should be given their plain meaning unless that meaning is inconsistent with the patent specification or the patent's history of examination before the Patent Office.

Counsel has also informed me, and I understand that, the words of the claims should be interpreted as they would have been interpreted by one of ordinary skill at the time the invention was made (not today). Because I do not know at what date the invention as claimed was made, I have used the earliest priority date of the '760 patent as the point in time for claim interpretation purposes. That date was November 21, 2001.

B. Legal Standards for Anticipation

30. I have been informed by Counsel and understand that documents and materials that qualify as prior art can render a patent claim unpatentable as anticipated. I am informed by Counsel and understand that all prior art references are to be looked at from the viewpoint of a person of ordinary skill in the art.

31. I am informed by Counsel and understand that a challenged claim is unpatentable as “anticipated” under 35 U.S.C. § 102 if it is determined that all the limitations of the claim are described in a single prior art reference. I am informed by Counsel and understand that, to anticipate a claim, a prior art reference must disclose, either expressly or inherently, each and every limitation of that claim and enable one of ordinary skill in the art to make and use the invention.

32. I have been informed by Counsel and understand that in an inter partes review, “the petitioner shall have the burden of proving a proposition of unpatentability,” including a proposition of anticipation, “by a preponderance of the

evidence.” 35 U.S.C. § 316(e).

C. Legal Standards for Obviousness

33. I have been informed by Counsel and understand that documents and materials that qualify as prior art can render a patent claim unpatentable as obvious. I am informed by Counsel and understand that all prior art references are to be looked at from the viewpoint of a person of ordinary skill in the art at the time of the invention, and that this viewpoint prevents one from using his or her own insight or hindsight in deciding whether a claim is obvious.

34. I have been informed by Counsel and understand that a claim is unpatentable for obviousness under 35 U.S.C. § 103 (in the pre-AIA form of that statute that applies to the '760 Patent) “if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” I am informed by Counsel and understand that obviousness may be based upon a combination of references. I am informed by Counsel and understand that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. However, I am informed by Counsel and understand that a patent claim composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.

35. I am informed by Counsel and understand that when a patented invention is a combination of known elements, a court must determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue by considering the teachings of prior art references, the effects of demands known to people working in the field or present in the marketplace, and the background knowledge possessed by a person having ordinary skill in the art.

36. I am informed by Counsel and understand that a patent claim composed of several limitations is not proved obvious merely by demonstrating that each of its limitations was independently known in the prior art. I am informed by counsel and understand that identifying a reason those elements would be combined can be important because inventions in many instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. I am informed by Counsel and understand that it is improper to use hindsight in an obviousness analysis, and that a patent's claims should not be used as a "roadmap."

37. I am informed by Counsel and understand that an obviousness inquiry requires consideration of the following factors: (1) the scope and content of the prior art; (2) the differences between the claims and the prior art; (3) the level of ordinary skill in the pertinent art; and (4) any objective indicia of non-obviousness,

such as commercial success, long-felt but unresolved need, failure of others, industry recognition, copying, and unexpected results. I understand that the foregoing factors are sometimes referred to as the “Graham factors.”

38. I have been informed by Counsel and understand that an obviousness evaluation can be based on a combination of multiple prior art references. I understand that the prior art references themselves may provide a suggestion, motivation, or reason to combine, but that the nexus linking two or more prior art references is sometimes simple common sense. I have been informed by Counsel and understand that obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references may be supplied by the direction of the marketplace.

39. I have been informed by Counsel and understand that if a technique has been used to improve one device, and a person of ordinary skill at the time of invention would have recognized that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

40. I have been informed by Counsel and understand that practical and common sense considerations should guide a proper obviousness analysis, because familiar items may have obvious uses beyond their primary purposes. I have been informed by Counsel and understand that a person of ordinary skill looking to

overcome a problem will often be able to fit together the teachings of multiple prior art references. I have been informed by Counsel and understand that obviousness analysis therefore takes into account the inferences and creative steps that a person of ordinary skill would have employed at the time of invention.

41. I have been informed by Counsel and understand that a proper obviousness analysis focuses on what was known or obvious to a person of ordinary skill at the time of invention, not just the patentee. Accordingly, I understand that any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed. I have been informed by Counsel and understand that a claim can be obvious in light of a single reference, without the need to combine references, if the elements of the claim that are not found explicitly or inherently in the reference can be supplied by the common sense of one of skill in the art.

42. I have been informed by Counsel and understand that secondary indicia of non-obviousness may include (1) a long felt but unmet need in the prior art that was satisfied by the invention of the patent; (2) commercial success of processes covered by the patent; (3) unexpected results achieved by the invention; (4) praise of the invention by others skilled in the art; (5) taking of licenses under the patent by others; (6) deliberate copying of the invention; (7) failure of others to find a solution to the long felt need; and (8) skepticism by experts. I understand

that evidence of secondary indicia of non-obviousness, if available, should be considered as part of the obviousness analysis.

43. I have been informed by Counsel and understand that there must be a relationship between any such secondary considerations and the invention, and that contemporaneous and independent invention by others is a secondary consideration supporting an obviousness determination.

44. In summary, my understanding is that prior art teachings are properly combined where one of ordinary skill having the understanding and knowledge reflected in the prior art and motivated by the general problem facing the inventor, would have been led to make the combination of elements recited in the claims. Under this analysis, the prior art references themselves, or any need or problem known in the field of endeavor at the time of the invention, can provide a reason for combining the elements of multiple prior art references in the claimed manner.

45. I have been informed by Counsel and understand that in an *inter partes* review, “the petitioner shall have the burden of proving a proposition of unpatentability,” including a proposition of obviousness, “by a preponderance of the evidence.” 35 U.S.C. § 316(e).

VI. TECHNOLOGY BACKGROUND

46. Electronic displays generally work by providing a matrix of “pixels,” each of which emit light. EX-1013 (*Flat Panel Displays for Portable Systems* by

Kalluri R. Sarma and Tayo Akinwande, Journal of VLSI Signal Processing Systems 13, 165-190 (1996)) at 6. By controlling the light emitted by each pixel, these displays can generate images. *See id.*

47. The '760 patent and the prior art references I discuss below are “electroluminescent” type displays. An “electroluminescent display,” also known in the art as an “EL” display or “ELD,” creates light by using electrodes to apply a voltage or current to a material that emits light under these conditions, as electroluminescent material is material that emits light when excited by an electric voltage or current. The Sarma paper describes an ELD that “creates light by the excitation of a powder phosphor or a thin-film phosphor layer.” *See id.* at 4-5. For color displays “red, green, and blue phosphor layers” can be used. *See id.*

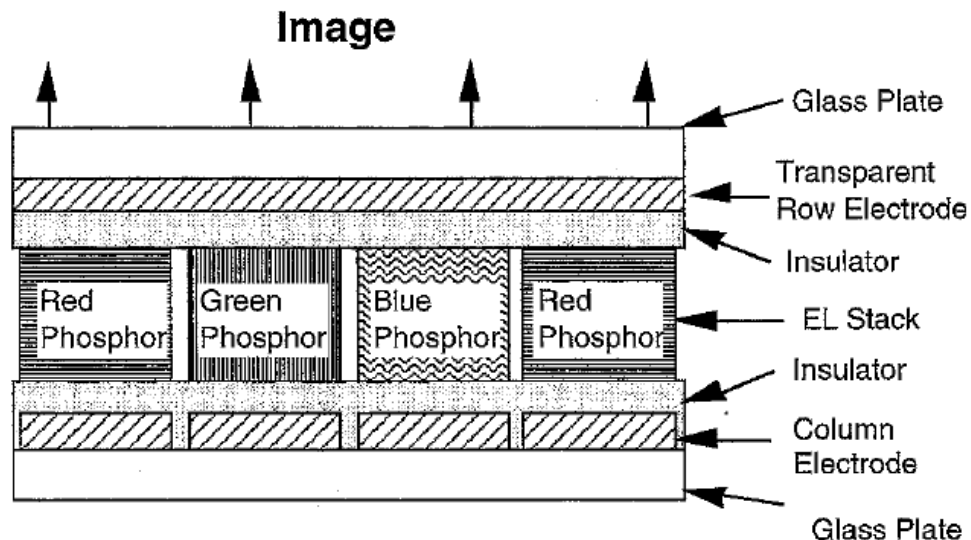


Figure 1. Device structure of the electroluminescent display (ELD).

48. To address specific pixels in a display, active matrix technology may be implemented, which utilizes active transistors to drive specific electro-optical elements. *See* EX-1013 at 11-13. An active matrix display generally consists of a matrix of pixels, generating light (luminescence) upon electrical activation, that have been deposited or integrated onto thin-film transistor arrays (arrays of unit driving circuits), with these “TFT” array functioning as a series of control and data input to control the current flowing to each pixel. *See id.* In other words, each pixel comprises a pixel circuit, which in turn comprises an electro-optical element and a driving transistor, which supplies power to the electro-optical element. *See id.*

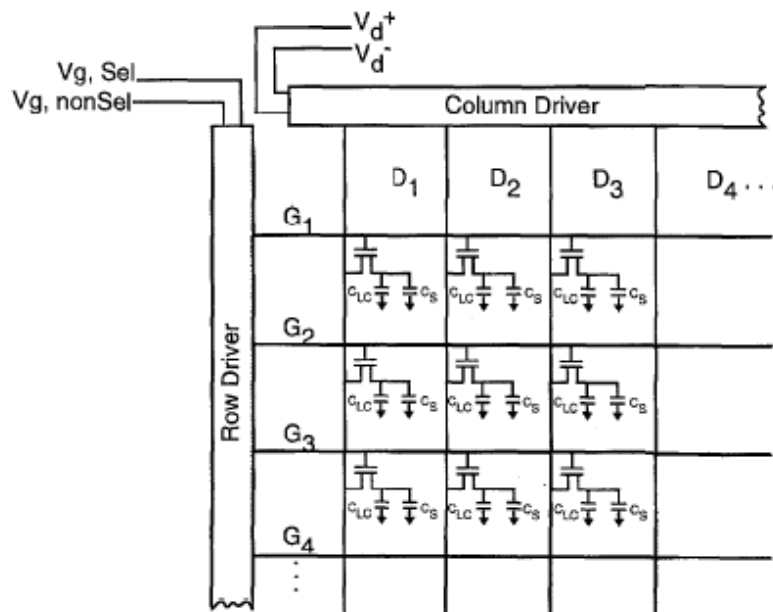


Figure 7. Schematic of a TFT active matrix array.

Id. at Fig. 7.

49. Each of the plurality of pixel circuits in an active matrix display is arranged to correspond to the intersection of a data line and a control line (gate signal line or scan line):

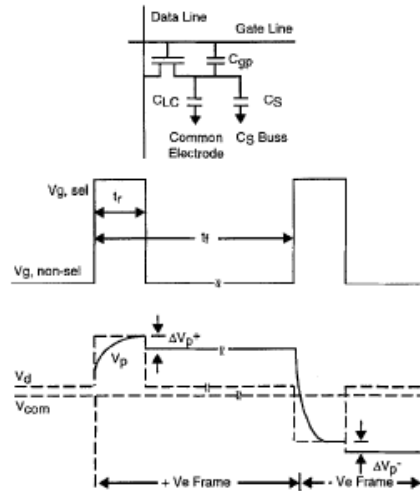


Figure 10. Electrical equivalent of a TFT-LCD pixel, and its operation.

Id. at Fig. 10.

50. The current flowing through an electro-optical device in an “active matrix” arrangement is fundamentally controlled by two TFTs at each pixel: one TFT driven by the control line to start and stop the charging of a storage capacitor to a level according to the signal supplied by the data line; another TFT to provide a voltage level needed, based on the voltage of the stored capacitor, to create a constant current to the pixel. *See id.* at 12-13.

51. Due to the many advantages offered by the active matrix system, such as improved contrast, a POSITA would have looked to various teachings in the field that offer an improved active matrix system in implementing a display panel

device. This would not only include LCD or plasma displays, but electroluminescent and other self-emission type of display devices. This endeavor would also include looking into various teachings that would improve upon or mitigate the variations introduced by the inherent device characteristics variations of TFT transistors implemented in non-single crystalline silicon.

52. One very common technique employed by semiconductor circuits, as well as circuits that employ multiple layers of conductor in a circuit formation process in general, is the use of a “jumper” wire to electrically connect two circuit elements. In a circuit, electricity flows from one element to another by means of a conductor, such as a metal wire. The circuits in a typical consumer device can feature hundreds or thousands of circuit elements connected to each other via conductors. But not every circuit element connects to every other circuit element. Because these circuit elements are laid out in a relatively small area, conductors often need to cross one another without forming a “short” circuit between them. To accomplish this, circuits may use an upper layer of conductor “jumper” wires such that a signal can effectively “jump” over a wire that carries another signal. This amounts to creating the jumper wire at a higher or lower layer compared to the wire being jumped over.

53. The “jumper” concept is illustrated, for example, by the paper “The

Challenge of Signal Integrity in Deep Submicrometer CMOS Technology” by Fabrice Caignet, et al. *See* EX-1012. This paper describes design considerations in “interconnect technologies” used in semiconductor circuits. It depicts, for example, a cross section of a 0.18 micron device that implements a jumper wire using multiple layers. *See id.* at 2-3. “Seven horizontal layers of interconnects appear, with vias between each layer.” *Id.* Each metal layer serves as a conductor connecting different circuits. In the annotated figure 2, reproduced below, a signal (represented by red arrows) carried by a wire can “jump” over another wire (circled in blue) without shorting.

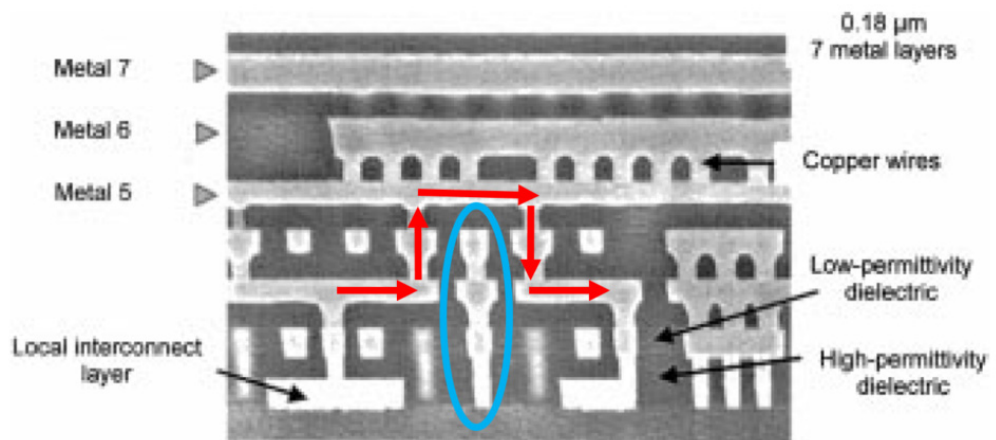


Fig. 2. Cross section of a 0.18-μ seven-metal process (courtesy ST Microelectronics).

EX-1012 at Fig. 2.

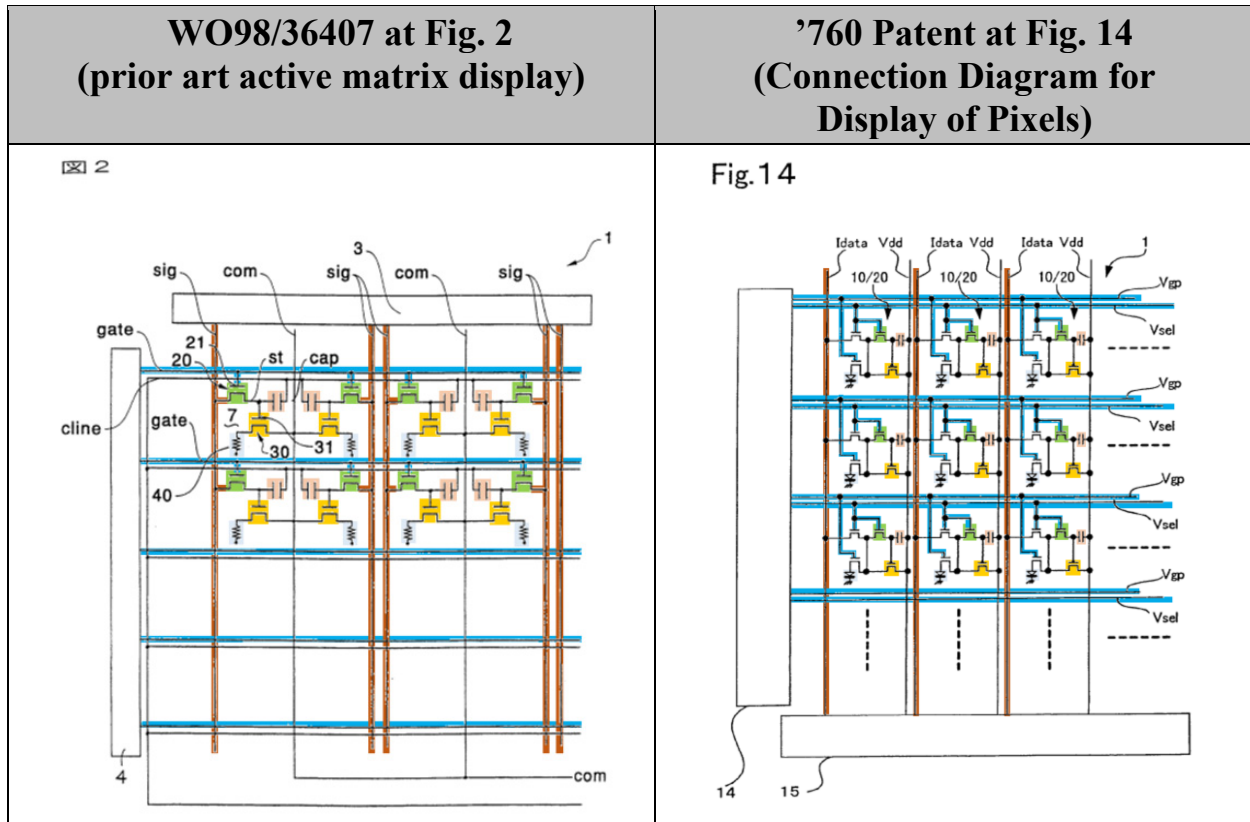
VII. THE '760 PATENT

A. Overview of the '760 Patent

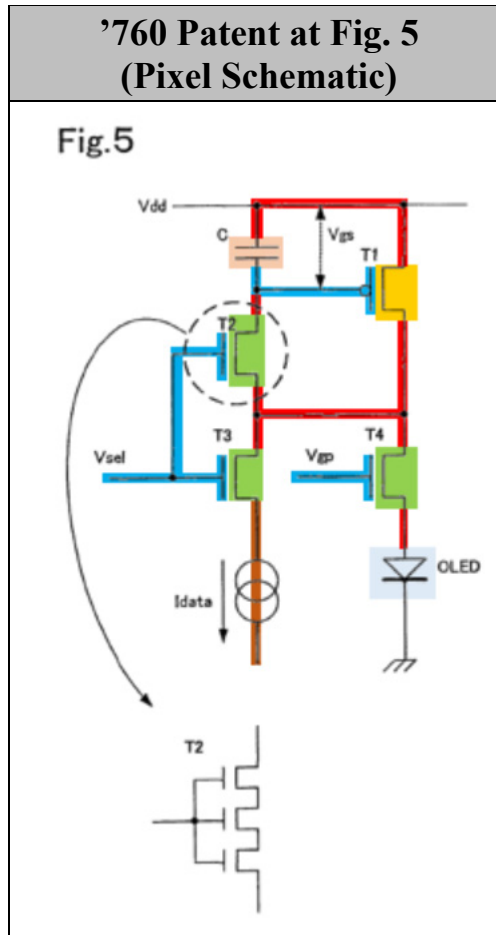
54. The '760 patent generally relates to “an active matrix substrate suitable for electro-optical devices, an electro-optical device, and electronic device.”

EX-1001 at 1:14-16. It purports to provide an “optimal pixel layout for the stable driving of electro-optical elements.” *Id.* at 1:43-47. In certain electroluminescent displays, “because organic EL elements are current-driving type electro-optical elements, the brightness is directly affected by the current.” *Id.* at 1:33-35. Thus, “the amount of power supplied to electro-optical elements must be precisely controlled.” *Id.* at 1:31-33. The ’760 patent purports to optimize the driving of these elements through the use of additional transistors, to offset or mitigate impact of variation to the drive current, compared to conventional active matrix systems.

55. The ’760 patent discloses as background that “active matrix” systems for driving pixels were known. Such a prior art system is illustrated by figure 2 of WO98/36407, addressed in the background section of the ’760 patent. *See* EX-1001 at 1:17-30; EX-1005 at 56. Such systems featured a transistor (in green) with its gate connected to a control line (also known as a gate line or scan line) (in blue) that starts and stops charging of a storage capacitor (in pale red). Turning on that transistor resulted in charging the capacitor to a voltage level based on the signal supplied by a data line (in brown). Another transistor (in orange) supplied current to an electro-optical element (in pale blue) based on the voltage stored on the capacitor. The ’760 patent’s specification generally discloses using additional transistors (not highlighted below) compared to conventional active matrix displays.



56. The '760 patent specification discloses various techniques that allegedly improve the display by, for example, improving control over the brightness of each pixel. The patent discloses five “Embodiments” but its claim 1 relates most closely to Embodiments 1 (EX-1001 at 10:52-19:10) and 5 (EX-1001 at 23:55-24:46). Embodiment 1 describes the “Operational of Peripheral Circuits” that drive electro-optical elements. *See id.* at 17:57-18:12. As I mentioned above, in an active matrix display, each pixel has a peripheral circuit that drives the electro-optical element in that pixel. The peripheral circuit described in this passage includes four transistors (T1 (in orange), T2, T3, and T4 (green)), a holding capacitor (C (pale red)), and an electro-optical element (OLED (pale blue)). *See id.*



57. The '760 patent describes the operation of these pixels as follows:

“Pixel display begins with the selection of the write control line Vsel as a data writing operation, putting the transistors T2 and T3 into the turned-on state.” EX-1001 at 17:63-65. “When the transistors T2 and T3 are put into the conducting state, the transistor T1 reaches a steady state after a prescribed time, and electric charge accumulates in the holding capacitor C according to the data current Cdata” provided by data line Idata. *Id.* at 17:66-18:2. “As light emission action, the write control line Vsel is put into the unselected state, the transistors T2 and T3 are turned off, and after stopping supply of the data current Cdata, the light emission

control line V_{gp} is selected. As a result, the transistor T4 is turned on, and a current corresponding to the potential difference V_{gs} between the voltage stored in the holding capacitor C and the power supply voltage V_{dd} is supplied to the light-emitting portion OLED via the transistors T1 and T4, so that light is emitted from the light-emitting layer.” EX-1001 at 18:3-12.

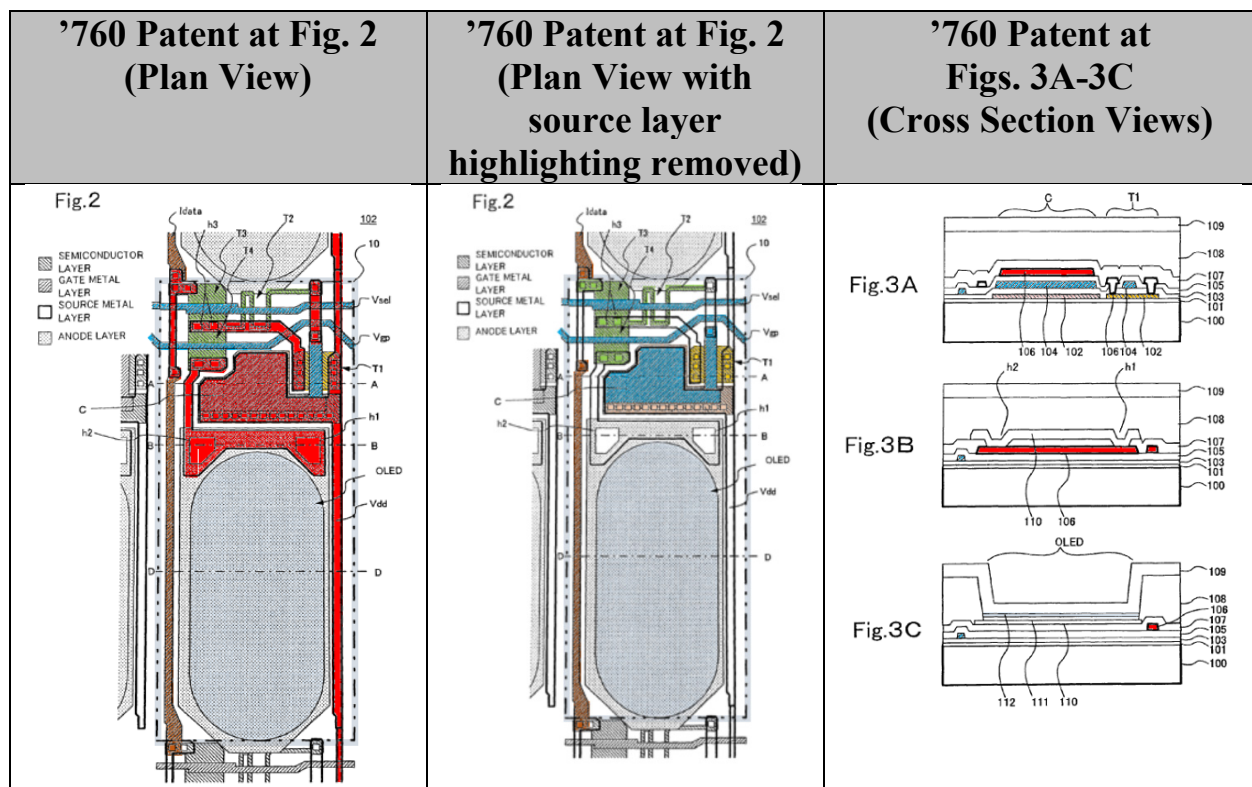
58. The transistor T2 can be a “multi-gate” type of transistor. *See* EX-1001 at 18:15-40. Such transistors have multiple gates, which helps prevent “leakage current” from flowing from the transistor when the transistor is turned off. *See id.*

59. The ’760 patent also shows “plan” and “cross section” views of the peripheral circuit. *See* EX-1001 11:45-14:3, Figs. 2, 3A-3C. These views show the “layers” of the circuit. Microelectronic circuits are built in a series of “layers” stacked on top of each other like those disclosed in the Caginet article. The ’760 patent circuit consists of an anode layer, semiconductor layer, gate metal layer (*id.* at 12:63-67), and source metal layer (*id.* at 13:6-12) stacked. The semiconductor layer is used to form channel regions as well as source and drain regions, of transistors by being “doped.” *See id.* at 12:37-51. Doping generally refers to the process of implanting impurities in a semiconductor to imbue certain properties to that semiconductor. The channel portion of the semiconductor layer (shown in green or

orange) can be patterned and doped to form “n-type” or “p-type” transistor channels. *See id.* The gate layer (shown in blue) above that can be patterned to form control or data lines, and certain portions of signal lines formed in the gate layer also function as gate electrodes for the transistors. *See id.* at 5:41-43; 17:30-49.

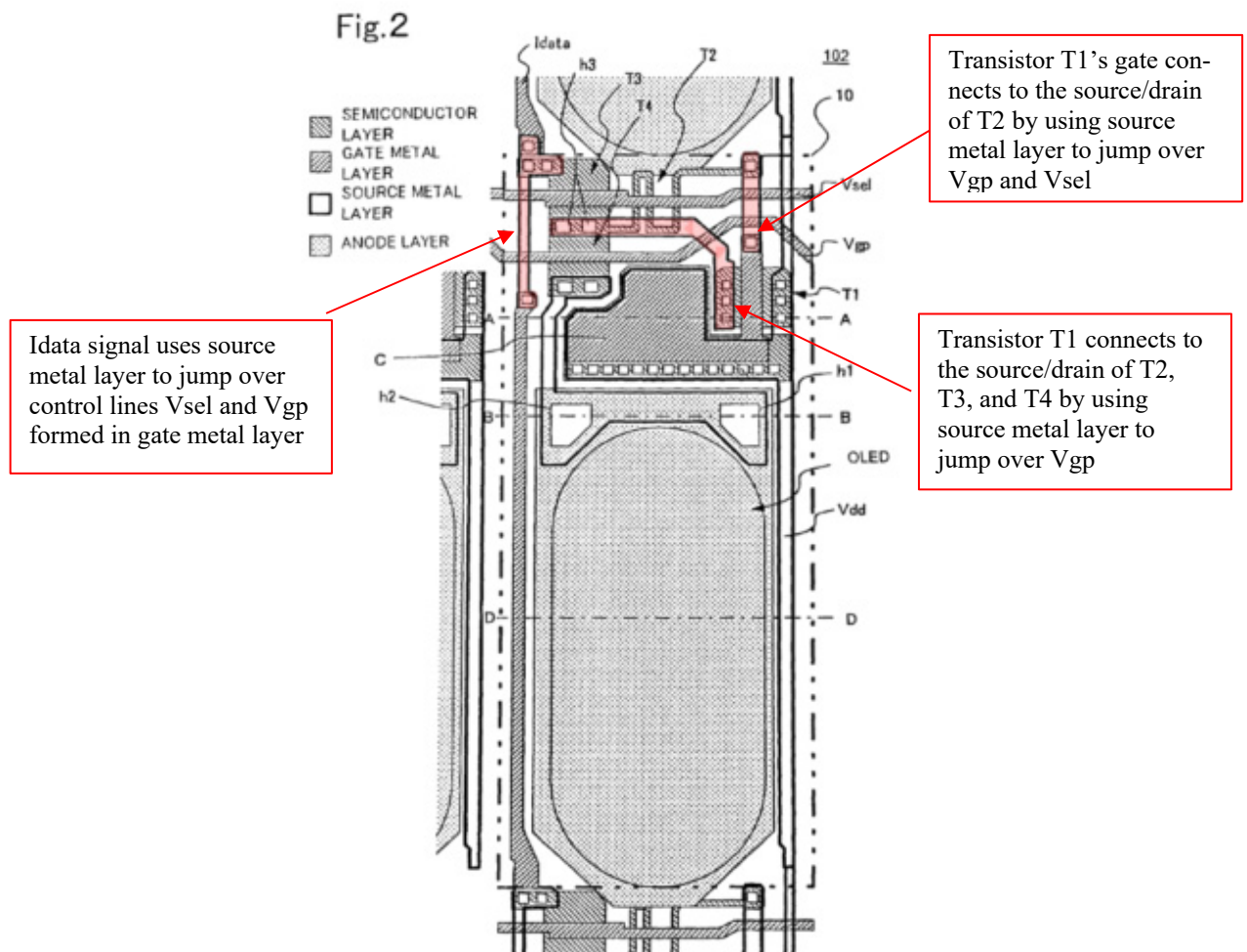
The control line Vsel, for example, implements the multiple gates of transistor T2.

This can be observed by noting that the green semiconductor layer snakes back and forth to allow the Vsel control line cross over it several times. Each instances where the lines intersect form one of the gates of the multi-gate structure.



60. The '760 patent's pixel circuit, as shown in plan view figure 2, uses wires to “jump” over other wires. These are shown by the red highlighting below.

The '760 patent does not describe these jumpers aside from referencing "the intersections between data lines *Idata* and scan lines *Vsel*, data lines *Idata* are formed in the source metal layer." *See id.* at 17:30-39. It does not describe any alleged benefits of these jumper wires or how they relate to what came before.



61. Claim 1 of the '760 patent is reproduced below. It does not reflect any

teachings that the patent specification deems as significant or as an improvement over the prior art. For example, the patent discloses that the second active element can have “a structure which prevents leakage currents during shutoff.” EX-1001 at 1:61-62; *see also id.* at 2:18-24 (explaining leakage current phenomenon: “Normally, when an active element is in the non-conducting state, whereas ideally there should be no current flowing, a current, albeit slight may flow.”). The patent discloses “multi-gate” transistors (*see* EX-1001 at 2:25-30) and “lightly doped drain” transistors (*see id.* at 2:34-48) as examples of such structures. Yet the challenged claim does not require any such structures. *See id.*; *see also* EX-1001 at 18:13-60, Claim 1. The challenged claim also does not require that a peripheral circuit must be formed in a particular region relative to a “prescribed curvature” of a light-emitting portion (EX-1001 at 14:6-15:57), nor does it require a “plurality of contact holes” (*id.* at 15:57-16:17), nor does it require that lower layers have a “larger . . . pattern shape” compared to higher layers (*id.* at 16:18-61), nor does it require that the “gate metal layer is positioned with a separation of at least a prescribed distance” from the light-emitting layer’s electrodes (*id.* at 16:62-17:56), nor does it require that data lines be “formed in the conducting layer which is at the greatest distance from the common electrode” (*id.*), nor does it require that “at least one active element among the plurality of transistors and other active elements is connected to another active element by the same contact hole” (*id.* at 18:61-19:9).

Figure 5	Claim 1
Fig.5	1. An electro-optical device comprising: a data line; a control line; and a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit including: a first transistor that includes a first semiconductor film; an electro-optical element electrically connected to one of a source or a drain of the first transistor; a second transistor that includes a second semiconductor film, the second transistor connected between the one of the source or the drain and a gate of the first transistor; a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor according to a data signal; and a wiring connected between the second transistor and the gate of the first transistor, the first transistor supplying a current based on the gate voltage to the electro-optical element, the wiring being formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film are formed,

	the wiring having a portion formed in the layer different from a gate layer in which the gate of the first transistor is formed, the portion crossing the control line .
--	---

B. United States Patent Office Proceedings

62. The '760 patent was filed as a continuation of application no. 11/483,109, which was filed as a division of application no. 10/299,861. *See* EX-1001 at (60); *see also* EX-1002 (prosecution history of '861 application); EX-1003 (prosecution history of '109 application). The '861 application prosecution history culminated in claims requiring a “second transistor having a structure to prevent leakage currents during shutoff, and the polarity of the second transistor being opposite to the polarity of the first transistor.” *Id.* at 1615-1619 (independent claim 46). The '109 application prosecution history generally pertained to requiring that a pixel’s “peripheral circuitry” is formed in a region surrounded by an electro-optical element’s boundary having a “specified curvature” and “a polygon circumscribing the electro-optical element.” *See id.* at 61, 996-999; EX-1001 at 14:6-16:17, Figs. 4A-4C.

63. On November 2, 2010, the Applicant filed application no. 12/917,885 as a continuation of the '109 application with original claims 1 and 3:

<u>What Is Claimed Is:</u>	
1.	An electro-optical device comprising: a data line; a control line; and a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit comprising: a first transistor; an electro-optical element electrically connected to one of a source or a drain of the first transistor; a second transistor connected between the one of the source or the drain and a gate of the first transistor; and a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor according to a data signal, the first transistor supplying a current based on the gate voltage to the electro-optical element, and the second transistor having a multi-gate structure.
3.	The electro-optical device according to claim 1, wherein at least a portion of wiring between the first transistor and the second transistor is formed in a metal layer which is different from a semiconductor layer in which the first transistor and the second transistor are formed, and wherein the metal layer is a layer different from a gate metal layer in which a gate of the second transistor is formed, and the wiring between the first transistor and the second transistor is provided through a contact hole.

EX-1004 ('885 App.) at 72, 259-278.

64. A few days later, the U.S. Examiner rejected these claims as obvious over U.S. Patent Nos. 6,229,506 (“Dawson”); 8,859,193 (“Yumoto”); and 7,277,070 (“Koyama”). *See id.* at 282-292.

65. On May 9, 2011, the Applicant amended the claims to require that the first transistor has a “single-gate structure,” in contrast to the second transistor,

which has a multi-gate structure. *Id.* at 341-346. The Examiner maintained the obviousness rejection based on Dawson, Yumoto, and Koyama. *Id.* at 351-359

66. On October 19, 2011, the Applicant broadened claim 1 to no longer require that the second transistor have a “multi-gate structure,” but instead incorporated claim 3’s requirement of a wiring being formed in a layer different from the semi-conductor layer and the gate layer:

1. (Currently Amended) An electro-optical device comprising:

- a data line;
- a control line; and
- a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit comprising:
 - a first transistor;
 - an electro-optical element electrically connected to one of a source or a drain of the first transistor;
 - a second transistor connected between the one of the source or the drain and a gate of the first transistor; and
 - a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor according to a data signal; and
 - a wiring connected between a gate of the first transistor and the second transistor;
 - the first transistor supplying a current based on the gate voltage to the electro-optical element;
 - the wiring being formed in a layer which is different from a semiconductor layer in which the first transistor and the second transistor are formed; and
 - the wiring being formed in a layer different from a gate layer in which a gate of the first transistor formed.
 - ~~the first transistor having a single-gate structure, and~~
 - ~~the second transistor having a multi-gate structure.~~

Id. at 591-601.

67. On November 2, 2011, the USPTO rejected claim 1 as anticipated by 7,277,070 (“Koyama”), but noted that claims 11, 12, 15, and 16 would be allowable if rewritten in independent form. *Id.* at 609-614; *see also id.* at 598.

68. On April 26, 2012, the Applicant amended claim 1 to clarify that the “wiring” connects the “second transistor and the gate of the first transistor” and that it was formed in a layer different from the layer of the “first semiconductor film and the second semiconductor film”:

1. (Currently Amended) An electro-optical device comprising:

a data line;

a control line; and

a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit ~~including~~comprising:

_____a first transistor ~~that includes a first semiconductor film~~;

_____an electro-optical element electrically connected to one of a source or a drain of the first transistor;

_____a second transistor ~~that includes a second semiconductor film, the second transistor~~ connected between the one of the source or the drain and a gate of the first transistor;

_____a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor according to a data signal; and

_____a wiring connected between ~~a gate of the first transistor and the second transistor and the gate of the first transistor~~;

the first transistor supplying a current based on the gate voltage to the electro-optical element;

the wiring being formed in a layer which is different from a ~~semiconductor~~ layer in which ~~the first semiconductor film and the second semiconductor film~~ the first transistor and the second transistor are formed; and

the wiring being formed in a layer different from a gate layer in which ~~a the~~ gate of the first transistor is formed.

Id. at 657-664, 788-789. The Applicant argued that Koyama did not disclose the “wiring” limitation. *See id.* at 663.

69. On June 28, 2012, the Examiner rejected this argument, and maintained the rejection of claim 1. *See id.* at 799-808.

70. On September 28, 2012, the Applicant amended claim 1 to further recite that the wiring has a “portion extending in a direction in which the data line

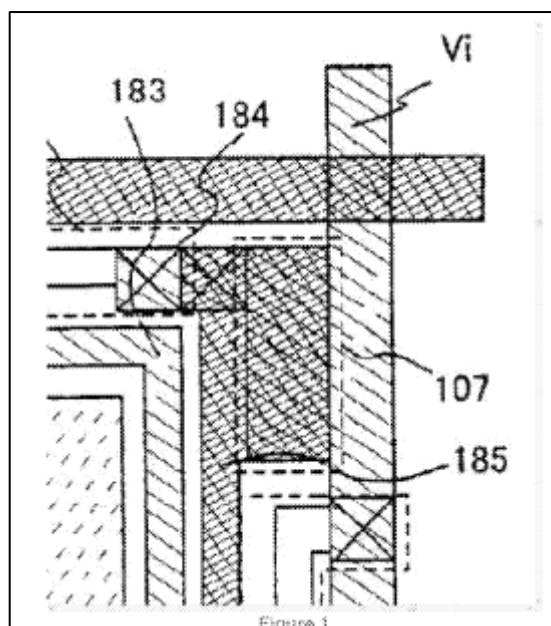
extends.” *See id.* at 822-835. The Applicant argued that Koyama did not disclose the “wiring” limitation, based on both the new limitation introduced as well as the reasoning previously provided. *See id.* at 832-835.

71. On October 18, 2012, the Examiner again rejected these arguments and maintained the rejection based on Koyama. *See id.* at 837-851.

72. On January 18, 2013, the Applicant eliminated from claim 1 the requirement that the wiring’s portion “extend[s] in a direction in which the data line extends” and instead added the requirement that it “cross[es] another wiring formed in the gate layer.” *See id.* at 855-866.

73. On February 13, 2013, the Examiner rejected this claim based on Koyama:

the wiring having a portion formed in the layer different from a gate layer in which the gate of the first transistor is formed (as shown in fig. 20, the wiring 184 and gate layer 185 are in different layers (col. 27, line 60 – col. 28, line 20)), and the portion (wiring 184 of fig. 20) crossing another wiring formed in the gate layer (as shown in fig. 20 (corresponding to Figure 1 bellow), the wiring 184 crosses gate wiring 185 to form a junction such that wiring 184 and 185 may be connected: “the other of which [drain or source] is connected to a connection wiring line 184 and to a gate wiring line 185”, col. 27, line 60 – col. 28, line 20. It is absolutely necessary when connecting two wirings disposed in two different layers to overlap and since 184 and 185 are connected they necessarily overlap).



Id. at 870-889.

74. On April 11, 2013, the Applicant cancelled claim 1 and introduced new claim 21, which was substantially similar to claim 1, except that it required the wiring portion to be “crossing the control line.” *See id.* at 894-900.

21. (New) An electro-optical device comprising:
a data line;
a control line; and
a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit including:
a first transistor that includes a first semiconductor film;
an electro-optical element electrically connected to one of a source or a drain of the first transistor;
a second transistor that includes a second semiconductor film, the second transistor connected between the one of the source or the drain and a gate of the first transistor;
a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor according to a data signal; and
a wiring connected between the second transistor and the gate of the first transistor,
the first transistor supplying a current based on the gate voltage to the electro-optical element,
the wiring being formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film are formed,

the wiring having a portion formed in the layer different from a gate layer in which the gate of the first transistor is formed, the portion crossing the control line.

Id. at 897-898.

75. On April 26, 2013, the Examiner allowed the claims. *See id.* at 904-906. The Examiner did not provide reasons for the allowance.

VIII. SUMMARY OF THE CITED PRIOR ART

76. Published Patent Application Nos. U.S. 2002/0000576A1 (“Inukai 576”) and E.P. 1 111 574A2 (“Inukai 574”) are both published patent applications filed by Semiconductor Energy Laboratory Co. Ltd. and invented by Kazutaka

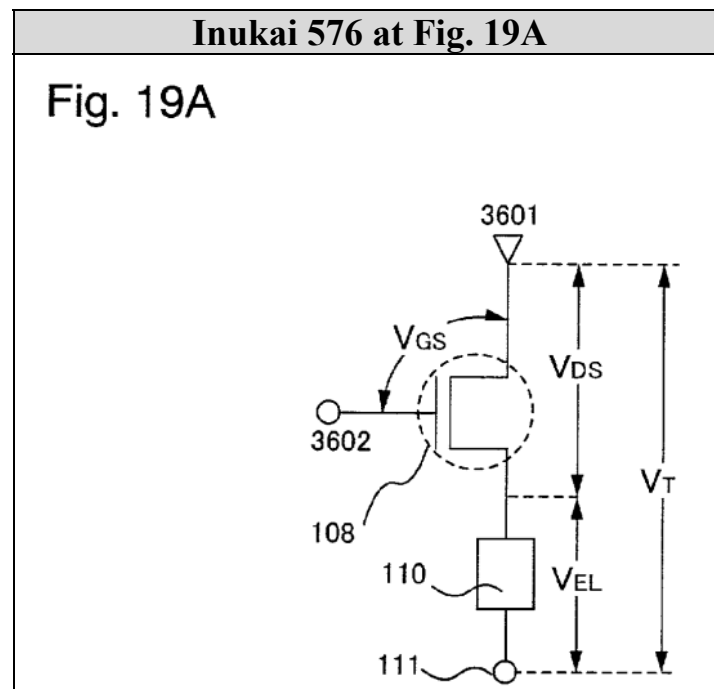
Inukai.

77. Inukai 576 was filed June 22, 2001 (before the Critical Date of the '760 patent) and it published January 3, 2002. I understand that Inukai 576 therefore qualifies as prior art to the '760 patent under pre-AIA 35 U.S.C. § 102(e). Inukai 574 published June 27, 2001 (before the Critical Date of the '760 patent). I understand that Inukai 574 therefore qualifies as prior art to the '760 patent under pre-AIA 35 U.S.C. § 102(a).

78. Inukai 576 and Inukai 574 both generally related to an electroluminescent or “EL” “active matrix” type of display. *See* EX-1007 at [0001]-[0006], [0036]; EX-1008 at [0001]-[0007], [0030]. The references each teach that it was difficult to control the brightness of EL elements driven by conventional active matrix systems. EX-1007 at [0012]-[0035], [0037]; EX-1008 at [0009]-[0029], [0031]. Such systems featured transistors (such as thin film transistors or “TFTs”) that supplied an analog current to EL elements and “the EL element emits light in an amount which corresponds to the amount of current.” EX-1007 at [0032]; *see also* EX-1008 at [0018]. The behavior of these transistors (and transistors generally) are described by their “characteristics,” which refer to mathematical relationships between the voltages that can be applied across different transistor terminals and the currents that flow into or out of those terminals.

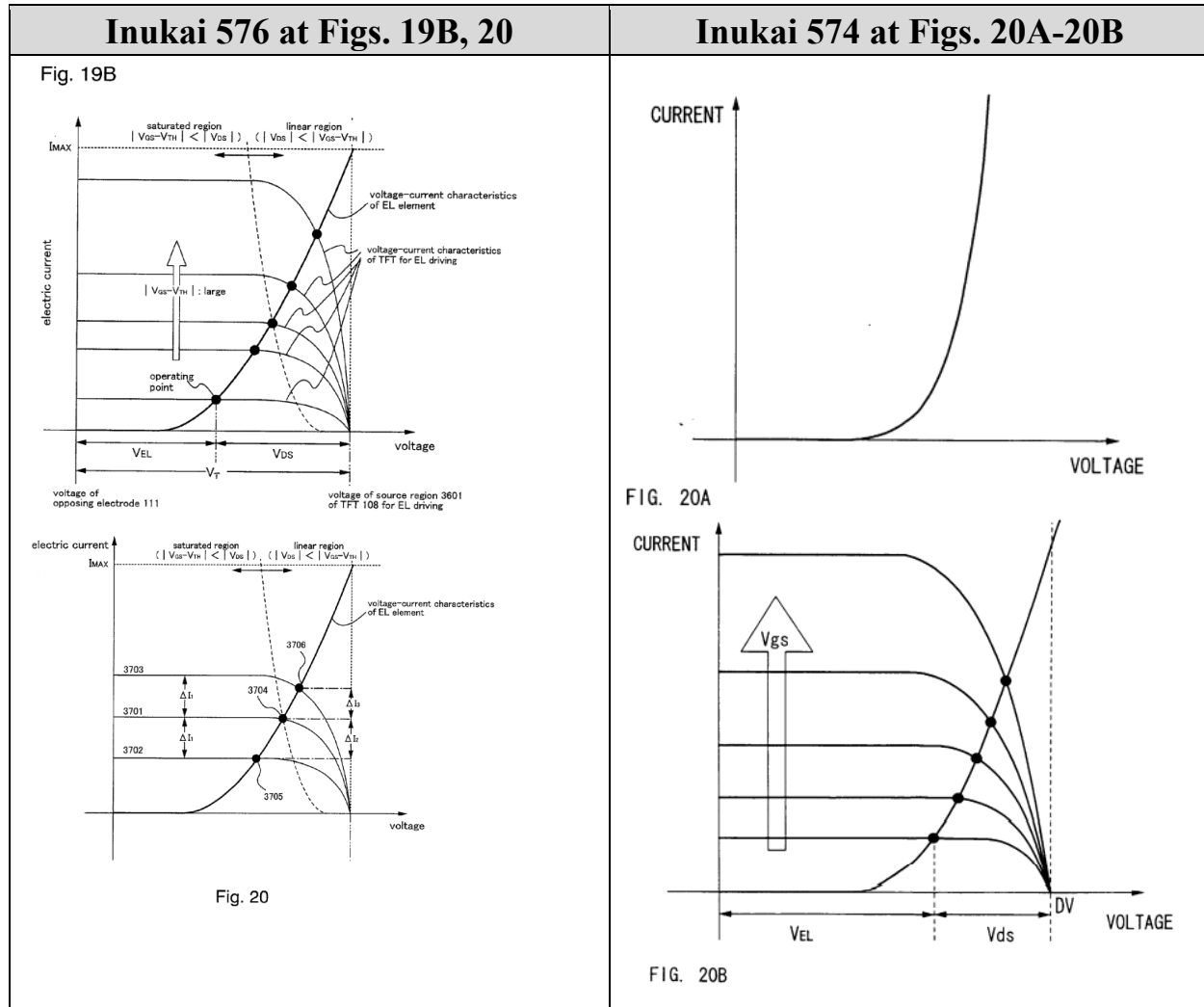
79. Of particular relevance, one characteristic is the relationship between

the current outputted by a transistor's drain terminal (I_{DS}) and its gate-to-source voltage (V_{GS}). The current provided by any given driving transistor in an active matrix system is determined by the gate-to-source voltage applied to it and this characteristic. Inukai 576's figure 19A illustrates the gate-to-source voltage that determines the current provided by the drain.



80. Inukai 576 and Inukai 574 teach that because the I_{DS} - V_{GS} characteristic may vary from transistor to transistor, “the amount of outputted current even if equal gate voltage is applied.” EX-1007 at [0034]; *see also* EX-1008 at [0028]. Thus even “slight variation in the I_{DS} - V_{GS} characteristics results in considerable difference in the amount of light emitted from the EL elements between adjacent pixels even if a signal of equal voltage is inputted thereto.” EX-1007 at [0034]; *see also* EX-1008 at [0132]. The references illustrate these characteristics in the

figures reproduced below as a curve. Transistors with different characteristics will have different curves.

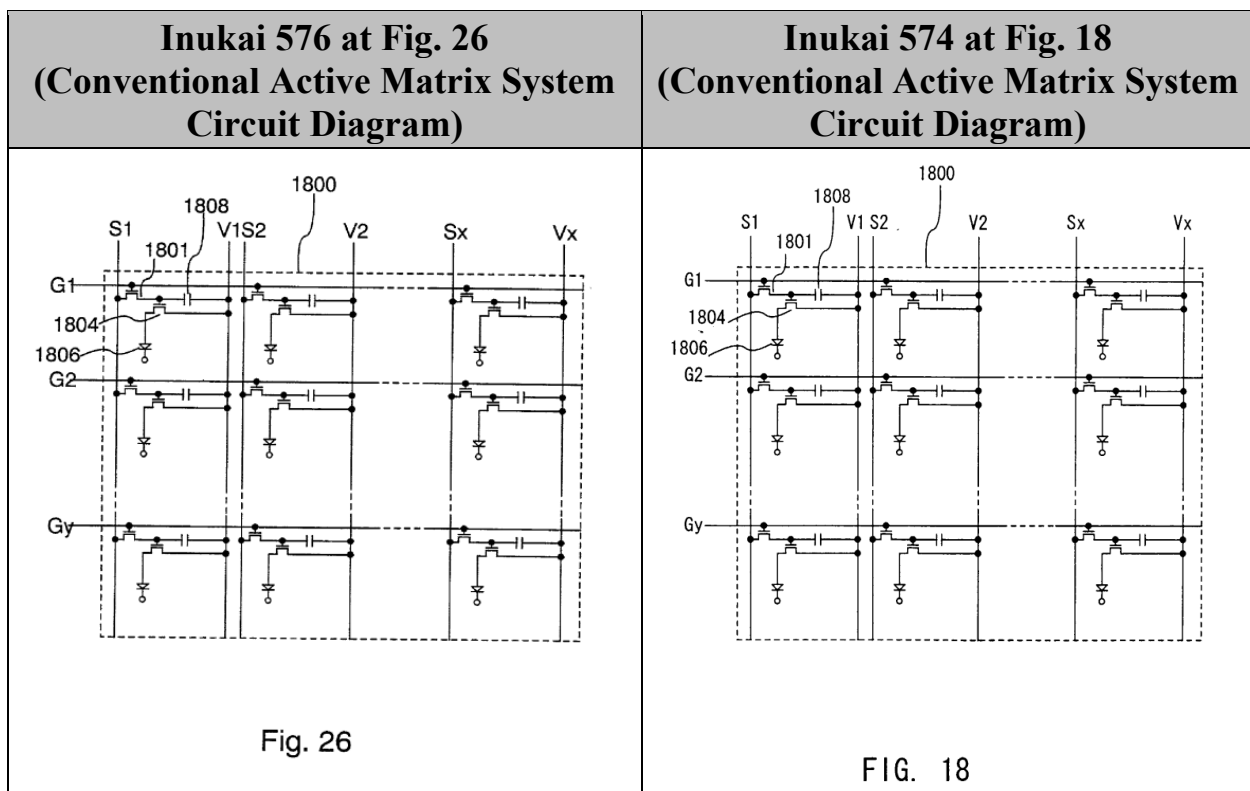


81. The Inukai references address that sensitivity by proposing pixel circuitry that results in a digital driving system rather than an analog driving system. In this method, “the amount of light emitted from EL elements is carried out not through control of current using the saturated region but mainly through control of time during which the EL elements emit light.” EX-1007 at [0039]; *see also* EX-

1008 at [0033]. This method improves “control of the amount of light emitted from EL elements” because the EL element’s brightness does not depend on its driving transistor’s characteristics. *See id.*

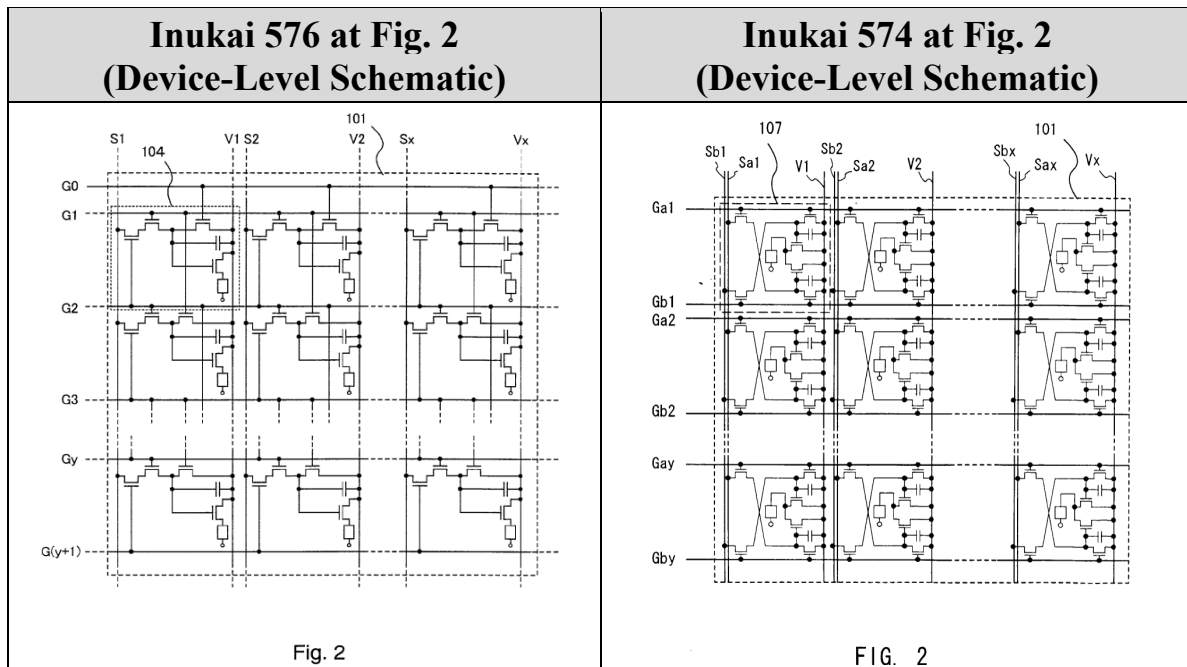
82. The Inukai references propose a slightly different pixel circuit, relative to conventional active matrix pixel circuits, to implement digital control over EL element brightness.

83. The figures below reflect circuit-level schematics of prior art active matrix driving systems. *See* EX-1007 at [0013]; EX-1008 at [0010]

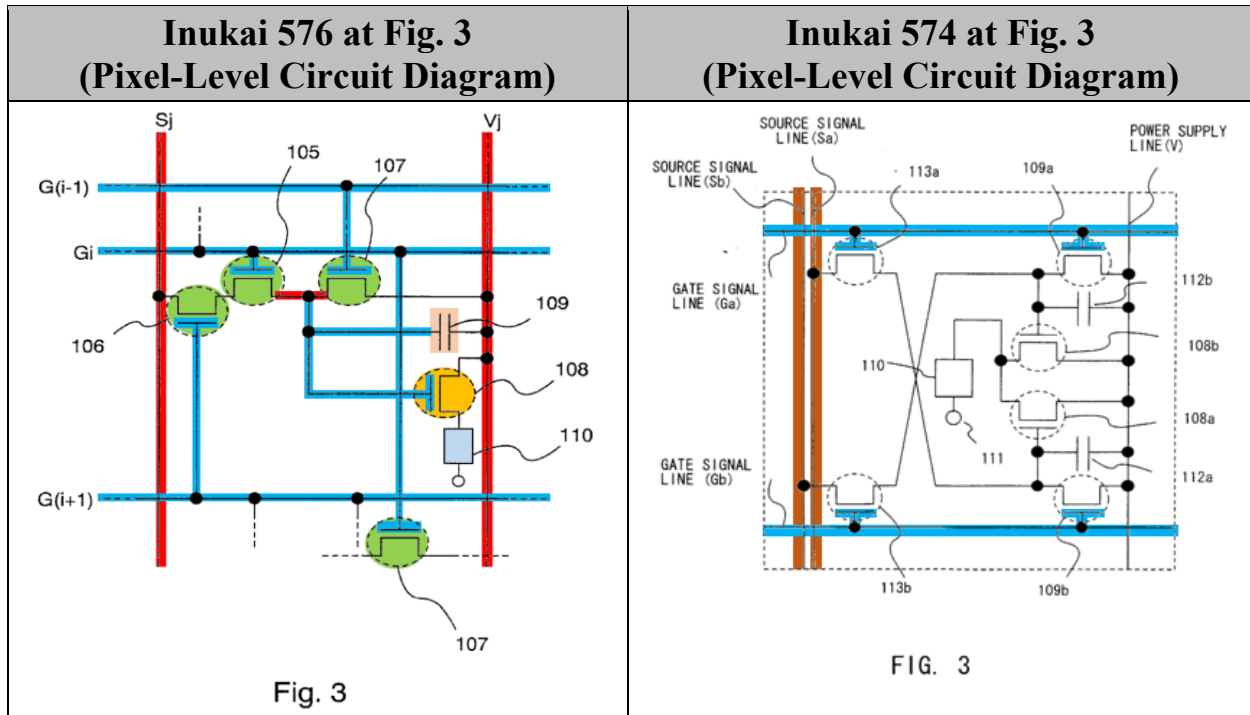


84. The figures below reflect circuit level schematics of a device implementing the teachings of the Inukai references. *See* EX-1007 at [0074]; EX-1008

at [0079].

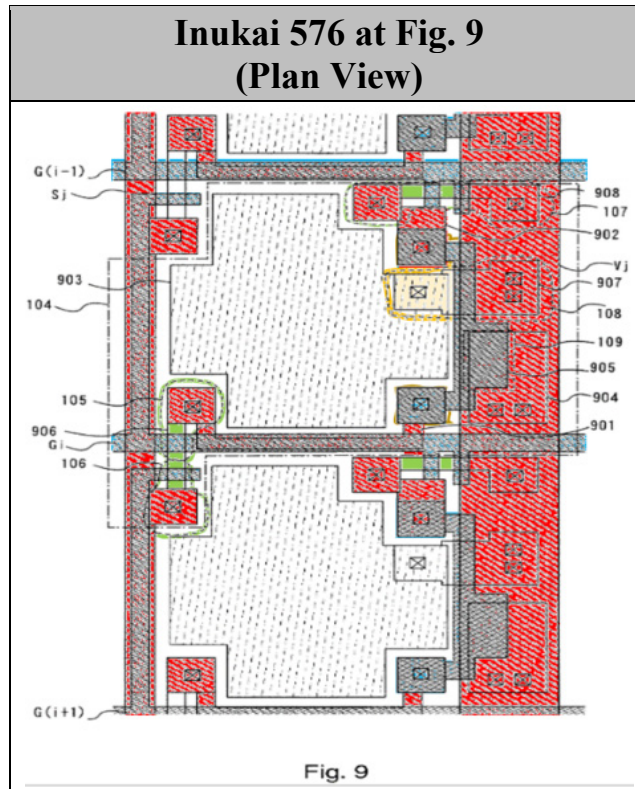


85. The figures below reflect pixel-level circuit schematics implementing the teachings of the Inukai references. *See* EX-1007 at [0077]-[0088] (describing “circuit diagram of the pixel 104”); EX-1008 at [0101]-[0109] (describing “enlarged view of the pixel 107”); *see also* EX-1007 at [0089]-[0138], Figs. 4-5 (describing timing diagram of signals that operate Inukai 576’s pixels); EX-1008 at [0110]-[0146], Fig. 4.



86. The Inukai references both disclose embodiments that employ a “jumper wire” technique.

87. Inukai 576, for example, discloses a plan view showing how the pixel elements can be laid out. See EX-1007 at [0220]-[0229], Fig. 9. This plan view shows, for example, that “TFT 108 for EL driving uses a part of the gate wiring 905 as its gate electrode” (*id.* at [0225]) that is also “connected through a connection wiring 902 to one of a source region and a drain region of the TFT 107 for erasing” (*id.* at [0224]). In other words, TFT 108’s gate is connected to TFT 107’s source or drain through gate wiring 905 and connection wiring 902. As shown in figure 9 below, connection wiring 902 jumps over a portion of control line G(i-1) that functions as one of the two gate electrodes controlling TFT 108.



88. Inukai 574 does not use plan views to depict its circuitry. It does, however, disclose alternative pixel circuits that can implement the described digital driving system. Inukai 574 discloses certain embodiments that can be implemented by the pixel circuit schematic illustrated by figure 3. See EX-1008 at [0149]-[0176] (describing Embodiment 1 as a “64 gray-scale display from a 6-bit digital data signal”); *id.* at [0177]-[0195] (describing Embodiment 2 as a “256 gray-scale display system”); *id.* at [0196]-[0211] (describing Embodiment 3 as a “64 gray-scale display system”); *id.* at [0212]-[0229] (describing Embodiment 4 as a “64 gray-scale display system”). The reference also discloses an Embodiment 5, which corresponds to the alternative pixel circuit schematics illustrated by figures

5, 6, and 7. *See id.* at [0230]-[0233]. “Fig. 5 is an example of a case in which the electric current supply line 3803 is formed parallel to the gate wirings 3801a and 3801b.” *Id.* at [0231]. “Figs. 6 and 7 are an example of a case in which the electric current supply line 3803 is common between two pixels.” *Id.* at [0232]. “Fig. 6 is an example of a case in that the electric current supply line 3803 and the source wiring 3802a, 3802b are formed in parallel. Fig. 7 is an example of a case in that the electric current supply line 3803 and the gate wiring 3801a, 3801b are formed in parallel.” *Id.* at [0233]. The instances in which two wires meet and form a black circle indicate that they are electrically connected to one another. Alternatively, where one wire in a schematic “dead ends” into another (as opposed to passing beyond it), a POSITA would generally understand that indicates that the two wires are connected to one another. The instances in which one line crosses another without a black circle or dead-ending, however, indicate that one line crosses over another without any electrical connection between the two.

**Inukai 574 at Fig. 3
(Pixel-Level Schematic,
Embodiment 1)**

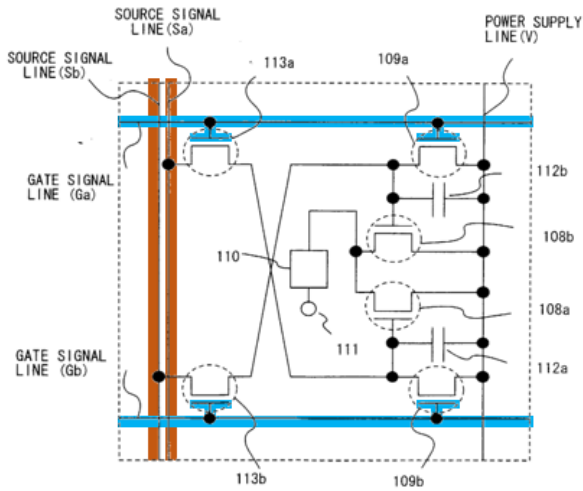


FIG. 3

**Inukai 574 at Fig. 5
(Pixel-Level Schematic,
Embodiment 5)**

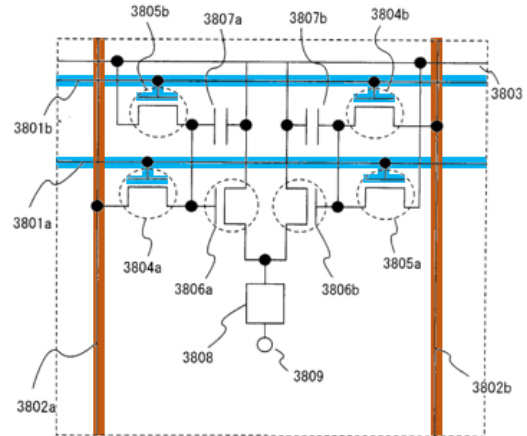


FIG. 5

**Inukai 574 at Fig. 6
(Pixel-Level Schematic,
Embodiment 5)**

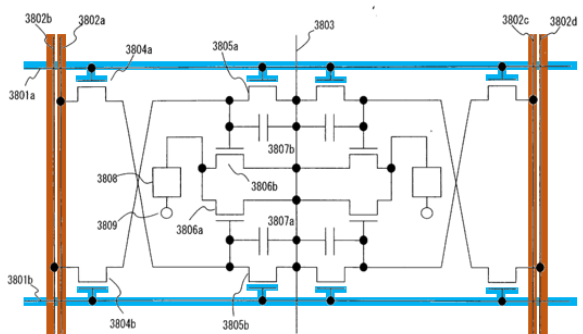


FIG. 6

**Inukai 574 at Fig. 7
(Pixel-Level Schematic,
Embodiment 5)**

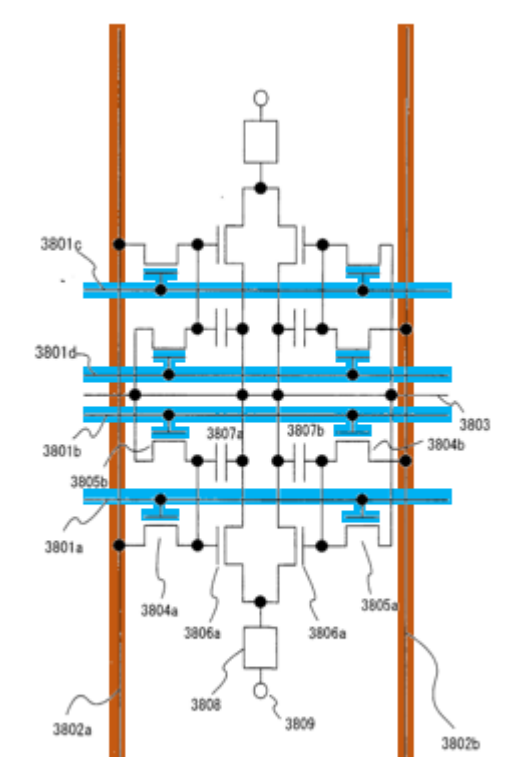


FIG. 7

IX. GROUND 1A

89. In my opinion, Inukai 576 anticipates claim 1. Additionally, in my opinion, Inukai 576 renders obvious claim 1.

90. Inukai 576 discloses an “electro-optical device.” *See* EX-1007 at Title, Abstract, [0002], [0436]-[0437], [0442]-[0443], Figs. 24A-24F. It discloses a number of electronic devices that incorporate displays, which the ’760 patent identifies as “electro-optical devices.” *See* EX-1001 at 1:18-21, 9:60-67, 23:55-24:46, Figs. 15A-15F. For example, the “EL monitor” depicted by Figure 24A of Inukai 576 is an electro-optical device.

91. Inukai 576 discloses a “data line,” “control line,” and a “unit circuit arranged corresponding to an intersection of the data line and the control line.”

92. The reference’s “source signal line driver circuit 102” provides a “digital video signal . . . to the source signal lines S1 to Sx,” which includes source signal line Sj. EX-1007 at [0094]; *see also id.* at [0013], [0022]-[0025], [0070]-[0075]. These source signal lines are data lines because they provide data to the pixels. Moreover, Inukai 576 specifically refers to these lines as “data signal lines.” *See id.* at [0013].

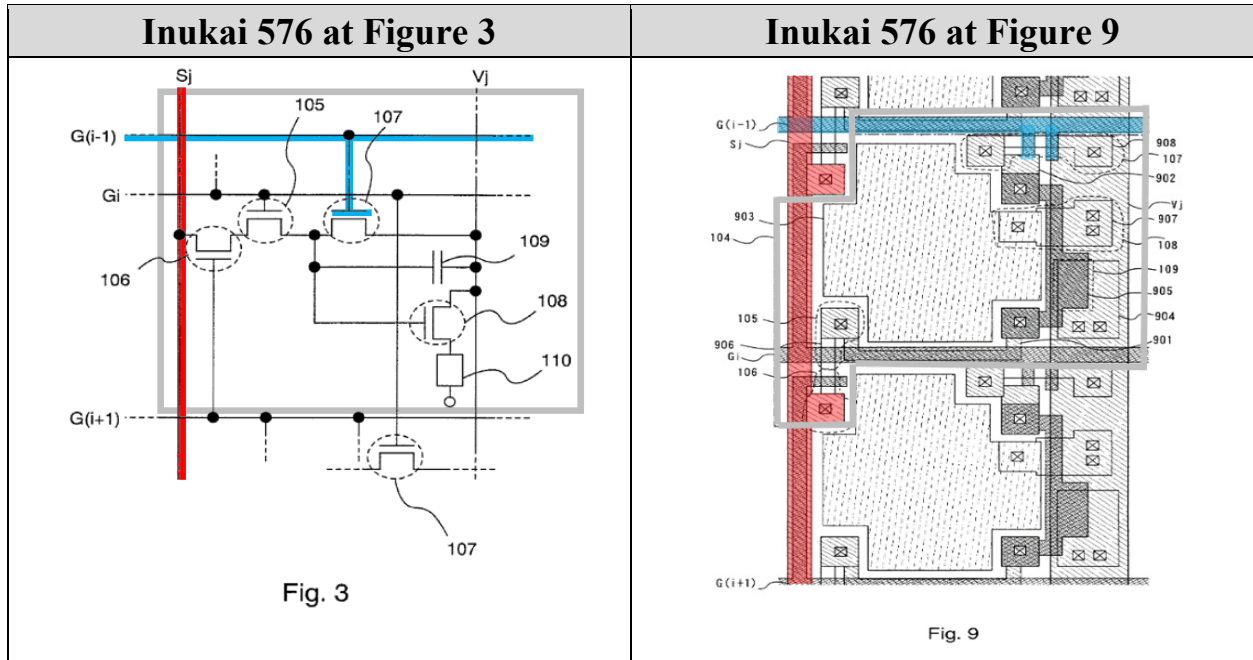
93. The reference’s “gate signal line driver circuit 103” provides a “gate signal” to “[g]ate signal lines G1-Gy,” which includes source signal line G(i-1).

EX-1007 at [0013]; *see also id.* at [0070], [0073]. These gate signal lines are control lines because they control when a given pixel will receive data by selectively turning its switching transistors on or off. *See id.* at [0093]-[0094]; EX-1001 at 17:63-65.

94. “Unit circuit” is not a definitive term of art. The ’760 patent does not specifically define the term, but generally uses the term to refer to a collection circuit elements. *See* EX-1001 at 2:54-67, 4:3-29, 4:37-48, 9:11-23. Inukai 576 discloses such a unit circuit corresponding to the intersection of a data line and a control line. For example, Inukai depicts the “circuit diagram of the pixel 104” in both schematic view and plan view. *See* EX-1007 at [0075]-[0077], Fig. 3, Fig. 9. In these depictions, gate signal line G(i-1) controls erasing TFT 107, gate signal line G(i) controls switching TFT 105, and gate signal line G(i+1) controls switching TFT 106. Source signal line S_j provides a data signal to driving TFT 108 through the two switching TFTs. Thus, one could identify these elements by combinations of gate signal lines and source signal lines, such as S_j and G(i) or S_j and G(i-1). Either combination of lines defines a “unit circuit” consisting of the circuit elements discussed above.

95. For purposes of this declaration, an example of a unit circuit (indicated by the gray outline) includes TFTs 105, 106, 107, 108, capacitor 109, and EL element 110 that correspond to the intersection of the data line S_j (highlighted in

red below) and control line $G(i-1)$ (highlighted in blue below).



96. Inukai 576 discloses “a first transistor that includes a first semiconductor film, an “electro-optical element electrically connected to one of a source or a drain of the first transistor,” “a second transistor that includes a second semiconductor film, the second transistor connected between the one of the source or drain and a gate of the first transistor,” and “a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor according to a data signal.”

97. Inukai 576 discloses “TFTs” which stands for “thin film transistor.” For purposes of this declaration, the “TFT 108 for EL driving” constitutes a first transistor and “TFT 107 for erasing” constitutes a second transistor. *See* EX-1007 at [0224]-[0225], Fig. 3, Fig. 9. Inukai 576 also discloses “EL element 110” that “emits light when the power source potential is applied to the pixel electrode.” *See id.* at [0077], [0084-[0085]. EL element 110 is thus an “electro-optical element.” *See* EX-1001 at 1:63-2:5 (defining electro-optical element as “general elements which emit light”). Inukai 576 also discloses a “capacitor 109” which constitutes a holding element. *See* EX-1001 at 2:17-18 (identifying capacitors as an example of a holding element). Figure 3 has been highlighted below to identify Inukai 576’s disclosure of first transistor (TFT 108 in orange), second transistor (TFT 107 in green), electro-optical element (EL element 110 in pale blue), and holding element (capacitor 109 in pale red).

**Inukai 576 at Fig. 3
(Schematic, Data Line S_j highlighted)**

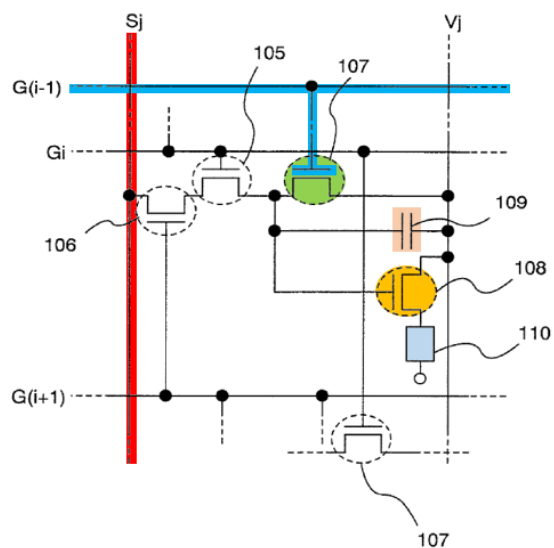


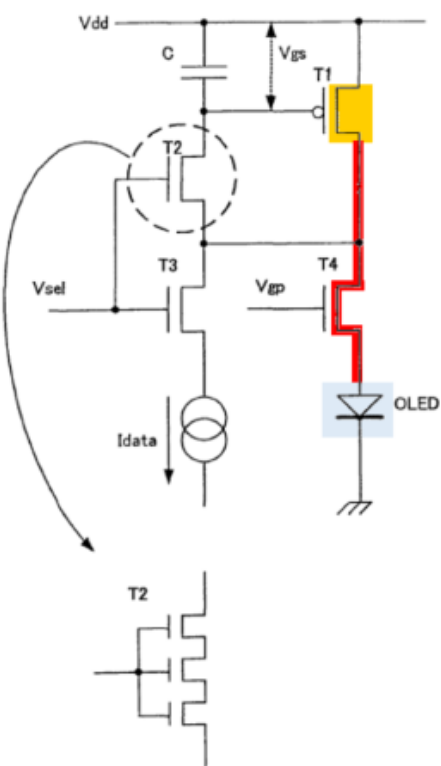
Fig. 3

98. Inukai 576's circuit elements are also connected to one another in the manner claimed by the '760 patent. The electro-optical element (110) is "electrically connected" to "one of a source or a drain of the first transistor." Specifically, Inukai 576 discloses that the EL element 110 is connected to TFT 108's drain region. *See* EX-1007 at [0082]. Furthermore, by being connected to TFT 108's drain, EL element 110 is also "electrically connected" to TFT 108's source.

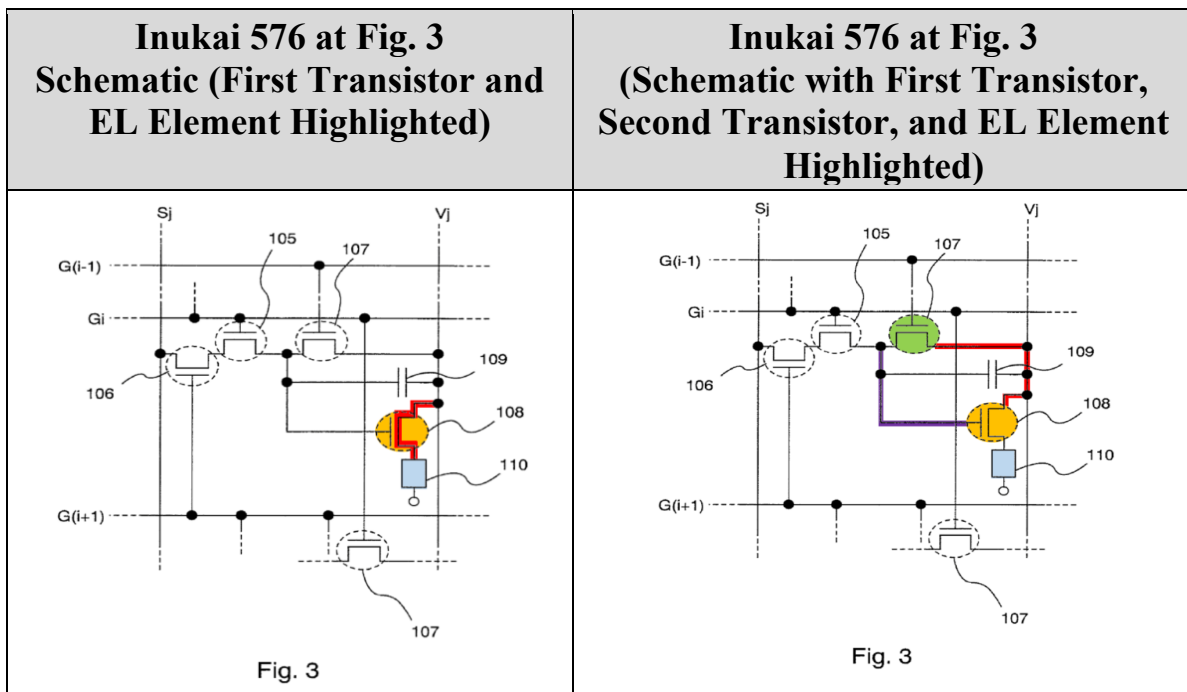
99. "Electrically connected" as used by the '760 patent, refer to two points being connected by an electrical path that allows signals to flow from one point to another. Transistors include drains and sources that are connected to each other by a channel. Thus, one circuit node can be "electrically connected" to another node if the two nodes are connected through a transistor that allows a signal to pass from one node to another when the transistor is turned on. The '760 patent demonstrates this concept through figure 5, which shows an electro-optical element being "electrically connected" to transistor T1 through transistor T4. Moreover, during prosecution of the Japanese counterpart to the '760 patent, the Japanese examiner stated "being 'electrically connected' recited in amended claims 1 and 2 obviously includes connections other than a 'serial connection.'" *See id.*; EX-1004 at 272.

**'760 Patent at Fig. 5
(Electro-optical element (OLED)
is Electrically Connected to
First Transistor (T1) Through (T4))**

Fig.5



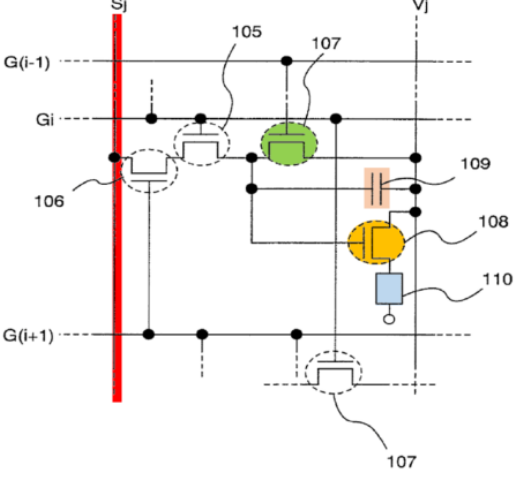
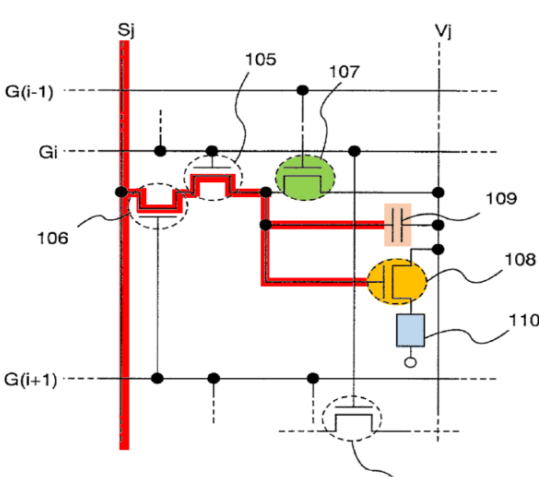
100. Applying that principle here, EL element 110 is electrically connected to a node that corresponds to the source of TFT 108 (and line Vj) through TFT 108 itself. The second transistor (107) is “connected” between TFT 108’s source and its gate. *See* EX-1007 at [0080]-[0082]. Specifically, TFT 107 connects to “power supply line Vj,” which is the same node to which TFT 108’s source connects. Thus, TFT 107 and EL 110 connect and electrically connect, respectively, to the same node (TFT 108’s source). The figures below use red lines to show how EL 110 electrically connects to this node and how TFT 107 connect to this node. The figure on the right uses a purple line to show how TFT 107 connects to the gate of TFT 108.



101. The capacitor (109) connects to TFT 108’s gate and holds a gate voltage to it according to a data signal. “The capacitor 109 is provided for the purpose

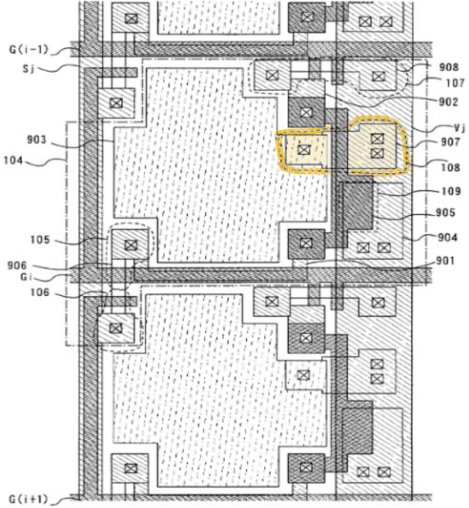
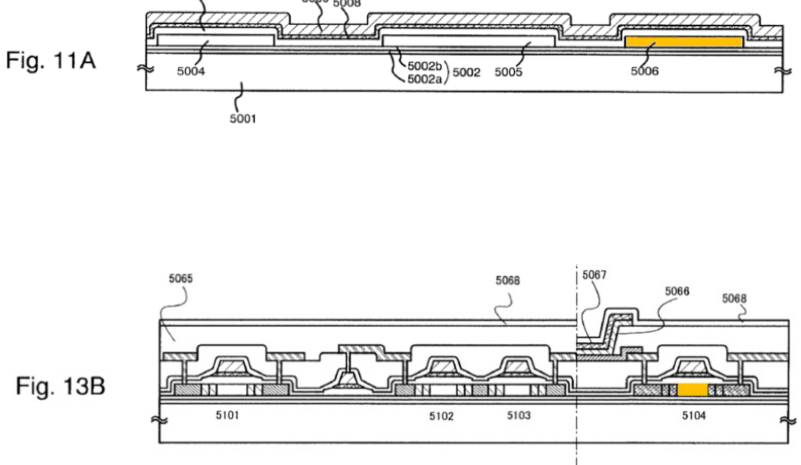
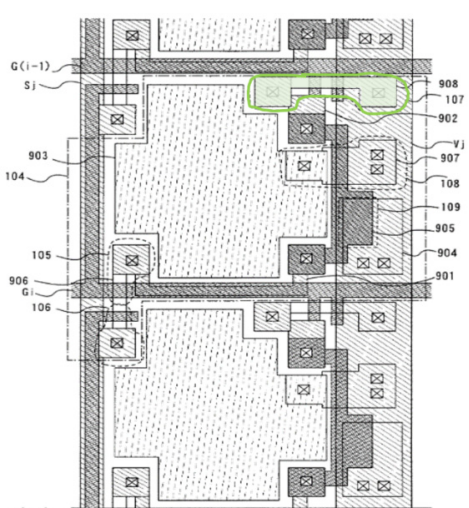
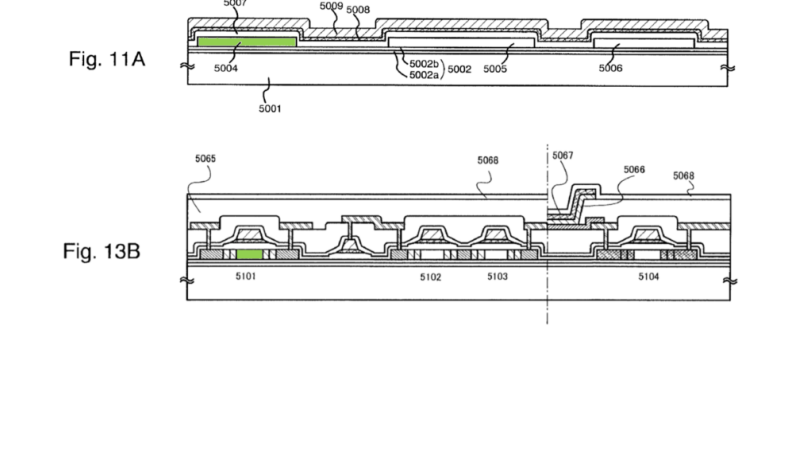
of retaining the gate voltage of the TFT 108 for EL driving when the TFT 107 for switching is in a nonselected state (an OFF state).” EX-1007 at [0081]. “When the first TFTs 105 for switching and the second TFTs 106 for switching are simultaneously in the ON state, a first bit of a digital video signal is inputted from the source signal line driver circuit 102 to the source signal lines S1 to Sx.” *Id.* at [0094]. “The first bit of the digital video signal is inputted through the first TFTs 105 for switching and the second TFTs 106 for switching to the gate electrodes of the TFTs 108 for EL driving of the pixels in the first line.” *Id.* As I discussed above, the source signal lines are data lines. *See id.* at [0013].

102. The figures below use red to show the path taken by a data signal. When the switching TFT 105 and 106 are off, with respect to the pixel depicted, the data signal is confined to the source signal line S_j. When these TFTs are turned on, however, the data signal can propagate through the provided circuitry to both the gate of the TFT 108 and to the capacitor 109. The purpose of a capacitor is to store a voltage or signal, and it does so in this circuitry below. If the switching TFTs are subsequently turned off, the capacitor can still hold this data signal to the gate of transistor 108.

Inukai 576 at Fig. 3 (Illustrating in red path taken by data signal when switching TFTs 106 and 105 are OFF)	Inukai 576 at Fig. 3 (Illustrating in red path taken by data signal when switching TFTs 106 and 105 are ON)
 Fig. 3	 Fig. 3

103. Inukai 576's first and second transistors have first and second semiconductor films, respectively. Transistors in general require a semiconductor film as part of the channel region that connects the source to the drain. Inukai 576 reflects this property by disclosing "active layers" that constitute semiconductor films. *See* EX-1007 at [0002]-[0004], [0254]. The first transistor "TFT 108 for EL driving has an active layer 907" (*id.* at [0225]), and the second transistor "TFT 107 for erasing [that] has an active layer 908" (*id.* at [0224]). Active layer 907 thus is a first semiconductor layer, and active layer 908 is a second semiconductor layer.

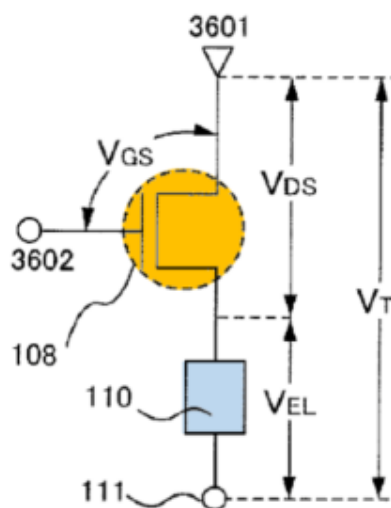
104. The reference depicts a series of cross section images that show how these TFTs are formed. *See id.* at Figs. 11-14. Figure 11A shows an early stage in this process in which active layers (which at an initial stage are "semiconductor layers" 5006 and 5004) are deposited. *See id.* at [0248]. Figure 13B shows a later stage in which additional layers are provided to form a p-channel type TFT 5104, which can correspond to the driving TFT, and n-channel type TFT 5105, which can correspond to the erasing TFT. *See id.* at [0281]

Inukai 576 at Fig. 10 (Plan View with First Transistor and First Semiconductor Film highlighted)	Inukai 576 at Figs. 11A, 13B (Cross Sections with First Semiconductor Film highlighted)
 Fig. 9	 Fig. 11A Fig. 13B
Inukai 576 at Fig. 9 (Plan View with Second Transistor and Second Semiconductor Film Highlighted)	Inukai 576 at Figs. 11A, 13B (Cross Sections with Second Semiconductor Film Highlighted)
 Fig. 9	 Fig. 11A Fig. 13B

105. Inukai 576 discloses “the first transistor supplying a current based on the gate voltage of the first transistor.” A basic property of transistors is that they

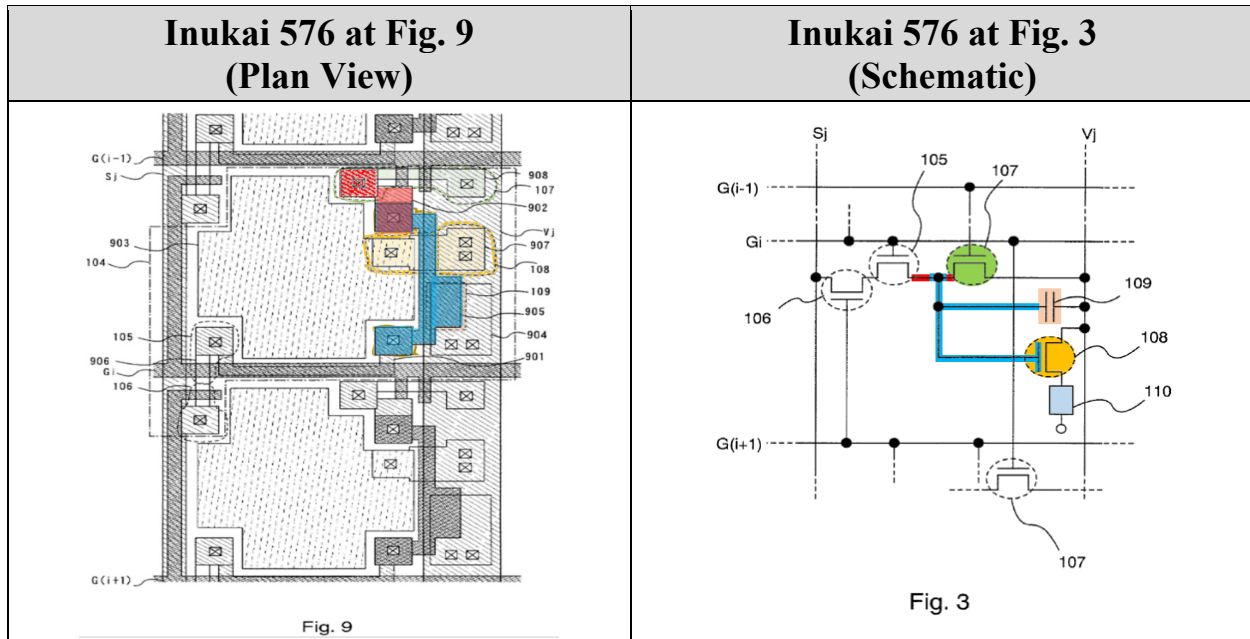
provide current based on the voltage applied to their gate. Inukai 576 expressly illustrates this property in figure 19A. Each “V” in this image represents a particular voltage from one point to another point. For example, V_{GS} represents the voltage from the gate to the source of a driving TFT 108 (which is the first transistor described above and shown in orange below). It supplies current to EL element 110 (which is the electro-optical element described above and shown in pale blue below). *See* EX-1007 at [0371] (disclosing that because “[t]he TFT 108 for EL driving and the EL element 110 are connected in series. . . , the amount of current flowing through the TFT 108 for EL driving and the amount of current flowing through the EL element 110 are the same”); *id.* at [0372] (“[A]s $|V_{GS}-V_{TH}|$ of the TFT 108 for EL driving becomes larger, in other words as $|V_{GS}|$ becomes larger, the amount of current flowing through the TFT 108 for EL driving becomes larger.”); *see also id.* at [0082].

Fig. 19A



106. Inukai 576 discloses “a wiring connected between the second transistor and the gate of the first transistor” that is “formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film are formed” but also has a “portion formed in the layer different from a gate layer in which the gate of the first transistor is formed.” A POSITA would have understood the “wiring” discussed in the ’760 patent to mean a conductive material, since such a material would allow a signal to flow between the two points. Inukai 576 discloses such a wiring: “One of a source region or a drain region of the TFT 107 for erasing” (the second transistor) “is connected to the gate electrode of the TFT 108 for EL driving” (the first transistor). EX-1007 at [0080].

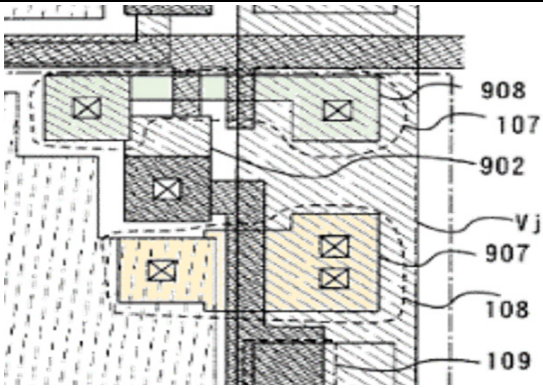
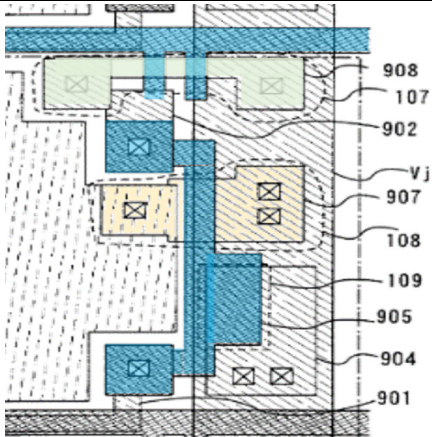
107. Figure 9 depicts a plan view of the wiring that connects those transistors. This wiring consists of gate wiring 905 and connection wiring 902. *See* EX-1007 at [0224] (“The gate wiring 905 is connected through a connection wiring 902 to one of a source region and a drain region of the TFT 107 for erasing.”). The blue region represents the gate layer (“gate wiring 905”) that forms the gate of TFT 108. It extends towards the top of the figure to reach a contact hole (signified by the “X” in a box) that connects it to a region at a higher layer, marked as “connection wiring 902.” That region connects to a source or drain of TFT 107 through another contact hole (also signified by an “X” in a box). That region (“connection wiring 902”) constitutes the wiring “portion” recited by the ’760 patent.

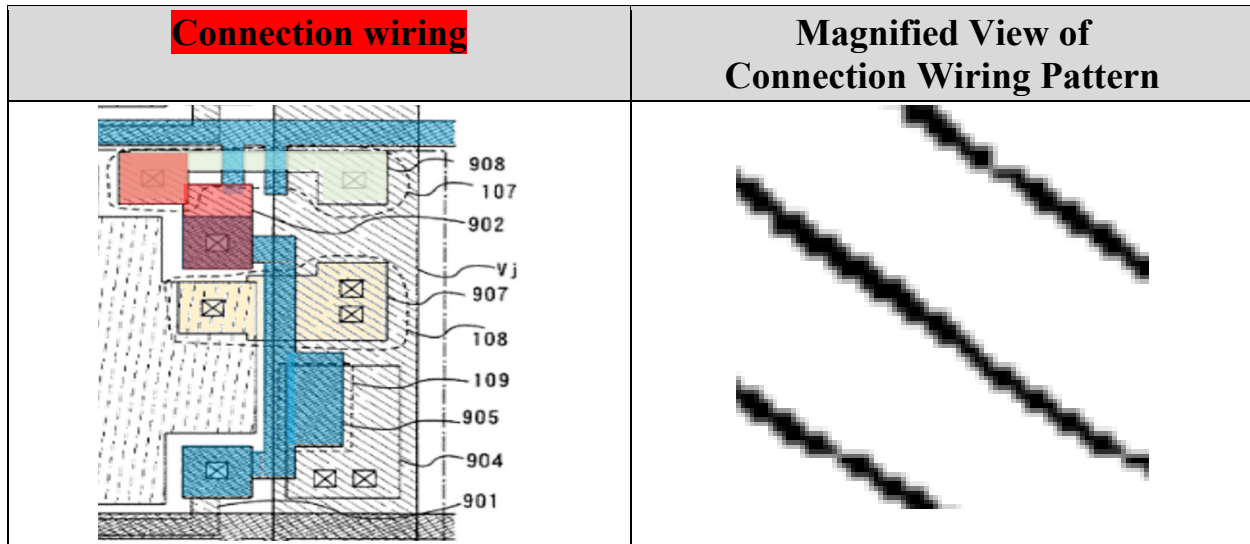


108. Inukai 576 further discloses that this “portion” is formed at a different layer from the layer in which the semiconductor films are formed and the layer in which the first transistor’s gate is formed. Inukai 576 adopts a convention that uses different “hashing patterns”—such as diagonal lines that consistently point to the right—to indicate different layers. The magnified views below illustrate these different patterns. The semiconductor film layer is shown by a “blank” pattern, the gate layer is shown by a “rectangular grid” sort of pattern, and the connection wiring layer is shown by diagonal lines that points down and to the right. See EX-1007 at [0251], [0224].

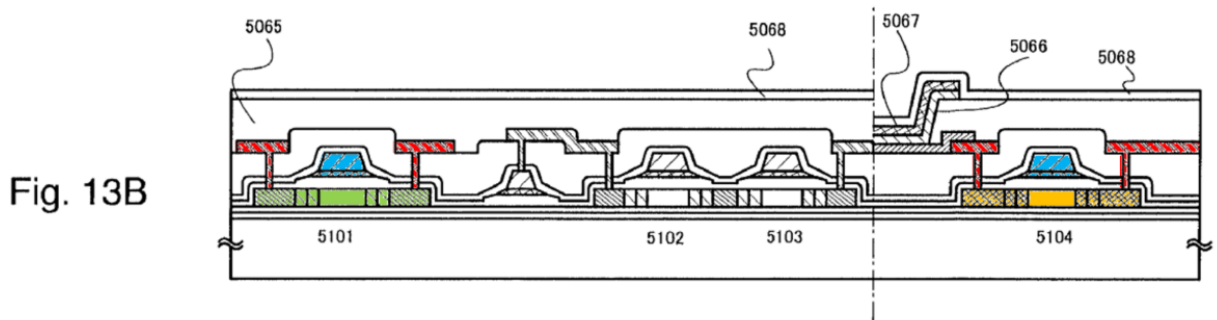
109. “The gate wiring 905 is connected through a connection wiring 902 to one of a source region and a drain region of the TFT 107 for erasing.” EX-1007 at [0224]. As shown by the images below, “connection wiring 902” corresponds to a

layer illustrated by lines that point diagonally, which is different from the gate layer (“rectangular grid” pattern) and the semiconductor film layer (“blank” pattern).

First Semiconductor Film and Second Semiconductor Film	Magnified View of Semiconductor Film Pattern
	
Conductive Film for Gates	Magnified View of Conductive Film for Gates Pattern
	



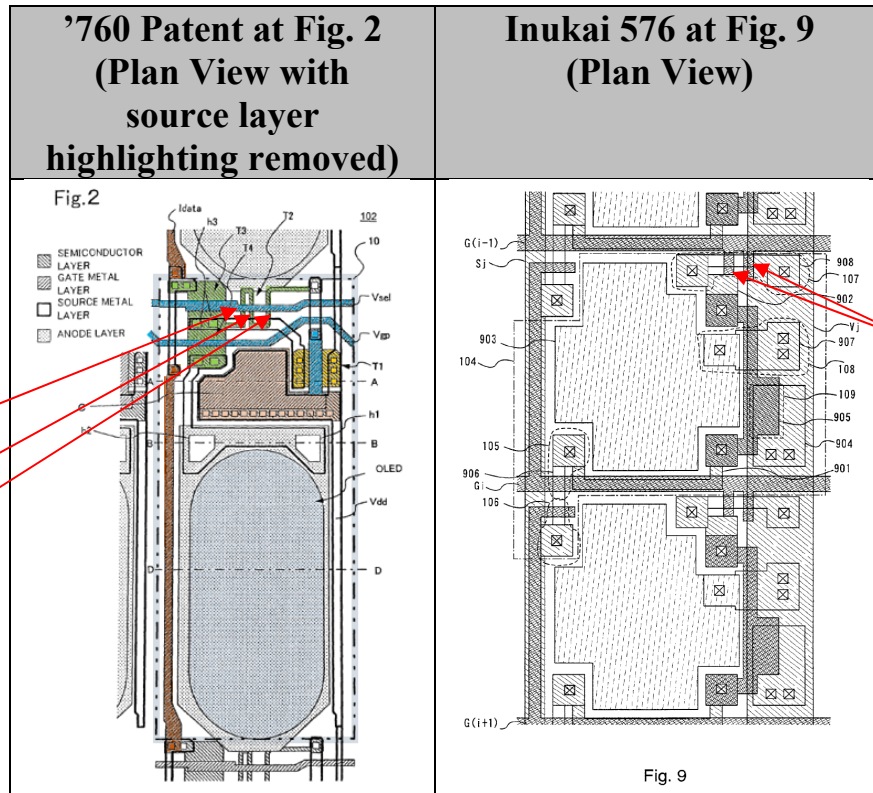
110. Inukai 576's figure 13B also shows these layers. TFT 5101 is a TFT for erasing (second transistor TFT 107), 5102 is a first switching TFT (TFT 105), 5103 is a second switching TFT (TFT 106), and TFT 5104 (TFT 108) drives the EL element.



111. Inukai 576 discloses that the wiring's "portion" ("connection wiring 902") crosses "the control line." As shown in figure 9, two portions of the control signal line G(i-1) protrudes over the second transistor (erasing TFT 107). These portions form gate electrodes for the erasing TFT 107 to implement a multi-gate structure. This multi-gate structure serves the same purpose as the multi-gate

structure in the '760 patent, which is to reduce leakage current. *See* EX-1007 at [0307] (“The multi-gate structure is very effective in reducing OFF current.”); EX-1001 at 3:5-9 (“By adopting a multi-gate structure and an LDD structure, GDD structure, or DDD structure, the leakage current when the second transistor is in the turned-off state can be reduced, so that the electric charge accumulated in the holding element can be maintained for a long period of time.”).

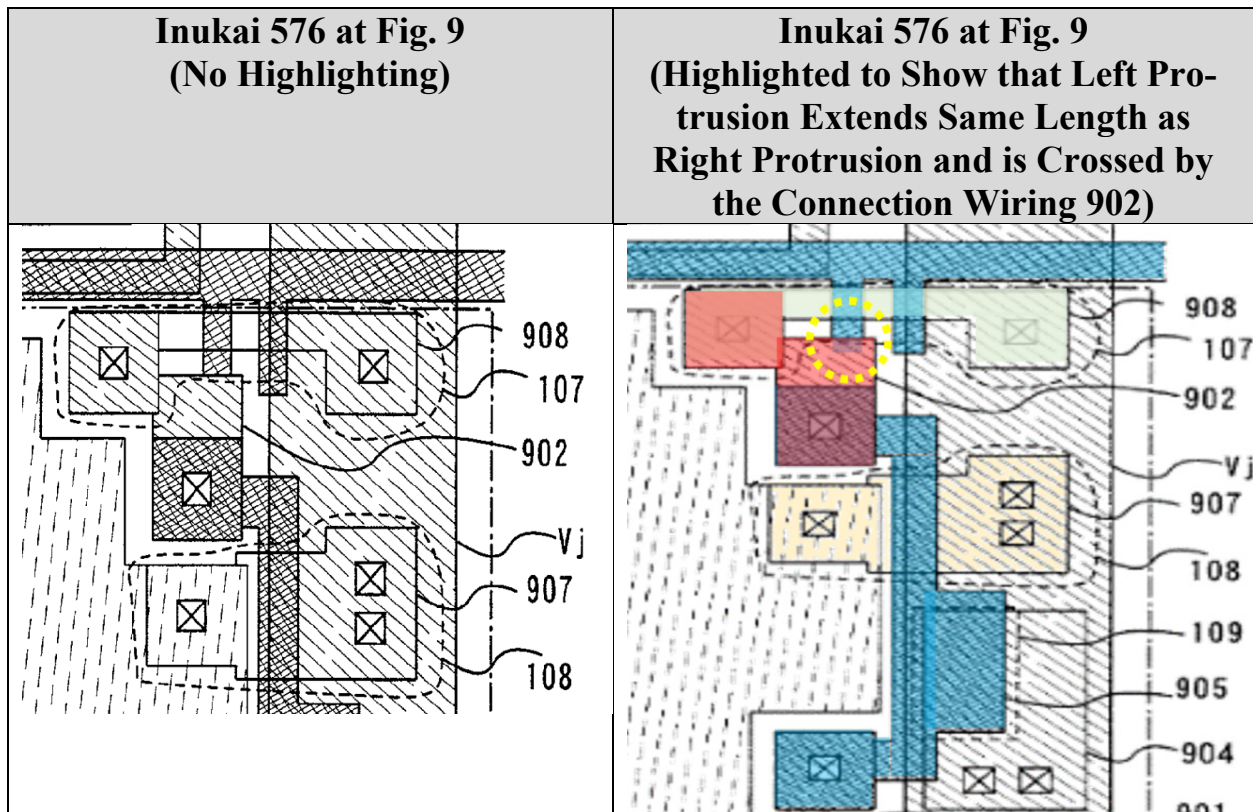
112. The '760 patent uses a control line (Vsel) in the same manner. As shown by the '760 patent at figure 2, a semiconductor layer (shown in green) snakes back and forth, like a river bending back on itself. A POSITA would have understood that the purpose of this pattern is to implement a multi-gate transistor. *See also* EX-1001 at Fig. 5 (showing that T2 is implemented with a multi-gate structure). The portions of Vsel that cross over T2 constitute gate electrodes of T2. U.S. 7,277,070 to Koyama, a comparable prior art reference, provides another example of using a gate signal line's portions as gate electrodes for a transistor, stating “writing gate signal line Gaj partially functions as gate electrodes of the first switching TFT 102 and the second switching TFT 103.” EX-1009 at 28:5–7.



Transistor T2 is implemented as a multi-gate structure

Transistor 107 is implemented as a multi-gate structure

113. In figure 9, because the connection wiring layer sits at a relatively higher layer, it obscures the left protrusion of the control signal line G(i-1) that it crosses. However, a POSITA would understand that the left side protrusion extends the same length as the right side protrusion. The yellow circle in the annotated version of figure 9 below shows where the crossing occurs.

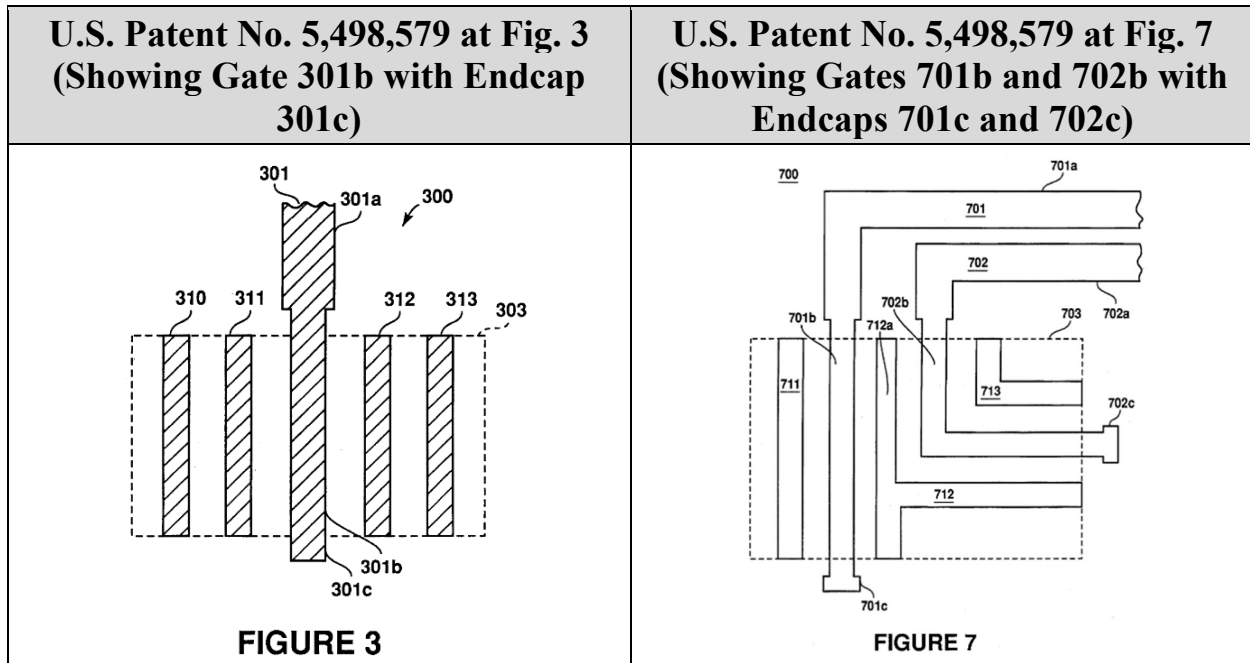


114. That the two protrusions extend the same length is a product of the “endcap” rule. This is a universal rule in semiconductor design requiring gates to have a certain minimum length beyond the semiconductor layer it intersects. Since the purpose of the two protrusions are to serve as the two gates of the multi-gate

transistor 107 (in this case a double-gate transistor), a POSITA would have understood that an adequate extension of each of the gate (protrusion) beyond the semiconductor layer is necessary to ensure that the function of the transistor will not be compromised due to variations from printing and misalignments in the photolithographic process steps, and thereby be able to have enough contact area with the transistor's channel to exert sufficient control. The minimum adequate extension is commonly known as the gate endcap rule. A POSITA would further have known that in order to maintain a consistent current voltage characteristics for the double-gate transistors, the two channel portions of the double-gate structure would be made as uniformly identical as possible. The endcap rule applies to all gates fabricated in the transistor, so a POSITA would have understood that the two gates over transistor 107 have equal length. Thus, a POSITA would have understood that the two protrusions would extend equal distance beyond the semiconductor layer.

115. The endcap rule existed at the time of the '760 patent, as illustrated, for example, by U.S. Patent No. 5,498,579. It states that "polysilicon line 301" has a "portion 301b which forms the gate of a transistor" as well as an "endcap 301c extends a distance beyond diffusion region 303" and "ensures that any rounding which occurs at the end of a polysilicon line occurs over the field, and not the active region 303, as rounding over the active region 303 may lead to punch-

through.” *Id.* at 4:21-33; *see also id.* at 6:11-17 (“As shown, gates 701b and 702b have endcaps 701c and 702c, which prevent punch-through at the edge of the diffusion region 703.”). The ’579 patent also confirms that gate endcaps have the same length, which in a preferred embodiment is 0.24 μm .



116. Moreover, it is my opinion that a POSITA would have found it obvious that Inukai 576’s connection wiring 902 extends over the control line G(i-1). As I discussed above, a POSITA would have been motivated to ensure the control line’s gate protrusions extend far enough so that they can exert control over the transistor, as a product of the endcap rule. Given that the right gate extends a certain length, there would be no reason why the left gate should be shorter or have a different length. Thus, applying the “endcap rule” principle to Inukai 576 would have resulted in the connection wiring extending over the control line.

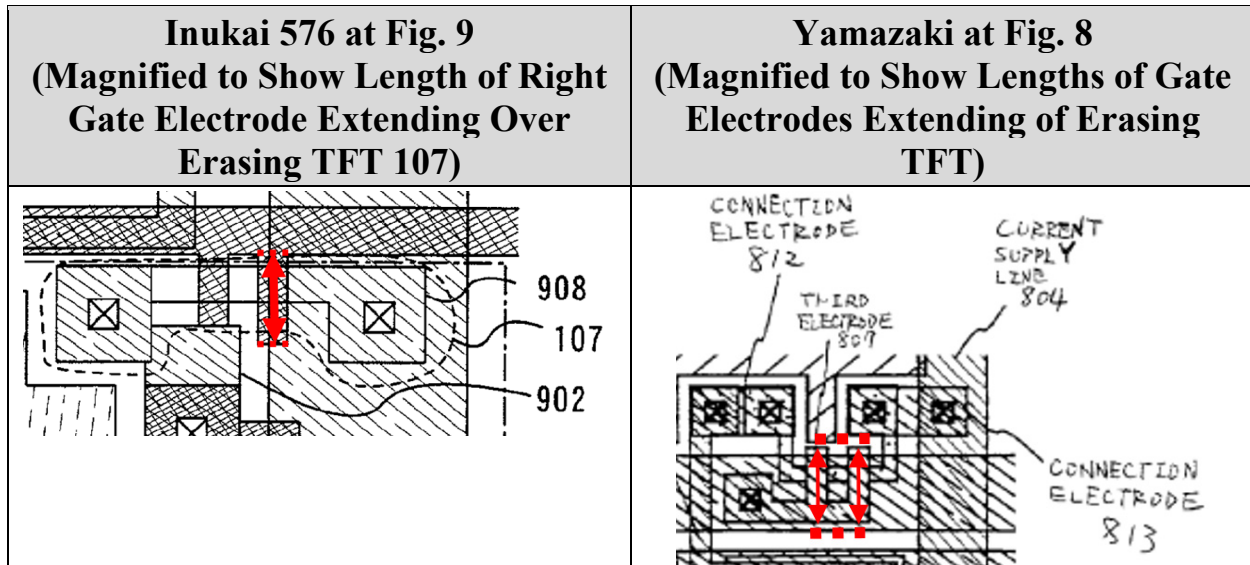
X. GROUND 1B

117. In my opinion, Inukai 576 in view of Yamazaki renders obvious claim 1.

118. A POSITA would have been motivated to combine the teachings of Inukai 576 and Yamazaki to implement Inukai 576 in such a manner that the two protrusions of control signal line G(i-1) depicted by Inukai 576's figure 9 plan view have equal length and the one on the left side extends far enough such that the wiring 902 crosses over it.

119. The references share a common inventor (Kazutaka Inukai) and assignees and pertain to the same sort of active matrix electroluminescent display. They also feature similar arrangements of circuitry to drive electro-optical elements. *See* EX-1007 at [0002]-[0036], [0077]; EX-1011 at [0002]-[0013], [0025]-[0028]. A POSITA would further have recognized that Yamazaki's techniques for preventing "deterioration of the device" and improves its "aperture ratio . . . without using a black mask and without increasing the number of masks" could potentially be beneficial to Inukai 576 and therefore be motivated to combine the references *See id.* at Abstract. Moreover, both references disclose a multi-gate "erasing TFT" which is illustrated as TFT 107 in Inukai 576 Fig. 9 and at the top right portion of Yamazaki Fig. 8. *See* EX-1007 at [0088]; EX-1011 at [0167]-[0168]

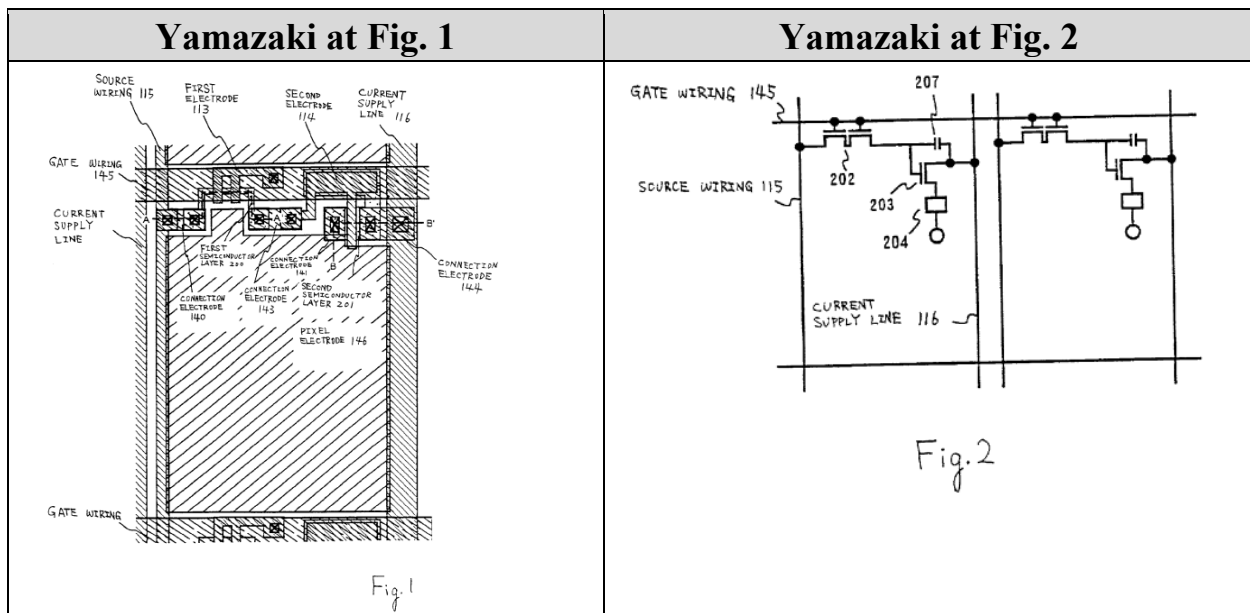
(identifying erasing TFT 906 as connected to other components through “connection electrode 812” and “connection electrode 809”). While Inukai 576 does not expressly show the length of the left-side erasing TFT gate depicted in its figure 9, Yamazaki shows the lengths of both the left-side and right side erasing TFT gates, as shown by the annotated figures below. A POSITA would have been motivated to look to Yamazaki as a source of how long the left side gate electrode could be and recognized that the left and right gates could have equal length, as taught by Yamazaki. A POSITA would have also had a reasonable expectation of success for this combination given that the gate electrode and connection wiring of Inukai 576 are formed in different layers and, by design, intended not to electrically short to one another. Because they are at different layers, they are electrically insulated from one another by an insulating film. *See* EX-1007 at [0267] (referencing inter-layer insulating films), Fig. 13A. This electrical isolation allows signals to pass over one another without shorting.

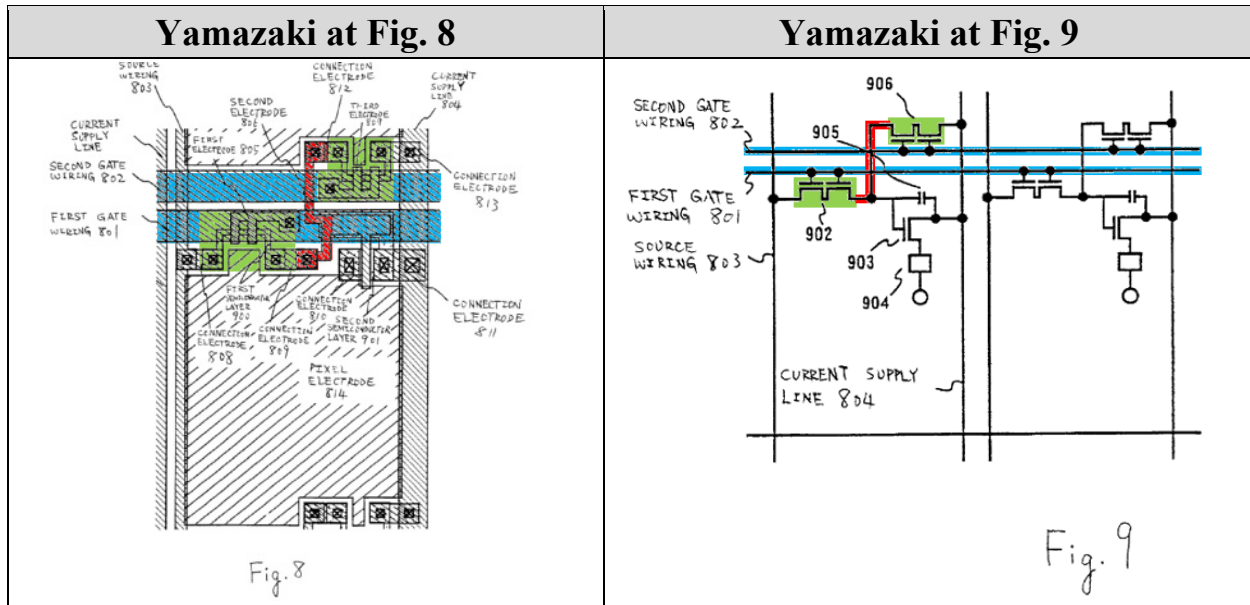


120. As discussed above, it is my opinion that Inukai 576 discloses or renders obvious the elements of claim 1 of the '760 patent. Moreover, Inukai 576 combined with Yamazaki would render obvious that the wiring portion (Inukai 576's connection wiring 902) is formed in a layer different from a gate layer in which the first transistor's gate is formed and that portion crossing the control line.

121. Yamazaki confirms my discussion above that it would have been obvious to a POSITA to implement Inukai 576's multi-gate transistors to extend equally far, which would have resulted in the gate electrode depicted on the left side of figure 9 extending at least as far as the gate electrode depicted on the right side of figure 9, so that the portion (902) crosses the left side electrode. Yamazaki discloses various multi-gate transistors, including switching TFT 202 in the schematic of figure 2 and the switching TFT 902 in the schematic of figure 9. See EX-1011 at EX-1011 at [0023], [0061]-[0062], [0174], Figs. 1-2, 8-9. Figures 1 and 8,

respectively, provide plan views illustrating how these multi-gate transistors can be laid out. In these plan views, each of the two gates of these transistors have equal length. *See* EX-1011 at [0055]-[0056] (referencing electrode 113, which implements the gates of TFT 202). A POSITA would have recognized in light of Yamazaki's teachings that each of the gates could advantageously extend the same length, in accordance with optimizing the layout under the "endcap rule" as discussed above. Moreover, Yamazaki's "Embodiment 7," as shown by the highlighted versions of figures 8 and 9, feature a wire (shown in red) that connects two transistors (shown in green) by crossing control lines (shown in blue).





XI. GROUND 2A

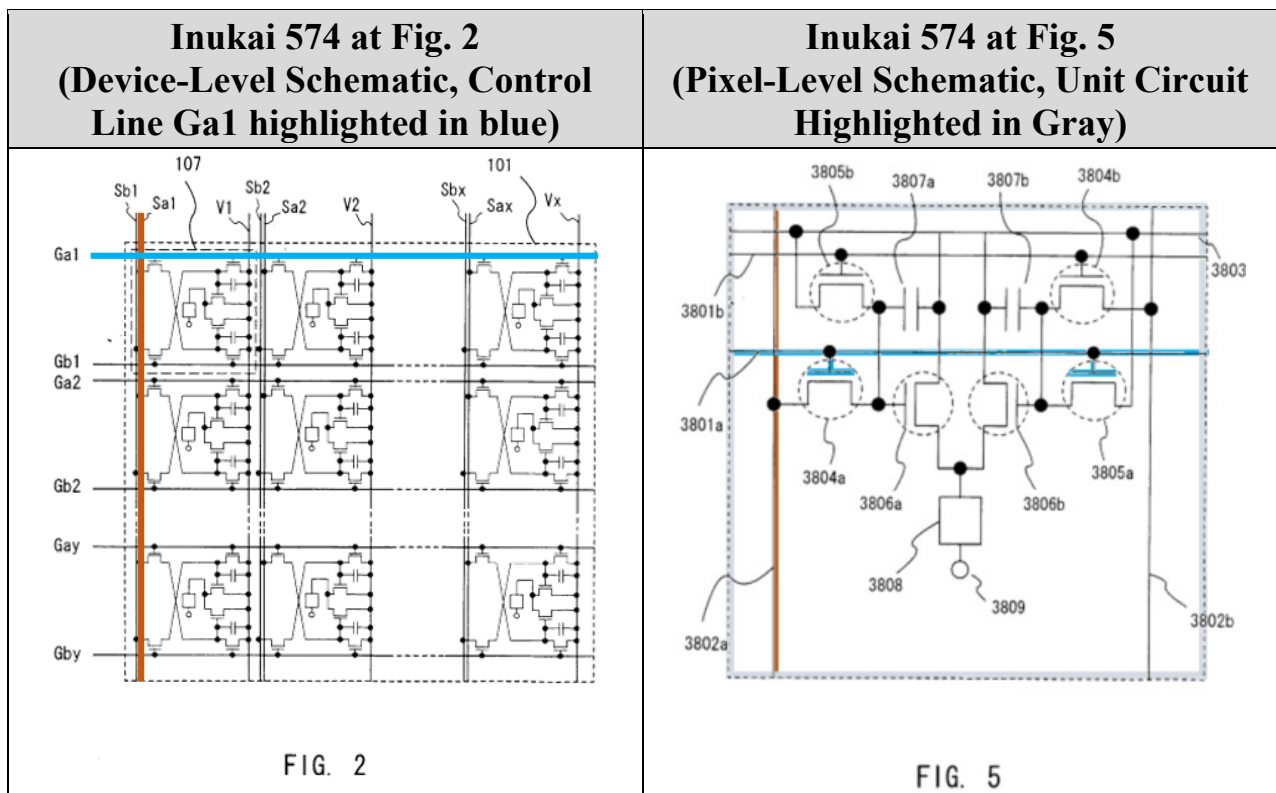
122. In my opinion, Inukai 574 anticipates claim 1. Additionally, in my opinion, Inukai 574 renders obvious claim 1.

123. Inukai 574 discloses an “electro-optical device.” EX-1008 at Title, [0001], [0382]-[0396], [0384], Figs. 26A-26F, 27A-27B.

124. Inukai 574 discloses a “data line,” “control line,” and a “unit circuit arranged corresponding to an intersection of the data line and the control line.” Inukai 574 discloses “source signal line driver circuits (102, 104)” that provide “digital data signals” to “source signal lines.” *See* EX-1008 at [0092], [0083]-[0084]. These source signal lines are data lines because they supply data to pixels. *See id.* at [0010]. Inukai 576 also discloses a “(plurality of gate signal lines G1 to Gy) for inputting a gate signal from a gate signal line driver circuit is connected to a gate electrode of a switching TFT 1801 of the respective pixels.” EX-1008 at

[0010]. These gate signal lines are control lines because they determine when electro-optical elements receive data from the data signal line. *See id.* at [0010], [0017], [0020].

125. “Fig. 5 is a diagram showing a circuit configuration of a pixel of the EL display.” EX-1008 at [0079]. These pixel elements can be identified by a particular data line and a particular control line.



126. Inukai 574 discloses “a first transistor that includes a first semiconductor film, an “electro-optical element electrically connected to one of a source or a drain of the first transistor,” “a second transistor that includes a second semiconductor film, the second transistor connected between the one of the source or drain and a gate of the first transistor,” and “a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor according to a data signal.”

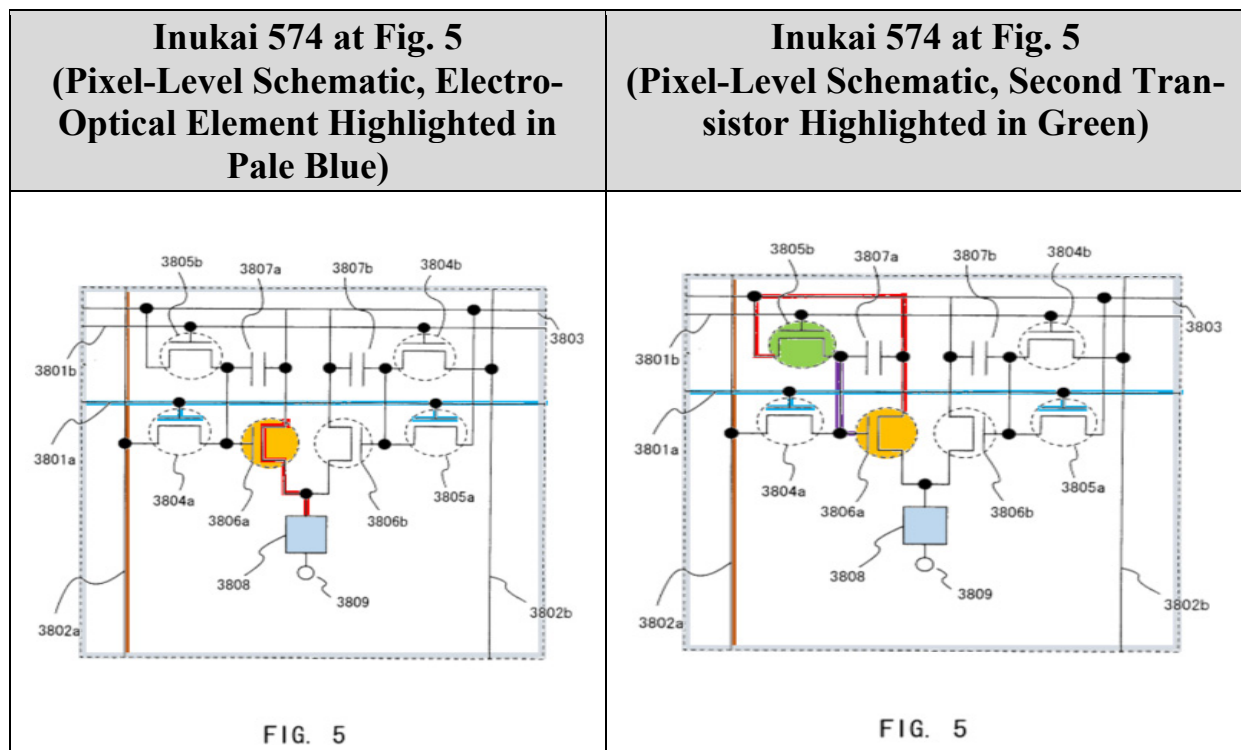
127. Inukai 574 discloses “TFTs” which stands for “thin film transistor.” For purposes of this declaration, the TFT 3806a, which “denotes a EL driver TFT” constitutes a first transistor (*see* EX-1008 at [0230]) and the TFT 3805b, which “denotes a[n] erasing TFT” constitutes a second transistor (*see id.* at [0230]). Inukai 576 also discloses EL element 3808, which constitutes an “electro-optical element.” *See id.* at [0230]. Inukai 576 also discloses capacitor 3807a, which constitutes a holding element. *See id.*

128. Inukai 574’s circuit elements are also connected to one another in the manner claimed by the ’760 patent. The electro-optical element (3808) is “electrically connected” to “one of a source or a drain of the first transistor.” Specifically, Inukai 574 discloses that “one of a source region and a drain region of the first EL driver TFT . . . is connected to the EL element.” EX-1008 at [0052]. Furthermore, by being connected to EL driver TFT 3806a’s source or drain, EL element 3808 is

also “electrically connected” to TFT 3806a’s other drain or source, respectively.

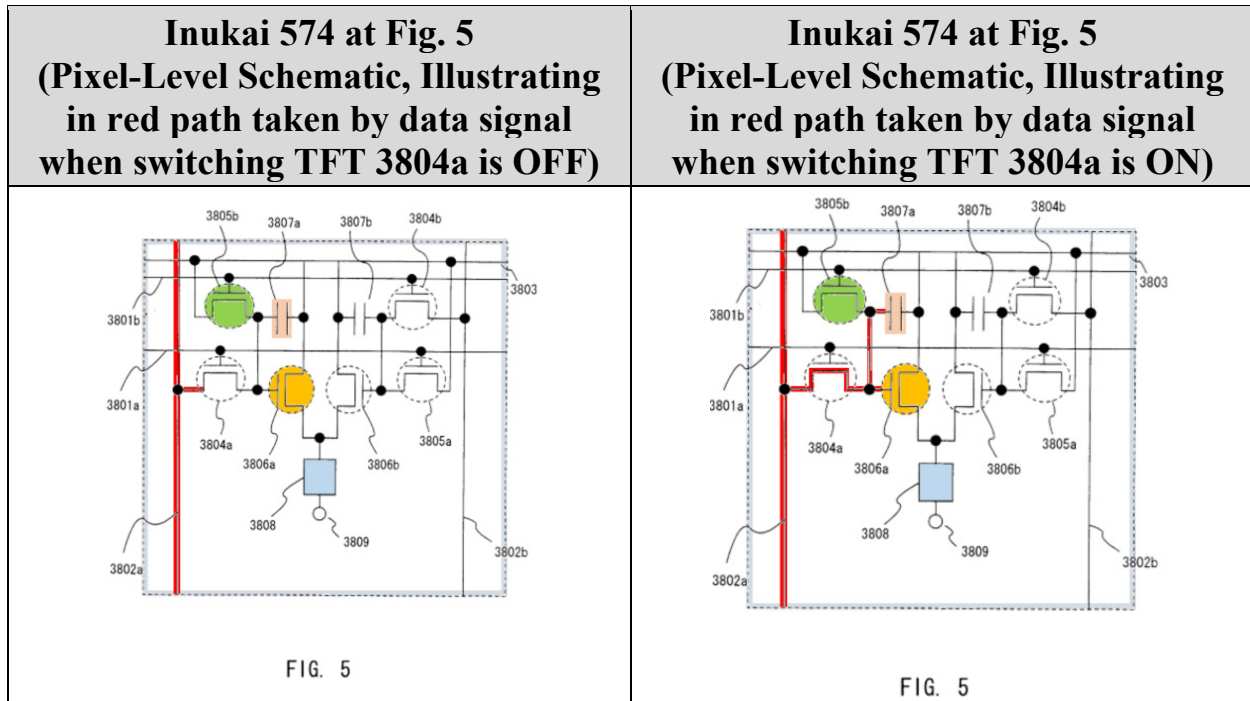
Similar to my discussion above with respect to Inukai 576, the EL element is “electrically connected” to both the source and the drain of the driving TFT.

129. The second transistor (TFT 3805b) is “connected” between TFT 3806a’s source or drain and its gate. *See* EX-1008 at [0230]. Specifically, TFT 3805b connects to “electric current supply line” 3803, which is the same node that TFT 3806a’s source or drain is connected to. Thus, TFT 3805b and EL 3808 connect and electrically connect, respectively, to the same node (TFT 3806a’s source or drain). The figures below use red lines to show how EL 3808 electrically connects to this node and how TFT 3805b connect to this node. The figure on the right shows how TFT 3805b connects to the gate of TFT 3806a.



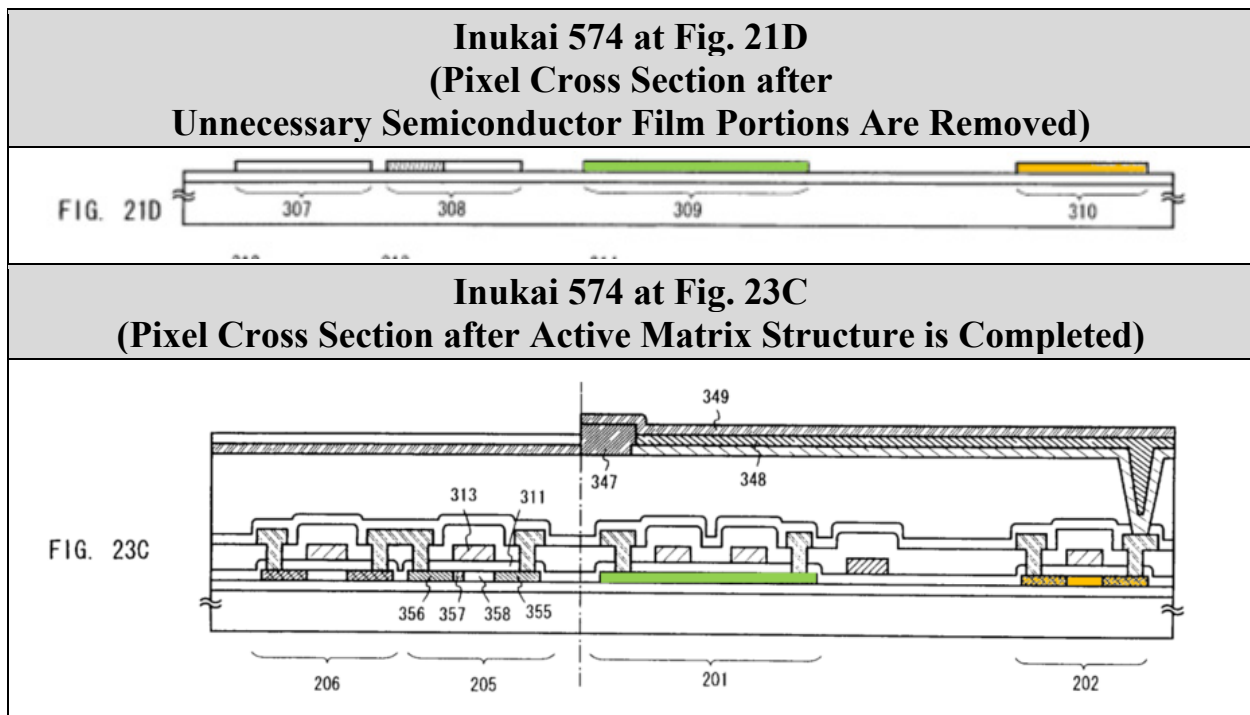
130. The capacitor (3807) connects to TFT 3806a's gate and holds a gate voltage to it according to a data signal. In the context of Embodiment 1, Inukai 574 discloses capacitors that are "provided for holding gate voltages of the EL driver TFTs." EX-1008 at [0230]. This same principle would have applied to Embodiment 5, as implemented by figure 5: A POSITA would have understood that by being connected to a gate of the EL driver TFT, the capacitor holds a voltage to it.

131. The figures below use red to show the path taken by a data signal. When the switching TFT 3804a is off, with respect to the pixel depicted, the data signal is confined to the source signal line 3802a. When this TFT is turned on, however, the data signal can propagate through the provided circuitry to both the gate of the TFT 3806a and to the capacitor 3807a. The purpose of a capacitor is to store a voltage or signal, and it does so in this circuitry below. If the switching TFTs are subsequently turned off, the capacitor can still hold this data signal to the gate of transistor 3806a.



132. Inukai 574's first and second transistors have first and second semiconductor films, respectively. Transistors in general require a semiconductor film as part of the channel region that connects the source to the drain. Inukai 574 reflects this property by disclosing "active layers" that constitute semiconductor films. There are "first" and "second" semiconductor films because the active layers for the transistors are described as "islands," meaning that they are not connected to one another but instead are distinct films. *See* EX-1008 at [0330] ("[I]sland shape semiconductor films (hereafter referred to as active layers) 307 to 310 are formed"); *see also id.* at [0292] ("[A]n erasing TFT 3504 can be using an p-channel TFT manufactured using a known method"), [0293] ("An EL driving TFT 3503 is using an n-channel TFT"), [0315], [0319].

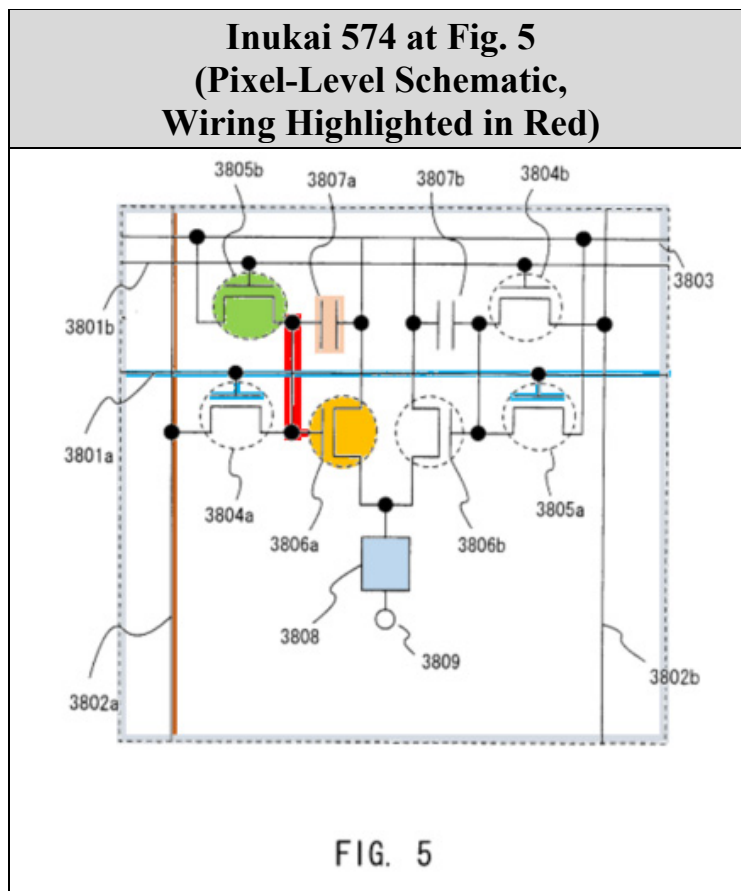
133. The reference depicts a series of cross section images that show how these TFTs are formed. Figures 21-23 show the “method of simultaneous manufacture of a pixel portion, and TFTs of a driver circuit portion formed in the periphery of the pixel portion.” *See id.* at [0317]. In the cross section figures shown below, element 310 represents the first semiconductor film that is used with “EL driver TFT 202,” which represents the first transistor. *See id.* at [0330], [0353], [0364]. In the cross section figures shown below, element 309 represents the second semiconductor film that is used with TFT 201, which represents the second transistor. *See id.* at [0330], [0353], [0363].



134. Inukai 574 discloses “the first transistor supplying a current based on the gate voltage of the first transistor.” “3803 denotes electric current supply

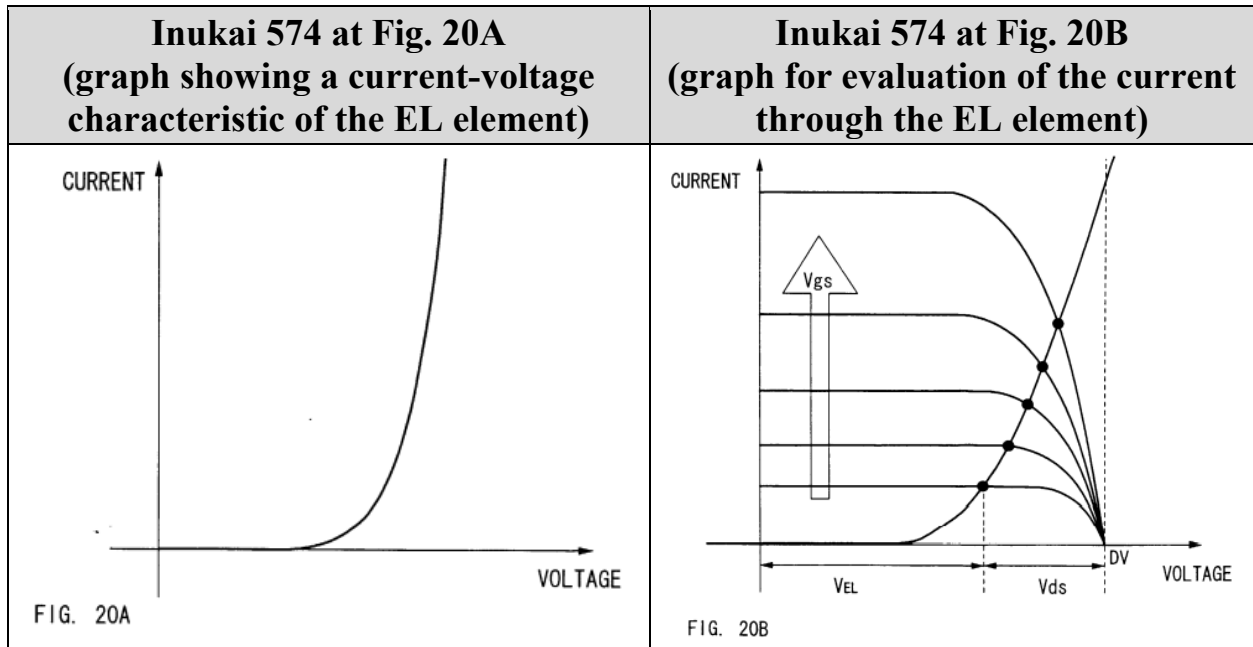
lines,” which are connected to the source or drain of the first transistor (3806a).

See EX-1008 at [0230], Fig. 5. The current supply from line 3803 connects to electro-optical element 3808 through the first transistor, as shown by the circuit diagram below. See EX-1008 at [0153]. As a basic property of a transistor 3806a, the amount of current supplied by the first transistor is based on the amount of voltage applied to its gate.



135. Inukai 574’s background section further acknowledges that supply of a current based on a transistor’s gate voltage is a basic operational principle of a transistor. See EX-1008 at [0024]-[0025] (“Fig. 20B is a graph for evaluation of

the current through the EL element, in which . . . V_{gs} [represents] a voltage applied between the gate and the source of the EL driver TFT (called gate voltage). . . . At this time, the current flowing through the EL element is determined in the one-to-one relationship with the gate voltage according to the current-voltage characteristic shown in Fig. 20B.”).



136. Inukai 574 discloses “a wiring connected between the second transistor and the gate of the first transistor” that is “formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film are formed” and has “a portion formed in the layer different from a gate layer in which the gate of the first transistor is formed, the portion crossing the control line.” As shown in figure 16 reproduced below, “drain wiring 31 of an erasing TFT 3504 [shown in green] is electrically connected to a drain wiring 35 of the switching TFT 3502 and a gate electrode 37 [shown in blue] of an EL driving TFT [shown in orange] by a wiring 36 [shown in red].” EX-1008 at [0291]; *see also id.* at [0293]. A POSITA would have understood that the wiring depicted by figure 16’s cross section could implement the circuit schematic of figure 5 because Inukai 574 discloses that these figures are directed at embodiments that may be combined. *See* EX-1008 at [0230]-[0231], [0308].

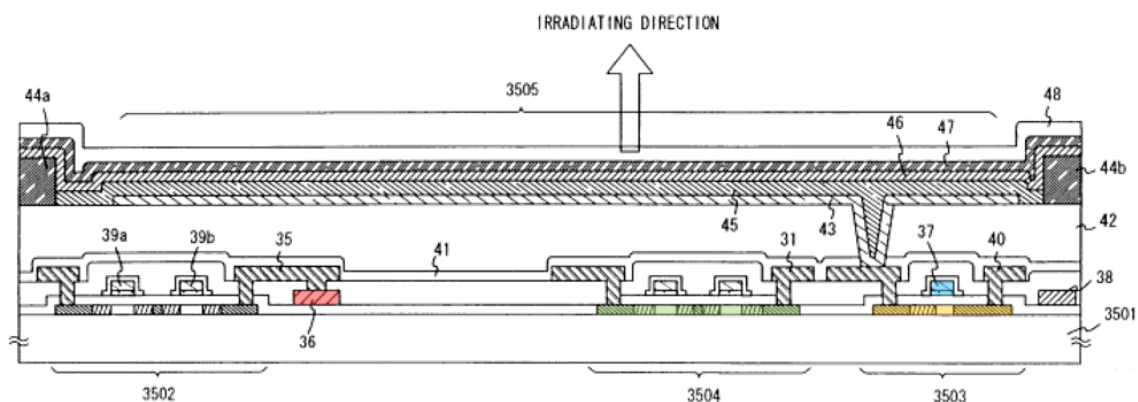
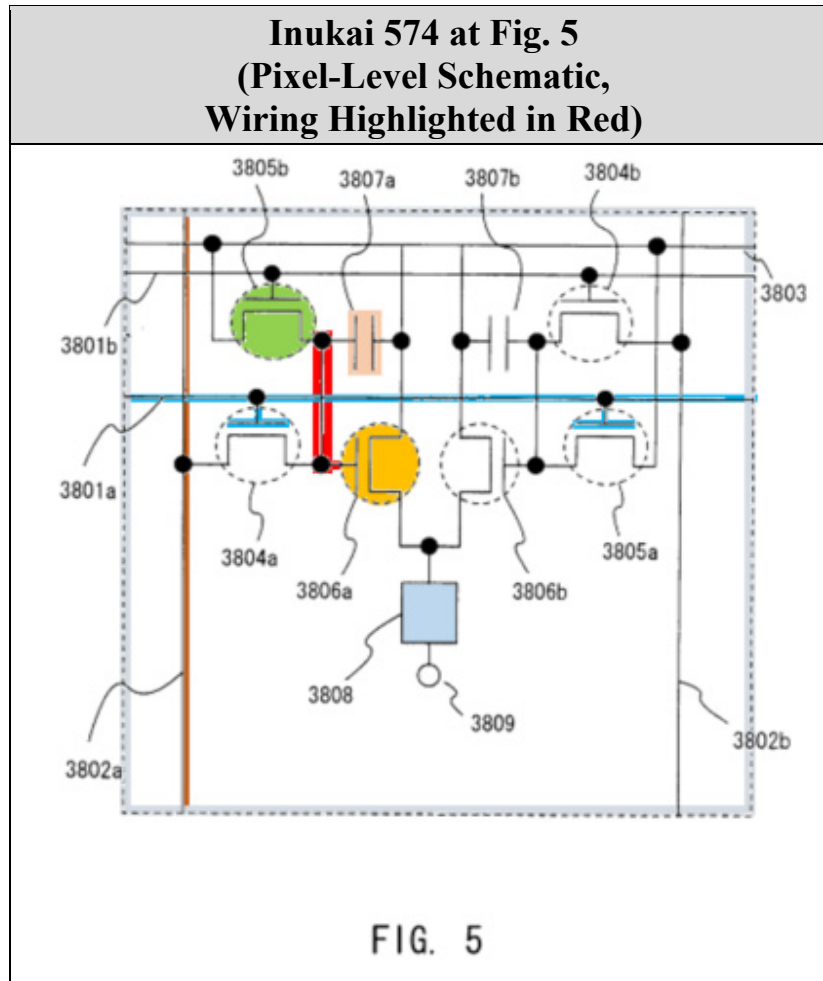


FIG. 16

137. Figure 5 below shows that wiring 36 that connects the gate of first transistor 3806a to second transistor 3805b crosses the control line 3801a. Inukai 574 teaches that in this particular schematic “the electric current supply line 3803 is formed parallel to the gate wirings 3801a and 3801b.” EX-1008 at [0231]. This schematic thus reflects not just how elements logically connect to one another, but also how those connections should be physically laid out. A POSITA would thus have understood Inukai 574’s figure 5 to be disclosing a potential layout in which the wiring crosses over the control line. Moreover, a POSITA would have found it obvious and advisable in light of this schematic to lay out the circuit such that the wiring crossed over the control line. Such an implementation could provide a smaller footprint for the circuit. Moreover, implementing a circuit schematic using a circuit layout that reflects the same sort of geometry depicted by the schematic would have been a matter of common engineering practice, and typically the most straightforward way to implement the schematic.



138. To the extent Inukai 574 does not explicitly disclose that the wiring's portion crosses a control line, a POSITA would have found it obvious to modify Inukai 574 in this manner. A circuit schematic can typically be implemented using a circuit layout that reflects the geometry depicted by the schematic. Sometimes, it can be the most straightforward way to implement the schematic. Inukai 574's schematic in particular describes physical properties of the circuit that lays it out in that it requires one line (i.e., the electric current supply line 3803) to be formed parallel to another (i.e., the gate wirings 3801a and 3801b). *See id.*; *see also* EX-

1001 at [0231].

XII. GROUND 2B

139. In my opinion, Inukai 574 in view of Yamazaki renders obvious claim 1.

140. A POSITA would have been motivated to combine the teachings of Inukai 574 and Yamazaki to implement Inukai 574 in such a manner that the schematic illustrated in Inukai 574's figure 5 would be implemented by a circuit layout that Inukai 574's wiring that connects the first transistor's gate to the second transistor would cross the control line.

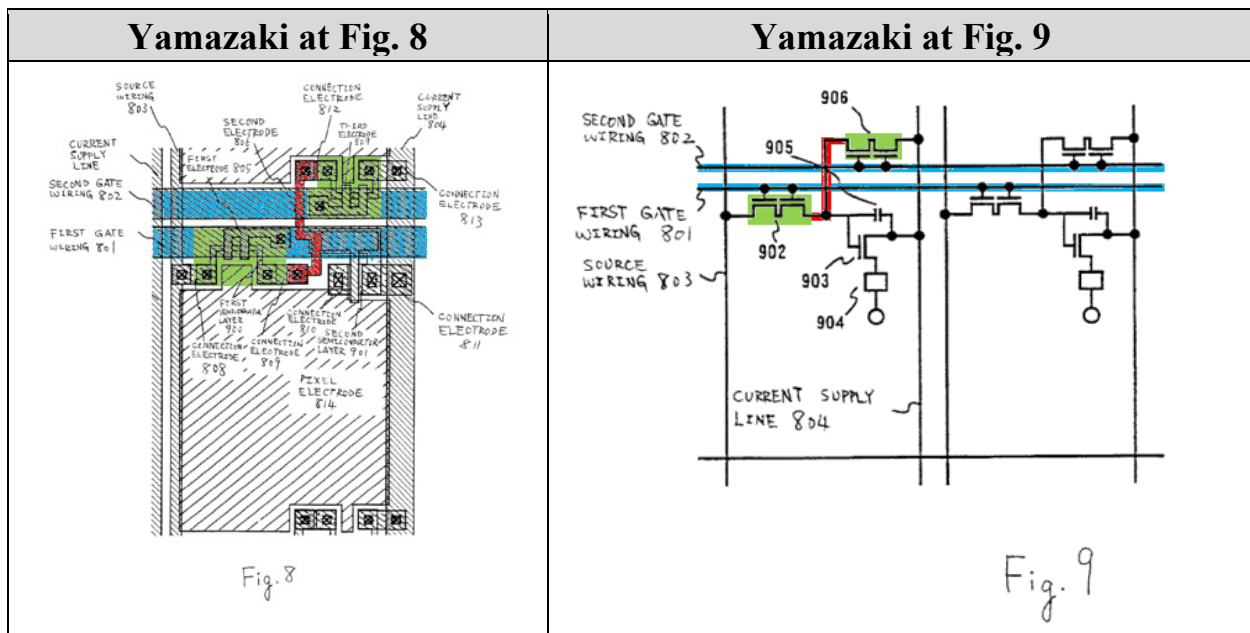
141. The references share a common inventor (Kazutaka Inukai) and assignees and pertain to the same sort of active matrix electroluminescent display. They also feature similar arrangements of circuitry to drive electro-optical elements. *See* EX-1011 at Abstract, [0002]-[0013], [0025]-[0028]. Moreover, because Inukai 574 does not provide a "plan view" to implement its schematic-represented circuitry, a POSITA would be motivated to look to Yamazaki for guidance as to how the circuit may be laid out. A "schematic" representation depicts how circuit elements are logically connected to one another with conductive wiring. A "plan view" or "top view" representation depicts how those elements are reduced to an equivalent physical form, which typically can track the schematic representation to a large extent. Yamazaki shows both sorts of views whereas Inukai 574

only shows schematic views. The circuits disclosed in these two references are similar in that they both disclose electro-optical elements, driving transistors, and erasing transistors, so a POSITA would have recognized that Yamazaki's teachings would provide examples as to how the Inukai 574's schematics could be reduced to an exact physical form. A POSITA would have also had a reasonable expectation of success that Inukai 574 and Yamazaki could be combined. Inukai 574 does not restrict the exact physical layout of how its circuit schematics would be implemented. Therefore, a POSITA would have recognized that certain of the implementation details disclosed in Yamazaki, like the fact that the schematic representation of a wiring connecting two transistors over a control line could be mirrored by a circuit lay out in which that wiring physically passes over the control line, could be applied to Inukai 574.

142. As discussed above, it is my opinion that Inukai 574 discloses or renders obvious the elements of claim 1 of the '760 patent. Moreover, Inukai 574 combined with Yamazaki would render obvious that the wiring portion (Inukai 574's wiring that connects the gate of transistor 3806a to transistor 3805b) is formed in a layer different from a gate layer in which the first transistor's gate is formed and that portion crossing the control line.

143. Yamazaki confirms my discussion above that it would have been obvious to a POSITA to implement Inukai 574's circuit schematic.

144. Yamazaki's "Embodiment 7" is depicted by a "pixel structure" plan view in figure 8 and an "equivalent circuit" schematic view in figure 9. *See* EX-1011 at [0164]-[0175], Figs. 8-9. These views depict a "switching TFT" (depicted as 902 in figure 9) connected to an "erasing TFT" (depicted as 906 in figure 9) through wiring that crosses over both the first gate wiring 801 and the second gate wiring 802 (as depicted in both views). *See id.* Yamazaki thus demonstrates that a circuit schematic, when reduced to physical form, can generally follow the same sort of geometry illustrated in the circuit schematic. A POSITA would have recognized that this same implementation of a wiring that crosses over a control line could have been implemented in Inukai 574.



XIII. CONCLUSION

145. I reserve the right to supplement my opinions to address any information obtained, or positions taken, based on any new information introduced throughout this proceeding.

146. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both (under Section 1001 of Title 18 of the United States Code).

By:  _____

David K. Liu, Ph.D.

March 15, 2023

APPENDIX A

DAVID KUAN-YU LIU, Ph.D.

42063 Benbow Drive, Fremont, CA 94539 • (510) 770-9449 or (510) 579-5029

www.davidkyliu.com davidkyliu@comcast.net

PROFESSIONAL PROFILE

- Technical expert with over 20 years of industrial experience in the development of advanced CMOS devices and process technology, with special emphasis on non-volatile semiconductor memory devices and process technology, and high-voltage semiconductor devices, with additional 12 years of experience serving as expert consultant.
 - Named inventor on 99 US patents.
- Consultant and expert witness for past 15 years in semiconductor intellectual property evaluation and patent litigation, with deposition experience and successful ITC trial testifying experience.
- Successful track record in transitioning products from development phase to high-volume manufacturing phase, both as an individual contributor and as manager/director.
- Co-founder of an LLC in the development and licensing of intellectual property with emphasis on embedded flash memory technology.
- Co-founder of a semiconductor memory start-up company (Progressant Technologies, Inc.); participated in its successful sale to Synopsys, Inc.
- Fluent in Mandarin Chinese (native language) and English; over 10 years experience as real-time translator of church sermons and proficient in written translation.

EDUCATION

Stanford University, Palo Alto, California

Ph.D., Electrical Engineering (1989)

Thesis: Physics and Technology of Novel Conductivity-Modulated Power MOSFET's

M.S., Electrical Engineering (1985)

Coursework in integrated-circuit technology, semiconductor device physics, computer modeling of semiconductor devices and fabrication processes, and solid-state physics

University of California, Berkeley, California

B.S., Electrical Engineering (1983)

Certificate of Distinction (awarded annually to the top EECS graduate)

KEY EXPERT WORK EXPERIENCE:

Case:	Netlist, Inc. vs. Samsung Electronics Co. Ltd. et al.,
Jurisdiction:	Civil Action No. 2:21-cv-00463 Eastern District of Texas
Work Product:	Expert relating to memory modules.
Nature of Case:	Civil action.
Counsel:	Retained by Fish & Richardson (Contact: Tony Nguyen)
Date:	8/22 – Current

Case: **Vervain, LLC vs. *Micron Technology* & related IPR Petition**
Jurisdiction: Action No. 6:21-cv-00487-ADA
Western District of Texas
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 4 patents, all 4 petitions instituted, and deposed on both initial declaration and reply declaration.
Counsel: Retained by Orrick, Herrington & Sutcliffe LLP (Contact: Jared Bobrow)
Date: 8/21 – Current

Case: **Monterey Research vs. *Qualcomm* PTAB Matter**
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Jones Day (Contact: David Cochran)
Date: 12/21 – Current

Case: ***Semiconductor Energy Laboratory Co., OLED Patent Matters***
Jurisdiction: Action No. 8:21-cv-00554-JAK-ADS
Central District of California
Work Product: Expert for infringement on 3 patents relating to OLED driver circuit and layout, responsibilities include source code viewing, GDS layers viewing, and claim charts review.
Nature of Case: Civil action.
Counsel: Retained by Fish & Richardson (Contact: Bryan Basso)
Date: 9/21 – 4/22

Case: ***Apple Inc. IPR Petition for U.S. Patents 6,622,108 & 6,807,505***
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Erise IP (Contact: Paul Hart)
Date: 8/21 – 9/21

Case: ***Texas Instruments IPR Petition***
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: Josh Griswold)
Date: 9/20 – 4/21

Case: ***Micron Technology vs. UMC/JinHua***
Jurisdiction: Case No. 4:17-CV-06932-MMC
United States District Court for the Northern District of California
Work Product: Testifying expert, trade secret documents review, and declaration submission.
Nature of Case: Trade secret contention of Micron confidential documents.
Counsel: Retained by Jones Day (Contact: Randy Kay)
Date: 3/17 – Current

Case: ***SK Hynix vs. BitMicro***
Jurisdiction: Investigation No. 337-TA-1097
United States International Trade Commission
Work Product: Testifying expert for non-infringement on 2 patents, issued expert rebuttal report, deposition taken, issued witness statement.
Nature of Case: ITC infringement case concerning module stacking of SDRAM.
Counsel: Retained by Fish Richardson (Contact: Joseph Colaianni)
Date: 11/18 – 4/19

Case: ***Rohm Company IPR Petition***
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: Matt Colvin)
Date: 4/18 – 8/18

Case: ***Apple Inc., vs. Qualcomm Incorporated***
Jurisdiction: Case No. 3:17-CV-02402
United States District Court for the Southern District of California
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration, 2 depositions taken.
Counsel: Fish & Richardson (Contact: Tony Nguyen)
Date: 1/18 – 5/19

Case: ***Macronix vs. Toshiba***
Jurisdiction: Investigation No. 337-TA-1046
United States International Trade Commission
Work Product: Testifying expert for infringement and non-invalidity on 2 patents, claim construction analysis, technical tutorial, database viewing for evidence gathering, issuing expert report and expert rebuttal report, deposition taken for 2 patents, issued witness statement and rebuttal witness statement, testified in ITC court on both infringement and invalidity.
Nature of Case: ITC infringement case concerning advanced NAND Flash memory.
Counsel: Retained by Fish Richardson (Contact: David Barken)
Date: 4/17 – 10/18

Case: *Novatek Microelectronics Corp. IPR Petition*
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Kroub, Silbersher & Kolmykov PLLC (Contact: Sergey Kolmykov)
Date: 2/17 – 4/17

Case: *Taiwan Semiconductor Manufacturing Company IPR Petition*
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: John Goetz)
Date: 7/15 – 4/17

Case: *Triune Systems, LLC vs. Wayne Chen, et al.,*
Jurisdiction: Case No. 296-03209-2013,
District Court of Collin County, TX
Work Product: Testifying expert, database viewing, expert report, video-taped testimony
Nature of Case: Defending against trade secret contention.
Counsel: Retained by Gordon & Rees LLP (Contact: Robert Bragalone)
Date: 5/15 – 9/15

Case: *Macronix vs. Spansion*
Jurisdiction: Investigation No. 337-TA-922
United States International Trade Commission
Work Product: Testifying expert, claim construction analysis, technical tutorial, database viewing for evidence gathering, expert report, expert rebuttal report.
Nature of Case: ITC infringement case concerning Flash memory cell
Counsel: Retained by Fish Richardson (Contact: David Barken)
Date: 9/14 – 1/15

Case: *Macronix vs. Spansion*
Jurisdiction: Investigation No. 337-TA-909
United States International Trade Commission
Work Product: Database viewing for evidence gathering, support technical content of expert report, support technical content against rebuttal report.
Nature of Case: ITC infringement case concerning Flash memory cell
Counsel: Retained by Winston & Strawn (Contact Michael Murray)
Date: 5/14 – 1/15

Case: ***Keranos, LLC v. Analog Devices et. al.***
Jurisdiction: Civil Case No. 2:10-CV-00207
United States District Court for the Eastern District of Texas
Work Product: Claim Chart Generation and Claim Construction
Nature of Case: Patent infringement case concerning split gate Flash memory cell
Counsel: Retained by Agility IP (Contact Michelle Breit)
Date: 2/09 – 2/14

Case: ***Silicon Storage Technology, Inc. v. Xicor, LLC***
Jurisdiction: Civil Case No. CV 10-01515
United States District Court for the Northern District of California
Work Product: Expert report and declarations
Nature of Case: Matter concerning United States Reissue Patent RE38,370 on the process of flash memory cell.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 6/11 – 10/11

Case: ***Fast Memory Erase, LLC v. Spansion et.al.***
Jurisdiction: Civil Case No. 3:10CV-481
United States District Court for the Northern District of Texas
Work Product: Declarations
Nature of Case: Defending Motion for Attorney Fees.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 2/10 – 6/10

Case: ***Fast Memory Erase, LLC v. Spansion et.al.***
Jurisdiction: Civil Case No. 3-08cv0977M
United States District Court for the Northern District of Texas
Work Product: Testifying expert: issuing expert report, declarations, and deposition taken.
Nature of Case: Patent infringement case concerning minimizing source current during erase of Flash memory cell.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 2/09 – 5/10

EXPERIENCE:

10/07 to present: **Technical Consultant/Expert Witness**

Serving as a technical consultant and advisor in the area of semiconductor device and process technologies. Expert witness in ITC cases and district court cases, with successful testifying experience in trial hearing. Depositions taken at least 6 times for both litigation cases and IPR petitions. Experienced in source code viewings of circuit schematics and GDS layouts; seasoned in reverse engineering of integrated circuits, as well as techniques for de-processing and analyzing semiconductor chips. Responsibilities including gathering and reviewing of evidence, issuing declaration on claim construction, giving technical tutorial, issuing expert report and expert rebuttal report. Technical consultant for evaluating numerous flash memory and CMOS image sensor patent portfolios for licensing and acquisition consideration. Assessed qualitative merits of each patent portfolio and identified potential infringers and potential licensees. Generated numerous claim charts against potential infringers based on published patents, technical papers and datasheets, and reverse engineering reports.

10/07 to 4/11: **Jonker, LLC**

Inventor and Partner. Developed an intellectual property (IP) portfolio (7 U.S. patents granted and 3 U.S. patent applications pending) on zero-cost CMOS-logic-compatible embedded flash memory. Successfully negotiated the acquisition of this IP portfolio by a major semiconductor company.

8/04 to 10/07: **Maxim Integrated Products, San Jose, California**

Senior Scientist. Responsible for developing embedded non-volatile memory process technology for battery management products. Duties included supervising the development of integrated process flows at the 0.35 μ m and 0.18 μ m CMOS technology nodes. Analyzed and solved process-related reliability issues.

5/00 to 8/04: **Xilinx, Incorporated, San Jose, California**

Senior Manager. Responsible for developing non-volatile memory process technology for flash and CPLD products, as well as advanced CMOS process technology (75nm node). Duties included supervising the development of integrated non-volatile memory process flows at multiple CMOS technology nodes to meet product application requirements. Analyzed and solved process-related reliability issues.

2/00 to 5/00 **Progressant Technologies, Fremont, California**

Co-Founder. Facilitated IP development and sale of the company to Synopsys, Inc.

9/98 to 2/00

Programmable Silicon Solutions, Sunnyvale, California

Director of Process Engineering. Responsible for developing a fully logic compatible embedded flash memory technology for WSMC (a semiconductor foundry). Developed a new integrated process flow to implement a proprietary flash cell in a high-performance logic process, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement. Applied interpersonal skills to align the goals of the foundry technology development group to that of PSS. Participated in the strategic planning of a technology roadmap and foundry strategy for the company.

9/97 to 9/98

AMIC Technology, Santa Clara, California

Director of Flash Technology. Responsible for developing 0.35 μ m ETOX-based flash memory technology. Prepared the business plan and technology roadmap. Developed a new integrated process flow, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement.

5/96 to 9/97

Altera Corp., San Jose, California

Device Engineering Manager. Responsible for technology development, process integration, and foundry interface for 0.35 μ m generation of logic and EEPROM programmable logic device technology. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, and product yield enhancement.

7/95 to 5/96

Information Storage Devices, San Jose, California

Technology Development Manager/Program Manager. Led a project team of 10 in technology development, process integration, and first product introduction, with a new foundry. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, resolution of sorting issues and yield enhancement.

5/92 to 7/95

Advanced Micro Devices, Sunnyvale, California

Member of Technical Staff. Led the development of low-energy/DINOR-type flash EPROM technology. Key individual contributor in optimizing the process and design of flash cell and periphery devices in AMD's 0.5 μ m and 0.35 μ m flash EPROM technologies. Duties included process integration, device modeling, and development of triple-well technology and high-voltage transistors for negative gate erase operation.

1/89 to 4/92

Texas Instruments, Dallas, Texas

Member of Technical Staff. Research and development of 16Mb generation of flash EPROM technology, as well as a new generation of antifuse-based FPGAs. Duties included process integration, device modeling, high-voltage CMOS process integration, and investigation of a novel source-side injection mechanism for EPROM channel hot-electron programming.

AWARDS/HONORS

U.C. Berkeley Certificate of Distinction Award, 1983

AEA Faculty Development Fellowship, 1983-1985

AMD Spotlight Award, 1995

PATENTS

1. U.S. Patent 5,106,773, "Programmable Gate Array and Methods for Its Fabrication" (with K-L. Chen and H. Tigelaar), issued April 21, 1992.
2. U.S. Patent 5,166,557, "Gate Array with Built-in Programmable Circuitry" (with K.-L. Chen), issued November 24, 1992.
3. U.S. Patent 5,202,576, "Asymmetrical Non-Volatile Memory Cell, Arrays, and Methods for Fabricating the Same" (with M. Wong), issued April 13, 1993.
4. U.S. Patent 5,219,782, "Sublithographic Antifuse and method for Manufacturing" (with K.-L. Chen), issued June 15, 1993.
5. U.S. Patent 5,250,464, "Method of Making a Low Capacitance, Low Resistance Sidewall Antifuse Structure" (with M. Wong), issued October 5, 1993.
6. U.S. Patent 5,264,384, "Method of Making a Non-Volatile Memory Cell" (with C. Kaya), issued November 23, 1993.
7. U.S. Patent 5,300,803, "Source Side Injection Non-volatile Memory Cell," issued April 5, 1994.
8. U.S. Patent 5,365,105, "Sidewall Antifuse Structure and Method for Making," issued November 15, 1994.
9. U.S. Patent 5,371,402, "Low Capacitance, Low Resistance Sidewall Antifuse Structure and Process" (with M. Wong), issued December, 1994
10. U.S. Patent 5,395,797, "Antifuse Structure and Method of Fabrication," issued March 7, 1995.
11. U.S. Patent 5,470,773, "Method of Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch" (with Y. Sun and C. Chang), issued November 28, 1995.
12. U.S. Patent 5,482,880, "Non-Volatile Memory and Fabrication Method," (with C. Kaya), issued January 9 1996.
13. U.S. Patent 5,517,443, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device," issued May 14, 1996.
14. U.S. Patent 5,521,867, "Adjustable Threshold Voltage Conversion Circuit" (with Jian Chen), issued May 28, 1996.
15. U.S. Patent 5,534,455, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device," issued July 9, 1996.
16. U.S. Patent 5,541,875, "High Energy Buried Layer Implant To Provide A Low Resistance P-Well in A Flash EPROM Array" (with Jian Chen), issued May 28, 1996.
17. U.S. Patent 5,590,076, "Channel Hot-Carrier Page Write," issued December 31, 1996.

18. U.S. Patent 5,596,531, "Method for Decreasing the Discharge Time of A Flash Memory Cell," issued January 21, 1997.
19. U.S. Patent 5,612,914, "Asymmetrical Non-volatile Memory Cell, Arrays and Methods for Fabricating Same" (with Man Wong), issued May 18, 1997.
20. U.S. Patent 5,624,859, "Method for Providing Device Isolation and Off-State Leakage Current for a Semiconductor Device," issued April 29, 1997.
21. U.S. Patent 5,625,220, "Sublithographic Antifuse," (with K.L. Chen), issued April 29, 1997.
22. U.S. Patent 5,646,430, "Non-volatile Memory Cell Having Lightly-Doped Source Region" (with C. Kaya), Issued July 8, 1997.
23. U.S. Patent 5,650,964, "Method of Inhibiting Degradation of Ultra Short Channel Charge-carrying Devices during Discharge," (with Jian Chen), Issued July 22, 1997.
24. U.S. Patent 5,652,155, "Method for Making Semiconductor circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant," Issued July 27, 1997.
25. U.S. Patent 5,656,509, "Method and Test Structure for Determining Gouging in a Flash EPROM Cell During SAS Etch," Issued July 29, 1997
26. U.S. Patent 5,661,059, "Boron Penetration to Suppress Short Channel Effect in P-channel Device," Issued August 26, 1997.
27. U.S. Patent 5,674,764, "Method of Making Asymmetrical Non-volatile Memory Cell," Issued October 7, 1997.
28. U.S. Patent 5,693,972, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self-Aligned Source (SAS) Etch in a Semiconductor Device," Issued December 2, 1997.
29. U.S. Patent 5,751,631, "Flash memory cell and a new method for sensing the content of the new memory cell," Issued May 12, 1998
30. U.S. Patent 5,789,295, "Method of Eliminating or Reducing Poly1 Oxidation at Stacked Gate Edge in Flash EPROM Process," Issued August 4, 1998.
31. U.S. Patent 5,814,854, "Highly scalable FLASH EEPROM cell," Issued September 29, 1998.
32. U.S. Patent 5,814,864, "Semiconductor Circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant," Issued September 29, 1998.
33. U.S. Patent 5,912,836, "Circuit for Detecting Both Charge Gain and Charge Loss Properties in a Non-Volatile Memory Array," Issued June 15, 1999.
34. U.S. Patent 5,930,174, "Circuit and Method for Erasing Flash Memory Array," Issued July 27, 1999.
35. U.S. Patent 5,981,994, "Method and Semiconductor circuit for Maintaining Integrity of Field Threshold Voltage Requirements," Issued November 9, 1999.

36. U.S. Patent 5,995,418, "Circuit and Method for Erasing Flash Memory Array," Issued November 30, 1999.
37. U.S. Patent 6,026,017, "Compact nonvolatile memory," Issued February 15, 2000.
38. U.S. Patent 6,027,974, "Nonvolatile memory," Issued February 22, 2000.
39. U.S. Patent 6,088,263, "Non-volatile memory using substrate electrons," Issued July 11, 2000.
40. U.S. Patent 6,091,636, "Flash memory cell and a new method for sensing the content of the new memory cell," Issued July 18, 2000.
41. U.S. Patent 6,127,225, "Memory cell having implanted region formed between select and sense transistors," Issued October 3, 2000.
42. U.S. Patent 6,159,800, "Method of forming memory cell," Issued December 12, 2000.
43. U.S. Patent 6,188,604, "Flash memory cell & array with improved pre-program and erase characteristics," Issued February 13, 2001.
44. U.S. Patent 6,185,133, "Flash EPROM using junction hot hole injection for erase," Issued February 6, 2001.
45. U.S. Patent 6,252,799, "Device with embedded Flash and EERPOM memories," Issued June 26, 2001.
46. U.S. Patent 6,326,265, "Device with Embedded Flash and EPROM Memories," Issued December 4, 2001.
47. U.S. Patent 6,417,550, "High voltage MOS devices with high gated-diode breakdown voltage and punch-through voltage," Issued July 9, 2002.
48. U.S. Patent 6,479,862, "Charge trapping device and method for implementing a transistor having a negative differential resistance mode," Issued November 12, 2002.
49. U.S. Patent 6,512,274, "CMOS-process compatible, tunable NDR (negative differential resistance) device and method of operating same," Issued January 28, 2003.
50. U.S. Patent 6,596,617, "CMOS compatible process for making a tunable negative differential resistance (NDR) device," Issued July 22, 2003.
51. U.S. Patent 6,624,026, "Nonvolatile Memory," Issued September 23, 2003.
52. U.S. Patent 6,680,245, "Method for making both a negative differential resistance (NDR) device and a non-NDR device using a common MOS process," Issued January 20, 2004.
53. U.S. Patent 6,686,631, "Negative differential resistance (NDR) device and method of operating same," Issued February 3, 2004.
54. U.S. Patent 6,693,027, "Method for configuring a device to include a negative differential resistance (NDR) characteristic," Issued February 17, 2004.
55. U.S. Patent 6,700,155, "Charge trapping device and method for implementing a transistor having a configurable threshold," Issued March 2, 2004.

56. U.S. Patent 6,711,063, "EEPROM memory cell array architecture for substantially eliminating leakage," Issued March 23, 2004.
57. U.S. Patent 6,835,979, "Nonvolatile Memory," Issued December 28, 2004.
58. U.S. Patent 6,969,894, "Variable threshold semiconductor device and method of operating same," Issued November 29, 2005.
59. U.S. Patent 6,972,234, "High Voltage MOS Devices with High Gated-Diode Breakdown Voltage and Punch-through Voltage," Issued December 6, 2005.
60. U.S. Patent 6,972,465, "CMOS process compatible, tunable negative differential resistance (NDR) device and method of operating same," Issued December 6, 2005.
61. U.S. Patent 7,067,873, "Charge Trapping Device," Issued June 27, 2006.
62. U.S. Patent 7,091,077, "Method of directionally trimming polysilicon width," Issued August 15, 2006.
63. U.S. Patent 7,109,078, "CMOS compatible process for making a charge trapping device," Issued September 19, 2006.
64. U.S. Patent 7,301,194, "Shrinkable and highly coupled double poly EEPROM with Inverter," Issued November 27, 2007.
65. U.S. Patent 7,436,710, "EEPROM memory device with cell having NMOS in a P pocket as a control gate, PMOS program/erase transistor, and PMOS access transistor in a common well," Issued October 14, 2008.
66. U.S. Patent 7,535,758, "One or Multiple-Times Programming Device," Issued May 19, 2009.
67. U.S. Patent 7,782,668, "Integrated circuit embedded with Non-volatile One-Time-Programmable and Multiple-Time Programmable memory," Issued August 24, 2010.
68. U.S. Patent 7,787,295, "Integrated circuit embedded with Non-volatile Multiple-Time Programmable memory having variable coupling," Issued August 31, 2010.
69. U.S. Patent 7,787,304, "Method of making integrated circuit embedded with Non-volatile One-Time-Programmable and Multiple-Time Programmable memory," Issued August 31, 2010.
70. U.S. Patent 7,787,309, "Method of operating integrated circuit embedded with Non-volatile One-Time Programmable and Multiple-Time Programmable memory," Issued August 31, 2010.
71. U.S. Patent 7,791,955, "Method of erasing a block of memory cells," Issued September 7, 2010.
72. U.S. Patent 7,835,184, "EEPROM memory cell with first-dopant-type control gate transistor, and second-dopant type program/erase and access transistors formed in common well," Issued November 16, 2010.
73. U.S. Patent 7,835,186, "Method of programming a selected memory cell," Issued November 16, 2010.

74. U.S. Patent 7,852,672, "Integrated Circuit embedded with Non-Volatile programmable memory having variable coupling," Issued December 14, 2010
75. U.S. Patent 7,876,615, "Method of operating integrated circuit embedded with Non-Volatile programmable memory having variable coupling related application data," Issued January 25, 2011
76. U.S. Patent 7,920,426, "Non-volatile memory programmable through areal capacitive coupling," Issued April 5, 2011
77. U.S. Patent 7,944,750, "Multi-programmable Non-Volatile Memory Cell," Issued May 17, 2011
78. U.S. Patent 8,203,861, "Non-Volatile One-Time Programmable and Multiple-Time Programmable Device," Issued June 19, 2012
79. U.S. Patent 8,208,299, "Integrated Circuit Embedded with Non-Volatile Programmable Memory Having Variable Coupling and Separate Read/Write Paths," Issued June 26, 2012
80. U.S. Patent 8,300,470, "Two Terminal Programmable Hot Channel Electron Non-Volatile Memory," Issued October 30, 2012
81. U.S. Patent 8,305,805, "Common Drain Non-Volatile Multiple-Time Programmable Memory," Issued November 6, 2012
82. U.S. Patent 8,325,519, "Method of Operating Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling Ratio," Issued December 4, 2012.
83. U.S. Patent 8,580,622, "Method of Making Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling," Issued November 12, 2013.
84. U.S. Patent 8,582,342, "Non-Volatile One-Time-Programmable and Multiple-Time Programmable Memory Configuration Circuit," Issued November 12, 2013.
85. U.S. Patent 8,599,612, "Method of Operating Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling Related Application data," Issued December 3, 2013.
86. U.S. Patent 8,705,263, "Non-Volatile One-Time-Programmable and Multiple-Time Programmable Memory Configuration Circuit," Issued April 22, 2014.
87. U.S. Patent 8,988,103, "Capacitively Coupled Logic Gate," Issued March 24, 2015.
88. U.S. Patent 9,064,192, "Automatic Valid Vote Count Storage using Secure Embedded Non-Volatile Memory," Issued June 23, 2015.
89. U.S. Patent 9,224,739, "Method of Making Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling," Issued December 29, 2015.
90. U.S. Patent 9,305,931, "Zero Cost NVM Cell Using High Voltage Devices in Analog Process," Issued April 5, 2016.

91. U.S. Patent 9,324,438, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued April 26, 2016.
92. U.S. Patent 9,558,813, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued January 31, 2017.
93. U.S. Patent 9,570,161, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued February 14, 2017.
94. U.S. Patent 9,570,175, "Incrementally Programmable Non-Volatile Memory," Issued February 14, 2017.
95. U.S. Patent 10,061,738, "Ephemeral Peripheral Device," Issued August 28, 2018.
96. U.S. Patent 10,115,467, "One time Accessible (OTA) Non-Volatile Memory," Issued October 30, 2018.
97. U.S. Patent 10,198,889, "Automatic Valid Vote Count Storage Using Secure Embedded Non-Volatile Memory," Issued February 5, 2019
98. U.S. Patent 10,559,700, "Zero Cost ANVM Cell Using High Voltage Devices in Analog Process," Issued February 11, 2020.
99. U.S. Patent 10,629,607, "Semiconductor CMOS Non-Volatile Memory Device," Issued April 21, 2020

(additional patent applications pending)

PUBLICATIONS

1. S.D. Leeke, D. K. Y. Liu and J. P. McVittie, "Plasma mode trench etching with direct hydrocarbon injection," *Materials Research Society Symposium Proceedings*, Vol. 68, pp. 21-27, 1986.
2. D. K. Y. Liu and J. D. Plummer, "A novel trench-injector power device with low ON-resistance and high switching speed," *IEEE Electron Device Letters*, Vol. 9, No. 7, pp. 321-323, 1988.
3. D. M. Boisvert, D. K. Y. Liu and J. D. Plummer, "Circuit approaches to increasing IGBT switching speed," *IEEE Journal of Solid-State Circuits*, Vol. 23, No. 5, pp. 1276-1279, 1988.
4. D. K. Y. Liu and J. D. Plummer, "Device physics and optimization of conductivity-modulated power MOSFET's," *IEEE Transactions on Electron Devices*, Vol. 35, No. 12, pp. 2457-2458, 1988.
5. D. K. Y. Liu, K.-L. Chen, H. Tigelaar, J. Paterson and S. O. Chen, "Scaled dielectric antifuse structure for field-programmable gate array applications," *IEEE Electron Device Letters*, Vol. 12, No. 4, pp. 151-153, 1991.
6. M. Wong, D. K. Y. Liu, M. M. Moslehi and D. W. Reed, "Preoxidation treatment using HCl/HF vapor," *IEEE Electron Device Letters*, Vol. 12, No. 8, pp. 425-426, 1991.
7. D. K. Y. Liu, C. Kaya, M. Wong, J. Paterson and P. Shah, "Optimization of a source-side injection FAMOS cell for flash EPROM applications," *International Electron Devices Meeting Technical Digest*, pp. 315-318, 1991.
8. K.-L. Chen, D. K. Y. Liu, G. Misium, W. M. Gosney, S.-J. Wang, J. Camp and H. Tigelaar, "A sublithographic antifuse structure for field-programmable gate array applications," *IEEE Electron Device Letters*, Vol. 13, No. 1, pp. 53-55, 1992.
9. K. T. San, C. Kaya, D. K. Y. Liu, T. P. Ma, and P. Shah, "A new technique for determining capacitive coupling coefficients in flash EPROMs," *IEEE Electron Device Letters*, Vol. 13, No. 6, pp. 328-331, 1992.
10. C. Kaya, D. K. Y. Liu, J. Paterson and P. Shah, "Buried source-side injection (BSSI) for flash EPROM programming," *IEEE Electron Device Letters*, Vol. 13, No. 9, pp. 465-467, 1992.
11. M. Wong, D. K. Y. Liu and S. S.-W. Huang, "Analysis of the subthreshold slope and the linear transconductance techniques for the extraction of the capacitance coupling coefficients of floating-gate devices," *IEEE Electron Device Letters*, Vol. 13, No. 11, pp. 566-568, 1992.
12. D. K. Y. Liu and J. D. Plummer, "Design and analysis of a new conductivity-modulated power MOSFET," *IEEE Transactions on Electron Devices*, Vol. 40, No. 2, pp. 428-438, 1993.
13. J. Z. Peng, S. Haddad, H. Fang, C. Chang, S. Longcor, B. Ho, Y. Sun, D. Liu, Y. Tang, J. Hsu, S. Luan, J. Lien, "Flash EPROM endurance simulation using physics-based models," In *International Electron Devices Meeting Technical Digest*, pp. 295-298, 1994.
14. J. Chen, J. Hsu, S. Luan, Y. Tang, D. Liu, S. Haddad, C. Chang, S. Longcor, J. Lien, "Short Channel enhanced degradation during discharge of Flash EEPROM memory Cell," *International Electron Devices Meeting Technical Digest*, pp. 331-334, 1995.

15. V. H. Chan and D. Liu, "An Enhanced Erase Mechanism During Channel Fowler-Nordheim Tunneling in Flash EPROM Memory Devices," *IEEE Electron Devices Letters*, Vol. 20, No. 3, pp. 140-142, 1999.