

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

**BOE TECHNOLOGY GROUP CO., LTD.,
BEIJING BOE DISPLAY TECHNOLOGY CO., AND
MOTOROLA (WUHAN) MOBILITY TECHNOLOGIES
COMMUNICATION CO., LTD.**

Petitioner,

v.

ELEMENT CAPITAL COMMERCIAL COMPANY PTE. LTD.

Patent Owner.

IPR2023-00696
Patent No. 8,525,760

PATENT OWNER'S PRELIMINARY RESPONSE

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Exhibit	Description
2001	Declaration of Aris K. Silzars
2002	Curriculum Vitae of Dr. Aris Silzars
2003	U.S. Patent Publication No. 2007/0236620 to Yan
2004	U.S. Patent No. 5,317,178A to Wu
2005	U.S. Patent No. 6,739,931 B2 to Yamazaki et al.
2006	United States District Courts — National Judicial Caseload Profile, “ https://www.uscourts.gov/statistics-reports/federal-court-management-statistics-march-2023 ”
2007	Explanation of Selected Terms for United States District Courts — National Judicial Caseload Profile, “ https://www.uscourts.gov/statistics-reports/federal-court-management-statistics-march-2023 ”
2008	Plaintiff’s Motion for Leave to Effect Service by Alternate Means, <i>Element Capital Commercial Company PTE. Ltd. v. BOE Technology Group Co., Ltd. et al.</i> , Case No. 2:22-cv-0118-JRG (EDTX)
2009	Order Granting Motion for Leave, <i>Element Capital Commercial Company PTE. Ltd. v. BOE Technology Group Co., Ltd. et al.</i> , Case No. 2:22-cv-0118-JRG (EDTX)
2010	Joint Motion for Entry of Agreed Docket Control Order, <i>Element Capital Commercial Company PTE. Ltd. v. BOE Technology Group Co., Ltd. et al.</i> , Case No. 2:22-cv-0118-JRG (EDTX)
2011	USPTO Memo regarding Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation (“Fintiv Memo”)

Patent Owner Element Capital Commercial Company Pte. Ltd (“Element” or “Patent Owner”) submits this Preliminary Response to the Petition seeking *inter partes* review of claim 1 (“the Challenged Claim”) of U.S. Patent No. 8,525,760 (“the ’760 Patent,” Ex-1001), filed by BOE Technology Group Co., Ltd (“BOE” or “Petitioner”).

I. SUMMARY OF ARGUMENT

The Board should deny BOE’s Petition because it fails to establish a reasonable likelihood of success under any of Grounds 1a, 1b, 2a, and 2b. The Challenged Claim of the ’760 Patent recites a particular arrangement of a pixel unit circuit in which a wiring portion crosses a control line. The prior art as applied in the Petition does not disclose or render obvious such an arrangement.

Thus, Petitioner has failed to meet its initial burden to show that each element of the Challenged Claim was known or obvious over the prior art references. The Board should therefore deny institution.

II. OVERVIEW OF THE ’760 PATENT

A. The ’760 Patent

The ’760 Patent is directed to an active matrix type electro-optical device, for example, an organic light-emitting diode (“OLED”) display. EX-1001, 1:14-16. In particular, the ’760 Patent aims to improve brightness of the electro-optical device by increasing a region occupied by the electro-optical element that emits light while

decreasing a region occupied by a peripheral circuit driving the electro-optical element in each pixel. EX-1001, 14:26-32. This decrease in the circuit region is achieved by the particular layout and configuration of circuit components as disclosed in the patent. EX-1001, 18:62-65; EX-2001, ¶¶ 10-12, 24-25, 28-29.

The '760 Patent describes that each pixel unit in the matrix arrangement corresponds to an intersection of a data line and a control line. EX-1001, 1:27-29. As shown below, FIG. 2 of the '760 Patent illustrates a plan view of a pixel unit 10 corresponding to an intersection of the data line *Idata* and control line *Vsel*. EX-2001, ¶ 26.

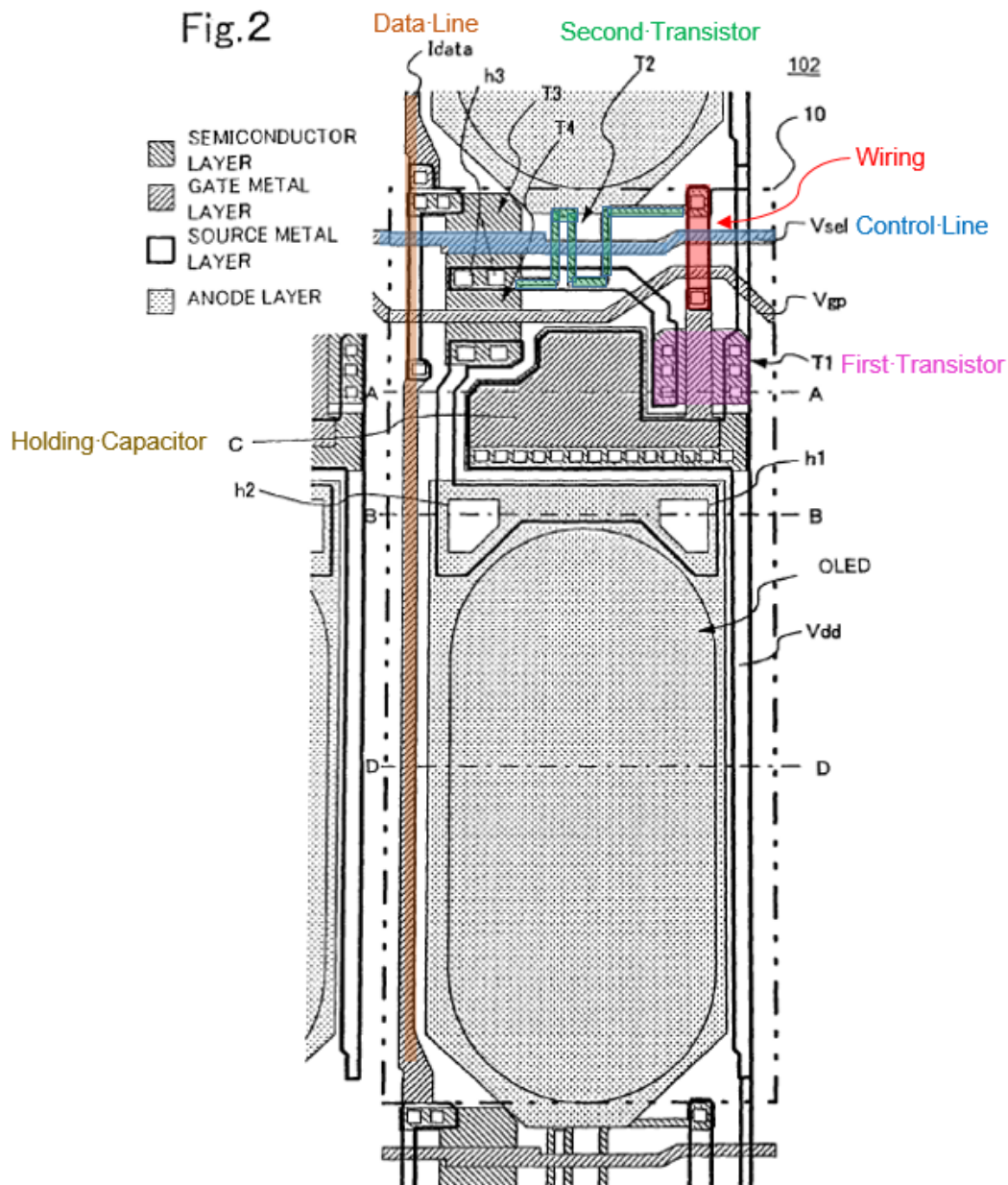


FIG. 2 of the '760 Patent (annotated)

The pixel unit 10 includes a light-emitting portion OLED (electro-optical element) and a peripheral circuit to drive the light-emitting portion OLED. In particular, the peripheral circuit includes a first transistor T1, a second transistor T2, and a holding capacitor C. The source of the second transistor T2 is connected to

the gate of the first transistor T1 through a wiring (highlighted in red above). Notably, in the compact circuit design of the patent, the wiring crosses the control line Vsel corresponding to its same pixel unit circuit. EX-2001, ¶¶ 27-29.

B. Prosecution History of the '760 Patent

The Petition sets forth a detailed summary of the prosecution history of the '760 Patent, but incorrectly states that “[t]he Examiner did not provide reasons for the allowance.” Pet., 17. To the contrary, in the Office Action dated February 13, 2013, the Examiner stated that claim 21 (which later issued as claim 1) is allowed because the cited art “does not disclose that a wiring connecting the second transistor and the gate of the first transistor comprises a portion formed in a layer other than semiconductor layer or the gate layer of the first transistor, and said portion crossing the control line of the electro-optical device.” Ex-1004, 880.

III. CLAIM CONSTRUCTION

At this stage of the proceeding and for purposes of this Preliminary Response, Patent Owner submits that no formal claim constructions are needed and the claim terms should be understood in accordance with their plain and ordinary meaning.

IV. PERSON OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) would have had at least a Master’s degree in electrical engineering, physics, or a related field, and at least two years of relevant work experience in the field of display device technology. EX-

2001, ¶¶ 21-23. Additional education can remedy lack of work experience and vice versa. *Id.*

V. OVERVIEW OF PRIOR ART

A. Inukai 576 (Ex-1007)

Inukai 576 is directed to an active matrix display device formed by electroluminescence elements EL. EX-1007, ¶ [0002]. FIG. 3 of Inukai 576 illustrates a circuit diagram of a pixel unit (j,i) 104 of the EL display. As with the '760 Patent, and as is well known in the art, each pixel unit in the matrix corresponds to a particular intersection of a control line G_i and a data line S_j . EX-2001, ¶ 33.

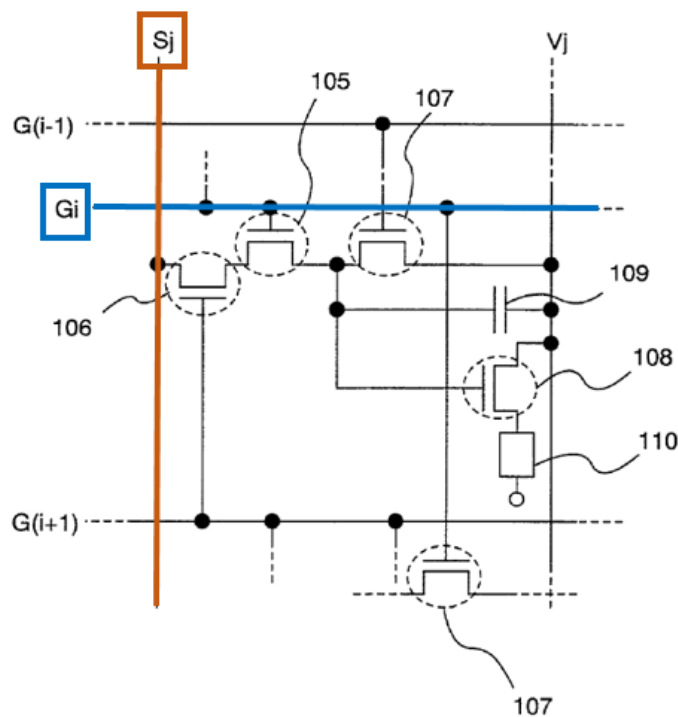


FIG. 3 of Inukai 576 (annotated)

FIG. 9 of Inukai 576 reproduced below is a plan view of the pixel unit (j,i)
104 in FIG. 3 of Inukai 576.

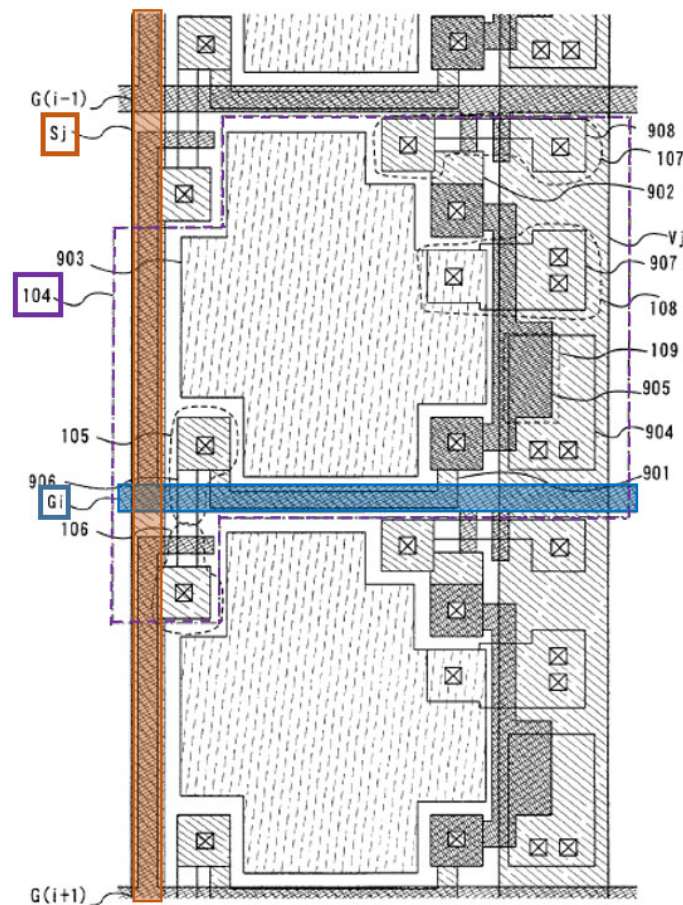


FIG. 9 of Inukai 576 (annotated)

As described in the reference, the pixel unit (j,i) 104 is defined by a region corresponding to a data line S_j and a control line G_i . EX-1007, ¶¶ [0075] and [0077]. Further, the TFT 108 for EL driving uses a part of the gate wiring 905 as its gate electrode and the gate wiring 905 is connected through a connection wiring 902 to a source/drain of the TFT 107 for erasing. The gate electrodes of the TFT 107 for erasing are connected to the connection wiring 902 and a control line $G(i-1)$ of a *different* pixel unit (j, i-1) than that of the connection wiring 902, the TFT 108 for EL driving, etc., of the pixel unit (j, i). Moreover, the gate electrodes of the TFT 107 for erasing are not *part of* the control line $G(i-1)$, but are instead *connected to* the control line $G(i-1)$. *See, e.g.*, EX-1007, ¶ [0201] (“gate electrodes [of the TFT 107] are *connected to* the gate signal line” (emphasis added)); EX-2001, ¶¶ 35-36.

B. Overview of Inukai 574 (Ex-1008)

Inukai 574 is directed to an EL display formed by electroluminescence EL elements. EX-1008, ¶ [0001]. As shown below, FIG. 2 of Inukai 574 illustrates a pixel unit 107 corresponding to an intersection of a data line S_{a1} and a control line G_{a1} :

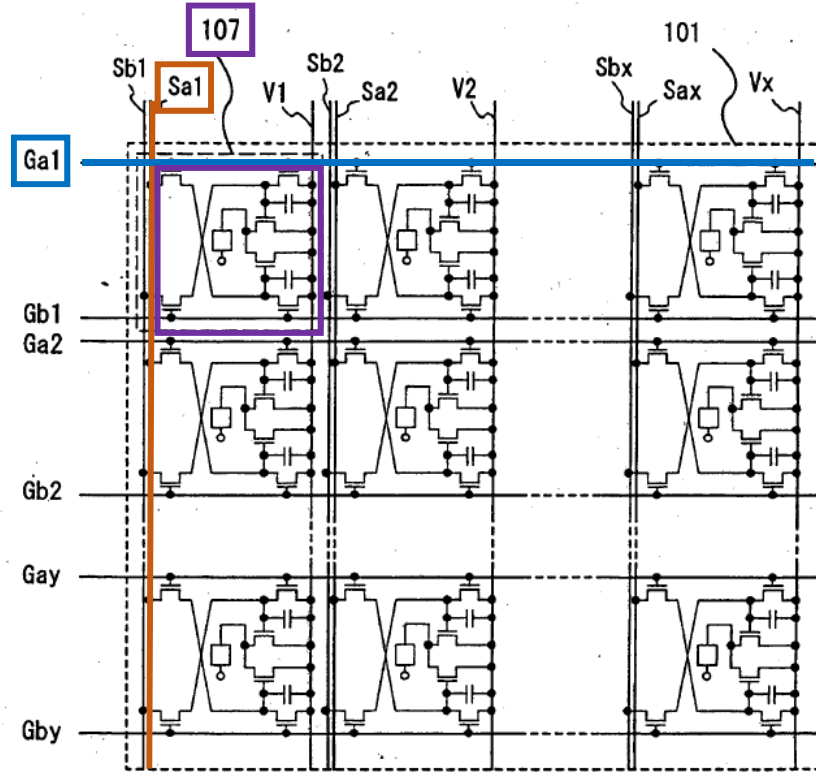


FIG. 2 of Inukai 574 (annotated)

FIG. 5 of Inukai 574, reproduced below, illustrates a pixel unit circuit schematic, in which the pixel unit includes the circuit components (*e.g.*, transistor 3805b, transistor 3806a, etc.) in an area corresponding to the intersection of a data line 3802a and the upper control line 3801b. As shown, the pixel unit includes a transistor 3805b and a transistor 3806a connected to the control line 3801b. In the circuit schematic, the transistor 3805b connected to the gate of the transistor 3806a crosses a different control line 3801a than the control line 3801b that intersects

with the data line 3802a to define the pixel unit circuit area in the matrix. EX-2001, ¶¶ 37-38.

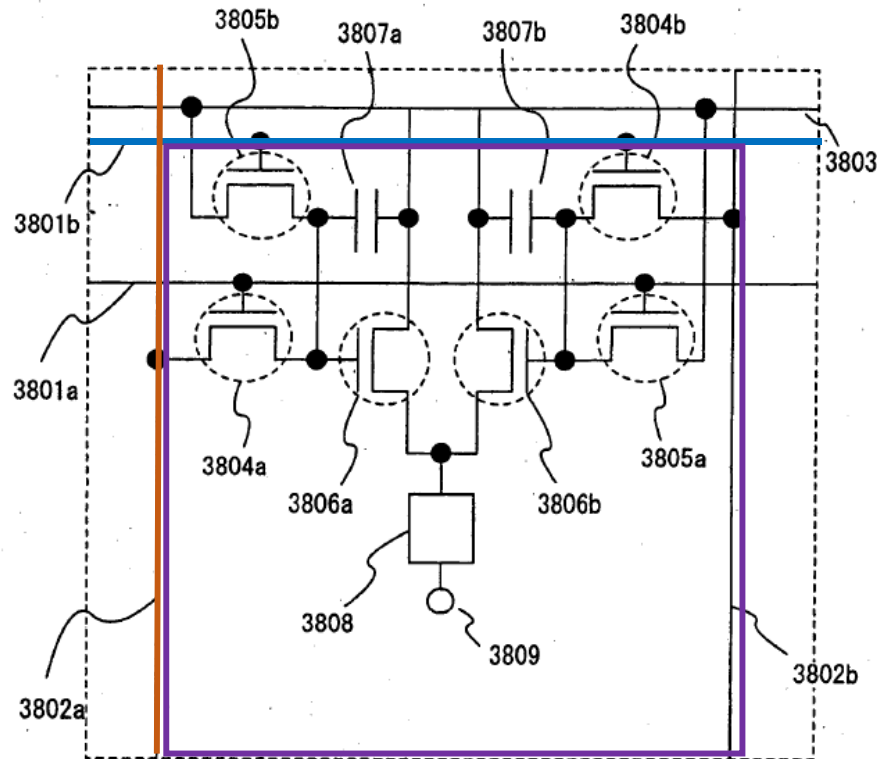


FIG. 5 of Inukai 574 (annotated)

Inukai 574 does not provide or otherwise describe a plan view of the physical layout of its circuit components within a pixel unit. EX-2001, ¶ 39.

VI. THE BOARD SHOULD DENY INSTITUTION ON THE MERITS FOR ALL GROUNDS

The Petition should be denied at least because the applied references do not teach or render obvious “a wiring having a portion ... the portion crossing the control line.”

A. The Petition has failed to establish a reasonable likelihood of prevailing on Ground 1a because Inukai 576 fails to anticipate or render obvious the claimed wiring

Ground 1a of the Petition must fail because Inukai 576 does not disclose a portion of a wiring that crosses a control line, let alone that crosses a control line corresponding to its same unit circuit. Instead, Inukai 576 discloses a wiring portion adjacent to a gate electrode (a) that is not a control line, (b) that is not crossed by the wiring portion, and (c) that corresponds to a different unit circuit than that of the wiring portion. EX-2001, ¶¶ 40-41.

a. Inukai 576 fails to disclose a wiring portion that crosses a control line

Claim 1 recites “a wiring... having a portion ... crossing [a] control line.” An example of such a wiring crossing a control line is illustrated in FIG. 2 of the '760 Patent:

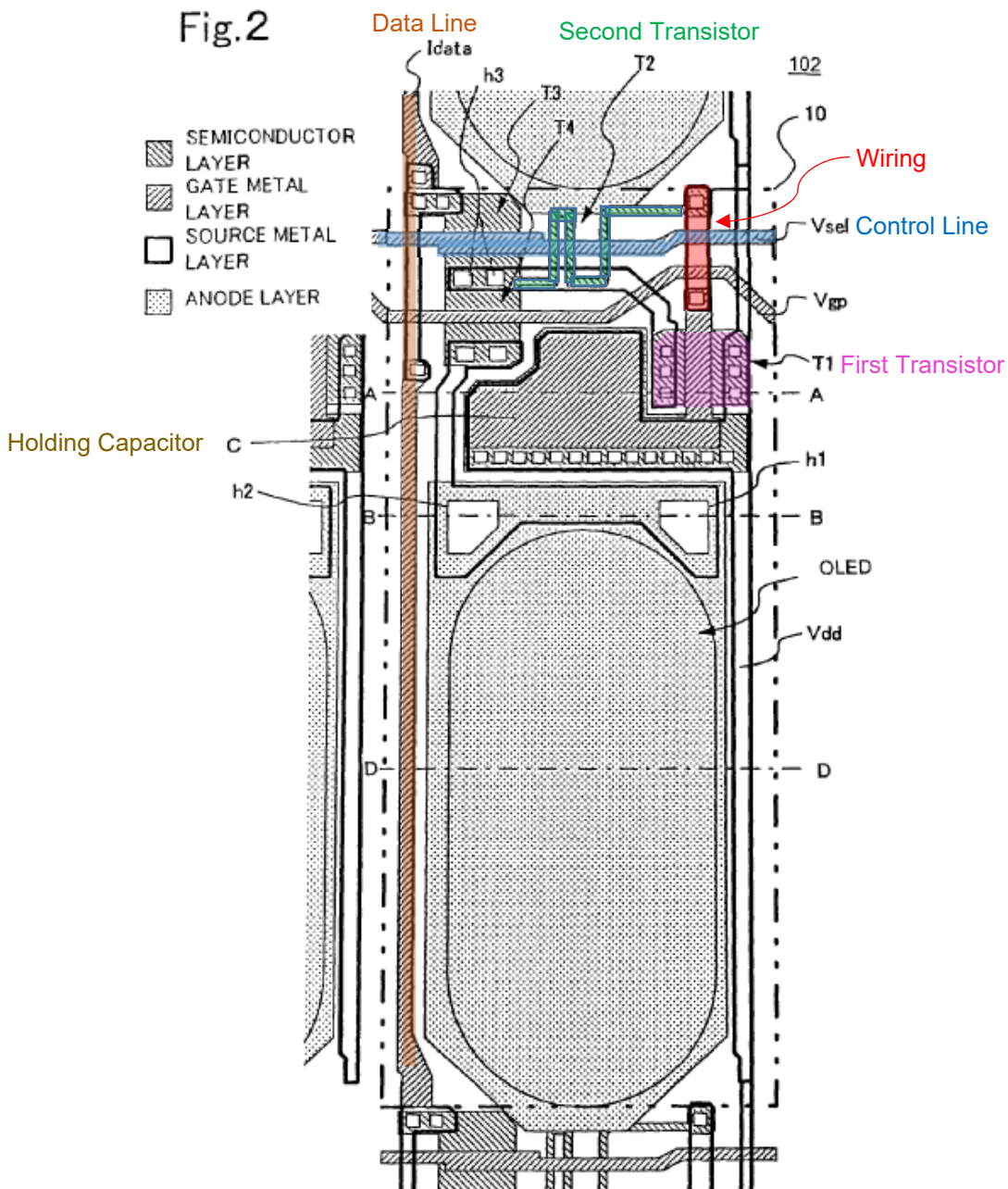
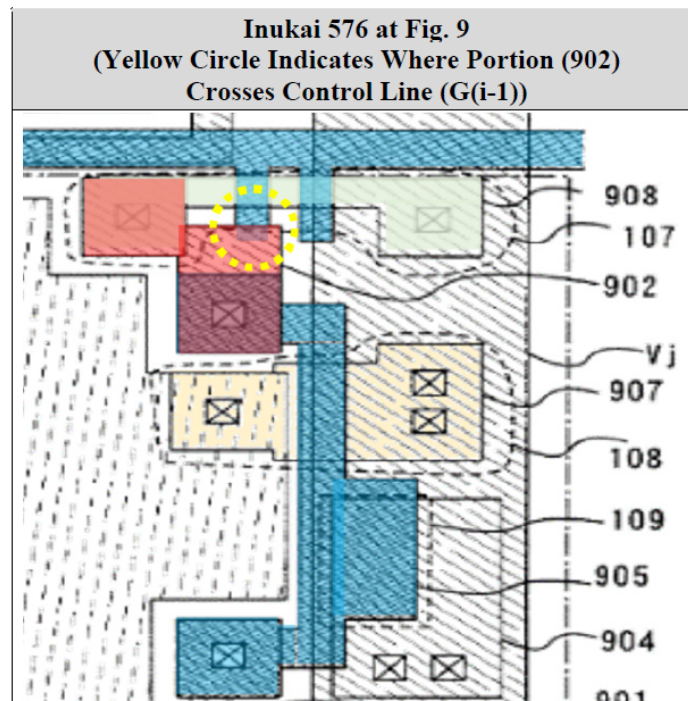


FIG. 2 of the '760 Patent (annotated)

Inukai 576 does not disclose a wiring portion crossing a *control line*. For an alleged teaching of the control line, Petitioner points to a gate signal line G(i-1)

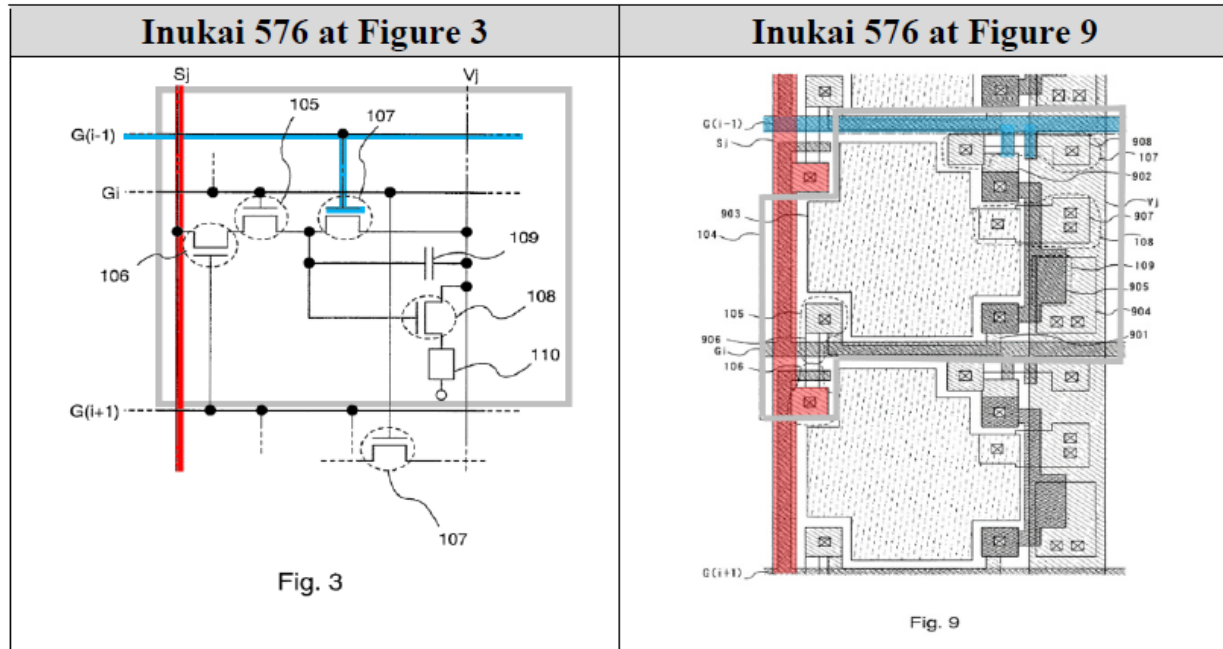
and **protrusions** off of the gate signal line G(i-1), as shown in Petitioner's annotation of FIG. 9 of Inukai 576, Pet., 50, reproduced below:



Petitioner alleges that the protrusion to the left is crossed by the wiring portion 902. The protrusions, however, are not control lines but are gate electrodes of the TFT 107. EX-2001, ¶¶ 43-44. Indeed, Petitioner and its expert admit that the protrusions are gate electrodes of the TFT 107, Pet., 49, but attempt to argue that these protrusions are both part of the TFT 107 (as gate electrodes thereof) and the control line, *i.e.*, the gate signal line G(i-1). Not so.

First, the claim defines the unit circuit as corresponding to an intersection of the data line and the control line. In other words, the control line is the **line** that

intersects the data line, *i.e.*, the horizontal control line shown in both the '760 Patent and Inukai 576 that intersects the vertical data line. EX-2001, ¶ 45.



FIGS. 3 and 9 of Inukai 576, Pet., 29

As can be seen above, the protrusions (*i.e.*, gate electrodes) in Inukai 576, are not a portion of the horizontal control **line** that intersects the vertical data line. EX-2001, ¶¶ 46-47.

Second, Inukai 576 itself expressly distinguishes the gate electrodes (*i.e.*, protrusions) from the gate signal line G (control line), and describes the gate electrodes as part of the TFT 107 and “connected to”—not part of—the gate signal line G. *See, e.g.*, Ex-1007, ¶[0201] (“When the gate signal line G1 is selected, **the TFT 107... whose gate electrodes are connected to the gate signal line G1** are

turned on.”); *see also id.*, ¶¶ [0107] (“...the TFTs 107..., the gate electrodes of which are connected to the gate signal line G1...”), [0160] (“...*the TFT 107...* whose gate electrodes are connected to the gate signal line G1 are turned on”).

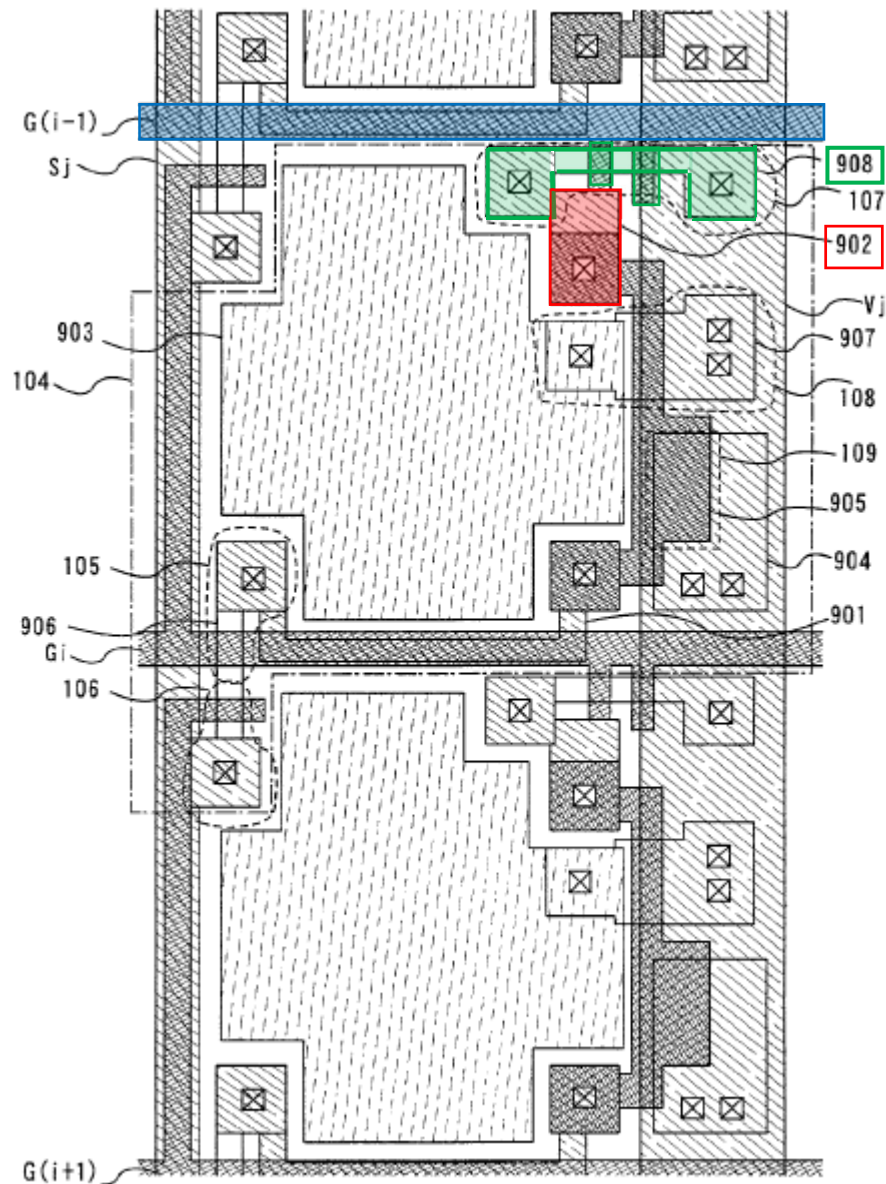
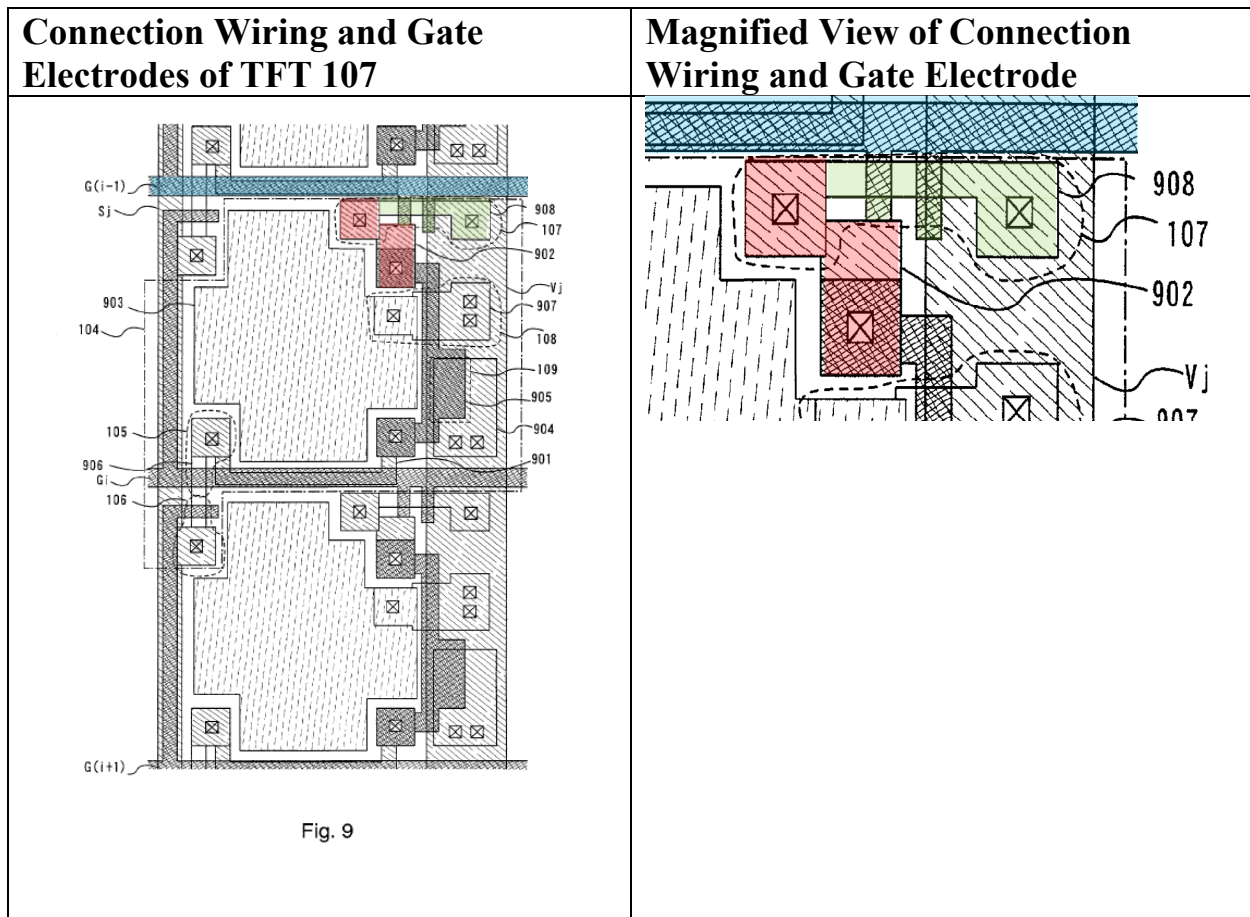


FIG. 9 of Inukai 576

Thus, as the protrusions (gate electrodes) are not the control line and are explicitly distinguished from the control line in the reference, the wiring portion 902 in Inukai 576 cannot be said to cross the horizontal control line. Inukai 576 therefore fails to disclose “a wiring... having a portion ... crossing [a] control line,” as required by the claim. EX-2001, ¶¶ 48-49.

b. Inukai 576 fails to disclose a wiring portion that crosses a control line

Even if, *arguendo*, Inukai 576’s gate electrode is considered to be the control line, the electrode is not crossed by a wiring portion, unlike the claimed control line (claim 1: “a wiring... having a portion ... crossing [a] control line.”). Instead, Inukai 576 provides a wiring portion 902 that extends near but does not cross the gate electrode of the TFT 107:



Notably, FIG. 9's plan view explicitly shows the outlines of component parts irrespective of whether that component would otherwise be hidden by another layer "topographically above" (Pet., 51). For example, the transistor body outline can be seen even though it is below the gate electrode (protrusion), which runs above the transistor body. EX-2001, ¶¶ 50-51.

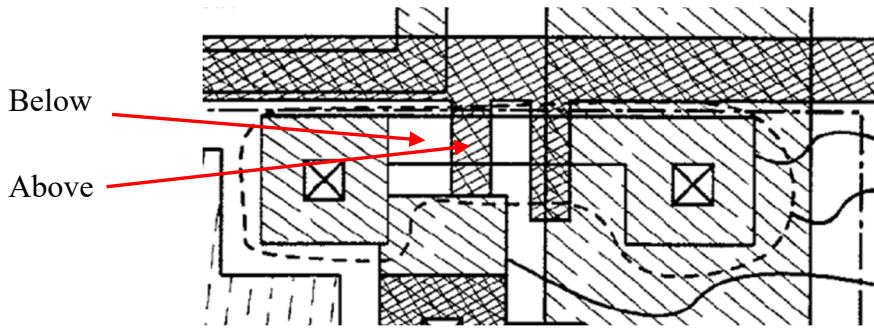


FIG. 9 of Inukai 576 (magnified and annotated)

Thus, a POSITA would have understood that the Inukai 576 inventor deliberately designed its gate electrode such that it does not overlap with the wiring portion 902, as unambiguously shown in the figure. EX-2001, ¶ 52. This is for good reason; even if the gate electrode and the wiring portion 902 of Inukai 576 are considered to be in different layers, and even if there was an insulating layer therebetween, a POSITA would still want to avoid overlapping the two in order to avoid unwanted interference (*e.g.*, crosstalk) between the gate electrode and wiring portion 902. EX-2001, ¶¶ 52-58; EX-2003 ¶[0080], FIG. 6 (overlapping gate and data line causes interference and deteriorates quality of displayed images, even with insulating layer in between).

Nevertheless, Petitioner argues that “a POSITA would have understood or found obvious that the protrusion would have been the same length as the protrusion on the right, due to the ‘endcap rule.’” Pet., 51. According to Petitioner, the “endcap rule” refers to “a universal rule in semiconductor design that requires gates to have

a certain minimum length.” Pet., 52. Notably, Petitioner and its expert provide no support for its allegation that the “endcap rule” is universally applied.

At best, Petitioner cites to Borodovsky (Ex-1010), but Borodovsky does not actually state that the “endcap rule” is *universally* applied. Rather, Borodovsky merely describes the general concept that an endcap of a transistor gate may extend some minimum distance beyond an active region so as to ensure that any rounding of the endcap does not occur over the active region. Ex-1010, 4:21-33. Absent from the reference is any suggestion that the rule is universal, or how the rule would have been applied to Inukai 576 in view of its particular manufacturing process and materials. *See* EX-2001, ¶¶ 59-61, 63.

Nor does Borodovsky provide any basis to conclude that the “endcap rule” would yield gate electrodes of the *same* size or length. All that Borodovsky’s design rule necessitates is that the endcap extends at least a minimum length—not an exact length—beyond the active region, and “other size up amounts may be used.” Ex-1010, 9:42-46. The Petition itself recognizes that the endcap rule does not require equal length electrodes, but only that the length of each electrode exceeds “a minimum length.” Pet., 52. There is no universal rule or reason to require gate electrodes to be of the same length, as evidenced by Inukai 576 itself in which the gate electrodes have different lengths. EX-2001, ¶¶ 62-66; *see also* EX-2004, 5:4-9, FIG. 11.

Furthermore, while Petitioner alleges that the “endcap rule” is *universally* applied, it provides no basis to believe that Inukai 576 has not already complied with it. In other words, accepting Petitioner’s allegation on the universality of the “endcap rule,” a POSITA would have therefore understood that the gate electrodes in Inukai 576 were designed in compliance with this “universal rule in semiconductor design.” Petitioner has provided no reason to believe otherwise. Indeed, referring to FIG. 9 of Inukai 576, the left protrusion of the TFT 107 for erasing extends beyond the active layer 908 that is a semiconductor layer, such that the structural configuration of the protrusions in Inukai 576 has presumably already complied with the endcap rule. EX-2001, ¶ 67. Therefore, the Petition fails to provide a sufficient rationale for a POSITA to have found it obvious to modify the length of the left gate electrode of the TFT 107 for erasing to be equal to a length of the right protrusion.¹

In sum, Inukai 576 expressly discloses a wiring portion that does *not* cross a gate electrode (let alone a control line). Further, the Petition fails to provide a sufficient rationale to modify the length of the gate electrode such that it is crossed

¹ Even if it would have been obvious to modify the lengths of the parallel gate electrodes to be the same, that does not require extending the length of the left gate electrode. Rather, the right gate electrode could be reduced in length.

by the wiring portion, as explained in further detail below with reference to Ground 1b. Instead, Petitioner cites to a rule without addressing the fact that Inukai 576 must already comply with it. Ground 1a therefore fails as Inukai 576 does not disclose or render obvious a wiring portion crossing a control line.

c. Inukai 576 fails to disclose a unit circuit corresponding to a control line and comprising a wiring portion crossing that control line

Inukai 576 does not disclose a unit circuit including each of the constituent elements as arranged in the claim. Specifically, Inukai 576 fails to disclose a wiring portion, of a unit circuit, that crosses a control line corresponding to that unit circuit. Instead, the Petition improperly relies on components across multiple different unit circuits in Inukai 576, and cites to a wiring portion alleged to cross a control line corresponding to a different unit circuit.

Claim 1 recites “a unit circuit arranged corresponding to an intersection of the data line and the control line.” Per the claim, one unit circuit includes a first transistor, a second transistor, an electro-optical element, a holding element, and wiring. In other words, each unit circuit “*corresponding to an intersection* of the data line and the control line” constitutes a pixel unit as understood in the art. Ex-1001, 1:27-29 (“Each of the plurality of pixel circuits is arranged to correspond to the intersection of a data line and a scan line.”); *see e.g.* EX-2001, ¶¶ 71-72; EX-2005, 16:61-65 and FIGS. 9A and 9B.

As recognized by the Petition, Inukai 576 also discloses a unit circuit ***corresponding to the intersection*** of a particular data line and scan (or control) line (*i.e.*, pixel unit). EX-2001, ¶ 73. Each pixel unit 104 is “designated by a particular gate signal line and a particular source signal line.” Pet., 28 (citing Ex-1007, ¶¶ [0075] and [0077]). Inukai 576 defines its pixel unit 104 (highlighted in orange below) corresponding to the intersection of the particular data line Si and the particular control line Gi (highlighted in blue below), and the constituent components of that unit circuit (*e.g.*, highlighted in red below):

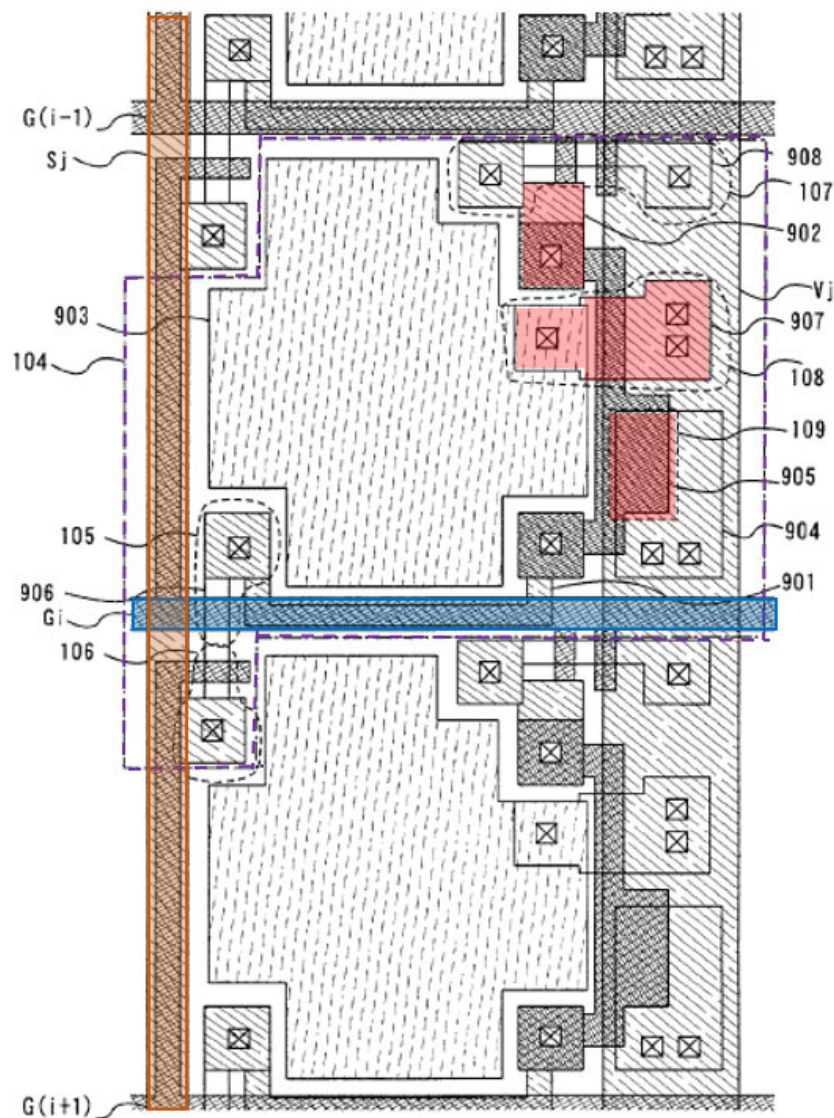
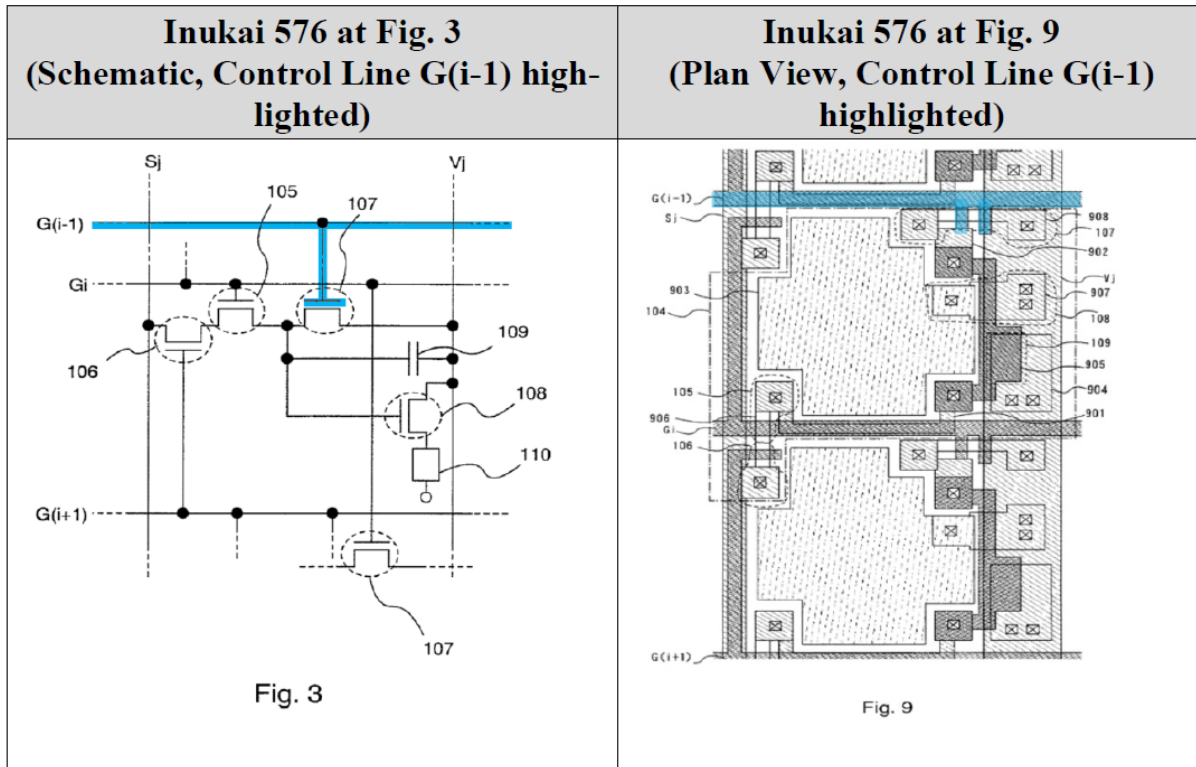


FIG. 9 of Inukai 576 (annotated)

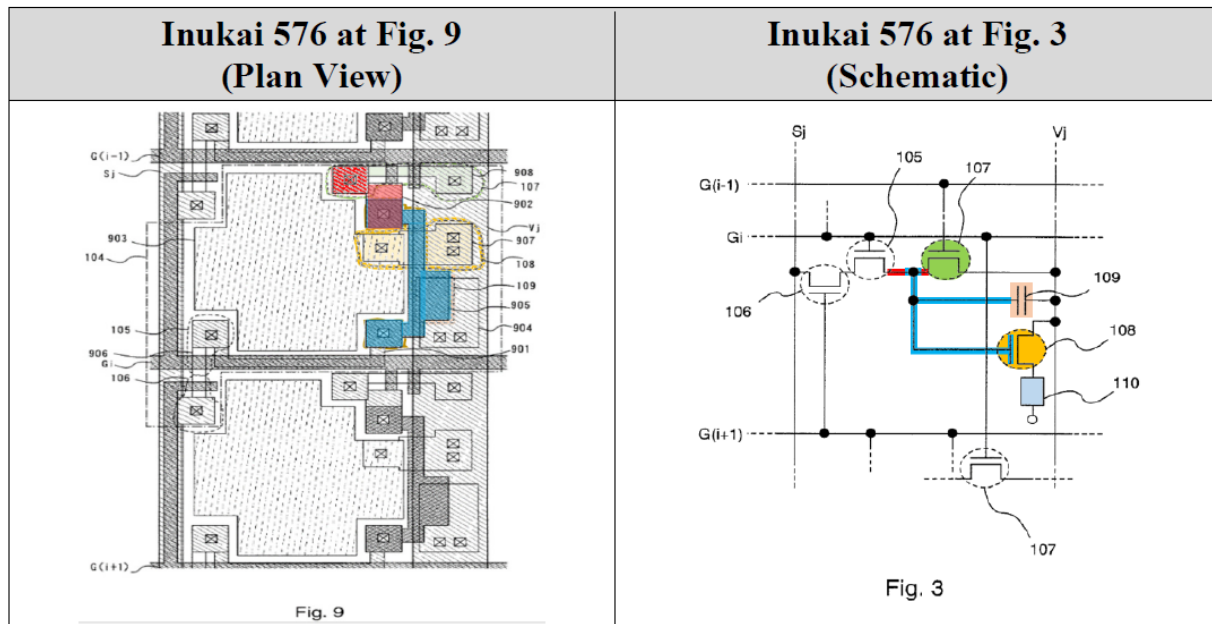
Consistent with Inukai 576's unit circuit, the Petition cites to TFT 108 for the first transistor, capacitor 109 for the holding circuit, and wiring 904 for the claimed wiring portion, each of which corresponds to the intersection of the particular data line S_i and the particular control line G_i . Nevertheless, for an alleged teaching of the wiring portion crossing the control line, the Petition cites to a different control

line $G(i-1)$ that corresponds to and defines a different pixel unit than the unit circuit of the wiring portion, the first transistor, etc. EX-2001, ¶ 74.



FIGS. 3 and 9 of Inukai 576 (annotated in Pet., 27)

The control line $G(i-1)$ intersects with the data line to define a different corresponding unit circuit (or pixel), as shown in FIG. 2 of Inukai 576 (showing different pixel unit circuits respectively corresponding to different intersections of scan lines and control lines). To be clear, the wiring portion, the first transistor, the holding circuit, etc., cited by the Petition are plainly of the pixel unit circuit corresponding to the intersection of G_i and S_j , NOT the distinct pixel unit circuit corresponding to the intersection of $G(i-1)$ and S_j . EX-2001, ¶ 75.



FIGS. 9 and 3 of Inukai 576 (annotated at Pet., 42)

Thus, even assuming *arguendo* that the gate electrode is part of the control line $G(i-1)$ and that it would have been obvious to extend the length of this gate electrode under the wiring portion 902, as alleged by Petitioner, the wiring portion 902 would not cross the control line G_i corresponding to its pixel unit circuit. Instead, under Petitioner's theory, the wiring portion would at best cross the control line $G(i-1)$ corresponding to a different pixel unit circuit. EX-2001, ¶ 76. For at least this reason, Grounds 1a and 1b must fail as the Petition fails to show a wiring portion crossing a control line corresponding to the same unit circuit.

B. The Petition has failed to establish a reasonable likelihood of prevailing on Ground 1b because Yamazaki does not cure the deficiencies of Ground 1a

Petitioner alleges that it would have been obvious for a POSITA to modify Inukai 576 in view of Yamazaki such that the left protrusion is the same length as the right protrusion. As an initial point, the Petition fails to establish that the proposed combination would have been obvious to extend the length of Inukai 576's left protrusion instead of reducing the length of the right protrusion. Nevertheless, Petitioner fails to establish a likelihood of success under Ground 1b at least because (a) Petitioner does not provide a sufficient rationale to support the legal conclusion of obviousness, and (b) the combination does not cure the deficiencies of Inukai 576 as set forth above with reference to Ground 1a.

a. Petitioner fails to establish *prima facie* case of obviousness in modifying Inukai 576 in view of Yamazaki

Ground 1b is deficient because Petitioner does not adequately provide an “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

Petitioner relies on a motivation to combine rationale to allege that it would have been obvious to extend the length of the left gate electrode in Inukai 576 so as to be equal in length to the right gate electrode. According to Petitioner, “[a] POSITA, upon ascertaining a given endcap length, would have been motivated to

ensure that all gates (and especially gates that are part of the same multi-gate transistor) to be designed to have endcaps of equal lengths to ensure that the gates are long enough to exert control.” Pet., 54; *see also id.*, 55. This rationale fails for a number of reasons. EX-2001, ¶¶ 77-78.

First, a necessary premise for Petitioner’s motivation is that the left gate electrode in Inukai 576 does not already comply with the endcap rule, such that a POSITA would have been motivated to modify the electrode to comply with this rule. This premise is unproven in the Petition, but simply assumed without any basis or support. In fact, the record provided by Petition instead supports the conclusion that the left gate electrode in Inukai 576 already complies with the endcap rule, as Petitioner and its expert argue that this rule is universally applied. Pet., 52 (“The ‘endcap rule’ refers to **a universal rule** in semiconductor design that **requires** gates to have a certain minimum length.”). Notably, the left gate electrode in Inukai 576 extends beyond the active region of the transistor, and therefore complies with the endcap rule. Ex-1007, FIG. 9. The Petitioner does not argue or allege otherwise. Absent the Petition’s unsupported premise that is contradicted by the record, Petitioner’s motivation is inapplicable to the cited art. In other words, Petitioner has failed to establish a motivation to extend the length of Inukai 576’s left gate electrode. EX-2001, ¶ 79.

Second, contrary to Petitioner’s allegations, the endcap rule does not require or motivate design of gate electrodes to have *equal* length. Rather, the endcap rule only requires gates to have “a certain **minimum** length.” Pet., 52. Two gates can satisfy the endcap rule yet have unequal lengths, as is the case with Inukai 576. Nothing about the endcap rule requires or otherwise motivates two gates to be of equal length, let alone motivates modifications to an already-compliant gate. EX-2001, ¶ 80.

Third, the Petition fails to establish a reasonable expectation of success in extending the length of the left gate electrode in Inukai 576, as required by a motivation to combine rationale. MPEP 2143(I)(G)(1). The Petition alleges a reasonable expectation of success because “[t]he gate electrodes... are formed in... a different layer from the connection wiring layer 902” and “[a]s a result, those two regions will be electrically isolated from each other due to intervening insulating layers and a signal carried by one region will not interfere with a signal carried by the other.” Pet., 56 (citing Ex-1007, ¶[0267]). The Petition does not establish that the insulating layer would prevent signal interference between the gate electrode and the wiring portion 902 due to overlap. To the contrary, as mentioned in Section VI.A.a above, a POSITA would recognize that even if a gate electrode and the wiring portion were separated with an insulating layer, interference would still occur. *See* EX-2001, ¶¶ 52-58, 81-82; EX-2003 ¶ [0080], FIG. 6 (overlapping gate and data

line causes interference and deteriorates quality of displayed images, even with insulating layer in between). The Petition's conclusory statements that no interference would occur are no substitute for the required obviousness rationale. *KSR*, 550 U.S. at 418 (“[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements”).

As set forth above, the Petition does not sufficiently show either a motivation or a reasonable expectation of success for a POSITA to modify Inukai 576 such that the left gate electrode (“protrusion”) extends further than what is already clearly shown in FIG. 9 of Inukai 576.

b. Yamazaki does not cure the deficiencies of Inukai 576

Even if a POSITA would have found it obvious to extend the length of the left gate electrode in Inukai 576, such a modification would not have cured the above-noted deficiencies of Inukai 576. For example, Ground 1b's modification would not cure the fact that the gate electrodes in Inukai 576 are part of the alleged second electrode and explicitly distinguished from the control line. *See above* Section IV.A.a. Furthermore, Ground 1b does not cure Inukai's failure to disclose a wiring portion crossing a control line corresponding to the same unit circuit. *See above* Section IV.A.c. As such, even with the modification, the wiring portion would not cross a control line as required by the claim. EX-2001, ¶ 83.

C. The Petition has failed to establish a reasonable likelihood of prevailing on Grounds 2a because Inukai 574 fails to anticipate or render obvious the claimed wiring

Inukai 574 does not disclose a physical layout of a circuit in which a portion of a wiring crosses a control line, as required by claim 1. Instead, Inukai 574 discloses only circuit schematics without any description of a plan view of the corresponding physical layout. Where Inukai 574 does provide a description of a physical layout, it is clear that the wiring portion CANNOT cross the control line as they are formed on the same layer. EX-2001, ¶ 85. Petitioner fails to address this significant impediment, and therefore has not shown a reasonable likelihood of success on either Ground 2a or Ground 2b.

a. Inukai 574 fails to disclose a wiring portion that crosses a control line

Inukai 574 does not include any description or a plan view of a physical layout of a unit circuit that includes a wiring portion crossing a control line. FIG. 5 of Inukai 574 illustrates a schematic circuit diagram—NOT an actual physical layout showing the actual structural arrangement—including a control line 3801a, a control line 3801b, and a data line 3802a. EX-2001, ¶ 86. The Petition cites to a control line 3801a as the “control line,” a data line 3802a as the “data line,” a transistor 3806a as the “first transistor,” and a transistor (TFT) 3805b as the “second transistor”

of the Challenged Claim. *See* Pet., 63-80. Petitioner further cites to a wiring portion (annotated in red below) as the “wiring.”

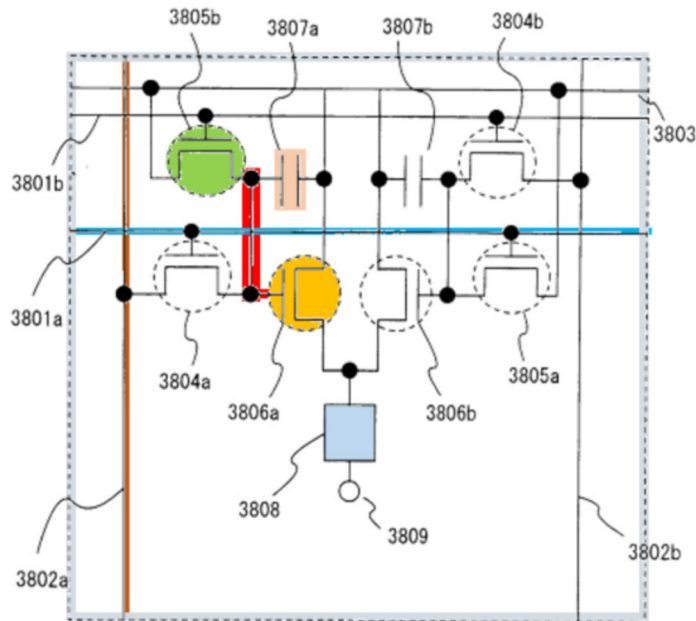


FIG. 5

FIG. 5 of Inukai 574 (annotated in Pet., 80)

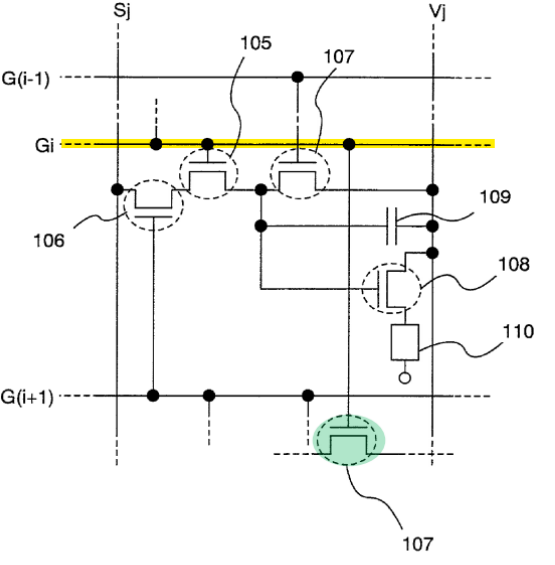
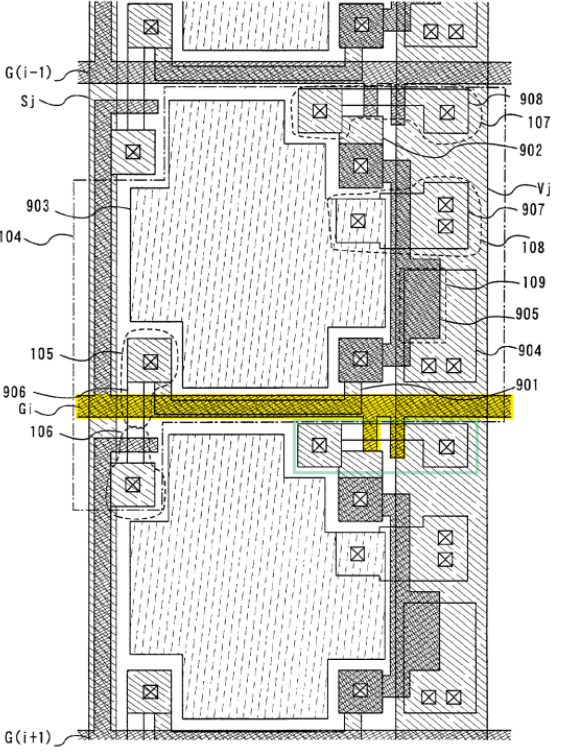
According to Petitioner, the circuit schematic shows the wiring portion crossing control line 3801a. But this does not amount to a teaching of the wiring portion crossing the control line 3801a in the actual implementation of the circuit. As conceded by Petitioner, Inukai 574 does not include any plan view or description of a wiring, connecting the erasing TFT 3805b to a gate of the EL driving TFT 3806a, that includes a portion crossing the gate wiring 3801a. Pet., 81-82. Instead, Petitioner alleges that the circuit schematic establishes a possible physical layout.

Pet., 79. According to Petitioner, this possible physical layout would have been an obvious modification to Inukai 574, because “[i]mplementing a circuit schematic using a circuit layout that generally reflects the same sort of geometry depicted by the schematic would have been a matter of common engineering practice, and typically the most straightforward way to implement the schematic.” Pet., 80. Petitioner is incorrect for a number of reasons. EX-2001, ¶ 87.

First, Petitioner’s allegation that a circuit schematic illustrates not just a possible physical layout, but the most straightforward implementation, is a baseless generalization with no support in the record. In fact, a POSITA would understand that a schematic circuit diagram does not necessitate or otherwise suggest a physical layout of the actual circuit to have its same geometry, and that other considerations such as circuit board size, heat dissipation, signal coupling between components, physical ruggedness, and space limitations would need to be considered in optimally designing the physical layout of the actual circuit. None of these factors are addressed or considered in the Petition’s unsupported oversimplification of circuit design. *See* EX-2001, ¶¶ 88-89.

A POSITA would understand that an actual circuit conforming to “the same sort of geometry” of a schematic circuit diagram is not a matter of common engineering practice, but nearly impossible. EX-2001, ¶ 90. In fact, the record provided by Petitioner establishes that the physical layout of a circuit does not mirror

the geometry of its corresponding circuit diagram. FIGS. 3 and 9 of Inukai 576 (EX-1006) illustrate a schematic circuit diagram and a corresponding plan view of the actual circuit, where the physical layout of the actual circuit does not correspond to or have “the same sort of geometry” as the circuit diagram, but is substantially different. This is abundantly clear by a side-by-side comparison of the two:

Circuit Schematic (Inukai 576)	Physical Layout (Inukai 576)
 Fig. 3	 Fig. 9

FIGS. 3 and 9 of Inukai 576 (annotated)

For example, in the schematic circuit diagram in FIG. 3 of Inukai 576, the gate of the lower TFT 107 for erasing (highlighted in green below G_i) is connected to the

signal line Gi in yellow. The wiring between the signal line Gi (highlighted in yellow) and the gate of the lower TFT 107 (highlighted in green) passes over multiple components such as, for example, the gate of TFT 108 for driving EL, an electrode of capacitor 109, and the source/drain of the upper TFT 107 for erasing.

However, in the actual physical layout of the circuit as illustrated in the annotated FIG. 9 of Inukai 576, the wiring connecting the signal line Gi (highlighted in yellow) and the gate of the lower TFT 107 for erasing (highlighted in green) does not pass over the above-mentioned components, *i.e.*, the gate of TFT 108 for driving EL, an electrode of capacitor 109, and the source/drain of the upper TFT 107 for erasing. EX-2001, ¶¶ 90-92.

Additionally, in the circuit schematic, the majority of the pixel unit's circuit components (*e.g.*, 105, 108, 110) are below the corresponding signal line Gi, whereas in the actual layout they are provided above the corresponding signal line Gi. Petitioner's allegation that the geometry of a physical layout can be understood from the circuit schematic is a dubious oversimplification contradicted by the record, which shows that a schematic circuit diagram would generally not conform to the actual layout of the circuit. EX-2001, ¶ 93.

Moreover, the Petition fails to address that a physical layout in which the alleged wiring portion of Inukai 574 crosses the gate signal line 3801a is NOT possible from the actual physical layout disclosed by Inukai 574 and relied on by

Petitioner. EX-2001, ¶ 94. To this end, the Petition cites to FIG. 16 of Inukai 574 for an actual implementation in which, according to Petitioner, the alleged wiring portion 36 is formed in a layer different from the first transistor's gate layer, as required by the claim (“wiring having *a portion formed in the layer different from a gate layer in which the gate of the first transistor is formed*, the portion crossing the control line”). Pet., 78. According to Petitioner, the wiring 36 highlighted in red in its annotation of FIG. 16 corresponds to the claimed wiring portion, and connects the switching transistor 3502, the alleged second transistor 3504, and the gate of the alleged first transistor 3503:

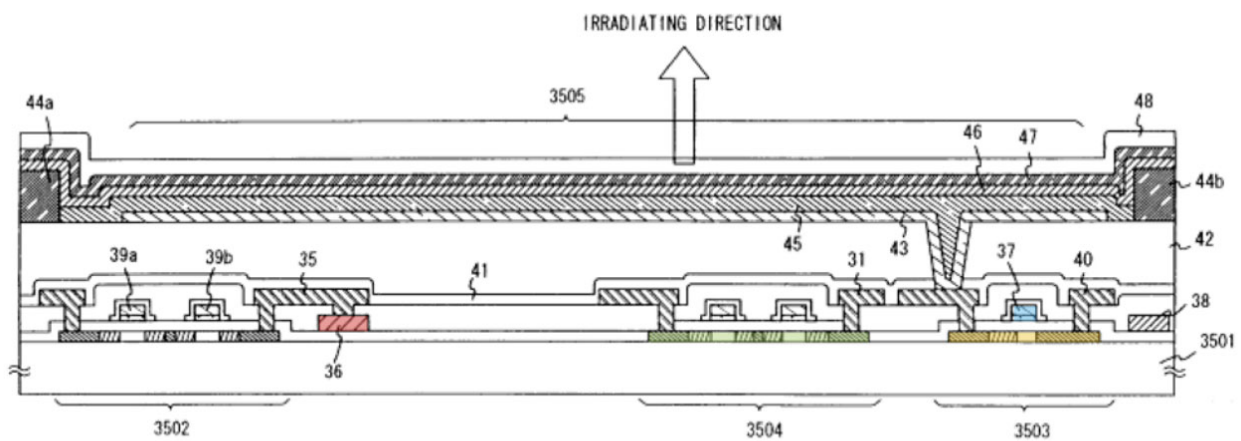


FIG. 16

FIG. 16 of Inukai 574 (annotated in Pet., 80)

Interestingly, Petitioner does not annotate the gate signal line 38 that that Petitioner alleges corresponds to the claimed control line crossed by the wiring portion. EX-2001, ¶ 95. The gate signal line 38 “connects the gate electrodes 38a,

38b of the switching TFT 3502.” EX-1008, ¶ [0290]. In other words, the gate signal line 38 corresponds to the gate signal line 3801a (alleged control line) connecting to the gates of the switching TFT 3804a in FIG. 5, which like in FIG. 16 is connected to the alleged second transistor 3805b and the gate of the alleged first transistor 3806a via the alleged wiring portion:

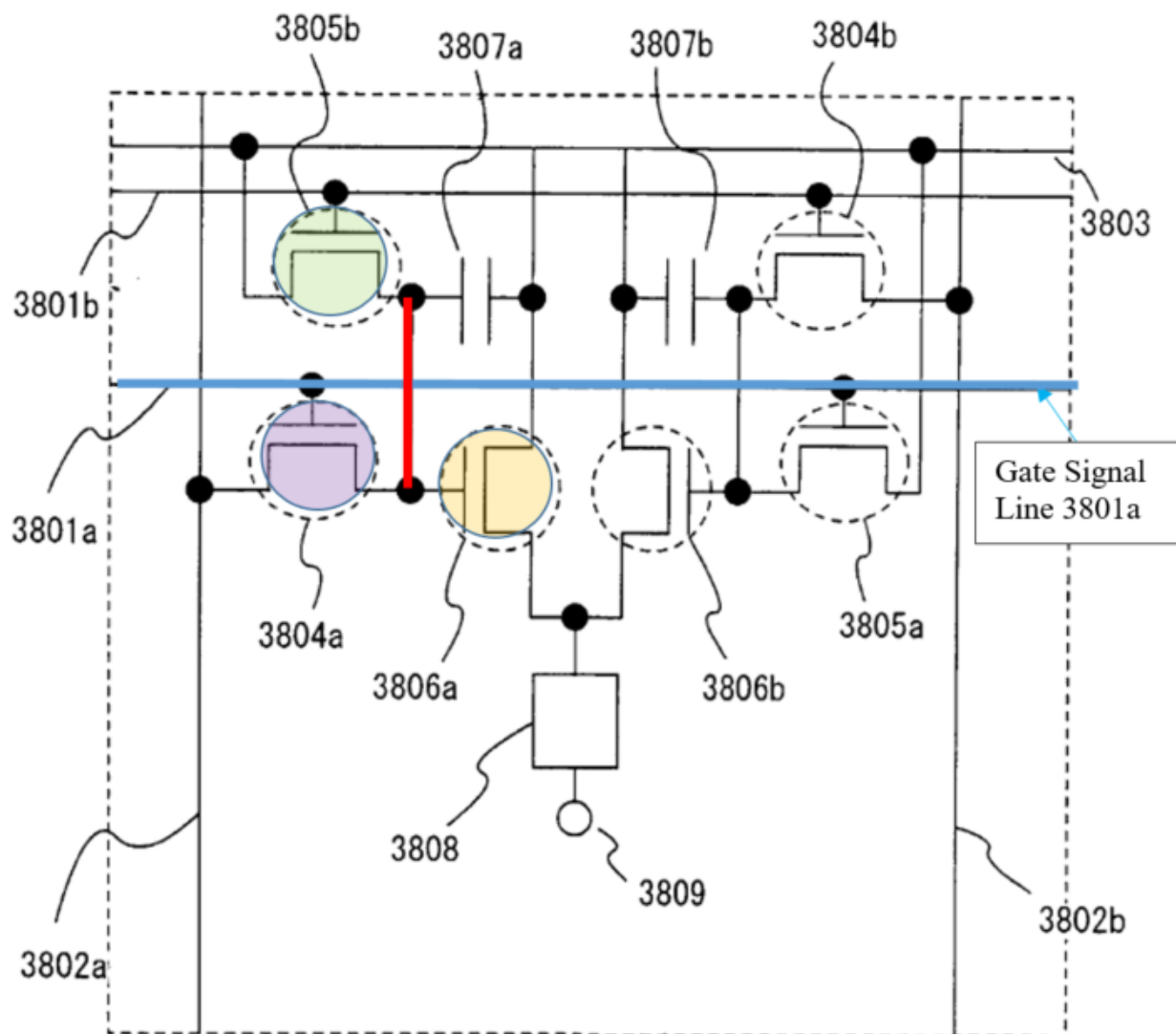


FIG. 5 of Inukai 574 (annotated)

Petitioner relies on the particular layer arrangement of the wiring portion 36 relative to other portions of the layout shown in FIG. 16 to allege invalidity of claim 1 (Pet., 77), but fails to note that this arrangement places the wiring portion on the exact same layer as the gate signal line 3801a:

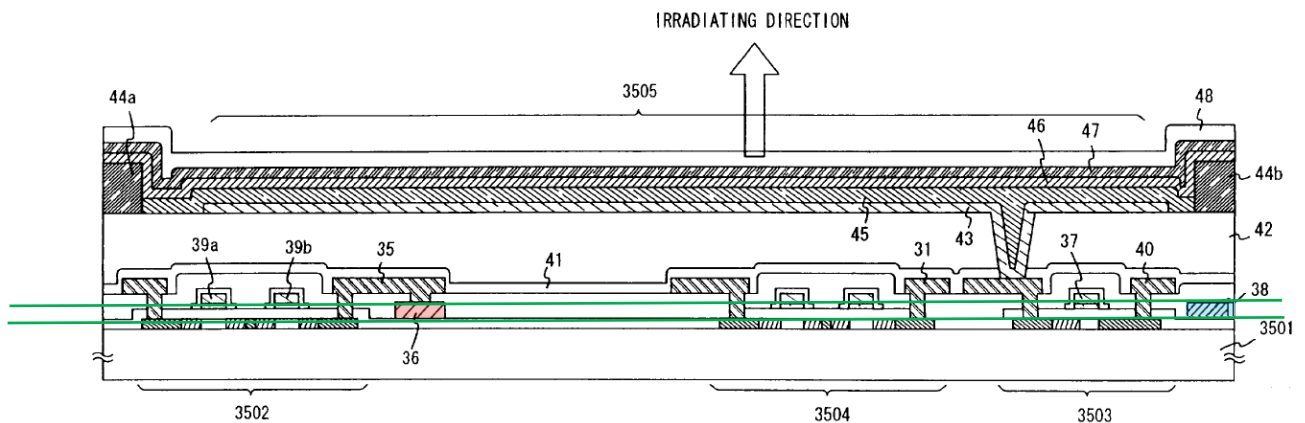


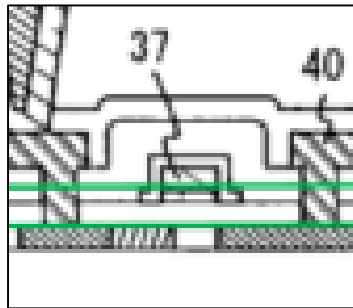
FIG. 16

FIG. 16 of Inukai 574 (annotated)

Thus, the physical layout disclosed in Inukai 574 and relied on by Petitioner prevents the alleged wiring portion 36 from crossing the gate signal line 38, as the two are on the same layer. EX-2001, ¶¶ 96-97. Petitioner entirely fails to address this disclosure of Inukai 574 that flatly contradicts its allegations of anticipation and obviousness.

Additionally, Petitioner cites to FIG. 16 of Inukai to allege that the wiring portion 36 and the alleged gate layer 37 are formed on different layers, as required

by claim 1. (Pet., 77). FIG. 16 (as annotated above, magnified below), however, shows the two components as overlapping in height and therefore not on different layers:



Magnified Annotation of FIG. 16; EX-2001, ¶ 98.

Accordingly, the Petition fails to sufficiently establish that Inukai 574 discloses or renders obvious its alleged wiring portion both crossing the control line Gi and formed on a different layer than a gate layer of the first transistor.

Ground 2a therefore fails as Inukai 574 does not disclose or render obvious a wiring portion as claimed.

b. Inukai 574 fails to disclose a unit circuit corresponding to a an intersection of a data line and a control line and comprising a wiring portion crossing that control line

Even assuming *arguendo* that the circuit schematic in FIG. 5 of Inukai reflects the physical layout of the circuit, Inukai 574 does not disclose a unit circuit including each of the constituent elements as arranged in the claim. Specifically, Inukai 574 fails to disclose a wiring portion, of a unit circuit, that crosses a control line corresponding to that unit circuit. EX-2001, ¶¶ 101-104.

The Challenged Claim recites a data line, a control line, and a unit circuit corresponding to an intersection of the two lines. A POSITA would have understood that the claim is defining its pixel unit circuit as corresponding to a particular intersection of a control line and a data line, which is a conventional pixel matrix arrangement well known in the art, including that of record in this proceeding. *See e.g.* EX-1008, ¶¶ [0010] and [0100]; EX-2001, ¶¶ 102-104.

In Inukai 574, for example, pixels are arranged in a matrix defined by particular intersections of control lines and data lines. EX-1008, ¶[0100], FIG. 2. As recognized by the Petition, Inukai 574's unit circuit *corresponds to the intersection* of a particular data line and scan (or control) line (*i.e.*, pixel unit). That is, Inukai 574 defines its pixel unit 107 (highlighted in orange below) corresponding to the intersection of the particular data line Sa1 (highlighted in green below) and the particular control line Ga1 (highlighted in blue below), *i.e.*, the intersections that define and thereby correspond to the matrix element in the active matrix arrangement that constitutes a unit pixel area:

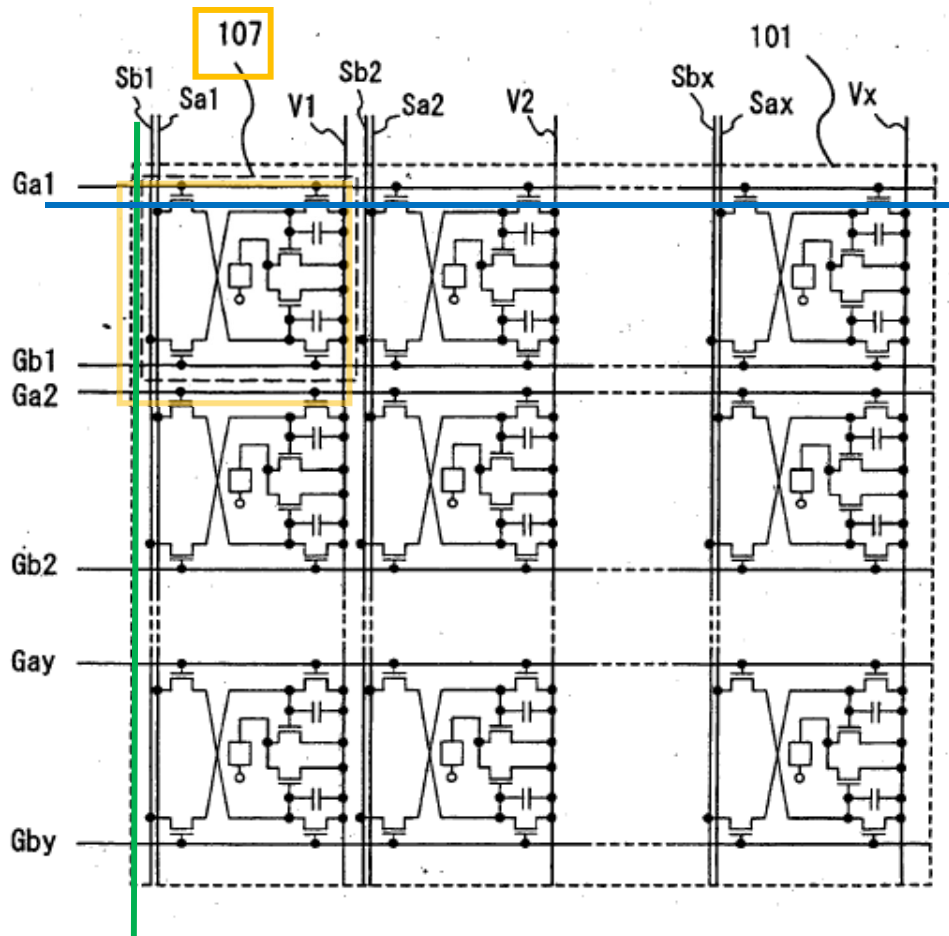


FIG. 2 of Inukai 574 (annotated)

The cited unit pixel circuit shown in FIG. 5 of Inukai 574 would have been understood as corresponding to the particular intersection of its outer control line 3801b and the data line 3802a, *i.e.*, the lines defining the matrix element that is the pixel unit, not the interior line 3801a that crosses through the middle of the unit circuit within the circuit schematic. EX-2001, ¶ 104. Thus, the control line 3801a cited by the Petition does not correspond to the claimed control line; at best, it is the outer control line 3801b that defines the pixel unit circuit area and the matrix

arrangement of pixels. The outer control line 3801b, however, is not crossed by the alleged wiring portion in the circuit schematic. Thus, even assuming *arguendo* that a physical layout of the circuit would conform to the circuit schematic in FIG. 5, Inukai 574 does not render obvious the claimed wiring portion that crosses the control line corresponding to the pixel unit circuit area.

D. The Petition has failed to establish a reasonable likelihood of prevailing on Grounds 2b because Yamazaki fails to cure the deficiencies of Ground 2a

Petitioner has failed to show a reasonable likelihood of success on Ground 2b, at least because Yamazaki fails to cure the deficiencies of Inukai 574 and Ground 2a, and Petitioner has failed to satisfy its burden of a *prima facie* case of obviousness.

a. Yamazaki does not cure the deficiencies of Inukai 574

Yamazaki does not cure the above-described deficiencies of Inukai 574's physical layout, in which the alleged wiring portion and the control line are on a same layer and therefore cannot cross. EX-2001, ¶¶ 106-110.

As an initial point, the Petition's brief obviousness allegation in no way addresses the inability of Inukai 574's wiring portion to cross a control line on its same layer. The Petition does not explain how or why the combined teachings of Yamazaki and Inukai 574 would have overcome this impediment in the primary reference.

In fact, Yamazaki's electrode 806 (alleged wiring portion) is able to cross the control line 802 because they are formed on different layers, a construction that does not exist in Inukai 574. Petitioner does not allege that it would have been obvious to modify Inukai 574's arrangement of components and formation of layers or otherwise provide any basis to support such a conclusion. Nor does Petitioner allege how such a modification would impact other requirements of the claim, such as the requirement that the wiring portion that crosses the control line be *formed on a different layer* than the gate of the first transistor. Contrary to the Challenged Claim, the crossing portion in Yamazaki is itself a component of the second transistor (annotated in green below) and is *formed on the same layer* as the gate of the first transistor (annotated in orange below). EX-2001, ¶¶ 108-109.



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much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art”); *see also Eli Lilly & Co. v. Actavis Elizabeth LLC*, 435 F. App'x 917, 921 (Fed. Cir. 2011) (“entirety of the prior art must be considered in determining obviousness”); EX-2001, ¶ 110.

In sum, the Petition’s modification of Inukai 574 by the teachings of Yamazaki (1) does not address or otherwise overcome the preventative limitation in Inukai 574 (*i.e.*, that the wiring portion is on the same layer as the control line and therefore cannot cross), and (2) does not address that the relied-upon teachings of Yamazaki violate other limitations of the Challenged Claim (*e.g.*, “a [wiring] portion formed in the layer different from a gate layer... of the first transistor”).

As such, the Petition’s allegation that Yamazaki would have rendered obvious an unworkable physical layout in Inukai 574 is unsubstantiated and conclusory at best. Ground 2b, therefore, fails to establish a reasonable likelihood of success. *KSR*, 550 U.S. at 418 (“[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements”).

b. Petitioner fails to establish *prima facie* case of obviousness in modifying Inukai 574 in view of Yamazaki

Petitioner attempts to support its conclusory obviousness analysis by alleging a “reasonable expectation of success” for two reasons: (1) “Inukai 574 does not

restrict how its circuits must be laid out by specifying particular plan views”; and (2) “the schematic views of both references depict transistors connected by a wire that crosses a gate wiring.” Pet., 82. Petitioner is flatly wrong on both accounts. EX-2001, ¶¶ 111-121.

First, as discussed above, Inukai 574 does in fact provide a description of a physical implementation at FIG. 16 (relied on by Petitioner in an attempt to show other structural features of the claim, Pet., 78) that restricts how its circuits must be laid out. Namely, this physical implementation provides the alleged wiring portion on a particular layer (cited and relied on by Petitioner in Grounds 2a and 2b) that is the same layer as the control line, therefore restricting a crossing of the two. EX-2001, ¶ 112. Grounds 2a and 2b ignore this critical disclosure, and therefore fail to show a reasonable likelihood of success. *In re Wesslau*, 353 F.2d at 241 (improper to “pick and choose” parts of reference to exclusion of “other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art”); *see also Eli Lilly*, 435 F. App'x at 921 (must consider entirety of prior art).

Second, and contrary to Petitioner’s allegation, the schematic view of Yamazaki does NOT “depict transistors connected by a wire that crosses a gate wiring.” Instead, Yamazaki explicitly discloses that the portion crossing the gate wiring is an electrode (not wiring) that is part of (not connected to) the second transistor. EX-1011, ¶¶ [0030] and [0168]; EX-2001, ¶ 113.

In detail, Petitioner relies on the portion annotated in red in FIGS. 8 and 9 of Yamazaki below as the alleged wiring, and the transistors 906 and 902 as the alleged first transistor and the second transistor. However, Yamazaki at FIG. 8 and the corresponding description in the specification explicitly discloses that the portion annotated in red is a second *electrode* 806 which is an electrode of the erasing transistor (TFT) 902. EX-1011, ¶¶[0030] and [0168]; EX-2001, ¶ 114.

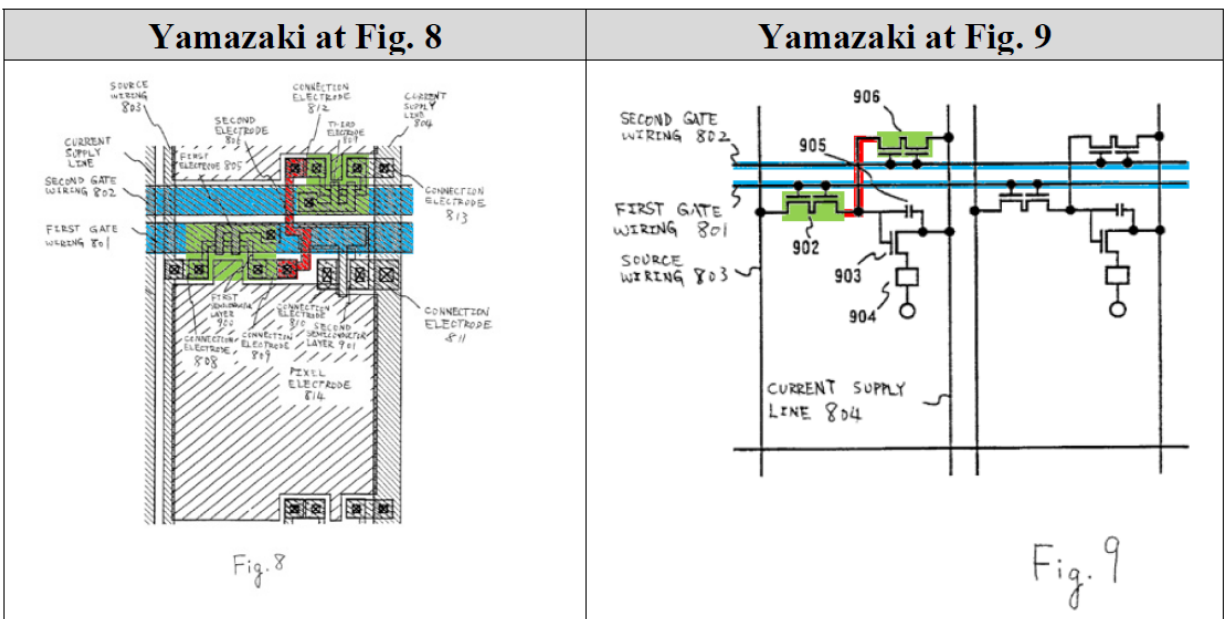


FIG. 9 of Yamazaki (annotated in Pet., 84)

That is, Yamazaki distinguishes electrodes from wiring, and the alleged wiring portion in Yamazaki is not a wiring portion but an *electrode* (“second electrode 806”). EX-1011, ¶[0030]. Further, the second electrode 806 is not connected to the transistor, but is explicitly a part of transistor (erasing TFT) 906 as a source/drain of the transistor 906. EX-1011 ¶¶ [0166]-[0168]; EX-2001, ¶ 115.

Contrary to the Petition’s unsupported allegation that the two references have “similar circuitry,” the circuits in Inukai 574 and Yamazaki have substantial differences, as discussed above and as further set forth in Dr. Aris’ Declaration. EX-2001, ¶¶ 116-121. By entirely ignoring these differences and relying on mischaracterizations of the cited art as the basis for its insufficient obviousness allegation, Petitioner has failed to show a reasonable likelihood of success with respect to both Grounds 2a and 2b.

VII. THE BOARD SHOULD EXERCISE ITS AUTHORITY AND DENY INSTITUTION IN VIEW OF FINTIV AND JUDICIAL ECONOMY

The Board should exercise its discretion to deny institution under 35 U.S.C. §314(a) “because institution of a trial at the PTAB would be an inefficient use of Board resources in light of the ‘advanced state’ of the parallel district court litigation in which the petitioner had raised the same invalidity challenges.” *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11, 2 (PTAB 2020) (precedential) (“*Fintiv*”) (citing *NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 (PTAB 2018) (precedential) (“*NHK*”).

In determining whether to deny institution, the Board is to consider the presence and status of parallel district court litigation. *See NHK*, 11 and *Fintiv*, 11. *Fintiv* sets forth a non-exhaustive list of factors that balance system efficiency and fairness considerations when considering discretionary denial. *Fintiv*, 5–6:

1. Whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. Proximity of the court's trial date to the Board's projected statutory deadline for a final written decision;
3. Investment in the parallel proceeding by the court and the parties;
4. Overlap between issues raised in the petition and in the parallel proceeding;
5. Whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. Other circumstances that impact the Board's exercise of discretion, including the merits.

Id.

Additionally, the *Fintiv* factors should be considered in view of the guidance provided in the June 21, 2022 Memo regarding Post-Grant Proceedings with Parallel District Court Litigation. ("*Fintiv* Memo"). EX-2011.

Discretionary denial is warranted here because institution would be an inefficient duplication of a parallel district court litigation in which the same grounds of invalidity are being raised by Petitioner. Each *Fintiv* factor favors exercising discretion to deny institution and none of the circumstances presented in the *Fintiv* Memo are applicable because Petitioners did not present compelling evidence of

unpatentability (*see* section V), there is no parallel ITC proceeding, and the Petitioners have not submitted a *Sotera* stipulation.

A. Factor 1: Whether a Stay Exists or is Likely to be Granted

The District Court has not instituted a stay, the Petitioners have not filed a motion to stay the District Court litigation, and there is no evidence that a stay would be granted if this IPR proceeding is instituted. This factor weighs against institution. *See Fintiv*, 12.

B. Factor 2: Proximity of the District Court’s Trial Date

Trial with Petitioners in the District Court is scheduled to start on May 20, 2024, nearly five months before the projected deadline on October 13, 2024 for when any final written decision would be due should this petition be instituted. *See* 35 U.S.C. §§314(b) (“The Director shall determine whether to institute an *inter partes* review under this chapter pursuant to a petition filed under section 311 within 3 months after ... receiving a preliminary response to the petition under section 313.”) and 316(a)(11) (“requiring that the final determination in an *inter partes* review be issued not later than 1 year after the date on which the Director notices the institution of a review under this chapter.”); EX-2011. There is no reason to believe that trial will be delayed.

Petitioners argue that, based on Federal Court management statistics at uscourts.gov, the median time from filing to trial in the Eastern District of Texas is

ordinarily 24.5 months, and thus, according to that estimate, the trial for the District Court litigation would likely take place in April 2024 since Patent Owner filed the complaint on April 18, 2022. Pet., 85. Petitioners' argument demonstrates that the actual trial start date of May 20, 2024 is unlikely to be moved to a later date, at least since the actual trial start date gives the parties and court an additional month to prepare for trial in comparison to an estimated trial start date of April 2024 (that is based on Petitioners' alleged median period of filing to trial of 24.5 months).

Petitioners further argue that the median time to trial should be measured from the date of service² of the complaint, instead of the date of filing of the complaint.

² Patent Owner filed the Complaint on April 18, 2022, and then initiated the Hague process for international service, and sent via Federal Express, a copy of the Complaint with exhibits and a waiver form, in both English and Chinese, to each of the Petitioners, requesting the Petitioners to waive formal service. EX-2008, 3-4. Because none of the Petitioners had responded to these requests and one of the Petitioners has refused to accept the Federal Express package, Patent Owner requested leave, on July 22, 2022, from the District Court to serve the Petitioners through alternative means. *Id.* The Court granted the motion for leave on September 22, 2022, and the Petitioners were served the Complaint thereafter. EX-2009.

Pet., 86. However, Petitioners have not provided any evidence related to the Federal Court management statistics to support this contention. Instead, a document, from uscourts.gov that explains terms of the Federal Court management statistics, states that statistics on median time to trial is measured from the “date a case was filed.” EX-2007, 2. Even under Petitioner’s unsupported contention of such a later trial date, such a later trial date would still precede the expected Final Written Decision deadline.

Moreover, the most recent Federal Court management statistics indicate that, in the latest 12-month period ending on March 31, 2023, the median time from filing to trial in the Eastern District of Texas is 19.0 months, not 24.5 months as contended by the Petitioners. EX-2006, 35. Thus, even if the median time to trial is measured from the service date of the complaint of September 27, 2022, as erroneously contended by the Petitioners, instead of correctly from the filing date of April 18, 2022, the estimated trial start date would be April 2024 based on the most recent statistical data of median time (19.0 months). Such date is still a month before the currently scheduled trial start date of May 20, 2024, and over fourth months before the Final Written Decision deadline of October 13, 2024, should this petition be instituted.

Also, in the District Court litigation, subsequent to the last service date of the Complaint of which the Petitioners alleged caused a delay, Petitioners and Patent

Owners jointly agreed to entry of a proposed docket control order on February 2, 2023, which stated that jury selection for trial should be on May 20, 2024, and the court established such date for the jury selection. EX-1015 (Docket Control Order); EX-2010 (Joint Motion for Entry of Agreed Docket Control Order). Since Patent Owner, Petitioners, and the District Court established that May 20, 2024 was a suitable date to start trial, and because no material delay has occurred after filing of the proposed docket control order and entering of the docket control order, there is no evidence that the trial date of May 20, 2024, will be moved to a later date.

Given that at least the trial in the District Court will proceed well before the Final Written Decision deadline, this factor favors denial of institution. *Roku, Inc. v. IOENGINE, LLC*, No. IPR2022-01554, Paper 11 (PTAB 2023) (“Roku”); *Samsung Electronics Co. Ltd. v. California Institute of Tech.*, No. IPR2023-00130, Paper 10 (PTAB 2023) (“Samsung”); *Google, LLC. v. Personalized Media Comm., LLC.*, IPR2020-00723, Paper 22, 7 (PTAB 2020).

C. Factor 3: Investment in the Parallel Proceeding

Under the third factor, the Board is to “consider[] the amount and type of work already completed in the parallel litigation by the court and the parties at the time of the institution decision.” *Fintiv*, 9.

Patent Owner, Petitioners, and the District Court have already spent and will continue to spend significant resources on litigating '760 patent at and around the time of the institution decision.

Discovery is on-going in the District Court litigation, with both parties having already exchanged document requests and interrogatories. Additionally, infringement and invalidity contentions have been exchanged, and proposed claim terms for claim construction have been exchanged.

Around October 12, 2023, the approximate date for the institution decision, the exchange of claim construction briefs between the Patent Owner and the Petitioners should be ongoing, and the Patent Owner, Petitioners, and the District Court will conduct the Markman Hearing shortly thereafter on November 7, 2023. EX-1015.

The parties' substantial investment in the District Court litigation favors denial of institution. *See Canadian Solar Inc. v. The Solaria Corporation*, IPR2021-00095, Paper 12, 11 (PTAB 2021).

D. Factor 4: Overlap Between Issues Raised in the Petition

Under the fourth factor, as the Board found in *Fintiv*, “if the petition includes the same or substantially the same claims, grounds, arguments, and evidence as presented in the parallel proceeding, this fact has favored denial.” *See Fintiv*, 12.

Issues related to the '760 Patent are being litigated in the parallel District Court litigation. Petitioners already set forth the grounds raised in this Petition in their invalidity contentions.

Additionally, Petitioners refuse to mitigate concerns of potentially conflicting decisions and duplicative efforts by failing to submit a stipulation in the District Court proceedings or elsewhere per *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020) (precedential). Pet., 6 (Petitioners only agreed to “cease asserting in the district court any invalidity contention based on the prior art presented in this petition that constitutes part of a ground.” Petitioners omit a stipulation with respect to any ground that reasonably could have been raised, as required for *Sotera* to apply.)

These circumstances favor denial of institution. See *Roku*, 11 (PTAB 2023); *Samsung*, 10 (PTAB 2023); *Sand Rev’n II LLC v. Cont’l Intermodal Grp. – Trucking LLC*, IPR2019-01393, Paper 24, 7 (PTAB 2020) (informative); *Sotera*, 18 (weighing Factor 4 in favor of denial of institution based on “concerns of inefficiency and the possibility of conflicting decisions”).

E. Factor 5: Whether Petitioners and the Defendant(s) in the Parallel Proceeding(s) are the Same Party

The Petitioners and the Defendants in the District Court litigation are the same parties. This factor favors denial of institution.

F. Factor 6: Other Circumstances that Impact the Board’s Exercise of Discretion, Including the Merits

The Board is to consider the merits of a petitioner’s challenge when determining whether to institute a post-grant proceeding in view of parallel district court litigation. EX-2011, 4. As explained in more detail above in section V, Petitioners have failed to meet their burden under 37 C.F.R. §42.108(c) of establishing a reasonable likelihood of success that any of the challenged, pending claims are unpatentable, let alone a compelling case. *CommScope Techs. LLC v. Dali Wireless, Inc.* IPR2022-01242, Paper 23, 3 and 5 (PTAB 2023) (precedential) (“As the Guidance Memo and my precedential decision in *OpenSky* make clear, the compelling merits standard is a higher standard than the standard for institution set by statute.”) (“[T]he Board must provide reasoning sufficient to allow the parties to challenge that finding and sufficient to allow for review of the Board’s decision.”).

In sum, each of the *Fintiv* factors weigh in favor of denying institution, and the Board should exercise its discretion in accordance therewith.

VIII. CONCLUSION

For at least the foregoing reasons, Petitioner fails to establish a reasonable likelihood of success with regard to Grounds 1a, 1b, 2a, and 2b. Therefore, the Petition should be denied in its entirety.

Respectfully submitted,

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July 13, 2023

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), Patent Owner hereby certifies that the present paper contains 9,254 words (as counted by the “Word Count” feature of Microsoft Word™). This word count excludes the table of contents, table of authorities, table of exhibits, certificate of word count, and certificate of service.

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CERTIFICATE OF SERVICE

The undersigned certifies that a copy of the attached Patent Owner Preliminary Response is being served by electronic mail on the following counsel of record:

/Soo Jin Hur/

Date: July 13, 2023