UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,
BEIJING BOE DISPLAY TECHNOLOGY CO., AND
MOTOROLA (WUHAN) MOBILITY TECHNOLOGIES
COMMUNICATION CO., LTD.,
Petitioner

v.

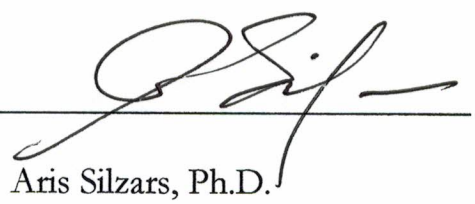
ELEMENT CAPITAL COMMERCIAL COMPANY PTE. LTD,
Patent Owner.

IPR2023-00696
U.S. PATENT NO. 8,525,760

DECLARATION OF DR. ARIS SILZARS

Declaration

I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

By: 

Aris Silzars, Ph.D.

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I, Dr. Aris Silzars, do hereby declare:

1. I am making this declaration at the request of Element Capital Commercial Company PTE. LTD in the matter of the BOE Technology Group Co., Ltd., Beijing BOE Display Technology Co., and Motorola (Wuhan) Mobility Technologies Communication Co., Ltd., petition for *inter partes* review of IPR2023-00696.

2. I am being compensated for my work in this matter at my standard hourly rate of $350 for consulting services. My compensation in no way depends on the outcome of this proceeding or the content of my testimony.

3. In preparing this Declaration, I considered the following materials:

a. U.S. Patent No. 8,525,760 to Yojiro Matsueda ("the '760 patent") (EX-1001)

b. Prosecution History of U.S. Application No. 10/299,861 (EX-1002)

c. Prosecution History of U.S. Application No. 11/483,109 (EX-1003)

d. Prosecution History of U.S. Application No. 12/917,885 (EX-1004)

e. P.C.T. Published Application No. WO98/36407 ("Ozawa") (EX-1005)

f. Declaration of Dr. David K. Liu (EX-1006)

g. U.S. Pub. No. 2002/0000576 to Kazutaka Inukai ("Inukai 576") (EX-1007)

h. European Pub. No. EP1111574A2 ("Inukai 574") (EX-1008)

i. U.S. Patent No. 7,277,070 to Jun Koyama ("Koyama") (EX-1009)

j. U.S. Patent No. 5,498,579 to Yan A. Borodovsky et al ("Borodovsky") (EX-1010)

k. U.S. Pub. Patent No. 2001/0025959 to Shunpei Yamazaki et al ("Yamazaki") (EX-1011)

l. Fabrice Caignet et al, The Challenge of Signal Integrity of Deep-Submicrometer CMOS Technology, 89 Proceedings of the IEEE, No. 4 (April 2001) ("Caignet") (EX-1012)

m. Flat Panel Displays for Portable Systems by Kalluri R. Sarma and Tayo Akinwande, Journal of VLSI Signal Processing Systems13, 165-190 (1996) ("Sarma") (EX-1013)

n. Complaint, *Element Capital Commercial Company PTE. Ltd. v. BOE Technology Group Co., Ltd. et al*., Case No. 2:22-cv-0118-JRG (EDTEX) (EX-1014)

o. Joint Agreed Scheduling Order, *Element Capital Commercial Company PTE. Ltd. v. BOE Technology Group Co., Ltd. et al.,*Case No. 2:22-cv-0118-JRG (EDTEX) (EX-1015)

p. The Petition filed by the Petitioner.

q. U.S. Patent Pub. No. US 2007/0236620 to Yan. (EX-2003)

r. U.S. Patent No. 5,317,178A to Wu (EX-2004)

s. U.S. Patent No. 6,739,931 B2 to Yamazaki et. Al. (EX-2005)

I. Professional Background

4. Information concerning my professional qualifications, experience, and publications, and the matters in which I have served as an expert, are set forth in my current curriculum vitae (EX-2002).

5. I received my Bachelor of Arts degree in Physics in 1963 from Reed College in Portland, Oregon. I received my Master of Arts degree in Physics in 1965 from the University of Utah. I received my Doctoral degree in Electrical Engineering in 1969 from the University of Utah.

6. I have been an active participant in the development of display device technologies and products that use displays since 1974. I have managed research groups as large as 350 technologists in creating and implementing display device technologies and high performance electronic circuits into products based on these technologies.

7. I have participated in numerous technical conference activities (including Program and General Chair of the International Society for Information Display symposium – the preeminent annual international conference on display technology) and made numerous presentations on display applications and on the technology evolution of those products. I was President of the Society for Information Display ("SID") from 2000 to 2002. With over 7000 members, SID is the premier organization for professionals and academics in the fields of display research, design, manufacturing, applications, standards development, and marketing.

8. Since 1995, I have been an independent industry consultant with a broad client base and continue to be active and knowledgeable regarding all new display device-related technologies. My area of expertise encompasses the fields of information display technology, liquid crystal, OLED, and LED displays, digital integrated circuits and systems, mechanical design, and packaging for electronic products and semiconductor technology.

9. I have authored over 100 publications, most related to display device technology. I am also a named inventor on fifteen patents, most of which are related to or in the field of display device technology. In my many years of engineering, manufacturing, and product development experience, I have personally been involved in the design of large segmented LED displays, including obtaining two patents on which I am a co-inventor.

II. ’760 Patent Technologies

10. The ’760 patent and features recited in claim 1 pertain to methods of driving electro-optical devices, and particularly active matrix driving in active matrix displays.

11. In an active matrix display, a plurality of pixels is arranged in a matrix and typically provided on a display panel. Each of the plurality of pixels comprises a pixel circuit (sometimes referred to as a “unit circuit”), which comprises an electro-

optical element and a driving transistor. The driving transistor supplies power to the electro-optical element in order to drive a pixel. A data line and a control line are used to address each pixel, and each plurality of pixels is arranged with respect to the intersection of the data line and the control line.

12. In order to control and optimize the brightness and quality of the display, the specific layout of each pixel circuit is one of the important considerations when designing and manufacturing an active matrix display.

III. Relevant Legal Standards

13. I have been asked to provide my opinions as to whether claim 1 of the '760 patent would have been obvious to a person of ordinary skill in the art ("POSITA") at the time of the filing date of the '760 patent.

14. I am an engineer by training and profession. The opinions I express in this declaration involve the application of my technical knowledge and experience to the evaluation of certain prior art with respect to the '760 patent. In addition, I understand that the following legal principles apply.

15. It is my understanding that, in determining whether claims of the '760 patent are obvious in this proceeding, the claim terms are generally given their ordinary and customary meaning as understood by a POSITA. A POSITA would

read the claim terms in the context of the entire patent specification in which they appear, as well as the prosecution history of the patent.

16. It is my understanding that a claim is anticipated under 35 U.S.C. § 102 if each and every element and limitation of the claim is found, either expressly or inherently, in a single prior art reference. I also understand that a reference must disclose all claimed elements as arranged in the claim, although identical terminology need not be used in the reference and claim elements.

17. It is my understanding that a claim is unpatentable under 35 U.S.C. § 103 if the claimed subject matter as a whole would have been obvious to a POSITA in the art at the time of the alleged invention. I also understand that an obviousness analysis takes into account the scope and content of the prior art, the differences between the claimed subject matter and the prior art, and the level of ordinary skill in the art at the time of the invention.

18. In determining the scope and content of the prior art, it is my understanding that a reference is considered relevant prior art if it falls within the field of the inventor's endeavor. In addition, a reference is prior art if it is reasonably pertinent to the particular problem with which the inventor was involved. A reference is reasonably pertinent if it logically would have commended itself to an inventor's attention in considering his problem. If a reference relates to the same

problem as the claimed invention, that supports use of the reference as prior art in an obviousness analysis.

19. To assess the differences between prior art and the claimed subject matter, it is my understanding that 35 U.S.C. § 103 requires the claimed invention to be considered as a whole. This "as a whole" assessment involves showing that one of ordinary skill in the art at the time of invention, confronted by the same problems as the inventor and with no knowledge of the claimed invention, would have selected the elements from the prior art and combined them in the claimed manner.

20. It is my further understanding that several rationales may be applied for combining references or modifying a reference to show obviousness of claimed subject matter. These rationales include: combining prior art elements according to known methods to yield predictable results; simple substitution of one known element for another to obtain predictable results; a predictable use of prior art elements according to their established functions; applying a known technique to a known device (method or product) ready for improvement to yield predictable results; choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and some teaching, suggestion, or motivation in

the prior art that would have led one of ordinary skill to modify a prior art reference or to combine prior art teachings to arrive at the claimed invention.

IV. Person of Ordinary Skill in the Art

21. It is my understanding that when interpreting the claims of the '760 patent I must do so based on the perspective of one of ordinary skill in the art at the relevant priority date. My understanding is that the earliest claimed priority date of the '760 patent is November 20, 2001.

22. It is my opinion that one of ordinary skill in the art in the field of display device technology in the 2001 time period, would have had at least a Master's degree in electrical engineering, physics, or a related field, and at least two years of relevant work experience in the field of display device technology. Additional education can remedy lack of work experience and vice versa.

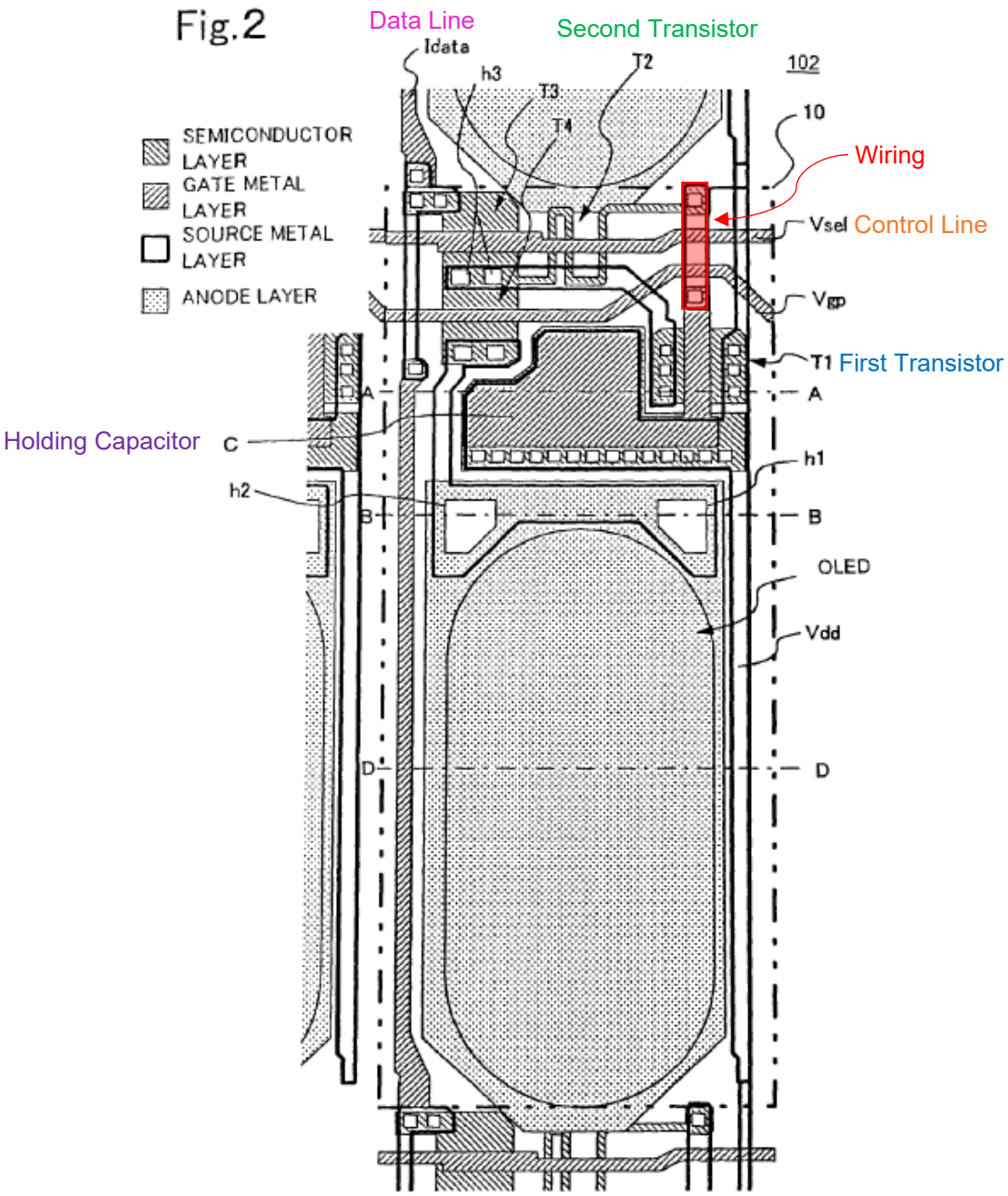
23. I am a person of at least ordinary skill in the art and was so at the time of the invention of the '760 patent.

V. Overview Of The Subject U.S. Patent No. 8,525,760

24. The '760 patent was assigned to Seiko Epson Corporation, the principal named inventor is Yojiro Matsueda. The patent is titled "Electro-Optical Device, Active-Matrix Substrate, and Electronic Apparatus."

25. The ’760 Patent is directed to an active matrix type electro-optical device, for example, an organic light-emitting diode (“OLED”) display. EX-1001, column 1, lines 14-16. In particular, the ’760 Patent aims to improve brightness of the electro-optical device by increasing a region occupied by the electro-optical element that emits light while decreasing a region occupied by a peripheral circuit driving an electro-optical element in each pixel. EX-1001, 14:26-32. This decrease in the circuit region is achieved by the particular layout and configuration of circuit components as disclosed in the patent. EX-1001, 18:62-65.

26. The ’760 Patent describes each pixel unit corresponds to an intersection of a data line and a control line. EX-1001, 1:27-29. As shown below, FIG. 2 of the ’760 Patent illustrates a plan view of a pixel unit 10 corresponding to an intersection of the data line Idata and control line Vsel.



Annotated FIG. 2 of the '760 Patent

27. As shown above, the pixel unit 10 includes a light-emitting portion OLED (electro-optical element) and a peripheral circuit to drive the light-emitting portion OLED. In particular, the peripheral circuit includes a first transistor T1, a second transistor T2, and a holding capacitor C. The source of the second transistor T2 is connected to the gate of the first transistor T1 through a wiring (highlighted in red above). Notably, the wiring crosses the control line Vsel corresponding to its same pixel unit circuit.

28. The physical layout of the peripheral circuit is an important aspect of optimizing the design, in view of the number of layers used to, as well as the arrangement (particularly by having wiring which crosses the control line, the amount of lateral space taken up by the circuit is reduced).

29. Another objective of the ’760 patent is to increase stability of holding capacitances of the holding element (which is used to hold the control voltage) and reduce leakage currents. To this end, a second transistor which may be a multi-gate transistor (T2) is connected directly to a holding capacitor. Since the second transistor is connected to the holding capacitor, leakage current may be suppressed. Accordingly, variations and/or fluctuation in viewing brightness of the display may be averted. *See* EX-1001, 3:5-10 and 18:15-60.

VI. Prosecution History of the Subject U.S. Patent No. 8,525,760

30. I have reviewed the file history of U.S. Patent Application No. 12/917,885 (the "Patent Application"), from which the '760 patent issued.

31. I note that in the Office Action dated February 13, 2013, the Examiner stated that claim 21 (which later issued as claim 1) is allowed because the cited art "does not disclose that a wiring connecting the second transistor and the gate of the first transistor comprises a portion formed in a layer other than semiconductor layer or the gate layer of the first transistor, and said portion crossing the control line of the electro-optical device." EX-1004, 880.

32. This contradicts the statement in the Petition that "[t]he Examiner did not provide reasons for the allowance." Pet., 17.

VII. Summary of Alleged Prior Art

A. US. Pub. No. 2002/0000576 ("Inukai 576") EX-1007

33. Inukai 576 is directed to an active matrix display device formed by electroluminescence elements EL. EX-1007, ¶[0002]. FIG. 3 of Inukai 576 illustrates a circuit diagram of a pixel unit (j,i) 104 of the EL display. As with the '760 Patent, and as is well known in the art, each pixel unit corresponds to a control line Gi and a data line Sj. *See* EX-2005, 16:61-65 and FIG. 9A and 9B and description ina ¶71 below.

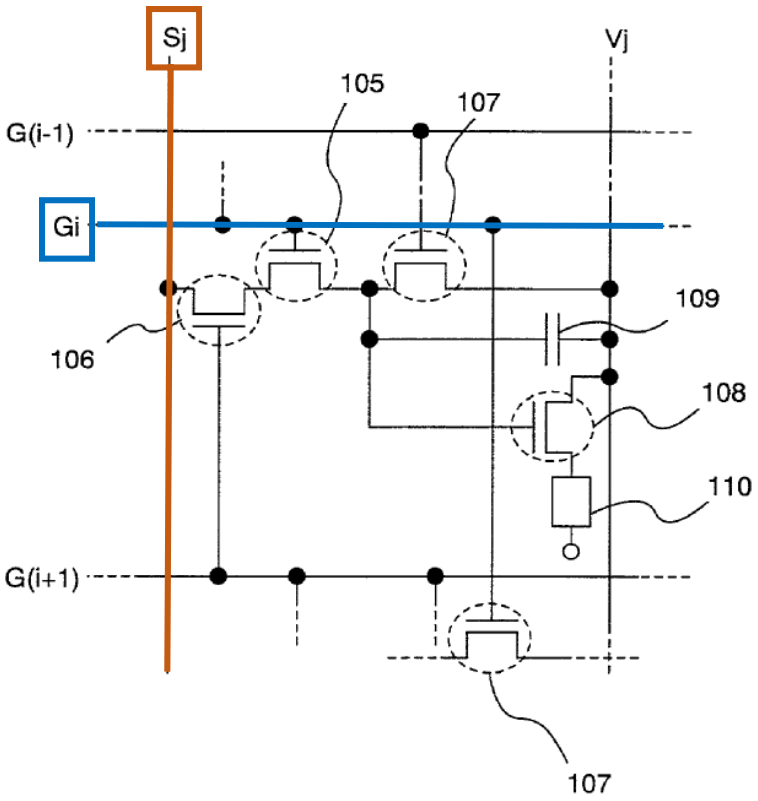


FIG. 3 of Inukai 576

34. As shown above, the pixel unit (j,i) 104 circuit includes a transistor 105 for switching, a transistor 106 for switching, a transistor 108 for EL driving, a capacitor 109, and an EL element 110. FIG. 3 of Inukai 576 also illustrates a transistor 107 for erasing that is connected to a control line G(i-1) corresponding to a different pixel unit (j, i-1) than the pixel unit (j,i) 104 including the transistors 105, 106, the capacitor 109, the EL element 110, etc., shown in the figure.

35. FIG. 9 of Inukai 576 reproduced below is a plan view of the pixel unit (j,i) 104 in FIG. 3 of Inukai 576.

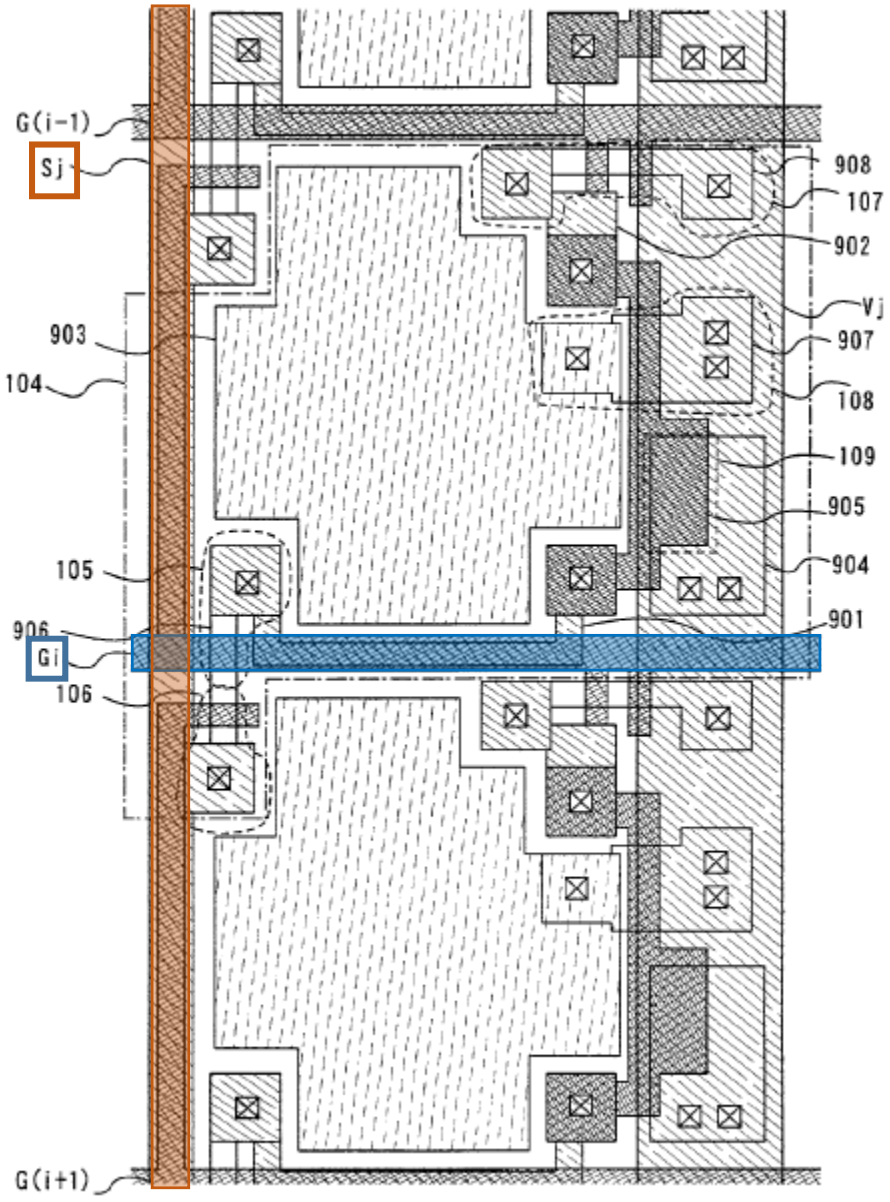


FIG. 9 of Inukai 576

36. As shown above and described in the reference, the pixel unit (j,i) 104 is defined by a region corresponding to a data line Sj and a control line Gi. EX-1007, ¶¶[0075], [0077]. Further, the transistor 108 for EL driving uses a part of the gate wiring 905 as its gate electrode and the gate wiring 905 is connected through a connection wiring 902 to a source/drain of the TFT 107 for erasing. The gate electrodes of the transistor 107 are connected to the connection wiring 902 and a control line G(i-1) of a ***different*** pixel unit (j, i-1) than that of the connection wiring 902, the transistor 108, etc., of the pixel unit (j, i). Moreover, the gate electrodes of the transistor 107 are not part of the control line G(i-1), but are instead *connected to* the control line G(i-1). *See, e.g.,* EX-1007, ¶[0201] ("gate electrodes [of the TFT 107] are *connected to* the gate signal line" (emphasis added)).

B. European Pub. No. EP1111574A2 ("Inukai 574") EX-1008

37. Inukai 574 is directed to an EL display formed by electroluminescence EL elements. As shown below, FIG. 2 of Inukai 574 illustrates a pixel unit 107 corresponding to an intersection of a data line Sa1 and a control line Ga1:

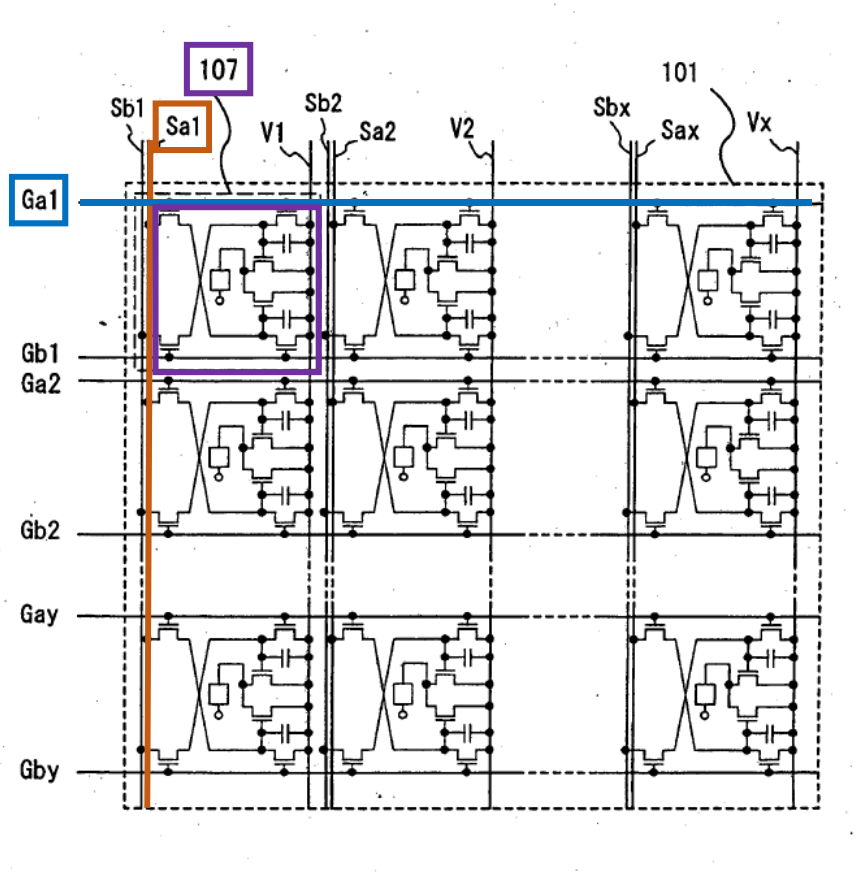


FIG. 2 of Inukai 574

38. FIG. 5 of Inukai 574, reproduced below, illustrates a different embodiment of the pixel unit circuit schematic, in which the pixel unit includes the circuit components (e.g., transistor 3805bm 3806a, etc.) in an area corresponding to the intersection of a data line 3802a and the upper control line 3801b. As shown, the pixel unit includes a transistor 3805b and a transistor 3806a connected to the control line 3801b. In the circuit schematic, the transistor 3805b connected to the

gate of the transistor 3806a crosses a different control line 3801a than the control line 3801b that intersects with the data line 3802a to define the pixel unit circuit area.

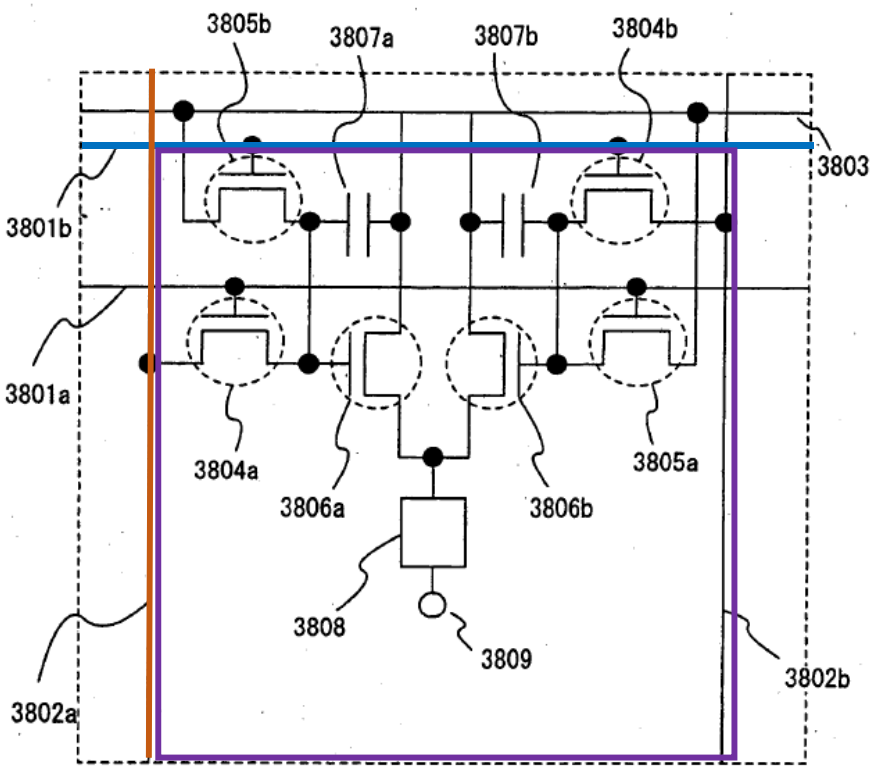


FIG. 5 of Inukai 574

39. Inukai 574 does not provide or otherwise describe a plan view of the physical layout of its circuit components within a pixel unit.

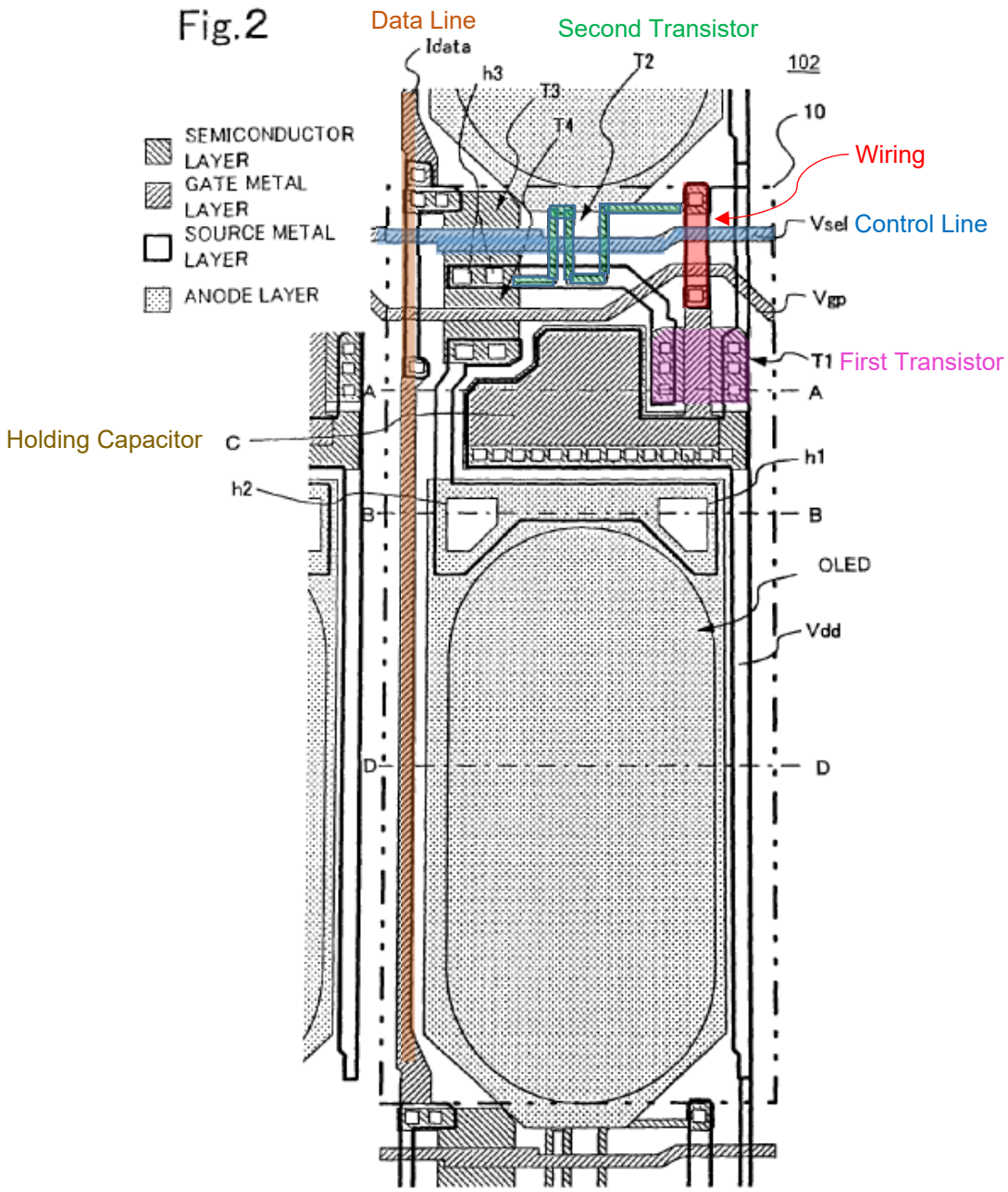
VIII. Ground 1a – Claim 1 Is Not Anticipated By Or Obvious over Inukai 576

40. As discussed below, it is my opinion that Inukai 576 does not disclose each element of claim 1, and it would not have been obvious to modify the configuration of Inukai 576 before the effective filing date of the '760 patent.

41. Inukai 576 does not disclose a portion of a wiring that crosses a control line, let alone that crosses a control line corresponding to its same unit circuit. Instead, Inukai 576 discloses a wiring portion adjacent to a gate electrode (a) that is not a control line, (b) that is not crossed by the wiring portion, and (c) that corresponds to a different unit circuit than that of the wiring portion.

a. Inukai 576 fails to disclose a wiring portion that crosses *a control line*

42. Claim 1 recites "a wiring… having a portion … crossing [a] control line." An example of such a wiring crossing a control line is illustrated in FIG. 2 of the '760 Patent:



Annotated FIG. 2 of the '760 Patent

43. Inukai 576 does not disclose a wiring portion crossing a ***control line***. For an alleged teaching of the control line, the Petitioner points to a gate signal line

G(i-1) and ***protrusions*** off of the gate signal line G(i-1), as shown in the Petitioner's annotation of FIG. 9 of Inukai 576 reproduced below:

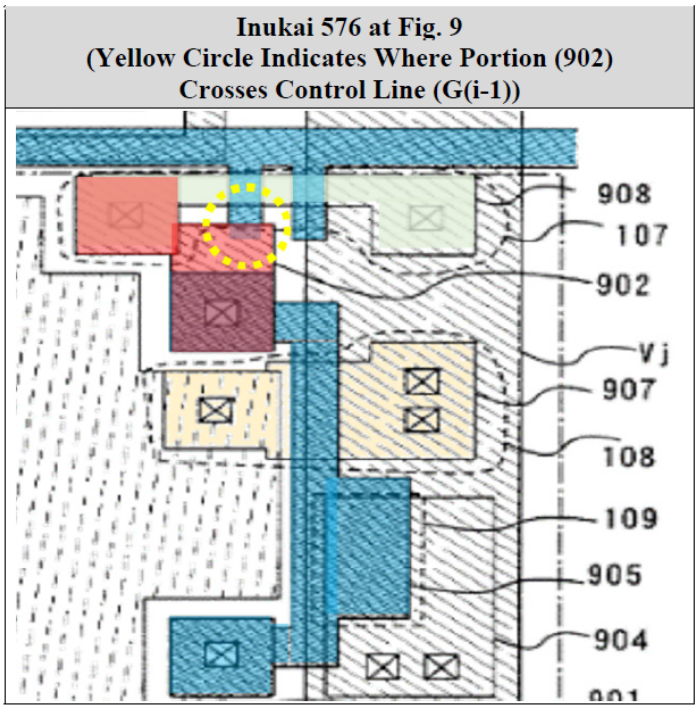
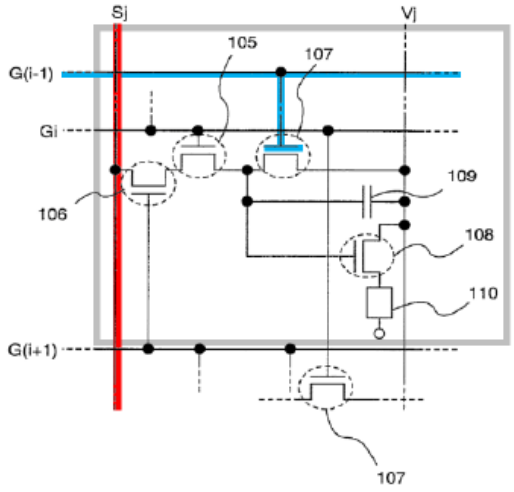
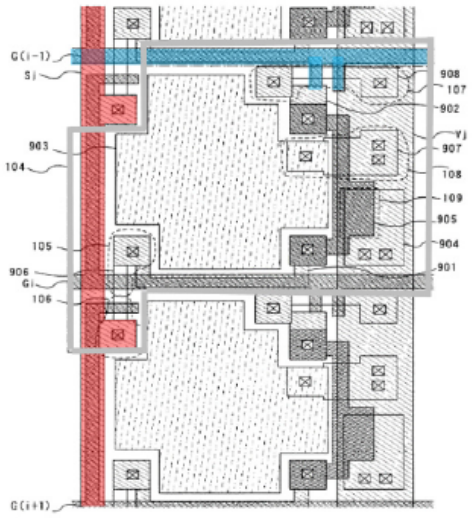


Fig. 9 of Inukai 576 (as annotated by the Petitioner)

44. The Petitioner alleges that the protrusion to the left is crossed by the wiring portion 902. The protrusions, however, are not control lines but are gate electrodes of the transistor 107. The Petitioner and its expert admit that the protrusions are gate electrodes of the transistor 107, Pet., 49, but attempt to argue that these protrusions are both part of the second transistor 107 (as gate electrodes thereof) and the control line, *i.e.*, the gate signal line G(i-1). This is not the case.

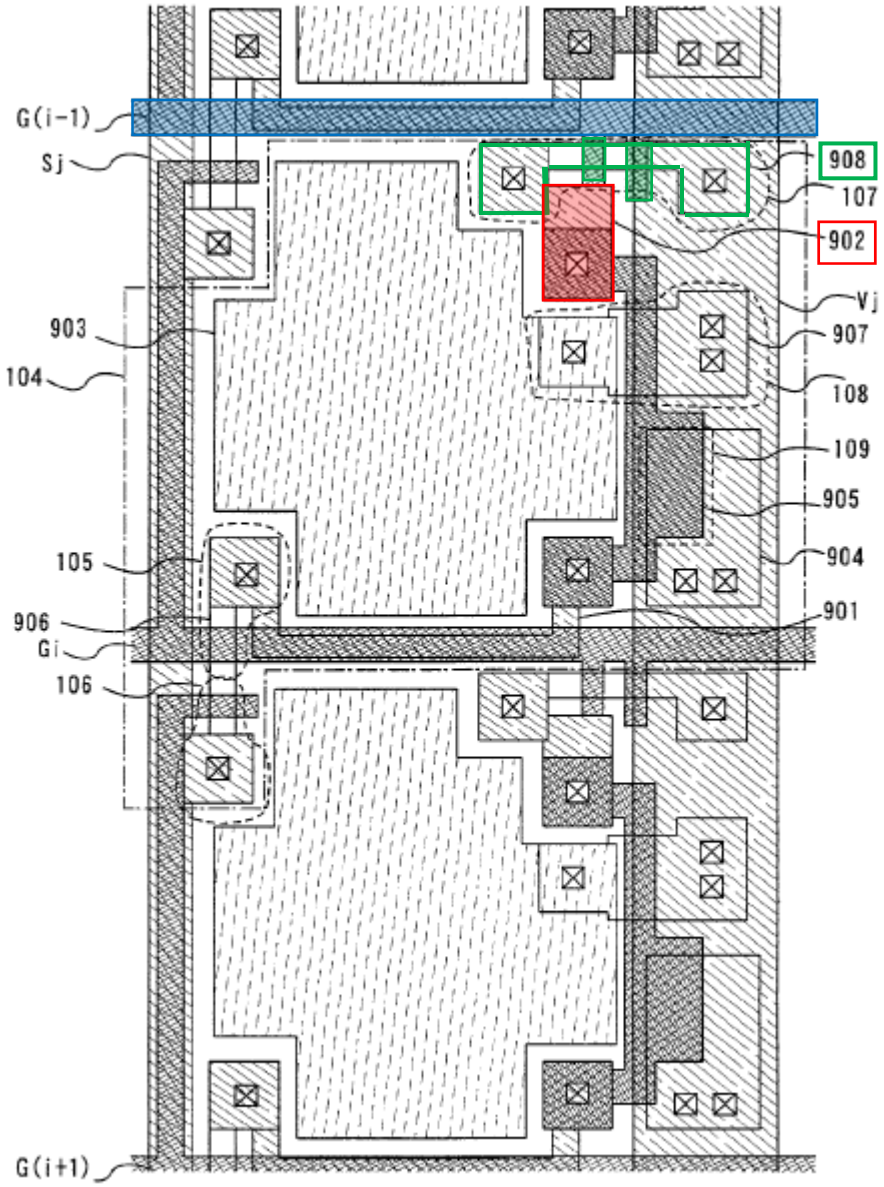
45. A control line, as would be understood by a POSITA, is a line which runs along a direction and carries an electrical signal. The gate electrodes are merely portions of a transistor which "tap off" of the control line in order to receive the control signal. Inukai 576 clearly shows its control lines (gate lines G(i-1), G(i)) in Fig. 9 as running horizontally.

46. In any event, the claim defines the unit circuit as corresponding to an intersection of the data line and the control line. In other words, the control line is the ***line*** that intersects the data line, *i.e.*, the horizontal control line shown in both the '760 Patent and Inukai 576 that intersects the vertical data line:

Inukai 576 at Figure 3	Inukai 576 at Figure 9
 Fig. 3	 Fig. 9

47. As can be seen above, the projections (*i.e.*, gate electrodes) in Inukai 576 are not a portion of the horizontal control ***line*** that intersects the vertical data line. *See* Pet., 29. It is quite clear that they are distinct pads which are connected to the control line.

48. Inukai 576 itself expressly distinguishes the gate electrodes (*i.e.*, projections) from the gate signal line G (control line), and describes the gate electrodes as part of the second transistor 107 and "connected to" —not part of—the gate signal line G. *See, e.g.,* EX-1007, ¶ [0201] ("When the gate signal line G1 is selected, ***the TFT 107… whose gate electrodes are connected to the gate signal line G1*** are turned on."); *see also id.*, ¶¶ [0107] ("…the TFTs 107…, the gate electrodes of which are connected to the gate signal line G1…"), [0160] ("…***the TFT 107… whose gate electrodes are connected to the gate signal line G1*** are turned on").

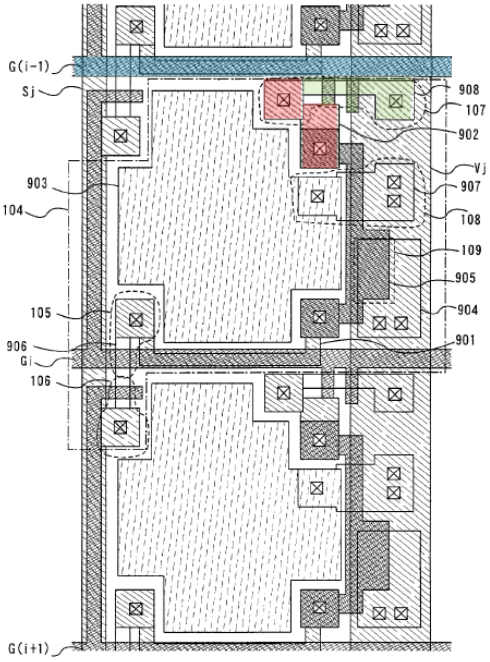
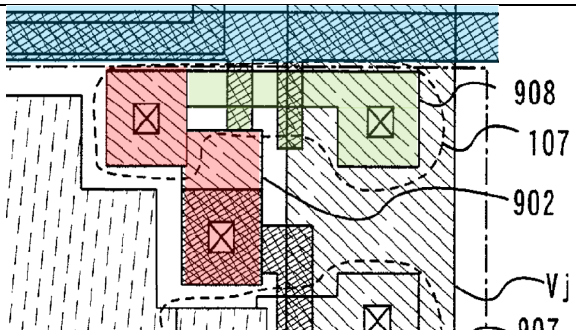


49. Thus, as the protrusions (gate electrodes) are not the control line and are explicitly distinguished from the control line in the reference, the wiring portion 902 in Inukai 576 cannot be said to cross the parallel control line. Inukai 576

therefore fails to disclose "a wiring… having a portion … crossing [a] control line," as required by the claim.

b. Inukai 576 fails to disclose a wiring portion that *crosses* a control line

50. Even if one assumed Inukai 576's gate electrode to be the control line, the electrode is not crossed by a wiring portion, unlike the claimed control line. Instead, Inukai 576 provides a wiring portion 902 that extends near but does not cross the gate electrode of the transistor 107:

Connection Wiring and Gate Electrodes of Transistor 107	**Magnified View of Connection Wiring and Gate Electrode**
 Fig. 9	

51. FIG. 9's plan view explicitly shows the outlines of component parts irrespective of whether that component would otherwise be hidden by another layer "topographically above" (contrary to Petitioner's statement on this point, Pet., 51), for example, the transistor body outline can be seen even though it is below the gate electrode (protrusion), which runs above the transistor body.

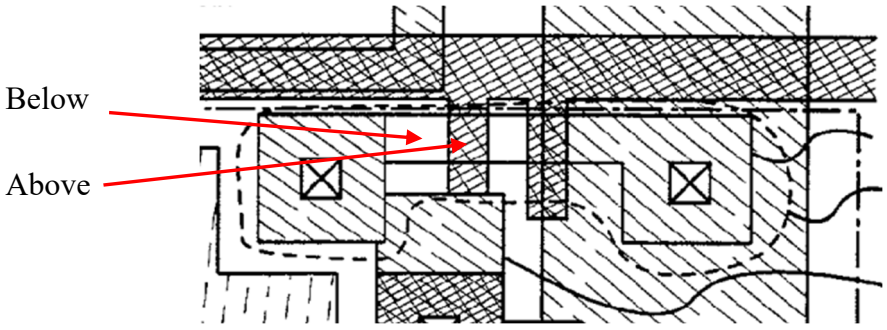


FIG. 9 of Inukai 576

52. It is therefore evident that the Inukai 576 inventor deliberately designed its gate electrode such that it does not overlap with the wiring portion 902, as unambiguously shown in the figure. This is for good reason; even if the gate electrode and the wiring portion 902 of Inukai 576 are considered to be in different layers, and even if there was an insulating layer therebetween, a POSITA would still want to avoid overlapping the two in order to avoid unwanted interference (e.g., crosstalk) between the gate electrode and wiring portion 902.

53. Specifically, when two elements (*e.g.*, a control line and a data line) are placed closed to each other, either in the same layer or different layers, electrical coupling may occur. Put in other words, if a current is applied to a first line, the second line which is close to the first line can pick up some of that energy and induce an unwanted signal in the second line. Although typically, there may be insulation placed between layers of a circuit, a POSITA would still avoid placing two lines on

top of each other, especially in the case where one of the lines is a control line. This is a well-known practice in the art.

54. An example description of this well-known effect can be found in EX-2003 which describes a problem that exists in prior art that interference may occur when overlap occurs between data lines and gate lines in separate layers, even if insulation is placed between the layers:

55. "An insulating layer 120 is deposited on the gate lines 101, and the data lines 102 are formed on the insulating layer 120. Parts of the data lines 102 overlap the gate lines 101… overlapping regions exist as between the data lines 102 and gate lines 101, interference is liable to occur therebetween when the scanning signal is applied to each gate line 101 and the data signals are applied to the data lines 102 individually. This kind of interference is sometimes referred to as 'cross talk'. The interference can cause distortion of the data signals applied to the data lines 102, and adversely impact the quality of images displayed by a display device employing the TFT substrate 100." EX-2003, ¶[0080].

56. As illustrated in FIG. 6 of EX-2003, gate line 101 is separated from data line 102 with insulating layer 120, yet even so, interference can still occur as described in the reference's description of the problem to be solved.

57. Accordingly, although the Petitioner asserts (with reference to the gate electrodes extending over erasing TFT 107 in Inukai 576 and wiring 902) that these "two regions will be electrically isolated from each other due to intervening insulating layers and a signal carried by one region will not interfere with a signal carried by the other," Pet., 56, this is not the case A POSITA would accordingly have no motivation to modify Inukai 576 such that the left protrusion is the same length as the protrusion on the right.

58. Thus, a POSITA who viewed the plan view of Inukai 576 would certainly understand that the left gate electrode being shorter is intentional to avoid unwanted interference between the left gate electrode with wiring portion 902.

59. Nevertheless, the Petitioner argues that "a POSITA would have understood or found obvious that the protrusion would have been the same length as the protrusion on the right, due to the 'endcap rule.'" Pet., 51. According to the Petitioner, the "endcap rule" refers to "a universal rule in semiconductor design that requires gates to have a certain minimum length." Pet., 52. The Petitioner and its expert provide no support for its allegation that the "endcap rule" is universally applied.

60. The "endcap rule" is, at best, a design generalization which may be used in some applications for semiconductor manufacturing, heavily dependent on what

materials are used, what the purpose of the semiconductor and especially the manufacturing process. For example, you may not even extend the length of the transistor gate, you may end up increasing the width instead depending on the process. It is thus not clear on what basis or motivation a POSITA would apply an "endcap rule" to Inukai 576.

61. Secondly, if we apply the Petitioner's definition that the "endcap rule" refers to "gates to have a certain minimum length", it is not clear whatsoever what this "minimum length" would be in the context of Inukai 576, but it can be assumed that the inventor considered such design generalizations when providing FIG. 9 of Inukai 576, and that the gate length of the left gate electrode of TFT 107 was intentionally shortened yet still extends past the active region of TFT 107 such that it fulfills the "endcap rule".

62. In any case, even considering this design generalization, an "endcap rule" does not necessitate that the sizes of two gate electrodes in a multigate thin film transistor, as is the case of Inukai 576, should be the same. It at best only dictates the ***minimum*** length of the gate electrodes.

63. The Petitioner cites to Borodovsky (Ex-1010), which describes the general concept that an endcap of a transistor gate may extend some minimum distance beyond an active region so as to ensure that any rounding of the endcap

does not occur over the active region. EX-1010, 4:21-33. Absent from the reference is any suggestion how the rule would have been applied to Inukai 576 in view of its particular manufacturing process and materials (refer to the above).

64. Nor does Borodovsky provide any basis to conclude that the "endcap rule" would provide gate electrodes of the ***same*** size or length. All that Borodovsky's design rule necessitates is that the endcap extends at least a minimum length—not an exact length—beyond the active region, and "other size up amounts may be used." Ex-1010, 9:42-46. The Petition itself recognizes that the endcap rule does not require equal length electrodes, but only that the length of each electrode exceeds "a minimum length." Pet., 52. There is no universal rule or reason to require gate electrodes to be of the same length, as evidenced by Inukai 576 itself in which the gate electrodes have different lengths.

65. In particular, it is well-known in the art that the gate electrodes may be different sizes or lengths, as exemplified in EX-2004 which illustrates a TFT having two gate electrodes, with one being larger than the other. "[U]pper gate electrode 30 overlies lower gate electrode 10, with one edge of electrode 30 directly over one edge of the lower electrode 10, and the opposite edge overlapping the edge of lower electrode 10 by a significant amount. This overlap 27 is in the range of 0.2 to 0.6 micrometers" (EX-2004, 5:4-9). In other words, the size of upper gate electrode 30

is intentionally larger than lower electrode 10. This can clearly be seen in FIG. 11 of EX-2004 (reproduced below)

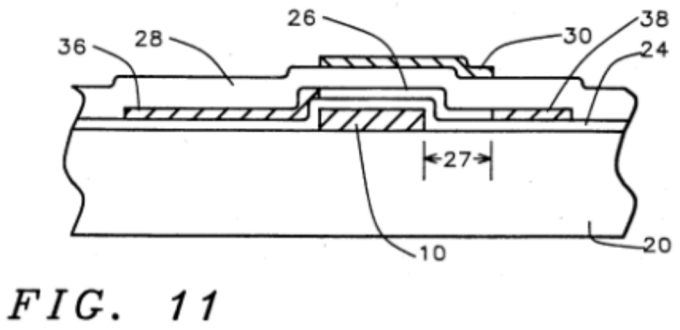


FIG. 11

FIG. 11 of EX-2004 (reproduced)

66. Even assuming for the sake of argument that the "endcap rule" is a universal rule, then a POSITA in EX-2004 would have complied with it while still making the size or lengths of the gate electrodes different.

67. Furthermore, while the Petitioner alleges that the "endcap rule" is ***universally*** applied, it provides no basis to believe that Inukai 576 has not complied with it. In other words, accepting the Petitioner's allegation on the universality of the "endcap rule," it should be understood that the gate electrodes in Inukai 576 were designed in compliance with this "universal rule in semiconductor design." The Petitioner has provided no reason to believe otherwise. As I discussed above, and referring to FIG. 9 of Inukai 576, the left protrusion of the TFT 107 for erasing

extends beyond the active layer 908 that is a semiconductor layer, such that the structural configuration of the protrusions in Inukai 576 has presumably already complied with the endcap rule. Therefore, the Petition provides no reason to modify the length of the left protrusion of the TFT 107 for erasing to be equal to a length of the right protrusion.

68. And even if it would have been obvious to modify the lengths of the parallel gate electrodes to be the same, that does not require extending the length of the left gate electrode. Rather, the right gate electrode could be reduced in length.

69. To summarize, Inukai 576 plainly and deliberately discloses a wiring portion that does ***not*** cross a gate electrode (let alone a control line). Further, the Petition does not provide any reason to modify the length of the gate electrode such that it is crossed by the wiring portion, as explained in further detail below with reference to Ground 1b. Instead, the Petitioner cites to a rule without addressing the fact that Inukai 576 must already comply with it. Inukai 576, therefore, does not disclose or render obvious a wiring portion crossing a control line.

c. Inukai 576 fails to disclose a unit circuit corresponding to a control line and comprising a wiring portion crossing that control line

70. Inukai 576 does not disclose a unit circuit including each of the constituent elements as arranged in the claim. Specifically, Inukai 576 fails to

disclose a wiring portion, of a unit circuit, that crosses a control line corresponding to that unit circuit. Instead, the Petition points to components across multiple different unit circuits in Inukai 576, and cites to a wiring portion alleged to cross a control line (but is actually a transistor gate) corresponding to a different unit circuit.

71. Claim 1 recites "a unit circuit arranged corresponding to an intersection of the data line and the control line." Thus, in the claim, one unit circuit includes a first transistor, a second transistor, an electro-optical element, a holding element, and wiring. In other words, each unit circuit "***corresponding to an intersection*** of the data line and the control line" constitutes a pixel as understood in the art. EX-1001, 1:27-29 ("Each of the plurality of pixel circuits is arranged to correspond to the intersection of a data line and a scan line.")

72. As an example of a pixel circuit which is arranged to correspond to the intersection of a data line and a scan line, EX-2005 describes an active matrix display that describes "The pixel portion is placed in the vicinity of the point of intersection of a gate wiring line and a data wiring line. The pixel portion is provided with switching TFT 454, current control TFT 455, and EL element 456." *See* EX-2005, 16:61-65. As can be seen below in FIG. 9A and 9B of EX-2005 (reproduced below), the pixel portion (which contains switching TFT 454, current control TFT 455, EL element 456) is clearly arranged about the intersection of gate line 410 (highlighted

in blue) and data line 414 (highlighted in yellow), which can be understood to define the outer perimeter of the pixel portion (highlighted in red).

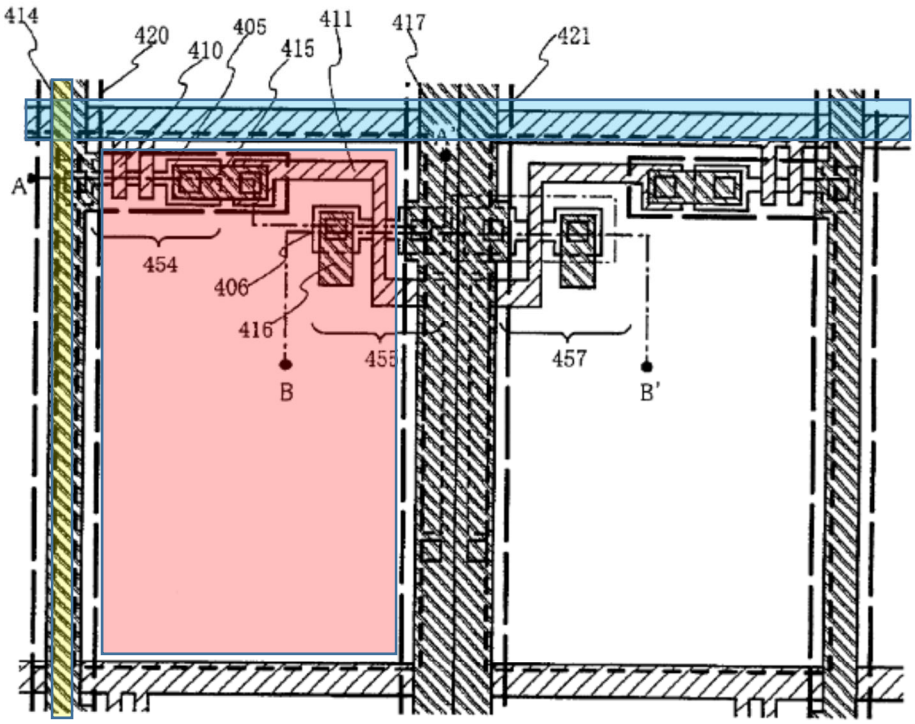


Fig. 9A

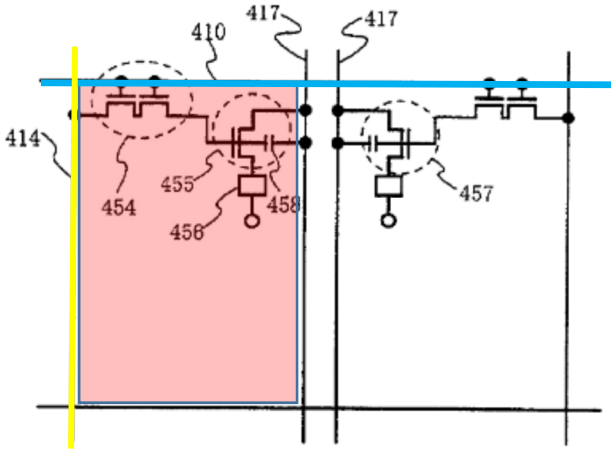
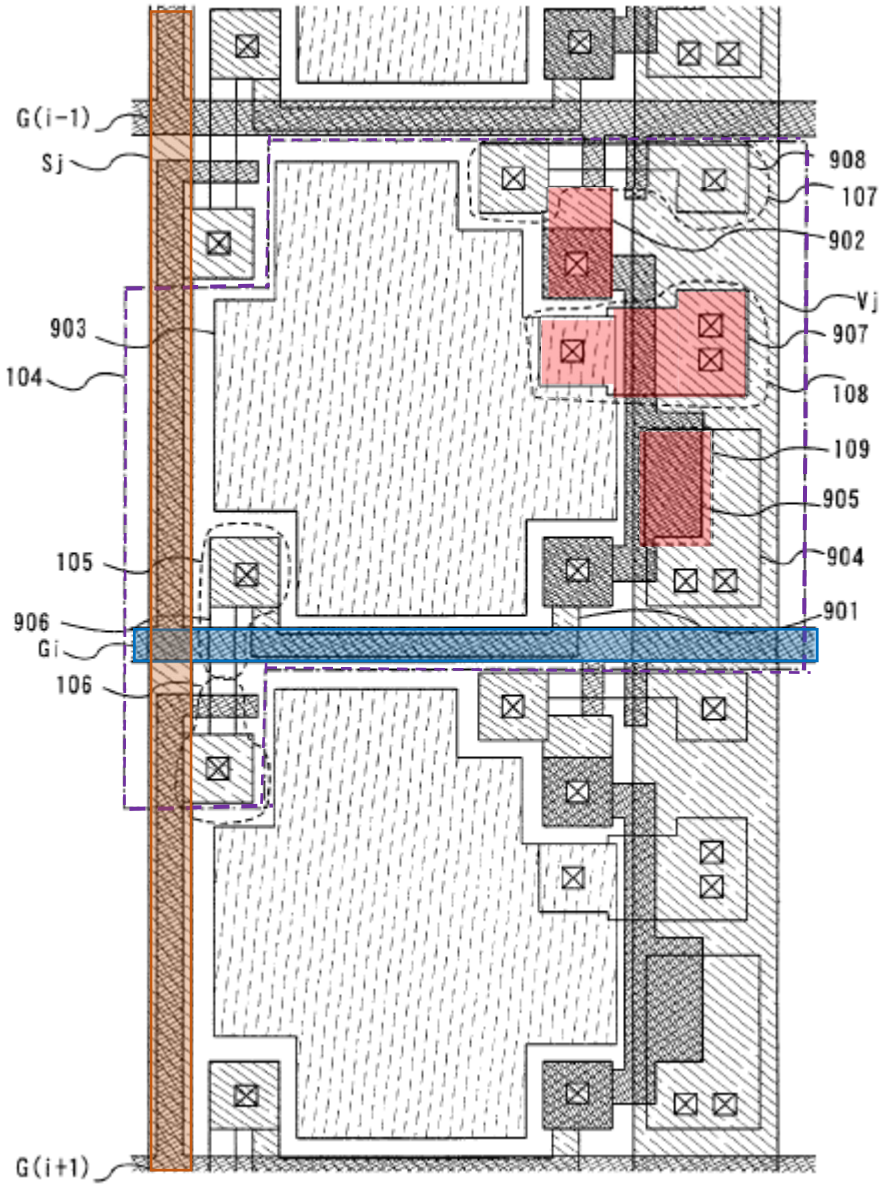


Fig. 9B

73. As recognized by the Petition, Inukai 576 also discloses a unit circuit ***corresponding to the intersection*** of a particular data line and scan (or control) line (*i.e.*, pixel unit). Per the Petition, each pixel 104 is "designated by a particular gate signal line and a particular source signal line." Pet., 28 (citing Ex-1007, ¶¶ [0075], [0077]). Inukai 576 defines its pixel 104 (highlighted in orange below) corresponding to the intersection of the particular data line Si and the particular control line Gi (highlighted in blue below), and the constituent components of that unit circuit (highlighted in red below):



74. Consistent with Inukai 576's unit circuit, the Petition cites to TFT 108 for the first transistor, capacitor 109 for the holding circuit, and wiring 904 for the claimed wiring portion, each of which corresponds to the intersection of the particular data line Si and the particular control line Gi. Nevertheless, for an alleged

teaching of the wiring portion crossing the control line, the Petition cites to a different control line G(i-1) that corresponds to and defines a different unit than the unit circuit of the wiring portion, the first transistor, etc.

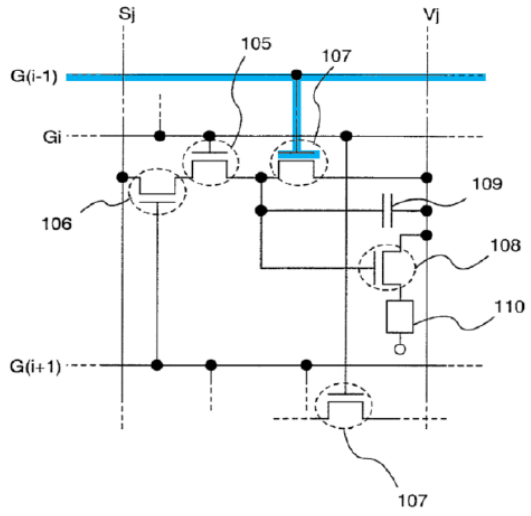
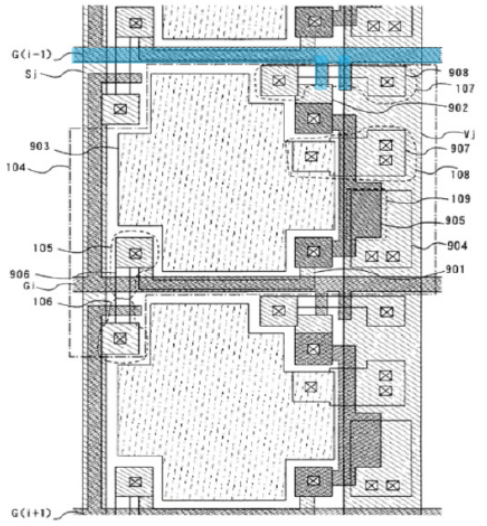
Inukai 576 at Fig. 3 (Schematic, Control Line G(i-1) high-lighted)	**Inukai 576 at Fig. 9 (Plan View, Control Line G(i-1) highlighted)**
 Fig. 3	 Fig. 9

FIG. 3 and FIG. 9 of Inukai 576 as annotated in Petition (Page 27)

75. The control line G(i-1) intersects with the data line to define a different corresponding unit circuit (or pixel), as shown in FIG. 2 of Inukai 576 (showing different pixel unit circuits respectively corresponding to different intersections of scan lines and control lines). To be clear, the wiring portion, the first transistor, the holding circuit, etc., cited by the Petition are unquestionably of the pixel unit circuit

corresponding to the intersection of Gi and Sj, *NOT* the distinct pixel unit circuit corresponding to the intersection of G(i-1) and Sj.

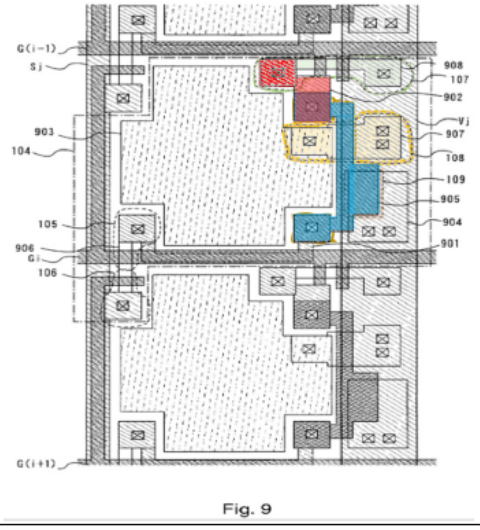
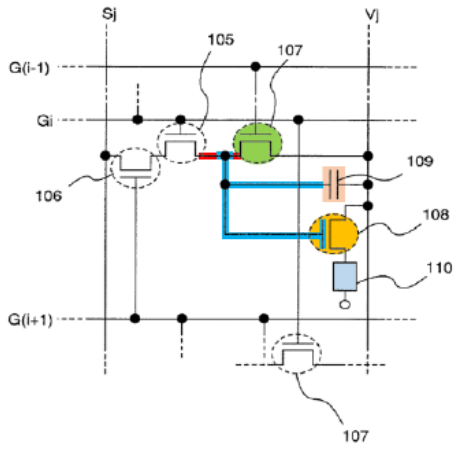
Inukai 576 at Fig. 9 (Plan View)	Inukai 576 at Fig. 3 (Schematic)
 Fig. 9	 Fig. 3

FIG. 9 and FIG. 3 of Inukai 576 as annotated in Petition (Page 42)

76. Thus, even assuming for the sake of argument that the gate electrode is part of the control line G(i-1) and that it would have been obvious to extend the length of this gate electrode under the wiring portion 902, as alleged by the Petitioner, the wiring portion 902 would not cross the control line Gi corresponding to its pixel unit circuit. Instead, under the Petitioner's theory, the wiring portion would at best cross the control line G(i-1) corresponding to a different pixel unit circuit. For at least this reason, Grounds 1a and 1b do not show a wiring portion crossing a control line corresponding to the same unit circuit.

IX. Ground 1b – Claim 1 Is Not Obvious Over Inukai 576 in view of Yamazaki

77. As discussed below, a POSITA would not have found it obvious to modify the configuration of Inukai 576 in view of Yamazaki before the effective filing date of the '760 patent.

78. In particular, there is no motivation or reason to modify Inukai 576 with respect to the left gate electrode. The Petitioner argues that there would be motivation to combine Yamazaki with Inukai 576 to extend the length of the left gate electrode in Inukai 576 so as to be equal in length to the right gate electrode. According to the Petitioner, "[a] POSITA, upon ascertaining a given endcap length, would have been motivated to ensure that all gates (and especially gates that are part of the same multi-gate transistor) to be designed to have endcaps of equal lengths to ensure that the gates are long enough to exert control." Pet., 54; see also id., 55. This rationale fails for a number of reasons.

79. Firstly, the gate electrodes in Inukai 576 appear to already comply with the endcap rule, so it is not clear why a POSITA would have been motivated to modify the electrode. The premise of the Petitoin's motivation (that Inukai 576 does not comply with the endcap rule) is unproven in the Petition, but simply assumed without any basis or support. In fact, the record provided by Petition instead

supports the conclusion that the left gate electrode in Inukai 576 already complies with the endcap rule, as the Petitioner and its expert argue that this rule is universally applied. Pet., 52 ("The 'endcap rule' refers to **a universal rule** in semiconductor design that **requires** gates to have a certain minimum length."). Notably, the left gate electrode in Inukai 576 extends beyond the active region of the transistor, and therefore complies with the endcap rule. Ex-1007, FIG. 9. The Petitioner does not argue or allege otherwise. The Petitioner has not established a motivation to extend the length of Inukai 576's left gate electrode.

80. It should be emphasized that the design generalization of the "endcap rule" as defined by the Petitioner does not require or motivate design of gate electrodes to have ***equal*** length. Rather, the endcap rule only requires gates to have "a certain **minimum** length." Pet., 52. Two gates can satisfy the endcap rule yet have unequal lengths, as is the case with Inukai 576. Nothing about the endcap rule requires or otherwise motivates two gates to be of equal length, let alone motivate modifications to an already-compliant gate.

81. Although the Petition considers that Inukai 576 can be combined with Yamazaki on the basis that "[t]he gate electrodes… are formed in… a different layer from the connection wiring layer 902" and "[a]s a result, those two regions will be electrically isolated from each other due to intervening insulating layers and a signal

carried by one region will not interfere with a signal carried by the other." Pet., 56 (citing EX-1007, ¶[0267]). The Petition does not establish that the insulating layer, would completely prevent signal interference between the gate electrode and the wiring portion 902 due to overlap.

82. To the contrary, as discussed previously, a POSITA would recognize that even if a gate electrode and the wiring portion were separated with an insulating layer, interference would still occur, as described with reference to FIG. 6 of EX-2003 (in EX-2003, even if gate line 101 is separated from data line 102 with insulating layer 120, interference can still occur). Accordingly, there would be no motivation for a POSITA to modify Inukai 576 such that the left gate electrode ("protrusion") extends further than what is already clearly shown in FIG. 9 of Inukai 576.

83. Even if a POSITA would have found it obvious to extend the length of the left gate electrode in Inukai 576, such a modification would not have cured the above-noted deficiencies of Inukai 576. For example, Ground 1b's modification would not cure the fact that the gate electrodes in Inukai 576 are part of the alleged second electrode and explicitly distinguished from the control line. *See* above section VIII.a. Furthermore, Ground 1b does not cure Inukai's failure to disclose a wiring portion crossing a control line corresponding to the same unit circuit. *See*

above section VIII.c. As such, even with the modification, the wiring portion would not cross a control line as required by the claim.

X. Ground 2a – Claim 1 Is Not Anticipated By Or Obvious Over Inukai 574

84. As discussed below, a POSITA would not have anticipated claim 1 of the '760 in view of Inukai 574, or found it obvious to modify the configuration of Inukai 574 before the effective filing date of the '760 patent.

85. Inukai 574 does not disclose a physical layout of a circuit in which a portion of a wiring crosses a control line, as required by claim 1. Instead, Inukai 574 discloses only circuit schematics without any description of a plan view of the corresponding physical layout. Where Inukai 574 does provide a description of a physical layout, it is clear that the wiring portion *CANNOT* cross the control line as they are formed on the same layer. The Petition does not address this significant issue.

a. Inukai 574 fails to disclose a wiring portion that crosses a control line

86. Inukai 574 does not include any description or a plan view of a physical layout of a unit circuit that includes a wiring portion crossing a control line. FIG. 5 of Inukai 574 illustrates a schematic circuit diagram—*NOT* an actual physical layout

showing the actual structural arrangement—including a control line 3801a, a control line 3801b, and a data line 3802a. The Petition cites to a control line 3801a as the "control line," a data line 3802a as the "data line," a transistor 3806a as the "first transistor," and a transistor TFT 3805b as the "second transistor." *See* Pet., 63-80. The Petitioner further cites to a wiring portion annotated in red as the "wiring."

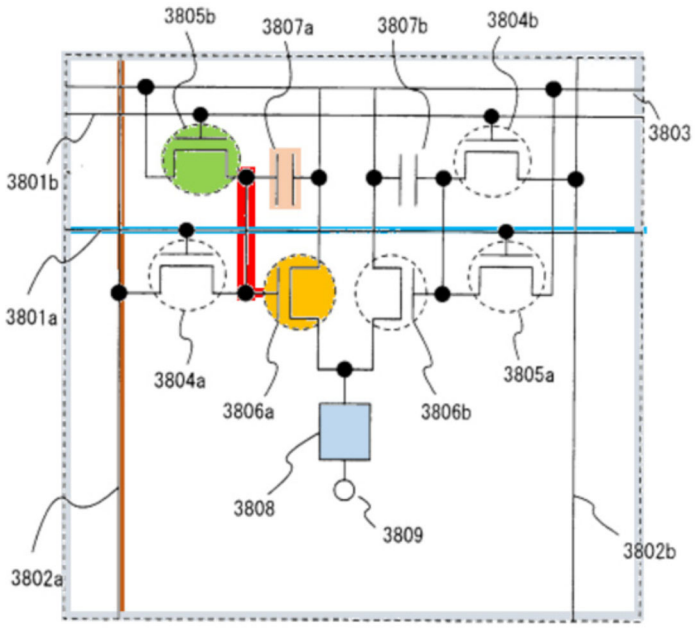


FIG. 5

Annotated FIG. 5 of Inukai 574 at page 80 of Petition

87. According to the Petitioner, the circuit schematic shows the wiring portion crossing control line 3801a. But this does not amount to a teaching of the wiring portion crossing the control line 3801a in the actual implementation of the

circuit. As conceded by the Petitioner, Inukai 574 does not include any plan view or description of a wiring, connecting the erasing TFT 3805b to a gate of the EL driving TFT 3806a, that includes a portion crossing the gate wiring 3801a. Pet., 81-82. Instead, the Petitioner alleges that the circuit schematic establishes a possible physical layout. Pet., 79. According to the Petitioner, this possible physical layout would have been an obvious modification to Inukai 574, because "[i]mplementing a circuit schematic using a circuit layout that generally reflects the same sort of geometry depicted by the schematic would have been a matter of common engineering practice, and typically the most straightforward way to implement the schematic." Pet., 80. The Petitioner is incorrect.

88. First, the Petitioner's allegation that a circuit schematic illustrates not just a possible physical layout, but the most straightforward implementation, is a baseless generalization. In fact, it is well known in the art that a schematic circuit diagram does not necessitate or otherwise suggest a physical layout of the actual circuit to have its same geometry, and that other considerations such as circuit board size, heat dissipation, signal coupling between components, physical ruggedness, and space limitations would need to be considered in optimally designing the physical layout of the actual circuit. None of these factors are addressed or

considered in the Petition's unsupported and incorrect oversimplification of circuit design.

89. For example, if an electrical circuit was implemented using only a single layered circuit board, and the circuit schematic layout illustrated certain components crossing each other with wiring, a POSITA would not simply follow the geometry of the circuit schematic and actually cross over the wiring in the physical layout because it would cause a short circuit. Moreover, it is not possible to have components cross over each other when they are on the same layer.

90. It is common knowledge in the art that an actual circuit conforming to "the same sort of geometry" of a schematic circuit diagram is not a matter of common engineering practice, but nearly impossible. In fact, the record provided by the Petitioner establishes that the physical layout of a circuit does not mirror the geometry of its corresponding circuit diagram. FIGS. 3 and 9 of Inukai 576 (EX-1006) illustrate a schematic circuit diagram and a corresponding plan view of the actual circuit, where the physical layout of the actual circuit does not correspond to or have "the same sort of geometry" as the circuit diagram, but is substantially different. This is indisputable from a side-by-side comparison of the two:

Circuit Schematic (Inukai 576) **Physical Layout (Inukai 576)**

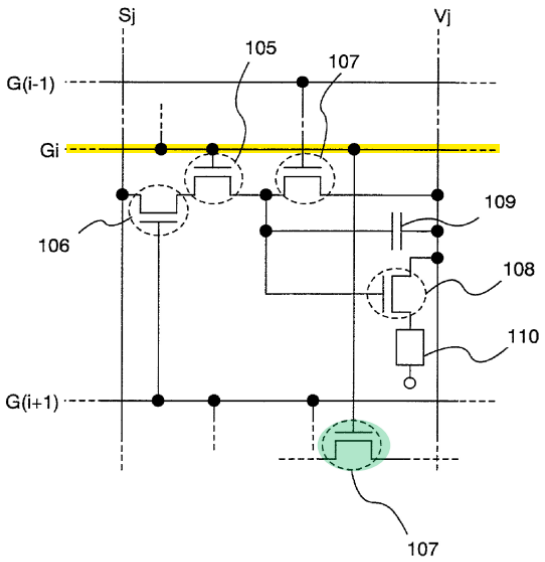


Fig. 3

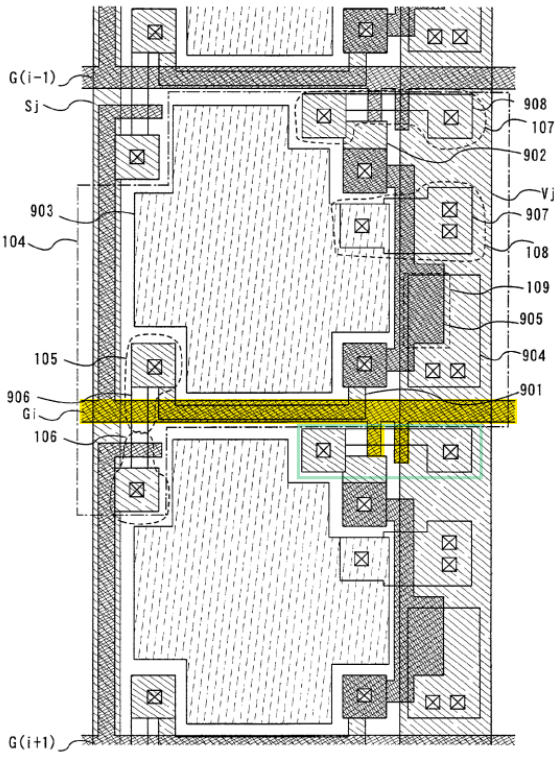


Fig. 9

91. For example, in the schematic circuit diagram in FIG. 3 of Inukai 576, the gate of the lower TFT 107 for erasing (highlighted in green below Gi) is connected to the signal line Gi in yellow. The wiring between the signal line Gi (highlighted in yellow) and the gate of the lower TFT 107 (highlighted in green) passes over multiple components such as, for example, the gate of TFT 108 for

driving EL, an electrode of capacitor 109, and the source/drain of the upper TFT 107 for erasing.

92. However, in the actual physical layout of the circuit as illustrated in the annotated FIG. 9 of Inukai 576, the wiring connecting the signal line Gi (highlighted in yellow below) and the gate of the lower TFT 107 for erasing (highlighted in green below) does not pass over the above-mentioned wirings such as, for example, the gate of TFT 108 for driving EL, one electrode of capacitor 109, the source/drain of the upper TFT 107 for erasing.

93. Additionally, in the circuit schematic, the majority of the pixel unit's circuit components (*e.g.*, 105, 108, 110) are below the corresponding signal line Gi, whereas in the actual layout they are provided above the corresponding signal line Gi. The Petitioner's allegation that the geometry of a physical layout can be understood from the circuit schematic is an incredulous over-simplification. Instead, the record shows that a schematic circuit diagram would generally not conform to the actual layout of the circuit.

94. I also note that a physical layout in which the alleged wiring portion of Inukai 574 crosses the gate signal line 3801a is not possible from the physical layout disclosed by Inukai 574 and relied on by the Petitioner. The Petition cites to FIG. 16 of Inukai 574 for an actual implementation in which, according to the Petitioner,

the alleged wiring portion 36 is formed in a layer different from the first transistor's gate layer (claim 1: "wiring having ***a portion formed in the layer different from a gate layer in which the gate of the first transistor is formed***, the portion crossing the control line"). Pet., 78. According to the Petitioner, the wiring 36 highlighted in red in its annotation of FIG. 16 corresponds to the claimed wiring portion, and connects the switching TFT 3502, the alleged second transistor 3504, and the gate of the alleged second transistor 3503:

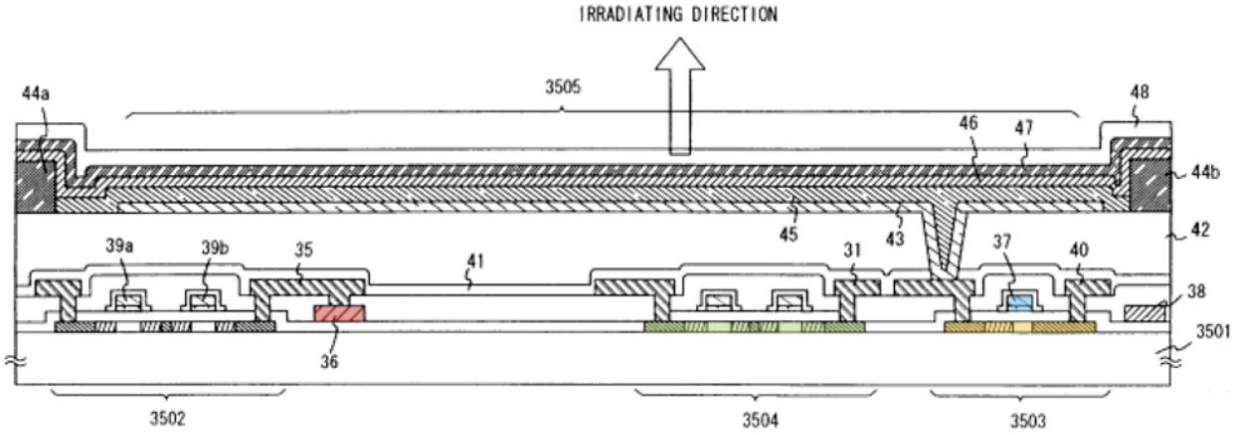


FIG. 16

FIG. 16 of Inukai 574 (annotated in Petition., 80)

95. What the Petition does not but should annotate is the gate signal line 38 "which connects the gate electrodes 38a, 38b of the switching TFT 3502." EX-1008, ¶[0290]. This gate signal line 38 corresponds to the lower gate signal line 3801a connecting to the gates of the switching TFT 3804a in FIG. 5, which like in FIG. 16

is connected to the alleged second transistor 3805b and the gate of the alleged first transistor 3806a via the alleged wiring portion:

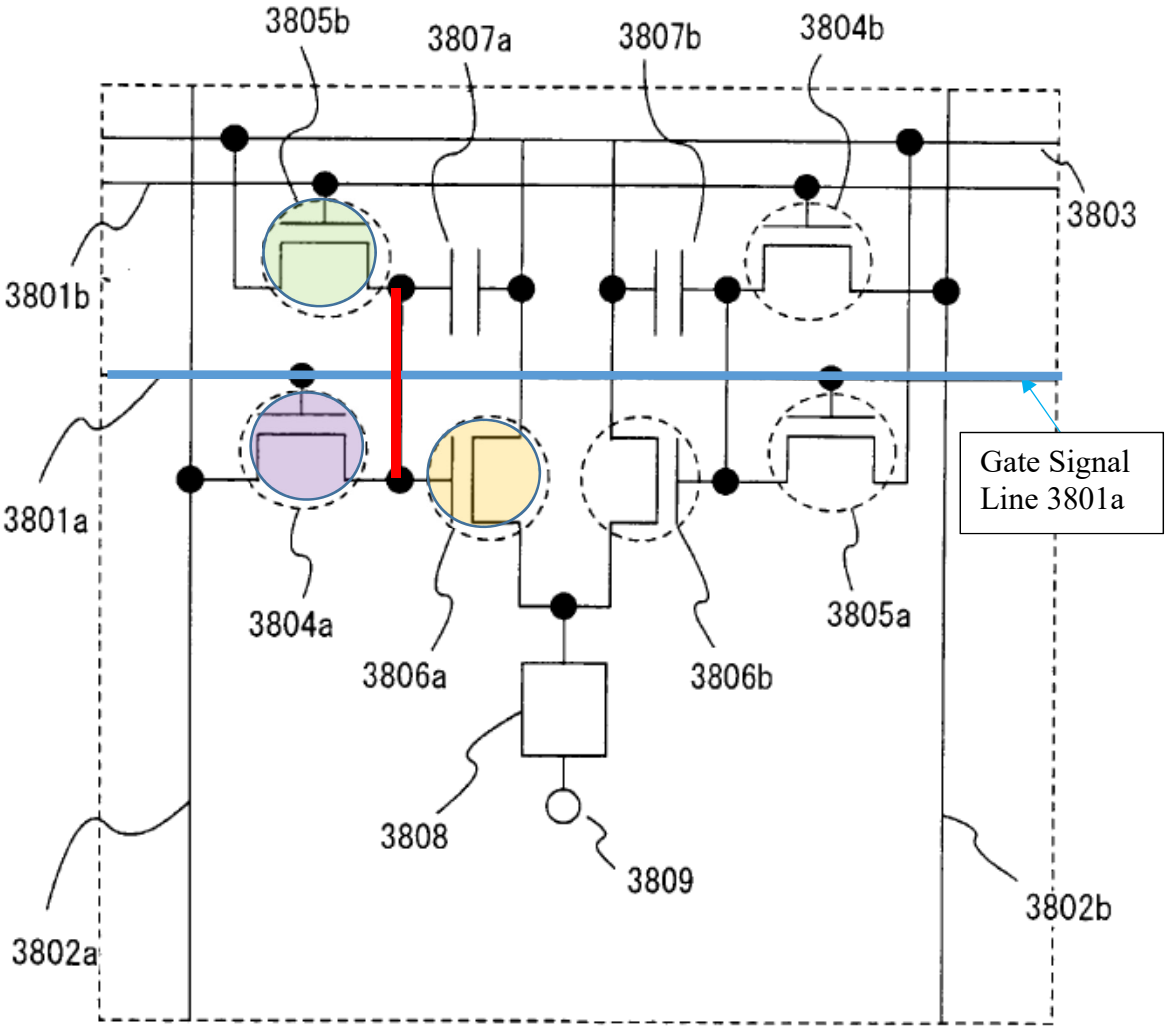


FIG. 5

FIG. 5 of Inukai 574 (annotated)

96. The Petitioner relies on the particular layer arrangement of the wiring portion 36 relative to other portions of the layout shown in FIG. 16 to allege invalidity of claim 1, but fails to note that this arrangement places the wiring portion on the exact same layer as the gate signal line 3801a:

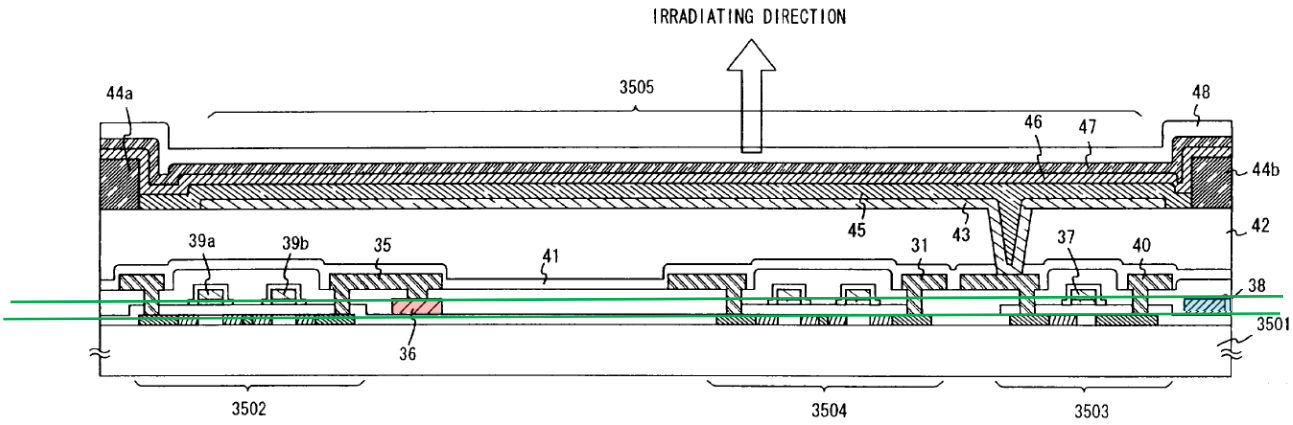
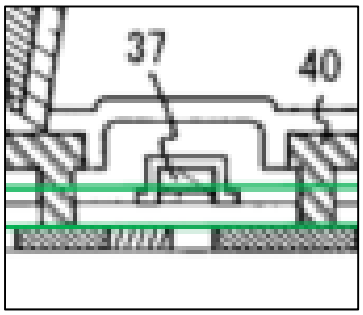


FIG. 16

FIG. 16 of Inukai 574 (annotated)

97. Thus, the physical layout disclosed in Inukai 574 and relied on by the Petitioner prevents the alleged wiring portion 36 from crossing the gate signal line 38. This disclosure of Inukai 574 flatly contradicts the Petitoin's allegations of anticipation and obviousness.

98. Additionally, the Petitioner cites to FIG. 16 of Inukai to allege that the wiring portion 36 and the alleged gate layer 37 are formed on different layers, as required by claim 1. (Pet., 77). FIG. 16 (magnified below), however, shows the two components as overlapping in height and therefore not on different layers:



Magnified Annotation of FIG. 16

99. Therefore, it is my opinion that Inukai 574 does not disclose or make obvious its alleged wiring portion both crossing the control line Gi and formed on a different layer than a gate layer of the first transistor.

100. Ground 2a, as a result, does not establish that Inukai 574 discloses or renders obvious a wiring portion that crosses a control line as claimed.

b. Inukai 574 fails to disclose a unit circuit corresponding to a an intersection of a data line and a control line and comprising a wiring portion crossing that control line

101. Even assuming for the sake of argument that the circuit schematic in FIG. 5 of Inukai reflects the physical layout of the circuit, Inukai 574 does not disclose a unit circuit including each of the constituent elements as arranged in the claim. Specifically, Inukai 574 fails to disclose a wiring portion, of a unit circuit, that crosses a control line corresponding to that unit circuit.

102. Claim 1 recites a data line, a control line, and a unit circuit corresponding to an intersection of the two lines. A POSITA would have understood that the claim is defining its pixel unit circuit as corresponding to a particular intersection of a control line and a data line, which is a conventional pixel matrix arrangement well known in the art, including that of record in this proceeding. (*See* EX-2005, 16:61-65 and FIG. 9A and 9B and description in ¶71. above)

103. In Inukai 574, for example, pixels are arranged in a matrix defined by particular intersections of control lines and data lines. EX-1008, ¶[0100], FIG. 2. As recognized by the Petition, Inukai 574's unit circuit ***corresponds to the intersection*** of a particular data line and scan (or control) line (*i.e.*, pixel unit). That is, Inukai 574 defines its pixel 107 (highlighted in orange below) corresponding to the intersection of the particular data line Sa1 (highlighted in green below) and the

particular control line Ga1 (highlighted in blue below), *i.e.*, the intersections that define and thereby correspond to the matrix element in the active matrix arrangement that constitutes a unit pixel. In FIG. 5 of Inukai 574, the Petition cites to a transistor 3806a as the "first transistor" and an EL element 3808 as the "electro-optical element," an transistor 3805b as the "second transistor," and a capacitor 3807a as the "holding element." *See* Pet., 63-74.

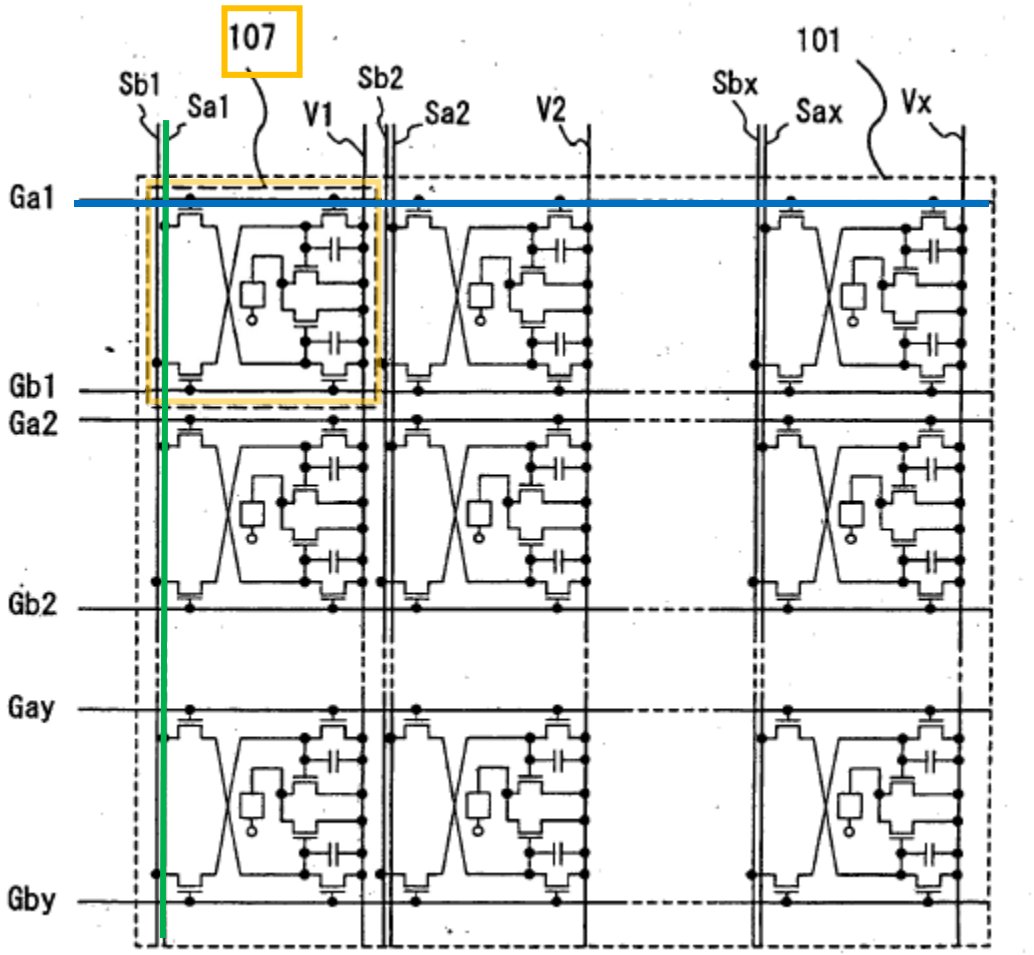


FIG. 2 of Inukai 574

104. The cited unit pixel circuit shown in FIG. 5 of Inukai 574 corresponds to the particular intersection of its outer control line 3801b and the data line 3802a, *i.e.*, the lines defining the matrix element that is the pixel unit, not the interior line 3801a that crosses through the middle of the unit circuit within the circuit schematic and is unrelated to the matrix arrangement of pixel units. Thus, the control line

3801a cited by the Petition does not correspond to the claimed control line; at best, it is the outer control line 3801b that defines the pixel unit circuit area and the matrix arrangement of pixels. The outer control line 3801b, though, is not crossed by the alleged wiring portion in the circuit schematic. Thus, even assuming for the sake of argument that a physical layout of the circuit would conform to the circuit schematic in FIG. 5, Inukai 574 does not render obvious the claimed wiring portion that crosses the control line corresponding to the pixel unit circuit area.

XI. Ground 2b – Claim 1 Is Not Obvious Over Inukai 574 in view of Yamazaki

105. As discussed below, a POSITA would not have found it obvious to modify the configuration of Inukai 574 in view of Yamazaki before the effective filing date of the '760 patent.

a. Yamazaki does not cure the deficiencies of Inukai 574

106. Yamazaki does not cure the above-described deficiencies of Inukai 574's physical layout, in which the alleged wiring portion and the control line are on a same layer and therefore cannot cross.

107. As an initial point, the Petition's brief obviousness analysis makes no attempt to address or acknowledge the inability of Inukai 574's wiring portion to cross a control line on its same layer. The Petition does not explain how or why the

combined teachings of Yamazaki and Inukai 574 would have overcome this impediment in the primary reference.

108. In fact, Yamazaki's electrode 806 (alleged wiring portion) is able to cross the control line 802 because they are formed on different layers, a construction that does not exist in Inukai 574. The Petitioner does not allege that it would have been obvious to modify Inukai 574's arrangement of components and formation of layers or otherwise provide any basis to support such a conclusion. The Petitioner also does not address how such a modification would impact other requirements of the claim, such as the requirement that the wiring portion that crosses the control line be ***formed on a different layer*** than the gate of the first transistor. Contrary to claim 1, the crossing "wiring" (alleged) portion in Yamazaki is itself a component of the second transistor (annotated in green below) and is ***formed on the same layer*** as the gate of the first transistor (annotated in orange below).

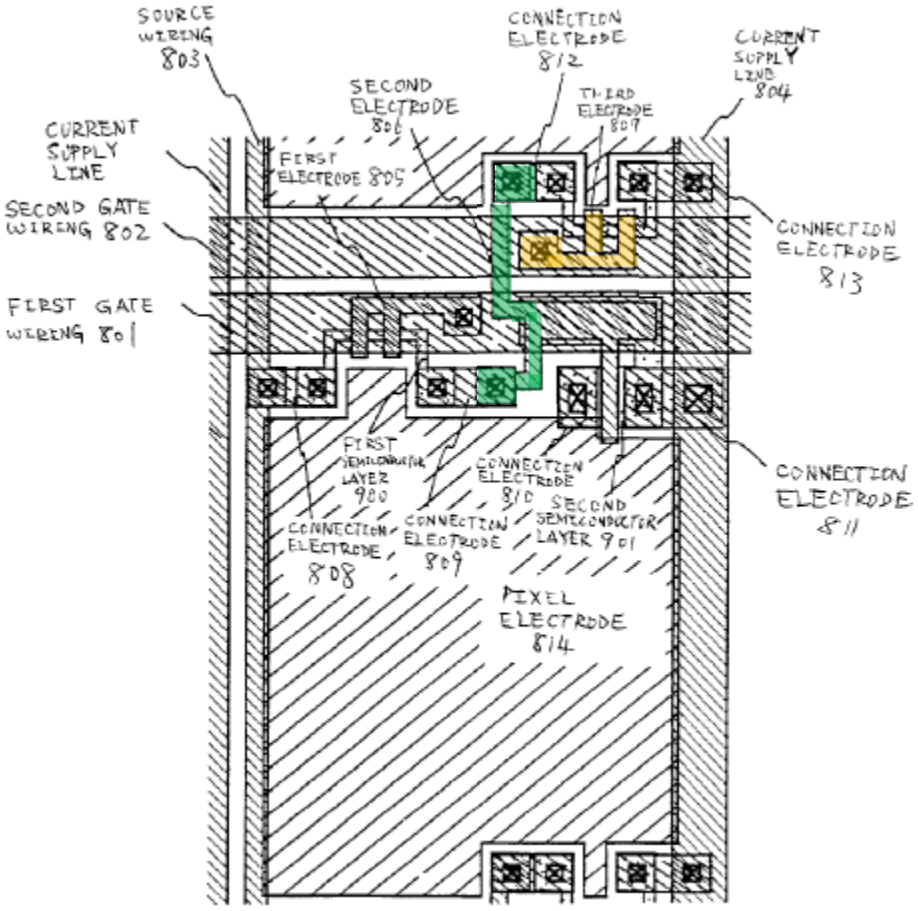


FIG. 8 of Yamazaki (annotated)

109. The components being formed on the same layer can be understood in view of EX-1011, ¶[0166]-[0168], which describes that first electrode 805 (which includes the gate electrode for the lower transistor 902), second electrode 806 (which is the connecting portion) and third electrode 807 (which includes the gate electrode for the upper transistor 906) as being formed on the same first insulating film. "island-like first electrode 805, a second electrode 806 and the third electrode 807

are formed on the first insulating film" EX-1011 ¶[0168], Therefore, it is clear that the crossing portion in Yamazaki and the gates of transistors 902 and 906 are formed on the same layer, since they are formed on the same first insulating film.

110. As set forth above, the alleged wiring portion (second electrode) in Yamazaki is on a different layer than the control line 802 and therefore able to cross the control line 802 because it is formed on the same layer as the gates of the first and second transistors, contrary the requirements of claim 1. Accordingly, Yamazaki would not have rendered it obvious to modify Inukai 574, since Yamazaki does not disclose that the alleged wiring portion (which is actually a second electrode) is on a different layer than the gates of the first and second transistors.

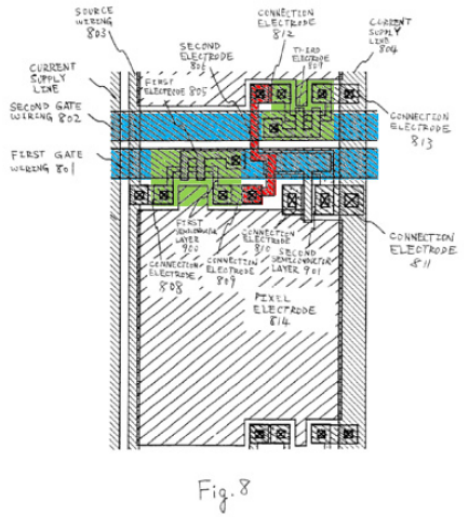
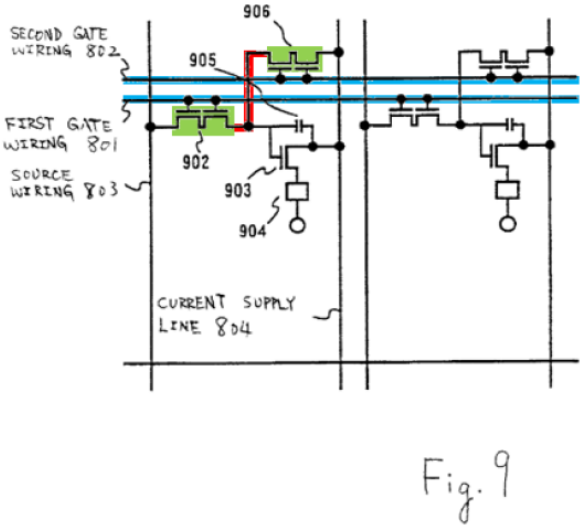
b. The Petitioner fails to establish reason for modifying Inukai 574 in view of Yamazaki for obviousness

111. The Petitioner alleges that it would be obvious to modify Inukai 574 in view of Yamazaki with a "reasonable expectation of success" for two reasons: (1) "Inukai 574 does not restrict how its circuits must be laid out by specifying particular plan views"; and (2) "the schematic views of both references depict transistors connected by a wire that crosses a gate wiring." Pet., 82. The Petitioner is incorrect on both accounts.

112. On the first point, as discussed above, Inukai 574 does in fact provide a description of a physical implementation at FIG. 16 (relied on by the Petitioner in an attempt to show other structural features of the claim, Pet., 78) that restricts how its circuits must be laid out. This physical implementation provides the alleged wiring portion on a particular layer (cited and relied on by the Petitioner its Grounds 2a and 2b) that is the same layer as the control line, therefore restricting a crossing of the two. Grounds 2a and 2b in the Petition ignore this critical disclosure.

113. On the second point, contrary to the Petitioner's allegation, the schematic view of Yamazaki does *NOT* "depict transistors connected by a wire that crosses a gate wiring." Instead, Yamazaki explicitly discloses that the portion crossing the gate wiring is an electrode (not wiring) that is part of (not connected to) the second transistor. EX-1011, ¶¶ [0030], [0168]

114. In detail, the Petitioner relies on the portion annotated in red in FIGS. 8 and 9 of Yamazaki below as the alleged wiring, and the transistors 906 and 902 as the alleged first transistor and the second transistor. However, Yamazaki at FIG. 8 and the corresponding description in the specification explicitly discloses that the portion annotated in red is a second ***electrode*** 806 which is an electrode of the erasing transistor (TFT) 902. EX-1011, ¶¶ [0030], [0168].FIG. 9 of Yamazaki (annotated in Pet., 84)

Yamazaki at Fig. 8	Yamazaki at Fig. 9
	

115. Yamazaki distinguishes electrodes from wiring, and the alleged wiring portion in Yamazaki is not a wiring portion but an ***electrode*** ("second electrode 806"). EX-1011, ¶ [0030]. Further, the second electrode 806 is not connected to the transistor, but is explicitly a part of transistor (erasing TFT) 906 as a source/drain of the transistor 906. *See* EX-1011 ¶[0166]-[0168].

116. Contrary to the Petition's unsupported allegation that the two references have "similar circuitry," the circuits in Inukai 574 and Yamazaki have substantial differences, as discussed above and as further set forth below.

117. The most clear difference is that the number of transistors per pixel unit circuit in Yamazaki and Inukai 574 is different. As can be seen in FIG. 5 of Inukai 574, there are 6 transistors and 2 holding elements per EL element, whereas

Yamazaki as seen in FIG. 9 only utilizes 3 transistors and 1 holding element per EL element. Noticeably, two driving TFTs 3806a and 3806b in Inukai 574 and connected to the EL element 3808, whereas Yamazaki only has a single current supply TFT 903 connected to EL element 904. Accordingly, simply on the number of components per EL element alone, the circuits cannot be considered to be similar.

118. The difference in the number of driving TFTs in Inukai 574 is not a nominal difference. In fact, the problem to be solved of Inukai 574 is mentioned to require using gate signal line driver circuits in order to increase the number of gray-scale levels. "In the present invention, a pair of gate signal line driver circuits and a pair of source signal line driver circuits are provided and different gate signal line driver circuits and different source signal line driver circuits may be used with respect to each adjacent pair of the writing-in periods to enable to overlap the two writing-in periods each other. For example, the writing-in period Ta2 can begin before the end of the writing-in period Ta1. Overlapping of the writing-in periods described above enables each display period to be set so as to be shorter than the corresponding writing-in period. Consequently, an extremely short display period can be set to realize a large number of gray-scale levels." *See* EX-1008, ¶[0047].

119. In contrast, Yamazaki does not describe whatsoever using a pair of gate signal line driver circuits, nor does it consider the problem to be solved of realizing

a large number of gray-scale levels. On this basis, it cannot be considered that Yamazaki and Inukai 574 are functionally similar.

120. It can further be noted that the number of data lines per pixel unit circuit is not the same. Two data lines, 3802a and 3802b are present in Inukai 574 as illustrated in FIG. 5 of Inukai 574, whereas Yamazaki only describes a single source wiring 803 as illustrated in FIG. 9 of Yamazaki.

121. The Petitioner completely ignores these differences and relies on mischaracterizations of the cited art as the basis for its obviousness allegation.

XII. Summary

122. For the reasons I set forth above, it is my opinion that claim 1 of the ’760 Patent is not anticipated or obvious by the prior art used in Grounds 1a through 2b in the Petition.