

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD., BEIJING BOE DISPLAY
TECHNOLOGY CO., and MOTOROLA (WUHAN) MOBILITY
TECHNOLOGIES COMMUNICATION CO., LTD.,

Petitioner,

v.

ELEMENT CAPITAL COMMERCIAL COMPANY PTE. LTD,
Patent Owner.

IPR2023-00696
Patent 8,525,760 B2

Before DAVID C. McKONE, TERRENCE W. McMILLIN, and
RUSSELL E. CASS, *Administrative Patent Judges*.

CASS, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314(a)

I. INTRODUCTION

A. Background

BOE Technology Group Co., Ltd., Beijing BOE Display Technology Co., and Motorola (Wuhan) Mobility Technologies Communication Co., Ltd. (“Petitioner”) filed a Petition requesting an *inter partes* review of claim 1 (the “challenged claim”) of U.S. Patent No. 8,525,760 B2 (Ex. 1001, “the ’760 patent”). Paper 4, 1 (“Pet.”). Element Capital Commercial Company PTE. LTD (“Patent Owner”) filed a Preliminary Response. Paper 8 (“Prelim. Resp.”).

An *inter partes* review may not be instituted unless it is determined that “the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314 (2018); *see also* 37 C.F.R § 42.4(a) (2021) (“The Board institutes the trial on behalf of the Director.”). The reasonable likelihood standard is “a higher standard than mere notice pleading,” but “lower than the ‘preponderance’ standard to prevail in a final written decision.” *Hulu, LLC v. Sound View Innovations, LLC*, IPR2018-01039, Paper 29 at 13 (PTAB Dec. 20, 2019) (precedential).

For the reasons provided below and based on the record before us, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing the unpatentability of the challenged claim. Accordingly, we do not institute an *inter partes* review on any grounds set forth in the Petition.

B. Real Parties in Interest

Petitioner states that the real parties in interest are BOE Technology Group Co., Ltd., Beijing BOE Display Technology Co., and Motorola (Wuhan) Mobility Technologies Communication Co., Ltd. Pet. 1, 87. Patent Owner states that Element Capital Commercial Company PTE. LTD is the real party in interest. Paper 5, 1.

C. Related Proceedings

The parties state that the '760 patent was asserted in *Element Capital Commercial Company PTE. Ltd. v. BOE Technology Group Co.*, 2:22-cv-00118-JRG (E.D. Tex.). Pet. 87; Paper 5, 1.

D. The '760 Patent (Ex. 1001)

The '760 patent is directed to “an active matrix substrate, electro-optical device, and electronic device comprising an optimal pixel layout for the stable driving of electro-optical elements.” Ex. 1001, 1:43–47. The '760 patent Specification explains that, in an active matrix electro-optical device, a plurality of pixels are arranged in a matrix, each of which includes a pixel circuit with an electro-optical element and a driving transistor for supplying power to the electro-optical element. *Id.* at 1:21–27. Each of the pixel circuits corresponds to an intersection of a data line and a scan line. *Id.* at 1:27–29. According to the Specification, the system must precisely control the power supplied to the electro-optical elements in order to precisely control the brightness of the display, and there is a need for a display with an optimized driving circuit, driving method, and pixel layout. *Id.* at 1:31–39. Problems encountered in actual pixel layouts, the Specification explains, include “contact between pixel electrodes and peripheral circuitry, stability of holding capacitances, and transistor turn-off currents.” *Id.* at 1:39–42.

In order to address these issues, the '760 patent proposes a display with “a first active matrix substrate” comprising “peripheral circuitry to supply a current to electro-optical elements provided in each pixel,” each peripheral circuit having “a holding element to control a control voltage, a first active element, connected to the holding element, to supply a current to the electro-optical element based on the control voltage, and a second active element, connected to the holding element, to control the charging and discharging of the holding element,” where the “second active element has a structure which prevents leakage currents during shutoff.” Ex. 1001, 1:51–62. One embodiment of the invention is shown in Figure 5, reproduced below.

Fig.5

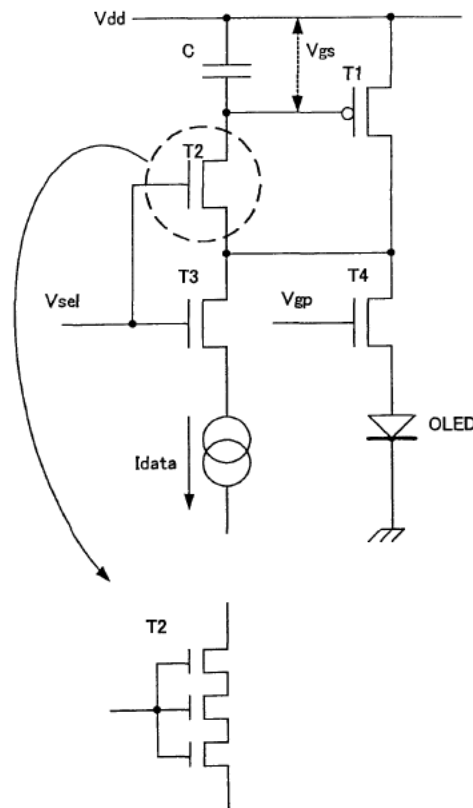


Figure 5 of the '760 patent is a circuit diagram of a pixel region in an embodiment of the invention. Ex. 1001, 10:17–18, Fig. 5.

As shown in Figure 5, the pixel region includes light emitting element OLED, capacitor C, transistors T1, T2, T3, and T4, write control line Vsel, light emission control line Vgp, and data line Idata. *Id.* at 17:57–18:12.

In the embodiment of Figure 5, “[p]ixel display begins with the selection of the write control line Vsel as a data writing operation, putting the transistors T2 and T3 into the turned-on state.” Ex. 1001, 17:63–65. When transistors T2 and T3 are put into the conducting state, “the transistor T1 reaches a steady state after a prescribed time, and electric charge accumulates in the holding capacitor C according to the data current Cdata” provided by data line Idata. *Id.* at 17:66–18:2. To emit light, “write control line Vsel is put into the unselected state, the transistors T2 and T3 are turned off, and after stopping supply of the data current Cdata, the light emission control line Vgp is selected.” *Id.* at 18:3–6. As a result, “transistor T4 is turned on, and a current corresponding to the potential difference Vgs between the voltage stored in the holding capacitor C and the power supply voltage Vdd is supplied to the light-emitting portion OLED via the transistors T1 and T4, so that light is emitted from the light-emitting layer.” *Id.* at 18:6–12.

A “plan[] view which explains the wiring pattern in one pixel region and the periphery” is shown in Figure 2, reproduced below. Ex. 1001, 11:13–14.

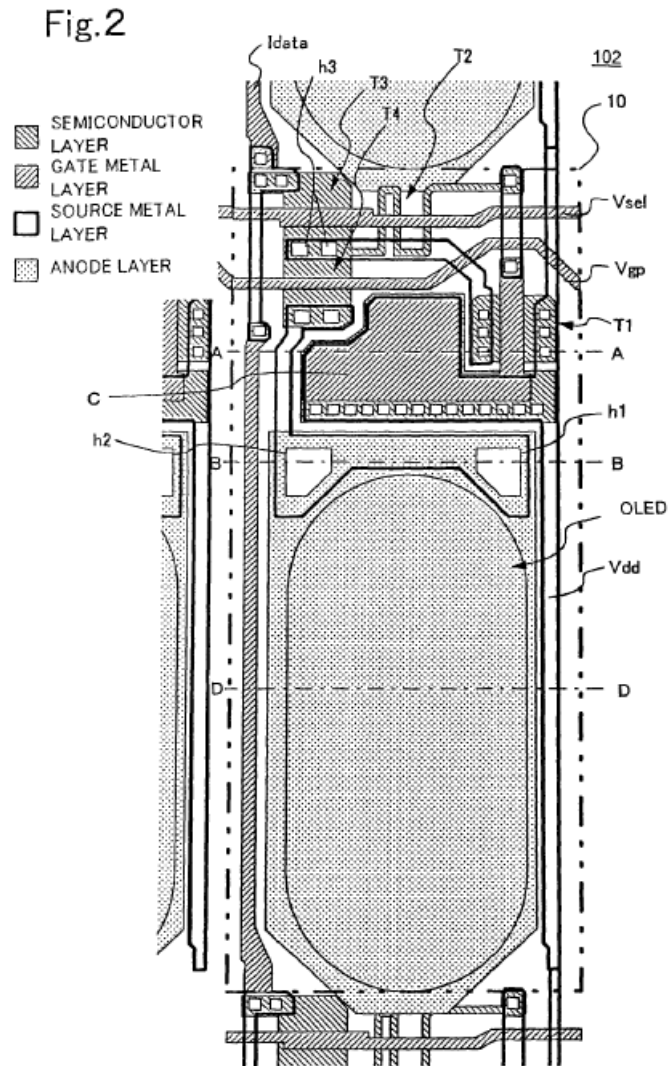
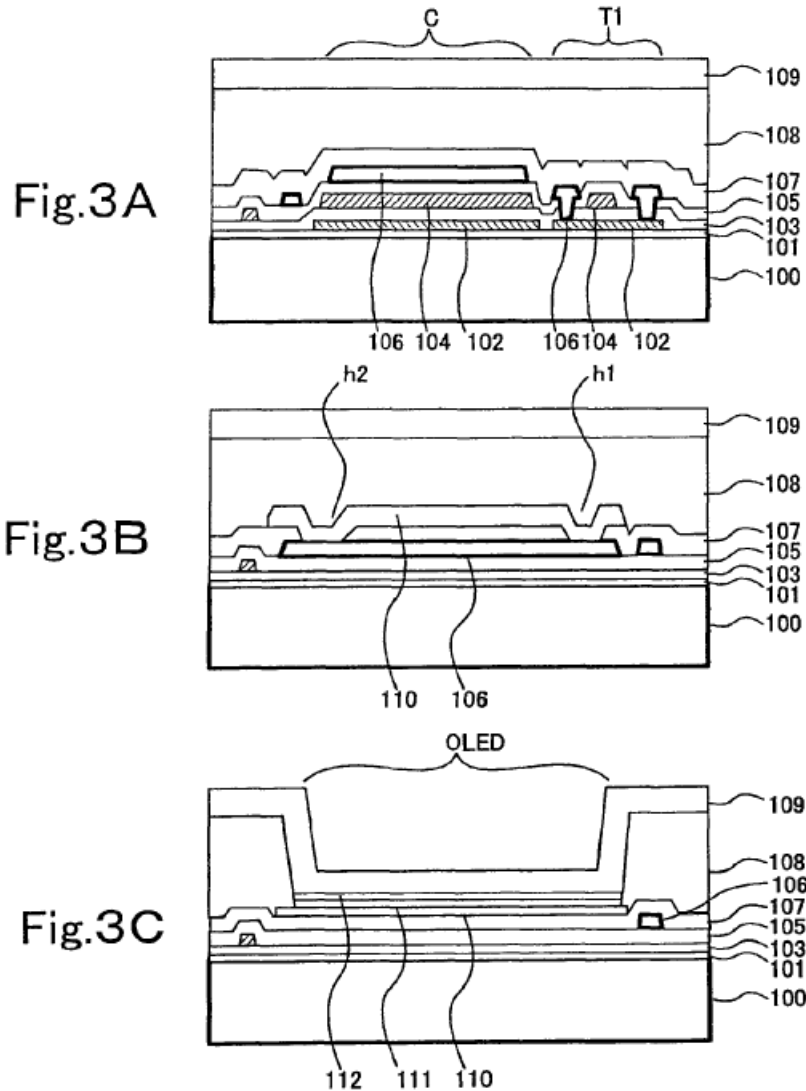


Figure 2 of the '760 patent is a plan view which shows the wiring pattern in one pixel and its periphery. Ex. 1001, 11:14–15, Fig. 2.

As shown in Figure 2, light emitting portion OLED and peripheral circuitry to drive it are positioned in the region enclosed by power supply line Vdd and data line Idata. *Id.* at 11:19–22. The peripheral circuitry includes transistor T1 as a first active element, transistor T2 as a second active element, transistor T3 as a current-controlling active element, transistor T4 as a light emission-controlling active element, and holding capacitor C as a holding element. *Id.* at 11:24–29. The transistor T1 has its source connected to power supply line Vdd and its drain connected to the drain side

of transistor T4. *Id.* at 11:33–35. The source of transistor T4 is connected to the anode of light emitting portion OLED, and holding capacitor C is formed between the power supply line Vdd and the gate of transistor T1. *Id.* at 11:35–38. The source of transistor T2 is connected to holding capacitor C and the gate of transistor T1, and the drain of transistor T2 is connected to the drain of transistor T3 and between transistors T1 and T4. *Id.* at 11:38–41. The source of transistor T3 is connected to the data line Idata, and the gate is connected, in common with the gate of transistor T2, to write control line Vsel. *Id.* at 11:41–44.

A cross-section of the layer structure in each of the cross-sectional planes of Figure 2 are shown in Figures 3A–3C, reproduced below.



Figures 3A–3C show cross sections of the layer structure of the planes in Figure 2. Ex. 1001, 11:45–46.

Figure 3A shows the layer structure in the A-A cross-sectional plane of Figure 2, Figure 3B shows the layer structure in the B-B cross-sectional plane, and Figure 3C shows the layer structure in the C-C cross-sectional plane. *Id.* at 11:46–49. As shown in Figure 3A, pixel region 10 is formed by stacking, on glass substrate 100, underlayer protection film 101, semiconductor layer 102, gate insulating layer 103, gate metal layer 104, first interlaminar insulating film 105, source metal layer 106, second interlaminar insulating film 107, bank layer 108, and cathode layer 109.

Id. at 11:50–56. As shown in Figures 3B and 3C, electric field light-emitting portion OLED is configured by stacking anode layer 110, hole transport layer 111, and light emitting layer 112. *Id.* at 11:56–59. The '760 patent further explains that “data lines Idata and scan lines Vsel use the gate metal layer 104,” and “at the intersections between data lines Idata and scan lines Vsel, data lines Idata are formed in the source metal layer 106” rather than in gate metal layer 104. *Id.* at 17:32–39.

E. Challenged Claim

Claim 1 is the only claim challenged in this proceeding, and is reproduced below.

1. [a] An electro-optical device comprising:
 - [b] a data line;
 - [c] a control line; and
 - [d] a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit including:
 - [e] a first transistor that includes a first semiconductor film;
 - [f] an electro-optical element electrically connected to one of a source or a drain of the first transistor;
 - [g] a second transistor that includes a second semiconductor film, the second transistor connected between one of the source or drain and a gate of the first transistor;
 - [h] a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor according to a data signal; and
 - [i] a wiring connected between the second transistor and the gate of the first transistor;
 - [j] the first transistor supplying a current based on the gate voltage of the first transistor;

[k] the wiring being formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film are formed;

[l] the wiring having a portion formed in the layer different from a gate layer in which the gate of the first transistor is formed, the portion crossing the control line.

Ex. 1001, 25:10–35 (indents and bracketed paragraph identifiers added).

F. Applied References

Petitioner relies upon the following references:

Inukai, US 2002/0000576 A1, published January 3, 2002 (Ex. 1007, “Inukai 576”);

Inukai, EP 1 111 574 A2, published June 27, 2001 (Ex. 1008, “Inukai 574”);

Yamazaki US 2001/0025959 A1, published October 4, 2001 (Ex. 1011, “Yamazaki”).

Pet. iii, 2. Petitioner submits the Declaration of Dr. David K. Liu (Ex. 1006). Patent Owner submits the Declaration of Dr. Aris Silzars (Ex. 2001).

G. Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claim 1 of the ’760 patent based on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1	102, 103(a)	Inukai 576
1	103(a)	Inukai 576, Yamazaki
1	102, 103(a)	Inukai 574
1	103(a)	Inukai 574, Yamazaki

Pet. 1.

II. DISCUSSION

A. Claim Construction

A claim “shall be construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b).” 37 C.F.R. § 42.100(b) (2020).

Petitioner proposes that no formal claim constructions are necessary in this proceeding. Pet. 18. Patent Owner agrees. Prelim. Resp. 4.

We determine that it is not necessary to construe any claim terms for purposes of this Decision. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1374 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

B. Principles of Law

A claim is unpatentable under 35 U.S.C. § 102 if a single prior art reference discloses each and every limitation of the claimed invention, either explicitly or inherently. *Allergan, Inc. v. Apotex Inc.*, 754 F.3d 952 (Fed. Cir. 2014). A single prior art reference may anticipate without disclosing a feature of the claimed invention if such feature is necessarily present, or inherent, in that reference. *Id.*

A claim is unpatentable under 35 U.S.C. § 103 if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying

factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, objective evidence of non-obviousness.¹ *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17–18 (1966). When evaluating a combination of teachings, we must also “determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). Whether a combination of prior art elements would have produced a predictable result weighs in the ultimate determination of obviousness. *Id.* at 416–17.

In an *inter partes* review, the petitioner must show with particularity why each challenged claim is unpatentable. *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016); 37 C.F.R. § 42.104(b). The burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

We analyze the challenges presented in the Petition in accordance with the above-stated principles.

C. Level of Ordinary Skill in the Art

Both parties agree that a person of ordinary skill in the art at the time of the alleged invention would have had “at least a Master’s degree in electrical engineering, physics, or a related field.” Pet. 2 (citing Ex. 1003 ¶¶ 26–27); Prelim. Resp. 4–5 (citing Ex. 2001 ¶¶ 22–23). The parties, however, disagree about the work experience one of ordinary skill would have had. Petitioner asserts that one of ordinary skill would have had “at

¹ At this stage of the proceeding, Patent Owner has not presented objective evidence of non-obviousness.

least two years of relevant work experience in the field of integrated circuit design and manufacturing.” Pet. 2 (citing Ex. 1003 ¶¶ 26–27). Patent Owner contends that one of ordinary skill would have had “at least two years of relevant work experience in the field of display device technology.” Prelim. Resp. 4–5 (citing Ex. 2002 ¶¶ 21–23). Both parties agree that “[a]dditional education can remedy lack of work experience and vice versa.” Pet. 2; Prelim. Resp. 5.

We note that the ’760 patent and challenged claim concern both display device technology and integrated circuit design for display devices. The ’760 patent and challenged claim do not appear to concern integrated circuit manufacturing processes. Accordingly, for purposes of this Decision, we determine that a person of ordinary skill in the art would have had a Master’s degree in electrical engineering, physics, or a related field and at least two years of relevant work experience in the field of integrated circuit design for display devices. However our decision in this proceeding would not change if we adopted either Petitioner’s or Patent Owner’s definition of the person of ordinary skill.

D. Ground 1a:² Asserted Anticipation or Obviousness of Claim 1 over Inukai 576

1. Overview of Inukai 576 (Ex. 1007)

Inukai 576 is directed to “an electronic display formed by forming EL (electroluminescence) elements on a substrate” and “a display device with an EL display used in its display portion.” Ex. 1007 ¶ 2. As background, Inukai 576 explains that EL elements driven by analog driving type circuitry

² Here, and elsewhere in the Decision, the identification of the grounds using designations such as “Ground 1a” and “Ground 1b” refers to the designation of the grounds as presented in the Petition.

could be “easily affected by variation in the characteristics of” transistors in that circuitry. *Id.* ¶¶ 12, 34, 35, 37. Slight variation of those characteristics “results in considerable difference in the amount of light emitted from the EL elements between adjacent pixels even if a signal of equal voltage is inputted thereto.” *Id.* ¶ 34. To address this issue, Inukai 576 proposes a driving method that improves “control of the amount of light emitted from EL elements” by primarily controlling the “time during which the EL elements emit light” rather than “control of current using the saturated region.” *Id.* ¶ 39. Inukai also discloses particular pixel driving circuitry to implement this driving method in Figures 3 and 9. *Id.* at Figs. 3, 9.

a) Elements 1[a]–1[k]

Petitioner argues that Inukai 576 discloses elements 1[a]–1[k]. Patent Owner does not dispute Petitioner’s showing as to these elements. For purposes of background, and to better understand the parties’ dispute concerning element 1[l], we summarize below Petitioner’s matching of claim elements 1[a]–1[k] with the disclosures of Inukai 576.

1. [a] “An electro-optical device comprising:”

Petitioner argues that Inukai 576 discloses an electronic device that incorporates a display and includes an “EL monitor,” as shown in Figure 24A, reproduced below. Pet. 23–24.

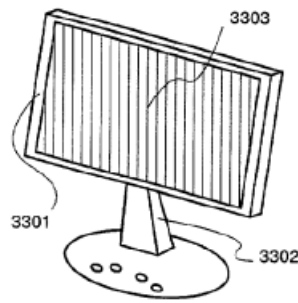
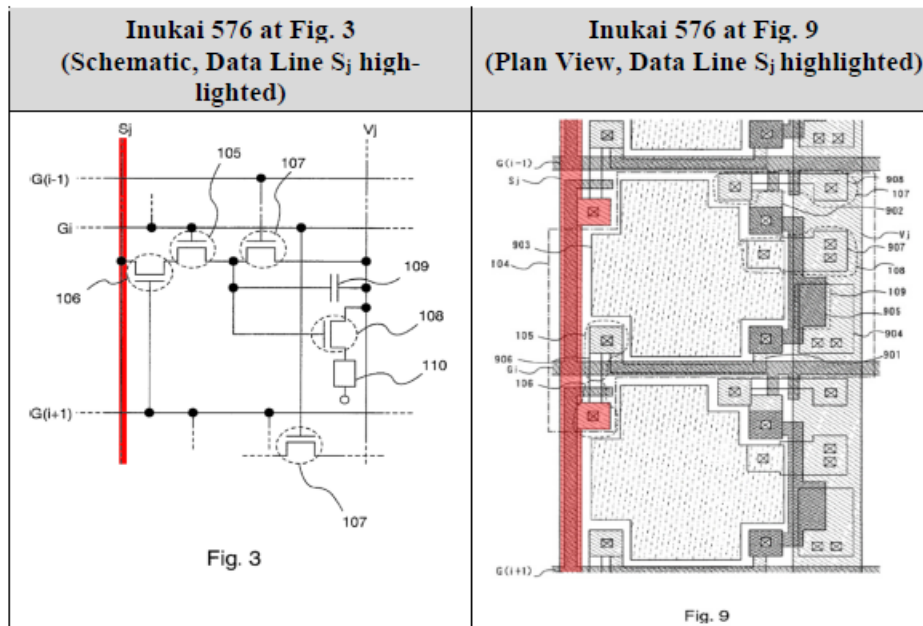


Fig. 24A

Figure 24A is a drawing of an electronic apparatus using an EL display.
Ex. 1007 ¶ 64. Petitioner relies on Figure 24A of Inukai 576 to show an EL monitor. Pet. 23–24.

1. [b] “a data line;”

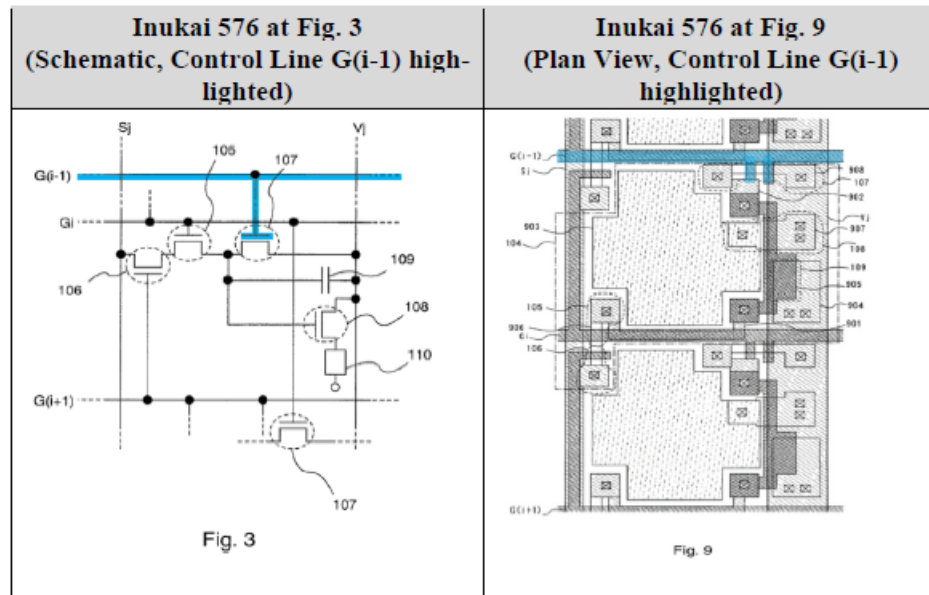
Petitioner argues that Inukai 576 discloses a data line in the form of “source signal line S_j ,” as depicted in red in Petitioner’s annotated versions of Figures 3 and 9 below. Pet. 25.



Petitioner’s annotated versions of Figures 3 and 9 of Inukai 576, a circuit diagram and a plan view, respectively, of pixels of an EL display, showing the “data line” S_j in red. Pet. 25; Ex. 1007 ¶¶ 43, 49.

1. [c] “a control line; and”

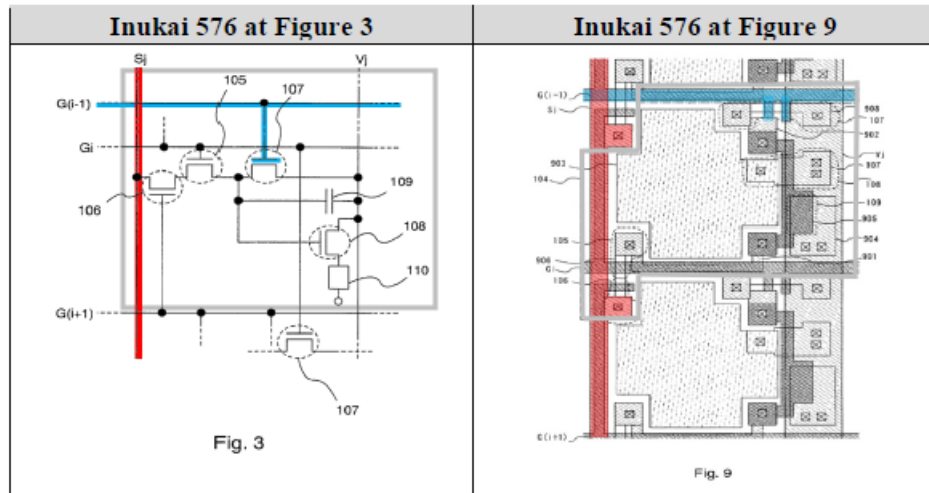
Petitioner argues that Inukai 576 discloses a control line in the form of “gate signal line G(i-1),” as depicted in blue in Petitioner’s annotated versions of Figures 3 and 9 below. Pet. 26.



Petitioner’s annotated versions of Figures 3 and 9 of Inukai 576, a circuit diagram and a plan view, respectively, of pixels of an EL display, showing the “control line” G(i-1) in blue. Pet. 27; Ex. 1007 ¶¶ 43, 49.

1. [d] “a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit including:”

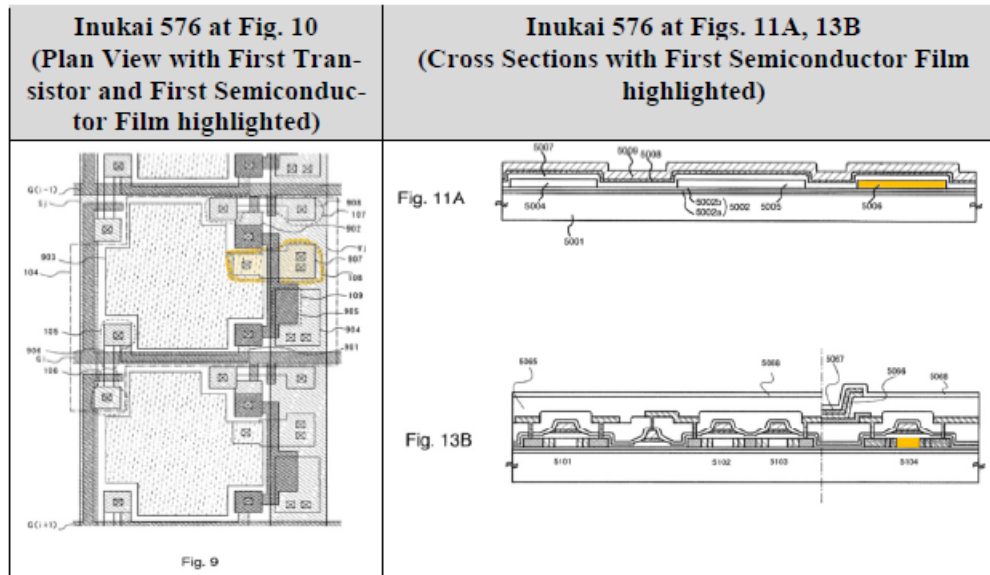
Petitioner argues that Inukai 576 discloses circuit elements (including driving TFT 108, erasing TFT 107, capacitor 109, TFTs 105 and 106, and EL element 110) that “correspond to the intersection of source signal line S_j and gate signal line G(i-1)” and “constitute[] a unit circuit,” as depicted in Petitioner’s annotated versions of Figures 3 and 9 below which “feature a gray box to highlight the unit circuit.” Pet. 29.



Petitioner’s annotated versions of Figures 3 and 9 of Inukai 576, a circuit diagram and a plan view, respectively, depicting a data line S_j (red), a control line $G(i-1)$ (blue), and a gray box to highlight the “unit circuit.”
Pet. 28–29; Ex. 1007 ¶¶ 43, 49.

1. [e] “a first transistor that includes a first semiconductor film;”

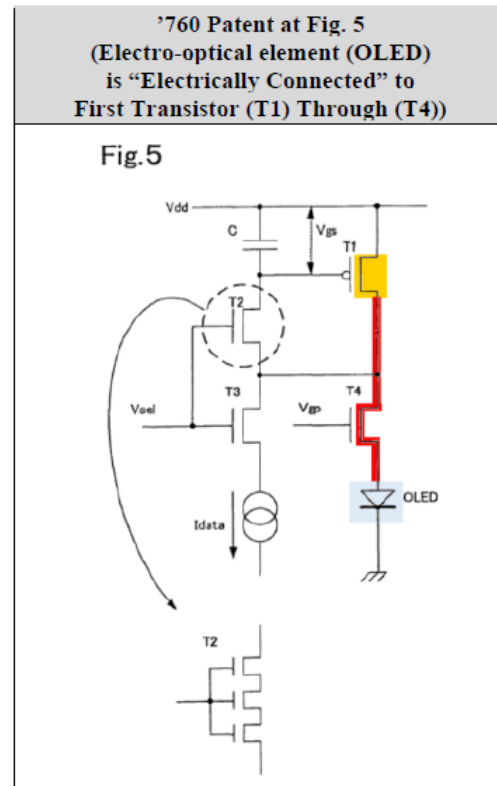
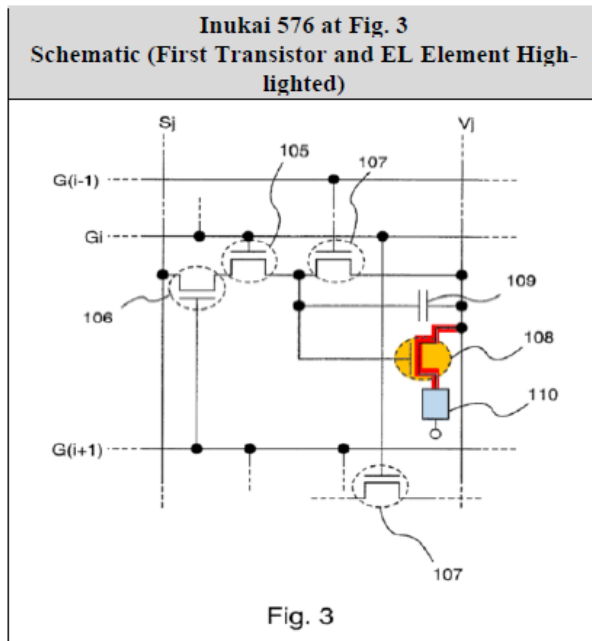
Petitioner argues that Inukai 576 discloses “a first transistor (TFT 108) and its first semiconductor film (active layer 907),” as depicted in yellow in Petitioner’s annotated versions of Figures 10, 11A, and 13B below. Pet. 30.



Petitioner’s annotated versions of Figure 10 (a block diagram) and Figures 11A and 13B (a manufacturing process) showing first transistor TFT 108 and first semiconductor film (active layer 907) highlighted in yellow. Pet. 30–31; Ex. 1007 ¶¶ 50, 51, 53.

1. [f] “an electro-optical element electrically connected to one of a source or a drain of the first transistor;”

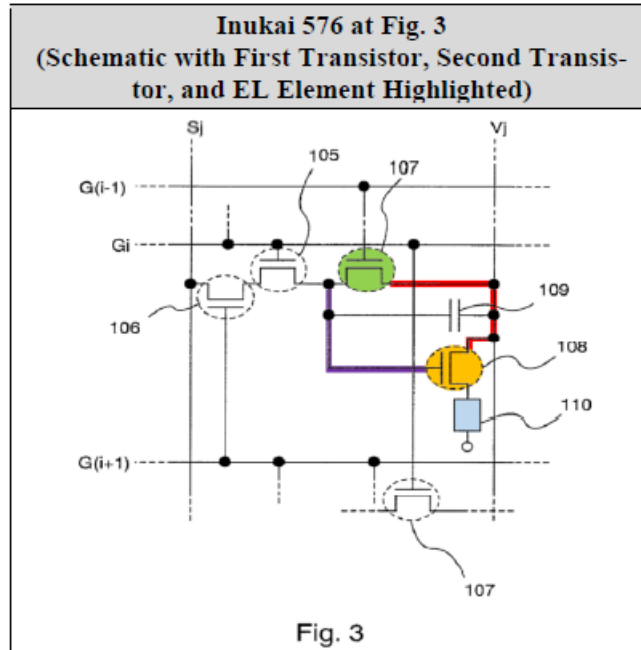
Petitioner argues that Inukai 576 discloses an electro-optical element being electrically connected to transistor T1 through transistor T4, as illustrated by the red electrical path in Petitioner’s annotated versions of Figures 3 and 5, reproduced below.



Petitioner's annotated versions of Figure 3 of Inukai 576 (a circuit diagram) and Figure 5 of the '760 patent (a circuit diagram), showing a red electrical path connecting an electro-optical element (110 or OLED) (pale blue) to transistor T1 (orange) through transistor 108 or T4. Pet. 31–34; Ex. 1001, 10:17–18; Ex. 1007 ¶ 43.

1. [g] "a second transistor that includes a second semiconductor film, the second transistor connected between one of the source or drain and a gate of the first transistor;"

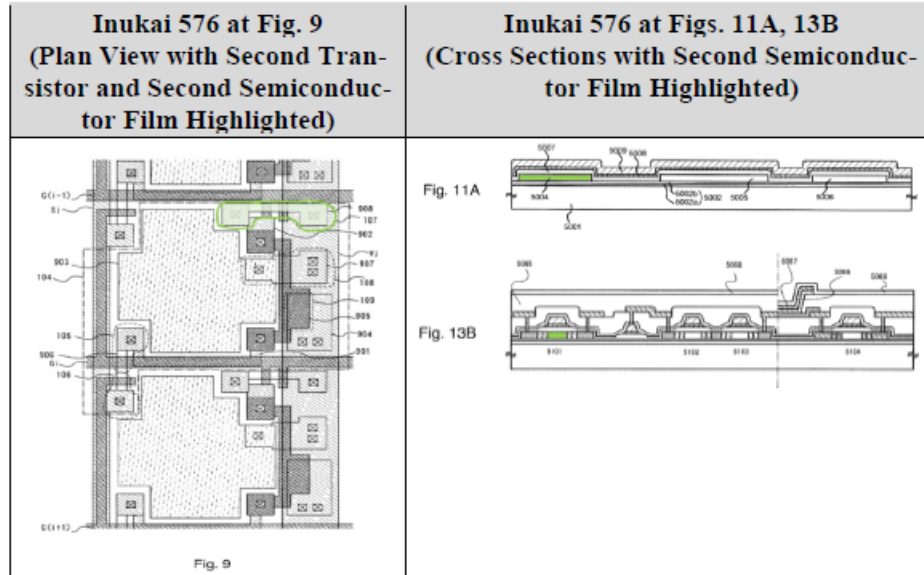
Petitioner argues that Inukai 576 discloses that the second transistor (TFT 107) is connected between the gate and the source of the first transistor (TFT 108), as shown by the purple and red electrical paths shown in Figure 3, reproduced below.



Petitioner's annotated version of the circuit schematic of Figure 3 showing a purple electrical path connecting the second transistor (TFT 107) to the path of the first transistor (TFT 108), and a red electrical path connecting the second transistor (TFT 107) to the source of the first transistor (TFT 108).

Pet. 36–37; Ex. 1007 ¶ 43.

Petitioner also includes annotated versions of Figures 9, 11A, and 13B, reproduced below, showing the second transistor and second semiconductor film highlighted in green.

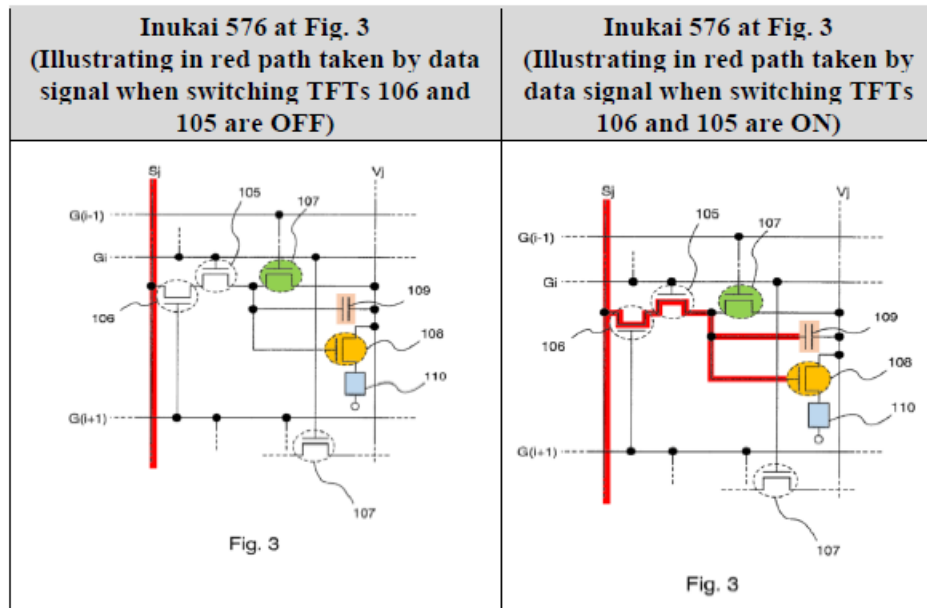


Petitioner’s annotated versions of the plan view of Figure 9 and the manufacturing process diagram of Figures 11A and 13B, showing the second transistor and second semiconductor film highlighted in green.

Pet. 35–36; Ex. 1007 ¶¶ 49, 51, 53.

1. [h] “a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor according to a data signal;”

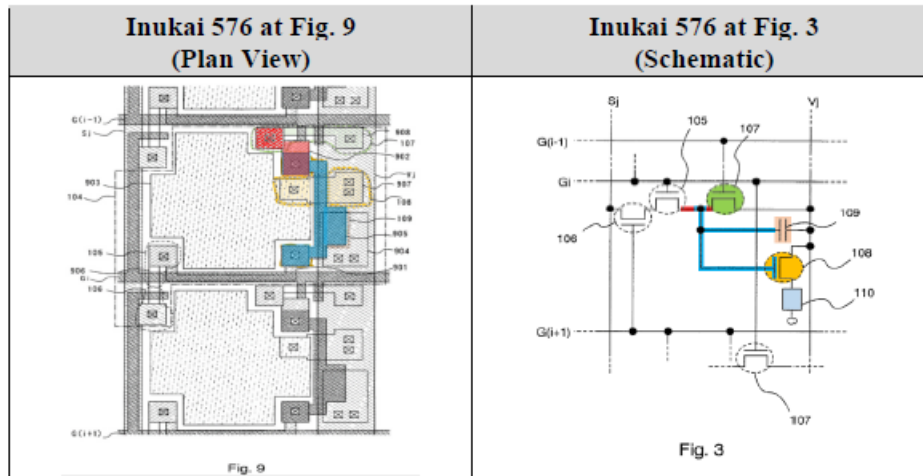
Petitioner argues that Inukai 576 discloses a “holding element” in the form of capacitor 109, which holds a gate voltage to TFT 108’s gate when the signal provided by signal line Sj passes through switching TFTs 105 and 106, as shown in Petitioner’s annotated versions of Figure 3 reproduced below.



Petitioner's annotated versions of the circuit schematic of Figure 3 showing the paths taken by the data signal (red) when switching TFTs 105 and 106 are "on" and "off." Pet. 38–41; Ex. 1007 ¶ 43.

1. [i] "a wiring connected between the second transistor and the gate of the first transistor;"

Petitioner argues that the claimed "wiring" is met by gate wiring 905 formed in the gate layer (blue) and connection wiring 902 formed in the connection wiring layer (red), as shown by Petitioner's annotated versions of Figures 3 and 9, reproduced below.

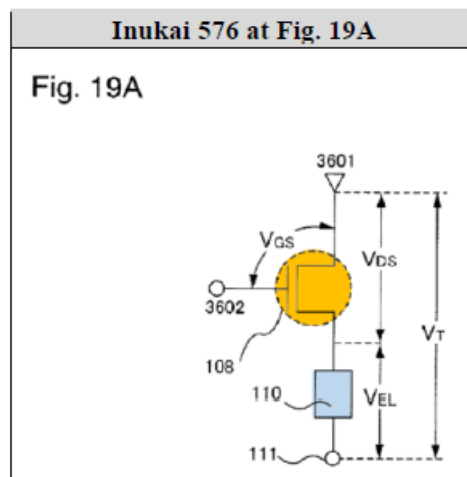


Petitioner's annotated versions of the plan view of Figure 3 and the circuit schematic of Figure 9 showing gate wiring 905 formed in the gate layer (blue) and connection wiring formed in the connection wiring layer (red).

Pet. 41–42; Ex. 1007 ¶¶ 43, 49.

1. [j] “the first transistor supplying a current based on the gate voltage of the first transistor;”

Petitioner argues that Inukai 576 discloses that transistor 108 supplies current to the EL element 110 based on the gate to source voltage V_{GS} of transistor 108, as shown in Petitioner's annotated version of Figure 19A, reproduced below.

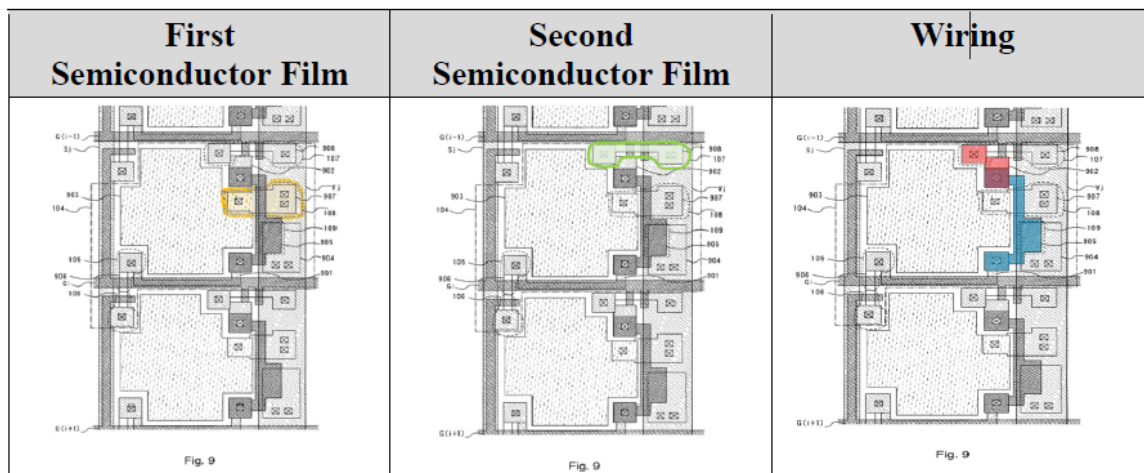


Petitioner's annotated version of the diagram of Figure 19A showing transistor 108 (yellow) supplying current to EL element 110 (light blue)

based on the gate to source voltage V_{GS} of transistor 108. Pet. 42–43;
Ex. 1007 ¶ 59.

1. [k] “the wiring being formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film are formed;”

Petitioner argues that Inukai 576 discloses a first semiconductor film (907), a second semiconductor film (908), and wiring (gate wiring 905 and connection wiring 902) that connects the first transistor’s gate to the second transistor, as shown in Petitioner’s annotated versions of Figure 9, reproduced below.

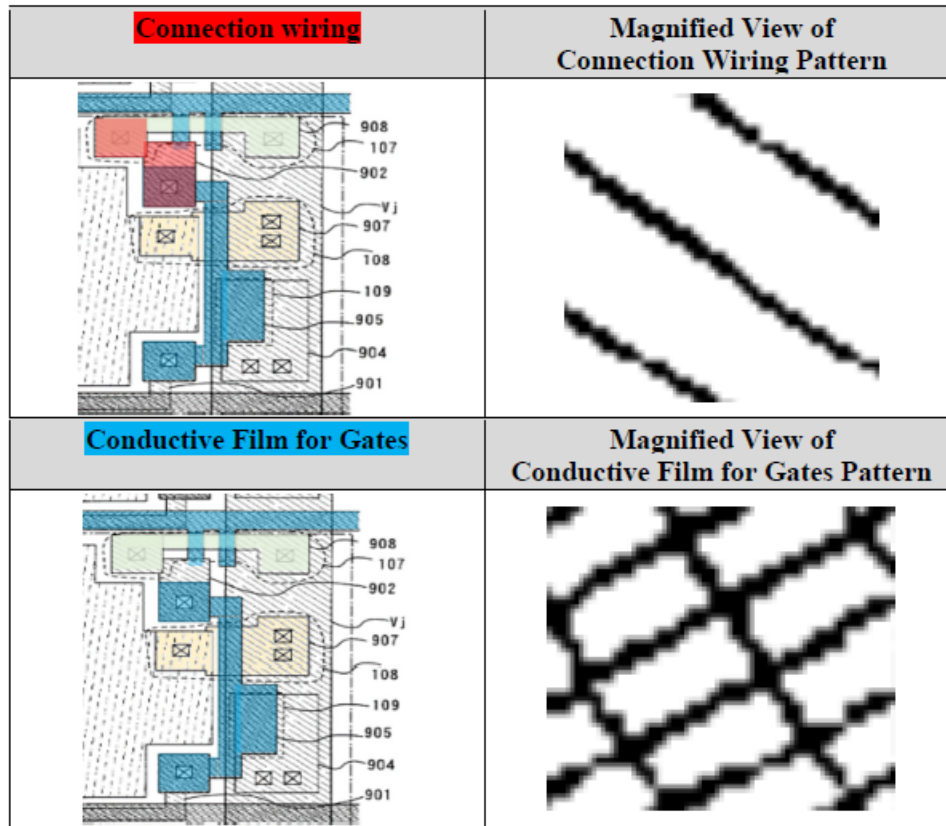


- b) *Element 1. [l] “the wiring having a portion formed in the layer different from a gate layer in which the gate of the first transistor is formed, the portion crossing the control line;”*

The parties dispute whether Inukai 576 discloses or suggests element 1[l]. Pet. 47–54; Prelim. Resp. 10–24.

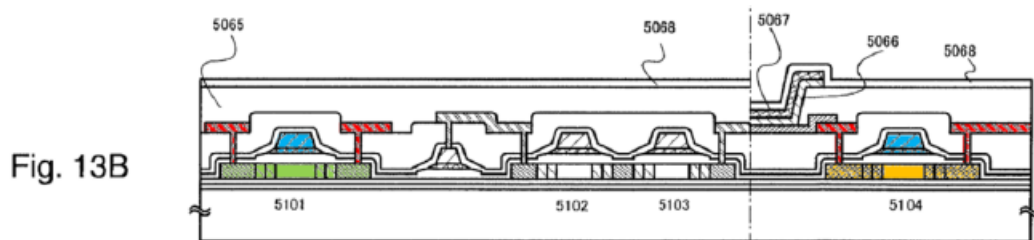
(1) Petitioner’s Contentions

Petitioner argues that Inukai 576 discloses that the wiring connecting the first transistor (TFT 108) to the second transistor (TFT 107) has a portion that exists in the “connection wiring” layer in red, which is a different layer than the gate layer in which the first transistor’s gate is formed (gate wiring 905) highlighted in blue, as shown in Petitioner’s annotated version of portions of Figure 9, reproduced below.



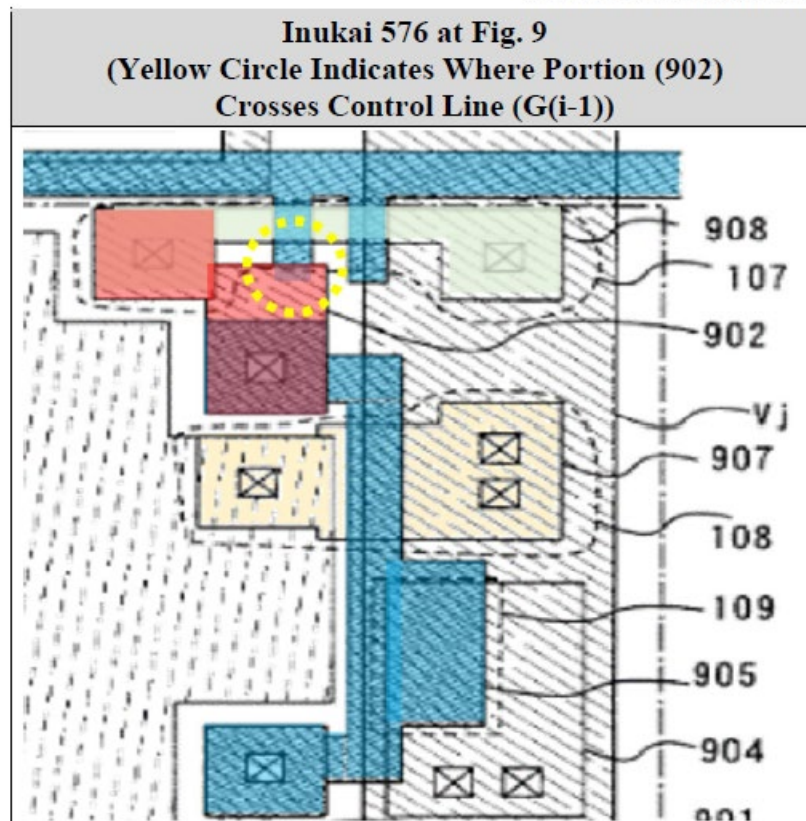
Petitioner's annotated versions of the plan view of Figure 9 showing the connection wiring (red) and the conductive film for the gates (blue). Pet. 48; Ex. 1007 ¶ 49.

Petitioner also argues that Figure 13B, reproduced below, further confirms that the connection layer (red) is different from the gate layer (blue).



Petitioner's annotated version of the manufacturing process diagram of Figure 13B showing the connection wiring (red) and the conductive film for the gates (blue). Pet. 48; Ex. 1007 ¶ 53.

Petitioner argues that the claimed “portion” is met by connection wiring 902 which crosses a protrusion of gate signal line G(i-1), which is part of the “control line,” as shown by the yellow circle in Petitioner’s annotated version of Figure 9, reproduced below.



Petitioner’s annotated version of the plan view of Figure 9 with a yellow circle showing how it contends that portion 902 crosses control line G(i-1).
Pet. 49–50; Ex. 1007 ¶ 49.

Petitioner argues that the protrusions of control line G(i-1) are part of the “control line” even though they function as gate electrodes. Pet. 50 (citing Ex. 1006 ¶¶ 110–111). Petitioner asserts that “the ’760 patent confirms this principle by identifying ‘Vsel’ as a control line, even though it has portions that also function as a gate electrode.” *Id.* (citing Ex. 1006 ¶¶ 110–111); Ex. 1001, 11:41–44. Petitioner acknowledges that the left protrusion’s “full outline is not explicitly shown,” but contends that one of

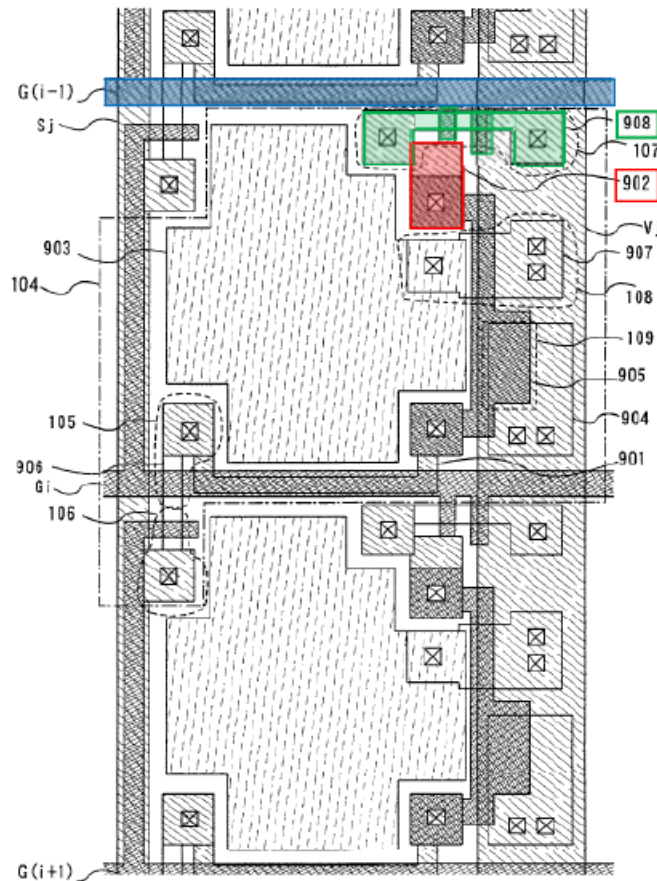
ordinary skill “would have understood or found obvious that the protrusion would have been the same length as the protrusion on the right, due to the ‘endcap rule.’” Pet. 51. According to Petitioner, the “endcap rule” is “a universal rule in semiconductor design that requires gates to have a certain minimum length,” and “further requires that the two gate electrodes protruding from gate signal line G(i-1) have the same length.” *Id.* at 51–52 (citing Ex. 1006 ¶¶ 113–115). Petitioner further argues that prior art U.S. Patent No. 5,498,579 to Borodovsky confirms its position. *Id.* at 52–53 (citing Ex. 1010, 4:21–33, 6:11–17, 9:42–46, Figs. 3, 7; Ex. 1006 ¶¶ 113–115).

Additionally, Petitioner argues that, “[t]o the extent Inukai 576 does not explicitly disclose that the control line’s left-hand side gate electrode extends far enough such that the connection wiring 902 passes over it,” one of ordinary skill “would have found it obvious to modify Inukai 576 in this manner” because “enforcing the ‘endcap rule’ would ensure that the gates extend sufficiently far such that they have good control over the transistor channel.” Pet. 54 (citing Ex. 1006 ¶¶ 113–116). Additionally, according to Petitioner, there would be no reason for the gates to have different lengths, and one of ordinary skill would have been motivated to ensure that all gates would have endcaps of equal length to ensure that they are long enough to exert control. *Id.* (citing Ex. 1006 ¶¶ 113–116; Ex. 1010, 9:42–46).

(2) Patent Owner’s Contentions

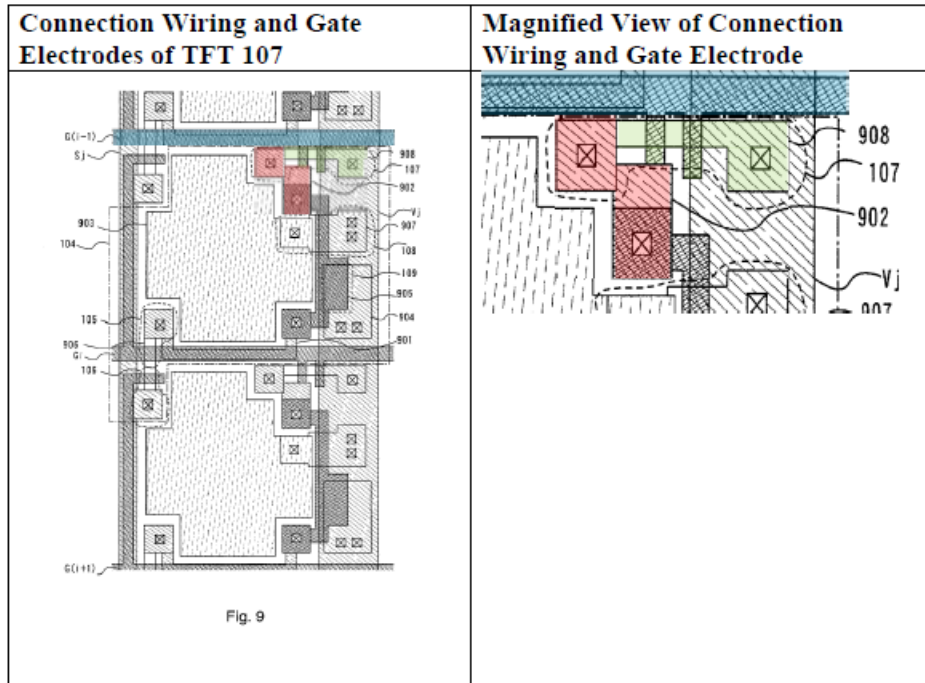
Patent Owner makes three arguments in response. First, Patent Owner argues that Inukai 576 fails to disclose a wiring portion that crosses “a control line,” because the protrusions that Petitioner points to as part of the “control line” G(i-1) “are not control lines but are gate electrodes of the TFT

107.” Prelim. Resp. 12 (citing Ex. 2001 ¶¶ 43–44). Patent Owner asserts that “the claim defines the unit circuit as corresponding to an intersection of the data line and the control line,” so “the control line is the *line* that intersects the data line, *i.e.*, the horizontal control line shown in both the ’760 Patent and Inukai 576 that intersects the vertical data line.” *Id.* at 12–13 (citing Ex. 2001 ¶ 45). Additionally, Patent Owner contends that “Inukai 576 expressly distinguishes the gate electrodes (*i.e.*, protrusions) from the gate signal line G (control line), and describes the gate electrodes as part of the TFT 107 and ‘connected to’—not part of—the gate signal line G.” *Id.* at 13 (citing Ex. 1007 ¶¶ 201, 107, 160). Patent Owner illustrates this argument with an annotated version of Inukai 576’s Figure 9, reproduced below.



Patent Owner’s annotated version of the plan view of Inukai’s Figure 9 showing the “control line” $G(i-1)$ (blue), the active layer 908 (including the protrusions from line $G(i-1)$ that act as gate electrodes) (green), and the wiring portion 102 (red). Prelim. Resp. 14; Ex. 1007 ¶ 49.

Second, Patent Owner argues that Inukai 576 fails to disclose a wiring portion that “crosses” a control line because “Inukai 576 provides a wiring portion 902 that extends near but does not cross the gate electrode of the TFT 107,” as shown by Patent Owner’s annotated versions of Figure 9 of Inukai 576, reproduced below. Prelim. Resp. 15.

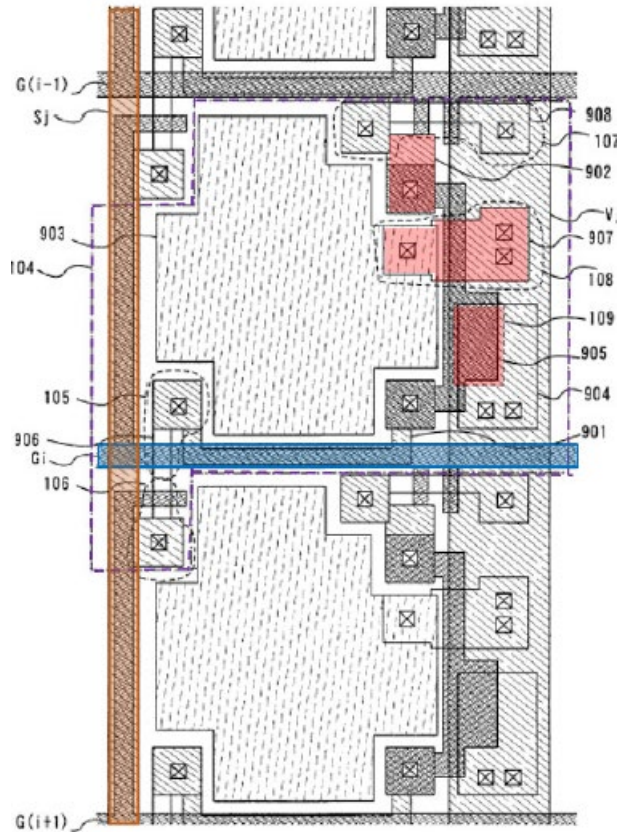


Patent Owner’s annotated version of the plan view of Inukai’s Figure 9 showing the “control line” G(i-1) (blue), the active layer 908 (including the protrusions from line G(i-1) that act as gate electrodes) (green), and the wiring portion 102 (red). Prelim. Resp. 16; Ex. 1007 ¶ 49.

Patent Owner argues that Figure 9 “explicitly shows the outlines of component parts irrespective of whether that component would otherwise be hidden by another layer ‘topographically above,’” such as the transistor body outline, which “can be seen even though it is below the gate electrode (protrusion), which runs above the transistor body.” *Id.* at 16 (citing Ex. 2001 ¶¶ 50–51). Thus, according to Patent Owner, one of ordinary skill “would have understood that the Inukai 576 inventor deliberately designed its gate electrode such that it does not overlap with the wiring portion 902, as unambiguously shown in the figure.” *Id.* at 17 (citing Ex. 2001 ¶ 52). Indeed, Patent Owner argues, one of ordinary skill would “want to avoid overlapping the two in order to avoid unwanted interference (*e.g.*, crosstalk) between the gate electrode and wiring portion 902.” *Id.* (citing Ex. 2001 ¶¶ 52–58; Ex. 2003 ¶ 80, Fig. 6).

Additionally, Patent Owner argues that neither Petitioner nor Dr. Liu provide support for the allegation that the “endcap rule” is universally applied. Prelim. Resp. 18. Patent Owner asserts that “Borodovsky merely describes the general concept that an endcap of a transistor gate may extend some minimum distance beyond an active region so as to ensure that any rounding of the endcap does not occur over the active region,” but does not say that this rule is “*universally* applied.” *Id.* (citing Ex. 1010, 4:21–33; Ex. 2001 ¶¶ 59–61, 63). Additionally, according to Patent Owner, Borodovsky does not “provide any basis to conclude that the ‘endcap rule’ would yield gate electrodes of the *same* size or length.” *Id.* (citing Ex. 1010, 9:42–46).

Third, Patent Owner argues that Inukai 576 fails to disclose a unit circuit corresponding to a control line and comprising a wiring portion crossing that control line. Prelim. Resp. 20–24. Patent Owner illustrates its argument with an annotated version of Inukai’s Figure 9, reproduced below.



Patent Owner’s annotated version of the plan view of Inukai’s Figure 9 showing components of a unit circuit (red) corresponding to the intersection of data line S_i (orange) and control line G_i (blue). Prelim. Resp. 21–22; Ex. 1007 ¶ 49.

Patent Owner argues that Inukai 576 defines its pixel unit 104 as corresponding to the intersection of data line S_i and control line G_i , which includes the components highlighted in red in the above annotated figure. Prelim. Resp. 21. And, Patent Owner contends, “the Petition cites to TFT 108 for the first transistor, capacitor 109 for the holding circuit, and wiring 904 for the claimed wiring portion, each of which corresponds to the intersection of the particular data line S_i and the particular control line G_i .” *Id.* at 22. However, according to Patent Owner, “for an alleged teaching of the wiring portion crossing the control line, the Petition cites to a different control line $G(i-1)$ that corresponds to and defines a different pixel unit than

the unit circuit of the wiring portion, the first transistor, etc.” *Id.* at 22–23 (citing Ex. 2001 ¶ 74). Thus, Patent Owner argues, “the wiring portion, the first transistor, the holding circuit, etc., cited by the Petition are plainly of the pixel unit circuit corresponding to the intersection of G_i and S_j , NOT the distinct pixel unit corresponding to the intersection of $G_{(i-1)}$ and S_j .” *Id.* at 23 (citing Ex. 2001 ¶ 75).

(3) *Analysis*

Based on the present record, we determine that Petitioner has failed to establish a reasonable likelihood that element 1[1] is disclosed or suggested by Inukai 576.

First, we determine that Petitioner has not sufficiently shown that the protrusions that Petitioner points to are part of the “control line.” Petitioner does not propose any claim construction for the term “control line,” much less one that would persuasively show that the claimed “control line” would include the protrusions relied on by Petitioner that act as gate electrodes of TFT 107. Patent Owner provides testimony from Dr. Silzars that one of ordinary skill would have understood a “control line” to be “a line which runs along a direction and carries an electrical signal,” and would not include the protrusions that form the gate electrodes, and Dr. Liu does not provide any testimony to the contrary. *See* Ex. 2001 ¶ 45. This is consistent with the ’760 patent, which shows “control line” V_{sel} in Figure 2 as being a horizontal line that crosses over second transistor T2. Ex. 1001, Fig. 2, 11:19–44). Dr. Silzars also opines that Inukai 576 distinguishes the gate electrodes (the projections) from the gate signal line G (the control line) by describing the gate electrodes as part of the second transistor 107 and “connected to,” rather than part of, the gate signal line G, which is consistent

with Inukai 576's disclosure. Ex. 2001 ¶ 48; Ex. 1007 ¶¶ 201 ("When the gate signal line G1 is selected, the TFT 107 . . . whose gate electrodes are connected to the gate signal line G1 are turned on."), 107 ("the TFTs 107 . . . , the gate electrodes of which are connected to the gate signal line G1"), 160 ("the TFT 107 . . . whose gate electrodes are connected to the gate signal line G1 are turned on"). In light of this testimony, and Petitioner's failure to address the proper construction of this term, Petitioner has failed to sufficiently show that the gate electrodes are part of the claimed "control line."

We also agree with Patent Owner that Petitioner has failed to sufficiently show that Inukai 576 discloses a wiring portion that "crosses" a control line. As noted above, Petitioner acknowledges that the right protrusion's "full outline is not explicitly shown," but contends that one of ordinary skill "would have understood or found obvious that the protrusion would have been the same length as the protrusion on the right, due to the 'endcap rule.'" Pet. 51. However, based on the present record, we agree with Patent Owner that Petitioner fails to provide sufficient support that the "endcap rule" is universally applied. In this regard, we find reasonable Dr. Silzars's testimony that the "endcap rule" is, "at best, a design generalization which may be used in some applications for semiconductor manufacturing, heavily dependent on what materials are used, what the purpose of the semiconductor [is] and especially the manufacturing process." Ex. 2001 ¶ 60.

Petitioner relies on the Borodovsky patent, but Borodovsky merely describes the general concept that an endcap of a transistor gate may extend some minimum distance beyond an active region so as to ensure that any

rounding of the endcap does not occur over the active region. Ex. 1010, 4:21–33; Ex. 2001 ¶ 63; Pet. 52–53. Borodovsky, however, does not suggest how the rule would have been applied to Inukai 576. *See* Ex. 2001 ¶ 63. Petitioner also does not point to anything in Borodovsky that states that the “endcap rule” requires gate electrodes of the same size or length. *See* Ex. 2001 ¶ 64. Borodovsky’s design rule merely requires that the endcap extends at least a minimum length, not an exact length, beyond the active region, and states that “other size up amounts may be used.” Ex. 1010, 9:42–46; Ex. 2001 ¶ 64. Thus, assuming Inukai 576’s protrusions are of different length, as pictured, Petitioner’s evidence does not show persuasively that the shorter protrusion would violate the “endcap rule” merely because it is shorter than the other protrusion.

We note that Dr. Liu testifies that one of ordinary skill would “have known that in order to maintain a consistent current voltage characteristic for the double-gate transistors, the two channel portions of the double-gate structure would be made as uniformly identical as possible.” Ex. 1002 ¶ 114. Dr. Liu, however, does not provide any evidence or citation for this statement. *Id.* Dr. Liu also states that “[t]he endcap rule applies to all gates fabricated in the transistor,” so one of ordinary skill “would have understood that the two gates over transistor 107 have equal length,” and thus “the two protrusions would extend equal distance beyond the semiconductor layer.” *Id.* Again, however, Dr. Liu does not explain why the “endcap rule” would require or suggest this outcome, particularly because the description of the “endcap rule” merely requires that gates have a certain minimum length beyond the semiconductor layer they intersect, not that the gates be of equal length. *Id.*

Consequently, we determined that Petitioner has failed to establish a reasonable likelihood that Inukai 576 discloses or suggests claim limitation 1[l].

c) Conclusion as to Claim 1

For the reasons set for above, we determine that Petitioner has failed to demonstrate a reasonable likelihood that claim 1 is anticipated by or would have been obvious over Inukai 576.

E. Ground 1b: Asserted Obviousness of Claim 1 over Inukai 576 in view of Yamazaki

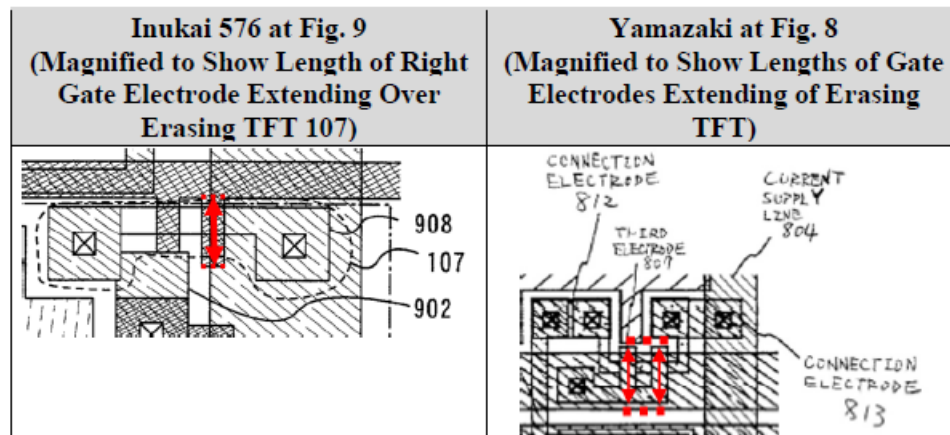
1. Overview of Yamazaki (Ex. 1011)

Yamazaki is directed to “an electronic device in which the deterioration of the device is prevented and an aperture ratio is improved without using a black mask and without increasing the number of masks.” Ex. 1011, code (57). In the device, a first electrode is disposed on another layer different from the layer on which a gate wiring is disposed as a gate electrode, and a semiconductor layer of a pixel switching TFT is superimposed on the gate wiring so as to be shielded from light. *Id.* “Thus,” Yamazaki explains, “the deterioration of the TFT is suppressed, and a high aperture ratio is realized.” *Id.*

2. Analysis of Claim 1

For claim elements 1[a]–1[k], Petitioner relies on Inukai 576 as argued with respect to Ground 1 above. Pet. 56. For claim element 1[l], Petitioner argues that it would have been obvious to combine Inukai 576 and Yamazaki such that “Inukai 576’s circuit is laid out such that each of the two multi-gate protrusions of control line G(i-1) depicted in figure 9 extends the same length, as taught by Yamazaki.” *Id.* at 55. Petitioner argues that, if

Inukai 576 does not expressly show the length of the gate electrode of its multi-gate erasing TFT 107, one of ordinary skill “would have been motivated to look to other references to determine a suitable length for the gate of electrode,” and “Yamazaki demonstrates that the length of the left gate electrode of an erasing transistor can be the same length as the gate electrode.” *Id.* (citing Ex. 1006 ¶ 119). Petitioner illustrates the combination using annotated versions of Figure 9 of Inukai 576 and Figure 8 of Yamazaki, reproduced below.

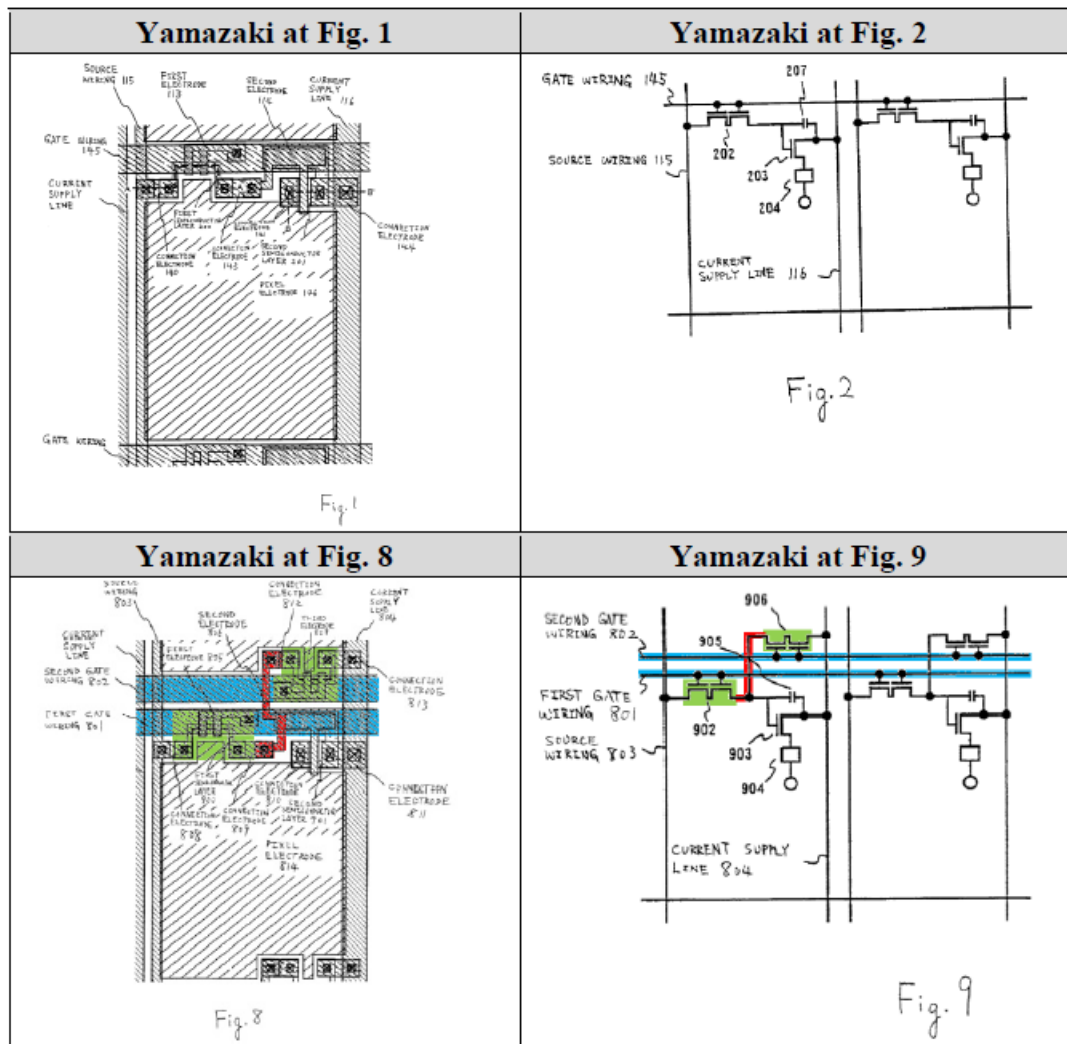


Petitioner’s annotated version of the plan view of Inukai 576’s Figure 9 magnified to show the length of the right gate electrode extending over erasing TFT 107, and the top view of Yamazaki’s Figure 8 magnified to show the lengths of the gate electrodes extending over the erasing TFT. Pet. 56; Ex. 1007 ¶ 49; Ex. 1011 ¶ 44.

Petitioner argues that one of ordinary skill would have had a reasonable expectation of success in combining the references because “[t]he gate electrodes extending over erasing TFT 107 in Inukai 576 . . . are formed in the gate layer, which is a different layer from connection wiring 902.” Pet. 56. “As a result,” Petitioner contends, “those two regions will be electrically isolated from each other due to intervening insulating layers and a signal carried by one region will not interfere with a signal carried by the other.” *Id.* (citing Ex. 1007 ¶ 267; Ex. 1006 ¶ 119, Fig. 13A).

Thus, Petitioner argues, Yamazaki demonstrates that it would have been obvious to one of ordinary skill to implement the left protrusion from the control line “so that it extended at least as far as the gate electrode depicted on the right side of figure 9,” so that a portion of the wiring “would have crossed the left side electrode.” Pet. 57. According to Petitioner, “Yamazaki discloses various multi-gate transistors, including switching TFT 202 in the schematic of figure 2 and the switching TFT 902 in the schematic of figure 9,” and “Figures 1 and 8, respectively, provide plan views illustrating how these multi-gate transistors can be laid out” such that “[t]he gates of these transistors have equal length.” *Id.* (citing Ex. 1011 ¶¶ 23, 55, 56, 61, 62, 174, Figs. 1, 2, 8, 9; Ex. 1006 ¶ 121). Thus, Petitioner asserts, one of ordinary skill “would have recognized in light of Yamazaki’s teachings that each of the gates could advantageously extend the same length, to implement the ‘endcap rule’ as discussed above.” *Id.* at 57–58.

Finally, Petitioner argues that “Yamazaki’s figures 8 and 9 also feature a wiring (shown in red) that crosses control lines (shown in blue) to connect transistors (shown in green),” as depicted in the annotated versions of Yamazaki’s Figures 1, 2, 8, and 9 reproduced below. Pet. 58.



Petitioner's annotated versions of the top views of Yamazaki's Figures 1 and 8 and the circuit schematics of Yamazaki's Figures 2 and 9 illustrating Petitioner's argument that Yamazaki discloses a wiring (red) crossing control lines (blue) to connect transistors (green). Pet. 58; Ex. 1011 ¶¶ 37, 38, 44, 45.

Patent Owner argues that one of ordinary skill would not have been motivated to combine Inukai 576 and Yamazaki for several reasons. First, Patent Owner argues that "the left electrode in Inukai 576 extends beyond the active region of the transistor, and therefore complies with the endcap rule." Prelim. Resp. 26 (citing Ex. 1007, Fig. 9). Thus, according to Patent

Owner, one of ordinary skill would not have been motivated to modify Inukai 576's left electrode to comply with this rule. *Id.*

Second, Patent Owner argues that “the endcap rule does not require or motivate design of gate electrodes to have *equal* length,” but rather “only requires gates to have ‘a certain **minimum** length.’” Prelim. Resp. 27. According to Patent Owner, “[t]wo gates can satisfy the endcap rule yet have unequal lengths, as is the case with Inukai 576,” and “[n]othing about the endcap rule requires or otherwise motivates two gates to be of equal length, let alone motivates modifications to an already-compliant gate.” *Id.* (citing Ex. 2001 ¶ 80).

Third, Patent Owner argues that Petitioner fails to establish a reasonable expectation of success in extending the length of the left gate electrode in Inukai 576 because it “does not establish that the insulating layer would prevent signal interference between the gate electrode and the wiring portion 902 due to overlap.” Prelim. Resp. 27. “To the contrary,” Patent Owner contends, one of ordinary skill “would recognize that even if a gate electrode and the wiring portion were separated with an insulating layer, interference would still occur.” *Id.* at 27–28 (citing Ex. 2001 ¶¶ 52–58, 81–82; Ex. 2003 ¶ 80, Fig. 6).

Based on the present record, we determine that Petitioner has failed to make a sufficient showing that one of ordinary skill would have been motivated to combine Inukai 576 and Yamazaki as Petitioner proposes. Petitioner presents evidence showing that Yamazaki discloses gate electrodes of equal length, and asserts that it would have been possible to modify Inukai 576 to also have gate electrodes of equal length. But neither Petitioner nor Dr. Liu adequately shows a *reason* why one of ordinary skill

would have been motivated to modify Inukai 576's gate electrodes in this manner. The mere fact that Yamazaki provides an example of electrodes of equal length in its particular configuration does not mean that one of ordinary skill would also have found it advantageous to have electrodes of equal length in the different configuration of Inukai 576.

Indeed, Dr. Liu only provides cursory testimony on this point. He states that that one of ordinary skill "would have been motivated to look to Yamazaki as a source of how long the left side gate electrode could be and recognized that the left and right gates could have equal length, as taught by Yamazaki." Ex. 1006 ¶ 119. But Dr. Liu does not provide any reason why one of ordinary skill would have recognized Inukai 576's gate electrodes to be deficient, or why modifying them would have been beneficial. The fact that "the left and right gates *could* have equal length" is not a reason why one of ordinary skill would have understood that such a modification would have been advantageous. *See id.* (emphasis added).

We also are not persuaded by Petitioner's reliance on the "endcap rule." As discussed with respect to Ground 1a, Petitioner has failed to establish that what it calls the "endcap rule" was a universal rule, rather than a general guideline that may be useful in certain situations. *See supra* § II.D.1. Moreover, Petitioner has failed to show that the endcap rule requires or suggests gate electrodes of identical length rather than merely providing that gates have a certain minimum length beyond the semiconductor layer they intersect. *See id.* Additionally, as Patent Owner points out, Inukai 576's left electrode already extends beyond the active region of the transistor, and therefore would appear to comply with the endcap rule. *See* Pet. 26; Ex. 1007, Fig. 9.

Finally, we are not persuaded by Petitioner's argument that Yamazaki's figures 8 and 9 feature a wiring that crosses control lines to connect transistors. *See* Pet. 58. Petitioner and Dr. Liu provide only cursory argument and testimony on this point, and do not explain why one of ordinary skill would have applied this wiring structure in Yamazaki to the layout of Inukai 576, or how such a modification would be carried out. *See* Pet. 58; Ex. 1006 ¶ 121.

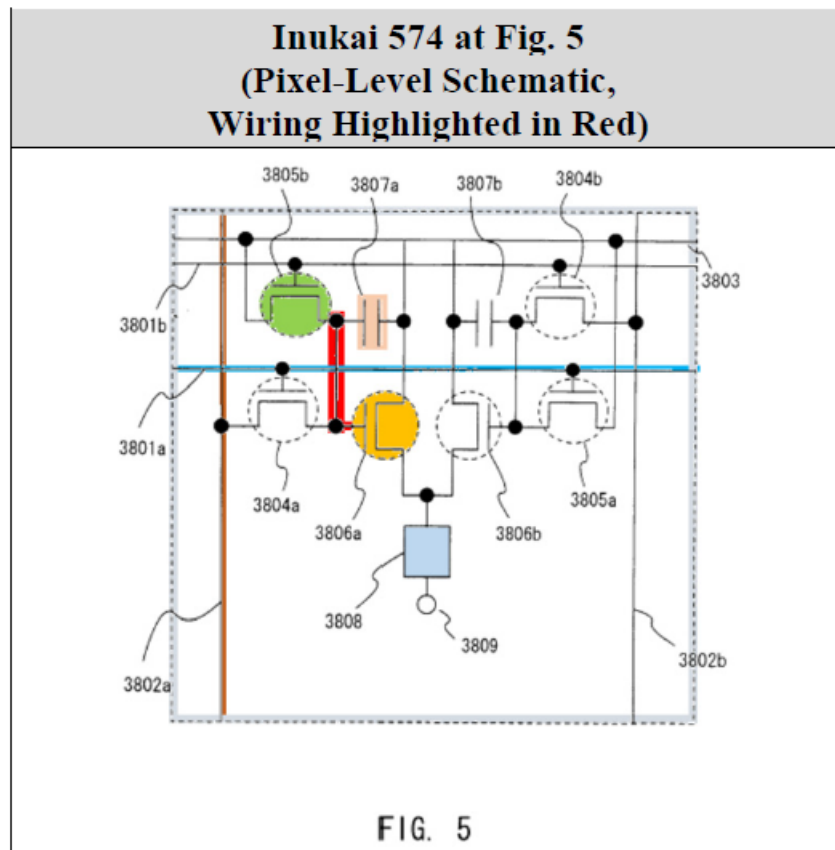
For the foregoing reasons, we determine that Petitioner has failed to establish a reasonable likelihood that claim 1 would have been obvious over the combination of Inukai 576 and Yamazaki.

F. Ground 2a: Asserted Anticipation or Obviousness Over Inukai 574
1. Overview of Inukai 574 (Ex. 1008)

Inukai 574 relates to an electroluminescent display, acknowledges that transistor characteristic variation in such displays could cause "EL elements [to] emit[] different luminous amounts," and addresses that problem with circuitry that controls light emission using a "digital data signal" rather than an "analog video signal." Ex. 1008 ¶¶ 1, 21–34. Inukai 574 discloses pixels arranged in a matrix, as well as "source signal lines (Sa1, Sb1), the power supply line (V1), and the gate signal lines (Ga1, Gb1)." *Id.* ¶ 100. To implement this digital data signal display scheme, Inukai 574 discloses "a pair of source signal line driver circuits [and] a pair of gate signal line driver circuits" that operate pixels that "each have an EL element, a pair of EL driver TFTs, a pair of switching TFTs and a pair of eliminating TFTs." *Id.* ¶ 51. Inukai 574 also provides various circuits for implementing these specific elements. *Id.* ¶¶ 149–176, 231, Figs. 3, 5, 6, 7.

2. *Claim 1*

As with Ground 1a, the parties' dispute in Ground 2a focuses on whether Inukai 574 discloses or renders obvious limitation 1[l]. Petitioner relies on the circuit schematic embodiment of Figure 5 of Inukai 574, and illustrates its arguments with an annotated version of Figure 5, reproduced below.



Petitioner's annotated version of the circuit diagram of Inukai 574's Figure 5 showing a pixel-level schematic. Pet. 80; Ex. 1008, 12:50–51.

According to Petitioner, annotated Figure 5 shows data line 3802 (brown), control line 3801a (blue), a unit circuit (gray box surrounding the schematic), first transistor 3806 (orange), EL element (pale blue), second transistor 3805b (green), and holding element 3807a (pale red). Pet. 60–72. Petitioner argues that Figure 5 also shows a wiring (red) that connects the

first transistor (TFT 3806a) to the second transistor (TFT 3805b). Pet. 73–74.

Petitioner argues that “[t]he wiring connecting the first and second transistors” can “be implemented using ‘wiring 36’ depicted in Inukai’s figure 16 cross section.” Pet. 76. Petitioner’s annotated version of Inukai 574’s Figure 16 is reproduced below.

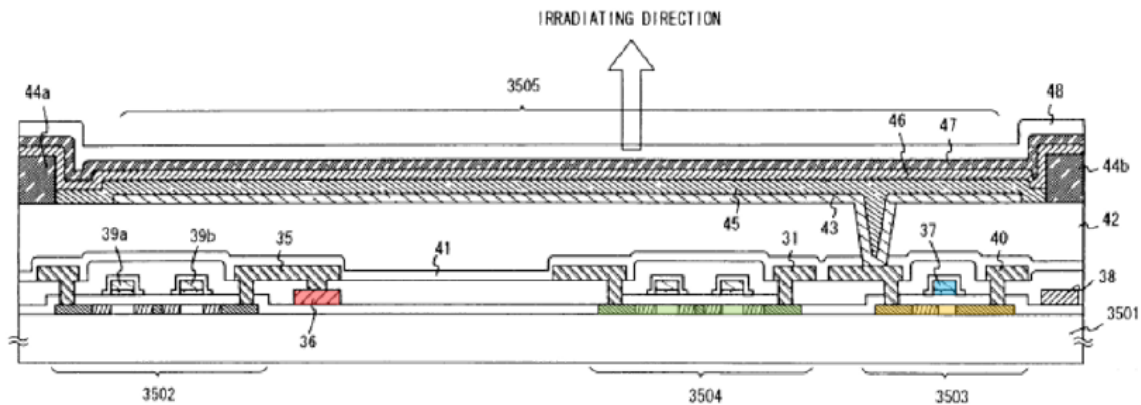
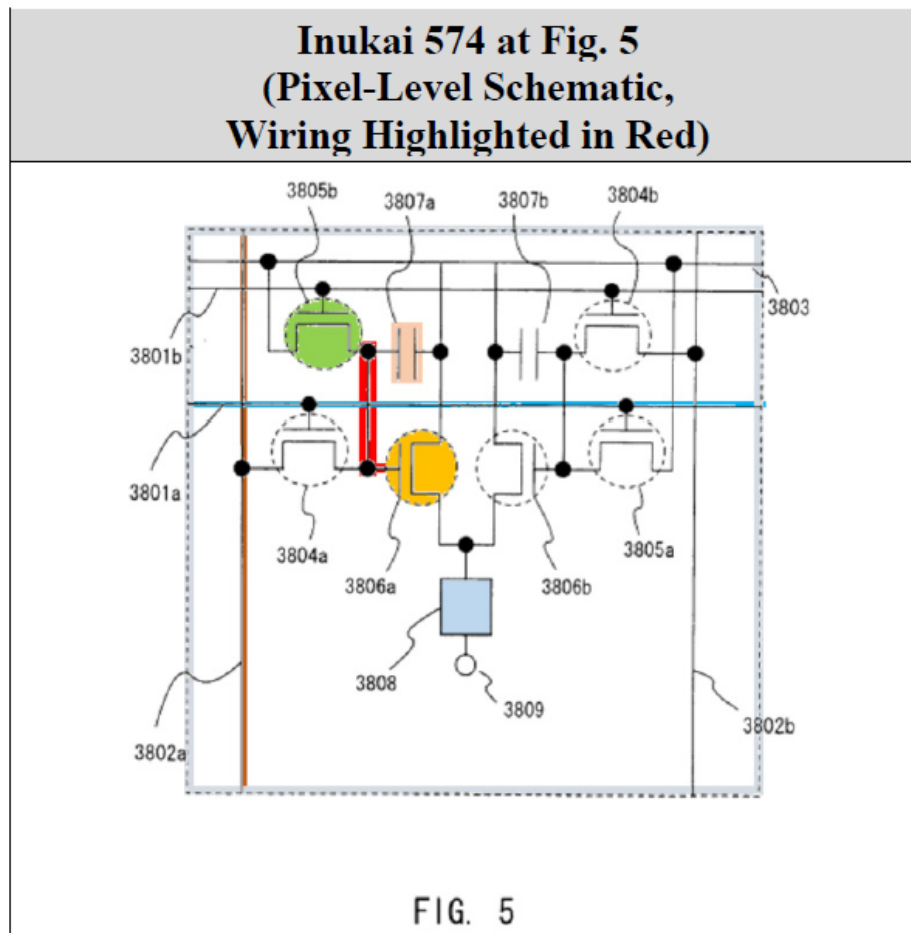


FIG. 16

Petitioner’s annotated version of the cross-sectional view of Figure 16 showing wiring 36 (red), first semiconductor film (orange), and second semiconductor film (green). Pet. 77; Ex. 1008, 13:18–19.

Petitioner argues that, in Figure 16, “[w]iring 36 (highlighted in red) is formed in a layer different from the layer in which the first transistor’s gate electrode 36 (in blue) is formed.” Pet. 78 (citing Ex. 1006 ¶¶ 136–137). Petitioner also asserts that “[t]he embodiment corresponding to figure 16 can be ‘combined with the constructions of Embodiments 1 to 7,’ which would include the circuit schematic depicted by figure 5.” *Id.* at 79 (citing Ex. 1008 ¶¶ 230–231, 308). As a result, according to Petitioner, Inukai 574 “discloses that figure 5’s schematic can be implemented using the layers and wires depicted by figure 16.” *Id.* Petitioner further argues that “[i]n this

implementation,” the “wiring crosses control line 3801a,” as shown in Petitioner’s annotated version of Figure 5, reproduced below.



Petitioner’s annotated version of the circuit diagram of Figure 5 illustrating Petitioner’s argument that Inukai 574 includes a wiring (red) that crosses the control line 3801a (blue). Pet. 80; Ex. 1008, 12:50–51.

Petitioner further argues that, “by teaching that the ‘electric current supply line 3803 is formed parallel to the gate wirings 3801a and 3801b,’ Inukai’s figure 5 not only reflects a circuit schematic, but also a possible physical layout of the circuit, featuring a wiring that crosses the control line.” *Id.* (citing Ex. 1008 ¶ 231; Ex. 1006 ¶ 137).

Additionally, Petitioner argues that, “[t]o the extent Inukai 574 does not explicitly disclose that the wiring’s portion crosses a control line,” one of

ordinary skill “would have found it obvious to modify Inukai 574 in this manner.” Pet. 80 (citing Ex. 1006 ¶ 138). According to Petitioner, “[i]mplementing a circuit schematic using a circuit layout that generally reflects the same sort of geometry depicted by the schematic would have been a matter of common engineering practice, and typically the most straightforward way to implement the schematic.” *Id.* Petitioner argues that “[t]his would be especially true with respect to Inukai 574 since its schematic requires that one line (i.e., the electric current supply line 3803) must be formed parallel to another (i.e., the gate wirings 3801a and 3801b).” *Id.*

Patent Owner responds that “Inukai 574 does not disclose a physical layout of a circuit in which a portion of a wiring crosses a control line,” but instead “discloses only circuit schematics without any description of a plan view of the corresponding physical layout.” Prelim. Resp. 29. According to Patent Owner, Figure 5 of Inukai 574 “illustrates a schematic circuit diagram—*NOT* an actual physical layout showing the actual structural arrangement—including a control line 3801a, a control line 3801b, and a data line 3802a.” *Id.* (citing Ex. 2001 ¶ 86). The circuit schematic of Figure 5 showing the wiring portion crossing control line 3801a, Patent Owner contends, “does not amount to a teaching of the wiring portion crossing the control line 3801a in the actual implementation of the circuit.” *Id.* at 30. Patent Owner also disagrees that Petitioner’s possible physical layout would have been an obvious modification to Inukai 574. *Id.* at 31–33.

Based on the present record, we determine that Petitioner has failed to show that limitation 1[l] is disclosed or suggested by Inukai 574. Patent

Owner introduces evidence from Dr. Silzars that Figure 5 of Inukai 574 discloses a schematic circuit diagram rather than an actual physical layout, and Petitioner does not appear to dispute this. *See* Ex. 1002 ¶ 86.

Dr. Silzars testifies that the notion that a circuit schematic illustrates the most straightforward implementation is a “baseless generalization,” and “it is well known in the art that a schematic circuit diagram does not necessitate or otherwise suggest a physical layout of the actual circuit to have its same geometry,” and that “other considerations such as circuit board size, heat dissipation, signal coupling between components, physical ruggedness, and space limitations would need to be considered in optimally designing the physical layout of the actual circuit.” *Id.* ¶ 88; *see id.* ¶ 89. Moreover, according to Dr. Silzars, “[i]t is common knowledge in the art that an actual circuit conforming to ‘the same sort of geometry’ of a schematic circuit diagram is not a matter of common engineering practice, but nearly impossible.” *Id.* ¶ 90; *see id.* ¶¶ 91–93 (illustrating examples of differences between the circuit schematics and actual physical layouts). Based on the present record, we find Dr. Silzar’s testimony on this point to be credible.

Dr. Liu’s testimony, by contrast, relies on generalizations and does not address these issues in any detail. Dr. Liu opines that one of ordinary skill would have understood “that the wiring depicted by figure 16’s cross section *could* implement the circuit schematic of figure 5,” but his only basis for this is the assertion that “Inukai 574 discloses that these figures are directed at embodiments that may be combined.” Ex. 1006 ¶ 136 (emphasis added) (citing Ex. 1008 ¶¶ 230–231, 308). Dr. Liu also states that Figure 5’s schematic reflects how the components and connections “should be physically laid out” because Inukai 574 states that “the electric current

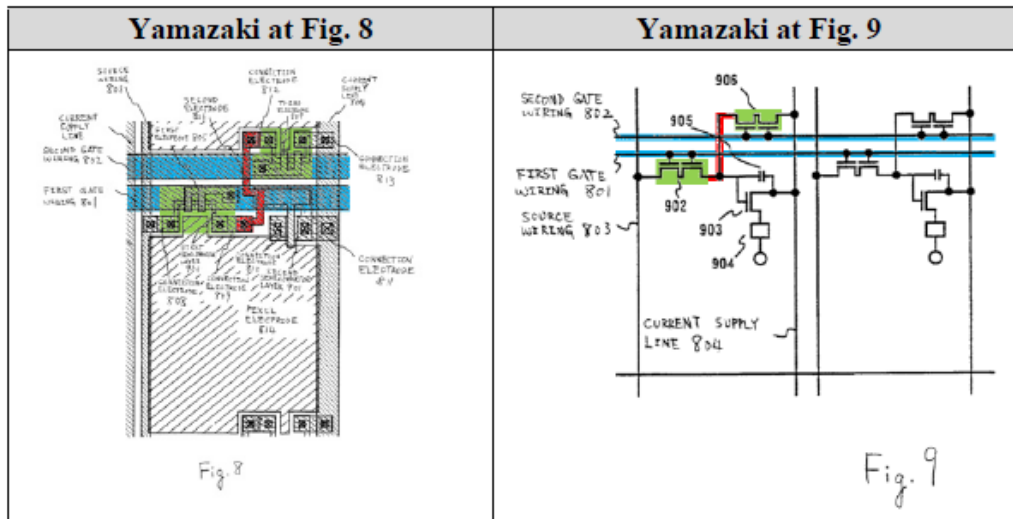
supply line 3803 is formed parallel to the gate wirings 3801a and 3801b,” but fails to sufficiently explain how this statement leads to the conclusion he reaches. *Id.* ¶ 137. Dr. Liu further speculates that a physical implementation following the Figure 5 schematic “could provide a smaller footprint for the circuit,” but fails to explain why this would be the case. *Id.* Finally, Dr. Liu states that implementing a schematic using a layout that reflects the same sort of geometry “would have been a matter of common engineering practice, and typically the most straightforward way to implement the schematic,” but fails to offer any support for this opinion. *Id.* ¶¶ 137–138. Based on the record to date, we determine that Dr. Liu’s testimony on this point is less persuasive than Dr. Silzars’s.

Consequently, we determine that Petitioner has failed to establish a reasonable likelihood that claim 1 is anticipated by or would have been obvious over Inukai 574.

G. Ground 2b: Asserted Obviousness of Claim 1 Based on Inukai 574 in view of Yamazaki

Petitioner argues that one of ordinary skill would have been motivated to combine Inukai 574 with Yamazaki. Pet. 81. Petitioner acknowledges that Inukai 574 does not provide a “plan view” that illustrates the exact physical layout of its circuitry, including the schematics shown in figure 5,” but argues that Yamazaki “provides both schematics and plan views for how to lay out that circuitry.” *Id.* at 81–82. According to Petitioner, Yamazaki discloses an “Embodiment 7,” depicted by a “pixel structure” plan view in Figure 8 that implements an “equivalent circuit” schematic view in Figure 9. *Id.* at 83–84 (citing Ex. 1011 ¶¶ 164–175). Collectively, Petitioner asserts, “these views depict a ‘switching TFT’ (depicted as 902 in figure 9) connected to an ‘erasing TFT’ (depicted as 906 in figure 9) through wiring

that crosses over both the first gate wiring 801 and the second gate wiring 802 (as depicted in both views).” *Id.* at 84. Petitioner provides annotated versions of Yamazaki’s Figures 8 and 9, reproduced below, to illustrate its argument.



Petitioner’s annotated versions of the top view of Yamazaki’s Figure 8 and the circuit diagram of Yamazaki’s Figure 9. Pet. 84; Ex. 1011 ¶¶ 44–45.

Patent Owner makes several arguments in response. First, Patent Owner argues that in Inukai 574’s physical layout of Figure 16, “the alleged wiring portion and the control line are on the same layer and therefore cannot cross,” and that “Yamazaki’s electrode 806 (alleged wiring portion) is able to cross the control line 802 because they are formed on different layers.” Pet. 40–41 (citing Ex. 2001 ¶¶ 106–110). According to Patent Owner, “Petitioner does not allege that it would have been obvious to modify Inukai 574’s arrangement of components and formation of layers or otherwise provide any basis to support such a conclusion.” *Id.* Second, Patent Owner argues that “the schematic view of Yamazaki does NOT ‘depict transistors connected by a wire that crosses a gate wiring,’” but instead “explicitly discloses that the portion crossing the gate wiring is an

electrode (not wiring) that is part of (not connected to) the second transistor.” Pet. 44–45 (citing Ex. 1011 ¶¶ 30, 168; Ex. 2001 ¶ 113).

Based on the present record, we determine that Petitioner has failed to make a sufficient showing with respect to claim 1. We agree with Patent Owner and Dr. Silzars that the only physical layout of Inukai 574, Figure 16, shows the alleged wiring portion and the control line on the same layer. *See* Ex. 1008, Fig. 16; Ex. 2001 ¶¶ 96–97, 106–107. We also agree with Patent Owner and Dr. Silzars that Yamazaki’s alleged wiring portion (electrode 806) is able to cross the control line because they are formed on different layers, which is not shown in Inukai 574’s Figure 16. Ex. 2001 ¶ 108; *see id.* ¶¶ 109–110. Furthermore, neither Petitioner nor Dr. Lui provides sufficient reasoning to explain why or how one of ordinary skill would have combined Inukai 574 and Yamazaki given these differences.

Consequently, we determine that Petitioner has failed to establish a reasonable likelihood that claim 1 would have been obvious over the combination of Inukai 574 and Yamazaki.

III. CONCLUSION

After considering the evidence and arguments presented in the current record, we determine that Petitioner has not demonstrated a reasonable likelihood of success in proving that the challenged claim of the ’760 patent is unpatentable. We therefore do not institute trial on the challenged claim and grounds raised in the Petition.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claim 1 of the '760 patent is not instituted with respect to any grounds set forth in the Petition.

IPR2023-00696
Patent 8,525,760 B2

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