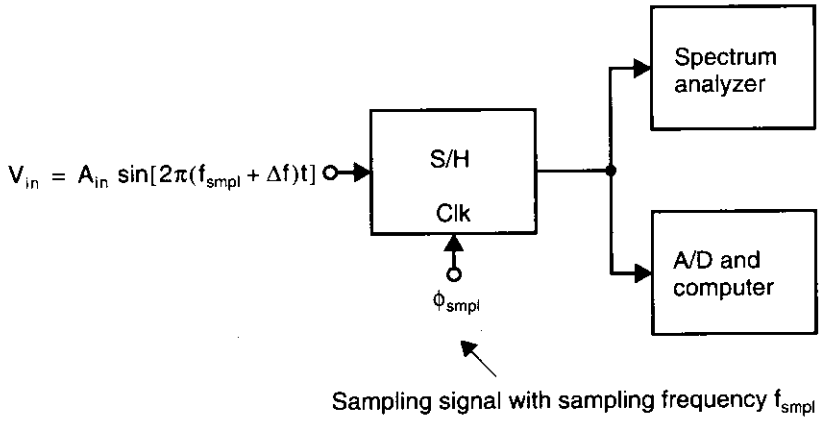


Fig. 8.1 The test setup for characterizing a sample and hold using a beat test.

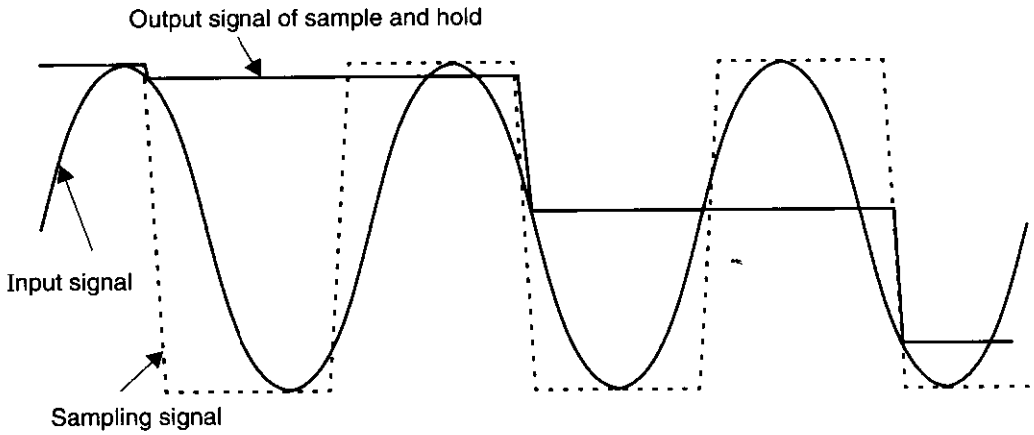


Fig. 8.2 Example waveforms for the test setup of Fig. 8.1.

If a computer is used for analysis, the signal would normally be curve-fitted to a sinusoidal wave at the beat (i.e., difference) frequency. This ideal closest-fit sinusoid would then be subtracted from the measured signal, and the error signal would be analyzed for RMS content and spectral components using a fast-Fourier transform.

It might be mentioned that a very similar test setup can be used for analog-to-digital converters, but now the output of the A/D converter would be loaded into the computer at a sampling rate equal to the beat frequency.

8.2 MOS SAMPLE-AND-HOLD BASICS

Perhaps the simplest sample and hold that can be realized using a CMOS technology is shown in Fig. 8.3. When ϕ_{clk} is high, V' follows V_{in}. When ϕ_{clk} goes low, V' will ideally stay constant from then on, having a value equal to V_{in} at the instance ϕ_{clk}

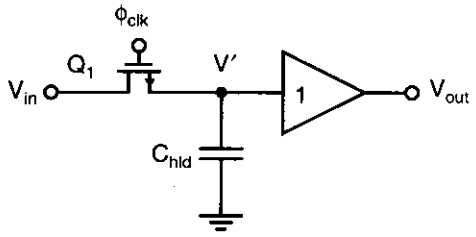


Fig. 8.3 An open-loop track and hold realized using MOS technology.

went low. Unfortunately, V′ will have a negative going hold step at this time caused by the channel charge of Q_1. When Q_1 turns off, its channel charge must flow out from under its gate into its junctions. Since this charge is negative, it will cause the junction voltages to have negative glitches. If one assumes the source impedance at the node V_{in} is very low, then the glitch at this node will be small and have a very short duration. However, the negative charge that goes to the node with C_{hld} connected to it (i.e., node V′) will cause a negative voltage change that is long lasting (until the next time Q_1 turns on again). If clock ϕ_{clk} turns off fast, then the channel charge, Q_{CH}, will flow equally into both junctions [Shieh, 1987] since the channel becomes pinched off at both ends (i.e., next to the junctions) while the charge is flowing out to the two junctions. The charge flowing to the junction labelled V′ is therefore given by

$$\Delta Q_{C_{hld}} = \frac{Q_{CH}}{2} = \frac{C_{ox}WLV_{eff\text{-}1}}{2} \tag{8.1}$$

where $V_{eff\text{-}1}$ is given by

$$V_{eff\text{-}1} = V_{GS1} - V_{tn} = V_{DD} - V_{tn} - V_{in} \tag{8.2}$$

Here, V_{in} is the input voltage at the instance Q_1 turns off. It should be noted here that this result assumes that the clock signal, ϕ_{clk}, goes between V_{DD} and the most negative voltage in the circuit.

The change in the voltage V′ is found by using the relationship $Q = CV$, resulting in

$$\Delta V' = \frac{\Delta Q_{C\text{-}hld}}{C_{hld}} = -\frac{C_{ox}WLV_{eff\text{-}1}}{2C_{hld}} = -\frac{C_{ox}WL(V_{DD} - V_{tn} - V_{in})}{2C_{hld}} \tag{8.3}$$

Notice that $\Delta V'$ is linearly related to V_{in}, which results in a gain error for the overall sample-and-hold circuit. However, more importantly, $\Delta V'$ is also linearly related to V_{tn}, which is nonlinearly related to the input signal, V_{in}, due to variations in the source-substrate voltage (assuming the substrate is tied to one of the voltage rails). This nonlinear relationship with V_{in} results in distortion for the overall sample-and-hold circuit.

There is also an additional change in V′ due to the gate overlap capacitance. Using a derivation similar to that used to find (7.8), we have

$$\Delta V' \cong -\frac{C_{ox}WL_{ov}(V_{DD} - V_{SS})}{C_{hld}} \tag{8.4}$$

where V_{SS} is the most negative voltage in the circuit. This component is usually smaller than that due to the channel charge, and appears simply as an offset since it is signal independent. Therefore, this error component is not typically important since signal-independent offsets can often be removed in most systems. However, it may cause noise problems if care is not taken to ensure that the clock signal, ϕ_{clk}, is relatively noise free. For example, if the clock signal has power-supply noise on it due to being realized with a simple inverter tied to digital power supplies, the power-supply rejection ratio of this circuit might be poor.

EXAMPLE 8.1

Consider the sample and hold of Fig. 8.3 with $C_{hld} = 1$ pF, $C_{ox} = 1.92$ fF/(μm)^2, $V_{tn} = 0.8$ V, and $(W/L)_1 = (5\ \mu m/0.8\ \mu m)$. Assume the power supply voltages are ±2.5 V and the input signal is 1 V peak to peak. Find the hold step for V_{in} equal to 1 V, and then repeat for V_{in} equal to −1 V. Use the estimates for errors at ±1 V to estimate the dc offset.

Solution

At $V_{in} = 1$ V, using (8.3), we find $\Delta V'(1\text{ V}) = -2.69$ mV. At $V_{in} = -1$ V, again using (8.3), we find $\Delta V'(-1\text{ V}) = -10.26$ mV. The average offset is given by

$$V_{offset\text{-}avg} = \frac{\Delta V'(1\text{ V}) + \Delta V'(-1\text{ V})}{2} = -6.48\text{ mV} \tag{8.5}$$

which is a reasonable estimate of the amount of dc offset injected in this example.

There have been a number of changes proposed to minimize the signal-dependent hold step. One approach is to replace the n-channel switch by a CMOS transmission gate, as shown in Fig. 8.4. The idea behind this approach is that if the size of the p-channel transistor is taken the same as the n-channel transistor, then the charge injection due to each transistor will cancel when the transmission gate turns off. This result is somewhat true when V_{in} is in the middle region between the power supplies, assuming the clock waveforms are fast and exactly complementary. Unfortunately, these conditions are seldom possible to achieve in practice. When the finite slopes of the clock waveforms are taken into account, it is seen (as is explained shortly) that the

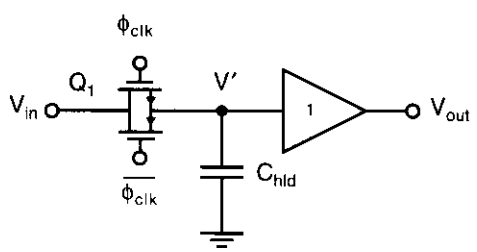


Fig. 8.4 An open-loop track and hold realized using a CMOS transmission gate.

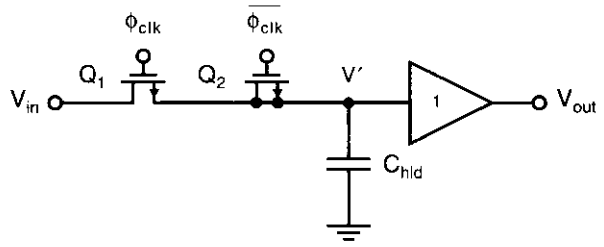


Fig. 8.5 An open-loop track and hold realized using an n-channel switch along with a dummy switch for clock-feedthrough cancellation.

turn-off times of the transistors are signal dependent and this signal dependence causes the n-channel transistor to turn off at different times than the p-channel transistor. Even if we ignore the errors caused by nonperfect clock waveforms, when V_{in} is closer to V_{DD}, the charge from the p-channel transistor is greater than that from the n-channel transistor because of its larger effective gate-source voltage resulting in a positive hold step. The opposite happens when the input signal is closer to the negative power supply. Seldom will these two effects have the same magnitude in practice.

Another modification, often proposed to minimize clock-feedthrough errors, is to add a dummy switch as shown in Fig. 8.5 [McCreary, 1975]. The theory behind this technique is that if the width of Q_2 is taken exactly one-half that of Q_1, and if the clock waveforms are fast, then the charges will cancel. In practice, it is seldom possible to have the clock waveforms change fast enough so that the ideal ratio of widths is exactly one-half. When the ideal ratio is not one-half, it is difficult to make the ratio equal to the optimum required for perfect cancellation. However, when the clock waveforms are fast, this technique usually can minimize the hold pedestal to less than about one-fifth the value it would have without it. For this to be the case, however, it is necessary

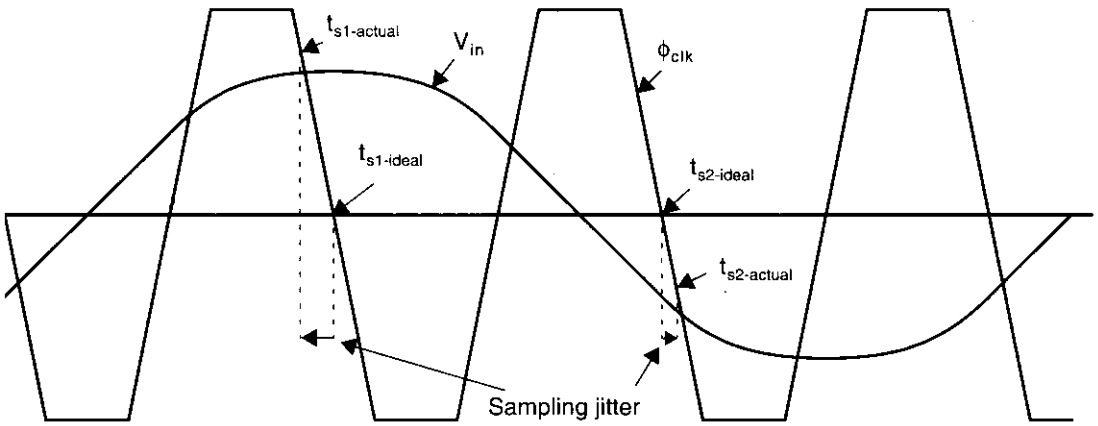


Fig. 8.6 The clock waveforms for V_{in} and ϕ_{clk} used to illustrate how a finite slope for the sampling clock introduces sampling-time jitter.

EXAMPLE 8.2

Consider the S/H circuit of Fig. 8.3, where V_{in} is a 20-MHz band-limited signal with a 2-V_{pp} amplitude. Assume that ϕ_{clk} is a 100-MHz square wave having a peak amplitude of ±2.5 V with linear rise and fall times of 1.5 ns. What is the maximum uncertainty of the sampling time? Assume V_{tn} is 0.8 V.

Solution

First, we note that the slope of ϕ_{clk} is (5 V)/(1.5 ns) = 3.33 V/ns, and the true sampling time is when the clock waveform is 0.8 V greater than the input signal.

For V_{in} equal to 1 V, the sampling transistor will turn off when ϕ_{clk} is 1.8 V, which is (0.7 V)/(3.33 V/ns) = 0.21 ns after the clock first starts to move down.

When V_{in} is –1 V, the sampling time occurs when ϕ_{clk} is –0.2 V, which is 0.81 ns after the clock first starts to move upward.

Therefore, the sampling-time uncertainty is 0.81 – 0.21 = 0.6 ns. Also, assuming the ideal sampling time is 0.75 ns after the clock first starts to move, the sampling jitter is from –0.54 ns to +0.06 ns from the ideal sampling time.

that the clock of Q_2 changes slightly after that of Q_1. This clock arrangement guarantees that the cancelling charge of Q_2 cannot escape through Q_1 while it is still on.

Another source of error for the simple sample and hold of Fig. 8.3 is caused by clock waveforms having finite slopes. To understand this error source consider the waveforms for V_{in} and ϕ_{clk} shown in Fig. 8.6. Assume the ideal sampling time is defined to be the negative-going zero-crossing of ϕ_{clk}. The true sampling time is that when the sampling-clock voltage passes through the value when it is one transistor threshold voltage drop above the input voltage. In other words, transistor Q_1 of Fig. 8.3 turns off when ϕ_{clk} is V_{tn} above V_{in}, as shown in Fig. 8.6. Thus, when V_{in} is above ground, the true sampling time is earlier than the ideal sampling time, whereas when V_{in} is less than 0 V, the true sampling time is late.

A more elaborate sample-and-hold circuit is to include an opamp in a feedback loop, as shown in Fig. 8.7. When the clock, ϕ_{clk}, is high, the complete circuit responds similarly to an opamp in a unity-gain feedback configuration. When ϕ_{clk} goes low, the input voltage at that time is stored on C_{hld}, similarly to a simple sample and hold. By including an opamp in the feedback loop, the input impedance of the sample and hold is greatly increased. Another advantage of this configuration is that even if the unity-gain buffer at the output has an offset voltage, the dc error due to this buffer will be divided by the gain of the input opamp (although the input-offset of the input opamp will remain). Thus, very simple source followers can be used for the output buffer.

A disadvantage of the configuration shown is that the speed of operation can be seriously degraded due to the necessity of guaranteeing that the loop is stable when it

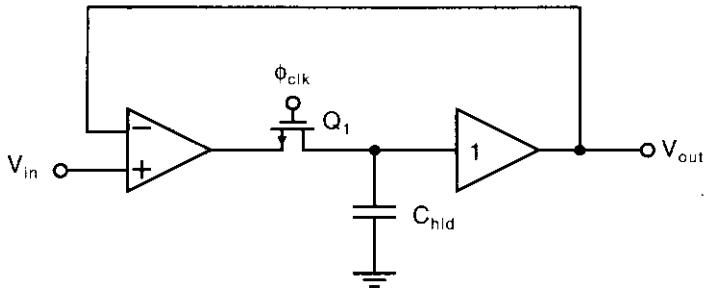


Fig. 8.7 Including an opamp in a feedback loop of a sample and hold to increase the input impedance.

is closed. Another source of speed degradation is that when in hold mode, the opamp is open loop, resulting in its output almost certainly saturating at one of the power-supply voltages. When the sample and hold next goes back into track mode, it will take some time for the opamp output voltage to slew back to its correct closed-loop value. This slewing time can be greatly minimized by adding two additional transistors as shown in Fig. 8.8. During hold mode, switch Q_2 keeps the output of the first opamp close to the voltage it will need to be at when the T/H goes into track mode. It should also be noted that this track-and-hold configuration still has errors due to charge injection from the switch, Q_1, similar to the simple S/H of Fig. 8.3. The errors due to finite clock rise and fall times are also similar.

A similar, but improved, configuration is shown in Fig. 8.9 [Stafford, 1974; Lim, 1991]. In this configuration, the holding capacitor is not going to ground, but rather is placed in the feedback path of a second opamp. This configuration has a number of desirable features. Perhaps the most important of these is due to the fact that, assuming the second opamp has a large gain, the voltages on both sides of switch Q_1 are very nearly signal independent. Thus, when Q_1 turns off, there will still be charge injection to the left side of C_{hld}, which will cause the output voltage of opamp 2 to

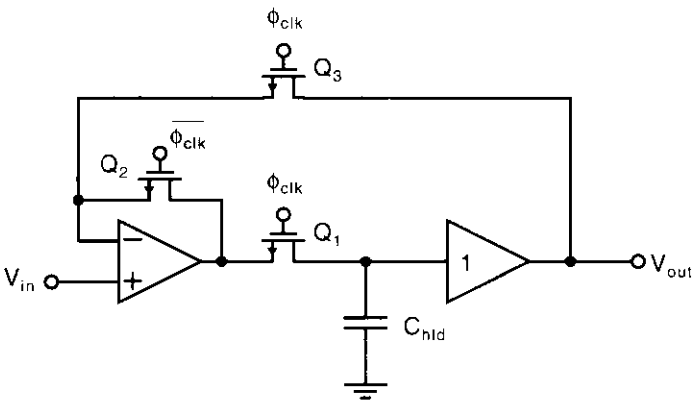


Fig. 8.8 Adding an additional switch to the S/H of Fig. 8.7 to minimize slewing time.

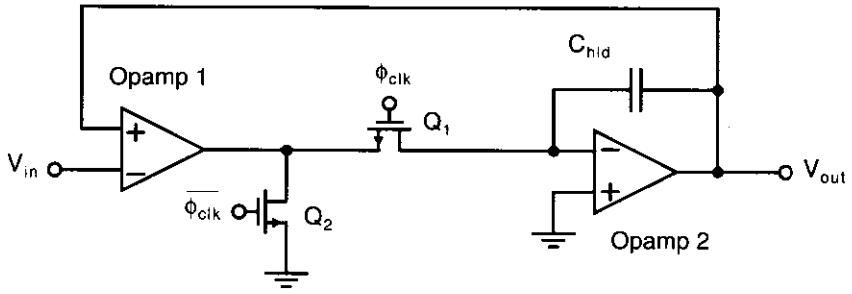


Fig. 8.9 An improved configuration for an S/H as compared to that of Fig. 8.8.

have a positive hold step, *but this hold step will be just a dc offset and will be signal independent*. In other words, the charge injection due to Q_1 will cause some dc offset but no distortion. In addition, the sampling time will not change because of the finite slopes of the sampling-clock waveform.

Another advantage is due to the inclusion of Q_2. This switch grounds the output of the first opamp during hold mode. This grounding keeps the output of the first opamp close to the voltage it must change to when the S/H goes back into track mode. This approach greatly speeds up the time it takes the S/H to return to track mode. The switch also greatly minimizes signal feedthrough when the S/H is in hold mode by grounding the signal path.

A major limitation of this configuration is that the speed will be degraded because of the necessity to guarantee stability in the track mode. This limitation is worsened since there are now two opamps in the loop along with the on resistance of the sampling switch, Q_1, during the closed-loop phase.

Figure 8.10 shows an interesting modification of Fig. 8.9 by including some additional circuitry intended to minimize the hold pedestal and thereby minimize the dc offset [Martin, 1987; Nayebi, 1989]. The basic idea is to match the charge injection into C_{hld} with a similar charge injection into C'_{hld}. Since these capacitors are chosen to have the same size, their voltage changes will match, and the common-

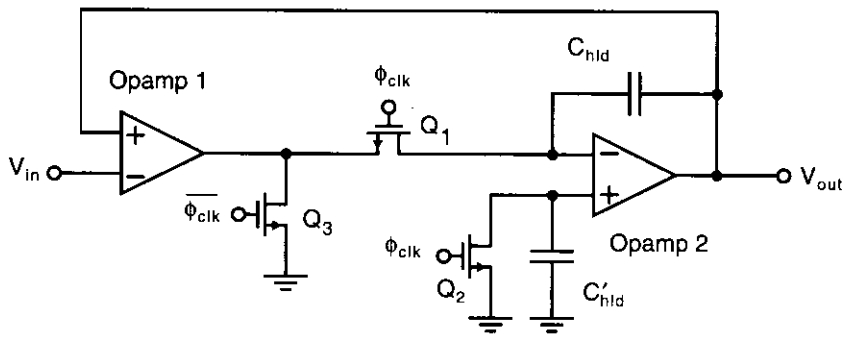


Fig. 8.10 An S/H similar to that of Fig. 8.9, but with clock-feedthrough cancellation circuitry added.

mode rejection of the opamp will eliminate the effects of these voltage changes on the output voltage of the S/H. The major limitation of this approach is a second-order effect caused by a mismatch in impedance levels at the left of Q_1 and the bottom of Q_2. Errors due to this mismatch can be minimized by including small capacitors (0.5 pf to 1 pf) between each node and ground. These extra capacitors help keep these nodes at constant voltages while the clocks are turning off, assuming the clock waveforms are fast. It should be mentioned that the configuration of [Nayebi, 1989] was a fully differential design and is a very reasonable choice for many S/H applications.

8.3 EXAMPLES OF CMOS S/H CIRCUITS

In this section, a number of CMOS S/H circuits are described other than those already mentioned. Unfortunately, the optimum choice for a sample-and-hold circuit is highly dependent on the application's requirements and the technology available. Therefore, choosing the best circuit is nontrivial and a matter of ongoing research. For these reasons, it is difficult to definitively state which configurations are superior or inferior.

Before proceeding, it should be noted that many of these circuits could also be realized in a BiCMOS technology, where a speed advantage would be obtained by increasing the unity-gain frequency of any opamps used. For even higher speeds, a BiCMOS circuit can make use of a bipolar diode bridge, as described in Section 8.4.

Another structure for an S/H circuit is shown in Fig. 8.11 [Ishikawa, 1988]. This configuration is intended to operate at higher speeds, assuming a high-speed opamp capable of driving resistive loads is available. Unfortunately, in CMOS technologies, such opamps are difficult to obtain. Furthermore, the required output buffer would not only limit speed, but could also limit the signal swing. In bipolar and BiCMOS technologies, this configuration could be a very viable alternative. When in track mode, Q_1 is on and Q_2 is off, resulting in the sample and hold acting as an inverting low-pass circuit having a –3-dB frequency given by $\omega_{-3\,dB} = 1/(RC)$. When Q_1 turns off, the output voltage will remain constant from then on. Since the junctions of Q_1 are always at voltages very close to ground, the clock feedthrough of this sample and

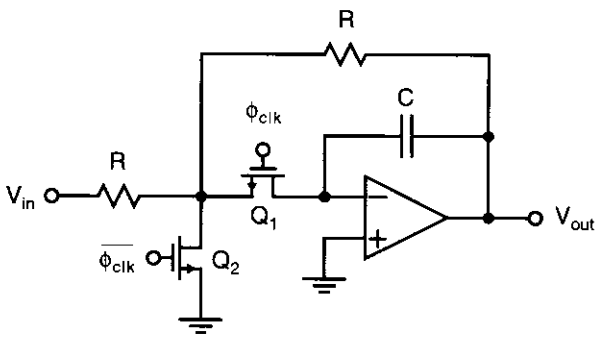


Fig. 8.11 An inverting track and hold.

hold is signal independent. Also, finite clock rise and fall times do not make the sampling time a function of the signal, either. The function of Q_2 is to minimize signal feedthrough when in hold mode and to keep the common node of the resistive network close to the voltage required when the S/H goes back into track mode. In the implementation described in [Ishikawa, 1988], an additional small bypass capacitor was included in parallel to the input resistor. It was reported, and supported by analysis, that this capacitor improved the speed of the S/H.

Another alternative is shown in Fig. 8.12 [Sone, 1993]. This track and hold places the opamp into a unity-gain follower during track mode. Also, the positive input terminal of the opamp is connected to V_{in} at this time. When the T/H goes into hold mode, the input signal is stored across C_1, since Q_1 is turned off. At the same time, transistor Q_2 is also turned off. Ideally, the charge feedthrough from Q_1, although signal dependent, will be matched by the charge feedthrough from Q_2, since both are at the same voltage and have the same clock waveforms. For this to be true, the opamp must have a low-impedance output.[2] Furthermore, the signal dependence of the clock signals can be minimized by having clock signals that change above and below the input signal by fixed amounts. As will be seen in the next section, this is not too difficult to realize using diode clamps in a bipolar or BiCMOS technology. In a CMOS technology, it is more difficult. Regardless, the topology of Fig. 8.12 is attractive for high-speed CMOS applications that are not too demanding.

Yet another S/H architecture is shown in Fig. 8.13 [Lim, 1991]. Shown in Fig. 8.14(*a*) is the circuit configuration when the S/H is in sample mode. During this mode, the opamp is being reset, and both capacitors are connected between the input voltage and the virtual input of the opamp. Thus the total capacitance that needs to be charged or discharged during this mode is $C_1 + C_2$. During hold mode, the configuration is as shown in Fig. 8.14(*b*). During this mode, the effective hold capacitor is the

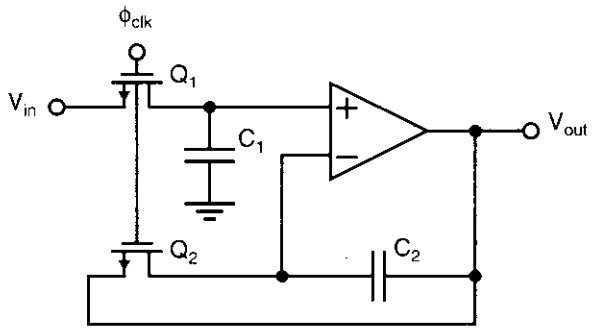


Fig. 8.12 A simple noninverting sample and hold with clock-feedthrough cancellation.

2. This can be partially realized using a high-output impedance OTA by having a load capacitor connected to ground, but without having a resistor included in series with the load capacitor (as would be required if lead compensation was desired).

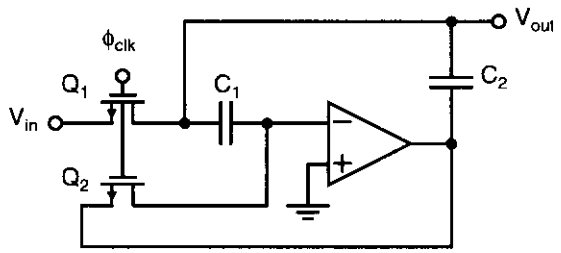


Fig. 8.13 An open-loop architecture but with a Miller holding capacitor.

Miller capacitor given by

$$C_{hld\text{-}eff} = (1 + A)\left(\frac{C_1 C_2}{C_1 + C_2}\right) \tag{8.6}$$

which is typically much larger than the capacitance that needs to be charged during the sampling mode. This allows smaller capacitances and therefore smaller switches to be used than would otherwise be the case. Since the voltage changes at the output

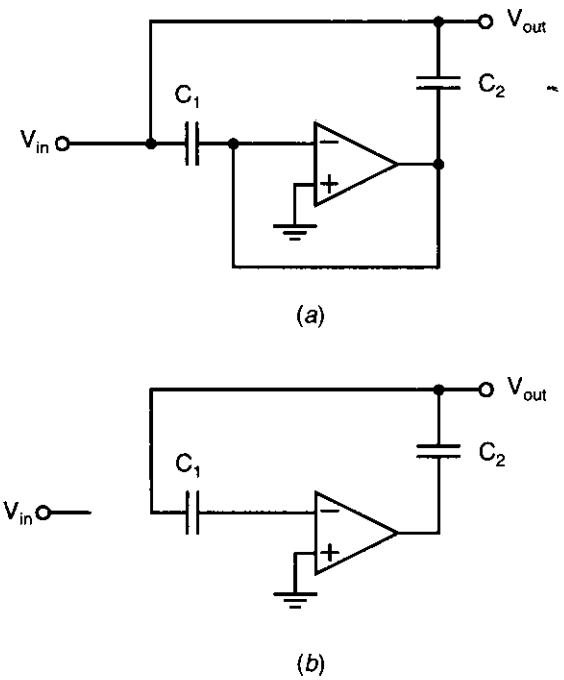


Fig. 8.14 The circuit configurations of the S/H of Fig. 8.13 during (*a*) sample mode and (*b*) hold mode.

of the amplifier are very small, it is easy to design the amplifier for very high speed. The sampling switch, Q_1, does inject signal-dependent charge as in other open-loop architectures, but again this is minimized by the large size of the Miller hold capacitance, especially if Q_2 is turned off slightly before Q_1.

At lower frequencies, there are a number of sample-and-hold architectures based on switched-capacitor technology that are often used. These S/Hs tend to be quite accurate but not necessarily fast. A simple example is shown in Fig. 8.15. Note how similar this S/H is to the S/H of Fig. 8.13. During ϕ_1, capacitor C_H is connected between the input signal source and the inverting input of the opamp. At the same time, the inverting input and the output of the opamp are connected together. This causes the voltages at both of these nodes to be equal to the input-offset voltage of the opamp, V_{off}. Thus, C_H is charged up to $V_{in} - V_{off}$. Next, during ϕ_2, the opamp is taken out of reset mode, and the capacitor C_H is connected between the opamp output and its inverting input. This will cause the output voltage to be equal to V_{in}, irrespective of the input-offset voltage of the opamp. Note that this circuit is an example of a sample and hold that is not thought of as a track-and-hold circuit. Specifically, during the sample phase, the opamp output voltage will be very close to 0 V rather than tracking the input voltage. This places a requirement on the opamp to have a very large slew rate, or the speed is seriously degraded. Also, obviously, the opamp output is invalid during ϕ_1, the sample phase.

An interesting variation somewhat similar to the S/Hs of Figs. 8.13 and 8.15 adds two unity-gain buffers and two more switches to help improve accuracy. The S/H is shown in Fig. 8.16 [Real, 1991]. During sampling, all switches are on except Q_2. This connects C_1 and C_2 together and charges them to the input voltage. During this time, the input impedance is quite large due to the inclusion of buffer B_1. At the same time, the opamp is being reset and the positive terminal of the opamp is charged to 0 V. Next, Q_4 and Q_5 are turned off, and shortly thereafter Q_1 and Q_3 are turned off. Finally, Q_2 is turned on. This configures the circuit as shown in Fig. 8.17. Note the similarity between this configuration and that of Fig. 8.14(*b*). The unity-gain feedback holds the output during this phase, and also the output impedance of the S/H is very low. Because Q_4 and Q_5 turn off slightly before Q_1 and Q_3, their clock feedthrough is not only signal

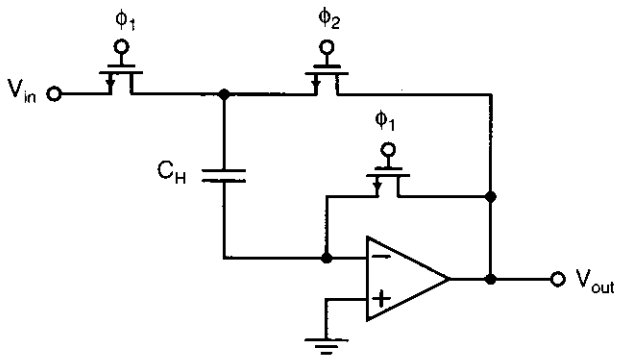


Fig. 8.15 A simple switched-capacitor S/H.

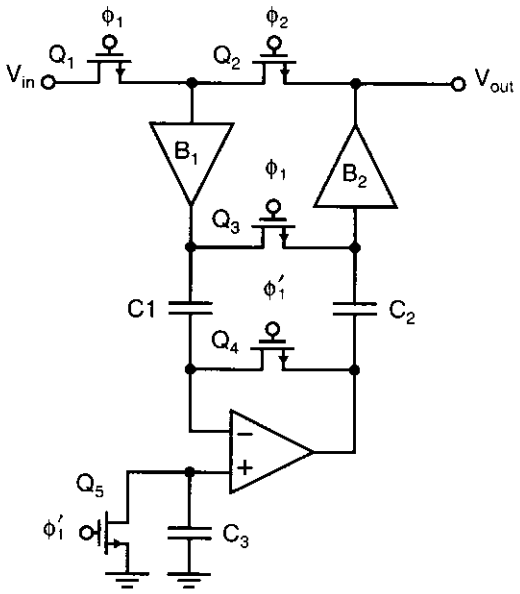


Fig. 8.16 A recycling S/H.

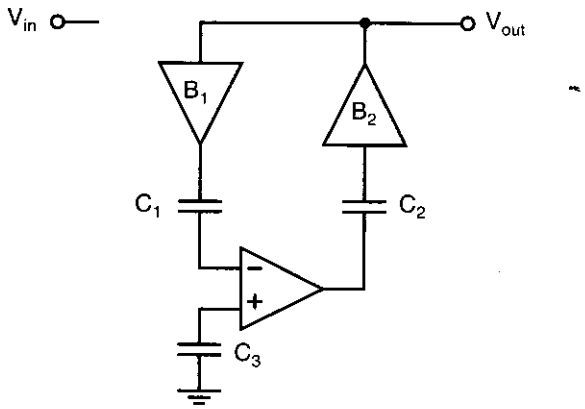


Fig. 8.17 The S/H of Fig. 8.16 when in hold mode.

independent but largely cancels due to the common-mode rejection of the input stage of the amplifier [Martin, 1987]. The charge injection of Q_1 and Q_2 does not affect the output voltage. The charge injection of Q_3 is signal dependent and does affect the output voltage, but its effect is minimized by the loop gain similar to the S/H of Fig. 8.13.

An interesting variation on the S/Hs of Figs. 8.10 and 8.15 is the S/H shown in Fig. 8.18 from [Gatti, 1992]. This T/H has an output that is always valid and incorporates a number of features. During sample mode, the input-offset voltage of the first opamp is stored across C_{OF}. At the same time, C_S is sampling the input voltage, and the second opamp is holding the previously-sampled input voltage. During the next

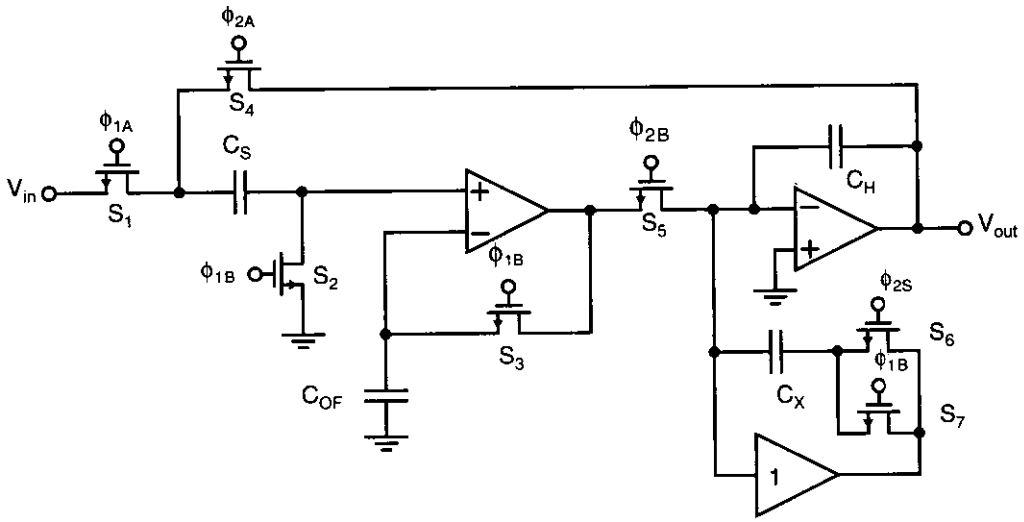


Fig. 8.18 A switched-capacitor S/H.

phase, the input-offset voltage of the first opamp is eliminated, and C_S is connected to the output while the feedback loop is enabled. This arrangement causes the output voltage to be equal to the just-sampled input voltage. The clock feedthrough of switch S_2 is cancelled by the clock feedthrough of switch S_3. The clock feedthrough of switch S_5 is cancelled by the clock feedthrough of switch S_6 and the added buffer network. The other switches ideally do not cause appreciable errors due to clock feedthrough. The details concerning the operation of this T/H and the required clocking waveforms are left for the interested reader to consult [Gatti, 1992].

Yet another example of a switched-capacitor S/H is shown in Fig. 8.19 [Sooch, 1991]. This circuit combines a sample and hold with a low-pass filter and was used to convert a signal from the sampled-data domain to the continuous-time domain at

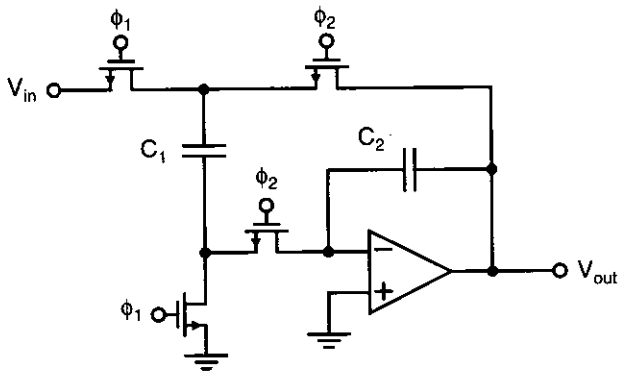


Fig. 8.19 A switched-capacitor sample and hold and low-pass filter.

the output of a high-quality audio digital-to-analog converter based on oversampling techniques. The low-pass filtering was used to help convert from a single-bit high-frequency signal to a decimated lower-frequency multi-bit signal. During ϕ_1, C_1 is connected between the input voltage and ground. Next, during ϕ_2, it is connected between the output and the inverting input of the opamp. At this time, its charge is shared with the charge being stored across C_2, which came from previous samples. For low-frequency signals, the output voltage will equal the input voltage in the steady state. Higher frequency changes in the input signal will be low-pass filtered. For C_2 greater than C_1 by at least a few times, it can be shown using switched-capacitor analysis techniques [Martin, 1980] that the –3-dB frequency of the low-pass filter is approximately given by

$$f_{-3\,dB} \cong \frac{1}{2\pi}\frac{C_1}{C_2}f_{clk} \tag{8.7}$$

where f_{clk} is the clock frequency. While this example does not eliminate the effects of opamp finite-input voltage offsets, unlike the previous two examples, it does have the advantage that its output is always valid.

The switched-capacitor sample-hold circuits just shown (except for that of Fig. 8.18) do have dc offsets due to clock feedthrough from the switches connected to the inverting inputs of the opamps. However, these offsets are largely signal independent assuming the opamp has a reasonable gain. Also, it is possible to minimize these offsets by including a clock-feedthrough cancellation network connected to the positive input of the opamp, similar to what is described in [Martin, 1987]. Alternatively, fully differential sample and holds can be used, which also helps minimize the effects of clock feedthrough.

8.4 BIPOLAR AND BICMOS SAMPLE AND HOLDS

In this section, bipolar and BiCMOS sample-and-hold circuits are described. It should be noted that BiCMOS sample-and-hold circuits are often realized using the CMOS techniques described above. Here, we look at BiCMOS circuits more closely related to their bipolar counterparts.

Most of the early integrated bipolar sample and holds were based on using a *diode-bridge* switch, as shown in Fig. 8.20 [Erdi, 1978]. In track mode the bias current, I_B, is turned on and evenly divides between D_1 and D_2, as well as between D_3 and D_4. This current division results in a low-impedance path between the input and the output with a small-signal impedance of r_d, where

$$r_d = \frac{V_T}{I_{D1}} = \frac{V_T}{I_B/2} \tag{8.8}$$

In hold mode, both current sources labelled I_B are turned off, leaving the hold capacitor, C_{hld}, open circuited.

A more practical realization of a diode-bridge track and hold is shown in Fig. 8.21 [Matsuzawa, 1990]. During track mode, V_{trk} is at a higher voltage than V_{hld},

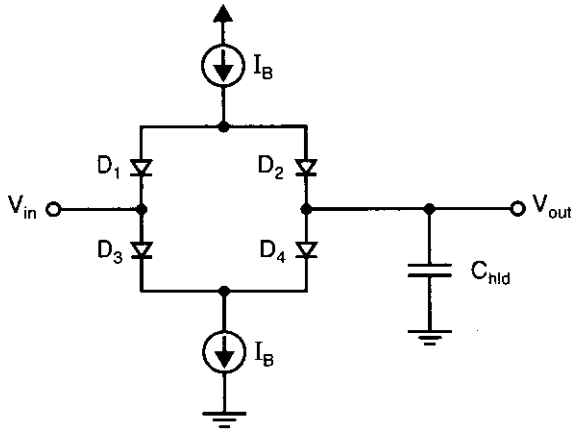


Fig. 8.20 A bipolar track and hold based on using a diode bridge.

and Q_2 will be on and conducting $2I_B$. Half of this current comes from the current source connected to the node V_2. The other half comes from the current source connected to node V_1 after going through the diode bridge. Thus, during track mode, the diode bridge is low impedance, and the node V_3 will track the input signal. The output voltage will also track this node through the unity-gain output buffer. Also, during this phase, the diodes D_5 and D_6 are reverse biased.

When the track and hold is placed in hold mode, Q_2 is turned off and Q_1 is turned on. Since Q_2 is turned off, the current from the source connected to the node V_2 now

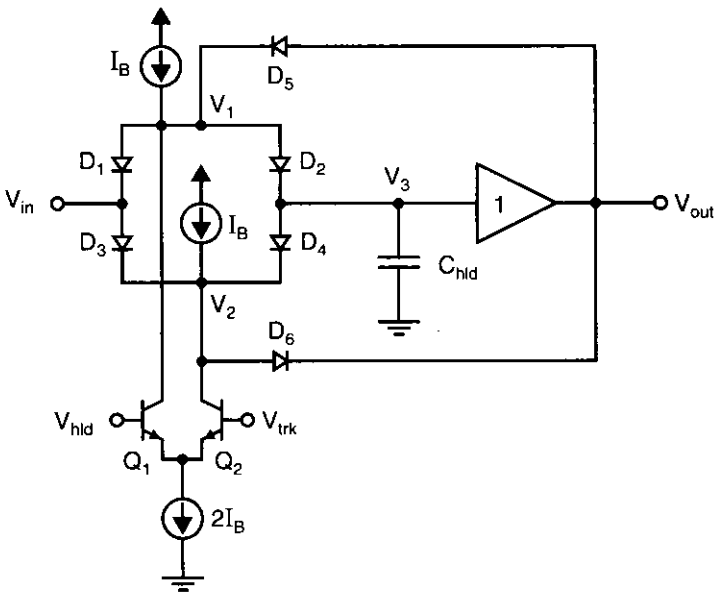


Fig. 8.21 An improved example of a diode-bridge track and hold.

flows through the diode D_6, turning it on. This causes V_2 to be one diode drop above V_{out}, which causes diodes D_3 and D_4 to become reverse biased. At the same time, Q_1 will be conducting current $2I_B$. Half of this will come from the current source connected to node V_1. The other half comes from V_{out} through diode D_5, causing it to become forward biased. Therefore, V_1 will be one diode drop below V_{out}, and diodes D_1 and D_2 will be reverse biased. Thus, all the diodes in the diode bridge are reverse biased, and the node V_3 is disconnected from the input signal.

The circuit of Fig. 8.21 has a number of advantages compared to the simple circuit of Fig. 8.20. Perhaps the most important of these is that the clock feedthrough is signal independent. This independence occurs because when the diode bridge turns off, the voltage changes of nodes V_1 and V_2 are from a voltage closely equal to V_{in}, to a voltage one diode drop below V_{in}, and a voltage one diode drop above V_{in}, respectively, regardless of the value of V_{in}. Thus, the charge from turning the diode bridge off, and changing the reverse-bias voltage of the diodes in the bridge, is signal independent. Furthermore, the charge from D_1 and D_2 will (to a first-order degree) cancel the charge from D_3 and D_4, assuming fast clock waveforms, which also minimizes the effects of charge injection. It should be mentioned that in many implementations, the diodes would all be Schottky diodes, which don't have minority carrier charge storage when they are on, and, thus, turn off faster than regular diodes and have smaller hold steps. A second advantage of Fig. 8.21 is that the sample-time uncertainty caused by the finite slope of the clock waveforms is greatly minimized. Finally, a third advantage of Fig. 8.21 is that when in hold mode, the signal feedthrough is substantially smaller. When the simple circuit of Fig. 8.20 is in hold mode, the diodes are turned off but are floating. The input signal is then capacitively coupled through the junction capacitance of these reverse-biased diodes to the hold capacitor. The magnitude of this signal feedthrough is easily calculated using the capacitor-divider formula. This signal feedthrough is minimized in the improved circuit of Fig. 8.21, because during hold mode, nodes V_1 and V_2 are connected to V_{out} through low-impedance paths consisting of conducting diodes D_5 and D_6, respectively. This effectively shields the node V_3 from the input signal during hold mode.

In the BiCMOS realization presented in [Matsuzawa, 1990], the input transistors to the unity-gain buffer were p-channel MOS transistors that minimized the droop on the hold capacitor during hold-mode, which would normally be caused by finite-based currents of bipolar input transistors.

It should be noted in Fig. 8.21 that the maximum input-signal excursions during hold mode are limited to less than two diode drops above or below the input signal voltage at the time the track and hold went into hold mode. Otherwise, one of the diodes D_1 or D_3 will become forward biased, which will tend to clamp the input signal. For high-speed track and holds, this input amplitude restriction is not usually a serious limitation as peak signals are usually limited to be less than one volt. Furthermore, the input signal range can be increased by replacing each of D_5 and D_6 with two series diodes. This would increase the maximum allowable signal-swing excursion to three diode drops.

One of the major limitations of bipolar S/Hs is a droop in the voltage being stored across a capacitor during hold mode, caused by the finite base currents of bipolar tran-

sistors. One of the major ways of minimizing this droop is to use fully differential approaches where the droop is the same in both paths, and the differential signal is, to a first-order approximation, unaffected. An example of a fully differential diode-bridge-based T/H is given in [Colleran, 1993]. In this example, the current sources were realized using resistors, and additional circuitry was also included to minimize errors introduced by these resistors.

An interesting BiCMOS S/H is shown in Fig. 8.22 [Wakayama, 1992]. This S/H uses bipolar switches that appear similar to the diode bridge switches, but operate differently. Note that the direction of diodes D_2 and D_4 have been reversed compared to the circuit of Fig. 8.20. When V_{trk1} is greater than V_{hld1}, then Q_3 will be conducting $3I_B$. I_B of this will come from M_5 through Q_1, I_B of this will come from M_6, and I_B of this will come from M_7 through D_2 and D_1. Since both Q_1 and D_1 are conducting, V_{out1} will equal V_{in}. Diodes D_3 and D_4 are reverse biased and V_{out2} is isolated from V_{in}. The ratios of the currents in M_2, M_3, and M_4 are accurately determined by the feedback loop including M_1, M_2, M_5, and the unity-gain buffer. When V_{trk1} is less than V_{hld1}, then Q_4 will be conducting $3I_B$. This will cause Q_1, D_1, and D_2 to turn off and Q_2, D_3, and D_4 to turn on. In this phase, V_{out1} will be isolated from V_{in}, and V_{out2} will track V_{in}. Notice that the input is buffered from the holding capacitors by emitter followers (either Q_1 or Q_2) and that the load current on the input source is constant (and equal to the base current of the emitter followers). Also, when one output is in track mode, the other is in hold mode. This arrangement can possibly be used to effectively double a data rate. Finally, as is explained in [Wakayama, 1992], during slewing the current available to charge or discharge the holding capacitors is dynamically increased to $3I_B$ rather than the quiescent I_B.

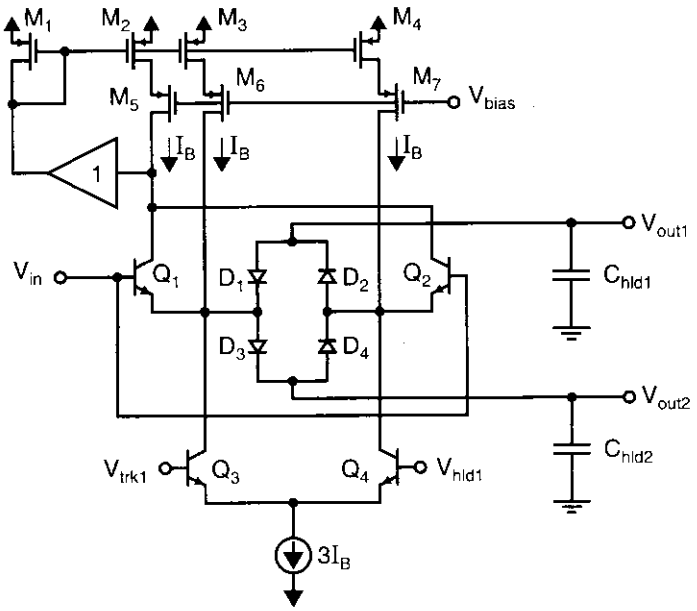


Fig. 8.22 A BiCMOS sample and hold.

An alternate BiCMOS S/H is described in [Sone, 1993], which makes use of the basic architecture shown in Fig. 8.12, except the switches are realized using bipolar switches. There have been a number of other alternative bipolar and BiCMOS track and holds that have been reported in the literature. Some alternative and interesting BiCMOS examples include [Fernandes, 1989; Robertson, 1990; and Real, 1991]. Some alternative and interesting bipolar examples include [Moraveji, 1991; Petschacher, 1990; and Vorenkamp, 1992]. The interested reader is referred to the applicable references.

8.5 BANDGAP VOLTAGE REFERENCE BASICS

Another important analog building block, especially in data acquisition systems, is a voltage reference. Ideally, this block will supply a fixed dc voltage of known amplitude that does not change with temperature. There have been a number of approaches that have been taken to realize voltage references in integrated circuits. These include

1. Making use of a zener diode that breaks down at a known voltage when reverse biased.
2. Making use of the difference in the threshold voltage between an enhancement transistor and a depletion transistor.
3. Cancelling the negative temperature dependence of a pn junction with a positive temperature dependence from a PTAT (proportional-to-absolute-temperature) circuit.

The first approach is not popular nowadays because the breakdown voltage of a zener diode is typically larger than the power supplies used in modern circuits. The second approach cannot be used in most CMOS circuits because depletion transistors are not typically available. In addition, although it can be used to make quite stable references, the actual value of the reference is difficult to determine accurately because of the process sensitivity of the difference between the threshold voltage of an enhancement device and a depletion device. For these reasons, the first two approaches are not covered here. Rather, the last approach, which is currently the most popular for both bipolar and CMOS technologies, will be discussed. Voltage references based on the last approach are commonly called "bandgap" voltage references for reasons that will become apparent shortly.

Bandgap Voltage Reference

As just mentioned, a bandgap voltage reference is based on subtracting the voltage of a forward-biased diode (or base-emitter junction) having a negative temperature coefficient from a voltage proportional to absolute temperature (PTAT). As we shall see, this PTAT voltage is realized by amplifying the voltage difference of two forward-biased base-emitter (or diode) junctions. A bandgap voltage reference system is shown symbolically in Fig. 8.23.

A forward-biased base-emitter junction of a bipolar transistor has an I-V relationship given by

$$I_C = I_S e^{qV_{BE}/kT} \tag{8.9}$$

where I_S is the transistor scale current and, although not shown, has a strong dependence on temperature.

Writing the base-emitter voltage as a function of collector current and temperature, it can be shown that [Brugler, 1967; Tsividis, 1980]

$$V_{BE} = V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\frac{T}{T_0} + \frac{mkT}{q}\ln\left(\frac{T_0}{T}\right) + \frac{kT}{q}\ln\left(\frac{J_C}{J_{C0}}\right) \tag{8.10}$$

Here, V_{G0} is the bandgap voltage of silicon extrapolated to 0 °K (approximately 1.206 V), k is Boltzmann's constant, and m is a temperature constant approximately equal to 2.3. Also, J_C and T are the collector current density and temperature, respectively, while the subscript 0 designates an appropriate quantity at a reference temperature, T_0. Specifically, J_{C0} is the collector current density at the reference temperature, T_0, whereas J_C is the collector current density at the true temperature, T. Also, V_{BE0} is the junction voltage at the reference temperature, T_0, whereas V_{BE} is the base-emitter junction voltage at the true temperature, T. Note that the junction current is related to the junction current density according to the relationship

$$I_C = A_E J_C \tag{8.11}$$

where A_E is the effective area of the base-emitter junction.

For I_C constant, V_{BE} will have approximately a −2 mV/°K temperature dependence around room temperature. This negative temperature dependence is cancelled by a PTAT temperature dependence of the amplified difference of two base-emitter junctions biased at fixed but different current densities. Using (8.10), it is seen that if there are two base-emitter junctions biased at currents J_2 and J_1, then the difference in their junction voltages is given by

$$\Delta V_{BE} = V_2 - V_1 = \frac{kT}{q}\ln\left(\frac{J_2}{J_1}\right) \tag{8.12}$$

Thus, the difference in the junction voltages is proportional to absolute temperature. This proportionality is quite accurate and holds even when the collector currents are temperature dependent, as long as their ratio remains fixed.

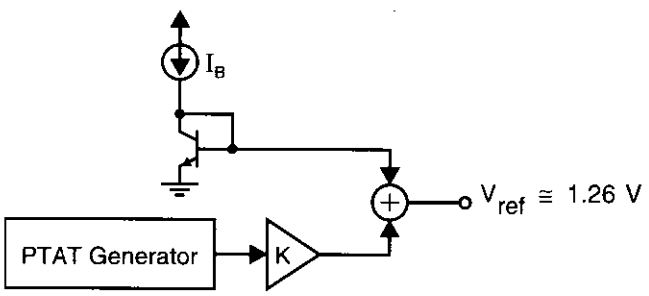


Fig. 8.23 A simplified circuit of a bandgap voltage reference.

EXAMPLE 8.3

Assume two transistors are biased at a current-density ratio of 10:1 at $T = 300\ ^\circ K$. What is the difference in their base-emitter voltages and what is its temperature dependence?

Solution

Using (8.12), we have

$$\Delta V_{BE} = \frac{kT}{q} \ln\left(\frac{J_2}{J_1}\right) = \frac{1.38 \times 10^{-23}(300)}{1.602 \times 10^{-19}} \ln(10) = 59.5 \text{ mV} \tag{8.13}$$

Since this voltage is proportional to absolute temperature, after a 1 °K temperature increase, the voltage difference will be

$$\Delta V_{BE} = 59.5 \text{ mV} \frac{301}{300} = 59.7 \text{ mV} \tag{8.14}$$

Thus, the voltage dependence is 59.5 mV/300 °K or 0.198 mV/°K. Since the temperature dependence of a single V_{BE} is −2 mV/°K, if it is desired to cancel the temperature dependence of a single V_{BE}, then ΔV_{BE} should be amplified by about a factor of 10, as explained next.

It will be seen shortly that when realizing a bandgap voltage reference, although the output voltage is temperature independent, the junction currents turn out to be proportional to absolute temperature (assuming the resistors used are temperature independent). Thus, to simplify derivations, we will first assume the junction currents are proportional to absolute temperature. Later, it will be verified that this proportionality relationship is true when circuit realizations are described. We therefore first assume

$$\frac{J_i}{J_{i0}} = \frac{T}{T_0} \tag{8.15}$$

where J_i is the current density of the collector current of the ith transistor, whereas J_{i0} is the same current density at the reference temperature.

Now, assume that the difference between two base-emitter voltages is multiplied by a factor of K and added to the base-emitter voltage of the junction with the larger current density. Using (8.12) and (8.15) along with (8.10), we have

$$\begin{aligned} V_{ref} &= V_{BE2} + K\Delta V_{BE} \\ &= V_{G0} + \frac{T}{T_0}(V_{BE0\text{-}2} - V_{G0}) + (m-1)\frac{kT}{q}\ln\left(\frac{T_0}{T}\right) + K\frac{kT}{q}\ln\left(\frac{J_2}{J_1}\right) \end{aligned} \tag{8.16}$$

Equation (8.16) is the fundamental equation giving the relationship between the output voltage of a bandgap voltage reference and temperature. If we want this relation-

ship to be zero at a particular temperature, we can differentiate (8.16) with respect to temperature and set the derivative to zero at the desired reference temperature. From (8.16), we have

$$\frac{\partial V_{ref}}{\partial T} = \frac{1}{T_0}(V_{BE0\text{-}2} - V_{G0}) + K\frac{k}{q}\ln\left(\frac{J_2}{J_1}\right) + (m-1)\frac{k}{q}\ln\left(\frac{T_0}{T} - 1\right) \tag{8.17}$$

Setting (8.17) equal to zero at $T = T_0$, we see that for zero temperature dependence at the reference temperature, we need

$$V_{BE0\text{-}2} + K\frac{kT_0}{q}\ln\left(\frac{J_2}{J_1}\right) = V_{G0} + (m-1)\frac{kT_0}{q} \tag{8.18}$$

The left side of (8.18) is the output voltage V_{ref} at $T = T_0$ from (8.16). Thus for zero temperature dependence at $T = T_0$, we need

$$V_{ref\text{-}0} = V_{G0} + (m-1)\frac{kT_0}{q} \tag{8.19}$$

For the special case of $T_0 = 300\ ^\circ\text{K}$ and $m = 2.3$, (8.19) implies that

$$V_{ref\text{-}0} = 1.24\ \text{V} \tag{8.20}$$

for zero temperature dependence. Notice that this value is independent of the current densities chosen. Thus, if a larger current density is chosen, then K must be taken appropriately smaller to achieve the correct reference output voltage. In many integrated voltage references, this correct output voltage will be achieved by trimming at the time the wafer is being tested. From (8.18), the required value for K is

$$K = \frac{V_{G0} + (m-1)\dfrac{kT_0}{q} - V_{BE0\text{-}2}}{\dfrac{kT_0}{q}\ln\left(\dfrac{J_2}{J_1}\right)} = \frac{1.24 - V_{BE0\text{-}2}}{0.0258\ln\left(\dfrac{J_2}{J_1}\right)} \tag{8.21}$$

at 300 °K.

The reason for the name of the bandgap voltage should now be apparent. Specifically, for zero temperature dependence, the output of a bandgap voltage reference is given by the bandgap voltage plus a small correction term to account for second-order effects.

The output voltage of the reference for temperatures different from the reference is found after back-substituting (8.18) and (8.19) into (8.16). After some manipulations, the result is

$$V_{ref} = V_{G0} + (m-1)\frac{kT}{q}\left[1 + \ln\left(\frac{T_0}{T}\right)\right] \tag{8.22}$$

and

$$\frac{\partial V_{ref}}{\partial T} = (m-1)\frac{k}{q}\ln\left(\frac{T_0}{T}\right) \tag{8.23}$$

These equations can be used to estimate the temperature dependence at temperatures different from the reference temperature. In the next section, a practical bipolar realization of a bandgap reference will be described.

EXAMPLE 8.4

Estimate the temperature dependence at 0 °C for a bandgap voltage reference that was designed to have zero temperature dependence at 20 °C. Present the result as ppm/°K.

Solution

Recalling that 0 °K corresponds to −273 °C, we can write $T_0 = 293$ °K and $T = 273$ °K. Substituting these values into (8.23), we have

$$\frac{\partial V_{ref}}{\partial T} = (2.3-1)\frac{1.38\times10^{-23}}{1.6\times10^{-19}}\ln\left(\frac{293}{273}\right) = 8\ \mu V/°K \tag{8.24}$$

For a reference voltage of 1.24 V, a dependency of 8 μV/°K results in

$$\frac{8\ \mu V/°K}{1.24\ V} = 6.5\times10^{-6}\ \text{parts}/°K = 6.5\ \text{ppm}/°K \tag{8.25}$$

where ppm represents parts per million. It should be mentioned here that practical effects result in voltage references with typically 4 to 10 times larger values than this small amount of temperature dependency. It should also be noted that the ideal first-order temperature of this bandgap voltage circuit is 0 ppm/°K at the reference temperature of 20 °C.

8.6 CIRCUITS FOR BANDGAP REFERENCES

Bipolar Bandgap References

A voltage reference originally proposed in [Brokaw,1974] has been the basis for many bipolar bandgap references. A simplified schematic of the circuit is shown in Fig. 8.24. The amplifier in the feedback loop keeps the collector voltages of Q_1 and Q_2 equal. Since $R_3 = R_4$, this guarantees that both transistors have the same collector currents and collector-emitter voltages. Also, notice that the emitter area of Q_1 has been taken eight times larger than the emitter area of Q_2. Therefore, Q_2 has eight times the current density of Q_1, resulting in

$$\frac{J_2}{J_1} = 8 \tag{8.26}$$

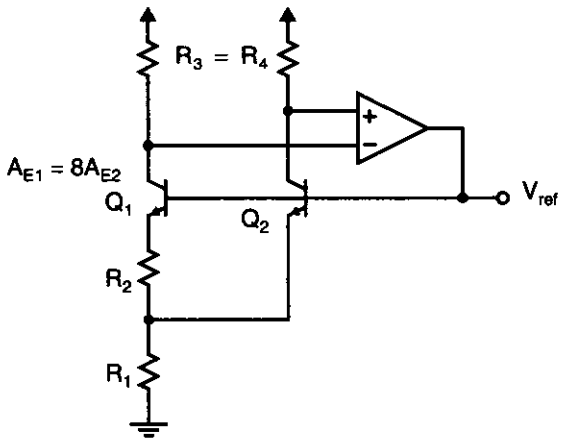


Fig. 8.24 A simplified schematic of a bipolar bandgap voltage reference.

We have for the circuit

$$V_{ref} = V_{BE2} + V_{R1} \tag{8.27}$$

Also

$$\begin{aligned} V_{R1} &= I_{R1}R_1 \\ &= 2I_{R2}R_1 \end{aligned} \tag{8.28}$$

But

$$I_{R2} = \frac{V_{R2}}{R_2} = \frac{V_{BE2} - V_{BE1}}{R_2} = \frac{\Delta V_{BE}}{R_2} \tag{8.29}$$

Substituting (8.28) and (8.29) into (8.27) gives

$$V_{ref} = V_{BE2} + \frac{2R_1}{R_2}\,\Delta V_{BE} \tag{8.30}$$

which is of the form desired to realize a bandgap reference. It is immediately recognizable that

$$K = \frac{2R_1}{R_2} \tag{8.31}$$

Assuming $V_{BE2\text{-}0} = 0.65$ V, from (8.21)

$$\frac{R_1}{R_2} = \frac{1}{2} \times \frac{1.24 - 0.65}{0.0258 \times \ln(8)} = 5.5 \tag{8.32}$$

In an integrated implementation, R_1 or R_2 would be trimmed while monitoring V_{ref} to force it equal to the desired reference voltage. Furthermore, the optimum value for

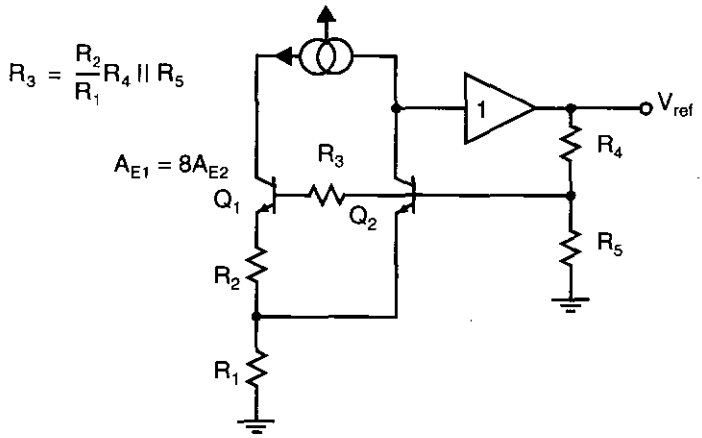


Fig. 8.25 A bipolar bandgap with output voltages greater than 1.24 V.

this voltage might be determined empirically during the prototype phase of the design cycle.

Notice also, from (8.12) and (8.29), we have

$$I_{E1} = I_{E2} = I_{R2} = \frac{\Delta V_{BE}}{R_2} = \frac{\frac{kT}{q} \ln\left(\frac{J_2}{J_1}\right)}{R_2} \tag{8.33}$$

implying that all currents are proportional to absolute temperature (assuming that resistor R_2 is temperature independent). Thus, as assumed earlier, all currents are indeed PTAT. It is worth mentioning here that PTAT currents are often used to bias many bipolar circuits, as they result in transistor transconductances being independent of temperature. This transconductance independence has the desirable feature that circuit speed is relatively independent of temperature, but, unfortunately, has the undesirable feature that the circuit power dissipation goes up considerably at high temperatures, which makes it more difficult to dissipate the heat.

In applications where it is desirable to have reference voltages larger than 1.24 V, a modified bandgap reference as shown in Fig. 8.25 can be used. It is not difficult to show that the output voltage is now given by

$$V_{ref\text{-}0} = \left(1 + \frac{R_4}{R_5}\right)\left[V_{G0} + (m-1)\frac{kT_0}{q}\right] \cong \left(1 + \frac{R_4}{R_5}\right)1.24 \text{ V} \tag{8.34}$$

Resistor R_3 has been added to cancel the effects of the finite base currents going through R_4 and should be chosen according to the formula in the figure. The interested reader is referred to [Brokaw, 1974] for additional details concerning this realization.

CMOS Bandgap References

The most popular method for realizing CMOS voltage references also makes use of a bandgap voltage reference despite the fact that *independent* bipolar transistors are not available. These CMOS circuits rely on using what are commonly called *well transistors*. These devices are vertical bipolar transistors that use wells as their bases and the substrate as their collectors. In an n-well process (the most common modern process), these vertical bipolar transistors are pnp types with their collectors connected to ground, as shown in Fig. 8.26(*a*). In a p-well process, they would be npn transistors with their collectors connected to the positive power supply, as shown in Fig. 8.26(*b*). These transistors have reasonable current gains, but their main limitation is the series base resistance, which can be high due to the large lateral dimensions between the base contact and the effective emitter region. To minimize errors due to this base resistance, the maximum collector currents through the transistors are usually constrained to be less than 0.1 mA. It is possible to use these transistors to implement bandgap voltage references using configurations similar to those shown in Fig. 8.27(*a*) for n-well processes [Kujik, 1973] or Fig. 8.27(*b*) for p-well processes [Ye, 1982].

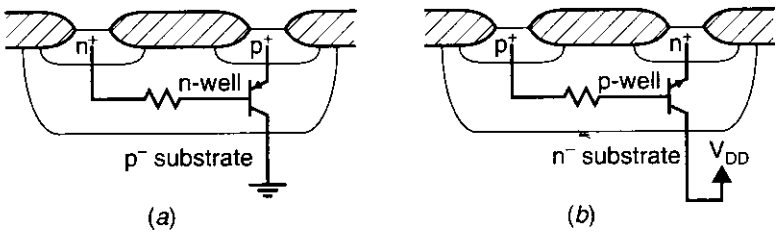


Fig. 8.26 Vertical CMOS well transistors realized in (*a*) an n-well process and (*b*) a p-well process.

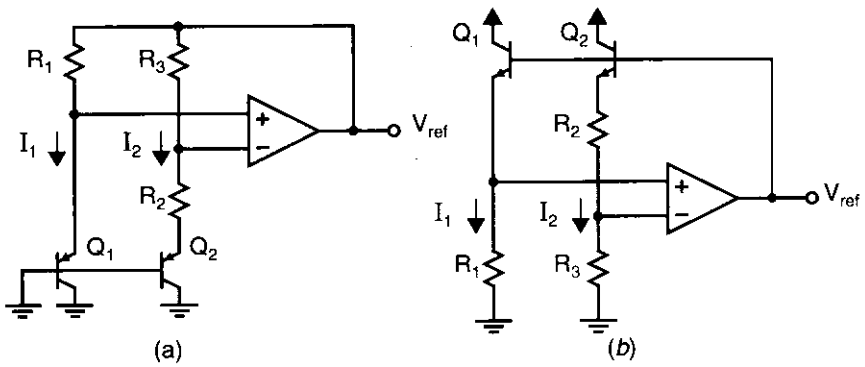


Fig. 8.27 Bandgap voltage references implemented with well transistors in (a) an n-well CMOS process, and (b) a p-well CMOS process.

With respect to the n-well implementation of Fig. 8.27(*a*), we have

$$V_{ref} = V_{EB1} + V_{R1} \tag{8.35}$$

Also, assuming the opamp has large gain and that its input terminals are at the same voltage, then

$$V_{R2} = V_{EB1} - V_{EB2} = \Delta V_{EB} \tag{8.36}$$

Now, since the current through R_3 is the same as the current through R_2, we have

$$V_{R3} = \frac{R_3}{R_2} V_{R2} = \frac{R_3}{R_2} \Delta V_{EB} \tag{8.37}$$

using (8.36). The opamp feedback also makes the voltage across R_1 equal to the voltage across R_3. Using this fact and substituting (8.37) into (8.35) results in

$$V_{ref} = V_{EB1} + \frac{R_3}{R_2} \Delta V_{EB} \tag{8.38}$$

which is in the required form to realize a bandgap reference. In integrated realizations of this reference, the bipolar transistors are often taken the same size, and the different current-densities are realized by taking R_3 greater than R_1, which causes I_1 to be larger than I_2. In this case, we would have

$$\frac{J_1}{J_2} = \frac{R_3}{R_1} \tag{8.39}$$

since R_1 and R_3 have the same voltage across them. Also, recalling from (8.12) that

$$\Delta V_{EB} = V_{EB1} - V_{EB2} = \frac{kT}{q} \ln\left(\frac{J_1}{J_2}\right) \tag{8.40}$$

and using (8.39) in (8.38) gives

$$V_{ref} = V_{EB1} + \frac{R_3}{R_2} \frac{kT}{q} \ln\left(\frac{R_3}{R_1}\right) \tag{8.41}$$

It is immediately recognizable that

$$K = \frac{R_3}{R_2} \tag{8.42}$$

EXAMPLE 8.5

Find the resistances of a bandgap voltage reference based on Fig. 8.27(*a*), where $I_1 = 80\ \mu A$, $I_2 = 8\ \mu A$, and $V_{EB1\text{-}0} = 0.65$ V at $T = 300$ °K.

Solution

Recalling from (8.20) that

$$V_{ref\text{-}0} = 1.24 \text{ V} \tag{8.43}$$

therefore, from (8.35), we require

$$V_{R1} = V_{ref\text{-}0} - V_{EB1\text{-}0} = 0.59 \text{ V} \tag{8.44}$$

Also, since $V_{R3} = V_{R1}$, we have

$$R_3 = \frac{V_{R3}}{I_2} = \frac{0.59 \text{ V}}{8 \text{ } \mu\text{A}} = 73.8 \text{ k}\Omega \tag{8.45}$$

and

$$R_1 = R_3 \frac{I_2}{I_1} = 7.38 \text{ k}\Omega \tag{8.46}$$

Now, recalling from (8.22) that

$$K = \frac{1.24 - 0.65 \text{ V}}{0.0258 \times \ln(10)} = 9.93 \tag{8.47}$$

therefore

$$R_2 = \frac{R_3}{K} = 7.43 \text{ k}\Omega \tag{8.48}$$

It is of interest to note here that using (8.40) and noting that $J_1/J_2 = I_1/I_2$ (since the sizes of Q_1 and Q_2 are assumed to be the same), we find that

$$\Delta V_{EB} = \frac{kT_0}{q} \ln\left(\frac{I_1}{I_2}\right) = 59 \text{ mV} \tag{8.49}$$

gives the temperature dependence value of 198 mV/°K, as found in Example 8.3, which requires approximately a gain of 10 to cancel temperature dependency (actually 9.93 in this case).

The design equations for a voltage reference that is suitable for p-well processes and shown in Fig. 8.27(*b*) are essentially identical to those just given for the n-well reference.

In CMOS realizations of the references just described, the large value resistors are often realized by well resistors. Unfortunately, these resistors have a temperature dependence approximately given by [Michejda, 1984]

$$R(T) = R_0 \frac{T^\eta}{T_0^\eta} \tag{8.50}$$

where $\eta = 2.2$. The errors caused by this temperature dependence can be eliminated by offsetting $V_{ref\text{-}0}$ slightly positive from the value given by (8.19) to

$$V_{ref\text{-}0} = V_{G0} + (m + \eta - 1)\frac{kT_0}{q} \tag{8.51}$$

Assuming the effects of the temperature coefficient of the resistors have been minimized, the next major source of error is often due to the input-offset voltage of the opamp [Michejda, 1984]. This results in an error term in the equation for ΔV_{BE} that is roughly equal to K times the input-offset voltage of the opamp. For example, a 1 mV offset error that is temperature independent causes a temperature coefficient (TC), error approximately given by [Song, 1983]

$$TC_{error} \cong 26 \text{ ppm}/^\circ\text{C} \tag{8.52}$$

One means of eliminating this source of error is to use switched-capacitor (SC) amplifiers that have input-offset compensation circuits [Song, 1983]. One possible SC-based voltage reference is shown in Fig. 8.28, where it makes use of an amplifier described in [Martin, 1987]. The amplifier shown results in a circuit having its output valid at all times and is less sensitive to finite opamp gain. A detailed explanation of how the amplifier shown in Fig. 8.28 operates is deferred until Chapter 10, where switched-capacitor circuits are discussed.

Assuming errors due to the input-offset voltage of the opamp have been minimized, there is still an inherent temperature dependence of the bandgap voltage reference, as we saw in (8.23). In addition, a further temperature dependence occurs because V_{G0} varies slightly with temperature (which has been ignored in the above analysis). Together, these two error sources limit the best achievable temperature coefficient to about 25 ppm/°K. Minimizing these second-order effects is beyond the scope of this book, but the interested reader is referred to [Palmer, 1981; Meijer, 1982; Song, 1983] to see examples of how errors due to second-order effects have been minimized.

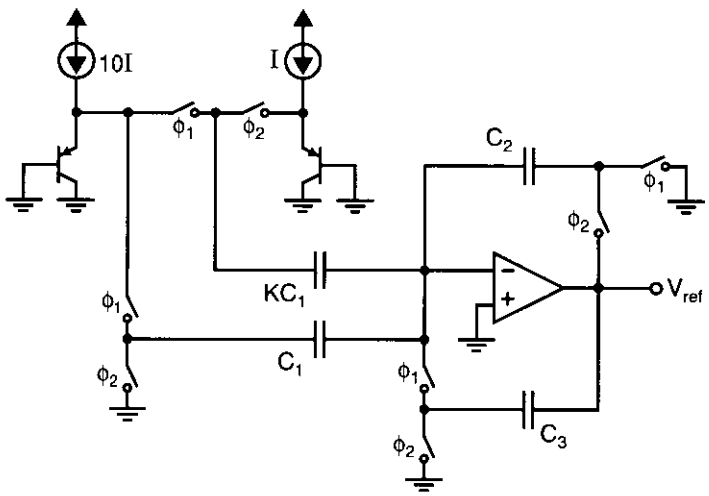


Fig. 8.28 An SC-based voltage reference that is insensitive to opamp input-offset voltages.

An alternative realization of a CMOS bandgap reference was reported in [Degrauwe, 1985], where lateral npn well transistors were used. Also, in [Tzanateas, 1979] a voltage reference was reported that was based on a realized PTAT voltage from the difference of the source-gate voltages of two MOS transistors biased in weak inversion. The interested reader can consult the references for details on these circuits.

8.7 TRANSLINEAR GAIN CELL

An important analog building block for bipolar circuits is the translinear gain cell[3] [Gilbert, 1968a; Gilbert, 1990]. These gain cells are useful when building circuits requiring varying gain, such as in adjustable continuous-time filters and voltage-controlled amplifiers. They are also useful in realizing four-quadrant analog multipliers, as will be seen in the next section.

A translinear gain cell is shown in Fig. 8.29. It has differential inputs and outputs that are current signals. The first stage simply consists of pn junction loads, which in this case are realized by the base-emitter junctions of Q_1 and Q_2. The second stage is a differential pair. To analyze this cell, we recall the relationship between the base-emitter voltage and collector current,

$$I_C = I_S e^{(v_{be}/V_T)} \quad \text{or} \quad v_{be} = V_T \ln\left(\frac{I_C}{I_S}\right) \tag{8.53}$$

Thus, ignoring the base currents of Q_3 and Q_4, we see that the voltage at the emitter of Q_1 is given by

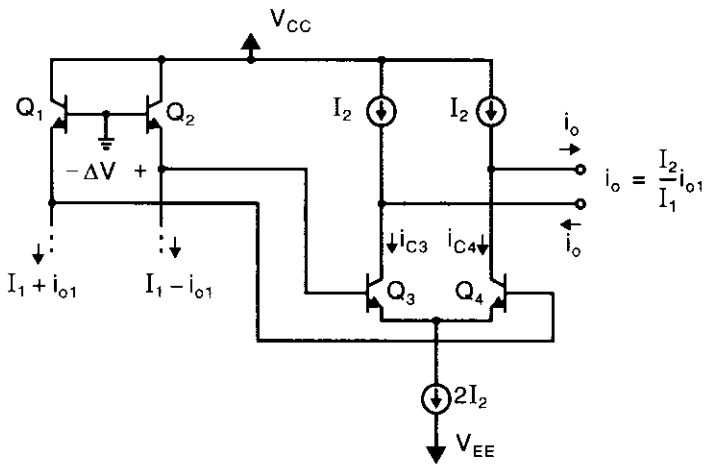


Fig. 8.29 A four-transistor gain cell. The output current, i_o, is a scaled version of i_{o1}.

3. These four transistor gain cells are also commonly called two-quadrant multipliers or Gilbert gain cells.

$$v_{e1} = (-V_T)\ln\left(\frac{I_1 + i_{o1}}{I_{S1}/\alpha}\right) \tag{8.54}$$

where $\alpha = \beta/(\beta + 1)$. For Q_2, we have

$$v_{e2} = (-V_T)\ln\left(\frac{I_1 - i_{o1}}{I_{S2}/\alpha}\right) \tag{8.55}$$

Now, assuming Q_1 and Q_2 are matched such that $I_{S1} = I_{S2}$, and defining ΔV to be the difference between v_{e2} and v_{e1}, we have

$$\Delta V \equiv v_{e2} - v_{e1} = V_T \ln\left(\frac{I_1 + i_{o1}}{I_1 - i_{o1}}\right) \tag{8.56}$$

Note that this voltage difference, ΔV, does not depend on the scale current, I_S.

To analyze the current output from the differential pair of Q_3 and Q_4, we recall from Section 3.10 that the large-signal emitter currents through a differential pair are given by

$$i_{E3} = \frac{2I_2}{1 + e^{(-\Delta V)/V_T}} \quad \text{and} \quad i_{E4} = \frac{2I_2}{1 + e^{(\Delta V)/V_T}} \tag{8.57}$$

Therefore, the collector current, i_{C3}, is equal to

$$i_{C3} = \alpha i_{E3} = \frac{\alpha 2I_2}{1 + \left(\dfrac{I_1 - i_{o1}}{I_1 + i_{o1}}\right)} = \alpha I_2 + \alpha\frac{I_2}{I_1} i_{o1} \tag{8.58}$$

and for $\alpha = 1$, we have

$$i_{C3} = I_2 + \frac{I_2}{I_1} i_{o1} \tag{8.59}$$

In a similar manner, i_{C4} is equal to

$$i_{C4} = I_2 - \frac{I_2}{I_1} i_{o1} \tag{8.60}$$

Finally, the output current, i_o, is given by

$$i_o = i_{C3} - I_2 = I_2 - i_{C4} = \frac{I_2}{I_1} i_{o1} \tag{8.61}$$

In other words, the output current is equal to a scaled version of the input current where the scaling factor is determined by the ratio of two dc bias currents, I_2 and I_1.

An important point to note here is that not only is the difference between i_{C3} and i_{C4} linearly related to the input current, *but also each of* i_{C3} *and* i_{C4} *is also linearly related* (except for the dc bias current). This result is important since it implies that

even if the difference between these two currents is not taken precisely, it does not affect the linearity of the overall circuit. Furthermore, note that the gain and linearity are not dependent on any transistor parameters such as β or I_S. However, one should be aware that there are mechanisms that will create distortion in a gain cell, such as mismatches between transistors and the occurrence of linear resistances in the pairs Q_1, Q_2 and Q_3, Q_4.

EXAMPLE 8.6

Consider the gain cell shown in Fig. 8.29 where I_1 is fixed to a bias current of 200 μA, while I_2 varies such that the gain changes from 0.5 to 4. What are the extreme values of I_2 needed? Also, what is the maximum peak current that should be used for i_{o1}, assuming all transistors should remain in the active region with at least 20 μA of emitter current?

Solution

Making use of (8.61), when a gain of 0.5 is needed, I_2 should be one-half of I_1, which is 100 μA. When a gain of 4 is needed, I_2 should be four times that of I_1, which is 800 μA. Therefore, the extreme values of I_2 are 100 μA and 800 μA.

The maximum peak current of i_{o1} is found by noting that the emitter currents of either transistors Q_1 or Q_2 should not go below 20 μA. Since they are biased with 200 μA each, the peak current of i_{o1} should be less than 180 μA. Note that if I_1 were varied while I_2 remained fixed, the maximum peak level of i_{o1} would change as I_1 was varied.

8.8 TRANSLINEAR MULTIPLIER

A translinear multiplier[4] is one approach for realizing a four-quadrant multiplier circuit. Multiplier circuits are useful in a variety of applications, such as frequency modulators in communication systems or phase detectors in phase-locked loops. A translinear multiplier can be realized using two translinear gain cells, as seen in the six-transistor translinear multiplier shown in Fig. 8.30 [Gilbert, 1968b]. We can analyze this multiplier by making use of the results for the gain-cell circuit just discussed preceding. Note that the preceding multiplier circuit is effectively two gain-cell circuits with their output signals cross-coupled. Specifically, one gain cell consists of the two differential pairs Q_1, Q_2 and Q_5, Q_6, while the other gain cell consists of the differential pair Q_3, Q_4 and makes use of the same voltage generating pair, Q_5, Q_6. Thus, recognizing the similarity of this circuit with that of Fig. 8.29 and making use of (8.59) and (8.60), we find the following four collector currents:

4. A translinear multiplier is also commonly called a Gilbert multiplier or an analog multiplier.

$$i_{C1} = \frac{(I_2 + i_2)}{2} + \frac{(I_2 + i_2)}{2I_1} i_1 \tag{8.62}$$

$$i_{C2} = \frac{(I_2 + i_2)}{2} - \frac{(I_2 + i_2)}{2I_1} i_1 \tag{8.63}$$

$$i_{C3} = \frac{(I_2 - i_2)}{2} + \frac{(I_2 - i_2)}{2I_1} i_1 \tag{8.64}$$

$$i_{C4} = \frac{(I_2 - i_2)}{2} - \frac{(I_2 - i_2)}{2I_1} i_1 \tag{8.65}$$

Note here that we have made the substitutions of signal currents, $I_2 \pm i_2$, in what was simply a bias current of $2I_2$ in Fig. 8.29. In addition, once again these four collector currents are linear in i_2 if i_1 remains a constant value and linear in i_1 if i_2 remains constant. To find the output currents, we combine collector currents to obtain

$$I_2 + i_o \equiv i_{C1} + i_{C4} = I_2 + \frac{i_1 i_2}{I_1} \tag{8.66}$$

and

$$I_2 - i_o \equiv i_{C2} + i_{C3} = I_2 - \frac{i_1 i_2}{I_1} \tag{8.67}$$

and taking the difference of these two equations results in

$$i_o = \frac{i_1 i_2}{I_1} \tag{8.68}$$

Thus, we see that the output signals are linear with respect to i_2 and can be scaled by the ratio i_1/I_1. Also, note that i_1 can be made positive or negative (as it is the amount of the bias current deviation from I_1), and so the output current, i_o, is a scaled positive or negative version of i_2. A similar result occurs with respect to the output signal and i_1. Thus, this multiplier is called a four-quadrant multiplier. Recall that a gain cell can only scale i_1 with respect to the ratio of two positive bias currents and is therefore only a two-quadrant multiplier.

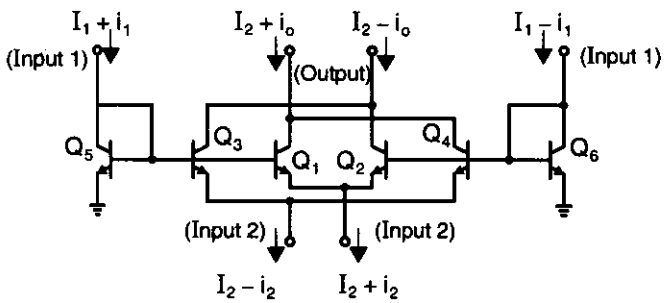


Fig. 8.30 A six-transistor translinear multiplier.

If voltage inputs, rather than current inputs, are desired, then one can precede the multiplier with voltage-to-current converters. The simplest of these are differential pairs having emitter degeneration. More linear, but more complicated, voltage-to-current converters include local feedback to eliminate distortions due to the modulation of the base-emitter voltages. Examples of these circuits are given in Chapter 15, where continuous-time filters are discussed.

EXAMPLE 8.7

Consider the translinear multiplier circuit shown in Fig. 8.30, where I_1 and I_2 are fixed bias currents of 100 μA and 200 μA, respectively. If i_1 is the gain-controlling current, what is that maximum gain for i_o/i_2, assuming all transistors should remain in the active region with at least 20 μA of emitter current?

Solution

To maintain 20 μA of current through Q_5 or Q_6, the magnitude of i_1 should be limited to 80 μA. As seen from (8.68), such a limit results in the peak gains being ±0.8. A gain of zero would occur if collector currents of Q_5 and Q_6 were equal.

Note that this multiplier circuit cannot get gain from i_2 to i_o, while gain is possible if the input signal is taken to be i_1.

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8.10 PROBLEMS

Unless otherwise stated, assume the following:

- n-channel MOS transistors:
  $\mu_n C_{ox} = 92\ \mu A/V^2$
  $V_{tn} = 0.8\ V$
  $\gamma = 0.5\ V^{1/2}$
  $r_{ds}\ (\Omega) = 8{,}000\ L\ (\mu m)/I_D\ (mA)$ in active region,
  $C_j = 2.4 \times 10^{-4}\ pF/(\mu m)^2$
  $C_{j\text{-}sw} = 2.0 \times 10^{-4}\ pF/\mu m$
  $C_{ox} = 1.9 \times 10^{-3}\ pF/(\mu m)^2$
  $C_{gs(overlap)} = C_{gd(overlap)} = 2.0 \times 10^{-4}\ pF/\mu m$
- p-channel MOS transistors:
  $\mu_p C_{ox} = 30\ \mu A/V^2$
  $V_{tp} = -0.9\ V$
  $\gamma = 0.8\ V^{1/2}$
  $r_{ds}\ (\Omega) = 12{,}000\ L\ (\mu m)/I_D\ (mA)$ in active region,
  $C_j = 4.5 \times 10^{-4}\ pF/(\mu m)^2$
  $C_{j\text{-}sw} = 2.5 \times 10^{-4}\ pF/\mu m$
  $C_{ox} = 1.9 \times 10^{-3}\ pF/(\mu m)^2$
  $C_{gs(overlap)} = C_{gd(overlap)} = 2.0 \times 10^{-4}\ pF/\mu m$

8.1 Using the transient analysis of SPICE with a sinusoidal input signal of 2 V peak-to-peak, find the offset, gain, and linearity error of the simple S/H of Fig. 8.3.

8.2 For the T/H of Fig. 8.4, assume V_{in} is a 20-MHz sinusoid with a 2 $V_{p\text{-}p}$ amplitude. Also assume that ϕ_{clk} is a 100-MHz square wave having a peak amplitude of ±2.5 V with rise and fall times of 1.5 ns. What is the maximum time difference between the turn-off times of the n-channel and p-channel transistors? Ignore the body effect.

8.3 The T/H of Fig. 8.5 has transistors that are 10 μm/0.8 μm and a 1-pF hold capacitor. Assume the clock waveforms are fast enough that the channel charge of the transistors is evenly distributed between the two junctions. Compare the final hold pedestal between the case when the dummy switch turns on substantially before the sampling switch turns off, and the case when it turns on substantially after the sampling switch.

8.4 Assume the second stage of the S/H of Fig. 8.10 has a gain of –30 and a unity-gain frequency of 100 MHz. Also assume the input signal is a 5-MHz sinusoid with a 2 $V_{p\text{-}p}$ amplitude and the clock signals are at 20 MHz and go between +2.5 V and –2.5 V, with rise and fall times of 1.5 ns. What is the sampling time uncertainty?

8.5 Assume the S/H of Fig. 8.12 is being realized in a BiCMOS process. This means that diodes and BJT transistors are available. Design a clock-driver circuit so that the clock voltages go from two diode drops above the input voltage (in track mode) to two diode drops below the output voltage (in hold mode).

8.6 Assume the opamp in the S/H of Fig. 8.15 has a finite gain of A_0. Derive the output voltage in terms of V_{in} and A_0 during hold mode (i.e., when ϕ_2 is high).

8.7 Derive the output voltage of the S/H of Fig. 8.19 at the end of ϕ_2 in terms of the input voltage at the end of ϕ_1, the output voltage at the end of ϕ_1 from the previous period, and the capacitor ratio C_1/C_2. Take the z-transform of this difference equation, and substitute $z = e^{j\omega T}$ to find the frequency-domain transfer function of the S/H. Making the assumption that $e^{j\omega T} \equiv 1 + j\omega T$ for $\omega << (1/T) = f_{clk}$, where f_{clk} is the sampling frequency, show that

$$f_{-3\,dB} \cong \frac{1}{2\pi}\frac{C_1}{C_2} f_{clk}$$

8.8 Assume the S/H of Fig. 8.21 has each of D_5 and D_6 replaced by two series diodes. Show the voltages at all nodes for the cases of sampling a 1 V input and a –1 V input for before as well as after track mode.

8.9 Assume two transistors in a PTAT are biased at a current-density ratio of 8 : 1 at $T = 320$ °K. What is the difference in their base-emitter voltages and what is its temperature dependence?

8.10 Assuming $V_{BE0\text{-}2} = 0.65$ V, what is the value required for K in order to get zero temperature dependence at $T = 320$ °K for a current-density ratio of 8:1 in the two transistors?

8.11 Prove equations (8.22) and (8.23).

8.12 Find values for the bipolar reference of Fig. 8.25, where $V_{ref} = 2.5$ V.

8.13 Prove that equation (8.41) holds for the voltage reference of Fig. 8.27(*b*).

8.14 Consider the gain cell shown in Fig. 8.29, where I_2 is fixed to a bias current of 200 μA while I_1 varies such that the gain changes from 0.5 to 4. What are the extreme values of I_1 needed? Also, what is the maximum peak current that should be used for i_{o1}, assuming all transistors should remain in the active region with at least 20 μA of emitter current?

8.15 Consider the translinear multiplier shown in Fig. 8.30, where $I_1 = 100$ μA, $I_2 = 200$ μA, and i_1 is set such that the gain $i_o/i_2 = 0.5$. If a common-mode noise signal of 5 μA appears on I_1, what is the size of the output signal due to that noise signal? Repeat for a common-mode noise signal on I_2.

8.16 Repeat Problem 8.15 when the β's of the transistors' worst-case mismatch is 5 percent.

8.17 Design a four-quadrant translinear multiplier having differential voltage-current conversion stages based on emitter degeneration at both inputs and a differential voltage output. All transistors should be biased at 0.2 mA. Design the multiplier so that when both differential inputs are 1 V the differential output should be 1 V. Assume a 5 V power supply is available.

CHAPTER

9 Discrete-Time Signals

A basic understanding of discrete-time signal processing is essential in the design of most modern analog systems. For example, discrete-time signal processing is heavily used in the design and analysis of oversampling analog-to-digital (A/D) and digital-to-analog (D/A) converters used in digital audio and instrumentation applications. Also, a discrete-time filtering technique known as switched-capacitor filtering is probably the most popular approach for realizing fully integrated analog filters. Switched-capacitor filters are in the class of analog filters since voltage levels in these filters remain continuous. In other words, switched-capacitor filters operate and are analyzed using discrete-time steps but involve no A/D or D/A converters. This chapter presents some basic concepts of discrete-time signals and filters.

9.1 OVERVIEW OF SOME SIGNAL SPECTRA

Consider the spectra of sampled and continuous-time signals in the block diagram systems shown in Fig. 9.1, where it is assumed that the continuous-time signal, $x_c(t)$, is band limited through the use of an anti-aliasing filter (not shown). *DSP* refers to *Discrete-time signal processing*, which may be accomplished using fully digital processing or discrete-time analog circuits such as switched-capacitor filters. Some

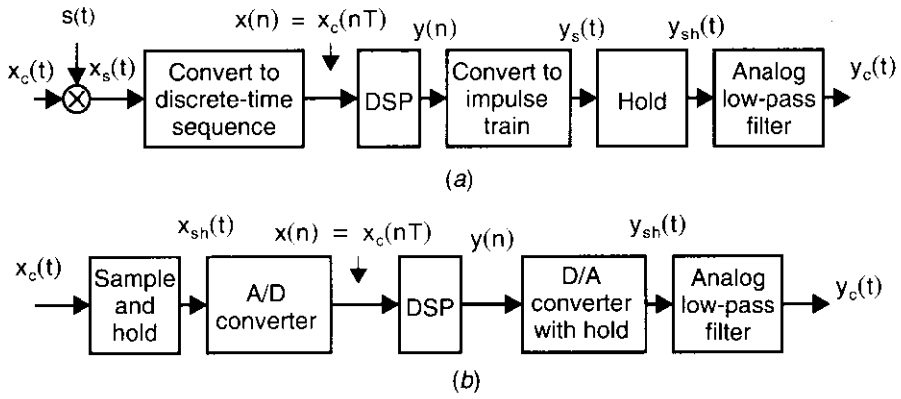


Fig. 9.1 Performing DSP on analog signals. (*a*) Conceptual realization, and (*b*) typical physical realization.

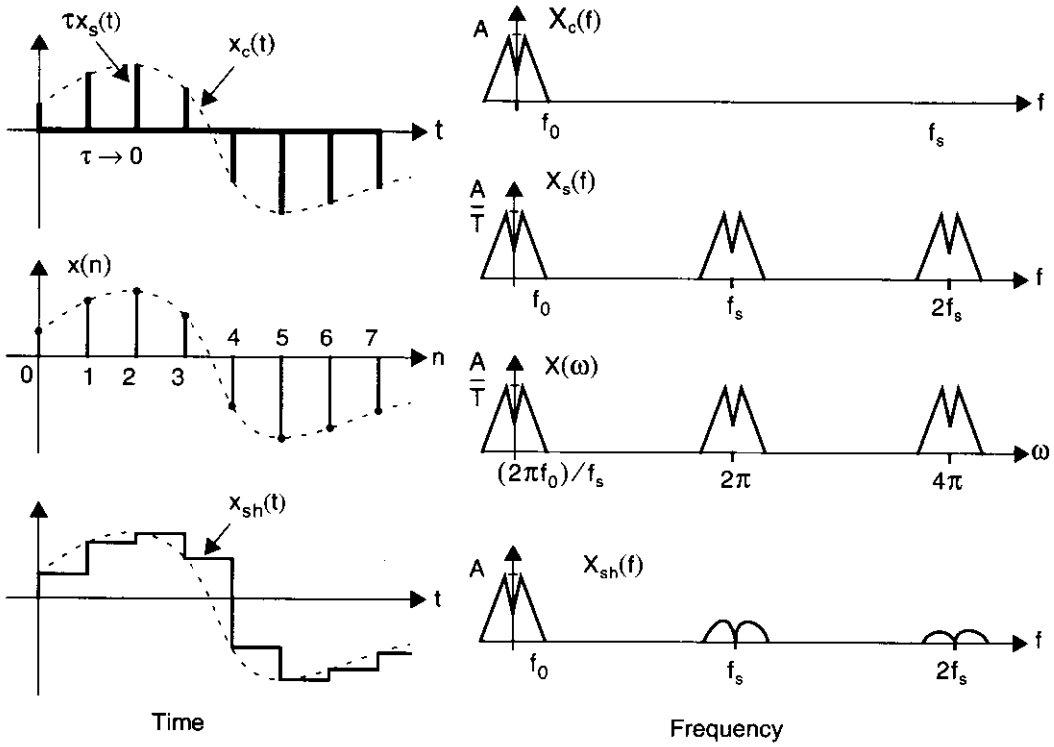


Fig. 9.2 Some time signals and frequency spectra.

example time signals and frequency spectra for this system are shown in Fig. 9.2. Here, $s(t)$ is a periodic impulse train in time with a period of T, where T equals the inverse of the sampling frequency, f_s. Some relationships for the signals in Figs. 9.1 and 9.2 are as follows:

1. $x_s(t)$ has the same frequency spectrum as $x_c(t)$, but the baseband spectrum repeats every f_s (assuming that no aliasing occurs and hence, an anti-aliasing filter is needed).
2. $x(n)$ has the same frequency spectrum as $x_s(t)$, but the sampling frequency is normalized to 1.
3. The frequency spectrum for $X_{sh}(t)$ equals that of $X_s(t)$ multiplied by a response of $(\sin x)/x$ (in effect, multiplying $X_s(f)$ by this response helps to remove high-frequency images).

The remainder of this chapter confirms these spectral relationships and introduces other basic discrete-time concepts.

9.2 LAPLACE TRANSFORMS OF DISCRETE-TIME SIGNALS

Consider the sampled signal, $x_s(t)$, related to the continuous-time signal, $x_c(t)$, as shown in Fig. 9.3. Here, $x_s(t)$ has been scaled by τ such that the area under the pulse

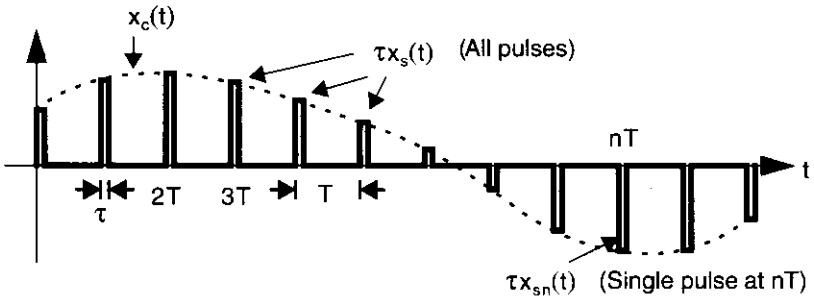


Fig. 9.3 Sampled and continuous-time signals.

at nT equals the value of $x_c(nT)$. In other words, at $t = nT$, we have

$$x_s(nT) = \frac{x_c(nT)}{\tau} \tag{9.1}$$

such that the area under the pulse, $\tau x_s(nT)$, equals $x_c(nT)$. Thus, as $\tau \to 0$, the height of $x_s(t)$ at time nT goes to ∞, and so we plot $\tau x_s(t)$ instead of $X_s(t)$.

We define $\vartheta(t)$ to be the step function given by

$$\vartheta(t) \equiv \begin{cases} 1 & (t \geq 0) \\ 0 & (t < 0) \end{cases} \tag{9.2}$$

Then $x_s(t)$ can be represented as a linear combination of a series of pulses, $x_{sn}(t)$, where $x_{sn}(t)$ is zero everywhere except for a single pulse at nT. The single-pulse signal, $x_{sn}(t)$, can be written as

$$x_{sn}(t) = \frac{x_c(nT)}{\tau}[\vartheta(t - nT) - \vartheta(t - nT - \tau)] \tag{9.3}$$

so that we can now write $x_s(t)$ as

$$x_s(t) = \sum_{n=-\infty}^{\infty} x_{sn}(t) \tag{9.4}$$

Note that these signals are defined for *all time*, so we can find the Laplace transform of $x_s(t)$ in terms of $x_c(t)$. Using the notation that $X_s(s)$ is the Laplace transform of $x_s(t)$, we find the Laplace transform $X_{sn}(s)$ for $x_{sn}(t)$ to be given by

$$X_{sn}(s) = \frac{1}{\tau}\left(\frac{1 - e^{-s\tau}}{s}\right) x_c(nT) e^{-snT} \tag{9.5}$$

Since $x_s(t)$ is merely a linear combination of $x_{sn}(t)$, we also have (for $\tau \neq 0$)

$$X_s(s) = \frac{1}{\tau}\left(\frac{1 - e^{-s\tau}}{s}\right) \sum_{n=-\infty}^{\infty} x_c(nT) e^{-snT} \tag{9.6}$$

Using the expansion $e^x = 1 + x + (x^2/2!) + \cdots$, when $\tau \to 0$, the term before the summation in (9.6) goes to unity. Therefore, in the limiting case as $\tau \to 0$, we have

$$X_s(s) = \sum_{n=-\infty}^{\infty} x_c(nT)e^{-snT} \tag{9.7}$$

Spectra of Discrete-Time Signals

The spectrum of the sampled signal, $x_s(t)$, can be found by replacing s by $j\omega$ in (9.7). However, a more intuitive approach to find the spectrum of $x_s(t)$ is to recall that multiplication in the time domain is equivalent to convolution in the frequency domain. To use this fact, note that, for $\tau \to 0$, $x_s(t)$ can be written as the product

$$x_s(t) = x_c(t)s(t) \tag{9.8}$$

where $s(t)$ is a periodic pulse train, or mathematically,

$$s(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT) \tag{9.9}$$

where $\delta(t)$ is the unit impulse function, also called the *Dirac delta function.* It is well known that the Fourier transform of a periodic impulse train is another periodic impulse train. Specifically, the spectrum of $s(t)$, $S(j\omega)$, is given by

$$S(j\omega) = \frac{2\pi}{T} \sum_{k=-\infty}^{\infty} \delta\left(\omega - k\frac{2\pi}{T}\right) \tag{9.10}$$

Now writing (9.8) in the frequency domain, we have

$$X_s(j\omega) = \frac{1}{2\pi} X_c(j\omega) \otimes S(j\omega) \tag{9.11}$$

where $\otimes$ denotes convolution. Finally, by performing this convolution either mathematically or graphically, the spectrum of $X_s(j\omega)$ can be seen to be given by

$$X_s(j\omega) = \frac{1}{T} \sum_{k=-\infty}^{\infty} X_c\left(j\omega - \frac{jk2\pi}{T}\right) \tag{9.12}$$

or, equivalently,

$$X_s(f) = \frac{1}{T} \sum_{k=-\infty}^{\infty} X_c(j2\pi f - jk2\pi f_s) \tag{9.13}$$

Equations (9.12) and (9.13) show that the spectrum for the sampled signal, $x_s(t)$, equals a sum of shifted spectra of $x_c(t)$, and therefore no aliasing occurs if $X_c(j\omega)$ is band limited to $f_s/2$. The relation in (9.13) also confirms the example spectrum for $X_s(f)$, shown in Fig. 9.2. Note that, for a discrete-time signal, $X_s(f) = X_s(f \pm kf_s)$, where k is an arbitrary integer as seen by substitution in (9.13).

Finally, note that the signal $x_s(t)$ cannot exist in practice when $\tau \to 0$ since an infinite amount of power would be required to create it. (Integrating $X_s(f)$ over all frequencies illustrates this remark.)

9.3 z-TRANSFORM

For our purposes, the z-transform is merely a shorthand notation for (9.7). Specifically, defining

$$z \equiv e^{sT} \tag{9.14}$$

we can write

$$X(z) \equiv \sum_{n=-\infty}^{\infty} x_c(nT)z^{-n} \tag{9.15}$$

where $X(z)$ is called the z-transform of the samples $x_c(nT)$.

Two properties of the z-transform that can be deduced from Laplace transform properties are as follows:

1. If $x(n) \leftrightarrow X(z)$, then $x(n-k) \leftrightarrow z^{-k}X(z)$
2. Convolution in the time domain is equivalent to multiplication in the frequency domain. Specifically, if $y(n) = h(n) \otimes x(n)$, where $\otimes$ denotes convolution, then $Y(z) = H(z)X(z)$. Similarly, multiplication in the time domain is equivalent to convolution in the frequency domain.

Note that $X(z)$ is not a function of the sampling rate but is related only to the numbers $x_c(nT)$, whereas $X_s(s)$ is the Laplace transform of the signal $x_s(t)$ as $\tau \to 0$. In other words, the signal $x(n)$ is simply a series of numbers that may (or may not) have been obtained by sampling a continuous-time signal. One way of thinking about this series of numbers as they relate to the samples of a possible continuous-time signal is that the original sample time, T, has been effectively normalized to one (i.e., $f_s' = 1$ Hz). Such a normalization of the sample time, T, in both time and frequency, justifies the spectral relation between $X_s(f)$ and $X(\omega)$ shown in Fig. 9.2. Specifically, the relationship between $X_s(f)$ and $X(\omega)$ is given by

$$X_s(f) = X\left(\frac{2\pi f}{f_s}\right) \tag{9.16}$$

or, equivalently, the following frequency scaling has been applied:

$$\omega = \frac{2\pi f}{f_s} \tag{9.17}$$

This normalization results in discrete-time signals having ω in units of radians/sample, whereas the original continuous-time signals have frequency units of cycles/second (hertz) or radians/second. For example, a continuous-time sinusoidal signal of 1 kHz when sampled at 4 kHz will change by $\pi/2$ radians between each sample.

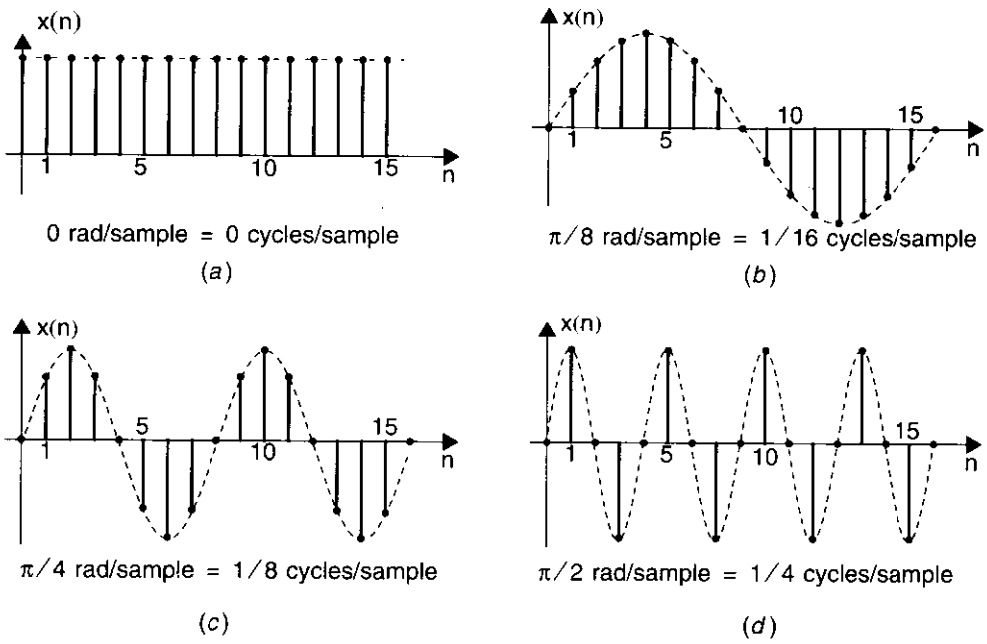


Fig. 9.4 Some discrete-time sinusoidal signals.

Therefore, such a discrete-time signal is defined to have a frequency of $\pi/2$ rad/sample. Other examples of discrete-time sinusoidal signals are shown in Fig. 9.4. It should be noted here that discrete-time signals are not unique since the addition of 2π results in the same signal. For example, a discrete-time signal that has a frequency of $\pi/4$ rad/sample is identical to that of $9\pi/4$ rad/sample. Thus, normally discrete-time signals are defined to have frequency components only between $-\pi$ and π rad/sample. For a more detailed discussion of this unit topic, see [Proakis, 1992].

EXAMPLE 9.1

Consider the spectra of $X_c(f)$ and $X_s(f)$, shown in Fig. 9.2, where f_0 is 1 Hz and f_s is 4 Hz. Compare the time and spectrum plots of $X_s(f)$ and $X_{s2}(f)$, where $X_{s2}(f)$ is sampled at 12 Hz. How does $X(\omega)$ differ between the two sampling rates?

Solution

By sampling at 12 Hz, the spectrum of $X_c(f)$ repeats every 12 Hz, resulting in the signals shown in Fig. 9.5.

Note that, for $X(\omega)$, 4 Hz is normalized to 2π rad/sample, whereas for $X_2(\omega)$, 12 Hz is normalized to 2π rad/sample.

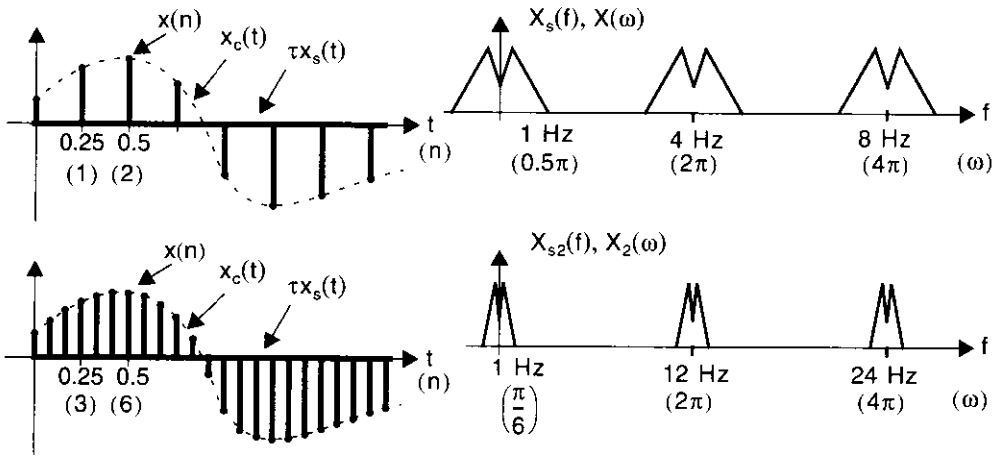


Fig. 9.5 Comparing time and frequency of two sampling rates.

9.4 DOWNSAMPLING AND UPSAMPLING

Two operations that are quite popular in discrete-time signal processing are downsampling and upsampling. Downsampling is used to reduce the sample rate (hopefully, without information loss), whereas upsampling is used to increase the sample rate. Although noninteger downsampling and upsampling rates can be achieved, here we consider only the case in which L is an integer value.

Downsampling is achieved by keeping every Lth sample and discarding the others. As Fig. 9.6 shows, the result of downsampling is to expand the original spectra by L. Thus, to avoid digital aliasing, the spectra of the original signal must be band limited to π/L before downsampling is done. In other words, the signal must be sampled L times above its minimum sampling rate so that no information is lost during downsampling.

Upsampling is accomplished by inserting $L-1$ zero values between samples, as shown in Fig. 9.7. In this case, one can show that the spectra of the resulting

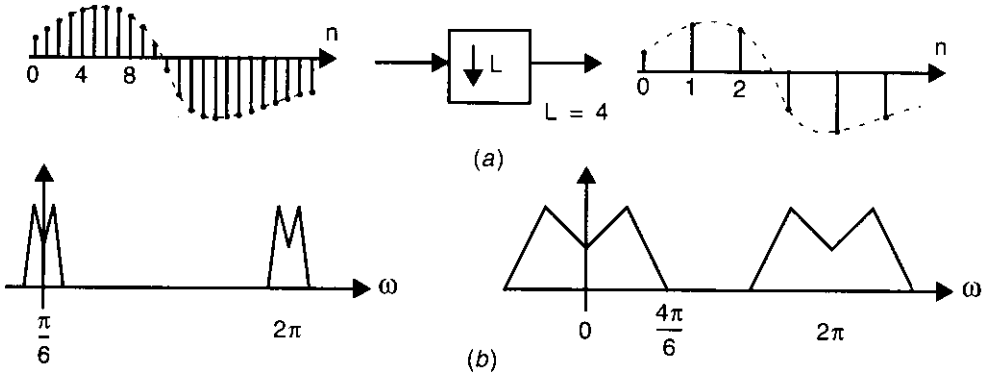


Fig. 9.6 Downsampling by 4: (*a*) time domain, and (*b*) frequency domain.

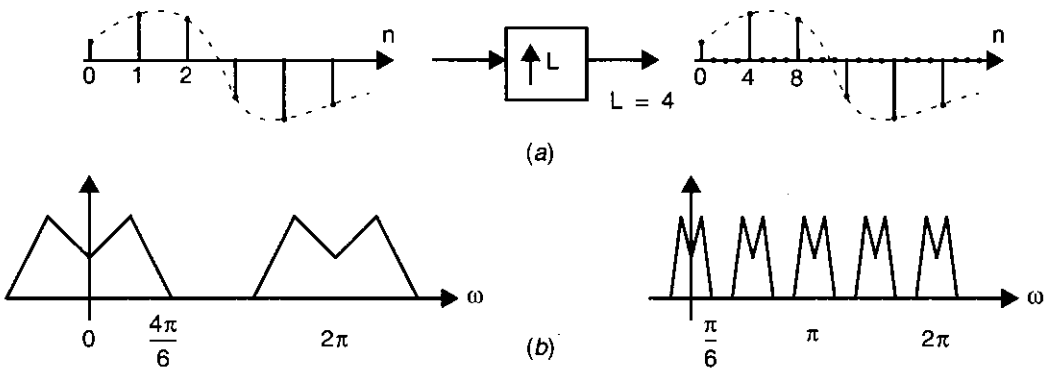


Fig. 9.7 Upsampling by 4: (*a*) time domain, and (*b*) frequency domain.

upsampled signal are identical to the original signal but with a renormalization along the frequency axis. Specifically, when a signal is upsampled by L, the frequency axis is scaled by L such that 2π now occurs where $L2\pi$ occurred in the original signal. This operation is useful when one wishes to increase the effective sampling rate of a signal, particularly if postfiltering is then applied.

Follow the next two examples carefully—they help explain the spectral changes due to downsampling and upsampling.

EXAMPLE 9.2

As an example of downsampling of the signal $x_2(n)$ in Example 9.1, find the new spectrum, $X_3(\omega)$, when every third sample is kept and the others are discarded (i.e., when we downsample by 3). In other words, if the original series of numbers is $x_1, x_2, x_3, x_4, \ldots$, the new series is $x_1, x_4, x_7, x_{10}, \ldots$.

Solution

Clearly the solution here is that the new sequence is equivalent to $x(n)$ in Example 9.1, and thus its spectrum is simply $X_3(\omega) = X(\omega)$.

Note that no information was lost in this example because the initial images of the signal $x_2(n)$ were far enough apart. However, if the downsampling operation results in the spectra overlapping one another, then an aliasing phenomenon occurs that is similar to that which occurs when sampling an analog signal lower than the Nyquist rate. In fact, it can be shown that, to avoid any aliasing during downsampling by the factor L, the original signal should be band limited to π/L.

EXAMPLE 9.3

As an example of upsampling of the signal $x(n)$ in Example 9.1, find the new spectrum, $X_4(\omega)$, if two zeros are inserted between each sample (i.e., if we

upsample by 3). In other words, if the original series of numbers was $x(n) = x_1, x_2, x_3, \ldots$ and had a spectrum $X(\omega)$, then the new series of numbers is now $x_4(n) = (x_1, 0, 0, x_2, 0, 0, x_3, \ldots)$ and has a spectrum $X_4(\omega)$.

Solution

Perhaps the simplest way to conceptualize the insertion of these extra 0 samples in a series is to look at $X_{s4}(f)$ in time and frequency when we let $f_{s4} = 12$ Hz. Recall that $x_{s4}(t)$ is defined for all time, where it is zero between its impulses, and the Laplace transform is used to observe its frequency response. With such a sampling frequency, we note that $x_{s4}(t)$ is equal to the signal $x_s(t)$, and thus $X_{s4}(f) = X_s(f)$. To find $X_4(\omega)$, recall that it is simply a frequency normalization of $X_{s4}(f)$, where the sampling frequency is normalized to 2π. In other words, the series $x(n)$ is simply a normalization of the time between impulses to 1. However, by inserting extra zeros between samples, the normalization is effectively being done for a time period smaller than that between nonzero impulses. Thus, the images remain the same while the normalization along the frequency axis is different.

In this example, since two zeros are inserted, the effective sampling rate might be thought of as 12 Hz, but now the images at 4 Hz and 8 Hz remain in contrast to $X_2(\omega)$ in Example 9.1. The resulting signals are shown in Fig. 9.8.

Finally, note that if signal processing is used on the samples $x_4(n)$ to eliminate the two images at $(2\pi)/3$ and $(4\pi)/3$, then the resulting signal will equal $x_2(n)$. In other words, as long as an analog signal is originally sampled higher than the Nyquist rate, we can use upsampling and digital-signal processing to derive signals that are the same as if the analog signal were sampled at a much higher rate.

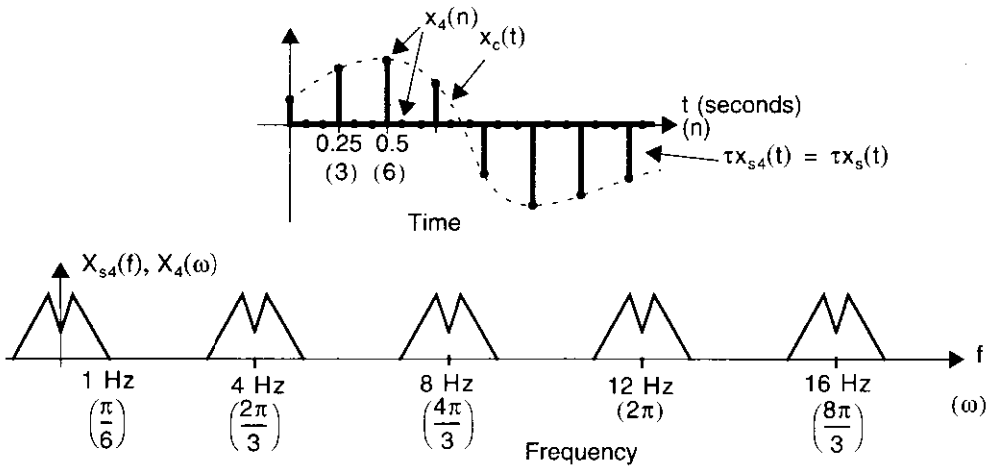


Fig. 9.8 Spectrum of a discrete-time signal upsampled by 3.

9.5 DISCRETE-TIME FILTERS

Thus far, we have seen the relationship between continuous-time and discrete-time signals in the time and frequency domain. However, often one wishes to perform filtering on a discrete-time signal to produce another discrete-time signal. In other words, an input series of numbers is applied to a discrete-time filter to create an output series of numbers. This filtering of discrete-time signals is most easily visualized with the shorthand notation of z-transforms.

Consider the system shown in Fig. 9.9, where the output signal is defined to be the impulse response, h(n), when the input, u(n), is an impulse (i.e., 1 for n = 0 and 0 otherwise). The transfer function of the filter is said to be given by H(z), which is the z-transform of the impulse response, h(n).

Frequency Response of Discrete-Time Filters

The transfer functions for discrete-time filters appear similar to those for continuous-time filters, except that, instead of polynomials in s, polynomials in z are obtained. For example, the transfer function of a low-pass, continuous-time filter, $H_c(s)$, might appear as

$$H_c(s) = \frac{4}{s^2 + 2s + 4} \tag{9.18}$$

The poles for this filter are determined by finding the roots of the denominator polynomial, which are $-1.0 \pm 1.7321j$ for this example. This continuous-time filter is also defined to have two zeros at ∞ since the denominator polynomial is two orders higher than the numerator polynomial. To find the frequency response of $H_c(s)$, the poles and zeros can be plotted in the s-plane (Fig. 9.10(*a*)), and the substitution $s = j\omega$ is equivalent to finding the magnitude and phase of vectors from a point along the $j\omega$ axis to all the poles and zeros.

An example of a discrete-time, low-pass transfer function is given by the following equation:

$$H(z) = \frac{0.05}{z^2 - 1.6z + 0.65} \tag{9.19}$$

Here, the poles now occur at $0.8 \pm 0.1j$ in the z-plane, and two zeros are again at ∞. To find the transfer function of H(z), the poles and zeros can be plotted in the z-plane; however, instead of going along the vertical $j\omega$ axis as in the s-plane,

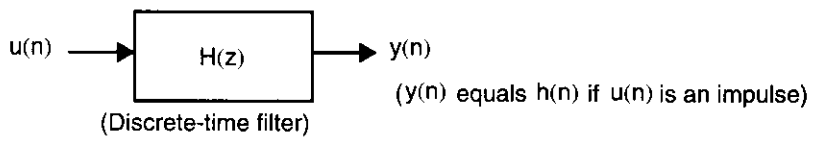


Fig. 9.9 Discrete-time filter system.

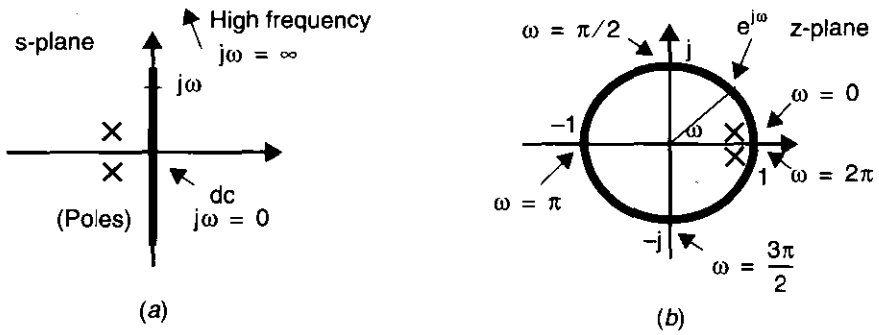


Fig. 9.10 Transfer function response. (*a*) Continuous-time, and (*b*) discrete-time.

the unit circle contour is used, so that $z = e^{j\omega}$, as shown in Fig. 9.10(*b*). Note that substituting $z = e^{j\omega}$ in the z-domain transfer function, $H(z)$, is simply a result of substituting $s = j\omega$ into (9.14), where T has been normalized to 1, as discussed in Section 9.3. Also note that poles or zeros occurring at $z = 0$ do not affect the magnitude response of $H(z)$ since a vector from the origin to the unit circle always has a length of unity. However, they would affect the phase response.

We see here that in the discrete-time domain, $z = 1$ corresponds to the frequency response at both dc (i.e., $\omega = 0$) and at $\omega = 2\pi$. Also, the time normalization of setting T to unity implies that $\omega = 2\pi$ is equivalent to the sampling-rate speed (i.e., $f = f_s$) for $X_s(f)$. In addition, note that the frequency response of a filter need be plotted only for $0 \le \omega \le \pi$ (i.e., $0 \le \omega \le f_s/2$) since, for filters with real coefficients, the poles and zeros always occur in complex-conjugate pairs (or on the real axis), so the magnitude response of the filter is equal to that for $\pi \le \omega \le 2\pi$ (the filter's phase is antisymmetric). Going around the circle again gives the same result as the first time, implying that the frequency response repeats every 2π.

Before we leave this section, a word of caution is in order. To simplify notation, the same variables, f and ω, are used in both the continuous-time and discrete-time domains in Fig. 9.10. However, these variables are not equal in the two domains, and care should be taken not to confuse values from the two domains. The continuous-time domain is used here for illustrative reasons only since the reader should already be quite familiar with transfer function analysis in the s-domain. In summary, the unit circle, $e^{j\omega}$, is used to determine the frequency response of a system that has its input and output as a series of numbers, whereas the $j\omega$-axis is used for a system that has continuous-time inputs and outputs. However, ω is different for the two domains.

EXAMPLE 9.4

Assuming a sample rate of $f_s = 100$ kHz, find the magnitude of the transfer function in (9.19) for 0 Hz, 100 Hz, 1 kHz, 10 kHz, 50 kHz, 90 kHz, and 100 kHz.

Table 9.1 Finding the gain of H(z) at some example frequencies

	z-plane locations		
Frequency (kHz)	$e^{j\omega}$	$z = x + jy$	$\lvert H(z)\rvert$
0	e^{j0}	1.0 + j0.0	1.0
0.1	$e^{j0.002\pi}$	0.9999803 + j0.00628314	0.9997
1	$e^{j0.02\pi}$	0.9980267 + j0.06279052	0.968
10	$e^{j0.2\pi}$	0.809 + j0.5878	0.149
50	$e^{j\pi}$	− 1.0 + j0.0	0.0154
90	$e^{j1.8\pi}$	0.809 − j0.5878	0.149
100	$e^{j2\pi}$	1.0 + j0.0	1.0

Solution

To find the magnitude of $H(z)$ at these frequencies, first we find their equivalent z-domain locations by normalizing f_s to 2π. Next, we find the gain of $H(z)$ by putting these z-domain values into (9.19) and finding the magnitude of the resulting complex value. Table 9.1 summarizes the results.

Note that the gain of $H(z)$ is the same at both 0 Hz and 100 kHz, as expected, since their z-plane locations are the same. Also, the gain is the same at both 10 kHz and 90 kHz since their z-plane locations are complex conjugates of each other. Finally, note that the minimum gain for this transfer function occurs at $z = -1$, or equivalently, $f_s/2 = 50$ kHz.

EXAMPLE 9.5

Consider a first-order $H(z)$ having its zero at ∞ and its pole on the real axis, where $0 < a < 1$. Mathematically, the transfer function is represented by $H(z) = b/(z - a)$. Find the value of ω, where the magnitude of $H(z)$ is 3 dB lower than its dc value. What is the 3-dB value of ω for a real pole at 0.8? What fraction of the sampling rate, f_s, does it correspond to?

Solution

Consider the pole-zero plot shown in Fig. 9.11, where the zero is not shown since it is at ∞. Since the zero is at ∞, we need be concerned only with the magnitude of the denominator of $H(z)$ and when it becomes $\sqrt{2}$ larger than its dc value. The magnitude of the denominator of $H(z)$ for $z = 1$ (i.e., dc) is shown as the vector I_1 in Fig. 9.11. This vector changes in size as z goes around the unit circle and is shown as I_2 when it becomes $\sqrt{2}$ larger than I_1. Thus we can write,

$$I_2 = e^{j\omega} - a \equiv \sqrt{2}(1 - a) \tag{9.20}$$

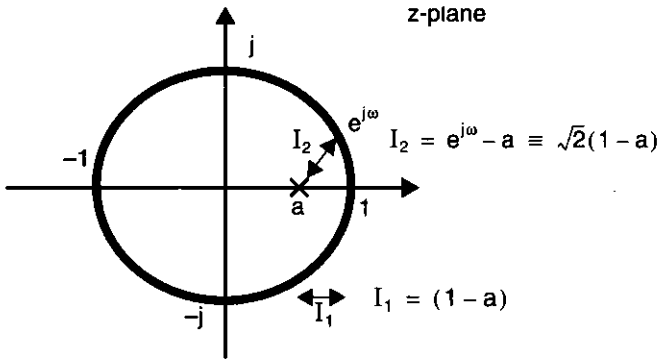


Fig. 9.11 Pole-zero plot used to determine the 3-dB frequency of a first-order, discrete-time filter.

Writing $e^{j\omega} = \cos(\omega) + j\sin(\omega)$, we have

$$|(\cos(\omega) - a) + j\sin(\omega)|^2 = 2(1-a)^2 \tag{9.21}$$

$$\cos^2(\omega) - (2a)\cos(\omega) + a^2 + \sin^2(\omega) = 2(1-a)^2 \tag{9.22}$$

$$1 - (2a)\cos(\omega) + a^2 = 2(1 - 2a + a^2) \tag{9.23}$$

which is rearranged to give the final result.

$$\omega = \cos^{-1}\left(2 - \frac{a}{2} - \frac{1}{2a}\right) \tag{9.24}$$

For $a = 0.8$, $\omega = 0.2241$ rad, or 12.84 degrees. Such a location on the unit circle corresponds to $0.2241/(2\pi)$ times f_s or, equivalently, $f_s/28.04$.

Stability of Discrete-Time Filters

To realize rational polynomials in z, discrete-time filters use delay elements (i.e., z^{-1} building blocks) much the same way that analog filters can be formed using integrators (i.e., s^{-1} building blocks). The result is that finite difference equations represent discrete-time filters rather than the differential equations used to describe continuous-time filters.

Consider the block diagram of a first-order, discrete-time filter shown in Fig. 9.12. A finite difference equation describing this block diagram can be written as

$$y(n+1) = bx(n) + ay(n) \tag{9.25}$$

In the z-domain, this equation is written as

$$zY(z) = bX(z) + aY(z) \tag{9.26}$$

where the z-domain property of delayed signals is used. We define the transfer function of this system to be $H(z)$ given by

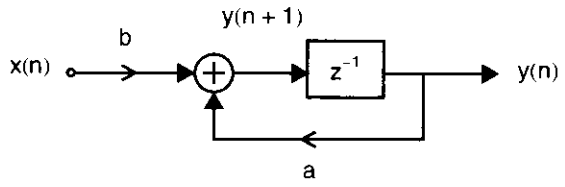


Fig. 9.12 A first-order, discrete-time filter.

$$H(z) \equiv \frac{Y(z)}{X(z)} = \frac{b}{z - a} \tag{9.27}$$

which has a pole on the real axis at $z = a$.

To test for stability, we let the input, $x(n)$, be an impulse signal (i.e., 1 for $n = 0$ and 0 otherwise), which gives the following output signal, according to (9.25),

$$y(0) = k$$

where k is some arbitrary initial state value for y.

$$\begin{aligned} y(1) &= b + ak \\ y(2) &= ab + a^2k \\ y(3) &= a^2b + a^3k \\ y(4) &= a^3b + a^4k \\ &\vdots \end{aligned}$$

More concisely, the response, $h(n)$, is given by

$$h(n) = \begin{cases} 0 & (n < 1) \\ (a^{n-1}b + a^n k) & (n \geq 1) \end{cases} \tag{9.28}$$

Clearly, this response remains bounded only when $|a| \leq 1$ for this first-order filter and is unbounded otherwise.

Although this stability result is shown only for first-order systems, in general, an arbitrary, linear, time-invariant, discrete-time filter, $H(z)$, is stable if and only if all its poles are located within the unit circle. In other words, if z_{pi} are the poles, then $|z_{pi}| < 1$ for all i. Locating some poles on the unit circle is similar to poles being on the imaginary $j\omega$-axis for continuous-time systems. For example, in the preceding first-order example, if $a = 1$, the pole is at $z = 1$, and the system is marginally stable (in fact, it is a discrete-time integrator). If we let $a = -1$, this places the pole at $z = -1$, and one can show that the system oscillates at $f_s/2$, as expected.

IIR and FIR Filters

Infinite-impulse-response (IIR) filters are discrete-time filters that, when excited by an impulse, their outputs remain nonzero, assuming infinite precision arithmetic. For

example, the filter given in (9.27) is an IIR filter (for a not equal to zero) since, although its impulse response decays to zero (as all stable filters should), it remains nonzero for a finite value of n.

Finite-impulse-response (FIR) filters are discrete-time filters that, when excited by an impulse, their outputs go precisely to zero (and remain zero) after a finite value of n. As an example of an FIR filter, consider the following filter,

$$y(n) = \frac{1}{3}[x(n) + x(n-1) + x(n-2)] \tag{9.29}$$

Defining the transfer function for this filter to be $H(z)$, we can easily show that

$$H(z) = \frac{1}{3}\sum_{i=0}^{2} z^{-i} \tag{9.30}$$

This filter is essentially a running average filter since its output is equal to the average value of its input over the last three samples. Applying an impulse signal to this filter results in an output that is nonzero for only three samples and, therefore, this is an FIR type filter. Note that this FIR filter has poles, but they all occur at $z = 0$.

Some advantages of FIR filters are that stability is never an issue (they are always stable) and exact linear phase filters can be realized (a topic beyond the scope of this chapter). However, for many specifications, an IIR filter can meet the same specifications as an FIR filter, but with a much lower order, particularly in narrowband filters in which the poles of an IIR filter are placed close to the unit circle (i.e., has a slowly decaying impulse response).

Bilinear Transform

With modern filter design software, desired discrete-time transfer functions that meet specifications can be obtained entirely within the discrete-time domain. However, another approach draws on the wealth of knowledge of continuous-time transfer-function approximation and uses the bilinear transform. Assuming that $H_c(p)$ is a continuous-time transfer function (where p is the complex variable equal to $\sigma_p + j\Omega$), the bilinear transform is defined to be given by[1]

$$p = \frac{z-1}{z+1} \tag{9.31}$$

The inverse transformation is given by

$$z = \frac{1+p}{1-p} \tag{9.32}$$

1. It should be noted here that in many other textbooks, the bilinear transform is defined as $s = (2/T)[(z-1)/(z+1)]$ where T is the sampling period. Here, we have normalized T to 2 since we use the bilinear transform only as a temporary transformation to a continuous-time equivalent, and then we inverse transform the result back to discrete time. Thus, the value of T can be chosen arbitrarily as long as the same value is used in each transformation.

A couple of points of interest about this bilinear transform are that the z-plane locations of 1 and –1 (i.e., dc and $f_s/2$) are mapped to p-plane locations of 0 and ∞, respectively. However, with a little analysis, we will see that this bilinear transformation also maps the unit circle, $z = e^{j\omega}$, in the z-plane to the entire $j\Omega$-axis in the p-plane. To see this mapping, we substitute $z = e^{j\omega}$ into (9.31),

$$p = \frac{e^{j\omega} - 1}{e^{j\omega} + 1} = \frac{e^{j(\omega/2)}\left(e^{j(\omega/2)} - e^{-j(\omega/2)}\right)}{e^{j(\omega/2)}\left(e^{j(\omega/2)} + e^{-j(\omega/2)}\right)} \tag{9.33}$$

$$= \frac{2j\sin(\omega/2)}{2\cos(\omega/2)} = j\tan(\omega/2)$$

Thus, we see that points on the unit circle in the z-plane are mapped to locations on the $j\Omega$-axis in the p-plane, and we have

$$\Omega = \tan(\omega/2) \tag{9.34}$$

As a check, note that the z-plane locations of 1 and –1, which correspond to ω equal to 0 and π, respectively, map to Ω equal to 0 and ∞.

One way to use this transform is to design a continuous-time transfer function, $H_c(p)$, and choose the discrete-time transfer function, $H(z)$, such that

$$H(z) \equiv H_c[(z-1)/(z+1)] \tag{9.35}$$

With such an arrangement, one can show that

$$H(e^{j\omega}) = H_c[j\tan(\omega/2)] \tag{9.36}$$

and so the response of $H(z)$ is shown to be equal to the response of $H_c(p)$, except with a frequency warping according to (9.34). Note that the order of $H(z)$ equals that of $H_c(p)$ since, according to (9.35), each p term is replaced by another first-order function.

EXAMPLE 9.6

Using the bilinear transform, find the 3-dB frequency of a first-order discrete-time filter, $H(z)$, that has a pole at 0.8 and a zero at –1.

Solution

Using (9.31), we see that the z-plane pole of 0.8 and zero of –1 are mapped to a pole at –0.11111 and to a zero at ∞ in the p-plane, respectively. Such a continuous-time filter has a 3-dB frequency at $\Omega = 0.11111$ rad/s. Using (9.34), we find that the equivalent 3-dB frequency value in the z-plane is given by $\omega = 0.2213$ rad/sample, or $f_s/28.4$.

Note that this result is very close to that in Example 9.5. However, the two results are not in exact agreement since a zero at –1 is also present in this example.

EXAMPLE 9.7

Using the bilinear transform, find a first-order $H(z)$ that has a 3-dB frequency at $f_s/20$, a zero at -1, and a dc gain of 1.

Solution

Using (9.34), the frequency value, $f_s/20$, or equivalently, $\omega = (2\pi)/20 = 0.314159$ is mapped to $\Omega = 0.1584$ rad/s. Thus, $H_c(p)$ should have a 3-dB frequency value of 0.1584 rad/s. Such a 3-dB frequency value is obtained by having a p-plane zero equal to ∞ and a pole equal to 0.1584. Transforming these continuous-time pole and zero back into the z-plane using (9.32) results in a z-plane zero at -1 and a pole at 0.7265. Therefore, $H(z)$ appears as

$$H(z) = \frac{k(z+1)}{z-0.7265}$$

The constant k can be determined by setting the dc gain to 1, or equivalently, $|H(1)| = 1$, which results in $k = 0.1368$.

9.6 SAMPLE-AND-HOLD RESPONSE

In this section, we look at the frequency response that occurs when we change a discrete-time signal back into an analog signal with the use of a sample-and-hold circuit. Note that here we plot a frequency response for all frequencies (as opposed to only up to $f_s/2$) since the output signal is a continuous-time signal rather than a discrete-time one.

A sample-and-hold signal, $x_{sh}(t)$, is related to its sampled signal by the mathematical relationship

$$x_{sh}(t) = \sum_{n=-\infty}^{\infty} x_c(nT)[\vartheta(t-nT) - \vartheta(t-nT-T)] \tag{9.37}$$

Note that, once again, $x_{sh}(t)$ is well defined for all time, and thus the Laplace transform can be found to be equal to

$$\begin{aligned} X_{sh}(s) &= \frac{1-e^{-sT}}{s} \sum_{n=-\infty}^{\infty} x_c(nT)e^{-snT} \\ &= \frac{1-e^{sT}}{s} X_s(s) \end{aligned} \tag{9.38}$$

This result implies that the hold transfer function, $H_{sh}(s)$, is equal to

$$H_{sh}(s) = \frac{1-e^{-sT}}{s} \tag{9.39}$$

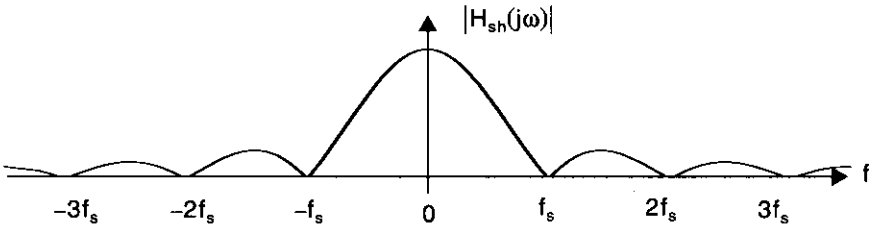


Fig. 9.13 Sample-and-hold response (also called the sinc response).

It should be mentioned here that this transfer function is usually referred to as the *sample-and-hold response* although, in fact, it only accounts for the hold portion.

The spectrum for $H_{sh}(s)$ is found by substituting $s = j\omega$ into (9.39), resulting in

$$H_{sh}(j\omega) = \frac{1 - e^{-j\omega T}}{j\omega} = T \times e^{-j\omega T/2} \times \frac{\sin(\omega T/2)}{(\omega T/2)} \tag{9.40}$$

The magnitude of this response is given by

$$|H_{sh}(j\omega)| = T\frac{|\sin(\omega T/2)|}{|\omega T/2|}$$

or

$$|H_{sh}(f)| = T\frac{|\sin(\pi f/f_s)|}{|(\pi f)/f_s|} \tag{9.41}$$

and is often referred to as the $(\sin x)/x$ or *sinc response*. This magnitude response is illustrated in Fig. 9.13.

Multiplying this sinc response by $X_s(f)$ in Fig. 9.2 confirms the spectral relationship for $X_{sh}(f)$. It should be noted here that this frequency shaping of a sample and hold occurs only for a continuous-time signal. Specifically, although the sample and hold before the A/D converter shown in Fig. 9.1(*b*) would result in $x_{sh}(t)$ having smaller images at higher frequencies (due to the sinc response), the images of $x(n)$ are all of the same height (i.e., they are not multiplied by the sinc response) since it is a discrete-time signal. In other words, a sample and hold before an A/D converter simply allows the converter to have a constant input value during one conversion and does not aid in any anti-aliasing requirement.

EXAMPLE 9.8

Consider the discrete-time signal processing system shown in Fig. 9.1(*b*), where a sample (and clock rate) of 50 kHz is used and the digital filter has the response

$$H(z) = \frac{0.2}{z - 0.8}$$

For a 10-kHz input sinusoidal signal of 1 V rms, find the magnitude of the output signal, $y_{sh}(t)$, at 10 kHz, and at the images 40 kHz and 60 kHz. Assume

the quantization effects of the A/D and D/A converters are so small that they can be ignored. Also assume the converters complement each other such that a 1-V dc signal into the A/D converter results in a 1-V dc signal from the D/A converter if the converters are directly connected together.

Solution

First, the magnitude of $H(z)$ is found for a 10-kHz signal when the sampling rate is 50 kHz by noting that

$$e^{j(2\pi \times 10\ \text{kHz}/50\ \text{kHz})} = e^{j0.4\pi} = \cos(0.4\pi) + j\sin(0.4\pi)$$
$$= 0.309017 + j0.951057$$

and therefore the gain of $H(z)$ for a 10-kHz signal is found to be given by,

$$|H(e^{j0.4\pi})| = \frac{0.2}{|(0.309017 - 0.8) + j0.951057|} = 0.186864$$

To determine the magnitude of $y_{sh}(t)$ at various frequencies, we need only multiply the filter's gain by the sinc response shown in Fig. 9.13. Specifically, the magnitude of the sample-and-hold response for a 10-kHz signal when using a 50-kHz clock is equal to

$$|H_{sh}(10\ \text{kHz})| = T\frac{\sin(\pi 10/50)}{(\pi 10/50)} = 0.9355T$$

and therefore the magnitude of $y_{sh}(t)$ at 10 kHz is equal to $18686 \times 0.9355 = 175\ \text{mV}_{\text{rms}}$ (note that the T term cancels with a similar T term due to the creation of a discrete-time signal—see (9.13) in Section 9.2). Similarly, the magnitude of $H_{sh}(f)$ at 40 kHz and 60 kHz is 0.2399 and 0.1559, respectively, resulting in the magnitude of $y_{sh}(t)$ at 40 kHz and 60 kHz to be 43.7 and $29.1\ \text{mV}_{\text{rms}}$, respectively.

9.7 REFERENCES

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A. V. Oppenheim and R. W. Schafer, *Discrete-Time Signal Processing*. Prentice Hall, Englewood Cliffs, New Jersey, 1989.

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9.8 PROBLEMS

9.1 Show that if $x(n) \leftrightarrow X(z)$, then $x(n-k) \leftrightarrow z^{-k}X(z)$.

9.2 What is the maximum amount of downsampling that can be applied to $x_{s2}(n)$ in Example 9.1 before aliasing occurs?

9.3 Is downsampling a time-invariant operation? If so, explain. If not, give a simple counter example. Is downsampling a linear operation?

9.4 Repeat Example 9.3, but upsample by 8 (i.e., insert 7 zeros between samples).

9.5 Upsampling and downsampling are often used for converting between two sample rates. Give a block diagram showing how one might convert 0 – 20 kHz band-limited audio signal from a sampling rate of 50 kHz to 40 kHz.

9.6 Find the location of the poles and zeros of the transfer function given by $H(z)$ in (9.19).

9.7 Find the location of the pole required in a first-order filter that has its zero at ∞ such that its 3-dB frequency is at $f_s/10$.

9.8 Sketch the magnitude response (in dB) of the following transfer function, $H(z)$, by finding the gains at dc and at $\omega = \pi$, as well as the location of the 3-dB frequency.

$$H(z) = \frac{0.05z}{z - 0.95}$$

9.9 Consider the following difference equation, which describes a filter with input $u(n)$ and output $y(n)$.

$$y(n) = u(n) - 0.3y(n-1)$$

Determine $y(n)$ when $u(n)$ is an impulse (i.e., when the impulse is 1 at $n = 1$ and 0 otherwise) assuming $y(0) = 0$.

9.10 Find a first-order $H(z)$ that has a 3-dB frequency at $f_s/30$, a zero at -1, and a dc gain of 1. Sketch the magnitude response from $\omega = 0$ to $\omega = 2\pi$.

9.11 Using a bilinear transform, find an $H(z)$ to realize a second-order transfer function with a dc gain of one, a maximally-flat passband (i.e., $Q = 1/\sqrt{2}$ in the continuous-time domain), and a -3-dB frequency at 1 kHz when the sampling rate is 100 kHz.

9.12 Find the output sequence of a discrete-time integrator, $H(z) = 1/(z-1)$, when its input is a sinusoidal waveform of peak height 1 at $f_s/4$ and its initial state is zero. In other words, the input waveform is the series of numbers $\{1, 0, -1, 0, 1, 0, -1, \ldots\}$. Using a frequency analysis, what is the magnitude and phase response for $H(z)$ at $f_s/4$? Check the frequency domain result with the time domain result.

9.13 A 100-Hz sinusoidal signal, $x(n)$, is digitally created using a 400-Hz sampling rate producing a sample-and-hold signal, $x_{sh}(t)$. Before any smoothing filter is applied and assuming the magnitude of $x_{sh}(t)$ at 100 Hz is 1 V_{rms}, what is the magnitude of $x_{sh}(t)$ at 300 Hz? Also, find the magnitude of $x_{sh}(t)$ at 500 Hz and at 700 Hz.

9.14 Repeat Problem 9.13, but assume the 100-Hz signal is digitally created using a 10-kHz signal, and find the magnitude of $x_{sh}(t)$ at 9.9 kHz and at 10.1 kHz.

9.15 Repeat Example 9.8, but assume an input signal frequency of 100 Hz and find the magnitude of the output signal, $y_{sh}(t)$, at 100 Hz, 99.9 kHz, and 100.1 kHz.

9.16 A 0–5-kHz voiceband microphone is modelled as having a low-pass, first-order frequency response with a pole at 10 kHz. If the microphone output is sampled at 100 kHz, how much attenuation is required in the anti-aliasing filter for 80-dB noise rejection around 100 kHz?

CHAPTER

10 Switched-Capacitor Circuits

Perhaps the most popular approach for realizing analog signal processing in MOS (or BiCMOS) integrated circuits is through the use of switched-capacitor circuits [Poschenrieder, 1966; Fried, 1972; Caves, 1977; Hosticka, 1977; Young, 1977]. A switched-capacitor circuit operates as a discrete-time signal processor (although without the use of A/D or D/A converters). As a result, these circuits are most easily analyzed with the use of z-transform techniques and typically require anti-aliasing and smoothing filters.

As a filtering technique, switched-capacitor circuits have become extremely popular due to their accurate frequency response as well as good linearity and dynamic range. Accurate discrete-time frequency responses are obtained since filter coefficients are determined by capacitance ratios which can be set quite precisely in an integrated circuit (on the order of 0.1 percent). Such an accuracy is orders of magnitude better than that which occurs for integrated RC time constants (which can vary by as much as 20 percent). Once the coefficients of a switched-capacitor discrete-time filter are accurately determined, its overall frequency response remains a function of the clock (or sampling) frequency. Fortunately, clock frequencies can also be set very precisely through the use of a crystal oscillator.

In addition to creating filtering functions, switched-capacitor circuit techniques can be used to realize a variety of other signal-processing blocks such as gain-stages, voltage-controlled oscillators, and modulators. This chapter will introduce the basic principles of switched-capacitor filters as well as some other nonfiltering functions realized using switched-capacitor circuits.

10.1 BASIC BUILDING BLOCKS

A switched-capacitor circuit is realized with the use of some basic building blocks such as opamps, capacitors, switches, and nonoverlapping clocks. Brief descriptions of each of these blocks and their important nonidealities with respect to switched-capacitor circuits are given in this section.

Opamps

The basic principles of switched-capacitor circuits can be well understood assuming ideal opamps. However, some important opamp nonidealities in practical switched-

capacitor circuits are dc gain, unity-gain frequency and phase-margin, slew-rate, and dc offset. Of less concern is opamp input impedance as it is essentially capacitive assuming MOSFET input stages are used.[1]

The *dc gain* of opamps in a MOS technology intended for switched-capacitor circuits is typically on the order of 40 to 80 dB. Low dc gains affect the coefficient accuracy of the discrete-time transfer function of a switched-capacitor filter.

The *unity-gain frequency and phase margin* of an opamp gives an indication of the small signal settling behavior of an opamp. A general rule of thumb is that the clock frequency should be at least five times lower in frequency than the unity-gain frequency of the opamp assuming little slew-rate behavior occurs and the phase margin is greater than 70 degrees. Modern SC circuits are often realized using high-frequency single-stage opamps having very large output impedances (on the order of 100 kΩ or much larger). Since the loads of these opamps are purely capacitive (never resistive), their dc gains remain high despite the lack of an output buffer stage. It should be noted here that their unity-gain frequency and phase margin are determined by the load capacitance, which also serves as the compensation capacitor. Thus, in these single-stage opamps, doubling the load capacitance would halve the unity-gain frequency and *improve* the phase margin.

The finite *slew rate* of an opamp can limit the upper clock rate in a switched-capacitor circuit as these circuits rely on charge being quickly transferred from one capacitor to another. Thus, at the instance of charge transfer, it is not uncommon for opamps to slew-rate limit.

A nonzero *dc offset* can result in a high output dc offset for the circuit depending on the topology chosen. Fortunately, a technique known as correlated double sampling can significantly reduce this output offset and at the same time reduce low frequency opamp input noise (known as 1/f noise).

Capacitors

A highly linear capacitance in an integrated circuit is typically constructed between two polysilicon layers, as shown in Fig. 10.1(*a*).[2] These capacitors are known as double-poly capacitors. The thin oxide is an insulating layer separating the two relatively conductive polysilicon layers, while the thick oxide is also an insulating layer but of much thicker width. The desired capacitance, C_1, is formed as the intersection of area between the two polysilicon layers, poly1 and poly2. However, since the substrate below the poly2 layer is an ac ground (the substrate is connected to one of the power supplies or analog ground), there also exists a substantial parasitic capacitance, C_{p2}, which may be as large as 20 percent of C_1. This large parasitic capacitance, C_{p2}, is known as the bottom plate capacitance. A top plate capacitance, C_{p1},

1. BJT input stages are rarely used as they would result in charge leakage due to their nonzero input bias current.
2. It is also possible to realize capacitors between other layers such as polysilicon and heavily-doped silicon, or between two metal layers.

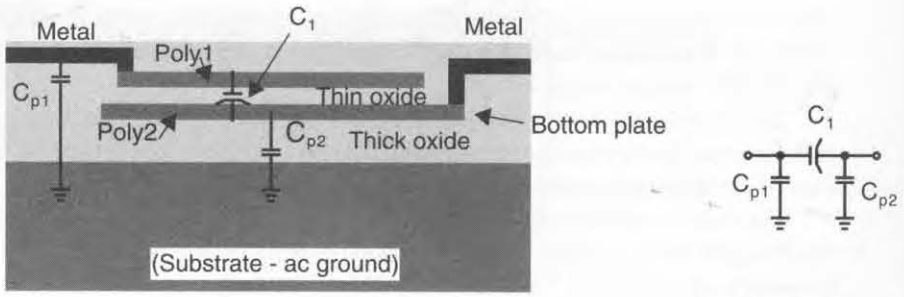


Fig. 10.1 A double-poly capacitor, C_1. Note that a large parasitic capacitance, C_{p2}, to ground exists on the bottom plate of C_1 while a smaller parasitic capacitance, C_{p1}, exists on the top plate.

also exists due primarily to the interconnect capacitance, but it is typically much smaller (on the order of 1 to 5 percent of C_1). In summary, the equivalent model for a single integrated capacitor is three capacitors, as shown in Fig. 10.1(*b*), where the bottom plate is often explicitly shown to indicate that a larger parasitic capacitance occurs on that node.

Switches

The requirements for switches used in switched-capacitor circuits are that they have a very high off resistance (so little charge leakage occurs), a relatively low on resistance (so that the circuit can settle in less than half the clock period), and introduce no offset voltage when turned on (as does a bipolar switch whose on voltage equals $V_{CE(sat)}$). The use of MOSFET transistors as switches satisfies these requirements, as MOSFET switches have off resistances in the GΩ range,[3] have no offset on voltages, and have on resistances in the 100 Ω to 5 kΩ range depending on transistor sizing.

The symbol for a switch and some MOSFET circuits that realize a switch are shown in Fig. 10.2. Here, the signal ϕ is one of two logic levels typically corresponding to the maximum and minimum power supply levels. As a convention, when the clock signal ϕ is high, the switch is assumed to be on (i.e., shorted). Although a switch can be implemented using a single transistor, as shown in Fig. 10.2(*b*) and Fig. 10.2(*c*), the signal range of the switch is reduced. For example, consider the ideal n-channel transistor switch shown in Fig. 10.2(*b*) being used in a circuit having power supplies of 0 to 5 V and a threshold voltage of V_{tn} = 0.8 V. The switch can

3. Leakage current is typically dominated by reverse biased diodes rather than the MOSFET channel which is assumed off.

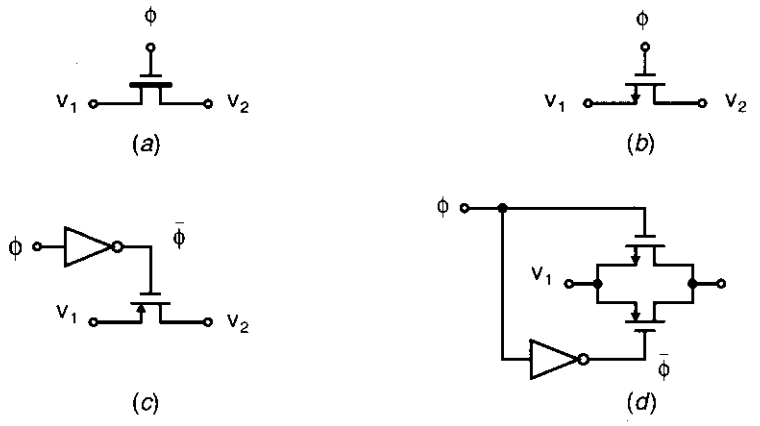


Fig. 10.2 Switch symbol and some transistor circuits: (*a*) symbol, (*b*) n-channel switch, (*c*) p-channel switch, (*d*) transmission gate.

always be turned off irrespective of the input voltage by putting 0 V on its gate. However, when the switch is on, its gate voltage will be V_{DD} or 5 V; in this case, the switch can only equalize the two voltages if V_1 and/or V_2 are lower than $V_{DD} - V_{tn}$ or around 4.0 V taking the body effect into account. Thus, the signal range for this switch is limited from 0 to 4.0 V. A similar argument can be made for the p-channel switch shown in Fig. 10.2(*c*) except that its signal range would be limited from 1.0 to 5 V. While this signal range is acceptable in many situations, the full signal range of 0 to 5 V can be achieved using two transistors in parallel, as shown in Fig. 10.2(*d*). This combination is commonly called either a CMOS switch (as opposed to an NMOS switch of Fig. 10.2(*a*)) or a CMOS transmission gate.

Some of the important nonideal switch effects in switched-capacitor circuits are the nonlinear capacitance on each side of the switch, channel charge injection, and capacitive coupling from the logic signal, ϕ, to each side of the switch. Nonlinear capacitance effects are alleviated through the use of parasitic insensitive structures, as discussed in Section 10.2, while channel charge injection is reduced by careful switch timing, as seen in Section 10.5.

Nonoverlapping Clocks

At least one pair of nonoverlapping clocks is essential in switched-capacitor circuits. These clocks determine when charge transfers occur and they must be nonoverlapping in order to guarantee charge is not inadvertently lost. As seen in Fig. 10.3(*a*), the term *nonoverlapping clocks* refers to two logic signals running at the same frequency and arranged in such a way that at no time are both signals high. Note that the time axis in Fig. 10.3(*a*) has been normalized with respect to the clock period, T. Such a normalization illustrates the location of the sample numbers of the discrete-time signals that occur in switched-capacitor filters. As a convention, we denote the sampling numbers

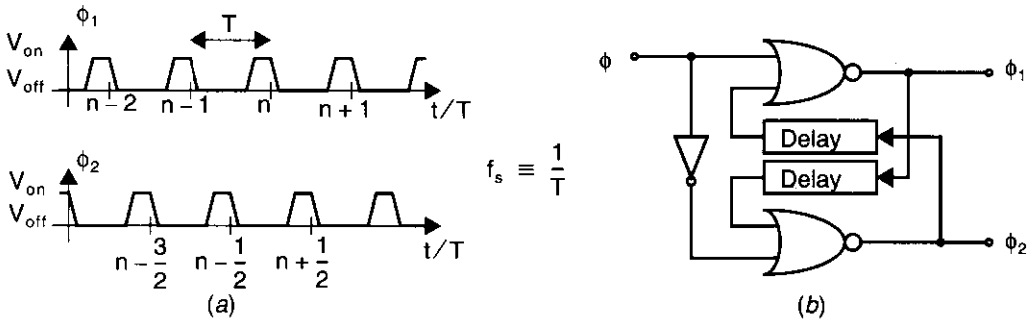


Fig. 10.3 Nonoverlapping clocks. (*a*) Clock signals, ϕ_1 and ϕ_2. (*b*) A possible circuit implementation of nonoverlapping clocks from a single clock.

to be integer values (i.e., $(n-1)$, (n), $(n+1)$, etc.) just before the end of clock phase ϕ_1, while the end of clock phase ϕ_2 is deemed to be $1/2$ sample off the integer values as shown (i.e., $(n-3/2)$, $(n-1/2)$, etc.). However, it should be noted that it is not important that the falling clock edge of ϕ_2 occur precisely one-half a clock period earlier than the falling edge of ϕ_1. In general, the locations of the clock edges of ϕ_1 and ϕ_2 need only be moderately controlled to allow for complete charge settling (assuming separate low-jitter sample and holds are used at the input and output of the overall circuit).

One simple method for generating nonoverlapping clocks is shown in Fig. 10.3(*b*) [Martin, 1981]. Here, delay blocks are used to ensure that the clocks remain nonoverlapping. These delays could be implemented as a cascade of an even number of inverters or perhaps an RC network.

10.2 BASIC OPERATION AND ANALYSIS

Resistor Equivalence of a Switched Capacitor

Consider the switched-capacitor circuit shown in Fig. 10.4(*a*), where V_1 and V_2 are two dc voltage sources. To analyze this circuit's behavior, we analyze the circuit from a charge perspective. Recall that the charge on a capacitor, Q_x, is equal to the capacitance value, C_x, times the voltage across it, V_x. In mathematical terms, we have

$$Q_x = C_x V_x \tag{10.1}$$

Now, since ϕ_1 and ϕ_2 are assumed to be a pair of nonoverlapping clocks, C_1 is charged to V_1 and then V_2 during each clock period. Therefore, the change in charge (in coulombs) over one clock period, ΔQ_1, that is transferred from node V_1 into node V_2 is given by

$$\Delta Q_1 = C_1(V_1 - V_2) \tag{10.2}$$

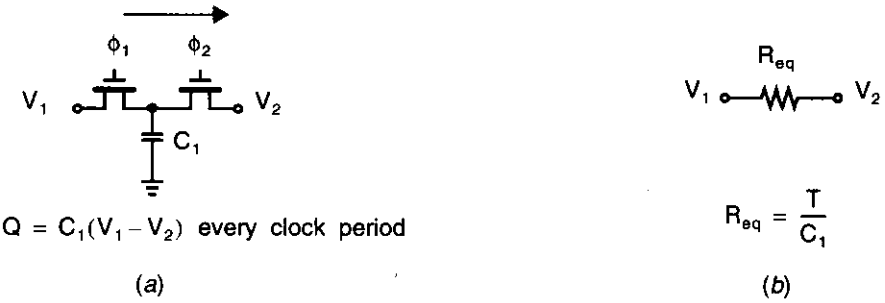


Fig. 10.4 Resistor equivalence of a switched capacitor. (*a*) Switched-capacitor circuit (*b*) Resistor equivalent.

Since this charge transfer is repeated every clock period, we can find the equivalent average current due to this charge transfer by dividing by the clock period. In other words, the average current, I_{avg} (in amps), is equal to the average number of coulombs/second and is given by

$$I_{avg} = \frac{C_1(V_1 - V_2)}{T} \tag{10.3}$$

where T is the clock period (i.e., the sampling frequency $f_s = 1/T$). Relating (10.3) to an equivalent resistor circuit shown in Fig. 10.4(*b*) where

$$I_{eq} = \frac{V_1 - V_2}{R_{eq}} \tag{10.4}$$

we see that the average current through the switched-capacitor circuit of Fig. 10.4(*a*) will equal that for the resistor circuit of Fig. 10.4(*b*) if

$$R_{eq} = \frac{T}{C_1} = \frac{1}{C_1 f_s} \tag{10.5}$$

Note that the above relation makes intuitive sense. For example, as the clock frequency is increased, the same charge is transferred each period but at a faster rate, so the average current is higher. If C_1 is increased, a larger amount of charge is transferred each period, which would also increase the average current. In addition, increasing the average current is equivalent to decreasing the equivalent resistance seen between the two voltage nodes, and therefore the equivalent resistance is inversely related to the capacitance and clock frequency.

Finally, it should be noted that this resistor approximation is mainly useful for looking at the low-frequency behavior of a switched-capacitor circuit. For moderate input frequencies (in relation to the sampling frequency), an accurate discrete-time analysis is required, as discussed in the next subsection. Discrete-time analysis can be used in switched-capacitor circuits because the charge transfers are dependent on values of node voltages at particular instances in time and are ideally independent of transients during nonsampled times.

EXAMPLE 10.1

What is the equivalent resistance of a 5 pF capacitance sampled at a clock frequency of 100 kHz?

Solution

Using (10.5), we have

$$R_{eq} = \frac{1}{(5 \times 10^{-12})(100 \times 10^{3})} = 2\ \text{M}\Omega$$

What is interesting here is that a very large impedance of 2 MΩ can be realized on an integrated circuit through the use of two transistors, a clock, and a relatively small capacitance. Such a large impedance typically requires a large amount of CMOS silicon area if it is realized as a resistor without any special processing fabrication steps.

Parasitic-Sensitive Integrator

An example of one of the first switched-capacitor discrete-time integrators [Hosticka, 1977] is shown in Fig. 10.5. Here, an extra switch is shown near the output voltage, $v_{co}(t)$, to indicate to the reader that the output signal is valid at the end of ϕ_1 in keeping with the sampling-time convention shown in Fig. 10.3(*a*). In other words, another circuit that uses the output of this discrete-time integrator should sample $v_{co}(t)$ on ϕ_1. Note however that no assumptions are made about when $v_{ci}(t)$ changes its value (it could be either ϕ_1 or ϕ_2); it is not important because $v_{ci}(t)$ is sampled at the end of ϕ_1 by the circuit shown.

To analyze this circuit, we again look at the charge behavior and note that a virtual ground appears at the opamp's negative input. Assuming an initial integrator output voltage of $v_{co}(nT - T)$ implies that the charge on C_2 is equal to $C_2 v_{co}(nT - T)$ at time $(nT - T)$. Now also at time $(nT - T)$, ϕ_1 is just turning off (and ϕ_2 is off) so the input signal $v_{ci}(t)$ is sampled, resulting in the charge on C_1 being equal to

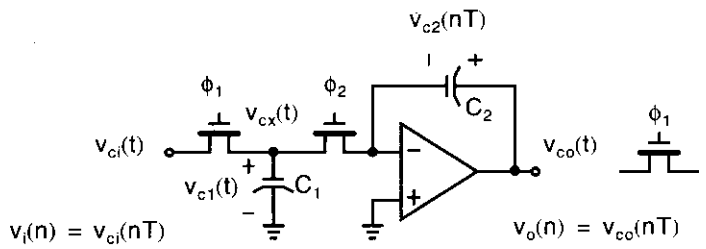


Fig. 10.5 A discrete-time integrator. This structure is sensitive to parasitic capacitances (not shown).

$C_1 v_{ci}(nT - T)$, as shown in Fig. 10.6(*a*). When ϕ_2 goes high, its switch forces C_1 to discharge since it places a virtual ground on the top plate of C_1, as shown in Fig. 10.6(*b*). However, this discharging current must pass through C_2 and hence the charge on C_1 is added to the charge already present on C_2. Note that a positive input voltage will result in a negative voltage across C_2 and therefore a negative output voltage; thus, the integrator is an inverting integrator. At the end of ϕ_2 (once things have settled out), we can write the charge equation

$$C_2 v_{co}(nT - T/2) = C_2 v_{co}(nT - T) - C_1 v_{ci}(nT - T) \tag{10.6}$$

The negative sign in (10.6) reflects the fact that the integrator is an inverting integrator.

Although (10.6) is correct, we would like to find the charge on C_2 at the end of ϕ_1 (or equivalently, nT) as indicated by the switch shown near $v_{co}(t)$ in Fig. 10.5. To find this charge, we note that once ϕ_2 turns off, the charge on C_2 will remain the same during the next ϕ_1, until ϕ_2 turns on again in its next cycle. Therefore, the charge on C_2 at time (nT) at the end of the next ϕ_1 is equal to that at time $(nT - T/2)$, or mathematically,

$$C_2 v_{co}(nT) = C_2 v_{co}(nT - T/2) \tag{10.7}$$

and we can combine (10.6) and (10.7) to write

$$C_2 v_{co}(nT) = C_2 v_{co}(nT - T) - C_1 v_{ci}(nT - T) \tag{10.8}$$

Dividing by C_2 and using the discrete-time variables $v_i(n) = v_{ci}(nT)$ and $v_o(n) = v_{co}(nT)$, we have the following discrete-time relationship for the circuit of Fig. 10.5:

$$v_o(n) = v_o(n-1) - \frac{C_1}{C_2} v_i(n-1) \tag{10.9}$$

Taking the z-transform of (10.9), we also have

$$V_o(z) = z^{-1} V_o(z) - \frac{C_1}{C_2} z^{-1} V_i(z) \tag{10.10}$$

from which we can finally find the transfer function, $H(z)$, to be given by

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\left(\frac{C_1}{C_2}\right) \frac{z^{-1}}{1 - z^{-1}} \tag{10.11}$$

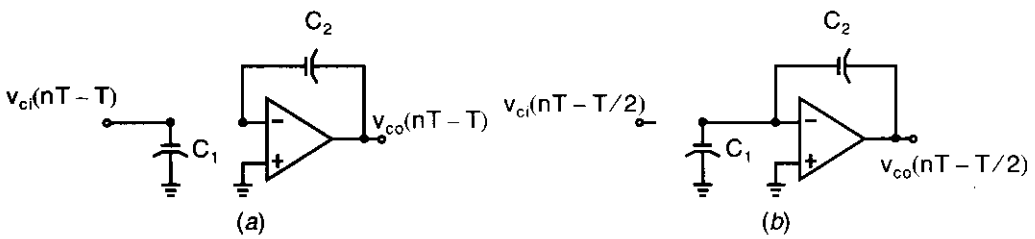


Fig. 10.6 The parasitic-sensitive integrator circuit for the two clock phases: (*a*) ϕ_1, 6(*b*) ϕ_2.

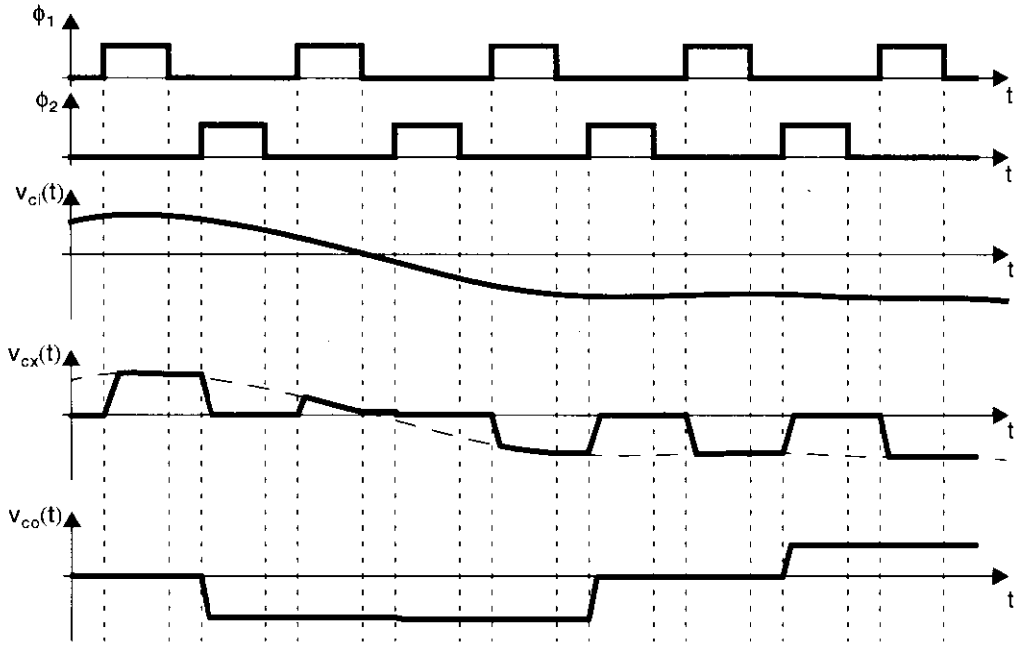


Fig. 10.7 Typical voltage waveforms for the discrete-time integrator shown in Fig. 10.5.

Note that this transfer function realizes its gain coefficient as a ratio of two capacitances, and thus the transfer function can be accurately defined in an integrated circuit. Often, the transfer function would be rewritten to eliminate terms of z having negative powers to give

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\left(\frac{C_1}{C_2}\right)\frac{1}{z-1} \tag{10.12}$$

Some typical voltage waveforms for this discrete-time integrator are shown in Fig. 10.7. Note here that the discrete-time equation derived only represents the relationship of the voltage signals $v_{ci}(t)$ and $v_{co}(t)$ at the time (nT), which occurs just before the end of ϕ_1. It does not say anything about what the voltages are at other times. In actual fact, the voltages are constant at other times (ignoring second-order effects), which is equivalent to taking the sampled voltages and then using them as inputs to a sample and hold for this particular SC integrator.

EXAMPLE 10.2

Show that for frequencies much less than the sampling frequency, equation (10.11) approximates the transfer function of an ideal continuous-time integrator.

Solution

Equation (10.11) can be rewritten as

$$H(z) = -\left(\frac{C_1}{C_2}\right)\frac{z^{-1/2}}{z^{1/2} - z^{-1/2}} \tag{10.13}$$

To find the frequency response, we make use of the fact that

$$z = e^{j\omega T} = \cos(\omega T) + j\sin(\omega T) \tag{10.14}$$

where T, the period, is one over the sampling frequency. Therefore,

$$z^{1/2} = \cos\left(\frac{\omega T}{2}\right) + j\sin\left(\frac{\omega T}{2}\right) \tag{10.15}$$

and

$$z^{-1/2} = \cos\left(\frac{\omega T}{2}\right) - j\sin\left(\frac{\omega T}{2}\right) \tag{10.16}$$

Substituting (10.15) and (10.16) into (10.13) gives

$$H(z) = -\left(\frac{C_1}{C_2}\right)\frac{z^{-1/2}}{j2\sin\left(\frac{\omega T}{2}\right)} \cong -\left(\frac{C_1}{C_2}\right)\frac{z^{-1/2}}{j\omega T} \tag{10.17}$$

for $\omega T << 1$. The $z^{-1/2}$ in the numerator represents a simple delay and can be ignored. Thus, we see that the transfer function is approximately that of a continuous-time integrator having a gain constant of

$$K_I \cong -\left(\frac{C_1}{C_2 T}\right) \tag{10.18}$$

which is a function of the integrator capacitor ratio and clock frequency only.

Thus far we have ignored the effect of the parasitic capacitances due to the creation of C_1 and C_2 as well as the nonlinear capacitances associated with the switches. The addition of such parasitic capacitances results in the circuit shown in Fig. 10.8. Here, C_{p1} represents the parasitic capacitance of the top plate of C_1 as well as the nonlinear capacitances associated with the two switches; C_{p2} represents the parasitic capacitance of the bottom plate of C_1; while C_{p3} represents the parasitic capacitance associated with the top plate of C_2, the input capacitance of the opamp, and that of the ϕ_2 switch. Finally, C_{p4} accounts for the bottom plate parasitic capacitance of C_2 as well as any extra capacitance that the opamp output must drive.

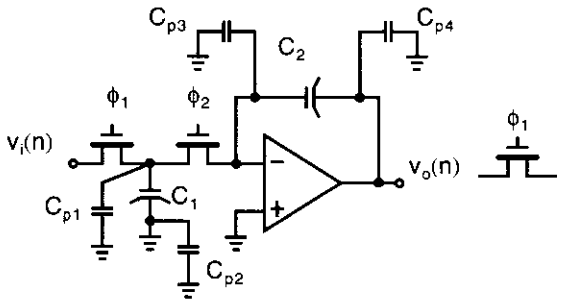


Fig. 10.8 A discrete-time integrator with parasitic capacitances shown.

In accounting for these parasitic capacitances, we can immediately discard the effect of C_{p2} since it always remains connected to ground. Similarly, the effect of C_{p3} on the transfer function is small since it is always connected to the virtual ground of the opamp. Also, C_{p4} is connected to the opamp output; therefore, although it may affect the speed of the opamp, it would not affect the final settling point of the opamp output. Finally, we note that C_{p1} is in parallel with C_1 and therefore the transfer function of this discrete-time integrator including the effects of parasitic capacitance is given by

$$H(z) = -\left(\frac{C_1 + C_{p1}}{C_2}\right)\frac{1}{z-1} \tag{10.19}$$

From (10.19), we see that the gain coefficient is related to the parasitic coefficient C_{p1}, which is not well controlled and would be partially nonlinear due to the input capacitances of the switches and top-plate parasitic capacitance. To overcome this deficiency, ingenious circuits known as parasitic-insensitive structures were developed [Martin, 1978; Allstot, 1978; Jacobs, 1978].

Parasitic-Insensitive Integrators

The parasitic-insensitive integrator was a critical development that allowed the realization of high-accuracy integrated circuits. In the first integrated integrator-based filters, the noninverting integrators (Fig. 10.9) were parasitic insensitive, whereas the inverting integrators (Fig. 10.8) were parasitic sensitive [Allstot, 1978]. The development of the parasitic-insensitive inverting integrator [Martin, 1978; Jacobs, 1978] allowed the complete filter to be insensitive, which greatly decreased second-order errors. To realize a parasitic-insensitive discrete-time integrator, two extra switches are used, as shown in Fig. 10.9. Analyzing this circuit as before, note that when ϕ_1 is on, C_1 is charged to $C_1 v_{ci}(nT - T)$, as shown in Fig. 10.10(*a*). When ϕ_2 turns on, C_1 is effectively "hooked" up backwards, and the discharge now occurs through what was the ground node rather than the input signal side, as shown in Fig. 10.10(*b*). Such

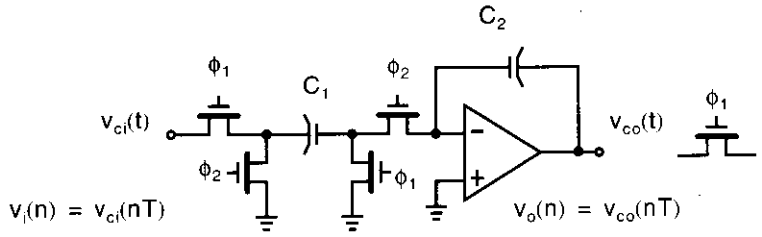


Fig. 10.9 A noninverting delaying discrete-time integrator (not sensitive to parasitic capacitances).

a reverse connection results in $v_{co}(t)$ rising for a positive $v_{ci}(nT - T)$, and therefore the integrator is noninverting. With the rest of the analysis being performed as before, the transfer function, $H(z)$, for this discrete-time integrator is given as

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = \left(\frac{C_1}{C_2}\right)\frac{z^{-1}}{1 - z^{-1}} \tag{10.20}$$

Note that (10.20) represents a positive discrete-time integrator with a full delay from input to output (due to the z^{-1} in the numerator, which represents a one-period delay) so we refer to the circuit of Fig. 10.9 as a delaying discrete-time integrator. As was done for the stray sensitive inverting integrator of Fig. 10.8, one often rewrites the transfer function to eliminate negative powers of z to give

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = \left(\frac{C_1}{C_2}\right)\frac{1}{z - 1} \tag{10.21}$$

To investigate the behavior of this noninverting integrator with respect to parasitic capacitances, consider the same circuit drawn with parasitic capacitances, as shown in Fig. 10.11. Here, C_{p3} and C_{p4} do not affect the operation of the circuit as before. In addition, C_{p2} is either connected to ground through the ϕ_1 switch or to virtual ground through the ϕ_2 switch. Therefore, since C_{p2} always remains discharged (after settling), it also does not affect the operation of the circuit. Finally, C_{p1} is continuously being charged to $v_i(n)$ and discharged to ground. However during ϕ_1 on, the fact that C_{p1} is also charged to $v_i(n - 1)$ does not affect the charge that is placed on

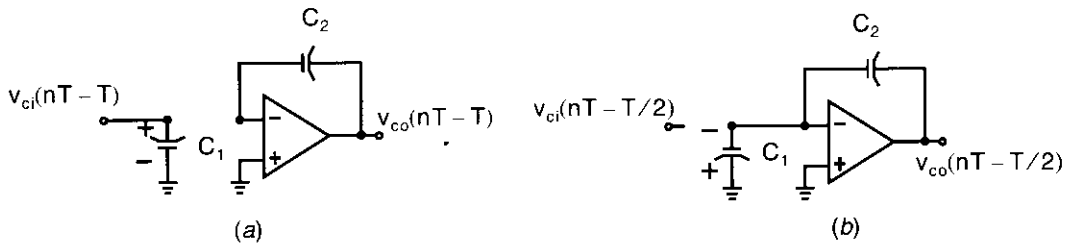


Fig. 10.10 The noninverting discrete-time integrator on the two clock phases: (*a*) ϕ_1, (*b*) ϕ_2.

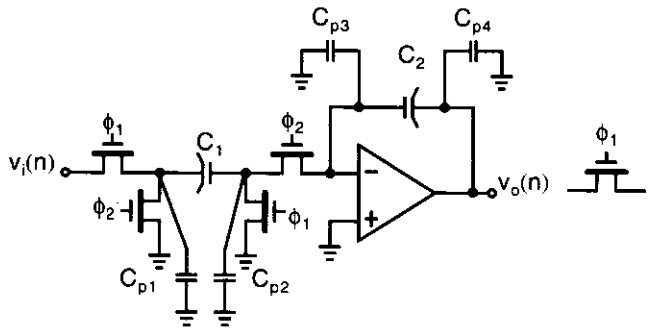


Fig. 10.11 A parasitic-insensitive integrator with parasitic capacitances shown.

C_1. When ϕ_2 is turned on, C_{p1} is discharged through the ϕ_2 switch attached to its node and none of its discharging current passes through C_1 to affect the charge accumulating on C_2. Therefore, it also does not affect the circuit operation. In summary, while the parasitic capacitances may slow down settling time behavior, they do not affect the discrete-time difference equation that occurs in the integrator shown in Fig. 10.9.

To obtain an inverting discrete-time integrator that is also parasitic insensitive, the same circuit as the parasitic-insensitive noninverting integrator can be used, but with the two switch phases on the switches near the input side of C_1 (that is, the top-plate of C_1) interchanged as shown in Fig. 10.12 [Martin, 1978]. With this arrangement, note that the charge on C_2 does not change when ϕ_2 turns on (and ϕ_1 is off). Therefore, we can write

$$C_2 v_{co}(nT - T/2) = C_2 v_{co}(nT - T) \tag{10.22}$$

Also note that C_1 is fully discharged at the end of ϕ_2 on. Now when ϕ_1 is turned on, C_1 is charged up to $v_{ci}(t)$. However, the current needed to charge C_1 passes through C_2, in effect changing the charge on C_2 by that amount. At the end of ϕ_1 on, the charge left on C_2 is equal to its old charge (before ϕ_1 was on) subtracted from the charge needed to charge up C_1 to $v_{ci}(nT)$. Thus, we have the following charge relationship:

$$C_2 v_{co}(nT) = C_2 v_{co}(nT - T/2) - C_1 v_{ci}(nT) \tag{10.23}$$

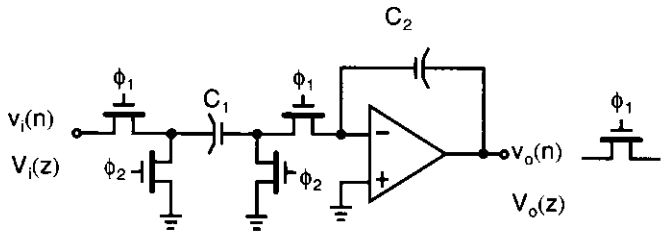


Fig. 10.12 A delay-free discrete-time integrator (not sensitive to parasitic capacitances).

Note that $v_{ci}(nT)$ occurs in the above equation rather than $v_{ci}(nT - T)$, since the charge on C_2 at the end of ϕ_1 is related to the value of $v_{ci}(nT)$ at the same time, and therefore the integrator is considered to be delay free. Substituting in (10.22), dividing by C_2, and switching to discrete-time variables, we have

$$v_o(n) = v_o(n-1) - \frac{C_1}{C_2} v_i(n) \tag{10.24}$$

Taking the z-transform of both sides, the transfer function, $H(z)$, for this delay-free integrator is found to be

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\left(\frac{C_1}{C_2}\right)\frac{1}{1 - z^{-1}} \tag{10.25}$$

where the fact that the numerator has a purely real term is indicative of the integrator being delay free. As before, (10.25) is often rewritten as

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\left(\frac{C_1}{C_2}\right)\frac{z}{z - 1} \tag{10.26}$$

Finally, note that the above delay-free integrator has a negative gain, while the delaying integrator has a positive gain. While these sign changes in the gain can be quite useful in single-ended switched-capacitor designs, many modern integrated circuits make use of fully differential signals for improved noise performance, and sign changes can be achieved by simply cross-coupling output wires.

Signal-Flow-Graph Analysis

Clearly, applying the charge equations just described would be quite tedious for larger circuits. So instead, a few rules can be developed to create and analyze such circuits. Consider the three-input integrator shown in Fig. 10.13. Using the principle of superposition, it is clear that the input-output relationships for $V_2(z)$ and $V_3(z)$ are given by

$$\frac{V_o(z)}{V_2(z)} = \left(\frac{C_2}{C_A}\right)\left(\frac{z^{-1}}{1 - z^{-1}}\right) \tag{10.27}$$

$$\frac{V_o(z)}{V_3(z)} = -\left(\frac{C_3}{C_A}\right)\left(\frac{1}{1 - z^{-1}}\right) \tag{10.28}$$

For the input $V_1(z)$, we note that its relationship to $V_o(z)$ is simply an inverting gain stage given by

$$\frac{V_o(z)}{V_1(z)} = -\left(\frac{C_1}{C_A}\right) \tag{10.29}$$

with the output once again being sampled at the end of ϕ_1 as shown.

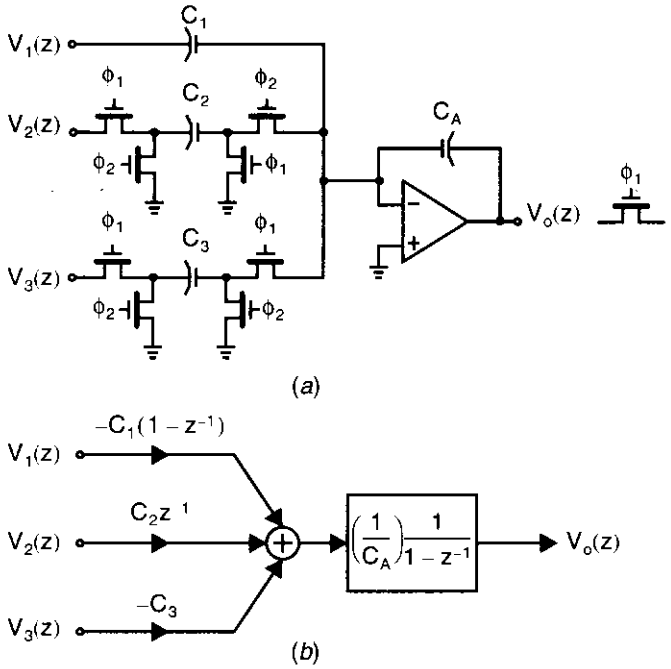


Fig. 10.13 Three-input switched capacitor summing/integrator stage. (*a*) Circuit. (*b*) Equivalent signal flow graph.

Combining (10.27), (10.28), and (10.29), the input-output relationship for the circuit of Fig. 10.13(*a*) is equal to

$$V_o(z) = -\left(\frac{C_1}{C_A}\right)V_1(z) + \left(\frac{C_2}{C_A}\right)\left(\frac{z^{-1}}{1-z^{-1}}\right)V_2(z) - \left(\frac{C_3}{C_A}\right)\left(\frac{1}{1-z^{-1}}\right)V_3(z) \qquad (10.30)$$

Such a relationship can also be represented by the signal flow graph shown in Fig. 10.13(*b*), where the input stages have been separated from the opamp stage. Thus, we see that to obtain an equivalent signal flow graph, the block $(1/C_A)[1/(1-z^{-1})]$ is used to represent the opamp stage, while three different gain factors are used to represent the possible input stages. For a nonswitched capacitor input stage, a gain factor of $-C_1(1-z^{-1})$ is used. If a delaying switched capacitor is used, it is represented by C_2z^{-1}. Finally, for a delay-free switched-capacitor input, a gain factor of $-C_3$ is used. Note, however, that the output, $V_o(z)$, should be sampled on ϕ_1 when the switched-capacitor inputs sample their input signals on ϕ_1.

As before, this transfer function might often be rewritten in powers of z rather than z^{-1}, resulting in

$$V_o(z) = -\left(\frac{C_1}{C_A}\right)V_1(z) + \left(\frac{C_2}{C_A}\right)\left(\frac{1}{z-1}\right)V_2(z) - \left(\frac{C_3}{C_A}\right)\left(\frac{z}{z-1}\right)V_3(z) \qquad (10.31)$$

10.3 FIRST-ORDER FILTERS

We saw on page 398 that at low frequencies, a switched capacitor is equivalent to a resistor. Such an equivalence is often used to derive good switched-capacitor filter structures from their active-RC counterparts. However, although such structures would behave very similarly for low-frequency input signals (when compared to the clock frequency), for signal frequencies moderately close to the clock frequency, the behavior of the switched-capacitor circuit is precisely determined through the use of the z-domain signal-flow-graph approach just discussed.

A general first-order active-RC filter is shown in Fig. 10.14. To obtain a switched-capacitor filter having the same low-frequency behavior, the resistors are replaced with delay-free switched capacitors (delay-free inputs are used since they create negative integration, as do resistive inputs), while the nonswitched capacitor feed in is left unchanged. The resulting first-order switched-capacitor filter and its equivalent signal flow graph are shown in Fig. 10.15. An equation that describes this signal flow graph is

$$C_A(1-z^{-1})V_o(z) = -C_3V_o(z) - C_2V_i(z) - C_1(1-z^{-1})V_i(z) \tag{10.32}$$

from which the transfer function for this first-order filter is found to be

$$\begin{aligned} H(z) \equiv \frac{V_o(z)}{V_i(z)} &= -\frac{\left(\frac{C_1}{C_A}\right)(1-z^{-1}) + \left(\frac{C_2}{C_A}\right)}{1 - z^{-1} + \frac{C_3}{C_A}} \\ &= -\frac{\left(\frac{C_1 + C_2}{C_A}\right)z + \frac{C_1}{C_A}}{\left(1 + \frac{C_3}{C_A}\right)z - 1} \end{aligned} \tag{10.33}$$

The pole of (10.33) is found by equating the denominator to zero, which results in a pole location, z_p, given by

$$z_p = \frac{C_A}{C_A + C_3} \tag{10.34}$$

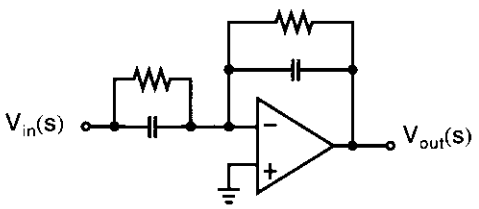


Fig. 10.14 A first-order active-RC filter.

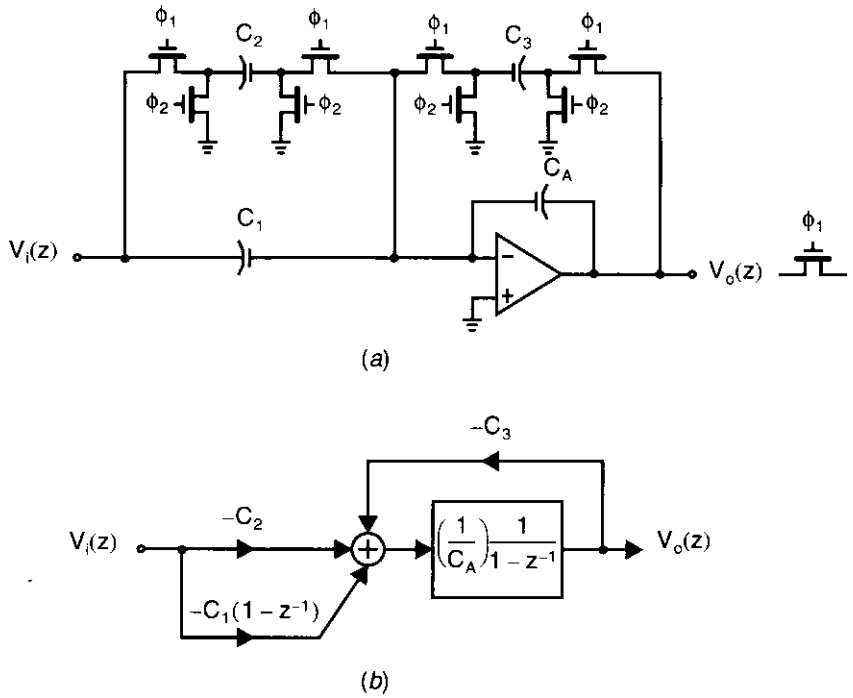


Fig. 10.15 A first-order switched-capacitor filter: (*a*) circuit (no switch sharing), (*b*) equivalent signal flow graph.

Note that for positive capacitance values, this pole is restricted to the real axis between zero and one, and therefore the circuit is always stable. In fact, with $C_3 = 0$ the circuit's pole is at $z = 1$ or, in other words, it becomes a discrete-time integrator, as expected. The zero of (10.33) is found by equating the numerator to zero, which results in a zero location, z_z, given by

$$z_z = \frac{C_1}{C_1 + C_2} \tag{10.35}$$

Therefore, for positive capacitance values, this zero location is also restricted to the real axis between zero and one. Additionally, the dc gain for this circuit is found by setting $z = 1$, which results in the dc gain being given by

$$H(1) = \frac{-C_2}{C_3} \tag{10.36}$$

Finally, it should be noted that in a fully differential implementation, effective negative capacitances for C_1, C_2, and C_3 can be achieved by simply interchanging the input wires. In this way, a zero at $z = -1$ could be realized by setting

$$C_1 = -0.5C_2 \tag{10.37}$$

In other words, the pair of capacitors representing C_1 would be half the size of those representing C_2 and the input wires interchanged into the C_1 pair such that $-V_i(z)$ is applied to that input branch.

EXAMPLE 10.3

Find the capacitance values needed for a first-order switched-capacitor circuit such that its 3-dB point is at 10 kHz when a clock frequency of 100 kHz is used. It is also desired that the filter have zero gain at 50 kHz and the dc gain be unity. Assume $C_A = 10$ pF.

Solution

First note that having a zero gain at 50 kHz is equivalent to placing a zero at -1. Now, making use of the bilinear transform $p = (z-1)/(z+1)$ as described in Section 9.5, the zero at -1 is mapped to $\Omega = \infty$. In addition, the frequency warping between the two domains, $\Omega = \tan(\omega/2)$, maps the –3-dB frequency of 10 kHz (or 0.2π rad/sample) in the z-domain to

$$\Omega = \tan\left(\frac{0.2\pi}{2}\right) = 0.3044$$

in the continuous-time domain. Therefore, our specification is now simplified to find the pole location for a continuous-time filter having a –3-dB frequency equal to 0.3044 rad/s and a zero at ∞. Clearly, the continuous-time pole, p_p, required here is

$$p_p = -0.3044$$

This pole is mapped back to a z-domain pole, z_p, of value

$$z_p = \frac{1+p_p}{1-p_p} = 0.53327$$

Therefore, the desired discrete-time transfer function, $H(z)$, is given by

$$H(z) = \frac{k(z+1)}{z-0.53327}$$

where k is determined by setting the dc gain to one (i.e., $H(1) = 1$) resulting in

$$H(z) = \frac{0.23337(z+1)}{z-0.53327}$$

or equivalently,

$$H(z) = \frac{0.43762z + 0.43762}{1.87522z - 1}$$

Equating these coefficients with those of (10.33) (and assuming $C_A = 10$ pF) results in

$$C_1 = 4.376 \text{ pF}$$
$$C_2 = -8.752 \text{ pF}$$
$$C_3 = 8.752 \text{ pF}$$

where a differential input can realize the negative capacitance.

For designs where the zero and pole frequencies are substantially less than the clock frequency (unlike the previous example, which had a zero at one-half the clock frequency), it is not necessary to pre-warp the specifications using the bilinear transform. Rather, some approximations can be used to derive equations for the capacitor ratios given the desired zero and pole, which are both assumed to be real and positive. As in Example 10.2, using (10.33), we have

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\frac{\left(\frac{C_1}{C_A}\right)(z^{1/2} - z^{-1/2}) + \left(\frac{C_2}{C_A}\right)z^{1/2}}{z^{1/2} - z^{-1/2} + \frac{C_3}{C_A}z^{1/2}} \tag{10.38}$$

Substituting (10.15) and (10.16) into (10.38) gives

$$H(e^{j\omega T}) \equiv \frac{V_o(e^{j\omega T})}{V_i(e^{j\omega T})} = -\frac{j\frac{2C_1 + C_2}{C_A}\sin\left(\frac{\omega T}{2}\right) + \frac{C_2}{C_A}\cos\left(\frac{\omega T}{2}\right)}{j\left(2 + \frac{C_3}{C_A}\right)\sin\left(\frac{\omega T}{2}\right) + \frac{C_3}{C_A}\cos\left(\frac{\omega T}{2}\right)} \tag{10.39}$$

This transfer function is exact. Making the approximation $\omega T << 1$ allows (10.39) to be simplified as

$$H(e^{j\omega T}) \equiv \frac{V_o(e^{j\omega T})}{V_i(e^{j\omega T})} = \frac{j\left(\frac{C_1 + C_2/2}{C_A}\right)\omega T + \frac{C_2}{C_A}}{j\left(1 + \frac{C_3}{2C_A}\right)\omega T + \frac{C_3}{C_A}} \tag{10.40}$$

The procedure just used is quite useful when finding a continuous-time transfer function that approximates a discrete-time transfer function. Setting the numerator of (10.40) to zero gives the following approximate equation for the zero frequency:

$$j\omega_z T = \frac{-C_2/C_1}{1 + \frac{C_2}{2C_1}} \tag{10.41}$$

Similarly, setting the denominator to zero gives the following approximate equation for the pole frequency:

$$j\omega_p T = \frac{-C_3/C_A}{1 + \dfrac{C_3}{2C_A}} \tag{10.42}$$

EXAMPLE 10.4

Find the capacitance values C_1 needed for a first-order low-pass switched-capacitor filter that has $C_1 = 0$ and a pole at the 1/64th sampling frequency using the approximate equations. The low-frequency gain should be unity.

Solution

Using (10.42) and solving for C_3/C_A, we have

$$\frac{C_3}{C_A} = \frac{\omega_p T}{1 - \omega_p T/2} = \frac{2\pi/64}{1 - 2\pi/128} = 0.1032 \tag{10.43}$$

If we choose $C_A = 10$ pF, then we have $C_3 = 1.032$ pF. From (10.40) with $C_1 = 0$, we see that the low-frequency gain is given by C_2/C_3. For unity gain, this means we need $C_2 = 1.032$ pF as well.

Switch Sharing

Careful examination of the switched-capacitor filter shown in Fig. 10.15(*a*) reveals that some of the switches are redundant. Specifically, the top plate of both C_2 and C_3 are always switched to the opamp's virtual ground and true ground at the same time. Therefore, one pair of these switches can be eliminated and the two top plates of C_2 and C_3 can be connected together, as shown in Fig. 10.16.

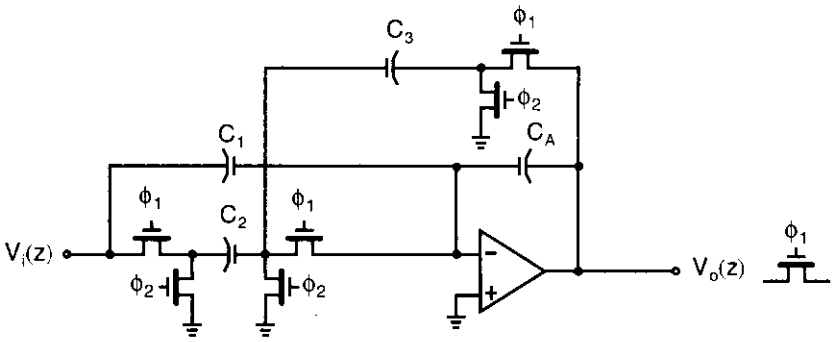


Fig. 10.16 A first-order switched-capacitor filter with switch sharing.

Fully Differential Filters

While the circuits seen so far have all been shown with single-ended signals, in most analog applications it is desirable to keep the signals fully differential. Fully differential signals imply that the *difference between two lines represents the signal component,* and thus any noise which appears as a common-mode signal on those two lines does not affect the signal. Fully differential circuits should also be balanced, implying that the differential signals operate symmetrically around a dc common-mode voltage (typically, analog ground or halfway between the power-supply voltages). Having balanced circuits implies that it is more likely noise will occur as a common-mode signal due to the symmetry of the circuit. Fully differential circuits have the additional benefit that if each single-ended signal is distorted symmetrically around the common-mode voltage, the differential signal will have only odd-order distortion terms (which are often much smaller). To see this distortion improvement, consider the block diagram shown in Fig. 10.17, where the two nonlinear elements are identical and, for simplicity, the common-mode voltage is assumed to be zero. If the nonlinearity is memoryless, then the outputs can be found as a Taylor series expansion given by

$$v_o = k_1 v_i + k_2 v_i^2 + k_3 v_i^3 + k_4 v_i^4 + \cdots \tag{10.44}$$

where k_i are constant terms. In this case, the differential output signal, v_{diff}, consists of only the linear term, $2k_1v_1$, and odd-order distortion terms (which are typically smaller than the second-order term). With these two important advantages, most modern switched-capacitor circuits are realized using fully differential structures.

A fully differential realization of the first-order filter is shown in Fig. 10.18. Note here that the fully differential version is essentially two copies of the single-ended version, which might lead one to believe that it would consume twice the amount of integrated area. Fortunately, the increased area penalty is not that high. First, we see that only one opamp is needed although it does require extra common-mode feedback circuitry. Secondly, note that the input and output signal swings have now been doubled in size. For example, if single-ended signals are restricted to ±1 V, then the maximum peak-to-peak signal swing of single-ended signals is 2 V, while for differential signals it is 4 V. Thus, to maintain the same dynamic range due to $(kT)/C$ noise, the

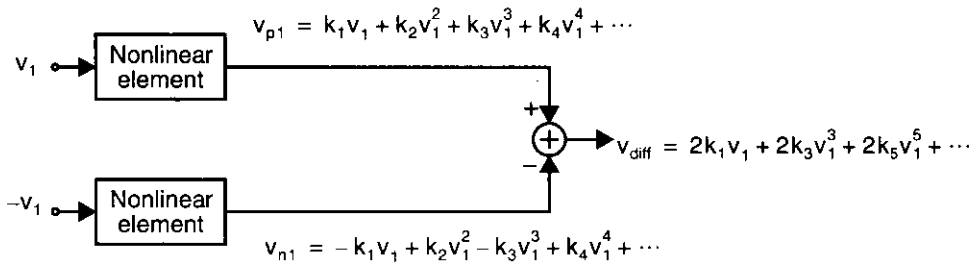


Fig. 10.17 Demonstrating that even-order distortion terms cancel in fully differential circuits if the distortion is symmetrical around the common-mode voltage. Here, the common-mode voltage is assumed to be zero.

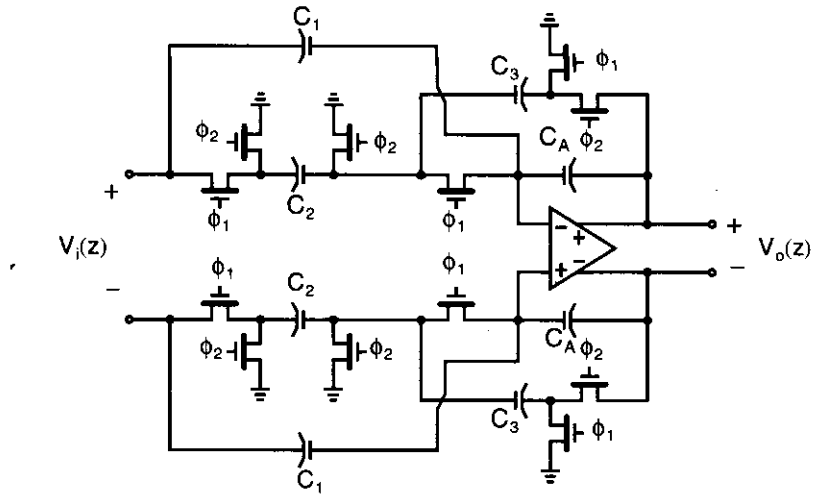


Fig. 10.18 A fully differential first-order switched-capacitor filter.

capacitors in the fully differential version can be half the size of those in the single-ended case.[4] Since smaller capacitors can be used, the switch size widths may also be reduced to meet the same settling-time requirement. However, the fully differential circuit has more switches and wiring so this circuit will be somewhat larger than its single-ended counterpart. However, recall that the fully differential circuit has the advantages of rejecting much more common-mode noise signals as well as having better distortion performance.

10.4 BIQUAD FILTERS

Similar to the first-order case, good switched-capacitor biquad filter structures can be obtained by emulating well-known continuous-time filter structures. However, also as in the first-order case, once a filter structure is obtained, its precise frequency response is determined through the use of discrete-time analysis using the signal-flow-graph technique discussed in Section 10.2. This exact transfer function, or a close approximation to it, is then used when determining capacitor ratios during the design phase.

Low-Q Biquad Filter

A direct-form continuous-time biquad structure can be obtained by rewriting the general biquad transfer function, $H_a(s)$, as follows:

4. When the signal voltage doubles, the signal power goes up by a factor of four. Fully differential circuits would have twice the noise power of single-ended circuits having the same size capacitors due to there being two capacitive networks generating noise. Halving the capacitor size of the differential circuit would result in another doubling in noise power, resulting in a signal-to-noise ratio equal to that of a single-ended circuit having capacitors twice as large.

$$H_a(s) \equiv \frac{V_{out}(s)}{V_{in}(s)} = -\frac{k_2 s^2 + k_1 s + k_0}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2} \tag{10.45}$$

Here, ω_0 and Q are the pole frequency and pole Q, respectively, whereas k_0, k_1, and k_2 are arbitrary coefficients that place this biquad's zeros (i.e., the numerator's roots). Multiplying through by the denominators and dividing by s^2, (10.45) can be written as

$$V_{out}(s) = \left[-k_2 - \frac{k_1}{s}\right]V_{in}(s) - \frac{\omega_0}{Qs}V_{out}(s) - \frac{k_0}{s^2}V_{in}(s) - \frac{\omega_0^2}{s^2}V_{out}(s) \tag{10.46}$$

Finally, (10.46) can be expressed as two integrator-based equations. Specifically,

$$V_{c1}(s) \equiv -\frac{1}{s}\left[\frac{k_0}{\omega_0}V_{in}(s) + \omega_0 V_{out}(s)\right] \tag{10.47}$$

and

$$V_{out}(s) = -\frac{1}{s}\left[(k_1 + k_2 s)V_{in}(s) + \frac{\omega_0}{Q}V_{out}(s) - \omega_0 V_{c1}(s)\right] \tag{10.48}$$

A signal flow graph describing the preceding two equations is shown in Fig. 10.19.

Now, allowing negative resistors to be used, an active-RC realization of this general biquad signal flow graph is shown in Fig. 10.20 [Brackett, 1978]. Note that for convenience the integrating capacitors, C_A and C_B, have been set to unity.

A switched-capacitor biquad based on this active-RC circuit can be realized as shown in Fig. 10.21 [Martin, 1979]. Here, all positive resistors were replaced with delay-free feed-in switched-capacitor stages while the negative resistor was replaced with a delaying feed-in stage. Note that this switched-capacitor biquad circuit has redundant switches, as switch sharing has not yet been applied.

The input capacitor K_1C_1 is the major signal path when realizing low-pass filters; the input capacitor K_2C_2 is the major signal path when realizing bandpass filters; whereas, the input capacitor K_3C_2 is the major signal path when realizing high-pass filters.

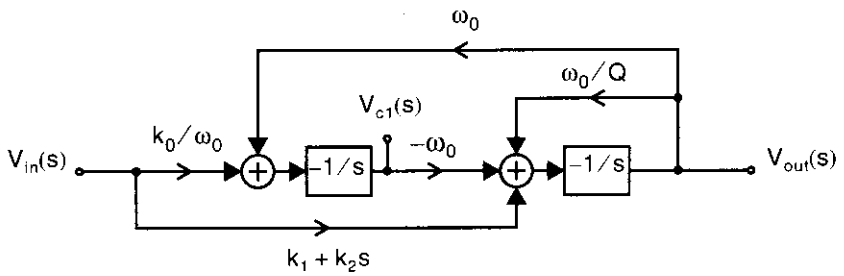


Fig. 10.19 A signal-flow-graph representation of a general continuous-time biquad filter.

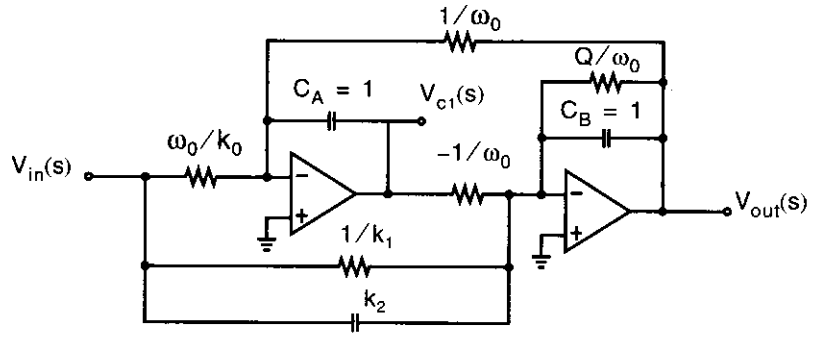


Fig. 10.20 An active-RC realization of a general continuous-time biquad filter.

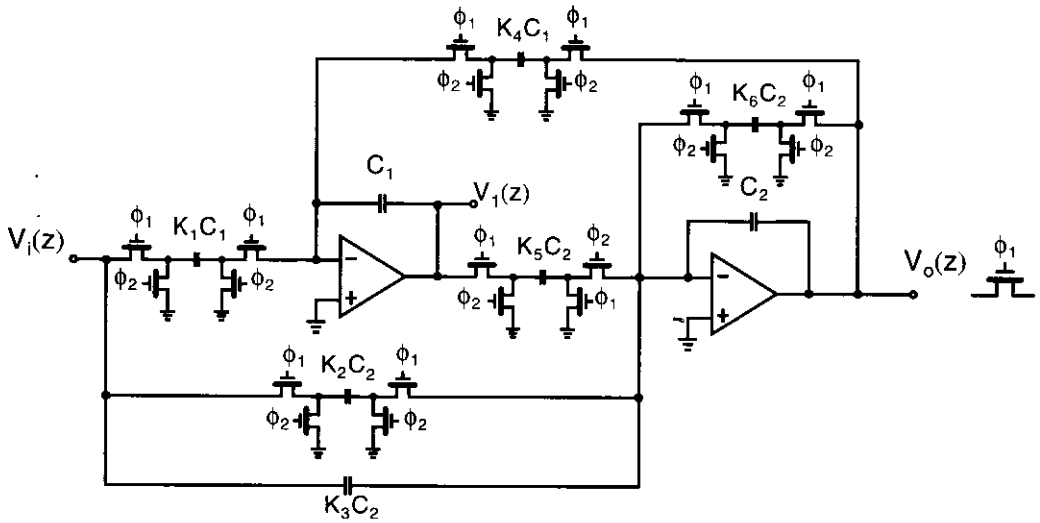


Fig. 10.21 A low-Q switched-capacitor biquad filter (without switch sharing).

Before proceeding, it is worth mentioning that while this switched-capacitor filter is a natural result when using single-ended circuits, the use of fully differential circuits could result in quite a few other circuits, some of which could have poor performance properties. For example, all the positive resistors could be replaced with delay-free feed-in stages as before, but in addition, the negative resistor could also be replaced with a delay-free feed-in stage where the differential input wires are interchanged. Such a circuit would have a delay-free loop around the two integrators and may have an excessive settling time behavior. As another example, all resistors might be replaced with delaying feed-in stages where positive resistors are realized by interchanging the input wires of those stages. In this case, settling time behavior would not suffer as there would be two delays around the two-integrator loop, but coefficient sensitivity would be worse for filters having high-Q poles. In summary, what is important is that the two-integrator loop have a single delay

around the loop. Such an arrangement is referred to as using lossless discrete integrators (LDI) [Bruton, 1975].

Using the approach presented in Section 10.2, the signal flow graph for the biquad circuit shown in Fig. 10.21 can be found and is shown in Fig. 10.22. The transfer function, $H(z)$, for this signal flow graph is found to be given by

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\frac{(K_2 + K_3)z^2 + (K_1K_5 - K_2 - 2K_3)z + K_3}{(1 + K_6)z^2 + (K_4K_5 - K_6 - 2)z + 1} \tag{10.49}$$

While the preceding relation is useful for analyzing the switched-capacitor circuit shown, this relation can also be used during design of a desired transfer function. Assuming the desired discrete-time biquad transfer function has been found using a digital-filter design program, and is given by

$$H(z) = -\frac{a_2z^2 + a_1z + a_0}{b_2z^2 + b_1z + 1} \tag{10.50}$$

we can equate the individual coefficients of z in (10.49) and (10.50), resulting in the following design equations:

$$K_3 = a_0 \tag{10.51}$$

$$K_2 = a_2 - a_0 \tag{10.52}$$

$$K_1K_5 = a_0 + a_1 + a_2 \tag{10.53}$$

$$K_6 = b_2 - 1 \tag{10.54}$$

$$K_4K_5 = b_1 + b_2 + 1 \tag{10.55}$$

Note that there is some flexibility in choosing the values of K_1, K_4, and K_5. This single degree of freedom occurs because specifying the overall transfer function, $H(z)$, places no constraint on the size of the signal at the internal node, $V_1(z)$. Thus, one way to choose appropriate capacitor values is to initially let $K_5 = 1$ and determine other initial component values, find the signal levels that occur at nodes $V_1(z)$

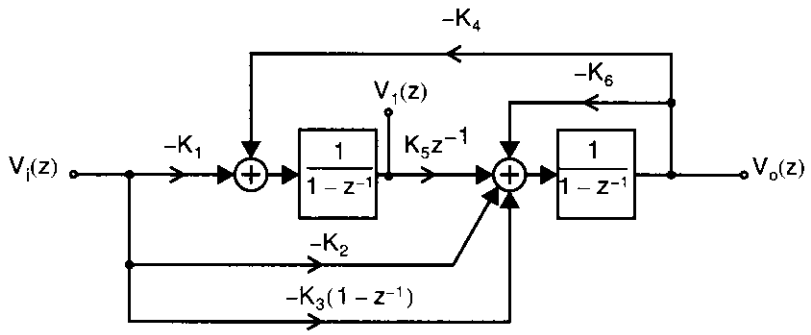


Fig. 10.22 A signal flow graph describing the switched-capacitor circuit in Fig. 10.21.

and $V_o(z)$, then using that signal level information, perform dynamic range scaling to find the final component values. Alternatively, the time constants of the two discrete-time integrators can be set equal by choosing

$$K_4 = K_5 = \sqrt{b_1 + b_2 + 1} \tag{10.56}$$

Such a choice usually results in a near optimal dynamically range-scaled circuit.

If it is desired to design the SC biquad so that its transfer function matches that of a continuous-time transfer function as closely as possible, then the approach used in Example 10.2 can be taken. Specifically, (10.49) can be rewritten as

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\frac{K_1K_5 + K_2(z^{1/2} - z^{-1/2})z^{1/2} + K_3(z^{1/2} - z^{-1/2})^2}{K_4K_5 + K_6(z^{1/2} - z^{-1/2})z^{1/2} + (z^{1/2} - z^{-1/2})^2} \tag{10.57}$$

Rewriting (10.15) and (10.16) here for convenience, we have

$$z^{1/2} = \cos\left(\frac{\omega T}{2}\right) + j\sin\left(\frac{\omega T}{2}\right) \tag{10.58}$$

and

$$z^{-1/2} = \cos\left(\frac{\omega T}{2}\right) - j\sin\left(\frac{\omega T}{2}\right) \tag{10.59}$$

Substituting these equations into (10.57) and rearranging gives

$$H(e^{j\omega T}) \equiv \frac{V_o(e^{j\omega T})}{V_i(e^{j\omega T})} = -\frac{K_1K_5 + jK_2\sin(\omega T) + (4K_3 + 2K_2)\sin^2\left(\frac{\omega T}{2}\right)}{K_4K_5 + jK_6\sin(\omega T) + (4 + 2K_6)\sin^2\left(\frac{\omega T}{2}\right)} \tag{10.60}$$

For $\omega T << 1$, we further have

$$H(e^{j\omega T}) \equiv \frac{V_o(e^{j\omega T})}{V_i(e^{j\omega T})} \approx -\frac{K_1K_5 + jK_2(\omega T) + (K_3 + K_2/2)(\omega T)^2}{K_4K_5 + jK_6(\omega T) + (1 + K_6/2)(\omega T)^2} \tag{10.61}$$

The coefficients of (10.61) can be matched to the desired coefficients of the continuous-time transfer function. A closer matching between transfer functions can be obtained if one chooses capacitor ratios to match the real and imaginary parts of both the numerators and denominators of (10.60) and the desired continuous-time transfer function at the resonant frequency, as is outlined in [Martin, 1980].

Finally, an estimate of the largest to smallest capacitance ratio can be made by using the resistor approximation (10.5) for this switched-capacitor circuit. Comparing Fig. 10.20 and Fig. 10.21 and using (10.5), we see the following approximations are valid for the feedback capacitor ratios, K_4, K_5, and K_6 (the capacitor ratios that determine the pole locations).

$$K_4 \cong K_5 \cong \omega_0 T \tag{10.62}$$

$$K_6 \cong \frac{\omega_0 T}{Q} \tag{10.63}$$

However, the sampling rate, $1/T$, is typically much larger that the approximated pole frequency, ω_0, resulting in

$$\omega_0 T << 1 \tag{10.64}$$

Thus, the largest capacitors (that determine the pole locations) in the switched-capacitor biquad circuit of Fig. 10.21 are the integrating capacitors, C_1 and C_2. Additionally, if $Q < 1$, then the smallest capacitors are K_4C_1 and K_5C_2, resulting in an approximate capacitance spread of $1/(\omega_0 T)$. However, if $Q > 1$, then from (10.63) the smallest capacitor would be K_6C_2, resulting in an approximate capacitance spread of $Q/(\omega_0 T)$.

High-Q Biquad Filter

The resultant high-capacitance spread in the preceding low-Q circuit, when $Q >> 1$, was a direct result of having a large damping resistance value of Q/ω_0 in Fig. 10.20. One way to obtain a high-Q switched-capacitor circuit that does not have such a high capacitance spread is to eliminate this damping resistance in the continuous-time filter counterpart. Such an elimination can be accomplished by rewriting (10.46) as

$$V_{out}(s) = -\frac{1}{s}[k_2 s V_{in}(s) - \omega_0 V_{c1}(s)] \tag{10.65}$$

and

$$V_{c1}(s) = -\frac{1}{s}\left[\left(\frac{k_0}{\omega_0} + \frac{k_1 s}{\omega_0}\right)V_{in}(s) + \omega_0 V_{out}(s) + \frac{s}{Q}V_{out}(s)\right] \tag{10.66}$$

The signal-flow-graph representation of these two equations is shown in Fig. 10.23. Note that here the damping path, s/Q coefficient, passes through the first integrator stage and can be realized through the use of a capacitor, as shown in Fig. 10.24.

Once again, replacing resistors with appropriate switched-capacitor feed-in stages, the final high-Q switched-capacitor biquad circuit is shown in Fig. 10.25 [Martin, 1980].

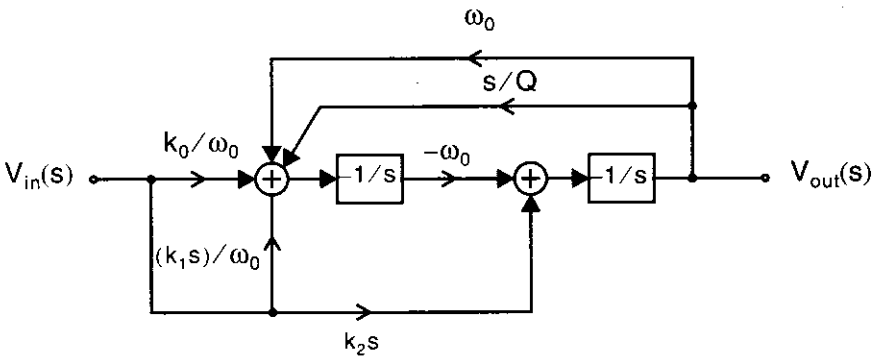


Fig. 10.23 An alternate realization for a general continuous-time biquad filter.

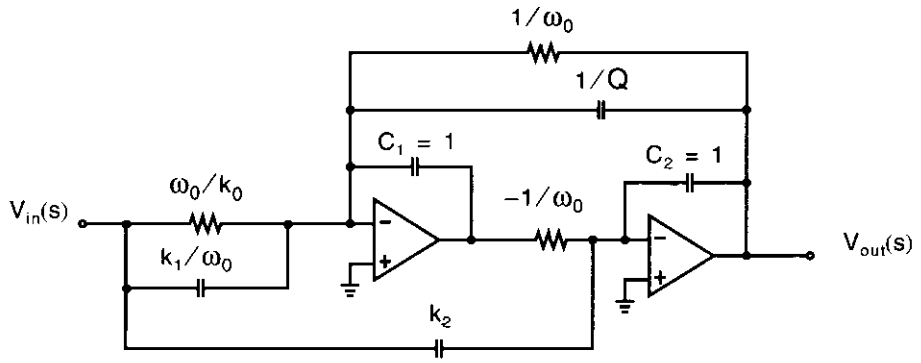


Fig. 10.24 An alternate realization of a general active-RC biquad filter.

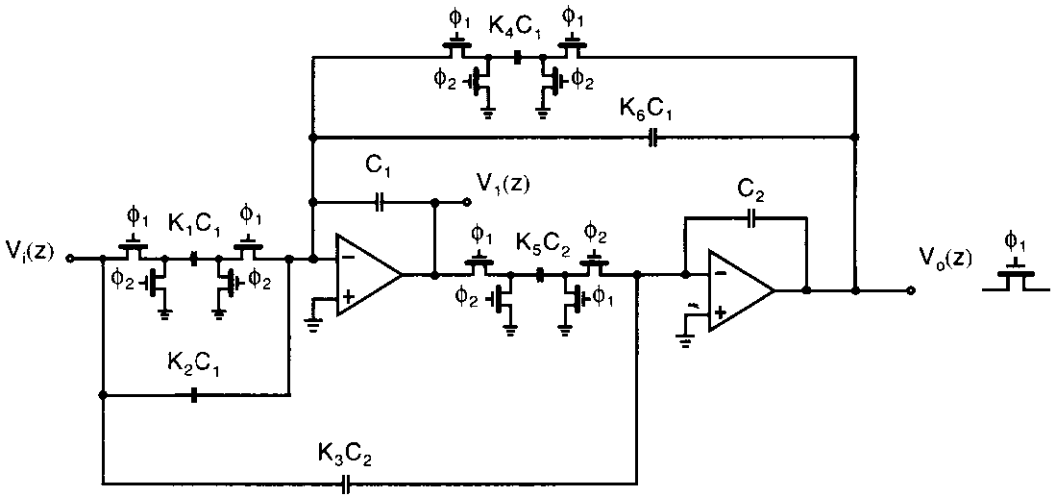


Fig. 10.25 A high-Q switched-capacitor biquad filter (without switch sharing).

The input capacitor K_1C_1 is the major signal path when realizing low-pass filters, the input capacitor K_2C_2 is the major signal path when realizing bandpass filters, and the input capacitor K_3C_2 is the major signal path when realizing high-pass filters. Other possibilities for realizing different types of functions exist. For example, a non-delayed switched capacitor going from the input to the second integrator could also be used to realize an inverting bandpass function. If the phases on the input switches of such a switched capacitor were interchanged, then a noninverting bandpass function would result, but with an additional period delay.

Using the signal-flow-graph approach described in Section 10.2, the transfer function for this circuit is found to be given by

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\frac{K_3z^2 + (K_1K_5 + K_2K_5 - 2K_3)z + (K_3 - K_2K_5)}{z^2 + (K_4K_5 + K_5K_6 - 2)z + (1 - K_5K_6)} \tag{10.67}$$

Matching the coefficients of (10.67) to the coefficients of a discrete-time transfer function given by[5]

$$H(z) = -\frac{a_2 z^2 + a_1 z + a_0}{z^2 + b_1 z + b_0} \tag{10.68}$$

the following equations result:

$$K_1 K_5 = a_0 + a_1 + a_2 \tag{10.69}$$

$$K_2 K_5 = a_2 - a_0 \tag{10.70}$$

$$K_3 = a_2 \tag{10.71}$$

$$K_4 K_5 = 1 + b_0 + b_1 \tag{10.72}$$

$$K_5 K_6 = 1 - b_0 \tag{10.73}$$

As for the low-Q biquad, we see that there is some freedom in determining the coefficients as there is one less equation than the number of coefficients. A reasonable first choice might be to take

$$K_4 = K_5 = \sqrt{1 + b_0 + b_1} \tag{10.74}$$

after which all other ratios follow. This will give a good dynamic range but not necessarily optimum. After the biquad has been designed, it can be analyzed and the ratios adjusted to equalize the maximum signal strength at the two opamp outputs.

EXAMPLE 10.5

The following transfer function describes a bandpass filter having a peak gain of 5 near $f_s/10$ and a Q of about 10.

$$H(z) = -\frac{0.288(z-1)}{z^2 - 1.572z + 0.9429} \tag{10.75}$$

Find the largest to smallest capacitor ratio if this transfer function is realized using the high-Q biquad circuit. Compare the results to those which would be obtained if the low-Q circuit were used instead. Let $C_1 = C_2 = 1$ in both cases.

Solution

For the high-Q biquad circuit, making use of (10.69) to (10.72) and assuming $K_4 = K_5$ results in the following capacitor values.

$$K_4 = K_5 = 0.6090$$

$$K_1 = 0$$

$$K_2 = 0.4729$$

5. Note that (10.68) is written in slightly different form than (10.50) to simplify the resulting equations.

$$K_3 = 0$$

$$K_6 = 0.0938$$

Recalling that $C_1 = C_2 = 1$, in this high-Q circuit the smallest capacitor is $K_6 C_1$, which makes the capacitance spread about 11 to 1.

For the low-Q biquad circuit design, we first rewrite (10.75) as

$$H(z) = -\frac{0.3054(z-1)\,z}{1.0606z^2 - 1.667z + 1} \tag{10.76}$$

which makes applying equations (10.51) to (10.56) easier. In addition, an extra zero at $z = 0$ was added to avoid negative capacitances. This extra zero does not change the magnitude response.

We obtain the following ratios assuming $K_4 = K_5$:

$$K_4 = K_5 = 0.6274 \tag{10.77}$$

$$K_1 = 0 \tag{10.78}$$

$$K_2 = 0.3054 \tag{10.79}$$

$$K_3 = 0 \tag{10.80}$$

$$K_6 = 0.0606 \tag{10.81}$$

Thus the capacitance ratio for this circuit is determined by K_6, which primarily sets the accuracy of the pole-Q factor, resulting in a spread of near 17. It should be noted here that worse capacitance spreads will occur for this low-Q circuit if the pole Q is higher and/or the sampling frequency is increased relative to the passband edge.

There are many other biquadratic stages than the two presented here. For example, a general stage capable of realizing any z-transform is described in [Laker, 1994]. However, the authors have found that for the great majority of filtering applications, the choice of the circuits of either Fig. 10.21 or Fig. 10.25 (with switch sharing) is nearly optimum. The exception to this is for phase equalizers, where often feed-ins approximating negative resistors are needed. To realize higher-order switched-capacitor filters, one can cascade a number of biquad and/or first-order stages. Alternatively, one can use lower-sensitivity techniques such as signal-flow-graph simulations of the relationships between the state variables of passive doubly terminated LC ladder filters. The interested reader is referred to [Gregorian, 1986] for detailed descriptions on the design of high-order SC filters.

10.5 CHARGE INJECTION

As seen in Chapter 7, comparators that make use of switches suffer from charge-injection errors. Fortunately, by turning off certain switches first, the charge-injection

errors of the overall circuit are due to only those early switches. This same result applies to switched-capacitor circuits, and thus charge-injection effects can be minimized by having some clock signals slightly advanced with respect to the remaining signals. Which clock signals should be advanced is most easily explained with the following example.

Consider the first-order switched-capacitor filter shown in Fig. 10.26, where switch sharing is used. Here, ϕ_{1a} and ϕ_{2a} are slightly advanced with respect to the remaining clock signals for the following reasons. First, since ϕ_{2a} is always connected to ground while ϕ_{1a} is always connected to virtual ground, when these switches are turned on they need only pass a signal near the ground node (not rail-to-rail signals as might occur at opamp outputs). Thus, these two switches can be realized using single n-channel transistors rather than full CMOS transmission gates.[6] A second, more important reason for using this clock arrangement is that the charge injections due to Q_3, Q_4 are not signal dependent, while those of Q_1, Q_6 are signal dependent. Specifically, we saw in Chapter 7 that the channel charge of an NMOS transistor in triode is given by

$$Q_{CH} = -WLC_{ox}V_{eff} = -WLC_{ox}(V_{GS} - V_t) \tag{10.82}$$

Here, we see that the charge is related to the gate-source voltage as well as to the threshold voltage. When Q_3 and Q_4 are on, $V_{GS} = V_{DD}$, and since their source remains at zero volts, their threshold voltages also remain constant. As a result, *the amount of charge injected by* Q_3, Q_4 *is the same from one clock cycle to the next and can be considered as a dc offset.* Unfortunately, the same cannot be said of Q_1 and Q_6. For example, when Q_1 is on, its channel charge is found from (10.82) to be

$$Q_{CH1} = -W_1L_1C_{ox}(V_{DD} - V_i - V_{tn}) \tag{10.83}$$

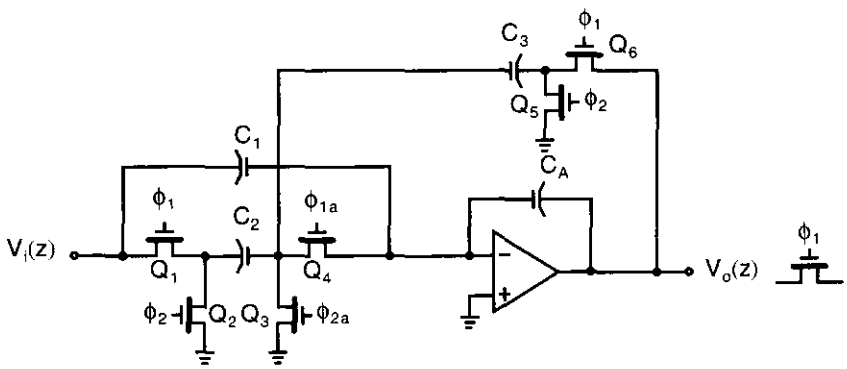


Fig. 10.26 A first-order switched-capacitor circuit with a clock arrangement to reduce charge-injection effects. ϕ_{1a} and ϕ_{2a} turn off Q_3 and Q_4 slightly early.

6. Typically, switches Q_1, Q_6 would be realized as CMOS transmission gates since they may need to pass large-swing signals.

Thus, one portion of the channel charge is linearly related to V_i. However, its source voltage settles to V_i and thus the transistor's threshold voltage changes in a nonlinear relationship (due to the bulk effect, assuming its substrate is set to a fixed voltage). As a result, Q_{CH1} has a linear and nonlinear relationship to V_i and thus would cause a gain error and distortion if Q_1 were turned off early. Finally, while Q_2 and Q_5 would also inject constant charge from one cycle to the next, it is best not to add any unnecessary charge into the circuit so these switches are also not advanced.

In summary, to reduce the effects of charge injection in switched-capacitor circuits, realize all switches connected to ground or virtual ground as n-channel switches only, and turn off the switches near the virtual ground node of the opamps first. Such an approach will minimize distortion and gain error as well as keeping dc offset low.

EXAMPLE 10.6

Assuming an ideal opamp, estimate the amount of dc offset in the output of the circuit shown in Fig. 10.26 due to channel-charge injection (ignore overlap capacitance charge injection) when $C_1 = 0$ and $C_2 = C_A = 10C_3 = 10$ pF. Assume that switches Q_3, Q_4 are n-channel devices with a threshold voltage of $V_{tn} = 0.8$ V, width of $W = 30\ \mu$m, length of $L = 0.8\ \mu$m, $C_{ox} = 1.9 \times 10^{-3}$ pF/μm^2, and that power supplies of ± 2.5 V are used.

Solution

From (10.82), we can calculate the amount of channel charge of Q_3, Q_4 (when on) to be

$$\begin{aligned} Q_{CH3} &= Q_{CH4} \\ &= -(30)(0.8)(0.0019)(2.5 - 0.8) = -77.5 \times 10^{-3}\ \text{pC} \end{aligned} \tag{10.84}$$

Note that the dc feedback around the opamp will keep the virtual input of the opamp at zero volts. Also, all of the dc feedback current is charge transferred through the switched capacitor C_3. Thus, the charge being transferred through this capacitor must equal the charge injected by both Q_3, Q_4 (assuming the input is at zero volts and therefore does not contribute charge). The charge transfer into C_3 is given by

$$Q_{C_3} = -C_3 v_{out} \tag{10.85}$$

Now, we estimate that half the channel charges of Q_3 and Q_4 are injected to the virtual ground node by the following reasoning. When ϕ_{1a} turns off, half the channel charge of Q_4 goes into the virtual ground while half of its charge is placed at the node between Q_3 and Q_4. When ϕ_{2a} goes high, the second charge escapes to ground, but when ϕ_{2a} goes low, half of its channel charge is left between Q_3 and Q_4 and is passed into the virtual ground when ϕ_{1a} goes high again. As a result, we can write the following charge equation,

$$\frac{1}{2}(Q_{CH3} + Q_{CH4}) = Q_{C_3} \tag{10.86}$$

which can be used to find Q_{C_3}, and hence the output voltage from (10.85)

$$v_{out} = \frac{77.5 \times 10^{-3}\ \text{pC}}{1\text{pF}} = 78\ \text{mV} \tag{10.87}$$

Thus, we see that this output dc offset value is affected by the size of capacitors used (in particular, C_3) as well as the switch sizes and power-supply voltage. It should be mentioned here that if the dc input offset voltage of the opamp was included in the analysis, it would be multiplied by the dc gain of the circuit similar to that which occurs in an active-RC circuit.

Charge-injection is especially troublesome at higher frequencies. At higher frequencies, the time constant of the switch-on resistance and the capacitor being charged or discharged must be smaller; this necessitates larger switches for a given size capacitor and therefore greater charge-injection. It is possible to derive a very simple formula that gives an approximate upper bound on the frequency of operation of an SC circuit for a specified maximum voltage change due to charge injection. This upper bound takes into account switch channel charge only and ignores charge injection due to overlap capacitance.

Most SC circuits will have two series switches for each capacitor. If one assumes that, for good settling, the sampling clock half-period must be greater than five time constants, then we have

$$\frac{T}{2} > 5R_{on}C \tag{10.88}$$

where T is the sampling period, R_{on} is the on resistance of the n-channel switch, and C is the capacitor. Equation (10.89) may be rewritten

$$f_{clk} < \frac{1}{10R_{on}C} \tag{10.89}$$

where $f_{clk} = 1/T$ is the clock frequency. Recalling (1.108) from Chapter 1, we have

$$R_{on} = \frac{1}{\mu_n C_{ox}\frac{W}{L}V_{eff}} \tag{10.90}$$

Also, using (10.83), the charge change due to the channel charge only caused by turning an n-channel switch off is approximated by

$$|\Delta V| = \frac{Q_{CH}}{2C} = \frac{WLC_{ox}V_{eff}}{2C} \tag{10.91}$$

For a specified $|\Delta V|_{max}$, (10.92) implies that

$$C = \frac{WLC_{ox}V_{eff}}{2|\Delta V|_{max}} \tag{10.92}$$

Substituting (10.91) and (10.93) into (10.90) gives

$$f_{clk} = \frac{\mu_n|\Delta V|_{max}}{5L^2} \tag{10.93}$$

a very simple expression. Thus, the upper frequency limit to charge injection for SC circuits is inversely proportional to L^2 and is approximately independent of the size of capacitors or the power-supply voltages, assuming the switch sizes are chosen optimally; as technology improves, much higher switching frequencies are attainable. Finally, (10.94) ignores overlap capacitance, so it is somewhat optimistic and should be therefore considered an upper bound on the maximum clocking frequency.

EXAMPLE 10.7

Assuming the maximum voltage change due to clock feedthrough is 1 mV, what are the maximum clocking frequencies considering only channel charge injection for technologies having minimum channel lengths of 0.8 μm, 0.5 μm, and 0.3 μm?

Solution

Using (10.94) and $\mu_n = 0.05\ M^2/V \cdot s$ gives f_{clk}, which must be less than 15.6 MHz, 40 MHz, and 111 MHz, respectively, for the three different technologies. Notice the substantial increase in speed for SC circuits as the technology improves.

10.6 SWITCHED-CAPACITOR GAIN CIRCUITS

Perhaps the most common nonfiltering analog function is a gain circuit where the output signal is a scaled version of the input. In this section, we shall see that it is possible to realize accurate gain circuits by making use of switched-capacitor techniques.

Parallel Resistor-Capacitor Circuit

In active-RC circuits, a gain circuit can be realized as parallel combinations of resistors and capacitors in both the feedback and feed-in paths, as shown in Fig. 10.27(*a*). One of the first switched-capacitor gain circuits uses a similar approach, where the two resistors have been replaced by their switched-capacitor equivalents, as shown in Fig. 10.27(*b*) [Foxall, 1980]. Using the signal-flow-graph technique of Section 10.2, straightforward analysis results in the transfer function for this switched-capacitor gain circuit being given by

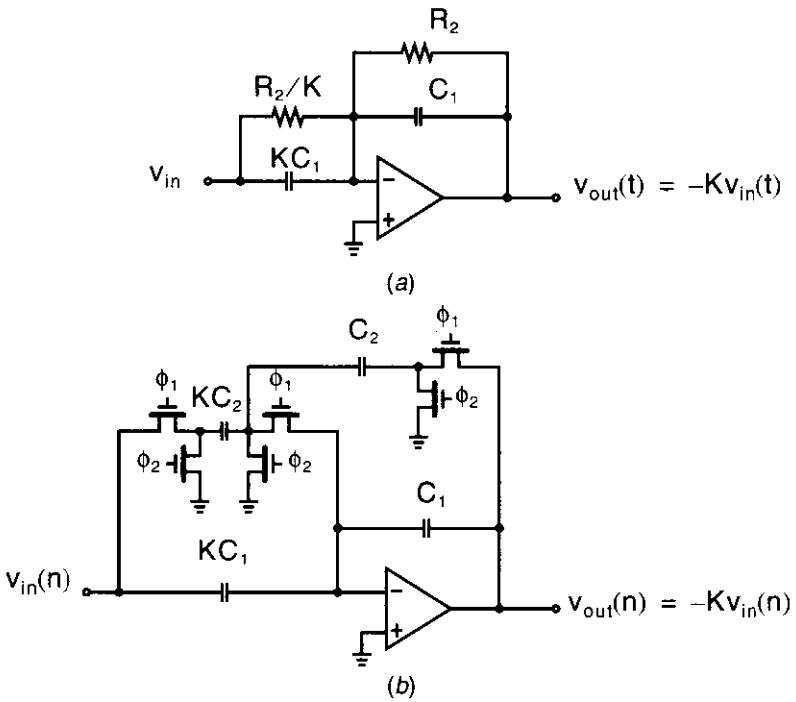


Fig. 10.27 (*a*) An active-RC gain circuit. (*b*) An equivalent switched-capacitor gain circuit.

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -K \tag{10.94}$$

Unfortunately, this design will also amplify the 1/f noise and offset voltage of the shown opamp by K. However, it does have the advantage that its output is a continuous waveform that does not incur any large slew-rate requirement (as occurs in the resettable gain circuit discussed next).

Resettable Gain Circuit

The next configuration continuously resets an integrating capacitor on each clock cycle, as shown in Fig. 10.28 [Gregorian, 1981]. Here, the voltage across the integrating capacitor, C_2, is cleared on each ϕ_2, while on ϕ_1 the input voltage charges C_1 and the charging current flows across C_2 at the same time. In this way, the change in charge across C_2, ΔQ_{C2}, equals the change in charge across C_1, ΔQ_{C1}, and therefore, at the end of ϕ_1, the output voltage is related to the input voltage by $V_{out}/V_{in} = -C_1/C_2$.

In addition, this circuit stores any opamp input-offset voltage across the input and feedback capacitors. When the output is sampled by the succeeding circuit (during ϕ_1), the effects of the input-offset voltage of the opamp are cancelled from the output

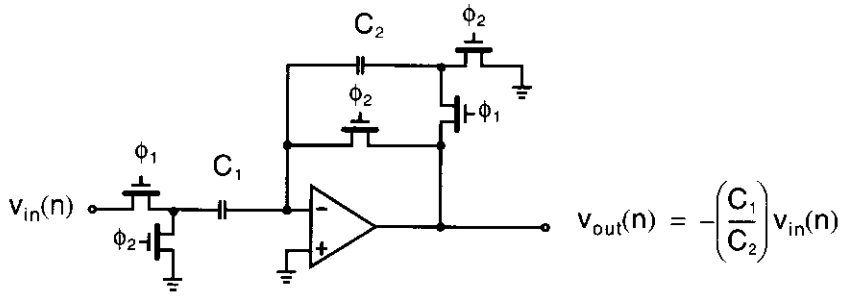


Fig. 10.28 A resettable gain circuit where opamp offset voltage is cancelled.

voltage. The elimination of the opamp's input-offset voltage is important for two reasons. One reason is that if the offset voltage is not cancelled, it will also be amplified when the input signal is amplified and therefore can be troublesome. A second reason (and often more important) is that when the offset voltage is eliminated, 1/f noise is also reduced. As we saw in Chapter 4, 1/f noise is large at low frequencies and can be a dominant noise source in many MOS circuits. However, when a circuit cancels dc offset voltages, the circuit has, in effect, a high-pass response from the opamp's input terminals to the output voltage. Thus, the 1/f noise is also high-pass filtered and hence reduced. It should be noted here that although there is a high-pass response from the opamp's input terminals to the output voltage, the response from the overall circuits does not necessarily have a high-pass response.

To see this offset cancellation, consider the gain circuit during ϕ_2 (i.e., when it is being reset) as shown in Fig. 10.29(*a*). The effect of the input offset voltage is being modelled as a voltage source, V_{off}, which is placed in series with one of the opamp inputs. In this case, it is placed in series with the positive input, which results in the analysis being marginally simpler. During ϕ_2, both the voltages across C_1 and C_2 are equal to the opamp offset voltage, V_{off}. Next, during ϕ_1 the circuit is configured as shown in Fig. 10.29(*b*), and at the end of ϕ_1 the voltage across C_1 is given by

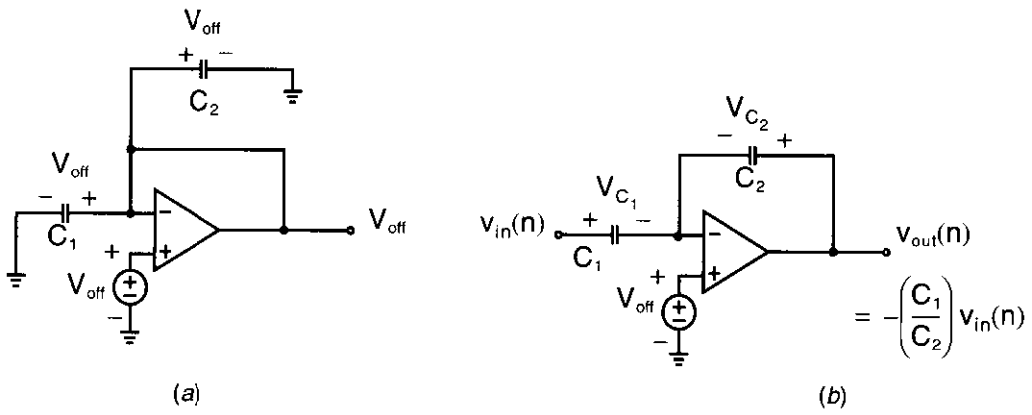


Fig. 10.29 The resettable gain circuit (*a*) during reset (ϕ_2), and (*b*) during valid output (ϕ_1).

$V_{C_1}(n) = v_{in}(n) - V_{off}$, while that for C_2 is given by $V_{C_2}(n) = v_{out}(n) - V_{off}$. Therefore we can write,

$$\Delta Q_{C1} = C_1[V_{C_1}(n) - (-V_{off})] = C_1 v_{in}(n) \tag{10.95}$$

and

$$V_{C_2}(n) = V_{C_2}(n - 1/2) - \frac{\Delta Q_{C2}}{C_2} \tag{10.96}$$

Since the voltage across C_2 one-half period earlier was $-V_{off}$ and $\Delta Q_{C2} = \Delta Q_{C1}$, we have

$$V_{C_2}(n) = -V_{off} - \frac{C_1 v_{in}(n)}{C_2} \tag{10.97}$$

Finally, since one side of C_2 is connected to the virtual ground of the opamp, which is at V_{off}, the output voltage is given by

$$\begin{aligned} v_{out}(n) &= V_{off} + V_{C_2}(n) \\ &= V_{off} + \left(-V_{off} - \frac{C_1 v_{in}(n)}{C_2}\right) \\ &= -\left(\frac{C_1}{C_2}\right) v_{in}(n) \end{aligned} \tag{10.98}$$

Thus, the output voltage is independent of the opamp offset voltage.

Note, however, that the output voltage is only valid during ϕ_1, and it is equal to V_{off} during ϕ_2, as shown in Fig. 10.30. The difficulty in realizing this waveform is that the opamp output must slew between $(-C_1/C_2)v_{in}$ and a voltage near 0 V each time the clock changes. Clearly, such a waveform requires a very high slew-rate opamp for proper operation.

Finally, note that a programmable gain circuit is easily realized by replacing C_1 with a programmable capacitor array[7] (PCA) where the capacitor size is determined by digital signals.

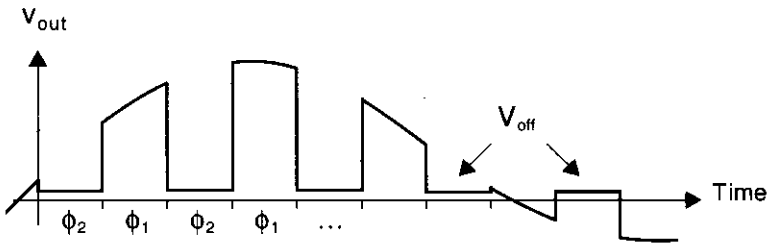


Fig. 10.30 An example output waveform for the resettable gain circuit.

7. A programmable capacitor array is a capacitor whose size can be digitally controlled. It normally consists of a number of binarily-weighted capacitors having one plate common for all capacitors and the other plate of each capacitor connected through digitally-controlled switches to either a second common node or ground.

Capacitive-Reset Gain Circuit

To eliminate the need for the opamp output to slew to approximately 0 V each clock period yet still cancel the opamp's offset voltage, a capacitive-reset gain circuit can be used. The basic idea of the gain circuit is to couple the opamp's output to the inverting input during the reset phase with a capacitor that has been previously charged to the output voltage. Thus, we shall see that one property of this gain circuit is that the opamp's output need only change by the opamp's offset voltage between clock phases. In addition, since the circuit is insensitive to the opamp's input offset voltage, it also reduces the effect of the opamp's 1/f noise. Finally, it can also be shown (see [Martin, 1987]) that for low-frequency inputs (or for inputs that are constant for at least two clock periods), the errors due to finite gain, A, of the opamp are proportional to $1/A^2$ (rather than the usual $1/A$). Such a result often allows the use of single-stage opamps that are very fast opamps.

The capacitive-reset gain circuit is shown in Fig. 10.31. Capacitor C_4 is an optional "deglitching" capacitor [Matsumoto, 1987] used to provide continuous-time feedback during the nonoverlap clock times when all the switches are open. This deglitching technique works well and should be used on almost all switched-capacitor circuits that would otherwise have no feedback connection at some instant of time. This capacitor would normally be small (around 0.5 pF or less).

This gain circuit can be either inverting or noninverting depending on the clock phases of the input stage. While the inverting circuit creates its output as a delay-free version of the input, the output for the noninverting case would be one-half clock cycle behind the input signal.

To see how this capacitive-reset gain circuit operates, consider the inverting circuit during the reset phase of ϕ_2, as shown in Fig. 10.32(*a*). We have assumed capacitor C_3 was charged to the output voltage during the previous ϕ_1 clock phase. Here we see that capacitors C_1 and C_2 are charged to the opamp's input-offset voltage, V_{off}, in the same manner as in the resettable gain circuit of Fig. 10.28. The next clock phase of ϕ_1 is shown in Fig. 10.32(*b*), where we see that the output voltage is

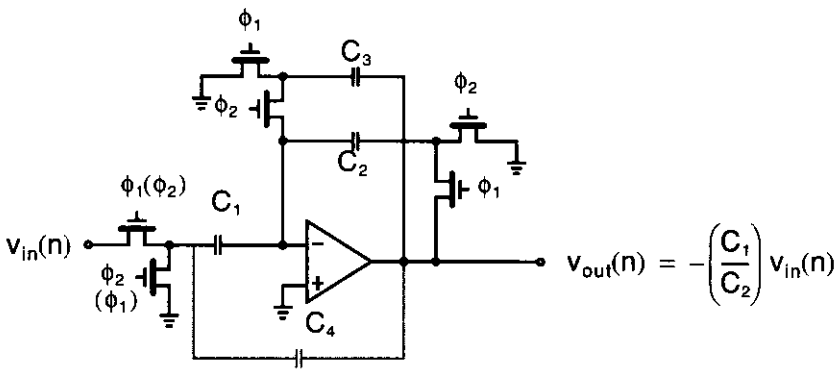


Fig. 10.31 A gain circuit using capacitive reset (C_4 is an optional deglitching capacitor). Depending on the input-stage clock signals, the gain can be either inverting (as shown) or noninverting (input-stage clocks shown in parentheses).

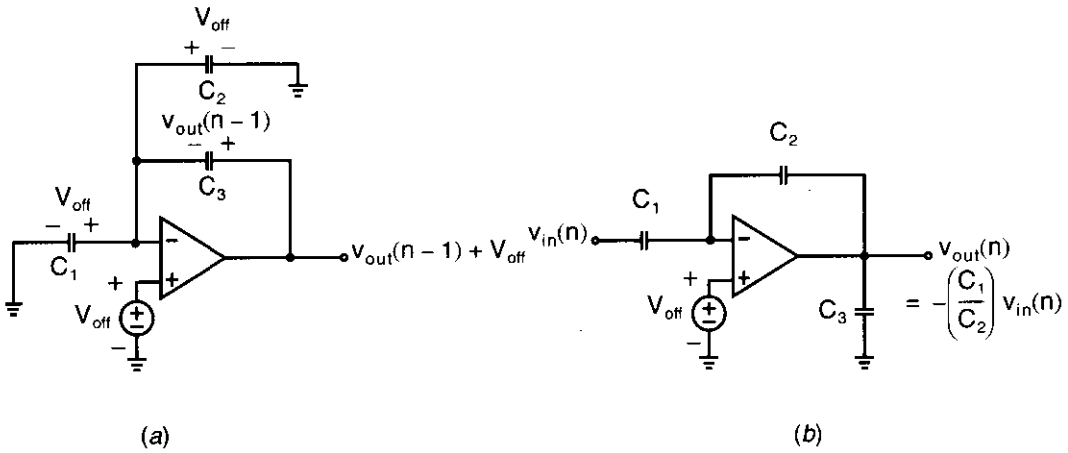


Fig. 10.32 Capacitive-reset gain circuit. (*a*) During reset (ϕ_2) when the output remains near previous output level. (*b*) During valid output (ϕ_1) when no offset error is present.

independent of the offset voltage in the same manner as the resettable gain circuit. In addition, we see that during ϕ_1, capacitor C_3 is charged to the output voltage. Before proceeding, it is of interest to note what happens to the charges on C_1 and C_2 when going from phase ϕ_1 to ϕ_2 (i.e., circuit (*b*) to (*a*) of Fig. 10.32). Since the charges on C_1 and C_2 are equal (recall that the charge on C_2 was obtained during the charging of C_1), when one side of each of C_1 and C_2 are grounded, their charges cancel each other and no charge is dumped onto C_3. Therefore, in the circuit of Fig. 10.32(*a*), the voltage on C_3 remains equal to the previous output voltage as shown. It should be

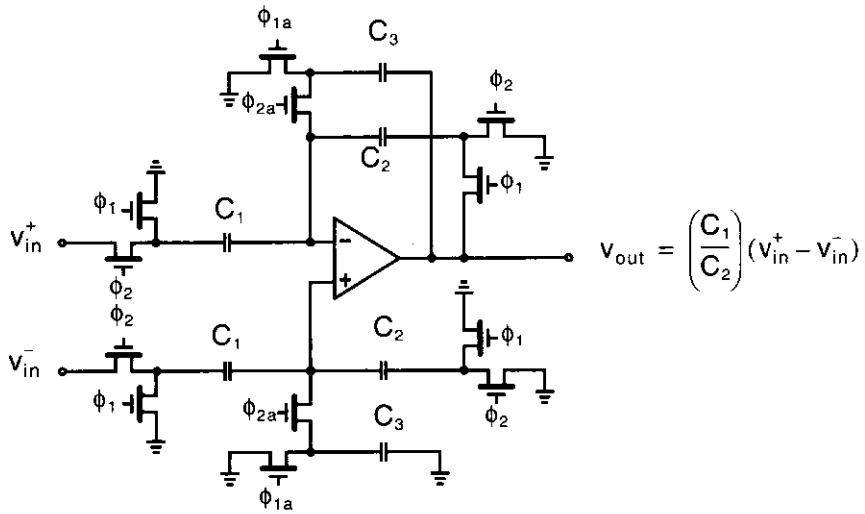


Fig. 10.33 A differential-to-single-ended gain circuit using capacitive reset.

noted here that even if the two charges did not precisely cancel, it would only result in the output voltage moving slightly further away from the previous output voltage during ϕ_2 but would not affect the output voltage during ϕ_1.

Finally, this capacitive-reset gain circuit can also realize a differential-to-single-ended gain stage, as shown in Fig. 10.33. Note that the shown circuit indicates that the switches connected around the virtual grounds are disconnected slightly sooner than other switches to reduce nonlinearities due to charge injection. This circuit has a switched-capacitor circuit connected to the positive input of the opamp that not only accepts differential inputs but also, to a first-order approximation, cancels the clock feedthrough of the switches [Martin, 1982]. The measured common-mode input rejection ratio for this circuit was 50 dB where a 5 μm technology was used together with a clock rate of 5 MHz [Martin, 1987].

10.7 CORRELATED DOUBLE-SAMPLING TECHNIQUES

The preceding SC gain amplifier is an example of using correlated double sampling (CDS) to minimize errors due to finite offset voltages, 1/f noise, and finite opamp gain. This technique is generally applicable to SC circuits of many different types [Temes, 1996]. To date, it has been used to realize highly accurate gain amplifiers, sample and holds, and integrators. The basic methodology in all cases is similar: During a calibration phase, the finite input voltage of the opamp is sampled and stored across capacitors; during the operation phase (when the output is being sampled), this error voltage is subtracted from the signal voltage by appropriate switching of the capacitors. A detailed description of CDS techniques is beyond the scope of this text; rather, a couple of examples will be briefly described and the interested reader can consult the tutorial [Temes, 1996] for more information.

A wide-band amplifier that uses CDS, similar to the SC amplifier of Fig. 10.31, but with superior high-frequency operation, is shown in Fig. 10.34. During ϕ_2, C_1' and C_2' are used to have

$$v_{out} \cong -\frac{C_1'}{C_2'} v_{in} \tag{10.99}$$

but with errors due to finite input-offset voltage, 1/f noise, and gain. At the same time, the finite opamp input voltage caused by these errors is sampled and stored across C_1 and C_2. Next, during ϕ_1, this input error voltage is subtracted from the signal (applied to the opamp input) at that time. Assuming that the input voltage and the opamp input error voltages did not change appreciably from ϕ_2 to ϕ_1, errors due to them will be significantly reduced.

The technique can also be used to realize accurate integrators. For example, the SC integrator shown in Fig. 10.35 [Nagaraj, 1986; Ki, 1991] uses an additional capacitor, C_2', to sample the opamp input error voltages during ϕ_1. Next, during ϕ_2, C_2' is connected in series with the opamp's inverting input and greatly minimizes the effects of these errors (by a factor of the inverse of the opamp's gain over what would otherwise occur at frequencies substantially less than the

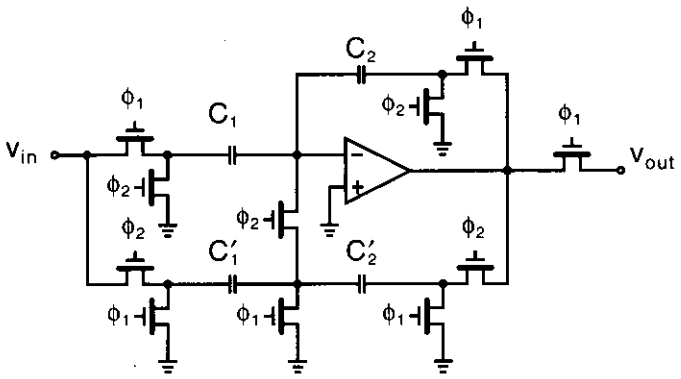


Fig. 10.34 An SC amplifier with CDS to minimize errors due to input- offset voltages, 1/f noise, and finite gain.

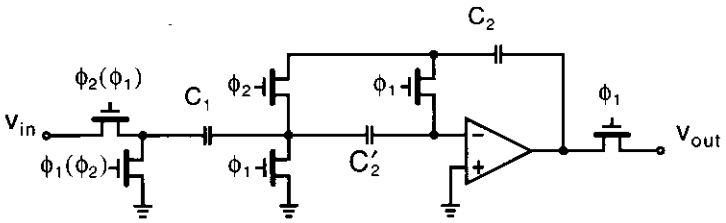


Fig. 10.35 An SC integrator with CDS to minimize errors due to input-offset voltages, 1/f noise, and finite gain.

sampling frequency). Similar architectures, with an open-loop capacitor in series with the opamp input during the phase when the output is sampled, can also be used for gain amplifiers.

When CDS sampling is used, the opamps should be designed to minimize thermal noise rather than 1/f noise. This might mean the use of n-channel input transistors rather than p-channel input transistors, for example.

When this technique is used in high-order SC filters, often only a couple of stages will have low-frequency gain from the opamp input terminals to the filter outputs and will require CDS circuitry. Other integrators can be more simply realized. This technique has proven to be very useful in applications such as oversampling A/D converters, where accurate integrators are required in the first stage [Hurst, 1989; Rebeschini, 1989] to reduce input-offset voltages and especially 1/f noise.

10.8 OTHER SWITCHED-CAPACITOR CIRCUITS

In this section, we present a variety of other switched-capacitor circuits useful for nonlinear applications. Specifically, we look at an amplitude modulator, full-wave rectifier, peak detector, voltage-controlled oscillator, and sinusoidal oscillator.

Amplitude Modulator

Amplitude modulators are used to shift a signal along the frequency axis. For example, to shift an information signal, $m(t)$, by a carrier frequency, ω_{ca}, we multiply $m(t)$ by a sinusoidal signal of frequency, ω_{ca}, or mathematically,

$$y(t) = m(t) \times \cos(\omega_{ca} t) \tag{10.100}$$

Since the Fourier transform of $\cos(\omega_{ca} t)$ is $\pi\delta(\omega - \omega_{ca}) + \pi\delta(\omega + \omega_{ca})$, and multiplication in the time domain is equivalent to convolution in the frequency domain, one can show that the spectrum of $y(t)$ is equal to

$$Y(\omega) = \frac{1}{2} M(\omega + \omega_{ca}) + \frac{1}{2} M(\omega - \omega_{ca}) \tag{10.101}$$

Thus, the output spectrum only has power around $\pm\omega_{ca}$.

However, in many cases it is difficult to realize a sinusoidal signal as well as a linear multiplier. As a result, many modulators make use of a square-wave carrier signal, in which case the output signal is simply

$$y(t) = m(t) \times s_q(t) = \pm m(t) \tag{10.102}$$

where $s_q(t)$ is a square wave operating at the carrier frequency whose amplitude has been normalized to 1. Thus, this approach simply requires a square-wave signal at the carrier frequency determining whether $m(t)$ or $-m(t)$ is passed to the output. The penalty paid here is that rather than $Y(\omega)$ having power located only around $\pm\omega_{ca}$, there will also be significant power around odd multiples of $\pm\omega_{ca}$ since a square-wave signal has power at odd harmonics of the fundamental. These extra images can typically be tolerated through the use of additional filtering stages.

A square-wave modulator can be realized using switched-capacitor techniques, as shown in Fig. 10.36. Here, the modulator is realized by making use of the capacitive-reset gain stage of Fig. 10.31. Note that the polarity of the output signal is determined by changing the clock phases of the input-transistor pair through the use of ϕ_A and ϕ_B, which are controlled by the square-wave carrier clock signal ϕ_{ca}. When ϕ_{ca} is high, $\phi_A = \phi_2$ and $\phi_B = \phi_1$, which results in a noninverting output of $(C_1/C_2)v_{in}$. When ϕ_{ca} goes low, the clock phases of ϕ_A, ϕ_B switch, and the circuit produces an inverting output of $-(C_1/C_2)v_{in}$.

Full-Wave Rectifier

A full-wave rectifier produces as its output the absolute value of the input. In other words, if the input is positive the output equals the input, but if the input is negative the output equals an inverted version of the input.

It is possible to realize a full-wave rectifier by making use of an amplitude modulator where, instead of a square-wave carrier signal being used, the output of a comparator controls the polarity of the output signal, as shown in Fig. 10.37. If the input signal is above ground, ϕ_{ca} goes high and the output is equal to a scaled version of the input. If the input signal is below ground, ϕ_{ca} goes low and the output equals an

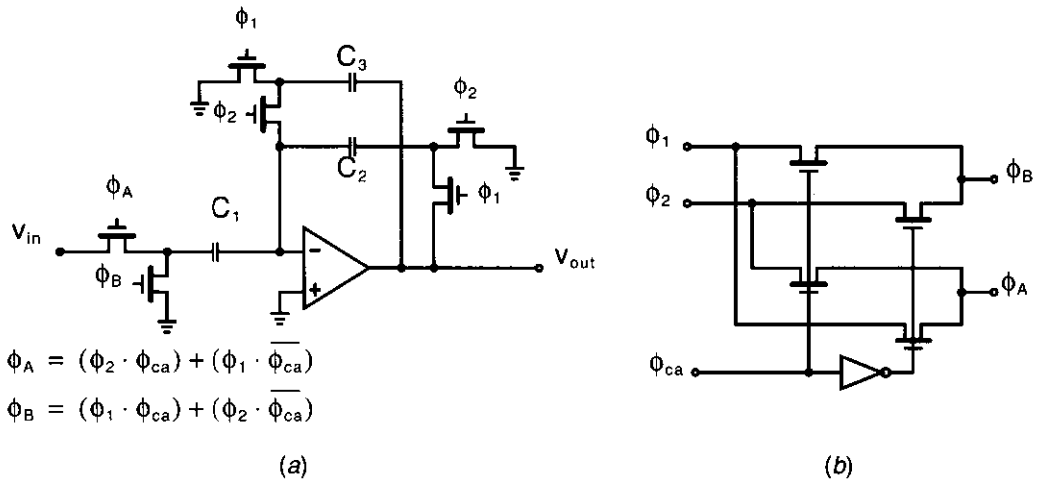


Fig. 10.36 (*a*) A switched-capacitor square-wave modulator where the input clock phases are controlled by the modulating square wave ϕ_M. (*b*) A possible circuit realization for ϕ_A and ϕ_B.

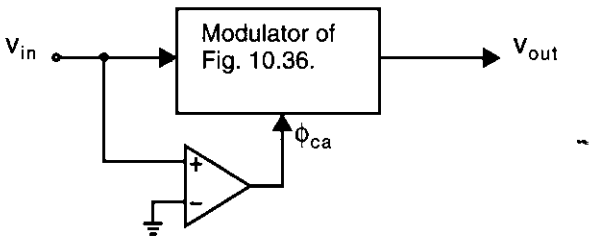


Fig. 10.37 A full-wave detector based on the square-wave modulator circuit of Fig. 10.36.

inverted scaled version of input. For proper operation, the comparator output must change synchronously with the sampling instances. Circuits to achieve this operation are given in [Gregorian, 1986].

Peak Detectors

Peak detectors produce as their output the maximum value of an input signal over some time period. While peak detectors will normally have some decaying circuitry associated with them (or a circuit to reset the peak occasionally), here we shall just look at the peak detector circuit itself. Two methods for realizing peak detectors are shown in Fig. 10.38.

In Fig. 10.38(*a*), a latched comparator is used to determine when $v_{in} > v_{out}$. When such a condition occurs, the comparator output goes high and the switch Q_1 turns on,

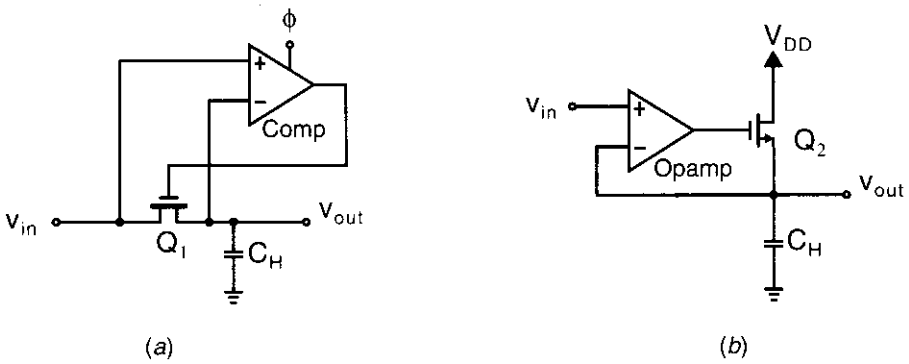


Fig. 10.38 Two-peak detectors: (*a*) latched-comparator approach; (*b*) continuous-time approach.

forcing $v_{out} = v_{in}$. The comparator is latched here to maintain its speed as well as ensuring that the comparator output is either high or low. Note that this circuit requires that the input signal directly drives C_H through Q_1, and hence buffering may be required. However, this circuit can be reasonably fast since latched comparators can be made to operate quickly and there is no opamp settling involved (only the RC time constant of Q_1 and C_H).

The circuit of Fig. 10.38(*b*) requires an opamp (with proper compensation), since it places Q_2 in a feedback connection. When $v_{in} > v_{out}$, the opamp output will start to go high, thus turning on Q_2 and hence turning on the feedback loop. While the feedback loop is on, the high loop gain will force $v_{out} = v_{in}$ with a high accuracy. Note that this circuit has a high input impedance as the input signal is applied to the noninverting terminal of an opamp. However, this opamp-based circuit will typically be slower than the comparator-based circuit of Fig. 10.38(*a*) since one needs to wait for the opamp output to slew and then settle. This slewing time can be minimized by adding circuitry to ensure that the gate of Q_2 never becomes lower than the output voltage when Q_2 is not conducting.

Voltage-Controlled Oscillator

A voltage-controlled oscillator (VCO) is an oscillator whose frequency can be adjusted through the use of a controlling voltage. As we shall see, the VCO described here generates an output square wave that places the oscillator alternatively in one of two states and is referred to as a relaxation oscillator. As we shall see in Chapter 16, a VCO is an integral part of a phase-locked loop (PLL).

The basic principle and typical waveforms of the relaxation oscillator are shown in Fig. 10.39 [Martin, 1981] and operate as follows. Assume that v_{out} has just toggled low to $-V_{ss}$ and node v_x is now at a level quite a bit higher than zero. On ϕ_1, k_2C will be charged up to a voltage of $-V_{SS}$, resulting in a charge

value given by

$$Q_{k_2C} = -k_2CV_{SS} \tag{10.103}$$

Note that the voltage across the unswitched capacitor k_1C remains unchanged at $-V_{SS}$. Next, as ϕ_2 goes high, the charge on k_2C will be transferred to C (while the voltage across unswitched k_1C again remains unchanged) and the output will fall by an amount equal to

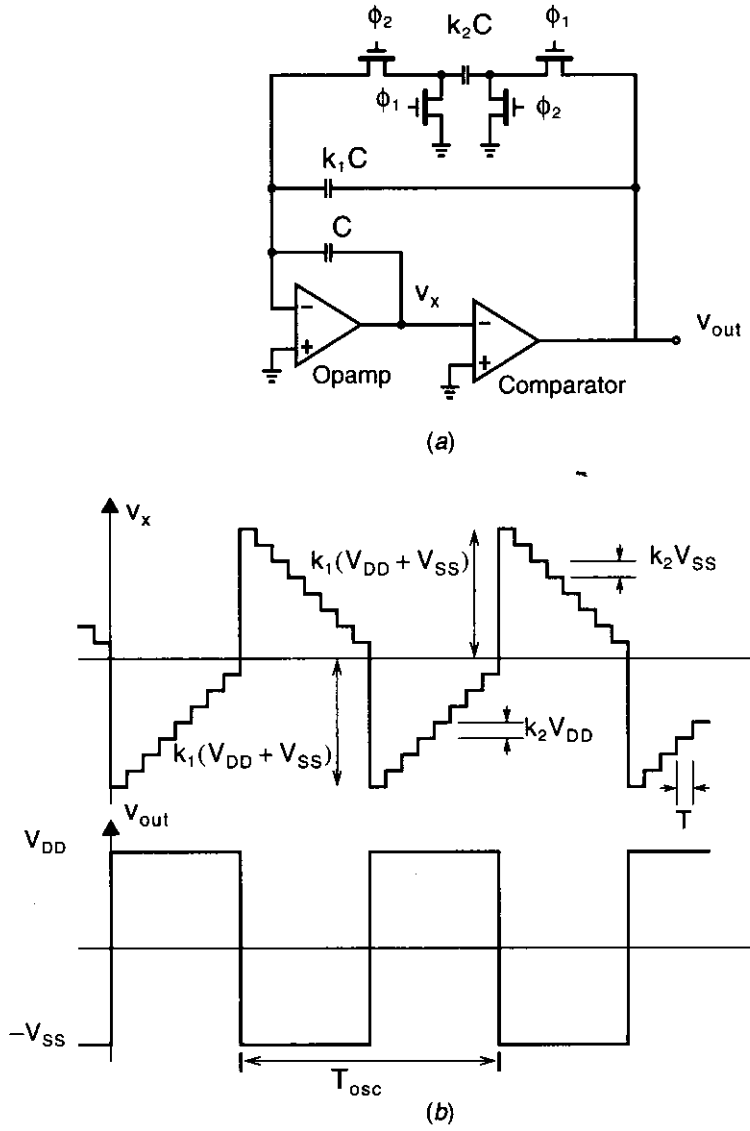


Fig. 10.39 A switched-capacitor relaxation oscillator.

$$\Delta v_x = \frac{\Delta Q_C}{C} = \frac{Q_{k_2C}}{C} = -k_2 V_{SS} \tag{10.104}$$

This operation will continue until v_x reaches zero volts. In effect, k_2C and C have formed a noninverting discrete-time integrator, while capacitor k_1C does not affect the operation of the circuit. Once v_x goes below zero, the comparator output will toggle to $-V_{DD}$, and at this point a large amount of charge will pass through k_1C while the voltage across it changes from $-V_{SS}$ to V_{DD}. This large charge value is equal to

$$\Delta Q_{k_1C} = k_1 C(V_{DD} - (-V_{SS})) \tag{10.105}$$

and since this charge is drawn across C, then $\Delta Q_C = \Delta Q_{k_1C}$ and node v_x drops by an amount equal to

$$\Delta v_x = -\frac{\Delta Q_C}{C} = -k_1(V_{DD} + V_{SS}) \tag{10.106}$$

as shown in Fig. 10.39(*b*). After this time, v_x will step up in increments of k_2V_{DD} (since v_{out} now equals V_{DD}) until $v_x = 0$, at which point a large positive voltage step will occur. Just after this positive step, we will be back at our starting point, and the entire operation will repeat indefinitely.

To derive a formula for the oscillation period T_{osc}, we make the assumption that $k_1 >> k_2$ such that many small steps occur over one-half T_{osc} period. With this assumption, we can now write that the total number of clock cycles, T_{osc}/T, equals the number of steps during negative sloping v_x plus the number of steps during positive sloping v_x. Mathematically, we have

$$\frac{T_{osc}}{T} = \frac{k_1(V_{DD} + V_{SS})}{k_2 V_{SS}} + \frac{k_1(V_{DD} + V_{SS})}{k_2 V_{DD}} \tag{10.107}$$

Assuming $V_{DD} = V_{SS}$, we have a 50 percent duty cycle with

$$T_{osc} = 4\left(\frac{k_1}{k_2}\right)T \tag{10.108}$$

or equivalently,

$$f_{osc} = \frac{1}{4}\left(\frac{k_2}{k_1}\right)f \tag{10.109}$$

This fixed-frequency oscillator can be made voltage controlled by adding an extra feed-in capacitor to the oscillator, $k_{in}C$, as shown in Fig. 10.40. Here, when V_{in} is positive, extra charge packets are added into the integrator with the same sign as those for k_2C, and the circuit reaches $v_x = 0$ sooner. If V_{in} is negative, then extra charge packets are added into the integrator with the opposite sign as those for k_2C, and the circuit reaches $v_x = 0$ later. Assuming $k_1 >> k_2$, k_{in} and $V_{DD} = V_{SS}$, it is left as an exercise to the reader (Problem 10.12) to show that the frequency of oscillation for the

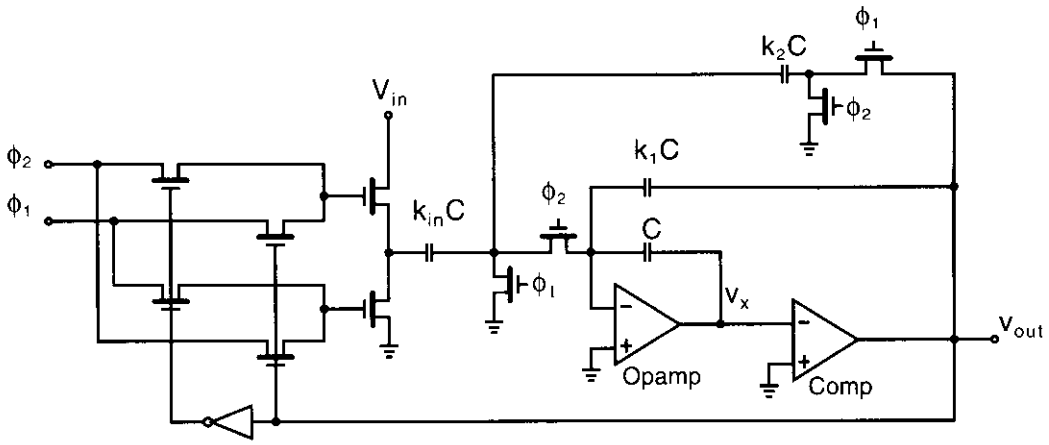


Fig. 10.40 A voltage-controlled oscillator (VCO) based on the relaxation oscillator of Fig. 10.39.

voltage-controlled oscillator of Fig. 10.40 is given by

$$f_{osc} = \frac{1}{4}\left(\frac{k_2}{k_1} + \frac{k_{in}V_{in}}{k_1 V_{DD}}\right) f \tag{10.110}$$

Sinusoidal Oscillator

In many applications, it is useful to realize an oscillator which produces a nearly sinusoidal output. For example, when a button is pressed on a touch-tone telephone, the signal sent down the telephone line is simply the sum of two sinusoidal signals at certain frequencies (the signal is known as a dual-tone multi-frequency (DTMF) signal). Thus, switched-capacitor sinusoidal oscillators could be used to generate the necessary touch-tone signals.

One method of generating a sinusoidal oscillator is shown in Fig. 10.41. Here, a high-Q bandpass filter with center frequency f_0 is used together with a hard limiter. Assuming some start-up circuit is used to force oscillations to exist, we see that a sinusoidal wave at v_{out} results in a square wave at v_1 which has a large component at f_0. The signal v_1 is filtered by the bandpass filter and thus maintains the sinusoidal signal, v_{out}. The oscillation frequency is set by the center frequency of the bandpass filter, while the sinusoidal amplitude is set by the center frequency gain of the filter and the peak values of the square-wave signal.

A switched-capacitor implementation of this sinusoidal oscillator is shown in Fig. 10.42 [Fleischer, 1985], where the high-Q bandpass filter has been realized using the circuit of Fig. 10.25. The comparator generates signals X and $\bar{X}$ with the result that the switched-input associated with V_{ref} is either positive or negative. The start-up circuit is used to sense when an ac signal is present at v_{out}. When no ac signal is detected, v_{st} is low and the extra capacitors C_5 and C_6 form a positive feedback

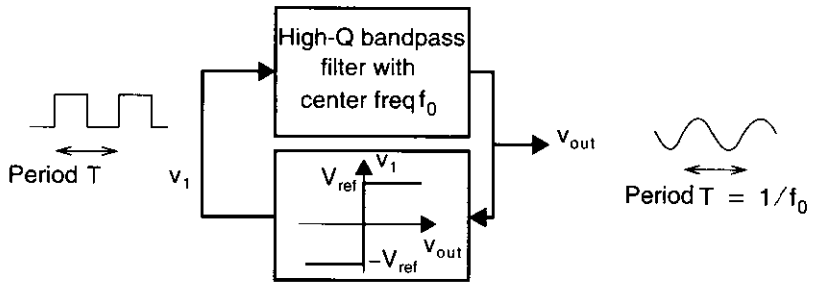


Fig. 10.41 A sinusoidal oscillator that makes use of a bandpass filter.

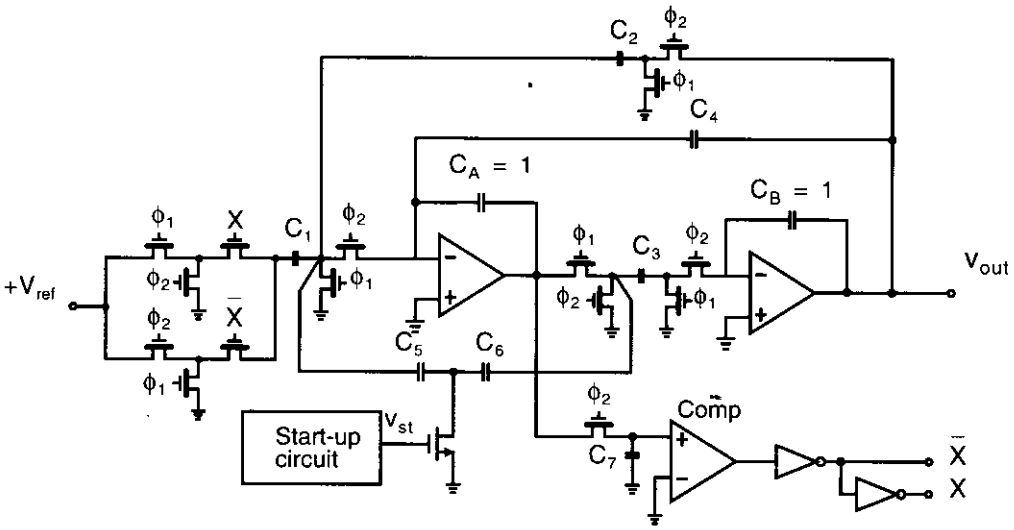


Fig. 10.42 A switched-capacitor implementation of a sinusoidal oscillator.

loop which causes oscillations to build up. Once an ac signal is detected, v_{st} goes high and the positive feedback loop is broken, thereby allowing oscillations to continue, as discussed previously.

For examples of other nonfiltering uses of switched-capacitor circuits, the interested reader is referred to [Gregorian, 1986].

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10.10 PROBLEMS

10.1 Assuming logic signals have infinitely fast fall and rise times but are delayed by 1 ns through a logic gate, draw the output waveforms of the two phase clock generators shown in Fig. 10.3(*b*). Assume the delay blocks add delays of 10 ns each and a clock frequency of 10 MHz is applied to the input.

10.2 Ignoring the effect of parasitic capacitances, find the discrete-time transfer function of the switched-capacitor circuit shown in Fig. P10.2.

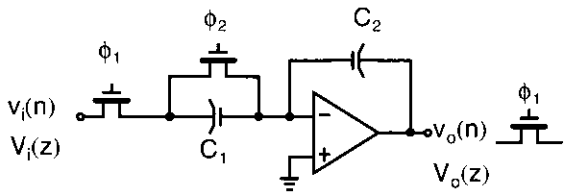


Fig. P10.2

10.3 Repeat Problem 10.2 but include the effect of parasitic capacitances.

10.4 Show that when an opamp has a finite gain of A, the transfer function for the discrete-time integrator of Fig. 10.5 is given by

$$\frac{V_o(z)}{V_i(z)} = -\left(\frac{C_1}{C_2}\right)\left(\frac{1}{z\left(1+\frac{C_1}{C_2 A}\right)-1}\right)$$

Also show that this transfer function has a dc gain of $-A$ and a pole that is located slightly to the left of 1 by an amount approximately equal to $(C_1/C_2)(1/A)$.

10.5 Repeat Example 10.3 but assume the discrete-time zero is at $z = 0$ and the pole remains at $z = 0.53327$. Note that with this change, C_1 is no longer required at the sacrifice of a nonzero gain being obtained at 50 kHz. What is the new gain at 50 kHz?

10.6 Find the capacitances needed for the first-order filter shown in Fig. 10.15(*a*) to realize a discrete-time transfer function having a dc gain of one, a zero at 0, and a 3-dB frequency of 1 kHz when a clock frequency of 50 kHz is used. Assume that $C_A = 50$ pF. What is the gain (in dB) at 25 kHz?

10.7 Find the transfer function of the circuit shown in Fig. 10.16 when $C_1 = 0$ pF, $C_2 = 2$ pF, $C_3 = 2$ pF; and $C_A = 20$ pF. What is the magnitude and phase of the gain at dc, $f_s/4$ and $f_s/2$?

10.8 Find the discrete-time transfer function of the switched capacitor circuit shown in Fig. P10.8.

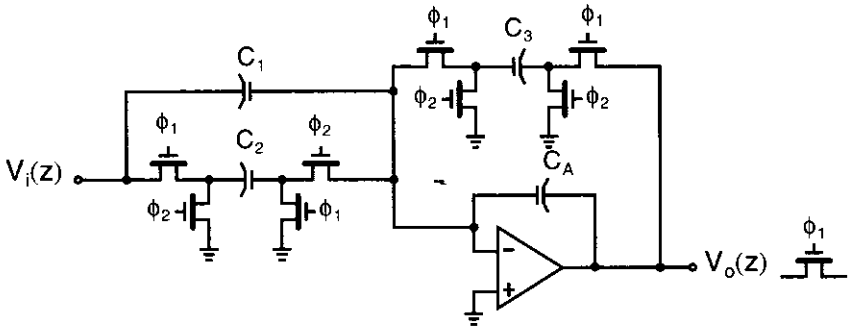


Fig. P10.8

10.9 Show that when $K_6 = 0$ in the biquad circuit of Fig. 10.21, if the poles are complex, they lie precisely on the unit circle (i.e., the circuit is a resonator).

10.10 Using the bilinear transform, design a bandpass filter with a $Q = 20$ (in the continuous-time domain) and a peak gain of one near $f_s/100$. Find the largest to smallest capacitor ratio if this transfer function is realized using the high-Q biquad circuit, and compare it to that which would be obtained if the low-Q circuit were used instead. Let $C_1 = C_2 = 1$ in both cases.

10.11 Sketch a typical output waveform for the capacitive-reset gain circuit of Fig. 10.31 if the opamp has an input offset of 100 mV and a gain of 10 is desired.

10.12 Verify that Eq. (10.104) gives the frequency of oscillation for the VCO of Fig. 10.40.

CHAPTER

11 Data Converter Fundamentals

In this chapter, fundamental aspects of analog-to-digital (A/D) and digital-to-analog (D/A) converters are presented without regard for their internal architecture or circuit design. In effect, converters are treated in this chapter as black boxes such that only their input-output relationships are discussed. Internal architectures and circuits techniques for realizing data converters are discussed in following chapters.

Before proceeding, it is useful to make the distinction between two main types of data converters.

Nyquist-Rate Converters We loosely define *Nyquist-rate data converters* as those converters that generate a series of output values in which each value has a one-to-one correspondence with a single input value. For example, a Nyquist-rate D/A converter would generate a series of analog output levels, where each level is a result of a single B-bit input word. However, it should be noted that Nyquist-rate converters are seldom used at the Nyquist rate due to the difficulty in realizing practical anti-aliasing and reconstruction filters. In most cases, Nyquist rate converters operate at 1.5 to 10 times the Nyquist rate (i.e., 3 to 20 times the input signal's bandwidth).

Oversampling Converters *Oversampling converters* are those converters that operate much faster than the input signal's Nyquist rate (typically 20 to 512 times faster) and increase the output's signal-to-noise ratio (SNR) by filtering out quantization noise that is not in the signal's bandwidth. In A/D converters, this filtering is performed digitally, whereas in D/A converters, analog filtering is used. Most often, oversampling converters use *noise shaping* to place much of the quantization noise outside the input signal's bandwidth (see Chapter 14).

This distinction is made here since much of the descriptions that follow refer more closely to Nyquist-rate converters than to oversampling converters.

11.1 IDEAL D/A CONVERTER

Consider the block diagram of an N-bit D/A converter shown in Fig. 11.1. Here, B_{in} is defined to be an N-bit digital signal (or word) such that

$$B_{in} = b_1 2^{-1} + b_2 2^{-2} + \cdots + b_N 2^{-N} \tag{11.1}$$

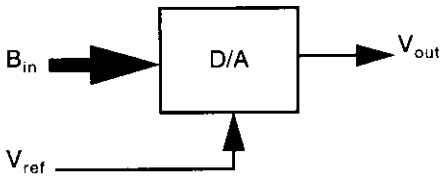


Fig. 11.1 A block diagram representing a D/A converter.

where b_i equals 1 or 0 (i.e., b_i is a binary digit). We also define b_1 as the most significant bit (MSB) and b_N as the least significant bit (LSB). Furthermore, we have assumed here that B_{in} represents a positive value, resulting in a unipolar D/A converter. A *unipolar D/A converter* produces an output signal of only one polarity. In contrast, *signed converters* produce output signals of either positive or negative polarity, depending on a sign bit (usually b_1). Extending the following concepts to the signed case is straightforward but requires knowledge of the type of digital representation used (i.e., sign magnitude, offset binary, or 2's complement). Signed codes are discussed in Section 11.4.

The analog output signal, V_{out}, is related to the digital signal, B_{in}, through an analog reference signal, V_{ref}. For simplicity, we assume that both V_{out} and V_{ref} are voltage signals, although, in general, they may be other physical quantities, such as current or charge. The relationship between these three signals for a unipolar D/A converter is given by

$$V_{out} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \cdots + b_N 2^{-N}) = V_{ref} B_{in} \tag{11.2}$$

It is useful to define V_{LSB} to be the voltage change when one LSB changes, or, mathematically,

$$V_{LSB} \equiv \frac{V_{ref}}{2^N} \tag{11.3}$$

Also useful (particularly in measuring errors) is the definition of a new "unit," namely, LSB units, which are in fact unitless.

$$1 \text{ LSB} = \frac{1}{2^N} \tag{11.4}$$

The transfer curve for an ideal 2-bit D/A converter is shown in Fig. 11.2. Note here that, although only a finite number of analog values occur at the output, for an ideal D/A converter, the output signals are well-defined values. Also note that the maximum value of V_{out} is not V_{ref} but rather $V_{ref}(1 - 2^{-N})$, or equivalently, $V_{ref} - V_{LSB}$. Finally, as we can see from (11.2), a multiplying D/A converter is realized by simply allowing the reference signal, V_{ref}, to be a varying input signal along with the digital input, B_{in}. Such an arrangement results in V_{out} being proportional to the multiplication of the input signals, B_{in} and V_{ref}.

EXAMPLE 11.1

An 8-bit D/A converter has $V_{ref} = 5$ V. What is the output voltage when $B_{in} = 10110100$? Also, find V_{LSB}.

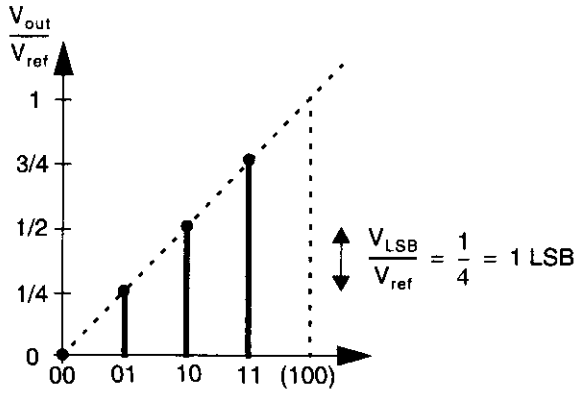


Fig. 11.2 Input-output transfer curve for an ideal 2-bit D/A converter.

Solution

We can find the decimal equivalent of B_{in} using (11.1)

$$B_{in} = 2^{-1} + 2^{-3} + 2^{-4} + 2^{-6} = 0.703125 \tag{11.5}$$

Then, using (11.2), we find

$$V_{out} = V_{ref}B_{in} = 3.516 \text{ V} \tag{11.6}$$

and

$$V_{LSB} = 5/256 = 19.5 \text{ mV} \tag{11.7}$$

11.2 IDEAL A/D CONVERTER

The block diagram representation for an A/D converter is shown in Fig. 11.3, where B_{out} is the digital output word while V_{in} and V_{ref} are the analog input and reference signals, respectively. Also, we define V_{LSB} to be the signal change corresponding to a single LSB change as in the D/A case.

For an A/D converter, the following equation relates these signals,

$$V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \cdots + b_N 2^{-N}) = V_{in} \pm V_x$$

where

$$-\frac{1}{2}V_{LSB} \le V_x < \frac{1}{2}V_{LSB} \tag{11.8}$$

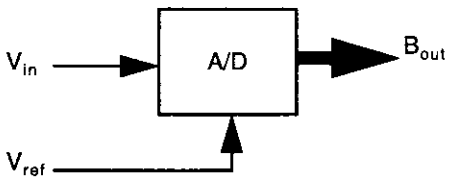


Fig. 11.3 A block diagram representing an A/D converter.

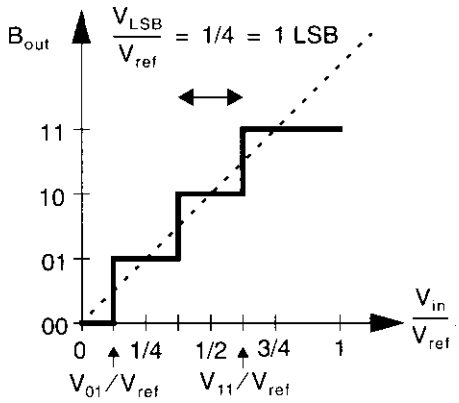


Fig. 11.4 Input-output transfer curve for a 2-bit A/D converter.

Note that there is now a range of valid input values that produce the same digital output word. This signal ambiguity produces what is known as *quantization error*. Also, note that no quantization error occurs in the case of a D/A converter since the output signals are well defined.[1]

As in the D/A case, a transfer curve for an A/D converter can be sketched as shown in Fig. 11.4 for a 2-bit converter. Note that the transitions along the V_{in} axis are offset by $1/2\ V_{LSB}$, so that the midpoints of the staircase curve fall precisely on the equivalent D/A transfer curve. Here, we define the transition voltages at V_{ij}, where the subscript ij indicates the upper B_{out} value of the transition. For example, V_{01} is shown in Fig. 11.4 as the voltage (normalized with respect to V_{ref}) for the transition from 00 to 01.

Finally, it should be noted that the relation shown in (11.8) holds only if the input signal remains within 1 LSB of the two last transition voltages. Specifically, for the 2-bit transfer curve shown in Fig. 11.4, V_{in} should remain less than $7/8\ V_{ref}$ and greater than $-1/8\ V_{ref}$. Otherwise, the quantizer is said to be *overloaded* since the magnitude of the quantization error would be larger than $V_{LSB}/2$.

11.3 QUANTIZATION NOISE

As mentioned in Section 11.2, quantization errors occur even in ideal A/D converters. In this section, we model these errors as being equivalent to an additive noise source and then find the power of this noise source. Consider the setup shown in Fig. 11.5, where both N-bit converters are ideal.

Since we have

$$V_Q = V_I - V_{in} \tag{11.9}$$

1. Of course, quantization errors will occur if a 6-bit D/A converter is used to convert a 10-bit digital signal, but in this case, the quantization error occurs in the conversion from a 10-bit digital signal to a 6-bit digital signal.

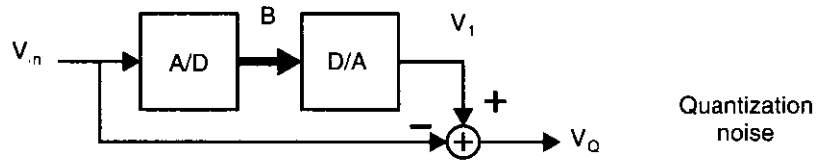


Fig. 11.5 A circuit to investigate quantization noise behavior.

we can rearrange this equation as

$$V_1 = V_{in} + V_Q \tag{11.10}$$

Although this rearrangement is trivial, it has important implications because (11.10) shows that the quantized signal, V_1, can be modelled as the input signal, V_{in}, plus some additive quantization noise signal, V_Q. Note that (11.10) is exact because no approximations have been made here. The quantization noise modelling becomes approximate once some assumptions are made about the statistical properties of V_Q.

Deterministic Approach

To gain an understanding of some of the properties of the quantization noise signal, V_Q, we will investigate its behavior when the input is a particular function. Specifically, let us assume the input signal, V_{in}, in Fig. 11.5 is a ramp. Such an input signal results in the output from the D/A, V_1, appearing as a staircase, as shown in Fig. 11.6, assuming no overloading occurs. Taking the difference between these two signals gives us the noise signal, V_Q, which is a result of quantization error. Note that the quantization signal, V_Q, is limited to $\pm V_{LSB}/2$ and will be so limited for all input signals (not just ramps). Clearly, the average of V_Q is zero. However, the rms value of the noise signal, $V_{Q(rms)}$, is given by

$$\begin{aligned} V_{Q(rms)} &= \left[\frac{1}{T}\int_{-T/2}^{T/2} V_Q^2\, dt\right]^{1/2} = \left[\frac{1}{T}\int_{-T/2}^{T/2} V_{LSB}^2\left(\frac{-t}{T}\right)^2 dt\right]^{1/2} \\ &= \left[\frac{V_{LSB}^2}{T^3}\left(\frac{t^3}{3}\Big|_{-T/2}^{T/2}\right)\right]^{1/2} \end{aligned} \tag{11.11}$$

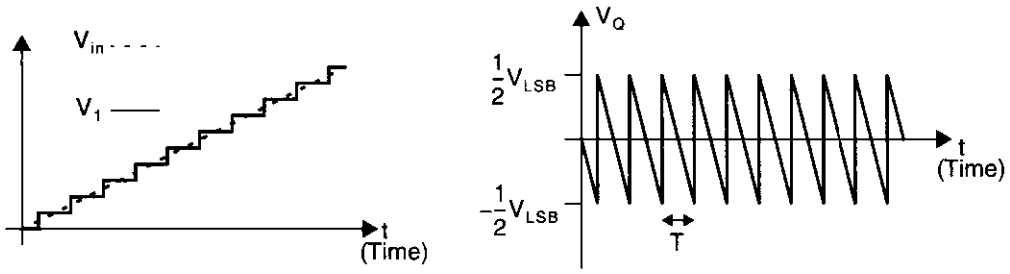


Fig. 11.6 Applying a ramp signal to the circuit in Fig. 11.5.

$$V_{Q(rms)} = \frac{V_{LSB}}{\sqrt{12}} \tag{11.12}$$

Thus, we see that the rms power of the quantization noise source is proportional to the size of V_{LSB}, which is determined by the number of bits, N, in the converter.

Stochastic Approach

The preceding deterministic approach was presented as a simple example to see some properties of the quantization noise signal. However, to deal with the more general input case, a stochastic approach is typically used. In a stochastic approach, we assume that the input signal is varying rapidly such that the quantization error signal, V_Q, is a random variable uniformly distributed between $\pm V_{LSB}/2$. The probability density function for such an error signal, $f_Q(x)$, will be a constant value, as shown in Fig. 11.7.

The average value of the quantization error, $V_{Q(avg)}$, is found to be zero as follows:

$$V_{Q(avg)} = \int_{-\infty}^{\infty} x f_Q(x)\,dx = \frac{1}{V_{LSB}}\left(\int_{-V_{LSB}/2}^{V_{LSB}/2} x\,dx\right) = 0 \tag{11.13}$$

In a similar fashion, the rms value of the quantization error is given by

$$V_{Q(rms)} = \left[\int_{-\infty}^{\infty} x^2 f_e(x)\,dx\right]^{1/2} = \left[\frac{1}{V_{LSB}}\left(\int_{-V_{LSB}/2}^{V_{LSB}/2} x^2\,dx\right)\right]^{1/2} = \frac{V_{LSB}}{\sqrt{12}} \tag{11.14}$$

which is the same result as (11.12), which is found using the deterministic ramp input signal. The fact that these two results are identical should come as no surprise since randomly chosen samples from the sawtooth waveform in the deterministic case would also have a uniformly distributed probability density function. In general, the rms quantization noise power equals $V_{LSB}/\sqrt{12}$ when the quantization noise signal is uniformly distributed over the interval $\pm V_{LSB}/2$.

Recalling that the size of V_{LSB} is halved for each additional bit and assuming that V_{ref} remains constant, we see from (11.14) that the noise power decreases by 6 dB for each additional bit in the A/D converter. Thus, given an input signal waveform, a

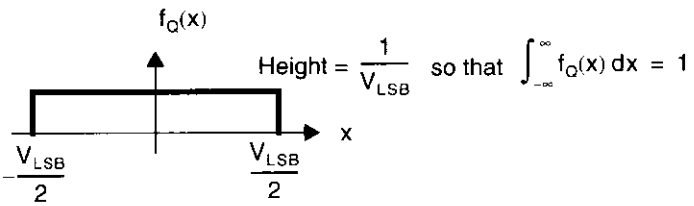


Fig. 11.7 Assumed probability density function for the quantization error, V_Q.

formula can be derived giving the best possible signal-to-noise ratio (SNR) for a given number of bits in an ideal A/D converter.

For example, assuming V_{in} is a sawtooth of height V_{ref} (or equivalently, a random signal uniformly distributed between 0 and V_{ref}) and considering only the ac power of the signal, the SNR is given by

$$\begin{aligned} \text{SNR} &= 20\log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) = 20\log\left(\frac{V_{ref}/\sqrt{12}}{V_{LSB}/\sqrt{12}}\right) \\ &= 20\log(2^N) = 6.02N \text{ dB} \end{aligned} \tag{11.15}$$

For example, a 10-bit A/D converter has a best possible SNR of about 60 dB.

Alternatively, a more common SNR formula is to assume V_{in} is a sinusoidal waveform between 0 and V_{ref}. Thus, the ac power of the sinusoidal wave is $V_{ref}/(2\sqrt{2})$, which results in

$$\begin{aligned} \text{SNR} &= 20\log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) \\ &= 20\log\left(\frac{V_{ref}/(2\sqrt{2})}{V_{LSB}/(\sqrt{12})}\right) \\ &= 20\log\left(\sqrt{\frac{3}{2}}2^N\right) \\ \text{SNR} &= 6.02N + 1.76 \text{ dB} \end{aligned} \tag{11.16}$$

In other words, a sinusoidal signal has 1.76 dB more ac power than a random signal uniformly distributed between the same peak levels.

Note that (11.16) gives the best possible SNR for an N-bit A/D converter. However, the idealized SNR decreases from this best possible value for reduced input signal levels. For example, Fig. 11.8 shows a plot of the idealized SNR for a 10-bit A/D converter versus the sinusoidal input signal amplitude. However, it should be noted that these SNR values could be improved through the use of oversampling techniques if the input signal's bandwidth is lower than the Nyquist rate. Oversampling will be discussed in detail in Chapter 14, where the design of oversampling converters is presented.

EXAMPLE 11.2

A 100-mV_{pp} sinusoidal signal is applied to an ideal 12-bit A/D converter for which $V_{ref} = 5$ V. Find the SNR of the digitized output signal.

Solution

First, we use (11.16) to find the maximum SNR if a full-scale sinusoidal waveform of ±2.5 V were applied to the input.

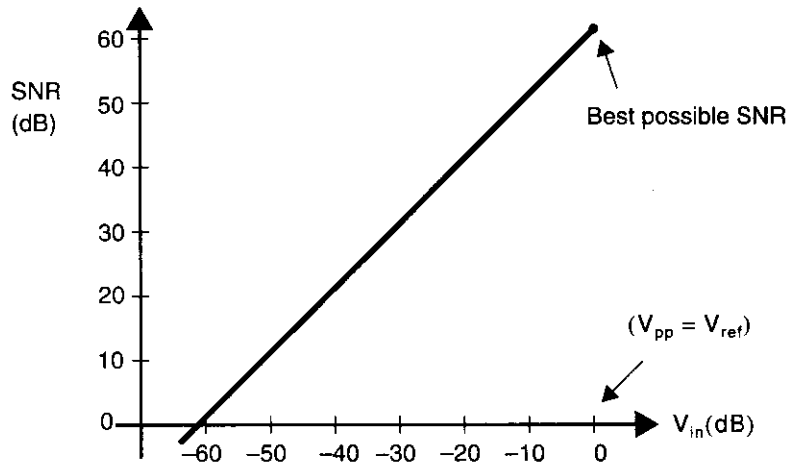


Fig. 11.8 Idealized SNR versus sinusoidal input signal amplitude for a 10-bit A/D converter. The 0-dB input signal amplitude corresponds to a peak-to-peak voltage equaling V_{ref}.

$$SNR_{max} = 6.02 \times 12 + 1.76 = 74 \text{ dB} \tag{11.17}$$

However, since the input is only a ±100-mV sinusoidal waveform that is 28 dB below full scale, the SNR of the digitized output is

$$SNR = 74 - 28 = 46 \text{ dB} \tag{11.18}$$

11.4 SIGNED CODES

In many applications, it is necessary to create a converter that operates with both positive and negative analog signals, resulting in the need for both positive and negative digital representations. Typically, the analog signal is bounded by $\pm 0.5V_{ref}$, such that its full-scale range is the same magnitude as in the unipolar case. Some common signed digital representations are sign magnitude, 1's complement, offset binary, and 2's complement, as shown in Table 11.1 for the 4-bit case. Note from Table 11.1 that all positive number representations are the same except for the offset-binary case, where the MSB is complemented.

Sign Magnitude

For negative numbers in the sign-magnitude case, all the bits are the same as for the positive number representation, except that the MSB is complemented. For example, the sign-magnitude representation for 5 is 0101, whereas for –5 it is 1101. However, note that this approach results in two representations for the number 0, and thus only $2^N - 1$ numbers are represented.

Table 11.1 Some 4-bit signed digital representations

Number	Normalized number	Sign magnitude	1's complement	Offset binary	2's complement
+7	+7/8	0111	0111	1111	0111
+6	+6/8	0110	0110	1110	0110
+5	+5/8	0101	0101	1101	0101
+4	+4/8	0100	0100	1100	0100
+3	+3/8	0011	0011	1011	0011
+2	+2/8	0010	0010	1010	0010
+1	+1/8	0001	0001	1001	0001
+0	+0	0000	0000	1000	0000
(–0)	(–0)	(1000)	(1111)		
–1	–1/8	1001	1110	0111	1111
–2	–2/8	1010	1101	0110	1110
–3	–3/8	1011	1100	0101	1101
–4	–4/8	1100	1011	0100	1100
–5	–5/8	1101	1010	0011	1011
–6	–6/8	1110	1001	0010	1010
–7	–7/8	1111	1000	0001	1001
–8	–8/8			0000	1000

1's Complement

In 1's-complement representation, negative numbers are represented as the complement of all the bits for the equivalent positive number. For example, here, 5 is once again 0101, whereas –5 is now 1010. It should be noted that the 1's-complement case also has two representations for 0, and thus only $2^N - 1$ numbers are represented.

Offset Binary

The offset-binary representation is obtained by assigning 0000 to the most negative number and then counting up, as in the unipolar case. In other words, this system can be thought of as simply a unipolar representation counting from 0 to 2^N, but where the decimal numbers represented are offset by 2^{N-1}, or equivalently, the decimal counts are from -2^{N-1} to 2^{N-1}. For example, the offset-binary code for the number 5 in the 4-bit case is the same as the unipolar code for the number 13, which is 1101, since $13 = 5 + 2^{4-1}$. The offset-binary code for –5 is the same as the unipolar code for 3, which is 0011. Note that the offset-binary code does not suffer from redundancy, and all sixteen numbers are uniquely represented. Also, this code has the advantage that it is closely related to the unipolar case through a simple offset.

Finally, the unipolar relationship for a D/A converter given in (11.2) is easily modified to the signed case, with offset-binary representation as

$$V_{out} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \cdots + b_N 2^{-N}) - 0.5V_{ref} \tag{11.19}$$

Note here that the output signal is now bounded by $\pm 0.5V_{ref}$.

2's Complement

Finally, the 2's-complement representation is obtained from the offset-binary number by simply complementing the MSB. For the 4-bit example, 5 becomes 0101 in 2's complement (the same as in sign magnitude and in 1's complement), whereas –5 is now 1011. It should be mentioned that the 2's-complement code for negative numbers can also be obtained by adding 1 LSB to the equivalent 1's-complement code.

The main advantage of 2's-complement coding is that addition of both positive and negative numbers is performed using straightforward addition, and no extra hardware is required. Also, the subtraction of two numbers, A – B, can be easily performed by complementing all the bits for B (i.e., forming the 1's-complement equivalent) and then adding this result to A at the same time as adding a single LSB in order to create the 2's-complement equivalent of –B. Adding a single LSB is easily accomplished in hardware by setting the *carry-in bit* high in the overall adder. Thus, subtraction requires only a small amount of extra hardware. Finally, if many numbers are being added using 2's-complement codes, no overflow hardware is required as long as the final result is within the digital code range (even if intermediate results go well out of range). For these reasons, 2's-complement codes are the most popular representation for signed numbers when arithmetic operations are to be performed.

EXAMPLE 11.3

Show that, when adding 2/8, 7/8, and –3/8 together as 2's-complement numbers, the final result is correct although an intermediate result is incorrect.

Solution

The addition of 2/8 and 7/8 is given by

$$0010 + 0111 = 1001 \tag{11.20}$$

which corresponds to –7/8 (note that this temporary result is two steps past 7/8 when thinking of a 2's-complement code as being circular). Although this intermediate result is incorrect since overflow occurred, we simply carry on and add –3/8 to find the final answer.

$$1001 + 1101 = 0110 \tag{11.21}$$

Thus, the final result of 6/8 is correct, although a temporary overflow occurred, as we just saw.

11.5 PERFORMANCE LIMITATIONS

In this section, some commonly used terms describing the performance of data converters are defined. Before proceeding, definitions are required for determining the transfer responses of both D/A and A/D converters. The transfer response of a D/A

converter is defined to be the analog levels that occur for each of the digital input words. Similarly, the transfer response of an A/D converter can be defined as the midpoints of the quantization intervals for each of the digital output words. However, since transitions are easier to measure than midpoint values, A/D converter errors are often measured in terms of the analog transition point values, V_{ij}, and we use that approach here.

Resolution The *resolution* of a converter is defined to be the number of distinct analog levels corresponding to the different digital words. Thus, an N-bit resolution implies that the converter can resolve 2^N distinct analog levels. Resolution is not necessarily an indication of the accuracy of the converter, but instead it usually refers to the number of digital input or output bits.

Offset and Gain Error In a D/A converter, the *offset error*, E_{off}, is defined to be the output that occurs for the input code that should produce zero output, or mathematically,

$$E_{off(D/A)} = \left.\frac{V_{out}}{V_{LSB}}\right|_{0\ldots0} \tag{11.22}$$

where the offset error is in units of LSBs. Similarly, for an A/D converter, the offset error is defined as the deviation of $V_{0\ldots01}$ from 1/2 LSB, or mathematically,

$$E_{off(A/D)} = \frac{V_{0\ldots01}}{V_{LSB}} - \frac{1}{2}\,\text{LSB} \tag{11.23}$$

The gain error is defined to be the difference at the full-scale value between the ideal and actual curves when the offset error has been reduced to zero. For a D/A converter, the gain error, $E_{gain(D/A)}$, in units of LSBs, is given by

$$E_{gain(D/A)} = \left(\left.\frac{V_{out}}{V_{LSB}}\right|_{1\ldots1} - \left.\frac{V_{out}}{V_{LSB}}\right|_{0\ldots0}\right) - (2^N - 1) \tag{11.24}$$

For an A/D converter, the equivalent gain error, $E_{gain(A/D)}$ (in units of LSBs), is given by

$$E_{gain(A/D)} = \left(\frac{V_{1\ldots1}}{V_{LSB}} - \frac{V_{0\ldots01}}{V_{LSB}}\right) - (2^N - 2) \tag{11.25}$$

Graphical illustrations of gain and offset errors are shown in Fig. 11.9.

Accuracy

The *absolute accuracy* of a converter is defined to be the difference between the expected and actual transfer responses. The absolute accuracy includes the offset, gain, and linearity errors.

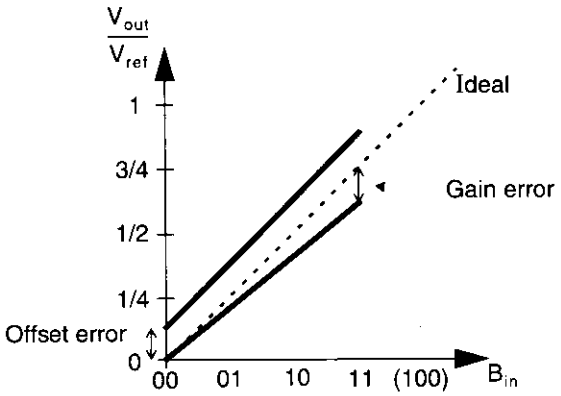


Fig. 11.9 Illustrating offset and gain errors for a 2-bit D/A converter.

The term *relative accuracy* is sometimes used and is defined to be the accuracy after the offset and gain errors have been removed. It is also referred to as the *maximum integral nonlinearity error* (described shortly) and we will refer to it as such.

Accuracy can be expressed as a percentage error of full-scale value, as the effective number of bits, or as a fraction of an LSB. For example, a 12-bit accuracy implies that the converter's error is less than the full-scale value divided by 2^{12}.

Note that a converter may have 12-bit resolution with only 10-bit accuracy, or 10-bit resolution with 12-bit accuracy. An accuracy greater than the resolution means that the converter's transfer response is very precisely controlled (better than the number of bits of resolution).

Integral Nonlinearity (INL) Error After both the offset and gain errors have been removed, the *integral nonlinearity (INL) error* is defined to be the deviation from a straight line. However, what straight line should be used? A conservative measure of nonlinearity is to use the endpoints of the converter's transfer response to define the straight line. An alternative definition is to find the best-fit straight line such that the maximum difference (or perhaps the mean squared error) is minimized. These two definitions are illustrated in Fig. 11.10. One should be aware that, in this book, we define INL values for each digital word (and thus these values can be plotted for a single converter), whereas others sometimes define the term "INL" as the maximum magnitude of the INL values (or equivalently, as the relative accuracy).

Differential Nonlinearity (DNL) Error In an ideal converter, each analog step size is equal to 1 LSB. In other words, in a D/A converter, each output level is 1 LSB from adjacent levels, whereas in an A/D, the transition values are precisely 1 LSB apart. *Differential nonlinearity* (DNL) is defined as the variation in analog step sizes away from 1 LSB (typically, once gain and offset errors have been removed). Thus, an ideal converter has its maximum differential nonlinearity of 0 for all digital values, whereas a converter with a maximum differential nonlinearity of 0.5 LSB has its step

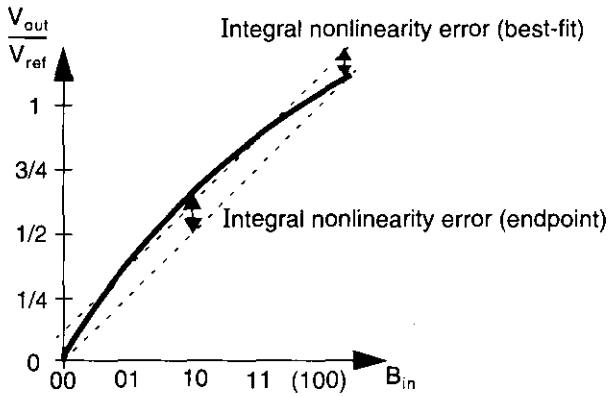


Fig. 11.10 Integral nonlinearity error in a 2-bit D/A converter.

sizes varying from 0.5 LSB to 1.5 LSB. Once again, as in the INL case, we define DNL values for each digital word, whereas others sometimes refer to DNL as the maximum magnitude of the DNL values.

Monotonicity A *monotonic* D/A converter is one in which the output always increases as the input increases. In other words, the slope of the D/A converter's transfer response is of only one sign. If the maximum DNL error is less than 1 LSB, then a D/A converter is guaranteed to be monotonic. However, many monotonic converters may have a maximum DNL greater than 1 LSB. Similarly, a converter is guaranteed to be monotonic if the maximum INL is less than 0.5 LSB.

Missing Codes Although monotonicity is appropriate for D/A converters, the equivalent term for A/D converters is *missing codes*. An A/D converter is guaranteed not to have any missing codes if the maximum DNL error is less than 1 LSB or if the maximum INL error is less than 0.5 LSB.

A/D Conversion Time and Sampling Rate In an A/D converter, the *conversion time* is the time taken for the converter to complete a single measurement including acquisition time of the input signal. On the other hand, the maximum sampling rate is the speed at which samples can be continuously converted and is typically the inverse of the conversion time. However, one should be aware that some converters have a large latency between the input and the output due to pipelining or multiplexing, yet they still maintain a high sampling rate. For example, a pipelined 12-bit A/D converter may have a conversion time of 2 μs (i.e., a sampling rate of 500 kHz) yet a latency from input to output of 24 μs.

D/A Settling Time and Sampling Rate In a D/A converter, the *settling time* is defined as the time it takes for the converter to settle to within some specified amount of the final value (usually 0.5 LSB). The *sampling rate* is the rate at which samples can be continuously converted and is typically the inverse of the settling time.

Sampling-Time Uncertainty Both A/D and D/A converters have limited accuracy when their sampling instances are ill defined. To quantify this *sampling time uncertainty,* also known as *aperture jitter,* for sinusoidal waveforms, consider a full-scale signal, V_{in}, applied to an N-bit, signed, A/D converter with frequency f_{in}. Mathematically,

$$V_{in} = \frac{V_{ref}}{2} \sin(2\pi f_{in} t) \tag{11.26}$$

Since the rate of change (or slope) of V_{in} at the peak of a sinusoidal waveform is small, sampling time uncertainty is less of a problem near the peak values. However, the maximum rate of change for this waveform occurs at the zero crossing and can be found by differentiating V_{in} with respect to time and setting $t = 0$. At the zero crossing, we find that

$$\left.\frac{\Delta V}{\Delta t}\right|_{max} = \pi f_{in} V_{ref} \tag{11.27}$$

If Δt represents some sampling-time uncertainty, and if we want to keep ΔV less than 1 V_{LSB}, we see that

$$\Delta t < \frac{V_{LSB}}{\pi f_{in} V_{ref}} = \frac{1}{2^N \pi f_{in}} \tag{11.28}$$

For example, an 8-bit converter sampling a full-scale 250-MHz sinusoidal signal must keep its sampling-time uncertainty under 5 ps to maintain 8-bit accuracy. Also, the same 5-ps time accuracy is required for a 16-bit converter operating on a full-scale, 1-MHz signal.

Dynamic Range The *dynamic range* of a converter is usually specified as the ratio of the rms value of the maximum amplitude input sinusoidal signal to the rms output noise plus the distortion measured when the same sinusoid is present at the output. The rms output noise plus distortion is obtained by first eliminating the sinusoid from the measured output. In a D/A converter, the output sinusoid can be eliminated by using a spectrum analyzer and ignoring the power at that particular frequency. For an A/D converter, a similar approach can be taken by using an FFT and eliminating the fundamental of the output, or a least-mean-squared fit can be used to find the amplitude and phase of a sinusoid at the input signal's frequency and then subtracting the best-fit sinusoid from the output signal. Dynamic range can also be expressed as an effective number of bits using the relationship presented in (11.16).

It should be noted that this approach often results in a dynamic range measurement that is a function of the frequency of the sinusoidal input. Hence, it is a more realistic way of measuring the performance of a converter than extrapolating the nonlinearity performance found using dc inputs. For example, if an 8-bit, 200-MHz, A/D converter has a band-limited preamplifier or a slew-rate limited sample and hold, dc inputs may show full 8-bit performance even at the maximum sample rate of 200 sample/s. However, a high-frequency, sinusoidal input, at, say, 40 MHz, will require

the input stage to track a rapidly varying signal and may result in only 6-bit performance.

Finally, it should be mentioned that the distortion level (or nonlinearity performance) of many converters remains at a fixed level and is not a function of the input signal level. Thus, as the input signal level is decreased, the signal-to-distortion ratio decreases. This behavior occurs because the distortion level is often determined by component matching and thus is fixed once the converter is realized. However, in some converters, the distortion level decreases as the input signal level is decreased, which is often a desirable property to have. For example, most 1-bit oversampling converters have this desirable property since they do not rely on component matching and their distortion level is often a result of weak nonlinear effects at the input stage.

EXAMPLE 11.4

Consider a 3-bit D/A converter in which $V_{ref} = 4$ V, with the following measured voltage values:

$$\{0.011 : 0.507 : 1.002 : 1.501 : 1.996 : 2.495 : 2.996 : 3.491\}$$

1. Find the offset and gain errors in units of LSBs.
2. Find the INL (endpoint) and DNL errors (in units of LSBs).
3. Find the effective number of bits of absolute accuracy.
4. Find the effective number of bits of relative accuracy.

Solution

We first note that 1 LSB corresponds to $V_{ref}/2^3 = 0.5$ V.

1. Since the offset voltage is 11 mV, and since 0.5 V corresponds to 1 LSB, we see that the offset error is given by

$$E_{off(D/A)} = \frac{0.011}{0.5} = 0.022 \text{ LSB} \tag{11.29}$$

For the gain error, from (11.25) we have

$$E_{gain(D/A)} = \left(\frac{3.491 - 0.011}{0.5}\right) - (2^3 - 1) = -0.04 \text{ LSB} \tag{11.30}$$

2. For INL and DNL errors, we first need to remove both offset and gain errors in the measured D/A values. The offset error is removed by subtracting 0.022 LSB off each value, whereas the gain error is eliminated by subtracting off scaled values of the gain error. For example, the new value for 1.002 (scaled to 1 LSB) is given by

$$\frac{1.002}{0.5} - 0.022 + \left(\frac{2}{7}\right)(0.04) = 1.993 \tag{11.31}$$

Thus, the offset-free, gain-free, scaled values are given by

$$\{0.0 : 0.998 : 1.993 : 2.997 : 3.993 : 4.997 : 6.004 : 7.0\}$$

Since these results are in units of LSBs, we calculate the INL errors as the difference between these values and the ideal values, giving us

INL errors: $\{0 : -0.002 : -0.007 : -0.003 : -0.007 : -0.003 : 0.004 : 0\}$

For DNL errors, we find the difference between adjacent offset-free, gain-free, scaled values to give

DNL errors: $\{-0.002 : -0.005 : 0.004 : -0.004 : 0.004 : 0.007 : -0.004\}$

3. For absolute accuracy, we find the largest deviation between the measured values and ideal values, which, in this case, occurs at 0 V and is 11 mV. To relate this 11-mV value to effective bits, 11 mV should correspond to 1 LSB when $V_{ref} = 4$ V. In other words, we have the relationship

$$\frac{4 \text{ V}}{2^{N_{eff}}} = 11 \text{ mV} \tag{11.32}$$

which results in an absolute accuracy of $N_{abs} = 8.5$ bits.

4. For relative accuracy, we use the INL errors found in part 2, whose maximum magnitude is 0.007 LSB, or equivalently, 3.5 mV. We relate this 3.5-mV value to effective bits in the same manner as in part 3, resulting in a relative accuracy of $N_{rel} = 10.2$ bits.

EXAMPLE 11.5

A full-scale sinusoidal waveform is applied to a 12-bit A/D converter, and the output is digitally analyzed. If the fundamental has a normalized power of 1 W while the remaining power is 0.5 μW, what is the effective number of bits for the converter?

Solution

Using (11.16), we have

$$\text{SNR} = 6.02N_{eff} + 1.76 \tag{11.33}$$

In this case, the signal-to-noise ratio is found to be

$$\text{SNR} = 10 \log\left(\frac{1}{0.5 \times 10^{-6}}\right) = 63 \text{ dB} \tag{11.34}$$

Substituting this SNR value into (11.33), we find

$$N_{eff} = \frac{63 - 1.76}{6.02} = 10.2 \text{ effective bits} \tag{11.35}$$

11.6 REFERENCES

Analog Devices. *Analog-Digital Conversion Handbook.* Prentice Hall, Englewood Cliffs, New Jersey, 1986.

A. B. Grebene. *Bipolar and MOS Analog Integrated Circuit Design.* John Wiley & Sons, New York, 1984.

R. van de Plassche. *Integrated Analog-to-Digital and Digital-to-Analog Converters.* Kluwer Academic Publishers, Dordrecht, the Netherlands, 1994.

11.7 PROBLEMS

11.1 For an ideal 10-bit, unipolar D/A converter with $V_{LSB} = 1$ mV, what is the largest output voltage?

11.2 What is the SNR for an ideal 12-bit unipolar A/D converter with $V_{ref} = 3$ V, when a sinusoidal input of 1 V_{pp} is applied? What size input would result in an SNR of 0 dB?

11.3 Find the equivalent of (11.19) for 2's-complement coding.

11.4 Show that, by using 4-bit 2's-complement words, the correct final sum is obtained when the numbers +5, +5, and –7 are added together while any overflow effects are ignored.

11.5 Starting with two 4-bit 2's-complement words, we want to add +5 and +7 to obtain the correct answer of +12 with a 5-bit word. Show how an extra bit can be added at the left of each of the 4-bit words such that numbers up to ±15 can be represented. This approach is called *sign extension* and can be used to increase the word size of any number.

11.6 What is the representation of +8 and –8 in 5-bit 2's complement? Assuming a circuit added only one of these two numbers to an arbitrary 5-bit word, show a simple logic circuit (i.e., nand, nor, xnor, etc.) that would accomplish such an addition. (*Hint:* Note that the 4 LSBs in +8 and –8 are all 0 and thus do not need to be added.)

11.7 The following measurements are found from a 3-bit unipolar D/A converter with $V_{ref} = 8$ V: (–0.01, 1.03, 2.02, 2.96, 3.95, 5.02, 6.00, 7.08). In units of LSBs, find the offset error, gain error, maximum DNL, and maximum INL.

11.8 How many bits of absolute accuracy does the converter in Problem 11.7 have? How many bits of relative accuracy does it have?

11.9 A 10-bit A/D converter has a reference voltage, V_{ref}, tuned to 10.24 V at 25 °C. Find the maximum allowable temperature coefficient in terms of $(\mu V)/°C$ for the reference voltage if the reference voltage is allowed to cause a maximum error of $(\pm 1/2)$ LSB over the temperature range of 0 to 50 °C.

11.10 Consider the following measured voltage values for a 2-bit D/A with a reference voltage of 4 V:

$$\{00 \leftrightarrow 0.01 \text{ V}\} \quad \{01 \leftrightarrow 1.02 \text{ V}\} \quad \{10 \leftrightarrow 1.97 \text{ V}\} \quad \{11 \leftrightarrow 3.02 \text{ V}\}$$

In units of LSB, find the offset error, gain error, worst absolute and relative accuracies, and worst differential nonlinearity. Restate the relative accuracy in terms of an N-bit accuracy.

11.11 Find the maximum magnitude of quantization error for a 12-bit A/D converter having V_{ref} equal to 5 V and 0.5-LSB absolute accuracy.

11.12 What sampling-time uncertainty can be tolerated for a 16-bit A/D converter operating on an input signal from 0–20 kHz ?

CHAPTER

12 Nyquist-Rate D/A Converters

In this chapter, a variety of methods are discussed for realizing integrated Nyquist-rate digital-to-analog converters (DAC). Nyquist-rate D/A converters can be roughly categorized into four main types: decoder-based, binary-weighted, thermometer-code, and hybrid. Oversampling D/A converters are discussed separately in Chapter 14 due to their importance and because they are best described using many signal processing concepts.

12.1 DECODER-BASED CONVERTERS

Perhaps the most straightforward approach for realizing an N-bit D/A converter is to create 2^N reference signals and pass the appropriate signal to the output, depending on the digital input word. We refer to such D/A converters as *decoder-based converters.*

Resistor String Converters

One of the first integrated MOS 8-bit D/A converters was based on selecting one tap of a segmented resistor string by a switch network [Hamadé, 1978].[1] The switch network was connected in a tree-like decoder, as in the 3-bit D/A converter shown in Fig. 12.1. Notice that there will be one, and only one, low-impedance path between the resistor string and the input of the buffer, and that path is determined by the digital input word, B_{in}. In a CMOS implementation, transmission gates might be used rather than n-channel switches. However, when only n-channel pass transistors are used, the transistor-tree decoder can be laid out quite compactly since no contacts are required in the tree. Also, an n-channel-only approach is not much different in speed than a CMOS transmission-gate implementation; a transmission-gate approach has extra drain and source capacitance to ground, but this extra capacitance is offset by the reduced switch resistance, which is due to the parallel combination of p-channel and n-channel transistors. In addition, a transmission-gate implementation can operate closer to the positive voltage supply.

1. In fact, the resistor-string D/A was used to realize an A/D converter in the reference.

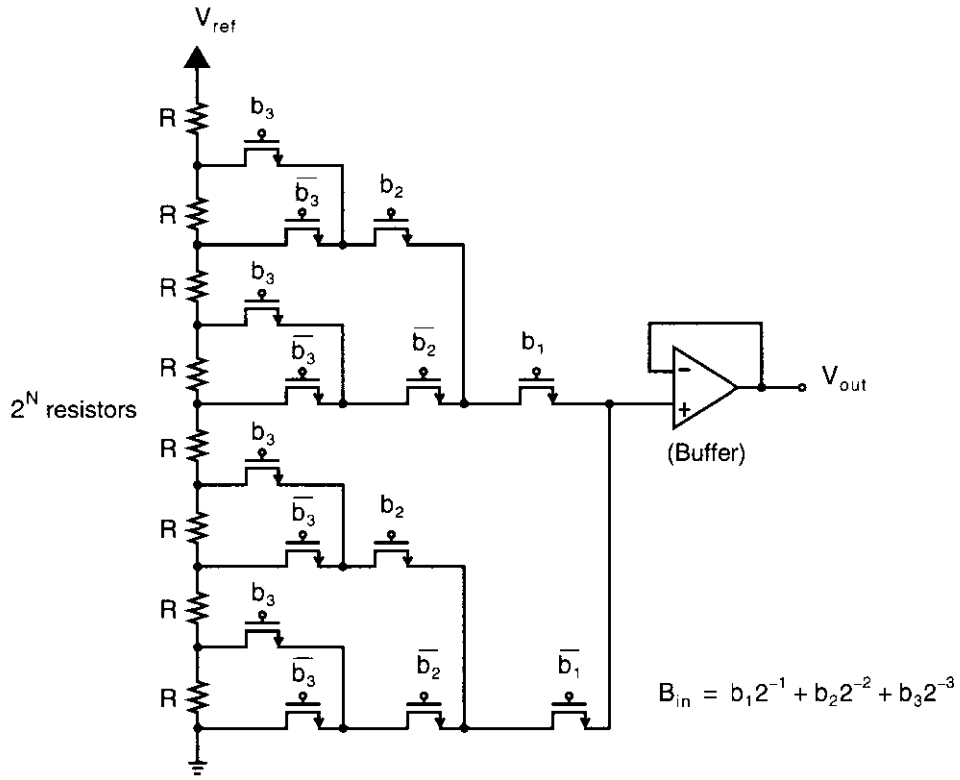


Fig. 12.1 Resistor-string 3-bit D/A converter with a transmission-gate, tree-like decoder.

With a resistor-string approach, if we assume the buffer's offset voltage does not depend on its input voltage, the D/A converter has guaranteed monotonicity since any tap on the resistor string must have a lower voltage than its upper, neighbor tap. Also, the accuracy of this D/A depends on the matching precision of R in the resistor string. Although this resistor-matching precision depends on the type of resistors used, the use of polysilicon resistors that have a resistivity of around 20–30 (ohms per square) can result in up to 10 bits of accuracy.

The delay through the switch network is the major limitation on speed. However, in a multiplying D/A, the delay through the resistor string would also be a major source of delay since V_{ref} would become a second input signal. A useful technique for estimating the settling-time behavior in RC type circuits (i.e., circuits that have only real-axis poles) is the *open-circuit time-constant* approach [Sedra, 1991]. Specifically, the dominant high-frequency time constant is estimated as the sum of the individual time constants due to each of the capacitances when all other capacitances are set to zero (i.e., replaced with open circuits). To find the individual time constant for a given capacitance, independent voltage sources are replaced with ground (independent current sources are opened), and the resistance seen by that capacitor is determined.

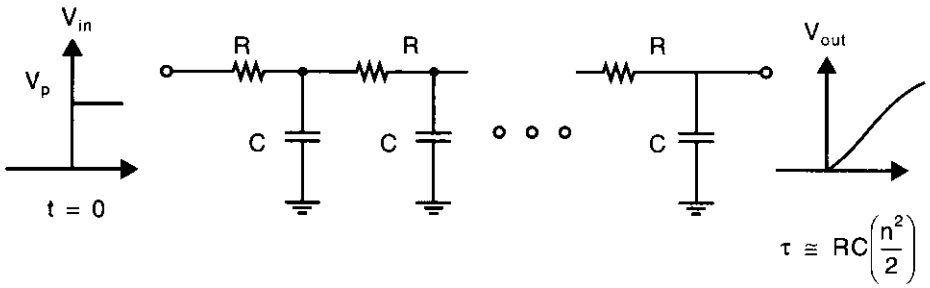


Fig. 12.2 Estimating the time constant for n resistors and capacitors in series.

EXAMPLE 12.1

Show that an estimate of the time constant for a network of n resistors, each of size R in series, with capacitive loading C at each node (see Fig. 12.2), is given by $\tau = RC(n^2/2)$. How much settling time is required for the output to settle to 0.1 percent of its final value?

Solution

The open-circuit time constant due to the first capacitor on the left is simply RC. The second capacitor from the left has an individual time constant of $2RC$ and so on. Thus, the dominant high-frequency time constant, τ, is estimated as

$$\tau \cong RC(1 + 2 + \cdots + n)$$

The sum from 1 to n can be shown to be equal to $n(n + 1)/2$ and, thus, for a large n, the dominant time constant can be estimated by

$$\tau \cong RC\left(\frac{n^2}{2}\right)$$

Using this time constant to estimate the output voltage charging behavior, we have

$$v_{out} \cong (1 - e^{-(t/\tau)})V_p$$

Thus, for v_{out} to equal 0.999 V_p, we find that a time of about 7 τ is needed.

In a higher-speed implementation, logic can be used for the decoder, and a single bus is connected to a single resistor-string node, as shown in Fig. 12.3. This approach takes more area for the decoder and also results in a large capacitive loading on the single bus because the 2^N transistors' junctions are connected to the bus. However, if the digital decoder is pipelined, the D/A can be moderately fast.

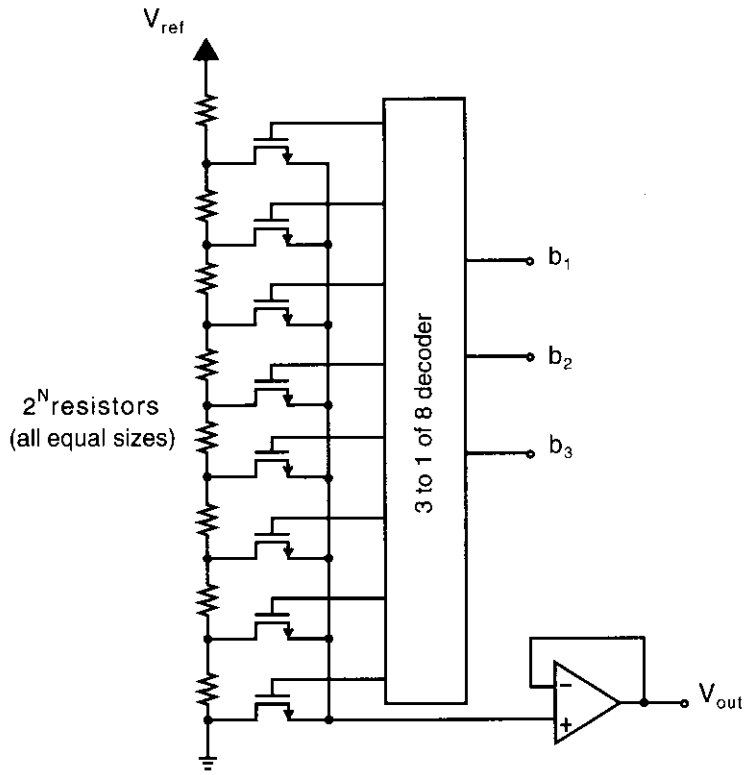


Fig. 12.3 Resistor-string 3-bit D/A converter with digital decoding.

Folded Resistor-String Converters

To reduce the amount of digital decoding and large capacitive loading, a *folded resistor-string D/A* can be used, as shown in Fig. 12.4 [Abrial, 1988]. This approach makes the decoding very similar to that for a digital memory, which reduces the total decoding area. To convert a digital input in this 4-bit example, the most significant bits, $\{b_1, b_2\}$, determine the single word line to be selected (all others will remain low). This operation connects a block of four adjacent resistor nodes to the four-bit lines. One of these bit lines is then connected to the output buffer by the bit-line decoder. Notice that the total number of transistor junctions on the output line is now $2\sqrt{2^N}$ because a set of transistors is connected directly to the output line and another set is connected to the chosen bit line. Thus, for a 10-bit converter, this approach would have a capacitive load of 64 junctions, as opposed to 1,024 junctions when we use the digital-decoding approach shown in Fig. 12.3. Unfortunately, the increase in speed is not equal to this large ratio since, when a word line goes high, all the bit lines must be pulled to new voltage levels—not just the one bit line connected to the output buffer.

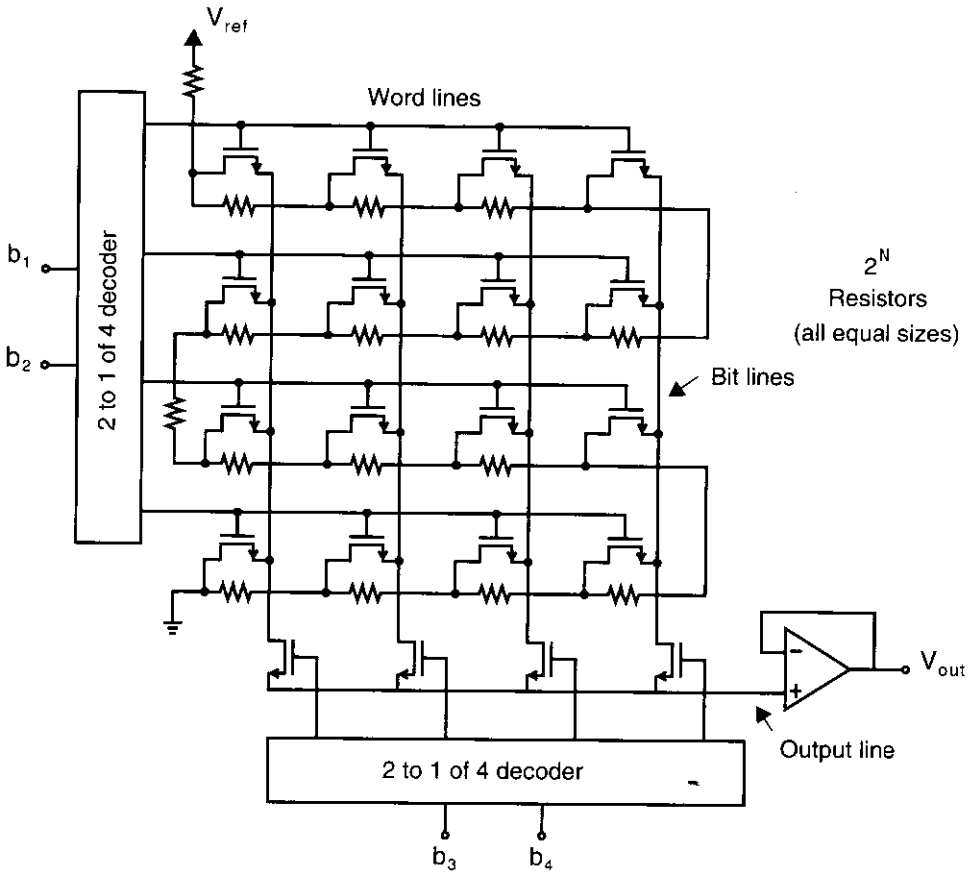


Fig. 12.4 A 4-bit folded resistor-string D/A converter.

Multiple R-String Converters

In this variation, a second tapped resistor string is connected between buffers whose inputs are two adjacent nodes of the first resistor string, as shown in Fig. 12.5 [Holloway, 1984]. In the shown 6-bit example, the three MSBs determine which two adjacent nodes of the first resistor string are connected to the two intermediate buffers. The second resistor string linearly interpolates between the two adjacent voltages from the first resistor string. Finally, the output is determined by the lower LSBs where extra logic must take into account that sometimes the top intermediate buffer has the higher voltage, whereas at other times it has the lower voltage. This approach requires only $2 \times 2^{N/2}$ resistors, making it suitable for higher-resolution, low-power applications. This approach also has guaranteed monotonicity, assuming the opamps have matched, voltage-insensitive offset voltages. However, the opamps must be fast and low noise, which can be achieved using a

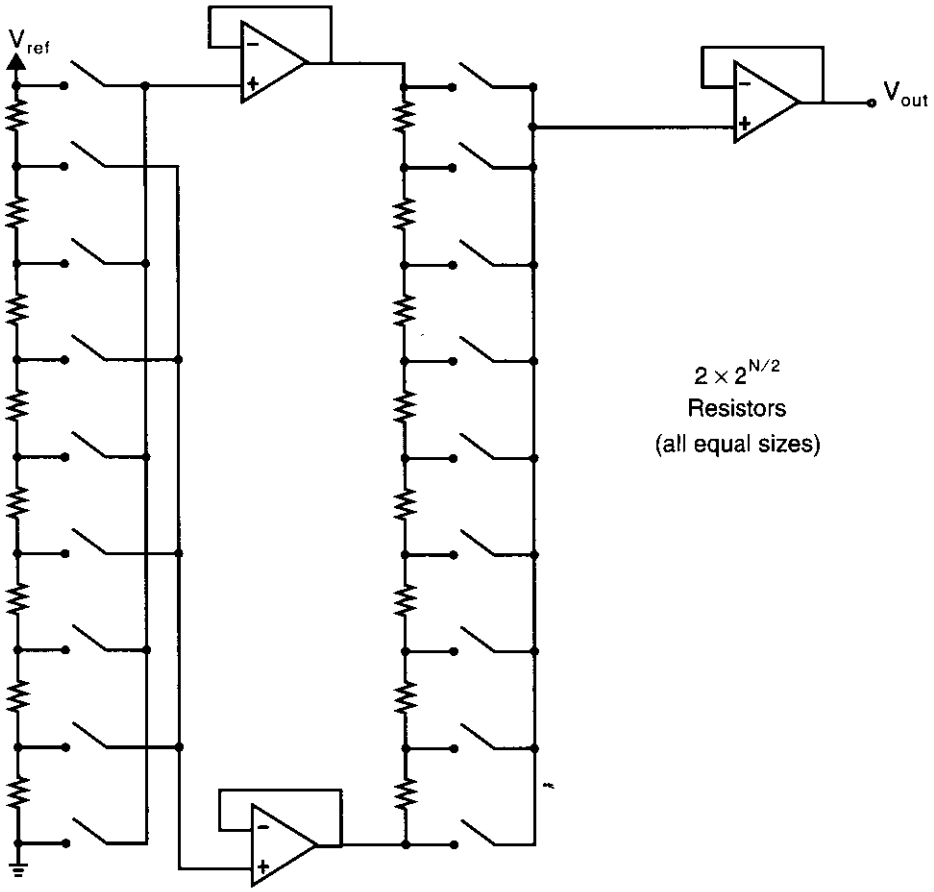


Fig. 12.5 Multiple R-string 6-bit D/A converter.

BiCMOS process. Another point to note here is that, since the second resistor string is used to decode only the lower-order bits, the matching requirements of the second resistor string are not nearly as severe as those for the first string.

EXAMPLE 12.2

Assume that the first resistor string of a 10-bit, multiple-R-string, D/A converter must match to 0.1 percent, and that the first string realizes the top 4 bits. What is the matching requirement of the second resistor string, which realizes the lower 6 bits?

Solution

Errors in the first resistor string correspond directly to errors in the overall D/A output. However, since the second resistor string forms the lower LSB

bits (6 bits, in this case), errors in the matching of these resistors cause an error only in the LSB portion of the output voltage. As a result, the second resistor string need match only to

$$2^4 \times 0.1\% = 1.6\% \tag{12.1}$$

Signed Outputs

In applications where negative output voltages are required, the bottom of the resistor string can be connected to $-V_{ref}$. This requires a negative power supply, and the circuit needed to realize a dual power supply with exactly matched voltages is nontrivial since any error in matching will result in an offset error. Many papers on D/A converters assume that $-V_{ref}$ is available but do not explain how it was obtained. If it is obtained off chip, the cost is significantly higher. One possibility is to use a switched-capacitor gain amplifier, as shown in Fig. 12.6, where a negative output can be realized by changing the clock phases of the input switches so an inverting amplifier is realized [Martin, 1987]. Another possibility is to sense the center tap of the resistor string and adjust $-V_{ref}$ to get the center tap voltage equal to zero volts.

12.2 BINARY-SCALED CONVERTERS

The most popular approach for realizing at least some portion of D/A converters is to combine an appropriate set of signals that are all related in a binary fashion. This binary array of signals might be currents (in resistor or current approaches), but binary-weighted arrays of charge are also commonly used. In this section, resistor approaches are first discussed, followed by charge redistribution and current mode.

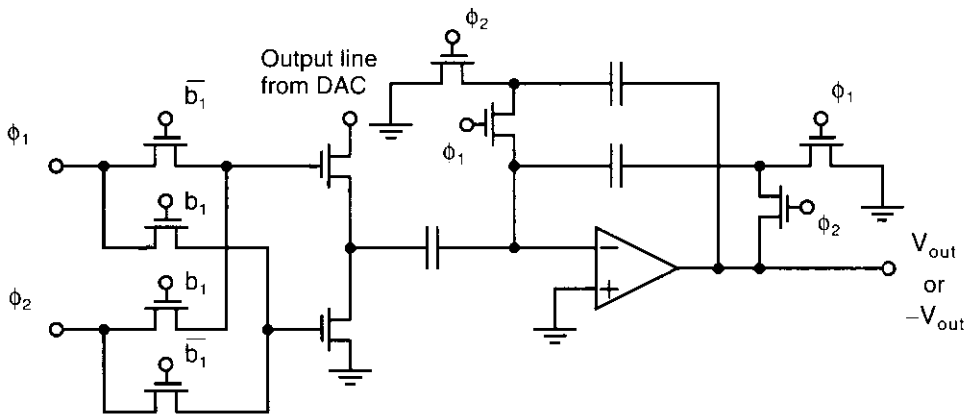


Fig. 12.6 Using an SC gain amplifier to realize a signed output from a unipolar (positive) DAC output. b_1 high causes a negative output.

Binary-Weighted Resistor Converters

Binary-weighted resistor converters are popular for a bipolar technology so that bipolar differential pairs can be used for current switches. The basic architecture for a 4-bit converter is shown in Fig. 12.7.

If b_i is a 1, then the current to the ith resistor comes from the virtual ground of the opamp; otherwise, it comes from ground. Therefore, we have

$$\begin{aligned} V_{out} &= -R_F V_{ref}\left(-\frac{b_1}{2R} - \frac{b_2}{4R} - \frac{b_3}{8R} - \cdots\right) \\ &= \left(\frac{R_F}{R} V_{ref}\right) B_{in} \end{aligned} \tag{12.2}$$

where

$$B_{in} = b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots \tag{12.3}$$

Although this approach does not require many resistors or switches, it does have some disadvantages. The resistor and current ratios are on the order of 2^N, which may be large, depending on N. This large current ratio requires that the switches also be scaled so that equal voltage drops appear across them for widely varying current levels. Also, monotonicity is not guaranteed. Finally, this approach is prone to glitches for high-speed operation, as discussed on page 474.

Reduced-Resistance-Ratio Ladders

To reduce the large resistor ratios in a binary-weighted array, signals in portions of the array can be scaled by introducing a series resistor, as shown in Fig. 12.8. Here, note that the voltage node, V_A, is equal to one-fourth the reference voltage, V_{ref}, as a result of inserting the series resistor of value 3R. Also note that an additional 4R resistor was added (to ground) such that resistance seen to the right of the 3R resistor equals

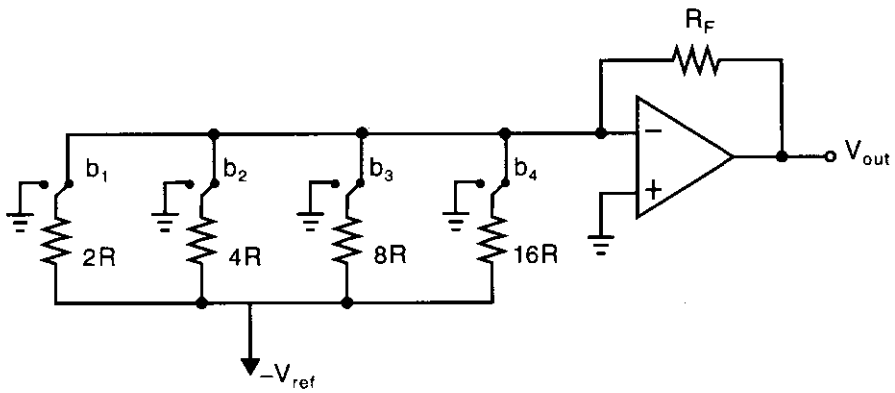


Fig. 12.7 Binary-weighted 4-bit resistor D/A converter.

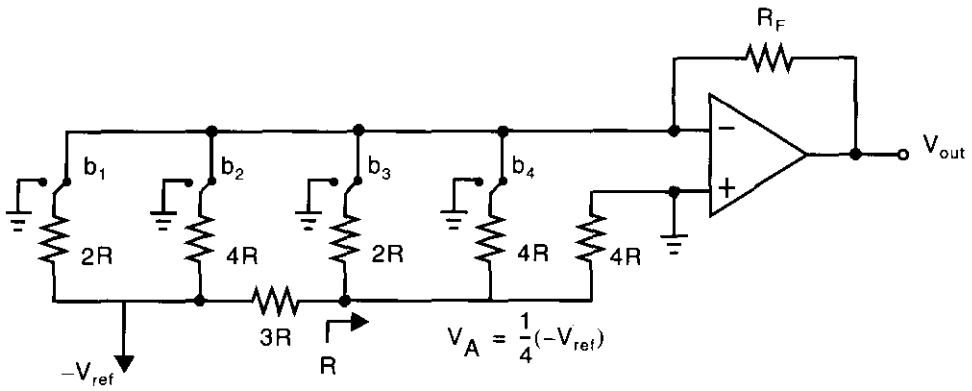


Fig. 12.8 Reduced-resistance-ratio 4-bit D/A converter.

R. Straightforward analysis shows that this converter has the same relationship to the binary digital signals as in the previous binary-weighted case, but with one-fourth the resistance ratio. Note, however, the current ratio has remained unchanged. Finally, note that, by repeating this procedure recursively to a binary-weighted ladder, one arrives at a structure commonly referred to as an *R-2R ladder,* described next.

R-2R-Based Converters

A very popular architecture for D/A converters uses R-2R ladders. These ladders are useful for realizing binary-weighted currents with a small number of components and with a resistance ratio of only 2, independent of the number of bits, N.

Consider the R-2R ladder network shown in Fig. 12.9. Analysis gives

$$\begin{aligned} R_4' &= 2R \\ R_4 &= 2R \parallel 2R = R \\ R_3' &= R + R_4 = 2R \\ R_3 &= 2R \parallel R_3' = R \end{aligned} \tag{12.4}$$

and so on. Thus, $R_i' = 2R$ for all i. This result gives the following current relationships:

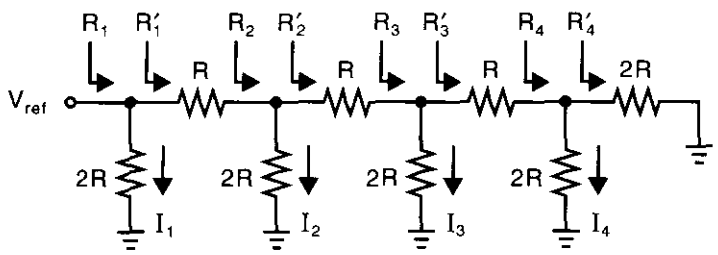


Fig. 12.9 R-2R resistance ladder.

$$I_1 = \frac{V_{ref}}{2R} \tag{12.5}$$

Also, the voltage at node 2 is one-half the voltage at node 1, giving

$$I_2 = \frac{V_{ref}}{4R} \tag{12.6}$$

At node 3, the voltage divides in half once again, therefore

$$I_3 = \frac{V_{ref}}{8R} \tag{12.7}$$

and so on.

Thus, the R-2R ladder can be used to obtain binary-weighted currents while using only a single-size resistor. (The resistors of size 2R are made out of two resistors of size R, to improve matching properties.) As a result, this R-2R approach usually gives both a smaller size and a better accuracy than a binary-sized approach.

A 4-bit D/A converter that uses an R-2R ladder is shown in Fig. 12.10. For this R-2R -based circuit, we see that

$$I_r = V_{ref}/(2R) \tag{12.8}$$

and

$$V_{out} = R_F \sum_{i=1}^{N} \frac{b_i I_r}{2^{i-1}} = V_{ref} \left(\frac{R_F}{R}\right) \sum_{i=1}^{N} \frac{b_i}{2^i} \tag{12.9}$$

However, as already mentioned, although the resistance ratio has been reduced, the current ratio through the switches is still large, and thus the switch sizes are usually scaled in size to accommodate the widely varying current levels. One approach to reduce this current ratio is shown in Fig. 12.11, where equal currents flow through all the switches. However, this configuration is typically slower since the internal nodes

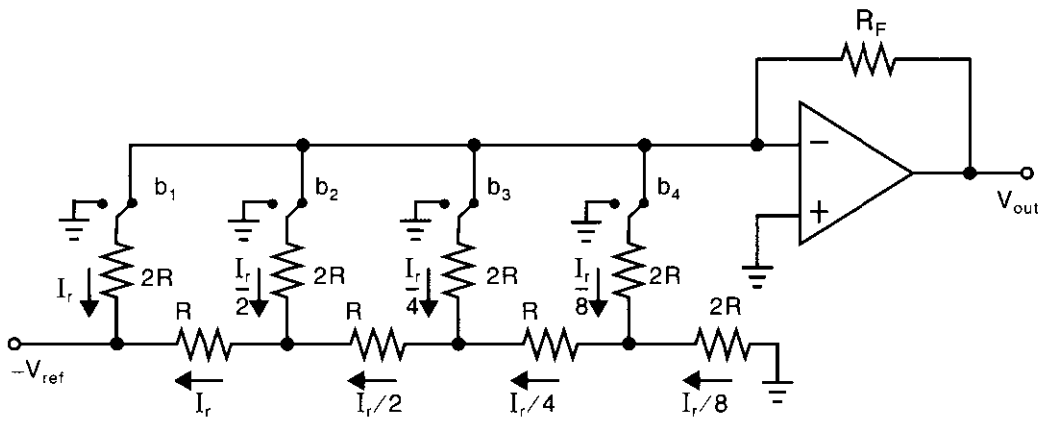


Fig. 12.10 4-bit R-2R based D/A converter.

of the R-2R ladder now exhibit some voltage swings (as opposed to the configuration in Fig. 12.10 where internal nodes all remain at fixed voltages).

Charge-Redistribution Switched-Capacitor Converters

The basic idea here is to simply replace the input capacitor of an SC gain amplifier by a *programmable capacitor array* (PCA) of binary-weighted capacitors, as shown in Fig. 12.12. As in the SC gain amplifier, the shown circuit is insensitive to opamp input-offset voltage, 1/f noise, and finite-amplifier gain. Also, an additional sign bit can be realized by interchanging the clock phases (shown in parentheses) for the input switches.

It should be mentioned here that, as in the SC gain amplifier, carefully generated clock waveforms are required to minimize the voltage dependency of clock feedthrough, and a deglitching capacitor should be used. Also, the digital codes should be

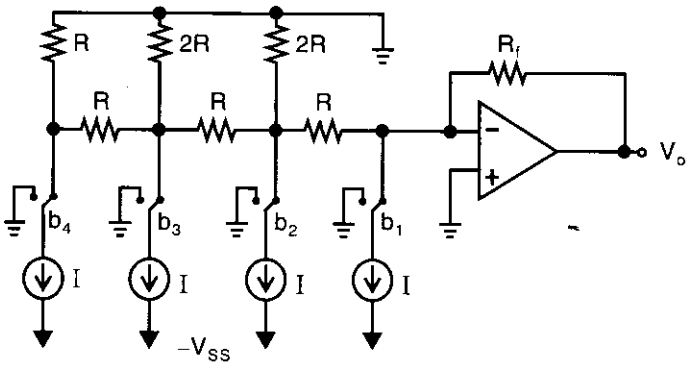


Fig. 12.11 R-2R ladder D/A converter with equal currents through the switches.

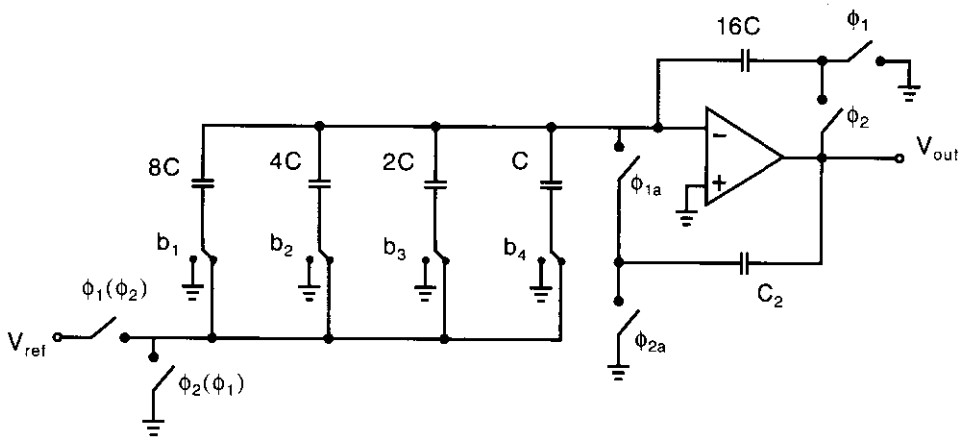


Fig. 12.12 Binary-array charge-redistribution D/A converter.

changed only when the input side of the capacitors are connected to ground, and thus the switching time is dependent on the sign bit, which requires some extra digital complexity.

Current-Mode Converters

Current-mode D/A converters are very similar to resistor-based converters, but are intended for higher-speed applications. The basic idea is to switch currents to either the output or to ground, as shown in Fig. 12.13. Here, the output current is converted to a voltage through the use of R_F, and the upper portion of each current source always remains at ground potential. Implementations of current-mode D/A converters are more fully discussed in Section 12.3, where thermometer codes are introduced.

Glitches

Glitches are a major limitation during high-speed operation for converters that have digital logic, $\{b_1, b_2, \ldots, b_N\}$, directly related to switching signals. Glitches are mainly the result of different delays occurring when switching different signals. For example, when the digital input code changes from 0111 . . . 1 to 1000 . . . 0, all of the $N-1$ LSBs turn off and the MSB turns on. However, it is possible that the currents due to the LSB switches will turn off slightly before the MSB current, causing the current to temporarily fall to zero. Alternatively, if the LSB switches turn off slightly after the MSB current, the current will temporarily go to its maximum value. In either case, a glitch occurs at the output unless these two delays are exactly matched, which is highly unlikely since the branches have different currents. This glitch phenomenon is illustrated in Fig. 12.14.

The glitch disturbance can be reduced by limiting the bandwidth (by placing a capacitor across the resistor R_f in Fig. 12.14), but this approach slows down the circuit. Another approach is to use a sample and hold on the output signal. Finally, the most popular way to reduce glitches is to modify some or all of the digital word from a binary code to a thermometer code, as discussed next.

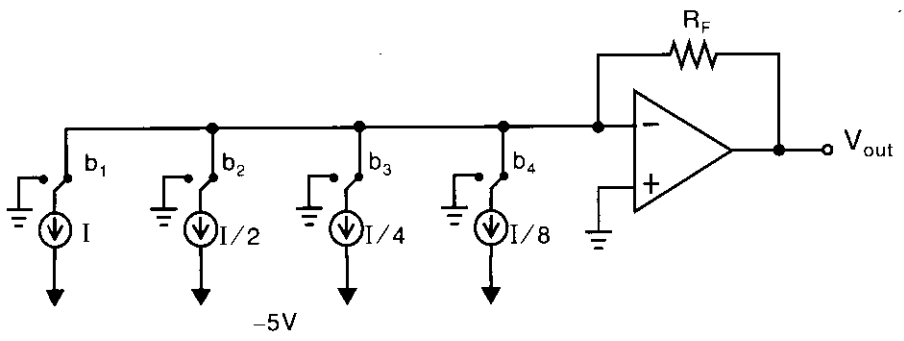


Fig. 12.13 Binary-weighted current-mode D/A converter.

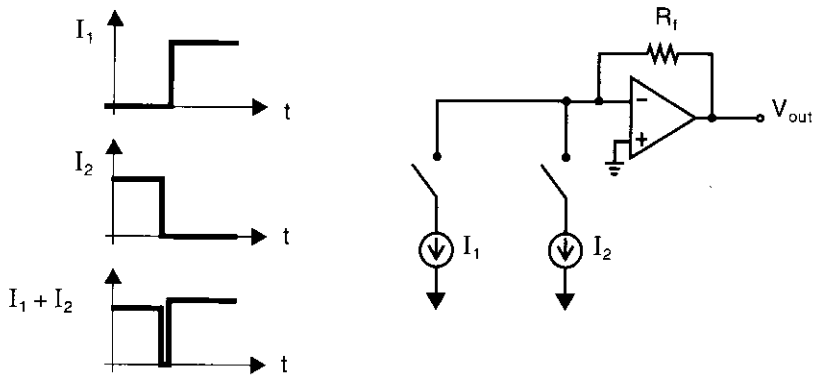


Fig. 12.14 Glitches. I_1 represents the MSB current, and I_2 represents the sum of the $N-1$ LSB currents. Here, the MSB current turns off slightly early, causing a glitch of zero current.

12.3 THERMOMETER-CODE CONVERTERS

Another method for realizing a D/A converter is to digitally recode the input value to a thermometer-code equivalent. A *thermometer code* differs from a binary one in that a thermometer code has $2^N - 1$ digital inputs to represent 2^N different digital values. Clearly, a thermometer code is not a minimal representation since a binary code requires only N digital inputs to represent 2^N input values. However, as we will see, a thermometer-based converter does have advantages over its binary counterpart, such as low DNL errors, guaranteed monotonicity, and reduced glitching noise.

Typically, in a thermometer-code representation, the number of 1s represents the decimal value. For example, with a 3-bit binary input, the decimal value 4 is binary coded as 100 while its thermometer equivalent is 0001111. The codes for the remaining values in this 3-bit example are shown in Table 12.1.

One method to realize a D/A converter with the use of a thermometer-code input is to build $2^N - 1$ equal-sized resistors and switches attached to the virtual ground of an opamp, as shown in Fig. 12.15. Note that monotonicity is guaranteed here since,

Table 12.1 Thermometer-code representations for 3-bit binary values

Decimal	Binary			Thermometer Code						
	b_1	b_2	b_3	d_1	d_2	d_3	d_4	d_5	d_6	d_7
0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	1
2	0	1	0	0	0	0	0	0	1	1
3	0	1	1	0	0	0	0	1	1	1
4	1	0	0	0	0	0	1	1	1	1
5	1	0	1	0	0	1	1	1	1	1
6	1	1	0	0	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1	1	1

when the binary input changes to the next higher number, one more digital value in the thermometer code goes high, causing additional current to be drawn out of the virtual ground and forces the opamp output to go some amount higher (never lower). This is not necessarily the case for a binary-array D/A converter since mismatches between elements may cause the output to go lower even though the digital input value is increased. It should be noted that this mismatch effect is usually the largest in a binary-array converter when the MSB is changed, resulting in the largest DNL at this location.

Perhaps more importantly, a D/A converter based on a thermometer code greatly minimizes glitches, as compared to binary-array approaches, since banks of resistors are never exchanged at slightly different times when the output should change by only 1 LSB. It should also be mentioned here that latches can be used in the binary-to-thermometer code conversion such that no glitches occur in the digital thermometer-code words and pipelining can be also used to maintain a high throughput speed.

It is also of interest to note that the use of a thermometer code does not increase the size of the analog circuitry compared to a binary-weighted approach. In a 3-bit binary-weighted approach, the resistor values of R, 2R, and 4R are needed for a total resistance of 7R. This total value is the same as for the 3-bit thermometer-code approach shown in Fig. 12.15, and since resistors are created on an integrated circuit using area that is proportional to their size, each approach requires the same area (ignoring interconnect). The same argument can be used to show that the total area required by the transistor switches is the same since transistors are usually size-scaled in binary-weighted designs to account for the various current densities. All transistor switches in a thermometer-code approach are of equal sizes since they all pass equal currents. Finally, it should be mentioned that a thermometer-code charge-redistribution D/A can also be realized, as shown in Fig. 12.16.

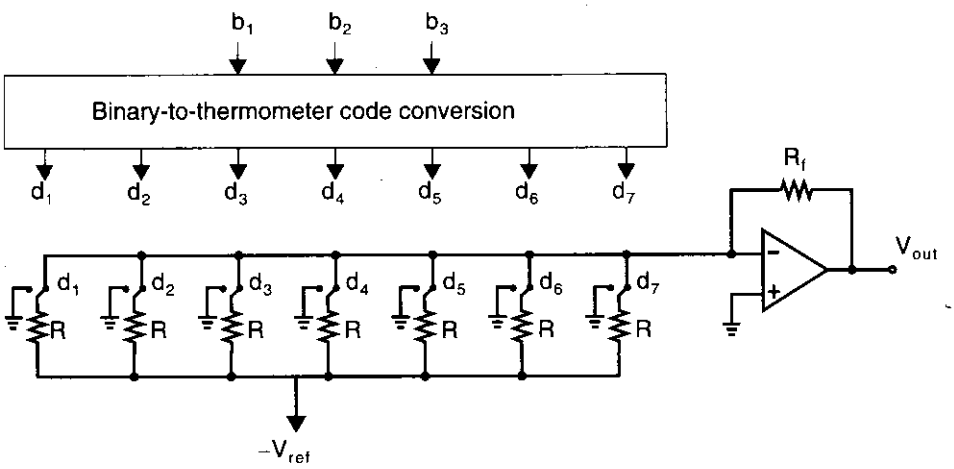


Fig. 12.15 A 3-bit thermometer-based D/A converter.

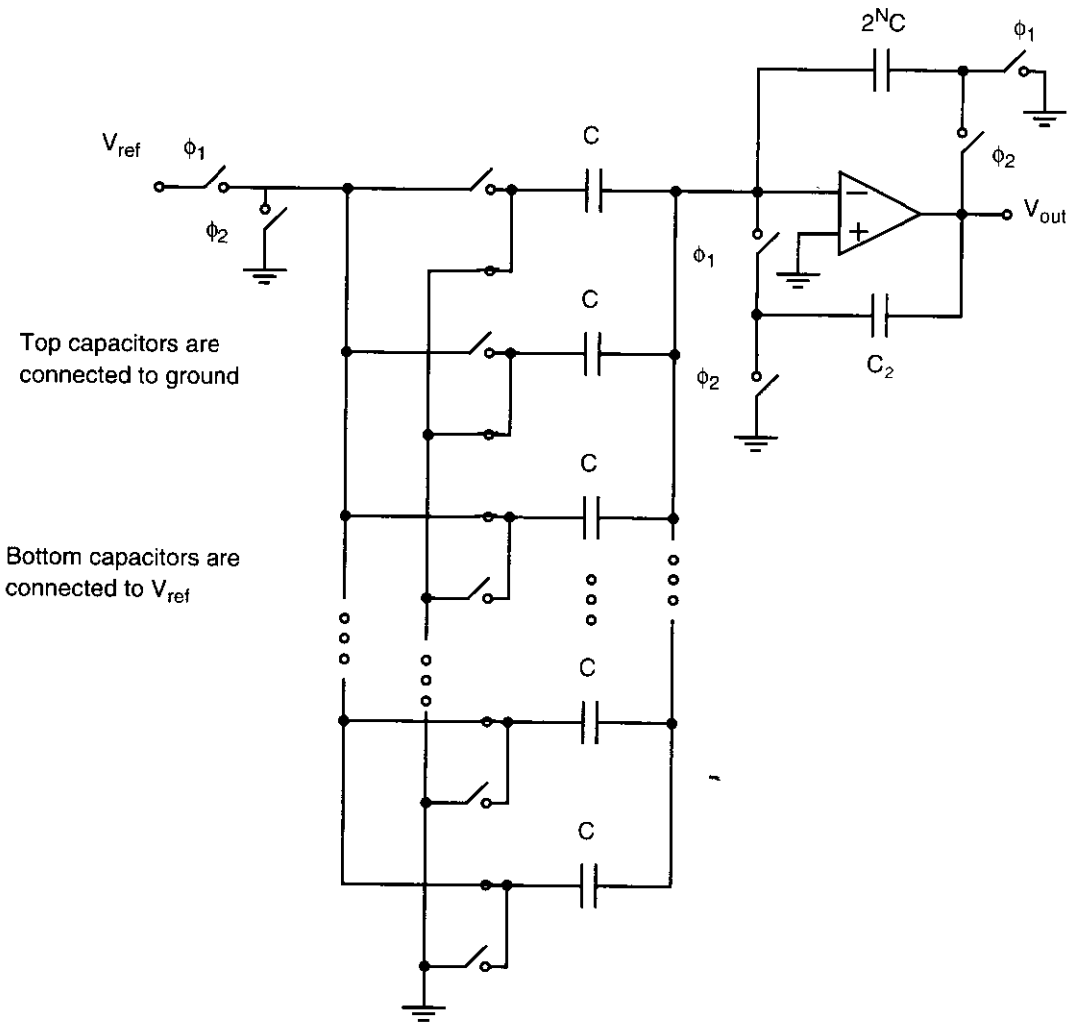


Fig. 12.16 Thermometer-code charge-redistribution D/A converter.

Thermometer-Code Current-Mode D/A Converters

A thermometer-code-based current-mode D/A converter, shown in Fig. 12.17, has been the basis for a variety of designs (see, for example, [Miki, 1986; Chi, 1986; and Letham, 1987]). Here, thermometer-code decoders are used for both the row and column decoders, resulting in inherent monotonicity and good DNL errors. Current is switched to the output when both row and column lines for a cell are high. Also, in high-speed applications, the output feeds directly into an off-chip 50-Ω or 75-Ω resistor, rather than an output opamp. Note that cascode current sources are used here to reduce current-source variation due to voltage changes in the output signal, V_{out}.

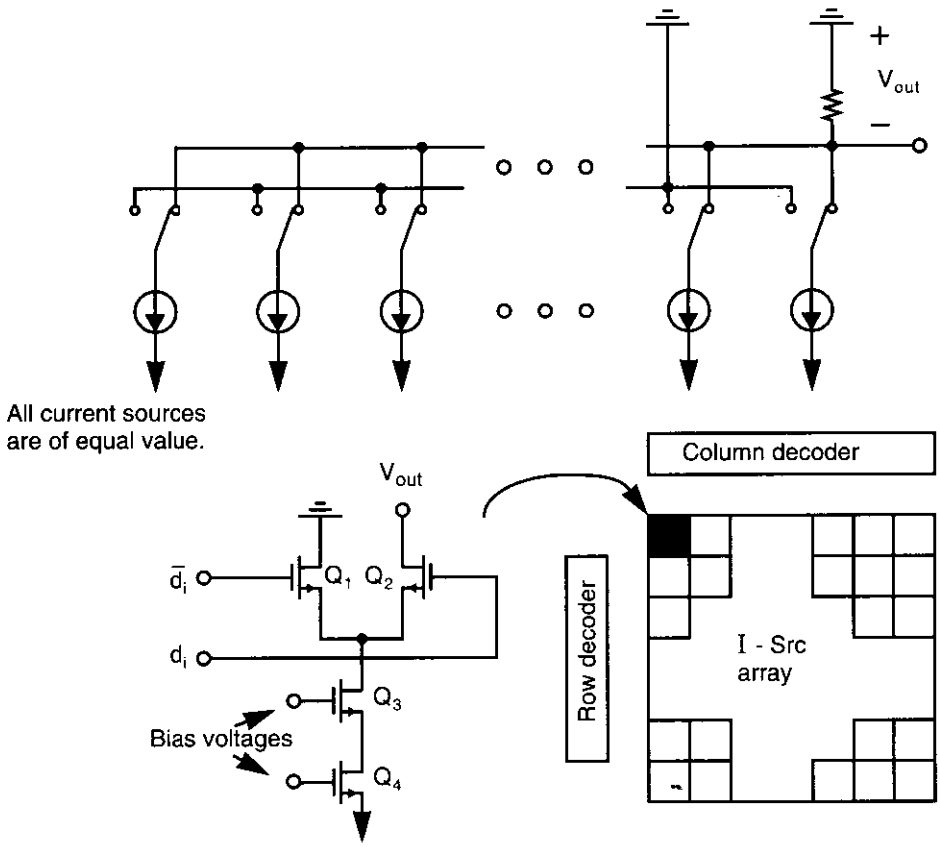


Fig. 12.17 Thermometer-code current-mode D/A converter. Q_1 and Q_2 form the current switch, whereas Q_3 and Q_4 implement a cascode current source.

Note the need here for precisely timed edges of d_i and $\bar{d}_i$. If both logic levels are high simultaneously, V_{out} is shorted to ground. If both logic levels are low at the same time, the drain of Q_3 is pulled low and the circuit takes longer to respond. To avoid the use of two logic driving levels, the gate of Q_2 should be connected to a dc bias voltage, as described in the next approach.

Single-Supply Positive-Output Converters

The architecture for a fast single-supply positive-output D/A (often used in video RAMs, which are known as RAMDACs) is shown in Fig. 12.18 [Colles, 1988]. Here, a matched feedback loop is used to set up accurate known current-source biasing. (Note that the opamp input connections appear reversed but are correct due to signal inversion by Q_4.) Also, to maintain accurate current matching that is independent of V_{out}, one side of each differential current-steering pair is connected to V_{bias}, rather than to the inversion of the bit signal. For example, when the current is steered to the output through Q_2, the drain-source voltage across the current source, Q_3, remains mostly constant if V_{out} stays near zero, such that Q_2 remains in the active region.

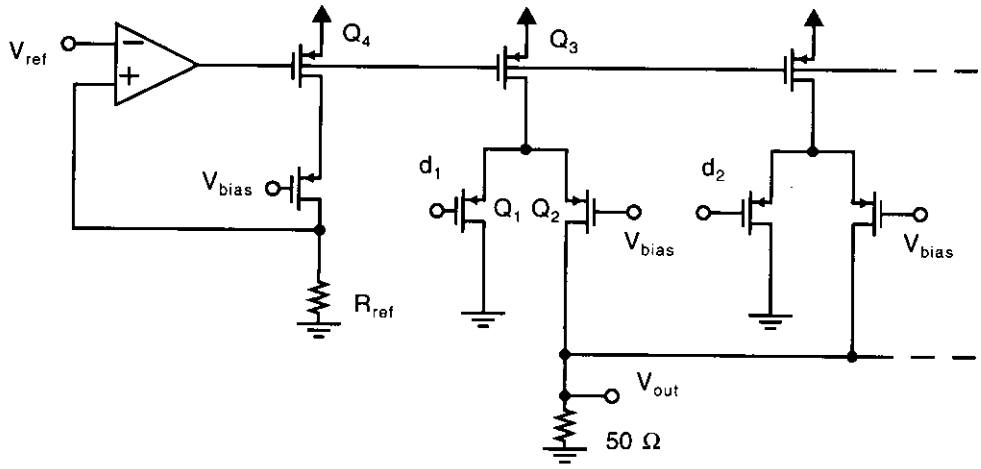


Fig. 12.18 A single-supply positive-output D/A converter.

Thus, Q_2 and Q_3 effectively form a *cascode current source* when they drive current to the output.

To maximize speed in this converter, the voltage swing at the common connections of the current switches (for example, Q_1, Q_2, and Q_3) should be small. To keep this swing small, this common connection should be at a voltage where the output transistors are just turned off when the current is steered to ground. It should also be noted that when a switch is turning on or off, the switching feedthrough from the digital input connected to the grounding transistor (for example, Q_1) actually enhances the switching. Finally, note that this design does not use two logic driving signals, d_i and $\bar{d}_i$, and can therefore be clocked at the maximum rate without the need for precisely timed edges.

Dynamically Matched Current Sources

The use of dynamic techniques with current switching is a method for realizing very well-matched current sources (up to 16-bit accuracy) for audio-frequency D/A converters [Schouwenaars, 1988].

This approach was used to design a 16-bit audio-frequency D/A converter, where the 6 MSB were realized using a thermometer code. Since the accuracy requirements are reduced for the remaining bits, a binary array was used in their implementation. The basic idea for realizing 63 accurately matched current sources for the 6 MSBs is illustrated in Fig. 12.19. Here, we want to set all the currents I_{di} to the same precise value, independent of transistor mismatches and charge injection. To accomplish this high degree of matching, each current source I_{di} is periodically calibrated with the use of a single reference current source, I_{ref}, through the use of the shift register. In other words, once calibration is accomplished on I_{d1}, the same current source, I_{ref}, is used to set the next current source, I_{d2}, to the same value as I_{d1}, and so on. Before proceeding to see how this calibration is accomplished, it is worth mentioning that the values of I_{di} need not precisely equal I_{ref} but do need to accurately match each other.

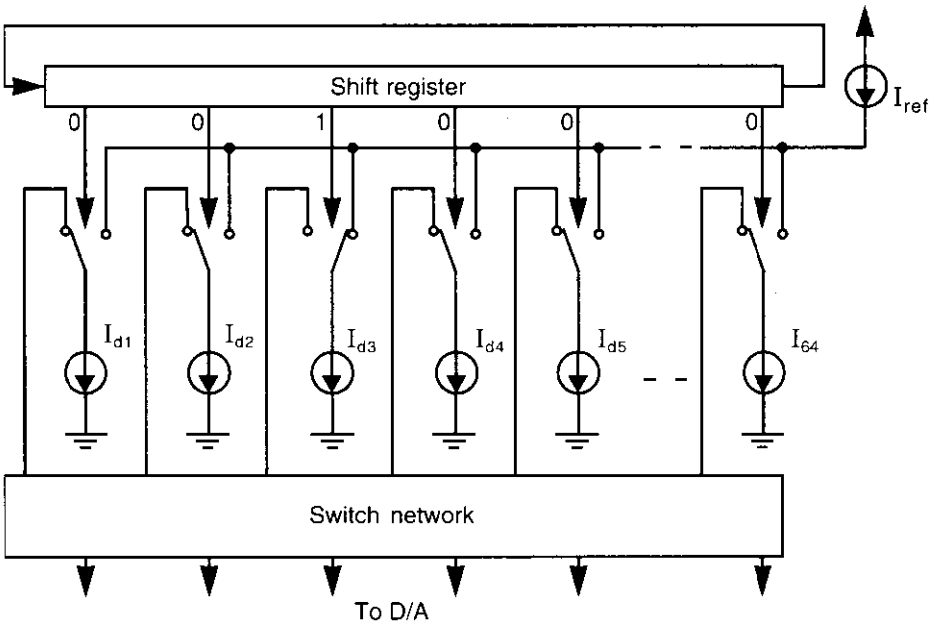


Fig. 12.19 Dynamically matching current sources for 6 MSB.

Therefore, any common errors in the calibration stage are not a problem. Also, note that 64 current sources are calibrated, even though only 63 are required for the 6 MSB. This extra current source is needed so that the D/A converter can continuously operate, even when one of the current sources is being calibrated.

The method for calibrating and using one of the current sources is shown in Fig. 12.20, for I_{d1}. During calibration, the current source is connected to the reference current I_{ref}, while Q_1 is configured in a diode-connected mode. This places whatever voltage is necessary across the parasitic C_{gs} so that I_{d1} equals I_{ref}. When S_1 is opened, I_{d1} remains nearly equal to I_{ref}, assuming the drain-source voltage of Q_1 doesn't change and the clock feedthrough and charge injection of S_1 are small. During regular system use, the gate voltage (and therefore current) is determined by the voltage stored on the parasitic capacitance, C_{gs}.

A major limitation in matching the 64 current sources is due to the differences in clock feedthrough and charge injection of the switches S_i. Since mismatches will always exist between different switches, the best way to keep all current sources equal is to minimize the total amount of clock feedthrough and charge injection. These non-ideal effects can be minimized by having the capacitance C_{gs} and bias voltage V_{GS} large. (A large V_{GS} voltage implies that a small voltage difference will cause a smaller current deviation.) To accomplish these requirements, the current source $0.9I_{ref}$ was added in parallel to Q_1, so that Q_1 needs only to source a current near $0.1I_{ref}$. With such an arrangement, a large, low-transconductance device can be used (a W/L = 1/8 might be used).

Finally, each current source must be recalibrated before the leakage currents (on the order of 10 pA/μm^2 of junction area) on C_{gs} cause the current source to deviate

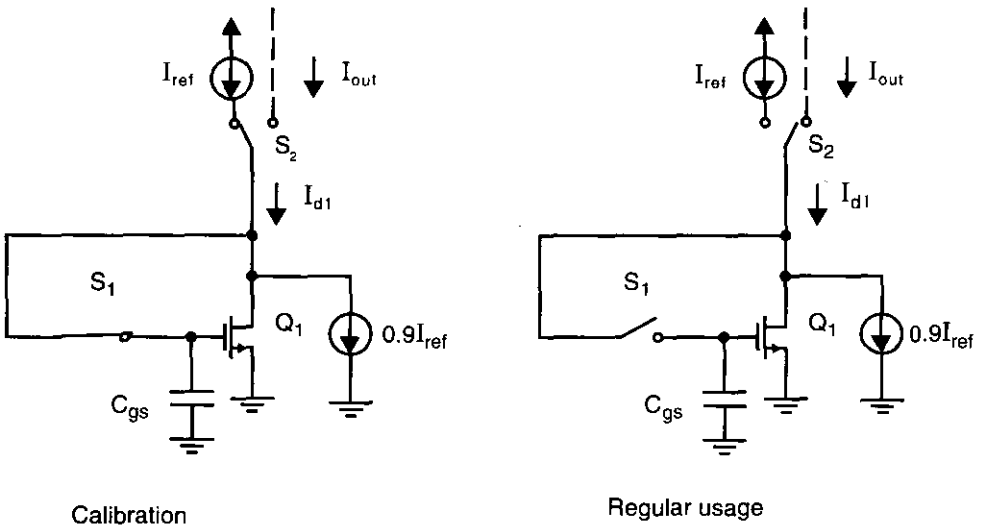


Fig. 12.20 Dynamically setting a current source, I_{d1}.

by 0.5LSB. Fortunately, having a large C_{GS} and V_{GS} has the added benefit of extending this calibration interval (every 1.7 ms in [Schouwenaars, 1988]).

Many other additional details are described in [Schouwenaars, 1988]. For example, during calibration, a p-channel-input common-gate amplifier is added to the diode-connected loop. This is typically done in dynamic switched-current circuits to control the drain-source voltage of Q_1 (i.e., to keep it constant independent of the actual current and to keep it matched to its value during regular use) and to speed up the circuit by decreasing the effect of parasitic capacitances on the large I_{ref} bus. Also, dummy switches are connected to S_1 to help minimize clock feedthrough by partially cancelling the charge injected.

The converter in [Schouwenaars, 1988] achieves 0.0025 percent distortion, 92 dB S/(N+D), 94 db S/N, and only dissipated 20 mW. The converter could also be run using only a 3-V power supply. The clocking frequency is limited to 44 kHz by the digital audio application. No mention is made on the upper limit of the clocking frequency.

12.4 HYBRID CONVERTERS

Combining the techniques discussed in Sections 12.1–12.3 for realizing different portions of a D/A converter results in hybrid designs. Hybrid designs are an extremely popular approach for designing converters because they combine the advantages of different approaches. For example, it is quite common to use a thermometer-code approach for the top few MSBs while using a binary-scaled technique for the lower LSBs. In this way, glitching is significantly reduced and accuracy is high for the MSB where it is needed most. However, in the LSBs where glitching and accuracy requirements are much reduced, valuable circuit area is saved with a binary-scaled approach. This section discusses some useful hybrid designs.

Resistor-Capacitor Hybrid Converters

It is possible to combine tapped resistor strings with switched-capacitor techniques in a number of different ways. In one approach, an SC binary-weighted D/A converter has its capacitors connected to adjacent nodes of a resistor-string D/A converter, as shown in Fig. 12.21 [Yang, 1989]. Here, the top 7 bits determine which pair of voltages across a single resistor is passed on to the 8-bit capacitor array. For example, if

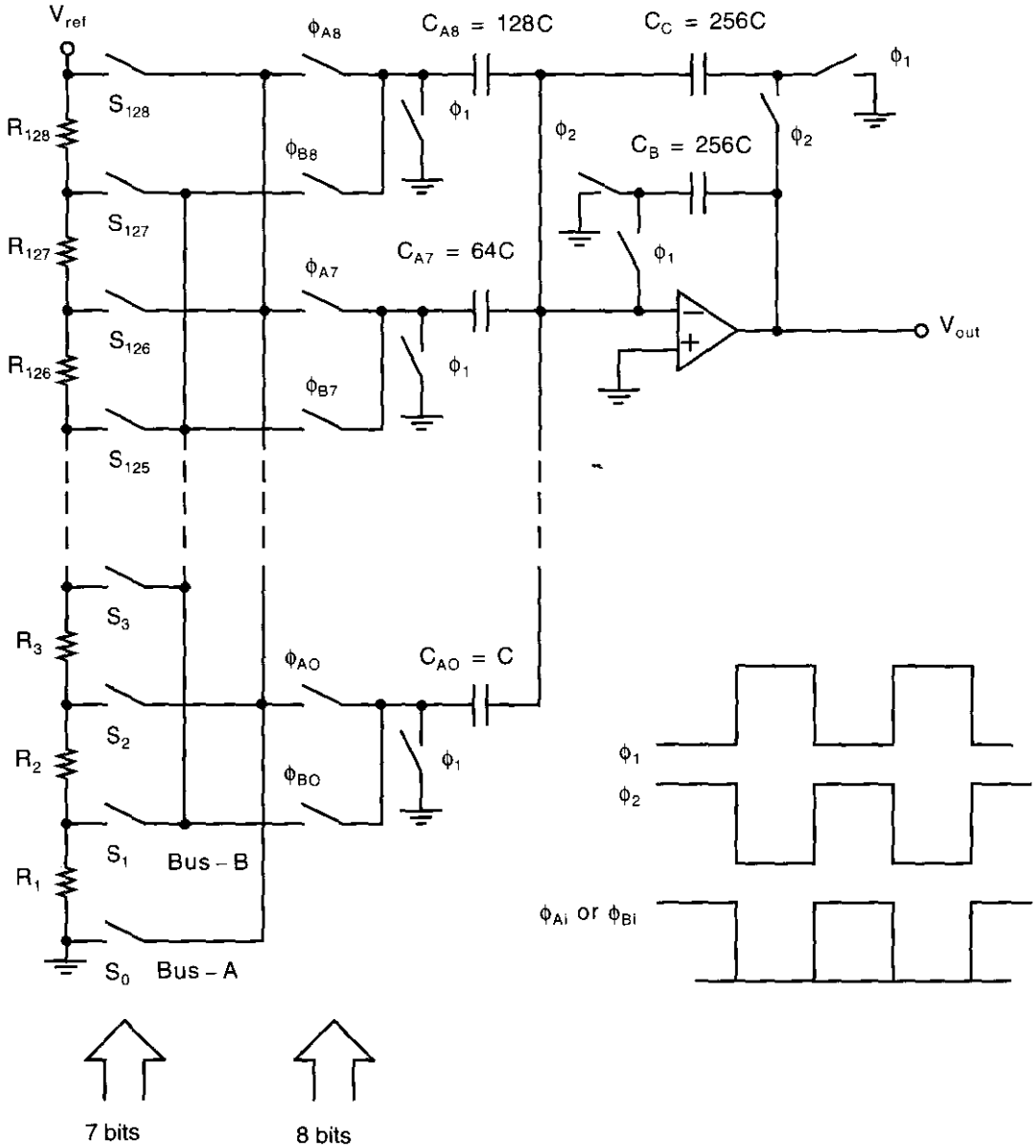


Fig. 12.21 One example of a 15-bit resistor-capacitor hybrid D/A converter.

the top 7 bits are 0000001, then switches S_1 and S_2 would be closed, while the other S_i switches would remain open. The capacitor array then performs an 8-bit interpolation between the pair of voltages by connecting the capacitors associated with a 1 to the higher voltage and the capacitors associated with a 0 to the lower voltage. This approach gives guaranteed monotonicity, assuming the capacitor array is accurate to only 8 bits. The converter in [Yang, 1989] has 15-bit monotonicity, without trimming, and 100-kHz sampling frequencies for a very-low-power 10-mW realization.

Segmented Converters

Segmented converters have probably become the most popular design approach for D/A converters [Schoeff, 1979; Grebene, 1984; Schouwenaars, 1988]. A 6-bit segmented D/A converter is shown in Fig. 12.22. In this approach, the two MSB currents are obtained in one segment from three equal current sources using thermometer coding. High bits are switched to the output, whereas low bits are switched to ground. As discussed in Section 12.3, the use of a thermometer code for the MSB currents greatly minimizes glitches. For the four LSBs, one additional current source from the MSB

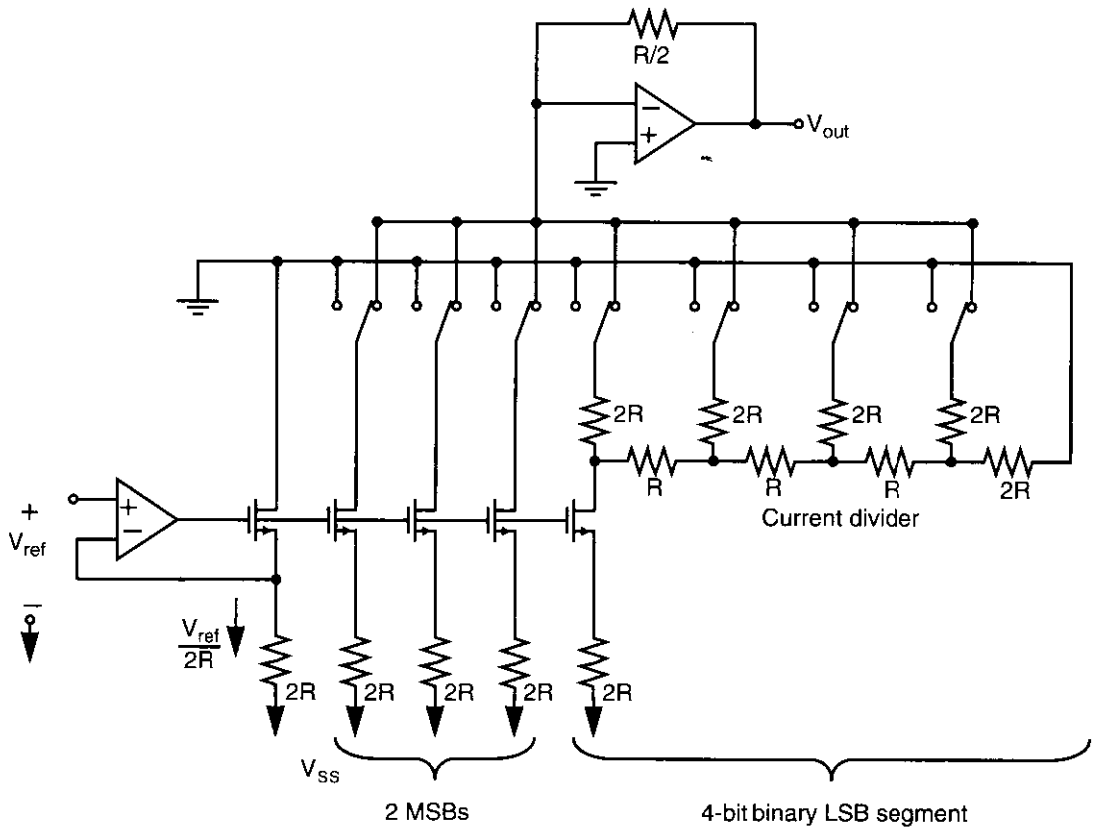


Fig. 12.22 A 6-bit segmented D/A converter.

segment is diverted where it is divided into binary-weighted currents, which are also switched to either ground or the output. Although this four-LSB segment is not guaranteed to be monotonic, its accuracy requirements are very relaxed, since it is used only for the LSBs.

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12.6 PROBLEMS

12.1 Derive an expression for the number of switches in a general N-bit resistor-string D/A converter similar to that shown in Fig. 12.1.

12.2 Assume that an 8-bit resistor-string D/A converter with digital decoding (see Fig. 12.3) has a total resistor-string resistance of 400 Ω, that its pass transistors have an on resistance of 400 Ω, and that the drain-source capacitances to

ground of its pass transistors are 0.1 pF. Ignoring all other effects and using the open-circuit time-constant approach, estimate the worst-case settling time to 0.1 percent.

12.3 Derive an expression for the number of switches in an N-bit folded resistor-string D/A converter similar to that shown in Fig. 12.4 (Assume N is even).

12.4 Assume that the first resistor string of a 10-bit multiple-R-string D/A converter must match to 0.1 percent whereas the second string must match to 1.6 percent since the converters realize the top 4 bits and lower 6 bits, respectively. For $V_{ref} = 5$ V, how much offsets in the opamps can be tolerated?

12.5 For a binary-weighted 10-bit resistor D/A converter (see Fig. 12.7), assume that R_F is chosen such that the output goes from 0 to $V_{ref} - V_{LSB}$. What is the resistor ratio between the largest and smallest resistors? What is the ratio between the currents through the switches for b_1 and b_{10}?

12.6 It is desired to realize a binary-weighted 4-bit resistor D/A converter, as shown in Fig. 12.7, that must be linear to 10 bits. Ignoring all other nonidealities except for resistance mismatch error, what percentage matching accuracy is required for each of the $b_2 - b_4$ resistors relative to the b_1 resistor?

12.7 Consider an 8-bit D/A converter built using binary-weighted capacitors, where capacitor tolerances are ±0.5 percent. What would be the worst-case differential nonlinearity in units of LSBs, and at what transition does it occur?

12.8 Consider the reduced-resistance-ratio approach shown in Fig. 12.8, where a single series resistor is applied to an N-bit converter, and where N is an even number. What is the improvement in the resistance ratio compared to using all binary-scaled resistances?

12.9 Draw the circuit for a reduced-resistance-ratio 8-bit D/A converter (see Fig. 12.8), where a resistor is inserted between b_4 and b_5. Ignoring R_F, what is the resistance spread? Now draw a similar circuit, but add resistors between b_2 and b_3 as well as between b_6 and b_7. What is this circuit's resistance spread?

12.10 Assuming all the switches in Fig. P12.10 are MOSFETS and are scaled so that each has 100 mV across the drain source when on (including s_4, which always remains on), show that no accuracy is lost.

12.11 For the 4-bit R-2R-ladder D/A converter shown in Fig. P12.10, what is the output error (in LSBs) when $R_A = 2.01R_B$? What is the output error when $R_C = 2.01R$?

12.12 Show that the D/A converter circuit shown in Fig. 12.11 operates correctly. Estimate the speed of this circuit if the opamp has infinite bandwidth, $R = 10$ kΩ, and all nodes have a capacitance of 0.5 pF to ground.

12.13 Consider the D/A converter shown in Fig. 12.11, where $I = 1$ mA, $R_f = 2$ kΩ and $R = 10$ kΩ. If this converter is perfectly linear but is found to have an offset error of 0.15LSB and a gain error of 0.2LSB, find the output levels for the inputs $b_1b_2b_3b_4$ equal to 0000, 1000, and 1111.

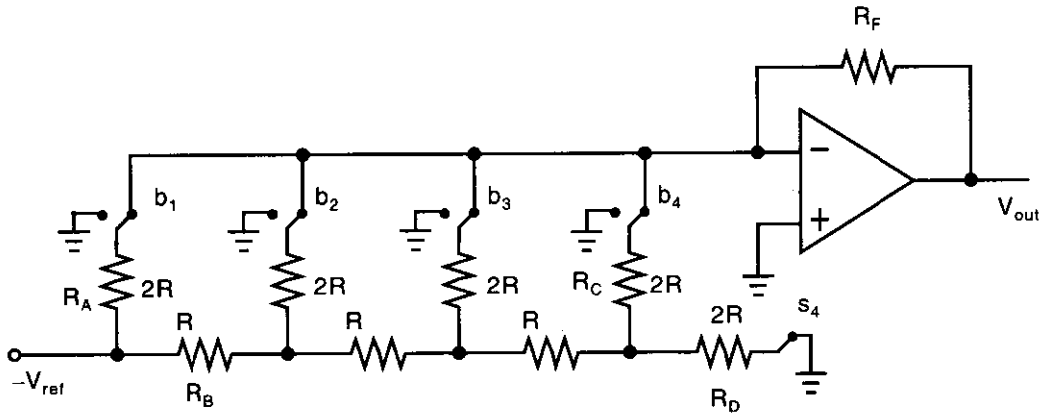


Fig. P12.10

12.14 A 12-bit binary-weighted D/A converter produces a glitch voltage of 0.5 V when the MSB is changed. What is the glitch voltage reduced to if a thermometer-code approach is used for the top 4 bits, whereas binary-weighting is used for the remaining 8 bits?

12.15 For the circuit in Fig. 12.17, sketch a typical waveform that would occur on the node connecting Q_1, Q_2, and Q_3 when the code signals, d_i and $\bar{d}_i$, are nonoverlapping. Repeat this sketch if the code signals are overlapping. Assume the code signals have logic swings from 0 to –5 V and that the threshold voltage for the transistors equals 1 V.

12.16 For the circuit in Fig. 12.18, sketch a typical waveform that would occur on the node connecting Q_1, Q_2, and Q_3 when the code signal, d_i, goes low-to-high and high-to-low. Assume here that the code signal has a logic swing of 0 to 5 V, that the threshold voltage for the transistors equals –1 V, and that V_{bias} is 1 V.

12.17 A D/A converter is realized using dynamically matched current sources, as shown in Fig. 12.20. Assuming all the transistors are ideal, find W/L for the Q_1 needed to set $V_{GS} = 3$ V when $I_{ref} = 50\ \mu A$, $V_t = 1$ V, and $\mu_n C_{ox} = 92\ \mu A/V^2$. If switch S_1 causes a random charge injection voltage of 1 mV, what is the expected percentage of random variation of the current being held on Q_1?

12.18 Repeat Problem 12.17 if the design does not incorporate the $0.9I_{ref}$ extra current source (i.e., if Q_1 must be the source for all of I_{ref}).

CHAPTER

13 Nyquist-Rate A/D Converters

Architectures for realizing analog-to-digital converters (ADC) can be roughly divided into three categories (Table 13.1)—low-to-medium speed, medium speed, and high speed. In this chapter, design details are discussed for these different approaches except for oversampling converters. Oversampling converters are best described using many signal processing concepts and are therefore discussed separately in Chapter 14.

Before proceeding, it should be noted that when discussing the design of A/D converters, we usually ignore the 0.5 LSB offset present in the A/D transfer characteristic. Such a simplification is made so as not to complicate the concepts presented.

13.1 INTEGRATING CONVERTERS

Integrating A/D converters is a popular approach for realizing high-accuracy data conversion on very slow-moving signals. These types of converters have very low offset and gain errors in addition to being highly linear. A further advantage of integrating converters is the small amount of circuitry required in their implementation. One application that has traditionally made use of integrating converters is measurement instruments such as voltage or current meters.

A simplified diagram for a *dual-slope* integrating converter is shown in Fig. 13.1. Dual-slope refers to this converter performing its conversion in two phases, (I) and (II), in the following manner (Fig. 13.2):

Phase (I) Phase (I) is a fixed time interval of length T_1 determined by running the counter for 2^N clock cycles. Thus, we have

$$T_1 = 2^N T_{clk} \tag{13.1}$$

Table 13.1 Different A/D converter architectures

Low-to-Medium Speed, High Accuracy	Medium Speed, Medium Accuracy	High Speed, Low-to-Medium Accuracy
Integrating	Successive approximation	Flash
Oversampling	Algorithmic	Two-step
		Interpolating
		Folding
		Pipelined
		Time-interleaved

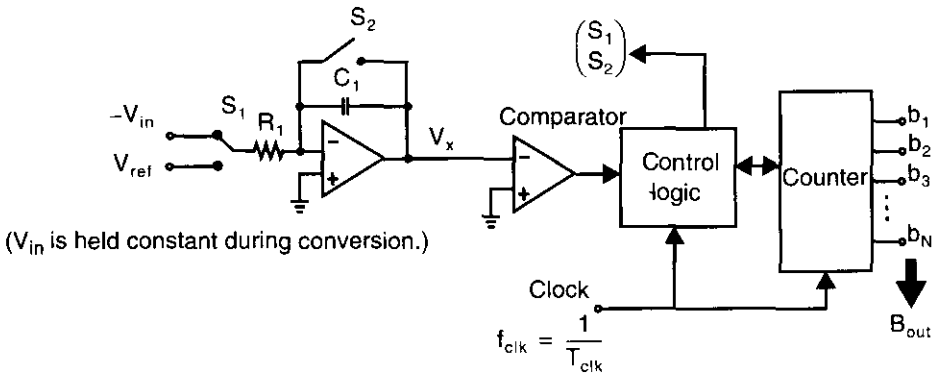


Fig. 13.1 Integrating (dual slope) A/D converter.

where T_{clk} is the period for one clock cycle. During this interval, switch S_1 is connected to $-V_{in}$ such that V_x ramps up proportional to the magnitude of V_{in}. Assuming V_x is initially equal to zero (due to a pulse on S_2), we have the following relationship for V_x:

$$V_x(t) = -\int_0^t \frac{(-V_{in})}{R_1C_1}\,d\tau = \frac{V_{in}}{R_1C_1}t \tag{13.2}$$

Thus, at the end of phase (I), the value of V_x is equal to $V_{in}T_1/R_1C_1$.

Phase (II) Phase (II) occurs for a variable amount of time, T_2, as shown in Fig. 13.2 for three different input voltages. At the beginning of this phase, the counter is reset and switch S_1 is connected to V_{ref}, resulting in a constant slope for the decaying voltage at V_x. To obtain the digital output value, the counter simply counts until V_x is less than zero, at which point that count value equals the digitized value of the input

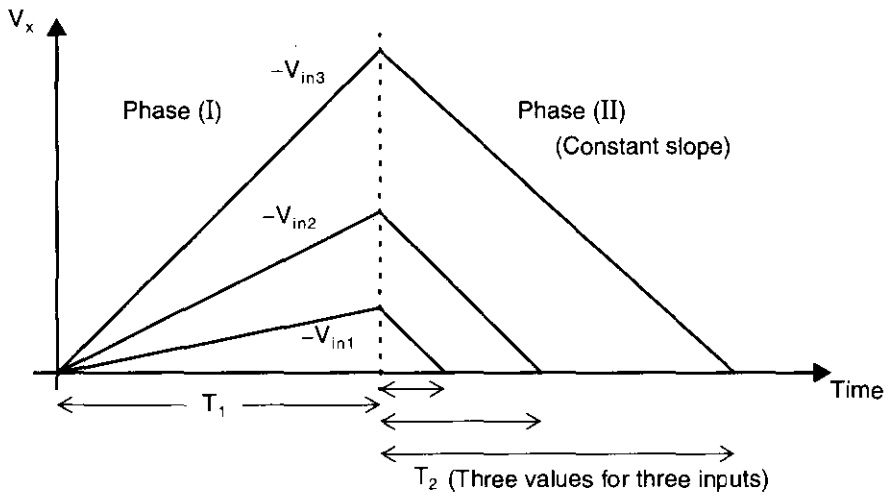


Fig. 13.2 Operation of the integrating converter for three different input voltages.

signal, V_{in}. Thus, assuming the digital output count is normalized so that the largest count is unity, the counter output, B_{out}, can be defined to be

$$B_{out} = b_1 2^{-1} + b_2 2^{-2} + \cdots + b_{N-1} 2^{-(N-1)} + b_N 2^{-N} \tag{13.3}$$

and we have

$$T_2 = 2^N B_{out} T_{clk} = (b_1 2^{N-1} + b_2 2^{N-2} + \cdots + b_{N-1} 2 + b_N) T_{clk} \tag{13.4}$$

To see why this count gives the correct value, we find the equation for V_x during phase (II) to be given by

$$\begin{aligned} V_x(t) &= -\int_{T_1}^{t} \frac{V_{ref}}{R_1 C_1} d\tau + V_x(T_1) \\ &= \frac{-V_{ref}}{R_1 C_1}(t - T_1) + \frac{V_{in} T_1}{R_1 C_1} \end{aligned} \tag{13.5}$$

Since V_x equals zero when $t = T_1 + T_2$, we can write

$$0 = \frac{-V_{ref} T_2}{R_1 C_1} + \frac{V_{in} T_1}{R_1 C_1} \tag{13.6}$$

and thus T_2 is related to T_1 by the following relationship:

$$T_2 = T_1 \left(\frac{V_{in}}{V_{ref}} \right) \tag{13.7}$$

Combining (13.7) with (13.1) and (13.4), we find

$$B_{out} = b_1 2^{-1} + b_2 2^{-2} + \cdots + b_{N-1} 2^{-(N-1)} + b_N 2^{-N} = \frac{V_{in}}{V_{ref}} \tag{13.8}$$

as expected.

From (13.8), we see that by going to a dual-slope conversion (i.e., two phases), the digital output does not depend on the time constant, $R_1 C_1$. In fact, the value of this time constant need only be stable during a single conversion for proper operation. However, R_1 and C_1 should be chosen such that a reasonable large peak value of V_x is obtained without clipping to reduce noise effects. If instead of dual-slope, a single-slope conversion was used, then a gain error would most likely occur, and this error would be a function of the time-constant value, $R_1 C_1$.

Although a dual-slope converter does not suffer from gain error, it can have an offset error due to opamp offset and other factors. Such an offset error can be calibrated out by going to a quad-slope conversion. In a quad-slope conversion, a dual-slope conversion is performed twice, once with the input connected to ground and then with the input connected to the signal to be converted. A subtraction of the two output words causes the offset error to be reduced to zero.

The conversion speed for these types of converters is quite slow. For example, in a dual-slope converter, the worst-case conversion speed occurs when V_{in} equals V_{ref}. In this case, the number of clock cycles to perform a conversion is 2^{N+1}. Thus

for a 16-bit converter with a clock frequency equal to 1 MHz, the worst-case conversion rate is around 7.6 Hz.

Finally, it should be mentioned that by a careful choice for T_1, certain frequency components superimposed on the input signal can be significantly attenuated. For example, if the input signal, V_{in}, is a dc level with power line noise of 60 Hz superimposed on it, choosing T_1 equal to an integer multiple of 16.67 ms filters out the power line noise. To see why this filtering effect occurs, we write V_{in} as

$$V_{in} = V_{in(ideal)} + V_{in(60\ Hz)} \tag{13.9}$$

where $V_{in(ideal)}$ is the desired dc level and $V_{in(60\ Hz)}$ is the interfering 60 Hz noise; or mathematically,

$$V_{in(60\ Hz)} = A \sin(120\pi t + \phi) \tag{13.10}$$

where A and ϕ are arbitrary magnitude and phase values. Now substituting this relationship for V_{in} into (13.2), we have

$$V_x(T_1) = -\int_0^{T_1} \frac{(-V_{in})}{R_1C_1}\,d\tau = -\int_0^{T_1} \frac{(-V_{in(ideal)})}{R_1C_1}\,d\tau - \int_0^{T_1} \frac{(-V_{in(60\ Hz)})}{R_1C_1}\,d\tau \tag{13.11}$$

However, the last term in (13.11) can be shown to equal zero when T_1 is an integer multiple of $1/(60\ Hz)$ (i.e., 16.67 ms). In this way, the peak value, $V_x(T_1)$, remains correct so that the conversion is performed without error. Note that for this same value of T_1, the harmonics of 60 Hz are also suppressed (i.e., 120 Hz, 180 Hz, 240 Hz, etc.). In fact, other frequencies are also attenuated but not fully suppressed as are the harmonics of 60 Hz. To quantify the filtering effect, we note that this converter effectively "integrates and dumps" the input signal. Such an integrating-then-reset behavior results in the impulse response of this converter being a square pulse of length T_1. Since the Fourier transform of a square pulse is a "sin(x)/x" type response, we have an effective input filter, as shown in Fig. 13.3. Here we have assumed that $T_1 = 1/(60\ Hz)$, resulting in a filter transfer function, $H(f)$, being given by

$$|H(f)| = \left|\frac{\sin(\pi f T_1)}{(\pi f T_1)}\right| \tag{13.12}$$

Note that higher frequencies are attenuated more and that full suppression is achieved at harmonics of 60 Hz, as expected.

EXAMPLE 13.1

It is desired to build a 16-bit two-slope integrating A/D such that a maximum input signal of $V_{in} = 3$ V results in the peak voltage of V_x being 4 V. In addition, input noise signals at 50 Hz and harmonics should be significantly attenuated. Find the required RC time constant and clock rate. Also, find the attenuation of a noise signal around 1 kHz superimposed on the input signal.

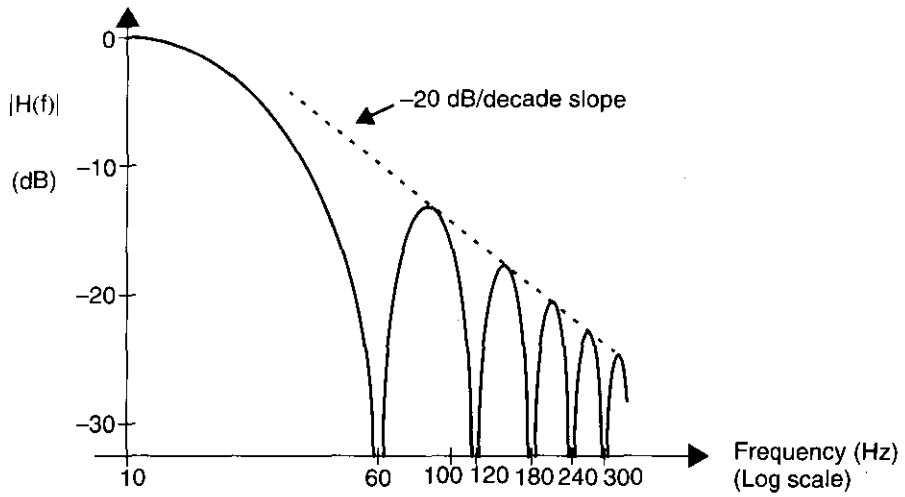


Fig. 13.3 Magnitude response of the effective input filter for an integrating-type converter with $T_1 = 1/(60\ \text{Hz})$.

Solution

Since 50 Hz and harmonics are to be rejected, we choose

$$T_1 = \frac{1}{50} = 20\ \text{ms} \tag{13.13}$$

Thus, for a 16-bit converter, we require a clock frequency of

$$f_{clk} = \frac{1}{T_{clk}} = \frac{2^{16}}{T_1} = 3.28\ \text{MHz} \tag{13.14}$$

To find the RC time constant needed, we note that at the end of phase (I), V_x is given by

$$V_x = \frac{V_{in}T_1}{R_1C_1} \tag{13.15}$$

and using the values of $V_x = 4$ V, $V_{in} = 3$ V, and $T_1 = 20$ ms results in

$$R_1C_1 = 15\ \text{ms} \tag{13.16}$$

Finally, the attenuation of a 1-kHz signal is infinite since it is a harmonic of 50 kHz. However, as seen in (13.12), attenuation is reduced halfway between harmonics, so we find the gain for an input signal at 975 Hz to be

$$|H(f)| = \left|\frac{\sin(\pi \times 975\ \text{Hz} \times 20\ \text{ms})}{\pi \times 975\ \text{Hz} \times 20\ \text{ms}}\right| = 16.3 \times 10^{-3} \tag{13.17}$$

which implies the attenuation is 36 dB.

13.2 SUCCESSIVE-APPROXIMATION CONVERTERS

Successive-approximation A/D converters are one of the most popular approaches for realizing A/D converters due to their reasonably quick conversion time, yet moderate circuit complexity. To understand the basic operation of successive-approximation converters, knowledge of the search algorithm referred to as a "binary search" is helpful. As an example of a binary search, consider the game of guessing a random number from 1 to 128 where one can ask only questions that have a "yes/no" response. The first question might be, "Is the number greater than 64?" If the answer is yes, then the second question asks whether the number is greater than 96. However, if the first answer is no, then the second question asks whether the number is greater than 32.

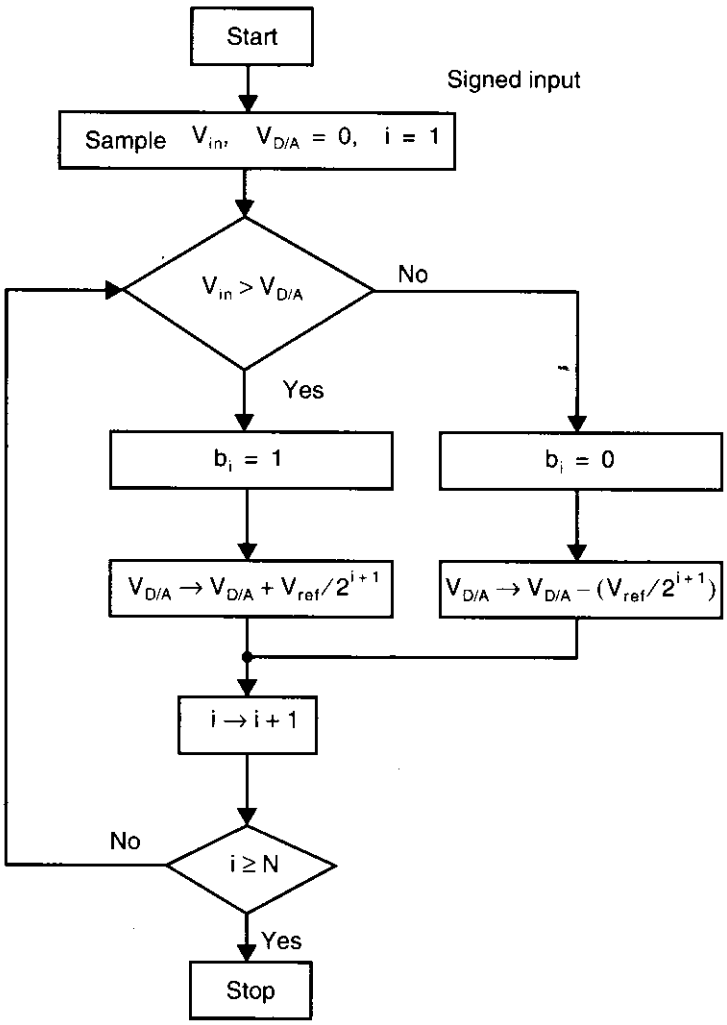


Fig. 13.4 Flow graph for the successive-approximation approach.

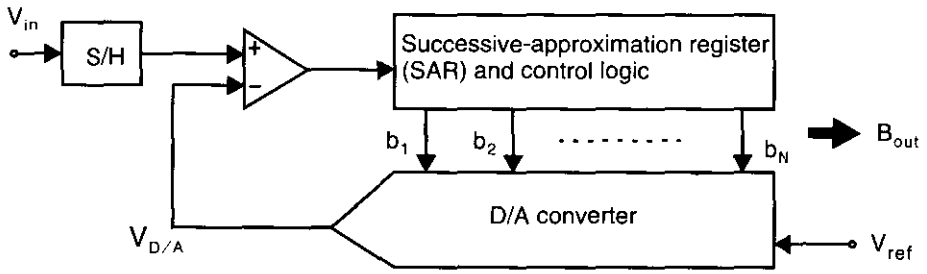


Fig. 13.5 D/A converter-based successive-approximation converter.

The third question divides the search space in two once again and the process is repeated until the random number is determined. In general, a binary search divides the search space in two each time, and the desired data can be found in N steps for a set of organized data of size 2^N.

Successive-approximation converters apply a binary search algorithm to determine the closest digital word to match an input signal. Specifically, in the first period, after possibly the reset period, the MSB, b_1, is determined. In the second period, the next bit, b_2, is determined, followed by b_3 and so on until all N bits are determined. Thus, in its most straightforward implementation, a successive-approximation converter requires N clock cycles to complete an N-bit conversion. A flow graph for a *signed* conversion using a successive-approximation approach is shown in Fig. 13.4. Here, the signed output is in offset-binary coding and the input signal is assumed to be within $\pm 0.5\ V_{ref}$. The flow graph for a *unipolar* conversion is only slightly different and is left as an exercise for the reader.

DAC-Based Successive Approximation

The block diagram for a unipolar successive-approximation A/D converter that uses a DAC is shown in Fig. 13.5. The successive-approximation register (SAR) and control logic are entirely digital and perform the necessary binary search. At the end of the conversion, the digital value in the SAR results in the voltage $V_{D/A}$ being within $0.5\ V_{LSB}$ of the input signal. With this type of architecture, the D/A converter typically determines the accuracy and speed of the A/D converter. Note that a sample and hold is required at the input so that the value to be converted does not change during the conversion time.

EXAMPLE 13.2

Consider the case where $V_{ref} = 8$ V, $V_{in} = 2.831$ V, and a 3-bit conversion is performed. Find intermediate D/A values and the final output.

Solution

In this case, $V_{LSB} = 1.0$ V.

In cycle 1: $B_{out} = 100$ so that $V_{D/A} = 4.0$ V. Since $V_{in} < V_{D/A}$, b_1 is set to 0.

In cycle 2: $B_{out} = 010$ so that $V_{D/A} = 2.0$ V. Since $V_{in} > V_{D/A}$, b_2 is set to 1.

In cycle 3: $B_{out} = 011$ so that $V_{D/A} = 3.0$ V. Since $V_{in} < V_{D/A}$, b_3 is set to 0.

Therefore, the resulting output is the last value of B_{out}, which is 010. Although the final quantization error is 0.831 V_{LSB}, it is greater than ± 0.5 V_{LSB} because we have not accounted for the 0.5 LSB offset as discussed at the beginning of this chapter.

Unipolar Charge-Redistribution A/D

The straightforward approach of using a separate D/A converter and setting it equal to the input voltage (within one LSB) can be modified to the flow graph shown in Fig. 13.6. Here, the error signal V equals the difference between the input signal, V_{in}, and the D/A output, $V_{D/A}$. As a result, V is always compared to ground, as seen at the top of the flow graph, and the goal is to set this error difference with one LSB of zero.

One of the first switched-capacitor analog systems using this approach is a charge-redistribution MOS A/D converter [McCreary, 1975]. With such a converter, the sample and hold, D/A converter, and the difference portion of the comparator are all combined into a single circuit. The unipolar case is shown in Fig. 13.7 and operates as follows:

1. *Sample mode:* In the first step, all the capacitors are charged to V_{in} while the comparator is being reset to its threshold voltage through s_2, In this step, note that the capacitor array is performing the sample-and-hold operation.
2. *Hold mode:* Next, the comparator is taken out of reset by opening s_2, and then all the capacitors are switched to ground. This causes V_x, which was originally zero, to change to $-V_{in}$, thereby holding the input signal, V_{in}, on the capacitor array. (This step is sometimes merged with the first bit time during bit cycling). Finally, s_1 is switched so that V_{ref} can be applied to the capacitor array during bit cycling.
3. *Bit cycling:* Next, the largest capacitor (i.e., the $16C$ capacitor in this example) is switched to V_{ref}. V_x now goes to $(-V_{in} + V_{ref}/2)$. If V_x is negative, then V_{in} is greater than $V_{ref}/2$, and the MSB capacitor is left connected to V_{ref}. Also b_1 is considered to be a 1. Otherwise, the MSB capacitor is reconnected to ground and b_1 is taken to be 0. This process is repeated N times, with a smaller capacitor being switched each time, until the conversion is finished.

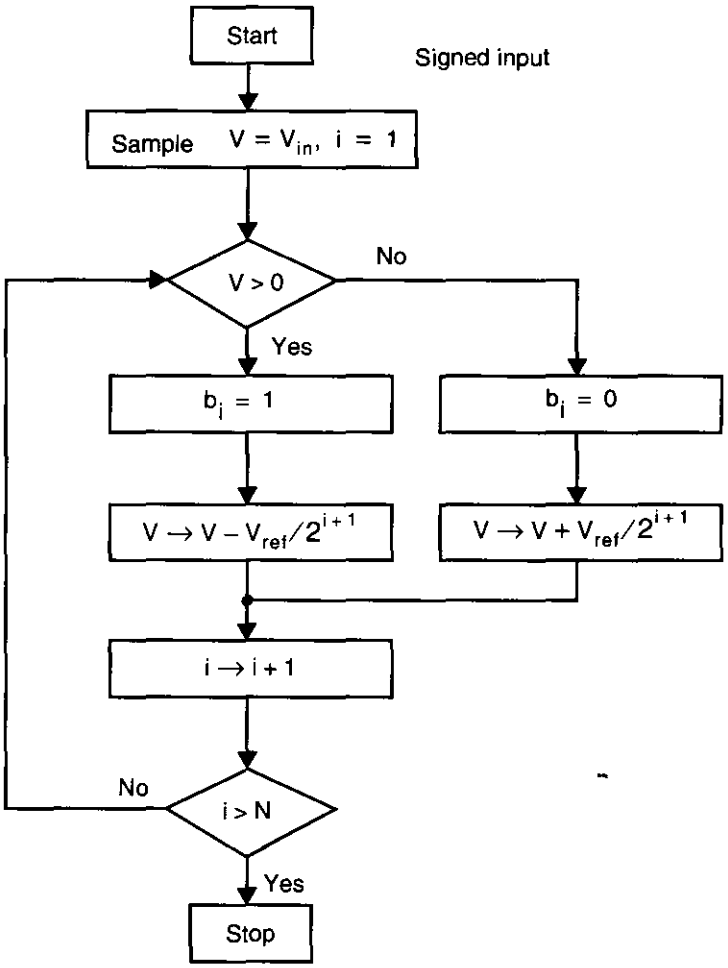


Fig. 13.6 Flow graph for a modified successive approximation (divided remainder).

To get an exact division by two, note that an additional unit capacitor of size C has been added so that the total capacitance is $2^N C$ rather than $(2^N - 1)C$. Also, the capacitor *bottom plates* should be connected to the V_{ref} side, not to the comparator side, to minimize the parasitic capacitance at node V_x. Although parasitic capacitance at V_x does not cause any conversion errors with an ideal comparator, it does attenuate the voltage V_x.

A signed A/D conversion can be realized by adding a $-V_{ref}$ input. If V_x is less than zero at the first step, then proceed as in the unipolar case using V_{ref}. Otherwise, if V_x is greater than zero, use $-V_{ref}$ and test for V_x greater than zero when deciding whether to leave the capacitors connected to $-V_{ref}$ or not at each bit cycling.

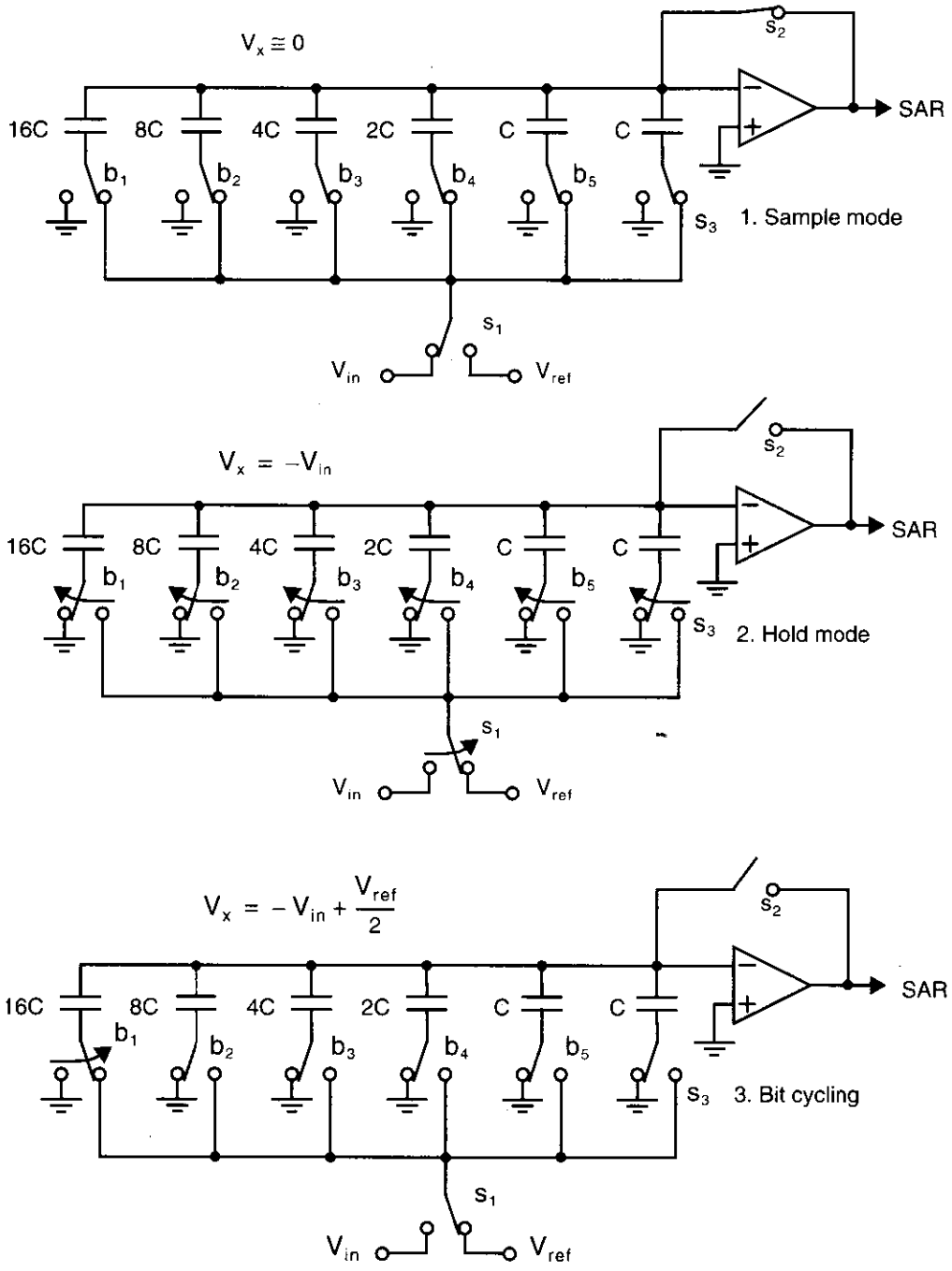


Fig. 13.7 A 5-bit unipolar charge-redistribution A/D converter.

EXAMPLE 13.3

Find intermediate node voltages at V_x during the operation of the 5-bit charge-redistribution converter shown in Fig. 13.7 when $V_{in} = 1.23$ V and $V_{ref} = 5$ V. Assume a parasitic capacitance of $8C$ exists on the node at V_x.

Solution

First, $V_x = 0$ during sample mode. Next, during hold mode, all capacitors are switched and the charge on V_x is shared between the $32C$ total converter capacitance and the parasitic $8C$ capacitance, resulting in

$$V_x = \frac{32}{32+8} \times -V_{in} = -0.984 \text{ V} \tag{13.18}$$

During the first bit cycling, b_1 is switched, resulting in

$$V_x = -0.984 + \frac{16}{40} \times 5 \text{ V} = 1.016 \text{ V} \tag{13.19}$$

Since this result is greater than zero, switch b_1 is reversed back to ground and V_x returns to -0.984 V. Thus, $b_1 = 0$.

Next, b_2 is switched, and we have

$$V_x = -0.984 + \frac{8}{40} \times 5 \text{ V} = 0.016 \text{ V} \tag{13.20}$$

It is also greater than zero, so $b_2 = 0$, and V_x is set back to -0.984 V by switching b_2 back to ground.

When b_3 is next switched, we have

$$V_x = -0.984 + \frac{4}{40} \times 5 = -0.484 \text{ V} \tag{13.21}$$

Since this result is less than zero, $b_3 = 1$, and switch b_3 is left connected to V_{ref}.

Next, b_4 is switched, resulting in

$$V_x = -0.484 + \frac{2}{40} \times 5 = -0.234 \text{ V} \tag{13.22}$$

which is also less than zero, so $b_4 = 1$, and this switch is left connected to V_{ref}.

Finally, b_5 is switched, resulting in

$$V_x = -0.234 + \frac{1}{40} \times 5 = -0.109 \text{ V} \tag{13.23}$$

which is also less than zero, so $b_5 = 1$.

Therefore, the output is given by $B_{out} = 00111$ and voltage V_x is within a V_{LSB} of ground ($V_{LSB} = 5/32$ V).

Signed Charge-Redistribution A/D with a Single Reference Voltage

The same structure as the unipolar case can be used to realize a signed A/D conversion while using only a single V_{ref} if a slightly modified switching arrangement is used. Referring to Fig. 13.8, and assuming V_{in} is between $\pm V_{ref}/2$, the conversion proceeds as follows:

1. *Sample mode:* In the first step, all the capacitors, except for the largest capacitor, are charged to V_{in} while the comparator is being reset to its threshold voltage. For the signed case, the largest capacitor is now connected to $V_{ref}/2$.
2. *Hold mode:* Next, the comparator is first taken out of reset, and then all the capacitors, except the largest one, are switched to ground. This causes V_x, which was originally zero, to change to $-V_{in}/2$. At the end of this step, the sign of the input signal is determined by looking at the comparator output.
3. *Bit cycling:* Next, the largest capacitor (i.e., the 16C capacitor in this example) is switched to ground *if, and only if,* V_x is larger than zero (i.e., when V_{in} is less than zero). Specifically, if V_x is less than zero, then V_{in} is positive and b_1 is set to 1, and conversion proceeds as in the unipolar case, starting with b_2, until conversion is completed. However, if V_x is larger than zero, b_1 is set to 0, the largest capacitor is switched to ground, causing V_x to become $-V_{in}/2 - V_{ref}/4$ (which is a negative value), and conversion proceeds as in the unipolar case, starting with b_2. Once conversion is completed, some digital recoding may be required to obtain the desired output code.

This approach for realizing signed A/Ds has the disadvantage that V_{in} has been attenuated by a factor of two, which makes noise more of a problem for high-resolution A/Ds. Also, any error in the MSB capacitor now causes both an offset and a sign-dependent gain error. The latter causes integral nonlinearity errors.

Resistor-Capacitor Hybrid

A combination of the resistor-string and capacitor-array approaches in a hybrid A/D converter, similar to the hybrid D/A converter [Fotouhi, 1979], is shown in Fig. 13.9.

The first step is to charge all the capacitors to V_{in} while the comparator is being reset. Next, a successive-approximation conversion is performed to find the two adjacent resistor nodes that have voltages larger and smaller than V_{in}. One bus will be connected to one node while the other is connected to the other node. All of the capacitors are connected to the bus having the lower voltage. A successive approximation using the capacitor-array network is then done. Starting with the largest capacitor, a capacitor is switched to the adjacent resistor-string node having a larger voltage. If the comparator output is a 1, it is switched back and b_i is a 0. Otherwise, the switch is left as is and b_i is a 1. Since the resistor string is monotonic, this type of converter is guaranteed monotonic if the capacitor array is monotonic.

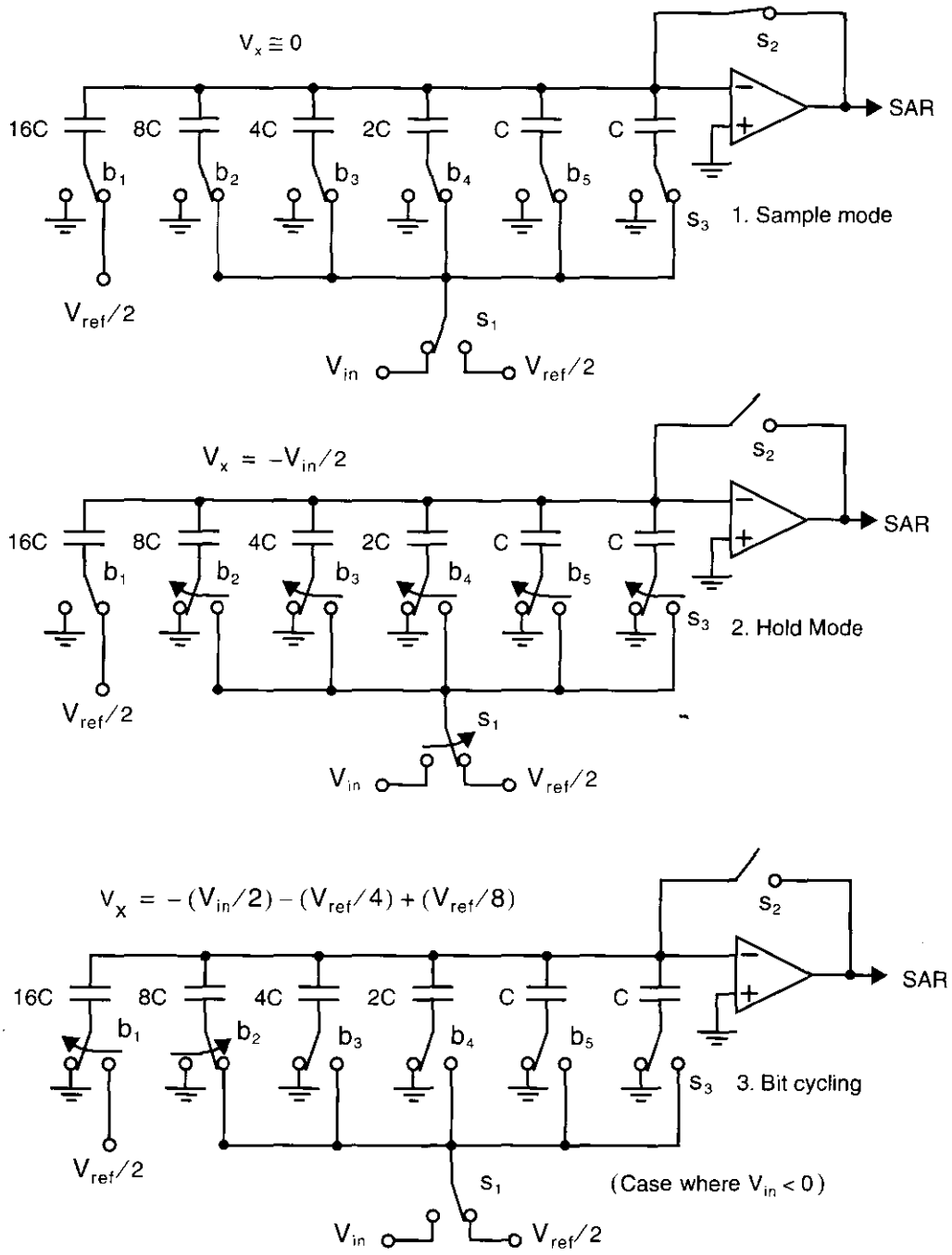


Fig. 13.8 A 5-bit signed charge-redistribution A/D converter.

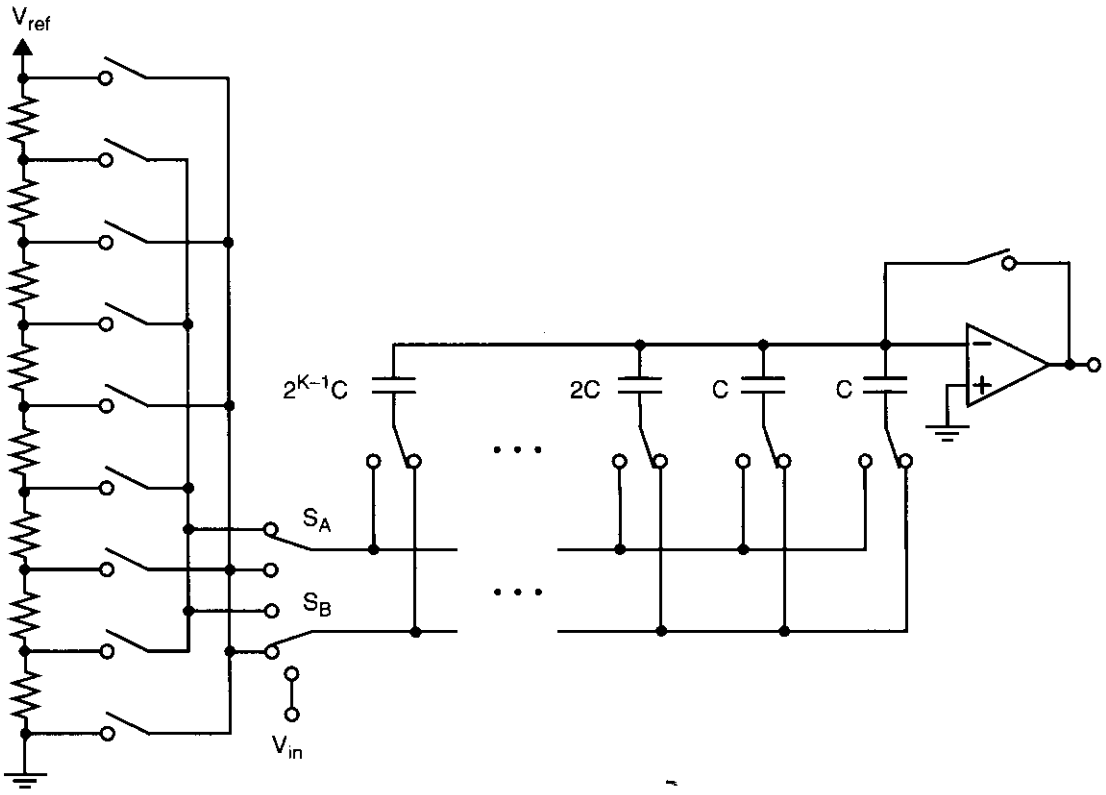


Fig. 13.9 Resistor-capacitor hybrid A/D converter.

Charge-Redistribution with Error Correction

With the best matching accuracy of on-chip elements being about 0.1 percent, one is limited to successive-approximation converters having 10-bit accuracy specifications without some sort of calibration. One error-correction technique that has been used to obtain 16-bit linear converters is shown in Fig. 13.10 [Lee, 1984]. In this approach, the MSB array is realized using binary-weighted capacitors that determine, for example, the first 10 bits. For a 16-bit converter, the final 6 bits are determined using an additional capacitor and a resistor string referred to as a *sub-dac.* Although this combination of an MSB capacitor array and an LSB resistor string is not inherently monotonic, it can be easily autocalibrated at start-up by adding a second resistor string referred to as a *cal-dac.*

Calibration is done by measuring the errors of each capacitor, starting with the largest capacitor, calculating the correction terms required, and then storing the correction terms in a data register as DV_{ej}. During a regular successive approximation operation, whenever a particular capacitor is used, its error is cancelled by adding the value stored in the data register to that stored in an accumulator register, which con-

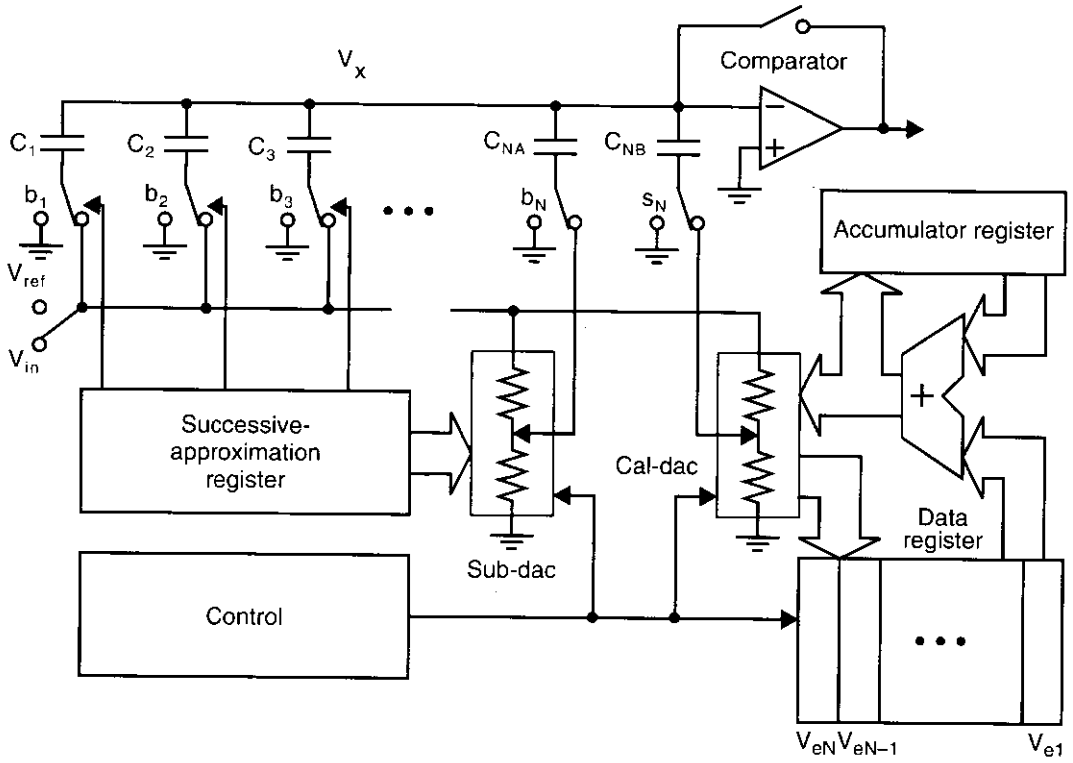


Fig. 13.10 A charge-redistribution A/D converter with error correction.

tains the sum of the correction terms for all of the other capacitors currently connected to V_{ref}. No correction terms are measured for the resistor sub-dac; its accuracy is not critical since it only determines the remaining LSBs.

The error terms are found starting with the MSB capacitor, C_1. It is connected to ground and all of the other capacitors are connected to V_{ref} while the comparator is reset. Next, the comparator is taken out of reset mode, all of the other capacitors are switched to ground, and C_1 is switched to V_{ref}. Defining C_{total} to be the sum of all the capacitors in the array, the ideal value of C_1 is $C_{total}/2$. However, in practice C_1 varies from its ideal value, and thus, C_1 can be written as

$$C_1 \equiv (C_{total}/2) + \Delta C_1 \tag{13.24}$$

where ΔC_1 is the capacitance error (either positive or negative). As a result, the simplified model shown in Fig. 13.11(*a*) occurs after the switches are reversed. Here, the remaining capacitance equals $(C_{total}/2) - \Delta C_1$ to make the total capacitance correct. With the above switch operation, V_x would remain zero if ΔC_1 equals zero. However, when ΔC_1 is not zero, the resulting voltage, V_x, is twice the error voltage, defined as V_{e1}, that would be introduced during a normal successive approximation when C_1 alone is switched to V_{ref}. A digital representation of V_{e1}, defined as DV_{e1}, is obtained by doing a successive approximation using the cal-dac shown in

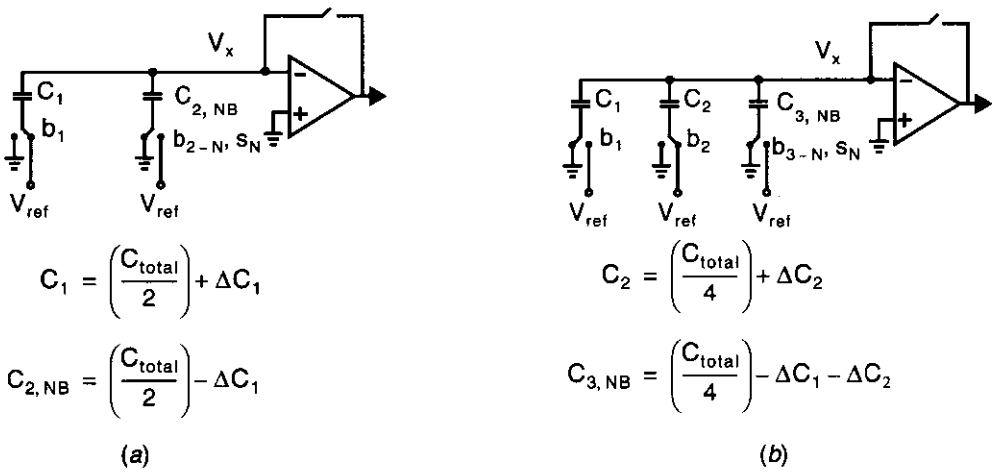


Fig. 13.11 Equivalent models for determining capacitance errors. (*a*) During calibration for C_1. (*b*) During calibration for C_2.

Fig. 13.10 and then dividing the resulting digital value by 2 to obtain DV_{e1}. This digital correction term, DV_{e1}, is stored in the data register for use during regular conversion.

To obtain the similar correction term for C_2, defined as DV_{e2}, the model in Fig. 13.11(*b*) is used. Here, the switch procedure is to always leave the b_1 switch grounded while the comparator is reset, the b_2 switch is grounded, and the remaining switches b_{3-N}, s_N are connected to V_{ref}. Next, the b_2 and b_{3-N}, s_N switches are all reversed (i.e., b_2 set to V_{ref} and the others grounded). Note, however, that even if ΔC_2 equals zero, the measured value of V_x will be equivalent to $-DV_{e1}$, since $-\Delta C_1$ is assumed to be part of $C_{3,NB}$. Therefore, the error voltage that would be due only to C_2 can be calculated by digitizing V_x, as before, but then subtracting off DV_{e1} using digital circuitry. Mathematically,

$$DV_{e2} = \frac{1}{2}(DV_{x2} - DV_{e1}) \tag{13.25}$$

A similar procedure is used for the other capacitors. Specifically, DV_{xi} is found by connecting all capacitors smaller than C_i to V_{ref}, and connecting C_i and all larger capacitors to ground while the comparator is reset. Next, the comparator is taken out of reset mode, all capacitors smaller than C_i are switched to ground, C_i is switched to V_{ref}, and all capacitors larger than C_i are left connected to ground. DV_{xi} is then found using the cal-dac and successive approximation. DV_{ei} is finally calculated using the formula

$$DV_{ei} = \frac{1}{2}\left(DV_{xi} - \sum_{j=1}^{i-1} DV_{ej}\right) \tag{13.26}$$

and stored in the ith word of the data register.

During a regular conversion, normal successive approximation is performed with the MSB capacitor array; however, appropriate correction voltages are either added or subtracted using the cal-dac and C_{NB} capacitor. The proper correction voltage is determined through the use of a digital accumulator that stores the sum of all digital errors of those MSB capacitors deemed to be a 1 (i.e., connected to V_{ref}). In other words, when the ith bit is being tested, DV_{ei} is added to the digital accumulator that is driving the cal-dac. If the ith bit is determined to be a 0, then the digital accumulator returns to its previous value; otherwise, it maintains its new accumulated value. Finally, normal successive approximation is performed using the sub-dac to determine the final LSBs. With this approach, a digital addition must be performed during each bit cycle, and a small amount of digital RAM is required (10 bytes in the case of a 10-bit MSB array).

Finally, it should be mentioned that similar error correction techniques have also been described to account for capacitor inaccuracies (for example, [Tan, 1990]).

Speed Estimate for Charge-Redistribution Converters

The major limitation on speed with charge redistribution converters is often due to the RC time constants of the capacitor array and switches. To estimate this time, consider the simplified model of a capacitor array being reset, as shown in Fig. 13.12. Here, R, R_{s1}, and R_{s2} represent the switch-on resistances of the bit line, s1 and s2 switches, respectively. Although this circuit is easily simulated using Spice to find its settling time, it is useful to have a rough estimate of the charging time to speed up the design process. As in Section 12.1, the open-circuit time constant approach [Sedra, 1991] can be used to obtain an estimate of the high-frequency time constant by summing individual time constants due to each capacitor. For example, the individual time constant due to the capacitance 2C equals $(R_{s1} + R + R_{s2})2C$. Following such

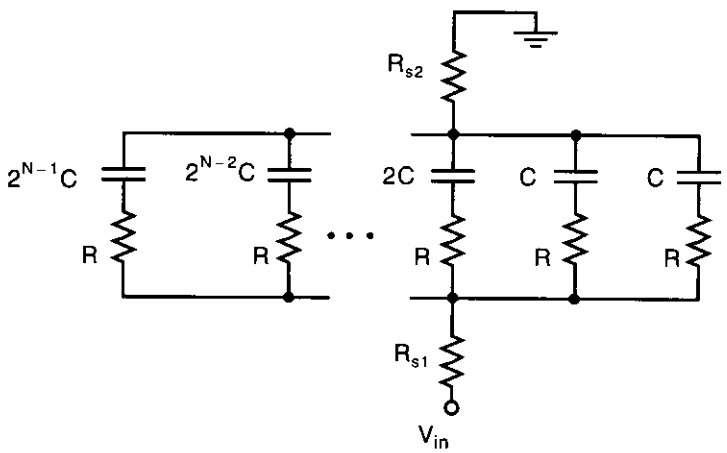


Fig. 13.12 Simplified model of a capacitor array during the sampling time.

an approach, the open-circuit time constant for the circuit shown in Fig. 13.12 is equal to

$$\tau_{eq} = (R_{s1} + R + R_{s2})2^N C \tag{13.27}$$

For better than 0.5-LSB accuracy, we need

$$e^{-T/\tau_{eq}} < \frac{1}{2^{N+1}} \tag{13.28}$$

where T is the charging time. This equation can be simplified to

$$T > \tau_{eq}(N+1)\ \ln(2) = 0.69(N+1)\tau_{eq} \tag{13.29}$$

It has been observed that (13.29) gives results about 30 percent higher than those obtained by simulating the actual RC network shown in Fig. 13.12. So while (13.29) can be used to roughly determine the maximum sampling rate, the final design should be simulated using accurate transistor models. Finally, although this result is not the same for all charge-redistribution A/D converters (for example, the size of the switches going to the larger capacitors may be increased to reduce their on resistance), the basic approach can be modified for most charge-redistribution A/D converters.

13.3 ALGORITHMIC (OR CYCLIC) A/D CONVERTER

An algorithmic converter operates in much the same way as a successive-approximation converter. However, whereas a successive-approximation converter halves the reference voltage in each cycle, an algorithmic converter doubles the error voltage while leaving the reference voltage unchanged. The flow graph for a signed algorithmic conversion is shown in Fig. 13.13.

Ratio-Independent Algorithmic Converter

The block diagram for an algorithmic converter is shown in Fig. 13.14 [McCharles, 1977; Li, 1984]. This converter requires a small amount of analog circuitry because it repeatedly uses the same circuitry to perform its conversion cyclically in time.

One of the difficulties in realizing a high-precision algorithmic converter is building an accurate multiply-by-two gain amp. Fortunately, it is possible to realize the gain amp so that it does not rely on any capacitor matching if four clock cycles are taken for the multiply-by-two operation. The operation of the multiply-by-two gain amp is shown in Fig. 13.15. Although this gain-amp circuitry is shown using single-ended circuits for simplicity, fully differential circuits are normally used.

The basic idea of this gain amp is to sample the input signal twice using the same capacitor. During the second sampling, the charge from the first capacitor is stored on a second capacitor whose size is unimportant. After the second sampling, both charges are recombined into the first capacitor which is then connected between the opamp input and output.

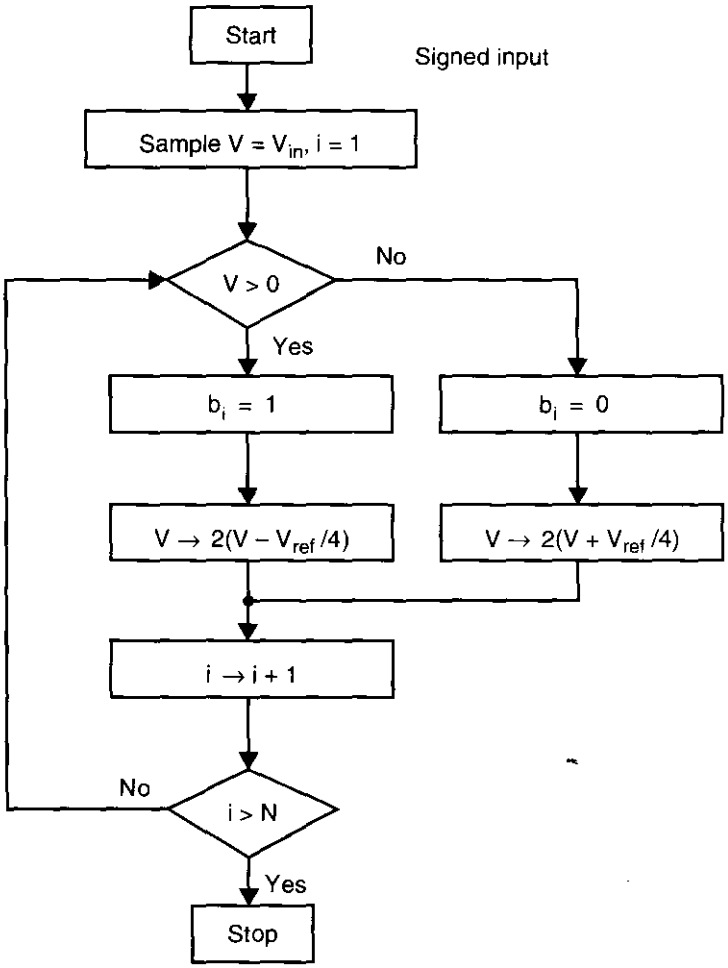


Fig. 13.13 Flow graph for the algorithmic approach.

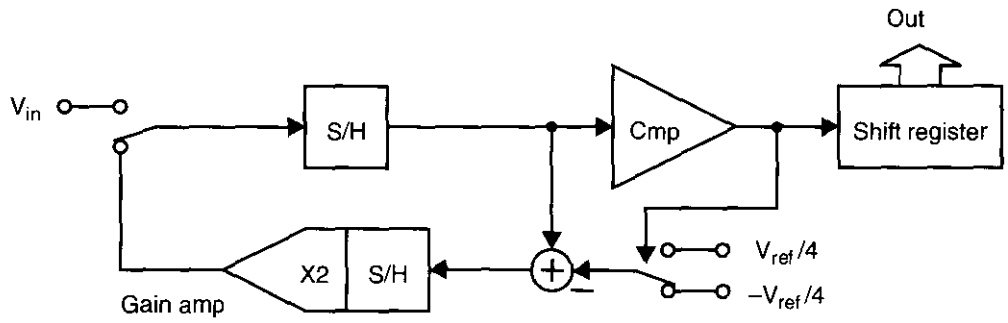
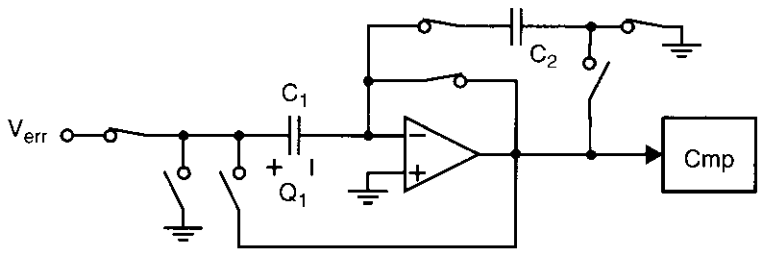
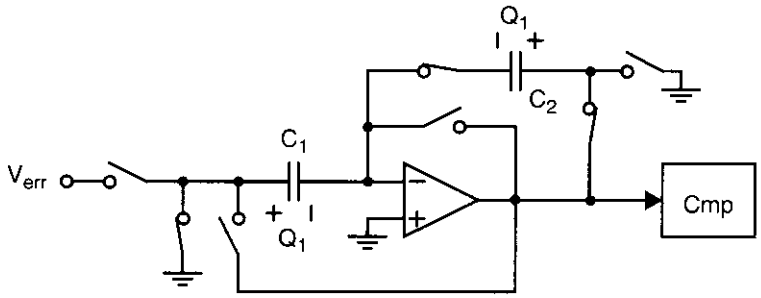


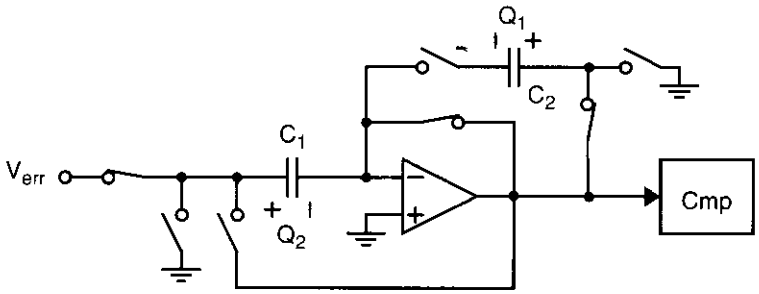
Fig. 13.14 Algorithmic converter.



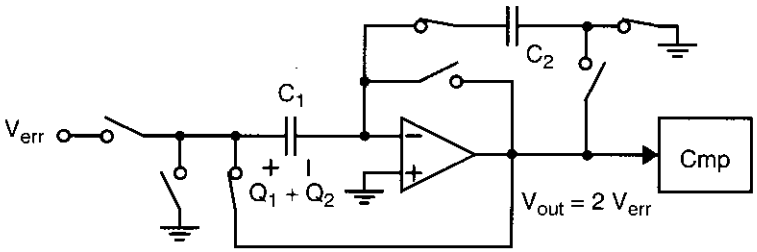
1. Sample remainder and cancel input-offset voltage.



2. Transfer charge Q_1 from C_1 to C_2.



3. Sample input signal with C_1 again, after storing charge Q_1 on C_2.



4. Combine Q_1 and Q_2 on C_1, and connect C_1 to output.

Fig. 13.15 Multiply-by-two gain circuitry for an algorithmic converter that does not depend on capacitor matching.

EXAMPLE 13.4

Consider the multiply-by-two gain circuitry shown in Fig. 13.15. Assuming the opamp has an input offset designated as V_{off}, find the values of V_{C1}, V_{C2}, and V_{out} at the end of each of the phases shown.

Solution

During phase one, the opamp output, V_{out}, is connected to the negative opamp input, resulting in

$$V_{out} = V_{off} \tag{13.30}$$

and the voltages across the two capacitors are

$$V_{C1} = V_{err} - V_{off} \tag{13.31}$$

$$V_{C2} = 0 - V_{off} = -V_{off} \tag{13.32}$$

At the end of phase two, we have

$$V_{C1} = 0 - V_{off} = -V_{off} \tag{13.33}$$

implying that its charge change was

$$\Delta Q_{C1} = C_1(V_{err} - V_{off} - (-V_{off})) = C_1 V_{err} \tag{13.34}$$

All this charge is placed on C_2, resulting in

$$V_{C2} = -V_{off} + \left(\frac{C_1}{C_2}\right)V_{err} \tag{13.35}$$

and $V_{out} = (C_1/C_2)V_{err}$.

At the end of phase three, V_{C2} remains unchanged since one side of it has been opened. Also, $V_{C1} = V_{err} - V_{off}$ and $V_{out} = V_{off}$ as in phase one.

Finally, at the end of phase four, C_2 is discharged to the same value it had in phase 1, resulting in $V_{C2} = -V_{off}$ and its change in charge being

$$\Delta Q_{C2} = C_2\left(\frac{C_1}{C_2}\right)V_{err} = C_1 V_{err} \tag{13.36}$$

All of this charge is placed back on C_1, resulting in

$$V_{C1} = 2\,V_{err} - V_{off} \tag{13.37}$$

and the output voltage being the desired result of $V_{out} = 2\,V_{err}$. Note that this final result is independent of the sizes of C_1, C_2, and the offset value, V_{off}.

13.4 FLASH (OR PARALLEL) CONVERTERS

Flash converters are the standard approach for realizing very-high-speed converters, as seen in some recent publications [Peetz, 1986; Yoshii, 1987; Hotta, 1987; and

Gendai, 1991]. The input signal in a flash converter is fed to 2^N comparators in parallel, as shown in Fig. 13.16. Each comparator is also connected to a different node of a resistor string. Any comparator connected to a resistor string node where V_{ri} is larger than V_{in} will have a 1 output while those connected to nodes with V_{ri} less than V_{in} will have 0 outputs. Such an output code word is commonly referred to as a thermometer code since it looks quite similar to the mercury bar in a thermometer. Note that the top and bottom resistors in the resistor string have been chosen to create the 0.5 LSB offset in an A/D converter.

The NAND gate that has a 0 input connected to its inverting input and a 1 input connected to its noninverting input detects the transition of the comparator outputs from 1s to 0s, and will have a 0 output. All other NAND-gate outputs will be 1, resulting in simpler encoding. It also allows for error detection by checking for more than one 0 output, which occurs during a bubble error (see the next subsection) and, perhaps, error correction.

Flash A/Ds are fast but they require a large number of comparators, which typically take up a large area and are very power hungry—especially when they are

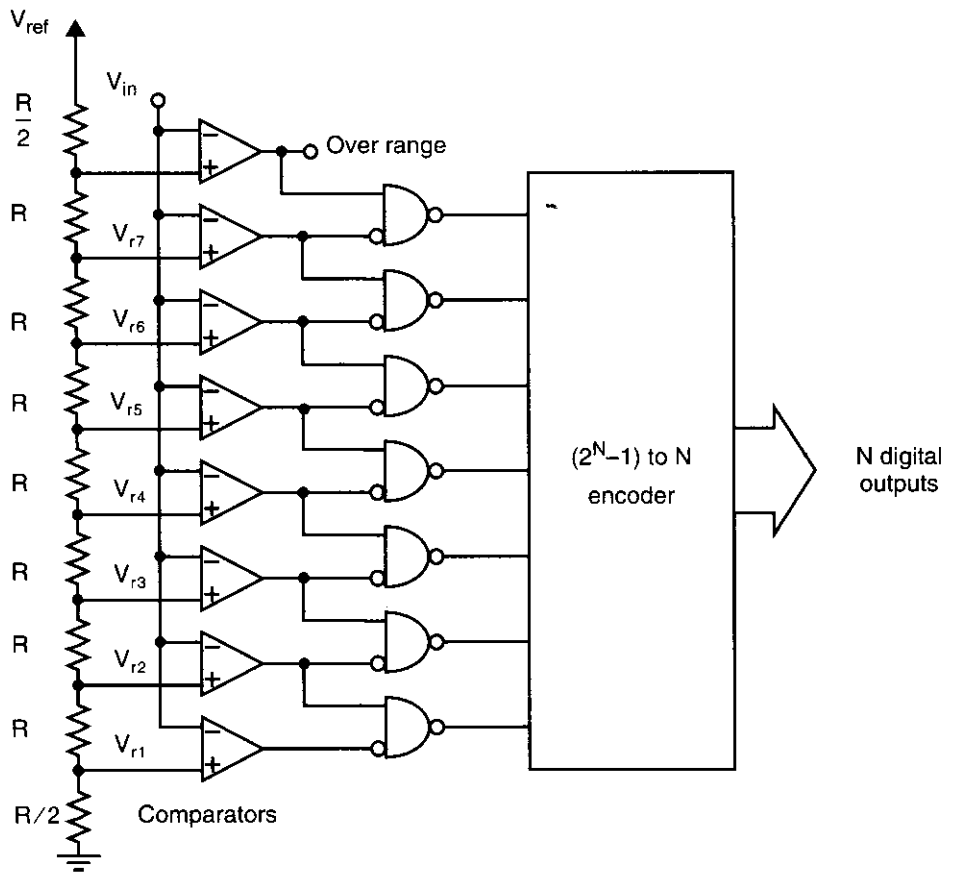


Fig. 13.16 A 3-bit flash A/D converter.

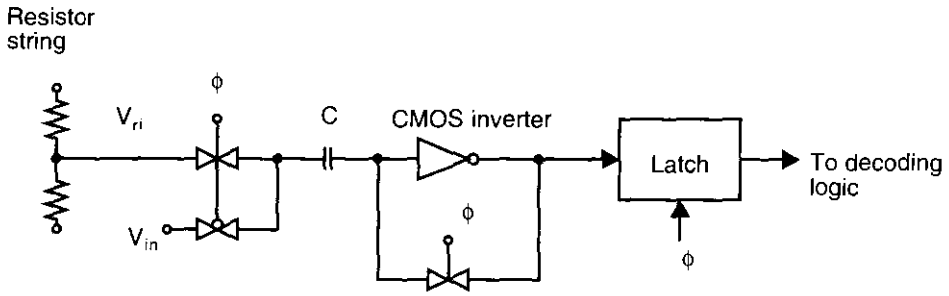


Fig. 13.17 A clocked CMOS comparator.

clocked fast. One way to realize a small clocked CMOS comparator is by using a CMOS inverter, as shown in Fig. 13.17 [Dingwall, 1979].

When ϕ is high, the inverter is set to its bistable operating point, where its input voltage equals its output voltage (i.e., its threshold voltage). Normally with an odd number of inverters, a ring oscillator is formed; however, in the case of a single CMOS inverter, the inverter operates as a single stage opamp with only one pole (no nondominant poles), so stability is guaranteed. With this inverter set to its threshold voltage, the other side of C is charged to V_{ri}. When ϕ goes low, the inverter is free to fall either high or low depending on its input voltage. At the same time, the other side of C is pulled to the input voltage, V_{in}. Since the inverter side of the capacitor is floating, C must keep its original charge, and therefore the inverter's input will change by the voltage difference between V_{ri} and V_{in}. Since the inverter's input was at its bistable point, the difference between V_{ri} and V_{in} will determine which direction the inverter's output will fall. However, it should be mentioned that this simple comparator suffers from poor power supply rejection, which is often a critical design specification in fast converters. Using fully differential inverters helps alleviate this shortcoming.

Issues in Designing Flash A/D Converters

We discuss here some important design issues that should be addressed when building high-speed flash A/D converters.

Input Capacitive Loading The large number of comparators connected to V_{in} results in a large parasitic load at the node V_{in}. Such a large capacitive load often limits the speed of the flash converter and usually requires a strong and power-hungry buffer to drive V_{in}. We shall see that this large capacitive loading can be reduced by going to an interpolating architecture.

Resistor-String Bowing The input currents of bipolar comparators cause errors in the voltages of the nodes of the resistor string. These errors usually necessitate the bias current in the resistor string being two orders of magnitude greater than the input

currents of the comparators. However, these errors are greatest at the center node of the resistor string and thus considerable improvement can be obtained by using additional circuitry to force the center tap voltage to be correct.

Comparator Latch-to-Track Delay Another consideration that is often overlooked is the time it takes a comparator latch to come from latch mode to track mode when a small input signal of the opposite polarity from the previous period is present. This time can be minimized by keeping the time constants of the internal nodes of the latch as small as possible. This is sometimes achieved by keeping the gain of the latches small, perhaps only two to four. In some cases, the differential internal nodes might be shorted together temporarily just after latch time.

Signal and/or Clock Delay Even very small differences in the arrival of clock or input signals at the different comparators can cause errors. To see this, consider a 250-MHz, 1-V peak-input sinusoid. This signal has a maximum slope of 1570 V/μs at the zero crossing. If this signal is being encoded by an 8-bit A/D converter with $V_{ref} = 2$ V (i.e., the sinusoid covers the whole range), then it would only take 5 ps to change through 1 LSB. This time is roughly about the same time it takes a signal to propagate 500 μm in metal interconnect. If there is clock skew between comparators greater than this, the converter will have more than 1 LSB error. One means of easing this problem is to precede the converter by a sample-and-hold circuit. However, high-speed sample-and-hold circuits can be more difficult to realize than the flash converter itself. In addition, the clock and V_{in} should be routed together with the delays matched [Gendai, 1991]. It should also be noted that the delay differences may not be caused just by routing differences, but could also be caused by different capacitive loads, or by phase differences between the comparator preamplifiers at high frequencies.

Substrate and Power-Supply Noise For $V_{ref} = 2$ V and an 8-bit converter, only 7.8 mV of noise injection would cause a 1 LSB error. Typically, on an integrated circuit having a clock signal in the tens of MHz, it is difficult to keep power-supply noise below a few tenths of a volt. This power-supply noise can easily couple through the circuitry or substrate, resulting in errors. To minimize this problem, the clocks must be shielded from the substrate and from analog circuitry. Also, running differential clocks closely together will help prevent the signals being coupled into the substrate or through the air. Also, analog power supplies should be separated from digital power supplies including having analog power to the comparator preamps while using digital power to the latch stages. On-chip power-supply bypassing is a necessity. It is also necessary to make sure the power-supply bypassing circuitry doesn't form a resonant circuit with the bonding wires—include small resistors in series with the bypass capacitors.

Bubble Error Removal The outputs of the comparators should be a thermometer code with a single transition. However, sometimes a lone 1 will occur within the string of 0s (or a 0 within the string of 1s) due to comparator metastability, noise,

cross talk, limited bandwidth, etc. These bubbles usually occur near the transition point of the thermometer code. Fortunately, these bubbles can usually be removed with little extra complexity by replacing the two-input NAND gates shown in Fig. 13.16 with three-input NAND gates, as shown as shown in Fig. 13.18 [Steyaert, 1993]. With this modification, there must now be two 1s immediately above a 0 in determining the transition point in the thermometer code. However, this circuit will not eliminate the problem of a stray 0 being two places away from the transition point, which may cause a large decoding error. Another digital approach for reducing the effect of bubble errors is to allow bubble errors in the lower 2 LSBs but have the remaining MSBs determined by looking for transitions between every *fourth* comparator [Gendai, 1991]. With this approach, bubble errors that occur within four places of the transition point do not cause any large errors. An alternate approach to reduce the effect of distant bubble errors is to create two encoders (one AND type and one OR type) rather than a single encoder [Ito, 1994]. When an unexpected output pattern occurs at the NAND outputs, the errors in two different encoders tend to be equal in magnitude but opposite in sign. Thus, the final output is taken as the average of the two encoder outputs, which is performed by adding the two outputs and dropping the LSB (to divide by two).

An alternate method to remove bubble errors that does not increase the power dissipation is shown in Fig. 13.19. Here, extra transistors have been added to the inputs of the slave latches, which are driven by the comparator master latches [van Valburg, 1992]. These extra transistors make the value stored in a slave latch not just a function of its master latch, but also a function of the two adjacent master latches. If a bubble occurs, the outputs from the two adjacent master latches are the same, but different from the center master latch. In this case, the values from the adjacent master latches overrule the center master latch. Note that with this approach, the power dissipation is not increased because the added transistors make use of existing current in the slave latch. Alternatively, this same voting scheme can be implemented entirely in digital form.

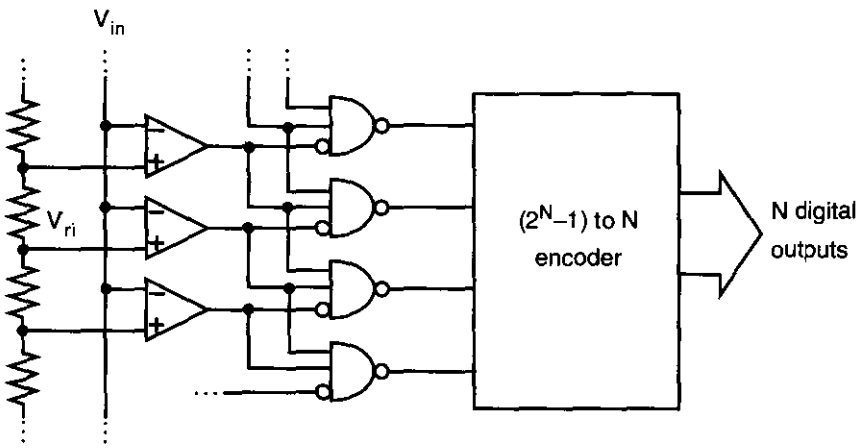


Fig. 13.18 Using three-input NAND gates to remove single bubble errors.

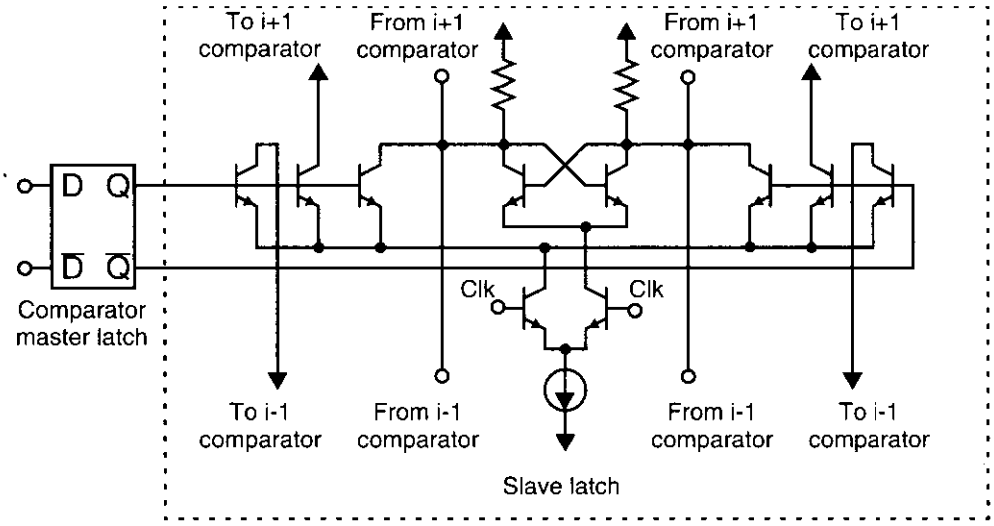


Fig. 13.19 Bubble-error voting circuit that does not increase the power dissipation.

Flashback An additional source of error is flashback. Flashback is caused by latched comparators, which are almost always used. When clocked comparators are switched from track to latch mode, or vice-versa, there is major charge glitch at the inputs to the latch. If there is no preamplifier, this will cause major errors due to the unmatched impedances at the comparator inputs (one input goes to the resistor

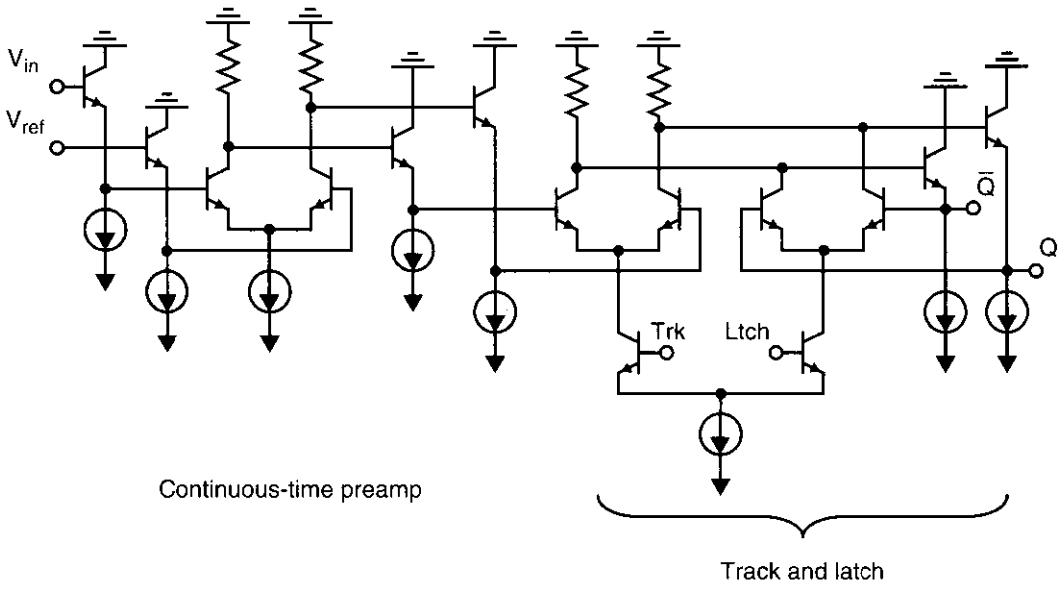


Fig. 13.20 Clocked comparator with a preamplifier to reduce flashback.

string—the other to the input signal). To minimize this effect, most modern comparators have one or two stages of continuous-time buffering and/or preamplification. For example, a commonly used comparator is shown in Fig. 13.20. Notice that it has a buffer, a low-gain preamp, and another buffer before the track-and-latch circuitry. Also notice that in the positive feedback latch the feedback is taken from the emitter-follower outputs, which minimizes the capacitances of the internal nodes of the latch.

Another technique sometimes used to minimize the effects of flashback is to match the input impedances as much as is possible. For example, it is possible to implement a second matched resistor string, with the nodes of the comparators that were originally connected to V_{in} now being connected to it, and the end nodes of the string connected together to V_{in}. This approach matches impedances and also minimizes the resistor-string bowing due to the comparator input currents. Unfortunately, it does result in different delays for V_{in} reaching the various comparators, and unless these are matched to the routing of the clock signals, these different delays may not be tolerable.

13.5 TWO-STEP A/D CONVERTERS

Two-step (or subranging) converters are currently the most popular approach for high-speed medium-accuracy A/D converters. This popularity is due to several advantages they have over their flash counterparts. Specifically, two-step converters require less silicon area, dissipate less power, have less capacitive loading, and the voltages the comparators need to resolve are less stringent than for flash equivalents. However, two-step converters do have a larger latency delay, although their throughput approaches that of flash converters.

The block diagram for a two-step converter is shown in Fig. 13.21. The operation of this two-step converter is as follows. The 4-bit MSB A/D determines the first four MSBs. To determine the remaining LSBs, the quantization error is found by reconverting the 4-bit digital signal to an analog value using the 4-bit D/A and subtracting that

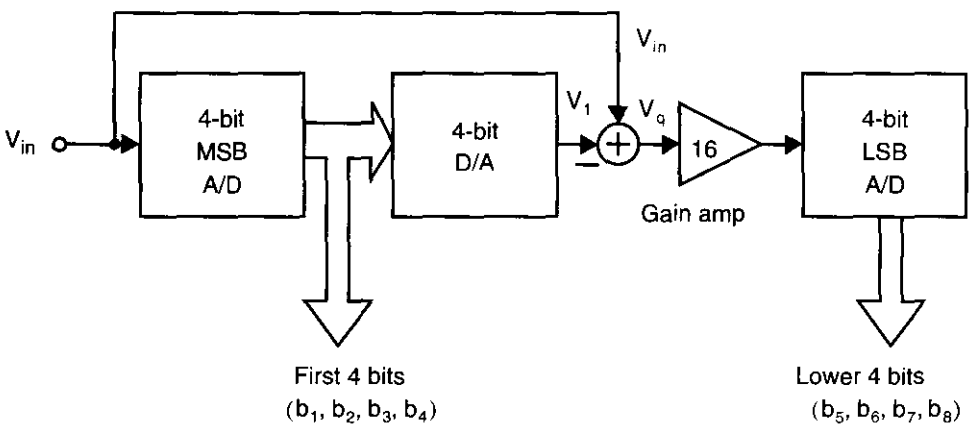


Fig. 13.21 An 8-bit two-step A/D converter.

value from the input signal. To ease the requirements in the circuitry for finding the remaining LSBs, the quantization error is first multiplied by 16 using the gain amplifier, and the LSBs are determined using the 4-bit LSB A/D. With this approach, rather than requiring 256 comparators as in an 8-bit flash converter, only 32 comparators are required for a two-step A/D converter. However, this straightforward approach would require all components to be at least 8-bit accurate. To significantly ease the accuracy requirements of the 4-bit MSB A/D converter, digital error correction is commonly used and is discussed next.

Digital Error Correction

The block diagram for a two-step converter with digital error correction is shown in Fig. 13.22. Although the second sample and hold (S/H_2) is not necessary, its purpose is to allow the first S/H_1 to sample a new input signal before the gain amplifier has finished settling. However, the first S/H_1 is critical and its performance often limits the overall linearity. The reason for digital error correction is to significantly ease the requirements placed on the 4-bit MSB A/D converter. Without error correction, this first A/D converter needs to be at least 8-bit accurate. However, with error correction, the requirements on this MSB A/D converter are that it need only be 4-bit accurate. To see how this correction works and why a second-stage 5-bit converter is needed (rather than 4-bit), consider the quantization error that occurs in an ideal converter. Defining $V_{LSB} = V_{ref}/2^8$ (i.e., always relative to 8-bit accuracy), we have for an

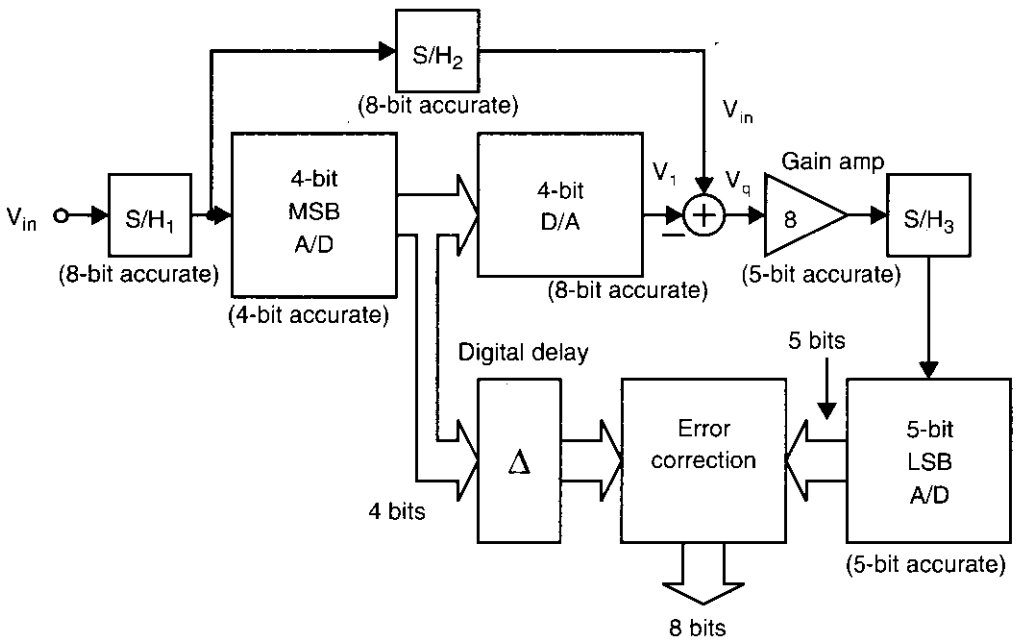


Fig. 13.22 An 8-bit two-step A/D converter with digital error correction.

ideal 8-bit converter,

$$V_{ref}B_{out} = V_{in} + V_q \quad \text{where} \quad -\frac{1}{2}V_{LSB} < V_q < \frac{1}{2}V_{LSB} \tag{13.38}$$

However, for a nonideal 8-bit converter with an absolute accuracy of 0.5 LSB, we have

$$V_{ref}B_{out} = V_{in} + V_q \quad \text{where} \quad -V_{LSB} < V_q < V_{LSB} \tag{13.39}$$

In other words, the maximum quantization signal is now twice that of the ideal case.

Similarly, for an ideal 4-bit A/D converter, we have (keeping the 8-bit definition of V_{LSB}),

$$V_{ref}B_{out} = V_{in} + V_q \quad \text{where} \quad -8V_{LSB} < V_q < 8V_{LSB} \tag{13.40}$$

Thus in the ideal case, the value of V_q can be determined (to 8-bit accuracy) using a 4-bit A/D converter since V_q must be within $16V_{LSB}$. However, for the nonideal case where the 4-bit MSB flash converter has an absolute accuracy of $8V_{LSB}$, the quantization error, V_q, is now bounded within $32V_{LSB}$. Thus, in the case of a non-ideal 4-bit MSB converter, a 5-bit LSB converter must be used; otherwise V_q may go out of range. Note that the gain amplifier of 8 is used to amplify the quantization error back to maximum signal levels to ease the requirements of the 5-bit LSB converter. Finally, to determine V_{in}, we see that the digital value of V_q has been found to within $0.5V_{LSB}$ and the digital value of V_1 is known to the same accuracy since we assumed the D/A converter to be 8-bit accurate (and the digital word applied to the D/A converter is known). Therefore, we find V_{in} from the relation

$$V_{in} - V_1 = V_q \tag{13.41}$$

Specifically, V_{in} is found by properly combining the digital equivalents of V_1 and V_q.

In summary, the MSB A/D need only be accurate to $1/2^4 = 1/16$. The only components that need 0.5 LSB accuracy at the 8-bit level are S/Hs 1 and 2, the D/A, and the subtraction circuit. Besides the difficulty in realizing the S/H circuits, another major limitation is the difficulty of designing a high-speed, accurate (to 0.5 LSB at the 5-bit level) gain amplifier. In fact, due to difficulties in realizing high-speed circuits with gain, often fewer bits are determined in the first stage of a two-step converter to reduce the amplification required. For a more detailed treatment of a two-step A/D converter, the reader is referred to a 10-bit 75 MHz implementation (with integrated S/H), described in [Petschacher, 1990].

EXAMPLE 13.5

For the two-step 8-bit A/D converter shown in Fig. 13.22, what is the maximum voltage range at V_q when the converter's full-scale input is ±2.5 V in the case

where the 4-bit MSB A/D converter is (a) 8-bit accurate and (b) 4-bit accurate? Assume all other components are ideal.

Solution

With a full-scale peak-to-peak input voltage of 5 V applied to an 8-bit A/D converter, we have

$$V_{LSB} = \frac{5}{2^8} = 19.5 \text{ mV} \tag{13.42}$$

For an ideal 4-bit A/D converter, we have from (13.40) the maximum voltage range of V_q is $16V_{LSB}$, or equivalently, 312 mV.

(a) If we go to the trouble to make the 4-bit A/D converter have an absolute accuracy of $0.5V_{LSB}$ (i.e., 8-bit accurate), then V_q becomes bounded between $\pm 8.5V_{LSB}$. In other words, the maximum range of V_q would now be $17V_{LSB}$, or equivalently, 332 mV. Note that the input range of the LSB converter is 8×332 mV = 2.7 V (a little more than half of the input range of the overall converter), so more gain could be used in this case.

(b) In the case of a 4-bit accurate MSB converter, V_q is bounded between $\pm 16V_{LSB}$, implying that the maximum range of V_q is 32 V_{LSB}, or equivalently, 618 mV. After the gain of 8, the input range of the LSB converter becomes 8×618 mV = 4.9 V (the same as the input range of the overall converter).

13.6 INTERPOLATING A/D CONVERTERS

Interpolating converters make use of input amplifiers, as shown in Fig. 13.23. These input amplifiers behave as linear amplifiers near their threshold voltages but are allowed to saturate once their differential inputs become moderately large. As a result, noncritical latches need only determine the sign of the amplifier outputs since the differences between the input signal and threshold voltages have been amplified. Also, the number of input amplifiers attached to V_{in} is significantly reduced by interpolating between adjacent outputs of these amplifiers. While this approach is often combined with a "folding" architecture [van de Grift, 1987; van Valburg, 1992], the interpolating architecture has also been used quite successfully by itself [Goodenough, 1989; Steyaert, 1993].

To further understand this interpolation approach, some possible signals for the input-amplifier outputs, V_1 and V_2, as well as their interpolated values are shown in Fig. 13.24. As can be seen in the figure, the logic levels are assumed to be zero and five volts, with the input comparators having a maximum gain of about −10. Also, here the latch threshold is near the midpoint of the two logic levels (or about 2.5 volts). As V_{in} increases, the latch for V_1 is first triggered, followed by V_{2a} and so on until V_2. As a result, more reference levels have been created between V_1 and V_2. It should be noted here that for good linearity, the interpolated signals need only cross the latch threshold at the correct points, while the rest of the interpolated signals responses are of secondary importance. One way to create such correct crossing

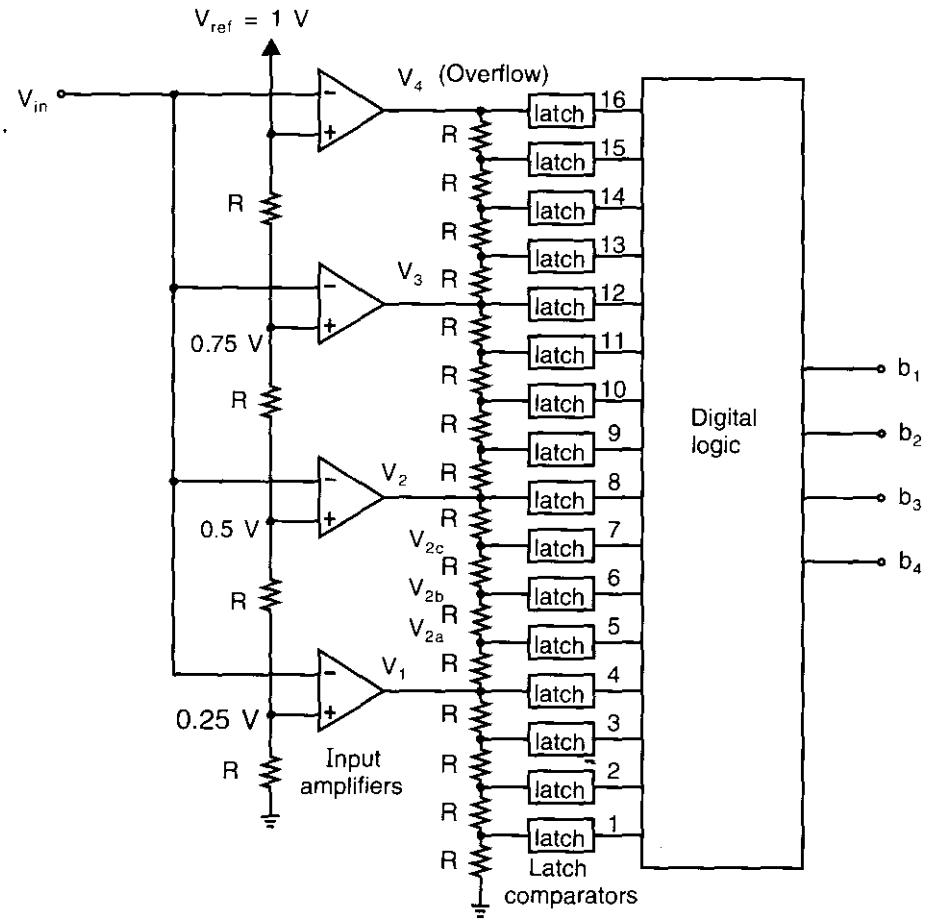


Fig. 13.23 A 4-bit interpolating A/D converter (interpolating factor of 4).

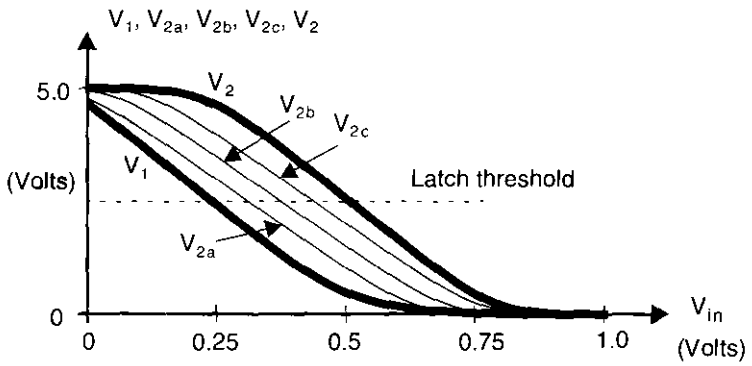


Fig. 13.24 Possible transfer responses for the input-comparator output signals, V_1 and V_2, and their interpolated signals.

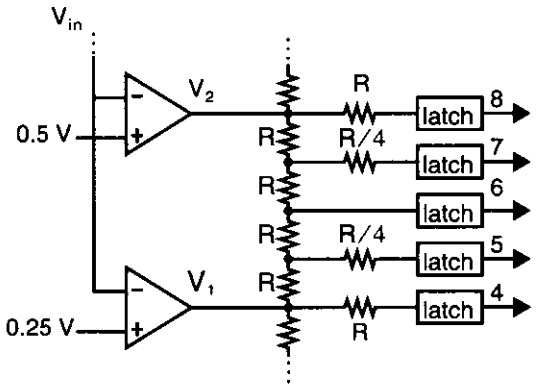


Fig. 13.25 Adding series resistors to equalize delay times to the latch comparators.

points is to ensure that V_1 and V_2 are linear between their own thresholds. In Fig. 13.24, this linear region corresponds to $0.25 < V_{in} < 0.5$.

For fast operation, it is important that the delays to each of the latches are made to equal each other as much as possible. Since the latch comparators have similar input capacitances associated with them, the delays can be made nearly equal by adding extra series resistors, as shown in Fig. 13.25. These series resistors equalize the impedances seen by each latch comparator looking back into the resistive string, assuming the input-amplifier outputs are low impedance [van de Plassche, 1988].

As mentioned earlier, the main benefit of an interpolating architecture is the reduction in the number of differential pairs attached to the input signal, V_{in}. Such a reduction results in a lower input capacitance (which is quite high for a flash converter), a slightly reduced power dissipation, and a lower number of accurate reference voltages that need to be created. Finally, it should be mentioned that circuit techniques other than resistive strings can be used to realize this interpolative approach. In [Steyaert, 1993], current mirrors were used to interpolate eight times between comparators, resulting in a 100-MHz 8-bit A/D converter realized with a 1.5-μm CMOS process. In another implementation, two stages of interpolation using capacitors to interpolate resulted in a 10-bit 20-MHz A/D low-power converter [Kusumoto, 1993].

EXAMPLE 13.6

Using current mirrors, show how one can interpolate two current outputs, I_1 and I_2, by three. What reduction in input capacitance of the converter would be expected over a traditional flash architecture?

Solution

If interpolating by three, it is desired to create two new currents, I_{2a}, I_{2b} such that

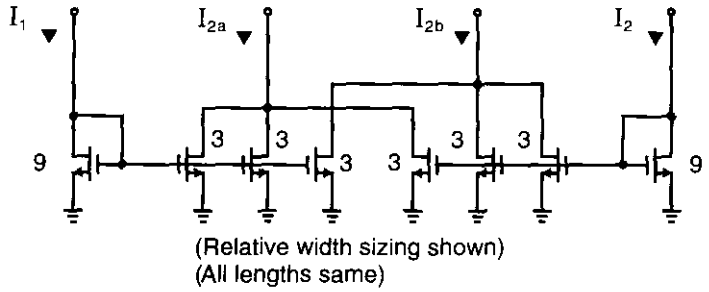


Fig. 13.26 Interpolating by three between two current outputs.

$$I_{2a} = \frac{2}{3}I_1 + \frac{1}{3}I_2 \tag{13.43}$$

$$I_{2b} = \frac{1}{3}I_1 + \frac{2}{3}I_2 \tag{13.44}$$

These output currents can be realized as shown in Fig. 13.26. These four currents can be converted back to voltages to send to the latches. Alternatively, the currents can be directly sent to latches which make use of current inputs.

Since we are interpolating by three here, this converter would require one-third the number of input amplifiers in relation to a traditional flash converter. Thus, the input capacitance for this interpolated approach would be one-third of that for a flash.

13.7 FOLDING A/D CONVERTERS

We just saw that the number of input amplifiers can be reduced through the use of an interpolating architecture. However, the number of latch comparators remains at 2^N for an N-bit converter. This large number of latch comparators can be significantly reduced through the use of a *folding architecture*. A folding A/D converter is similar in operation to a two-step (or subranging) converter in that a group of LSBs are found separately from a group of MSBs. However, whereas a two-step converter requires an accurate D/A converter, a folding converter determines the LSB set more directly through the use of analog preprocessing while the MSB set is determined at the same time.

As an example, consider the 4-bit folding converter shown in Fig. 13.27. Defining the *folding rate* to be the number of output transitions for a single folding block as V_{in} is swept over its input range, we see that the folding rate here is four. This folding rate determines how many bits are required in the MSB converter. The operation of this converter is as follows. The MSB converter determines whether the input signal, V_{in}, is in one of four voltage regions (i.e., between 0 and 1/4, 1/4 and 1/2, 1/2 and 3/4, or 3/4 and 1). Although the MSB converter is shown separately, these bits are usually

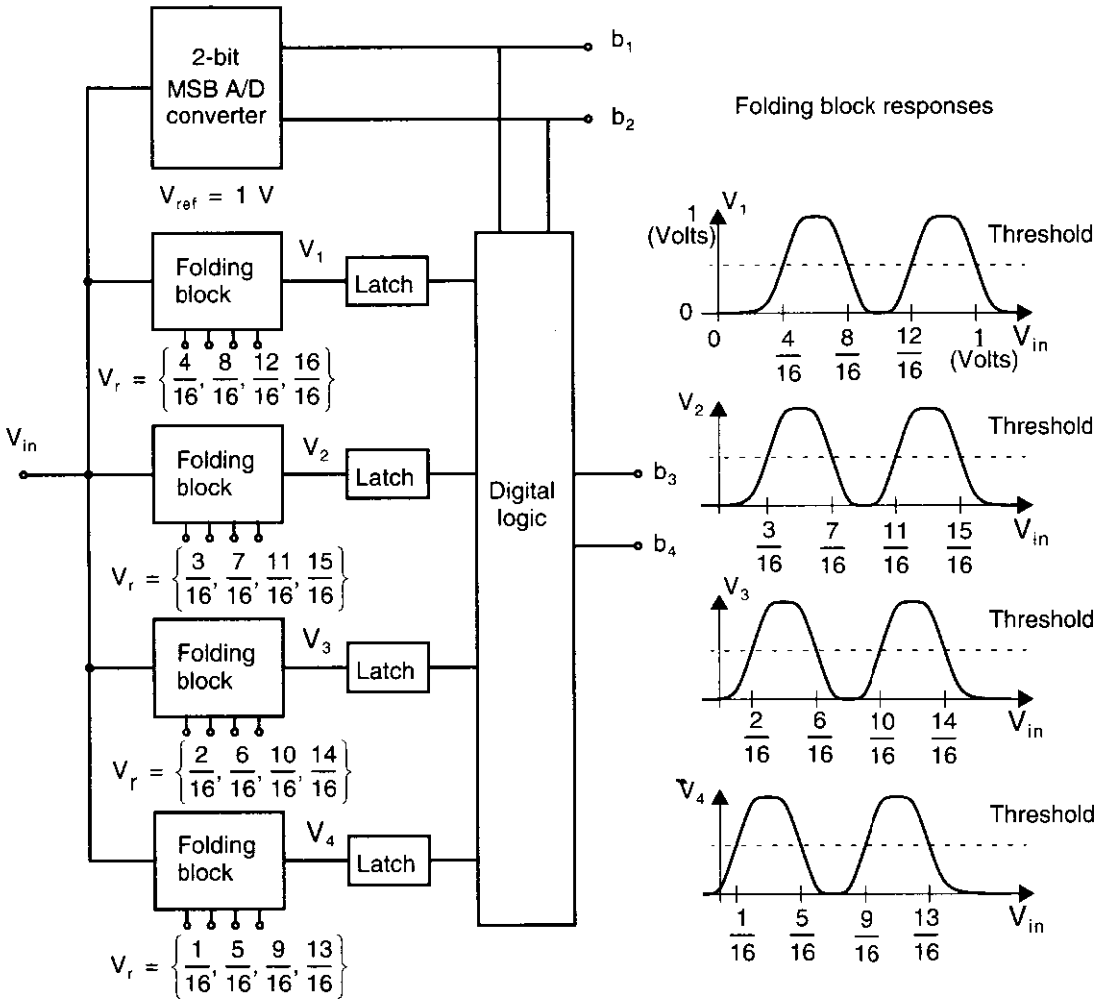


Fig. 13.27 A 4-bit folding A/D converter with a folding rate of four. (The MSB converter would usually be realized by combining some folding block signals.)

determined by combining appropriate signals within the folding blocks. To determine the 2 LSBs, V_1 to V_4 produce a thermometer code for each of the four MSB regions. Note, however, that the four LSB latches are also used for different MSB regions and the thermometer code is inverted when V_{in} is between either 1/4 and 1/2 or 3/4 and 1. For example, as V_{in} increases from 0 to 1/4, the thermometer code changes as 0000, 0001, 0011, 0111, 1111. However, as V_{in} continues to increase to 1/2, the code changes as 1110, 1100, 1000, 0000. Also, note that latch comparators can be used for the LSB set since the transitions are amplified by the folding blocks. In summary, folding reduces the number of latch comparators needed as compared to a flash converter. For example, in a flash 4-bit converter, 16 latches would be required whereas only eight are needed in the 4-bit folding example of Fig. 13.27. Specifically, four

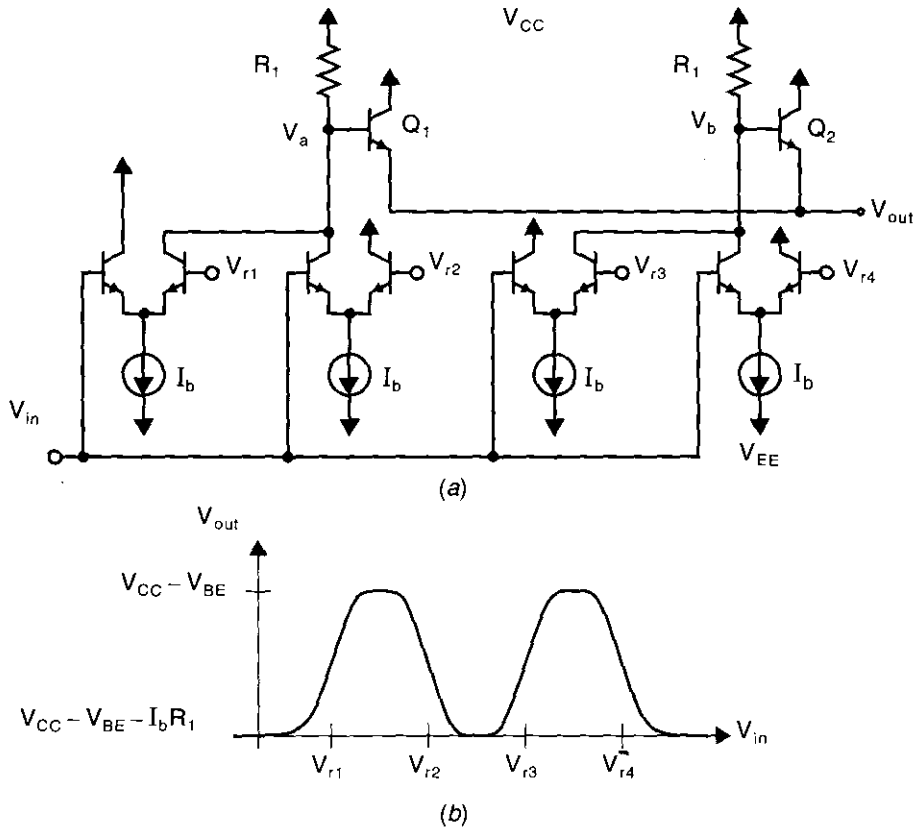


Fig. 13.28 A folding block with a folding-rate of four. (*a*) A possible single-ended circuit realization; (*b*) input-output response.

latches are used for the MSB converter and the other four are shown explicitly. In general, the savings can be greater (see Problem 13.21).

The folding blocks can be realized using cross-coupled differential pairs, as seen in the simplified bipolar circuit shown in Fig. 13.28. Here, four sets of differential-pair transistors are connected in such a way as to realize the input-output response shown in Fig. 13.28(*b*). The output signal V_{out} is related to the voltages V_a and V_b in an "or" type fashion. In other words, V_{out} is low only if both V_a and V_b are low; otherwise, V_{out} is high. With regard to the behavior of V_a and V_b, note that V_b remains low whenever V_{in} is less than V_{r3} or greater than V_{r4}. However, V_a remains low whenever V_{in} is greater than V_{r2} or less than V_{r1}. Also, the cross coupling of adjacent differential pairs causes V_a to go high when V_{in} is between V_{r1} and V_{r2}, while V_b goes high when V_{in} is between V_{r3} and V_{r4}. Such behaviors for V_a and V_b give rise to the folding output for V_{out}, as shown.

Some points worth mentioning here are that for full-scale input signals, the output signal from a folding block is at a much higher frequency than the input signal. In fact, the frequency of the folding block's output signal is equal to the multiplication of the frequency of the input signal times the folding rate. This multiplying effect limits

the practical folding rate used in high-speed converters. Also, it should be mentioned that the circuit shown is a single-ended version, and differential circuits are almost always used in practical implementations.

Another point to note here is that while the folding approach reduces the number of latch comparators, a large input capacitance similar to that for a flash converter is also present with the folding circuit shown. In fact, flash converters have similar input stages of differential pairs of transistors for each comparator, but they are, of course, not cross coupled. Since the number of differential pairs in each folding block equals the folding rate, and the input signal goes to one side of each differential pair, it can be shown that the number of transistors driven by the input signal equals 2^N—the same number as for a flash converter. To reduce this large input capacitance, folding converters also make use of an interpolating architecture. With an interpolate-by-two

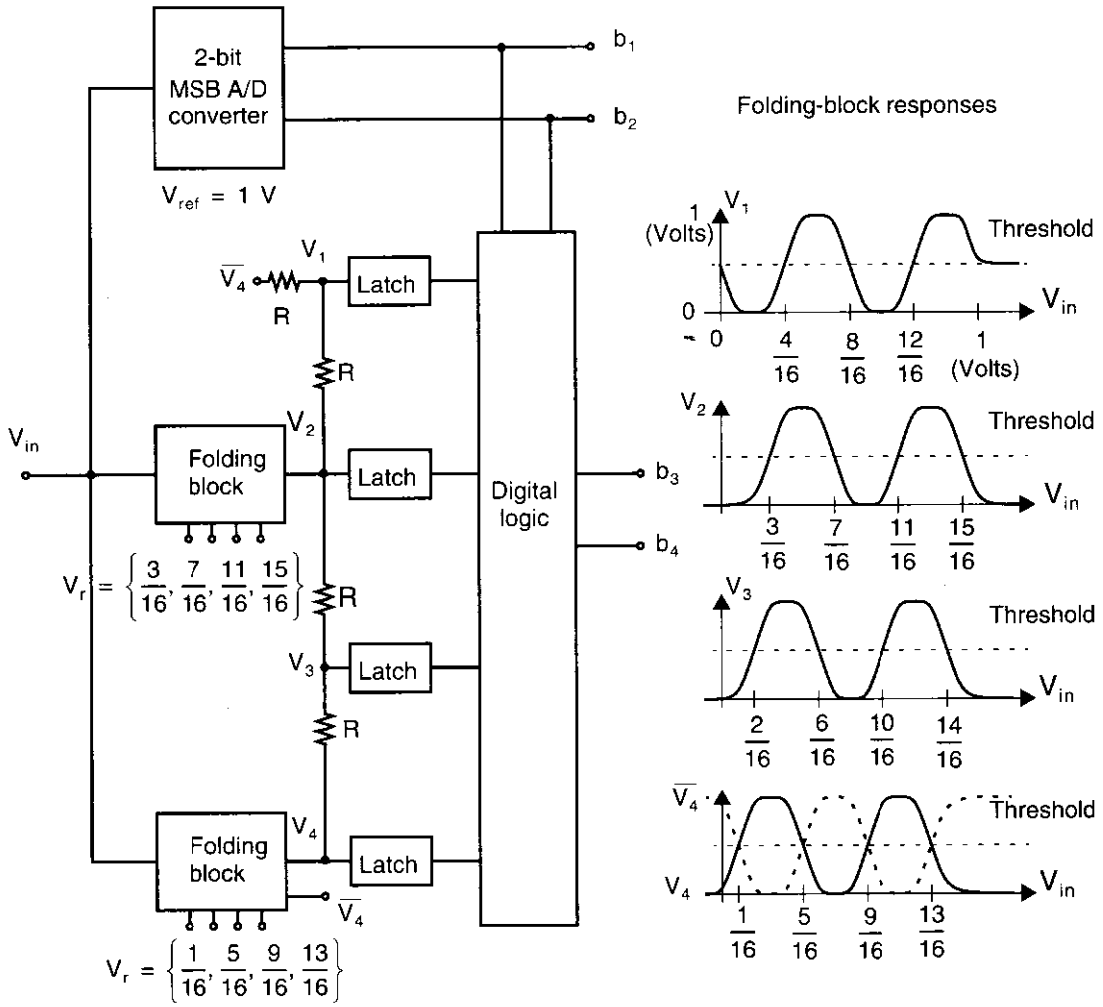


Fig. 13.29 A 4-bit folding A/D converter with a folding rate of four and an interpolate-by-two. (The MSB converter would usually be realized by combining some folding-block signals.)

technique applied to the 4-bit example, the resulting architecture would be that shown in Fig. 13.29. Note that a new inverted signal $\overline{V_4}$ is required to connect the top folding block to the bottom one. Although the creation of this inverted signal is needed in a single-ended version, no extra circuitry is required in a differential version since it can be accomplished by simply cross-coupling the differential output wires.

In [van Valburg, 1992], in order to realize a very-high-speed 8-bit converter, four folding blocks each with a folding rate of eight were used. Assuming $V_{ref} = 1$ V, then the difference between reference voltages of adjacent inputs of a folding block was 1/8 V. Each adjacent folding block was offset by 1/32 V, giving zero crossings at each 1/32 V. By interpolating between each adjacent folding block using four 8-tap resistor strings, zero crossings every 1/256 V were obtained (i.e., an 8-bit converter with 32 latch comparators connected to the interpolating resistor strings). The MSBs were realized by taking appropriate outputs from selected differential pairs and summing them separately to realize additional folding amplifiers with reduced folding rates. The final A/D converter could be clocked at 650 MHz and could resolve a 150-MHz sinusoid with 7.8 bits effective resolution, while dissipating only 0.8 W and requiring only 1.8×2 mm^2 active area. The converter also included circuitry to prevent bubble errors, as shown in Fig. 13.19. Other examples of folding converters are given in [van de Grift, 1987, and Colleran, 1993]. In addition, folding converters have been used in the internal operation of a two-step converter [Vorenkamp, 1992].

EXAMPLE 13.7

In Fig. 13.27, show how the two MSBs can be derived using internal signals from the folding blocks.

Solution

The MSB, b_1 is determined by the input signal being above or below $V_{ref}/2$. Looking at Fig. 13.27, we see that the input is compared to the appropriate signal, $(8/16)V_{ref}$ in the top folding block, producing V_1. As a result, the MSB is easily obtained by using the collector current of the transistor connected to V_{r2} in the top folding block. Similarly, the top folding block uses references 4/16 and 12/16, which are needed to determine the second bit, b_2. In fact, the signal V_1 can be used directly as the second bit, b_2, as seen in Fig. 13.27. Thus, the top two bits, b_1 and b_2, can be determined using the top folding block, as shown in Fig. 13.30.

13.8 PIPELINED A/D CONVERTERS

The two-stage architecture described in Section 13.5 can be generalized to multiple stages, where each stage finds a single bit. Specifically, the first stage finds the most-significant bit, b_1, the second stage finds the next bit, b_2, and so on. Unfortunately, a straightforward implementation of this approach would be too slow, since the final bit

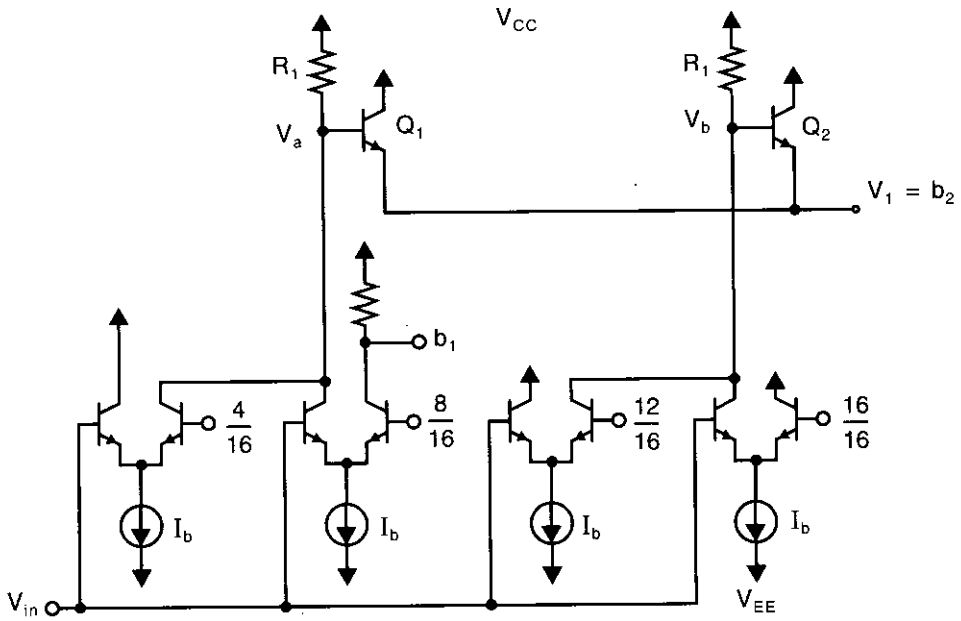


Fig. 13.30 Using the V_1 folding block to also determine the top two MSBs.

would not be available until residual errors ripple through the entire converter. A better approach is to also incorporate *pipelining* such that once the first stage completes its work, it does not sit idle while the remaining lower bits are found, but immediately starts work on the next input sample. A block diagram of a pipelined A/D converter is shown in Fig. 13.31 [Martin, 1981].

Each digital approximator (DAPRX) performs the basic operation required in the algorithmic algorithm. Specifically, for a signed conversion, the input voltage is compared to 0 V. If $V_{in} > 0$, then $V_{out} = 2\,V_{in} - V_{ref}/2$, and $B_{out} = 1$. Otherwise, $V_{out} = 2\,V_{in} + V_{ref}/2$, and $B_{out} = 0$.

Also, each DAPRX contains an S/H to store the input signal. This S/H allows the preceding DAPRX to be immediately used to process its next input signal before the succeeding DAPRX has finished, as long as the preceding DAPRX's digital output is also stored.

Although it takes N clock cycles to process each input signal (i.e., the latency is N), a new sample can be entered in the pipeline each clock cycle. Thus, the processing rate is one sample/cycle, but the complexity is only proportional to N, which is less than other architectures also processing one sample/cycle. This makes pipelined A/D converters a good choice where small area is important. The block diagram of a DAPRX is shown in Fig. 13.32. It should be mentioned here that the S/H can be incorporated into the gain of two amplifiers, if desired.

In some pipelined implementations, more than one bit is converted per stage. In this case, the DAPRX can be realized as shown in Fig. 13.33. For a multi-bit per stage pipelined converter, digital error correction can be added similar to that for a two-stage A/D converter. The major limitation on the accuracy in pipelined convert-

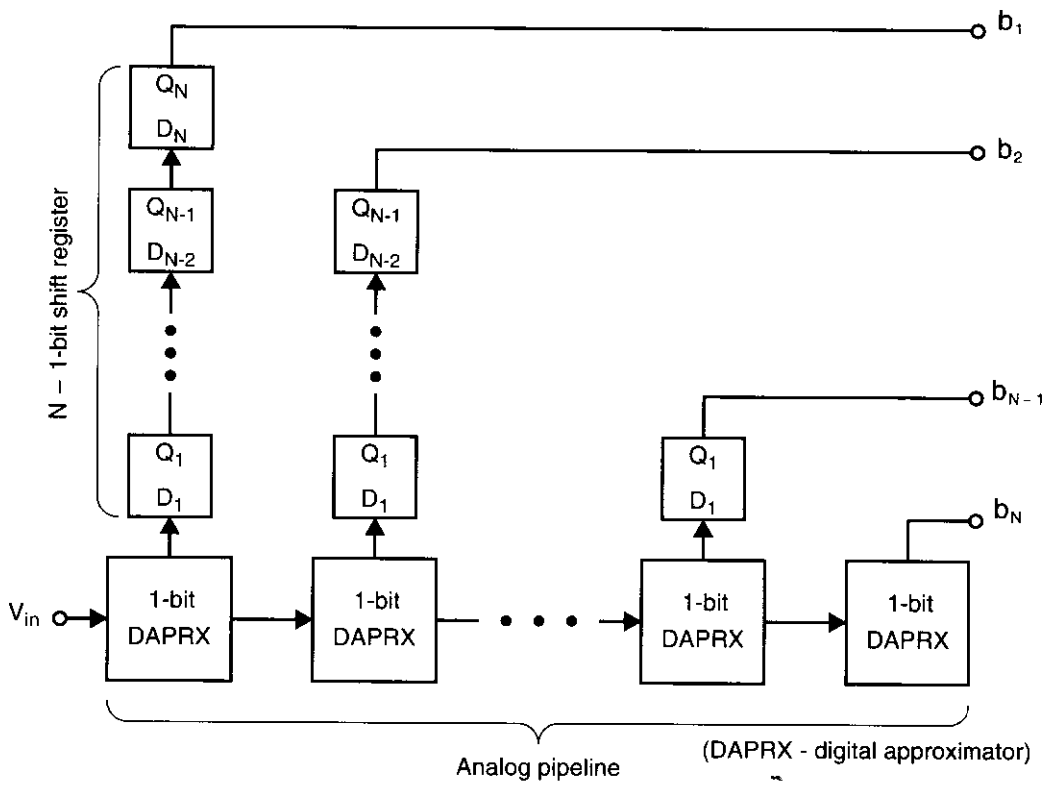


Fig. 13.31 A pipelined A/D converter.

ers is the gain amplifier, especially in the first few stages, where accuracy requirements are most stringent. For this reason, the gain is often taken smaller for the first stages (perhaps even equal to unity), which makes the realization of a high-speed gain amplifier considerably easier. The S/H is also a critical component, especially for multi-bit implementations. Also, presently most pipelined A/D converters are switched-capacitor implementations.

Current state of the art is 12 to 15 bits for pipelined converters with error correction at 1 to 2 MHz. The speed is expected to go up substantially in the near future. Some examples of pipelined A/D converters are given in [Martin, 1981; Sutarja, 1988; Song, 1988; Lin, 1991; and Karanicolas, 1993].

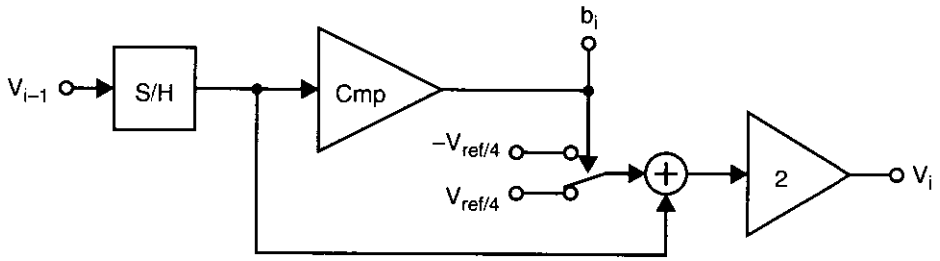


Fig. 13.32 A 1-bit digital approximator (DAPRX).

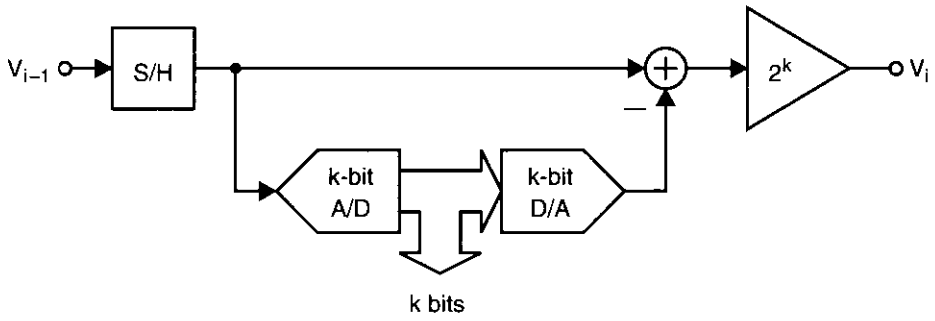


Fig. 13.33 A multi-bit digital approximator (DAPRX).

13.9 TIME-INTERLEAVED A/D CONVERTERS

Very-high-speed A/D conversions can be realized by operating many A/Ds in parallel [Black, 1980]. The system architecture for a four-channel A/D is shown in Fig. 13.34. Here, ϕ_0 is a clock at four times the rate of ϕ_1 to ϕ_4. Additionally, ϕ_1 to ϕ_4 are delayed with respect to each other by the period of ϕ_0, such that each converter will

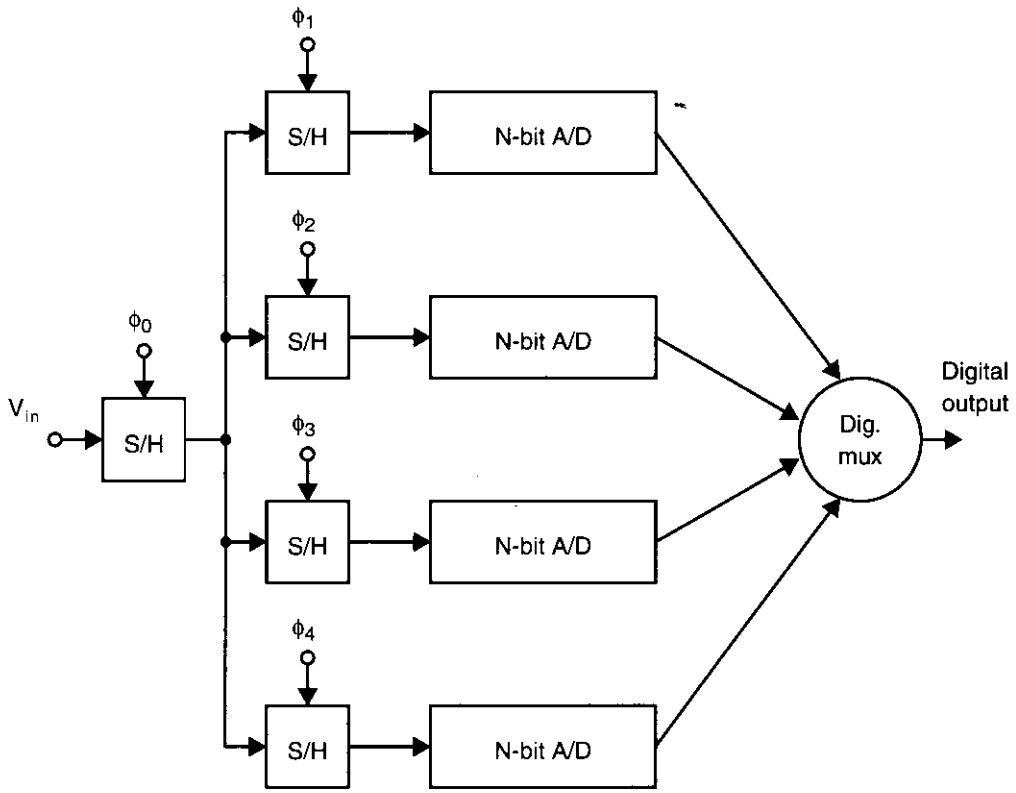


Fig. 13.34 A four-channel time-interleaved A/D converter.

get successive samples of the input signal, V_{in}, sampled at the rate of ϕ_0. In this way, the four A/D converters operate at one-quarter the rate of the input sampling frequency.

With this approach, the input S/H making use of ϕ_0 is critical, while the remaining four S/H converters can have considerable jitter since the signal is already sampled at that point. Thus, sometimes the input S/H is realized in a different technology, such as GaAs, while the remaining S/H circuits could be realized in silicon. An example of a 1 GHz 6-bit A/D converter using time interleaving and GaAs S/H circuits is described in [Poulton, 1987], where four bipolar converters operating at 250 MHz were used.

It is also essential that the channels are extremely well matched, as mismatches will produce tones at f_s/m when there are m channels. For example, consider a dc input signal in a four-channel time-interleaved converter where one converter has a dc offset of, say, 100 mV. Such a system will produce every fourth digital word different from the other three and hence a tone at $f_s/4$. Such nonideal behavior can be disastrous for many applications since the tone may reside well within the frequency of interest.

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13.11 PROBLEMS

13.1 What is the worst-case conversion time for an 18-bit dual-slope integrating A/D converter when the clock rate is 5 MHz?

13.2 Consider an 18-bit integrating A/D converter, as shown in Fig. 13.1, where V_{ref} equals 10 volts, $C_1 = 100$ pF, and a clock frequency of 1 MHz is used. What value of R_1 should be chosen such that the opamp output never exceeds 10 volts when $0 \text{ V} < V_{in} < 10 \text{ V}$?

13.3 Derive the equivalent of (13.8) for Fig. 13.1 when the opamp has an input-offset voltage of V_{off1} and the comparator has an input-offset voltage of V_{off2}.

13.4 What is the offset error (in LSBs) of the converter described in Problem 13.2 when the integrating opamp has an input-offset voltage of 20 mV?

13.5 What input-signal frequencies are completely attenuated by a dual-slope 16-bit integrating A/D having a clock frequency of 1 MHz ? For this same converter, what is the attenuation of an input signal at 60 Hz ?

13.6 Repeat Problem 13.5 with the converter's clock frequency being equal to 100 kHz.

13.7 Consider a 4-bit unipolar DAC-based successive-approximation A/D converter, as shown in Fig. 13.5. Find the sequence of the D/A converter's output levels for an input of 3.333 volts when $V_{ref} = 8$ V. What is the final digital output?

13.8 Consider a 4-bit unipolar charge-redistribution A/D converter, as shown in Fig. 13.7, where $V_{ref} = 8$ V. Find the sequence of the voltage level for V_x if the input signal is 3.333 volts.

13.9 Repeat Problem 13.8, assuming that a parasitic capacitance of 8 C is connected between the node at V_x and ground. Is the final digital result affected?

13.10 Show a method for modifying the unipolar charge-redistribution A/D converter shown in Fig. 13.7 such that the threshold offsets of $0.5V_{LSB}$ are correctly realized.

13.11 How is the digital code obtained from the signed charge redistribution A/D converter shown in Fig. 13.8 converted to a 2's complement code?

13.12 What value of error voltage V_{x1} would be measured in Fig. 13.11(*a*) if the total array capacitance equals 64 pF, the MSB (i.e., b_1) capacitor equals 31.5 pF, and there is a parasitic capacitance to ground of 10 pF on node V_x? For the same circuit, show that the error voltage, V_{e1}, that occurs when using the MSB capacitor during a normal conversion equals $0.5V_{x1}$.

13.13 For the same circuit as described in Problem 13.12, what value of error voltage V_{x2} would be measured in Fig. 13.11(*b*) if the MSB-1 (i.e., b_2) capacitor equals 16.4 pF? Show that the error voltage, V_{e2}, that occurs when using the MSB-1 capacitor during a normal conversion equals $0.5(V_{x2} - V_{e1})$.

13.14 Assuming switch resistances are all about 1 kΩ, estimate the settling time needed for a 12-bit charge-redistribution A/D converter where the total array capacitance equals 128 pF.

13.15 Draw a block diagram similar to that for Fig. 13.22 for a 10-bit two-step A/D converter where the first stage determines 4 bits. Indicate the accuracy needed in all the blocks.

13.16 Show that the circuit shown in Fig. 13.25 results in all time constants being equal when each of the latches has the same input capacitance and the amplifiers have zero output impedance.

13.17 Consider the clocked comparator shown in Fig. 13.18, where

$$\mu_n C_{ox} = 2\,\mu_p C_{ox} = 100\ \mu A/V^2$$

$$2\left(\frac{W}{L}\right)_n = \left(\frac{W}{L}\right)_p = 2$$

$$|V_{tn}| = |V_{tp}| = 1 \text{ V}$$

$$V_{DD} = 5 \text{ V}$$

$$\text{and } V_{SS} = 0 \text{ V}$$

If the MOSFETS in the inverter are ideal except for each having a 100-kΩ output impedance when active, find the minimum differential input that will cause a 1-volt change (use a linear analysis). Assuming this minimum differential input corresponds to (1/2) LSB, what is the maximum number of bits that this comparator could determine in a flash A/D converter?

13.18 In Section 13.6, it was stated that the interpolated signals will have the correct threshold crossings if V_1 and V_2 in Fig. 13.24 are linear in the region $0.25 < V_{in} < 0.5$. In fact, this region is larger than what is actually necessary. What is the minimum region of V_{in} that V_1 and V_2 should be linear over?

13.19 Many very-high-speed A/D converters do not use a sample and hold since it would limit their speed, but instead allow the input signal to be applied to the array of comparators, which are all clocked "simultaneously." Qualitatively, explain why a clocked flash or interpolating A/D converter might operate faster than a sample-and-hold circuit.

13.20 In an N-bit folding A/D converter (with no interpolation), what is the product of the folding rate times the number of folding blocks?

13.21 Find an expression for the number of latches in an N-bit folding A/D converter where the folding rate is $FR = 2^F$.

13.22 Assuming the input capacitance of a differential stage is the same in either a flash or folding/interpolating A/D converter, what reduction of input capacitance over a flash converter would be achieved with an 8-bit folding/interpolating A/D converter having four folding blocks, each with a folding rate of eight? If a straight interpolating A/D converter is to have the same reduction in input capacitance, how many resistors are required between "input comparators"?

13.23 Draw the clock waveforms of the sample-and-hold circuits for the time-interleaved A/D converter shown in Fig. 13.34.

CHAPTER

14 Oversampling Converters

Recently, oversampling A/D and D/A converters have become popular for high-resolution medium-to-.low-speed applications such as high-quality digital audio. The major reasons for their popularity include the following: First, oversampling converters relax the requirements placed on the analog circuitry at the expense of more complicated digital circuitry. This trade-off becomes more desirable for modern submicron technologies with 3.3-V power supplies where complicated high-speed digital circuitry is more easily realized in less area, but the realization of high-resolution analog circuitry is complicated by low power-supply voltages and poor transistor output impedance (caused by short-channel effects). With oversampling data converters, the analog components have reduced requirements on matching tolerances and amplifier gains. A second advantage of oversampling converters is that they simplify the requirements placed on the analog anti-aliasing filters for A/D converters and smoothing filters for D/A converters. For example, usually only a first-order anti-aliasing filter is required for A/D converters, which can often be realized on chip or at worst case very inexpensively off chip. Furthermore, a sample-and-hold is usually not required at the input of an oversampling A/D converter.

In this chapter, the basics of oversampling converters are discussed first. We shall see that extra bits of resolution can be extracted from converters that sample much faster than the Nyquist rate. Furthermore, this extra resolution can be obtained with lower oversampling rates by spectrally shaping the quantization noise through the use of feedback. The use of shaped quantization noise applied to oversampling signals is commonly referred to as delta-sigma ($\Delta\Sigma$) modulation.[1] Simple first- and second-order $\Delta\Sigma$ modulators are discussed, followed by a discussion of typical system architectures for $\Delta\Sigma$ data converters. Next, two popular approaches for realizing decimation filters are described. Descriptions of some modern approaches are then described along with some practical considerations. The chapter concludes with an example design of a third-order $\Delta\Sigma$ A/D converter.

14.1 OVERSAMPLING WITHOUT NOISE SHAPING

In this section, the advantage of sampling at higher than the Nyquist rate is discussed. Here, we shall see that extra dynamic range can be obtained by spreading the

1. Delta-sigma modulation is also sometimes referred to as sigma-delta modulation.

quantization noise power over a larger frequency range. However, we shall see that the increase in dynamic range is only 3 dB for every doubling of the sample rate. To obtain much higher dynamic-range improvements as the sampling rate is increased, noise shaping through the use of feedback can be used and is discussed in the next section.

Quantization Noise Modelling

We begin by modelling a quantizer as adding quantization error $e(n)$, as shown in Fig. 14.1. The output signal, $y(n)$, is equal to the closest quantized value of $x(n)$. The *quantization error* is the difference between the input and output values. This model is exact if one recognizes that the quantization error is not an independent signal but may be strongly related to the input signal, $x(n)$. This linear model becomes approximate when assumptions are made about the statistical properties of $e(n)$, such as $e(n)$ being an independent white-noise signal. However, even though approximate, it has been found that this model leads to a much simpler understanding of $\Delta\Sigma$ and with some exceptions is usually reasonably accurate.

White Noise Assumption

If $x(n)$ is very active, $e(n)$ can be approximated as an independent random number uniformly distributed between $\pm\Delta/2$, where Δ equals the difference between two adjacent quantization levels. Thus, the quantization noise power equals $\Delta^2/12$ (from Section 11.3) and *is independent of the sampling frequency*, f_s. Also, the spectral density of $e(n)$, $S_e(f)$, is white (i.e., a constant over frequency) and all its power is within $\pm f_s/2$ (a two-sided definition of power).

Assuming white quantization noise, the spectral density of the quantization noise, $S_e(f)$ appears as shown in Fig. 14.2.

The spectral density height is calculated by noting that the total noise power is $\Delta^2/12$ and, with a two-sided definition of power, equals the area under $S_e(f)$ within

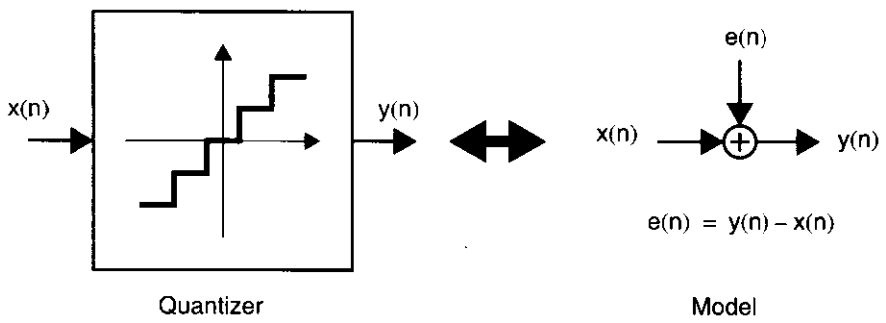


Fig. 14.1 Quantizer and its linear model.

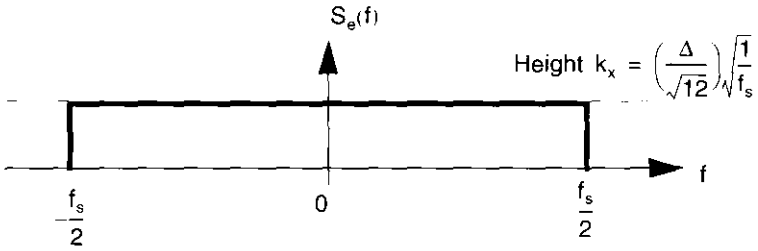


Fig. 14.2 Assumed spectral density of quantization noise.

$\pm f_s/2$, or mathematically,

$$\int_{-f_s/2}^{f_s/2} S_e^2(f)\,df = \int_{-f_s/2}^{f_s/2} k_x^2\,df = k_x^2 f_s = \frac{\Delta^2}{12} \tag{14.1}$$

Solving this relation gives

$$k_x = \left(\frac{\Delta}{\sqrt{12}}\right)\sqrt{\frac{1}{f_s}} \tag{14.2}$$

EXAMPLE 14.1

Find the output and quantization errors for two different quantizers, as shown in Fig. 14.3, when the input values are

$$x(n) = \{0.01, 0.31, -0.11, 0.80, 0.52, -0.70\} \tag{14.3}$$

Also find the expected power and the power density height, $S_e^2(f)$, of the quantization noise when the sampling frequency is normalized to 2π rad/sample.

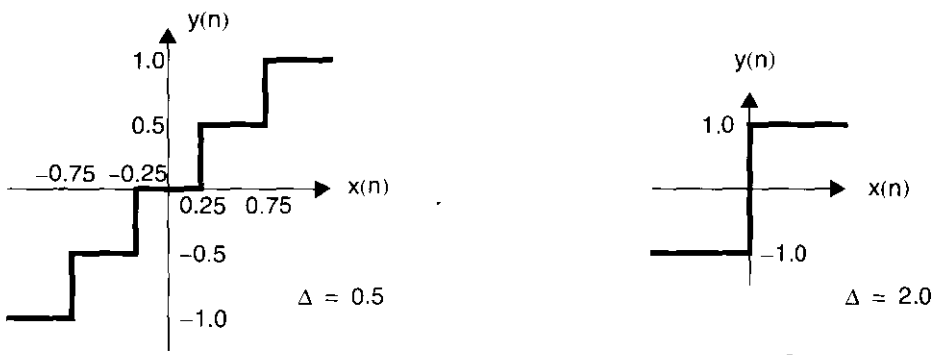


Fig. 14.3 Two example quantizers.

Table 14.1 Example signal values and quantization noise for two quantizers.

	Quantizer I (Five Levels)		Quantizer II (Two Levels)	
x(n)	y(n)	e(n)	y(n)	e(n)
0.01	0.0	–0.01	1	0.99
0.31	0.5	0.19	1	0.69
–0.11	0.0	0.11	–1	–0.89
0.80	1.0	0.2	1	0.20
0.52	0.5	–0.02	1	0.48
–0.70	–0.5	0.2	–1	–0.30

Solution

The output and quantization noise values for this example are given in Table 14.1. Note that although the output signals, $y(n)$, are well-defined values, the quantization error values can be approximated as uniformly distributed random numbers since the input signal is quite active.

Recalling that the quantization noise power is given by

$$P_e = \frac{\Delta^2}{12} \tag{14.4}$$

then the expected noise powers of the two quantizers are

$$P_I = \frac{0.5^2}{12} = 0.0208 \text{ W} \tag{14.5}$$

$$P_{II} = \frac{2^2}{12} = 0.333 \text{ W} \tag{14.6}$$

where we note that these values are not affected by normalizing the sampling frequency. Also note that the two power estimates for P_I and P_{II} correspond to rms power levels of 0.144 and 0.577, respectively.

For the power density, we note that the power is spread evenly between $\pm f_s/2$, resulting in a density of

$$S_e^2(f) = \frac{P_e}{f_s} \tag{14.7}$$

which results in

$$S_{eI}^2(f) = \left(\frac{0.0208}{2\pi}\right) = 0.00331 \frac{\text{W}}{\text{rad/sample}} \tag{14.8}$$

$$S_{eII}^2(f) = \left(\frac{0.333}{2\pi}\right) = 0.053 \frac{\text{W}}{\text{rad/sample}} \tag{14.9}$$

Oversampling Advantage

Oversampling occurs when the signals of interest are bandlimited to f_0 yet the sample rate is at f_s, where $f_s > 2f_0$ ($2f_0$ being the Nyquist rate or, equivalently, the minimum sampling rate for signals bandlimited to f_0). We define the oversampling ratio, OSR, as

$$\text{OSR} \equiv \frac{f_s}{2f_0} \tag{14.10}$$

After quantization, since the signals of interest are all below f_0, $y_1(n)$ is filtered by $H(f)$ to create the signal $y_2(n)$, as shown in Fig. 14.4. This filter eliminates quantization noise (together with any other signals) greater than f_0.

Assuming the input signal is a sinusoidal wave, its maximum peak value without clipping is $2^N(\Delta/2)$. For this maximum sinusoidal wave, the signal power, P_s, has a power equal to

$$P_s = \left(\frac{\Delta 2^N}{2\sqrt{2}}\right)^2 = \frac{\Delta^2 2^{2N}}{8} \tag{14.11}$$

The power of the input signal within $y_2(n)$ remains the same as before since we assumed the signal's frequency content is below f_0. However, the quantization noise power is reduced to

$$P_e = \int_{-f_s/2}^{f_s/2} S_e^2(f)|H(f)|^2\,df = \int_{-f_0}^{f_0} k_x^2\,df = \frac{2f_0\Delta^2}{f_s}\frac{}{12} = \frac{\Delta^2}{12}\left(\frac{1}{\text{OSR}}\right) \tag{14.12}$$

Therefore, doubling OSR (i.e., sampling at twice the rate) decreases the quantization noise power by one-half or, equivalently, 3 dB (or, equivalently, 0.5 bits).

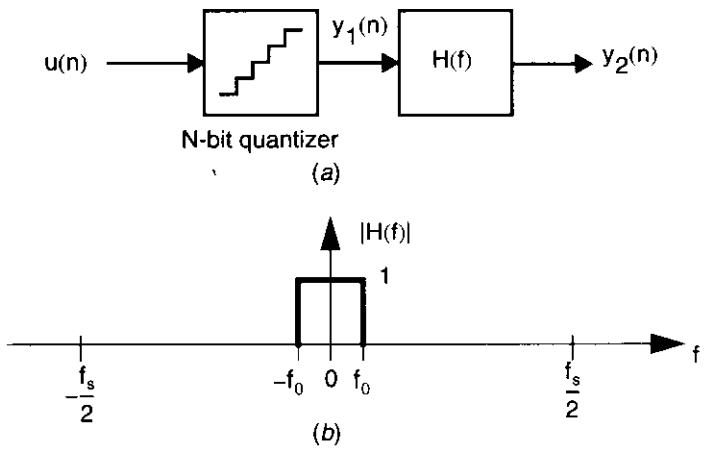


Fig. 14.4 *(a)* A possible oversampling system without noise shaping. *(b)* The brick-wall response of the filter to remove much of the quantization noise.

We can also calculate the maximum SNR (in dB) to be the ratio of the maximum sinusoidal power to the quantization noise in the signal $y_2(n)$. Mathematically, we have through the use of (14.11) and (14.12)

$$\mathrm{SNR}_{\max} = 10\log\left(\frac{P_s}{P_e}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log(\mathrm{OSR}) \tag{14.13}$$

which is also equal to

$$\mathrm{SNR}_{\max} = 6.02N + 1.76 + 10\log(\mathrm{OSR}) \tag{14.14}$$

The first term is the SNR due to the N-bit quantizer while the OSR term is the SNR enhancement obtained from oversampling. Here we see that straight oversampling gives a SNR improvement of 3 dB/octave or, equivalently, 0.5 bits/octave. The reason for this SNR improvement through the use of oversampling is that when quantized samples are averaged together, the signal portion adds linearly, whereas the noise portion adds as the square root of the sum of the squares.

EXAMPLE 14.2

Consider a sampled dc signal, V_s, of value 1 V where the measured voltage, V_{meas}, is V_s plus a noise signal, V_{noise}. Assume V_{noise} is a random signal uniformly distributed between $\pm\sqrt{3}$. What is the SNR for V_{meas} when looking at individual values? If eight samples of V_{meas} are averaged together, roughly what is the new SNR? To illustrate the results, use eight typical samples for V_{meas} of {0.94, –0.52, –0.73, 2.15, 1.91, 1.33, –0.31, 2.33}.

Solution

Referencing signals to 1 Ω, we calculate the power of V_s and V_{noise} to both be 1 watt. Thus the SNR for V_{meas} is 0 dB when looking at individual V_{meas} values. Note that it is difficult to see the signal value of 1 V in the example V_{meas} samples since the SNR is so poor.

If eight samples are averaged, we are realizing a modest low-pass filter, resulting in the oversampling ratio being approximately equal to 8 (this is a rough estimate since a brick-wall filter is not being used). Since each octave of oversampling results in a 3-dB SNR improvement, the averaged value should have a SNR of around 9 dB. Note that averaging the eight given V_{meas} samples results in 0.8875, which more closely represents the signal value of 1 V.

The reason oversampling improves the SNR here is that by summing eight measured values, the eight signal values add linearly to 8 V_{rms} (or 64 watts) while the eight noise values add to $\sqrt{8}$ V_{rms} (or 8 watts), since the noise values are assumed to be independent.

EXAMPLE 14.3

Given that a 1-bit A/D converter has a 6-dB SNR, what sample rate is required using oversampling (no noise shaping) to obtain a 96-dB SNR (i.e., 16 bits) if $f_0 = 25$ kHz ? (Note that the input into the A/D converter has to be very active for the white-noise quantization model to be valid—a difficult arrangement when using a 1-bit quantizer with oversampling without noise shaping).

Solution

Oversampling (without noise shaping) gives 3 dB/octave where 1 octave implies doubling the sampling rate. We require 90 dB divided by 3 dB/octave , or 30 octaves. Thus, the required sampling rate, f_s, is

$$f_s = 2^{30} \times 2f_0 \cong 54{,}000 \text{ GHz !}$$

This example shows why noise shaping is needed to improve the SNR faster than 3 dB/octave , since 54,000 GHz is highly impractical.

The Advantage of 1-bit D/A Converters

While oversampling improves the signal-to-noise ratio, it does not improve linearity. For example, if a 16-bit linear converter is desired while using a 12-bit converter with oversampling, the 12-bit converter must have an integral nonlinearity error less than $1/2^4$ LSB (here, LSB refers to that for a 12-bit converter). In other words, the component accuracy would have to match better than 16-bit accuracy (i.e., $100 \times (1/2^{16}) = 0.0015$ percent accuracy). Thus, some sort of auto calibration or laser trimming must be used to obtain the required linearity. However, as we saw in Example 14.3, with a high enough sampling rate, the output from a 1-bit converter can be filtered to obtain the equivalent of a 16-bit converter. *The advantage of a 1-bit D/A is that it is inherently linear.*[2] This linearity is a result of a 1-bit D/A converter having only two output values and, since two points define a straight line, no trimming or calibration is required. This inherent linearity is one of the major motivations for making use of oversampling techniques with 1-bit converters. In fact, the reader may be aware that many audio converters presently use 1-bit converters for realizing 16- to 18-bit linear converters (with noise shaping). In addition, 20-bit linearity has been reported without the need for any trimming [Leopold, 1991]. Finally, it should be mentioned that there are other advantages when using oversampling techniques, such as a reduced requirement for analog anti-aliasing and smoothing filters.

2. This assumes that second-order errors due to imperfections such as signal-dependent power supply, or reference voltages, or memory in the D/A converter are not present.

14.2 OVERSAMPLING WITH NOISE SHAPING

In this section, the advantage of noise shaping the quantization noise through the use of feedback is discussed. Here, we shall see a much more dramatic improvement in dynamic range when the input signal is oversampled as compared to oversampling the input signal with no noise shaping. Although this section illustrates the basic principles with reference to A/D converters, much of it applies directly to ΔΣ D/A converters as well.

The system architecture of a ΔΣ oversampling A/D converter is shown in Fig. 14.5. The first stage is a continuous-time anti-aliasing filter and is required to band-limit the input signal to frequencies less than one-half the oversampling frequency, f_s. When the oversampling ratio is large, the anti-aliasing filter can often be quite simple, such as a simple RC low-pass filter. Following the anti-aliasing filter, the continuous-time signal, $x_c(t)$, is sampled by a sample-and-hold. This signal is then processed by the ΔΣ modulator, which converts the analog signal into a noise-shaped low-resolution digital signal. The third block in the system is a decimator. It converts the oversampled low-resolution digital signal into a high-resolution digital signal at a lower sampling rate usually equal to twice the frequency of the desired bandwidth of the input signal. The decimation filter can be conceptually thought of as a low-pass filter followed by a down sampler, although in many systems the decimation is performed in a number of stages. It should be mentioned that in many realizations where the ΔΣ modulator is realized using switched-capacitor circuitry, a separate sample-and-hold is not required, as the continuous-time signal is inherently sampled by the switches and input capacitors of the SC ΔΣ. In the next few sections the operation of the various building blocks will be described in greater detail.

Noise-Shaped Delta-Sigma Modulator

A general noise-shaped delta-sigma (ΔΣ) modulator and its linear model are shown in Fig. 14.6. This arrangement is known as an interpolative structure and is analogous to an amplifier realized using an opamp and feedback. In this analogy, the feedback reduces the effect of the noise of the output stage of the opamp in the closed-loop amplifier's output signal at low frequencies when the opamp gain is high. At high frequencies, when the opamp's gain is low, the noise is not reduced. Note that the quan-

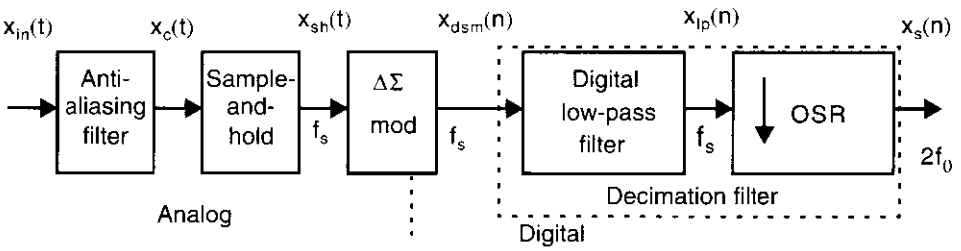


Fig. 14.5 Block diagram of an oversampling A/D converter.

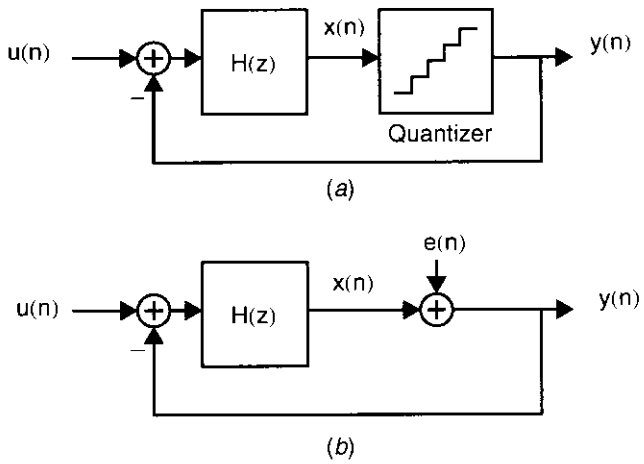


Fig. 14.6 A modulator and its linear model: (*a*) a general $\Delta\Sigma$ modulator (interpolator structure); (*b*) linear model of the modulator showing injected quantization noise.

tizer here is shown for the general case where many output levels occur. While most present oversampling converters make use of 1-bit quantizers (i.e., only two output levels) due to reasons already discussed, there is certainly no reason to restrict ourselves to such implementations. In fact, multibit oversampling converters, discussed in Section 14.8, are gaining in popularity.

Treating the linear model shown in Fig. 14.6(*b*) as having two *independent* inputs (which is an approximation), we can derive a signal transfer function, $S_{TF}(z)$, and a noise transfer function, $N_{TF}(z)$.

$$S_{TF}(z) \equiv \frac{Y(z)}{U(z)} = \frac{H(z)}{1 + H(z)} \tag{14.15}$$

$$N_{TF}(z) \equiv \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} \tag{14.16}$$

Note that the zeros of the noise transfer function, $N_{TF}(z)$, will be equal to the poles of $H(z)$. In other words, when $H(z)$ goes to infinity, we see by (14.16) that $N_{TF}(z)$ will go to zero. We can also write the output signal as the combination of the input signal and the noise signal, with each being filtered by the corresponding transfer function. In the frequency domain, we have

$$Y(z) = S_{TF}(z)U(z) + N_{TF}(z)E(z) \tag{14.17}$$

To noise-shape the quantization noise in a useful manner, we choose $H(z)$ such that its magnitude is large from 0 to f_0 (i.e., over the frequency band of interest). With such a choice, the signal transfer function, $S_{TF}(z)$, will approximate unity over the frequency band of interest very similarly to an opamp in a unity-gain feedback configuration. Furthermore, the noise transfer function, $N_{TF}(z)$, will approximate zero over the same band. Thus, the quantization noise is reduced over the frequency band

of interest while the signal itself is largely unaffected. The high-frequency noise is not reduced by the feedback as there is little loop gain at high frequencies. However, additional post filtering can remove the out-of-band quantization noise with little effect on the desired signal.

Before choosing specific functions for $H(z)$, note that the maximum level of the in-band input signal, $u(n)$, must remain within the maximum levels of the feedback signal, $y(n)$; otherwise the large gain in $H(z)$ will cause the signal $x(n)$ to saturate. For example, if a 1-bit quantizer having output levels of ± 1 is used, the input signal must also remain within ± 1 for frequencies where the gain of $H(z)$ is large. In fact, for many modulators the input signal needs to be significantly smaller than the bounds of the quantizer output levels to keep the modulator *stable.*[3] However, the maximum level of the input signal, $u(n)$, for frequencies where the gain of $H(z)$ is small will not necessarily cause the signal $x(n)$ to saturate. In other words, the maximum level of the out-of-band input signal can be quite a bit larger than the feedback levels (see Problem 14.4).

First-Order Noise Shaping

To realize first-order noise shaping, the noise transfer function, $N_{TF}(z)$, should have a zero at dc (i.e., $z = 1$) so that the quantization noise is high-pass filtered. Since the zeros of $N_{TF}(z)$ are equal to the poles of $H(z)$, we can obtain first-order noise shaping by letting $H(z)$ be a discrete-time integrator (i.e., have a pole at $z = 1$).[4] Specifically,

$$H(z) = \frac{1}{z-1} \tag{14.18}$$

A block diagram for such a choice is shown in Fig. 14.7.

Time Domain View From a time domain point of view, if the feedback is operating correctly and the system is stable, then the signal $x(n)$ is bounded (i.e., $\neq \infty$). Since the integrator has infinite dc gain, the *average value of the discrete-time integrator's input must exactly equal zero* (i.e., average value of $u(n) - y(n)$ equals zero). This

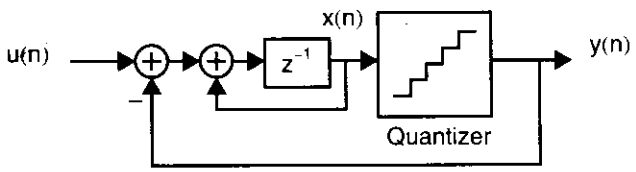


Fig. 14.7 A first-order noise-shaped interpolative modulator.

3. A modulator is defined to be stable if the input to the quantizer does not become so large as to cause the quantizer error to become greater than $\pm\Delta/2$ (which is referred to as overloading the quantizer). See Section 14.7.

4. A continuous-time integrator can also be used, but discrete-time integrators are more popular in integrated realizations as they are less sensitive to sampling jitter and have better distortion characteristics.

result implies that the average value (i.e., dc value) of $u(n)$ must equal the average value (i.e., dc value) of $y(n)$.

Again, the similarity of this configuration and an opamp having unity-gain feedback is emphasized. The open-loop transfer function of an opamp is closely approximated by a first-order integrator having very large gain at low frequencies.

EXAMPLE 14.4

Find the output sequence and state values for a dc input, $u(n)$, of $1/3$ when a two-level quantizer of ± 1.0 is used (threshold at zero) and the initial state for $x(n)$ is 0.1.

Solution

The output sequence and state values are given in Table 14.2.

Table 14.2 First-order modulator example

n	x(n)	x(n + 1)	y(n)	e(n)
0	0.1	–0.5667	1.0	0.9
1	–0.5667	0.7667	–1.0	–0.4333
2	0.7667	0.1	1.0	0.2333
3	0.1	–0.5667	1.0	0.9
4	–0.5667	0.7667	–1.0	–0.4333
5	...	...	...	...

Note that the average of $y(n)$ exactly equals $1/3$ as expected. However, also note that the output pattern is periodic, which implies that the quantization noise is not random in this example. (However, the result is much more satisfying than applying $1/3$ directly into a 1-bit quantizer using straight oversampling, which would give all 1s as its output.)

Frequency Domain View From a frequency domain view, the signal transfer function, $S_{TF}(z)$, is given by

$$S_{TF}(z) = \frac{Y(z)}{U(z)} = \frac{1/(z-1)}{1+1/(z-1)} = z^{-1} \tag{14.19}$$

and the noise transfer function, $N_{TF}(z)$, is given by

$$N_{TF}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+1/(z-1)} = (1-z^{-1}) \tag{14.20}$$

We see here that the signal transfer function is simply a delay, while the noise transfer function is a discrete-time differentiator (i.e., a high-pass filter).

To find the magnitude of the noise transfer function, $|N_{TF}(f)|$, we let $z = e^{j\omega T} = e^{j2\pi f/f_s}$ and write the following:

$$N_{TF}(f) = 1 - e^{-j2\pi f/f_s} = \frac{e^{j\pi f/f_s} - e^{-j\pi f/f_s}}{2j} \times 2j \times e^{-j\pi f/f_s}$$
$$= \sin\left(\frac{\pi f}{f_s}\right) \times 2j \times e^{-j\pi f/f_s} \tag{14.21}$$

Taking the magnitude of both sides, we have the high-pass function

$$|N_{TF}(f)| = 2\sin\left(\frac{\pi f}{f_s}\right) \tag{14.22}$$

Now the quantization noise power over the frequency band from 0 to f_0 is given by

$$P_e = \int_{-f_0}^{f_0} S_e^2(f)|N_{TF}(f)|^2\,df = \int_{-f_0}^{f_0}\left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}\left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^2 df \tag{14.23}$$

and making the approximation that $f_0 << f_s$ (i.e., OSR >> 1), so that we can approximate $\sin((\pi f)/f_s)$ to be $(\pi f)/f_s$, we have

$$P_e \cong \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^2}{3}\right)\left(\frac{2f_0}{f_s}\right)^3 = \frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3 \tag{14.24}$$

Assuming the maximum signal power is the same as that obtained before in (14.11), the maximum SNR for this case is given by

$$SNR_{max} = 10\log\left(\frac{P_s}{P_e}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left[\frac{3}{\pi^2}(OSR)^3\right] \tag{14.25}$$

or, equivalently,

$$SNR_{max} = 6.02N + 1.76 - 5.17 + 30\log(OSR) \tag{14.26}$$

We see here that doubling the OSR gives an SNR improvement for a first-order modulator of 9 dB or, equivalently, a gain of 1.5 bits/octave. This result should be compared to the 0.5 bits/octave when oversampling with no noise shaping.

Switched-Capacitor Realization of a First-Order A/D Converter

It is possible to realize a first-order modulator using switched-capacitor (SC) techniques. An example of a first-order modulator where a 1-bit quantizer is used in the feedback loop is shown in Fig. 14.8. Here, the ΔΣ modulator consists of both analog and digital circuitry. It should be mentioned that the two input capacitances to the discrete-time integrator in Fig. 14.8 can be combined to one capacitance, as shown in Fig. 14.9 [Boser, 1988]. However, such an approach does not easily allow scaling of the feedback signal relative to the input signal.

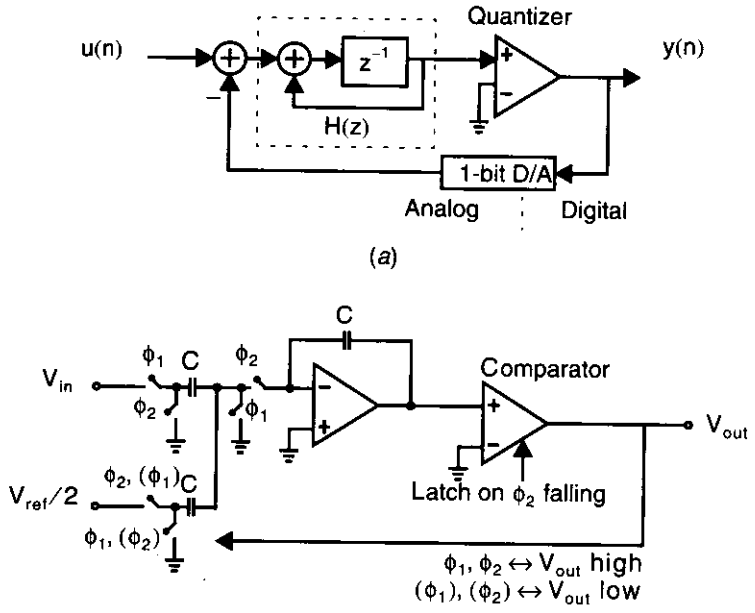


Fig. 14.8 First-order A/D modulator: (*a*) block diagram; (*b*) switched-capacitor implementation.

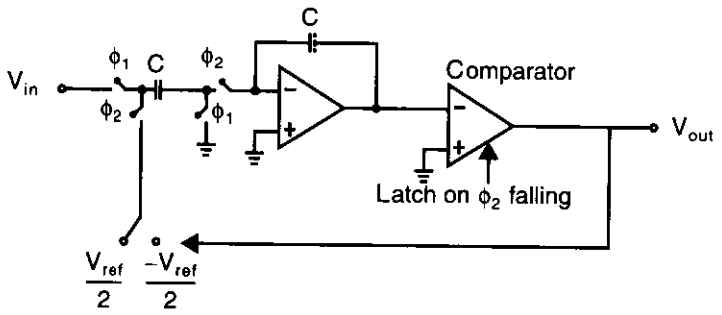


Fig. 14.9 First-order A/D modulator using only one input capacitance to the discrete-time integrator.

Second-Order Noise Shaping

The modulator shown in Fig. 14.10 realizes second-order noise shaping (i.e., the noise transfer function, $N_{TF}(z)$, is a second-order high-pass function). For this modulator, the signal transfer function is given by

$$S_{TF}(f) = z^{-1} \tag{14.27}$$

and the noise transfer function is given by

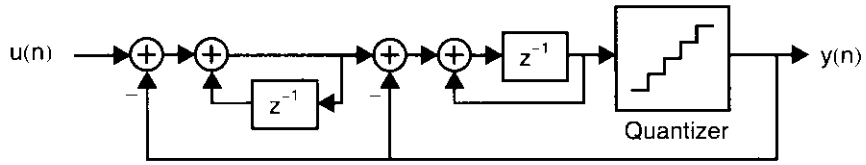


Fig. 14.10 Second-order ΔΣ modulator.

$$N_{TF}(f) = (1 - z^{-1})^2 \tag{14.28}$$

Additionally, the magnitude of the noise transfer function can be shown to be given by

$$|N_{TF}(f)| = \left[2 \sin\left(\frac{\pi f}{f_s}\right)\right]^2 \tag{14.29}$$

resulting in the quantization noise power over the frequency band of interest being given by

$$P_e \cong \frac{\Delta^2 \pi^4}{60}\left(\frac{1}{OSR}\right)^5 \tag{14.30}$$

Again, assuming the maximum signal power is that obtained in (14.11), the maximum SNR for this case is given by

$$SNR_{max} = 10 \log\left(\frac{P_s}{P_e}\right) = 10 \log\left(\frac{3}{2} 2^{2N}\right) + 10 \log\left[\frac{5}{\pi^4}(OSR)^5\right] \tag{14.31}$$

or, equivalently,

$$SNR_{max} = 6.02N + 1.76 - 12.9 + 50 \log(OSR) \tag{14.32}$$

We see here that doubling the OSR improves the SNR for a second-order modulator by 15 dB or, equivalently, a gain of 2.5 bits/octave.

The realization of the second-order modulator using switched-capacitor techniques is straightforward and is left as an exercise for the interested reader.

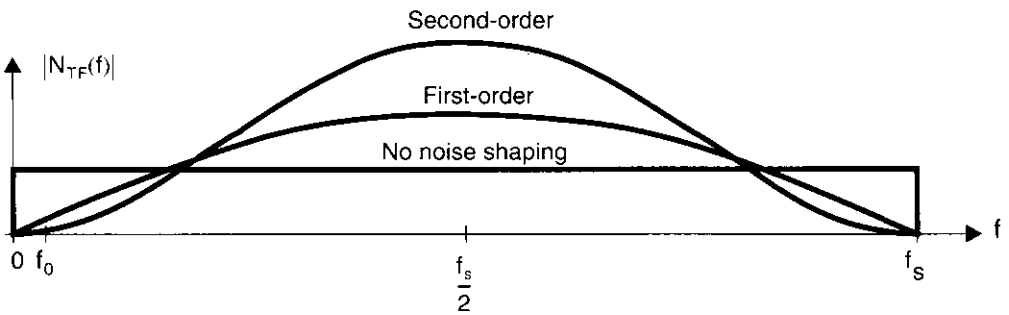


Fig. 14.11 Some different noise-shaping transfer functions.

Noise Transfer-Function Curves

The general shape of zero-, first-, and second-order noise-shaping curves are shown in Fig. 14.11. Note that over the band of interest (i.e., from 0 to f_0), the noise power decreases as the noise-shaping order increases. However, the out-of-band noise increases for the higher-order modulators.

EXAMPLE 14.5

Given that a 1-bit A/D converter has a 6-dB SNR, what sample rate is required to obtain a 96-dB SNR (or 16 bits) if $f_0 = 25$ kHZ for straight oversampling as well as first- and second-order noise shaping?

Solution

Oversampling with No Noise Shaping From before, straight oversampling requires a sampling rate of 54,000 GHz.

First-Order Noise Shaping First-order noise shaping gives 9 dB/octave where 1 octave is doubling the OSR. Since we lose 5 dB, we require 95 dB divided by 9 dB/octave, or 10.56 octaves. Thus, the required sampling rate, f_s, is

$$f_s = 2^{10.56} \times 2f_0 \cong 75 \text{ MHz}$$

This compares very favorably with straight oversampling, though it is still quite high.

Second-Order Noise Shaping Second-order noise shaping gives 15 dB/octave, but loses 13 dB. Thus we required 103 dB divided by 15 dB/octave, resulting in a required sampling rate of only 5.8 MHz. However, this simple calculation does not take into account the reduced input range for a second-order modulator needed for stability.

Quantization Noise Power of 1-bit Modulators

Assuming the output of a 1-bit modulator is ± 1, then one can immediately determine the total power of the output signal, $y(n)$, to be a normalized power of 1 watt. Since $y(n)$ consists of both signal and quantization noise, it is clear that the signal power can never be greater than 1 watt. In fact, as alluded to earlier, the signal level is often limited to well below the ± 1 level in higher-order modulators to maintain stability. For example, assuming that the maximum peak signal level is only ± 0.25, then the maximum signal power is 62.5 mW. And since the signal power plus quantization noise power equals 1 W, the maximum signal power is about 12 dB below

the quantization noise power. Fortunately, as we saw above, the quantization noise power is mostly in a different frequency region than the signal power and can therefore be filtered out. Note, however, that the filter must have a dynamic range capable of accommodating the full power of $y(n)$ at its input. For a $\Delta\Sigma$ A/D converter, the filtering would be done by digital filters following the quantizer.

Error-Feedback Structure

Before leaving this section, it is of interest to look at another structure for realizing a delta-sigma modulator—an error-feedback structure, as shown in Fig. 14.12 [Anastassiou, 1989]. Using a linear model for the quantizer, it is not difficult to show that this error-feedback structure has a signal transfer function, $S_{TF}(z)$, equal to unity while the noise transfer function, $N_{TF}(z)$, equals $G(z)$. Thus for a first-order modulator, $G(z) = 1 - z^{-1}$, or in other words, the block $(G(z) - 1)$ is simply $-z^{-1}$.

Unfortunately, a slight coefficient error can cause significant noise-shaping degradation with this error-feedback structure. For example, in a first-order case, if the delayed signal becomes $-0.99z^{-1}$ (rather than $-z^{-1}$), then $G(z) = 1 - 0.99z^{-1}$, and the zero is moved off dc. Such a shift of the zero will result in the quantization noise not being fully nulled at dc and therefore would not be suitable for high oversampling ratios. Thus, this structure is not well suited to analog implementations where coefficient mismatch occurs. In contrast, an interpolative structure has the advantage that the zeros of the noise transfer function remain at dc as long as $H(z)$ has infinite gain at dc. This high gain at dc can usually be obtained in analog implementations by using opamps with large open-loop gains and does not rely on component matching. The error feedback structure is discussed here because it is useful for analysis purposes and can work well for fully digital implementations where no coefficient mismatches occur.

A second-order modulator based on the error-feedback structure is shown in Fig. 14.13. For this case we have

$$G(z) - 1 = z^{-1}(z^{-1} - 2) \tag{14.33}$$

implying that

$$\begin{aligned} G(z) &= 1 - 2z^{-1} + z^{-2} \\ &= (1 - z^{-1})^2 \end{aligned} \tag{14.34}$$

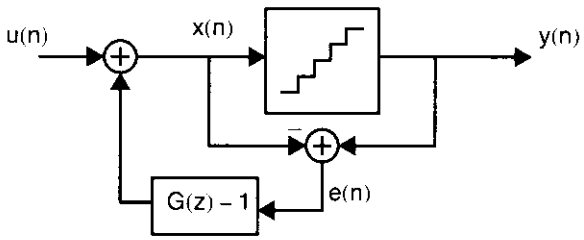


Fig. 14.12 The error-feedback structure of a general $\Delta\Sigma$ modulator.

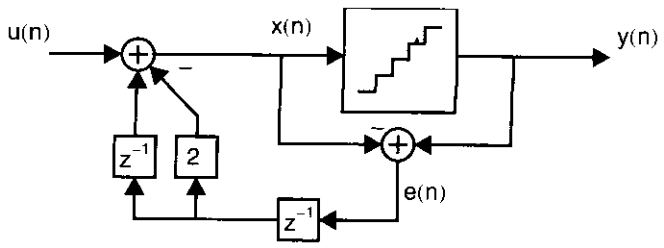


Fig. 14.13 The error-feedback structure of a second-order ΔΣ modulator.

which is identical to (14.28), and we see that second-order noise shaping is obtained. In practical realizations, one might have to take into account additional details such as preventing overflow and reducing complexity. For these more advanced topics, the reader is referred to [Temes, 1996].

14.3 SYSTEM ARCHITECTURES

In this section, we look at typical system architectures for oversampled A/D and D/A converters.

System Architecture of Delta-Sigma A/D Converters

The system architecture for a typical ΔΣ oversampling A/D converter is shown in Fig. 14.14, and some example signal spectra are shown in Fig. 14.15. In the case of digital audio, various sampling frequencies might be f_s = 5.6448 MHz, f_0 = 44.1 kHz, which represent an oversampling ratio of 128. Here, the input signal, $x_c(t)$, is sampled and held,[5] resulting in the signal $x_{sh}(t)$. This sampled-and-held signal is then applied to an A/D ΔΣ modulator, which has as its output a 1-bit digital signal $x_{dsm}(n)$. This 1-bit digital signal is assumed to be linearly related to the input signal

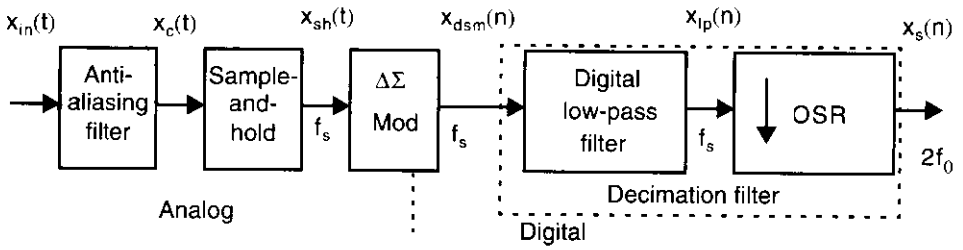


Fig. 14.14 Block diagram of an oversampling A/D converter.

5. This sample-and-hold block is often inherent in the switched-capacitor modulator. Thus, the signal $x_{sh}(t)$ may never physically exist in many realizations.

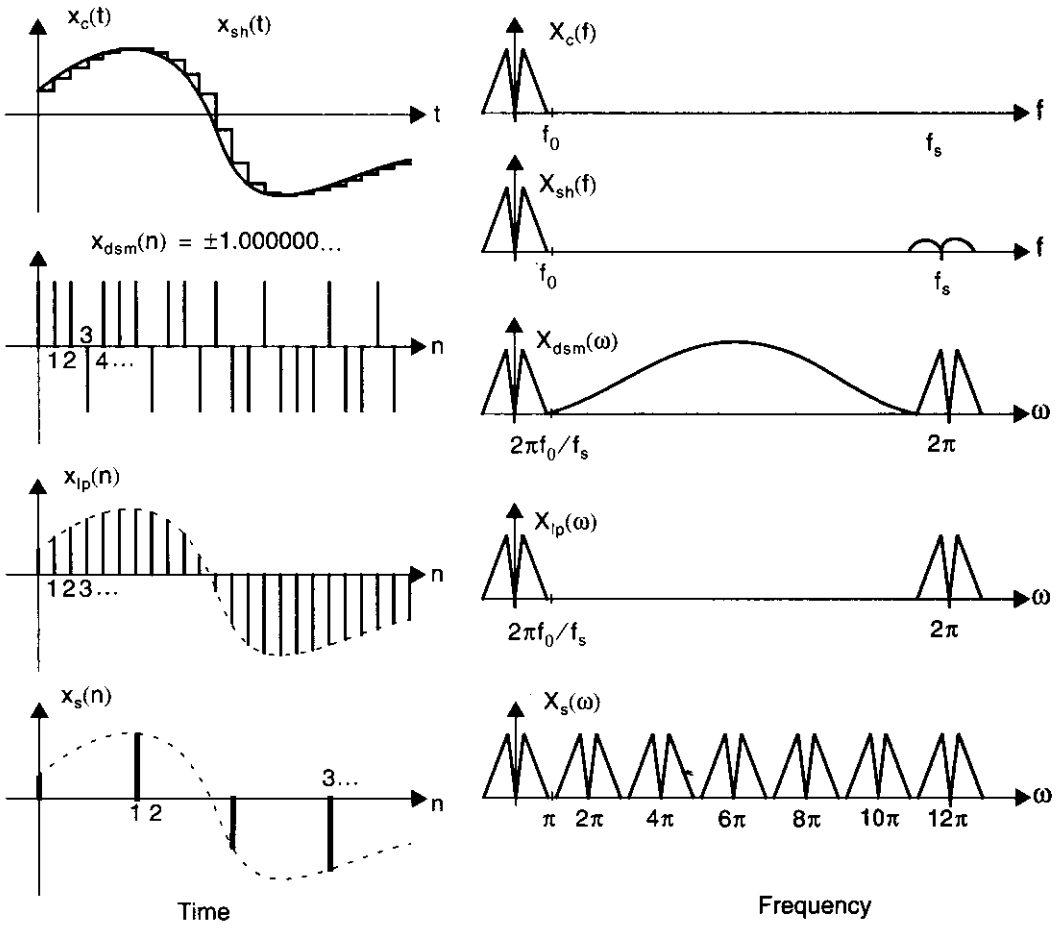


Fig. 14.15 Signals and spectra in an oversampling A/D converter.

$x_c(t)$ (accurate to many bits of resolution), although it includes a large amount of out-of-band quantization noise. To remove this out-of-band quantization noise, a digital decimation filter is used as shown. Conceptually, one can think of the decimation process as first reducing the quantization noise through the use of a digital low-pass filter, resulting in the multi-bit signal $x_{lp}(n)$. Note that this low-pass filter will also remove any higher-frequency signal content that was originally on the input signal, $x_c(t)$, and thus also acts as an anti-aliasing filter to limit signals to one-half the final output sampling rate, $2f_0$, as opposed to the anti-aliasing filter at the input, which needed to only limit signals to frequencies less than $f_s/2$. Next, $x_{lp}(n)$ is resampled at $2f_0$ to obtain $x_s(n)$ by simply keeping samples at a submultiple of the oversampling rate and throwing away the rest. In Fig. 14.15 an oversampling rate of only 6 is shown for clarity as opposed to the more typical values of 64 or 128 that are used in many commercial applications. This decimation process does not result in any loss of information, since the bandwidth of the original signal was assumed to be f_0. In other words, the signal

$x_{lp}(n)$ has redundant information since it is an oversampled signal where all of its spectral information lies well below π, and by throwing away samples, the spectral information is spread over 0 to π. Finally, it should be noted that there is no need to actually create the signal $x_{lp}(n)$, and much digital circuit complexity can be saved by combining the digital low-pass filter with the resampling block to directly produce the downsampled signal $x_s(n)$, as discussed in Section 14.4: The final signal, $x_s(n)$, would typically have 16-bit resolution in digital audio applications.

It is of interest to look at what element most strongly affects the linearity of this oversampling A/D system. Returning to the $\Delta\Sigma$ modulator, note that an internal 1-bit D/A converter is used whose output signal is combined with the input signal such that, over the frequency band of interest, these two signals are nearly the same. As a result, the overall linearity of this $\Delta\Sigma$ modulator converter depends strongly on the linearity of its internal D/A converter. For example, with a nonlinear internal D/A converter and a slow linear ramp input signal, the low-frequency content of the D/A converter's output would essentially equal that ramp. However, the low-frequency content of the digital input to the D/A converter would be a nonlinear ramp to account for the D/A converter's nonlinearity. Since the remaining digital circuitry is linear, the overall linearity of this oversampling A/D converter is most strongly dependent on realizing a linear D/A converter inside the $\Delta\Sigma$ modulator. In fact, nonlinearities in the internal A/D converter (if it was multi-bit) have only a small effect on the linearity of the overall converter, since the high gain in the feedback loop compensates for that nonlinearity.

System Architecture of Delta-Sigma D/A Converters

Most of the discussion so far has focused on $\Delta\Sigma$ A/D converters, but much of it also applies to $\Delta\Sigma$ D/A converters, with a few qualifications. A high-resolution oversampling D/A converter using a 1-bit converter can be realized as shown in the block diagram in Fig. 14.16. Some illustrative signals that might occur in this system are shown in Fig. 14.17. The digital input signal, $x_s(n)$, is a multi-bit signal and has an equivalent sample rate of $2f_0$, where f_0 is slightly greater than the highest input signal frequency. For example, in a compact disc audio application, a 16-bit input signal is used with a frequency band of interest from 0 to 20 kHz while the sample rate, $2f_0$,

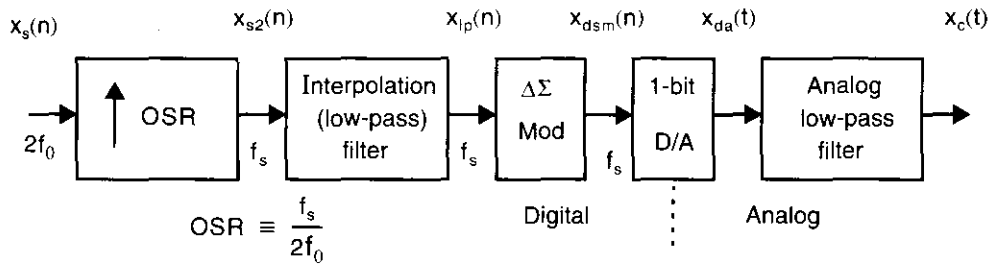


Fig. 14.16 Block diagram of a 1-bit oversampling D/A converter.

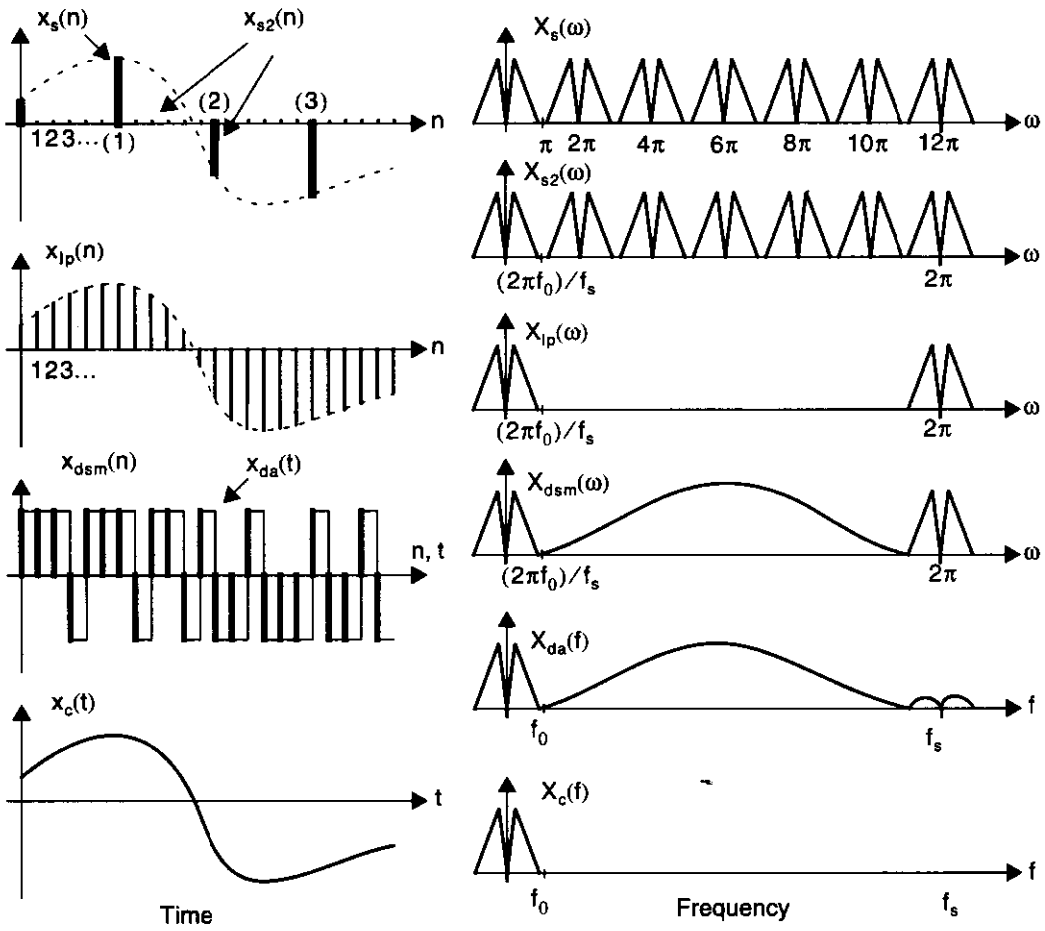


Fig. 14.17 Signals and spectra in an oversampling D/A converter.

is 44.1 kHz. Note, however, that $x_s(n)$ is actually just a series of numbers and thus its shown frequency spectrum has normalized the sample rate to 2π. Next, the input signal is upsampled to an equivalent higher sampling rate, f_s, resulting in the upsampled signal $x_{s2}(n)$. In the example shown, the oversampling rate is only six (i.e., $f_s = 6 \times 2f_0$), while in typical audio applications, f_s is often near a 5-MHz rate (i.e., oversampling rate of 128). However, $x_{s2}(n)$ has large images left in its signal so an interpolation filter is used to create the multi-bit digital signal, $x_{lp}(n)$, by digitally filtering out the images. This interpolation filter is effectively a digital brick-wall-type filter that passes 0 to $(2\pi f_0)/f_s$ and rejects all other signals. The resulting signal, $x_{lp}(n)$, is then applied to a fully digital $\Delta\Sigma$ modulator that produces a 1-bit output signal, $x_{dsm}(n)$, which has a large amount of shaped quantization noise. As discussed earlier, the main reason for going to a 1-bit digital signal is so that a 1-bit D/A converter can now be used to create $x_{da}(t)$, which has excellent linearity properties but still a large amount of out-of-band quantization noise. Finally, the desired output sig-

nal, $x_c(t)$, can be obtained by using an analog filter to filter out this out-of-band quantization noise. The analog filter may be a combination of switched-capacitor and continuous-time filtering.

Some points to note here are that while oversampling allows the use of a 1-bit D/A converter, which can have excellent linearity, the use of oversampling also relaxes some of the analog-smoothing filter specifications. For example, if a 16-bit converter was used at the Nyquist rate, $2f_0$, the analog-smoothing filter would have to remove the images in the signal instead of a precise digital interpolation filter removing these images. This specification can be very demanding, as in a digital-audio application, where a near 96-dB attenuation is required at 24 kHz, while up to 20 kHz should pass with unity gain. With the use of an oversampling approach, the digital interpolation filter is faced with this strict specification rather than an analog smoothing filter. In fact, oversampling is often used in audio applications with multi-bit D/A converters just to reduce this analog-smoothing filter's complexity.

Another point to note is that the order of the analog low-pass filter should be at least one order higher than that of the $\Delta\Sigma$ modulator. The reason for this choice is that if the analog filter's order is equal to that of the modulator, the slope of the rising quantization noise will match the filter's falling attenuation, and thus the resulting quantization noise will be approximately a constant spectral density up to one-half the sampling rate (i.e., $f_s/2$). By having a higher-order analog filter, the spectral density of the output signal's quantization noise will have a bandwidth similar to the analog filter's bandwidth, which is around f_0.

Finally, note that the analog filter must be able to strongly attenuate high-frequency noise, as much of the quantization noise is centered around $f_s/2$, and this analog filter should be linear so it does not modulate the noise back to the frequency band of interest. In many applications, the realization of these filters, especially if they are integrated, is nontrivial.

14.4 DIGITAL DECIMATION FILTERS

There are many techniques for realizing digital decimation filters for oversampling A/D converters. In this section, we discuss two popular approaches—multi-stage and single-stage.

Multi-Stage

One method for realizing decimation filters is to use a multi-stage approach, as shown in Fig. 14.18. Here, the first-stage FIR filter, $T_{sinc}(z)$, removes much of the quantization noise such that its output can be downsampled to four times the Nyquist rate (i.e., $8f_0$). This lower-rate output is applied to the second-stage filter, which may be either an IIR filter, as shown in Fig. 14.18(*a*), or a cascade of FIR filters, as shown in Fig. 14.18(*b*).

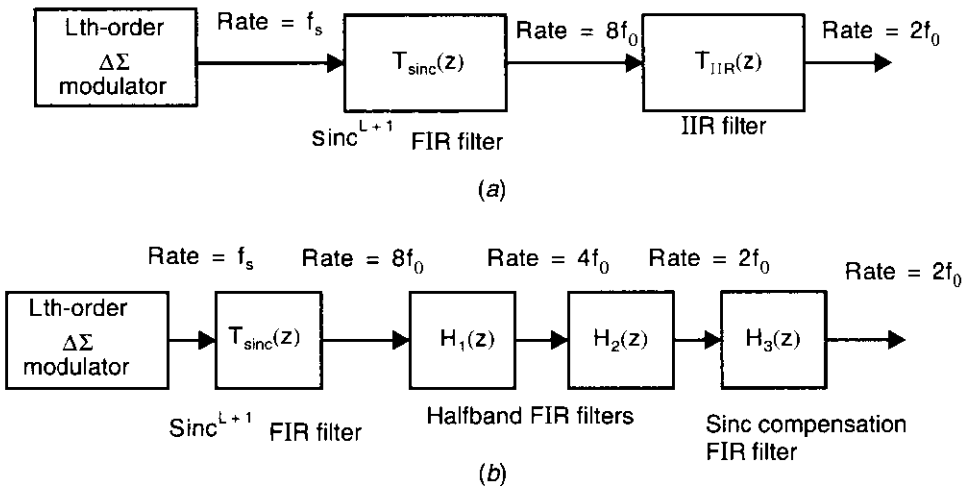


Fig. 14.18 Multi-stage decimation filters: (*a*) sinc followed by an IIR filter; (*b*) sinc followed by halfband filters.

The sinc^{L+1} FIR filter is a cascade of $L + 1$ averaging filters where the transfer function of a single averaging filter, $T_{avg}(z)$, is given by

$$T_{avg}(z) = \frac{Y(z)}{U(z)} = \frac{1}{M}\sum_{i=0}^{M-1} z^{-i} \tag{14.35}$$

and M is the integer ratio of f_s to $8f_0$ (i.e., $8f_0 = f_s/M$). Note that the impulse response of this filter is finite, implying it is an FIR-type filter. In addition, all of its impulse response coefficients are symmetric (in fact, they are all equal), and thus it is also a linear-phase filter.[6] Finally, note that the $1/M$ multiplication term is easily realized by changing the location of the fractional bits when M is chosen to be a power of two.

As an illustration of a series of averaging filters reducing quantization noise, consider an average-of-four filter (i.e., $M = 4$) operating on the output of the 1-bit signal in Example 14.4. Since the output 1-bit sequence is $\{1, 1, -1, 1, 1, -1, 1, 1, -1, \ldots\}$, the first averaged output, $x_{lp1}(n)$, would be given by

$$x_{lp1}(n) = \{0.5, 0.5, 0.0, 0.5, 0.5, 0.0, \ldots\}$$

To obtain more attenuation of the quantization noise, the signal $x_{lp1}(n)$ can also be applied to a running-average-of-four filter, giving $x_{lp2}(n)$ as

$$x_{lp2}(n) = \{0.375, 0.375, 0.25, 0.375, 0.375, 0.25, \ldots\}$$

and repeating this process to get $x_{lp3}(n)$ would give

$$x_{lp3}(n) = \{0.344, 0.344, 0.313, 0.344, 0.344, 0.313, \ldots\}$$

6. A linear-phase filter results in all frequency components being delayed by the same amount and is therefore desirable in applications where phase distortion is unwanted (such as hi-fi audio).

Note the convergence of these sequences to a series of all samples equalling 1/3 as expected.

To show that the frequency response of an averaging filter, $T_{avg}(z)$, has a sinc-type behavior, it is useful to rewrite (14.35) as

$$MY(z) = \left(\sum_{i=0}^{M-1} z^{-i}\right)U(z) = (1 + z^{-1} + z^{-2} + \cdots + z^{-(M-1)})U(z) \tag{14.36}$$

which can also be rewritten as

$$\begin{aligned} MY(z) &= (z^{-1} + z^{-2} + \cdots + z^{-M})U(z) + (1 - z^{-M})U(z) \\ &= Mz^{-1}Y(z) + (1 - z^{-M})U(z) \end{aligned} \tag{14.37}$$

Finally, we group together $Y(z)$ terms and find the transfer function of this averaging filter can also be written in the recursive form as

$$T_{avg}(z) = \frac{Y(z)}{U(z)} = \frac{1}{M}\left(\frac{1 - z^{-M}}{1 - z^{-1}}\right) \tag{14.38}$$

The frequency response for this filter is found by substituting $z = e^{j\omega}$, which results in

$$T_{avg}(e^{j\omega}) = \frac{\text{sinc}\left(\frac{\omega M}{2}\right)}{\text{sinc}\left(\frac{\omega}{2}\right)} \tag{14.39}$$

where $\text{sinc}(x) \equiv \sin(x)/x$.

A cascade of $L + 1$ averaging filters has the response $T_{sinc}(z)$ given by

$$T_{sinc}(z) = \frac{1}{M^{L+1}}\left(\frac{1 - z^{-M}}{1 - z^{-1}}\right)^{L+1} \tag{14.40}$$

The reason for choosing to use $L + 1$ of these averaging filters in cascade is similar to the argument that the order of the analog low-pass filter in an oversampling D/A converter should be higher than the order of the $\Delta\Sigma$ modulator. Specifically, the slope of the attenuation for this low-pass filter should be greater than the rising quantization noise, so that the resulting noise falls off at a relatively low frequency. Otherwise, the noise would be integrated over a very large bandwidth, usually causing excessive total noise.

An efficient way to realize this cascade-of-averaging filters is to write (14.40) as

$$T_{sinc}(z) = \left(\frac{1}{1 - z^{-1}}\right)^{L+1}(1 - z^{M})^{L+1}\frac{1}{M^{L+1}} \tag{14.41}$$

and thus realize it as shown in Fig. 14.19 [Candy, 1992]. A point to note here is that at first glance it appears as though this circuit will not operate properly due to a dc input

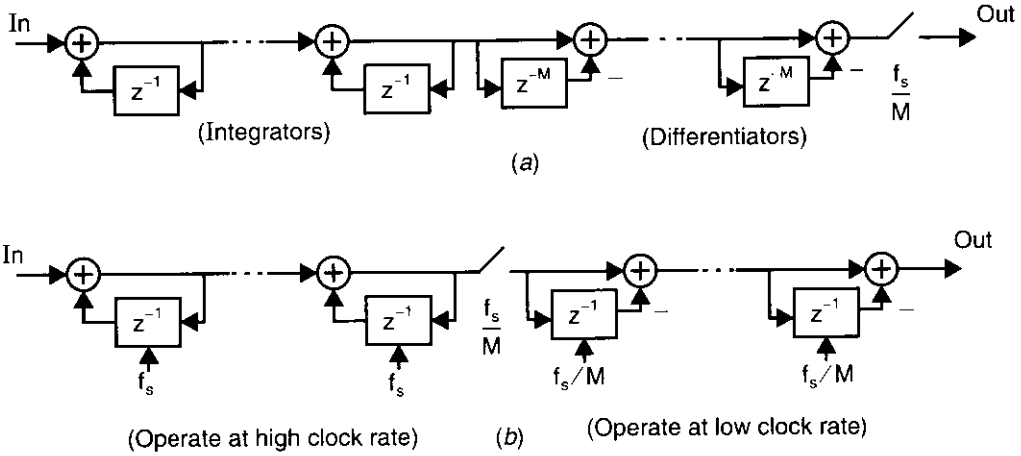


Fig. 14.19 Realizing $T_{sinc}(z)$ as a cascade of integrators and differentiators: (*a*) downsampling performed after all the filtering; (*b*) a more efficient method where downsampling is done before the differentiators.

causing saturation of the discrete-time integrators. Fortunately, such a result does not occur when 2's-complement arithmetic is used due to its wrap-around characteristic. Specifically, although the dc levels at the integrator outputs may be incorrect, the differentiators compare the present sample with that of M samples past while rejecting the dc component. Thus, as long as this difference is properly maintained (as it would be using 2's-complement arithmetic) the correct calculation is performed.

Referring once again to Fig. 14.18, the purpose of the filters following the $T_{sinc}(z)$ filter is twofold. One reason for their use is to remove any higher-frequency input signals (in effect, a sharp anti-aliasing filter) before the signal is downsampled to the final Nyquist rate (i.e., $2f_0$). In other words, while the $T_{sinc}(z)$ filter is good at filtering out the quantization noise, it is not sharp enough to act as a reasonable anti-aliasing filter for input signals slightly higher than f_0. A second reason is to compensate for the frequency drop in the passband caused by the $T_{sinc}(z)$ filter. This anti-aliasing and sinc-compensation filter might be realized using a single IIR filter, as shown in Fig. 14.18(*a*). Alternatively, a few halfband FIR filters might be used together with a separate sinc-compensation FIR filter, as shown in Fig. 14.18(*b*). A halfband FIR filter has a passband from 0 to $\pi/2$, while its stopband is from $\pi/2$ to π with every second coefficient being zero [Vaidyanathan, 1993]. Thus, with a high enough filter order, its output can be downsampled by a factor of two. It has also been shown that in some applications, these halfband and sinc-compensation filters can be realized using no general multi-bit multipliers [Saramaki, 1990].

Single Stage

Another approach for realizing decimation filters is to use a relatively high-order FIR filter. For example, in [Dattorro, 1989], a 2048 tap FIR filter was used to decimate

1-bit stereo outputs from two $\Delta\Sigma$ modulators, each having an oversampling ratio of 64. While this FIR order seems high, note that no multi-bit multiplications are needed, since the input signal is simply 1-bit, so all multiplications are trivial. In addition, the output need only be calculated at the Nyquist rate (intermediate samples would be discarded anyway) such that 2048 additions are required during one clock cycle at the Nyquist rate. However, if only one accumulator is used to perform all 2048 additions, the clock rate of that accumulator would be 2048 times the Nyquist rate. For example, if the Nyquist rate is 48 kHz, the single accumulator would have to be clocked at 98.3 MHz. To overcome this high clock rate, 32 separate FIR filters are realized (with shared coefficients) in a time-interleaved fashion, with each FIR having 2048 coefficients and each producing an output at a clock rate of 1.5 kHz. In this way, each of the 32 FIR filters uses a single accumulator operating at 3 MHz (i.e., 2048 times 1.5 kHz). The coefficient ROM values were shared between the FIR filters (as well as in the two stereo channels), and the ROM size can also be halved if coefficients are duplicated, as in the case of linear-phase FIR filtering.

Finally, it is also possible to reduce the number of additions by grouping together input bits. For example, if 4 input bits are grouped together, then a 16-word ROM lookup table can be used rather than using 3 additions. With such a grouping of input bits, each of the 32 FIR filters would require only 512 additions.

14.5 HIGHER-ORDER MODULATORS

In general, it can be shown that an Lth-order noise-shaping modulator improves the SNR by $6L + 3$ dB/octave, or equivalently, $L + 0.5$ bits/octave. In this section, we look at two approaches for realizing higher-order modulators—interpolative and MASH. The first approach is typically a single high-order structure with feedback from the quantized signal. The second approach consists of a cascade of lower-order modulators, where the latter modulators are used to cancel the noise errors introduced by the earlier modulators.

Interpolative Architecture

As discussed earlier, when compared to the error-feedback structure, the interpolative structure of Fig. 14.6(*a*) is much better suited to analog implementations of modulators due to its reduced sensitivity. One of the first approaches for realizing higher-order interpolative modulators was presented in [Chao, 1990]. It used a filtering structure very similar to a direct-form filter structure; however, a direct-form-type structure made it sensitive to component variations, which can cause the zeros of the noise transfer function to move off the unit circle. To improve component sensitivity, resonators can be used together with a modified interpolative structure, as shown in Fig. 14.20 [Ferguson, 1991]. Note here that a single 1-bit D/A signal is still used for feedback, and therefore its linearity will be excellent. The resonators in this structure are due to the feedback signals associated with f_1 and f_2, resulting in the placement of zeros in the noise transfer function spread over the frequency-of-interest band.

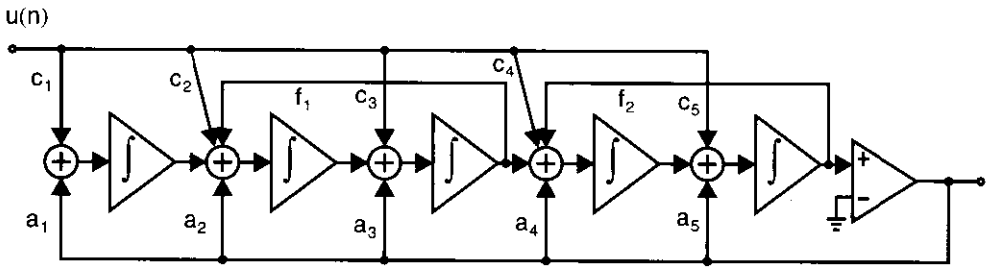


Fig. 14.20 A block diagram of a fifth-order modulator.

Such an arrangement gives better dynamic range performance than placing all the zeros at dc as we have been assuming thus far.

Unfortunately, it is possible for modulators of order two or more to go unstable, especially when large input signals are present. When they go unstable, they may never return to stability even when the large input signals go away. Guaranteeing stability for an interpolative modulator is nontrivial and is discussed further in Section 14.7.

Multi-Stage Noise Shaping (MASH) Architecture

Another approach for realizing modulators is to use a cascade-type structure where the overall higher-order modulator is constructed using lower-order ones. The advantage of this approach is that since the lower-order modulators are more stable, the overall system should remain stable. Such an arrangement has been called MASH (Multi-stAge noise SHaping) [Matsuya, 1987].

The arrangement for realizing a second-order modulator using two first-order modulators is shown in Fig. 14.21. The basic approach here is to pass along the first section's quantization error, $e_1(n)$, to another modulator and combine the outputs of both modulators in such a way that the first section's quantization noise is removed completely. The output is then left with only the second section's quantization noise, which has been filtered twice—once by the second modulator and once by the post digital circuitry. Assuming linear models for the quantizers, straightforward linear analysis gives

$$Y(z) = z^{-2}U(z) - (1 - z^{-1})^2 E_2(z) \tag{14.42}$$

Thus, a MASH approach has the advantage that higher-order noise filtering can be achieved using lower-order modulators. The lower-order modulators are much less susceptible to instability as compared to an interpolator structure having a high order with a single feedback.

Unfortunately, MASH or cascade approaches consisting of a cascade of first-order stages are sensitive to finite opamp gain and mismatches between the analog and digital circuitry. Such mismatches in the above example cause first-order noise to leak through from the first modulator and hence reduce dynamic range performance.

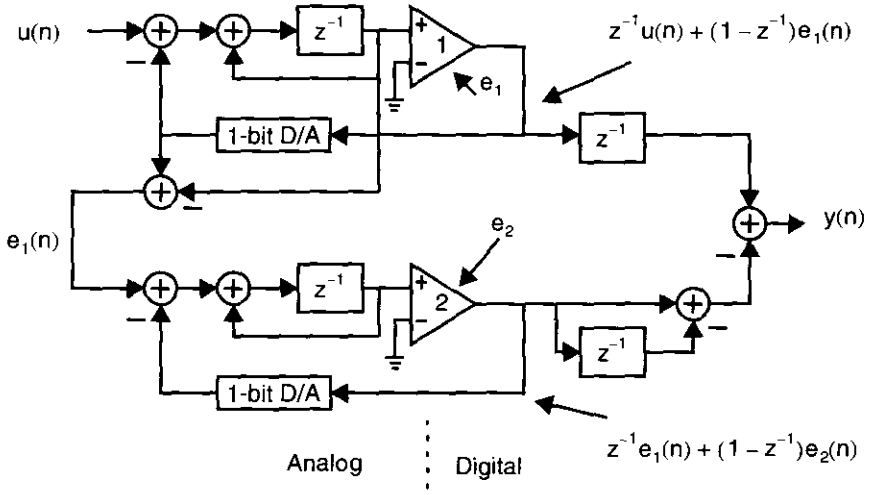


Fig. 14.21 A second-order MASH modulator using two first-order modulators. Note that the output, y(n), is a four-level signal.

To alleviate this mismatch problem, often the first stage is chosen to be a higher-order modulator such that any leak-through of its noise does not have as serious an effect as it would if this first modulator was first-order. For example, a third-order modulator would be realized using a second-order modulator for the first stage and a first-order modulator for the second stage. Also, it is very important to minimize errors due to input-offset voltages that might occur because of clock feedthrough or opamp input-offset voltages. Typically, in practical realizations additional circuit design techniques will be employed to minimize these effects.

Finally, note that the use of this MASH approach results in the digital output signal, y(n), being a four-level signal (rather than two-level) due to the combination of the original two-level signals. Such a four-level signal would require a linear four-level D/A converter in a D/A application. For A/D applications, it makes the FIR decimation filter slightly more complex.

14.6 BANDPASS OVERSAMPLING CONVERTERS

As we have seen, oversampling converters have the advantage of high linearity through the use of 1-bit conversion and reduced anti-aliasing and smoothing-filter requirements. However, at first glance some signals do not appear to easily lend themselves to oversampling approaches such as modulated radio signals. Such signals have information in only a small amount of bandwidth, say 10 kHz, but have been modulated by some higher-frequency carrier signal, say 1 MHz. For such applications, one can make use of bandpass oversampling converters.

In low-pass oversampling converters, the transfer function H(z) in Fig. 14.6 is chosen such that it has a high gain near dc, and thus quantization noise is small around

dc. In a similar way, bandpass oversampling converters are realized by choosing $H(z)$ such that it has a high gain near some frequency value, f_c, [Schreier, 1989]. With such an approach, the quantization noise is small around f_c, and thus most of the quantization noise can be removed through the use of a narrow bandpass filter of total width f_Δ following the modulator. Thus, in the case of a bandpass A/D converter intended for digital radio, post narrowband digital filtering would remove quantization noise as well as adjacent radio channels. In addition, further digital circuitry would also perform the necessary demodulation of the signal.

An important point here is that the oversampling ratio for a bandpass converter is equal to the ratio of the sampling rate, f_s, to two times the width of the narrowband filter, $2f_\Delta$, and it does not depend on the value of f_c. For example, consider a bandpass oversampling converter having a sampling rate $f_s = 4$ MHz, which is intended to convert a 10 kHz signal bandwidth centered around 1 MHz (or $f_c = f_s/4$). In this case, $f_\Delta = 10$ kHz, resulting in the oversampling ratio being equal to

$$\text{OSR} = \frac{f_s}{2f_\Delta} = 200 \tag{14.43}$$

To obtain a high gain in $H(z)$ near f_c, a similar approach to the low-pass case is taken. In a first-order low-pass oversampling converter, $H(z)$ is chosen such that it has a pole at dc (i.e., $z = 1$) and such that the noise transfer function, $N_{TF}(z)$, has a zero at dc. In a second-order bandpass oversampling converter with $f_c = f_s/4$, $H(z)$ is chosen such that it has poles at $e^{\pm j\pi/2} = \pm j$. In other words, $H(z)$ is a resonator that has an infinite gain at the frequency $f_s/4$. The zeros of the noise transfer function for this type of second-order oversampling converter are shown in Fig. 14.22, together with a similar low-pass case.

A block diagram for the example bandpass modulator is shown in Fig. 14.23, where one can derive $H(z)$ to be given by

$$H(z) = \frac{z}{z^2 + 1} \tag{14.44}$$

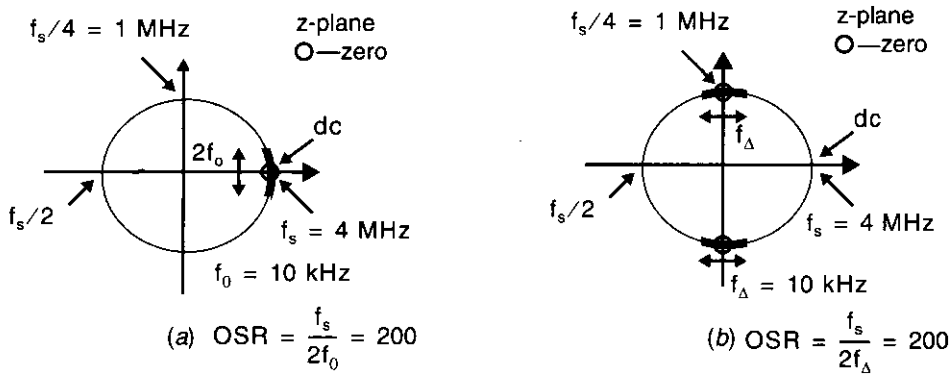


Fig. 14.22 Noise-transfer-function zeros for oversampling converters: (*a*) first-order low-pass; (*b*) second-order bandpass.

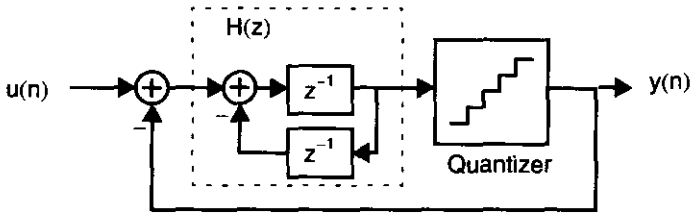


Fig. 14.23 A second-order bandpass oversampling modulator that shapes the quantization noise away from $f_s/4$.

Note that this second-order example has poles at $\pm j$, and therefore the noise transfer function, $N_{TF}(z)$, has only one zero at j and another zero at $-j$. For this reason, the dynamic range increase of a second-order bandpass converter equals that of a first-order low-pass converter that also has only one zero at dc. Specifically, the dynamic range increase of a second-order bandpass converter is 1.5 bits/octave or, equivalently, 9 dB/octave. To obtain the equivalent dynamic range increase of a second-order low-pass converter (i.e., 15 dB/octave), a fourth-order bandpass converter would have to be used. The first design of an integrated bandpass oversampling A/D converter was presented in [Jantzi, 1993].

14.7 PRACTICAL CONSIDERATIONS

Stability

As with any feedback-type system, delta-sigma modulators have the potential to go unstable. A stable modulator is defined here as one in which the input (or inputs) to the quantizer (or quantizers) remains bounded such that the quantization does not become *overloaded.* An overloaded quantizer is one in which the input signal goes beyond the quantizer's normal range, resulting in the quantization error becoming greater than $\pm\Delta/2$.

Unfortunately, the stability of higher-order 1-bit modulators is not well understood as they include a highly nonlinear element (a 1-bit quantizer), resulting in the system being stable for one input but unstable for another. As a general rule of thumb, keeping the peak frequency response gain of the noise-transfer function, $N_{TF}(z)$, less than 1.5 often results in a stable modulator [Chao, 1990].[7] In mathematical terms,

$$\left|N_{TF}(e^{j\omega})\right| \le 1.5 \qquad \text{for } 0 \le \omega \le \pi \tag{14.45}$$

should be satisfied for a 1-bit quantizer. It should be noted that this stability criterion has little rigorous justification and that there does not presently exist any necessary and sufficient stability criterion for $\Delta\Sigma$ modulators having arbitrary inputs. There is,

7. A figure of 2 was used in the reference but 1.5 appears to be a more practical choice.

however, a rigorous 1-norm stability test (which is sufficient but not necessary), but it is often too conservative, as it eliminates many "stable" modulators [Anastassiou, 1989]. For a summary of stability tests for $\Delta\Sigma$ modulators, the reader is referred to [Schreier, 1993].

It should be mentioned here that the stability of a modulator is also related to the maximum input signal level with respect to the 1-bit feedback as well as the poles of the noise transfer function. Specifically, a modulator can be made more stable by placing the poles of the system closer to the noise-transfer-function zeros. Also, a more stable modulator allows a larger maximum input signal level. However, this stability comes at a dynamic-range penalty since less of the noise power will then occur at out-of-band frequencies, but instead the noise will be greater over the in-band frequencies.

Since the stability issues of higher-order modulators are not well understood (particularly for arbitrary inputs), additional circuitry for detecting instability is often included, such as looking for long strings of 1s or 0s occurring. Alternatively, the signal amplitude at the input of the comparator might be monitored. If predetermined amplitude thresholds are exceeded for a specified number of consecutive clock cycles, then it is assumed that the converter has gone (or is going) unstable. In this case, the circuit is changed to make it more stable. One possibility is to turn on switches across the integrating capacitors of all integrators for a short time. This resets all integrator outputs to zero. A second alternative is to change the modulator into a second- or even first-order modulator temporarily by using only the first one or two integrators and resetting other integrators. Another possibility is to eliminate the comparator temporarily and feed back the input signal to the comparator. This changes the modulator into a stable filter.

Finally, it should be mentioned that modulators having multi-bit DACs appear to exhibit improved stability over their 1-bit counterparts but often require high-linearity DACs. There have been a number of architectures proposed to lessen the linearity requirements on the DACs, as described in Section 14.8.

Linearity of Two-Level Converters

It was stated earlier that 1-bit D/A converters are inherently linear since they need only produce two output values and two points define a straight line. However, as usual, practical issues limit the linearity of D/A converters having only two output levels. It should be pointed out here that most of the linearity issues discussed below are also applicable to multi-level converters, but we restrict our attention to two-level converters for clarity.

One limitation is when the two output levels somehow become functions of the low-frequency signal they are being used to create. For example, if the two voltage levels are related to power supply voltages, then these power-supply voltages might slightly rise and fall as the circuit draws more or less power. Since typically the amount of power drawn is related to the low-frequency signal being created, distortion will occur. A mechanism whereby this occurs is if a different amount of charge is being taken from the voltage references when a 1 is being output from the 1-bit D/A converter, as opposed to when a 0 is being output from the D/A converter. A somewhat

more subtle but similar mechanism can occur due to the clock feedthrough of the input switches. This feedthrough is dependent on the gate voltages driving the input switches and therefore on the power-supply voltages connected to the drivers of the input switches. It is possible that these voltages can change when more 1s than 0s are being output by the D/A converter; having well-regulated power-supply voltages on the drivers for the input switches is very important. A similar argument can be made about any clock jitter in the converter. Thus, for high linearity it is important that the two output levels and associated clock jitter not be a function of the low-frequency input signal.

A more severe linearity limitation occurs if there is memory between output levels. For example, consider the ideal and typical output signals for a two-level D/A converter, shown in Fig. 14.24. The area for each symbol is defined to be the integral of the waveform over that symbol's time period. Notice that for the typical output signal, the area is dependent on the past symbol and that difference is depicted using δ_i. As an illustrative example, consider the average voltage for three periodic patterns corresponding to average voltages of 0, 1/3, and −1/3 when V_1 and V_2 are ±1 volt.

In the ideal case, both δ_1 and δ_2 are zero as the waveform is memoryless. Thus, the three periodic patterns 0, 1/3, and −1/3 result in the following averages:

$$0: \quad \{1,-1,1,-1,1,-1,1,-1,\ldots\} \rightarrow \overline{v_a(t)} = \frac{A_1 + A_0}{2}$$

$$1/3: \quad \{1,1,-1,1,1,-1,1,1,-1,\ldots\} \rightarrow \overline{v_b(t)} = \frac{2A_1 + A_0}{3}$$

$$-1/3: \quad \{-1,-1,1,-1,-1,1,-1,-1,1,\ldots\} \rightarrow \overline{v_c(t)} = \frac{A_1 + 2A}{3}$$

By calculating the differences, $\overline{v_b(t)} - \overline{v_a(t)}$ and $\overline{v_a(t)} - \overline{v_c(t)}$, and noting that they are identical, we conclude that $\overline{v_a(t)}$, $\overline{v_b(t)}$, and $\overline{v_c(t)}$ lie along a straight line and therefore this memoryless D/A converter is perfectly linear.

In the typical waveform case, the three periodic patterns result in the following averages:

$$0: \quad \{1,-1,1,-1,\ldots\} \rightarrow \overline{v_d(t)} = \frac{A_1 + A_0 + \delta_1 + \delta_2}{2} = \overline{v_a(t)} + \frac{\delta_1 + \delta_2}{2}$$

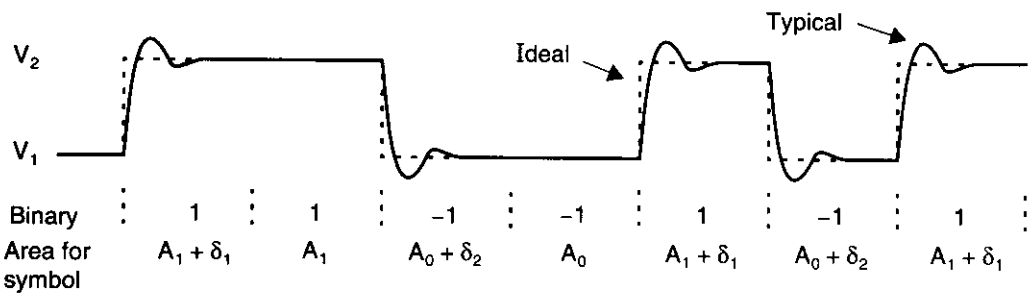


Fig. 14.24 A nonreturn-to-zero (NRZ) 1-bit D/A converter typical output.

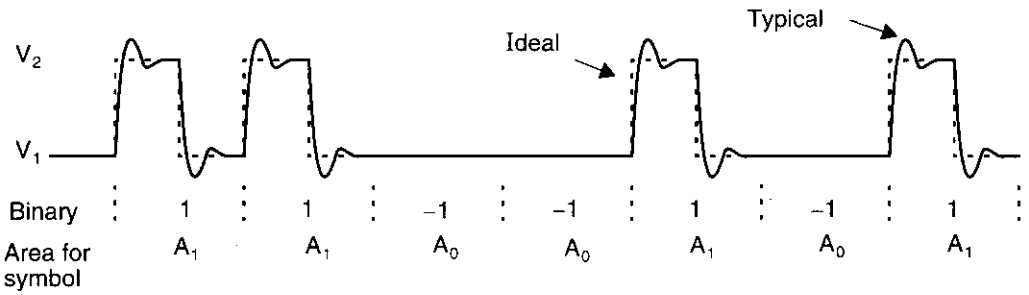


Fig. 14.25 A return-to-zero (RTZ) coding scheme, which is one example of a memoryless coding scheme.

$$1/3: \quad \{1, 1, -1, \ldots\} \rightarrow \overline{v_e(t)} = \frac{2A_1 + A_0 + \delta_1 + \delta_2}{3} = \overline{v_b(t)} + \frac{\delta_1 + \delta_2}{3}$$

$$-1/3: \quad \{-1, -1, 1, \ldots\} \rightarrow \overline{v_f(t)} = \frac{A_1 + 2A_0 + \delta_1 + \delta_2}{3} = \overline{v_c(t)} + \frac{\delta_1 + \delta_2}{3}$$

Now, these three averages do not lie on a straight line except when $\delta_1 = -\delta_2$. Thus, one way to obtain high linearity is to match falling and rising signals—a very difficult task since they are typically realized with different types of devices.

A better way to obtain linearity without matching rising and falling signals of the D/A converter is to use some sort of *memoryless coding scheme*. For example, consider the return-to-zero coding scheme shown in Fig. 14.25. It is not difficult to see here that since the area of one output bit does not depend on any previous bits, the coding scheme is memoryless and the output signal will remain linear. Naturally, other memoryless schemes can also be used, such as using two levels of opposite signs but ensuring that the signal settles to ground between samples.

It is of interest to see how this memoryless coding is applied in oversampling A/D converters. Presently, most oversampling A/D converters are realized using a switched-capacitor technology for linearity reasons. Switched capacitor circuits naturally realize memoryless levels as long as enough time is left for settling on each clock phase. In other words, switched-capacitor circuits implement memoryless coding since capacitors are charged on one clock phase and discharged on the next. For the same reason, the first stage of filtering in oversampling D/A converters is often realized using switched-capacitor filters, which is followed by continuous-time filtering. However, some type of memoryless coding should be used when high linearity is desired from a 1-bit D/A output either fed directly to a continuous-time filter in an oversampling D/A or used in the internal operation of a continuous-time oversampling A/D converter.

Idle Tones

Consider the case of applying a dc level of 1/3 to a first-order $\Delta\Sigma$ modulator having a 1-bit quantizer with output levels of ± 1 (as in Example 14.4). With such an input, the

output of the modulator will be a periodic sequence of two 1s and one –1. In other words,

$$y(n) = \{1, 1, -1, 1, 1, -1, 1, 1, \ldots\} \tag{14.46}$$

This output periodic pattern is three cycles long and its power is concentrated at dc and $f_s/3$. Although the output pattern is periodic, the post low-pass filter will eliminate the high-frequency content such that only the dc level of 1/3 remains.

Now consider applying a dc level of $(1/3 + 1/24) = 3/8$ to the same modulator. For this case, the output sequence becomes

$$y(n) = \{1, 1, -1, 1, 1, -1, 1, 1, -1, 1, 1, -1, 1, 1, 1, -1, 1, 1, -1, \ldots\} \tag{14.47}$$

The period of this output pattern is now 16 cycles long and has some power at $f_s/16$. With an oversampling ratio of eight (i.e., $f_0 = f_s/16$), the post low-pass filter will not attenuate the signal power at $f_s/16$ since that frequency is just within the frequency band of interest. In other words, a dc level of $3/8$ into this modulator will produce the correct dc output signal but have a superimposed $f_s/16$ signal on it even when using a brick-wall type low-pass filter.

While the above example shows a tone occurring at $f_s/16$, it is not difficult to find other cases that would produce frequency tones at much lower frequencies, say $f_s/256$. Such low-frequency tones *will not be filtered out by the next stage low-pass filter* and can lead to annoying tones in the audible range.[8] In addition, although a first-order modulator was used in the above example, it has been shown that annoying audible tones exist even in higher-order modulators [Norsworthy, 1993]. Finally, it should be mentioned that these tones might not lie at a single frequency but instead be short-term periodic patterns. In other words, a tone appearing near 1 kHz might actually be a signal varying between 900 Hz and 1.1 kHz in a random-like fashion.

Dithering

One way to reduce the amount of idle tones in modulators is through the use of dithering. The term dithering here refers to the act of introducing some random (or pseudo-random) signal into a modulator.

Assuming the random signal to be introduced has a white-noise type spectrum, then the most suitable place to add the dithering signal is just before the quantizer, as shown in Fig. 14.26. The reason for adding it at this location is so that the dithering signal becomes noise shaped in the same manner as the quantization noise, and thus a large amount of dithering can be added. Typically, the dithering signal is realized using some sort of pseudo-random number generator with only a few bits of resolution, but its total noise power is comparable to the quantization noise power. Thus, the use of dithering in a D/A converter would require a small additional digital adder, while a small D/A converter would be needed in an oversampling A/D converter.

It should be noted that the use of dither to reduce idle tones is not an attempt to add noise to mask out the tones but instead breaks up the tones so that they never

8. Human hearing can detect tones buried beneath white noise.

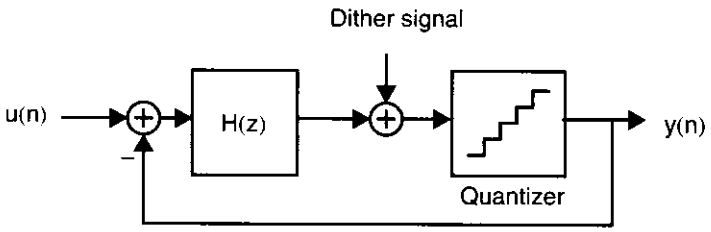


Fig. 14.26 Adding dithering to a delta-sigma modulator. Note that the dithered signal is also noise shaped.

occur. However, since the noise power of the dithering signal is similar to the quantization noise power, the use of dithering adds about 3 dB extra in-band noise and often requires rechecking the modulator's stability.

Opamp Gain

In Chapter 10, we saw that a switched-capacitor integrator with a finite opamp gain, A, results in the pole of the integrator moving to the left of $z = 1$ by an amount $1/A$ (see Problem 10.4 and assume $C_2 \approx C_1$ as is typical in oversampled converters). With this knowledge, we can determine the new NTF zeros due to finite opamp gain by substituting $z - 1$ with $z - (1 - 1/A)$. In other words, we substitute all ideal integrators with damped integrators and recalculate the transfer functions. Such an approach results in the NTF zeros, which were located at $z = 1$ for a low-pass design, to be moved to $z = (1 - 1/A)$. Thus, the shaped quantization noise does not drop to zero at dc but instead levels off near dc. Such a zero near $z = 1$ results in the 3-dB break frequency being approximately equal to $1/A$ rad/sample. Now, we note that the frequency band of interest, f_0, should be greater than $1/A$ rad/sample since the shaped quantization noise is flat below that level. In other words, if f_0 is below where the quantization noise flattens out, then we are not obtaining any further *noise-shaping* benefits. Thus, any further doubling of the oversampling ratio will only improve the SNR by 3 dB/octave. Finally, we can write the following requirement,

$$\frac{f_0}{f_s} > \frac{1/A}{2\pi} \tag{14.48}$$

and recalling that $OSR = f_s/(2f_0)$, we can rearrange the above to

$$A > \frac{OSR}{\pi} \tag{14.49}$$

Of course, some approximations have been made here, such as having the two capacitors of the integrator equal (that is $C_2 \approx C_1$) and having the 3-dB break point being sharp, as well as allowing noise to be flat from dc to f_0 (rather than shaped). In summary, designers will typically ensure that the opamp gain is at least twice the oversampling ratio, which is not usually a difficult requirement.

In addition, the above analysis only applies for modulators having a single D/A feedback and does not apply to MASH or cascade modulators, where larger opamp gains are often required to aid matching between digital and analog signal paths.

14.8 MULTI-BIT OVERSAMPLING CONVERTERS

Although 1-bit oversampling converters have the advantage that they can realize highly linear data conversion, they also have some disadvantages. For example, 1-bit oversampling modulators are prone to instability due to the high degree of nonlinearity in the feedback. Another disadvantage is the existence of idle tones, as previously discussed. Additionally, in oversampling D/A converters, the use of a 1-bit D/A converter results in a large amount of out-of-band quantization noise, which must be significantly attenuated using analog circuitry. Such a task often requires relatively high-order analog filtering (recall that the low-pass filter should be at least one order higher than the modulator order). Also, the dynamic range of the analog filter may have to be significantly higher than the converter's dynamic range since the filter's input must cope with power of both the quantization noise and signal itself. Since the quantization noise may be up to 15 dB larger in level than the signal level, such an extension in the dynamic range makes the realization of analog filters for oversampling D/A converters nontrivial. The use of a multi-bit D/A converter can significantly reduce this large amount of quantization noise, but care must be taken to ensure that the multi-bit converter remains linear. Typically, a multi-bit oversampling system would be similar to that shown in Fig. 14.16, except that an M-bit quantizer would be used in the digital modulator, and its output would drive an M-bit D/A converter. This section will briefly discuss some multi-bit oversampling converter architectures that employ methods so that the overall system remains highly linear.

Multi-bit Randomizer D/A Converter

One approach for realizing a multi-bit D/A converter intended for oversampling systems is that of dynamic element matching [Carley, 1989]. With this approach, a thermometer-code D/A converter is realized, and randomization is used to effectively spread the nonlinearity over the whole frequency range. For example, a 3-bit D/A converter using dynamic element matching is shown in Fig. 14.27. Here, the 8-line randomizer makes use of a pseudo-random code to distribute the thermometer lines equally to each of the unit capacitances, C. One point to note here is that the mismatch "noise" from this multi-bit converter is not shaped by any feedback loop and therefore appears more white than high-pass filtered. In [Carley, 1989], the resulting multi-bit oversampling D/A converter had 15-bit linearity while using peak element mismatches of 0.2 percent.

Recently, this dynamic element matching has been extended to include noise shaping the nonlinearity introduced by the DAC [Chen, 1995; Adams, 1995; Baird,

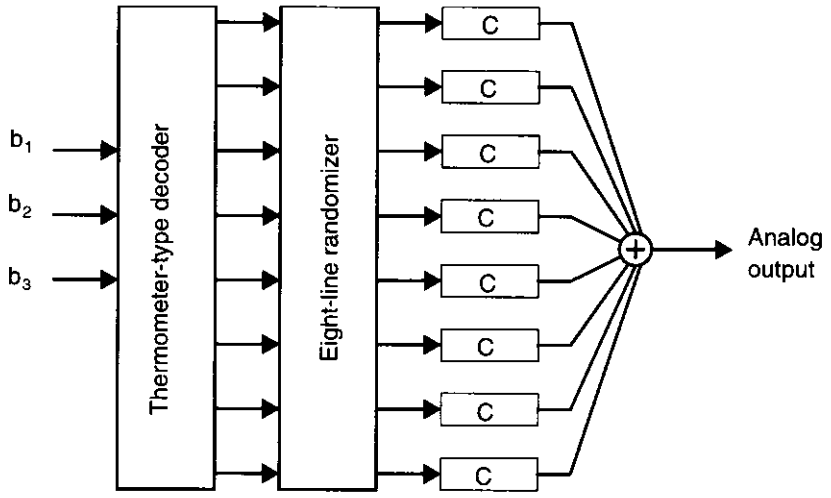


Fig. 14.27 Dynamic element matching 3-bit D/A converter.

1995]. This new approach is quite promising, since much lower oversampling ratios can be used while maintaining high linearity with a reasonably coarse DAC mismatch.

Dynamic Matched Current Sources in a D/A Converter

Another method of maintaining high linearity in an oversampling D/A system is through the use of a highly linear D/A converter operating at the fast oversampling rate. Such high linearity has been achieved using dynamically matched current sources similar to those described in Chapter 12 [Schouwenaars, 1991]. With this approach, a 5-bit D/A converter operating at 5.6 MHz was used to realize an effective 90 dB of dynamic range with a full-scale 0-dB input signal. Also, when an input signal of –30 dB (relative to full scale) was applied, the noise plus distortion was –85 dB lower than the signal power, indicating an effective dynamic range of 115 dB. The output bandwidth of the converter was dc to 20 kHz.

Digital Calibration A/D Converter

One way to make use of a multi-bit D/A converter in an oversampling A/D modulator is to have a calibration cycle where digital circuitry is used to model the static nonlinearity of the D/A converter, as shown in Fig. 14.28 [Larson, 1988]. With this approach, the multi-bit digital signal $x_2(n)$ creates 2^N output levels at $x_1(n)$, which are consistent in time but not necessarily linearly related to $x_2(n)$. However, the feedback loop of the modulator forces the in-band frequency of $x_1(n)$ to very closely equal $u(n)$, and thus $x_1(n)$ is still linearly related to $u(n)$. Through the use of the digital correction circuitry, the signal $y(n)$ also equals $x_1(n)$ if its nonlinearity equals that of the D/A con-

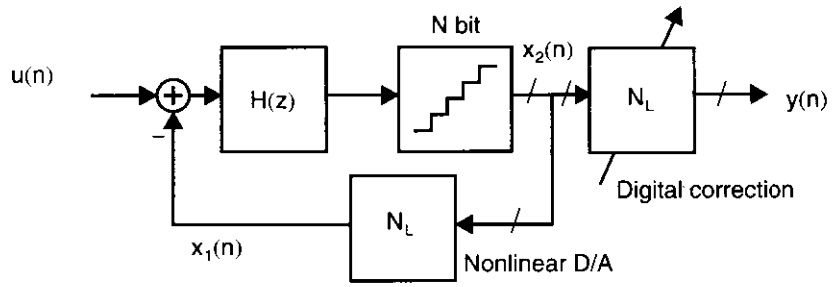


Fig. 14.28 Digitally corrected multi-bit A/D modulator.

verter. To realize this digital correction circuitry, a 2^N word look-up RAM is used where the size of each RAM word is at least equal to the desired linearity. For example, if a 4-bit D/A converter is used and 18 bits of linearity is desired, then the digital correction circuitry consists of a 16-word RAM, each of length 18 bits or greater (or equivalently, a 288-bit RAM). Furthermore, this RAM size can be reduced by digitizing only the difference between the desired linearity and the expected linearity of the D/A converter [Sarhang-Nejad, 1993]. For example, if the D/A converter is expected to have a linearity of at least 9 bits, then the RAM need only have a word length of 10 bits for 18-bit overall linearity.

The calibration of the digital correction circuitry can be accomplished by reconfiguring the $\Delta\Sigma$ A/D modulator to a single-bit system. Next, the input to this 1-bit converter is one of the 4-bit D/A converter levels to be calibrated. In other words, the multi-bit converter's input is held constant while its output is applied to the 1-bit A/D modulator for many clock cycles. The resulting 1-bit signal is digitally low-pass filtered and gives the desired digital equivalent value of that particular dc level for the D/A converter. This procedure is repeated 16 times to find all the 16 words of RAM.

Finally, it should be mentioned that a similar approach can be used to improve the linearity of a multi-bit oversampling D/A converter, except in this case the digital correction circuit would be in the feedback portion of the digital modulator.

A/D with Both Multi-Bit and Single-Bit Feedback

Another very interesting alternative architecture uses both multi-bit feedback and single-bit feedback [Hairapetian, 1994]. A third-order example of this A/D is shown in Fig. 14.29. If one assumes that the errors due to the quantization of the 1-bit A/D and 5-bit A/D are Q_1, and Q_5, respectively, and also that the 5-bit D/A injects errors due to its nonlinearity given by Q_d, then by applying a linear analysis to the system of Fig. 14.29 it can be shown that

$$U_s(z) = U(z)z^{-1} + Q_1(z)\frac{(1-z^{-1})^2}{1-0.5z^{-1}} - Q_5(z)\frac{z^{-1}(1-z^{-1})^{-2}}{1-0.5z^{-1}} - Q_d(z)\frac{z^{-1}(1-z^{-1})^{-2}}{1-0.5z^{-1}} \tag{14.50}$$

To find the poles of the system (i.e., the roots of D(z)), we need to ensure modulator stability while shaping as much quantization noise away from dc as possible. To ensure modulator stability, recall that a heuristic approach is to restrict the peak NTF to be less than 1.5. However, to shape the quantization noise away from dc, we wish to make the NTF as large as possible outside the frequency band of interest. Thus, the best NTF choice would be one which has a flat gain of 1.4 at high frequencies. Such a high-pass filter is obtained (i.e., no peaking in the NTF) when the poles are placed in a Butterworth configuration, as shown in Fig. 14.30. Thus, the denominator is found using digital filter software to design a third-order high-pass digital filter where the passband is adjusted until the peak NTF is less than 1.4 (i.e., $|NTF(e^{j\omega})| < 1.4$). Specifically, with a passband edge at $f_s/20$, a third-order Butterworth high-pass filter has a peak gain equal to 1.37, and thus the NTF(z) is given by

$$NTF(z) = \frac{(z-1)^3}{z^3 - 2.3741z^2 + 1.9294z - 0.5321} \tag{14.53}$$

Now, by rearranging (14.16), we can find H(z) in term of NTF(z), resulting in

$$H(z) = \frac{1 - NTF(z)}{NTF(z)} \tag{14.54}$$

which, for the function given in (14.53), results in

$$H(z) = \frac{0.6259z^2 - 1.0706z + 0.4679}{(z-1)^3} \tag{14.55}$$

Next, a suitable implementation structure is chosen. In this case, a cascade-of-integrators structure was used, as shown in Fig. 14.31. The α_i coefficients are included for dynamic-range scaling and are initially set to $\alpha_2 = \alpha_3 = 1$, while the last term, α_1, is initially set equal to β_1. By initially setting $\alpha_1 = \beta_1$, we are allowing the input signal to have a power level similar to that of the feedback signal, y(n). In other words, if α_1 were initially set equal to one and β_1 were quite small, then the circuit would initially be stable for only small input-signal levels.

Coefficient values for β_i are then found by deriving the transfer function from the 1-bit D/A output to V_3 and equating that function to $-H(z)$ in (14.55). Specifically, assuming $\alpha_2 = \alpha_3 = 1$, we find the following H(z):

$$H(z) = \frac{z^2(\beta_1 + \beta_2 + \beta_3) - z(\beta_2 + 2\beta_3) + \beta_3}{(z-1)^3} \tag{14.56}$$

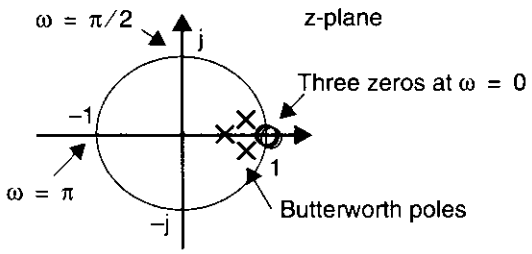


Fig. 14.30 Pole and zero locations for the third-order NTF.

To find the poles of the system (i.e., the roots of D(z)), we need to ensure modulator stability while shaping as much quantization noise away from dc as possible. To ensure modulator stability, recall that a heuristic approach is to restrict the peak NTF to be less than 1.5. However, to shape the quantization noise away from dc, we wish to make the NTF as large as possible outside the frequency band of interest. Thus, the best NTF choice would be one which has a flat gain of 1.4 at high frequencies. Such a high-pass filter is obtained (i.e., no peaking in the NTF) when the poles are placed in a Butterworth configuration, as shown in Fig. 14.30. Thus, the denominator is found using digital filter software to design a third-order high-pass digital filter where the passband is adjusted until the peak NTF is less than 1.4 (i.e., $|NTF(e^{j\omega})| < 1.4$). Specifically, with a passband edge at $f_s/20$, a third-order Butterworth high-pass filter has a peak gain equal to 1.37, and thus the NTF(z) is given by

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$$H(z) = \frac{z^2(\beta_1 + \beta_2 + \beta_3) - z(\beta_2 + 2\beta_3) + \beta_3}{(z-1)^3} \tag{14.56}$$

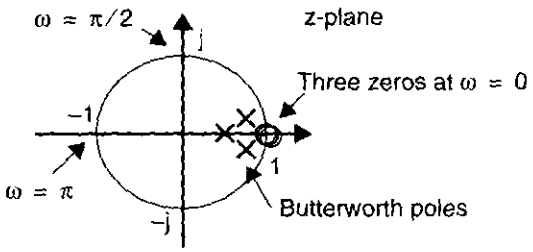


Fig. 14.30 Pole and zero locations for the third-order NTF.

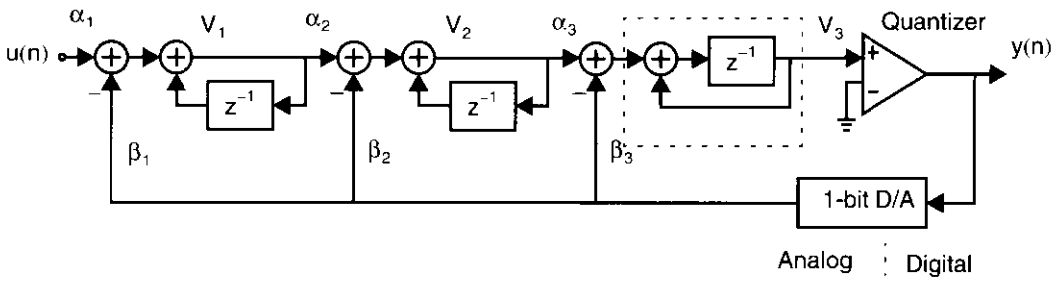


Fig. 14.31 The cascade-of-integrators structure used to realize the third-order modulator. Note that α_i coefficients are used for dynamic-range scaling and are initially set to $\alpha_1 = \beta_1$ and $\alpha_2 = \alpha_3 = 1$.

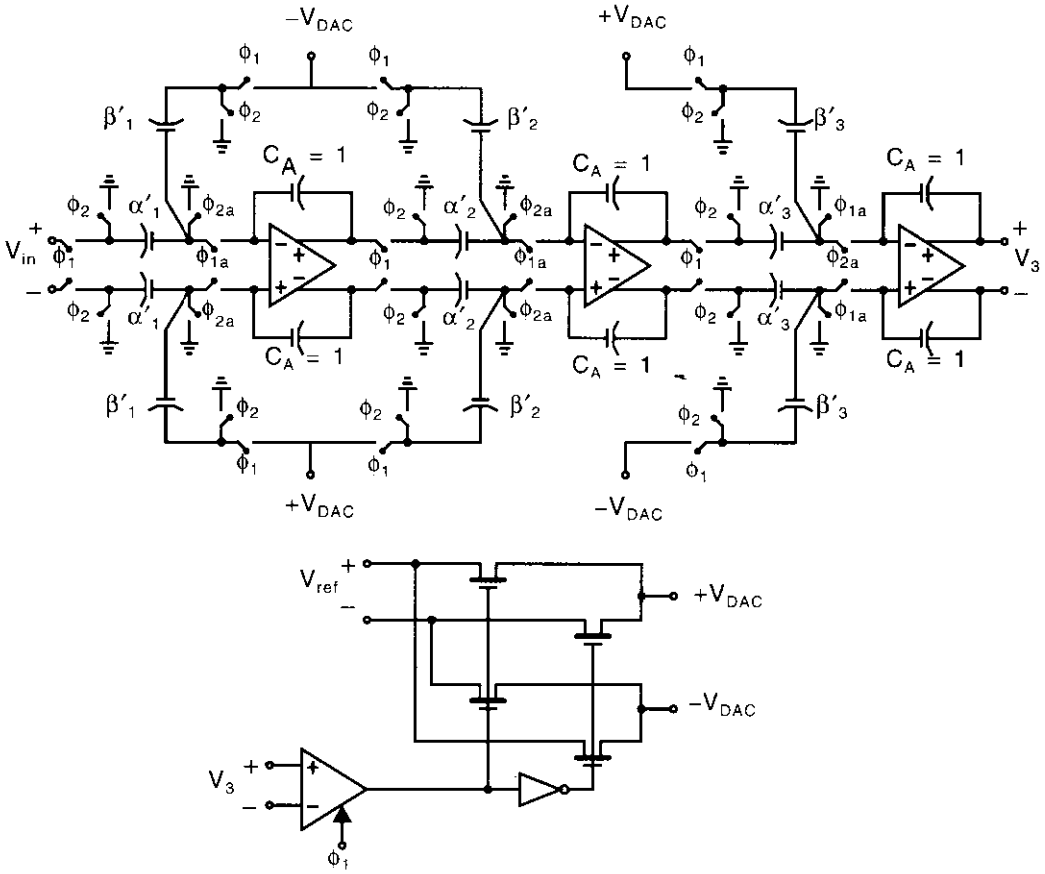


Fig. 14.32 A switched-capacitor realization of the third-order modulator example.

Equating (14.56) with (14.55), we find an initial set of coefficients to be

$$\begin{aligned} \alpha_1 &= 0.0232, \quad \alpha_2 = 1.0, \quad \alpha_3 = 1.0 \\ \beta_1 &= 0.0232, \quad \beta_2 = 0.1348, \quad \beta_3 = 0.4679 \end{aligned} \tag{14.57}$$

It is then necessary to perform dynamic-range scaling. Dynamic scaling is necessary to ensure that all nodes have approximately the same power level, so that all nodes will clip near the same level, and there will be no unnecessarily large noise gains from nodes with small signal levels. Here, dynamic-range scaling was accomplished by simulating the system in Fig. 14.31 with the coefficients just given and an input sinusoidal wave with a peak value of 0.7 at a frequency of $\pi/256$ rad/sample. Following the simulation, the maximum values at nodes V_1, V_2, V_3 were found to be 0.1256, 0.5108, and 1.004, respectively. To increase the output level of a node by a factor k, the input branches should be multiplied by k, while the output branches should be divided by k. For example, the maximum value of node V_1 is increased to unity by multiplying both α_1 and β_1 by $1/0.1256$ and dividing α_2 by $1/0.1256$. Similarly, node V_2 is scaled by dividing $0.1256\alpha_2$ and β_2 by 0.5108 and multiplying α_3 by 0.5108. Node V_3 was left unchanged, as its maximum value was already near unity. Such a procedure results in the following final values for the coefficients.

$$\begin{aligned} \alpha'_1 &= 0.1847, \quad \alpha'_2 = 0.2459, \quad \alpha'_3 = 0.5108 \\ \beta'_1 &= 0.1847, \quad \beta'_2 = 0.2639, \quad \beta'_3 = 0.4679 \end{aligned} \tag{14.58}$$

Finally, the block diagram of Fig. 14.31 can be realized by the switched-capacitor circuit shown in Fig. 14.32 to obtain the final oversampled A/D converter.

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14.11 PROBLEMS

14.1 Assuming oversampling with no noise shaping and using (14.14), find the approximate sampling rate required to obtain a maximum SNR of 80 dB on a signal with a 1-kHz bandwidth using a 1-bit quantizer.

14.2 Repeat Example 14.4, except use a dc input level of $1.2/3$. At what frequency would a tone appear (relative to the sampling rate, f_s)?

14.3 Repeat Example 14.4, except use a dc input level of 1.1 to see if the internal state of the modulator saturates.

14.4 Repeat Example 14.4, except use an input sequence of $\{10, -10, 10, -10, 10, -10, \ldots\}$ to see if the internal state of the modulator saturates. This problem demonstrates that a large level input signal can be applied to a modulator if its signal power resides at a frequency where the gain of $H(z)$ is low.

14.5 Given that an 8-bit A/D converter has a SNR of 50 dB but is linear to 12 bits, what is the sampling rate required to achieve 12 bits of accuracy using straight oversampling on a signal bandwidth of 1 MHz?

14.6 Repeat Problem 14.5, assuming that the 8-bit A/D converter is placed inside a first-order delta-sigma modulator. What is the sampling rate if a second-order modulator is used?

14.7 Repeat Problem 14.1, assuming a first-order modulator is used. What is the sampling rate if a second-order modulator is used?

14.8 Assuming a 1-bit output signal of ± 1 and a sinusoidal signal of ± 0.5 peak-to-peak, what is the ratio of the signal power to quantization noise power before any filtering is applied?

14.9 What does the block $G(z) - 1$ need to be in Fig. 14.13 in order that a second-order noise transfer function is realized equal to $(1 - z^{-1})^2$?

14.10 Show a switched-capacitor modulator so that the second-order modulator shown in Fig. 14.10 is realized.

14.11 Show that the sequence of $\{1, 1, -1, 1, 1, -1, 1, 1, -1, \ldots\}$ into a cascade of three integrators and differentiators shown in Fig. 14.19 gives the correct running average. Assume that the adders have infinite width and that $M = 4$.

14.12 At first glance, the impulse response of a running average filter of length 4 is the same as that for a hold system that holds the input signal for length 4. By producing a block diagram for each system, explain the difference between the two systems.

14.13 Verify (14.42).

14.14 Show the block diagram for a MASH architecture that realizes third-order noise shaping using a second-order modulator (as shown in Fig. 14.10) and a first-order modulator.

14.15 Sketch the noise transfer function from 0 to 4 MHz for the second-order bandpass modulator shown in Fig. 14.23, assuming the sampling rate, f_s, equals 4 MHz.

14.16 Show how the block diagram in Fig. 14.23 can be modified so that the bandpass modulator places zeros at $\pm f_s/8$ rather than $\pm f_s/4$.

14.17 Using the "typical" waveform pattern shown in Fig. 14.24, find the practical average outputs when 0, $1/2$, and $-1/2$ have been applied to the first-order modulator shown in Fig. 14.7.

CHAPTER

15 Continuous-Time Filters

There are two main techniques for realizing integrated analog filters. One technique is the use of switched-capacitor circuits, as discussed in Chapter 10. A switched-capacitor circuit, although its signal remains continuous in voltage (i.e., it is never quantized), is, in fact, a discrete-time filter since it requires sampling in the time domain. Because of this time-domain sampling, the clock rate must always be at least twice that of the highest frequency being processed to eliminate aliasing. In fact, typically the clock rate is much greater than twice the signal bandwidth, to reduce the requirements of an anti-aliasing filter. As a result, switched-capacitor filters are limited in their ability to process high-frequency signals. Presently, the second most popular technique for realizing integrated analog filters is *continuous-time filtering*. As their name suggests, continuous-time filters have signals that remain continuous in time and that have analog signal levels. Since no sampling is required, continuous-time filters have a significant speed advantage over their switched-capacitor counterparts.

Although continuous-time filters can operate successfully on high-speed signals, they do have some disadvantages that have thus far restricted most of their industrial use to high-speed but otherwise lower-performance applications. One disadvantage is their need for some sort of tuning circuitry. Tuning is required because their filter coefficients are determined by the product of two dissimilar elements, such as capacitance and resistor (or transconductor) values. Thus, although switched-capacitor filters have coefficient accuracies of 0.1 percent, integrated continuous-time coefficients are initially set to only about 30-percent accuracy! Fortunately, tuning circuitry can set the filter coefficient accuracy to around 1 percent at the cost of more (and sometimes complex) circuitry, as we will see in Section 15.7. Another practical disadvantage exhibited by most continuous-time filters is their relatively poor linearity and noise performance. Although low-frequency switched-capacitor filters have been realized with nonlinear distortion and noise performance better than 90 dB, high-frequency continuous-time filters typically have distortion plus noise performance not much better than 60 dB (often it is much worse). Fortunately, there are numerous high-speed applications in which distortion and noise performances are not too demanding, such as many data communication and video circuits.

15.1 INTRODUCTION TO G_m-C FILTERS

This section gives a brief introduction to G_m-C filters. We will see here that the main circuit building blocks of G_m-C filters are transconductors. The basic functions of transconductors are described in this section, and circuit techniques for realizing transconductors are presented in the following sections.

Integrators

An integrator is the main building block for most continuous-time filters. To realize an integrator in G_m-C technology, a transconductor and a capacitor can be used as shown in Fig. 15.1. A transconductor is essentially a transconductance cell (an input voltage creates an output current) with the additional requirement that the output current be *linearly related to the input voltage*. Here, the output of the transconductor is the current i_o, and, in the ideal case, both the input and output impedance of this block are infinite. The output current is linearly related to the differential input voltage signal by

$$i_o = G_m v_i \tag{15.1}$$

where G_m is the transconductance of the cell. It should be re-emphasized that this relationship is different from that of an operational-transconductance-amplifier (OTA) in that here, the output current should be *linearly* related to the input voltage. In addition, a transconductor should have a well-known (or at least controllable) transconductance value. In the case of an OTA, the transconductance does not necessarily need to be a linear function of the input voltage or a well-controlled value (though usually the transconductance value should be as large as possible).

This output current is applied to the integrating capacitor, C_1, resulting in the voltage across C_1 being given by

$$V_o = \frac{I_o}{sC_1} = \frac{G_m V_i}{sC_1} \tag{15.2}$$

Defining ω_{ti} to be the unity-gain frequency of the integrator, we can write

$$V_o \equiv \left(\frac{\omega_{ti}}{s}\right)V_i = \left(\frac{G_m}{sC_1}\right)V_i \tag{15.3}$$

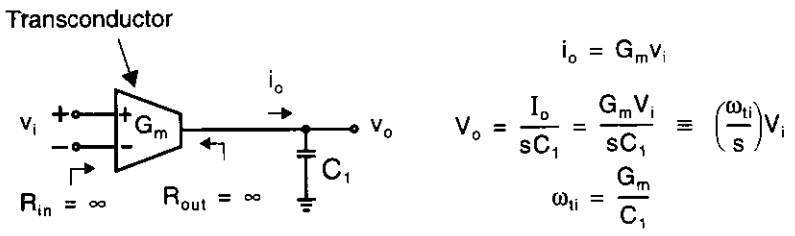


Fig. 15.1 A single-ended G_m-C integrator.

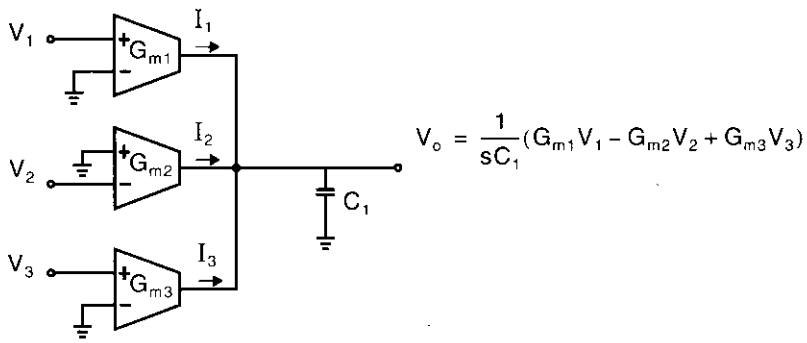


Fig. 15.2 A three-input, single-ended integrator/summer circuit.

Thus, we see that the output voltage is equal to the integration of the differential input voltage multiplied by the integrator unity-gain frequency, which is given by

$$\omega_{ti} = \frac{G_m}{C_1} \tag{15.4}$$

To realize a more general integrator/summer circuit, one need only connect multiple transconductors in parallel since the output currents all sum together. An example of a three-input integrator/summer circuit is shown in Fig. 15.2.

EXAMPLE 15.1

What transconductance is needed for an integrator that has a unity-gain frequency of 20 MHz, assuming a 2-pF integrating capacitor?

Solution

Rearranging (15.4), we have

$$\begin{aligned} G_m &= 2\pi \times 20 \text{ MHz} \times 2 \text{ pF} \\ &= 0.251 \text{ mA/V} \end{aligned} \tag{15.5}$$

Note that this transconductance value corresponds to

$$G_m = 1/3.98 \text{ k}\Omega \tag{15.6}$$

which, not surprisingly, is related to the unity-gain frequency by

$$2\pi \times 20 \text{ MHz} = \frac{1}{3.98 \text{ k}\Omega \times 2 \text{ pF}} \tag{15.7}$$

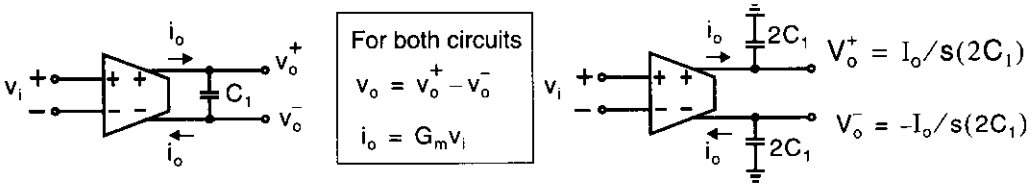
In other words, the required transconductance value is the inverse of the resistance value needed to form an RC time constant that corresponds to the desired unity-gain frequency.

Fully Differential Integrators

Although the preceding blocks have all been shown with single-ended signals,[1] in most integrated applications it is desirable to keep the signals fully differential. As discussed in Chapter 10, fully differential circuits have better noise immunity and distortion properties. Thus, mostly fully differential circuits are discussed in the remainder of this chapter.

A fully differential transconductor has two outputs—one positive output (current flowing out for a positive input voltage) and one negative output (current flowing in for a positive input voltage). With this new degree of freedom (having two outputs instead of just one), a fully differential integrator can be realized in one of two ways, as shown in Fig. 15.3.

Note that the integrator shown in Fig. 15.3(*a*) requires one-fourth the capacitance needed for the integrator of Fig. 15.3(*b*) to achieve the same integrator coefficient. Although at first glance, this increase in size appears to be a disadvantage of the circuit shown in Fig. 15.3(*b*), it should be mentioned that fully differential circuits require some method of common-mode feedback. This requirement is due to the fact that, although the differential signal remains stable due to connections of the filter feedback network, the common-mode signal is free to drift if it is not also controlled using some feedback circuit. As a result, one must also be concerned with the stability of the common-mode feedback circuit. Since, typically, dominant pole compensation using capacitors on the output node is often used to stabilize the common-mode network, the integrator shown in Fig. 15.3(*b*) has the advantage that the integrating capacitors, $2C_1$, can also be used for this purpose. Also, recall that



$$V_o = \frac{I_o}{sC_1} = \frac{G_m V_i}{sC_1}$$

$$\omega_{ti} = \frac{G_m}{C_1}$$

(*a*)

$$V_o = \frac{2I_o}{s(2C_1)} = \frac{G_m V_i}{sC_1}$$

$$\omega_{ti} = \frac{G_m}{C_1}$$

(*b*)

Fig. 15.3 Fully differential G_m-C integrators: (*a*) single capacitor, (*b*) two capacitors.

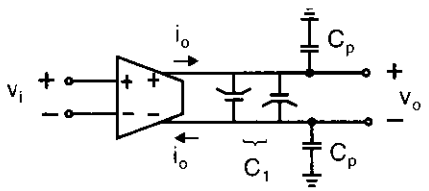
1. The transconductor input may be differential, but its output is single ended, and single-ended signals are typically applied to the transconductor inputs.

the single capacitor of the integrator shown in Fig. 15.3(a) must be realized using integrated capacitors, and thus top- and bottom-plate parasitic capacitances exist. Since the bottom-plate parasitic capacitance can be quite large (up to 20 percent of the capacitance value), to maintain symmetry, C_1 is often realized using two parallel capacitors, as shown in Fig. 15.4. We take the parallel combination of the two capacitances, which equals C_1, and include the effect of the parasitic capacitances, C_p, to obtain the output voltage, given by

$$V_o = \frac{G_m V_i}{s(C_1 + C_p/2)} \tag{15.8}$$

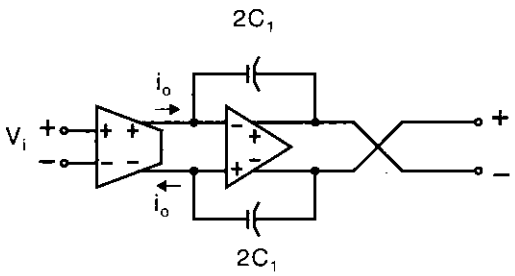
Thus, we see here that the parasitic capacitances affect the integration coefficient and must be taken into account.

Parasitic capacitances can also cause linearity problems since these capacitances are partially nonlinear (as most parasitic capacitances are). To reduce the effects of these parasitic capacitances, a common approach is to realize the integrating function using a Miller integrator, as shown in Fig. 15.5. As the figure shows, the integrating



$$V_o = \frac{G_m V_i}{s(C_1 + C_p/2)} \qquad \omega_{ti} = \frac{G_m}{(C_1 + C_p/2)}$$

Fig. 15.4 A fully differential integrator maintaining symmetry and showing parasitic capacitances.



$$V_o = \frac{2I_o}{s(2C_1)} = \frac{G_m V_i}{sC_1} \qquad \omega_{ti} = \frac{G_m}{C_1}$$

Fig. 15.5 A G_m-C opamp integrator (also called a Miller integrator). Note the cross coupling of the output wires to maintain a positive integration coefficient. Do not cross-couple the output if a negative coefficient is desired.This circuit requires that the common-mode voltage of the input nodes (as well as that of the output nodes) of the fully differential opamp be set to a specified value.

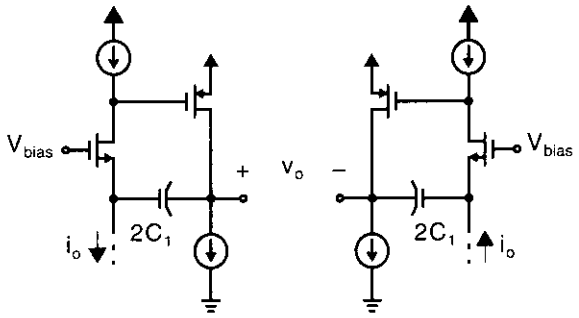


Fig. 15.6 A simple high-speed differential Miller integrator.

coefficient for this G_m-C opamp integrator is the same as that for the integrator in Fig. 15.3(*b*). The advantage of using the extra amplifier is that the effect of parasitic capacitances is reduced by the gain of the opamp. An additional advantage is that the output of the transconductance cell drives an opamp virtual ground, and so lower-output-impedance transconductance cells can be used. Another benefit is that the transconductance output nodes (i.e., the opamp input nodes) are maintained at a specific operating voltage set by a common-mode feedback circuit. As a result, the transconductance output stage can use small voltage swing circuitry, which is easier to design. Finally, the lower impedances at the transconductor output nodes make those nodes less sensitive to capacitive coupling of noise.

In summary, the addition of this extra opamp can simplify the design of the transconductance cell's output stage since the transconductor does not have to swing a large voltage range; it can have larger (and nonlinear) parasitic capacitances, it need not have a large output impedance, and it can be less sensitive to noise. The penalty paid here is a lower operating speed and a potential increase in circuit area and power. These two penalties can be reduced by using a simple high-speed design for the amplifier in the Miller integrator. For example, a current-input common-gate common-source amplifier, as shown in Fig. 15.6, is simple and moderately fast [Willingham, 1993; Padmanabhan, 1994]. The input impedance of this amplifier is small, on the order of $2/(g^2_m r_{ds})$, due not only to the low impedance of a common-gate first stage, but also due to feedback. Finally, it should be noted that either a low- or high-output-impedance opamp can be used for the Miller integrator since it needs to drive only capacitive loads. Typically, high-output-impedance amplifiers are used since they tend to have higher unity-gain frequencies, be simpler, and have less power dissipation.

First-Order Filter

A block diagram for a general first-order continuous-time filter is shown in Fig. 15.7. It can be shown that the transfer function for this block diagram is given by

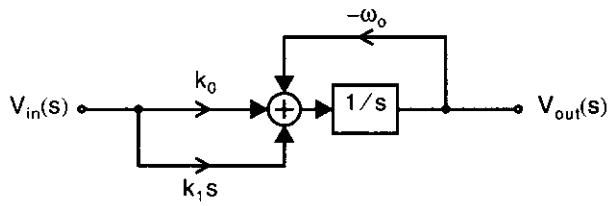


Fig. 15.7 A block diagram of a general first-order continuous-time filter.

$$H(s) \equiv \frac{V_{out}(s)}{V_{in}(s)} = \frac{k_1 s + k_o}{s + \omega_o} \tag{15.9}$$

A single-ended G_m-C filter that realizes a first-order filter is shown in Fig. 15.8. The transfer function for this first-order G_m-C filter is found by writing a current equation for the output node, $V_{out}(s)$:

$$G_{m1}V_{in}(s) + sC_X[V_{in}(s) - V_{out}(s)] - sC_A V_{out}(s) - G_{m2}V_{out}(s) = 0 \tag{15.10}$$

Rearranging to find $V_{out}(s)/V_{in}(s)$, we have

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{sC_X + G_{m1}}{s(C_A + C_X) + G_{m2}} = \frac{\left[s\left(\frac{C_X}{C_A + C_X}\right) + \left(\frac{G_{m1}}{C_A + C_X}\right)\right]}{\left[s + \left(\frac{G_{m2}}{C_A + C_X}\right)\right]} \tag{15.11}$$

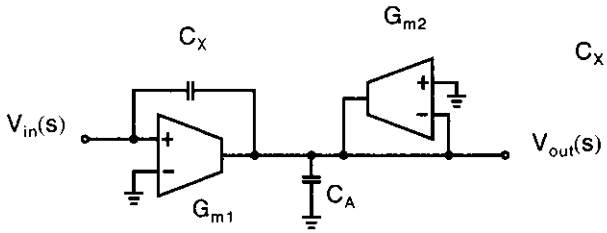
Equating (15.11) with (15.9) results in the following relationships:

$$C_X = \left(\frac{k_1}{1 - k_1}\right)C_A \tag{15.12}$$

$$G_{m1} = k_0(C_A + C_X) \tag{15.13}$$

$$G_{m2} = \omega_o(C_A + C_X) \tag{15.14}$$

It should be noted from (15.12) that, for C_X to remain a positive value, the term k_1 must satisfy $0 \le k_1 < 1$. What this restriction implies is that the shown circuit cannot realize a filter that has a high-frequency gain that is either negative or greater



$$C_X = \left(\frac{k_1}{1 - k_1}\right)C_A \text{ where } 0 \le k_1 < 1$$

$$G_{m1} = k_0(C_A + C_X)$$

$$G_{m2} = \omega_o(C_A + C_X)$$

Fig. 15.8 A single-ended general first-order G_m-C filter.

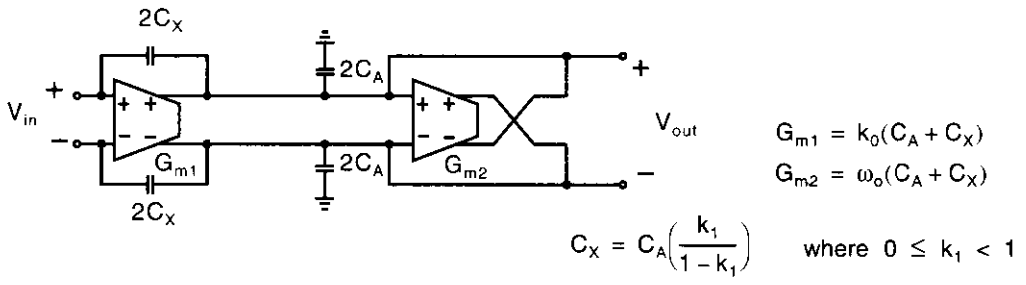


Fig. 15.9 A fully differential general first-order G_m-C filter.

than 1. Such a result should come as no surprise since the high-frequency gain of this circuit is simply a capacitor-divider circuit, and hence the restriction on k_1. Such a restriction on the maximum magnitude of the high-frequency gain would not occur if a G_m-C opamp filter were used since the feed-in capacitor could go into the virtual ground of an opamp and high-frequency gains greater than one would be possible.

Finally, the equivalent fully differential first-order G_m-C filter is shown in Fig. 15.9. Note that capacitor sizes are doubled here, in relation to the single-ended case, so that the same design equations occur. Also note that the same restriction holds on k_1, although a negative value of k_1 can be realized by cross-coupling the feed-in capacitor pair, C_X.

EXAMPLE 15.2

Based on Fig. 15.9, find component values for a first-order filter with a dc gain of 0.5, a pole at 20 MHz, and a zero at 40 MHz. Assume the integrating capacitors are sized $C_A = 2$ pF.

Solution

A first-order filter with a zero at 40 MHz and a pole at 20 MHz is given by

$$H(s) = \frac{k(s + 2\pi \times 40 \text{ MHz})}{(s + 2\pi \times 20 \text{ MHz})} \tag{15.15}$$

The leading coefficient is determined by setting the dc gain to 0.5, resulting in $k = 0.25$. Thus, we have

$$H(s) = \frac{0.25s + 2\pi \times 10 \text{ MHz}}{s + 2\pi \times 20 \text{ MHz}} \tag{15.16}$$

and equating this transfer function to (15.9) results in

$$k_1 = 0.25 \tag{15.17}$$

$$k_0 = 2\pi \times 10^7 \tag{15.18}$$

$$\omega_o = 4\pi \times 10^7 \tag{15.19}$$

Using the design equations shown in Fig. 15.9, we find

$$C_X = 2\text{ pF} \times \frac{0.25}{1 - 0.25} = 0.667\text{ pF} \tag{15.20}$$

$$G_{m1} = 2\pi \times 10^7 \times 2.667\text{ pF} = 0.168\text{ mA/V} \tag{15.21}$$

$$G_{m2} = 4\pi \times 10^7 \times 2.667\text{ pF} = 0.335\text{ mA/V} \tag{15.22}$$

where $C_A = 2$ pF, as given.

Second-Order Filter

To realize a second-order, or *biquad,* filter in G_m-C technology, we use the block diagram derived in Chapter 10 for a general continuous-time biquad filter. The block diagram of Fig. 10.19, slightly modified to make use of positive integrators, is shown in Fig. 15.10. The transfer function for this second-order filter is given by

$$H(s) \equiv \frac{V_{out}(s)}{V_{in}(s)} = \frac{k_2 s^2 + k_1 s + k_o}{s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2} \tag{15.23}$$

where it should be noted that the leading negative coefficient in (10.45) is no longer present due to the use of positive integrators. Of course, the inversion of the output signal could easily be obtained by simply cross-coupling the output wires. The fully differential version of this filter is shown in Fig. 15.11. The transfer function of this biquad filter is found to be given by

$$H(s) \equiv \frac{V_{out}(s)}{V_{in}(s)} = \frac{s^2\left(\frac{C_X}{C_X + C_B}\right) + s\left(\frac{G_{m5}}{C_X + C_B}\right) + \left(\frac{G_{m2}G_{m4}}{C_A(C_X + C_B)}\right)}{s^2 + s\left(\frac{G_{m3}}{C_X + C_b}\right) + \left(\frac{G_{m1}G_{m2}}{C_A(C_X + C_B)}\right)} \tag{15.24}$$

Equating the coefficients of (15.23) and (15.24) results in

$$k_2 = \frac{C_X}{C_X + C_B} \tag{15.25}$$

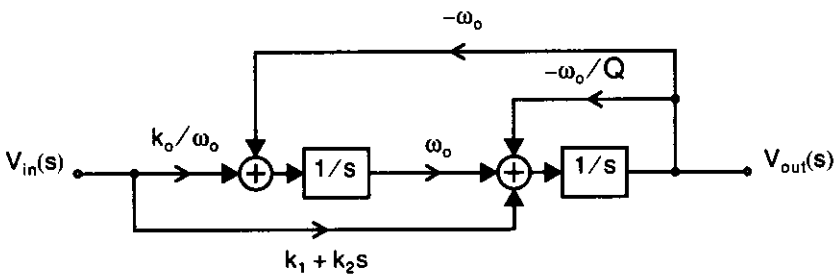


Fig. 15.10 A block diagram of a general second-order continuous-time filter.

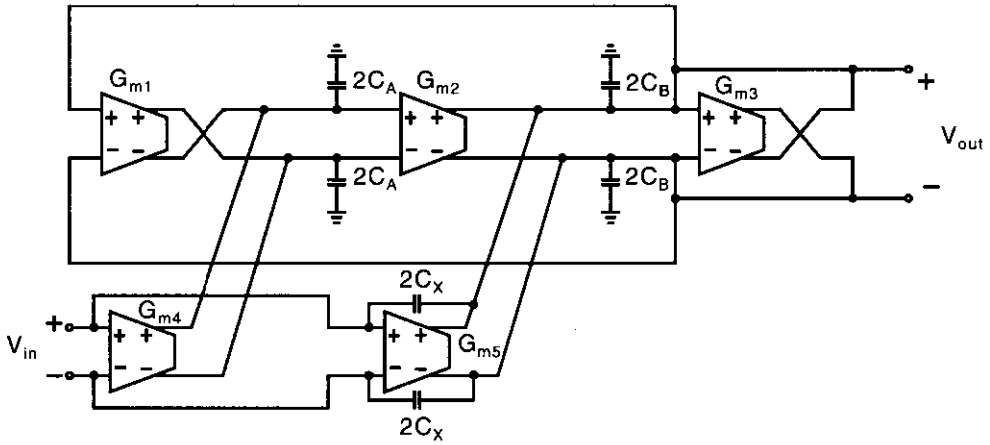


Fig. 15.11 A general second-order filter using fully differential G_m-C technology.

$$k_1 = \frac{G_{m5}}{C_X + C_B} \tag{15.26}$$

$$k_0 = \frac{G_{m2}G_{m4}}{C_A(C_X + C_B)} \tag{15.27}$$

and

$$\omega_o^2 = \frac{G_{m1}G_{m2}}{C_A(C_X + C_B)} \tag{15.28}$$

For Q, we note that

$$\frac{\omega_o}{Q} = \frac{G_{m3}}{C_X + C_b} \tag{15.29}$$

and so, by using (15.28), we can solve for Q, resulting in

$$Q = \sqrt{\left(\frac{G_{m1}G_{m2}}{G_{m3}^2}\right)\left(\frac{C_X + C_B}{C_A}\right)} \tag{15.30}$$

Although the preceding equations are for analyzing a given circuit, they can also be used for design, resulting in the following design equations:

$$C_X = C_B\left(\frac{k_2}{1 - k_2}\right) \quad \text{where } 0 \le k_2 < 1$$

$$G_{m1} = \omega_o C_A \quad G_{m2} = \omega_o(C_B + C_X) \quad G_{m3} = \frac{\omega_o(C_B + C_X)}{Q}$$

$$G_{m4} = (k_o C_A)/\omega_o \quad G_{m5} = k_1(C_B + C_X)$$

Note that for this design, there is a restriction on the high-frequency gain coefficient, k_2, similar to that occurring in the first-order case.

EXAMPLE 15.3

Find the transconductance and capacitor values for a second-order filter that has a bandpass response with a center frequency of 20 MHz, a Q value of 5, and a center frequency gain of 1. Assume that $C_A = C_B = 2$ pF.

Solution

A bandpass transfer function has the form

$$H(s) \equiv \frac{V_{out}(s)}{V_{in}(s)} = \frac{G s \frac{\omega_o}{Q}}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2} \tag{15.31}$$

where $G = 1$ is the gain at the center frequency. Using the facts that $\omega_o = 2\pi \times 20$ MHz and $Q = 5$, we find

$$k_1 = G\frac{\omega_o}{Q} = 2.513 \times 10^7 \text{rad/s} \tag{15.32}$$

Since k_0 and k_2 are zero, we have $C_x = G_{m4} = 0$ and

$$G_{m1} = \omega_o C_A = 0.2513 \text{ mA/V} \tag{15.33}$$

$$G_{m2} = \omega_o(C_B + C_X) = 0.2513 \text{ mA/V} \tag{15.34}$$

and, in this case,

$$G_{m3} = G_{m5} = k_1 C_B = 50.27 \ \mu\text{A/V} \tag{15.35}$$

15.2 BIPOLAR TRANSCONDUCTORS

There are two main approaches for realizing bipolar transconductors. One approach is to use a fixed transconductor cascaded with a gain cell. The fixed transconductor is typically a differential pair linearized through resistor degeneration. The gain cell allows scaling of the output current by varying the ratio of two current sources. The other approach is to use a differential input stage with multiple inputs, where the transistors are scaled such that improved linearity occurs. In this case, the transconductance value can be tuned by varying the bias current through the input stage.

Fixed Transconductors Using Resistors

Two similar approaches for using resistors to linearize a differential pair of transistors are shown in Fig. 15.12. To understand the basic operation of the two circuits, we first

make the simplifying assumption that the V_{be} voltages of the transistors are constant. As a result, we see that the differential input voltage, v_i, appears across the two $R_E/2$ resistors in Fig. 15.12(*a*) and across R_E in Fig. 15.12(*b*). Thus, the emitter current I_{E1} is given by

$$I_{E1} = I_1 + \frac{v_i}{R_E} \tag{15.36}$$

and the emitter current I_{E2} is given by

$$I_{E2} = I_1 - \frac{v_i}{R_E} \tag{15.37}$$

Ignoring base currents, these two emitter currents equal their respective collector currents. Then defining i_{o1} to be the difference in the output collector currents from I_1 (as shown), we have

$$i_{o1} = \frac{v_i}{R_E} \tag{15.38}$$

Thus, we see that the transconductance of these two differential input circuits is a fixed value of $1/R_E$. One important difference between the two fixed transconductors of Fig. 15.12 is that, in the case of $v_i = 0$, a bias current of I_1 flows through the two $R_E/2$ resistors in Fig. 15.12(*a*), whereas no bias current is flowing through R_E in Fig. 15.12(*b*). As a result, the common-mode voltage of Fig. 15.12(*b*) can be closer to ground. For example, if a bias current of $I_1 = 100\ \mu A$ is used together

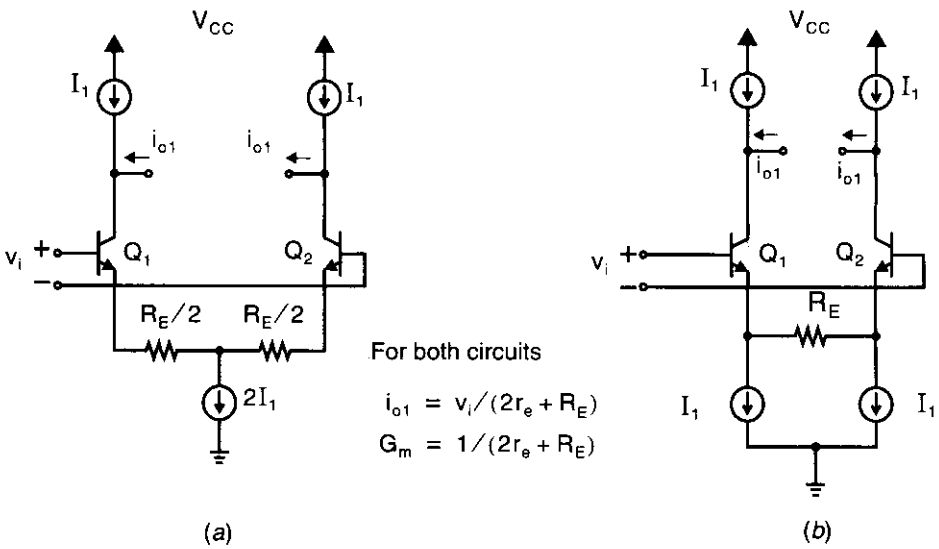


Fig. 15.12 Fixed transconductors using resistors. The lower common-mode range of the circuit in (*a*) is not as low as that of the circuit in (*b*) due to bias currents flowing through the $R_E/2$ resistors.

with $R_E = 20\ k\Omega$, then the voltage drop across each of the two $R_E/2$ resistors would result in 1 V less of common-mode range. It should be noted here that the common-mode input voltage must be far enough above ground to account for the largest expected differential input voltage, v_i. Specifically, one must ensure that the circuit remains functional while the base of one side of the differential pair is lower than the common-mode voltage by $v_i/2$.

A simple estimate of the maximum differential input range for both these circuits can be found by determining how much voltage exists across the linearizing resistors at the point where one transistor just turns off. For example, in Fig. 15.12(*a*), when Q_2 turns off due to a large positive input voltage, all of $2I_1$ flows through $R_E/2$ on the left and nothing flows through $R_E/2$ on the right. Thus, the voltage at the center of the two resistors equals that of the emitter of Q_2 (since no current flows right), and the maximum input voltage equals that voltage across the left $R_E/2$ resistor, giving

$$V_{i,max} = I_1 R_E \tag{15.39}$$

A similar argument gives the same maximum input voltage for the circuit of Fig. 15.12(*b*). It should be noted here that this simple estimate does not take into account that significant distortion occurs when this maximum input voltage is applied. Specifically, at $V_{i,max} = I_1 R_E$, one of the two transistors will be off, implying that V_{be} has not remained a relatively constant value, as we assumed earlier in this section. Typically, the maximum input range that applies to the preceding fixed transconductors might be one-half that of (15.39), or, equivalently, $(I_1/2)R_E$.

So far, we have assumed that the transistor's V_{be} voltages remain constant. Such an assumption is reasonably valid due to the exponential current-voltage relationship of bipolar transistors. Specifically, this assumption is reasonable when one restricts the minimum emitter current, $I_{E,min}$, in either transistor to be that which keeps the small-signal emitter resistance, r_e, much smaller than R_E. Recalling that

$$r_e \equiv \frac{V_T}{I_E} \tag{15.40}$$

we then have the requirement,

$$r_{e,max} = \frac{V_T}{I_{E,min}} << R_E \tag{15.41}$$

or equivalently,

$$I_{E,min} >> \frac{V_T}{R_E} \tag{15.42}$$

For example, if $R_E = 20\ k\Omega$ and $V_T = 25$ mV, the minimum emitter current in either transistor should be much greater than 1.25 μA. A good question is, How much is "much greater than"? The answer to this question depends on how much distortion can be tolerated since, when r_e becomes a comparable size to R_E, the varying V_{be} voltage will result in the output current, i_o, being a significant nonlinear function of the input voltage, v_i. For example, if the maximum value of r_e goes to 10 percent of

that of R_E when the maximum applied input voltage is $(I_1/2)R_E$, then a linearity deviation of about 3 percent occurs. Thus, to attain a high linearity with the preceding circuits, the bias currents should be large (resulting in a small value of r_e) and the input signal should be small (to maintain the small values of r_e). Of course, the use of small input signals may result in noise becoming a problem.

In applications in which a moderate amount of nonlinearity can be tolerated, R_E might be chosen similar in size to the nominal bias value of r_e. In this case, the overall transconductance of this transconductor is most easily found using the hybrid T model for the input transistor pair. With such an approach, the output current is more accurately described by

$$i_{o1} = \frac{v_i}{r_{e1} + R_E + r_{e2}} = \frac{v_i}{2r_e + R_E} \tag{15.43}$$

where r_e is the small-signal emitter resistance (equal to α/g_m), given by

$$r_e = \frac{V_T}{I_E} = \frac{V_T}{I_1} \tag{15.44}$$

Note that (15.43) reduces to (15.38) when R_E is chosen much larger than $2r_e$. In summary, a more accurate formula for the transconductance of the two circuits of Fig. 15.2 is

$$G_m = \frac{i_{o1}}{v_i} = \frac{1}{2r_e + R_E} \tag{15.45}$$

EXAMPLE 15.4

Consider the circuit of Fig. 15.2(*b*), where $R_E = 3\ \text{k}\Omega$ (such that $G_m \approx 0.333\ \text{mA/V}$) and the maximum differential input voltage is ±500 mV. Choose an appropriate bias current, I_1, such that $r_{e,max} < 0.1R_E$, and find a more precise value for G_m. Find the new value of I_1 and G_m if the constraint $r_{e,max} < 0.01R_E$ is used instead.

Solution

In the first case, we have $r_{e,max} < 0.1R_E = 300\ \Omega$. Thus, in the case of $v_i = 500$ mV, we require that $r_{e2} \approx 300\ \Omega$, which is attained for an emitter current of

$$I_{E2,min} = \frac{V_T}{r_{e,max}} = \frac{26\ \text{mV}}{300\ \Omega} = 86.7\ \mu\text{A} \tag{15.46}$$

For this same input voltage, the resistor current is approximately

$$I_{RE} \cong \frac{500\ \text{mV}}{3\ \text{k}\Omega} = 167\ \mu\text{A} \tag{15.47}$$

and since the current through R_E plus I_{E2} must equal I_1 (according to the node currents at the emitter of Q_2), we have

$$I_1 = 167 + 86.7 = 253\ \mu A \tag{15.48}$$

In other words, a minimum bias current of 253 μA should be chosen. For this value of bias current, the nominal value of r_e is given by

$$r_e = \frac{V_T}{I_1} = 103\ \Omega \tag{15.49}$$

resulting in

$$G_m = \frac{1}{(2r_e + R_E)} = 0.312\ mA/V \tag{15.50}$$

For the case $r_{e,max} < 0.01R_E$, one finds $I_1 = 1.03$ mA and $G_m = 0.328$ mA/V. Note here that the nominal value of r_e is now only 26 Ω, which is significantly less than R_E. Although this second design will have less distortion than the first (about 10 times better), it uses much more power. Next, we look at using feedback to improve distortion without resorting to large bias currents.

One way to improve the distortion properties of the above fixed transconductors without using large bias currents and small input signal levels is to use an extra pair of amplifiers, as shown in Fig. 15.13. Here, the virtual ground in each opamp forces the emitter voltages of Q_1 and Q_2 to equal those of v_i^+ and v_i^-. As a result, the input

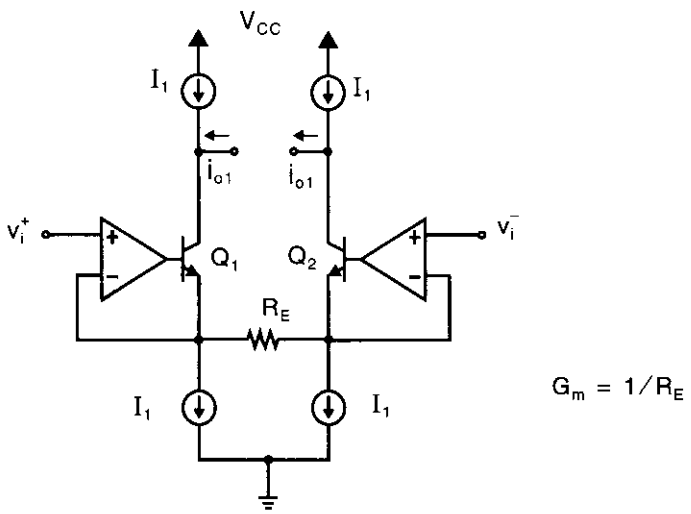


Fig. 15.13 Improving the linearity of a fixed transconductor through the use of opamps.

voltage appears directly across R_E and does not depend on the V_{be} voltages of Q_1 and Q_2. Thus, the transconductance of this circuit is given by

$$G_m = \frac{i_{o1}}{v_i^+ - v_i^-} = \frac{1}{R_E} \tag{15.51}$$

It should be mentioned here that the opamps can be quite simple (typically, a single stage) because they merely improve an input stage that is already reasonably linear.

Another method for improving the linearity of a fixed transconductor is to force constant currents through Q_1 and Q_2 such that their V_{be} voltages are fixed, as shown in Fig. 15.14 [Koyama, 1993]. Here, I_1 flows through each of Q_1 and Q_2, while Q_3 and Q_4 have varying collector currents corresponding to the current flow through R_E. The output currents can then be obtained at the collectors of Q_7 and Q_8, which mirror the current through Q_3 and Q_4. Thus, assuming the current mirror transistors consisting of Q_7 and Q_8 are equal in size to those of Q_3 and Q_4, the transconductance of this cell is given by

$$G_m = \frac{i_{o1}}{v_i^+ - v_i^-} = \frac{1}{R_E} \tag{15.52}$$

If the current mirror transistors are scaled in relation to Q_3 and Q_4, then the transconductance for this cell is also scaled by the same amount.

It should be noted that simple diode-connected transistors are not used at Q_3 and Q_4 since a feedback circuit is required to set the voltage level at the collectors of Q_1

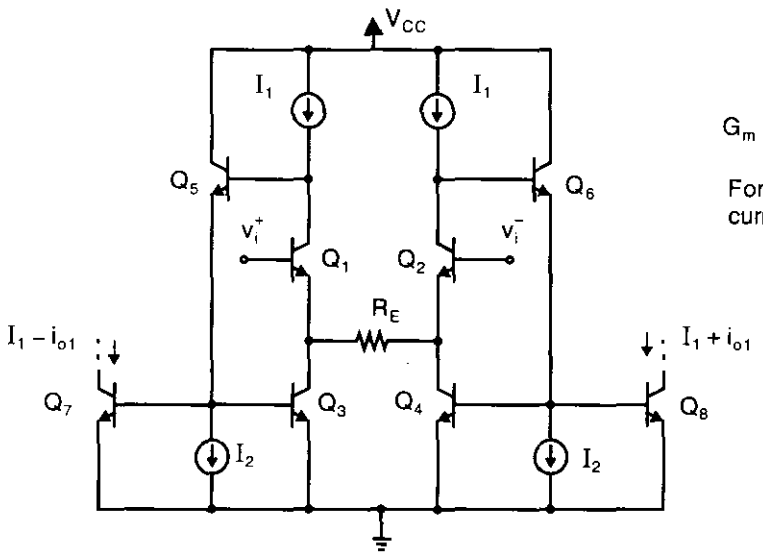


Fig. 15.14 Improving the linearity of a fixed transconductor by maintaining a constant V_{be} voltage for Q_1 and Q_2. Level shifts should be added at the emitters of Q_5, Q_6 if a larger input range is desired.

and Q_2 without drawing much current. The feedback loop occurs as follows: If the voltage at the collector of Q_1 increases because I_{C1} is less than I_1, then V_{be3} also increases, forcing more current through Q_3 and Q_1 until I_{C1} once again equals I_1. Although the circuit shown results in each of Q_1 and Q_2 collector voltages being set to two diode drops above ground (i.e., $V_{be3} + V_{be5}$), a larger voltage can be obtained by adding diode-connected transistors that operate as voltage level-shifters. It is possible to combine parts of this fixed-transconductor circuit with a gain-cell stage, as was done in [Koyama, 1993]. Finally, it should be mentioned here that the same linearization technique has been used in a CMOS variable transconductor, where the resistance R_E was realized using a MOS transistor operating in the triode region [Welland, 1994].

Gain-Cell Transconductors

The transconductors just described have a fixed transconductance value equal to approximately $1/R_E$. However, to accommodate tuning, variable transconductance values are required. One common approach for creating tunable transconductors that have a fixed transconductance input stage is to use a gain cell as described in Section 8.7. Recall that in a gain cell, the output current is equal to a scaled version of the input current, where the scaling factor is determined by the ratio of two dc bias currents. In addition, the circuit is highly linear.

A tunable transconductor that uses a gain cell is shown in Fig. 15.15. Here, the voltage sources, V_{LS}, represent voltage level shifters and could be realized using the circuit shown in Fig. 15.16. By combining the relationships given for the fixed

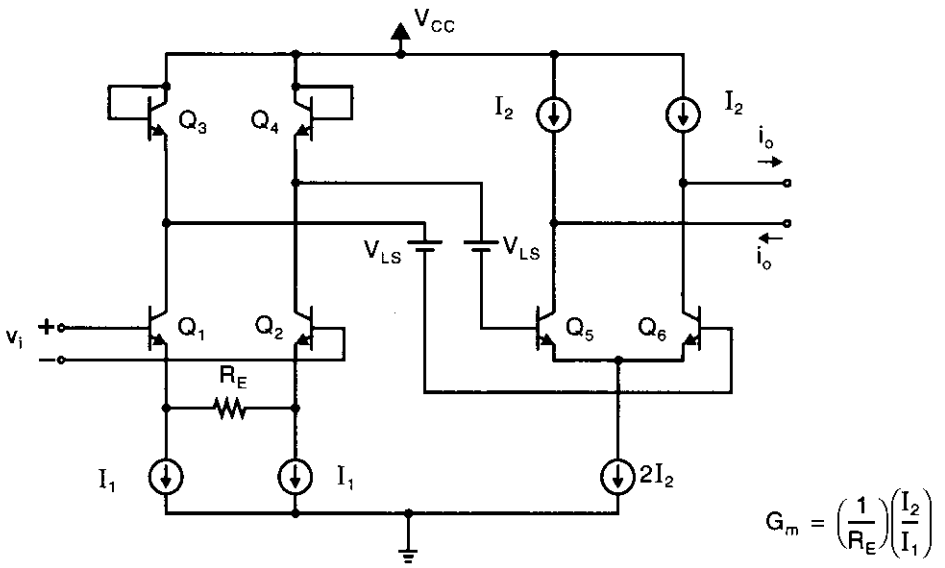


Fig. 15.15 A typical gain-cell transconductor.

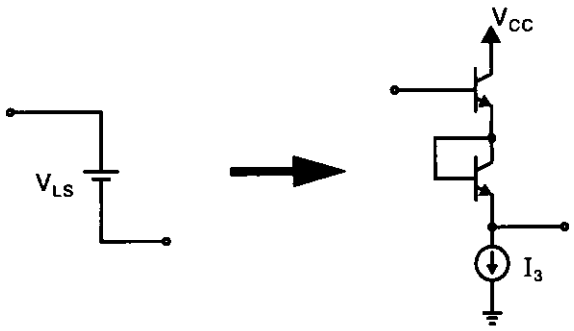


Fig. 15.16 A possible realization of the level shifters.

transconductor and the gain cell, specifically, (15.38) and (8.61), then the output current is given by

$$i_o = \frac{v_i I_2}{R_E I_1} \tag{15.53}$$

resulting in a transconductance value equal to

$$G_m = \left(\frac{1}{R_E}\right)\left(\frac{I_2}{I_1}\right) \tag{15.54}$$

Thus, the transconductance value is proportional to the ratio of I_2/I_1.

It is also possible to place the gain cell below the input differential pair, as shown in Fig. 15.17 [Wyszynski, 1993; Moree, 1993]. Note that while the previous designs

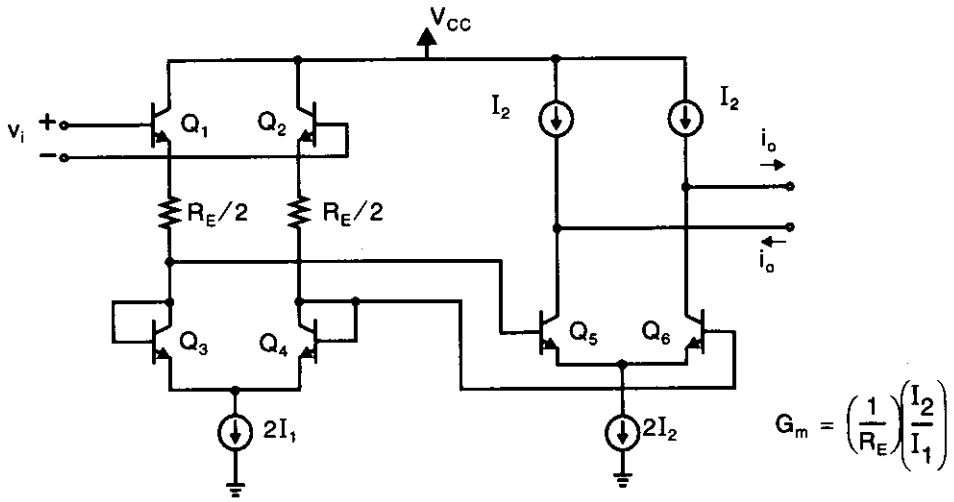


Fig. 15.17 A gain-cell transconductor with the gain cell below the input differential pair.

have $2r_e$ in series with the degeneration resistor, R_E, this circuit has $4r_e$ in series with R_E (that of $Q_1 - Q_4$), which might affect the distortion performance. However, the gain cell shown has less distortion due to finite β effects and has therefore been referred to as a *beta-immune type-A cell* [Gilbert, 1990].

Transconductors Using Multiple Differential Pairs

Quite a different approach for realizing a bipolar transconductor is by partially linearizing the input stage through the use of multiple differential pairs. To see how this linearization is achieved, consider a simple differential pair, as shown in Fig. 15.18(*a*). Ignoring base currents, we saw in Section 3.10 that the collector current i_{C2} is given by

$$i_{C2} = \frac{I_1}{1 + e^{v_i/V_T}} \tag{15.55}$$

This current is plotted in Fig. 15.18(*b*), where we note that the curve is relatively linear near $v_i = 0$. It is well known that the slope at this point equals the transconductance of this differential input stage and is given by

$$G_m = \frac{1}{2r_e} = \frac{I_1}{4V_T} \tag{15.56}$$

Thus, we see that the transconductance is proportional to the bias current, I_1. Unfortunately, this two-transistor input stage has a very limited input range when used as a linear transconductor. In fact, when v_i becomes greater than around 32 mV_{pp} (i.e., $v_i > \pm 16$ mV), the total harmonic distortion of the output current becomes greater than 1 percent (see Example 15.5). We now discuss a method to use parallel differential pairs to increase the linear input range [Calder, 1984].

Consider the input stage shown in Fig. 15.19(*a*), where two differential pairs are connected in parallel but with a dc offset voltage applied to each. The currents of the

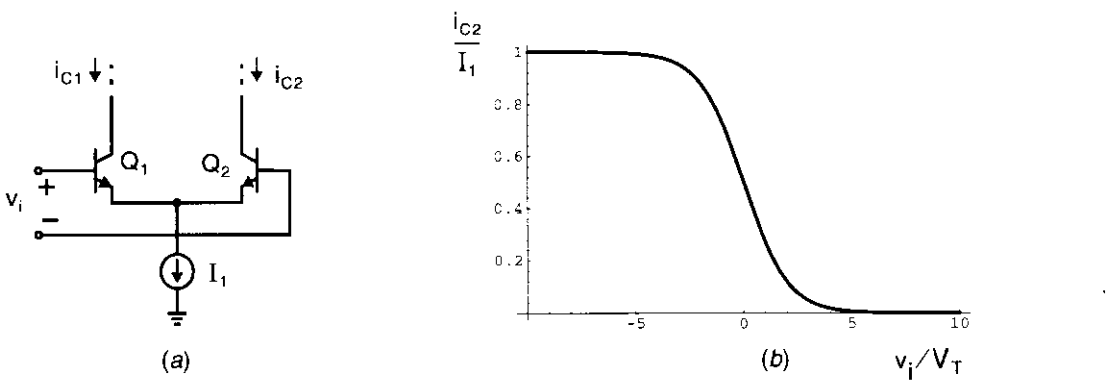


Fig. 15.18 (*a*) Differential pair. (*b*) Current output versus input voltage.

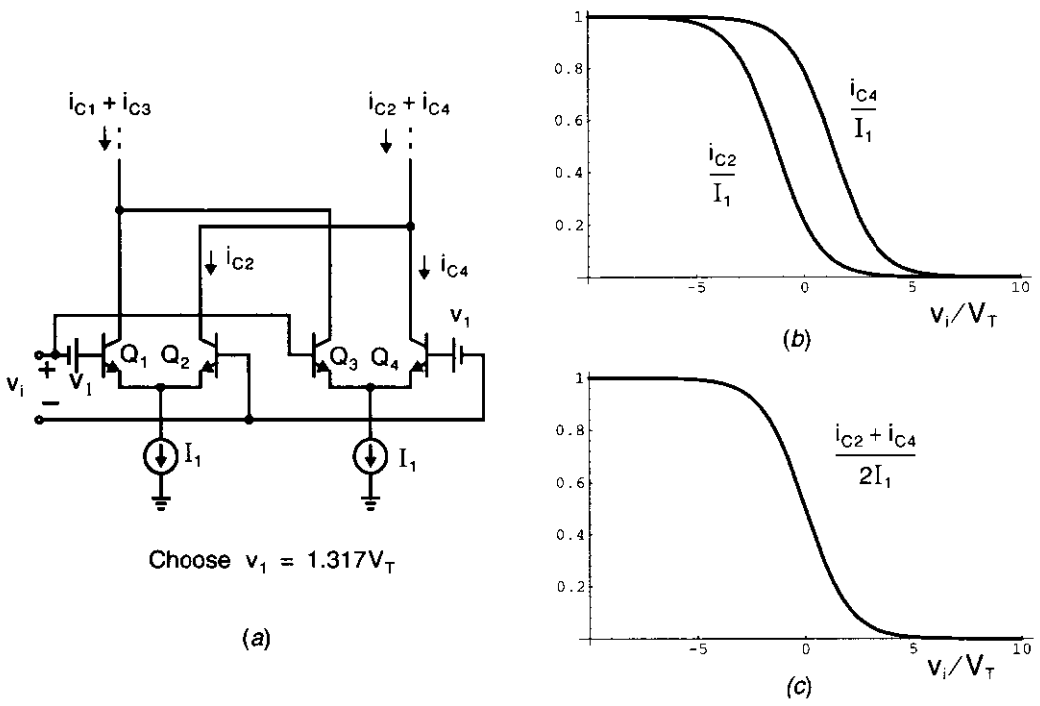


Fig. 15.19 *(a)* A linearized differential input; *(b)* individual right-side currents; *(c)* total linearized right-side current. The left-side currents are similar.

right side transistors in each transistor pair are shown in Fig. 15.19(*b*). If the dc offset voltages, V_1, are chosen carefully, then the two current curves will partially linearize each other when they are added together, as shown in Fig. 15.19(*c*). In this case, V_1 is chosen to be equal to $1.317V_T$ to maximize the linear input range [Tanimoto, 1991]. As a result of this linearization technique, the input range can now be approximately three times that of the original differential pair or, equivalently, 96 mV_{pp}, and achieve the same distortion performance.

To reduce circuitry, the two dc offset voltage sources can be eliminated by sizing the differential pair of transistors appropriately. Specifically, assuming that $V_i = 0$, then when $V_1 = 1.317V_T$, the collector currents of Q_2 and Q_4 are given by

$$i_{C2} = \frac{I_1}{1 + e^{1.317}} = 0.2113I_1 \tag{15.57}$$

and

$$i_{C4} = i_{C1} = \frac{I_1}{1 + e^{-1.317}} = 0.7887I_1 \tag{15.58}$$

If a two-transistor differential pair has unequal-sized transistors such that the same two currents occur for $V_i = 0$, then this unequal-sized differential pair will behave the

same as that of an equal-sized differential pair with a dc offset applied. To determine the sizing of the unequal-sized differential pair, define k to be the ratio of the base-emitter area of Q_1 with respect to Q_2. Thus, for this unequal-sized case, when $v_i = 0$, we have

$$i_{C1} = kI_s e^{(v_{be}/V_T)} = 0.7887I_1 \tag{15.59}$$

and

$$i_{C2} = I_s e^{(v_{be}/V_T)} = 0.2113I_1 \tag{15.60}$$

Dividing (15.59) by (15.60), we obtain

$$k = 3.73 \tag{15.61}$$

Thus, we should make Q_1 3.73 times larger than Q_2, and similarly Q_4 should be 3.73 times larger than Q_3. Such transistor sizing achieves the same result as the dc offset voltages. This result should make intuitive sense since we require that the ratio of the two currents be 0.7887/0.2113 when their base-emitter voltages are equal; this requirement results in the area ratio. Typically, this area ratio is set to 4 for practical reasons, and the final linearized transconductor is realized as shown in Fig. 15.20. Thus, for this circuit with $v_i = 0$, the currents through Q_1 and Q_2 are $0.8I_1$ and $0.2I_1$, respectively.

To determine the transconductance of the circuit of Fig. 15.20, we note that G_m equals the sum of the transconductance of the two differential pairs, resulting in

$$G_m = \frac{1}{r_{e1} + r_{e2}} + \frac{1}{r_{e3} + r_{e4}} \tag{15.62}$$

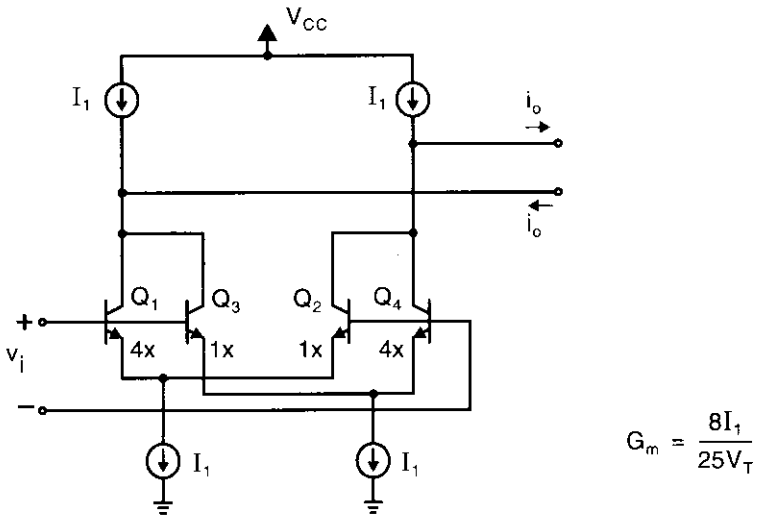


Fig. 15.20 Using transistor sizing to create a linearized differential transconductor.

Also, at $v_i = 0$, we have

$$r_{e1} = r_{e4} = \frac{V_T}{0.8I_1} \tag{15.63}$$

and

$$r_{e2} = r_{e3} = \frac{V_T}{0.2I_1} \tag{15.64}$$

Combining (15.62) to (15.64), we have

$$G_m = \frac{8I_1}{25V_T} \tag{15.65}$$

which is 28 percent greater than the transconductance value for the transistor pair shown in Fig. 15.18(*a*). However, this comparison is not fair since two differential pairs and twice the current are used in this linearized approach. If two differential pairs of Fig. 15.18(*a*) are used together, then their total transconductance would be $G_m = I_1/(2V_T)$, implying that this linearized approach has a 36 percent smaller transconductance. Also note that, as in the two-transistor pair case, this transconductance value is also proportional to the bias current, I_1, and thus no gain cell is required.

Recent circuits based on this approach have resulted in a 2- to 10-MHz programmable filter intended for disk-drive applications [De Veirman, 1992]. Finally, it should be mentioned here that this same technique can be extended to a larger number of input stages to further improve the linear input range [Tanimoto, 1991]. Using four differential input pairs in parallel, the linear input range was reported to be 16 times better than that for a single differential pair.

EXAMPLE 15.5

Consider the single differential pair shown in Fig. 15.18(*a*), where $I_1 = 2$ mA. Find the percentage error between an ideal linear transconductor and the true output current when $v_i = 16$ mV.

Solution

Using (15.56), we have

$$G_m = \frac{I_1}{4V_T} = 19.2 \text{ mA/V} \tag{15.66}$$

Thus, for an ideal linear transconductor, the output current for a 16-mV input voltage would be

$$i_o = G_m \times 16 \text{ mV} = 0.307 \text{ mA} \tag{15.67}$$

The true output current can be found from (15.55) as

$$I_{C2} = \frac{2 \text{ mA}}{1 + e^{16/26}} = 0.702 \text{ mA} \tag{15.68}$$

$$I_{C1} = \frac{2\text{ mA}}{1 + e^{-16/26}} = 1.298\text{ mA} \tag{15.69}$$

implying that the change in current from the bias current of 1 mA is 0.298 mA. Thus, the percentage error between the true output current and the ideal linear transconductor output is

$$\frac{0.298 - 0.307}{0.307} \times 100 = -3\% \tag{15.70}$$

In this case, the deviation is three-percent worst case, which results in about a one-percent total-harmonic-distortion (THD) measurement (see Section 15.8).

EXAMPLE 15.6

Consider the linearized differential pairs shown in Fig. 15.19(*a*), where $I_1 = 2$ mA. Find the percentage error between an ideal linear transconductor and the true output current when $v_i = 16$ mV.

Solution

First, we need to derive a formula for G_m in a manner similar to that for (15.65), where

$$r_{e1} = r_{e4} = \frac{V_T}{0.7887 I_1} \tag{15.71}$$

$$r_{e2} = r_{e3} = \frac{V_T}{0.2113 I_1} \tag{15.72}$$

Thus, the transconductance is given by

$$G_m = \frac{1}{r_{e1} + r_{e2}} + \frac{1}{r_{e3} + r_{e4}} = \frac{0.333 I_1}{V_T} = 25.6\text{ mA/V} \tag{15.73}$$

For an ideal linear transconductor, the output current for a 16-mV input voltage would result in

$$i_o = G_m \times 16\text{ mV} = 0.4102\text{ mA} \tag{15.74}$$

To calculate the true output current, we first note that

$$v_1 = 1.317 V_T = 34.24\text{ mV} \tag{15.75}$$

and since $v_i = 16$ mV, we use $v_i + v_1$ to find I_{C1}, resulting in

$$I_{C1} = \frac{2\text{ mA}}{1 + e^{-50.24/26}} = 1.747\text{ mA} \tag{15.76}$$

$$I_{C2} = 2\text{ mA} - I_{C1} = 0.253\text{ mA} \tag{15.77}$$

For I_{C4}, we use $v_1 - v_i$ to obtain

$$I_{C4} = \frac{2\text{ mA}}{1 + e^{-18.24/26}} = 1.337\text{ mA} \tag{15.78}$$

$$I_{C3} = 2\text{ mA} - I_{C4} = 0.663\text{ mA} \tag{15.79}$$

The true output is then equal to

$$I_{C1} + I_{C3} = 2.41\text{ mA} \tag{15.80}$$

$$I_{C2} + I_{C4} = 1.59\text{ mA} \tag{15.81}$$

implying that the change in current from the bias current of 2 mA is 0.4099 mA. Thus, the percentage error between the true output current and the ideal linear transconductor output is

$$\frac{0.4099 - 0.4102}{0.4102} \times 100 = -0.1\% \tag{15.82}$$

Note that this error is over ten times better than with a simple differential pair.

15.3 CMOS TRANSCONDUCTORS USING TRIODE TRANSISTORS

In this section, we discuss transconductor circuit techniques that rely on transistors operating in the triode region. It should be stated here that in the following circuits, not all transistors are in the triode region. As we will see, most of the transistors are biased in the active region, but the transconductance of the circuit relies on one or two key transistors biased in the triode region.

We begin this section by recalling the classical model equation for an n-channel transistor operating in the triode region.

$$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS} - V_{tn})V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{15.83}$$

Also recall that a transistor remains in the triode region as long as the drain-source voltage is lower than the effective gate-source voltage. In other words, the following condition must be satisfied:

$$V_{DS} < V_{eff} \quad \text{where } V_{eff} = V_{GS} - V_{tn} \tag{15.84}$$

We will see next that if the preceding equations were exact, then perfectly linear circuits could be realized. However, these equations are only mildly accurate for a modern short-channel process, and therefore some distortion occurs because higher-order terms are not modelled in the preceding equations. Hence, almost all practical continuous-time circuits use fully differential architectures (see Section 10.3) to reduce even-order distortion products, leaving the third-order term to dominate.

Transconductors Using a Fixed-Bias Triode Transistor

We see from (15.83) that if a small drain-source voltage, V_{DS}, is used, the V_{DS}^2 term goes to zero quickly and the drain current is approximately linear with respect to an applied drain-source voltage. Thus, we can model a transistor in triode as a resistor given by

$$r_{DS} \equiv \left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1}\Bigg|_{v_{DS}=0} \tag{15.85}$$

which results in a small-signal resistance of

$$r_{DS} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{GS} - V_{tn}\right)} \tag{15.86}$$

One approach for using this equivalent resistance to realize a transconductor with moderate linearity is shown in Fig. 15.21 [Welland, 1994]. This circuit has the same structure as that of the bipolar circuit of Fig. 15.14. However, here the bipolar transistors are replaced with their MOSFET counterparts (biased in the active region), and the resistor is replaced with a transistor operating in the triode region. Note that the circuit of Fig. 15.21 forces constant currents through Q_1 and Q_2 (as in the bipolar case) such that their individual gate-source voltages remain constant. As a result, the

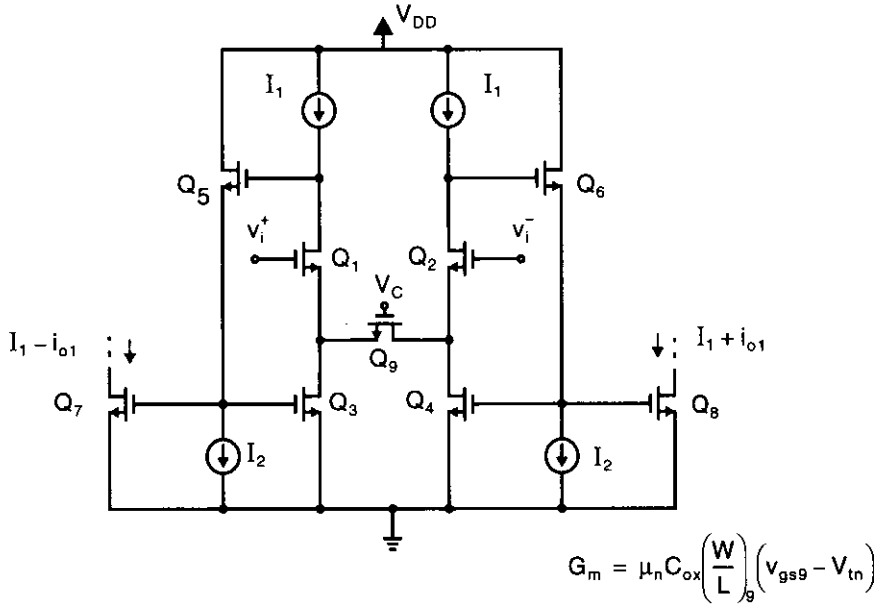


Fig. 15.21 A CMOS transconductor using Q_9 in the triode region.

transconductance of this cell is equal to the inverse of the small-signal resistance, r_{ds}, of Q_9. Using the small-signal resistance result of (15.86), the overall transconductance of this cell is given by

$$G_m = \frac{i_{o1}}{v_i^+ - v_i^-} = \mu_n C_{ox}\left(\frac{W}{L}\right)_9 (V_{gs9} - V_{tn}) \tag{15.87}$$

Thus, this transconductor has a variable transconductance value that can be adjusted by changing the value of V_{gs9}. As in the bipolar case, this transconductance value can be scaled by scaling the current mirrors Q_7 and Q_8 with respect to Q_3 and Q_4.

A similar approach but with reduced complexity and fewer p-channel inputs is shown in Fig. 15.22 [Kwan, 1991]. Here, a constant current of I_2 is forced through each of Q_1 and Q_2, whereas the dc bias current for each of Q_3 and Q_4 equals the difference between I_1 and I_2. The signal current, i_{o1}, also flows through Q_3 and Q_4, which is mirrored to the output transistors, Q_5 and Q_6. Note that this configuration has one less transistor stage around the input transistor loops. Specifically, the Q_5 and Q_6 source followers shown in Fig. 15.21 are not required in the circuit of Fig. 15.22, which usually results in a speed advantage for the latter.

An advantage of the transconductors in Figs. 15.21 and 15.22 (and other similar ones) is that they are easily modified to have multiple outputs by simply including output transistors. For example, the transconductor in Fig. 15.22 with two outputs is shown in Fig. 15.23. These additional transistors can be scaled for any desired ratio of output currents. These multiple outputs often allow filters to be realized using fewer transconductors. For example, a biquad similar to that in Fig. 15.11, but using multiple-output transconductors, is shown in Fig. 15.24. The transconductors are now associated with the outputs rather than the inputs. There is one transconductor per filter order plus an additional one for the input conversion from voltage to current. This approach has resulted in a savings of two transconductors. Not only does this approach save die area, but, often more importantly, it saves power.

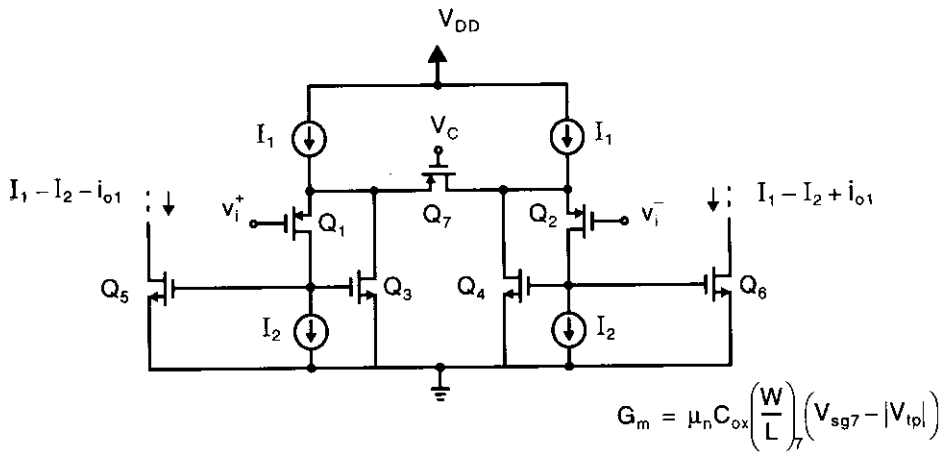


Fig. 15.22 A CMOS transconductor with p-channel inputs.

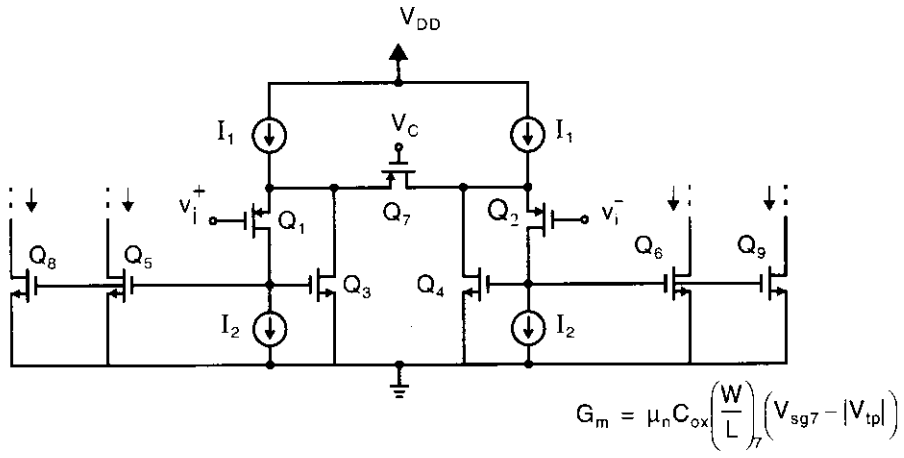


Fig. 15.23 A multiple-output CMOS transconductor.

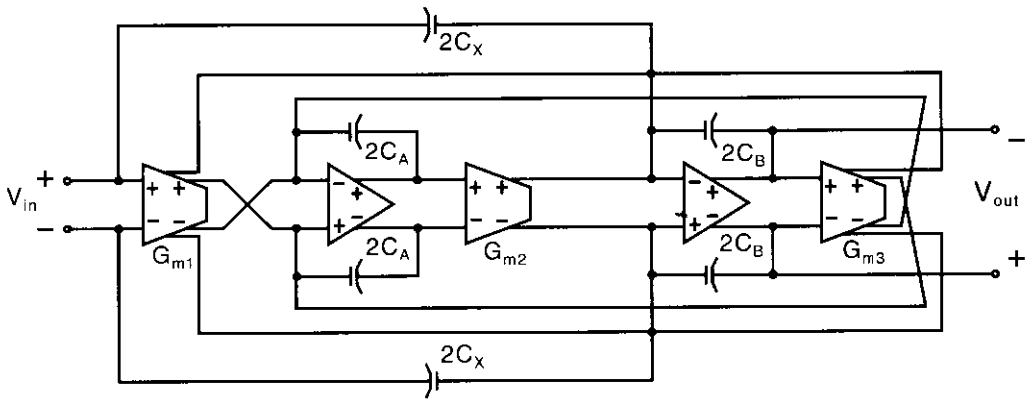
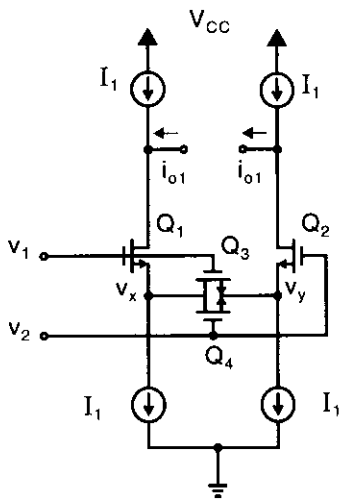


Fig. 15.24 A general biquad realized using multiple-output transconductors.

The biquad in Fig. 15.24 illustrates the use of Miller integrators. Because Miller integrators are used, the interconnects are all low-impedance nodes with current signals rather than voltage signals. This helps make these nodes insensitive to capacitively coupled noise and interconnect resistance. This current-mode style of design is increasing in popularity.

Transconductors Using Varying Bias-Triode Transistors

Another way to linearize a MOSFET differential stage, using transistors primarily in the triode region, is shown in Fig. 15.25 [Krummenacher, 1988]. Note that here the gates of transistors Q_3, Q_4 are connected to the differential input voltage rather than to a bias voltage. As a result, triode transistors Q_3 and Q_4 undergo varying bias con-



$$G_m = \frac{4k_1k_3\sqrt{I_1}}{(k_1 + 4k_3)\sqrt{k_1}}$$

Fig. 15.25 A linearized CMOS differential pair using transistors Q_3, Q_4 primarily in the triode region. The top pair of current sources can be set equal to the bottom pair through the use of a common-mode feedback.

ditions to improve the linearity of this circuit (as discussed shortly). To see that Q_3 and Q_4 are generally in the triode region, we look at the case of equal input signals (i.e., $v_1 = v_2$), resulting in

$$v_x = v_y = v_1 - v_{GS1} = v_1 - (v_{eff1} + V_{tn}) \tag{15.88}$$

Thus, the drain-source voltages of Q_3, Q_4 are both zero. However, their gate-source voltages equal those of Q_1, Q_2, implying that they are indeed in the triode region.

To determine the small-signal transconductance of this stage, we note from (15.86) that the small-signal drain-source resistance of Q_3, Q_4 is given by

$$r_{ds3} = r_{ds4} = \frac{1}{2k_3(V_{GS1} - V_{tn})} \tag{15.89}$$

where we have assumed that Q_3 and Q_4 are matched devices and have defined

$$k_3 = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_3 \tag{15.90}$$

Note that in this circuit we cannot ignore the effect of the varying gate-source voltages of Q_1 and Q_2 since their drain currents are not fixed to a constant value (as in Fig. 15.21). The small-signal source resistance values of Q_1 and Q_2 are given by

$$r_{s1} = r_{s2} = \frac{1}{g_{m1}} = \frac{1}{2k_1(V_{GS1} - V_{tn})} \tag{15.91}$$

Using the small-signal T model, we find the small-signal output current of i_{o1} to be equal to

$$i_{o1} = \frac{v_1 - v_2}{r_{s1} + r_{s2} + (r_{ds3} \parallel r_{ds4})} \tag{15.92}$$

Thus, defining $G_m \equiv i_{o1}/(v_1 - v_2)$, we have

$$G_m = \frac{1}{r_{s1} + r_{s2} + (r_{ds3} \parallel r_{ds4})} \tag{15.93}$$

which can be shown to be

$$G_m = \frac{4k_1k_3(V_{GS1} - V_{tn})}{k_1 + 4k_3} \tag{15.94}$$

Finally, to modify this result such that it is in terms of current, we note that

$$I_1 = k_1(V_{GS1} - V_{tn})^2 \tag{15.95}$$

or, equivalently,

$$(V_{GS1} - V_{tn}) = \sqrt{\frac{I_1}{k_1}} \tag{15.96}$$

which leads to

$$G_m = \frac{4k_1k_3\sqrt{I_1}}{(k_1 + 4k_3)\sqrt{k_1}} \tag{15.97}$$

Thus, we see that the transconductance of this transconductor can be tuned by changing the bias current, I_1. Note also that the transconductance is proportional to the square root of the bias current as opposed to a linear relation in the case of a bipolar transconductor.

To see how varying bias conditions for the triode transistors improves the linearity of this circuit, first consider the case of small differences in v_1 and v_2 (say, 100 mV). In this small-input-signal case, Q_3 and Q_4 essentially act as two source degeneration resistors. Thus, linearity improves (assuming $r_{ds3} >> r_{s1}$) over that of a simple differential pair, since transistors in triode are more linear than the source resistances of transistors in the active region. In other words, for a small-input-signal value, the linearity of this circuit is similar to that for a circuit in which the gates of Q_3, Q_4 are connected to fixed-bias voltages. However, if the gates of Q_3, Q_4 *were* connected to fixed-bias voltages, (15.83) shows that, as the drain-source voltage is increased, the drain current is reduced below that which would occur in a linear relationship due to the squared v_{DS} term. In addition, the changing values of V_{GS1} and V_{GS2} (due to current changes) also reduce the value of V_{DS}, and hence the transconductance of the cell for large input signals. To alleviate this reduction in transconductance for large input signals, the gates of Q_3 or Q_4 are connected to the input signals as shown. Now, as the input signal is increased, the small-signal resistance of one of the two triode transistors in parallel, Q_3 or Q_4, is reduced. This reduced resistance attempts to increase the transconductance, resulting in a partial cancelling of the decreasing transconductance value. Thus, if a proper ratio of k_1/k_3 is chosen, a more

stable transconductance (and hence better linearity) is achieved. For a 4-MHz filter presented in [Krummenacher, 1988], a ratio of $k_1/k_3 = 6.7$ is used to obtain distortion levels around 50 dB below the maximum output signal level of 350 mVrms. Also, an extension of this approach is presented in [Silva-Martinez, 1991], where the input signal is split over two input stages to further improve the distortion performance.

EXAMPLE 15.7

Consider the circuit of Fig. 15.25 with the following values: $I_1 = 100\ \mu A$, $\mu_n C_{ox} = 96\ \mu A/V^2$, $(W/L)_1 = (W/L)_2 = 20$, $(W/L)_3 = 3$, and $v_2 = 0$ V.

1. Assuming a perfectly linear transconductor, use (15.97) to find i_{o1} when v_1 equals 2.5 mV and 250 mV.
2. Assume the gates of Q_3, Q_4 are connected to ground and use classical models for both the triode and active regions. Find the true value of i_{o1} when v_1 equals 2.5 mV and 250 mV. Compare your results with those in part 1.
3. Repeat part 2, assuming the gates of Q_3, Q_4 are connected to the input signals as shown in Fig. 15.25.

Solution

1. For the given values, we have

$$k_1 = \frac{96}{2} \times 20 = 960\ \mu A/V^2 \tag{15.98}$$

$$k_3 = \frac{96}{2} \times 3 = 144\ \mu A/V^2 \tag{15.99}$$

and substituting the above values in (15.97), we have

$$G_m = \frac{4k_1k_3\sqrt{100}}{(k_1 + 4k_3)\sqrt{k_1}} = 116.2\ \mu A/V \tag{15.100}$$

Now, to find i_{o1}, we use the definition of G_m to find

$$i_{o1} = G_m(v_1 - v_2) = G_m v_1 \tag{15.101}$$

Thus, for $v_1 = 2.5$ mV, we have $i_{o1} = 0.2905\ \mu A$. However, if $v_1 = 250$ mV, then $i_{o1} = 29.05\ \mu A$. In other words, for a 250-mV input voltage, the total drain current of Q_1 would be 129.05 μA, whereas that for Q_2 would be 70.95 μA.

2. To find i_{o1} in this case, we first note that the sum of the drain currents in Q_1 and Q_2 must equal the total bias current, 200 μA. In other words,

$$i_{D1} + i_{D2} = 2I_1 = 200\ \mu A \tag{15.102}$$

And since (using $v_{effi} = v_{GS} - V_{tn}$) the drain currents in Q_1 and Q_2 are given by

$$i_{D1} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_1 (v_{eff1}^2) \quad \text{and} \quad i_{D2} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_2 (v_{eff2}^2) \tag{15.103}$$

we can write (15.102) as

$$v_{eff1}^2 + v_{eff2}^2 = \frac{5}{24} V^2 \tag{15.104}$$

The current from node v_x to v_y through the two triode transistors is given by

$$i_{xy} = 2 \times i_{D3} = 2\mu_n C_{ox}\left(\frac{W}{L}\right)_3 \left(v_{eff2} v_{xy} - \frac{v_{xy}^2}{2}\right) \tag{15.105}$$

where we have noted that $v_{eff3} = v_{eff2}$. The sum of i_{xy} and i_{D2} must equal I_1, resulting in

$$960 v_{eff2}^2 + 576\left(v_{eff2} v_{xy} - \frac{v_{xy}^2}{2}\right) = 100 \tag{15.106}$$

Finally, we note that the input signal is equal to the following sum (the threshold voltage terms cancel):

$$-v_{eff2} + v_{xy} + v_{eff1} = v_{in} \tag{15.107}$$

Equations (15.104), (15.106), and (15.107) can be solved using an equation solver and then choosing the solution that has all positive values.

For a value of $v_{in} = 2.5$ mV, the following results are obtained.

$$\begin{aligned} v_{eff1} &= 0.32322 \text{ V} \\ v_{eff2} &= 0.32228 \text{ V} \\ v_{xy} &= 0.0015648 \text{ V} \end{aligned} \tag{15.108}$$

These values of effective gate voltages imply that the drain currents are

$$i_{D1} = 100.2898 \ \mu\text{A} \qquad i_{D2} = 99.7104 \ \mu\text{A} \tag{15.109}$$

which, in turn, imply that

$$i_{o1} = i_{D1} - 100 \ \mu\text{A} = 0.2898 \ \mu\text{A} \tag{15.110}$$

Such a result agrees closely with that of part 1.

However, for the case of $v_{in} = 250$ mV, we have

$$\begin{aligned} v_{eff1} &= 0.35452 \text{ V} \\ v_{eff2} &= 0.28749 \text{ V} \\ v_{xy} &= 0.18297 \text{ V} \end{aligned} \tag{15.111}$$

resulting in $i_{o1} = 20.66\ \mu A$. This result is about 30 percent lower than that expected by a linear transconductor value of 29.05 μA, as found in part 1.

3. Finally, if the gates are connected to the input signal, the preceding equations in part 2 remain the same, except for i_{xy}, which is now the sum of i_{D3} and i_{D4}, resulting in,

$$i_{xy} = \mu_n C_{ox}\left(\frac{W}{L}\right)_3\left[(v_{eff2} + v_{in})v_{xy} - \frac{v_{xy}^2}{2}\right] + \mu_n C_{ox}\left(\frac{W}{L}\right)_4\left(v_{eff2}v_{xy} - \frac{v_{xy}^2}{2}\right) \tag{15.112}$$

and so (15.105) is replaced with

$$960v_{eff2}^2 + 576[(2v_{eff2} + v_{in})v_{xy} - v_{xy}^2] = 100 \tag{15.113}$$

Once again, using an equation solver, we find that in the case of $v_{in} = 2.5$ mV, the results are essentially the same as in parts 1 and 2. However, in the case of $v_{in} = 250$ mV, we find that

$$\begin{aligned} v_{eff1} &= 0.36620\ \text{V} \\ v_{eff2} &= 0.27245\ \text{V} \\ v_{xy} &= 0.15625\ \text{V} \end{aligned} \tag{15.114}$$

These values lead to $i_{o1} = 28.74\ \mu A$, which is only 1 percent below that expected by a linear transconductor value of 29.05 μA.

Transconductors Using Constant Drain-Source Voltages

Recall, once again, the classical model for a transistor biased in the triode region,

$$i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS} - V_{tn})V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{15.115}$$

We see here that if the drain-source voltage, V_{DS}, is kept constant, the drain current is linear with respect to an applied gate-source voltage (ignoring the dc offset current due to the squared V_{DS} term) [Pennock, 1985]. Unfortunately, this simple model does not account for important second-order effects (such as velocity saturation and mobility degradation) that severely limit the accuracy of the preceding equation model. However, if fully differential structures are used to cancel even-order error terms, a reasonably linear transconductor (around 50 dB) can be built using this constant-V_{DS} approach.

One possible implementation based on the linearization scheme just described is shown in Fig. 15.26. Here, Q_1 and Q_2 are placed in the triode region and their drain-source voltages are set equal to V_C through the use of Q_3, Q_4 and two extra amplifiers.

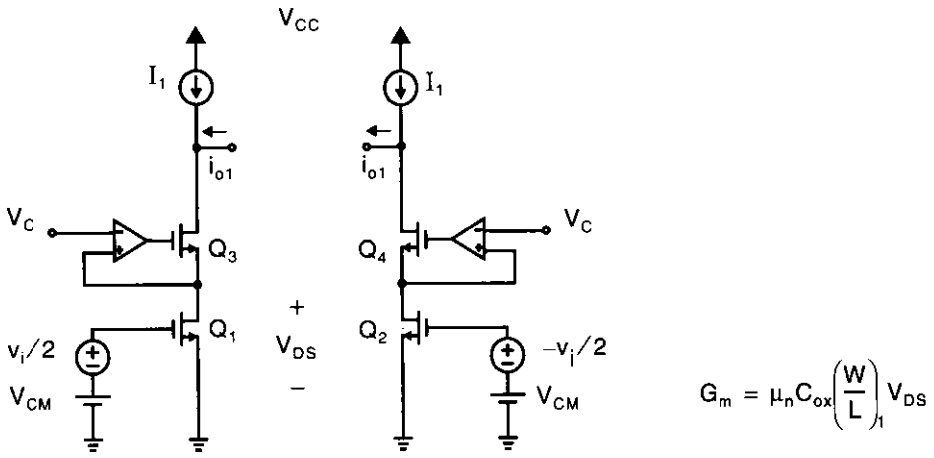


Fig. 15.26 A differential transconductor using triode transistors that have constant drain-source voltages. The control signal, V_C, adjusts the transconductance value, whereas V_{CM} is a fixed common-mode voltage. The top current pair, I_1, is set equal to the bias current through Q_1, Q_2, using a common-mode feedback circuit (not shown).

The differential input signal is applied to the gates of Q_1, Q_2 and is superimposed on a constant common-mode voltage signal, V_{CM}. An alternative design here is to use an extra opamp to create a G_m-C opamp integrator [Wong, 1989].

For the circuit of Fig. 15.26, we have

$$i_{D1} = \mu_n C_{ox}\left(\frac{W}{L}\right)_1\left[\left(\frac{v_i}{2} + V_{CM} - V_{tn}\right)V_{DS} - V_{DS}^2/2\right] \tag{15.116}$$

Noting that i_{o1} is the difference between this current and I_1, which is set via a common-mode feedback signal equal to

$$I_1 = \mu_n C_{ox}\left(\frac{W}{L}\right)_1\left[(V_{CM} - V_{tn})V_{DS} - V_{DS}^2/2\right] \tag{15.117}$$

we then have

$$i_{o1} = i_{D1} - I_1 = \mu_n C_{ox}\left(\frac{W}{L}\right)_1\left(\frac{v_i}{2}\right)V_{DS} \tag{15.118}$$

Then, defining $G_m \equiv i_{o1}/v_i$ results in

$$G_m = \mu_n C_{ox}\left(\frac{W}{L}\right)_1 V_{DS} \tag{15.119}$$

Note that here the transconductance value is proportional to the drain-source voltage, and from (15.117), we see that the bias current is also approximately proportional to the drain-source voltage (if V_{DS} is small).

EXAMPLE 15.8

Consider the circuit shown in Fig. 15.26, where $\mu_n C_{ox} = 96\ \mu A/V^2$, $(W/L)_1 = (W/L)_2 = 10$, $V_{tn} = 0.8$ V, and $V_{CM} = 2$ V. Find the transconductance value when $V_C = 0.2$ V and when $V_C = 0.4$ V. For these two control-signal values, also find the bias currents through Q_1 and Q_2 (i.e., when $v_i = 0$) and the maximum input signal swing before either transistor exits the triode region (assume the classical transistor model).

Solution

Using (15.119), for $V_C = 0.2$ V, we have

$$G_m = 96\ \mu A/V^2 \times 10 \times 0.2\ V = 0.192\ mA/V$$

Also, the bias current through Q_1 or Q_2 for this V_C value can be found using (15.117):

$$I_1 = 96\ \mu A/V^2 \times 10\left[(2-0.8)0.2 - \frac{0.2^2}{2}\right] = 0.211\ mA$$

Finally, to remain in the triode region, the *effective* gate-source voltages of Q_1 and Q_2 must remain above $V_{DS} = 0.2$ V. In other words, their gate-source voltages must remain above $V_{DS} + V_t = 1.0$ V. Since the common-mode voltage, V_{CM}, equals 2 V, the negative portion, $v_i/2$, must not go below a level of -1 V, otherwise the transistor will enter the active region. Thus, a maximum differential input voltage, v_i, of 2 V can be applied in this case.

Similarly, for $V_C = 0.4$ V, we have twice the transconductance value of $G_m = 0.384$ mA/V. Here, the bias current is found to be $I_1 = 0.384$ mA and the maximum input signal swing is a differential voltage of $v_i = 1.6$ V. Note that doubling the drain-source voltage doubles the transconductance (as expected) but requires almost a doubling of the bias current and a loss of signal swing.

15.4 CMOS TRANSCONDUCTORS USING ACTIVE TRANSISTORS

In general, CMOS transconductors based on the use of active transistors[2] have worse linearity performance than their triode-based counterparts. However, active-based designs often have improved speed performance (assuming equal bias currents in the two cases). The linearity of active-transistor transconductors is only moderate (around 30 to 50 dB) because they rely on the square-law model of MOS transistors, which is not very accurate (particularly in short-channel processes). In addition, only the difference

2. Active transistors are those transistors that operate in the active region. The active region is also known as the pinch-off, or saturation, region. This active region for an n-channel transistor occurs when V_{GS} is greater than V_{tn} and $V_{DS} \geq V_{GS} - V_{tn} = V_{eff}$.

in output currents is ideally linear, whereas individual currents have significant second-order harmonics. Thus, second-order harmonic distortion also occurs if the difference is not taken precisely.

We should mention here that not all linearization techniques using active transistors are discussed. For example, one approach not discussed is a technique in which the tail current of a differential pair is adaptively biased [Nedungadi, 1984]. This technique is limited in its frequency response, and thus a designer would usually choose a triode-based design instead. In summary, in this section we present CMOS linearization techniques intended for high-speed operation and only moderate linearity.

CMOS Pair

Before proceeding to look at transconductor circuits that have active transistors, it is worthwhile to introduce a two-transistor circuit known as the *CMOS pair*, as shown in Fig. 15.27 [Seevinck, 1987]. As we will show, this two-transistor pair acts as a single transistor, assuming that both transistors remain in the active region. Such an observation allows one to more easily derive some of the CMOS transconductors described later in this section.

To show that this two-transistor pair acts as a single transistor, we first assume that both transistors remain in the active region. Thus, we can write their drain currents as

$$I_D = K_n(V_{GSn} - V_{tn})^2 \qquad \text{where } V_{tn} > 0 \tag{15.120}$$

and

$$I_D = K_p(V_{SGp} + V_{tp})^2 \qquad \text{where } V_{tp} < 0 \tag{15.121}$$

Rearranging these two equations in terms of their gate-source voltages gives

$$V_{GSn} = V_{tn} + \frac{1}{\sqrt{K_n}}\sqrt{I_D} \tag{15.122}$$

and

$$V_{SGp} = -V_{tp} + \frac{1}{\sqrt{K_p}}\sqrt{I_D} \tag{15.123}$$

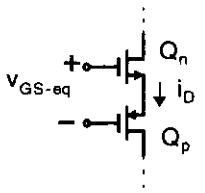
Defining the equivalent gate-source voltage, $V_{GS\text{-}eq}$, to be the difference between the two gate voltages, we have

$$V_{GS\text{-}eq} \equiv V_{GSn} + V_{SGp} = (V_{tn} - V_{tp}) + \left(\frac{1}{\sqrt{K_n}} + \frac{1}{\sqrt{K_p}}\right)\sqrt{I_D} \tag{15.124}$$

Since this equation has the same form as those for a single transistor (equations (15.122) and (15.123)), we define the equivalent threshold voltage, $V_{t\text{-}eq}$, as

$$V_{t\text{-}eq} \equiv V_{tn} - V_{tp} \qquad \text{where } V_{tn} > 0 \text{ and } V_{tp} < 0 \tag{15.125}$$

and we define the equivalent device parameter, K_{eq}, as



$$i_D = K_{eq}\left(v_{GS-eq} - V_{t-eq}\right)^2$$

$$K_{eq} = \frac{K_n K_p}{\left(\sqrt{K_n} + \sqrt{K_p}\right)^2}$$

$$V_{t-eq} = V_{tn} - V_{tp}$$

(where $V_{tn} > 0$ and $V_{tp} < 0$)

Fig. 15.27 A CMOS double pair, where both transistors are in the active region. The transistor pair is equivalent to a single transistor with an equivalent threshold voltage, V_{t-eq}, and device parameter, K_{eq}.

$$\frac{1}{\sqrt{K_{eq}}} \equiv \frac{1}{\sqrt{K_n}} + \frac{1}{\sqrt{K_p}} \tag{15.126}$$

which can be rewritten as

$$K_{eq} = \frac{K_n K_p}{\left(\sqrt{K_n} + \sqrt{K_p}\right)^2} \tag{15.127}$$

Finally, combining (15.124), (15.125), and (15.127) and rearranging, we see that when both transistors are in their active regions, the drain current can be written as

$$i_D = K_{eq}(v_{GS-eq} - V_{t-eq})^2 \tag{15.128}$$

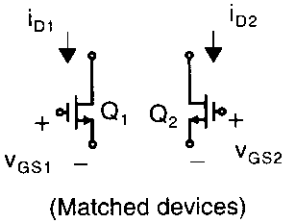
where K_{eq}, V_{GS-eq}, and V_{t-eq} are defined as just described. Clearly, this equation is in the same form as that for a single transistor, and thus this two-transistor pair can replace single transistors in many circuits. As we will see next, this replacement can be quite useful in designing linear transconductor circuits.

Constant Sum of Gate-Source Voltages

One popular approach for creating an active transistor transconductor is by using a constant sum of gate-source voltages, as shown in Fig. 15.28. Assuming the two transistors are operating in the active region (i.e., the drain voltages are high and each of v_{GS1} and v_{GS2} remain greater than V_{tn}), the output differential current is given by

$$(i_{D1} - i_{D2}) = K\left(v_{GS1} + v_{GS2} - 2V_{tn}\right)(v_{GS1} - v_{GS2}) \tag{15.129}$$

Here, the *output differential current is linear if the sum of the two gate-source voltages remains constant.* As we will see next, there are a variety of ways to make the sum of the gate-source voltages remain constant when applying an input signal. One important point to note here is that, although the differential current is linear, the individual drain currents are not linear. Thus, if the subtraction between currents has some



$$K = (\mu_n/2)C_{OX}\left(\frac{W}{L}\right)$$

$$i_{D1} = K\left(v_{GS1} - V_{tn}\right)^2 \quad \text{and} \quad i_{D2} = K\left(v_{GS2} - V_{tn}\right)^2$$

$$(i_{D1} - i_{D2}) = K\left(v_{GS1} + v_{GS2} - 2V_{tn}\right)\left(v_{GS1} - v_{GS2}\right)$$

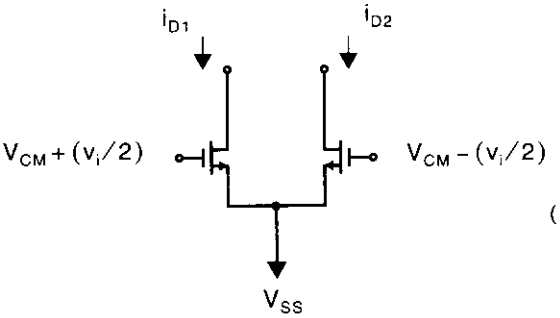
Fig. 15.28 Two-transistor circuit in which the difference in the drain currents is linear with respect to $(v_{GS1} - v_{GS2})$ if the sum of the two gate-source voltages remains constant. Transistors are matched and in the active region.

error (as it certainly will), some distortion products will occur even if perfect square-law devices are obtainable.

Source-Connected Differential Pair

One approach to maintain a constant sum of gate-source voltages is to apply a balanced differential input voltage, as shown in Fig. 15.29. Here, the differential pair is biased using the dc common-mode voltage, V_{CM}, whereas the input signal varies *symmetrically* around this common-mode voltage. Note that, from the preceding analysis, this input signal symmetry is important in maintaining linearity. However, in practice, a slightly nonbalanced input signal is not the dominant source of nonlinearity. Specifically, the linearity achievable with this approach is quite limited because MOS transistors are not well modelled by square-law behavior. In addition, it is difficult to obtain a precise difference between the two drain currents, which also causes even-order harmonics. As a result, this technique is typically limited to less than 50 dB of linearity.

To tune the transconductance of this circuit, the common-mode voltage, V_{CM}, can be adjusted. However, it should be noted that, in a short-channel process and when moderate gate-source voltages are used, carrier velocity saturation occurs and limits the transconductance variation. In addition, one should be aware that as the input



$$(i_{D1} - i_{D2}) = 2K\left(V_{CM} - V_{SS} - V_{tn}\right)(v_i)$$

$$G_m = 2K\left(V_{CM} - V_{SS} - V_{tn}\right)$$

Fig. 15.29 A source-connected differential-pair transconductor. The differential input signal must be balanced around V_{CM} for linearization of the transistor square-law relation to occur.

common-mode voltage is adjusted, linearity performance and maximum signal swing levels change as well. One example of this approach is presented in [Snelgrove, 1992] where speeds up to 450 MHz are demonstrated in a 0.9-μm CMOS process with around a 30- to 40-dB dynamic range performance.

Inverter-Based

A transconductor approach similar to the source-connected differential pair is the inverter-based transconductor, shown in Fig. 15.30 [Park, 1986]. Here, two CMOS pairs, Q_{1a}, Q_{1b} and Q_{2a}, Q_{2b}, have replaced the two individual transistors in a traditional CMOS inverter, and the difference in their output currents is the overall output current, i_o. Assuming that all four transistors are in the active region and that the two CMOS pairs are matched, we can use the previous results on CMOS pairs to write

$$i_1 = K_{eq}(V_{GS\text{-}eq1} - V_{t\text{-}eq})^2 \tag{15.130}$$

and

$$i_2 = K_{eq}(V_{GS\text{-}eq2} - V_{t\text{-}eq})^2 \tag{15.131}$$

Note here that these equations are in the same form as those shown in Fig. 15.28. Thus, as in (15.129), the output current is given by

$$i_o \equiv i_1 - i_2 = K_{eq}(V_{GS\text{-}eq1} + V_{GS\text{-}eq2} - 2V_{t\text{-}eq})(V_{GS\text{-}eq1} - V_{GS\text{-}eq2}) \tag{15.132}$$

Thus, the output current is linearly related to the difference in equivalent gate-source voltages of the CMOS pairs if the sum of their equivalent gate-source voltages is a constant value. To see that a constant equivalent gate-source voltage sum occurs, we have

$$V_{GS\text{-}eq1} = V_{C1} - v_{in} \tag{15.133}$$

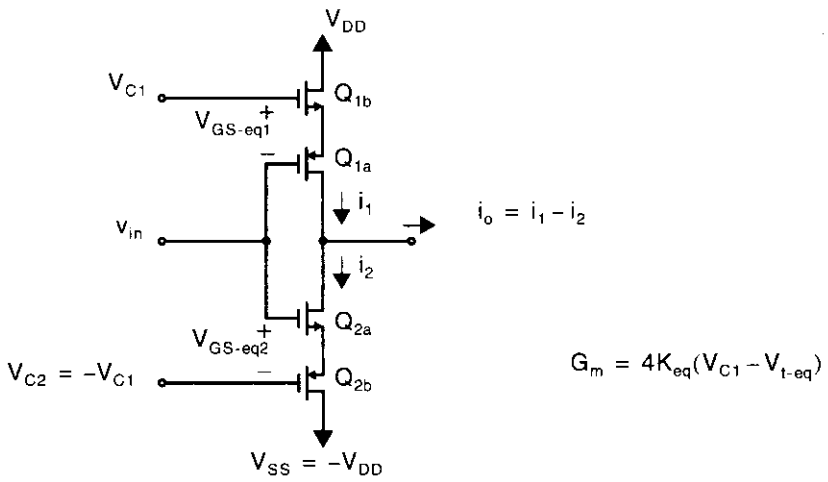


Fig. 15.30 Complementary differential-pair transconductor using CMOS pairs.

and

$$V_{GS\text{-}eq2} = v_{in} - V_{C2} \tag{15.134}$$

and therefore

$$V_{GS\text{-}eq1} + V_{GS\text{-}eq2} = V_{C1} - V_{C2} \tag{15.135}$$

Also, the difference in equivalent gate-source voltages is given by

$$V_{GS\text{-}eq1} - V_{GS\text{-}eq2} = V_{C1} + V_{C2} - 2v_{in} \tag{15.136}$$

Finally, in the case where we choose $V_{C2} = -V_{C1}$, we have

$$i_o = 4K_{eq}(V_{C1} - V_{t\text{-}eq})(v_{in}) \tag{15.137}$$

and the transconductance value can be varied by changing the control voltages, V_{C1} and V_{C2} (which, incidentally, are high-input impedance nodes and thus are easily adjustable). Note that, with this transconductor, matching need occur only for transistors of the same type. Specifically, the n-channel transistors should match and the p-channel transistors should match, but there is no need to match n- and p-channel transistors to each other.

Differential-Pair with Floating Voltage Sources

Another approach to maintain a constant sum of gate-source voltages is by using two floating dc voltage sources, as shown in Fig. 15.31 [Nedungadi, 1984]. Writing a voltage equation around the loop, we have

$$v_{GS1} - (V_x + V_{tn}) + v_{GS2} - (V_x + V_{tn}) = 0 \tag{15.138}$$

and thus,

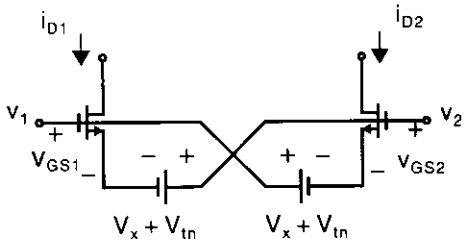
$$v_{GS1} + v_{GS2} = 2(V_x + V_{tn}) \tag{15.139}$$

As a result, this circuit maintains a constant sum of gate-source voltages even if the applied differential signal is not balanced. Also, writing two equations that describe the relationship between v_1 and v_2, we have

$$v_1 - v_{GS1} + V_x + V_{tn} = v_2 \tag{15.140}$$

and

$$v_2 - v_{GS2} + V_x + V_{tn} = v_1 \tag{15.141}$$



$$(i_{D1} - i_{D2}) = 4KV_x(v_1 - v_2)$$

$$G_m = 4KV_x$$

Fig. 15.31 A linearized differential pair using floating voltage sources.

Subtracting (15.140) from (15.141) and rearranging, we obtain

$$v_{GS1} - v_{GS2} = 2(v_1 - v_2) \tag{15.142}$$

Thus, the difference between the input voltages is equal to one half the difference between the gate-source voltages. Finally, the differential output current is found by combining (15.129), (15.139), and (15.142) to give

$$(i_{D1} - i_{D2}) = 4KV_x(v_1 - v_2) \tag{15.143}$$

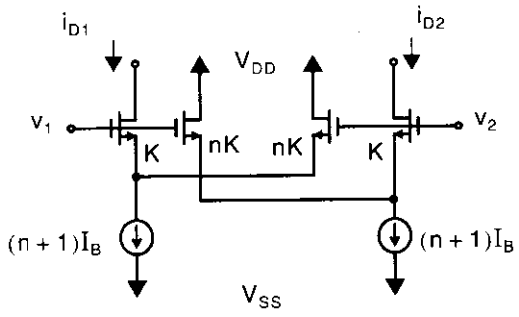
One simple way to realize the floating voltage sources of Fig. 15.31 is to use two source followers, as shown in Fig. 15.32 [Nedungadi, 1984]. The transistors labelled nK are n times larger than the other two transistors, and thus they act as source followers when n is large (typically, when n is 5 or greater). If n is not large, the bias current through the two source followers changes as the input signal is applied and linearity is worsened. A disadvantage of this circuit is that a large dc bias current passes through the two source followers. However, if only moderate linearity is desired and the input signal is relatively small (say, 500 mV), then this approach can be quite useful.

Since it is difficult to realize a floating voltage source that drives the source of another transistor, another approach is to modify the circuit of Fig. 15.31 such that the floating voltage sources need drive only the transistor gates. Such a modification is possible by replacing the single transistors shown in Fig. 15.31 with their CMOS pairs, as shown in Figure 15.33. Note that the voltage sources must now be larger than $V_{t\text{-}eq}$ and must include a controllable V_x voltage. Fortunately, such circuits are easily accomplished by using two more CMOS pairs, as shown in Fig. 15.34, where the pairs Q_{3a}, Q_{3b} and Q_{4a}, Q_{4b} have been added together with two adjustable current sources [Seevinck, 1987]. Referring back to (15.128), we see that V_x is given by

$$V_x = \frac{1}{\sqrt{K_{eq}}}\sqrt{I_B} \tag{15.144}$$

where, for simplicity, we have assumed that all CMOS pairs are matched. As a result, the differential output current is given by

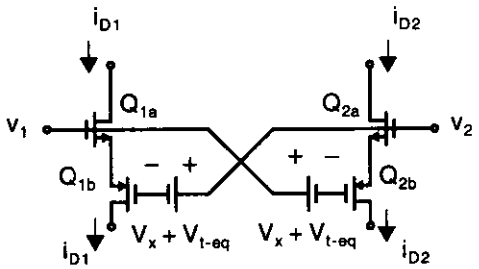
$$(i_{D1} - i_{D2}) = 4\sqrt{K_{eq}I_B}(v_1 - v_2) \tag{15.145}$$



$$(i_{D1} - i_{D2}) = \left(\frac{n}{n+1}\right)4\sqrt{KI_B}(v_1 - v_2)$$

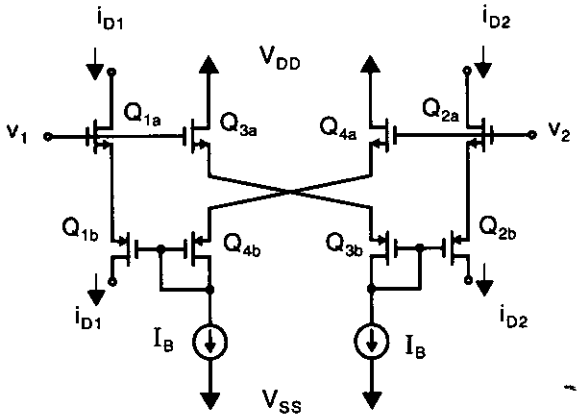
$$G_m = \left(\frac{n}{n+1}\right)4\sqrt{KI_B}$$

Fig. 15.32 A linear transconductor for large n.



$$(i_{D1} - i_{D2}) = 4K_{eq}V_x(v_1 - v_2)$$

Fig. 15.33 A linearized differential pair in which the floating voltage sources need drive only the transistor gates.



$$(i_{D1} - i_{D2}) = 4\sqrt{K_{eq}I_B}(v_1 - v_2)$$
$$G_m = 4\sqrt{K_{eq}I_B}$$

Fig. 15.34 A transconductor that uses CMOS pairs and floating voltage sources.

Thus, we see that the output current can be tuned by adjusting the dc bias current, I_B. Note that the transconductance coefficient is proportional to the square root of I_B and thus a fourfold increase in current results in only a factor of 2 coefficient increase.

Before leaving this circuit, a couple of points are worth mentioning. First, note that the output currents from this circuit are available at both the upper pair, Q_{1a}, Q_{2a}, as well as at the lower pair, Q_{1b}, Q_{2b}. Such flexibility may be useful in the remaining transconductor circuitry. Second, note that V_{SS} must be at least $V_{tn} + |V_{tp}|$ below the most negative input signal swing of either v_1 or v_2. If we assume v_1 and v_2 have ± 1-V signals associated with them around ground, then, for $V_{tn} = -V_{tp} = 1$ V, V_{SS} would have to be less than -3 V. Thus, assuming we have symmetrical power supplies, a 6-V power supply would be needed for only a 2-V signal swing. Finally, note that this circuit was discussed earlier in Chapter 6 as a class-AB input stage to improve the slew rate of an opamp (see Fig. 6.16 in Section 6.5). Thus, this particular class-AB input stage has a linear transconductance, when all transistors remain in the active region.

Bias-Offset Cross-Coupled Differential Pairs

Another approach to realize a transconductor with active transistors is to use two cross-coupled differential pairs where the input into one pair is intentionally voltage offset [Wang, 1990]. One implementation of this approach is shown in Fig. 15.35, where the differential pair Q_1, Q_2 is cross coupled with the bias-offset differential pair Q_3, Q_4. Here, we assume all transistors are in the active region and are matched (i.e., we assume all transistors have equal device parameters of K and equal threshold voltages of V_{tn}).

To find the differential output current, we first find

$$i_1 = K(v_1 - V_x - V_{tn})^2 + K(v_2 - V_B - V_x - V_{tn})^2 \tag{15.146}$$

and

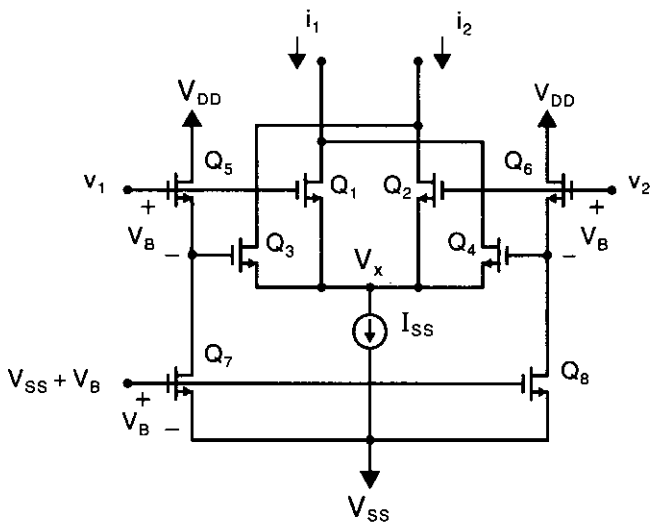
$$i_2 = K(v_2 - V_x - V_{tn})^2 + K(v_1 - V_B - V_x - V_{tn})^2 \tag{15.147}$$

Now finding the difference, $i_1 - i_2$, we have

$$(i_1 - i_2) = 2KV_B(v_1 - v_2) \tag{15.148}$$

Thus, the output differential current is linear with respect to the differential input voltage (as expected) and the transconductance value is proportional to V_B. Note, however, that the bias currents through Q_5, Q_6, Q_7, and Q_8 are all square-law related to V_B. Thus, the transconductance value is proportional to the square root of the changing bias current, as in the other active transistor CMOS transconductors. Also, note that the bias current, I_{SS}, does not affect the transconductance value but does determine the maximum (or minimum) output current available.

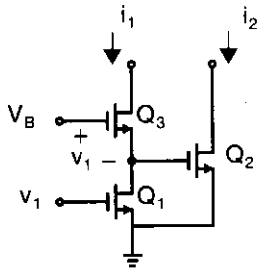
Finally, note that this offset-bias linearization technique can also be realized in a single-ended version with only a few transistors, as shown in Fig. 15.36 [Bult, 1987]. The analysis is left to the reader.



$$(i_1 - i_2) = 2KV_B(v_1 - v_2)$$

$$G_m = 2KV_B$$

Fig. 15.35 A bias-offset cross-coupled transconductor.



$$i_1 - i_2 = K\left(V_B - 2V_{tn}\right)\left(2v_1 - V_B\right)$$

Fig. 15.36 A single-ended offset-bias transconductor.

15.5 BICMOS TRANSCONDUCTORS

In this section, we discuss some of the reported approaches for realizing BiCMOS transconductors and filters.

Tunable MOS in Triode

One approach for realizing a BiCMOS integrator is shown in Fig. 15.37 [Laber, 1993]. Here, linearization and tuning are accomplished by using transistors Q_1 through Q_4, which are all assumed to be in the triode region. As we saw in Section 15.3, the currents through these transistors are ideally linear if their drain-source voltages are kept constant. Although in practice these currents have rather large

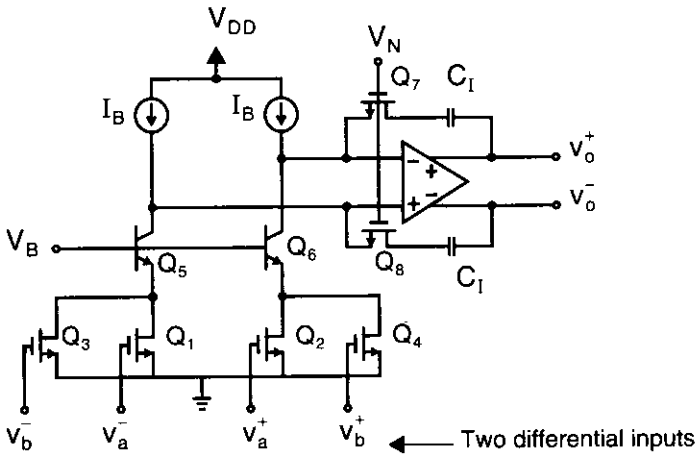


Fig. 15.37 A fully differential two-input BiCMOS integrator using MOS transistors in triode, Q_1 through Q_4. G_m-C opamp integration is used to reduce parasitic capacitance effects. Note that, in addition to a common-mode feedback circuit for the output (not shown), the common-mode voltage at the input nodes of the opamp must also be set.

second-order distortion, fortunately even-order distortion products are significantly reduced in a fully differential structure. The drain-source voltages of Q_1 through Q_4 are controlled through the use of the two emitter followers, Q_5, Q_6. This simple voltage control is one of the benefits of using a BiCMOS process since a MOS source follower would have too much voltage variation. Note that additional inputs into this integrator are added as simply two extra transistors (a two-input integrator is shown). Various coefficient ratios can be obtained by scaling the sizes of the input transistors. However, because of the shown tuning circuit connection, all coefficients in one integrator will scale together as the control voltage is varied. Note also that a G_m-C opamp integrator is used to reduce the effects of parasitic capacitance. Also, transistors Q_7, Q_8 are included to realize lead compensation. Finally, it should be mentioned that a common-mode feedback circuit is required at the output nodes of the differential opamp. Also, some method is needed for setting the common-mode voltage at the opamp inputs. The BiCMOS filter in [Laber, 1993] is built in a 1.5-μm, 4-GHz BiCMOS technology and operated around 20 MHz using a 5-V supply. The transconductor demonstrated moderate linearity of around 50 dB when processing 2-V_{pp} differential output signals, but no mention is made of any intermodulation results or the frequency of the test signals.

Fixed-Resistor Transconductor with a Translinear Multiplier

Another approach that has been successfully used to realize BiCMOS filters that have very high linearity has been to use highly linear transconductors realized using fixed resistors and then achieve tuning by following the transconductor with a translinear multiplier. As we saw in Chapter 8, the output of a translinear multiplier is linear with respect to one of its input currents, and its gain coefficient can be scaled as the ratio of two other currents in either a positive or negative fashion.

A translinear multiplier can be used for realizing a low-distortion BiCMOS integrator, as shown in Fig. 15.38 [Willingham, 1993]. Here, the output currents from fixed-value transconductors are applied to a translinear multiplier, such that tuning

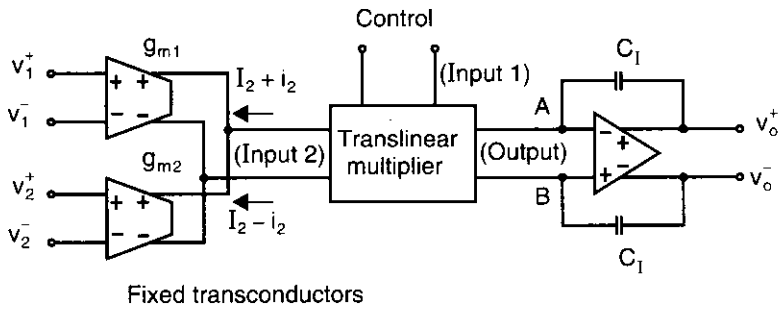


Fig. 15.38 A two-input BiCMOS integrator using fixed resistor-degenerated transconductors together with a translinear multiplier for tuning. The common-mode voltage at nodes A and B was set by using a low-input-impedance opamp.

can be accomplished while maintaining high linearity. The outputs of the translinear multiplier are applied to a Miller integrator to once again maintain high linearity. In this implementation, the input impedance of the fully differential opamp is kept low such that a fixed voltage occurs at the input nodes of the opamp, thereby setting the input common-mode voltage. Phase-lead resistors are also used in series with the integration capacitors (not shown) to improve the integrator's phase response.

The fixed transconductors are realized using resistor degeneration and local feedback, as shown in Fig. 15.39. Figure 15.39(*a*) shows that local feedback around the two shown opamps force their input nodes to be equal, and therefore the applied input voltage appears across R_x. A simplified circuit implementation of this approach is shown in Fig. 15.39(*b*), which shows that the opamps are implemented with only a PMOS transistor and current source.

This integrator was used to build a seventh-order low-pass filter in a 2-μm, 2.5-GHz BiCMOS process that featured thin-film resistors. The filter passband edge was tunable from 7.5 MHz to 10 MHz. The results of this low-distortion BiCMOS filter are quite impressive; third-order intermodulation products remained below 65 dB, with respect to the input signal, when measured using two-tone inputs near 4 MHz. Finally, it should be mentioned that the circuit also uses a center tap on each of the R_x resistors to set the common-mode voltage of the preceding output. With this simple addition, much of the traditional common-mode circuitry is eliminated since it is necessary only to compare the center tap voltage with a dc reference signal and then feed back the appropriate control signal.

Similar approaches, in which a highly linear transconductor that has local feedback is followed by a current attenuator, are also possible using ordinary CMOS and are now gaining in popularity [Chang, 1995].

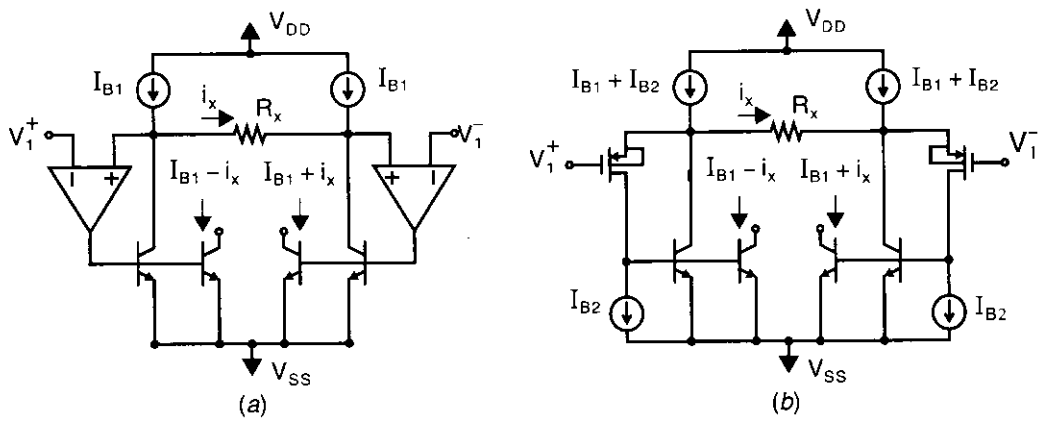


Fig. 15.39 A fixed BiCMOS transconductor: (*a*) the two local feedbacks keep the input voltage applied across R_x; (*b*) circuit implementation.

Fixed Active MOS Transconductor with a Translinear Multiplier

A BiCMOS integrator intended for applications that require high-speed operation, wide tuning range, and only moderate linearity is shown in Fig. 15.40 [Shoval, 1993]. In this circuit, the common-mode voltage, V_{CM}, is set to a constant value (it is set by a common-mode feedback circuit); the result is that the differential currents of Q_1, Q_4 and Q_2, Q_3 are linearly related to the balanced differential voltage (as discussed in Section 15.4). This linear voltage-to-current conversion remains at a fixed value (resulting in a relatively constant linearity performance and input swing level), and transconductance tuning is performed with the aid of a translinear multiplier. Note, however, that two pairs of MOS transistors are performing voltage-to-current conversion on the balanced input signal. The reason for using two pairs is to maximize the largest possible transconductance of the overall circuit for a given bias current. Specifically, if the multiplier is tuned to send all of i_{C6}, i_{C7} through to v_o^+, v_o^-, respectively, then the signal currents add together and the overall transconductance is equal to twice that which occurs for a single set of MOS transistors (without an increase in bias current). Alternatively, if the multiplier is tuned to send all of i_{C6}, i_{C7} through to v_o^-, v_o^+, respectively, then the currents subtract, causing a zero overall transconductance. Finally, if the translinear multiplier is tuned to cause a zero output (i.e., to cause two constant dc currents at the multiplier outputs), the overall transconductance is equal to that caused by transistors Q_2, Q_3, which is half the maximum value. Thus, the use of two pairs on the input signal doubles the maximum possible transconductance at the cost of being able to tune the transconductance only from zero to the maximum value. In other words, the overall transconductance value cannot change signs by changing the multiplier control signal. Of course, both positive and negative transconductance values can be obtained by cross-coupling the output signals.

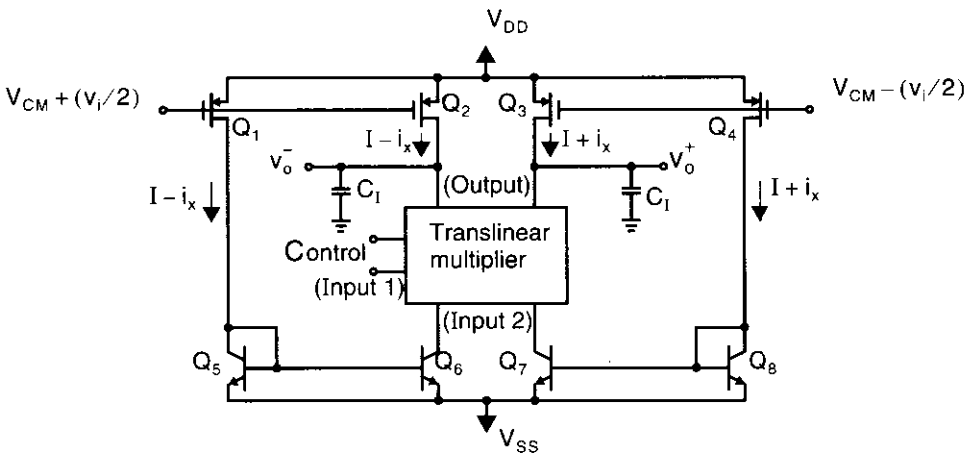


Fig. 15.40 A BiCMOS integrator using MOS transistors in the active region for linearization, and a translinear multiplier for tuning. The common-mode feedback circuit is not shown.

This BiCMOS integrator is used to realize a second-order pulse-shaping filter operating on 100-Mb/s data. Although the filter has a wide tuning range of approximately 10:1, it achieves only a moderate spurious-free dynamic range level of 35 dB.

15.6 MOSFET-C FILTERS

Although G_m-C filters are the most common type of continuous-time filters used in integrated circuit applications, another closely related technique is that of MOSFET-C filters. MOSFET-C filters are similar to fully differential active-RC filters, except resistors are replaced with equivalent MOS transistors in triode. Since active-RC and MOSFET-C filters are closely related, one benefit of MOSFET-C filters is that a designer can use the wealth of knowledge available for active-RC filters. However, MOSFET-C filters are generally slower than their G_m-C counterparts since they use Miller integration (i.e., the integrating capacitors are connected around a high-gain amplifier). Also, they are further reduced in speed in a CMOS technology because opamps capable of driving resistive loads are required as opposed to only capacitive G_m-C filters. However, they are competitive in BiCMOS technologies where high-transconductance opamps are available. Here, we discuss three variations of MOSFET-C filters—two-transistor integrators, four-transistor integrators, and R-MOSFET-C filters.

Two-Transistor Integrators

An example of a two-input fully differential active-RC integrator and its two-transistor MOSFET-C counterpart is shown in Fig. 15.41 [Banu, 1983]. Before we look at the linearization mechanism that occurrs in a MOSFET-C integrator, let us look at the equivalence of the two circuits in Fig. 15.41. In the active-RC filter, the two input

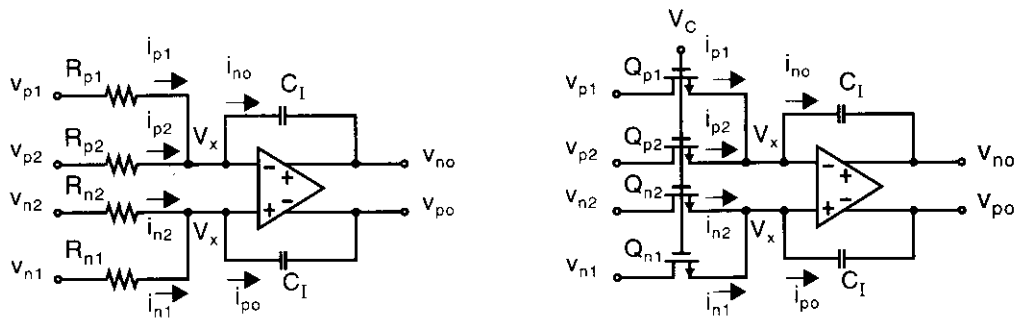


Fig. 15.41 (*a*) A two-input active-RC fully differential integrator. (*b*) A two-input two-transistor MOSFET-C integrator. The MOS transistors are in the triode region.

voltages of the opamp are equal (due to negative feedback) and, defining these two input voltages to be V_x, we can write

$$i_{no} = i_{p1} + i_{p2} = \frac{v_{p1} - V_x}{R_{p1}} + \frac{v_{p2} - V_x}{R_{p2}} \tag{15.149}$$

and

$$i_{po} = i_{n1} + i_{n2} = \frac{v_{n1} - V_x}{R_{n1}} + \frac{v_{n2} - V_x}{R_{n2}} \tag{15.150}$$

The output signals are given by

$$v_{po} = V_x - \frac{i_{po}}{sC_I} \tag{15.151}$$

and

$$v_{no} = V_x - \frac{i_{no}}{sC_I} \tag{15.152}$$

Thus, the differential output signal, v_{diff}, is

$$v_{diff} \equiv v_{po} - v_{no} = \frac{i_{no} - i_{po}}{sC_I} \tag{15.153}$$

Assuming the component values in the positive and negative half circuits are equal, or specifically, if

$$R_1 \equiv R_{p1} = R_{n1} \quad \text{and} \quad R_2 \equiv R_{p2} = R_{n2} \tag{15.154}$$

we have

$$v_{diff} = \frac{1}{sR_1C_I}(v_{p1} - v_{n1}) + \frac{1}{sR_2C_I}(v_{p2} - v_{n2}) \tag{15.155}$$

Thus, we see that the differential output signal, v_{diff}, equals positive integration of the two input differential signals. Negative integration is easily obtained by cross-coupling two input or output wires. Note that the common-mode signal, V_x, does not affect the final result.

Since the transistors in the MOSFET-C integrator, shown in Fig. 15.41(*b*), are assumed to be in the triode region, the small-signal analysis for the MOSFET-C integrator is quite similar to that for the active-RC circuit. Recall from (15.86) that the small-signal equivalent resistance of a transistor in triode is given by

$$r_{DS} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)\left(v_{GS} - V_{tn}\right)} \tag{15.156}$$

Thus, assuming the transistors are matched, the differential output of the MOSFET-C integrator is given by

$$v_{diff} = \frac{1}{sr_{DS1}C_I}(v_{p1} - v_{n1}) + \frac{1}{sr_{DS2}C_I}(v_{p2} - v_{n2}) \tag{15.157}$$

where

$$r_{DSi} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_i\left(V_C - V_x - V_{tn}\right)} \tag{15.158}$$

Here, note that V_x is important because it helps to determine the small-signal resistance of the transistors. Tuning can be accomplished by varying the control voltage, V_c.

So far, we have analyzed the small-signal operation of a MOSFET-C integrator. In this MOSFET-C case, the differential input signals, (v_{p1}, v_{n1}) and (v_{p2}, v_{n2}), are assumed to be balanced around a common-mode voltage, V_{CM}, set by the output common-mode feedback from the previous integrators. The common-mode feedback of the integrator causes the integrator's two outputs to be balanced also. As a result, it can be shown that V_x is related to the square of the input signal. This nonlinear relationship at V_x together with the nonlinear current through triode transistors results in quite linear single-ended signals at V_{no} and V_{po}. In addition, since the circuit is fully differential, even-order distortion products cancel, as depicted in Fig. 10.17. Thus, two-transistor MOSFET-C integrators can be used to realize filters with around a 50-dB linearity.

Based on the block diagram shown in Fig. 15.10, an example of a general second-order MOSFET-C filter is shown in Fig. 15.42(*a*). Here, the terms G_i represent the small-signal drain-source conductance of the transistors. The transfer function for this filter can be found by drawing its equivalent active-RC half circuit, as shown in Fig. 15.42(*b*). The output of the first integrator is given by

$$v_1(s) = -\frac{G_1}{sC_A}v_i(s) - \frac{G_4}{sC_A}v_o(s) \tag{15.159}$$

whereas the second integrator's output is given by

$$sC_B v_o(s) = G_3 v_1(s) - G_2 v_i(s) - sC_1 v_i(s) - G_5 v_o(s) \tag{15.160}$$

Combining the preceding two equations and rearranging, we have

$$\frac{v_o(s)}{v_i(s)} = -\frac{\left[\left(\frac{C_1}{C_B}\right)s^2 + \left(\frac{G_2}{C_B}\right)s + \left(\frac{G_1G_3}{C_AC_B}\right)\right]}{\left[s^2 + \left(\frac{G_5}{C_B}\right)s + \left(\frac{G_3G_4}{C_AC_B}\right)\right]} \tag{15.161}$$

Thus, we see that the transfer function is general, and that negative coefficients can be realized by cross-coupling appropriate signal wires.

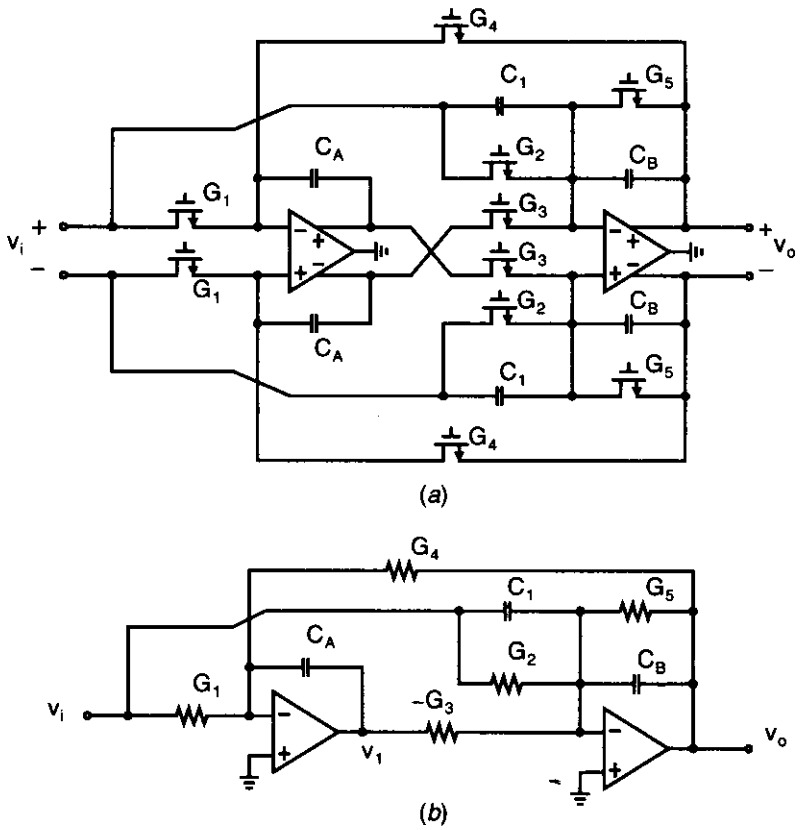


Fig. 15.42 (*a*) A general second-order MOSFET-C filter. (*b*) The equivalent active-RC half circuit.

Four-Transistor Integrators

One way to improve the linearity of a MOSFET-C filter is to use four-transistor MOSFET-C integrators, as shown in Fig. 15.43 [Czarnul, 1986]. The small-signal analysis of this four-transistor integrator can be found by treating this one-input integrator as effectively a two-input integrator in which the two input signals are $(v_{pi} - v_{ni})$ and the inverted signal is $(v_{ni} - v_{pi})$. With such an observation, and applying (15.157), the output signal is given by

$$v_{diff} = \frac{1}{sr_{DS1}C_I}(v_{pi} - v_{ni}) + \frac{1}{sr_{DS2}C_I}(v_{ni} - v_{pi}) \tag{15.162}$$

where

$$r_{DS1} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1\left(V_{C1} - V_x - V_t\right)} \tag{15.163}$$

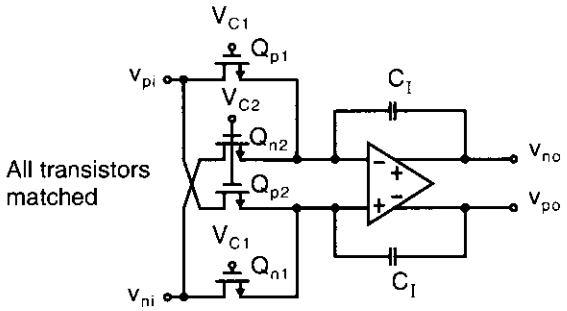


Fig. 15.43 A single-input four-transistor MOSFET-C integrator. It can cancel both even and odd distortion products if the nonlinear terms are not dependent on the control signals, V_{C1} and V_{C2}.

and

$$r_{DS2} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_2\left(V_{C2} - V_x - V_t\right)} \tag{15.164}$$

In the case where all four transistors are matched, we can combine the preceding equations to obtain

$$v_{diff} = v_{po} - v_{no} = \frac{1}{sr_{DS}C_I}(v_{pi} - v_{ni}) \tag{15.165}$$

where r_{DS} is given by

$$r_{DS} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{C1} - V_{C2}\right)} \tag{15.166}$$

Thus, we see that the effective resistance is determined by the difference in the control voltages.

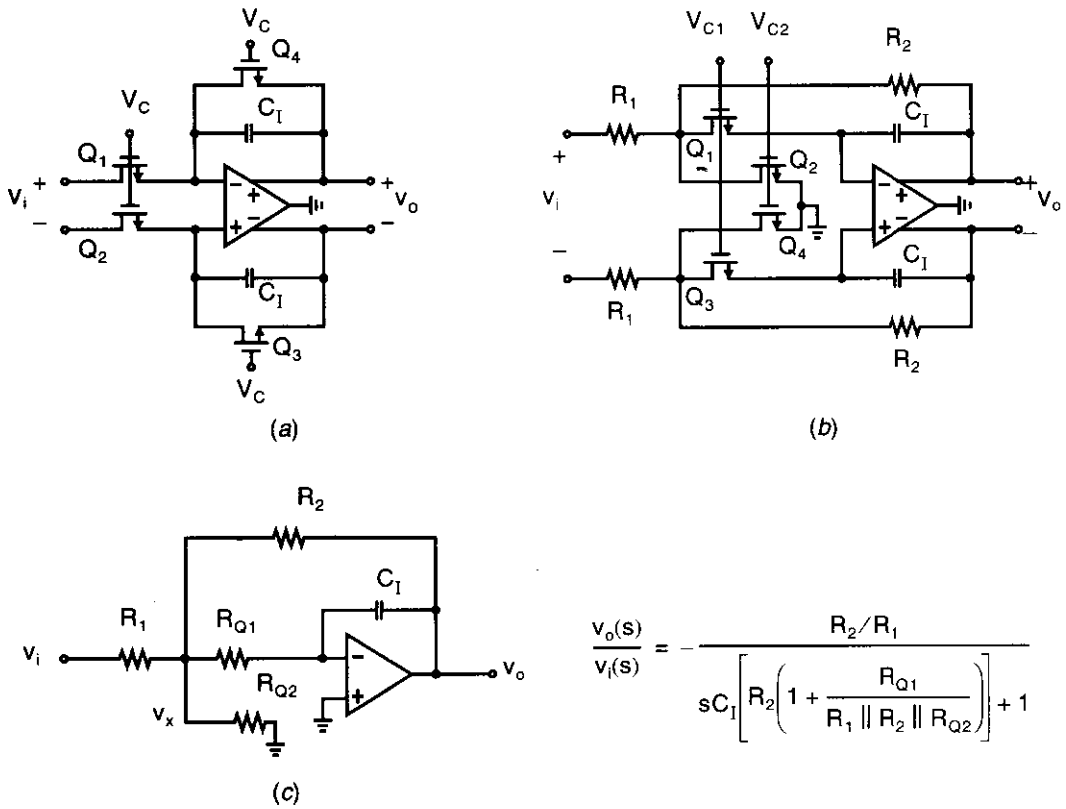
With regard to the distortion properties of this integrator, it has been shown for long channel-length transistors that the drain-source current in a triode transistor is reasonably well modelled by an equation in which the nonlinear distortion terms do not depend on the controlling gate voltage. In other words, although the linear term of each drain current is set by the controlling gate voltage, all distortion terms of the drain currents remain equal in the pair Q_{p1}, Q_{p2} as well as in the pair, Q_{n1}, Q_{n2} since, within each pair, the drain-source voltages are equal. As a result of the cross-coupling connection, *both the even and odd distortion terms cancel*. Unfortunately, this model does not hold as well for short-channel devices, and transistor mismatch also limits the achievable distortion performance. Hence, in practice, one might expect around a 10-dB linearity improvement using this technique over the two-transistor MOSFET-C integrator.

R-MOSFET-C Filters

Another technique intended to improve the linearity of MOSFET-C filters is the use of additional linear resistors [Moon, 1993]. An R-MOSFET-C first-order filter and its MOSFET-C counterpart are shown in Fig. 15.44. Using the equivalent active-RC half circuit, shown in Fig. 15.44(*c*), one finds the transfer function of this first-order R-MOSFET-C filter to be given by

$$\frac{v_o(s)}{v_i(s)} = -\frac{R_2/R_1}{sC_I\left[R_2\left(1+\dfrac{R_{Q1}}{R_1 \parallel R_2 \parallel R_{Q2}}\right)\right]+1} \tag{15.167}$$

where R_{Q1} and R_{Q2} represent the small-signal drain-source resistances of Q_1 and Q_2, respectively. Note that the dc gain of this first-order filter is not adjustable. However, it can be set precisely since it is determined by the ratio of two resistors. In addition, the time constant can vary from a minimum value of R_2C_I to an arbitrarily large value by changing the values of R_{Q1} and R_{Q2} via the control voltages, V_{C1} and V_{C2}. What this transfer function equation indicates is that at low-frequencies, the



$$\frac{v_o(s)}{v_i(s)} = -\frac{R_2/R_1}{sC_I\left[R_2\left(1+\dfrac{R_{Q1}}{R_1 \parallel R_2 \parallel R_{Q2}}\right)\right]+1}$$

Fig. 15.44 (*a*) A first-order MOSFET-C filter. (*b*) A first-order R-MOSFET-C filter. (*c*) Equivalent active-RC half-circuit for R-MOSFET-C filter.

feedback around R_2 forces node v_x to act as a virtual ground, and therefore excellent linearity is obtained since the circuit is essentially a resistor-only circuit. In [Moon, 1993], a linearity of approximately –90 dB is observed with input signals in the range of a few kilohertz. At higher frequencies, the linearity steadily decreases, and measured results of –70 dB are reported at the passband edge of a fifth-order Bessel filter (the passband is around 20 kHz). However, it should be noted that the measured values are total-harmonic-distortion values, and no intermodulation results are reported.

One other approach that has been used to realize high-linearity continuous-time filters is simply to realize differential active-RC filters, but to realize the capacitors using digitally programmable capacitor arrays. For example, [Durham, 1993] describes a filter intended for digital-audio interfaces that achieves distortion products at a –94-dB and a 95-dB signal-to-noise ratio.

15.7 TUNING CIRCUITRY

As mentioned at the beginning of this chapter, one disadvantage of continuous-time integrated filters is the requirement of additional tuning circuitry. This requirement is a result of large time-constant fluctuations due mainly to process variations. For example, integrated capacitors might have 10 percent variations, whereas resistors or transconductance values might have around 20 percent variations. Since these elements are constructed quite differently, the resulting RC or G_m/C time-constant products are accurate to only around 30 percent with these process variations. In addition, temperature variations further aggravate the situation because resistance and transconductance values change substantially over temperature. Thus, we need tuning circuitry to modify transconductance values such that the resulting overall time constants are set to known values. It should be noted, however, that although absolute component tolerances are high, relative accuracies can be quite good. Specifically, the ratio of two capacitors (or two resistors, or two transistors) can be matched to under 1 percent. This section discusses some techniques to realize tuning circuitry for integrated continuous-time filters. Note that, although the tuning approaches are discussed while we refer to G_m-C (transconductance-C) filters, the concepts are easily extended to other integrated continuous-time filters, such as MOSFET-C filters.

Tuning Overview

Consider once again the G_m-C continuous-time biquad filter shown in Fig. 15.11. Its transfer function, repeated here for convenience, is given by

$$H(s) = \frac{s^2\left[\frac{C_X}{C_X + C_B}\right] + s\left[\frac{G_{m5}}{C_X + C_B}\right] + \left(\frac{G_{m2}G_{m4}}{[C_A(C_X + C_B)]}\right)}{s^2 + s\left[\frac{G_{m3}}{C_X + C_B}\right] + \left(\frac{G_{m1}G_{m2}}{[C_A(C_X + C_B)]}\right)} \tag{15.168}$$

First, note that the numerator coefficient for s^2 is set by the capacitor ratio of $C_X/(C_X + C_B)$ and can therefore be quite accurate (i.e., the absolute values of the capacitors are unimportant—only their relative values matter). Second, although the transconductance values, G_{mi}, have large variations in their absolute values, relative transconductance values can also be set reasonably accurately. For example, if the transconductors are realized as bipolar differential pairs with an emitter degeneration resistor (as shown in Fig. 15.11), then the relative transconductance values of two transconductors is set by the ratio of their respective emitter degeneration resistor (assuming the gain-cell currents are equal in the two transconductors). Similarly, if other transconductors of the same type are used, their relative G_m values can be accurately set by choosing appropriate transistor sizes, bias currents, or resistor values (or some combination of the three). As a result, we can write all the transconductance values, G_{mi}, as an accurate constant multiplied by some basic transconductance value. Specifically, let us write all the transconductance values, G_{mi}, as a function of G_{m1}, resulting in

$$G_{mi} = k_{mi}G_{m1} \tag{15.169}$$

Here, the constants, k_{mi}, are set reasonably accurately by appropriate transistor, resistor, or bias-current scaling. Furthermore, let us also write

$$C_X + C_B = k_{XB}C_A \tag{15.170}$$

where k_{XB} is a constant that is accurately set as the ratio of capacitance values. With such an approach, (15.168) becomes

$$H(s) = \frac{s^2\left[\frac{C_X}{(C_X + C_B)}\right] + s\left(\frac{k_{m5}}{k_{XB}}\right)\left(\frac{G_{m1}}{C_A}\right) + \left(\frac{k_{m2}k_{m4}}{k_{XB}}\right)\left(\frac{G_{m1}}{C_A}\right)^2}{s^2 + s\left(\frac{k_{m3}}{k_{XB}}\right)\left(\frac{G_{m1}}{C_A}\right) + \left(\frac{k_{m1}k_{m2}}{k_{XB}}\right)\left(\frac{G_{m1}}{C_A}\right)^2} \tag{15.171}$$

We see from (15.17) that four of the coefficients for this second-order filter can be accurately set if only one ratio is tuned—that of G_{m1}/C_A. The other two coefficients (those corresponding to s^2) should not need adjustment since they do not rely on any RC-type time constant. Since it is difficult to tune C_A, the ratio G_{m1}/C_A is tuned by changing G_{m1}. Of course, as G_{m1} is varied, all the other transconductance values, G_{mi}, are also changed since their values track that of G_{m1} by their respective constants, k_{mi}. It should be mentioned here that this same single transconductance tuning is also valid for higher-order filter structures.

In summary, the most common way to tune a continuous-time integrated filter is to build an extra transconductor that is tuned (tuning details are discussed next) and to use the resulting tuning signal to control the filter transconductors, as shown in Fig. 15.45. Such an approach is commonly referred to as *indirect frequency tuning*. This tuning is indirect since one relies on matching between the filter transconductors (and parasitic capacitances) and the extra transconductor. In other words, the filter is not directly tuned by looking at its output signal. Frequency tuning refers to the fact that the ratio G_{m1}/C_A is equal to the unity-gain frequency of a G_m-C integrator

(G_{m1}/C_A is also proportional to the pole frequency, ω_o, in a first- or second-order filter).

Unfortunately, this frequency-tuning approach may not be sufficient in some applications due to nonideal integrators or mismatch effects. In these applications, some extra tuning circuitry known as Q-factor tuning (discussed later in this section) can be used. It is also possible to implement *direct tuning* where the filter is tuned by directly looking at the filter's output. Two such direct approaches are also discussed in this section.

Constant Transconductance

As just discussed, if no tuning is performed, one might expect around a 30-percent tolerance on the absolute value for the G_m/C ratio. However, integrated capacitance tolerance typically accounts for only a 10-percent variation in the overall 30-percent tolerance. Thus, in applications where a 10-percent variation can be permitted (such as an anti-aliasing filter with a sample rate moderately higher than the Nyquist rate), it is sufficient to set only the G_m value with the use of a fixed external resistor. As we will see below, such tuning of a G_m value is not difficult and does not require any clock signals.

In the case where 10-percent accuracy is not enough, clearly one must also account for capacitor tolerance. One way to do so (while still not needing a clock signal) is to have a variety of external resistors available and choose the most appropriate one to also account for capacitor tolerance. With such an approach, one might expect that the overall G_m/C ratio would be accurate to under 1 percent. Although a variety of methods exist for choosing this external resistance, one way is to use a known value of external resistance and measure the step response of the filter during system production. This step-response result can then be used to determine the C value, and hence the proper resistance value can be calculated. Finally, since integrated capacitors typically have small temperature coefficients, overall temperature effects are small if the external resistor is also chosen to have a low temperature coefficient.

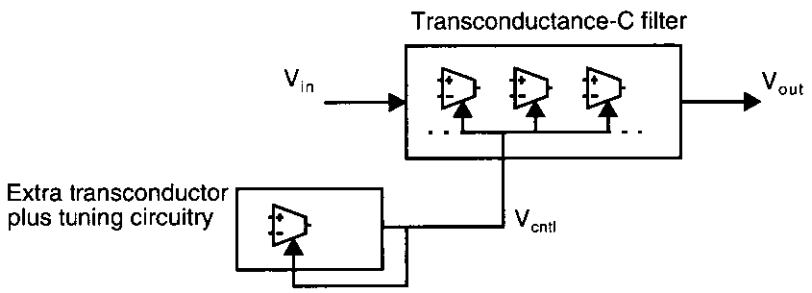


Fig. 15.45 Indirect frequency tuning. Note that, although the tuning signal is shown here as a voltage signal, it may also be realized using a set of current controlling signals.

To set a transconductance value equal to the inverse of an external resistance, (i.e., $G_m = 1/R_{ext}$), a variety of feedback circuits can be used. Two example circuits are shown in Fig. 15.46, where it should be noted that, in both cases, it is assumed the transconductor's transconductance increases as the level of the control signal is increased. In Fig. 15.46(*a*), if G_m is too small, the current through R_{ext} is larger than the current supplied by the transconductor, and the difference between these two currents is integrated with the opamp and capacitor. As a result, the control voltage, V_{cntl}, is increased until these two currents are equal (but opposite in direction) and, therefore, $G_m = 1/R_{ext}$. The circuit in Fig. 15.46(*b*) shows two voltage-to-current converters—one is the transconductor being tuned, and the other is a fixed voltage-to-current converter that simply needs a large transconductance and is not necessarily linear. (It might be implemented as a simple differential pair.) This circuit operates as follows: If G_m is too small, then the voltage at the top of R_{ext} will be less than V_B and the fixed V/I converter will increase I_{cntl}. At steady state, the differential voltage into the fixed V/I converter will be zero, resulting in $G_m = 1/R_{ext}$.

Frequency Tuning

A precise tuning of a G_m/C_A ratio can be achieved if an accurate time period is available. For example, assuming one has available an accurate clock frequency, say, f_{clk}, then one method of frequency tuning is by using a switch-capacitor circuit as shown in Fig. 15.47 [Viswanathan, 1982]. Here, the tuning circuit is quite similar to the constant-transconductance approaches of Fig. 15.46, except that the external resistance is replaced with a switched-capacitor equivalent resistance. From Chapter 10, the equivalence resistance of the switched-capacitor circuit is given by $R_{eq} = 1/(f_{clk}C_m)$, and therefore the transconductance value, G_m, is set to $f_{clk}C_m$. In this way, the G_m/C_A ratio is accurately set to $(f_{clk}C_m)/C_A$, and hence precise frequency tuning can be

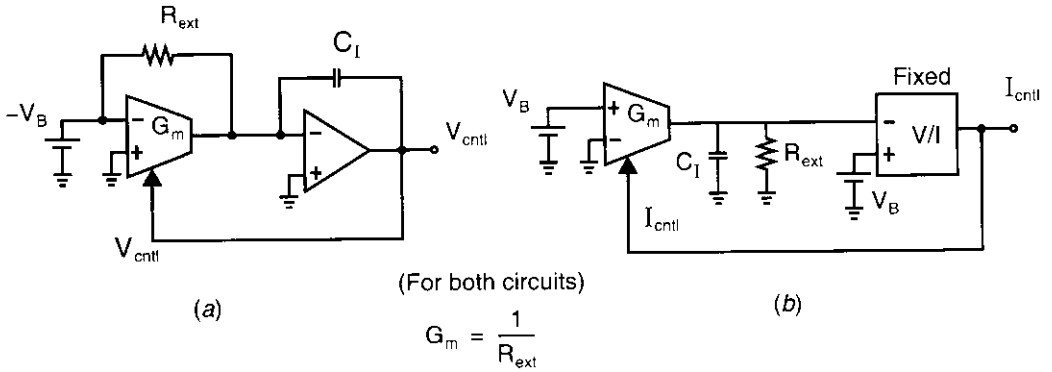


Fig. 15.46 Constant transconductance tuning. Possible tuning circuits if the transconductors are (*a*) voltage controlled or (*b*) current controlled. In both circuits, it is assumed the transconductor's transconductance increases as the level of the control signal increases. V_B is an arbitrary voltage level, whereas C_I is an integrating capacitor used to maintain loop stability.

achieved without any external components. Note that an additional low-pass filter, R_1C_1, has been added here to remove the high-frequency ripple voltage due to using a switched-capacitor circuit. It should also be noted that, since this method requires a clock signal, there is a strong possibility that some of the clock signal will leak into the continuous-time filter, either mainly through the transconductor controlling signal or through the IC substrate.

One difficulty with this switched-capacitor tuning approach is that it requires large transconductance ratios (and hence poorer matching) if high-frequency filters are desired. For example, consider the case of a 100-MHz filter, where the G_m/C_A ratio should be set to around $2\pi \times 100$ MHz. If a capacitance value, C_A, is assumed to be 1 pF, then $G_m = 2\pi \times 10^{-4}$ V/A. Thus, in the tuning circuit of Fig. 15.47, assuming that $C_m = 1$ pF, we would require the switched-capacitor circuit to be clocked at the impractical frequency of

$$f_{clk} = \frac{G_m}{C_m} = \frac{2\pi \times 10^{-4}}{1 \times 10^{-12}} = 628 \text{ MHz} \tag{15.172}$$

At first glance, one might consider reducing this clock frequency by increasing the value of C_m, but, although f_{clk} is reduced, settling-time requirements remain difficult since the capacitance, C_m, is larger. Another way to reduce f_{clk} is to let the tuning circuit set a smaller transconductance value, say, $0.1G_m$. In this way, f_{clk} is reduced by ten but the filter's transconductors must be 10 times greater than the tuning circuitry's transconductor. Thus, poorer matching occurs between the filter and the tuning circuitry, resulting in a less accurate frequency setting for the filter.

Another approach to lower the clock frequency of this switched-capacitor tuning circuitry is by using two scaled current sources, as shown in Fig. 15.48 [Silva-Martinez, 1992]. Using an equivalent resistance of $-1/f_{clk}C_m$ for the switched-capacitance circuit, and noting that the diode-connected transconductor is equivalent to a resistor of value $1/G_m$, one can show that when the average current into the integrator is zero, the transconductance value is given by

$$G_m = Nf_{clk}C_m \tag{15.173}$$

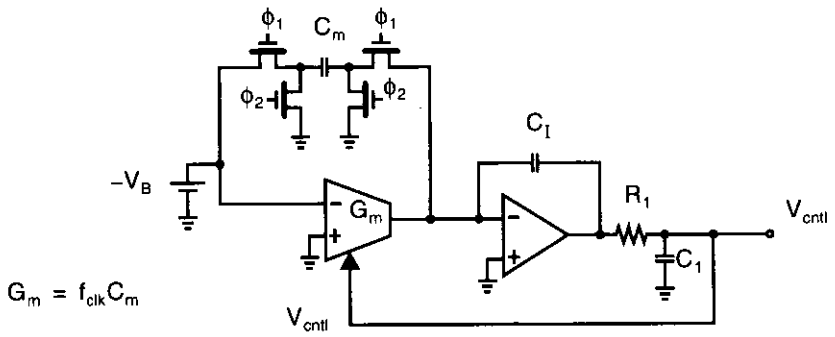


Fig. 15.47 A frequency-tuning circuit where G_m is set by a switched-capacitor circuit. The switched-capacitor branch has a clock frequency of f_{clk}. The low-pass filter, R_1C_1, is set to a frequency low enough to reduce the high-frequency ripple voltage.

Thus, the clock frequency of this circuit is N times lower than that for the circuit shown in 15.47. This circuit was used to tune a 10.7-MHz bandpass filter, where a value of N = 148 was used, resulting in a clock frequency of only 450 kHz. The low-pass filter was also realized by using a switched-capacitor circuit and an off-chip capacitor.

Another approach to achieving frequency tuning is to use a phase-locked loop (PLL) (described in Chapter 16) as shown in Fig. 15.49 [Tan, 1978]. Here, two continuous-time integrators are placed in a loop to realize a voltage-controlled oscillator that is placed into a phase-locked loop. After the circuit is powered up, the negative-feedback of the PLL causes the VCO frequency and phase to lock to the external reference clock. Once the VCO output is locked to an external reference signal, the G_m/C ratio of the VCO is set to a desired value, and the control voltage, V_{cntl}, can be used to tune the integrated filter. It should be noted that choosing the external reference clock is a trade-off because it affects both the tuning accuracy as well as the tuning signal leak into the main filter. Specifically, for best matching between the tuning circuitry and the main filter, it is best to choose the reference frequency that is equal to the filter's upper passband edge. However, noise gains for the main filter are typically the largest at the filter's upper passband edge, and therefore the reference-signal leak into the main filter's output might be too severe. As one moves away from the upper passband edge, the matching will be poorer, but an improved immunity to the reference signal results. Another problem with this approach is that, unless some kind of

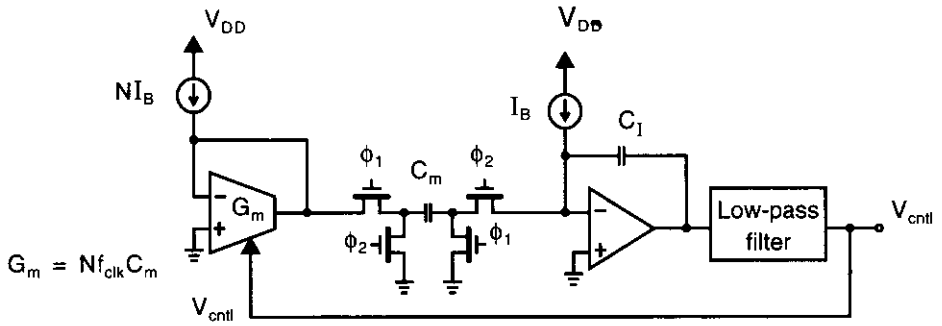


Fig. 15.48 A switched-capacitor frequency-tuning circuit that operates at a lower clock frequency.

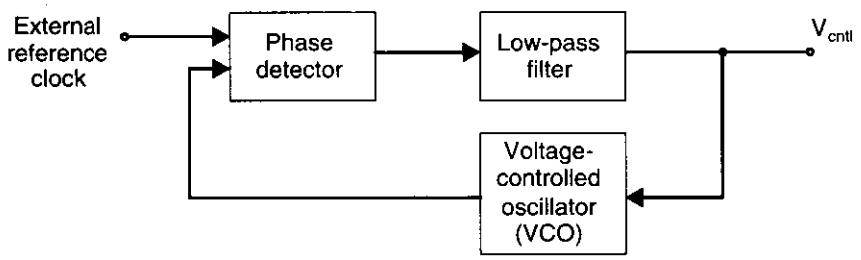


Fig. 15.49 Frequency tuning using a phase-locked loop. The VCO is realized by using transconductor-based integrators that are tuned to adjust the VCO's frequency.

power-supply-insensitive voltage control is added to the VCO, any power-supply noise will inject jitter into the control signal, V_{cntl}. The addition of amplitude control is quite complicated. For a good discussion of this phase-locked-loop approach, see [Krummenacher, 1988; Khoury, 1991]. For a better understanding of the operation of a phase-locked loop, see Chapter 16.

Another, somewhat similar, approach that has been used is based on having a tracking filter that locks onto a fixed-frequency input [Khorramabadi, 1984]. This approach is reported to be less sensitive to power-supply noise. The control voltage for the tracking filter is used to adjust the transconductors that are used in the actual system, assuming the transconductors in the tracking filter match the transconductors in the actual system. An example calibration system is shown in Fig. 15.50. When the low-pass filter has the same resonant frequency as the external reference clock, it has exactly a 90-degree phase shift. Therefore, the correlation between its input and output is zero. If the frequencies are not the same, then the correlation, as obtained by the multiplier and integrator, is nonzero. The negative feedback from the output of the integrator to the frequency-control voltage of the filter drives the resonant frequency in the proper direction to equalize the two frequencies. After lock is obtained, the same control voltage can be used for other filters. The other filters will be tuned to known time constants, assuming they match the filter in the control loop.

It is important that the integrator in the loop have a very low-frequency time constant in order to filter out the component at twice the external reference frequency that is present at the output of the multiplier. Otherwise, this component can cause clock leakage into the other filters being tuned. A variant on this scheme drives the correlation between a notch output and a low-pass filter output (obtained from the same biquad) to zero when one is obtaining the control voltage [Kwan, 1991]. This latter method has much fewer signal components at twice the frequency of the external reference clock and does not require as large a time constant for the integrator in the loop. This makes the latter method more readily integrable without external components. Also, the loop is less sensitive to phase errors; it will always converge to the notch frequency, even when the difference in phase between the low-pass and notch outputs is not exactly 90°.

Q-Factor Tuning

In some applications, such as high-speed or highly-selective filtering, nonideal integrator effects and parasitic components force the need to also tune the Q factors of the

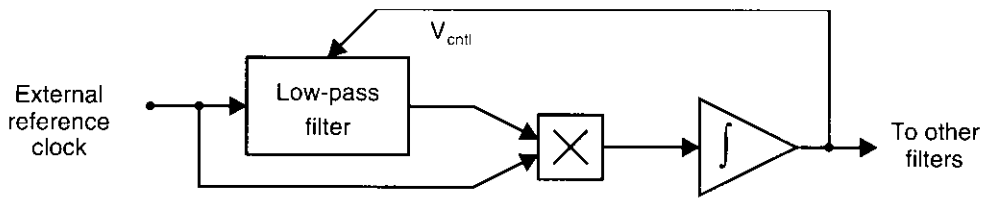


Fig. 15.50 Using a tracking filter to derive a control signal for tuning continuous-time filters.

poles of the integrated filter. However, it should be noted that most commercial integrated filters do not presently have Q-factor tuning due to increased circuit complexity and design difficulty. Also, the addition of a Q-factor tuning circuit increases the possibility that some of the reference tuning signal leaks into the main filter. However, it is likely that more applications in the near future will require Q-factor tuning, and thus we present a brief discussion of it here.

One way to perform Q-factor tuning is to tune the phase of the filter's integrators to ensure that they all have a 90-degree phase lag near the filter's passband edge. An integrator's phase response can be adjusted by introducing a tunable resistance (say, realized as a transistor in triode) in series with the integrating capacitor. The control voltage for this tunable resistance, V_Q, is generated by a Q-factor tuning circuit, shown in Fig. 15.51, and passed to all the filter integrators.

Alternatively, in the case where the integrated filter is second order, the pole Q can be adjusted by changing the transconductance of the damping transconductor in the filter. Specifically, referring back to (15.171) and equating the denominator to a second-order denominator written in the form of ω_o and Q, we have,

$$s^2 + s\left(\frac{k_{m3}}{k_{XB}}\right)\left(\frac{G_{m1}}{C_A}\right) + \left(\frac{k_{m1}k_{m2}}{k_{XB}}\right)\left(\frac{G_{m1}}{C_A}\right)^2 = s^2 + s\left(\frac{\omega_o}{Q}\right) + \omega_o^2 \qquad (15.174)$$

Equating the two sides of (15.174), we find the following relationships:

$$\omega_o = \left(\frac{G_{m1}}{C_A}\right)\sqrt{\frac{k_{m1}k_{m2}}{k_{XB}}} \qquad (15.175)$$

$$Q = \left(\frac{k_{XB}}{k_{m3}}\right)\sqrt{\frac{k_{m1}k_{m2}}{k_{XB}}} \qquad (15.176)$$

From this Q relationship, we see that the Q factor of the filter's poles is inversely proportional to k_{m3}, and hence one need only tune G_{m3} to adjust the Q factor of this second-order filter.

The control signal, V_Q, for either of the preceding Q-factor tuning approaches can be realized using the magnitude-locked loop system shown in Fig. 15.51 [Schaumann, 1990]. The circuit's operation is based on the knowledge that a Q-factor error results in a magnitude error in a filter's frequency response. To measure the magnitude error, a sinusoidal signal of an appropriate reference frequency is applied to a Q-reference circuit, and the magnitude of its output is compared to a scaled version of the input signal's magnitude. This sinusoidal frequency might be obtained as the output of the VCO in the frequency-tuning circuitry.

Tuning Methods Based on Adaptive Filtering

Adaptive filters are commonly used in digital-signal-processing applications such as model matching, channel equalization, and noise (or echo) cancellation. It is also

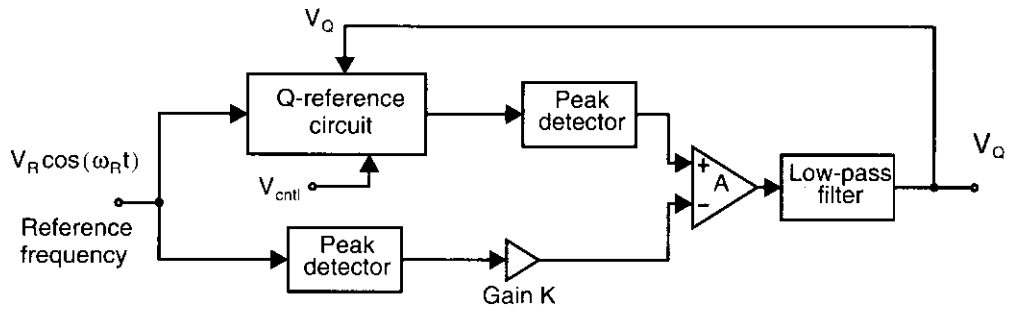


Fig. 15.51 A magnitude-locked loop for Q-factor tuning. The Q-reference circuit is typically a second-order filter that is frequency tuned through the use of V_{cntl}.

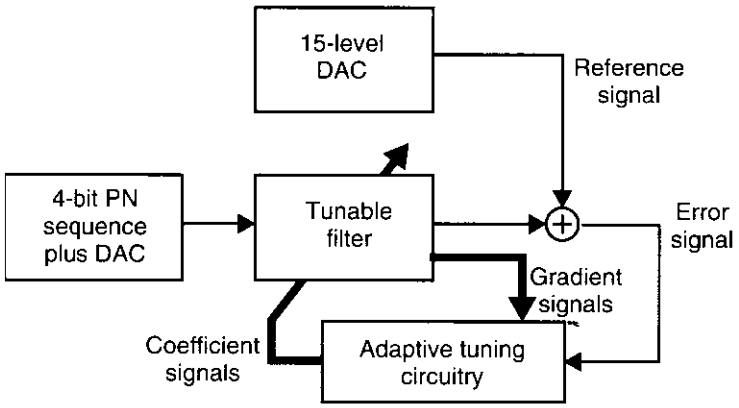


Fig. 15.52 A tuning approach in which all the poles and zeros of the tunable filter can be adjusted. The 15-level DAC outputs are determined by what the ideal filter response would generate, while the adaptive tuning circuitry minimizes the error signal.

possible to use adaptive filter techniques to tune a continuous-time integrated filter to a given specification. One example of such an approach is shown in Fig. 15.52 [Kozma, 1991], where the adaptive tuning circuitry is used to minimize the error signal. During tuning, the input to the tunable filter is a predetermined output from a pseudorandom (PN) 4-bit sequence and a D/A converter. Since the input is known and repetitive, the ideal output from a desired transfer-function can be precalculated (or simulated) and used as a reference signal for the adaptive system. After adaptation, the transfer function of the tunable filter should match that of the desired filter, and, by freezing the coefficients (assuming they are digitally controlled), the tunable filter can be disconnected from the tuning circuit and used in the desired operation. With this approach, it is possible to tune all the poles and zeros of the tunable filter to better match the desired transfer function. Although the adaptive tuning circuitry simply consists of comparators, analog multiplexors, and integrators, note that this adaptive tuning scheme has not yet been fully integrated or experimentally verified in a high-frequency application.

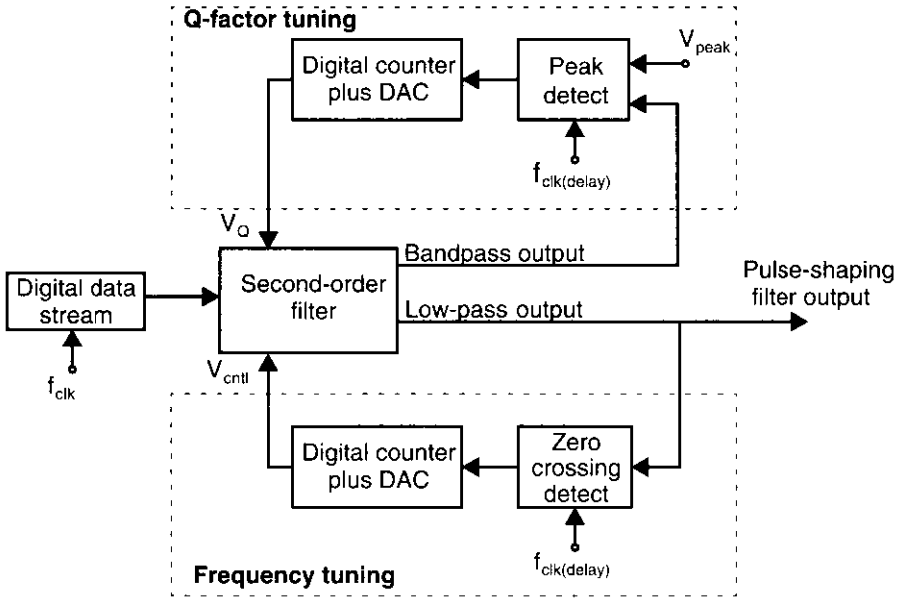


Fig. 15.53 A tuning method to implement a pulse-shaping filter needed for data communication systems.

Another adaptive-filter tuning method intended for high-speed data transmission over a twisted-wire pair is shown in Fig. 15.53 [Shoval, 1995]. In this application, the filter input is a data stream of ones and zeros that are represented by the input signal being either high or low. Before transmission, a pulse-shaping filter is required to ensure that not too much high-frequency power is radiated from the twisted-wire channel. The two tuning loops (frequency and Q-factor loops) rely on the fact that the input to the filter is a series of steps (say, ±1 V), and thus, in fact, tune the step response of the filter. Specifically, frequency tuning is accomplished by ensuring that the zero crossing of the filter's low-pass output occurs at the correct time period after a data transition. Also, Q-factor tuning is performed by comparing the peak in the filter's bandpass output with a known voltage. Fortunately, the peak in the bandpass output occurs at approximately the same time as the zero crossing, so both detectors can be realized through the use of two clocked comparators, which are triggered at a set time after a data transition. This approach was used to tune a second-order filter intended as a pulse-shaping filter for a 100-Mb/s data transmission. In summary, clever tuning techniques can be implemented when a restricted set of input signals are applied to a tunable filter such as in data communication circuits.

15.8 DYNAMIC RANGE PERFORMANCE

Analog circuits generally have many different performance criteria that must be met so that overall system performance meets specifications. Some typical analog filter

performance criteria are transfer-function accuracy, power consumption, linearity, and noise performance. In this section, we discuss the last two items—linearity and noise performance. Linearity limits the value of the largest useful signals that can occur in the filter, whereas noise limits the value of the smallest useful signals. Thus, we find that linearity and noise together determine the useful dynamic range of a filter. It should be noted here that the dynamic range of integrated continuous-time filters is often a crucial measure since its value is often low and can seriously impair system performance.

Total Harmonic Distortion (THD)

If a sinusoidal waveform is applied to a linear time-invariant system, it is well known that the output will also be a sinusoidal waveform at the same frequency, but possibly with different magnitude and phase values. However, if the same input is applied to a nonlinear system, the output signal will have frequency components at harmonics of the input waveform, including the fundamental (or first) harmonic. For example, if a 1-MHz sinusoidal input signal is used, the output signal will have power at the fundamental, 1 MHz, as well as at the harmonic frequencies, 2 MHz, 3 MHz, 4 MHz, and so on. The *total harmonic distortion* (THD) of a signal is defined to be the ratio of the total power of the second and higher harmonic components to the power of the fundamental for that signal. In units of dB, THD is found using the following relation:

$$\text{THD} = 10 \log \left(\frac{V_{h2}^2 + V_{h3}^2 + V_{h4}^2 + \cdots}{V_f^2} \right) \tag{15.177}$$

where V_f is the amplitude of the fundamental and V_{hi} is the amplitude of the ith harmonic component. Sometimes THD is presented as a percentage value. In this case,

$$\text{THD} = \frac{\sqrt{V_{h2}^2 + V_{h3}^2 + V_{h4}^2 + \cdots}}{V_f} \times 100 \tag{15.178}$$

For example, a 0.1-percent THD value implies that the amplitude of the fundamental is 1,000 times larger than the amplitude of the harmonic components. This 0.1-percent THD value is equivalent to a value of –60 dB THD. It should also be noted that the THD value is almost always a function of the amplitude of the input (or output) signal level, and thus the corresponding signal amplitude must also be reported. Also, for practical reasons, typically the power of only the first few harmonics (say, the first 5) are included since the distortion components usually fall off quickly for higher harmonics.

One difficulty with the use of THD in reporting filter performance is that often the harmonic components fall in the stopband of the filter, and thus the THD value is falsely improved. For example, if a 21-MHz low-pass filter is being tested, then a 5-MHz input signal results in the 10-MHz, 15-MHz, and 20-MHz components falling within the passband, whereas higher distortion components will be attenuated by the filter. However, filter linearity is often worse when higher input signal frequencies are

applied due to nonlinear capacitances or, worse, nonlinear signal cancellation. Thus, it is useful to measure filter linearity with input signals near the upper edge of the passband. Unfortunately, if a 20-MHz input signal is applied to the example low-pass filter, the second and higher harmonic components lie in the stopband and the THD value will indicate much better linearity than would occur for a practical application. Moreover, the testing of a narrowband filter always has this THD measurement difficulty since the use of an input frequency in the passband will be attenuated by the filter's stopband. In summary, a THD measurement is straightforward to perform but does not work well in the important test of high-frequency signals near the upper passband of the filter. Fortunately, as we will see next, one can use intermodulation tests to measure filter linearity near the upper passband edge.

EXAMPLE 15.9

Calculate the THD value of a signal in which the fundamental component is at 1 MHz and has a power level of –10 dBm, and the only significant harmonics are the first three above the fundamental. These harmonics, at 2 MHz, 3 MHz, and 4 MHz, are measured to have power levels of –53 dBm, –50 dBm, and –56 dBm, respectively.

Solution

Recalling that 0 dBm refers to a 1-mW signal, then the power of the fundamental component is 100 μW, whereas the power of the first three harmonics are 5 nW, 10 nW, and 2.5 nW, respectively. Thus, the total power of the harmonics is equal to

$$P_{harm} = (5^2 + 10^2 + 2.5^2)^{1/2} = 11.5 \text{ nW} \tag{15.179}$$

As a result, the THD is calculated to be

$$\text{THD} = 10\log\left(\frac{100\ \mu\text{W}}{11.5\ \text{nW}}\right) = 39.4 \text{ dB} \tag{15.180}$$

Note here that the third harmonic (i.e., 30 MHz) essentially dominates the THD measurement.

Third-Order Intercept Point (IP3)

Here, we introduce the concept of the *third-order intercept point* (IP3) as a measure for the third-order distortion component [Carson, 1990]. We focus here on third-order distortion since, for fully differential circuits, the even-order distortion components are ideally zero and, thus, third-order distortion typically dominates. However, in cases where second-order distortion dominates, a similar concept is also possible and is referred to as the *second-order intercept point* (IP2).

Consider a nonlinear system[3] with an input signal, $v_{in}(t)$, and an output signal, $v_o(t)$. The output signal can be written as a Taylor series expansion of the input signal:

$$v_o(t) = a_1 v_{in}(t) + a_2 v_{in}^2(t) + a_3 v_{in}^3(t) + a_4 v_{in}^4(t) + \cdots \tag{15.181}$$

Here, the linear term is a_1, whereas a_2, a_3, and a_4 characterize the second-, third-, and fourth-order distortion terms, respectively. As mentioned previously, in fully differential circuits, all even terms (i.e., a_2 and a_4) are small, so typically a_3 dominates and we approximate $v_o(t)$ as

$$v_o(t) \cong a_1 v_{in}(t) + a_3 v_{in}^3(t) \tag{15.182}$$

If $v_{in}(t)$ is a sinusoidal signal given by

$$v_{in}(t) = A\cos(\omega t) \tag{15.183}$$

the output signal can be shown to be approximated by

$$v_o(t) \cong a_1 A\cos(\omega t) + \frac{a_3}{4}A^3[3\cos(\omega t) + \cos(3\omega t)] \tag{15.184}$$

where we see a fundamental term and a third-harmonic term. Defining H_{D1} and H_{D3} to be the amplitudes of the fundamental and third-harmonic terms, respectively, we can write

$$v_o(t) \equiv H_{D1}\cos(\omega t) + H_{D3}\cos(3\omega t) \tag{15.185}$$

Since, typically, $(3/4)a_3A^3 << a_1A$, one usually approximates the linear component of the output signal as

$$H_{D1} = a_1 A \tag{15.186}$$

and the third-harmonic term as

$$H_{D3} = \frac{a_3}{4}A^3 \tag{15.187}$$

Finally, we see that the third-order distortion term results in power at the third harmonic frequency and the ratio of H_{D3}/H_{D1} is defined as the third-order harmonic distortion ratio, given by

$$HD_3 \equiv \frac{H_{D3}}{H_{D1}} = \left(\frac{a_3}{a_1}\right)\left(\frac{A^2}{4}\right) \tag{15.188}$$

Unfortunately, as just noted, this distortion term lies at $3\omega t$ for a single sinusoidal input, and thus we resort to an intermodulation test to move the distortion term back near the frequency of the input signals.

Consider now the case of an intermodulation test, where the input signal consists of two equally sized sinusoidal signals and is written as

$$v_{in}(t) = A\cos(\omega_1 t) + A\cos(\omega_2 t) \tag{15.189}$$

3. We assume here that the nonlinear system is memoryless and time invariant. Unfortunately, filters are not memoryless, and a Volterra series should be used; however, this assumption simplifies the analysis and usually results in good approximations for distortion figures.

In this case, the output signal can be shown to be approximated by

$$\begin{aligned} v_o(t) \equiv & \left(a_1 A + \frac{9a_3}{4}A^3\right)[\cos(\omega_1 t) + \cos(\omega_2 t)] \\ & + \frac{a_3}{4}A^3[\cos(3\omega_1 t) + \cos(3\omega_2 t)] \\ & + \frac{3a_3}{4}A^3[\cos(2\omega_1 t + \omega_2 t) + \cos(2\omega_2 t + \omega_1 t)] \\ & + \frac{3a_3}{4}A^3[\cos(\omega_1 t - \Delta\omega t) + \cos(\omega_2 t + \Delta\omega t)] \end{aligned} \tag{15.190}$$

where $\Delta\omega$ is defined to be the difference between the input frequencies (i.e., $\Delta\omega \equiv \omega_2 - \omega$) which we assume to be small. Here, we see that the first line of (15.90) is the fundamental components, the second line shows the levels at three times the fundamentals, the third line also describes distortion at nearly three times the fundamentals, and the fourth line describes the distortion levels at two new frequencies that are close to the input frequencies (slightly below ω_1 and slightly above ω_2). As a result, for a narrowband or low-pass filter, these two new distortion components (due to third-order distortion) fall in the passband and can be used to predict the third-order distortion term.

Using the same notation as in the harmonic distortion case, we have the intermodulation distortion levels given by

$$I_{D1} = a_1 A \tag{15.191}$$

and

$$I_{D3} = \frac{3a_3}{4}A^3 \tag{15.192}$$

The ratio of these two is the third-order intermodulation value, given by

$$ID_3 = \frac{I_{D3}}{I_{D1}} = \left(\frac{a_3}{a_1}\right)\left(\frac{3A^2}{4}\right) \tag{15.193}$$

From (15.191) and (15.192), note that, as the amplitude of the input signal, A, is increased, the level of the fundamental rises linearly, whereas the I_{D3} rises in a cubic fashion. For example, if A is increased by 1 dB, then I_{D1} also increases by 1 dB while I_{D3} increases by 3 dB. Thus, when the fundamental and intermodulation levels are plotted in a dB scale against the signal amplitude, A, the two curves are linear, but with different slopes, as shown in Fig. 15.54. The third-order intercept point is defined to be the intersection of these two lines. Note, however, that as the signal amplitude rises, the linear relationships of I_{D1} and I_{D3} are no longer obeyed due to the large amount of nonlinearities violating some of our original assumptions. For example, in (15.190), we ignored the cubic A term in estimating the fundamental level, I_{D1}. Also, other distortion terms that were ignored now become important. As a result, it is impossible to directly measure the third-order intercept point, and thus it must be extrapolated from the measured data. The third-order intercept point results in two

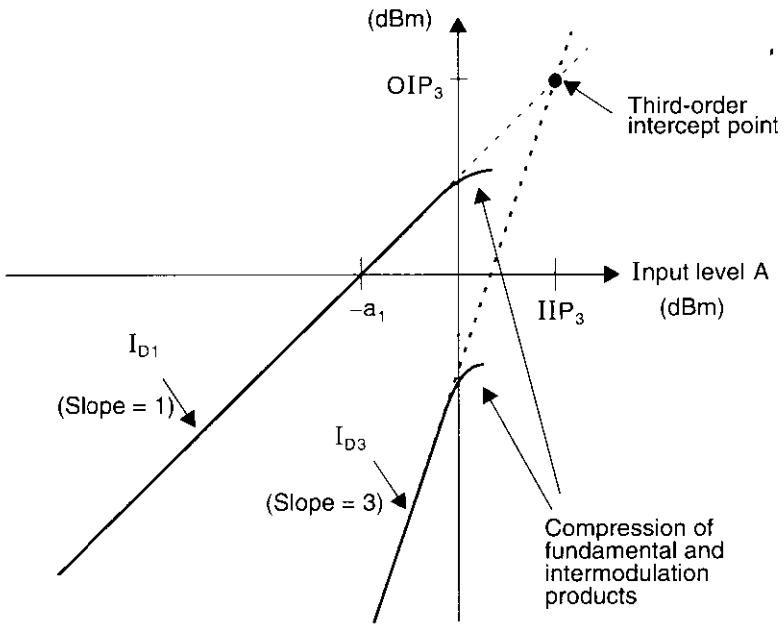


Fig. 15.54 Graphical illustration of the third-order intercept-point. IIP_3 and OIP_3 are the input and output third-order intercept points, respectively. They cannot be measured directly due to compression of the fundamental and intermodulation products at high-power levels.

values—IIP_3 and OIP_3, which are related to the input and output levels, respectively. If the linear gain term, a_1, is unity (or, equivalently, 0 dB), then $IIP_3 = OIP_3$. However, if a_1 is not unity, one must be careful to state which of the two intercept points is being reported.

Knowledge of the third-order intercept point is quite useful in determining what signal level should be chosen to achieve a desired intermodulation ratio, ID_3. Specifically, we see from (15.193) that ID_3 improves by 2 dB for every 1 dB of signal level decrease (since it is related to A^2) and that OIP_3 is defined to be the I_{D1} point where $ID_3 = 0$ dB. Thus, we have the simple relationship (all in decibels)

$$OIP_3 = I_{D1} - \frac{ID_3}{2} \tag{15.194}$$

EXAMPLE 15.10

If $OIP_3 = 20$ dBm, what output-signal level should be used such that the third-order intermodulation products are 60 dB below the fundamental?

Solution

Using (15.194) with $ID_3 = -60$ dB, we have

$$I_{D1} = OIP_3 + \frac{ID_3}{2} = -10 \text{ dBm} \tag{15.195}$$

Thus, an output level of −10 dBm should be used.

Spurious-Free Dynamic Range (SFDR)

Spurious-free dynamic range (SFDR) is defined to be the signal-to-noise ratio when the power of the third-order intermodulation products equals the noise power. In Fig. 15.55, the filter's output noise power is shown along the vertical axis as N_o. If a low enough signal level is used, I_{D3} will be well below the noise floor. However, since I_{D3} rises 3 dB for every 1 dB of signal-level increase, there will soon be a point where I_{D3} is equal to the noise power. As the figure shows, SFDR is defined to be the output SNR ratio when I_{D3} is equal to N_o. Alternatively, one can measure SFDR using the input-signal levels as the difference between the level that results in $I_{D3} = N_o$ and the level A_{No} that results in a fundamental output level equal to N_o.

To find a formula relating SFDR, OIP_3, and N_o (all in dB units), we first note that

$$SFDR = I_{D1}^* - N_o = I_{D1}^* - I_{D3}^* \tag{15.196}$$

where I_{D1}^* and I_{D3}^* refer to the output and distortion levels when $I_{D3} = N_o$, as shown in Fig. 15.55. Since the units are assumed to be in dB, we also have, from (15.193),

$$ID_3 = I_{D3} - I_{D1} \tag{15.197}$$

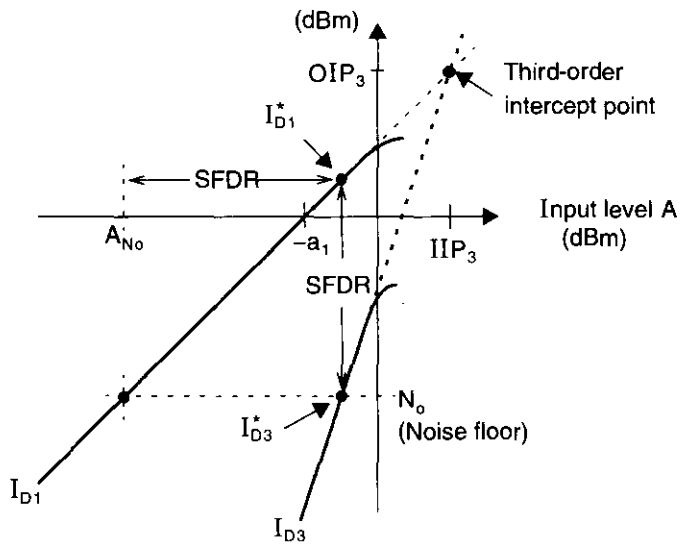


Fig. 15.55 Graphical illustration of spurious-free dynamic range (SFDR).

Using (15.194), we have

$$\mathrm{OIP}_3 = I_{D1}^* - \frac{(N_o - I_{D1}^*)}{2} \tag{15.198}$$

and substituting in $I_{D1}^* = \mathrm{SFDR} + N_o$ from (15.196) and rearranging, we have

$$\mathrm{SFDR} = \frac{2}{3}(\mathrm{OIP}_3 - N_o) \tag{15.199}$$

EXAMPLE 15.11

At an input-signal level of 0 dBm, an intermodulation ratio of −40 dB was measured in an filter with a gain of 2 dB. Calculate the value of the input and output third-order intercept points. What input-signal level should be applied if one wants an intermodulation ratio of −45 dB? If the noise power at the output is measured to be −50 dBm, what is the expected SFDR, and what output-signal level does it correspond to?

Solution

With an input level of 0 dBm and a gain of 2 dB, the output level is $I_{D1} = 2$ dBm with a measured value of $\mathrm{ID}_3 = -40$ dB. Using (15.194), we have

$$\mathrm{OIP}_3 = I_{D1} - \frac{\mathrm{ID}_3}{2} = 22 \text{ dBm} \tag{15.200}$$

whereas the IIP_3 is 2 dB lower (i.e., $\mathrm{IIP}_3 = 20$ dBm).

For signal levels corresponding to an intermodulation of $\mathrm{ID}_3 = 45$ dB, we have

$$I_{D1} = \mathrm{OIP}_3 + \frac{\mathrm{ID}_3}{2} = 22 - \frac{45}{2} = -0.5 \text{ dBm} \tag{15.201}$$

However, this value is the level of the output signal, so the input signal should be 2 dB lower or, equivalently, the input-signal level should be at −2.5 dBm. Note that this result could have been obtained more directly by noting that a 5-dB improvement in distortion was desired, implying that the signal level should be decreased by (5 dB)/2.

Finally, we use (15.199) to find

$$\mathrm{SFDR} = \frac{2}{3}(22 + 50) = 48 \text{ dB} \tag{15.202}$$

from which the output level is given by

$$I_{D1}^* = \mathrm{SFDR} + N_o = -2 \text{ dBm} \tag{15.203}$$

Thus, when the output level is at –2 dBm, the third-order intermodulation power equals the noise power. If the output level is increased, the distortion products will increase and limit the dynamic-range performance. However, if the output level is decreased, the distortion products will be buried below the noise floor, and the noise will limit dynamic-range performance. Therefore, optimum dynamic-range performance is obtained at an output level of –2 dBm. However, note that the dynamic-range performance is actually 3 dB below the SFDR value since the dynamic range is based on the ratio of the signal power to the distortion plus the noise power (which are both equal at this point).

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15.10 PROBLEMS

Unless otherwise stated, assume the following:

- npn bipolar transistors:
  $\beta = 100$
  $V_A = 80$ V
  $\tau_b = 13$ ps
  $\tau_s = 4$ ns
  $r_b = 330\ \Omega$
- n-channel MOS transistors:
  $\mu_n C_{ox} = 92\ \mu A/V^2$
  $V_{tn} = 0.8$ V
  $\gamma = 0.5\ V^{1/2}$
  $r_{ds}(\Omega) = 8{,}000L\ (\mu m)/I_D\ (mA)$ in active region
  $C_j = 2.4 \times 10^{-4}\ pF/(\mu m)^2$
  $C_{j\text{-}sw} = 2.0 \times 10^{-4}\ pF/(\mu m)$
  $C_{ox} = 1.9 \times 10^{-3}\ pF/(\mu m)^2$
  $C_{gs(overlap)} = C_{gd(overlap)} = 2.0 \times 10^{-4}\ pF/\mu m$
- p-channel MOS transistors:
  $\mu_p C_{ox} = 30\ \mu A/V^2$
  $V_{tp} = -0.9$ V
  $\gamma = 0.8\ V^{1/2}$
  $r_{ds}(\Omega) = 12{,}000L(\mu m)/I_D(mA)$ in active region
  $C_j = 4.5 \times 10^{-4}\ pF/\mu m^2$
  $C_{j\text{-}sw} = 2.5 \times 10^{-4}\ pF/\mu m$
  $C_{ox} = 1.9 \times 10^{-3}\ pF/(\mu m)^2$
  $C_{gs(overlap)} = C_{gd(overlap)} = 2.0 \times 10^{-4}\ pF/\mu m$

15.1 Show that the input impedance (at nodes i_o) of the Miller integrator shown in Fig. 15.6 is on the order of $2/(g_{m2}^2 r_{ds})$ at frequencies where capacitors $2C_1$ can be considered short circuits.

15.2 Based on the block diagram of Fig. 15.9, find transconductance values for a first-order filter with a dc gain of 10 and a pole at 15 MHz (no finite zero). Assume the integrating capacitors are sized $C_A = 5$ pF.

15.3 Find the transconductance and capacitance values of the second-order filter of Fig. 15.11 for a low-pass filter with a pole frequency of 10 MHz, $Q = 1$, and a dc gain of 5.

15.4 Derive the design equations for the biquad circuit shown in Fig. 15.24.

15.5 Consider the transconductor shown in Fig. 15.13. Find the transconductance of this circuit for finite opamp gains A.

15.6 In the transconductor of Fig. 15.12(*b*), find the minimum collector voltages of Q_1, Q_2 such that they remain in the active region for $v_i = \pm 1$ V around a common-mode voltage of 2 V. Repeat for the transconductor of Fig. 15.13.

15.7 In the transconductor of Fig. 15.14, find the new transconductance value if the base-emitter areas of Q_7, Q_8 are four times those of Q_3, Q_4.

15.8 Consider the transconductor of Fig. 15.14, where we want $G_m = 1$ mA/V. What are reasonable values for I_1 and I_2 such that all transistors do not fall below 20 percent of their nominal bias current when the peak value of $v_i = v_i^+ - v_i^-$ is 500 mV?

15.9 Consider the linearized two-differential pairs shown in Fig. 15.20, where $I_1 = 2$ mA. Find the percentage of error between an ideal linear transconductor and the true output current when $v_i = 48$ mV.

15.10 Consider the circuit Fig. 15.21, with $I_1 = 100$ μA, $I_2 = 10$ μA, $(W/L)_9 = 2$, $V_C = 5$ V, and $v_i^- = 2.5$ V.

- **a.** Find the transconductance, G_m.
- **b.** Assuming a perfectly linear transconductor, find i_{o1} when v_i^+ equals 2.6 V and 3 V.
- **c.** Find the true value of i_{o1} when v_i^+ equals 2.6 V and 3 V by taking into account the triode equation for Q_9 (assume everything else is ideal). Compare your results with those in part b.

15.11 Choose reasonable transistor sizes for the circuit in Fig. 15.25 to realize a transconductor that has $G_m = 0.3$ mA/V, $k_1/k_3 = 6.7$, and a peak differential-input voltage of 1 V.

15.12 Consider the circuit in Fig. 15.30, where all transistors have $W/L = 10\ \mu m/2\ \mu m$, $V_{DD} = -V_{SS} = 2.5$ V, and $V_{C1} = -V_{C2} = 2.0$ V. Find the transconductance of the circuit.

15.13 Show that the transconductance of Fig. 15.32 is given by

$$G_m = \left(\frac{n}{n+1}\right)4\sqrt{kI_B}$$

15.14 Consider the transconductor shown in Fig. 15.34, where all transistors have size $W/L = 10\ \mu m/2\ \mu m$, $I_B = 50$ μA, and $V_{DD} = -V_{SS} = 3$ V. What

is the maximum differential input, $v_1 - v_2$ (centered around 0 V), that can be used while maintaining proper operation?

15.15 Show that the circuit of Fig. 15.36 results in

$$i_1 - i_2 = K\left(V_B - 2V_{tn}\right)\left(2v_1 - V_B\right)$$

15.16 Using two-transistor integrators, design a MOSFET-C second-order low-pass filter with a pole frequency of 1 MHz, $Q = 1$, and a dc gain of 2. Let the integrating capacitors be 10 pF, $V_C = 3$ V, and $V_x = 0$ V.

15.17 Calculate the percentage THD value of a signal in which the fundamental component is at 1 MHz and has a voltage level of 1 V_{rms}, and the only significant harmonics are the first three above the fundamental. These harmonics, at 2 MHz, 3 MHz, and 4 MHz, are measured to have voltage levels of 1 mV_{rms}, 0.5 mV_{rms}, and 0.3 mV_{rms}, respectively.

15.18 If a circuit is measured to have $IIP_3 = 10$ dBm and has a gain of 6 dB, what output-signal level should be used such that the third-order intermodulation products are 60 dB below the fundamental?

15.19 At an input-signal level of −4 dBm, an intermodulation ratio of −40 dB was measured in a filter with a gain of 6 dB. Calculate the value of the input and output third-order intercept points. What input-signal level should be applied if we want an intermodulation ratio of −50 dB? If the noise power at the output is measured to be −60 dBm, what is the expected SFDR and what output-signal level does it correspond to?

CHAPTER

16 Phase-Locked Loops

Phase-locked loops (PLL) are analog building blocks used extensively in many analog and digital systems. An application where PLLs are used is clock recovery in many communication and digital systems. A second application area is frequency synthesizers used in televisions or wireless communication systems to select different channels. A third area is in the demodulation of frequency-modulated signals. These are only a few of the application areas, but it is safe to say that phase-locked loops have become an important building block in many electronic systems.

Although PLLs are highly nonlinear systems, it has been found that when they are in lock, their transient behavior can be reasonably well approximated by linear differential equations. Indeed, analysis methods similar to those first developed to describe PLLs have now been applied to other important nonlinear systems such as adaptive filters and switching power supplies. Thus, understanding the small-signal modelling of PLLs can be very useful in understanding many important signal-processing systems.

16.1 BASIC LOOP ARCHITECTURE

The basic architecture of a PLL is shown in Fig. 16.1 The PLL usually consists of a phase detector, a low-pass filter, a gain stage, and a *voltage-controlled oscillator* (VCO) configured in a loop. The phase detector is a circuit that normally has an output voltage with an average value proportional to the phase difference between the input signal and the output of the VCO. The low-pass filter is used to extract the average value from the output of the phase detector. This average value is then amplified and used to drive the VCO. The negative feedback of the loop results in the output of the VCO being synchronized with the input signal. Depending on the type of the phase-locked loop, the output of the oscillator may or may not have a phase difference compared with the phase of the input signal.

In most PLLs, the low-pass filter is first or second order. The simplest possibility is an RC low-pass filter, which historically has been the most commonly used filter. However, as will be seen shortly, a first-order filter having a low-frequency pole and a higher-frequency zero is recommended. There are many possibilities for the phase detector, including a simple exclusive-OR gate, a sample and hold, an analog multiplier, or a combination of digital circuits such as D flip-flops. The voltage-controlled

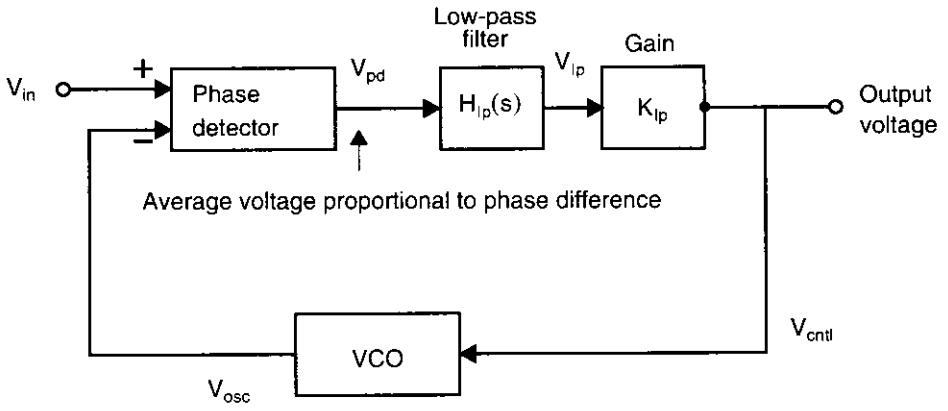


Fig. 16.1 The basic architecture of a phase-locked loop.

oscillator typically has an output that is either a square wave or a sinusoidal signal. A square-wave output might be used in applications where the input is a digital signal, whereas a sinusoidal output might be used in a wireless frequency synthesizer, for example. Normally, the amplitude of the input signal will be known, since its value can affect loop dynamics depending on the choice of phase detector. When the input signal's amplitude is not known, the input might be converted into a digital signal by first sending it through a limiter circuit, or perhaps the input signal may be amplified to a predetermined amplitude by applying it to an automatic-gain-control (AGC) circuit.

To understand phase-locked loops, a simple example will be considered. In this example, the input signal, V_{in}, is assumed to be a sinusoid with a known amplitude. The phase detector is realized as an analog multiplier having a relationship given by

$$V_{pd} = K_M V_{in} V_{osc} \tag{16.1}$$

where V_{osc} is the VCO output, V_{pd} is the phase-detector output, and K_M is a multiplication constant. It will also be assumed that the low-pass filter has a transfer function given by

$$H_{lp}(s) = \frac{1 + s\tau_z}{1 + s\tau_p} \tag{16.2}$$

where $\tau_z << \tau_p$. This first-order transfer function is known as a *lead-lag filter* and represents a fairly general form for PLL applications.

Let the input signal be described by a sinusoid having

$$V_{in} = E_{in} \sin(\omega t) \tag{16.3}$$

and the output of the voltage-controlled oscillator is given by a sinusoid where

$$V_{osc} = E_{osc} \sin(\omega t - \phi_d + 90°) = E_{osc} \cos(\omega t - \phi_d) \tag{16.4}$$

The argument ϕ_d represents the phase difference between the input signal and the output of the oscillator. The reason for the 90° offset is so that when the phase difference

is zero the average output of the phase detector (which is an analog multiplier for our example) is zero. The combination of an analog multiplier followed by a low-pass filter performs what is commonly known as the correlation function on analog signals. When the input signal and the VCO output have a 90° phase difference (i.e., $\phi_d = 0$), they are uncorrelated and the output of the low-pass filter will be zero. From this 90° phase offset, if the phase difference changes so that the two waveforms are more in phase (i.e., $\phi_d > 0$), then the correlation and, therefore, the output of the low-pass filter will be positive. For example, from (16.4), if $\phi_d = 90°$, then the output of the oscillator and the input signal would be exactly in phase, and the average output of the phase detector is found to be the amplitudes of the two sinusoids multiplied together and divided by two, resulting in

$$V_{cntl} = K_{lp}K_M\frac{E_{in}E_{osc}}{2} \tag{16.5}$$

This situation is approximately shown in Figure 16.2, where ϕ_d is taken slightly smaller than 90° to distinguish the two waveforms. Also shown is the output of the multiplier, V_{pd}, for the case of $E_{in} = E_{osc} = 1$ V, and $K_M = 1\ V^{-1}$. Here, it is seen that the output is at twice the frequency of the input signal and that it has an offset voltage of approximately 1/2 V. This corresponds closely to the maximum possible output of the low-pass filter. On the other hand, if the phase changes so as to make the two waveforms more out of phase, then the correlation between them and the output of the low-pass filter will be negative. Shown in Fig. 16.3 are some examples of the different waveforms. It is readily seen that $\phi_d > 0$ corresponds to the waveforms that are more in phase.

These statements can be quantified analytically. The output of the phase detector is given by

$$V_{pd} = K_M V_{in} V_{osc} = K_M E_{in} E_{osc} \sin(\omega t)\cos(\omega t - \phi_d) \tag{16.6}$$

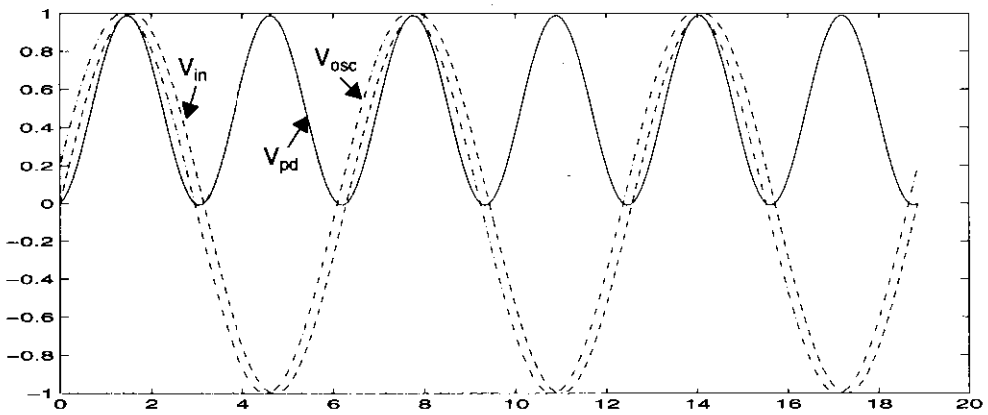


Fig. 16.2 The output of the phase detector when the input signal and the oscillator are nearly in phase.

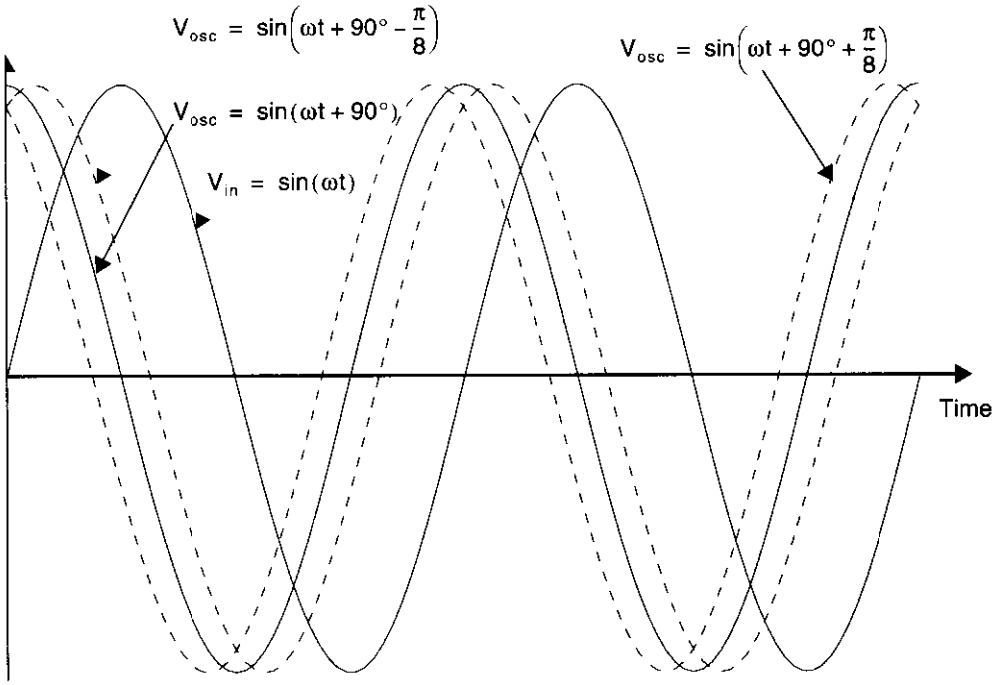


Fig. 16.3 The relative phase angles of the input signal and the output of the oscillator.

Using the trigonometric identity

$$\sin(A)\cos(B) = \frac{1}{2}[\sin(A+B) + \sin(A-B)] \tag{16.7}$$

we have

$$V_{pd} = K_M \frac{E_{in}E_{osc}}{2}[\sin(\phi_d) + \sin(2\omega t - \phi_d)] \tag{16.8}$$

The low-pass filter's function is to remove the second term at twice the frequency of the input signal.[1] The signal V_{cntl} is therefore given by

$$V_{cntl} = K_{lp}K_M \frac{E_{in}E_{osc}}{2}\sin(\phi_d) \tag{16.9}$$

Note that V_{cntl} is either a dc value or a slowly varying signal, assuming that the frequency of the input signal is constant or slowly varying. For small ϕ_d, we can approximate (16.9) as

$$V_{cntl} \cong K_{lp}K_M \frac{E_{in}E_{osc}}{2}\phi_d = K_{lp}K_{pd}\phi_d \tag{16.10}$$

1. The extent to which this is not true is a major source of distortion when sinusoidal VCOs are used.

Thus, the output of the low-pass filter is approximately proportional to the phase difference between the output of the oscillator and the input signal, assuming the 90° offset bias is ignored. This approximation is used in analyzing the PLL to obtain a linear model. The constant of proportionality is called K_{pd} and is given by

$$K_{pd} = K_M \frac{E_{in}E_{osc}}{2} \tag{16.11}$$

Note that with this analog-multiplier phase detector, K_{pd} is a function of the input amplitude and oscillator output amplitude. As we shall soon see, K_{pd} affects loop dynamics, and thus we see the need for having known values for E_{in} and E_{osc}.

To understand the operation of the PLL, assume the VCO has a free-running frequency ω_{fr} when its input is zero. Also, assume that the input signal is initially equal to the free-running frequency of the VCO, and the system is in lock with $\phi_d = 0$ and the output of the low-pass filter is also equal to zero. Next, assume the input frequency slowly increases. This will initially cause it to lead the VCO output (again ignoring the 90° offset), which corresponds to $\phi_d > 0$, since ϕ_d is defined as the difference between the input signal's phase minus the VCO's output signal's phase. Since for $\phi_d = 0$, the input and VCO output were 90° out of phase, now with $\phi_d > 0$, the two waveforms will become more in phase (see Fig. 16.3) and after a short time (roughly the time constant of the low-pass filter) the output of the low-pass filter will go positive. Since the two waveforms are now assumed to be at slightly different frequencies, the phase difference, and therefore the output of the low-pass filter, will slowly continue to increase. However, the frequency of the VCO is proportional to its control voltage, so the increase in the low-pass filter's output will cause the VCO's frequency to increase until it is the same as that of the input signal again, which will keep the two signals in synchronism (i.e., locked). Of course, the opposite would occur if the input signal's frequency decreased. Specifically, the average output of the phase detector would become negative, which, after being averaged by the low-pass filter, would drive the oscillator to a lower frequency until it is again identical to the frequency of the input signal and the two waveforms are again synchronized. It is readily seen here that the phase-locked loop stays in lock because of the negative feedback of the loop in which the phase of the oscillator's output is subtracted from the phase of the input signal.

Note, however, that at this new input frequency, which does not equal the free-running frequency of the VCO, their phase difference is no longer 90°. We can find the new phase difference for these two locked signals by noting that the frequency of the oscillator's output signal is given by

$$\omega_{osc} = K_{osc}V_{cntl} + \omega_{fr} \tag{16.12}$$

Here, ω_{fr} is the free-running frequency of the VCO when its control voltage is zero and K_{osc} is a constant relating the change in frequency to control voltage ratio. The output voltage of the amplified low-pass filter is now given by

$$V_{cntl} = \frac{\omega_{in} - \omega_{fr}}{K_{osc}} \tag{16.13}$$

where ω_{in} is the frequency of the input signal, which is equal to the frequency of the oscillator's output. From (16.10), we also have

$$\phi_d = \frac{V_{cntl}}{K_{lp}K_{pd}} = \frac{\omega_{in} - \omega_{fr}}{K_{lp}K_{pd}K_{osc}} \tag{16.14}$$

EXAMPLE 16.1

Consider a PLL where the amplitudes of the input signal and the oscillator output are both at a 0.75-V peak. An analog multiplier is being used for the phase detector, which would have a 2-V output when both inputs are dc values of 2 V. The VCO has a free-running frequency of 10 MHz, which would decrease to zero for $V_{cntl} = -1$ V, and the gain block is unity (i.e., $K_{lp} = 1$). When in lock, what is the phase difference between the input and oscillator output when the input frequency is 11 MHz? What is the phase difference when the input is 9 MHz? How does the phase difference change if $K_{lp} = 2$?

Solution

Since $V_{pd} = K_M V_{in} V_{osc}$, we have $K_M = 0.5\ V^{-1}$. Using (16.11), we also have

$$K_{pd} = K_M \frac{E_{in}E_{osc}}{2} = 0.1406\ \text{V/rad} \tag{16.15}$$

In addition, we find

$$K_{osc} = \frac{\Delta\omega_{osc}}{\Delta V_{cntl}} = \frac{2\pi \times 10^7\ \text{rad/s}}{1\text{V}} = 6.28 \times 10^7\ \text{rad/Vs} \tag{16.16}$$

Making use of (16.14), we have for the case $\omega_{in} = 11$ MHz,

$$\phi_d = \frac{2\pi \times (11\ \text{MHz} - 10\ \text{MHz})}{K_{lp}K_{pd}K_{osc}} = 0.7112\ \text{rad} = 40.8^\circ \tag{16.17}$$

resulting in the phase difference between the input and oscillator output being $90^\circ - 40.8^\circ = 49.2^\circ$ (i.e., becoming closer to an in-phase difference of 0°).

For the case where $\omega_{in} = 9$ MHz, we have $\phi_d = -40.8^\circ$, resulting in a phase difference of 130.8° (i.e., becoming closer to an out-of-phase difference of 180°).

If $K_{lp} = 2$, then half the phase difference results in the same VCO control voltage, V_{cntl}. Therefore, for $\omega_{in} = 11$ MHz, $\phi_d = 20.4^\circ$, and for $\omega_{in} = 9$ MHz, $\phi_d = -20.4^\circ$.

Linearized Small-Signal Analysis

The phase-locked loop is a highly nonlinear system. Fortunately, once a PLL is in lock, its dynamic response to input-signal phase and frequency changes can be well

approximated by a linear model, as long as these changes are slow and small about their operating or bias point.

Before the linear model is presented, first consider a sinusoidal signal where the frequency is slowly varying with time. This signal can be represented by the equation

$$v(t) = E \sin[\omega(t)t + \phi_d(t)] \tag{16.18}$$

where $\omega(t)$ and $\phi_d(t)$ are both deterministic signals that slowly change with time. The total phase at any instance in time is given by

$$\phi(t) = \omega(t)t + \phi_d(t) \tag{16.19}$$

For the time being, assume $\phi_d(t)$ is a constant. The instantaneous frequency is defined to be

$$\omega_{inst}(t) = \frac{d\phi(t)}{dt} \tag{16.20}$$

Note that in the case where $\omega(t)$ is also a constant, we see from combining (16.19) and (16.20) that we have the satisfying intuitive result that the instantaneous frequency, $\omega_{inst}(t)$, is equal to $\omega(t)$.

If we integrate both sides of (16.20), we have

$$\phi(t) = \phi(0) + \int_0^t \omega_{inst}(\tau)\, d\tau \tag{16.21}$$

and we see that the *instantaneous phase is the integral of the instantaneous frequency.* From here on, we will assume that the instantaneous frequency and $\omega(t)$ are, for practical purposes, the same and drop the subscript from $\omega_{inst}(t)$ to make our notation simpler (although this simplification is not necessary). If we take the Laplace transform of both sides of (16.20), we have

$$\phi(s) = \frac{\omega(s)}{s} \tag{16.22}$$

where $\phi(s)$ and $\omega(s)$ are the Laplace transforms of $\phi(t)$ and $\omega(t)$, respectively. This relationship will be used in modelling the relationship between the VCO's input-control voltage and the phase of its output signal.

We can now give an approximately equivalent, small-signal model for a phase-locked loop that relates the phase of the input signal and oscillator output to the low-pass filter output voltage. It should be noted that this model is a small-signal model in that it relates changes about an operating point. In other words, the phase variable represents *changes in phase* from reference signals that were identical to the true signals at the beginning of the analysis. Similarly, any frequency variables, which will be introduced shortly, also represent *changes from the original frequencies* at the beginning of the analysis. A signal-flow graph for the linearized small-signal model is shown in Fig. 16.4. The constant, K_{pd}, is given by (16.11). Recalling (16.12),

$$\omega_{osc} = K_{osc} V_{cntl} + \omega_{fr} \tag{16.23}$$

note that since we are only modelling changes about an operating point, the term ω_{fr} is absent from the signal-flow graph (SFG) of Fig. 16.4, as it is a nonchanging bias term.

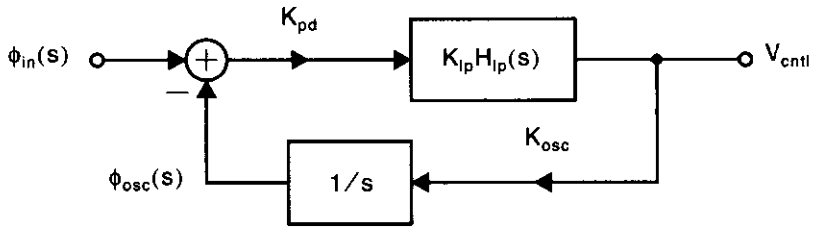


Fig. 16.4 A signal-flow graph for the linearized small-signal model of a PLL when in lock.

It is now possible to analyze the SFG of Fig. 16.4 to determine the transfer function that relates the Laplace transform of $V_{cntl}(s)$ to the Laplace transform of $\phi_{in}(s)$. We have

$$V_{cntl}(s) = K_{pd}K_{lp}H_{lp}(s)[\phi_{in}(s) - \phi_{osc}(s)] \tag{16.24}$$

and

$$\phi_{osc}(s) = \frac{K_{osc}V_{cntl}(s)}{s} \tag{16.25}$$

Combining equations (16.24) and (16.25) and rearranging gives

$$\frac{V_{cntl}(s)}{\phi_{in}(s)} = \frac{sK_{pd}K_{lp}H_{lp}(s)}{s + K_{pd}K_{lp}K_{osc}H_{lp}(s)} \tag{16.26}$$

Equation (16.26) is general in that it applies to almost every phase-locked loop. Differences between one PLL and another are determined only by what is used for the low-pass filter (which determines $H_{lp}(s)$), the phase detector (which determines K_{pd}), or the oscillator (which determines K_{osc}). Normally, most low-pass filters have a function similar to that given in (16.2). Substituting the first-order low-pass relation given in (16.2) into (16.26) and rearranging results in

$$H(s) = \frac{V_{cntl}(s)}{\phi_{in}(s)} = \frac{\frac{1}{K_{osc}}s(1 + s\tau_z)}{1 + s\left(\frac{1}{K_{pd}K_{lp}K_{osc}} + \tau_z\right) + \frac{s^2\tau_p}{K_{pd}K_{lp}K_{osc}}} \tag{16.27}$$

Thus, we see that the relationship is a second-order transfer function. The fact that the gain is zero at dc signifies that for phase changes (not frequency changes), the output of the low-pass filter will eventually settle to its original bias value.

To find the relationship between V_{cntl} and the input frequency, we can use (16.22) to obtain

$$\frac{V_{cntl}(s)}{\omega_{in}(s)} = \frac{\frac{1}{K_{osc}}(1 + s\tau_z)}{1 + \left(s\frac{1}{K_{pd}K_{lp}K_{osc}} + \tau_z\right) + \frac{s^2\tau_p}{K_{pd}K_{lp}K_{osc}}} \tag{16.28}$$

This transfer function has a dc gain of $1/K_{osc}$. This result was expected because the input voltage to the VCO must change by exactly this amount to keep the loop in lock when the input frequency changes.

Note that (16.28) has frequency appearing in two fashions. Specifically, we see that the input is frequency and the relationship between the input frequency and the low-pass filter's output voltage is also a function of the frequency variable, s. What this implies is that the low-pass filter's output voltage is a function of how fast the input frequency changes, which we have constrained to be slow. The variable s, when replaced by $j\omega$, represents the periodic rate at which the input frequency changes, assuming this change is sinusoidal.

In results of both (16.27) and (16.28), the transfer functions are second-order—a fortunate occurrence, as these transfer functions are well understood. Second-order transfer functions are often written in the form

$$H(s) = \frac{N(s)}{D(s)} \tag{16.29}$$

where $D(s)$, the denominator, is expressed as

$$D(s) = 1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2} \tag{16.30}$$

The constant ω_0 is called the resonant frequency of the transfer function. For small Q (around 1/2 or slightly larger), the transient time constant of the complete loop for small phase or frequency changes is roughly given by

$$\tau_{pll} \cong \frac{1}{\omega_0} \tag{16.31}$$

The constant Q is called the Q factor[2] of the transfer function. Normally, for good settling behavior when step changes of the input signal occur, one would choose a Q factor equal to 1/2. Such a choice results in real poles for the transfer function. Alternatively, one might want maximally flat group delay, in which case one would choose $Q = 1/\sqrt{3} = 0.577$. A third alternative would be to have maximally flat amplitude response, in which case one would choose $Q = 1/\sqrt{2} = 0.707$. For most PLL applications, the first choice of setting $Q = 1/2$ is recommended.

Setting the term multiplying each power of s in (16.30) equal to the corresponding term in the denominator of (16.27) or (16.28), then solving for ω_0 and Q, results in

$$\omega_0 = \frac{K_{pll}}{\sqrt{\tau_p}} \tag{16.32}$$

and

$$Q = \frac{\sqrt{\tau_p}}{\frac{1}{K_{pll}} + \tau_z K_{pll}} \tag{16.33}$$

2. For those more familiar with damping factor, σ, of a second-order transfer function, note that $\sigma = 1/2Q$.

where

$$K_{pll} = \sqrt{K_{pd}K_{lp}K_{osc}} \tag{16.34}$$

For most cases, when ω_0 is much less than the oscillator's free-running frequency, we have $\tau_z >> (1/K_{pll}^2) = 1/(K_{pd}K_{osc})$, and therefore

$$Q \cong \frac{1}{\omega_0 \tau_z} = \frac{\sqrt{\tau_p}}{\tau_z K_{pll}} \tag{16.35}$$

Note that taking $Q = 1/2$ and using (16.32) and (16.35) results in

$$\tau_z = \frac{2\sqrt{\tau_p}}{K_{pll}} = \frac{2}{\omega_0} \tag{16.36}$$

Thus, the frequency of the zero in the numerator of (16.28) (that is, $1/\tau_z$) is at one-half the resonant frequency of the loop. Remembering this fact makes for very simple component selection in PLLs. Note also that this zero is responsible for some peaking in the magnitude of the transfer function given in (16.28). This peaking might be a problem in some PLL applications (such as in some communication systems) but can be eliminated if necessary [Lee, 1992].

In a normal design process, the designer will either have little choice over K_{pd} and K_{osc} or will choose them based on practical considerations such as power dissipation and desired signal amplitudes. One would next choose τ_p to achieve the desired loop settling time, using (16.31) and (16.32). Finally, one would choose τ_z to obtain the desired Q factor of the loop.

Note that in the special case where $\tau_z = 0$ and the low-pass filter is a simple first-order low-pass filter with no zero (in which case it could be easily implemented using a resistor and a capacitor only), we have from (16.33)

$$Q = \sqrt{\tau_p}K_{pll} \tag{16.37}$$

Substituting (16.37) into (16.32) results in

$$\omega_0 = \frac{K_{pll}^2}{Q} = \frac{K_{pd}K_{osc}}{Q} \tag{16.38}$$

Thus, for a given K_{pll} and Q factor, the resonant frequency of the loop is completely determined. If the loop is designed to have ω_0 substantially less than $K_{pd}K_{osc}$, then Q will be large and its transient response will be extremely poor. This limitation is the major reason why most well-designed PLLs have a zero in the loop filter (i.e., $\tau_z \neq 0$).

EXAMPLE 16.2

Assuming the same conditions as in Example 16.1, design a low-pass filter for the loop so that the loop time constant is approximately 10 periods at 10 MHz and $Q = 1/2$.

Solution

Recall that $K_{pd} = 0.1406$ V/rad and $K_{osc} = 6.28 \times 10^7$ rad/Vs. Assuming $K_{lp} = 1$, then we have, using (16.34),

$$K_{pll} = \sqrt{K_{pd}K_{lp}K_{osc}} = 2{,}972 \text{ s}^{-1/2} \tag{16.39}$$

Since it is desired that the loop have a time constant of 100 periods, we have

$$\omega_0 = \frac{1}{\tau_{pll}} = \frac{10^7}{100} = 10^5 \text{ s}^{-1} \tag{16.40}$$

Using (16.32) gives

$$\tau_p = \left(\frac{K_{pll}}{\omega_0}\right)^2 = \frac{K_{pd}K_{lp}K_{osc}}{\omega_0^2} = 0.883 \text{ ms} \tag{16.41}$$

Thus, the pole of the low-pass filter is at a frequency given by

$$f_p = \frac{\omega_p}{2\pi} = \frac{1}{2\pi\tau_p} = 180 \text{ Hz} \tag{16.42}$$

Using (16.33) gives

$$\tau_z = \frac{\sqrt{\tau_p}}{QK_{pll}} - \frac{1}{K_{pll}^2} = 19.89 \ \mu\text{s} \tag{16.43}$$

which is almost twice as large as the time constant of the loop. Therefore, the zero of the low-pass filter is at 8.0 kHz. Note that if the slightly less accurate but simpler equation (16.36) had been used, we would have had $\tau_z = 20$ μs, an insignificant difference. The low-pass filter can be realized by the circuit shown in Fig. 16.5. This circuit has a transfer function given by

$$H_{lp}(s) = \frac{1 + sR_2C_1}{1 + s(R_1 + R_2)C_1} \tag{16.44}$$

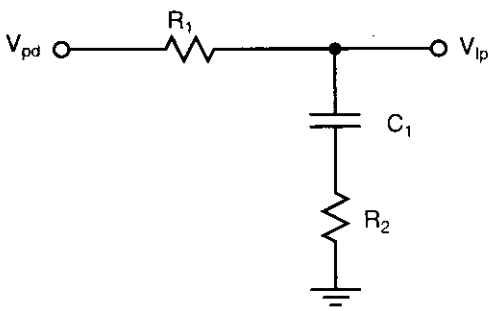


Fig. 16.5 The low-pass filter of Example 16.2.

If we somewhat arbitrarily choose $C_1 = 10$ nF, we find

$$R_2 = \frac{\tau_z}{C_2} = 1.99\ \text{k}\Omega \tag{16.45}$$

and

$$R_1 = \frac{\tau_p}{C_1} - R_2 = 86.4\ \text{k}\Omega \tag{16.46}$$

As an aside, if there were no zero in the low-pass filter's transfer function, using (16.37) we would have

$$Q = \sqrt{\tau_p} K_{pll} = 88.4 \tag{16.47}$$

This is an extremely high Q factor, which would cause the loop to be very slow when settling after a transient in either the input signal's phase or frequency. After the transient, the phase settling would be oscillatory, with an envelope having a time constant given by [Desoer, 1969]

$$\tau_{env} = \frac{2Q}{\omega_0} = 0.156\ \text{s} \tag{16.48}$$

which is 177 times greater than desired. This example points out the importance of having a zero in the PLL's low-pass filter.

Capture Range

The preceding linearized analysis describes the loop's dynamics accurately when it is in lock. However, the process of attaining lock is highly nonlinear, and little useful quantitative analysis has been developed to describe this process. Nonetheless, a qualitative description of what happens as the PLL is attaining lock is possible.

First, assume there is no input signal. The VCO would then oscillate at its free-running frequency, since the phase detector's output will, on average, be zero. Next, assume that an input signal appears close to the free-running frequency. If the frequency of the signal is close enough to the free-running frequency of the oscillator, then eventually the loop will lock onto the input signal. The maximum difference between the input signal's frequency and the oscillator's free-running frequency where lock can eventually be attained is defined as the *capture range*. This frequency is on the order of the pole frequency of the low-pass filter.

Next, assume the input signal suddenly appears at a slightly different frequency than the oscillator's frequency. Then the input signal will slowly wander in and out of phase with respect to the oscillator's output. Let us assume the input frequency is greater than the frequency of the oscillator's output. When the signals are in phase, the correlation between the two signals, and therefore the output of the low-pass filter, will be positive and the oscillator will be driven toward lock. When the signals are out

of phase, the correlation is negative and the oscillator's frequency will be driven away from lock. This phenomenon is called beating. The analog multiplier can be considered a demodulator. When the input signal's frequency is different from the oscillator's frequency, the input signal is demodulated to a frequency different from, but close to, dc. If this frequency is in the transition region of the low-pass filter, then when the oscillator is being driven toward lock, the output of the low-pass filter will increase in amplitude; whereas when the oscillator is being driven away from lock, the output of the low-pass filter decreases in amplitude. Therefore, with each beat, when the PLL is being driven toward lock, (which occurs when the two signals are more in phase than out of phase), the larger amplitude of the low-pass filter's output drives the loop closer toward lock than the smaller amplitude (which occurs when the signals are out of phase) drives the loop away from lock. Thus, during each beat, the VCO increases in frequency more than it decreases in frequency, and the loop gets closer to lock until eventually, after a number of beats, lock is attained.

Another reason for the VCO being driven toward lock, on the average, is that the demodulated beat signal is distorted, because when it is being driven away from lock it is at a higher instantaneous frequency than when it is being driven toward lock [Gardner, 1979]. This causes the time during which it is being driven toward lock to be larger than the amount of time it is being driven away from lock. The net effect is to cause the loop to become closer to lock with each beat.

However, if the initial frequency difference is quite large, the demodulated signal will not be in the transition region of the low-pass filter (assuming a zero is present). As a result, the difference in the VCO positive- and negative-going excursions will be zero or insignificant, and lock will not be attained, or only attained after an impractically long time.[3]

Analyses of the time required to attain lock are given in [Viterbi, 1966; Blanchard, 1976; and Gardner, 1979]. For the case where the initial difference between the input signal's frequency and the oscillator's frequency is moderately large, Blanchard showed that the acquisition time, t_{acq}, is approximately given by

$$t_{acq} = \frac{Q(\omega_{in} - \omega_{osc})^2}{\omega_0^3} \tag{16.49}$$

Obviously, when a PLL is designed to have a narrow loop bandwidth, ω_0, the acquisition time can be quite large. In many applications this process, whereby lock is attained, is too slow, especially when multipliers are used for the phase detectors. It is therefore common to add circuitry that will detect when the frequencies of the input signal and the VCO are different and drive the loop toward lock much more quickly than would otherwise occur. Once lock is attained, this additional circuitry will then detect that fact and no longer have an effect on the loop. This additional circuitry is

3. In [Blanchard, 1976; Gardner, 1979], it is stated that the capture range is theoretically infinite when the low-pass filter has its pole at zero (as is the case for the charge pump PLL to be described shortly). However, even when there is no pole at zero, if the initial frequency difference is large, the acquisition time can be so large as to make the PLL unusable. Also, it is possible that, due to circuit nonidealities such as offset voltages, lock may never be attained.

usually called a frequency detector. Alternatively, some PLLs have a low-pass filter with a programmable pole frequency. During initial acquisition, the pole frequency is relatively high in order to broaden the capture range and speed up the acquisition process. Once lock is achieved, the pole is changed to a much lower frequency to increase noise rejection. A third possible alternative is to sweep the VCO's frequency through its entire range during acquisition, with the PLL disabled, until it is detected that the VCO's frequency is close to that of the input signal, at which time the sweeping circuitry is disabled and the PLL is enabled.

Lock Range

Once lock is attained, as long as the input signal's frequency changes only slowly it will remain in lock over a range that is much larger than the capture range. This range is calculated as follows. From (16.5), the maximum output of the amplified low-pass signal is given by

$$V_{cntl\text{-}max} = K_{lp}K_M\frac{E_{in}E_{osc}}{2} = K_{lp}K_{pd} \tag{16.50}$$

Therefore, the maximum excursion of the VCO's frequency away from its free-running frequency is given by

$$\omega_{lck} = \pm K_{osc}K_{lp}K_{pd} \tag{16.51}$$

This result is valid when using a multiplier for a phase detector and assumes that the lock range is limited by the phase-detector limit rather than some internal voltage limits.

The PLL will track the input signal as long as the frequency of the input signal does not exceed this range. However, one should be cautious because, if the loop is locked to a frequency very different from the free-running frequency and a sudden phase change occurs, it is possible that the loop could skip a beat and fall out of lock. Once it has gotten out of lock, lock cannot be attained again until the input signal's frequency is changed to be within the capture range of the free-running frequency, which is much smaller than the lock range. Also, when the PLL is near the edge of the lock range, the gain of the phase detector has decreased substantially from its value around the free-running frequency of the VCO and substantially changes the loop dynamics. Specifically, from (16.32), ω_0 will be decreased, and therefore the loop will be slower in responding. Also, from (16.35), Q will be larger, which may cause the loop to be underdamped and therefore exhibit ringing when the input has transients. For these reasons, one often designs the loop so that the VCO frequency changes only over half the lock range.

EXAMPLE 16.3

What is the lock range for the PLL of Example 16.1?

Solution

Recall that $K_{pd} = 0.1406$ V/rad and $K_{osc} = 6.28 \times 10^7$ rad/Vs. Assuming $K_{lp} = 1$, then we have, using (16.51),

$$\omega_{lck} = \pm 2\pi \times 1.41 \text{ MHz} \tag{16.52}$$

In other words, when the input is 1.41 MHz away from the free-running frequency, the output of the phase detector is at a maximum (or minimum). Any further deviation from the free-running frequency causes the phase detector's average output to decrease (or increase), which results in the PLL's losing lock.

False Lock

Another phenomenon that may possibly occur when a multiplier is used for the phase detector is that the loop locks to harmonics of the input signal. For example, the PLL could lock to twice the frequency of the input signal, three times the frequency of the input signal, or any other multiple. Alternatively, it could lock to a submultiple of the frequency of the input signal (i.e., one-half, one-third, or other submultiple). This false lock will occur whenever the free-running frequency of the VCO is closer to a multiple or submultiple of the input signal's frequency than to its actual frequency. False lock can only be alleviated by somehow guaranteeing that the free-running frequency of the oscillator is closer to the actual input frequency than it is to some multiple or submultiple thereof. This requires a priori knowledge of the input signal and is a limitation on how much the input signal's frequency can vary. In the next section, a PLL phase comparator that does not exhibit this false-lock phenomenon will be described.

Exclusive-OR Phase Comparators

A PLL with an exclusive-OR phase comparator operates very similarly to a PLL with an analog multiplier for a phase comparator. An exclusive-OR logic gate has an output given by $V_{pd} = V_{in} \oplus V_{osc}$, where the amplitudes of the signals are determined by the logic levels. Some typical waveforms are shown in Fig. 16.6. It is seen that

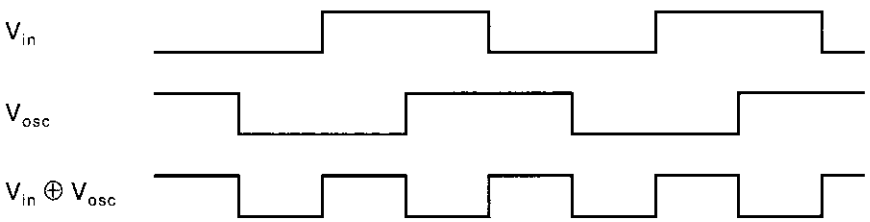


Fig. 16.6 Typical waveforms when an exclusive-OR gate is used as a phase comparator.

when the waveforms are 90° out of phase, the output is a waveform at twice the frequency of the input signal and has a 50 percent duty cycle. If all the waveforms are symmetric about 0 volts, then the output's average value as extracted by the low-pass filter would be zero. When the waveforms become more out of phase, the average value of the output signal is positive; whereas when they become more in phase, the average value of the output signal is negative. If the frequency of the input signal increases, the input signal and the oscillator become more out of phase, which causes the output of the low-pass filter to increase, thereby keeping the signals in lock. This is very similar to how the analog multiplier functions. Similar to PLLs using analog multipliers as phase comparators, PLLs having exclusive-OR gates as phase comparators also exhibit false lock.

16.2 PLLS WITH CHARGE-PUMP PHASE COMPARATORS

One phase-comparator that is popular for integrated applications is called the *charge-pump phase-comparator*. PLLs based on this phase comparator exhibit a number of desirable features. First, they do not exhibit false lock. Second, the input-signal and oscillator-output waveforms are exactly in phase when the system is in lock, even when the input frequency is not the same as the free-running frequency of the oscillator. Finally, the PLL attains lock quickly, even when the input frequency is quite different from the free-running frequency of the oscillator (assuming that a specific implementation of the sequential phase comparator is used). A charge-pump phase comparator is shown in Fig. 16.7. This phase comparator either injects, subtracts, or leaves alone the charge stored across a capacitor in the low-pass filter, depending on the output of a sequential phase-detector circuit. When S_1 is closed, I_{ch} flows into

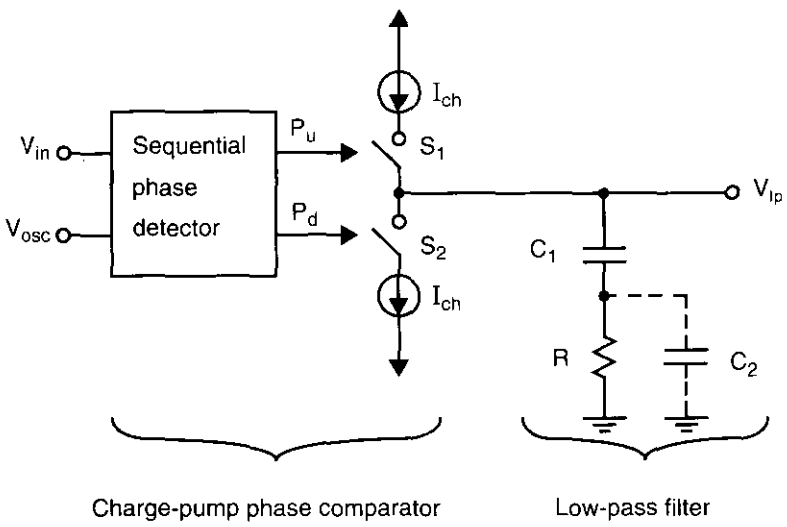


Fig. 16.7 A charge-pump phase comparator.

the low-pass filter, increasing the control voltage into the VCO; when S_2 is closed, I_{ch} flows out of the low-pass filter, decreasing the control voltage of the VCO. When both switches are open, the top plate of C_1 is open circuited and the output voltage remains constant in the steady state. The resistor, R, has been included to realize a zero in the low-pass filter's transfer function, similar to what was recommended when an analog multiplier is used for a phase comparator. This allows the designer to control the damping of the loop's transfer function separately from the time constant of the loop. The capacitor C_2 is included to suppress glitches; it has little effect on loop dynamics and will initially be ignored.

The sequential phase detector is a logic circuit that generates two outputs, P_u and P_d, depending on its inputs, V_{in} and V_{osc}. These are normally digital signals from the PLL input and the VCO, respectively.[4] Although there are many possibilities for the sequential phase detector, the one we will consider is controlled by the leading edges of V_{in} and V_{osc}. If V_{in} goes to 1 before V_{osc}, then P_u will be 1 during the time that the signals are different. This will inject some charge into the loop filter to speed up the VCO. Similarly, if V_{osc} goes to 1 before V_{in}, then P_d will be 1 during the time the inputs are different, S_2 will be closed, and charge will be subtracted from the loop filter, which decreases the VCO frequency. When the leading edges are coincident, ideally both P_u and P_d are always at 0, both S_1 and S_2 are always open, and the VCO input voltage is a constant dc value. For practical sequential phase detectors, both P_u and P_d may go high for a few gate delays when the input waveforms are coincident, but this time is usually short enough that it has very little effect on the dc output of the loop filter, and its effect is largely eliminated by the deglitching capacitor in the low-pass filter, C_2. The falling edges of both V_{in} and V_{osc} have no effect on P_u and P_d, which are both zero at this time. The waveforms when V_{in} leads V_{osc} are shown in Fig. 16.8. Notice that P_d never goes high in this case. Notice also that P_u only goes

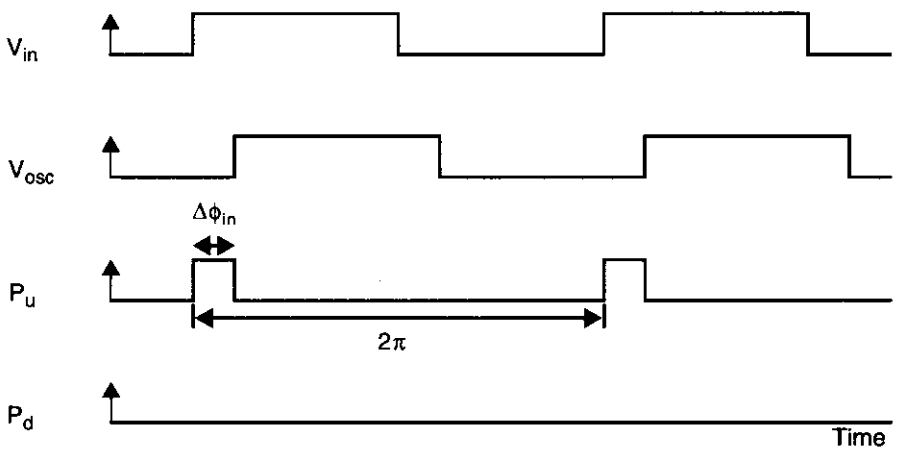


Fig. 16.8 Some typical waveforms of a charge-pump phase comparator.

4. This PLL is only used when the VCO output and the input are both digital signals or have been converted to digital signals by a limiter.

high at the leading edges but is insensitive to the falling edges. This makes the PLL insensitive to the duty cycles of the waveform.

As we shall see shortly, the resistor R in the low-pass filter is required to realize reasonable damping for the loop so that settling during transients is smooth, without oscillations. Unfortunately, it does cause a voltage glitch in the low-pass filter of magnitude $I_{ch}R$ when either S_1 or S_2 first turn on. Glitches occur because when the switches first turn on, the capacitors initially function as small-signal short circuits during the transients, and the change in the loop filter's output voltage is simply given by $I_{ch}R$. This glitch is greatly minimized by the inclusion of capacitor C_2. If C_2 is taken around $C_1/10$, then it usually has little effect on the loop dynamics, other than to decrease the damping slightly (i.e., increase the Q factor). To compensate for this, the loop is usually designed ignoring C_2, but the damping factor is taken greater than unity (or equivalently the Q factor is taken less than $1/2$) by a small factor.

To understand the operation of a charge-pump PLL, consider the case when the VCO's frequency is the same as the frequency of the input signal but their phases are different. Also, assume the input signal is leading the output of the VCO, as shown in Fig. 16.8. At each leading edge of V_{in}, S_1 turns on, which causes a current I_{ch} to flow into the low-pass filter. This current flows until the leading edge of V_{osc} goes high. The additional charge that is stored on C_1 is equal to the time that S_1 is on multiplied by I_{ch}, which causes an increase in the voltage across C_1 equal to

$$\Delta V_{C1} = \frac{\Delta Q_{C1}}{C_1} = \frac{I_{ch}\Delta t}{C_1} \tag{16.53}$$

This change increases the low-pass filter's output voltage, which in turn increases the frequency of the VCO. The VCO frequency increase causes the VCO's output to become more in phase with the input signal. Eventually they become locked in phase. At this time, ideally neither S_1 or S_2 will turn on anymore, and the output voltage of the low-pass filter, and therefore the control voltage of the PLL, will remain constant from then on, assuming the characteristics of the input signal remain constant.

Small-Signal Analysis of a Charge-Pump PLL

To do a small-signal analysis of a charge-pump PLL, it is necessary to make the assumption that the phase of the input and VCO signals change little in any given period. Assume that the frequencies of both signals are the same but the input signal leads the VCO output by a phase difference equal to $\Delta\phi_{in}$, as shown in Fig. 16.8. During this time, I_{ch} flows into the low-pass filter, whereas during the rest of the period, no charge will flow. Precise analysis of this system is difficult because it is time variant. Therefore, the analysis will be done on a different time-invariant system that has the same average charge flowing into the low-pass filter. As long as the dynamics of both systems change only slightly in a given period, the two systems are approximately equivalent. It might be mentioned that this type of approximation is also the basis for analyzing many other systems, such as switching power-supply regulators.

The average charge flowing into the low-pass filter for the charge-pump PLL is given by

$$I_{avg} = \frac{\Delta\phi_{in}}{2\pi} I_{ch} \tag{16.54}$$

So, we will analyze an approximately equivalent system that has a current I_{avg} flowing into an impedance $R + 1/(sC_1)$ (assuming C_2 is zero). We can then define a phase comparator for the approximately equivalent system, where

$$I_{avg} = K_{pd}(\phi_{in} - \phi_{osc}) = K_{pd}\Delta\phi_{in} \tag{16.55}$$

and

$$K_{pd} = \frac{I_{ch}}{2\pi} \tag{16.56}$$

If we further define $H_{lp}(s)$ to be given by

$$H_{lp}(s) = \frac{V_{lp}(s)}{I_{avg}(s)} = R + \frac{1}{sC_1} = \frac{1 + sRC_1}{sC_1} \tag{16.57}$$

we can substitute (16.55) and (16.57) into the general transfer function of a PLL, namely (16.26), to find the transfer function of a charge-pump PLL. Repeating (16.26) for clarity, we have

$$\frac{V_{lp}(s)}{\phi_{in}(s)} = \frac{sK_{pd}H_{lp}(s)}{s + K_{pd}K_{osc}H_{lp}(s)} \tag{16.58}$$

Note that K_{lp} has been absorbed into $H_{lp}(s)$ here for simplicity. Substituting (16.57) into (16.58) and rearranging gives

$$\frac{V_{lp}(s)}{\phi_{in}(s)} = \frac{1}{K_{osc}} \frac{s(1 + sRC_1)}{1 + sRC_1 + \dfrac{s^2C_1}{K_{pd}K_{osc}}} \tag{16.59}$$

Setting the coefficient of the s^2 term in the denominator of (16.59) equal to $1/\omega_0^2$ and solving for ω_0 results in

$$\omega_0 = \sqrt{\frac{K_{pd}K_{osc}}{C_1}} \tag{16.60}$$

Setting the coefficient of the s term in the denominator of (16.59) equal to $(1/\omega_0 Q)$ and solving for Q gives

$$Q = \frac{1}{RC_1\omega_0} = \frac{1}{R\sqrt{C_1K_{pd}K_{osc}}} = \frac{1}{R}\sqrt{\frac{2\pi}{C_1I_{ch}K_{osc}}} \tag{16.61}$$

When designing a charge-pump PLL one normally chooses I_{ch} based on practical considerations such as power dissipation and speed. Also, ω_0 is chosen so that the

loop has the desired transient settling-time constant according to

$$\omega_0 = \frac{1}{\tau_{pll}} \tag{16.62}$$

Next, C_1 is chosen using (16.60) and R is chosen using (16.61). At this point, it is a good idea to use a value for Q slightly less than what is eventually desired. This reduction accounts for the fact that when C_2 is eventually added to minimize glitches, the Q factor will be enhanced somewhat. A rule of thumb might be to take Q, say, 20 percent smaller than eventually desired. The final step is to add C_2. Another rule of thumb here is to take C_2 around one-eighth to one-tenth the size of C_1. The effect this will have on the transfer function is to make it third order by introducing a real pole at frequencies quite a bit higher than the resonant frequency of the loop. This could be taken into account during the design phase by substituting

$$H_{lp}(s) = \frac{R}{1 + sRC_2} + \frac{1}{sC_1} \tag{16.63}$$

into (16.58) and then solving for the poles. Since it is known that the additional pole will be real and at a frequency substantially higher than the original resonant frequency without C_2, the third-order system can be approximated by a second-order system. However, now the Q factor will be enhanced slightly by C_2,which is easily taken into account by taking R slightly larger than would be the case if C_2 were not present. Normally, this extra complication is not merited, but the complete system with C_2 should be simulated to ensure that the dynamics are not seriously degraded by the inclusion of C_2. The simulation of phase-locked loops is nontrivial and is the topic discussed in Section 16.4

EXAMPLE 16.4

Let $K_{osc} = 2\pi \times 50$ Mrad/V and $I_{ch} = 10$ μA. Assume that the free-running frequency of the oscillator is 50 MHz and that it is desired that the loop have a time constant of 100 cycles, or 2 μs. Design the components of the low-pass filter shown in Fig. 16.7.

Solution

A time constant of 2 μs corresponds to

$$\omega_0 = \frac{1}{2\ \mu s} = 500\ \text{krad/s} \tag{16.64}$$

Now, using (16.56) and (16.60), we have

$$C_1 = \frac{1}{\omega_0^2} \frac{I_{ch}}{2\pi} K_{osc} = 2\ \text{nF} \tag{16.65}$$

Let $C_2 = C_1/10 = 2.5$ pF and $Q = 0.4$. From (16.61), we have

$$R = \frac{1}{Q}\sqrt{\frac{2\pi}{C_1 I_{ch} K_{osc}}} = 31.4\,\text{k}\Omega \tag{16.66}$$

Phase / Frequency Detector

There are many ways to realize a sequential phase detector. Perhaps the most common sequential phase detector is the *phase/frequency detector* shown in Fig. 16.9. It is an asynchronous sequential logic circuit, and its operation is moderately complicated to follow. Although a detailed description of its operation will not be attempted here, a few comments are in order. The cross-coupled NOR gates basically form RS flip-flops. One of the top flip-flops will be set if either P_u or P_d is 1. One of the bottom flip-flops will be set whenever P_u or P_d must be disabled. When the PLL is in lock, this disabling occurs after the opposite signal has gone high. This disabling can also occur when the PLL is not in lock, by detecting a frequency difference between the input signal and the oscillator. The disabling flip-flops can only be reset when the appropriate input signal has changed to 0. The four-input NOR gate is primarily used to reset the top two flip-flops. This reset occurs when V_{in} and V_{osc} both become 1 when the loop is in lock. At this time, reset goes high, which resets the top two flip-flops, causing both P_u and P_d to go low.

To better understand the operation of the phase comparator, assume the PLL is in lock with V_{in} leading V_{osc}. Assume also that P_u, P_d, $P_{u\text{-dsbl}}$, $P_{d\text{-dsbl}}$, and reset are all low. In other words, all of the flip-flops are reset low. Furthermore, assume V_{in} and

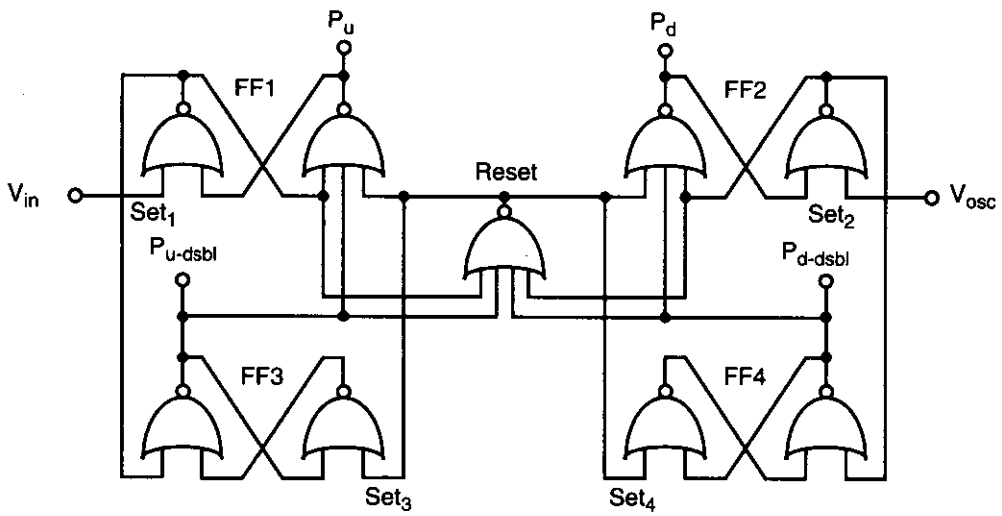


Fig. 16.9 A phase/frequency sequential phase detector based on NOR gates.

V_{osc} are both low, and then V_{in} goes high. The first thing that happens is FF1 gets set, causing P_u to go high. This causes the charge-pump to turn on and charge the low-pass filter, ultimately increasing the frequency of the VCO. Next, when V_{osc} goes to 1, FF2 is also set temporarily. Just after V_{osc} goes high, reset goes high. This causes P_u and P_d to go low one gate delay later. Also, reset going high causes FF3 and FF4 to be set. Thus, $P_{u\text{-}dsbl}$ and $P_{d\text{-}dsbl}$ go high two delays after reset goes high. These signals cause reset to go low one delay later. More importantly, they guarantee that FF1 and FF2 are kept in the reset mode, with both P_u and P_d low. It is only when V_{in} goes back to 0 that FF3 is reset and $P_{u\text{-}dsbl}$ is turned off. Similarly, when V_{osc} goes low, FF4 is reset and $P_{d\text{-}dsbl}$ goes low. We are now back in the original state, with all FFs in the reset state. The operation is very similar if V_{osc} leads V_{in}.

Now consider what happens when the frequencies are very different. Assume V_{in} is at a much higher frequency than V_{osc}. Whenever a positive-going edge of V_{in} occurs (which is quite often), P_u goes high, which causes the VCO frequency to increase. However, when V_{in} goes back to 0, P_u is still high if the much lower-frequency V_{osc} has not changed. P_u will stay high until both V_{in} and V_{osc} go to 1. At this time, reset goes high and $P_{u\text{-}dsbl}$ and $P_{d\text{-}dsbl}$ both get set, causing both P_u and P_d to go low. The next time V_{in} goes to 0, FF1 is reset, which in turn resets FF3, turning $P_{u\text{-}dsbl}$ off. However, if V_{osc} is still at a much lower frequency, V_{osc} is still at 1 and FF4 has not been reset. This guarantees that reset cannot go high. Thus, when V_{in} goes back to 1, FF1 is again set and remains set until V_{osc} eventually goes low (resetting FF2 and FF4) and then goes back high. Thus, it can be seen that most of the time P_u is high, with P_d seldom high, causing V_{osc} to quickly increase in frequency until lock is achieved.

The various waveforms when V_{in} is at a much higher frequency than V_{osc} are shown in Fig. 16.10. Note that most of the time P_u is at 1. It can only shut off if both $P_{u\text{-}dsbl}$ and $P_{d\text{-}dsbl}$ are in their reset states. For this to be the case, however, both V_{in}

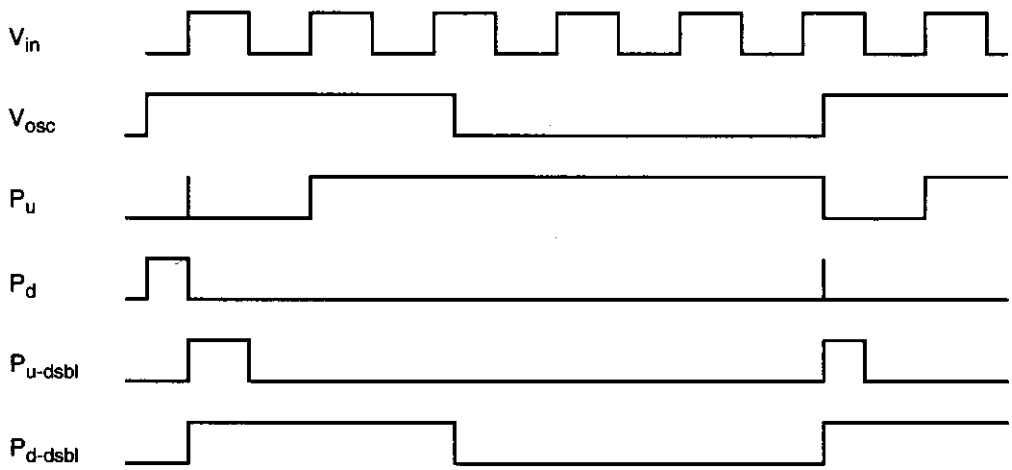


Fig. 16.10 The waveforms of a phase/frequency detector when V_{in} is at a much larger frequency than V_{osc}.

(for $P_{u\text{-}dsbl}$) and V_{osc} (for $P_{d\text{-}dsbl}$) must have been zero to reset FFs 3 and 4. Only after this happens, and then only after V_{in} and V_{osc} both go to 1, can reset go high, turning off P_u. Thus, this phase detector is very fast in acquiring lock. Also, it does not exhibit false lock as do multiplier or exclusive-OR phase detectors. Its only disadvantages are that it isn't suitable for nondigital or sinusoidal inputs and it can be "fooled" by noisy digital inputs having false edges or glitches because it is sensitive to positive-going edges of the input signal. If false edges are a possibility, one might put the input signal into a buffer to go through hysteresis before going into the PLL. Although this helps substantially, there will still be more jitter introduced than would be the case with a PLL having an analog multiplier, which averages the continuous waveforms rather than being sensitive to just the edges.

There are many other phase comparators that have been proposed for phase-locked loops. For example, sample and holds and D flip-flops. The interested reader is referred to [Buchwald, 1993; Meyr, 1990].

16.3 VOLTAGE-CONTROLLED OSCILLATORS

The first step in building a VCO, or *voltage-controlled oscillator*, is to realize an oscillator and then add a means whereby its frequency of oscillation can be controlled by an input voltage (although, in some cases the control signal could be a current). Oscillators come in a variety of different types, but perhaps the two major classifications are those that directly create sinusoidal outputs as opposed to those with square (or triangular) wave outputs. *Sinusoidal-output oscillators* are usually realized using some kind of frequency-selective or tuned circuit in a feedback configuration, whereas square-wave-output oscillators are usually realized using a nonlinear feedback circuit such as a relaxation oscillator or a ring counter. Sinusoidal oscillators realized using tuned circuits can be further classified into RC circuits, switched-capacitor circuits, LC circuits, and crystal oscillators. A table showing the classification of oscillators is shown in Fig. 16.11.

The design of tuned oscillators usually involves placing a tuned circuit into a feedback loop in which, at the oscillation frequency, the loop gain becomes positive and exactly equal to unity. Most integrated oscillators based on tuned circuits have

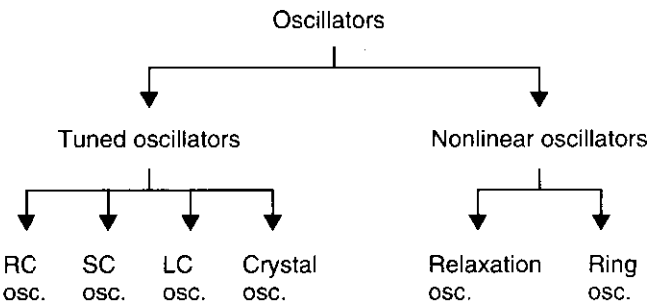


Fig. 16.11 Classification of oscillators.

been realized using either switched-capacitor circuits or integrated amplifiers with off-chip crystals or LC circuits. A switched-capacitor VCO has already been described in Chapter 10, and a number of other SC oscillators are described in [Gregorian, 1986]. The reference [Sedra, 1991] contains a good discussion on designing a variety of tuned oscillators that use RC circuits, LC circuits, and crystals. Most realizations of the first two types have been discrete circuits and were not integrated, although recently, integrated LC filters at frequencies of 1 GHz and up have been realized [Nguyen, 1992]. Another excellent reference on integrated oscillators, although somewhat dated, is [Grebene, 1984].

There are a variety of different methods used in maintaining the loop gain exactly at unity in tuned oscillators. Most of these techniques also determine the amplitude of the oscillator's output signal. The easiest method is to make use of some nonlinear element in the feedback loop. For small amplitude signals, the loop gain is greater than unity. The amplitude of the oscillator increases until the nonlinearity causes the effective loop gain to decrease to exactly unity. The simplest possible nonlinearity might be the limiting of the amplifier in the oscillator when its output gets too large, although for low distortion and a well-controlled amplitude, a more well-controlled nonlinearity is required. The former method is usually used for crystal oscillators. Other techniques might involve measuring the amplitude of the output signal, perhaps using a peak detector, and adjusting the Q factor of the poles of the circuit to be infinite when the amplitude is correct. When the amplitude is too large, the Q factor is changed to be large but positive, whereas when the amplitude is too small, the Q factor is adjusted to be large but negative. The first case corresponds to poles right on the $j\omega$ axis, the second case corresponds to poles close to the axis but in the left half-plane, whereas the last case corresponds to right-half-plane poles. In these cases, the oscillator's output amplitude remains constant, decreases, or grows, respectively. The amplitude-control loop can often be almost as complicated as a complete PLL. After this very cursory introduction to tuned amplifiers, they will be covered no further, as they are deemed to be out of the range of the subject matter of this book because very few of them have been integrated. Rather, a few examples of nonlinear digital-output VCOs will be described.

Bipolar Emitter-Coupled Multivibrator

One of the most popular configurations for a bipolar VCO has been the emitter-coupled multivibrator [Grebene, 1984]. This emitter-coupled oscillator is a form of a relaxation oscillator and is shown in Fig. 16.12. In this oscillator, Q_1 and Q_2 alternately turn on and off. When one of these transistors is off, the node at its emitter slowly changes to a more negative voltage due to the current flowing from the current source, I_1, connected to the emitter out of the capacitor, C_{osc}, which is also connected to the emitter. The node voltages for the case when Q_1 is cut off are shown in Fig. 16.13. During this time, the current through Q_2 is $2I_1$. The voltage at the collector of Q_2 will be one diode drop below the positive power-supply voltage, which is assumed to be 5 V. Here, we have assumed

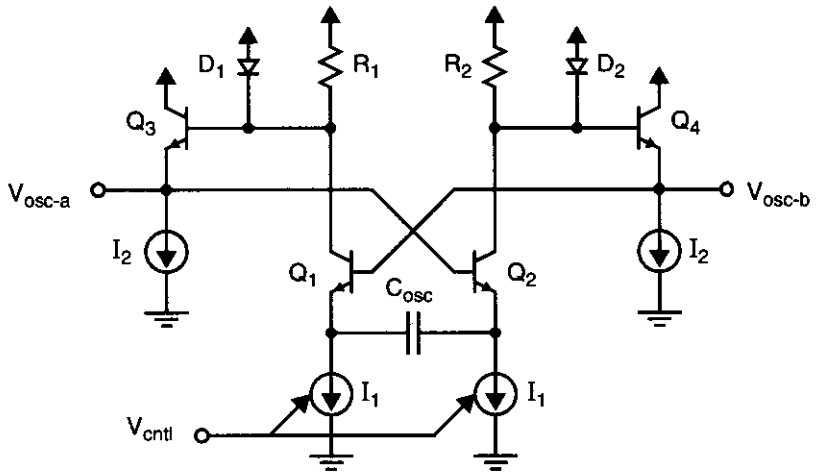


Fig. 16.12 An emitter-coupled relaxation oscillator.

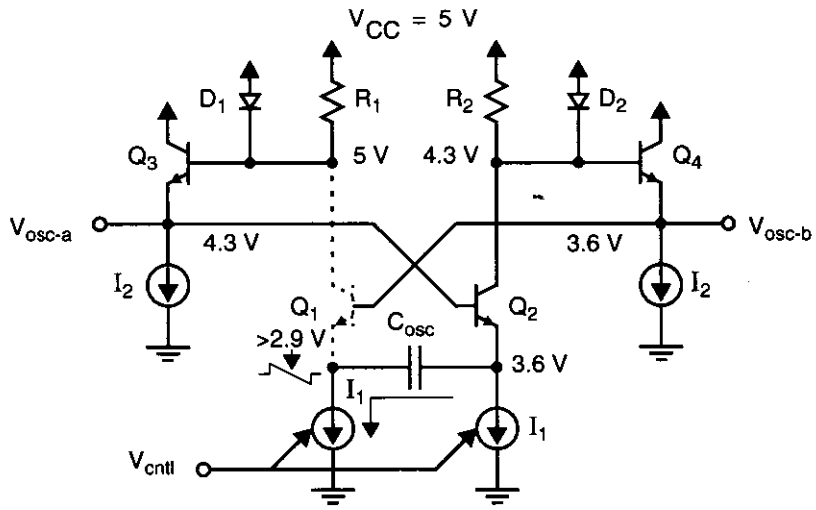


Fig. 16.13 The various voltages and currents of the oscillator in Fig. 16.12 when $V_{osc\text{-}a}$ is high.

$$2I_1R_2 > V_D \cong 0.7\ \text{V} \tag{16.67}$$

where V_D is the voltage drop of a conducting p-n junction. The voltage at the collector of Q_1 is approximately 5 V because Q_1 is off. Transistors Q_3 and Q_4 both operate as emitter-follower buffers and, thus, both have approximately 0.7 V base-emitter voltage drops. As a result, the right side of the capacitor C_{osc} is at 3.6 V and the left-side is at some voltage between 2.9 V and 4.3 V. This left-side voltage is changing in the negative-going direction with a rate of change given by

$$\frac{dV_{E1}}{dt} = \frac{I_1}{C_{osc}} \tag{16.68}$$

Its total voltage change will be from 3.6 V to 2.9 V or $2V_D \cong 1.4$ V. The time it takes for this voltage drop to occur is equal to one-half the period of oscillation and is given by

$$\frac{T}{2} = \frac{2V_D C_{osc}}{I_1} \tag{16.69}$$

After the emitter voltage reaches 2.9 V, Q_1 begins to conduct. The conduction of Q_1 causes its collector voltage to decrease from approximately V_{CC}, which in turn causes Q_2 to conduct less. A reduction in the conduction of Q_2 causes the collector voltage of Q_2 to increase, thereby turning Q_1 on more quickly. It is therefore seen that during the transition the circuit is in a positive-feedback loop, which causes it to change state very quickly. Thus, during the transition, Q_1 goes quickly from off to on, and Q_2 goes from on to off. When Q_2 turns off, its collector voltage goes to $V_{CC} = 5$ V, which, in turn, causes the left side of C_{osc} to quickly change from 2.9 V (its voltage when the transition began) to 3.6 V (its voltage after the change has taken place), via Q_4 and Q_1. The right side of C_{osc} must have the same voltage change, and it therefore changes from its 3.6-V initial voltage to 4.3 V. Since Q_2 is now turned off, the right side of C_{osc} is now discharged with a current equal to I_1, whereas the left side of C_{osc} is now held fixed at 3.6 V via Q_4 and Q_1. This process repeats itself indefinitely, resulting in the waveforms shown in Fig. 16.14. Thus, making use of (16.68), we have

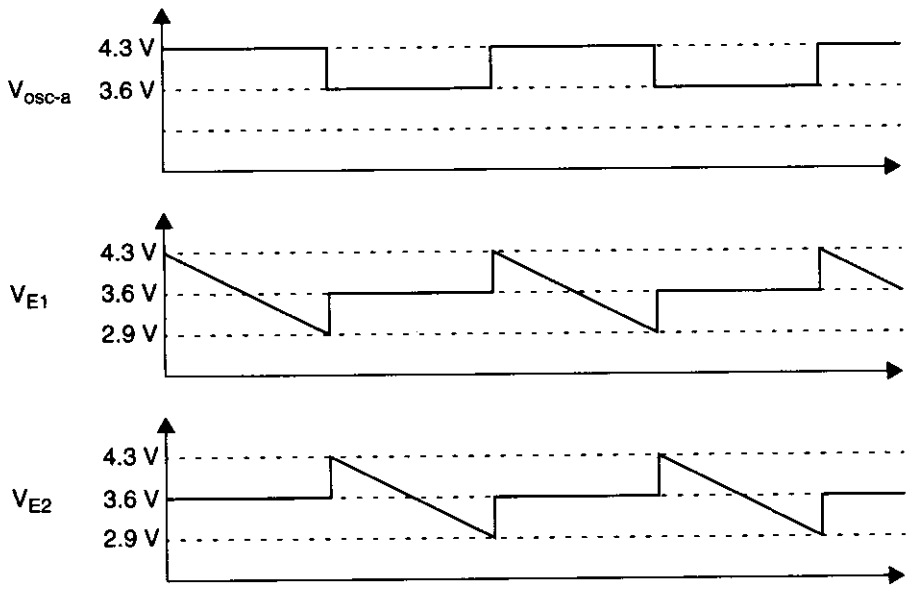


Fig. 16.14 The waveforms of the oscillator in Fig. 16.12.

$$f_{osc} = \frac{I_1}{4V_D C_{osc}} \tag{16.70}$$

To control the oscillator frequency, the current sources used to discharge C_{osc} (i.e., those labelled as I_1) are made proportional to a control voltage. Although methods for implementing linear voltage-controlled current sources were described extensively in Chapter 15 with respect to continuous-time filters, a simple example for making some reasonably linear, voltage-controlled current sources is shown in Fig. 16.15. This circuit uses emitter degeneration to obtain output currents at the collectors of Q_3 and Q_4, where

$$I_{C3} = I_{C4} \cong \frac{V_{cntl} - V_{ref}}{R} + I_1 \tag{16.71}$$

Combining equations (16.70) and (16.71), we have

$$f_{osc} = \frac{V_{cntl} - V_{ref}}{4V_D RC_{osc}} + f_{fr} \tag{16.72}$$

where

$$f_{fr} = \frac{I_1}{4V_D C_{osc}} \tag{16.73}$$

Therefore,

$$K_{osc} = \frac{1}{4V_D RC_{osc}} \tag{16.74}$$

These equations are all based on the assumption that the impedance looking into the emitters of the transistors is much less than R. When this is not the case, the linearity can be greatly improved by using techniques similar to those described in Section 15.2 on bipolar transconductors.

It should be noted that this oscillator can be strongly temperature dependent due to the temperature dependence of V_D—the voltage drop across a forward-biased

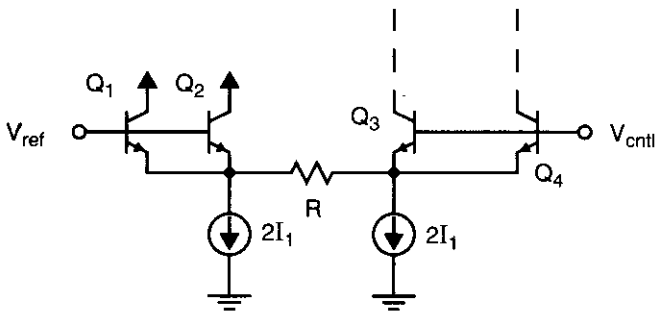


Fig. 16.15 A simple circuit for realizing approximately linear, voltage-controlled current sources.

diode. This temperature dependence can be greatly minimized by making all currents proportional to absolute temperature. The reader is referred to [Grebene, 1984] for details. Another source of error for this VCO is that as the currents I_1 of Fig. 16.12 become smaller, the base-emitter voltage drops of Q_1 and Q_2 also decrease. These V_{be} decreases cause the voltage changes across the capacitor C_{osc} to also become smaller. This source of nonlinearity can also be improved by circuit-design changes, but this topic is beyond the scope of this text.

Ring Oscillators

One of the most popular ways of realizing digital-output MOS VCOs is to use a *ring oscillator* and add voltage control to it. A ring oscillator is realized by placing an odd number of open-loop inverting amplifiers in a feedback loop. The simplest type of amplifier that can be used is a simple digital inverter, as shown in Fig. 16.16. This circuit is a form of negative feedback, but since each inverter has approximately 90° phase shift at its unity-gain frequency (assuming that all the loads on the inverters are matched and that there are at least three inverters in the loop) it is guaranteed that the loop gain will still be greater than unity when the phase shift around the loop becomes greater than 180°. As a result, the circuit is unstable and oscillations occur. Each half-period, the signal will propagate around the loop with an inversion. For example, assume the output of the first inverter changes to 1. This change will propagate through all five inverters in a time of $T/2$, at which time the output of the first inverter will change to 0; after an additional time of $T/2$, the first inverter's output will change back to 1, and so on. Assuming each inverter has a delay of τ_{inv} and that there are n inverters, we then have

$$\frac{T}{2} = n\tau_{inv} \tag{16.75}$$

Thus,

$$f_{osc} = \frac{1}{T} = \frac{1}{2n\tau_{inv}} \tag{16.76}$$

By making the delay of the inverters voltage controlled, the ring oscillator's frequency can be made voltage controlled.

It is very important that in CMOS technology, ordinary CMOS inverters not be used. This avoidance is because ordinary CMOS inverters have a gate-threshold voltage proportional to the power-supply voltage. Thus, when the power supply increases

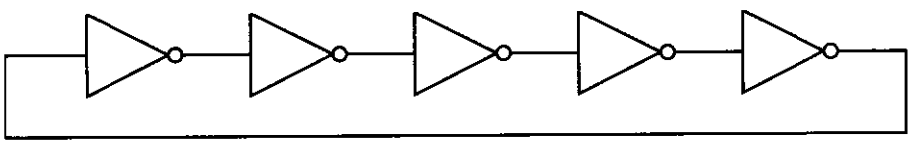


Fig. 16.16 A ring oscillator realized using five digital inverters.

in voltage, the voltage excursions increase in voltage proportionally, the currents of the inverters increase in proportion to the square of the power-supply voltages, and the frequency of oscillation increases proportionally to the power-supply voltage. Thus, any noise on the power-supply voltage will cause the oscillation frequency to have jitter. This poor power-supply rejection is perhaps the major source of jitter in integrated oscillators. In integrated oscillators, it is extremely important that the frequency of oscillation be independent of the power-supply voltage if low jitter is required.

In most integrated ring oscillators, fully differential inverters are used to obtain better power-supply insensitivity. When this is done, an even number of inverters can be used and the inversion required around the loop can be achieved by simply interchanging the outputs of the last inverter before feeding them back to the input, as shown in Fig. 16.17. This realization has a very important advantage in that the outputs of the middle inverters will have a quadrature phase relationship as compared with the last inverters (assuming all inverters and their loads are carefully matched) [Buchwald, 1991]. These quadrature outputs are very useful in many communication applications such as quadrature modulators and some clock-extraction circuits.

An example of realizing a fully differential inverter with a programmable delay is shown in Fig. 16.18, where the current-source loads are made voltage programmable. Cascode transistors, Q_3 and Q_4, have been added to increase the output impedance of the programmable current sources to make them more insensitive to power-supply noise. Assuming the current-source loads are proportional to V_{cntl} with a constant of

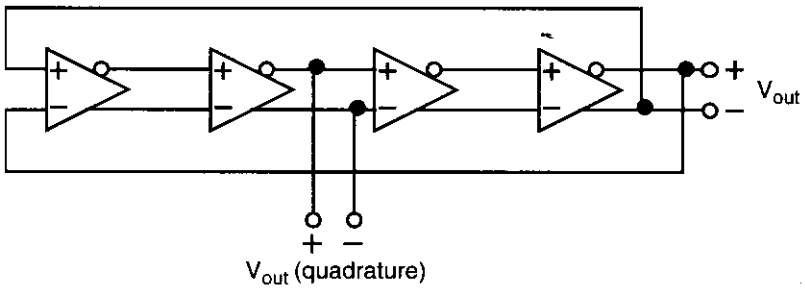


Fig. 16.17 Realizing a ring oscillator using fully differential inverters for improved power-supply rejection.

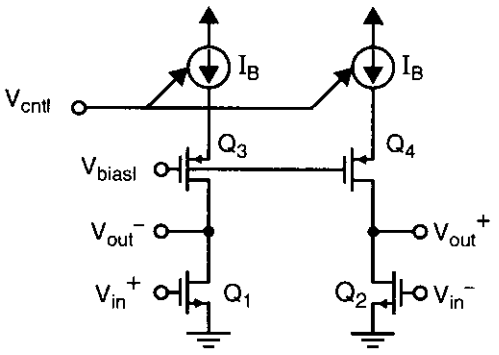


Fig. 16.18 A fully differential inverter with a programmable delay.

proportionality of K_{bias}, we have

$$I_B = K_{bias} V_{cntl} \tag{16.77}$$

The delay of each inverter is proportional to the unity-gain frequency of that inverter. In other words,

$$\tau_{inv} \propto \frac{C_L}{g_m} \tag{16.78}$$

where C_L is the load capacitance of the inverter and g_m is the transconductance of the drive transistors of the inverter. Since $g_m \propto \sqrt{I_B}$, we know that the delay is proportional to $1/\sqrt{I_B} \propto 1/\sqrt{V_{cntl}}$ and therefore, $f_{osc} \propto \sqrt{V_{cntl}}$. Thus, the relationship between the oscillation frequency and the control voltage is not very linear, but in many VCOs, this nonlinearity is not a problem. The major reason for nonlinearity is that at higher frequencies, the voltage changes at the outputs of each stage increase in amplitude because I_B increases. If the amplitudes of the voltage changes could be stabilized, the linearity would be greatly improved, as will be shown shortly.

The circuit shown in Fig. 16.19 can be used to realize the voltage-controlled current sources. The high gain of the opamp guarantees that its differential input voltage is very small, and, therefore, the voltage across the resistor R is very closely equal to V_{cntl}. Thus, the current through R is $I_R = V_{cntl}/R$. This current is mirrored by the wide-swing current mirrors consisting of Q_8 and Q_9 on the input side, and Q_3 and Q_5 for one output current source and Q_4 and Q_6 for the second output current source. The operation of the wide-swing current mirrors was described in Chapter 6, and will not be repeated here. In noncritical applications, it may be possible to use simpler current mirrors.

It is possible to realize a ring-oscillator VCO with good voltage-to-frequency linearity if one ensures that the voltage changes of the delay elements are independent of

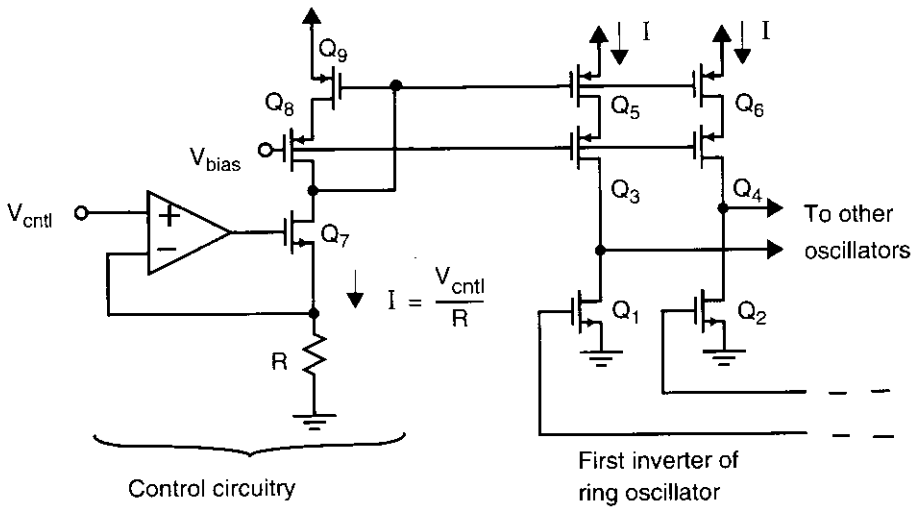


Fig. 16.19 A circuit that can be used to realize the voltage-controlled current sources required in Fig. 16.18.

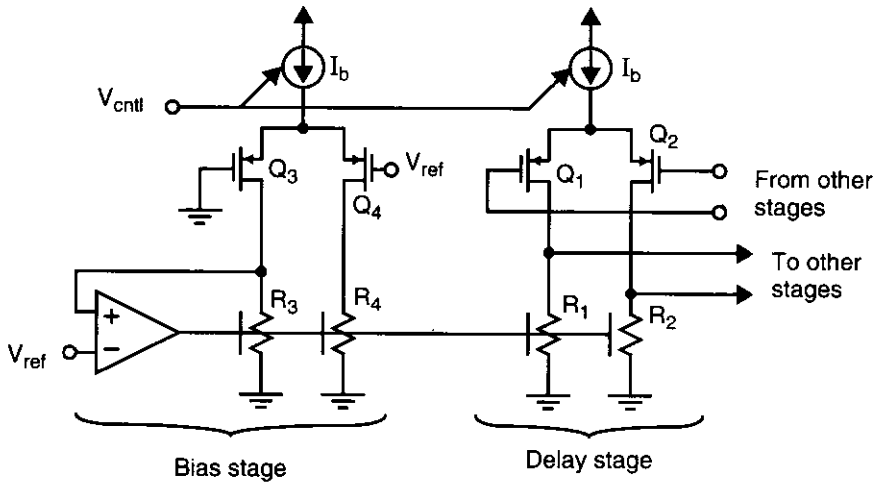


Fig. 16.20 A differential delay cell having resistive loads consisting of n-channel transistors.

the oscillation frequency [Kim, 1990; Young, 1992; Reynolds, 1994]. An alternative design for a differential delay stage where this linearization has been realized is shown in Fig. 16.20 [Young, 1992], along with the biasing circuitry that is used to control the voltage swings. Each stage consists of a differential amplifier with p-channel input resistors and resistive loads. The resistive loads are realized using n-channel transistors biased in the triode region. Their resistance is adjusted by the bias circuit so that when all of I_b is flowing through them, they will have V_{ref} across them, where V_{ref} is obtained from a temperature-independent voltage reference. This is achieved by using a replica of the delay cell in the bias circuit. The replica consists of Q_3, Q_4, R_3, and R_4. In the replica, all of I_b flows through Q_3 and R_3, so Q_4 and R_4 could have been eliminated from the circuit—they have been included in the figure for clarity only. Recalling that R_3 is actually realized by an n-channel transistor, it is seen that the negative feedback loop including the opamp will cause the voltage across R_3 to be equal to V_{ref} when I_b is going through it. Since the output of the opamp is also used to control the resistance of all the triode-region resistances used for the delay cells of the ring oscillator, they will also have V_{ref} across them when I_b flows through them. Next, if the VCO frequency changes because of a change in V_{cntl}, and therefore in I_b, the bias loop will change the resistance of the delay-stage loads so the maximum voltages across them will still equal V_{ref}. Assuming the capacitive loads of each stage are constant (a good assumption), the delay of each stage will be inversely proportional to I_b. This makes the frequency of oscillation proportional to I_b.

In an interesting modification of the ring oscillator of Fig. 16.17, two multipliers have been added in Fig. 16.21. This modification achieves a doubling in the output frequency while still realizing two quadrature outputs [Buchwald, 92]. Indeed, if quadrature outputs are not required, it is possible to connect the two multiplier outputs to an additional third multiplier. This achieves another doubling of frequency, but there is now only a single output. Another interesting variation of a ring oscillator is described

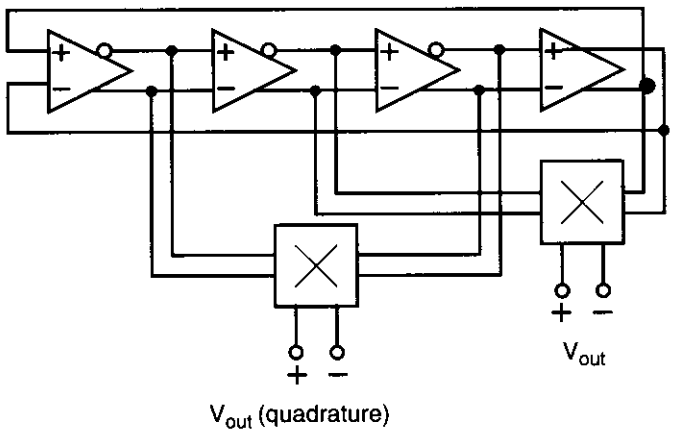


Fig. 16.21 Modifying the ring oscillator of Fig. 16.17 to achieve a doubling of frequency.

in [Razavi, 1994], where the outputs of a three-stage oscillator are combined in a novel manner to obtain a single output with a period equal to only two inverter delays.

CMOS Relaxation Oscillators

Another popular method for realizing digital-output VCOs in CMOS technology is a CMOS relaxation oscillator [Wakayama, 1989; Sun, 1987]. A typical example is shown in Fig. 16.22. In this oscillator, alternatively, C_1 and then C_2 are discharged by the voltage-controlled wide-swing cascode current-mirror consisting of Q_5 to Q_8, R, and the opamp. Due to the negative feedback around the opamp, the current through Q_5 and Q_7 is equal to V_{cntl}/R. Assume the S–R latch is in its reset state as shown in Fig. 16.22 (the S–R latch is simply two cross-coupled NOR gates). This state will cause Q_1 and Q_4 to be on and Q_2 and Q_3 to be off. Since Q_4 is on, the voltage across C_2 is clamped at V_{DD}. However, the voltage across C_1 will change in a negative-going direction because the current from the voltage-to-current converter is flowing through Q_1. This voltage, which started at V_{DD}, reaches the trip point of the comparator (i.e., V_{ref}) after one-half of a clock period. At this time, the output of the comparator goes positive, which causes the S–R latch to become set. This set state causes Q_2 and Q_3 to turn on and Q_1 and Q_4 to turn off. When Q_3 turns on, the voltage across C_1 is very quickly charged back up to V_{DD}. This increased voltage causes the output of the corresponding comparator to go to low (i.e., logic 0), so that both inputs to the S–R latch are again zero. At the same time, since Q_2 turns on, C_2 begins to discharge until its voltage reaches V_{ref}. This completes one period of oscillation. After the voltage across C_2 reaches V_{ref}, the S–R latch is reset, C_2 is quickly charged up to V_{DD}, and C_1 begins to discharge again. The reason for including the comparators, as opposed to connecting C_1 and C_2 directly to the S–R latch, is to make the voltage changes across the capacitors less sensitive to power-supply noise. This is also the major reason for making the current source consisting of Q_5 and Q_7 a cascode current source.

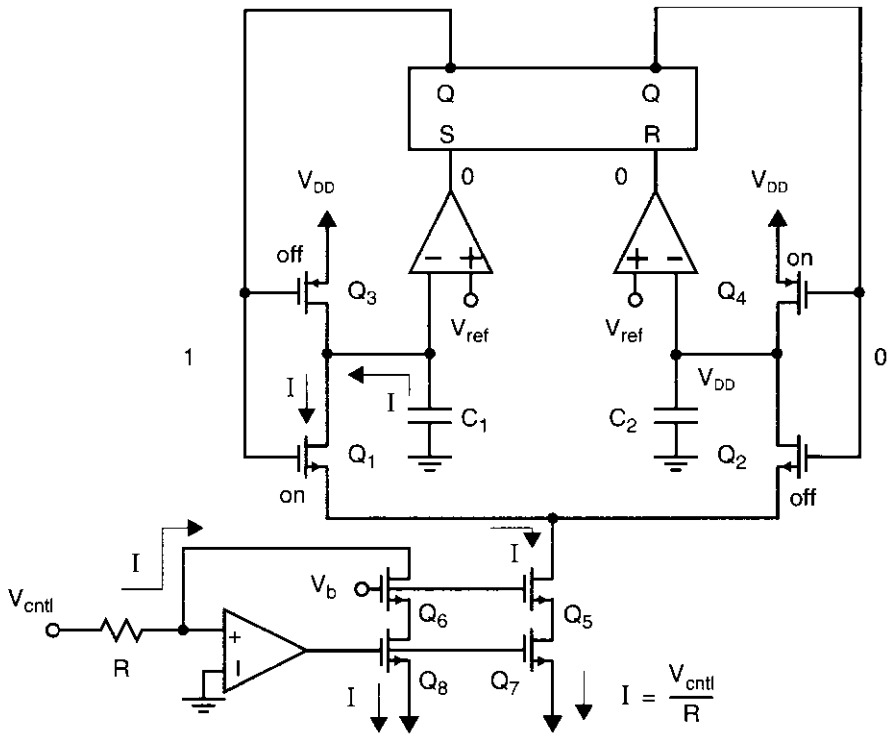


Fig. 16.22 A CMOS relaxation oscillator.

16.4 COMPUTER SIMULATION OF PLLS

Simulating the operation of PLLs is nontrivial because of the very wide range of time constants present in PLLs. Specifically, the voltage-controlled oscillator typically has nodes with important time constants much smaller than the period of its output waveform, whereas the time constants of the low-pass filter are orders of magnitude greater than the VCO's period. If SPICE is used for the simulation, the time steps must be less than the smallest time constant of the VCO, whereas the total simulation time must be greater than the largest time constant of the low-pass filter. This would take an exorbitant amount of time for simulation and is usually impractical. What normally is done is to have SPICE simulate the individual components over a few periods of the VCO's output waveform. The complete system is simulated based on simplified models in which the continuous-time components are replaced by approximately equivalent difference-equation models. This approach can be done by using difference-equation simulators, such as the Simulink program in Matlab [Simulink, 1992] or by writing custom difference-equation simulations using a computer language such as C. The former approach has the advantage that it doesn't require much expertise. The latter approach has the advantages that it runs much faster and can more easily be modified by the designer to include additional second-order effects for greater accuracy. It turns out that writing a difference-equation simulation is not too difficult and that the total amount of code that needs to be written is small.

The approach taken here is generally applicable to the simulation of many other analog systems as well. For example, it is the same approach typically used to simulate oversampling A/D converters. Thus, this section is useful for general analog IC design. However, for designers willing to use a commercial simulator such as Simulink, this section can be safely ignored.

The difference-equation simulation of PLLs will be explained by using a charge-pump PLL as an example. Other types of PLLs can be simulated by making fairly trivial changes to the example, most of them required to describe the operation of different phase detectors.

Describing Continuous-Time Components Using Difference Equations

When doing a simulation, a fixed time step, T, is chosen that might be between one-tenth and one-hundredth of the period of the VCO's output waveform. Ideally, during this fixed time step, all voltage and current changes are small. In the simulation, the voltage–current relationships of all continuous-time elements such as capacitors and resistors are described by approximately equivalent difference equations. In fact, it is not the voltage–current relationships that are usually approximated; rather, it is the voltage–charge relationships. As long as the currents don't change too much during the simulation time step, the current is simply given by the change in charge divided by the time step. The reason for approximating the voltage–charge relationships rather than the voltage–current relationships is that it is often easier to calculate total charge changes during a simulation time step than the average currents. For example, discrete-time analog circuits, such as switched-capacitor circuits, are much easier to analyze using voltage–charge relationships than by using voltage–current relationships. Thus, a single formulation can be used for both continuous-time and discrete-time circuits, and even for simulating systems containing both types of circuits.

To see how to transform the continuous-time voltage–current relationships of a component to the discrete-time simulation domain, consider an arbitrary component having a voltage–current relationship described in the frequency domain by impedance $Z(s)$. Since charge is the integral of current, the relationship between the impedance's charge and current in the frequency domain is given by

$$Q(s) = \frac{I(s)}{s} \tag{16.79}$$

Thus, we can define the voltage–charge transfer function, $M(s)$, as

$$M(s) = \frac{V(s)}{Q(s)} = sZ(s) \tag{16.80}$$

To approximate this relationship in the discrete-time domain, one must replace s with a polynomial of z (the discrete-time variable) in such a way that all relationships are approximately equivalent when $\omega T << 1$ and, therefore, $z = e^{j\omega T} \cong 1 + j\omega T$. One possible means of maintaining this approximation is to use the bilinear

z-transform[5], where every occurrence of s is replaced by the function

$$s \leftarrow \frac{2}{T}\frac{1 - z^{-1}}{1 + z^{-1}} \tag{16.81}$$

For $\omega T << 1$, we have

$$\frac{2}{T}\frac{1 - z^{-1}}{1 + z^{-1}} \cong \frac{2}{T}\frac{1 - (1 - j\omega T)}{1 + (1 - j\omega T)} \cong \frac{2}{T}\frac{j\omega T}{2 - j\omega T} \cong j\omega = s \tag{16.82}$$

as desired. Furthermore, the bilinear transform has the desirable features that stable functions remain stable and that the discrete-time transfer functions are simply frequency-warped versions of the continuous-time transfer functions in which higher frequencies are compressed. The discretization process therefore consists of taking $M(s) = sz(s)$ and replacing each occurrence of s according to (16.82) to obtain $M(z)$, where

$$M(z) = \frac{V(z)}{Q(z)} = sZ(s)\Big|_{s = \frac{2}{T}\frac{1 - z^{-1}}{1 + z^{-1}}} \tag{16.83}$$

During each simulation time step, one normally calculates the charge going into or out of the component. Thus, we are actually interested in the relationship between changes in charge rather than the total charge stored in a component. Noting that the change in charge is equal to the previous charge value subtracted from the present charge, we can write

$$\Delta Q(z) = (1 - z^{-1})Q(z) \tag{16.84}$$

Now, defining the voltage-to-charge-difference transfer function to be $P(z)$, we have

$$P(z) = \frac{V(z)}{\Delta Q(z)} = \frac{M(z)}{1 - z^{-1}} \tag{16.85}$$

The equivalent time-domain difference equation can be found by taking the inverse z-transform of (16.85). This difference equation allows the voltage across the component at time nT to be calculated from previous voltages across the component (i.e., at times $nT - T$, $nT - 2T$, $nT - 3T$, etc.) and the change in charge into the component at time nT (and, possibly, previous times).

When it is easier to calculate the currents than charge changes, the charge going into the component during one period is easily approximated by averaging the current at the beginning of the period with the current at the end of the period and then multiplying by T. Specifically, we can use the time-domain relationship

$$\Delta q(nT) = T\left[\frac{i(nT) + i(nT - T)}{2}\right] \tag{16.86}$$

5. The bilinear z-transform and the discrete z-transform, which is commonly abbreviated as the z-transform, are different.

This approach is general enough to handle mixed continuous-time systems and discrete-time systems such as those composed of switched-capacitor filters and continuous-time components. To make equations simpler, from here on, the variable T will be dropped from the time index. That is, i(nT) will be called i(n) and the difference between sampling times of T will not be given explicitly.

We are now ready to apply this simulation procedure to a charge-pump PLL. The system being simulated is shown in simplified form in Fig. 16.23. We will first derive a difference-equation model for a VCO and then derive the difference-equation model for the loop filter.

Difference-Equation Modelling of a VCO

The difference-equation modelling of the VCO is based on the circuit shown in Fig. 16.24. This model is a simplified model of a relaxation oscillator. It can approximately model most VCOs where the output is a digital signal.

The model operates as follows. First assume $v_{cntl} = V_{th1}$, where V_{th1} is the input voltage to the VCO when its output frequency is equal to its free-running frequency. Up to this point, we have assumed that $V_{th1} = 0$, but we will now be more general to allow for the simulation of PLLs that have only a single power-supply voltage. Since $v_{cntl} = V_{th1}$, the current source $g_{osc}v_1 = g_{osc}(v_{cntl} - V_{th1})$ is zero. Next, assume the capacitor C_{osc} is initially discharged. It will be slowly charged by current source I_{osc}, with the voltage v_2 increasing by an amount given by $\Delta v_2 = \Delta q_{Cosc}/C_{osc} = (I_{osc}T)/C_{osc}$ each analysis time step. Once the voltage across C_{osc} exceeds V_{th2}, then the output of the comparator, which was initially 0 will go high. This causes the output of the one-shot to go high for one analysis period, which has two effects. It first of all causes the output of the toggle flip-flop (which is the output

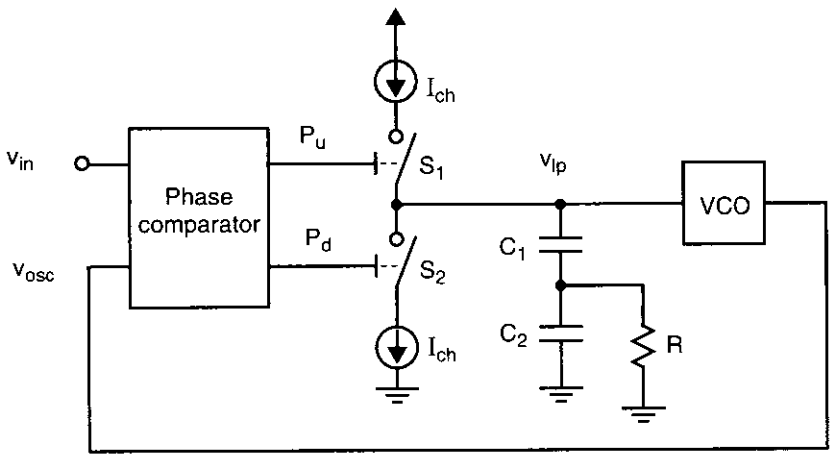


Fig. 16.23 The charge-pump PLL used as an example to illustrate how to simulate PLLs.

of the VCO, that is, v_{osc}) to change its state. It also causes the switch S_{vco} to come on. This quickly discharges C_{osc} to zero, which in turn causes the output of the comparator to go back to 0. This process repeats itself every half-period, $T_{osc}/2$. The number of analysis time steps, n, required for C_{osc} to charge from 0 to V_{th2} is given by

$$n = \frac{V_{th2} C_{osc}}{I_{osc} T} \tag{16.87}$$

Since

$$\frac{T_{osc}}{2} = nT \tag{16.88}$$

we have, after substituting (16.87) into (16.88),

$$T_{osc} = \frac{2V_{th2} C_{osc}}{I_{osc}} \tag{16.89}$$

and, therefore, the free-running frequency of the VCO, f_{fr}, is given by

$$f_{fr} = \frac{1}{T_{osc}} = \frac{I_{osc}}{2V_{th2} C_{osc}} \tag{16.90}$$

Next, consider a case when the control voltage to the VCO is not equal to the bias voltage V_{th1}. When v_{cntl} is a nonvarying value, the oscillation frequency is given by

$$f_{osc} = \frac{I_{osc} + g_{osc}(v_{cntl} - V_{th1})}{2V_{th2} C_{osc}} \tag{16.91}$$

By taking first-order derivatives of both sides of (16.91), we have

$$K_{osc} = 2\pi \frac{df_{osc}}{dv_{cntl}} = \frac{2\pi g_{osc}}{2V_{th2} C_{osc}} \tag{16.92}$$

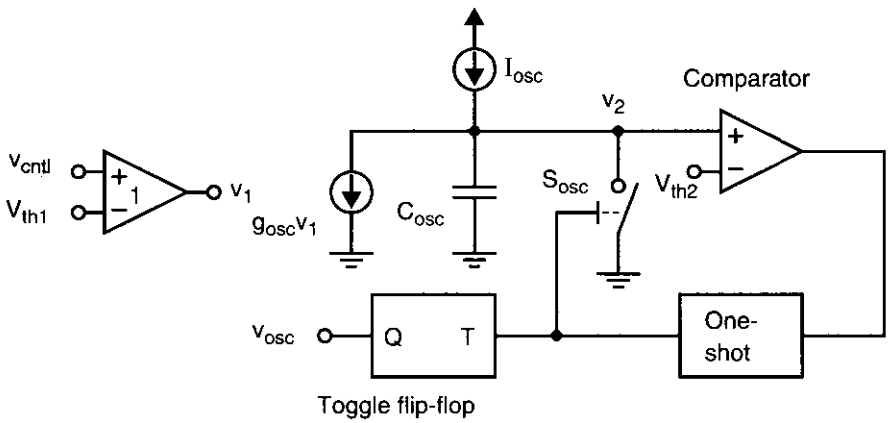


Fig. 16.24 The model used for the VCO.

The difference equations describing the system will be derived for the case where v_{cntl} can change with time using the difference-equation modelling presented above. Although this VCO is such a simple system that this formalism is unnecessary, the formal approach will still be used so that a simple example can be presented.

The capacitor, C_{osc}, has an impedance given by

$$z(s) = \frac{1}{sC_{osc}} \tag{16.93}$$

Using (16.80), we have

$$M(s) = sz(s) = \frac{1}{C_{osc}} \tag{16.94}$$

Since this is not a function of s but a constant, transforming it to the discrete-time domain is trivial. We have

$$M(z) = \frac{1}{C_{osc}} \tag{16.95}$$

Next, using (16.85), we have

$$P(z) = \frac{V_2(z)}{\Delta Q_{Cosc}(z)} = \frac{1/C_{osc}}{1 - z^{-1}} \tag{16.96}$$

which implies

$$V_2(z)(1 - z^{-1}) = \frac{\Delta Q_{Cosc}(z)}{C_{osc}} \tag{16.97}$$

Taking the inverse z-transform, we have

$$v_2(n) = v_2(n-1) + \frac{\Delta q_{Cosc}(n)}{C_{osc}} \tag{16.98}$$

Now, since

$$\Delta q_{Cosc}(n) = TI_{Cosc\text{-}avg} \tag{16.99}$$

and since

$$I_{Cosc\text{-}avg} = I_{osc} + g_{osc}\left[\frac{v_{cntl}(n) + v_{cntl}(n-1)}{2} - V_{th1}\right] \tag{16.100}$$

we have, using (16.98),

$$v_2(n) = v_2(n-1) + \frac{T}{C_{osc}}\left(I_{osc} + g_{osc}\left[\frac{v_1(n) + v_1(n-1)}{2} - V_{th1}\right]\right) \tag{16.101}$$

This is the basic difference equation that will be calculated once each analysis time step. After each updating of $v_2(n)$, its value is then compared with V_{th2}, and if it is larger than 0, then $v_2(n)$ is reset to zero and the logic value of v_{osc} is changed. The system can be initialized at time zero by setting $v_{cntl}(0) = V_{th1}$ and $v_2(0) = 0$.

Any nonlinearities between the VCO's control voltage and its frequency can be added to the model by making g_{osc} a function of v_1. This nonlinear modelling is most easily done by using a table lookup, whose entries are obtained from doing a number of simulations of the complete VCO at the transistor level using SPICE.

Difference-Equation Simulation of a Loop Filter

The loop-filter simulation is somewhat more complicated. Part of this complication comes from a need to maintain high numerical accuracy. The impedance of the loop filter is given by

$$Z_{lp}(s) = \frac{1}{sC_1} + \frac{1}{sC_2 + G} \tag{16.102}$$

where $G = 1/R$. Using (16.80), we have

$$\frac{V_{lp}(s)}{Q_{lp}(s)} = \frac{G + s(C_1 + C_2)}{GC_1 + sC_1C_2} \tag{16.103}$$

Next, each term of s is replaced using the bilinear z-transform according to (16.81). After this transform, we have

$$M(z) = \frac{V_{lp}(z)}{Q_{lp}(z)} = \frac{2(1 - z^{-1})(C_1 + C_2) + GT(1 + z^{-1})}{2C_1C_2(1 - z^{-1}) + C_1GT(1 + z^{-1})} \tag{16.104}$$

Using (16.85) and rearranging gives

$$P(z) = \frac{M(z)}{1 - z^{-1}} = \frac{GT + 2(C_1 + C_2) + z^{-1}[GT - 2(C_1 + C_2)]}{2C_1C_2 + GC_1T - z^{-1}4C_1C_2 + z^{-2}(2C_1C_2 - GC_1T)} \tag{16.105}$$

which can be rewritten as

$$\begin{aligned} P(z) = \frac{V_{lp}(z)}{\Delta Q_{lp}(z)} &= \frac{m_1 + m_2z^{-1}}{1 + z^{-1}(k - 2) + z^{-2}(1 - k)} \\ &= \left(\frac{1}{1 - z^{-1}}\right)\left(\frac{m_1 + m_2z^{-1}}{1 - z^{-1} + kz^{-1}}\right) \end{aligned} \tag{16.106}$$

where

$$k = \frac{2GC_1T}{D} \tag{16.107}$$

$$m_1 = \frac{2(C_1 + C_2) + GT}{D} \tag{16.108}$$

$$m_2 = \frac{-2(C_1 + C_2) + GT}{D} \tag{16.109}$$

and

$$D = 2C_1C_2 + GC_1T \tag{16.110}$$

This transfer function can be simulated by a discrete-time system that has the signal-flow graph shown in Fig. 16.25. This network is a "lossless-digital-integrator" (LDI) [Kingsbury, 1973] realization of the transfer function (16.106). This type of realization has very good numerical properties when the poles of the low-pass filter being simulated are at frequencies much less than the inverse of the analysis time step (which is certainly the case when simulating PLLs). A direct-form implementation would have quite poor numerical properties in this situation.

It is now possible to give the difference-equation updates for the low-pass filter, which are performed once each analysis time step based on the signal-flow graph of Fig. 16.25. Each simulation time step, do the following:

1. If P_u is 1, then take $\Delta q_{lp}(n) = TI_{ch}$. Or if P_d is 1, then take $\Delta q_{lp}(n) = -TI_{ch}$. Otherwise, take $\Delta q_{lp}(n) = 0$.
2. Update the difference equations for simulating the low-pass filter according to the following:

$$x_1(n) = \Delta q_{lp}(n) + x_1(n-1) \tag{16.111}$$

$$x_2(n) = x_1(n) + x_2(n-1) - kx_2(n-1) \tag{16.112}$$

$$v_{lp}(n) = m_1x_2(n) + m_2x_2(n-1) \tag{16.113}$$

Notice that (16.113) is a function of $x_2(n-1)$. This means that if a single variable is used to store x_2, its value must be temporarily stored, since x_2 is updated in (16.112) before (16.113).

There is one other complication. If it is desired at initialization that the low-pass filter have an initial output other than zero, as would be needed in simulations of PLLs realized using a single power-supply voltage, then the internal state variables of the difference-equation simulation should be initialized according to the following equations:

$$x_2(0) = \frac{v_{lp}(0)}{m_1 + m_2} \tag{16.114}$$

$$x_1(0) = kx_2(0) \tag{16.115}$$

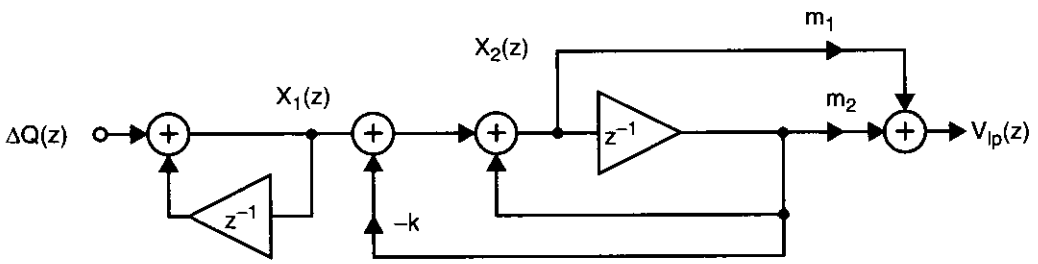


Fig. 16.25 The signal-flow graph of the difference equations used to simulate the PLL's low-pass filter.

Phase/Frequency Comparator Simulation

The phase/frequency comparator was described previously. Based on this description, the following formal definition specifies how its state variables, P_u, P_d, $P_{u\text{-}dsbl}$, and $P_{d\text{-}dsbl}$ should be updated each analysis time-step.

1. If V_{in} is 1 and $P_{u\text{-}dsbl}$ is 0, then set P_u to 1.
2. If V_{osc} is 1 and $P_{d\text{-}dsbl}$ is 0, then set P_d to 1.
3. If V_{in} and V_{osc} are both 1 and $P_{u\text{-}dsbl}$ and $P_{d\text{-}dsbl}$ are both 0, then set reset to 1; otherwise set it to 0.
4. If reset is 1, then set $P_{u\text{-}dsbl}$ and $P_{d\text{-}dsbl}$ to 1 and set P_u, P_d, and reset to 0.
5. If V_{in} and P_u are both 0, then set $P_{u\text{-}dsbl}$ to 0.
6. If V_{osc} and P_d are both 0, then set $P_{d\text{-}dsbl}$ to 0.

Complete Simulation

The simulation of the complete PLL is now accomplished by updating the difference equations for each block once each analysis time step. A C-program realization of this simulation is given in the appendix of this chapter. It should be relatively easy to modify this simulation so that it can also be used to simulate other PLLs as well.

EXAMPLE 16.5

Let $I_{ch} = 10\ \mu A$, $I_{osc} = 0.5$ mA, $V_{th1} = V_{th2} = 2.5$ V, and $f_{fr} = 50$ MHz. Also, assume that $K_{osc} = 2\pi \cdot 25\ \text{MHz} \cdot \text{V}^{-1} = 1.57 \times 10^8\ \text{rad} \cdot \text{V}^{-1}$.

Solution

First, using (16.90), we have

$$C_{osc} = \frac{I_{osc}}{2f_{fr}V_{th2}} = 2\ \text{pF} \tag{16.116}$$

Next, using (16.92), we have

$$g_{osc} = \frac{2V_{th2}C_{osc}K_{osc}}{2\pi} = 0.25\ \text{ms} \tag{16.117}$$

The values of the components of the low-pass filter were already found in Example 16.5. They are $C_1 = 25.3$ pF, $C_2 = 2.5$ pF, and $R = 31.4\ \text{k}\Omega$. These are the values used in the C-code simulation of this PLL given in the appendix of this chapter. The simulation was started with the VCO having a frequency of zero. It took 28.6 μs to obtain lock. Next, after 5 μs, the phase of the input signal was given a step change of 180°. It took the PLL 0.8 μs to settle to this new phase. In both cases, the transient responses were well behaved.

16.5 APPENDIX

The source code for a C-program simulation of a charge-pump PLL having a phase/frequency converter follows. Readers who wish to obtain this source code using ftp via internet should send e-mail to martin@eecg.toronto.edu for instructions.

```
/*  This is a difference-equation simulation of a charge pump PLL having a
    phase/frequency comparator. v1n is the output of the low-pass filter, which is
the input to the VCO.

    v2n is the internal voltage of the VCO across its capacitor. x1n and x2n are
the internal state variables of the low-pass filter simulation. pu, pd, pu_d, and
pd_d are the internal state variables of the charge pump. delt_q is the charge
change of the low-pass filter. The simulation is for 500,000 analysis time steps,
and then has a step change in phase of the input voltage. Currently the input fre-
quency is 50 MHz.
*/


#define IN_FREQ = 50e6 // The input frequency is 50 MHz
#define PI 3.141592654
#define VTH1 2.5 // the VCO input voltage to obtain the free-running frequency
#define VTH2 2.5 // the trip-point for the VCO relaxation oscillator
#define ICH 1e-5 // the charge-pump current is 10 μA
#define IOSC 5e-4 // the dc current in the VCO is 0.5 mA
#define GOSC 2.5e-4 // the transconductance of the VCO
#define C1 25e-12 // the large capacitor in the loop filter
#define C2 2.5e-12 // the deglitching capacitor in the loop filter
#define C3 2e-12 // the capacitor used in the VCO simulation
#define G 3.18e-5 // the transconductance of the loop filter, R=31.4 k
#define T 1e-11 // An analysis step is 10 ps
#define NSTEPS 1e7 // Analyze for 1 msec (i.e., 10 million steps)

#include <stdio.h>
#include <math.h>
main()
    {
    double D,k,m1,m2,v1n,v1n_1,v2n,v2n_1,x1n,x1n_1,x2n,x2n_1,delt_-
q,i_avg;
    double in_freq,in_per,half_per,time,per_tim,osc_freq;
    int i,j,inp_val,osc_val,pu,pu_d,pd,pd_d,rst;
```

```
// Initialize all variables

D = 2*C1*C2 + C1*G*T;
k = 2*C1*G*T/D;
m1 = (2*(C1+C2) + G*T)/D;
m2 = (-2*(C1+C2) + G*T)/D;
v1n = v1n_1 = VTH1 - 2.4; // The VCO is initialized less than 50 MHz
v2n = v2n_1 = 0.0;
x2n = x2n_1 = v1n/(m1+m2);
x1n = x1n_1 = k*x2n;

inp_val = osc_val = 0;
pu = pu_d = pd = pd_d = rst = 0;
in_freq = 50e6;
in_per = 1/in_freq;
half_per = in_per/2.0;
j = 0;

// Start the simulation

for (i=0; i < NSTEPS; i++)
{
time = T * (double) (i);

// The first set of statements is to produce the input square wave

per_tim = time - in_per*(double)j;
if (per_tim >= half_per) // change value of input signal
{
inp_val = (inp_val == 0)? 1:0;
j++;
if (j%4 == 0)
{
osc_freq = i_avg/(2.0*C3*VTH2);

// Print out the oscillator frequency once every four input periods
```

```
        printf("time: %.1lf, period: %.2lf, v1n: %.4lf, in_freq: %.2lf, osc_freq:
%.2lf\n",time * 1e9, (time/in_per), v1n, in_freq * 1e-6, osc_freq * 1e-6);
      }
    }

//  Have a 180-degree phase shift at analysis step 500000, or after 5 µs,

      if(i == 500000)
    {
    inp_val = (inp_val == 0)? 1:0;
    }

//  The next few statements simulate the phase/frequency comparator

      if (inp_val==1 && pu_d==0 && rst==0) pu=1;
      if (osc_val==1 && pd_d==0 && rst==0) pd=1;
      rst = (inp_val==1 && osc_val==1 && pu_d==0 && pd_d==0)? 1:0;
      if (rst==1) {pu=0; pd=0; pu_d=1; pd_d=1; rst=0;}
      if (inp_val==0 && pu==0) pu_d=0;
      if (osc_val==0 && pd==0) pd_d=0;

//  Now we simulate the charge pump and low-pass filter

      if (pu==1) delt_q = ICH*T;
      else if (pd==1) delt_q = -ICH*T;
      else delt_q = 0.0;

      x1n = delt_q + x1n_1;
      x2n = x1n + x2n_1 - k*x2n_1;
      v1n = m1*x2n + m2*x2n_1;

//  Now we simulate the VCO

      i_avg = IOSC + GOSC*((v1n + v1n_1)/2.0 - VTH1);
      v2n = v2n_1 + i_avg*T/C3;
      if (v2n >= VTH2)
    {
    v2n = v2n_1 = 0.0;
```

```
        osc_val = (osc_val == 0)? 1:0;
        }

    //  Update the state variables for the next iteration

        x1n_1 = x1n;
        x2n_1 = x2n;
        v1n_1 = v1n;
        v2n_1 = v2n;

        i++;
      }
    }
```

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16.7 PROBLEMS

16.1 A CMOS exclusive-OR gate is being used as phase-detector in a PLL. The power-supply voltages are 0 V and 5 V. The low-pass filter is composed of discrete components. The VCO has a 10 MHz free-running frequency for when $V_{cntl} = 2.5$ V, and it has $K_{osc} = 5$ MHz/V. Assume we want the time-constant of the loop to be 50 μs. Design the low-pass filter for $Q = 0.5$. Accurately sketch the voltage waveforms of all nodes in the loop for when the loop is in lock and the input frequency is 7 MHz, both with and without the deglitching capacitor, C_2, of the low-pass filter. Label the maximum and minimum voltages of each node voltage in your sketch. What is the phase difference between the input signal and the oscillator's output signal? What is the lock range of the loop, assuming the VCO is linear for $1V < V_{cntl} < 4$ V?

16.2 A PLL has an amplifier with a gain of A following its low-pass filter, as shown in Fig. P16.2. The conversion factor of the phase detector is 3 V/rad and the conversion factor of the VCO is 50 KHz/V. The phase detector is a multiplier. The design for the low-pass filter and the amplifier gain are to be chosen. The PLL is intended to be used to demodulate a 5-KHz signal that

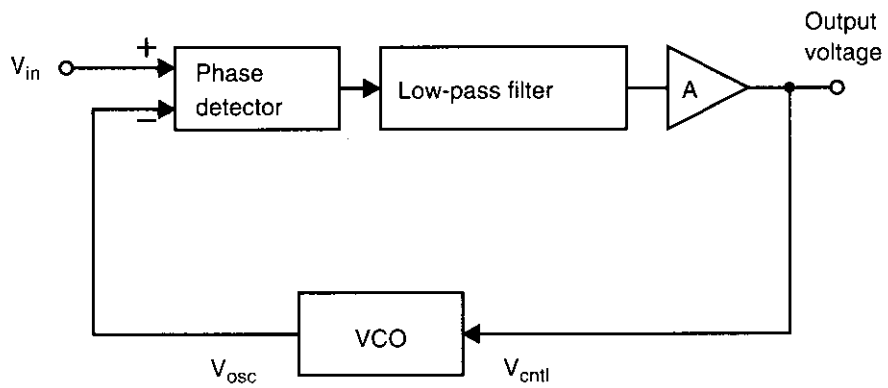


Fig. P16.2 A PLL in which an amplifier has been added after the low-pass filter.

has been frequency modulated on a 5-MHz carrier having a ±50-KHz deviation. Design the filter so that the magnitude of the transfer function of the small-signal model of the loop is maximally flat. The –3-dB frequency should be the same as the band width of the signal that has been modulated. The lock range should be chosen so that the VCO's frequency never exceeds one-half the maximum possible range. Explain what happens to the lock range if the amplifier gain is increased?

16.3 A PLL with a multiplier phase detector has been designed so its linearized small-signal transfer function has a Q factor of 1/2 and a resonant frequency of one-hundredth the free-running frequency of the VCO, when the VCO is at its free-running frequency. What are the resonant frequency and Q factor when the VCO's frequency is different from its free-running frequency by one-half the lock range?

16.4 The low-pass filter designed in Example 16.4 has V_{in} leading V_{osc} by $\pi/8$. Accurately sketch the voltage waveforms of P_u, P_d, and V_{lp} both with and without the deglitching capacitor, C_2. Label the values of the voltages at each major transition point. (*Hint:* The general equation that describes the transient relaxation of a first-order circuit may be useful).

16.5 Let $K_{osc} = 2\pi \cdot 25\ \text{MHz} \cdot \text{V}^{-1}$ and $I_{ch} = 10\ \mu\text{A}$ in a charge-pump PLL. Assume the time free-running frequency of the oscillator is 100 MHz and that we want the loop to have a time constant of 50 cycles, or 0.5 μs. Design the components of the low-pass filter. The filter should include the second deglitching capacitor, C_2.

16.6 Sketch the waveforms of V_{in}, V_{osc}, P_u, P_d, $P_{u\text{-}dsbl}$, and $P_{d\text{-}dsbl}$ of the phase/frequency comparator for the case when V_{in} has a much smaller frequency than V_{osc}.

16.7 Find reasonable values for all current sources, the resistors, and C_{osc} of the emitter-coupled multivibrator in Fig. 16.12 so that the multivibrator has a free-running frequency of 10 MHz. Assuming that the on voltage of a diode changes by –2 mV for every °C increase in temperature, estimate the change in frequency if the temperature increases by 20 °C.

16.8 Assume a ring oscillator is realized by five CMOS inverters that have a threshold voltage equal to $V_{DD}/2$. What would the change in frequency be if the power-supply voltage changes from 5 V to 5.5 V? If this happens right at the beginning of a period, what would the corresponding time jitter of output waveform be at the end of the period?

16.9 Derive an equation for the frequency of operation of a ring oscillator that has delay stages of the type shown in Fig. 16.20. Assume the capacitive load of each output is constant and equal to C_L. Also, assume that, when an inverter is switching, its bias current, I_b, changes very quickly from one side to the other.

16.10 Shown in Fig. P16.10 is the bias circuitry and one stage of a four-stage ring oscillator. Assume the loading at each output of the differential inverter is

0.1 pF. Assume transistors are all in the active region. Given that $V_{cntl} = 1$ V, $V_{ref} = 1$ V, and $R = 100$ kΩ, derive and give a value for the frequency of oscillation and for the oscillator's gain constant (in radians/volt).

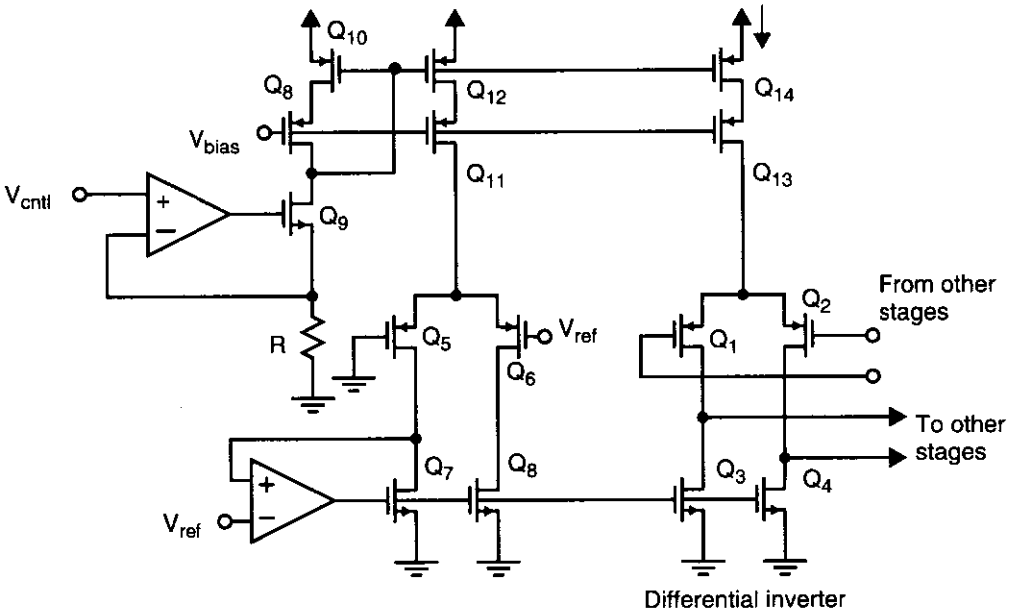


Fig. P16.10

16.11 Derive an equation for the frequency of operation of the CMOS relaxation oscillator shown in Fig. 16.22.

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