IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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CISCO SYSTEMS, INC.,
PALO ALTO NETWORKS, INC., and
FORTINET, INC.
Petitioner,

v.

LIONRA TECHNOLOGIES LIMITED
Patent Owner.

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*Inter Partes* Review No.: IPR2023-00703[1]
U.S. Patent No. 8,566,612

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**PETITIONER'S OPPOSITION TO PATENT OWNER'S MOTION TO STRIKE PORTIONS OF PETITIONER'S REPLY BRIEF**

***Mail Stop "PATENT BOARD"***
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

[1] The Board joined Palo Alto Networks, Inc. and Fortinet, Inc. as a party (Petitioner) to this proceeding via a Motion for Joinder in IPR2024-00158.

## I. INTRODUCTION

The Patent Owner's Motion to Strike (MTS) asserts that the Petitioner's Reply is improper in two respects. First, the MTS asserts that the Petitioner's Reply directed to FIG. 2 of Pham at pages 4-5 is improper because it is directed "to an embodiment in Pham that was **not** addressed in the Petition or the POR." MTS 4 (emphasis in original). Second, the MTS asserts that the Petitioner's Reply directed to Grounds 3 and 4 is improper because it is directed to including an intrusion detection system on a single chip, which Patent Owner asserts is a "new theory of obviousness." MTS 7. The MTS, like the Patent Owner's Response (POR) is without factual or legal support.

With respect to FIG 2, contrary to the MTS, **both** the Petition and the POR address the embodiment shown in FIG. 2. Thus, it is entirely proper for the Petitioner's Reply to address FIG. 2 on two independent bases---(1) to assist in crystalizing the Petition's discussion of the embodiment of FIG. 2 without changing the obvious rationale of Ground 1, and (2) to respond to the POR's discussion of the embodiment of FIG. 2. See 37 C.F.R. § 42.23; Consolidated Trial Practice Guide, November 2019, pp. 73-74.

With respect to Grounds 3 and 4, the MTS seeks to strike Petitioner's citation to the Petition (pages 64-66) directed to Krishna's disclosure of forming

discrete components of the security processor on a single chip including database lookups as described in the State of the Art Section. On its face, Petitioner's Reply is based on arguments previously made in the Petition, and thus, is clearly proper to assist in crystalizing the Petition's discussion of the motivation to form discrete components of the security processor on a single chip. In addition, Petitioner's argument is directly in response to the POR's discussion regarding how an IDS could be formed on a single chip. Thus, Petitioner's arguments with respect to Grounds 3 and 4 are entirely proper in a reply.

## II. Petitioner's Reply Appropriately Cites to the Embodiment of FIG 2 of Pham

### A. The Embodiment Of FIG. 2 Was Discussed In The Petition

In the Petition, for Ground 1, several embodiments of Pham were used to demonstrate the unpatentability of the claims. For example, the Petition states the network processors 112 (as shown in FIG. 4) process substantially all of the data packets received and transmitted by the VPN gateway (as shown in FIG. 6), including both clear text and encrypted packets:

> Pham discloses that the network processors 112 process substantial all the data packet received and transmitted by the VPN Gateway. For example, in one embodiment, Pham discloses that ingress processor 80 (Fig. 5) and network processor 112 in crypto processor 86 (Fig. 6) use the identical conventional processors and identical routing and SA tables to allow functions of the ingress processor to be offloaded to network processor 112, such as packet routing, SA parameter association and compression and decompression. EX-4 Figures 5, 6 [0049], [0051], [0053]. Thus, all packets, both clear text and encrypted can be sent to network processor 112 for routing using routing and SA table 118. EX-1003 ¶ 89.

Pet. 41.

Further, the Petition cites to the embodiment of FIG. 2 of Pham regarding the processing of both clear text and encrypted packets, specifically citing to LAN

38, Internet 18, ingress processors 30 and 34, egress processors 32 and 36, switch fabric 40, and data packet processors 42 and 44 (all as shown in FIG. 2):

> Pham further discloses passing encrypted data packets and clear text data packets to the encryption/decryption engine.
>
> > For the preferred IPsec processing embodiments of the present invention, clear text data packets forwarded from the LAN 38 through the VPN gateway 12 subject to the VPN encryption protection are routed by the ingress processor 30 through the switch fabric 40 to an available encryption data packet processor 42. The encrypted data packet is then returned through the Switch fabric 40 to the egress processor 32 and passed onto the Internet 18. Conversely, encrypted data packets received from the Internet 18 are routed by the ingress processor 34 through the switch fabric 40 to a decryption data packet processor 44. The resulting clear text data packet is then passed to the egress processor 36 for transferred onto the LAN 38. EX-1004 [0041]; EX-1003 ¶ 128.

Pet. 55-56.

Thus, the Petition expressly relies on the embodiment of FIG. 2 for the unpatentability of the Challenged Claims for Ground 1. This is not surprising as Pham describes data processor 42 is an encryption data packet processor, and data processor 44 is a decryption data packet processor, which means that data processors 42 and 44 of FIG. 2 are the crypto

processors 86 identified in FIG. 4, which demonstrates that the architecture of FIG. 2 is identical to the architecture of FIG. 4.

In the MTS, Patent Owner argues that "the Reply relies on a different element of Pham as an alleged packet engine and presents a new theory of unpatentability" because "Figure 2 does not even include crypto processors 86 or network processor 112 from Figures 4 and 6." MTS 5. This argument ignores the express teaching discussed above, that data processors 42 and 44 of FIG. 2 are crypto processors, and that data processors 42 and 44 each include a data engine, e.g., network processor. EX-1004 Abstract ("The data packet processors **each include a data processing engine** configured to perform a data processing function...")(emphasis added). Thus, the citation to FIG. 2 in the Petitioner's Reply was totally appropriate and did not raise a new theory of unpatentability.

### B. The Embodiment Of FIG. 2 Was Discussed In The POR

The POR asserted that in some embodiments disclosed in Pham, substantially all of the incoming and outgoing packets to the security processor do not transit one of the plurality of packet engines. POR 9-11, 13-14, 22-23, 26-28. In support, the POR repeatedly relies on the embodiment of FIG. 2, which is described at paragraphs [0038]-[0041] of Pham:

The POR at pages 9-11 cites to paragraphs [0038]-[0041].

The POR at page 13 cites to paragraph [0038].

The POR at page 22 cites to paragraphs [0038]-[0040].

The POR at page 26 cites to paragraph [0038].

Specifically, the POR relies on the embodiment of FIG. 2 in support of its main argument that in one embodiment, the "unencrypted packets do not require processing through data packet processors and are instead 'bypassed between the ingress and the egress processors.'" POR 10 (citing to EX-1004 [0038]-[0040]). The Petitioner's Reply responds to the POR arguments by showing that the embodiment of FIG. 2 does in fact show that substantially all of the incoming and outgoing packets to the security processor transit one of the plurality of packet engines. Pet. Rep. 4-5. Thus, the Petitioner's Reply citation to the embodiment of FIG 2 is in direct response to the POR and is appropriate and proper under 37 C.F.R. § 42.23.

## III. Petitioner's Reply Appropriately Cites to the Arguments Previously Made in the Petition for Grounds 3 and 4

### A. The Petition Describes Forming Discrete Security Processors On A Single Chip

The Petition includes a State of the Art Section that describes that by the priority date of the 612 Patent, a POSA understood that cryptographic processing was moving away from discrete processors and was being

implemented on a single chip, and identified an illustration of a chip having discrete security processors such as a packet engine and a cryptographic engine. Pet. 16 (citing EX-1010 Fig. 1, Abstract; EX-1003 ¶ 54). The packet engine included a packet classifier unit and a packet distributor. The classification engine performs lookups from databases stored in associated memory. Pet. 15 (citing EX-1006 5:37-53; EX-1003 ¶ 53).

In the Petition, Ground 3 includes Claim 4 which depends from independent Claim 1 and recites *wherein the packet engine, the cryptographic core, and the modulo engine are formed on a single chip*. The Petition identifies that this limitation is disclosed by the teachings of Krishna of forming discrete components of the security processor on a single chip as discussed in the State of the Art section. Pet. 64-66 (citing EX-1006 and EX-1010.)

In the Petition, Ground 4 includes Claim 17 which depends from independent Claim 13 and recites *wherein the security processor is formed on a single chip*. The Petition identifies that this limitation is disclosed by Krishna's teaching of "forming a security processor including a switching system, a packet engine and a cryptographic core **as well as other functions** on a single chip" and that it "would have been obvious to combine the

teachings of Krishna with the system of Pham in view of Wu for the same reasons discussed above with respect to Claim 4." Pet. 67 (emphasis added).

### B. The Petitioner's Reply Refers Back to Previous Arguments Made in the Petition and Does Not Raise a New Theory of Unpatentability

The POR treats Claim 4 and 17 as the same, and criticizes the Petition's analysis for "omitting a discussion of how [the IDS system limitation] could or would be satisfied if the packet engine, cryptographic core and modulo engine are formed on a single chip."[2] POR 33. The Petitioner's Reply responds by expressly referencing back to the arguments made in the Petition in the State of the Art section and the analysis of Claim 4 which identifies that Krishna's teachings apply equally to other security functions and are not just limited to the three discrete processors recited in Claim 4. Pet. Rep. 13-14. This is the identical theory that is set forth in the Petition, e.g., Krishna's teaching of "forming a security processor including a switching system, a packet engine and a cryptographic core **as well as other functions** on a single chip." Pet 67 (emphasis added).

[2] Claim 4 does not require that the IDS be formed on a single chip, only the packet engine, cryptographic core and modulo engine.

Thus, the Petitioner's Reply citation to arguments previously made in the Petition is to assist in crystalizing the Petition's discussion of the motivation to form discrete components of the security processor on a single chip, and in direct response to the POR and, thus is appropriate and proper under 37 C.F.R. § 42.23.

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## CERTIFICATION OF SERVICE ON PATENT OWNER

Pursuant to 37 C.F.R. §§ 42.6(e), the undersigned certifies that on May 13, 2024, a complete and entire copy of Petitioner's Opposition to Patent Owner's Motion to Strike, was served by electronic mail to the Patent Owner's counsel at the following addresses:

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