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(54) Title: METHOD AND COMMUNICATION SYSTEM FOR THE BIT-SERIAL EXCHANGE OF DATA (57) Abstract Method and communication system for serially exchanging data bits with one or more input (I) and/or output (O) modules (10), under the control of at least one master station (1). The I/O modules (10) are connected in cascade to a control module (9) via a local data bus (19) for serial bit transfer. The I/O modules (10) are provided with control means (35) for recording data bits at the input side (34) and/or presenting data bits at the output side (33). A control module (9) comprises means (16) coupled to the control means (35) for controlling in a synchronised manner the connected I/O modules (10) in response to control information received from the master (1). The I/O modules (10) can be connected in groups to the at least one master (1) via one or more substations (slaves) (2, 3, 4, 5) and a transmission system (7, 8) for serial bit transfer. The present method and communication system provide unambiguously in the communication of cause-and-effect relationships at I/O level, in particular, for measurement and control applications, monitoring purposes and data acquisition.			

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Method and communication system for the bit-serial exchange of data.

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The invention relates to a method and a communication system for exchanging data in discrete or digital form with one or more input (I) and/or output (O) modules, by means of serial transfer of data bits. under the control of at least one master station (master).

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Communication systems of this type are in practice known per se. Examples are the so-called "Local Area Networks" (LAN's) in, inter alia, office, factory, hospital and production environments. The physical transmission medium is usually coaxial or optical fibre cable.

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The information is primarily transferred in digital form and can vary from text and speech data to control and measurement data. For long-distance connections, public networks equipped with cables or radio links are, inter alia, available. LAN communication systems are, in principle, designed for communicatively coupling two or more connected stations together as required, whereas public networks primarily have the task of providing point-to-point connections between two stations.

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LAN topologies generally used in practice are star, bus, ring and tree configurations in which the data bits are transferred serially to the connected stations. Generally in packet form, that is to say a particular station cannot transmit uninterrupted information but only packets containing a measured information content. A large variety of protocols, such as CSMA/CD "token passing", Aloha etc., have been developed for controlling the communication. For further details, reference is made to the special issue entitled "Architectures of Local Area Networks (LAN's)" in IEEE Communication Magazine, vol. 22, no. 8, August 1984.

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Unambiguousness in the communication of cause-and-effect relationships is an important requirement, especially for measurement and control applications, monitoring purposes and data acquisition. That is to say, the reaction (the effect) to an

instruction (cause) must be transferred unambiguously as being related to said instruction. However, depending on a specific application, input and/or output variables of a system may change relatively rapidly.

5 Communication systems constructed in accordance with the LAN concept generally have the disadvantage that, for use in, for example, industrial measurement and control environments having a large number of I/O points (for example 1,000 or over), they are too slow to be able to fulfil the required cause-and-effect
10 unambiguousness, owing, among other things, to the communication protocols needed. Because the information is transferred bit-serially via the network but, on the other hand, is generally processed in parallel by the stations connected via bus networks, such as the known VME bus and SCSI bus, used for coupling
15 microcomputer systems and peripheral equipment, a further delay can arise as a consequence of the required parallel-to-serial (P/S) and serial-to-parallel (S/P) conversion, which may be understood as follows.

 Suppose that a plurality of I/O modules are connected to a
20 station via a local data bus for parallel-bit transfer, each I/O module receiving information in the form of x parallel data bits. Whenever x data bits are received serially by a station, a conversion beat from serial to parallel presentation has to be carried out for transfer to the I/O modules. After the converted
25 data bits have been transmitted to the relevant I/O module, data bits for a further I/O module can be converted, etc. In the case of a number of y I/O modules, the last one receives its information only with a delay after y conversion beats because, as is known, a certain time is necessary for each conversion beat. These time
30 delays may, for example, be reduced by employing a plurality of S/P converters and/or a plurality of local buses with associated interface. This latter results, however, in a structure which is unfavourable both in terms of cost and of installation.

 The bus networks, such as the said VME bus or SCSI bus, which
35 are used in practice to couple microcomputer systems and peripheral equipment together and via which the data bits are transferred in parallel in groups, rapidly become relatively expensive as the distance to be spanned increases as a consequence of the increase

in the cost of the transfer medium needed for parallel transmission of data bits, that is to say, bandwidth and/or physical medium. In order to limit said costs, serial transmission should always be used to span relatively great distances. Other bus networks used in practice are, inter alia, Multibus^R and Q-bus^R.

British Patent Application 2,080,000 discloses a communication system for exchanging, with the aid of a central control unit, data bits originating from a number of input modules connected in cascade. The data are transferred bit-serially. The system operates in a manner such that, on receiving data bits from an adjacent module, a module adds its information presented at that instant at the input to the data bits to be transmitted, etc.. In this manner a packet of data bits is produced which is transferred to the central control unit.

Apart from the lack of a facility for exchanging data bits from the central control unit to the connected modules, this manner of exchanging data has the disadvantage that the sampling point of time of a module depends on its position in the cascade. Such a system is, for example, unsuitable for measurement and control applications.

Suppose that the modules are designed to transfer the values of a number of measured variables to the central control unit. Because there is a certain time period between the sampling of, for example, the last and the first module in the cascade as a consequence of the sequential sampling, there is no guarantee that a change in the measured variable of the relevant modules is the result of the same cause. After all, a further cause may have arisen between the sampling of the modules, as a result of which the measured variable of the last module to be sampled has changed. It is therefore unclear to the central control unit whether the values of the measured variables received all refer to one and the same cause. In other words, cause-and-effect relationships cannot be unambiguously transferred at I/O level with this communication system.

European Patent Application 0,253,381 discloses a communication system in which the data bits are transferred serially up to I/O level. In this process, address information is added to the data bits intended for a particular substation.

Information received by a substation and transmitted under the control of a master station is investigated for address coincidence. In the case of a positive result, that is to say, when the address information added to a group of data bits corresponds to the address allocated to the relevant substation, exchange is initiated. In this process, the data bits intended for a substation are replaced in the same format by data bits originating from the relevant substation and intended for the master station. In the absence of address coincidence, the information concerned is not altered.

By making use of a transmitting and receiving buffer for each substation and ensuring that address coincidence can be established within the time duration of one bit, the transmitting buffer can be read out at the same time as the receiving buffer is read in and the data bits received can be consecutively substituted by data bits to be transmitted without interruption of, or delay of, the serial data flow between the master station and the substations.

Although delays due to P/S and/or S/P conversion are prevented with this communication system, it can, however, only be used to a limited extent. The reason is that the substations connected in a chain receive and process the data bits intended for them sequentially. This means that the first substation, viewed in the transmission direction, in a chain has processed its data bits earlier and consequently has performed the operations ensuing therefrom earlier, viewed in time, than, for example, the last substation in the chain. The difference in time between the relevant responses is under these circumstances dependent on the total number of bits to be transferred in the chain and the transmission speed. This latter, in particular, cannot be made as high as desired not only because of physical considerations but, more particularly, owing to the considerably increasing costs of the system as the transmission speed increases. Extension of a substation by means of a plurality of I/O points has a direct effect on the response time of the subsequent substations. Simultaneous sampling of the substations is equally impossible because only information to be exchanged with the master station can be incorporated in the data flow at the instant when the relevant substation is addressed.

None of the known communication systems fulfils the required unambiguousness in communicating cause-and-effect relationships. To achieve this, a communication system having a so-called deterministic nature is required. That is to say, a defined time relationship must exist, both during the input and the output phase, between the response of the separate I/O modules and within a module itself, regardless of the configuration or topology of the communication system.

The object of the invention is therefore to provide a method and a communication system for serial data bit transfer, suitable for exchanging data with a desired (large) number of information points, with which a relatively rapid response which is unambiguous in terms of cause-and-effect relationships is possible and which has a low-cost structure which is flexibly adaptable.

For this purpose, the invention provides a method of serially exchanging data bits, with a plurality of input (I) and/or output (O) modules, using at least one master station (master) to which the I/O modules are connected in a cascade arrangement, characterised by under the control of the at least one master:

- supplying data bits to the I/O modules, the sequence of the data bits corresponding to the sequence of the connected I/O modules;
- receiving data bits originating from the I/O modules, the sequence of the data bits corresponding to the sequence of the connected I/O modules;
- supplying control information to the I/O modules to enable the I/O modules:
 - to present in a mutually synchronised manner, at their output side, the data bits supplied by the at least one master, and
 - to record in a mutually synchronised manner, at their input side, data bits for supply to the at least one master.

In the method according to the invention, the desired cause-and-effect unambiguousness in the presentation (cause) and recording (effect) of the I/O variables is achieved by supplying separate control information to the I/O modules under the control of the master. It is consequently possible to activate all the I/O

modules simultaneously or in a mutually synchronised manner, regardless of their position and the number of I/O modules. As a result of the serial bit transfer to the I/O level in combination with implicit addressing in which the sequence of the data bits
5 corresponds to the sequence of the I/O modules, a desired fast data exchange is achieved.

If the I/O modules are arranged at a great distance, from a geographical or communication point of view, it may be more advantageous, from the point of view of material and installation
10 costs, to form clusters of I/O modules which are then connected in cascade arrangement to the at least one master via one or more substations via a transmission system for serial bit transfer.

A further embodiment of the method according to the invention, under the control of the at least one master, comprises
15 the steps of:

- supplying the data bits for the I/O modules to the slaves via the transmission system, the sequence of the data bits also corresponding to the sequence of the connected slaves;
- receiving from the slaves via the transmission system, the
20 data bits originating from the I/O modules, the sequence of the data bits received also corresponding to the sequence of the connected slaves;
- supplying control information to the slaves via the transmission system; and
- presenting and/or recording data bits of the I/O modules
25 connected to a respective slave under the influence of the control information received, controlled by the slaves.

In order to bring about a synchronised control of the I/O modules, in this embodiment of the method according to the
30 invention use is advantageously made of the fact that the transit time of information through a substation, or in general, a branching point "node" of the transmission system, is several orders of magnitude less than the transmission time of the data bits. That is to say, the time duration for transferring control
35 information, which may consist essentially of one bit, is only a fraction of the time which is necessary to transfer a number of data bits, typically in the order of 300-1,000 bits. As a departure from the said European Patent Application 0,253,381, by

controlling, in accordance with the invention, the I/O modules not as a function of the transfer of the data bits, but of the transit time of the control information, the desired unambiguousness in the communication of cause-and-effect relationships is again achieved.

5 This is because the response point of time of each I/O module is essentially determined by the transmission rate of the system which can in practice generally be chosen as greater than the response rate of a specific application.

10 A communication system functioning on the basis of the method according to the invention has a high degree of flexibility as regards the number of data bits to be transported and the number of data bits per slave or I/O module without affecting the intended deterministic nature in relation to sampling and activating I/O modules or the devices connected thereto. The sampling instants of
15 I/O modules or the devices connected thereto can be accurately set by means of the control information supplied, as intended.

Yet a further embodiment of the method according to the invention comprises via the transmission system:

- 20 - exchanging the control information under the control of the slaves between themselves;
- transferring the control information to the at least one master under the control of the slave receiving last, and
- receiving and processing the data bits originating from the I/O modules under the control of the at least one master
25 after receipt of the control information.

The control information may be arranged either at the end of, at the beginning of or between the data bits to be transferred. In the last case, it is, of course, necessary that the substations are arranged to control the I/O modules only at the instant when, for
30 example, all the data bits have arrived in the associated I/O modules.

Receipt, by the at least one master, of control information located at the beginning of a transfer of data bits means that the relevant data bits have arrived in the slaves or I/O modules. In
35 response thereto, the at least one master may then transmit further control information to the slaves and/or the I/O modules as an indication that the actual data bit exchange can take place at I/O level. The optimum situation is, however, the one in which the

control information is transmitted behind or after the data bits. Control information bits included at the end of a transfer of data bits can act directly as an indication to the substations that the data bits intended therefor have been received and can be exchanged with the connected I/O modules or that the data bits originating from the I/O modules can be read in and that transfer of information to the master can take place.

The control information does not essentially have to remain limited to the activation of the data exchange with the I/O modules but may, inter alia, contain information for a desired (re)configuration of the system, monitoring the system, achieving a safe failure behaviour, setting or altering data types used or other desired functions. Because of this, in the preferred embodiment of the method according to the invention, the added control information is successively transferred under the control of the substations or, generally, the "nodes". This also provides, for example, the possibility of exchanging deviations from the normal operating situation in a node directly to the other slaves.

By means of the implicit addressing used, which is based on the sequence of the connected I/O modules, the invention makes optimum use of the transparent structure of a serial communication system, in contrast to the said European Patent Application 0,253,381, in which every I/O module has to be addressed separately.

Yet a further embodiment of the method according to the invention, with which only the data bits intended for, and originating from the I/O modules connected to a local data bus are transferred on said data bus, comprises the steps of:

- adding address information, under the control of the at least one master (1), to the data bits intended for the I/O modules (10) connected to a respective slave (2, 3, 4, 5), and
- detecting the address information by the slaves (2, 3, 4, 5) and only exchanging with the connected I/O modules (10) the data bits intended therefor.

Although the maximum data exchange rate theoretically achievable is reduced by adding address information bits at the level of the slaves or nodes, this nevertheless offers a number of advantages with respect to that abovementioned implicit addressing.

The reliability of the data exchange is, after all, improved because the consequences of a malfunction in an I/O module remain limited only to the data exchange with the I/O modules connected to the associated slave. It is furthermore possible, in the event of
5 malfunctions in the transmission system, for example during the switching of transmission or communication direction, nevertheless to exchange the correct data bits with the correct slave. In addition to data relating to the address, the added address information may, of course, also comprise data relating to the
10 number of data bits to be exchanged.

According to yet a further embodiment of the method according to the invention, the communication system can furthermore be efficiently used by forming packets of data bits and exchanging via the transmission system further information between the at least
15 one master and/or one or more slaves and/or one or more further stations connected to the transmission system between consecutive packets of data bits. In addition to exchanging status information, type information and data bits, information not relating to the I/O modules may also advantageously be transmitted via the transmission
20 system.

The invention also relates to a communication system suitable for carrying out the method and arranged for serially exchanging data bits under the control of the at least one master station (master) having one or more input(I) and/or output(O) modules,
25 characterised in that the I/O modules are connected in cascade to a control module via a local data bus for serial bit transfer, the I/O modules being provided with control means and the control module being provided with means, coupled to the control means, for controlling in a synchronised manner, in response to control
30 information received from the at least one master, the inputting and/or outputting of data bits by the connected I/O modules.

In the communication system according to the invention, the data bits can be transmitted, virtually without time delay to the relevant I/O modules via a local data bus for serial bit transfer.
35 Once each I/O module has received the data bits intended for this purpose from a slave, each I/O module can simultaneously proceed to processing under control of the control module and the respective control means on receiving the control information. Where

necessary, conversion from or to a parallel presentation can be carried out in the relevant I/O module. The control information can be transmitted via the local data bus to which the I/O modules are connected, via a separate connection to each I/O module or via a control line which is common to all the I/O modules.

The communication system according to the invention is essentially comparable to a shift register system, i.e. one single shift register or shift register systems separated for input and output, and has the intended deterministic nature. Both during and between the output and the input phase there is a defined simultaneity relationship in the response of the separate I/O modules.

Because a data bus for serial bit transmission is also provided at local level in the solution according to the invention, the separate I/O modules can be connected in cascade. This produces a clear and relatively cheap wiring structure, which is especially of advantage in the case of process control systems and the like where the I/O modules may be in locations which are difficult to reach and relatively remote from a control module. It will be clear that, as the number of I/O modules increases, the cost aspect becomes ever more favourable to the advantage of the communication system according to the invention.

A further advantage of the shift register system structure is that the sequence and the number of the data bits in the system can correspond directly to the sequence and the number of data bits of the I/O modules thereof. The addition, to the data bits to be exchanged, of address information relating to the I/O modules is therefore not a requirement in this connection. This has a favourable effect on the effective speed at which the information can be exchanged.

In principle, the number of I/O modules can be increased indefinitely. Furthermore, a control module has only to be provided with one interface for connecting the cascade of I/O modules. This is in contrast to communication systems in which every I/O module is connected to a control module via a separate interface. The number of I/O modules to be connected is determined in such a case by the number of connection possibilities for which the relevant control is dimensioned.

A further embodiment of the communication system according to the invention, which is suitable for communication over relatively large distances, comprises one or more substations (slaves) each provided with a control module having one or more I/O modules
5 connected in cascade thereto via a local data bus for serial bit transfer, the slaves, including their control module, being connected to the at least one master via a transmission system for serial bit transfer.

The master station and the substations of said communication
10 system each form a node between which information is bit-serial exchanged. The said master/slave relationship only relates to the procedure followed, in which one or more nodes control the data exchange as a whole (masters) and the other nodes (slaves), in response thereto, providing the actual data exchange with the I/O
15 modules.

In order to approach the intended behaviour as a shift register system as much as possible, in a further embodiment of the communication system according to the invention, a slave is provided with time control means for the transfer, of the data bits
20 via the local data bus in synchronism with the transfer of the data bits via the transmission system. This communication system has a network structure which is "transparent" in relation to the bit transfer, which is a requirement for arriving at an exchange, having as little delay as possible, of information between the
25 master, the connected slaves and the I/O modules.

If the number of data bits per slave is equal, or if the master knows the number of data bits intended for each slave, it is not in principle necessary to add address information of the respective slaves to the data to be exchanged. In order, however,
30 to allow the slaves to operate mutually as independently of one another as possible with retention, of course, of the deterministic operation of the communication system as a whole, it is advantageous to provide a slave with an unambiguous address and to add address information bits to the data bits to be exchanged. The
35 transparent nature of the communication system according to the invention can then be retained without the need to transmit all the data bits to be exchanged via all the connected I/O modules.

In accordance with yet a further embodiment of the invention,

this can be achieved in that the control module is provided with selection means for only transmitting data bits intended for, or originating from the I/O modules connected to said control module via the local data bus.

5 In this further embodiment, there are transmitted via the local data bus only the data bits intended for the relevant I/O modules connected thereto or the data bits originating therefrom. The information for I/O modules connected to another slave is transmitted at the level of the slaves themselves. This embodiment
10 of the communication system increases the modularity thereof and the possibility of monitoring the data exchange and the operation of the connected nodes.

 In still a further embodiment, which makes use of the selection of data bits for the respective local data buses, the
15 control module is arranged to transfer the data bits via the local data bus at a rate deviating from the transfer of the data bits via the transmission system. Provided the field of application permits this, a relatively low transmission rate of data bits via the local data bus has a low-cost effect. After all, the price of electronic
20 components is known to increase as a higher processing speed is required. A higher transmission rate of the data bits via the local data bus, compared with the bit transfer via the transmission system between the slaves and the at least one master, has, on the other hand, the advantage that time becomes available in order, for
25 example, to allow the slave to carry out control operations prior to supply information to the I/O modules and/or to supply data originating from the I/O modules to the master, in order, for example, to prevent the exchange of erroneous data as much as possible.

30 In addition to the advantages already mentioned of a high flexibility in the number of I/O modules to be connected and an increase in the effective information exchange rate, an I/O module suitable for use in the communication system according to the invention can also be constructed particularly simply and cheaply.
35 In an embodiment of the invention, the means of an I/O module comprise for this purpose one or more shift registers for the serial transmission of the data bits via the local data bus.

 In a further embodiment based thereon, the shift registers

are arranged for the serial transfer of data bits supplied in parallel to the input side of an I/O module and/or for the parallel presentation, at the output side of an I/O module, of serially transferred data bits intended for the relevant I/O module. By
5 providing the shift register with a number of outputs corresponding to the number of data bits intended for a particular I/O module, provision can be made for a parallel representation of the relevant data bits at the output side of an I/O module. In the case of information which should be included in the data flow, the relevant
10 data bits can easily be replaced, using such a shift register, by the data bits supplied at the input side of an I/O module.

Because the information exchange takes place under the control of the master, it is necessary to transmit to the master every change in the state of a slave, such as, for example, the
15 connection or removal of a connected I/O module or the alteration of the type of I/O module, for example only an I module. In an embodiment of the communication system according to the invention, the control module is provided for this purpose with means for detecting and exchanging, with the at least one master, information
20 about the status condition and/or type coding of the connected I/O modules. It is obvious that errors in the functioning of a control module and/or an I/O module must be capable of being detected by the master. In this connection, use can advantageously be made of the exchange of the status condition and/or type coding, this being
25 because the non-receipt, or the receipt in a non-predetermined way, of the status information is an indication to the master that a possible error situation may have occurred.

With the same object, in an embodiment of the invention, the control means of an I/O module are arranged to monitor the
30 operation thereof and/or the operation of the local data bus. The monitoring of the operation of each separate I/O module and the local data bus is of essential importance because, as a consequence of a serial coupling of the I/O modules, a malfunction in the local data bus or a module can result in disruption of the information
35 exchange with the other I/O modules. Because all the lines of, for example, the local data bus are active at the same time during serial transmission, in contrast to a parallel bus in which the lines are in general not always active at the same time, the

monitoring means can be of relatively simple construction.

In particular, with implicit addressing of the I/O modules, that is to say, if the sequence of the data bits corresponds to the sequence of the I/O modules of the relevant slave, errors in the transmission system and/or the local data bus can give rise to undesirable responses. To prevent this as far as possible, in an embodiment of the communication system according to the invention, a slave is provided with means for monitoring the serial transfer of data bits via the transmission system and/or the local data bus.

A complete monitoring of the data exchange is achieved in that the at least one master is provided with means for detecting error situations in the transmission system. When a transmission error is detected, the control module of a slave will not accept the data received, nor will it transmit new data. The data bits received are then transferred further unchanged. The master then receives back the data bits despatched, possibly with transmission errors. By checking the transmitted and received data, information can be obtained about a transmission fault. If necessary, the relevant data bits can, for example, be transmitted again.

Owing to the serial transfer down to the level of the I/O modules, the nodes in the communication system according to the invention are particularly suitable for use in a ring network configuration. Making use of this, the slaves in a further embodiment of the invention are connected to the at least one master via a multiple ring transmission system, the at least one master and the slaves being provided with means for change-over of a transmission system ring.

A very flexible system is obtained in an embodiment of the invention in that the at least one master and slaves are designed to transmit or receive packets of data bits via a transmission system ring in one and/or the other direction. Master and/or slaves constructed in this way are capable of functioning as a switching centre so that, for example, the master is able to reach as many connected slaves as possible in a fault situation.

The invention also relates to an I/O module, a substation (slave) and a master station (master) corresponding to, and suitable for, use in the communication system according to one or more of the preceding embodiments.

The invention is now explained below in greater detail with reference to the description of an exemplary embodiment of the communication system and the accompanying drawings, in which:

Figure 1 shows diagrammatically the basic embodiment of the communication system according to the invention,

Figure 2 shows diagrammatically an extended communication system constructed according to the invention,

Figure 3 shows a block diagram of an exemplary embodiment of the transmission unit and the control module of a substation in Figure 2,

Figure 4 shows a block diagram of an exemplary embodiment of an I/O module, and

Figure 5 shows a block diagram of an exemplary embodiment of the master station in Figure 2.

Figure 1 shows diagrammatically the basic structure of the communication system according to the invention, comprising a master station (master) 1 to which one or more input (I) and/or output (O) module(s) 10 are connected via a control module 9. The I/O modules 10 are arranged in cascade for each control module and in this way form, as seen in abstraction, two shift register systems connected to the master 1, as indicated diagrammatically by the dash-dot lines.

The embodiment of the communication system according to the invention shown in Figure 1 is suitable for applications in which the I/O modules are situated relatively close to one another from a geometrical and transmission point of view, for example a measurement and control system in a machine of limited dimensions.

Figure 2 shows diagrammatically the architecture of a more extensive communication system according to the invention, comprising a master station (master) 1 and a plurality of substations (slaves) 2, 3, 4, 5. The master 1 and the slaves 2, 3, 4, 5 are mutually connected via a double-ring transmission system composed of transmitting/ receiving units 6 and transmission lines 7, 8. The transmission lines 7, 8 may, for example, consist of coaxial cable, optical fibre cable and the like.

Each slave 2, 3, 4, 5 comprises a control module 9 which is connected to the associated transmitting/receiving unit 6 and to which one or more input (I) and/or output (O) module(s) are

connected. The number of I/O modules 10 to be connected to a control module may vary from slave to slave depending on its function, for example controlling a measurement and control process.

5 The I/O modules are arranged in cascade for each slave and in this way form, seen in abstraction, a continuation of the transmission system. A dash-dot line 11 diagrammatically shows the data flow in the communication system. The data bits are serially transferred both in the transmission system 7, 8 and to the level
10 of the I/O modules 10.

As a result, the whole again has a structure corresponding to a shift register, every I/O module being implicitly addressed, as in the system according to Figure 1, by its position in the chain.

15 Although a double-ring transmission system is shown, it will be clear that it is possible to work with either a single-ring transmission system or with a transmission system containing more than two rings. Of course, more or fewer slaves can be used and the number of I/O modules per slave can be greater or smaller.

20 The shift register principle is also of advantage with respect to use, for example for reliability reasons, of a plurality of masters as is illustrated in Figure 2 by the broken lines. In such a multi-master concept, one of the masters is in general active in relation to data exchange, while one or more other masters only have a passive role therein. All the masters are so
25 designed that they can assume the function of the active master, for example in the event of faults. The passive masters are easily able to detect errors of the active master because, as a consequence of their cascade arrangement and the serial transfer of data bits in the communication system according to the invention,
30 they receive all the information which is intended for the active master. Consequently, no separate communication path is required between the various masters to keep the passive masters abreast of the operations, instruction etc. carried out by the active master. Such a "hot stand-by" mode is of importance, in particular, in
35 industrial process measurement and control in which failure or delay in the production process may, inter alia, have serious financial consequences. It is obvious that, in such a multi-master concept, the conditions under which, and the manner in which, the

tasks of a master are assumed by another master have to be specified in advance.

Figure 3 shows a block diagram of an exemplary embodiment of a portion of a slave 2, 3, 4, 5. Data bits are transported via connections provided with an arrow. The transmitting/receiving unit 6 comprises a multiplexer 12 consisting of two modems 13, 14 which are respectively connected to the first transmission ring 7 and to the second transmission ring 8. For the transmission of the data via the transmission system, signal coding techniques known per se in practice may be used. The operation of the relevant transmission ring 7, 8 can be monitored by means of line error detectors 15.

After demodulation by one of the modems 13, 14, the data received are fed to the control module 9 connected to the multiplexer 12 which, in the exemplary embodiment shown, is arranged to exchange information with the master in accordance with the known Synchronous Data Link Control (SDLC) protocol. Any other suitable protocol can be used instead of the SDLC protocol. The unit in the control module which caters for the exchange of the information in the chosen protocol is indicated by the reference numeral 16.

With the aid of time control means 17 connected to the multiplexer 12 and unit 16, the time control information required for the control module 9 is derived from the transmission of the data bits via the transmission system 7, 8. This achieves the result that the transfer of the data bits by the slave or the I/O modules can take place in synchronism with the transmission of the data bits via the transmission system 7, 8. All these features result in a transparent communication structure.

Driver and monitoring means 18 are furthermore connected to unit 16 to control and monitor the operation of a local data bus 19 for serial bit transfer. The respective I/O modules 10 are connected in cascade to a said local data bus 19 (not shown in Figure 3). A control line 39 is provided for controlling the I/O modules 10. Control information received is transmitted via said control line 39 to the I/O modules 10 to present them at their output side and/or record data bits at their input side.

As already discussed in the introduction, every slave can be

provided with an unambiguous address and the addressing of the separate I/O modules 10 can take place on the bases of their sequence in the cascade arrangement. Consequently, a unit 20 which is capable of decoding the address of a slave, a unit 21 which is capable of detecting information about the number of data bits for a relevant slave and, if necessary, a unit 22 which is capable of reading out information about the type coding of the I/O modules connected to the local data bus, for example a module having only an input side or a module having only an output side, are provided.

10 A further unit 23 is provided for a content check of the data bits received, for example on the basis of error detection techniques known per se. The relevant units 20, 21, 22, 23 are all connected to the unit 16 or form part thereof.

Status data relating to whether an I/O module is connected or not are collected in a unit 24 which also receives information about the operation of the multiplexer 12, the transmission ring 7, 8 in service and information about the power supply and the correct operation of the local data bus of the relevant slave. Said status information is transmitted to the master 1 via the unit 16. On the basis of this it is possible to correct the data flow for a respective slave or to generate information about the operational state of the slave.

A practical embodiment of the control module 9 is achieved with a single so-called "gate-array" integrated circuit of type EPM 5128 manufactured by Altera. Although the slaves do not essentially have to have any intelligence, it will be clear to the person skilled in the art that the possibilities include, for example, implementation with one or more microprocessors. In this connection, it is possible to think, in particular, of designs of the communication system in which the data bits are transmitted via the local data bus 19 with a rate deviating from the data bits via the transmission system 7, 8, these features being as described in the introduction.

For use in the basic embodiment of the communication system as shown in Figure 1, the control module 9, may, of course, be of simpler construction than the embodiment for use in the extended system according to Figure 2. In particular, the units 20 and 21 are superfluous.

A possible embodiment of an I/O module 10 is shown in block diagram in Figure 4. In its simplest form, an I/O module comprises a single shift register through which the data bits to be transmitted are shifted. When the data bits intended for the relevant I/O module are all, for example, received in the shift register, the relevant information can be read out, if necessary in parallel, by means of a control signal without disrupting the bit transfer. To place information, for example measurement data, in a packet, the reverse path can be traversed.

10 In the exemplary embodiment shown in Figure 4, the I/O module 10 has four shift registers 25, 26, 27 and 28, respectively. The number of bit positions in a shift register corresponds to the number of bit positions of the data bits for the relevant I/O module. The shift registers 25 and 26 are located in cascade at the output side 33 and the shift registers 27 and 28 are located at the
15 input side 34 of the I/O module. Data bits are transmitted from and to the relevant I/O module via the connections, provided with an arrow, to the local data bus 19.

The shift registers 25 and 27 provide, via the buffers 29 and
20 30, respectively, connected thereto, a parallel digital output and a parallel digital input, respectively. The shift registers 26 and 28 provide an analog output and analog input, respectively, via the D/A convertor 31 and the D/A convertor 32, respectively.

A practical embodiment of an I/O module is achieved with
25 digital shift registers 25, 26 of the type 74HC4094 and, for the digital shift registers 27, 28, of the type 74HC7597, all manufactured by Philips.

Connected to the buffers 29, 30 and the convertors 31, 32 are control signal lines which are activated from the control module 9
30 via the control line 39 and the control means 35, respectively, for the presentation of data bits at the output side 33 and the recording of data bits at the input side 34. The clock signal lines necessary for transmitting the data bits through the shift registers 25, 26, 27 and 28 are not explicitly shown for the sake
35 of clarity. Clock signals, in general time control signals, are preferably fed to the I/O modules via separate lines from the control module 9. It is, however, also possible, for example, to reconstruct the time control signals from the transfer of the data

bits over the local data bus 19.

If desired, the control means 35 of an I/O module may be designed to monitor the operation thereof and/or the operation of the local data bus 19. The control means 35 then monitor the activity on the local data bus 19 and also, at the input and output side respectively, the buffers 30, 29 and, if necessary, the convertors 32, 31. The result of the monitoring by the control means 35 can be transmitted to the means 23 in the control module 9 as information about the status condition of the relevant I/O module. The control means 35 can be implemented for this purpose in relatively simple manner by means of gate circuits because all the lines are active during serial data exchange.

The absence of the need to use intelligent components, such as microprocessors, in the I/O modules makes it possible to construct the latter relatively cheaply, which is of importance, especially in measurement and control process applications in which a large number of information points must be capable of being sampled and/or controlled. It will be clear that if it is used only for inputting information, the embodiment of an I/O module 10 shown in Figure 4 can be of simpler construction by the omission of the shift registers 25 and 26 and the associated buffer 29 and D/A convertor 31, respectively. In an analogous way, it is true of an I/O module which has only to be suitable for the delivery of signals that the shift registers 27 and 28, the buffer 30 and the A/D convertor 32 at the input side 34 are omitted. It is also not necessary per se to provide both a digital input and/or output and also an analog input/output. This clearly expresses the simplification of the I/O means intended by the invention. In practice, more input variables occur than output variables.

The software for controlling the communication system according to the invention is essentially concentrated in the master 1 which comprises, in an exemplary embodiment of the invention as shown in Figure 5, a control unit 36 for controlling the data flow via the transmission system 7, 8, with an associated memory 37 for storing and exchanging information with a control computer 38 which contains the calculations and background information necessary for the process to be controlled via the I/O modules. Further peripheral equipment, for example a further

computer (not shown) for supporting the control computer 38, may be connected to said control computer 38.

The transmitting/receiving unit 6 provides for the monitoring of the transmission and the control computer 38 provides for and
5 monitors the correct sequence of the data bits for a relevant slave, related to the sequence in which the I/O modules are arranged. The information about this sequence is extracted by the control unit 36 from the status information received from the relevant slaves.

10 In the case where the transmission system is constructed, as shown in Figure 2, as a multiple ring transmission system, the transmitting/receiving unit 6 also provides for the switching of the transmission ring or of the communication direction of the data flow. All this being on the basis of the information obtained about
15 whether the connection to the transmission system is or is not operating correctly. For use in the communication system according to Figure 1 the unit 6 can be omitted.

The transmitting/receiving unit 6 can be constructed in a similar way to that shown in Figure 3. A practical embodiment of
20 the master is achieved with a microprocessor of type MC 68020, manufactured by Motorola, as control computer and with a programmable logical device of the type EPM 5128, manufactured by Altera, as control unit 36.

It is true of the exemplary embodiments discussed of the
25 various components of the communication system according to the invention that a large number of the functions indicated with a block can be performed both by hardware and by software.

In a practical embodiment of the communication system according to Figure 2, in which glass-fibre cable is used as
30 transmission medium, information can be processed at 2 Mbit/sec. In, for example, an I/O configuration of 10,000 bits (10,000 I/O points) an I/O point can be scanned or driven every 10 msec. The cyclic nature of the data bit exchange, that is to say, every I/O module is regularly driven at a fixed interval or data are
35 requested from it, is an important characteristic of the present invention. Occasional errors in the information exchanged are very quickly corrected, as a result of which the information in the master about the I/O modules will always conform to reality.

Because the information exchange preferably takes place in packets, the transmission system can be used to transmit, for example, information for testing connected slaves and the like during the time when no exchange of information is taking place between the master and the connected slaves. For this purpose, one or more further processor(s) may, if necessary, be connected to the transmission system. Information not directly relevant to the application can also be exchanged with other stations connected to the transmission system.

10 It will be clear that the invention is not restricted to a communication system containing the embodiments, discussed by way of example, of the master, slaves and I/O models. A person skilled in the art can make many alterations and additions without deviating from the inventive idea underlying the invention.

Claims

1. Method of serially exchanging data bits with a plurality of input(I) and/or output(O) modules (10), using at least one master station (master) (1) to which the I/O modules (10) are connected in a cascade arrangement, characterised by under the control of the at least one master (1):
- supplying data bits to the I/O modules (10), the sequence of the data bits corresponding to the sequence of the connected I/O modules (10);
 - receiving data bits originating from the I/O modules (10), the sequence of the data bits corresponding to the sequence of the connected I/O modules (10);
 - supplying control information to the I/O modules (10) to enable the I/O modules (10):
 - to present in a mutually synchronised manner, at their output side (33), the data bits supplied by the at least one master (1), and
 - to record in a mutually synchronised manner, at their input side (34), data bits for supply to the at least one master (1).
2. Method according to Claim 1, wherein a plurality of I/O modules (10) are connected in cascade to one or more substations (slaves) (2, 3, 4, 5), which substations (2, 3, 4, 5) are connected to the at least one master (1) in cascade via a transmission system (7, 8) for serial bit transfer, characterised by under the control of the at least one master (1):
- supplying the data bits for the I/O modules (10) to the slaves (2, 3, 4, 5) via the transmission system (7, 8), the sequence of the data bits also corresponding to the sequence of the connected slaves (2, 3, 4, 5);
 - receiving from the slaves (2, 3, 4, 5) via the transmission system (7, 8) the data bits originating from the I/O modules (10), the sequence of the data bits received also corresponding to the sequence of the connected slaves (2, 3, 4, 5);
 - supplying control information to the slaves (2, 3, 4, 5) via the transmission system (7, 8); and

- presenting and/or recording data bits of the I/O modules (10) connected to a respective the relevant slave (2, 3, 4, 5) under the influence of the control information received, controlled by the slaves (2, 3, 4, 5).
- 5 3. Method according to Claim 2, comprising via the transmission system (7, 8):
- exchanging the control information under the control of the slaves (2, 3, 4, 5) between themselves;
 - transferring the control information to the at least one
10 master (1) under the control of the slave (2, 3, 4, 5) receiving last, and
 - receiving and processing the data bits originating from the I/O modules (10) under the control of the at least one master (1) after receipt of the control information.
- 15 4. Method according to Claim 2 or 3, in which the slaves (2, 3, 4, 5) are provided with selection means (20-22) for address information, comprising:
- adding address information under the control of the at least one master (1) to the data bits intended for the I/O modules
20 (10) connected to a respective slave (2, 3, 4, 5), and
 - detecting the address information by the slaves (2, 3, 4, 5) and only exchanging with the connected I/O modules (10) the data bits intended therefor.
- 25 5. Method according to one or more of Claims 2 to 4 inclusive, comprising under the control of the at least one master (1):
- forming a packet of data bits;
 - adding control information to the packet formed for exchanging data bits with the slaves (2, 3, 4, 5) and/or the I/O modules (10), in which
 - via the transmission system (7, 8) between the at least one
30 master (1) and/or one or more slaves (2, 3, 4, 5) and/or one or more further stations connected to the transmission system (7, 8) information can be exchanged, between packets of data bits and/or control information.
- 35 6. Communication system arranged for serially exchanging data bits under the control of at least one master station (1) having one or more input(I) and/or output(O) modules (10), characterised in that the I/O modules (10) are connected in cascade to a control

module (9) via a local data bus (19) for serial bit transfer, the I/O modules (10) being provided with control means (35) and the control module (9) being provided with means (16), coupled to the control means (35), for controlling in a synchronised manner, in response to control information received from the at least one master (1), the inputting and/or outputting of data bits by the connected I/O modules (10).

7. Communication system according to Claim 6, further comprising one or more substations (slaves) (2, 3, 4, 5) each provided with a control module (9) having one or more I/O modules (10) connected in cascade thereto via a local data bus (19) for serial bit transfer, the slaves (2, 3, 4, 5), including their control module (9), being connected to the at least one master (1) via a transmission system (7, 8) for serial bit transfer.

8. Communication system according to Claim 7, wherein a slave (2, 3, 4, 5) is provided with time control means (17) for the transfer of the data bits via the local data bus (19) in synchronism with the transfer of the data bits via the transmission system (7, 8).

9. Communication system according to Claim 7 or 8, wherein the control module (9) is provided with selection means (20-22) for only transmitting data bits intended for, or originating from the I/O modules (10) connected to said control module (9) via the local data bus (19).

10. Communication system according to Claim 9, wherein the control module (9) is arranged to transfer the data bits via the local data bus (19) at a rate deviating from the transmission of the data bits via the transmission system (7, 8).

11. Communication system according to one or more of Claims 7 to 10 inclusive, wherein a slave (2, 3, 4, 5) is provided with means (15, 18, 23) for monitoring the serial transfer of data bits via the transmission system (7, 8) and/or the local data bus (19).

12. Communication system according to one or more of Claims 7 to 11, wherein the at least one master (1) is provided with means for detecting error situations in the transmission system (7, 8).

13. Communication system according to one or more of Claims 7 to 12 inclusive, wherein the slaves (2, 3, 4, 5) are connected to the at least one master (1) via a multiple ring transmission system,

the at least one master (1) and the slaves (2, 3, 4, 5) being provided with means (6) for changeover of a transmission system ring (7, 8).

14. Communication system according to Claim 13, wherein the at least one master (1) and the slaves (2, 3, 4, 5) are arranged to transmit or receive data bits via a transmission ring (7, 8) in one and/or the other direction.

15. Communication system according to one or more of Claims 6 to 14 inclusive, wherein the control means (35) of an I/O module (10) are arranged to monitor the operation thereof and/or the operation of the local data bus (19).

16. Communication system according to one or more of Claims 6 to 15 inclusive, wherein the I/O modules (10) comprise one or more shift registers (25, 28) for serially transferring data bits via the local data bus (19).

17. Communication system according to Claim 15, wherein the shift registers (25-28) are arranged for the serial transfer of data bits supplied in parallel at the input side (34) of an I/O module (10) and/or for the presentation, parallel at the output side (33) of an I/O module (10), of serially transmitted data bits intended for the respective I/O module (10).

18. Communication system according to one or more of Claims 6 to 17, wherein the control module (9) is provided with means (23) for detecting and exchanging with the at least one master (1) information about the status condition and/or type coding of the connected I/O modules (10).

19. I/O module (10) provided with an input side (34) and/or output side (33) suitable for use in a communication system according to one or more of Claims 6 to 18 inclusive and arranged according to one or more of Claims 6, 15, 16 or 17.

20. Substation (slave) (2, 3, 4, 5) suitable for use in a communication system according to one or more of Claims 7 to 18 inclusive and arranged according to one or more of Claims 8, 9, 10, 11, 13, 14 or 18.

21. Master station (master) (1) suitable for use in a communication system according to one or more of Claims 6 to 18 inclusive and arranged according to one or more of Claims 6, 12, 13 or 14.

fig-5

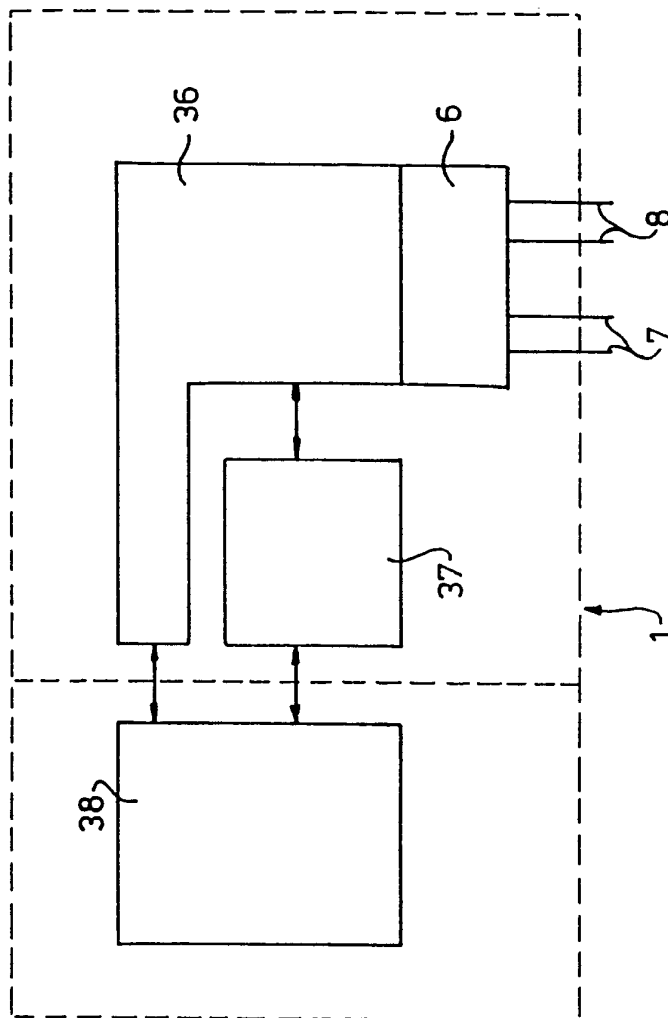
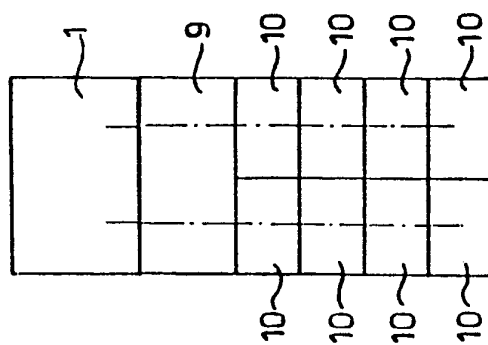


fig-1



SUBSTITUTE SHEET

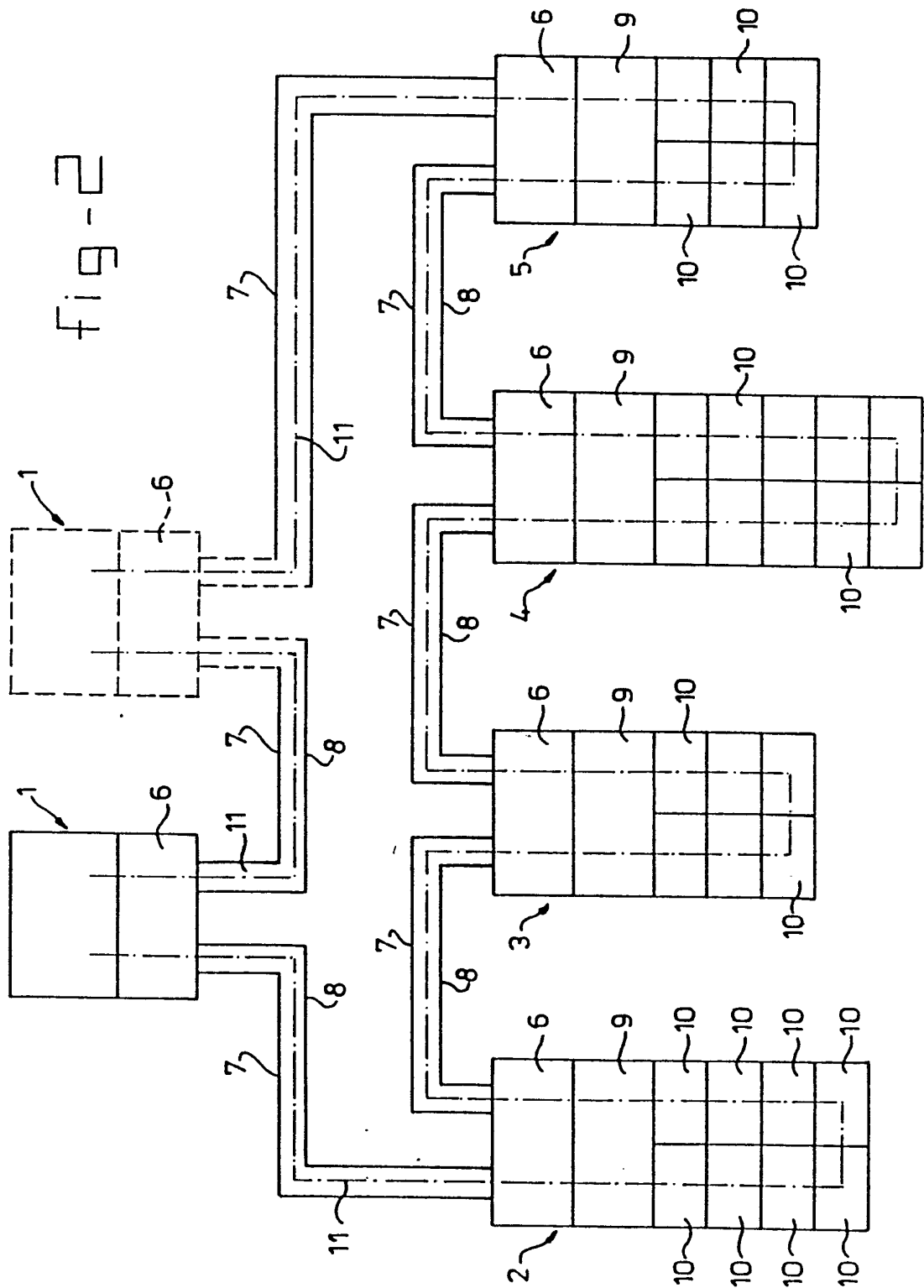
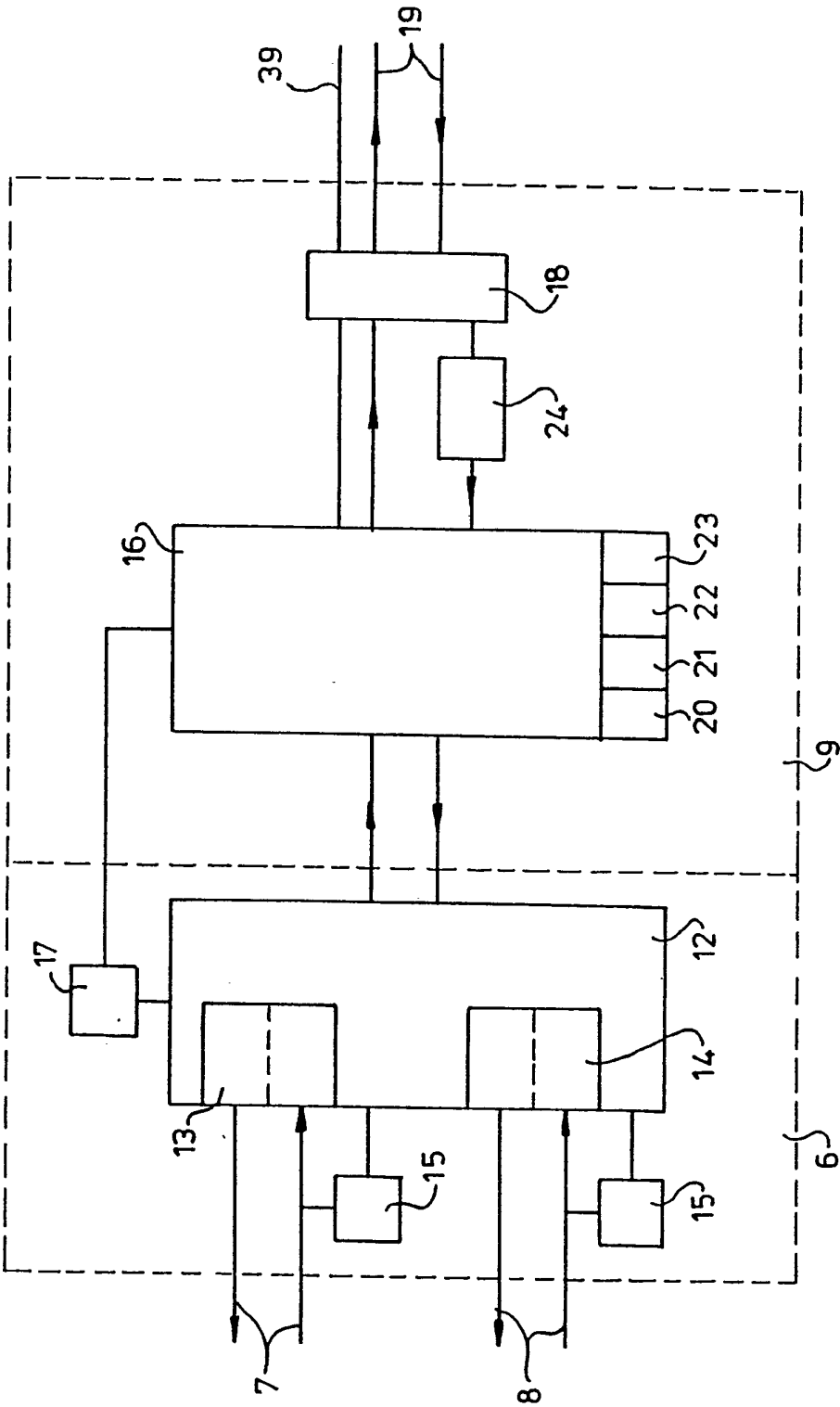
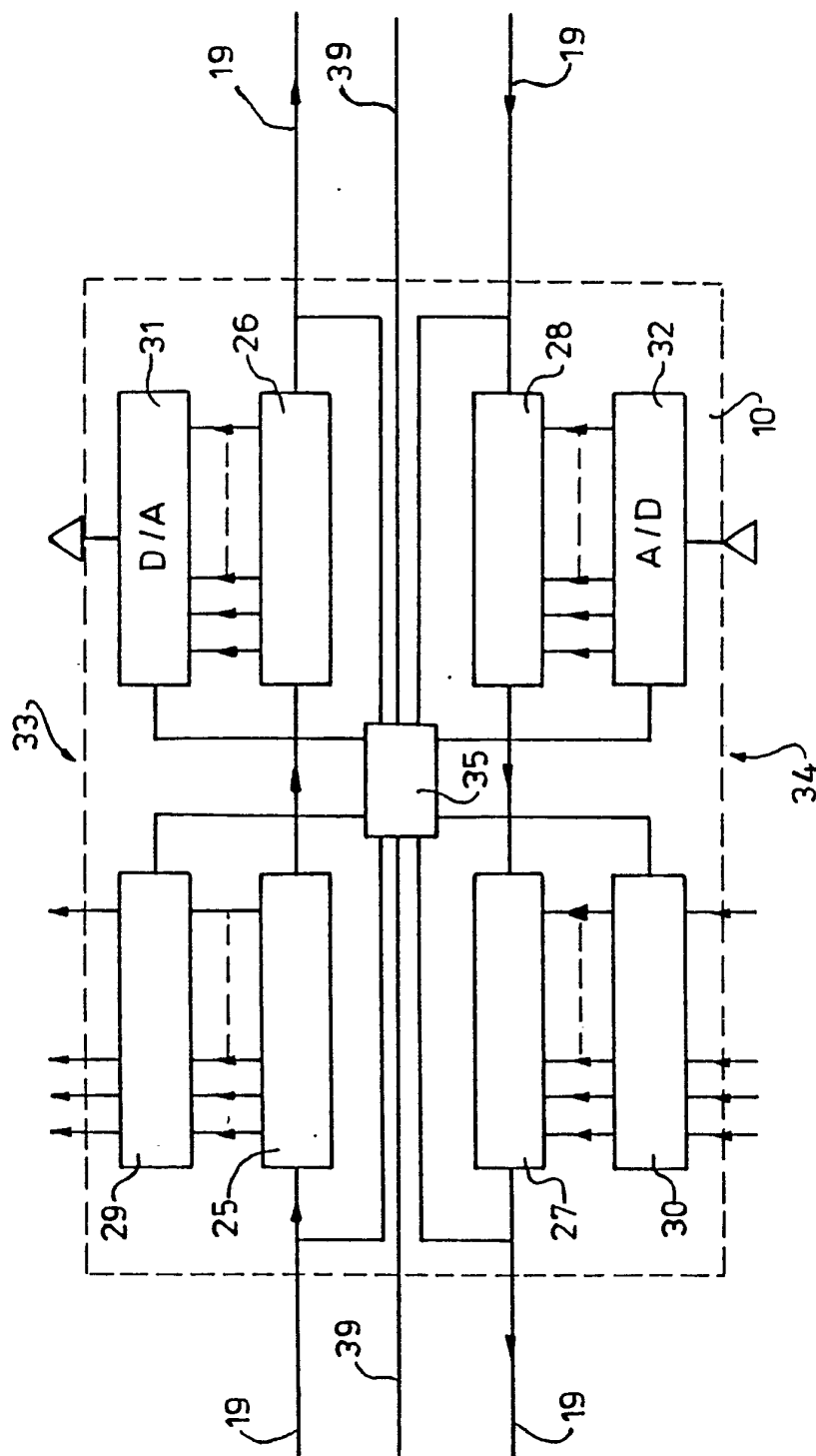


fig - 3



SUBSTITUTE SHEET

fig - 4



SUBSTITUTE SHEET

INTERNATIONAL SEARCH REPORT

International Application No

PCT/NL 91/00041

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) ⁶		
According to International Patent Classification (IPC) or to both National Classification and IPC: Int.Cl. 5 H04L12/28		
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁷		
Classification System	Classification Symbols	
Int.Cl. 5	H04L ; H04Q	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched ⁸		
III. DOCUMENTS CONSIDERED TO BE RELEVANT⁹		
Category ¹⁰	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³
Y	US,A,4004275 (R.L. ARNDT ET AL.) 18 January 1977 see column 1, line 67 - column 2, line 14 see column 3, line 42 - column 4, line 31 see column 7, line 52 - column 8, line 4 see column 8, line 60 - column 9, line 14	1, 6, 16
A	---	2, 7, 19-21
Y	EP,A,166402 (ALLEN-BRADLEY COMPANY) 02 January 1986 see abstract see page 2, line 19 - page 3, line 16 see page 4, line 6 - page 5, line 15 --- -/--	1, 6, 16
¹⁰ Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. "&" document member of the same patent family		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report	
1 27 JUNE 1991	14. 08. 91	
International Searching Authority	Signature of Authorized Officer	
EUROPEAN PATENT OFFICE	STAESSEN B.F.	

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)		
Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A	GB,A,2080000 (SHORROCK DEVELOPMENTS LTD) 27 January 1982 see abstract see page 1, left-hand column, lines 27 - 58 see page 2, right-hand column, lines 99 - 108; claim 1 (cited in the application) ---	1, 6-8, 15
A	EP,A,253381 (MATSUSHITA) 20 January 1988 see page 1, line 21 - page 2, line 23 see page 3, lines 9.- 26 see page 4, line 15 - page 6, line 12 see page 7, line 11 - page 10, line 16 see page 13, line 9 - page 15, line 6 (cited in the application) ---	1, 6-8, 16
A	MICROPROCESSORS AND MICROSYSTEMS. vol. 12, no. 1, January 1988, LONDON GB pages 3 - 12; D. Bracknell: "introduction to the Mil-Std-1553B serial multiplex data bus" see page 7, left-hand column, lines 15 - 56 see page 7, right-hand column, lines 16 - 36 see page 7, right-hand column, line 48 - page 8, left-hand column, line 37 ---	2, 7, 9-12, 19-21
A	LANDIS UND GYR MITTEILUNGEN. vol. 26, no. 1, 1979, ZUG CH pages 2 - 12; P. Schneider et al.: "VISIONIK-ZLT-System: Anwendung, Aufbau, Funktionen und Möglichkeiten zur Energieeinsparung" see page 4, middle column, lines 5 - 25 see page 5, left-hand column, lines 1 - 47; figures 3, 5 ---	2, 7, 11-13, 15
P,A	US,A,4982185 (R. HOLMBERG ET AL.) 01 January 1991 see abstract ---	1, 6

ANNEX TO THE INTERNATIONAL SEARCH REPORT
ON INTERNATIONAL PATENT APPLICATION NO.

PCT/NL 91/00041
SA 45898

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
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27/06/91

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EP-A-253381	20-01-88	JP-A- 63204940 JP-A- 63020936 US-A- 4847613	24-08-88 28-01-88 11-07-89
US-A-4982185	01-01-91	None	

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