

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LENNOX INDUSTRIES INC.,
Petitioner,

v.

ROSEN TECHNOLOGIES LLC,
Patent Owner.

Case No. IPR2023-00718
Patent 7,185,825 B1

**DECLARATION OF R. JACOB BAKER, PH.D., P.E. IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF CLAIMS 1, 4 AND 11-16 OF
U.S. PATENT NO. 7,185,825 B1**

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Appendix A: CV of R. Jacob Baker, Ph.D., P.E.

I, R. Jacob Baker, Ph.D., P.E., declare as follows:

I. INTRODUCTION

1. I have been retained by counsel for Lennox Industries Inc. (the “Petitioner”) in connection with the above-captioned *inter partes* review (“IPR”) of Claims 1, 4 and 11-16 of U.S. Patent No. 7,185,825 B1 (the “’825 Patent”), entitled Programmable Thermostat Employing A Fail Safe Real Time Clock, by named inventor Howard Rosen. I understand that the ’825 Patent is assigned to Rosen Technologies LLC (the “Patent Owner”). I have been asked to provide technical review, analysis, insights, and opinions regarding the ’825 Patent and the prior art references that form the basis for the ground of unpatentability set forth in the Petition for *Inter Partes* Review of the ’825 Patent (the “Petition”). I have been asked to provide a declaration regarding my opinions on the validity of Claims 1, 4 and 11-16 of the ’825 Patent.

2. This declaration sets forth the opinions I have formed in this IPR and provides the bases and reasons for those opinions. I have summarized in this section my educational background, professional experience, and publications. My education and professional experience are described in my curriculum vita, attached to this declaration as Appendix A.

3. This declaration is based on information currently available to me. I declare that I have personal knowledge of the facts set forth in this declaration and, if called to testify as a witness, could and would do so competently.

4. I am being compensated at my usual consulting rate of \$765 per hour for my work on this matter. I am also being reimbursed for any incurred expenses. My compensation is in no way dependent upon my opinions or testimony or the outcome of this proceeding. I have no other interests in this proceeding or with Petitioner or Patent Owner.

II. PROFESSIONAL BACKGROUND AND QUALIFICATIONS

5. My qualifications generally are set forth in my Curriculum Vitae, which is attached as **Appendix A**. Appendix A also includes a list of the publications I have authored and a list of the other cases in which I have testified during the last four years.

6. I have been working as an Engineer since 1985 and I have been teaching Electrical and Computer Engineering courses since 1991. I am currently a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas (“UNLV”).

7. I received B.S. and M.S. degrees in Electrical Engineering from UNLV in 1986 and 1988, respectively. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno, in 1993.

8. My doctoral research, culminating in the award of a Ph.D., investigated the use of power MOSFETs in the design of very high peak power, and high-speed, instrumentation. I developed techniques to reliably stack power MOSFETs to switch

higher voltages, that is, greater than 1,000 V and 100 Amps of current with nanosecond switching times. This work was reported in the paper entitled “Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices,” published in the IEEE Transactions on Power Electronics. The paper received the Best Paper Award in 2000.

A. Industry Experience

9. I have done technical and expert witness consulting for over 200 companies and their subsidiaries since I started working as an engineer in 1985. From 1985 to 1993, I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapon tests at the Nevada test site. During this time, I designed, and oversaw the fabrication of, over 30 electronic and electro-optic instruments, including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame and bit-syncs, data converters, streak-camera sweep circuits, Pockel’s cell drivers, micro-channel plate gating circuits, charging circuits for battery backup of equipment for recording test data, and analog oscilloscope electronics.

10. My work during this time, as one example, had a direct impact on my doctoral research work using power MOSFETs, subsequent publishing efforts, and industry designs. In addition to the 2000 Best Paper Award from the IEEE Power Electronics Society, I published several other papers in related areas while working

in industry. I hold a patent, Patent No. 5,874,830, in the area of power supply design, titled, “Adaptively biased voltage regulator and operating method,” which was issued on February 23, 1999. I have designed dozens of linear and switching power supplies for commercial products and scientific instrumentation.

11. I am a licensed Professional Engineer and have extensive industry experience in circuit design, fabrication, and manufacture of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, Phase-Change Random Access Memory (PCRAM) chips, and CMOS Image Sensors (CISs) at Micron Technology, Inc. (“MTI”) in Boise, Idaho. I spent considerable time working on the development of flash memory chips while at MTI. My efforts resulted in more than a dozen patents relating to flash memory. One of my projects at MTI included the development, design, and testing of circuit design techniques for a multi-level cell (MLC) flash memory using signal processing. This effort resulted in higher-density memories for use in solid-state drives and flash memory cards having an ATA interface that are ubiquitous in consumer electronics, including cameras and data storage systems. Further, the use of higher-density memory can result in fewer changes in the flash translation layer for logical-to-physical addressing, less need for garbage collection, and larger data segments that can improve a computing system’s performance. Another project I worked on at MTI focused on the design of buffers for high-speed double-data rate DRAM, which resulted in around 10 U.S. patents in

buffer design. Among many other experiences, I led the development of the delay locked loop (DLL) in the late 1990s so that MTI DRAM products could transition to the DDR memory protocol, used in mobile and non-mobile (server, desktop, cell phones, tablets, etc.) computing systems as main computer memory, for addressing and controlling accesses to memory via interprocess communications (IPC) with the memory controller (MC). I provided technical assistance with MTI's acquisition of Photobit during 2001 and 2002, including transitioning the manufacture of CIS products into MTI's process technology. Further, I did consulting work at Sun Microsystems and then Oracle on the design of memory modules during 2009 and 2010. This work entailed the design of low-power, high-speed, and wide interconnection methods with the goal of transmitting data to/from the memory module and the MC at higher speeds.

12. I have extensive experience in the development of instrumentation and commercial products in a multitude of areas including: integrated electrical/biological circuits and systems, array (memory, imagers, and displays) circuit design, CMOS analog and digital circuit design, diagnostic electrical and electro-optic instrumentation for scientific research, CAD tool development and online tutorials, low-power interconnect and packaging techniques, design of communication/interface circuits (to meet commercial standards such as USB, firewire, DDR, PCIe, SPI, etc.), circuit design for the use and storage of renewable

energy, and power electronics. For example, a part of my research at Boise State, for many years, focused on the use of Thru-Silicon-Vias (TSVs), aka Thru-Wafer Vias (TWVs), for high-density packaging. These packaging techniques were utilized in the memory module development work I did with Sun Microsystems and Oracle. As another example, I designed circuitry for use in implementing Universal Serial Bus (USB) interface circuits while I did consulting at Tower Semiconductor. I designed PCI communication circuits for IPC between a Graphics Processor Unit (GPU) and memory while consulting for Rendition, Inc.

13. My current research work is focused in part on the design of integrated circuits for wireless sensing using LIDAR (LIght Detection And Ranging). I have worked with several companies in the development of these circuits and systems including Freedom Photonics, Aerius Photonics, and FLIR. In the early 1990s, I worked on wireless systems for wideband impulse radar while at Lawrence Livermore Laboratory. Further, part of my research for several years focused on the digitization of IQ channels using delta-sigma modulation. The knowledge and experience gained from this effort are reflected in my textbook CMOS Mixed-Signal Circuit Design and a presentation, which I have presented at several universities and companies, http://cmosedu.com/jbaker/papers/talks/BP_DSM_talk.pdf.

B. Academic Experience

14. I was an adjunct faculty member in the Electrical Engineering departments of UNLV and UNR from 1991-1993. From 1993 to 2000, I served on the faculty at the University of Idaho as an Assistant Professor and then as a tenured Associate Professor of Electrical Engineering. In 2000, I joined a new Electrical and Computer Engineering program at Boise State University (“BSU”), where I served as department chair from 2004 to 2007. At BSU, I helped establish graduate programs in Electrical and Computer Engineering including, in 2006, the university’s second Ph.D. degree. In 2012, I re-joined the faculty at UNLV. Over the course of my career as a professor, I have advised more than 100 masters and doctoral students.

15. I have been recognized for my contributions as an educator in the field. While at Boise State University, I received the President’s Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001). In 2007, I received the Frederick Emmons Terman Award (the “Father of Silicon Valley”). The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator’s contributions to the profession. In 2011, I received the IEEE Circuits and Systems Education Award. I received the

Tau Beta Pi Outstanding Electrical and Computer Engineering Professor Award every year it was awarded while I have been back at UNLV.

16. I have authored several books and papers in the electrical and computer engineering area. My published books include CMOS Circuit Design, Layout, and Simulation (Baker, R.J., Wiley-IEEE, ISBN: 9781119481515 (4th ed., 2019)) and CMOS Mixed-Signal Circuit Design (Baker, R.J., Wiley-IEEE, ISBN: 9780470290262 (2nd ed., 2009) and ISBN: 9780471227540 (1st ed., 2002)). I co-authored DRAM Circuit Design: Fundamental and High-Speed Topics (Keeth, B., Baker, R.J., Johnson, B., and Lin, F., Wiley-IEEE, ISBN: 9780470184752 (2008)), DRAM Circuit Design: A Tutorial (Keeth, B. and Baker, R.J., Wiley-IEEE, ISBN: 0-7803-6014-1 (2001)), and CMOS Circuit Design, Layout and Simulation (Baker, R.J., Li, H.W., and Boyce, D.E., Wiley - IEEE, ISBN: 9780780334168 (1998)). I contributed as an editor and co-author on several other electrical and computer engineering books.

C. Other Relevant Experience

17. I have performed technical and expert witness consulting for more than 200 companies and their subsidiaries and given more than 50 invited talks at conferences, companies, and universities. Further, I am the author or co-author of more than 100 papers and presentations in the areas of electrical and computer engineering design, fabrication, and packaging.

18. I currently serve, or have served, as a volunteer on the IEEE Press Editorial Board (1999-2004); as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018); as the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015); on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016); as a Distinguished Lecturer for the SSCS (2012-2015); the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for IEEE Solid-State Circuits Magazine; IEEE Kirchhoff Award Committee (2020-2023); and advisor for the student branch of the IEEE at UNLV (2013-present). These meetings, groups, and publications are intended to allow researchers to share and coordinate research. My active participation in these meetings, groups, and publications allowed me to see what other researchers in the field have been doing.

19. In addition to the above, I am an IEEE Fellow for contributions to semiconductor memory design and a member of the honor societies Eta Kappa Nu and Tau Beta Pi.

III. MATERIALS CONSIDERED

20. The analysis that I provide in this declaration is based on my education, research, experience, and professional judgment, as well as the documents I have considered, including the '825 Patent (EX1001) and its prosecution history

(EX1003). I have reviewed and am familiar with the specification of the '825 Patent.

I have reviewed and am familiar with the file history of the '825 Patent.

21. In preparing this declaration, I have also reviewed and am familiar with the following prior art used in the Petition and in my declaration below:

Exhibit 1004 – U.S. Patent Application Publication No. 2003/0142121 by Rosen (“*Rosen*”) was filed on January 30, 2002 and published on July 31, 2003, which is more than one year before the June 24, 2004 filing date of the '825 Patent. I understand from counsel for Petitioner that *Rosen* qualifies as prior art under at least pre-AIA 35 U.S.C. §§ 102(a) and (b).

Exhibit 1005 – U.S. Patent No. 4,799,176 by Cacciatore (“*Cacciatore*”) was filed on December 29, 1986 and issued January 17, 1989, which is more than one year before the June 24, 2004 filing date of the '825 Patent. I understand from counsel for Petitioner that *Cacciatore* qualifies as prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b) and (e).

Exhibit 1006 – Japanese Patent Application Publication No. 2740118B2 by Shigeaki et al. (“*Shigeaki*”) was filed on December 1, 1993 and published on June 16, 1995, more than one year before the June 24, 2004 priority date of the '825 Patent. I understand from counsel for Petitioner that *Shigeaki* qualifies as prior art under at least pre-AIA 35 U.S.C. §§ 102(a) and (b).

Exhibit 1007 – U.S. Patent Application Publication No. 2003/0121652 by Carey et al. (“*Carey*”) was filed on February 18, 2003 and published July 3, 2003, nearly a year before the June 24, 2004 priority date of the ’825 Patent. I understand from counsel for Petitioner that *Carey* qualifies as prior art under at least pre-AIA 35 U.S.C. § 102(a).

Exhibit 1008 – U.S. Patent Application Publication No. 2003/0034898 by Shamoon et al. (“*Shamoon*”) was filed on November 13, 2001 and published on February 20, 2003, more than one year before the June 24, 2004 priority date of the ’825 Patent. I understand from counsel for Petitioner that *Shamoon* qualifies as prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b) and (e).

Exhibit 1009 – U.S. Patent No. 5,460,327 by Hill (“*Hill*”) was filed on July 1, 1994 and issued October 24, 1995, which is more than one year before the June 24, 2004 filing date of the ’825 Patent. I understand from counsel for Petitioner that *Hill* qualifies as prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b) and (e).

Exhibit 1010 – U.S. Patent No. 7,133,739 by Williamson et al. (“*Williamson*”) was filed on May 2, 2003 and published on March 25, 2004. I understand from counsel for Petitioner that *Williamson* qualifies as prior art under at least pre-AIA 35 U.S.C. §§ 102(a) and (e).

Exhibit 1011 – U.S. Patent No. 5,181,653 by Foster et al. (“*Foster*”) was filed on March 3, 1992 and published on January 26, 1993, which is more than one year before the June 24, 2004 filing date of the ’825 Patent. I understand from counsel for Petitioner that *Foster* qualifies as prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b) and (e).

Exhibit 1012 – U.S. Patent No. 6,318,639 by Toth (“*Toth*”) was filed on October 15, 1999 and published on November 20, 2001, which is more than one year before the June 24, 2004 filing date of the ’825 Patent. I understand from counsel for Petitioner that *Toth* qualifies as prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b) and (e).

Exhibit 1018 – International Publication No. WO 03/040839 by Geiwitz (“*Geiwitz*”) was filed on October 22, 2002 and published on May 15, 2003, which is more than one year before the June 24, 2004 filing date of the ’825 Patent. I understand from counsel for Petitioner that *Geiwitz* qualifies as prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b) and (e).

Exhibit 1019 – U.S. Patent No. 5,541,586 by Wise (“*Wise*”) was filed on December 22, 1994 and published on July 30, 1996, which is more than one year before the June 24, 2004 filing date of the ’825 Patent. I understand from counsel for Petitioner that *Wise* qualifies as prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b) and (e).

Exhibit 1020 – A Taxonomy of Internet Appliances by Gillett et al. (“*Gillett*”) was prepared for the Telecommunications Policy Research Conference in Alexandria, Virginia in September of 2000, which is more than one year before the June 24, 2004 filing date of the ’825 Patent. I understand from counsel for Petitioner that *Gillett* qualifies as prior art under at least pre-AIA 35 U.S.C. §§ 102(a) and (b).

Exhibit 1021 – U.S. Patent No. 6,593,766 by Aisa (“*Aisa*”) was filed on October 8, 1999 and published on July 15, 2003, nearly one year before the June 24, 2004 filing date of the ’825 Patent. I understand from counsel for Petitioner that *Aisa* qualifies as prior art under at least pre-AIA 35 U.S.C. §§ 102(a) and (e).

22. I have considered the following documents in my analysis below:

Exhibit No. ¹	Description
1001	U.S. Patent No. 7,185,825 (“’825 Patent”)
1003	Prosecution File History of the ’825 Patent

¹ Citations to issued patents (Exhibits 1001, 1005, 1006, 1009, 1010, 1011, 1012, 1019 and 1021) are made by column and line number. Citations to patent application publications (Exhibits 1004, 1007 and 1008) are made by paragraph number. Citations to Exhibits 1013 and 1018 are made by page and line number. Citations to Exhibits 1003, 1014, 1015, 1016, 1017, 1020, 1022, 1023, 1024, 1025, 1026 and 1027 are made by page number.

Exhibit No.¹	Description
1004	U.S. Patent Publication No. 2003/0142121 (“ <i>Rosen</i> ”)
1005	U.S. Patent No. 4,799,176 (“ <i>Cacciatore</i> ”)
1006	Certified Translation of Japanese Patent No. JP2740118B2 (“ <i>Shigeaki</i> ”)
1007	U.S. Patent Publication No. 2003/0121652 (“ <i>Carey</i> ”)
1008	U.S. Patent Publication No. 2003/0034898 (“ <i>Shamoon</i> ”)
1009	U.S. Patent No. 5,460,327 (“ <i>Hill</i> ”)
1010	U.S. Patent No. 7,133,739 (“ <i>Williamson</i> ”)
1011	U.S. Patent No. 5,181,653 (“ <i>Foster</i> ”)
1012	U.S. Patent No. 6,318,639 (“ <i>Toth</i> ”)
1013	Transcript of Deposition of Howard J. Rosen
1014	Plaintiff’s Proposed Claim Constructions, <i>Rosen Technologies LLC v. Lennox Industries, Inc.</i> , No. 3:22-cv-00732-K (N.D. Tex. Feb. 2, 2023)
1015	Defendant’s Disclosure of Claim Constructions Extrinsic Evidence, <i>Rosen Technologies LLC v. Lennox Industries, Inc.</i> , No. 3:22-cv-00732-K (N.D. Tex. Feb. 2, 2023)
1016	Scheduling Order, <i>Rosen Technologies LLC v. Lennox Industries, Inc.</i> , No. 3:22-cv-00732-K (N.D. Tex. Sept. 1, 2022)
1017	Joint Claim Construction and Prehearing Statement, <i>Rosen Technologies LLC v. Lennox Industries, Inc.</i> , No. 3:22-cv-00732-K (N.D. Tex. Feb. 23, 2023)
1018	International Publication No. WO 03/040839 (“ <i>Geiwitz</i> ”)
1019	U.S. Patent No. 5,541,586 (“ <i>Wise</i> ”)
1020	A Taxonomy of Internet Appliances (“ <i>Gillett</i> ”)
1021	U.S. Patent No. 6,593,766 (“ <i>Aisa</i> ”)
1022	Electronic Order Granting Unopposed Motion to Amend Scheduling Order, <i>Rosen Technologies LLC v. Lennox Industries, Inc.</i> , No. 3:22-cv-00732-K (N.D. Tex. March 13, 2023)
1023	Statutory Disclaimer and Related Documents filed in U.S. Patent No. 6,824,069 on February 22, 2005
1024	Network Time Protocol (NTP), https://www.rfc-editor.org/rfc/rfc958 , D.L. Mills (September 1985)
1025	S3C8248 Data Sheet, Samsung (Excerpted)
1026	Webster's Dictionary of Computer Terms, Bryan Pfaffenberger, 8th ed. (2000) (Excerpted)

Exhibit No.¹	Description
1027	Random House Webster's Computer & Internet Dictionary, Phillip E. Margolis, 3rd ed. (1999) (Excerpted)

IV. UNDERSTANDING OF APPLICABLE LEGAL STANDARDS

23. Although I am not an attorney, I have a general understanding of the applicable legal standards pertaining to the patentability issues presented in this proceeding. My understanding of legal principles as described in this section is based on communication of those principles to me by Petitioner's legal counsel. The analysis in this declaration is in accordance with the legal principles outlined below.

24. I understand that, in this *inter partes* review, Petitioner has the burden of proving that each challenged claim is unpatentable by a preponderance of the evidence.

A. My Understanding of Claim Construction

25. I have been informed by counsel that a purpose of claim construction is to determine what a person of ordinary skill in the art ("POSITA") would have understood the claim terms to mean. I understand that during an IPR proceeding, claims are to be construed in light of the specification as would be read by a POSITA at the time the application was filed. I understand that claim terms are given their ordinary and customary meaning as would be understood by a POSITA in the context of the entire disclosure. A claim term, however, will not receive its ordinary meaning if the patentee acted as his own lexicographer and clearly set forth a

definition of the claim term in the specification. In this case, the claim term will receive the definition set forth in the patent.

26. I understand that the prosecution history can inform the meaning of the claim language by demonstrating how the inventors understood the invention and whether the inventors limited the invention in the course of prosecution, making the claim scope narrower than it otherwise would be. I understand that extrinsic evidence may also be consulted in construing the claim terms, such as dictionary definitions and expert testimony.

27. I further understand that 35 U.S.C. § 112 ¶6 created an exception to the general rule of claim construction. I understand that patent claims may be drafted in means-plus-function format, in which a claim limitation is expressed as a means or step for performing a specified function, without a recital of structure. I understand that, under § 112 ¶6, a limitation will be presumed to be a “means-plus-function” limitation if (a) the claim limitation uses the word “means”; (b) the word “means” is modified by functional language; and (c) the word “means” is not modified by sufficient structure for achieving the specified function.

28. I understand that a means-plus-function limitation should be interpreted to cover only the recited function and the corresponding structure for performing the function as described in the specification, as well as equivalent structures. I understand that a structure is deemed equivalent to the corresponding structure in

the specification only if the difference between them is insubstantial. For example, two structures may be deemed equivalent if they perform the same function in substantially the same way to achieve substantially the same result. I further understand that a structural equivalent must have been available at the time of issuance of the claim.

B. My Understanding of Obviousness

29. I understand that a patent claim is unpatentable if, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of the prior art to yield the patent claim. I also understand that it is not required (although it is acceptable) that each element of a patent claim be found in a single reference in order to find a patent claim obvious. This means that even if all of the requirements of the claim cannot be found in a single prior art reference that would anticipate the claim, the claim can still be invalid. For a patent claim to be found obvious, all the elements of the patent claim may be found in a combination of references at which a POSITA would have been reasonable expected to arrive.

30. I understand that the following factors should be considered in analyzing obviousness: (1) the scope and content of the prior art; (2) the differences between the prior art and the claims; (3) the level of ordinary skill in the pertinent art; and (4) other objective considerations identified below. I understand that an invention is obvious when the differences between the subject matter sought to be

patented and the prior art are such that the subject matter as a whole would have been obvious to a POSITA at the time the invention was made.

31. I understand that a showing of obviousness requires some articulated reasoning with a rational underpinning to support the combination of references. I understand that in consideration of the issue of obviousness it is important to identify whether a reason existed at the time of the invention that would have led a person of ordinary skill in the pertinent art to combine elements of the references in a way that yields the claimed invention.

32. I understand that a POSITA is assumed to have knowledge of all prior art references. I also understand that when considering the obviousness of a patent claim, one may consider whether a teaching, suggestion, or motivation to combine the references exists so as to avoid impermissibly applying hindsight when considering the prior art. I understand this test should not be rigidly applied, but that the test can be important to avoiding such hindsight.

33. I understand that a POSITA can combine various prior art references based on the teachings of those prior art references, the general knowledge present in the art, or common sense. I understand that a motivation to combine the references may be implicit in the prior art, and there is no requirement that there be an actual or explicit teaching to combine two references. Thus, one may take into account the inferences and creative steps that a POSITA would employ to combine the known

elements in the prior art in the manner claimed by the patent-at-issue. I understand that one should avoid “hindsight bias” and ex post reasoning in performing an obviousness analysis. This does not mean, however, that a POSITA does not have recourse to common sense for purposes of the obviousness inquiry.

34. I understand that a claim may be considered unpatentable for obviousness for various reasons. I have been informed that the following exemplary rationales may support a finding of obviousness:

- A) combining prior art elements according to known methods to yield predictable results;
- B) simply substituting one known element for another to obtain predictable results;
- C) use of a known technique to improve similar devices (methods, or products) in the same way;
- D) applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;
- E) choosing from a finite number of identified, predictable solutions with a reasonable expectation of success;
- F) a predictable variation of work in the same or a different field of endeavor, which a POSITA would be able to implement;

G) if, at the time of the alleged invention, there existed a known problem for which there was an obvious solution encompassed by the patent's claim;

H) known work in one field of endeavor that prompts variations of it for use in either the same field or a different field based on technological incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art; and/or

I) some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior-art reference or to combine multiple prior-art references or teachings to arrive at the claimed invention.

35. I understand that even if a prima facie case of obviousness is established, the final determination of obviousness must also consider objective indicia of nonobviousness, which I understand are also referred to as "secondary considerations," if presented. I understand that these objective indicia can be important evidence as to whether a patent is obvious or nonobvious. Such secondary considerations include: (1) commercial success of products covered by the patent claims; (2) a long-felt but unsolved need for the invention; (3) failed attempts by others to make the invention; (4) copying of the invention by others in the field; (5) unexpected results achieved by the invention as compared to the closest prior art; (6) praise of the invention by the infringer or others in the field; (7) the taking of licenses under the patent by others; (8) expressions of surprise by experts and those skilled

in the art at the making of the invention; and (9) the patentee proceeded contrary to the accepted wisdom of the prior art. I further understand that secondary considerations evidence is only relevant if the offering party establishes a connection, or nexus, between the evidence and the claimed invention.

36. I also understand that “obviousness” is a legal conclusion based on the underlying factual issues of the scope and content of the prior art, the differences between the claimed invention and the prior art, the level of ordinary skill in the prior art, and any objective indicia of non-obviousness. For that reason, I am not rendering a legal opinion on the ultimate legal question of obviousness. Rather, my testimony addresses the underlying facts and factual analysis that would support a legal conclusion of obviousness, and when I use the term obvious, I am referring to the perspective of a POSITA at the time of invention.

C. Level of Ordinary Skill in the Art

37. I understand that an assessment of the claims of the '825 Patent should be undertaken from the perspective of a POSITA as of the earliest claimed priority date. I understand that a POSITA is presumed to be aware of all pertinent art, thinks with conventional wisdom in the art, and is a person of ordinary creativity—not an automaton.

38. I understand that to determine the appropriate level of a POSITA, the following factors may be considered: (1) the types of problems encountered by those

working in the field and prior art solutions thereto; (2) the sophistication of the technology in question, and the rapidity with which innovations occur in the field; (3) the educational level of active workers in the field; and (4) the educational level of the inventor.

D. Priority Date

39. I understand that, subject to the next paragraph, the asserted “priority date” of a patent is the earlier of: (a) the date on which a patent application is filed; or (b) the date on which an earlier-filed patent application is filed if the patentee claims the benefit of priority to that earlier-filed patent application.

40. I understand that it is not enough for a patent to merely claim the benefit of an earlier-filed application, but that additional criteria must be met. In particular, the prior application itself must describe the claimed invention, and must do so in sufficient detail that one skilled in the art can clearly conclude that the inventor invented the claimed invention as of the filing date sought. First, I understand that a priority-date analysis is on a claim-by-claim basis. Second, I understand that, in order for a patent claim to be entitled to the filing date of an earlier patent application, a “Section 112 analysis” must be conducted. I am informed that a “Section 112” analysis encompasses looking to the earlier patent application, and ascertaining whether that earlier patent application meets both the written-description and enablement requirements as of the filing date of the earlier application. I understand

that it is not enough that the claim would have been obvious from the earlier application, but that application itself must describe the claimed invention.

41. I understand that in order to satisfy the written description requirement the earlier application must reasonably convey to those skilled in the art that the inventors had possession of the subject matter of the patent as of the filing date of the earlier application. I have been informed that it is the disclosures of the earlier patent application that count, and that while the meaning of terms, phrases, or diagrams in the earlier patent application must be interpreted from the vantage point of one skilled in the art, all of the claimed limitations must appear in the specification. Further, I understand that this analysis is not a question of whether one skilled in the art might be able to construct the claimed invention from the teachings of the disclosure. The question is not whether a claimed invention is an obvious variant of that which is disclosed in the specification; rather, I understand that an earlier application must itself describe each of the claim limitations.

42. I also understand that in order to satisfy the enablement requirement, the earlier application must enable a person of ordinary skill in the art to practice the claimed invention without undue experimentation.

V. OVERVIEW OF THE '825 PATENT

43. I have reviewed the '825 Patent, which is entitled "Programmable Thermostat Employing A Fail Safe Real Time Clock." EX1001, Cover. I

understand that the '825 Patent was filed on June 24, 2004. As I describe in more detail below in Section V.D, I also understand that the '825 Patent originally claimed priority as a continuation-in-part of Application No. 10/060,768, filed on January 30, 2002, now U.S. Patent No. 6,824,069, but it is nonetheless not entitled to a priority date any earlier than June 24, 2004 due to disclaimer by the applicant. *Infra*, § V.D.

A. Subject Matter

44. The '825 Patent describes and claims a programmable thermostat system for controlling space conditioning equipment. EX1001, Abstract. More particularly, the '825 Patent relates to “a programmable thermostat incorporating a fail safe real time clock and which does not require battery or other backup device in case of a power failure.” *Id.*, 1:8-10.

45. The claimed thermostat system includes conventional components such as a temperature sensor, a touch screen for interactive interface with a user, a processor including a central processing unit, real time clock, memory, and input/output unit, and a control program. *Id.*, 3:62-4:36. The “Background of the Invention” section of the '825 Patent confirms that these components were well known by the time the '825 Patent was filed. For instance, the '825 Patent acknowledges that “[t]hermostats have been used for many years as a temperature sensitive switch which controls heating and/or cooling equipment for conditioning a

space[.]” EX1001, 1:14-16. The ’825 Patent admits that “[m]any modern thermostat systems include a real time clock, a memory and a data processor to run a process control program stored in the memory to accurately measure the temperature of a temperature sensor disposed in the conditioned space and to send signals to the heating and/or cooling equipment to closely control the temperature of the conditioned space.” *Id.*, 1:29-35. Additionally, the ’825 Patent itself admits that “[m]ost [] modern thermostats are programmable by a user. Typically, a programmable thermostat incorporates a tactile user interface with various buttons ... to be touched.” *Id.*, 1:43-46. In addition, Figure 1 of the Patent, which contains nearly all the hardware elements of Claims 1 and 11, is labeled as “prior art” and described as such. *Id.*, 3:54-57, 4:9-5:17. Thus, the ’825 Patent teaches that the majority of the elements of its thermostat system were well known in the art and in use in modern thermostat systems before the priority date of the ’825 Patent.

46. The ’825 Patent purports to address problems with existing programmable thermostat systems, namely, maintaining time and date information in the event of power failures. *Id.*, 2:18-60. According to the patent, the ’825 Patent eliminates “the need for providing a backup power source” such as a battery or supercapacitor, for a thermostat. EX1001, Abstract, 2:18-22, 2:37-40. The ’825 Patent describes that “[m]ost commonly, power to a programmable thermostat is supplied from the controlled space conditioning equipment, and either a battery or

very high capacity capacitor (‘supercap’) provides backup power to ‘ride out’ equipment power failure (‘outage’) until power is restored.” *Id.*, 2:18-22. According to the ’825 Patent, this “can have drastic consequences and, at best, can be a significant inconvenience.” *Id.*, 2:37-40. Thus, according to the ’825 Patent, “it would be highly desirable to provide a fail safe real time clock in a programmable clock, particularly a thermostat incorporating a vacation mode of operation.” *Id.*, 2:57-60.

47. The ’825 Patent purports to have invented “a programmable thermostat incorporating a fail safe real time clock and which does not require battery or other backup device in case of a power failure.” *Id.*, 1:8-10. Three options are provided for handling the real time clock in case of a power outage. First, the ’825 Patent “provide[s] a thermostat having a real time clock and a non-volatile random access memory in which the current time and date are periodically read from the real time clock into the random access memory such that, in the event of an outage, the last time and date previously stored is recovered from the non-volatile random access memory upon the restoration of power to reset the real time clock in anticipation of resuming operation in the mode running at the time of the outage.” *Id.*, 3:1-9. This concept was taught by the prior art. EX1006.

48. The ’825 Patent explains that a second option is that the system “normally keep[s], and resume[s] after an outage, precision time from a suitable

source such as WWVB.” EX1001, 6:26-28. WWVB concerns a time signal that has been broadcast using radio waves since the 1960s. This concept was known in the prior art. EX1007. A third option is also disclosed. Time can be retrieved via the Internet and stored in the clock of the thermostat. EX1001, 6:33-38. This concept was well known in the prior art. *See also* EX1020, 9 n.10 (“A very different segment of the media coverage of ‘Internet appliances’ concerns the notion of connecting traditional household appliances . . . to the Internet. . . . Some of these concepts make sense (e.g. connecting thermostats so you can program them through a Web site, not to have to reset time when power blinks, perform remote diagnostics on large appliances, etc.)”).

49. Figure 1 of the '825 Patent “is a block diagram of an exemplary space conditioning system incorporating a thermostat with backup power, in case of an outage, supplied from a battery or supercap in accordance with the prior art.” *Id.*, 3:54-56. The thermostat system includes admittedly conventional components including “a processor 1, a touch screen 2 and a temperature sensor 5 which is disposed in a conditioned space 4.” *Id.*, 4:10-11. The processor includes “a central processing unit (CPU) 9 in communication with a memory 8 for storing data and program information and also, via an input/output unit (I/O unit) 10, a touch pad 11 and a liquid crystal display (LCD) 12.” *Id.*, 4:22-26. “A settable real time clock 13 is used to keep time in the thermostat system to facilitate diverse operations.” *Id.*,

4:29-30. Additionally, “[i]n accordance with the prior art, power to the processor 1 is conventionally supplied from the space conditioning equipment 3 via a line 30 through an isolation diode 33.” *Id.*, 5:3-5.

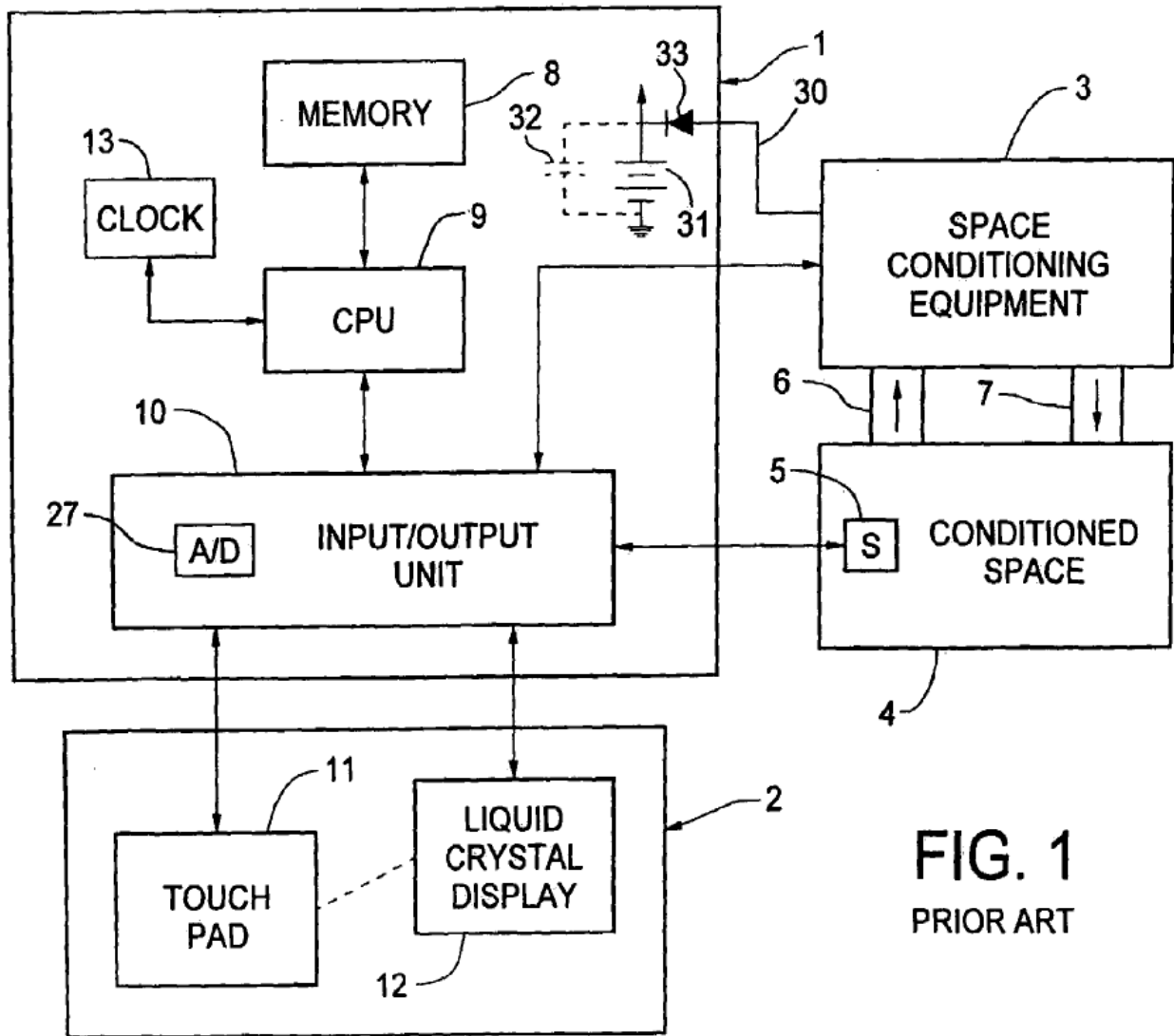


FIG. 1
PRIOR ART

Id., Figure 1. As seen in Figure 1 above, the '825 Patent admittedly contains hardware elements that are common in the prior art. *Id.*, Figure 1.

50. Figure 2 illustrates “a block diagram of a portion of the processor component of the thermostat particularly showing aspects of the thermostat clock

and its support circuitry in a first exemplary embodiment of the invention.” *Id.*, 3:58-61.

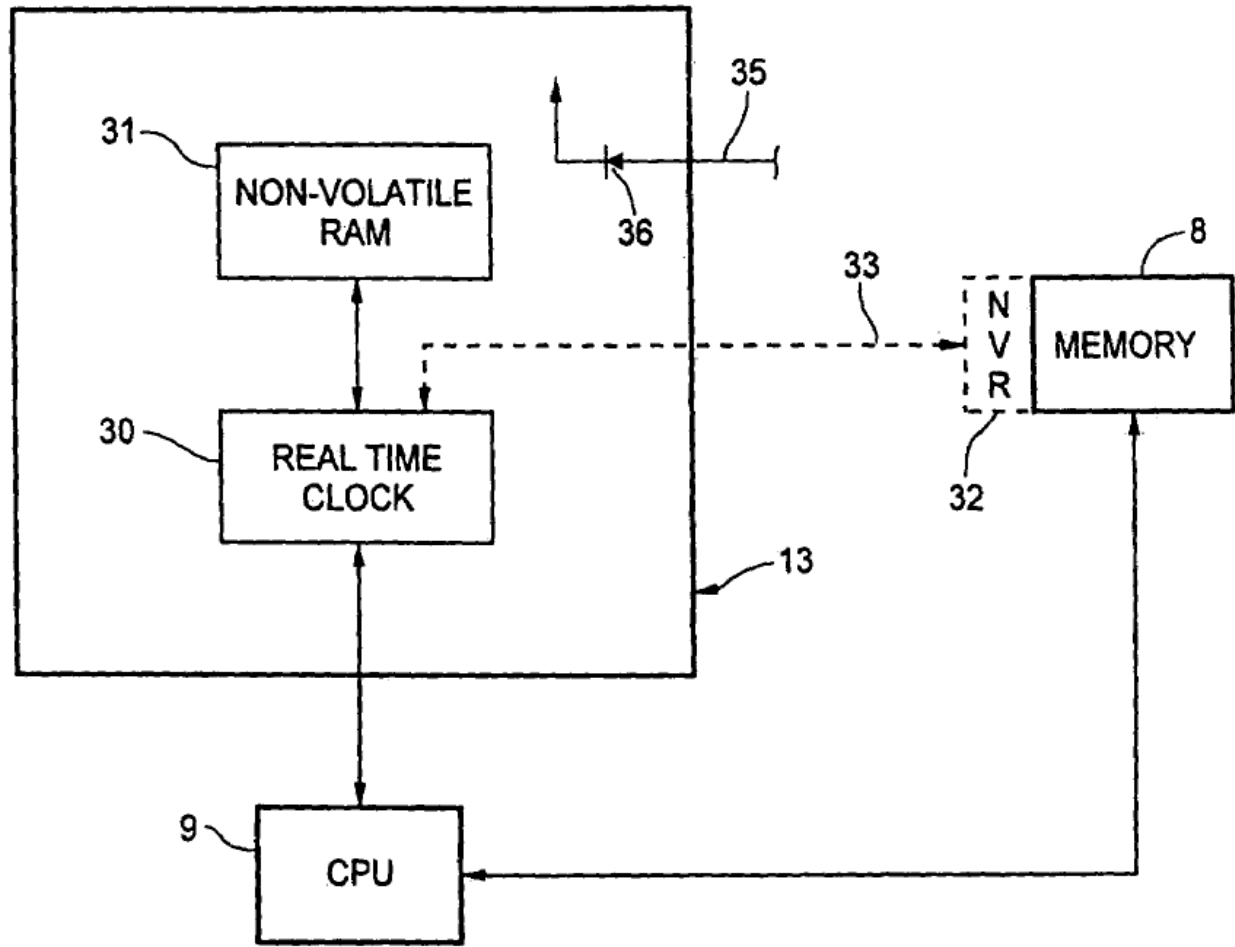


FIG. 2

Id., Figure 2.

51. The '825 Patent system “normally keep[s], and resume[s] after an outage, precision time from a suitable source such as WWVB.” *Id.*, 6:26-28. The '825 Patent also discloses that precision time can be retrieved via the Internet. *Id.*

6:33-38. Figure 5 illustrates “a block diagram of a portion of the processor component of the thermostat particularly showing aspects of the real time clock and its support circuitry in a second exemplary embodiment of the invention.” *Id.*, 4:3-4.

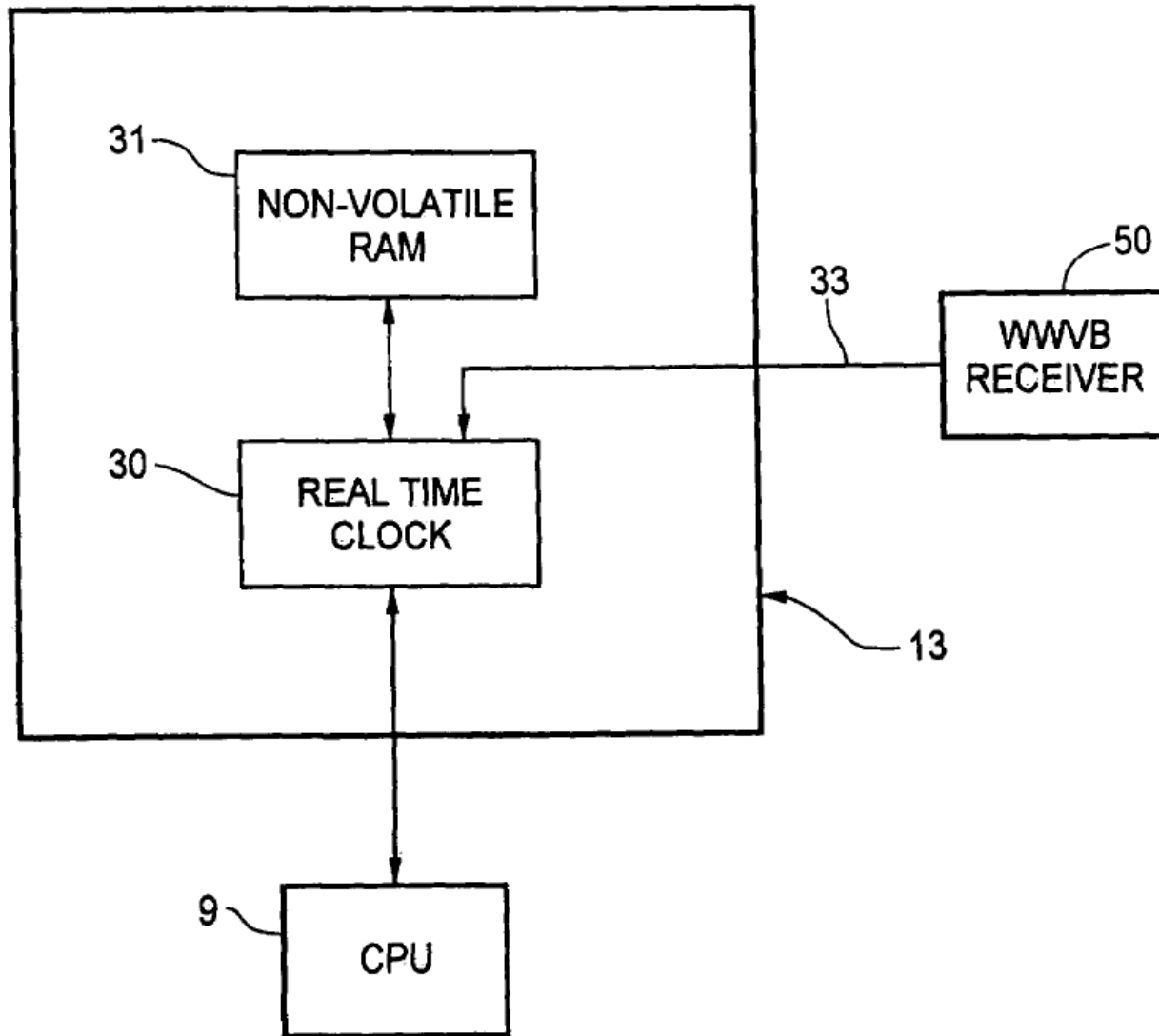


FIG. 5

Id., Figure 5.

52. The '825 Patent further discloses a vacation mode of operation. EX1001, Claim 4. The purpose of vacation mode is to: “maintain the temperature of a conditioned space which will be unoccupied for a period at a value which will substantially lower the cost of energy to heat/cool the conditioned space but which ensures that the temperature will not fall into a range at which damage to the premises, for example, freezing pipes, will occur.” *Id.*, 1:54-60. As the '825 Patent itself admits, “[t]he operation of programmable thermostats in the vacation mode is straightforward and well known.” *Id.*, 1:60-61. Vacation mode is well known in the art. *See e.g.*, EX1004; EX1012; EX1013.

B. Listing of Challenged Claims

53. Below I provide a listing of Claims 1, 4 and 11-16 of the '825 Patent. I will refer throughout this declaration to the elements of the claims with reference to the number and letter designations that have been added in the left column (e.g., “1[pre],” “1[a],” “1[b],” etc.).

Claim 1	
1[Pre]	A programmable thermostat for controlling space conditioning equipment comprising:
1[a]	A) means coupling suitable power for energizing said thermostat from said space conditioning equipment to said thermostat;
1[b]	B) an interactive interface for a user to enter programming information into said thermostat;

1[c]	C) a temperature sensor for providing an electrical signal indicative of the temperature of a conditioned space in which the temperature sensor is situated;
1[d]	D) a processor, said processor including:
1[e]	1) a central processing unit;
1[f]	2) a first memory coupled to said central processing unit for storing program and data information; and
1[g]	3) an input/output unit including:
1[h]	a) a sensor input coupled to said temperature sensor for receiving said electrical signal therefrom; and
1[i]	b) a control output coupled to the space conditioning equipment for issuing control signals thereto;
1[j]	4) a real time clock;
1[k]	5) a non-volatile random access memory; and
1[l]	6) a control program stored in said first memory directing:
1[m]	a) said real time clock to periodically read its current time and date information into said non-volatile memory; and
1[n]	b) upon restart after a loss and then return of power from said space conditioning equipment, read the time and date information stored in said non-volatile memory into said real time clock.
Claim 4	
4	The thermostat of claim 1 which includes a vacation mode of operation.
Claim 11	
11[pre]	A programmable thermostat for controlling space conditioning equipment comprising:
11[a]	A) means coupling suitable power for energizing said thermostat from said space conditioning equipment to said thermostat;

11[b]	B) an interactive interface for a user to enter programming information into said thermostat;
11[c]	C) a temperature sensor for providing an electrical signal indicative of the temperature of a conditioned space in which the temperature sensor is situated;
11[d]	D) a processor, said processor including:
11[e]	1) a central processing unit;
11[f]	2) a first memory coupled to said central processing unit for storing program and data information; and
11[g]	3) an input/output unit including:
11[h]	a) a sensor input coupled to said temperature sensor for receiving said electrical signal therefrom; and
11[i]	b) a control output coupled to the space conditioning equipment for issuing control signals thereto;
11[j]	4) a real time clock; and
11[k]	5) a receiver adapted to receive current time and date information from an external source of the current time and date, said receiver being coupled to said real time clock such that the time and date information thereof is updated from said receiver.
Claim 12	
12	The thermostat of claim 11 in which said receiver receives wireless signals from said external source.
Claim 13	
13	The thermostat of claim 12 which includes a vacation mode of operation.
Claim 14	
14	The thermostat of claim 11 in which said receiver receives signals via the Internet from said external source.

Claim 15	
15	The thermostat of claim 14 which includes a vacation mode of operation.
Claim 16	
16	The thermostat of claim 11 which includes a vacation mode of operation.

C. Prosecution History

54. The '825 Patent was filed as Application No. 10/875,579 on June 24, 2004. EX1001, Cover. The '825 Patent originally claimed priority as a continuation-in-part of Application No. 10/060,768, filed on January 30, 2002, now U.S. Patent No. 6,824,069. *Id.*

55. After the application was filed, the applicant submitted a preliminary amendment on February 7, 2005 disclaiming priority to Application No. 10/060,768, filed on January 30, 2002, now U.S. Patent No. 6,824,069 (the "'069 Patent"). EX1003, 58. Remarks accompanying the disclaimer explained that the applicant was disclaiming the '825 Patent's benefit of the '069 Patent's earlier filing date because the applicant had disclaimed all claims of the '069 Patent for its entire term. *Id.*, 60 ("Applicant hereby disclaims for the present application the benefit of the earlier filing date of Serial No. 10/060,768 pursuant to 35 USC § 120 and accepts as the filing date of this application that date on which the application was actually filed with the USPTO, i.e., the filing date indicated above with this application's information. All the claims of US Patent No. 6,824,069 are being disclaimed by the

Applicant for the entire term of that patent. Applicant seeks to sever all connection between US Patent No. 6,824,069 and the present application.”).

56. The prosecution history for the '825 Patent is minimal. The USPTO issued a non-final rejection based on §§ 102 and 103 on March 29, 2006. *Id.*, 41-45. Claims 1 and 3 were rejected under § 102 (b) based on U.S. Patent No. 4,431,134 by Hendricks (“*Hendricks*”), and Claims 2 and 4 were rejected under § 103 based on *Hendricks* as well. The applicant submitted a response on June 28, 2006 alleging that the non-volatile memory aspect of the claims was a non-obvious point of novelty over the art of record. *Id.*, 32-36.

57. A Notice of Allowance and Fee(s) Due was mailed on November 21, 2006. *Id.*, 19-21. As can be seen from the face of the '825 Patent, the Examiner cited only fourteen references (eleven of which were identified by the applicant in an information disclosure statement). EX1001, Cover; EX1003, 63-65, 171-172. Most of the prior art references relied upon in Grounds 1-9 were not considered by the Examiner during prosecution of the '825 Patent.

D. Priority Date

58. As discussed above, the '825 Patent originally claimed priority as a continuation-in-part of Application No. 10/060,768, filed on January 30, 2002, now the '069 Patent. EX1003, 149. However, the '825 Patent is **not** entitled to a priority date any earlier than its filing date, June 24, 2004. *See*, EX1001, Cover.

59. A preliminary amendment was entered during prosecution of the '825 Patent disclaiming the benefit of the earlier filing date of the '069 Patent. EX1003, 58-61. In fact, the applicant of the '825 Patent explicitly sought "to sever all connection between US Patent No. 6,824,069 and the present application." *Id.*, 60. On February 22, 2005, applicant disclaimed all claims of the '069 Patent because "newly-discovered prior art ... appears to fully anticipate the invention disclosed and claimed in the subject patent." EX1023, 2. Thus, the priority date of the '825 Patent, as disclosed on the face of the patent, is the June 24, 2004 filing date. EX1001, Cover.

E. Level of Ordinary Skill in the Art

60. I have been asked to consider the level of ordinary skill in the field that someone would have had at the time the claimed invention was made. My opinions regarding the level of ordinary skill in the art are based on, among other things, my nearly 40 years of experience in the field of electrical engineering and computer science, as well as: the levels of education and experience of persons working in the field, the types of problems encountered in the field; and the sophistication of the technology.

61. Based on the disclosure of the '825 Patent, in my opinion a POSITA as of June 24, 2004 would have had a Bachelor of Science degree in Electrical Engineering or a year or two of experience working with or designing processor-

based systems with network connectivity. This level of skill is approximate, and more experience would compensate for less formal education, and vice versa.

62. Based on my education and experience, I meet this definition of one of ordinary skill in the art, and I believe that I am qualified to provide opinions about how a POSITA at the relevant time would have interpreted and understood the '825 Patent and the prior art relied upon herein. Although my qualifications and experience exceed those of a POSITA, both in June 2004 and today, I have nevertheless applied the perspective of a POSITA in rendering my opinions below.

63. My opinions below explain how a POSITA would have understood the technology described in the '825 Patent and the prior art references I have identified herein around the June 24, 2004 timeframe. For purposes of this declaration, in general, and unless otherwise noted, my testimony below refers to the knowledge of one of ordinary skill in the art during the time period around the priority date of the '825 Patent. I would have been a person with at least ordinary skill in the art at that time.

F. Claim Construction

64. It is my understanding that in order to properly evaluate the '825 Patent, the terms of the claims must first be interpreted. It is my understanding that the claims are to be construed according to the same claim construction standard that district courts use. I have been informed by counsel for Petitioner that the challenged

claims of the '825 Patent are to be given their ordinary and customary meaning as understood by one of ordinary skill in the art at the time of the invention in light of the specification and the prosecution history pertaining to the patent.

65. In order to construe the claims, I have reviewed the entirety of the '825 Patent along with the prosecution history of the '825 Patent. Except as set forth below, it is my opinion that a POSITA would have understood each term of the Challenged Claims according to their plain and ordinary meaning as understood by a person of ordinary skill in the art.

66. I have offered certain claim construction opinions in the context of the NDTX litigation. As explained in the sections that follow, for purposes of this declaration I have been asked to make certain assumptions regarding the meaning of the claim language and provide an opinion as to obviousness based upon those assumptions. While I provide my opinion based upon those assumptions, I am not conceding that my prior opinions are incorrect.

1. Terms Governed by 35 U.S.C. § 112, ¶6

67. The Challenged Claims of the '825 Patent include certain claim elements that recite “means” for performing various functions. Element 1[a] of Claim 1 and element 11[a] of Claim 11 recite a “means coupling suitable power for energizing said thermostat from said space conditioning equipment to said

thermostat.” EX1001, 6:60-62, 8:5-7. I understand from counsel for Petitioner that the use of the word “means” creates a presumption that 35 U.S.C. § 112, ¶6 applies.

68. I understand that in the related NDTX Litigation, Petitioner and Patent Owner agree that element 1[a] of Claim 1 is governed by 35 U.S.C. § 112, ¶6 and further agree on the function of the limitation. EX1017, 61-62. Petitioner has argued in the related district court litigation that the corresponding structure includes both a power line and an isolation diode while Patent Owner contends that only a power line is corresponding structure. EX1017, 61-62. For purposes of this declaration, I have applied the constructions for element 1[a] of Claim 1 and element 11[a] of Claim 11 shown in the table below, without conceding they are correct.

Limitations	Structure and Function
1[a]/11[a]: “means coupling suitable power for energizing said thermostat from said space conditioning equipment to said thermostat”	<u>Function</u> : coupling suitable power for energizing said thermostat from said space conditioning equipment to said thermostat <u>Structure</u> : a (power) line and any equivalents EX1001, Figures 1-2, 2:18-22, 5:3-5, 5:43-47.

EX1017, 61-62. For this claim element, I do not believe it matters whether Petitioner’s or Patent Owner’s claim construction is correct as explained herein.

69. To the extent the Board disagrees with Patent Owner's proposed constructions, in my opinion, the claims of the '825 Patent are still obvious in view of prior art.

2. Additional Terms of the '825 Patent

70. I understand that in the related NDTX Litigation, Patent Owner contends that the claimed "sensor input coupled to said temperature sensor for receiving said electrical signal therefrom" in element 1[h] and "control output coupled to the space conditioning equipment for issuing control signals thereto" in element 1[i] are not subject to 35 U.S.C. § 112, ¶6. EX1017, 66, 72. Petitioner has argued that the "sensor input" and "control output" are indefinite for failing to disclose corresponding structure. EX1017, 66, 72-73. Patent Owner disagrees. See EX1017, 66-73. For purposes of this declaration, I was asked to apply Patent Owner's "plain and ordinary meaning" interpretations. For purposes of this declaration, I have applied Patent Owner's "plain and ordinary meaning" interpretations, without conceding definiteness or that they are correct.

VI. TECHNOLOGY BACKGROUND AND STATE OF THE ART

71. Before providing my analysis of the '825 Patent and the prior art references, as included below, a background discussion of the state of the art of thermostat systems and the technologies they employ is helpful.

A. Use of Nonvolatile Memory

72. The '825 Patent employs a nonvolatile memory for storing the time from the real time clock in case of a power failure. Nonvolatile memory had been used for many years prior to the filing of the '825 Patent for the purpose of storing information that one wanted to retain in the event of a power failure. For example, *Hill* teaches that nonvolatile memory should be used in a thermostat to retain critical information: “The setpoint information as well as mode of operation information and other critical user supplied data is preferably executable from an internal randomly addressable memory within the microprocessor 20. This information is permanently stored on an EEPROM 32. The EEPROM is a nonvolatile memory which retains any data written to it from the microprocessor 20 via a data line 34 and provides such data back to the microprocessor 20 via the same data line 34 in response to a read command.” EX1009, 3:1-10.

73. Multiple references teach the storage of the time data from a real time clock in a nonvolatile memory for use in setting the real time clock after a power failure. For example, *Shigeaki* teaches resetting of a clock in a control circuit for a gas hot-air heater. EX1006, ¶0005. A POSITA would understand that control circuit to be a thermostat. At a minimum, *Shigeaki* suggests to a POSITA the use of a nonvolatile memory in a thermostat like that of *Hill*. As *Shigeaki* explains, “When a power outage occurs, the time data pertaining to the current time is stored in

E²PROM 2, and when power is restored, the time data is read from E²PROM 2, and the time is resumed from the current time corresponding to the retrieved time data.” EX1006, ¶0061.

74. Similarly, *Aisa* discloses using a nonvolatile memory, a EEPROM, in a household appliance. EX1021, 4:62-5:5. The EEPROM may be used to store the “current time value, instant by instant,” as well as “information relating to the appliance Status. *Id.* The clock information stored in the nonvolatile memory is used to restore the time after a power outage. *Id.*, 6:6-11. *Aisa* discloses the use of a virtual clock with a thermostat when it refers to using the described electronics with a “boiler” that normally has a “room temperature sensor.” *Id.*, 6:63-7:2. It also suggests using the virtual clock with an oven having a temperature sensor—another thermostat. *Id.*, 7:3-18.

B. Use of a Receiver to Restore Time

75. For many years, devices connected to the Internet have had the ability to set a clock using time data that can be retrieved by any device connected to the Internet. *Gillett* teaches that it makes sense to connect thermostats to the Internet and that doing so can allow resetting of time in the event of a power failure. EX1020. This reference states: “A very different segment of the media coverage of “Internet appliances” concerns the notion of connecting traditional household appliances . . . to the Internet. . . . Some of these concepts make sense (e.g.,

connecting thermostats so you can program them through a Web site, not to have to reset time when power blinks, perform remote diagnostics on large appliances, etc.) . . .” *Id.*, p. 9, n.10. *Williamson* discloses that a “clock is periodically synchronized to a time message that the web server transmits to the intelligent controller and distributed by the power line communication unit to appliances that are capable of receiving the power line communications. The synchronization automatically corrects for time changes and assures all clocks report the correct time.” EX1010, 2:8-13. Thus, time is received over the Internet from a web server and used to set a real time clock.

76. *Carey* discloses using a WWVB receiver to set the real time clock in a thermostat to the correct time. EX1007, Abstract, ¶0004.

77. Thus, there are multiple options available to use a receiver to receive the time from a source outside of the thermostat to set the clock inside the thermostat.

78. As discussed above, prior to the June 24, 2004 priority date of the ’825 Patent, all of the technology at issue in the challenged claims was well known and broadly applied in various commercial applications. In my opinion, no individual elements of the challenged claims of the ’825 Patent were novel at the time of the alleged invention, and there was nothing novel or inventive about the manner in which those elements were combined in the challenged claims. Further, there were no technological barriers to combining these known elements to form the claimed

inventions. Indeed, combining these elements would have yielded predictable results.

VII. APPLICATION OF THE PRIOR ART TO THE CHALLENGED CLAIMS

79. I have been asked to provide my opinion as to whether the challenged claims of the '825 Patent would have been obvious in view of the prior art. The discussion below provides a detailed analysis of how the prior art references I reviewed disclose, teach, or suggest the limitations of the challenged claims of the '825 Patent.

80. As part of my analysis, I have considered the scope and content of the prior art and any potential differences between the claimed subject matter and the prior art. I have conducted my analysis as of the filing/priority date of the '825 Patent: June 24, 2004. I have also considered the level of ordinary skill in the pertinent art as of that date.

81. Below, I describe in detail the scope and content of the prior art, as well as any differences between the subject matter claimed and the prior art, on an element-by-element basis for each challenged claim of the '825 Patent. The analysis supports my finding that the differences between the claims of the '825 Patent and the prior art discussed herein are such that the subject matter as a whole would have been obvious at the time of the priority date of the '825 Patent to a POSITA.

82. In the ground below, I describe on an element-by-element basis how the prior art discloses or teaches all elements of Claims 1, 4 and 11-16 of the '825 Patent.

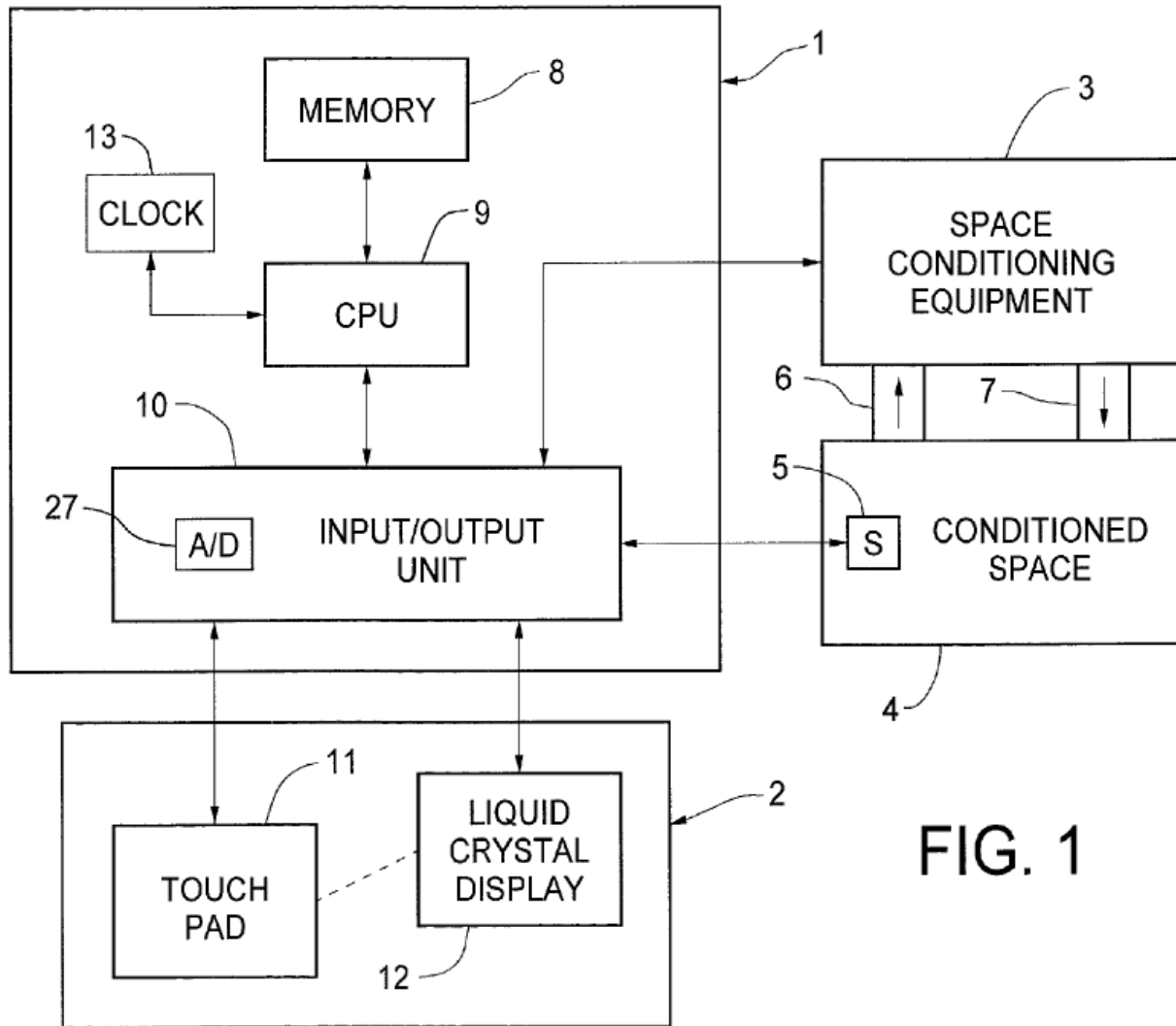
A. Summary of Prior Art

1. Overview of *Rosen* (Exhibit 1004)

83. *Rosen* (U.S. Patent Application Publication No. 2003/0142121) was filed on January 30, 2002 and published on July 31, 2003, nearly a year before the June 24, 2004 priority date of the '825 Patent. EX1004. Accordingly, *Rosen* is prior art to the '825 Patent at least under 35 U.S.C. §§ 102(a) and (e). The inventor of *Rosen*—Howard B. Rosen—is the same inventor as the '825 Patent. *Compare* EX1004, Cover with EX1001, Cover. Remarkably, however, *Rosen* was not disclosed to the USPTO by the applicant, nor cited or considered, during prosecution of the '825 Patent. EX1001, Cover.

84. *Rosen* relates to “a programmable thermostat system incorporating an integrated liquid crystal display/touch pad unit, constituting a touch screen, for interactive intuitive interface with a user to facilitate programming the thermostat system.” EX1004, ¶0001. *Rosen* explains that “[m]any modern thermostat systems include a real time clock, a memory and a data processor to run a process control program stored in the memory to accurately measure the temperature of a temperature sensor disposed in the conditioned space and to send control signals to

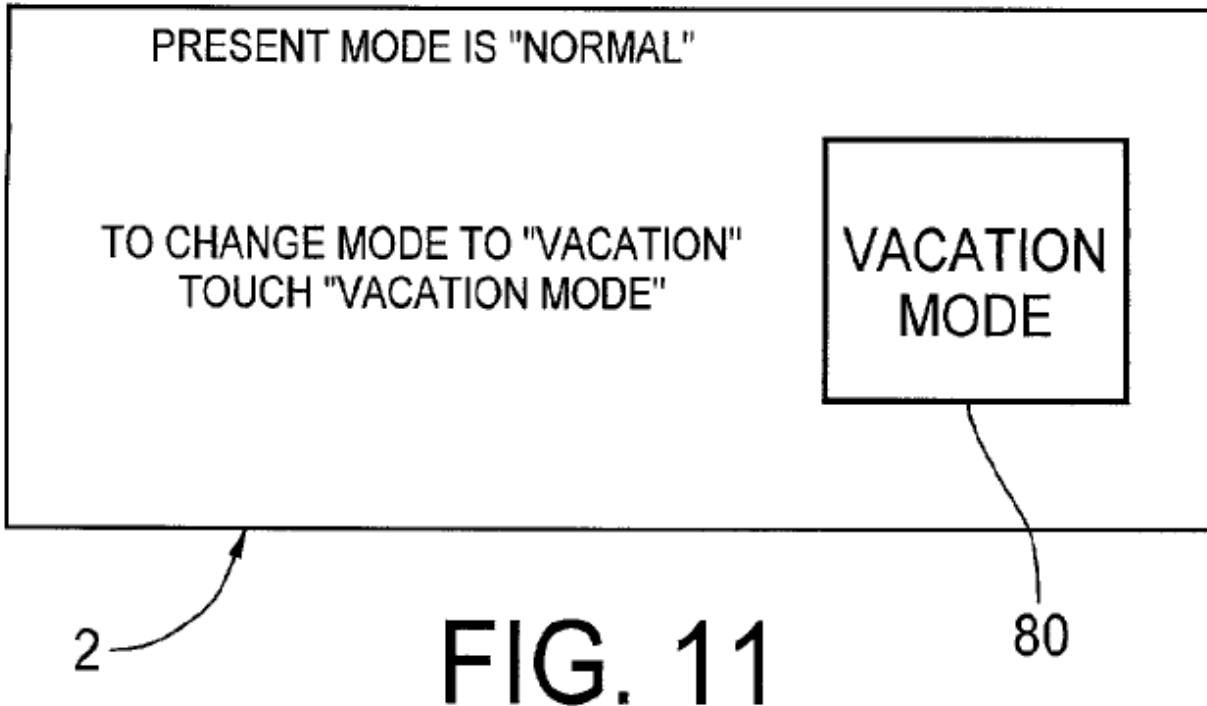
the heating and/or cooling equipment to closely control the temperature of the conditioned space.” *Id.*, ¶0003. Figure 1 of *Rosen* illustrates a programmable thermostat system similar to that of the ’825 Patent, which includes a settable real time clock 13:



Id., Figure 1, ¶0020.

85. *Rosen* explains that “[t]ypically, prior art programmable thermostat system[s] ... may include a vacation mode.” *Id.*, ¶0004. Figure 11 illustrates an

exemplary touch screen 2 with a vacation mode of operation according to the invention of *Rosen*:



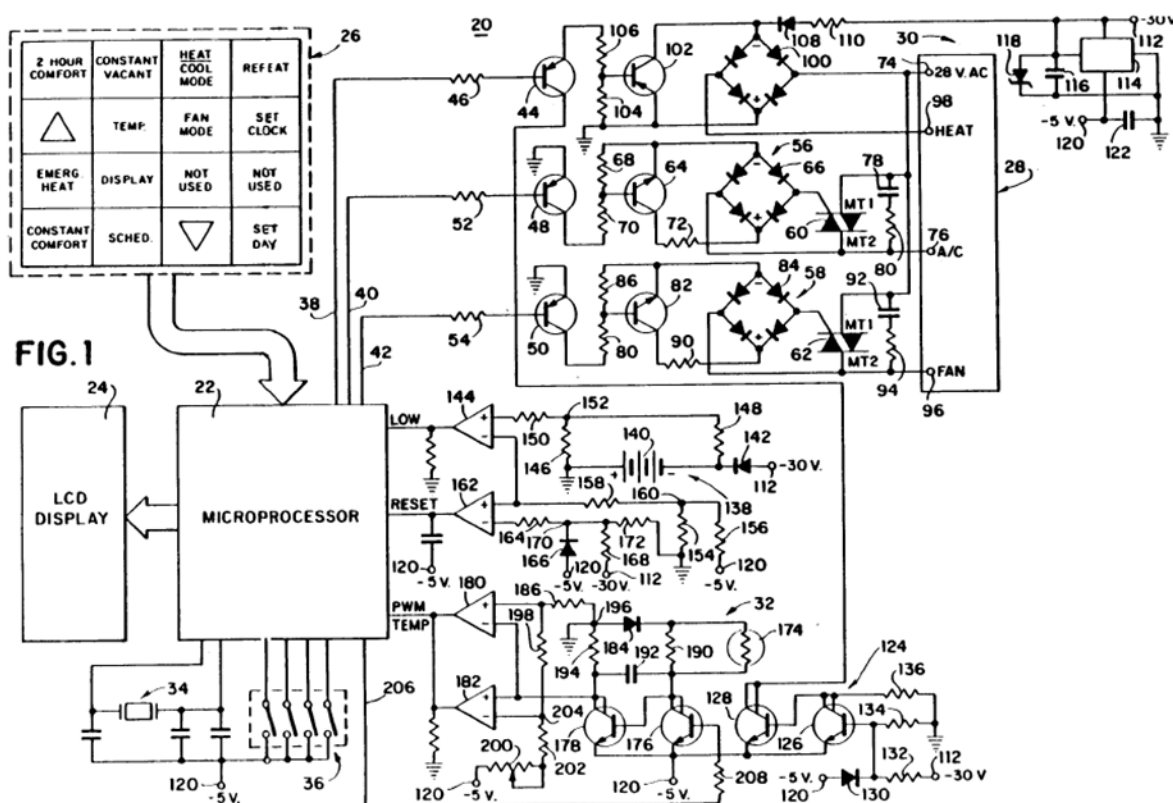
Id., Figure 11.

2. *Cacciatore* (Exhibit 1005)

86. *Cacciatore* (U.S. Patent No. 4,799,176) entitled “Electronic Digital Thermostat” was filed December 29, 1986 and issued January 17, 1989, and thus is prior art under pre-AIA 35 U.S.C. §§ 102(a), (b) and (e). EX1005. *Cacciatore* was not cited or considered during prosecution of the ’825 Patent. EX1003.

87. *Cacciatore* describes programmable electronic digital thermostats for use with heating and cooling systems. EX1005, 1:5-7. *Cacciatore* relates to a “thermostat [that] includes an improved power supply circuit for simply and

effectively providing its operating power utilizing an external alternating current power source of the temperature conditioning system and utilizing conventional existing wiring.” *Id.*, Abstract. *Cacciatore* explains that “provid[ing] [a] thermostat including a power supply circuit enabling efficient, effective and reliable operation utilizing existing wiring for a conventional electromechanical thermostat” is an important object of the present invention. *Id.*, 2:22-33. Figure 1 of *Cacciatore* illustrates a programmable thermostat system similar to that of the ’825 Patent, which includes diodes 108, 118, 130, 142, 166, and 184:



Id., Figure 1, 6:1-10, 6:18-21, 6:54-57, 7:14-20, 7:33-45.

88. *Cacciatore* utilizes power supplied from the “temperature conditioning system” to power the thermostat using “conventional existing wiring.” EX1005, Abstract, 1:18-22. The temperature condition systems would be understood, for example, to be a furnace, air condition unit, or heat pump. *Cacciatore* connects the thermostat to the temperature conditioning system via a “common 28 volt AC supply line.” *Id.*, 5:64-68, 2:14-15, 5:23-27, 6:16-21. *Cacciatore* also discloses protecting a backup battery via an isolation diode. EX1005, Figure 2, 6:48-58.

3. *Shigeaki* (Exhibit 1006)

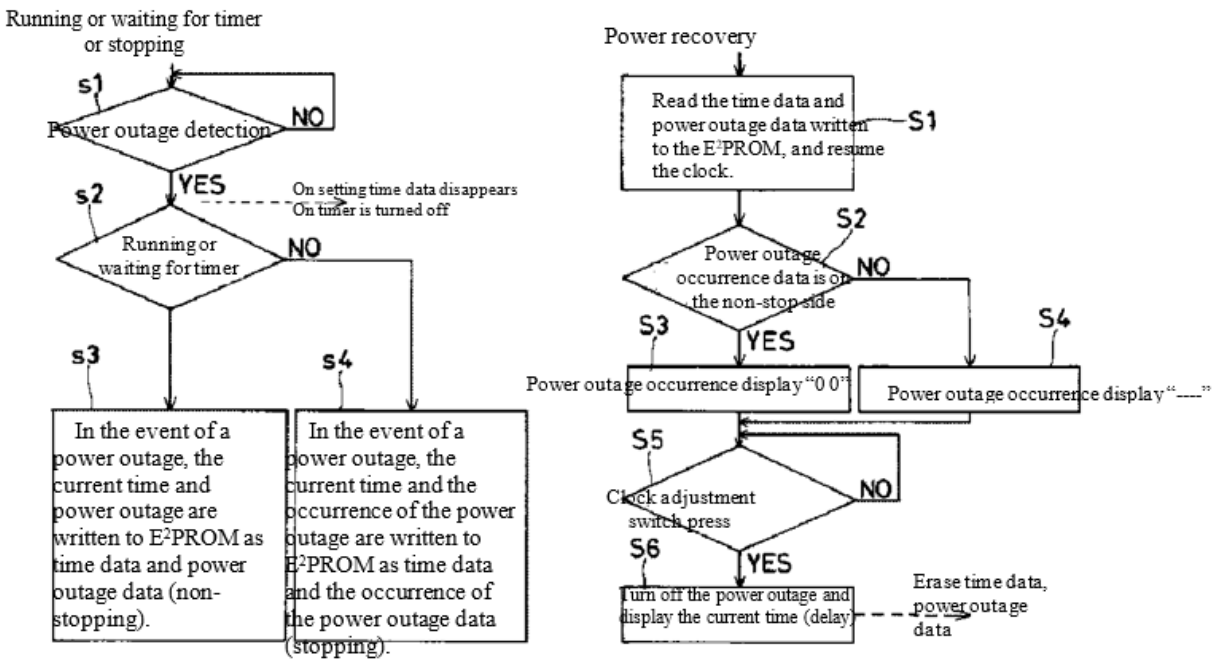
89. *Shigeaki* (Japanese Patent Application Publication No. 2740118B2) published on June 16, 1995, more than one year before the June 24, 2004 priority date of the '825 Patent. EX1006. Accordingly, *Shigeaki* is prior art to the '825 Patent at least under 35 U.S.C. §§ 102(a) and (b). *Shigeaki* was not cited or considered during prosecution of the '825 Patent. EX1003.

90. *Shigeaki* “relates to a clock device in which power for operation is supplied via a commercial power source.” EX1006, ¶0001. The clock devices of *Shigeaki* include control circuits for gas hot-air heaters. *Id.*, ¶¶0002, 0033-0035. *Shigeaki* explains that “there is known a technique for keeping a clock running with a backup power source even during a power outage, so that the clock will not go wrong even if the power outage occurs for a short period of time (several minutes).”

Id., ¶0004. To address the drawbacks of prior art clock components for these systems, *Shigeaki* employs the following operations: “[i]n the event of a power outage on a commercial power supply, the power outage detection means detects the power outage, and the data storage means stores the current time and the fact of the occurrence of the power outage in the semiconductor non-volatile memory as the current time data and power outage data” and then “[w]hen a power outage of the commercial power supply is restored, the power outage detection means detects the power recovery, and the data reading means reads time data and power outage data from the semiconductor non-volatile memory.” *Id.*, ¶¶0013-0014. *Shigeaki* operates such that “[t]he timekeeping means resumes timekeeping from the time corresponding to the read time data, and the display means displays the measured time delayed due to the occurrence of the power outage and the occurrence of the power outage on the display.” *Id.*, ¶0015.

91. Figure 2 of *Shigeaki* is a “flowchart showing the operation of the clock device” in accordance with *Shigeaki*’s invention:

[FIG. 2]



Id., ¶0065, Figure 2.

4. Carey (Exhibit 1007)

92. Carey (U.S. Patent Application Publication No. 2003/0121652) was filed on February 18, 2003 and published July 3, 2003, nearly a year before the June 24, 2004 priority date of the '825 Patent. EX1007, Cover. Accordingly, Carey is prior art to the '825 Patent at least under 35 U.S.C. § 102(a). Carey was cited during prosecution of the '825 Patent but not used in any rejection of the '825 Patent. EX1003, 48.

93. Carey relates to a "digital programmable thermostat" "that can automatically set the current time and date." EX1007, Abstract, ¶0004. Carey explains that "programming [the numerous existing programmable] thermostat[s]

typically requires the user to complete a complex series of steps to select the temperatures and time periods before the user can initiate the set back program, or force the user to use a default program that does not ideally meet the users schedule.” *Id.*, ¶0001. To address the drawbacks of prior art thermostat systems, the *Carey* thermostat “automatically sets the current time and date using information broadcasted by station WWVB, which is operated by the National Institute of Standards and Technology.” *Id.*, ¶0004. Figure 1 of *Carey* “is a schematic representation of the programmable digital thermostat in accordance with the present invention”:

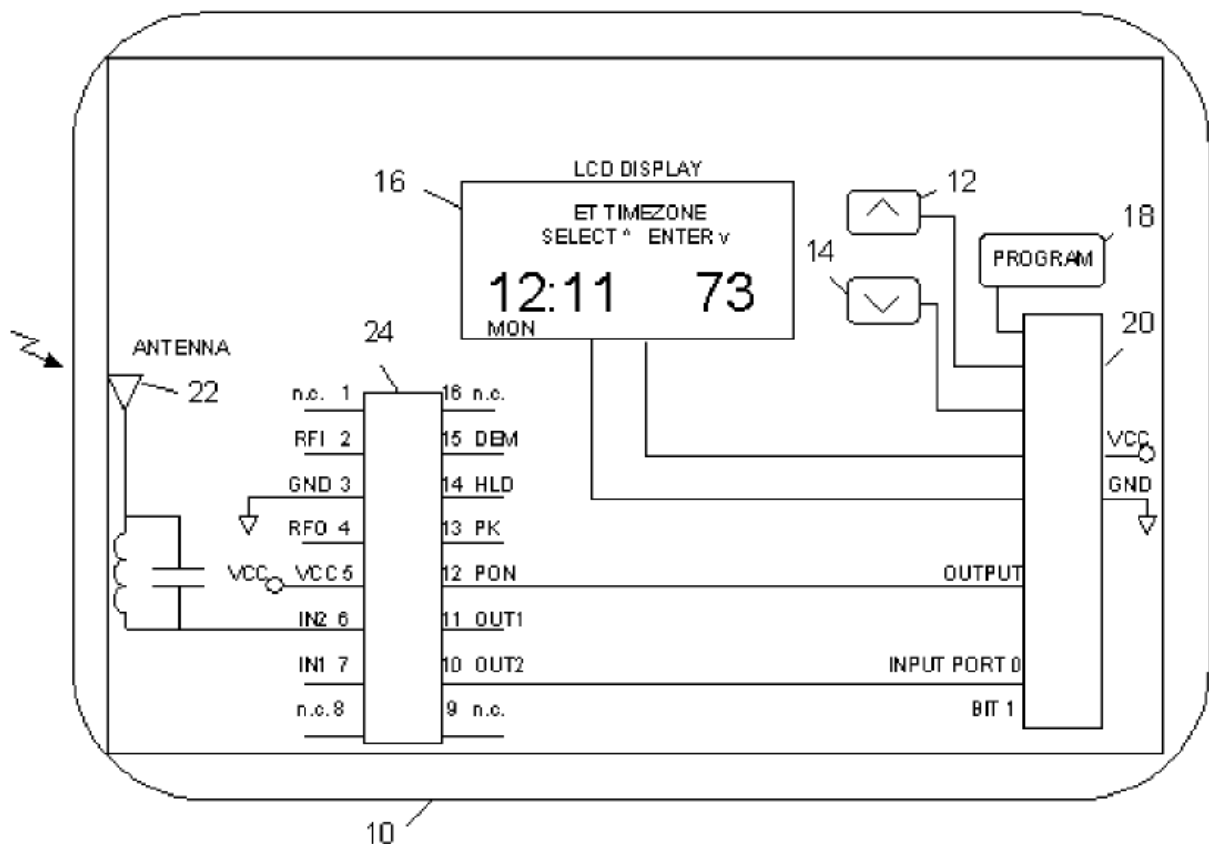


FIG. 1

Id., Figure 1, ¶0005.

94. Figure 2 of *Carey* “is a flow chart representing a program subroutine for setting the time of the programmable thermostat in accordance with the present invention”:

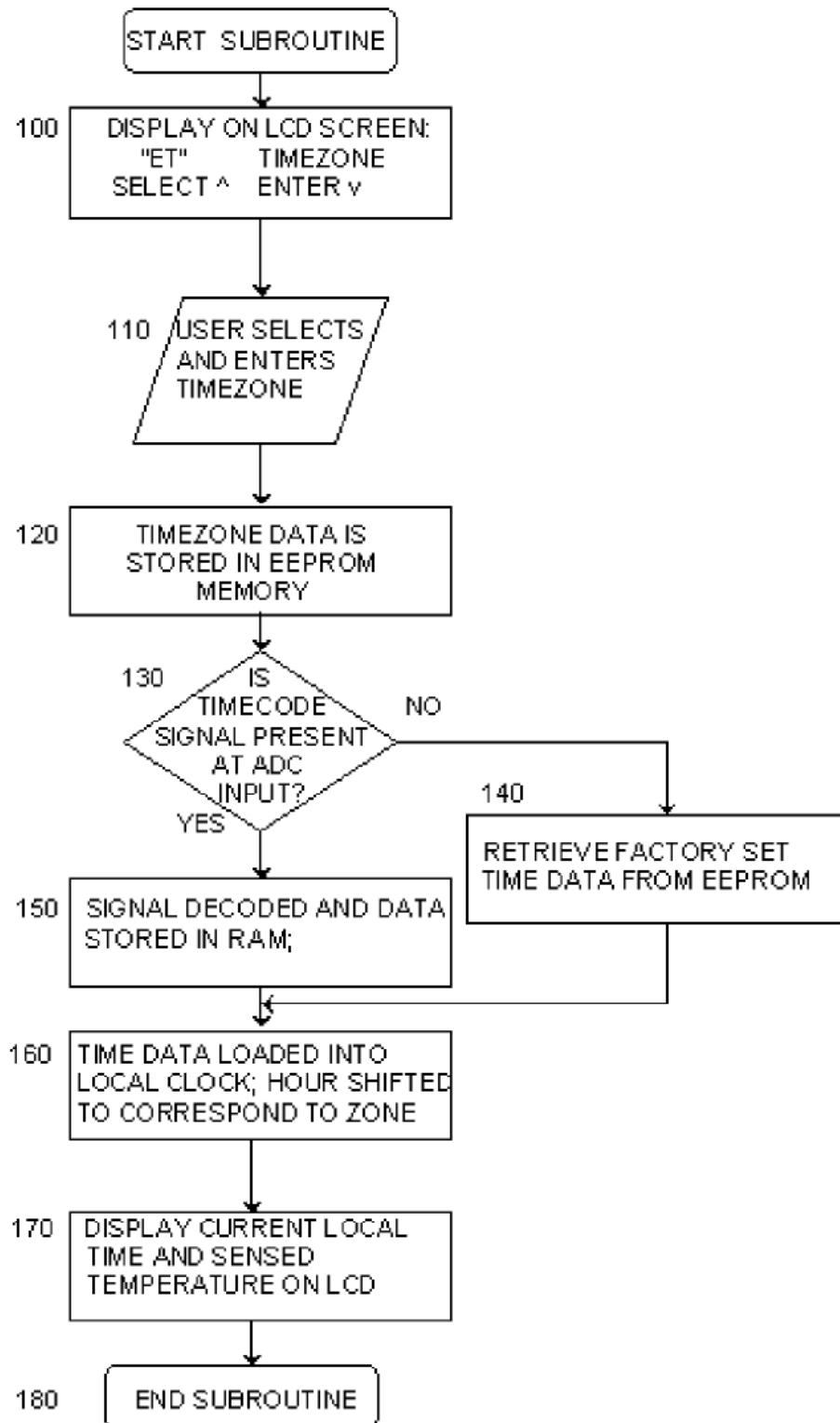


FIG. 2

Id., Figure 2, ¶0006.

5. *Shamoon* (Exhibit 1008)

95. *Shamoon* (U.S. Patent Application Publication No. 2003/0034898) was filed on November 13, 2001 and published on February 20, 2003, more than one year before the June 24, 2004 priority date of the '825 Patent. EX1008, Cover. Accordingly, *Shamoon* is prior art to the '825 Patent at least under 35 U.S.C. §§ 102 (a), (b) and (e). *Shamoon* was not cited or considered during prosecution of the '825 Patent. EX1003.

96. *Shamoon* relates to “an intelligent thermostat controller and hand held remote controller apparatus” that “consolidates all remote controls into a single remote control, as well as combines the capability to monitor and control a user’s thermostat and HVAC.” EX1008, ¶0042. Figure 6 of *Shamoon* “is a block diagram of a remote control apparatus and its thermostat and X-10 components according to the present invention.” *Id.*, ¶0034. While *Shamoon* refers to Figure 6 as a “remote control apparatus,” it also makes clear the wall thermostat would have the same functionality. “The wall thermostat controller of the invention uses the same operating system as the handheld controller, has similar hardware, and performs pretty much the same.” EX1008, ¶40. Based upon the teachings of Paragraph 40 of *Shamoon*, the wall thermostat would have all the functionality of the handheld controller except it would not have the functionality to control things like the entertainment system. *See id.* It does indicate that the wall thermostat will still be

able to perform the security functions as well. *See id.* Thus, a POSITA would understand that *Shamoon's* wall thermostat includes the features of Figure 6. I further note that Figure 6 of *Shamoon* discloses features such as connection to a telephone jack that are more consistent with a wall mounted unit. *Id.*, Figure 6. Thus, a POSITA would understand that what is disclosed in Figure 6 applies to a thermostat on a wall. This makes sense because Figure 6 illustrates connections to controls for space conditioning equipment and to a standard telephone jack.

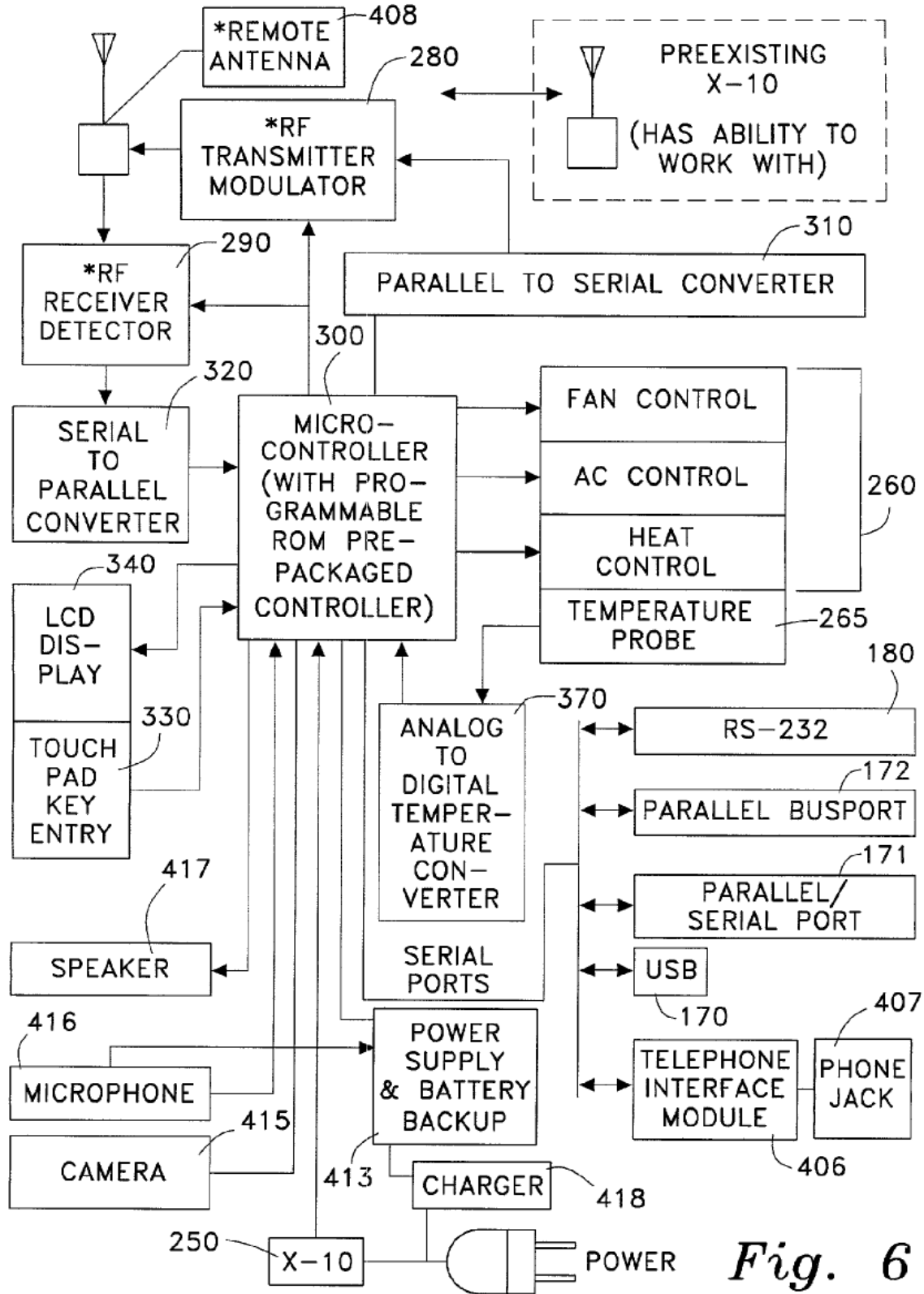


Fig. 6

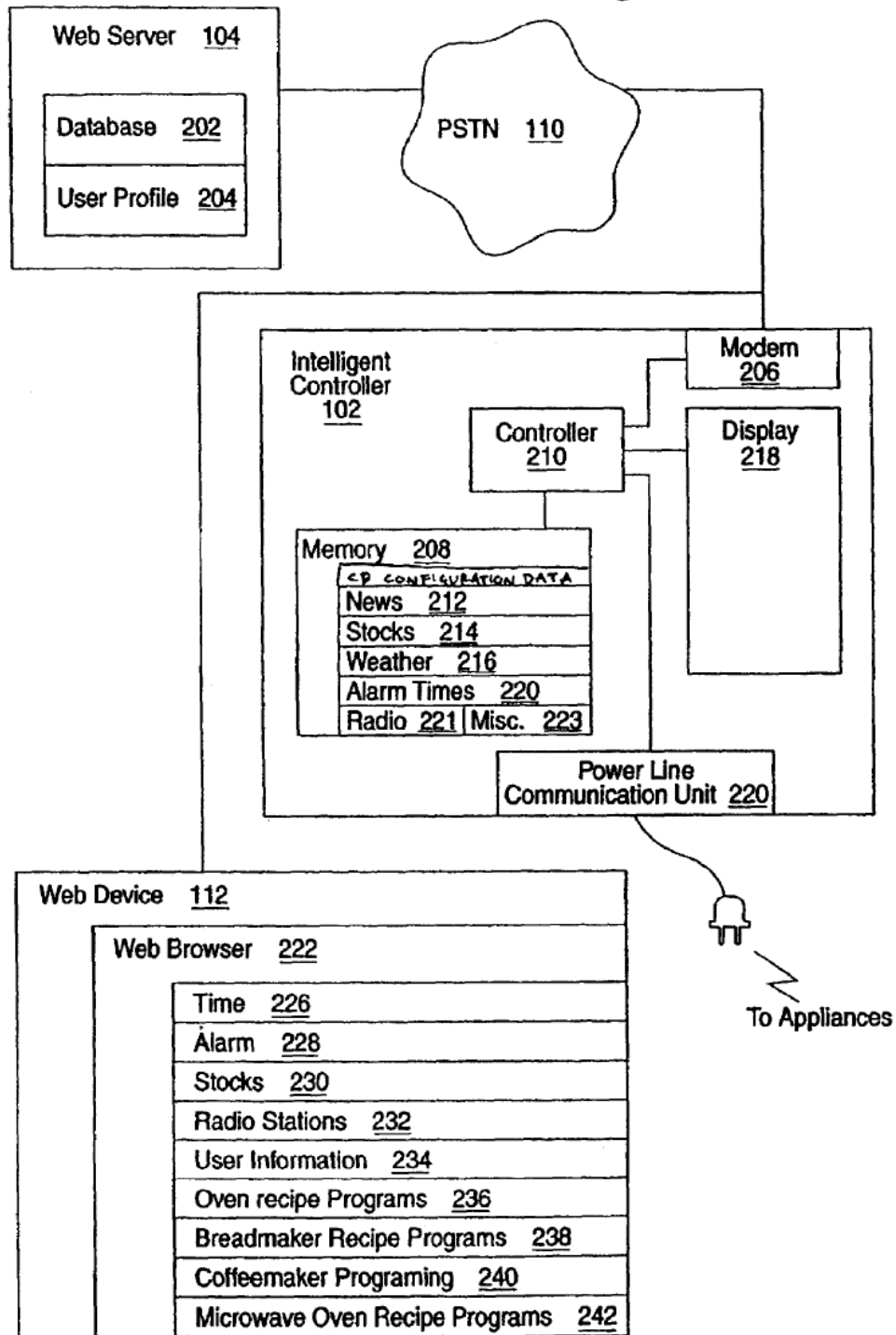
Id., Figure 6.

6. *Williamson* (Exhibit 1010)

97. *Williamson* (U.S. Patent No. 7,133,739) entitled “Intelligent Microwave Oven” was filed May 2, 2003 and published on March 25, 2004. EX1010, Cover. Accordingly, *Williamson* is prior art to the ’825 Patent at least under pre-AIA 35 U.S.C. §§ 102(a) and (e). *Williamson* was not cited or considered during prosecution of the ’825 Patent. EX1003. *Williamson* teaches setting a clock by receiving the correct time over the Internet—a second option to reset the clock according to Claim 11.

98. The invention of *Williamson* “may be broadly conceptualized as an approach in which a microwave oven receives a plurality of program recipes from a network ... while keeping a real-time clock synchronized and correctly set by receiving period time synchronization messages.” EX1010, Abstract. The appliance in *Williamson* includes a “web device 112 [that] communicates with the server 104 over an Internet Protocol connection. In an alternate embodiment, the intelligent controller 102 may [be] connected through an internet service provider and may even use a cable modem or DSL router to connect with the Internet. In yet another embodiment, a different communication protocol may be used by the device 112 to communicate with server 104.” *Id.*, 4:36-43. Figure 2 of *Williamson* illustrates “the intelligent controller in communication with the web server and web device.” *Id.*, 3:17-19.

Fig. 2



Id., Figure 2.

99. As described by *Williamson*, “[a] clock is periodically synchronized to a time message that the web server transmits to the intelligent controller and distributed by the power line communication unit to appliances that are capable of receiving the power line communications. The synchronization automatically corrects for time changes and assures all clocks report the correct time.” *Id.* 2:8-23. Thus, time is received over the Internet from a web server and used to set a real time clock.

100. Figure 3 of *Williamson* illustrates “a block diagram of the intelligent controller of FIG. 2.” *Id.*, 3:20-21.

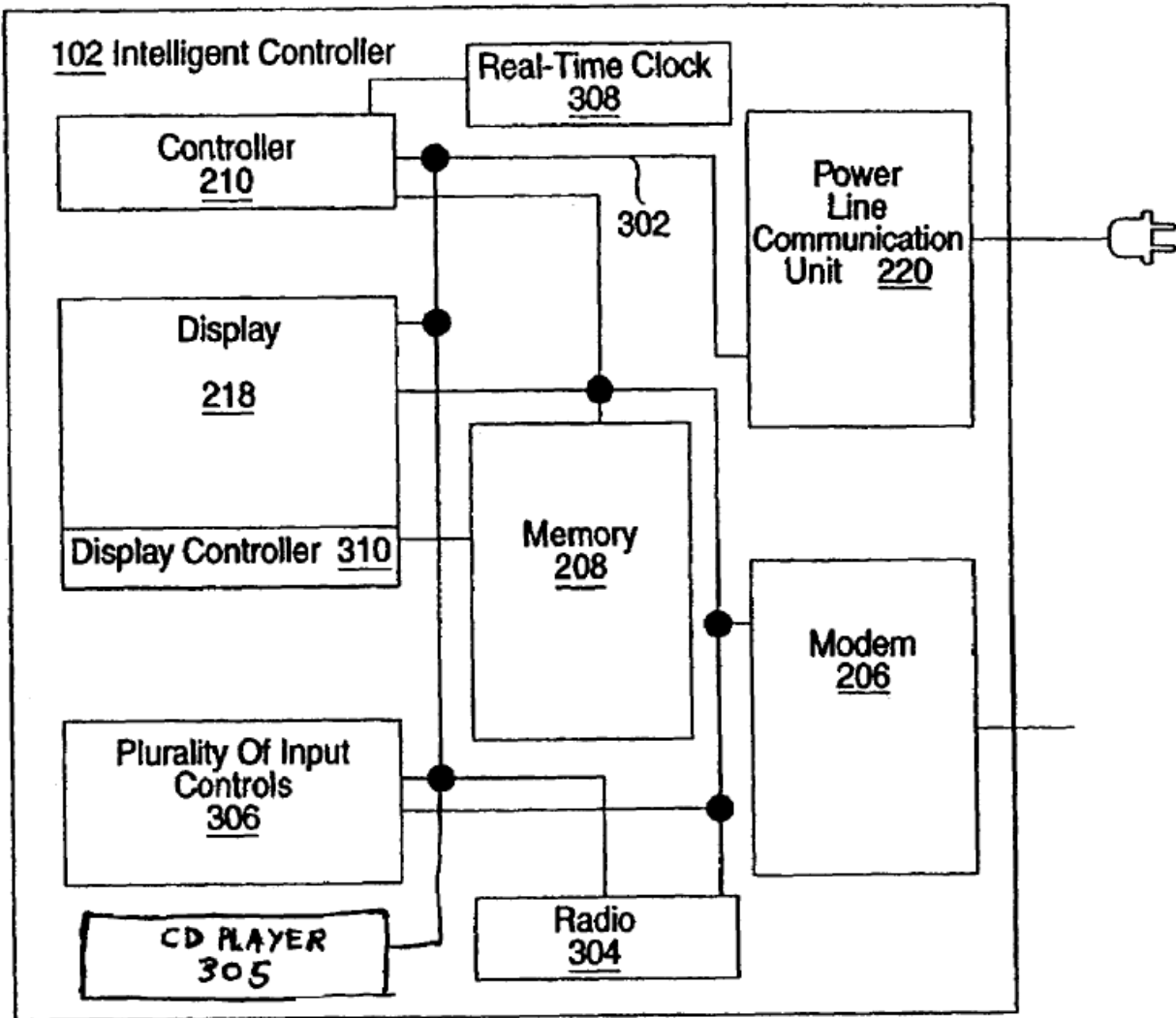


Fig. 3

Id., Figure 3.

B. Grounds of Unpatentability

101. I have reviewed and analyzed the prior art references and materials listed in Section VII.A above. In my opinion, the challenged claims of the '825

Patent are rendered obvious based on the following prior art set forth in Grounds 1-9 below:

Ground	'825 Patent Claims	Basis for Challenge under §103
1	1, 4	Obvious under § 103 based on <i>Rosen</i> in view of <i>Cacciatore</i> , and <i>Shigeaki</i>
2	11, 12, 13, 16	Obvious under § 103 based on <i>Rosen</i> in view of <i>Cacciatore</i> , and <i>Carey</i>
3	11, 14, 15, 16	Obvious under § 103 based on <i>Rosen</i> in view of <i>Cacciatore</i> , and <i>Williamson</i>
4	1	Obvious under § 103 based on <i>Shamoon</i> in view of <i>Cacciatore</i> , and <i>Shigeaki</i>
5	4	Obvious under § 103 based on <i>Shamoon</i> in view of <i>Cacciatore</i> , <i>Shigeaki</i> , and <i>Toth</i>
6	11, 12	Obvious under § 103 based on <i>Shamoon</i> in view of <i>Cacciatore</i> , and <i>Carey</i>
7	13, 16	Obvious under § 103 based on <i>Shamoon</i> in view of <i>Cacciatore</i> , <i>Carey</i> , and <i>Toth</i>
8	11, 14	Obvious under § 103 based on <i>Shamoon</i> in view of <i>Cacciatore</i> , and <i>Williamson</i>
9	15, 16	Obvious under § 103 based on <i>Shamoon</i> in view of <i>Cacciatore</i> , <i>Williamson</i> , and <i>Toth</i>

C. Ground 1: Claims 1 and 4 are obvious over *Rosen* in view of *Cacciatore*, and *Shigeaki*

102. Based on the following analysis, I conclude that a POSITA at the relevant time (June 24, 2004) would have understood the limitations of Claims 1 and

4 were expressly disclosed, taught, or suggested by *Rosen* in combination with *Cacciatore* and *Shigeaki* when considering the general knowledge of a POSITA.

1. Motivation to Combine

(i) Rationale and motivation for combining *Rosen* with *Cacciatore*

103. I provide *Cacciatore* in grounds involving *Rosen* due to the “means coupling suitable power for energizing said thermostat from said space conditioning equipment to said thermostat” element of Claim 1. This element is disclosed by *Rosen* and would be obvious in any case even in light of admissions in the specification of the ’825 Patent. To the extent the Board disagrees, *Cacciatore* supplies this element.

104. *Rosen* discloses supplying power to its thermostat system from space conditioning equipment and thus discloses the function of coupling suitable power for energizing said thermostat from said space conditioning equipment to said thermostat. EX1004, ¶0020 (“The thermostat system may be suitably powered ... from equipment to which it is connected.”). A POSITA would understand that *Rosen* is teaching to obtain power from the space conditioning equipment to which is connected and that this occurs via a power line. To my knowledge, power has not been supplied to a thermostat from space conditioning equipment using anything other than a power line (wiring). Thus, the mere disclosure that the space

conditioning equipment is powering the thermostat would disclose that a power line is being used to supply the power.

105. Thermostats have traditionally been powered by using wiring (a power line) to connect a source of power in the space conditioning equipment to the thermostat. The '825 Patent teaches that power is supplied “in accordance with the prior art.” EX1001, 5:3. Power is “conventionally supplied from the space condition equipment 3 via a line 30 through an isolation diode 33.” *Id.*, 5:3-5. Given this admission that it is conventional to supply power from space conditioning equipment via a “line,” a POSITA would understand *Rosen* to be teaching to power the thermostat by connecting it via a “line” to the space conditioning equipment. This element is also within the general knowledge of a POSITA. Thus, *Rosen* discloses this element and even if it didn't, it would be obvious to use what is admitted as “conventional” in the specification to supply power.

106. If the Board disagrees or determines that an “isolation diode” to protect the backup battery is part of the corresponding structure, then it would be obvious to use a line to connect the thermostat to the power source and protect the backup battery with an isolation diode. Again, the '825 Patent, in the passage quoted above, teaches that the power is “conventionally supplied” using a power line and an isolation diode to protect the battery. EX1001, 5:3-5. Inventor *Rosen* agrees that the isolation diode to protect the battery is prior art. EX1013, 96:9-97:6. Indeed, a

person of ordinary skill in the art knows that a primary function of a diode is to protect circuitry by allowing electrical current to flow in only one direction. Thus, it is obvious to use this prior art method of supplying power.

107. But if the Board disagrees with all of the above, then the power line and a diode to protect the battery (an isolation diode) is obvious to use given the teachings of *Cacciatore*. As an initial matter, *Rosen* and *Cacciatore* are in the same field of endeavor and are therefore analogous art to the '825 Patent and each other. Similar to the '825 Patent, both *Rosen* and *Cacciatore* relate to programmable thermostats. EX1004, ¶0001 (“This invention relates to ... a programmable thermostat system”); EX1005, 1:6-7 (“The present invention relates generally to programmable electronic digital thermostats.”); EX1001, Title (“Programmable Thermostat Employing a Fail Safe Real Time Clock”).

108. *Cacciatore*'s thermostat “includes an improved power supply circuit for simply and effectively providing its operating power utilizing an external alternating current power source of the temperature conditioning system and utilizing conventional existing wiring.” EX1005, Abstract. The temperature conditioning system is what is controlled by the thermostat and a POSITA would understand that to be a furnace, air conditioning unit or heat pump. EX1005, Abstract, 1:18-22. In particular, *Cacciatore* discloses “a terminal ... that is connected to the common **28 volt AC supply line** of the temperature conditioning

system” wherein a “[r]ectified voltage is supplied by the bridge rectifier 100 for the operating power supply 30. The negative output of the bridge rectifier is coupled through a series combination of a **diode 108** and a resistor 110 to an input 112 of a voltage regulator integrated circuit device 114.” *Id.*, 5:23-27, 5:64-68 (emphasis added); see also Abstract, 2:14-15, 6:16-21. This teaches connection via a power line (wiring) and through a diode. Moreover, *Cacciatore* also discloses protecting a backup battery via an isolation diode—the identical or equivalent structure under a different claim construction. EX1005, Figure 2, 6:48-58. Because *Cacciatore* relates to the art of thermostat systems, a POSITA would have recognized that *Cacciatore*’s power supply configuration is suitable for use in the programmable thermostat system of *Rosen*.

109. Based on *Cacciatore*’s disclosure that the configuration provides a means for “simply and effectively providing” operating power to a thermostat system, a POSITA would have been motivated to modify *Rosen* to use the power line and isolation diode taught by *Cacciatore* to supply energizing power to *Rosen*’s thermostat system from space conditioning equipment.

110. Modifying *Rosen* to incorporate the *Cacciatore*’s teachings would merely involve the application of a known technique (supplying power to a thermostat system from space conditioning equipment using a power line and protecting a battery with an isolation diode as taught by *Cacciatore*) to a known

device (the thermostat system of *Rosen*) to obtain predictable results (a thermostat system that receives energizing power from space conditioning equipment via a power line employs an isolation diode to protect a backup battery).

111. A POSITA would have had a reasonable expectation of success in making the combination. It was conventional to supply power using such structure so a POSITA would just be using prior art structure to supply power. EX1004, ¶0020; EX1001, 5:3-5; EX1013, 96:9-97:6. It was well known to use space conditioning equipment to supply energizing power to a thermostat system, as taught by *Rosen* and admitted by the '825 Patent. EX1004, ¶0020 (Programmable thermostats “may be suitably powered by a battery [] and/or from equipment to which is connected.”); EX1001, 5:3-5 (“[i]n accordance with the prior art, power to the processor 1 is conventionally supplied from the space conditioning equipment 3 via a line 30 through an isolation diode 33.”).

112. Additionally, power lines and isolation diodes are conventional, well-known components, and their use in power supply systems is well known and would have been within the knowledge of a POSITA before the priority date of the '825 Patent. It would have been within the skills of a POSITA to implement these elements in the thermostat system of *Rosen*.

113. Indeed, a POSITA would have recognized that the thermostat systems described in *Rosen* and *Cacciatore* are remarkably similar. The teachings of

Cacciatore are directed towards thermostat systems such that a POSITA would have understood that *Cacciatore*'s techniques were suitable for application with *Rosen*'s thermostat system. See EX1005, Title ("Electronic Digital Thermostat"). Thus, a POSITA would have understood that *Cacciatore*'s teaching of using space conditioning equipment to supply power to a thermostat system via an isolation diode could be readily incorporated into the thermostat system of *Rosen*. These aspects of *Rosen* and *Cacciatore* are discussed in more detail with respect to element 1[a]. *Infra*, § VII.C.2.iii.

(ii) Rationale and motivation for combining *Rosen* as modified by *Cacciatore* with *Shigeaki*

114. *Rosen* does not disclose the limitations of Claim 1 concerning the storage of time in a nonvolatile memory and putting that stored time into the real time clock after power is restored. *Shigeaki* discloses these limitations and it would be obvious to combine *Shigeaki* with *Rosen*. Specifically, *Shigeaki* discloses the precise method claimed in Claim 1 to reset the real time clock after a power outage: "When a power outage occurs, the time data pertaining to the current time is stored in E²PROM 2, and when power is restored, the time data is read from E²PROM 2, and the time is resumed from the current time corresponding to the retrieved time data." EX1006, ¶0061.

115. *Rosen* and *Shigeaki* are in the same field of endeavor and are therefore analogous art to the '825 Patent and each other. Both *Rosen* and *Shigeaki* relate to

programmable devices with real-time clocks that store time information. EX1004, Abstract (“A programmable thermostat system for controlling space conditioning equipment includ[ing] ... a liquid crystal display ... [and] a real time clock”); EX1006, ¶0002 (“heater is provided with a clock device having a timekeeping means for clocking the current time and a display means”).

116. *Shigeaki* provides two motivations to use its invention in a thermostat: (1) less time and effort to adjust the clock after a power outage and (2) saving the cost of a backup battery. “When the power outage of the commercial power source is restored, the clock is delayed only by the time of the power outage. Therefore, short power outage time means that the clock device requires less time and effort to adjust the clock when the power is restore. The clock device does not require a power supply for backup, saving the cost of parts.” EX1006, ¶¶0025-0026. The second motivation of eliminating the need for a backup power supply is mentioned again: “Because a backup power source, such as a capacitor, is unnecessary** to keep the control circuit 1 in operation during a power outage, part costs can be saved, and there is no need to replace the battery.” *Id.*, ¶0063. Eliminating the need for a capacitor or backup battery is precisely what the ’825 Patent discloses as an advantage of the invention. *E.g.*, EX1001, 3:30-31. Thus, a POSITA would have been motivated to use the method of restoring the clock after a power outage both to

make the clock easier to reset and to eliminate the need for a backup power source to save costs.

117. Keeping the clock of a thermostat as accurate as possible when power is restored after a power outage was a recognized problem for thermostats. EX1001, 2:18-55. Inventor Rosen acknowledged that prior art thermostats addressed the issue of keeping the correct time during a power outage. EX1013, 75:8-25. Thus, the problem of keeping the clock as correct as possible after a power outage was a recognized problem for thermostats. The '825 Patent discloses several prior art solutions to this problem—use of battery to power the clock or use of a capacitor to power the clock during a power outage. EX1001, 2:18-55. A POSITA would consider all available prior art methods to address that problem of keeping the clock as accurate as possible in the event of a power outage and thus would turn to *Shigeaki* as one design choice to solve the problem. Inventor Rosen agreed that a POSITA had various methods to choose from to keep the time as accurate as possible after a power failure. EX1013, 76:11-17. Given that *Shigeaki* provides a method to do so with identified advantages, it would be obvious to use the method of *Shigeaki* in the thermostat of *Rosen*.

118. A POSITA would have had a reasonable expectation of success in making the combination. As an initial matter, non-volatile memory and random access memory are conventional, well-known components, and their use in

thermostat systems as well as circuit chips is well-known. Writing data into and reading data from non-volatile memory is also a conventional technique commonly known to a POSITA and used in thermostat systems and analogous devices in the prior art.

119. Moreover, a POSITA would have had a reasonable expectation of success in making the combination because, *Rosen* explains that “integrated circuit chips including all the processor components with all the necessary interface conditioning circuits are available off-the-shelf” and that “[t]he subject invention only requires the capabilities of such a processor, and off-the-shelf integrated circuit processor chips may be used to advantage in the subject thermostat system.” EX1004, ¶0023. Nonvolatile memories, such as EEPROMs, are available off the shelf and have been used in the thermostats for a few years prior to the filing of the ’825 Patent. EX1018, 16:4, Figure 22b (Disclosing flash memory in an integrated thermostat system as early as October 22, 2002); EX1006, ¶0033 (EEPROMS are nonvolatile memories); EX1019, 7:29-32 (“The non-volatile RAM 108 may be an electrically erasable PROM or a ‘flash’ PROM which saves its contents even when power is lost.”).

120. Because the systems of *Rosen* and *Shigeaki* utilize commercially available, off-the-shelf components, and known techniques it would have been well within the abilities of a POSITA to modify *Rosen*’s thermostat system to include the

non-volatile memory of *Shigeaki* and its associated control program functionality (namely, periodically reading the current time and date information into non-volatile memory and reading such data from the non-volatile memory into the real time clock upon restoration of power after failure). EX1013, 97:21-99:9 (inventor of '825 Patent admitting that all of the hardware components in Claim 1 are off-the-shelf components available in the prior art).

121. The express teachings of *Shigeaki* evidence that a POSITA would have been motivated to combine *Shigeaki* with *Rosen*. The object of *Shigeaki*'s invention "is to provide a clock device that is connected to a commercial power supply, where it is easy to know whether or not a power outage has occurred, and ***less trouble is required for adjusting the clock when the power is restored.***" EX1006, ¶0006 (emphasis added). *Shigeaki* explains the problem that occurs when there is a power failure: power to the clock lapses and the clock resets. *Id.*, ¶0003. Once the power is eventually restored, a user must expend time and effort to reset the clock to the correct time. *Id.* *Shigeaki* acknowledges that there is a "known [] technique for keeping a clock running with a backup power source even during a power outage" and applies the known technique to a gas hot-air heater. *Id.*, ¶¶0004-0005.

122. A POSITA would have recognized that the systems described in *Rosen* and *Shigeaki* are complementary and very similar. The teachings of *Shigeaki* are directed towards a heater that includes various hardware elements, namely, a display

for displaying the current time, a processor, a clock and a memory. EX1006, ¶0033. *Rosen's* programmable thermostat system for controlling space conditioning equipment, e.g., a heater, includes similar hardware such as a display to prominently display the current time, a processor, a real time clock, and a memory. EX1004, Abstract, ¶0034. Given the similarities of the systems, a POSITA would have understood that *Shigeaki's* techniques were suitable for application with *Rosen's* thermostat system. *Rosen* explains that its “memory 8 may include ... a random-access part,” but does not disclose if the random-access memory is volatile or non-volatile. EX1004, ¶0020.

123. A POSITA would have understood as a matter of basic engineering knowledge that volatile memory does not retain stored data when a power failure occurs. Given that the “random-access part [of the memory] stores data subject to change during operation,” and power failures may occur, it would be obvious for a POSITA to design the *Rosen* system to include non-volatile random access memory so that certain information stored within is not lost in the event of a power failure. EX1004, ¶0020. In fact, well before the priority date of the '825 Patent, others in the art had chosen to include “flash memory” in thermostat systems. EX1009, 3:1-10; EX1018, 16:4, Figure 22b (disclosing flash memory in an integrated thermostat system). As known to a POSITA, EEPROMs and flash memory are non-volatile random access memories as disclosed in element 1[k] of the '825 Patent. EX1019,

7:29-32 (“The non-volatile RAM 108 may be an electrically erasable PROM or a ‘flash’ PROM which saves its contents even when power is lost.”).

124. As discussed in more detail below, *Shigeaki* discloses a circuit chip which includes a non-volatile memory. Based on *Shigeaki*’s teachings, a POSITA would have been motivated to include non-volatile random access memory in the *Rosen* system in order to improve upon the *Rosen* thermostat system by making it more resilient to power outages. Additionally, incorporating *Shigeaki*’s non-volatile memory would provide a better experience to the users of *Rosen*’s thermostat system because they would not have to engage in the multi-step process *Rosen* describes to “set the present time” in the event of an outage. EX1004, ¶0034.

125. In addition to including ***non-volatile*** memory as taught by *Shigeaki* in the *Rosen* system, a POSITA would have also been motivated to modify *Rosen*’s control program stored in memory to include the functionality required for operation of the device of *Shigeaki* (e.g., by modifying *Rosen*’s control program to include the functionality of *Shigeaki*’s control circuit for “stor[ing] the current time ... in the semiconductor non-volatile memory as the current time data,” and “[when] a power outage of the commercial power supply is restored, ... the data reading means reads time data and power outage data from the semiconductor non-volatile memory,” as described in *Shigeaki*). EX1006, ¶¶0013-0014; see also *id.*, Claims 1, 2, ¶¶0007-

0008, 0039. These aspects of *Rosen* and *Shigeaki* are discussed in more detail with respect to elements 1[m] and 1[n] below. *Infra*, § VII.C.2.ix.

126. Thus, a POSITA would have understood that the reading and writing of time data to and from the non-volatile memory of *Shigeaki* could be readily incorporated into the control program and memory in the thermostat system of *Rosen*. It would have been well within the abilities of a POSITA to modify *Rosen*'s thermostat system to include the non-volatile feature memory of *Shigeaki* and the reading and writing of time data to and from the non-volatile memory of the control circuit in *Shigeaki*.

2. Claim 1

(i) Admissions in the Patent

127. Each of the eleven elements 1[pre]-1[j] are disclosed by *Rosen*, as discussed below. Each of these elements is also common knowledge of a POSITA as admitted by the '825 Patent and its inventor. EX1001, 1:24-2:22, Figure 1, 3:54-57, 4:10-5:17; EX1013, 97:21-99:9 (inventor of '825 Patent admitting that all of the hardware components in Claim 1 are off-the-shelf components available in the prior art). Programmable thermostats for controlling space conditioning equipment were well known in the art, as acknowledged by the '825 Patent. EX1001, 5:28-35 ("Many modern thermostat[s] ... run a process control program ... to send control

signals to the heating and/or cooling equipment to closely control the temperature of the conditioned space.”).

128. The '825 Patent acknowledges that the use of space conditioning equipment to supply power to a thermostat system was “conventional[.]” EX1001, 5:3-5 (“in accordance with the prior art, power to the processor 1 is conventionally supplied from the space conditioning equipment 3 via a line 30 through an isolation diode 33”); *see also id.*, Figure 1, 2:18-19, 5:43-46; *see also* EX1013, 98:16-18 (“Q. There's no new isolation diode disclosed in the '825 Patent, correct? A. Correct.”). Figure 1 of the '825 Patent, labeled as “PRIOR ART,” shows “conventionally supply[ing]” “power to the processor 1” “from the space conditioning equipment 3 via a line 30 through an isolation diode 33.” EX1001, Figure 1, 5:3-5.

129. The '825 Patent does not purport to have invented a temperature sensor for providing an electrical signal indicative of the temperature of a conditioned space or improved upon existing temperature sensors. It was well known in the art that thermostat systems include a temperature sensor for providing an electrical signal indicative of the temperature of a conditioned space, as acknowledged by the '825 Patent. EX1001, Figure 1, 1:29-35 (“Many modern thermostat[s] include ... a process control program stored in the memory to accurately **measure the temperature of a temperature sensor disposed in the conditioned space** and to **send control signals** to the heating and/or cooling equipment to closely control the

temperature of the conditioned space.”) (emphasis added). Figure 1 of the ’825 Patent, labeled as “PRIOR ART,” illustrates “an exemplary thermostat [that] includes ... a temperature sensor 5 which is disposed in a conditioned space 4.” *Id.*, Figure 1, 4:9-11. The ’825 Patent itself further admits that the temperature sensor and its accompanying functionality as required by the claims was “very well known in the art”:

Thus, *in the usual manner* during normal operation, *the temperature sensor 5 sends an electrical signal* (e.g., if the sensor 5 is a simple thermistor, a resistance value; several types of temperature sensors are widely used) *representative of the temperature within the conditioned space 4* which the processor can compare against a previously entered set point to determine if control signals need to be sent to the space conditioning equipment 3. For example, if the temperature in the conditioned space 4 is found to be too low when operation is in the heating mode, the processor 1 signals the space conditioning equipment 3 to circulate, through ducts 6, 7, air from/to the conditioned space 4 which is heated by the space conditioning equipment before return to the conditioned space. This heating phase continues until the sensor 5 indicates that the space is now too hot (or approaching too hot) with reference to the current set point such that the processor 1 sends signal(s) to the space conditioning equipment 3 to cease the heating function, *all as very well known in the art.*

EX1001, 4:47-65 (emphasis added).

130. The ’825 Patent does not purport to have invented “D) a processor, said processor including: 1) a central processing unit; 2) a first memory coupled to said central processing unit for storing program and data information; and 3) an input/output unit” or improved upon existing versions of these elements. It was well

known in the art that thermostat systems include these elements, as acknowledged by the '825 Patent. EX1001, Figure 1. Figure 1 of the '825 Patent, labeled as "PRIOR ART," illustrates that "an exemplary thermostat includes a processor 1" which "includes a central processing unit (CPU) 9 in communication with a memory 8 for storing data and program information and also, via an input/output unit (I/O unit) 10." *Id.*, Figure 1, 4:9-10, 4:21-24. The '825 Patent itself admits that "[m]any modern thermostat[s] include a real time clock, a memory and a data processor to run a process control program stored in the memory to accurately measure the temperature of a temperature sensor disposed in the conditioned space and to send control signals to the heating and/or cooling equipment to closely control the temperature of the conditioned space." *Id.*, 1:29-36.

131. Moreover, it was well known in the art that thermostat systems include "a) a sensor input coupled to said temperature sensor for receiving said electrical signal therefrom; and b) a control output coupled to the space conditioning equipment for issuing control signals thereto" as acknowledged by the '825 Patent. EX1001, Figure 1. Figure 1 of the '825 Patent, labeled as "PRIOR ART," illustrates "an exemplary thermostat [that] includes ... a temperature sensor 5 which is disposed in a conditioned space 4" and "an input/output unit (I/O unit) 10." *Id.*, Figure 1, 4:9-11, 4:24-25; *see also id.* at 4:37-39 ("Temperature information from the sensor 5 and output signals to a space conditioning (heating and/or cooling) unit

3 pass through the I/O unit 10 under control of the CPU 9.”). The ’825 Patent itself further admits that the electrical signals from the temperature sensor and issued to the space conditioning equipment as required by the claims were “very well known in the art”:

Thus, *in the usual manner* during normal operation, the temperature sensor 5 sends an electrical signal (e.g., if the sensor 5 is a simple thermistor, a resistance value; several types of temperature sensors are widely used) representative of the temperature within the conditioned space 4 which the processor can compare against a previously entered set point to determine if control signals need to be sent to the space conditioning equipment 3. For example, if the temperature in the conditioned space 4 is found to be too low when operation is in the heating mode, the processor 1 signals the space conditioning equipment 3 to circulate, through ducts 6, 7, air from/to the conditioned space 4 which is heated by the space conditioning equipment before return to the conditioned space. ***This heating phase continues until the sensor 5 indicates that the space is now too hot (or approaching too hot)*** with reference to the current set point such that the ***processor 1 sends signal(s) to the space conditioning equipment 3 to cease the heating function, all as very well known in the art.***

EX1001, 4:47-65 (emphasis added); *see also id.* at 1:29-35 (“Many modern thermostat[s] ... run a process control program stored in the memory to accurately measure the temperature of a temperature sensor disposed in the conditioned space and to send control signals to the heating and/or cooling equipment to closely control the temperature of the conditioned space.”).

132. Moreover, it was well known in the art that thermostat systems include “4) a real time clock” as acknowledged by the ’825 Patent. EX1001, Figure 1.

Figure 1 of the '825 Patent, labeled as “PRIOR ART,” includes a “settable real time clock.” *Id.*, Figure 1, 4:29; *see also id.* at 1:29-30 (“[m]any modern thermostat[s] include a real time clock”). The '825 Patent itself admits that its “clock 13, in accordance with the present invention includes a real time clock module 30 which is an *off-the-shelf* integrated circuit component.” *Id.*, 5:24-29 (emphasis added).

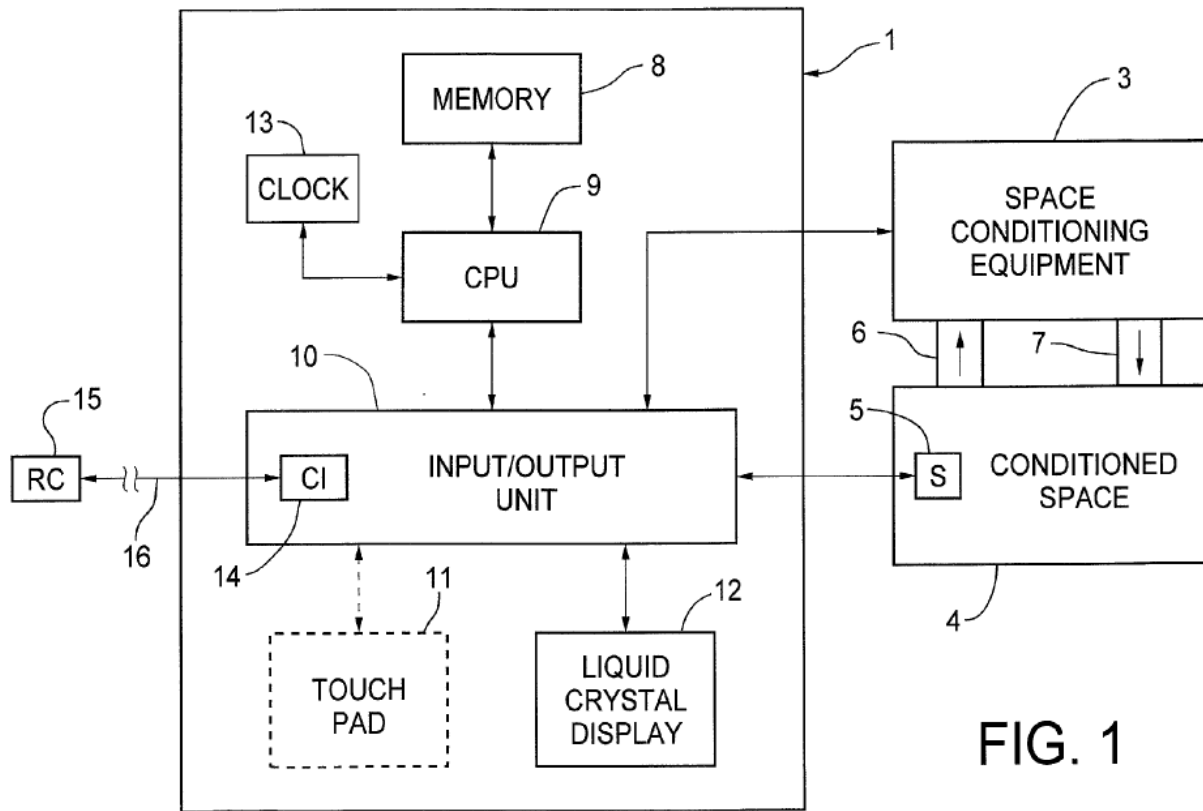
133. It was also well known in the art that thermostat systems include memory, as acknowledged by the '825 Patent. EX1001, 1:29-30 (“Many modern thermostat[s] include ... a memory”). Figure 1 of the '825 Patent, labeled as “PRIOR ART,” illustrates that “an exemplary thermostat includes a processor 1” which “includes ... a memory 8 for storing data and program information.” *Id.*, Figure 1, 4:9-10, 4:23-24. The '825 Patent further admits that “[a]s a practical matter, as the state of the art of circuit integration progresses, most or all the components of a programmable thermostat according to the invention may be incorporated as a single configurable and programmable integrated circuit or in a very few chips.” *Id.*, 5:38-42.

134. Further, it was well known in the art for thermostat systems to include a control program stored in memory, as acknowledged by the '825 Patent. EX1001, 1:29-31 (“Many modern thermostat[s] include a ... control program stored in the memory”).

(ii) 1[Pre]: “A programmable thermostat for controlling space conditioning equipment comprising:”

135. If the preamble is limiting, *Rosen* discloses it. The '825 Patent does not purport to have invented a programmable thermostat for controlling space conditioning equipment; those existed many years prior to the filing of the '825 application. EX1001, 5:28-35 (“Many modern thermostat[s] ... run a process control program ... to send control signals to the heating and/or cooling equipment to closely control the temperature of the conditioned space.”).

136. *Rosen* discloses “[a] programmable thermostat for controlling space conditioning equipment.” EX1004, Abstract, ¶0007. *Rosen* is titled “**Programmable Thermostat** System Employing A Touch Screen Unit For Intuitive Interactive Interface With A User.” *Id.*, Title (emphasis added). In particular, *Rosen* claims “[a] programmable thermostat system for controlling space conditioning equipment” as recited in preamble 1[Pre]. *Id.*, Claim 1. Figure 1 of *Rosen*, reproduced below, is nearly identical to Figure 1 of the '825 Patent and “is a block diagram of a first embodiment of a space conditioning system incorporating a thermostat system employing the present invention.” *Id.*, ¶0009.



Id., Figure 1; *see also id.*, ¶¶0001, 0003-0005, 0024 (describing a “programmable thermostat system”), 0037, Figures 3-11. Accordingly, based on my current analysis, *Rosen* discloses preamble 1[Pre].

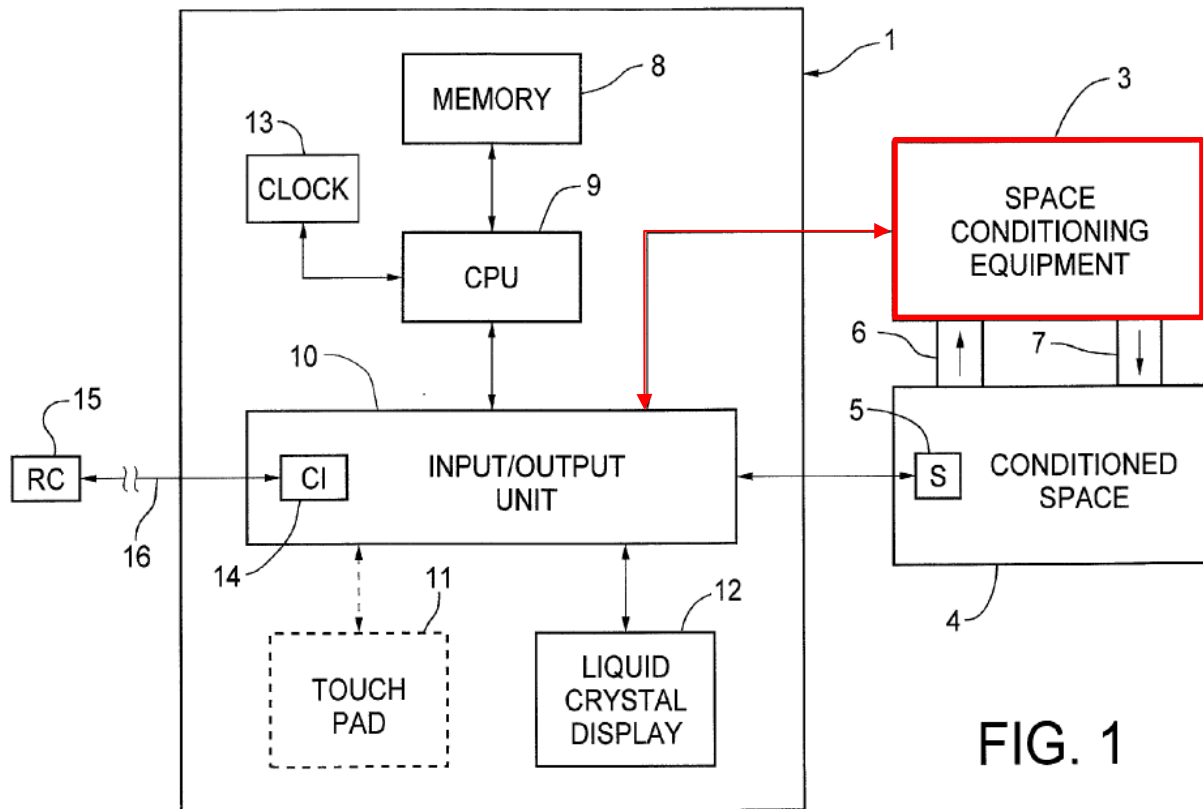
(iii) “1[a]: “A) means coupling suitable power for energizing said thermostat from said space conditioning equipment to said thermostat;”

137. *Rosen* or *Rosen* coupled with the general knowledge of a POSITA, or *Rosen* in combination with *Cacciatore* discloses element 1[a]. As discussed above, I understand that this claim element is governed by 35 U.S.C. § 112, ¶6. *Supra*, § V.F.1. The function is “coupling suitable power for energizing said thermostat from said space conditioning equipment to said thermostat,” and I am assuming the

corresponding structure to be a (power) line and any equivalents. *Id.* The disclosure of this claim element is discussed above in Section VII.C.1.i. That discussion is incorporated by reference here.

138. It was well known in the prior art to use space conditioning equipment to provide energizing power to a thermostat. Indeed, the '825 Patent acknowledges that the use of space conditioning equipment to supply power to a thermostat system was “conventional[.]” EX1001, 5:3-5; *see also id.*, Figure 1, 2:18-19,5:43-46; *see also* EX1013, 98:16-18.

139. *Rosen* discloses that its programmable thermostat “may be suitably powered by a battery [] and/or from equipment to which is connected” (e.g., space conditioning equipment). EX1004, ¶0020. Annotated Figure 1 below depicts the space conditioning equipment connected to the programmable thermostat of *Rosen* for control purposes:



Id., Figure 1 (annotated); *see also id.*, ¶0009 (“FIG. 1 is a block diagram of a space conditioning system incorporating a thermostat system employing the present invention”). From the passage of paragraph 20 quoted above, a POSITA would understand that *Rosen* discloses the claimed function of coupling suitable power for energizing the thermostat from the space conditioning equipment to the thermostat.

140. For the reasons discussed above in the section on motivation to combine, a POSITA would understand *Rosen* to be teaching that the power is obtained via a power line. *Supra* § VII.C.1.i. This is especially true in light of the general knowledge of a POSITA as acknowledged in the '825 Patent, that it is conventional to supply power by connecting the thermostat to the space conditioning

equipment via a power line (wiring). EX1001, 5:3-5. It certainly would be obvious to use what is admitted as “conventional” in the specification to supply power.

141. If the Board determines that an “isolation diode” to protect the battery is part of the corresponding structure, it would be obvious to use a line to connect the thermostat to the power source and to protect the backup battery with an isolation diode. The ’825 Patent teaches that power is “conventionally supplied” using a power line and an isolation diode to protect the battery. EX1001, 5:3-5. Inventor Rosen agreed that the isolation diode to protect the battery is prior art. EX1013, 96:9-97:6. Thus, it is obvious to use this prior art method of supply power that reflects the general knowledge of a POSITA.

142. If the Board disagrees with this, then the power line and a diode to protect the battery (an isolation diode) is obvious to use given the teachings of *Cacciatore*.

143. *Cacciatore* discloses a “programmable electronic digital thermostat” that includes a “power supply circuit utilizing an external power source of the temperature conditioning system” to supply power using “conventional existing wiring.” EX1005, Abstract, 2:14-15. As discussed above, a POSITA would understand the temperature conditioning system from which power is supplied to be a furnace, air conditioning unit, or heat pump. *Id.*, Abstract, 1:18-22.

144. The “power supply circuit” of *Cacciatore* includes a power line and diode in the circuit for supplying power. *Id.*, 5:23-27, 6:16-21; *see also id.*, 5:67-7:45 (discussing diodes). Particularly, *Cacciatore* discloses “a terminal ... that is connected to the common **28 volt AC supply line** of the temperature conditioning system” wherein a “[r]ectified voltage is supplied by the bridge rectifier 100 for the operating power supply 30. The negative output of the bridge rectifier is coupled through a series combination of a diode 108 and a resistor 110 to an input 112 of a voltage regulator integrated circuit device 114.” *Id.*, 5:23-25 (emphasis added), 5:64-69.

145. Moreover, *Cacciatore* also discloses protecting a backup battery via an isolation diode. EX1005, Figure 2, 6:48-58. Because *Cacciatore* relates to the art of thermostat systems, a POSITA would have recognized that *Cacciatore*’s power supply configuration is suitable for use in the programmable thermostat system of *Rosen*.

146. *Cacciatore* teaches using equipment from the temperature conditioning system (i.e., space conditioning equipment) to supply energizing power for a thermostat via a power supply circuit and wiring that includes a power line and an isolation diode, which discloses the corresponding structure for coupling suitable power for energizing said thermostat from said space conditioning equipment to said thermostat.

147. Based upon the above, *Rosen* and/or the general knowledge of a POSITA discloses the identical structure called for by the construction of the means plus function element of Claim 1[a]. Also, *Cacciatore* discloses the identical structure called for by the construction of the means plus function element of Claim 1[a]. To the extent the identical structure is not disclosed, the structure disclosed by (a) *Rosen*, (b) the general knowledge of a POSITA and (c) *Cacciatore* are all at least equivalent to the corresponding structure for element 1[a] because each disclosure concerns insubstantially different structure that can be interchanged with the disclosed structure to power the thermostat.

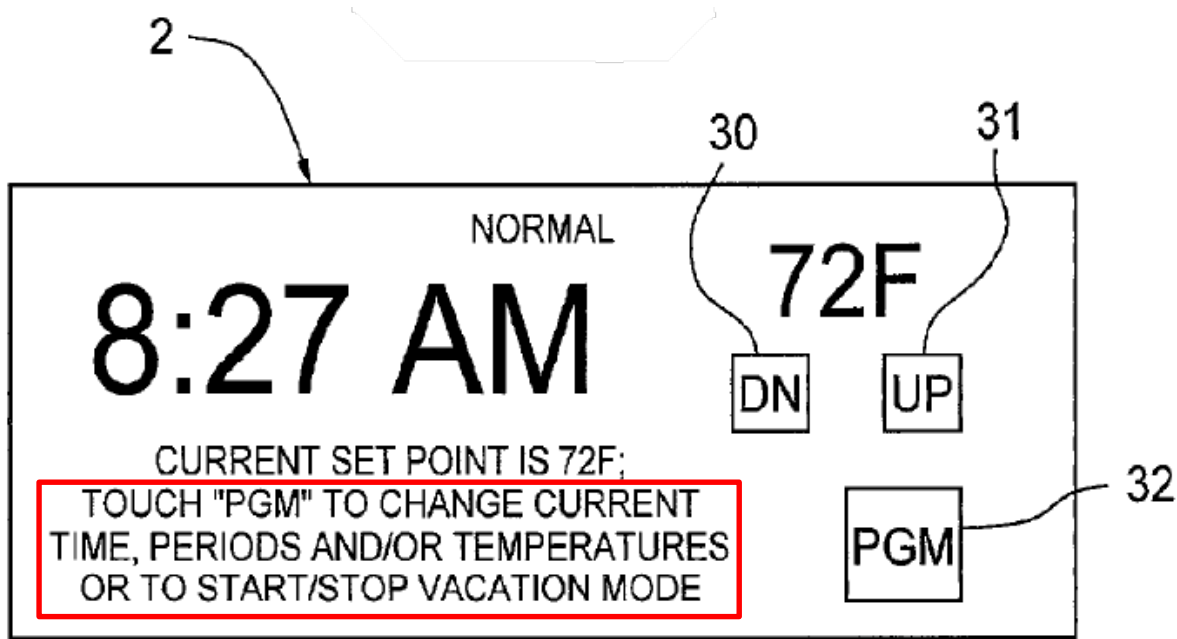
148. As described above in Section VII.C.1.i, it would have been obvious to a POSITA to combine *Cacciatore*'s teachings to supply energizing power from space conditioning equipment to the thermostat system of *Rosen*. *Supra*, § VII.C.1.i. Indeed, modifying *Rosen* to incorporate the *Cacciatore*'s teachings would merely involve the application of a known technique (supplying power to a thermostat system from space conditioning equipment using a power line and, if desired, employs an isolation diode, as taught by *Cacciatore*) to a known device (the thermostat system of *Rosen*) to obtain predictable results (a thermostat system that receives energizing power from space conditioning equipment via a power line and, if desired, employs an isolation diode). Accordingly, based on my current analysis,

Rosen as modified by *Cacciatore* discloses and suggests to a POSITA each limitation of element 1[a].

(iv) 1[b]: “B) an interactive interface for a user to enter programming information into said thermostat;”

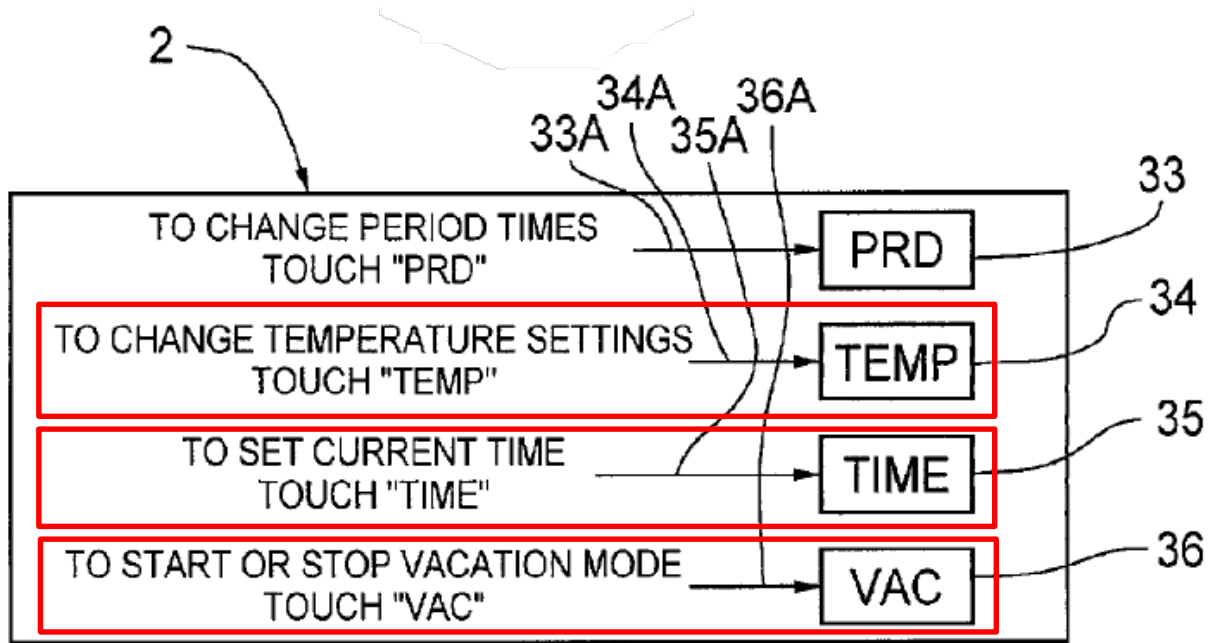
149. *Rosen* discloses element 1[b]. The ’825 Patent does not purport to have invented an interactive interface for a user to enter programming information into said thermostat or improved upon existing interactive interfaces for a user to enter programming information into said thermostat.

150. *Rosen* discloses “a touch screen, for interactive intuitive interface with a user to facilitate programming the thermostat system.” EX1004, ¶0001. *Rosen* further discloses “programmable thermostat systems in which ... programming steps have been entered using a ‘tactile’ touch pad while observing a display.” *Id.*, ¶0024. *Rosen* displays “[d]ifferent menus [that] can place [] buttons and messages in various positions on the touch screen to facilitate intuitive programming of the thermostat system.” *Id.*, Abstract. For example, Figure 3 of *Rosen* illustrates buttons to enter various programming information into the thermostat, such as current time, periods, and/or temperatures or to start/stop vacation mode. *Id.*, ¶0028.



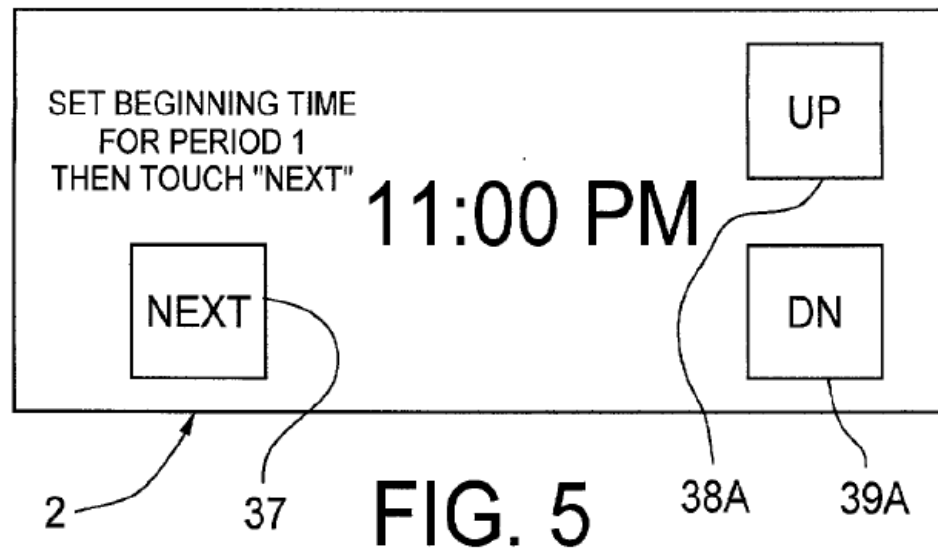
Id., Figure 3 (annotated).

151. In addition to the “high level interactive interface” shown in Figure 3 above, *Rosen* provides examples of “intermediate” and “low level” interactive interfaces displayed on the touch screen during normal operations. *Id.*, ¶¶0012-0018. For example, “[i]f the button 32 [in Figure 3] is touched, a menu such as that shown in FIG. 4 replaces (using display information prestored in memory 8) the display shown in FIG. 3.” *Id.*, ¶0029. Figure 4 of *Rosen* below “is an exemplary pictorial of an intermediate level interactive interface displayed on the touch screen.” *Id.*, ¶0012.



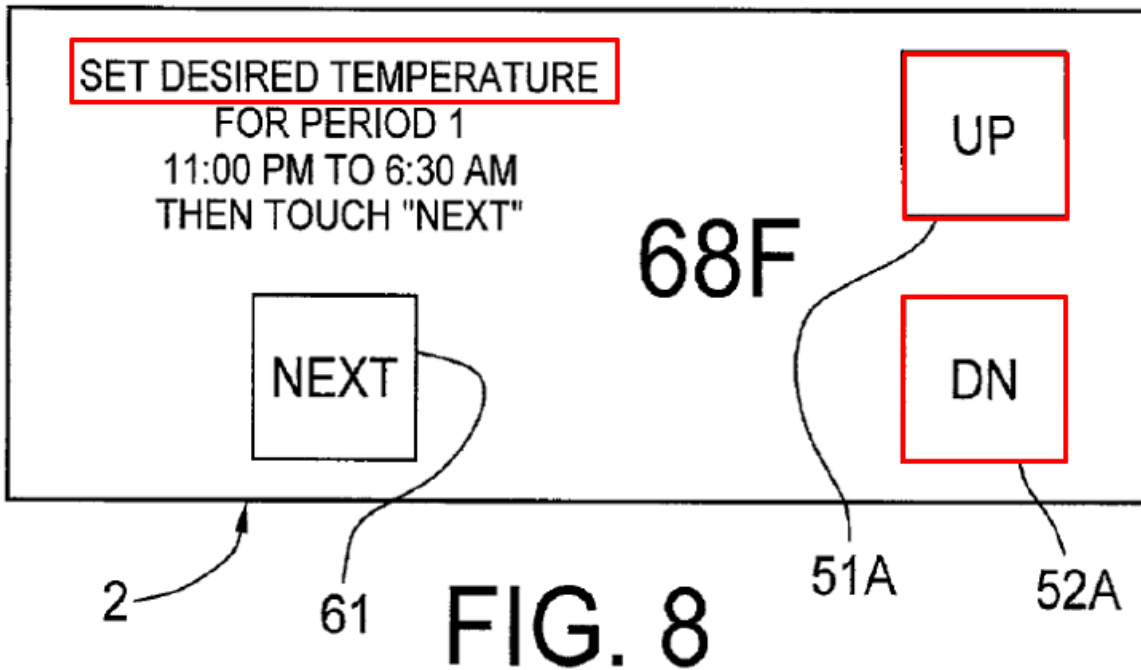
Id., Figure 4 (annotated).

152. *Rosen* describes that if a user wishes to change the period times by pressing the "PRD" button 33, the "processor 1 causes a lower level menu such as that shown in FIG. 5 to be displayed." *Id.*, ¶0032. Figure 5 "is an exemplary pictorial of a low level interactive interface displayed on the touch screen." *Id.*, ¶0013.

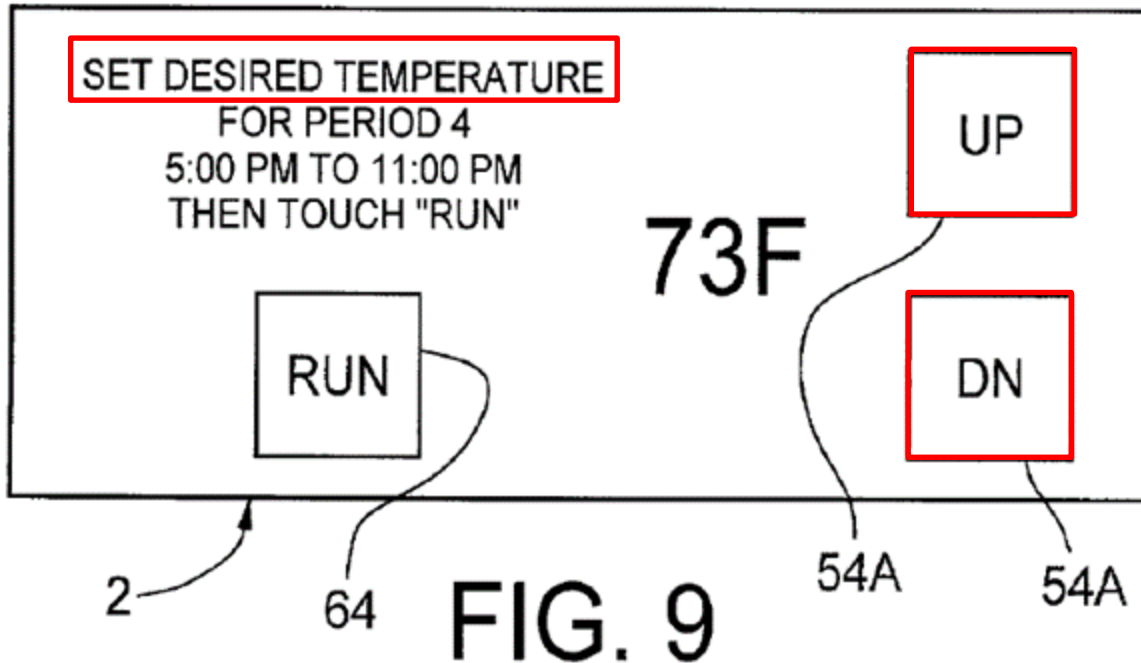


Id., Figure 5. As can be seen above, each of the high level, intermediate level, and low level interactive interfaces in Figures 3, 4, and 5, respectively, allows a user to enter programming information (e.g., time, temperature, mode of operation) into the thermostat.

153. Figures 8 and 9 of *Rosen* further disclose programming information that users can enter into the thermostat using the interactive interfaces discussed above. For example, users can touch the “UP” and “DN” buttons in Figures 8 and 9 to “set [a] desired temperature.” EX1004, Figures 8, 9.



Id., Figure 8.



Id., Figure 9 (annotated). Accordingly, based on my current analysis, *Rosen*

discloses element 1[b].

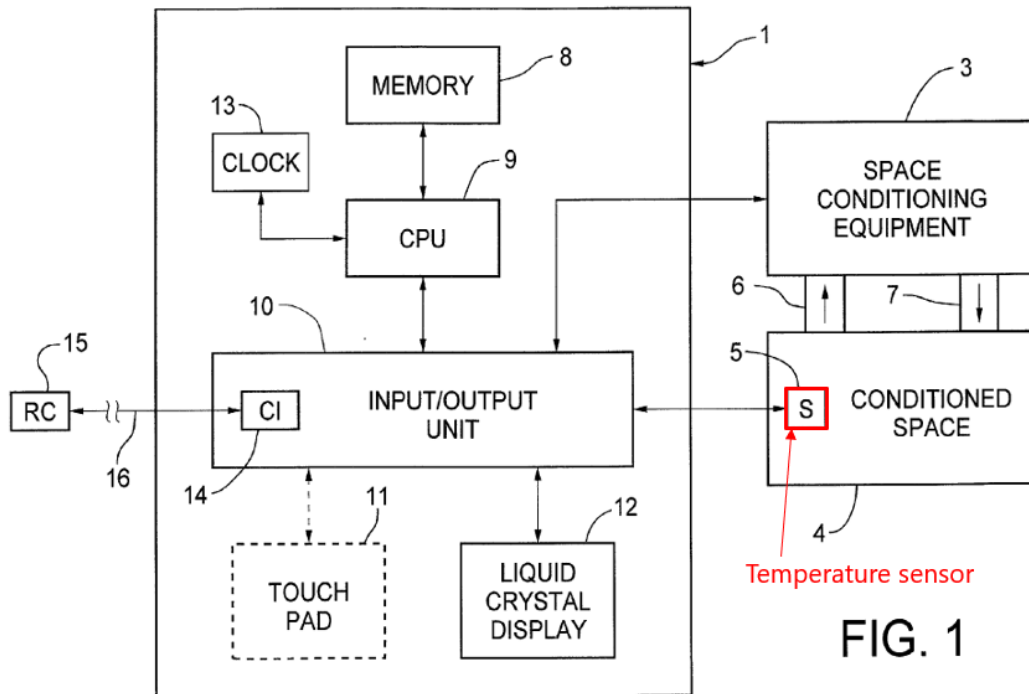
- (v) **1[c]: “C) a temperature sensor for providing an electrical signal indicative of the temperature of a conditioned space in which the temperature sensor is situated;”**

154. *Rosen* discloses element 1[c]. The ’825 Patent does not purport to have invented a temperature sensor for providing an electrical signal indicative of the temperature of a conditioned space or improved upon existing temperature sensors. It was well known in the art that thermostat systems include a temperature sensor for providing an electrical signal indicative of the temperature of a conditioned space, as acknowledged by the ’825 Patent. EX1001, Figure 1, 5:28-35.

155. The use of temperature sensors with thermostat systems was well known before the priority date of the ’825 Patent. *See, e.g.*, EX1004, ¶0002 (“Thermostats have been used for many years as a temperature sensitive switch which controls heating and/or cooling equipment for conditioning a space in which the thermostat, or a temperature sensor connected to the thermostat, is placed.”), and ¶0003 (explaining that “[m]any modern thermostat systems include . . . a data processor to run a process control program stored in the memory to accurately measure the temperature of a temperature sensor disposed in the conditioned space”).

156. *Rosen* discloses that its “programmable thermostat system for controlling space conditioning equipment according to [its] invention includes ... a

temperature sensor for providing an electrical signal indicative of the temperature of a conditioned space,” as recited in element 1[c]. EX1004, ¶10007; *see also id.*, Claim 1 (reciting “a programmable thermostat system for controlling space conditioning equipment comprising: . . . a temperature sensor for providing an electrical signal indicative of the temperature of a conditioned space in which the temperature sensor is situated”). Figure 1 of *Rosen*, annotated below, illustrates “a thermostat system” that includes “a temperature sensor 5 which is disposed in a conditioned space 4.”



Id., Figure 1 (annotated). *Rosen* discloses that, “in the usual manner during normal operation, the temperature sensor 5 sends an electrical signal (e.g., if the sensor 5 is a simple thermistor, a resistance value; several types of temperature sensors are widely used) representative of the temperature within the conditioned space 4[.]”

Id., ¶0022. Thus, *Rosen* discloses element 1[c].

(vi) Elements 1[d]-1[g]

1[d]: “D) a processor, said processor including:”

1[e]: “1) a central processing unit;”

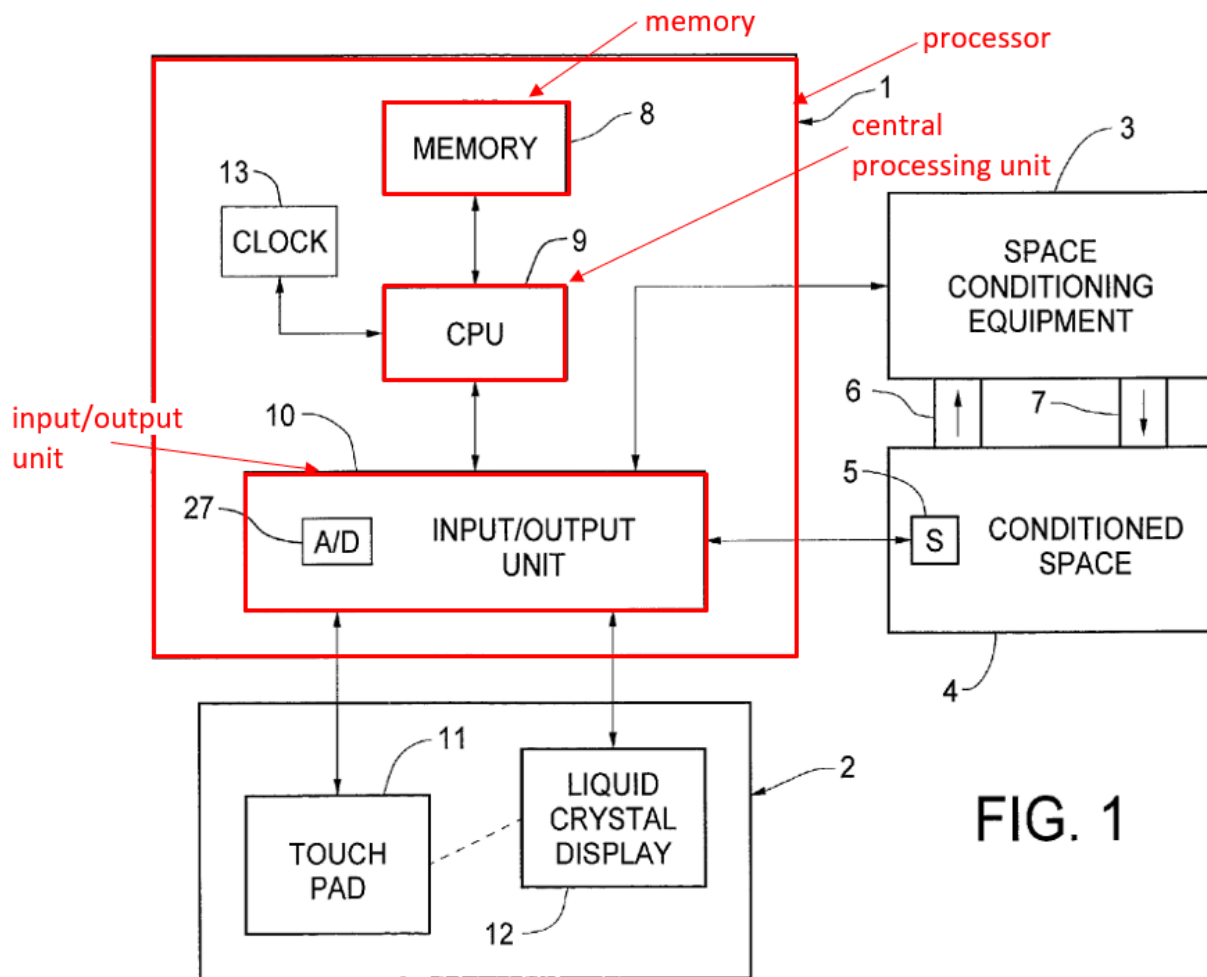
1[f]: “2) a first memory coupled to said central processing unit for storing program and data information; and”

1[g]: “3) an input/output unit including:”

157. *Rosen* also discloses elements 1[d]-1[g]. The '825 Patent does not purport to have invented any of these elements or improved upon existing versions of these elements. It was well known in the art that thermostat systems include these elements, as acknowledged by the '825 Patent. EX1001, Figure 1. *Rosen* discloses that its “programmable thermostat system for controlling space conditioning equipment according to the invention includes ... a processor including: a central processing unit, a real time clock, a memory coupled to the central processing unit for storing program and data information; and an input/output unit coupled between the processor and said touch screen for carrying out information transfer therebetween.” EX1004, ¶0007.

158. More particularly, *Rosen* Figure 1 illustrates “a thermostat system” that “includes a processor 1.” *Id.*, ¶0019. “The processor 1 includes a central processing unit (CPU) 9 in communication with a memory 8 for storing data and program information and also, via an input/output unit (I/O unit) 10, a touch pad 11 and a

liquid crystal display (LCD) 12.” *Id.*, ¶0020. The *Rosen* thermostat system “facilitate[s] diverse operations, such as different temperature set points (desired temperatures), during different periods of the day cycle.” *Id.* *Rosen* discloses a processor (element 1[d]), including a central processing unit (element 1[e]), a memory for storing program and data information (element 1[f]), and an input/output unit (element 1[g]) as shown in annotated Figure 1 below:



Id., Figure 1 (annotated); see also *id.*, Claims 1, 17 (reciting a processor including the features of elements 1[d]-1[g]), Claim 17 (reciting a processor including the

features of elements 1[d]-1[g]). As can be seen from Figure 1 above, “memory 8” is coupled to central processing unit 9. *See id.*, Figure 1; *see also id.*, ¶0020 (describing “central processing unit (CPU) 9 in communication with a memory 8”). As quoted above, *Rosen* states that the memory stores program and data information. The memory of *Rosen* is a “first memory” as claimed. The input/output unit is labeled as 27 in Figure 1 and identified as such in the passage quoted above. Thus, *Rosen* discloses elements 1[d]-1[g].

(vii) Elements 1[h]-1[j]

1[h]: “a) a sensor input coupled to said temperature sensor for receiving said electrical signal therefrom; and”

1[i]: “b) a control output coupled to the space conditioning equipment for issuing control signals thereto;”

1[j]: “4) a real time clock;”

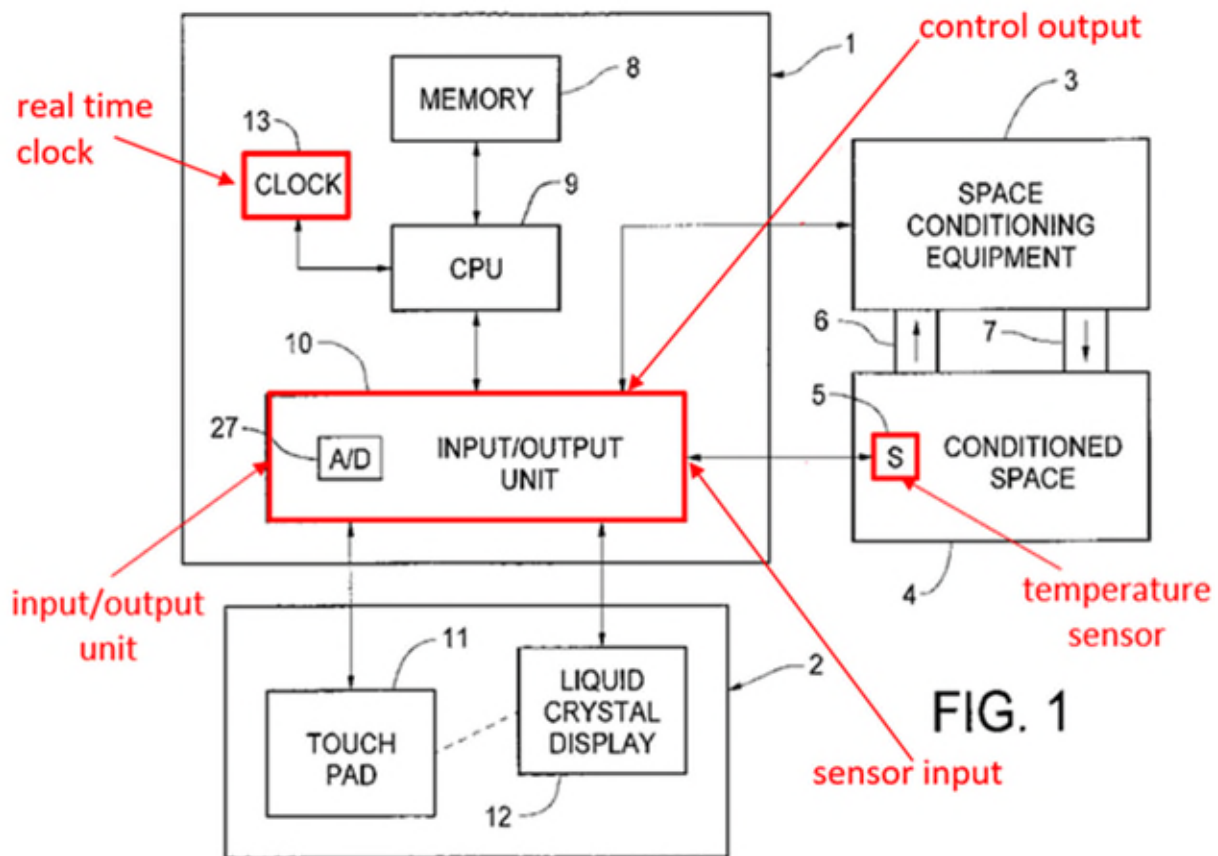
159. *Rosen* discloses elements 1[h]-1[j]. The '825 Patent does not purport to have invented any of these elements or improved upon existing versions of these elements. Moreover, it was well known in the art that thermostat systems include these elements, as acknowledged by the '825 Patent. EX1001, Figure 1. As discussed above for element 1[g], *Rosen* discloses the claimed input/output unit. *Supra*, § VII.C.2.vi; EX1004, Figure 1, ¶0007. *Rosen*'s input/output unit includes the features recited in elements 1[h]-1[i]. For instance, *Rosen*'s Claim 1 and Claim 11 disclose elements 1[h] and 1[i] verbatim: “[a] programmable thermostat for

controlling space conditioning equipment comprising: . . . a processor, said processor including: . . . an input/output unit including:

a) a sensor input coupled to said temperature sensor for receiving said electrical signal therefrom; [and]

b) a control output coupled to the space conditioning equipment for issuing control signals thereto[.]”

EX1004, Claim 1; *see also id.*, Claim 11 (reciting the same features). These features of *Rosen* input/output unit are shown in annotated Figure 1 below:



Id., Figure 1 (annotated). The description of Figure 1 provides further disclosure of

elements 1[h]-1[i]. EX1004, ¶0022.

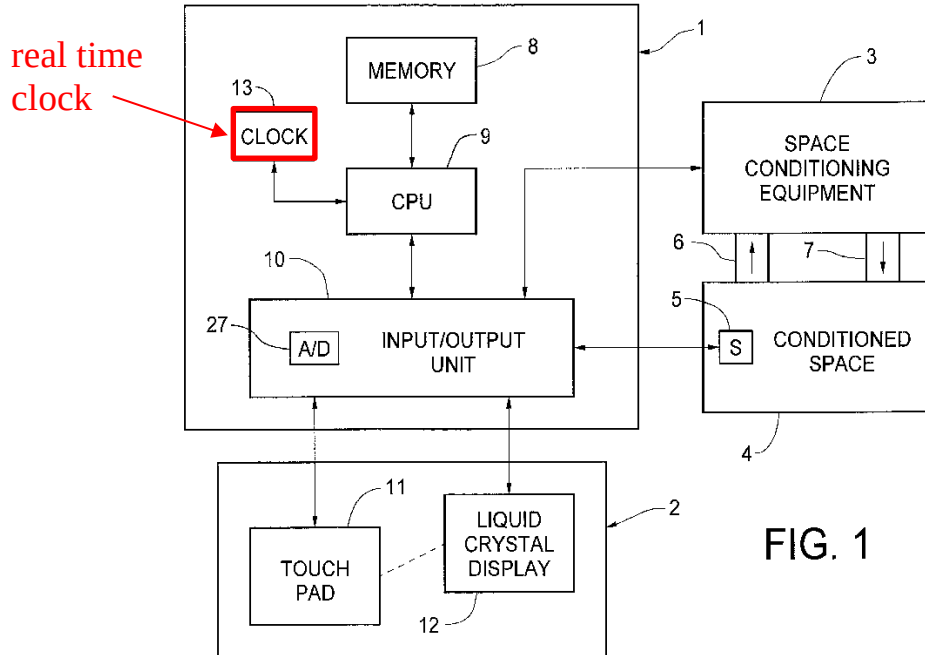
160. With respect to Figure 1, *Rosen* describes that:

Thus, in the usual manner during normal operation, ***the temperature sensor 5 sends an electrical signal*** (e.g., if the sensor 5 is a simple thermistor, a resistance value; several types of temperature sensors are widely used) ***representative of the temperature within the conditioned space 4 which the processor can compare against a previously entered set point to determine if control signals need to be sent to the space conditioning equipment 3.*** For example, if the temperature in the conditioned space 4 is found to be too low when operation is in the heating mode, the processor 1 signals the space conditioning equipment 3 circulate, through ducts 6, 7, air from/to the conditioned space 4 which is heated by the space conditioning equipment before return to the conditioned space.

Id. Thus, *Rosen* discloses that its processor 1 has an input/output unit 10 that includes “a sensor input coupled to said temperature sensor for receiving said electrical signal therefrom” (e.g., the input to I/O unit 10 from temperature sensor 5 in Figure 1) and “a control output coupled to the space conditioning equipment for issuing control signals thereto” (e.g., the output from I/O unit 10 to space conditioning equipment 3 in Figure 1) as recited in elements 1[h] and 1[i], respectively.

161. *Rosen* also discloses element 1[j]. *Rosen* discloses “[a] programmable thermostat system for controlling space conditioning equipment includ[ing] ... a real time clock.” EX1004, Abstract; *see also id.*, ¶0020 (“A settable real time clock 13 is used to keep time in the thermostat system to facilitate diverse operations”). The

real time clock 13 of the thermostat system of *Rosen* is shown in annotated Figure 1 above. *Id.*, Figure 1.

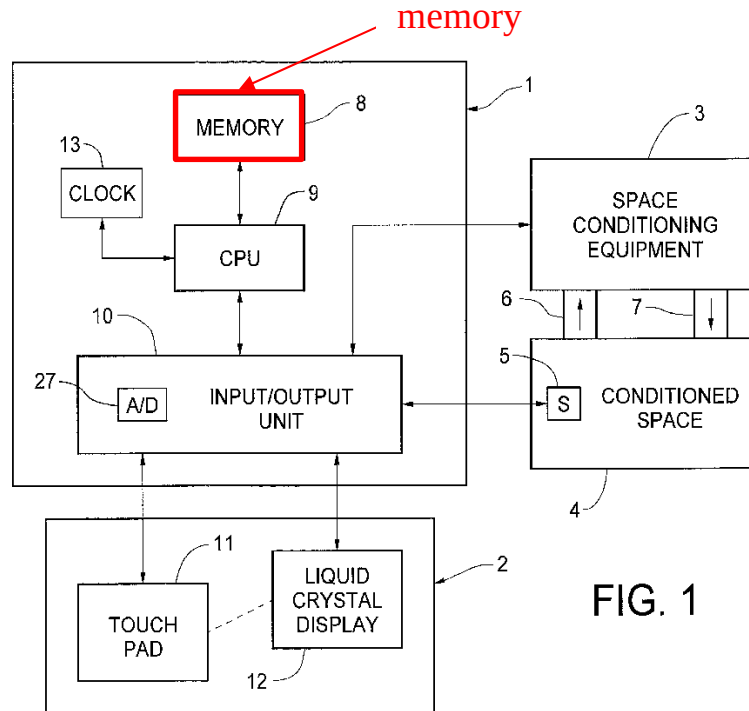


Id., Figure 1. Thus, *Rosen* discloses elements 1[h], 1[i], and 1[j].

(viii) 1[k]: “5) a non-volatile random access memory; and”

162. *Rosen* in combination with *Shigeaki* discloses element 1[k]. The '825 Patent does not purport to have invented a non-volatile random access memory or improved upon existing memory. Moreover, it was well known in the art that thermostat systems include memory, as acknowledged by the '825 Patent. EX1001, 1:29-30 (“Many modern thermostat[s] include ... **a memory**”) (emphasis added); see also *id.*, Figure 1. *Rosen* discloses that its thermostat system includes a “memory 8

[that] may include a ... random-access part which stores data subject to change during operation” as shown in annotated Figure 1 below:



EX1004, ¶0020, Figure 1 (annotated).

163. Although *Rosen* discloses random access memory, *Rosen* does not expressly disclose a **non-volatile** random access memory. *Rosen*’s teaching of “memory 8 for storing data and program information” makes obvious to a POSITA that the memory of *Rosen* would be non-volatile. *Id.*, ¶0020. If the program were not stored in non-volatile memory, the program would need to be loaded into the thermostat anytime there was a power failure. A POSITA would understand *Rosen*’s teaching of “storing program and data information” to disclose and/or make obvious the use of non-volatile memory. *Id.*, ¶0007, Abstract. Non-volatile memory was

well known in the art well before the priority date of the '825 Patent, including for use in thermostats. EX1013, 103:4-14. *Supra*, § VI.A. It was known to a POSITA prior to the claimed invention that the purpose of a non-volatile memory is to retain the contents of the memory even when no power is supplied to the memory. EX1013, 104:14-25.

164. It is not surprising that *Shigeaki* discloses this aspect of Claim 1. *Shigeaki* relates to “a clock device in which power for operation is supplied via a commercial power source.” EX1006, ¶0001. *Shigeaki* discloses “a semiconductor non-volatile memory capable of storing data and electrically rewriting the stored data” as well as a “data reading means [that] reads time data and power outage data from the semiconductor non-volatile memory” when power is recovered after a power outage. EX1006, Claim 1, ¶0014; *see also id.*, Claim 2, ¶¶0007-0008. Specifically, *Shigeaki* discloses an EEPROM for this purpose. EX1006, ¶0061 (referred to as E²PROM).

165. When *Shigeaki*'s teachings are applied to *Rosen*, in the combined system a non-volatile random access memory as taught by *Shigeaki* is added to store the clock information and retain it during a power outage. As described above in Section VII.C.1.ii, it would have been obvious to a POSITA to combine *Shigeaki*'s teachings of using non-volatile memory and its method of handling time during a power outage with *Rosen*'s programmable thermostat system to arrive at the claimed

invention including a non-volatile random access memory in element 1[k]. *Supra*, § VII.C.1.ii.

166. Indeed, modifying *Rosen* to incorporate the non-volatile memory disclosed in *Shigeaki* would merely involve the application of a known technique (the use of non-volatile memory as taught by *Shigeaki*) to a known device (*Rosen*'s thermostat system) ready for improvement to yield predictable results (a thermostat system with improved functionality in the case of power outages). Moreover, non-volatile random access memory was commonly used in thermostat systems before the priority date of the '825 Patent for other purposes such as retaining data such as the temperature setting and schedules for automatically changing the thermostat so those are not lost during a power outage. *Supra*, § VI.A. A POSITA would be motivated to include nonvolatile memory in a thermostat for that reason as well. Accordingly, based on my current analysis, the combination of *Shigeaki* and *Rosen* disclose and suggest to a POSITA element 1[k].

(ix) Elements 1[l]-1[n]

1[l]: “6) a control program stored in said first memory directing:”

1[m]: “a) said real time clock to periodically read its current time and date information into said non-volatile memory; and”

1[n]: “b) upon restart after a loss and then return of power from said space conditioning equipment, read the time and date information stored in said non-volatile memory into said real time clock.”

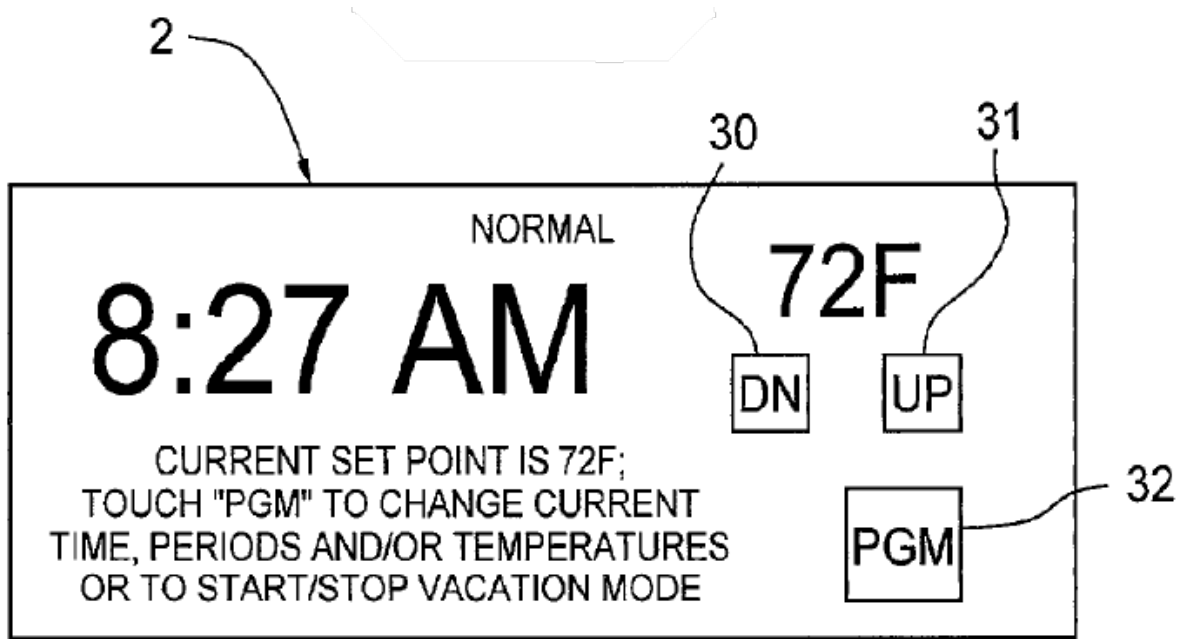
167. *Rosen* in combination with *Shigeaki* discloses elements 1[l] -1[n]. The '825 Patent does not purport to have invented the mere existence of a control program stored in memory. It was well known in the art for thermostat systems to include a control program stored in memory, as acknowledged by the '825 Patent. EX1001, 1:29-31 (“Many modern thermostat[s] include a ... control program stored in the memory”). *Rosen* discloses a “control program stored in the memory” of a thermostat system. EX1004, ¶0003; *see also id.*, Claim 1 (“a program stored in said memory”). Accordingly, based on my current analysis, *Rosen* discloses element 1[l].

168. *Rosen* in combination with *Shigeaki* discloses elements 1[m] -1[n]. As discussed above for element 1[j], the thermostat system of *Rosen* includes a “real time clock [] and a memory for storing ... data information.” EX1004, Abstract; *see also supra*, § VII.C.2.vii. As discussed above for element 1[k] *Shigeaki* discloses a nonvolatile memory. *Supra*, § VII.C.2.viii.



Id., Figure 1 (annotated). *Rosen’s* “real time clock 13 is used to keep time in the thermostat system to facilitate diverse operations, such as different temperature set points (desired temperatures), during different periods of the day cycle.” *Id.*, ¶10020.

169. *Rosen’s* interface also “prominently display[s]” the current time as shown below in Figure 3:



Id., ¶34, Figure 3.

170. Although *Rosen* discloses a thermostat system including a real time clock to keep time in the thermostat system, *Rosen* does not disclose that its real time clock periodically reads its current time and date information into said non-volatile memory and then reads the time from the non-volatile memory into the real time clock after a power failure. *Shigeaki* discloses these aspects of elements 1[m]-1[n].

171. *Shigeaki* discloses a “semiconductor non-volatile memory capable of storing data and electrically rewriting the stored data.” EX1006, Claims 1, 2, ¶¶0007-0008. The “data storage means” of *Shigeaki* “stores the current time and the fact of the occurrence of the power outage in the semiconductor non-volatile memory as the current time data and power outage data.” *Id.*, ¶0013. *Shigeaki* further discloses “a data storage means for allowing the timekeeping means to **store**

the following data in the semiconductor nonvolatile memory ... the data of the current time being measured by the remaining power and the fact that the power outage has occurred.” *Id.*, Claims 1, 2, ¶¶0007-0008 (emphasis added). Moreover, the “data storage means” of *Shigeaki* “stores the current time measured [by] the timekeeping means ... as the current time data.” *Id.*, ¶¶0013, 0039. A POSITA would understand that such storage occurs due to action by a control program, or at the very least that it would have been obvious.

172. *Shigeaki* further discloses that when “a power outage of the commercial power supply is restored, ... the data reading means reads time data and power outage data from the semiconductor non-volatile memory.” EX1006, ¶0014. When the system disclosed in *Shigeaki* detects that power has been restored, it reads the power failure data and time data from the non-volatile memory to update the display of the device. *Id.*, ¶0014-0015. “The data reading means reads the current time data and the power outage data from E²PROM 2 when power is restored after a power outage has occurred.” *Id.*, ¶0040.

173. The summary of what the control program of *Shigeaki* does is synonymous with elements 1[m]-1[n]. “When a power outage occurs, the time data pertaining to the current time is stored in E²PROM 2, and when power is restored, the time data is read from E²PROM 2, and the time is resumed from the current time corresponding to the retrieved time data.” EX1006, ¶61. A POSITA would

understand that *Shigeaki* discloses “periodic” storage and that the steps described in the prior paragraph are accomplished by a control program.

174. As described above in Section VII.C.1.ii, it would have been obvious to a POSITA to combine *Shigeaki*’s teachings of periodically storing time data into non-volatile memory and restoring the clock to that time after a power outage with *Rosen*’s programmable thermostat system. *Supra*, § VII.C.1.ii. When *Shigeaki*’s teachings are applied to *Rosen*, the real time clock of *Rosen* periodically reads its current time and date information into the non-volatile memory of the *Rosen-Shigeaki* combination as discussed above for element 1[k]). *Supra*, § VII.C.2.viii. Accordingly, based on my current analysis, the combination of *Shigeaki* and *Rosen* discloses and suggests to a POSITA elements 1[m]-1[n].

175. Claim 1 states that the program directs the real time clock to “periodically read its current time and date information into said nonvolatile memory.” In my experience, when a POSITA uses the term “periodically” with respect to storage of an item into a memory, they normally mean that the item is stored from time to time. In other words, at some undefined but reoccurring points in time, the storage occurs. Thus, I believe that *Shigeaki* discloses periodic storage. Whenever a periodic power outage occurs, the clock information is stored as well.

176. In some contexts, the term, “periodically,” refers to storage at regular time intervals—such as, for example, once per minute. The ’825 Patent does not

illuminate in which context it is using the term. Certainly, the '825 Patent does not state that the time is stored at regular intervals. Nor does the '825 Patent suggest that storage at regular intervals would be needed for the invention to function. Indeed, *Shigeaki* accomplishes the goals of the '825 Patent without needing to store the time at regular intervals.

177. However, it is general knowledge of a POSITA that if a program can direct storage of an item in memory, it could do so at regular intervals using a timer. It is standard for microprocessors to include a timer and interrupts to the processor are often generated when a timer expires so that the processor can perform various tasks at regular intervals. A POSITA reading *Shigeaki* would understand from their general knowledge that the storage could be performed at regular intervals in addition to when a power outage occurs. A reason to do might be as a fail-safe mechanism in case the storage upon occurrence of the power outage does not work for some reason. In fact, the *Aisa* reference discloses storage of the time in a nonvolatile memory “instant by instant” and that stored time is then used to reset the time of the real time clock after a power failure. EX1021, 4:62-5:5, 5:26-33. A POSITA would understand “instant by instant” storage to be storage at consecutive specific times which if not precisely regular intervals makes them obvious, as is consistent with the general knowledge of a POSITA that such storage is possible. Further, there are two primary ways to perform regular storage. One is to store with

a specific period (e.g. by waking or monitoring the time). The other is to perform repeatedly perform processing, storing, and sleeping. If the processing time is constant, this also results in periodic storage. However if the processing time is irregular and the sleep time constant, this approach results in regular but aperiodic storage. I have programmed both ways myself using basic knowledge of a POSITA. Given there are a small number of options, both approaches would be readily apparent and useable to a POSITA. Thus, *Shigeaki*, based upon the knowledge of a POSITA, would disclose to a POSITA storage of the clock value from time to time or at regular clock intervals—thus disclosing storage “periodically” whatever the meaning of the term in the claims of the ’825 Patent.

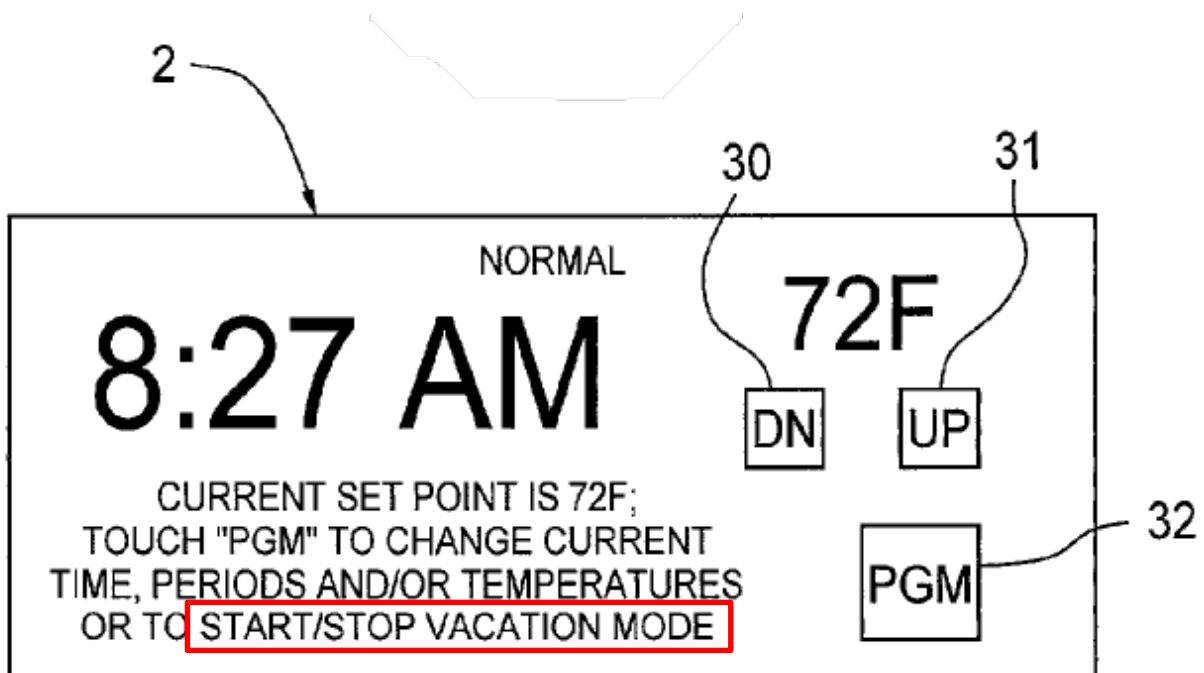
3. Claim 4: “The thermostat of claim 1 which includes a vacation mode of operation.”

178. The *Rosen-Cacciatore-Shigeaki* combined system discloses all elements in Claim 1 for the reasons discussed above for Claim 1. *Rosen* discloses the new elements of claim 4. The ’825 Patent does not purport to have invented a vacation mode of operation. It was well known in the art that thermostat systems often include vacation mode of operation, as acknowledged by the ’825 Patent. EX1001, 1:60-61 (“The operation of programmable thermostats in the vacation mode is straightforward and well known.”).

179. *Rosen* discloses a program that “may [] include a ‘vacation’ mode which employs different set points when the conditioned space is not occupied for

an extended period.” EX1004, ¶¶0003, 0035; *see also id.*, ¶0004, Figures 4, 11-12.

Thermostats that include a vacation mode of operation are well known in the art. *See, id.*, ¶0004 (“Typically, prior art programmable thermostat system[s] ... may include a ***vacation mode***.”) (emphasis added). In the annotated figures below *Rosen* illustrates how users can start, stop, or adjust vacation mode, and identifies the interface indicator present when the *Rosen* system is operating in vacation mode:



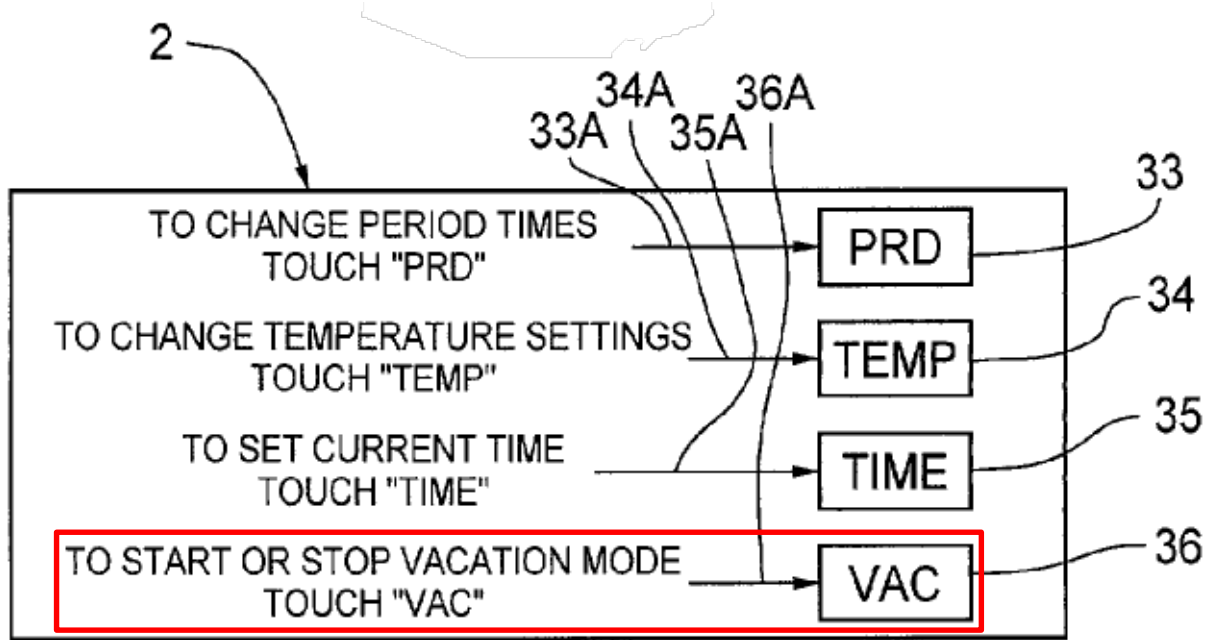


FIG. 4

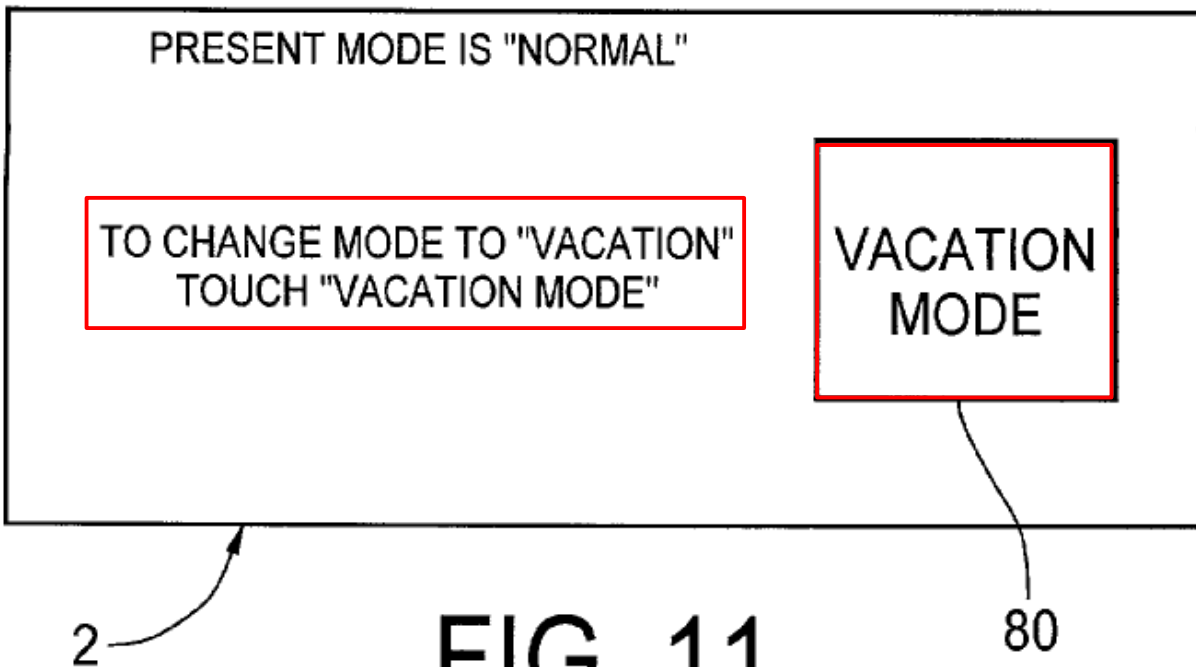
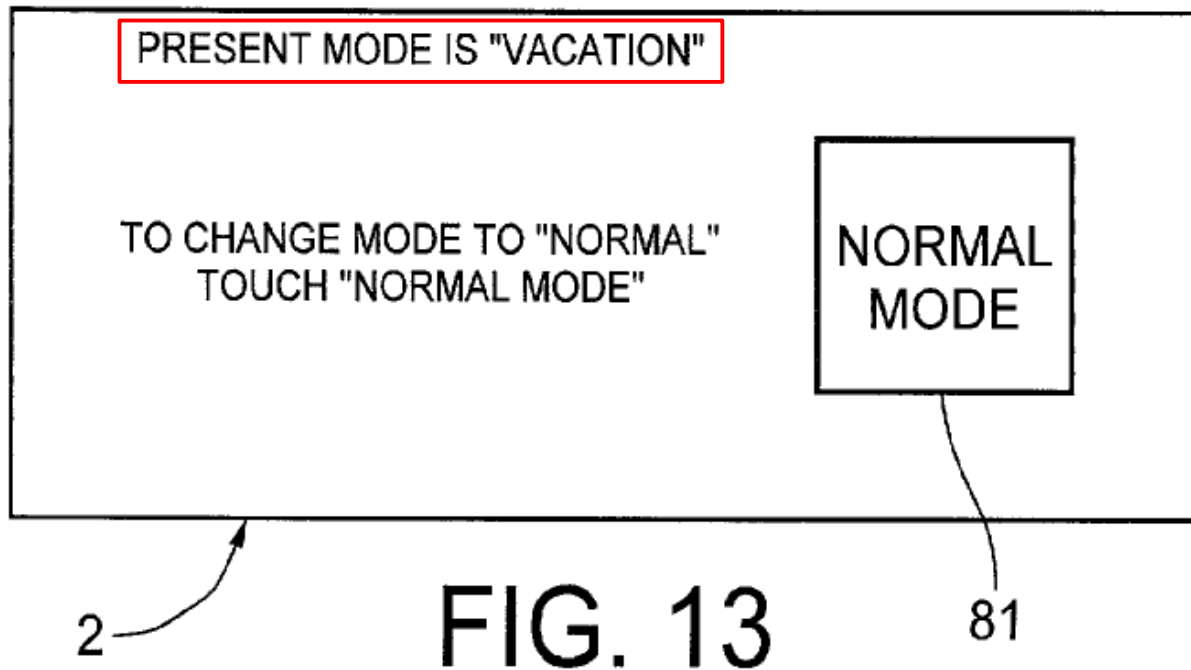
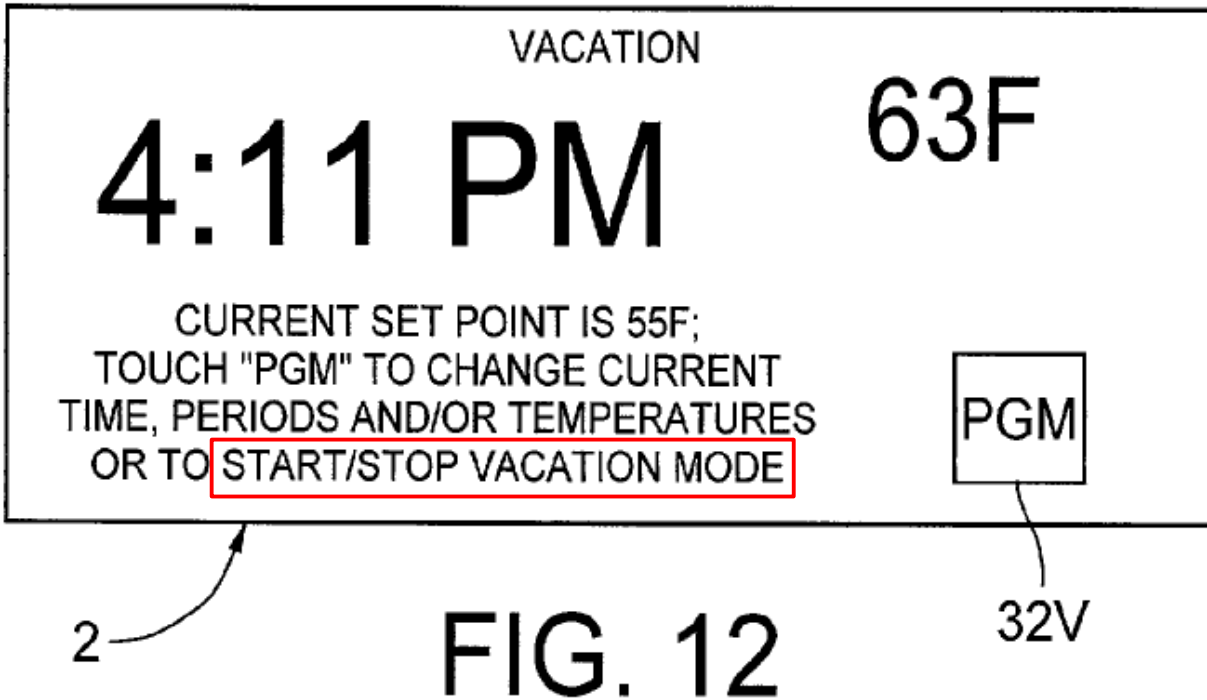


FIG. 11



Id., Figures 3-4, 11-13 (annotated); *see also id.*, ¶0035. *Rosen* thus discloses each additional limitation of Claim 4.

D. Ground 2: Claims 11-13 and 16 are obvious over *Rosen* in view of *Cacciatore*, and *Carey*

180. Based on the following analysis, I conclude that a POSITA at the relevant time (June 24, 2004) would have understood the limitations of Claims 11-13 and 16 were expressly disclosed, taught, or suggested by *Rosen* in combination with *Cacciatore*, and *Carey*.

1. Claim 11

(i) Elements 11[pre]-11[j]

11[pre]: “A programmable thermostat for controlling space conditioning equipment comprising:”

11[a]: “A) means coupling suitable power for energizing said thermostat from said space conditioning equipment to said thermostat;”

11[b]: “B) an interactive interface for a user to enter programming information into said thermostat;”

11[c]: “C) a temperature sensor for providing an electrical signal indicative of the temperature of a conditioned space in which the temperature sensor is situated;”

11[d]: “D) a processor, said processor including:”

11[e]: “1) a central processing unit;”

11[f]: “2) a first memory coupled to said central processing unit for storing program and data information; and”

11[g]: “3) an input/output unit including:”

11[h]: “a) a sensor input coupled to said temperature sensor for receiving said electrical signal therefrom; and”

11[i]: “b) a control output coupled to the space conditioning equipment for issuing control signals thereto;”

11[j]: “4) a real time clock; and”

181. Claim elements 11[pre]-11[j] are identical to claim elements 1[pre]-1[j] and are thus disclosed in the same manner as described in Sections VII.C.2.i-vii for claim elements 1[pre]-1[j]. For clarity, each of these elements is also common knowledge of a POSITA as admitted in the '825 Patent as explained in the introduction to Claim 1 above. *Supra*, § VII.C.2.i. Also, the analysis above in Section VII.C.1.i regarding combining of *Rosen* with *Cacciatore* applies to claim element 11[a] here as well.

(ii) **11[k]: “5) a receiver adapted to receive current time and date information from an external source of the current time and date, said receiver being coupled to said real time clock such that the time and date information thereof is updated from said receiver.”**

182. *Rosen* in combination with *Carey* discloses element 11[k]. Claim 11 is directed to a thermostat with a second method to try to maintain the time as accurately as possible in the event of a power outage. The second method, however is also disclosed in the prior art—e.g., by *Carey*. The '825 Patent acknowledges that the use of receivers adapted to receive time and date information from an external source and the use of such information to update the real time clock was “well known in the art.” EX1001, 6:13-24 (“a wireless *receiver 50 is tuned to a source of precision time* such as WWVB which operates at 60 khz. Such receivers are *well*

known in the art and ... can readily be incorporated into a thermostat. For example, a single chip WWVB receiver is available from Micro Analog Systems of Espoo, Finland, and is designated by part number MAS9178 in data sheet DA9178.000. *The output from the receiver 50 is ... the exact time ... and date. This information is used to periodically update the time and date information running in the real time clock 30.*”) (emphasis added). Thus, the prior art discloses the use of such receivers for thermostats.

183. As discussed above with respect to element 1[j], *Rosen* discloses a programmable thermostat system with a settable real-time clock. *Supra*, § VII.C.2.vii; *see also* EX1004, Abstract, ¶0020. *Rosen*, however, does not expressly disclose “a receiver adapted to receive current time and date information from an external source of the current time and date, said receiver being coupled to said real time clock such that the time and date information thereof is updated from said receiver.” EX1001, Claim 11. *Carey* discloses this aspect of element 11[k].

184. *Carey* discloses a programmable thermostat system that “automatically set[s] the current time and date using information broadcasted by station **WWVB**.” EX1007, ¶0004 (emphasis added); *see also id.*, Abstract. Similarly, the ’825 Patent explains that the claimed thermostat “includes a receiver for accessing precision time and date signals from, for example **WWVB**.” EX1001, Abstract (emphasis added). *Carey*’s thermostat includes an “antenna 22 [] tuned to receive a 60 kHz time code

signal broadcast from station WWVB in Fort Collins” and “a receiver integrated circuit 24 [that] detects and amplifies the time code signal.” EX1007, ¶¶0008-0009. Notably, “a small and relatively simple antenna and receiver can reliably decode the timecode signal from any location in the continental United States.” *Id.*, ¶0009.

185. Once *Carey*’s system receives and decodes a WWVB broadcasted time code signal, “the minutes, hours, day, and year information are stored into the [] RAM memory.” *Id.* *Carey*’s system then “loads the information from RAM memory into the local clock controlled by the microprocessor.” *Id.* This process is outlined in Figure 2 of *Carey*, annotated below:

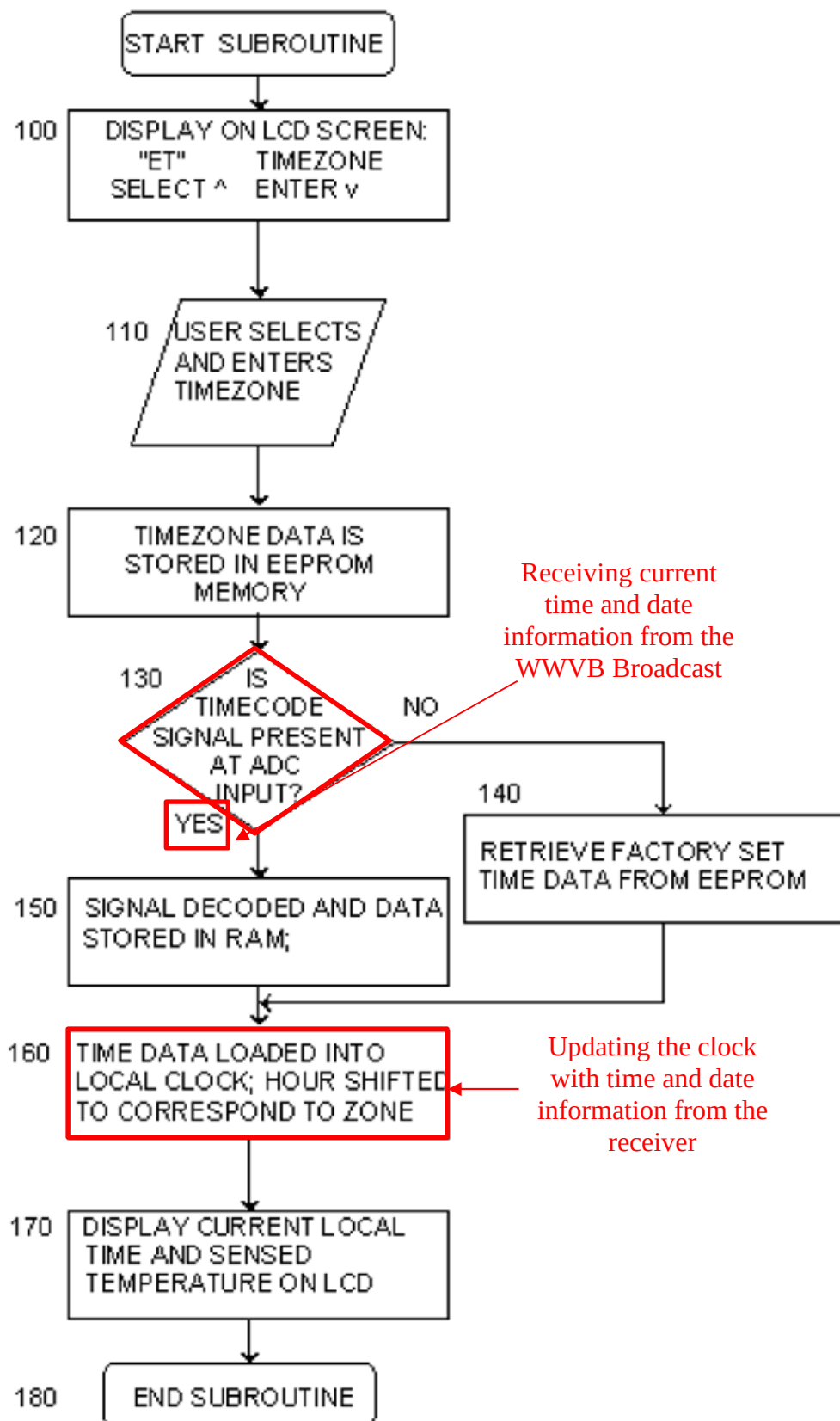


FIG. 2

Id., Figure 2 (annotated).

186. *Carey*'s microprocessor controls the local clock and "includes a digital input port pin, for decoding the time signal from the receiver 24," such that the receiver is coupled to the clock, as shown below in annotated Figure 1. *Id.*, ¶0009.

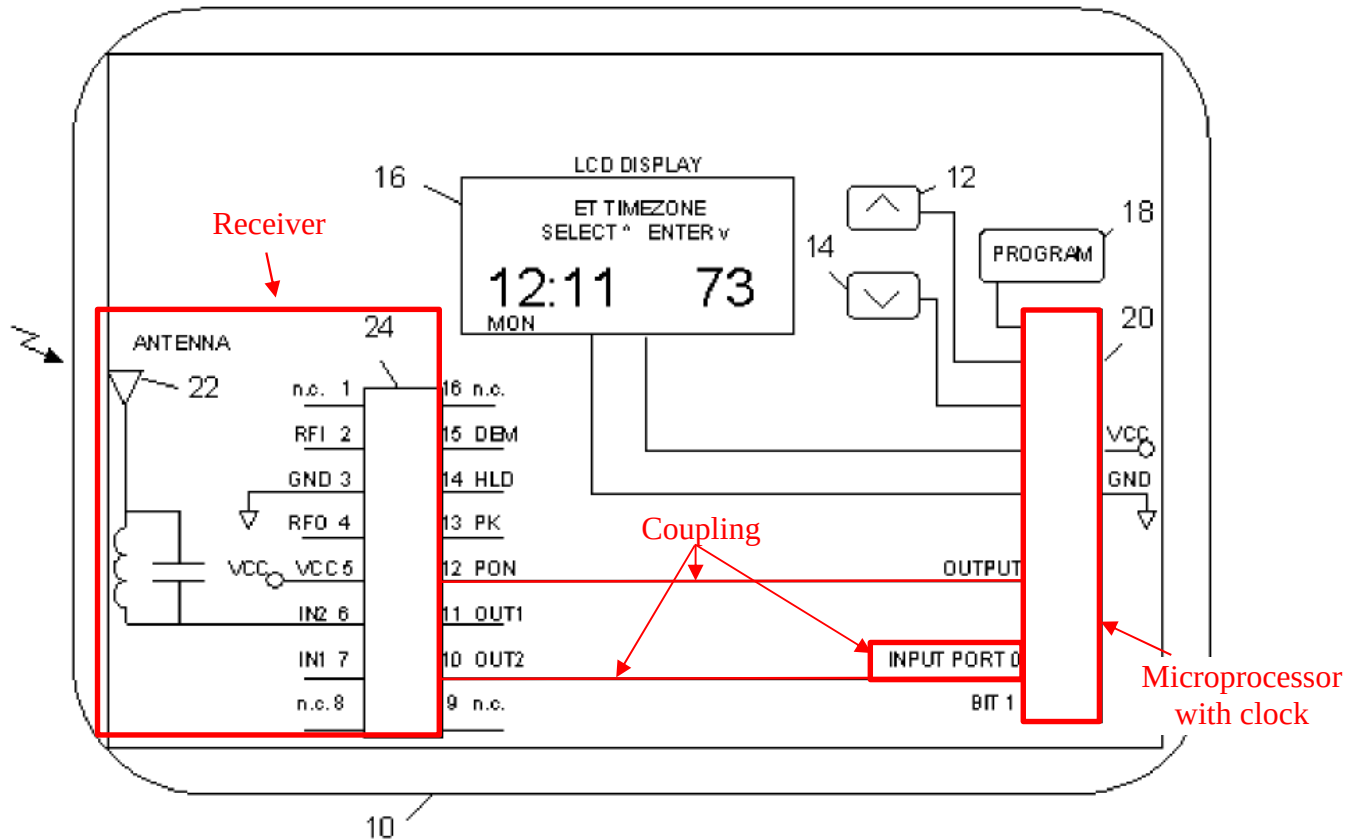


FIG. 1

Id., Figure 1 (annotated), ¶0008.

187. *Carey*'s receiver (WWVB antenna 22 along with integrated circuit receiver 24) is adapted to receive current time and date information (time code signals for minutes, hours, day, and year information) from an external source of the current time and date (the transmitter of the WWVB broadcasted time code signal),

said receiver being coupled via pins 10 and 12 of integrated circuit receiver 24 to said real time clock (coupled to the clock via the input port (“INPUT PORT 0”) of microprocessor 20 and the RAM) such that the time and date information thereof is updated from said receiver (loading minutes, hours, day, and year information stored in RAM memory into the clock). EX1007, ¶0009. Accordingly, based on my current analysis, the combination of *Carey* and *Rosen* together disclose each and every element of 11[k].

(a) Rationale and motivation for combining *Rosen* and *Carey*

188. It would have been obvious to a POSITA to combine *Carey*’s receiver with *Rosen*’s programmable thermostat system. Indeed, modifying the thermostat system of *Rosen* to incorporate the receiver of *Carey* would merely involve the simple addition of a known element (the receiver integrated circuit of *Carey*) for a generally known function (receiving time and date information from an external source) to obtain predictable results (a thermostat system with a receiver adapted to receive current time and date information from an external source to update the time and date of the thermostat system).

189. *Rosen* and *Carey* are in the same field of endeavor and are therefore analogous art to the ’825 Patent and each other. Both *Rosen* and *Carey* relate to programmable thermostats. EX1004, Abstract (“A programmable thermostat system ... include[ing] ... a real time clock”); EX1007, Abstract (“A digital

programmable thermostat ... [that] can [] automatically set the current time and date.”); EX1001, Title, Abstract (“Programmable Thermostat Employing a Fail Safe Real Time Clock”).

190. Keeping the clock of a thermostat as accurate as possible when power is restored after a power outage was a recognized problem for thermostats. EX1001, 2:18-55. Inventor Rosen acknowledged that prior art thermostats addressed the issue of keeping the correct time during a power outage. EX1013, 75:8-25. Thus, the problem of keeping the clock as correct as possible after a power outage was a recognized problem for thermostats. The ’825 Patent discloses several prior art solutions to this problem—use of battery to power the clock or use of a capacitor to power the clock during a power outage. EX1001, 2:18-55. A POSITA would consider all available prior art methods to address that problem of keeping the clock as accurate as possible in the event of a power outage and thus would turn to *Carey* as one design choice to solve the problem. Inventor Rosen agreed that a POSITA had various methods to choose from to keep the time as accurate as possible after a power failure. EX1013, 76:11-18. Given that *Carey* provides a method to do so with identified advantages, it would be obvious to use the method of *Carey* in the thermostat of *Rosen*. A POSITA would further understand from *Carey* that if the WWVB receiver was used, the receiver could be used to automatically reset the time after a power failure.

191. *Rosen* explains that a user of its system may wish to set the present time in order to set temperatures for certain time periods ahead of time, and it discloses a multi-step process for setting the real time clock. EX1004, ¶0034. *Carey* explains a problem with thermostat programs is that they “require[] the user to complete a complex series of steps.” EX1007, ¶0001. *Carey* discloses a technique to “simplif[y] programming by setting the time for the user.” EX1007, ¶0003. A POSITA would have been motivated to incorporate *Carey*’s receiver and known updating time and date from an external source technique in order to improve upon the *Rosen* thermostat by making it easier to set the time.

192. Incorporating the aforementioned technique of *Carey*’s thermostat system would provide a better experience to the users of *Rosen*’s thermostat system because they would not have to engage in the multi-step process *Rosen* describes to “set the present time.” EX1004, ¶0034. This streamlines the programming of the *Rosen* thermostat and would “allow a user to easily initiate a single set back program without having to set the current time and date.” EX1007, ¶0004.

193. A POSITA would have had a reasonable expectation of success in making the combination. As an initial matter, implementing the known technique of *Carey* would only require the addition of conventional, well-known components, e.g., antenna and receiver, to the *Rosen* system which the ’825 Patent teaches can be readily incorporated into a thermostat. Compare EX1007, Figure 1 and EX1004,

Figure 1; *see also* EX1001, 6:12-17 (“a wireless receiver 50 is tuned to a source of precision time such as WWVB which operates at 60 khz. ***Such receivers are well known in the art and may be implemented in small integrated circuits which can readily be incorporated into a thermostat.***”). Moreover, a POSITA would understand that antennas and receivers were commonly known in the art, and particularly, were included in thermostat systems. *See* EX1007, ¶0009. Using such known hardware to receive WWVB signals and update time and date information is a conventional technique commonly known to a POSITA and used in thermostat systems and analogous devices in the prior art.

194. A POSITA would have recognized that the systems described in *Rosen* and *Carey* are very similar as they are both thermostats with a real time clock. The teachings of *Carey* are directed towards a “programmable thermostat[] that will allow a user to set back the temperature set point during select periods.” EX1007, ¶0001. *Rosen*’s programmable thermostat system allows a user “to change the temperature set point in any of the exemplary [] periods.” EX1004, ¶0033; *see also id.*, Abstract. Given the similarities of *Rosen* and *Carey*, a POSITA would have understood that *Carey*’s techniques were suitable for application with *Rosen*’s thermostat system. Thus, a POSITA would have understood that *Carey*’s receiver and technique for updating time could be readily incorporated into the thermostat system of *Rosen*. It would have been well within the abilities of a POSITA to modify

Rosen's thermostat system to include the antenna and receiver of *Carey* and to couple the receiver of *Carey* to the already-present real time clock under control of the processor of *Rosen*.

195. Moreover, a POSITA would have had a reasonable expectation of success in making the combination because, *Rosen* explains that “integrated circuit chips including all the processor components with all the necessary interface conditioning circuits are available off-the-shelf” and that “[t]he subject invention only requires the capabilities of such a processor, and off-the-shelf integrated circuit processor chips may be used to advantage in the subject thermostat system.” EX1004, ¶0023.

196. Additionally, *Carey* also uses parts off the shelf—it elaborates that its antenna is “preferably a 60kHz LC tuned ferrite core antenna made by HKW Elektronik GmbH,” its receiver integrated circuit “is preferably an Atmel T4227 time code receiver chip,” and its microprocessor “is preferably a 32Kb microprocessor S3C8249XZZ-OWR9 manufactured by Samsung.” EX1007, ¶0008. Because the systems of *Rosen* and *Carey* utilize commercially available, off-the-shelf components, and known techniques it would have been well within the abilities of a POSITA to modify *Rosen*'s thermostat system to include the antenna and receiver of *Carey* and its associated functionality (namely, the receiver adapted to receive current time and date information from an external source of the current

time and date, said receiver being coupled to said real time clock such that the time and date information thereof is updated from said receiver).

2. Claim 12

(i) 12: “The thermostat of claim 11 in which said receiver receives wireless signals from said external source.”

197. *Rosen* in combination with *Carey* discloses Claim 12. The '825 Patent does not purport to have invented a receiver that receives wireless signals from said external source or improved upon existing receivers that receive wireless signals. Moreover, it was well known in the art that thermostat systems include wireless receivers, as acknowledged by the '825 Patent. EX1001, 6:13-24 (“a **wireless receiver 50** is tuned to a source of precision time such as WWVB which operates at 60 khz. **Such receivers are well known in the art and ... can readily be incorporated into a thermostat.**”) (emphasis added).

198. The *Rosen-Cacciatore-Carey* combined system discloses Claim 12 for the reasons discussed above for Claim 11. As discussed above with respect to element 11[k] above, *Rosen* modified by *Carey* discloses a receiver adapted to receive current time and date information from an external source of the current time and date. *Supra*, § VII.D.1.vii. The system disclosed in *Carey* includes a receiver that receives a “60kHz time code signal broadcast from station WWVB in Fort Collins.” EX1007, ¶0008. The station in Fort Collins is an “external source” and the signal it broadcasts is a wireless signal. As a POSITA would understand, *Carey*’s

WWVB signals are electromagnetic waves and are thus, wireless. The '825 Patent, as quoted above, acknowledges that a WWVB receiver is a wireless receiver. Accordingly, based on my current analysis, the thermostat systems in *Carey* and *Rosen* together disclose each additional limitation of Claim 12.

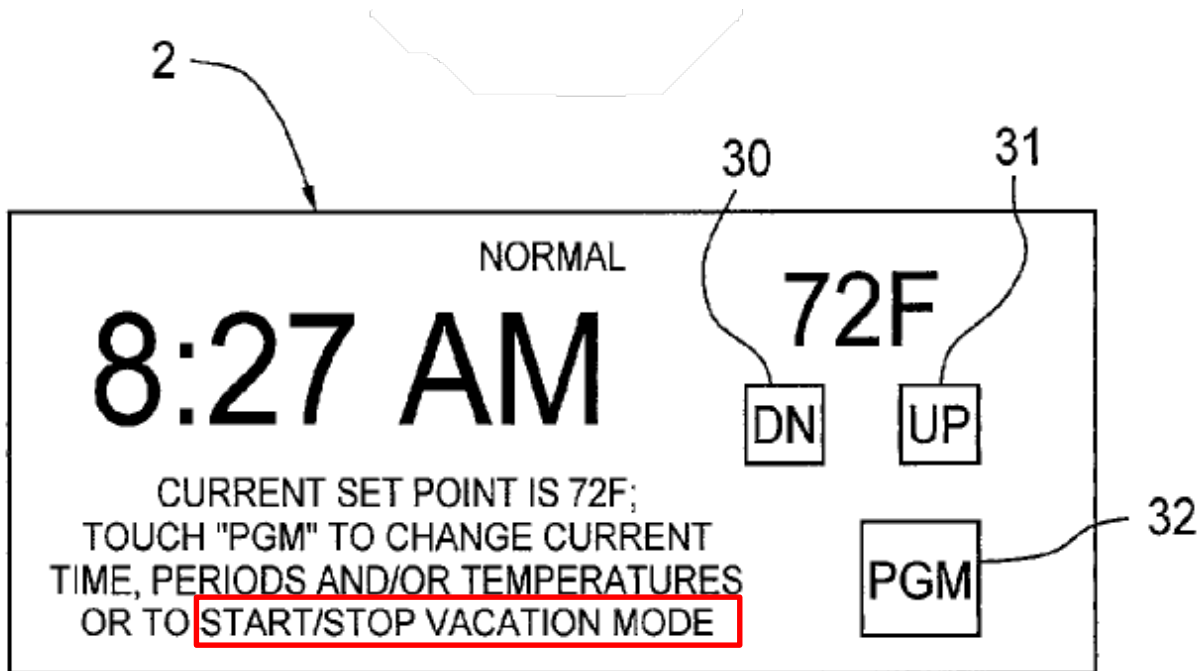
3. Claim 13

(i) 13: “The thermostat of claim 12 which includes a vacation mode of operation.”

199. *Rosen* discloses Claim 13. The '825 Patent does not purport to have invented a vacation mode of operation or improved upon existing vacation modes of operation. It was well known in the art that thermostat systems include a vacation mode of operation, as acknowledged by the '825 Patent. EX1001, 1:60-61 (“The operation of programmable thermostats in the vacation mode is straightforward and well known.”).

200. The *Rosen-Cacciatore-Carey* combined system discloses Claim 13 for the reasons discussed above for Claim 12. *Rosen* discloses a program that “may [] include a ‘vacation’ mode which employs different set points when the conditioned space is not occupied for an extended period.” EX1004, ¶0003. Thermostats that include a vacation mode of operation are well known in the art. *See, id.*, ¶0004 (“Typically, prior art programmable thermostat system[s] ... may include a ***vacation mode***.”) (emphasis added).

201. In the annotated figures below *Rosen* illustrates how users can start, stop, or adjust vacation mode, and identifies the interface indicator present when the *Rosen* system is operating in vacation mode:



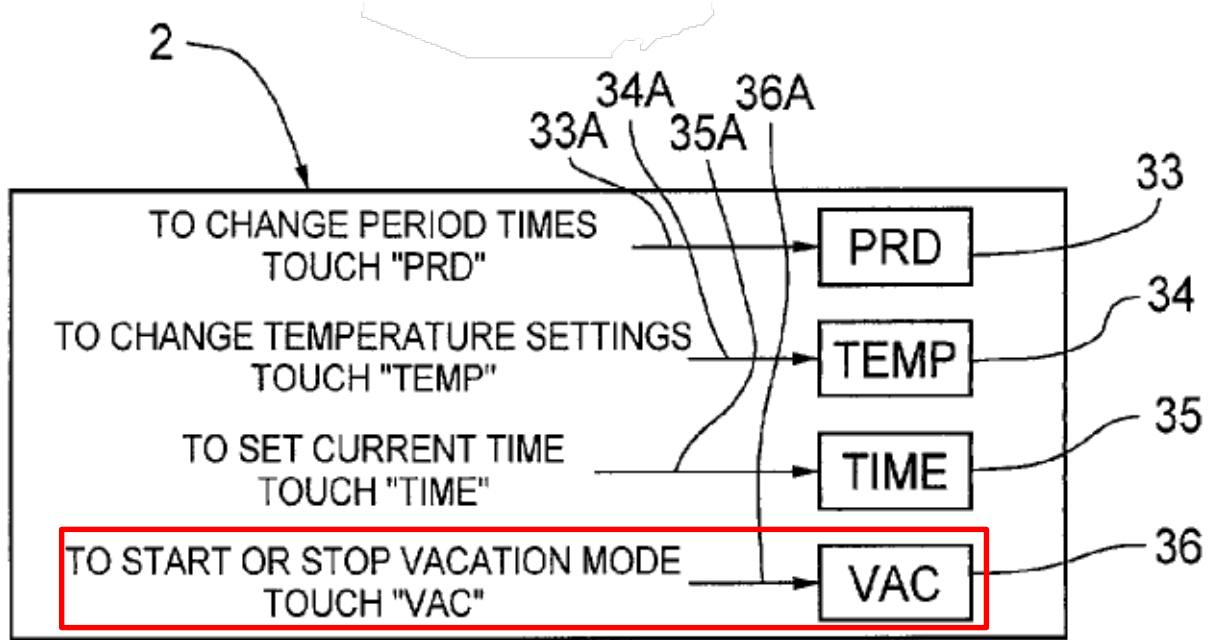


FIG. 4

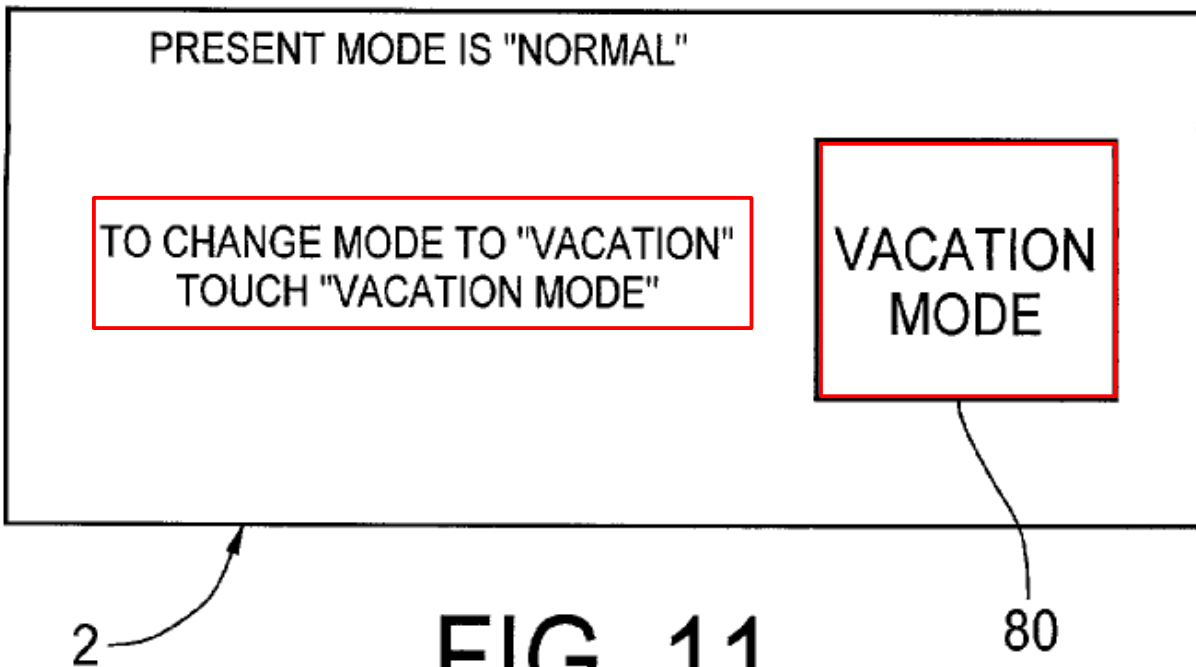
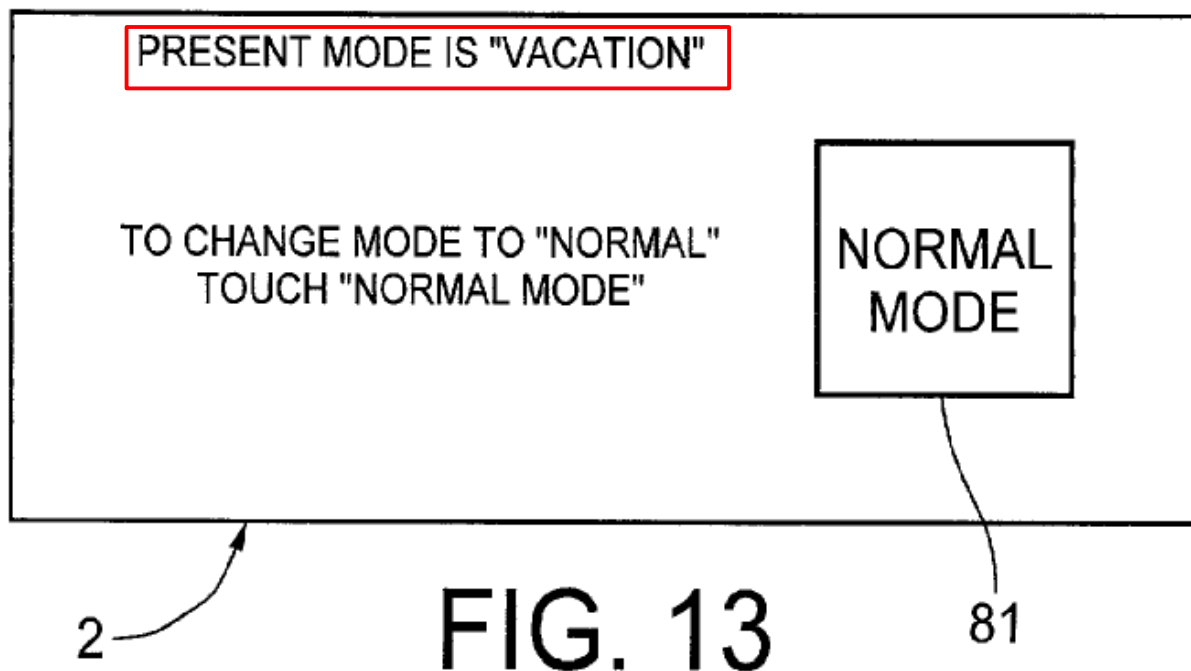
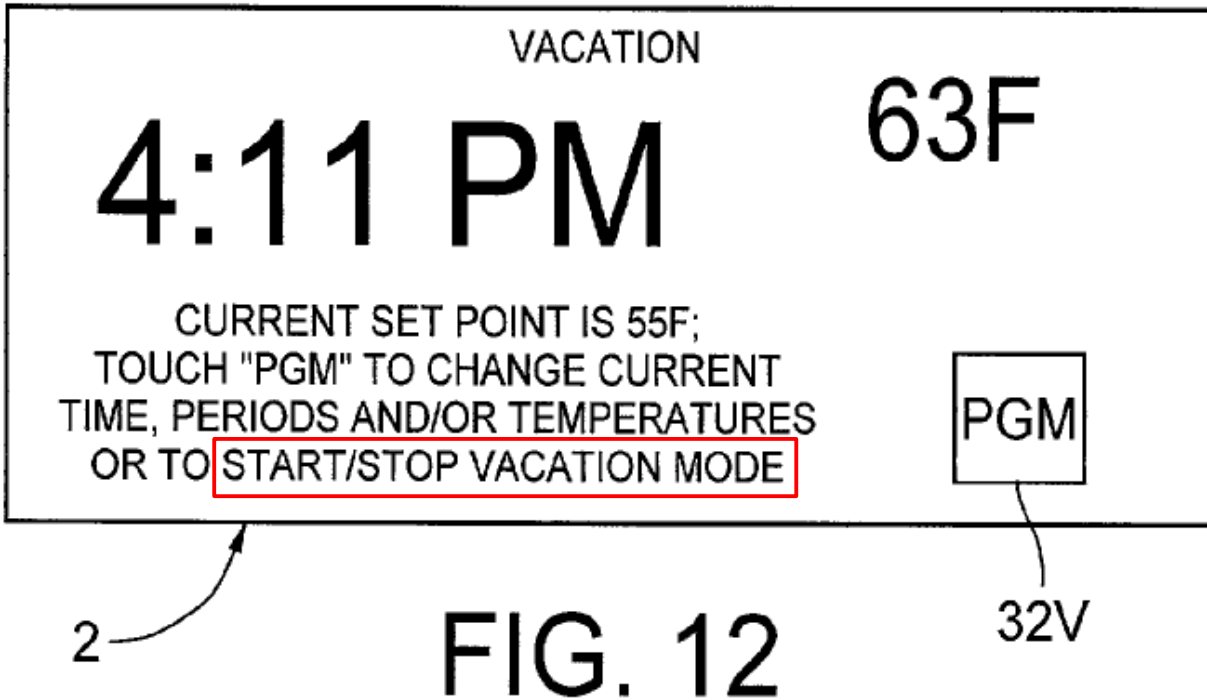


FIG. 11



Id., Figures 3-4, 11-13 (annotated); *see also id.*, ¶0035. *Rosen* thus discloses each additional limitation of Claim 13.

4. Claim 16

(i) 16: “The thermostat of claim 11 which includes a vacation mode of operation.”

202. The *Rosen-Cacciatore-Carey* combined system discloses Claim 16 for the reasons discussed in Sections VII.D.1 for Claims 11 and 13. Claim 16 includes each and every element disclosed in Claims 13 and 11 and is thus disclosed in the same manner as described in Sections VII.D.3 for Claims 13 and 11. *Rosen* discloses a thermostat with a vacation mode of operation as discussed above in Section VII.D.3. Thus, the combined references include all elements of Claim 16.

E. Ground 3: Claims 11 and 14-16 are obvious over *Rosen* in view of *Cacciatore*, and *Williamson*

203. Based on the following analysis, I conclude that a POSITA at the relevant time (June 24, 2004) would have understood the limitations of Claims 11 and 14-16 were expressly disclosed, taught, or suggested by *Rosen* in combination with *Cacciatore*, and *Williamson*.

204. This ground is included because the dependent claims of Claim 11 include two separate options for the signals received by the “receiver”—wireless signals in Claims 12 and 13 and signals from the Internet in Claims 14 and 15.

1. Claim 11

(i) Elements 11[pre]-11[i]

11[pre]: “A programmable thermostat for controlling space conditioning equipment comprising:”

11[a]: “A) means coupling suitable power for energizing said thermostat from said space conditioning equipment to said thermostat;”

11[b]: “B) an interactive interface for a user to enter programming information into said thermostat;”

11[c]: “C) a temperature sensor for providing an electrical signal indicative of the temperature of a conditioned space in which the temperature sensor is situated;”

11[d]: “D) a processor, said processor including:”

11[e]: “1) a central processing unit;”

11[f]: “2) a first memory coupled to said central processing unit for storing program and data information; and”

11[g]: “3) an input/output unit including:”

11[h]: “a) a sensor input coupled to said temperature sensor for receiving said electrical signal therefrom; and”

11[i]: “b) a control output coupled to the space conditioning equipment for issuing control signals thereto;”

11[j]: “4) a real time clock; and”

205. The analysis for elements 11[pre]-11[j] is identical to the analysis for Ground 2 as set forth in Sections VII.D.1.i-vi above.

- (ii) **11[k]: “5) a receiver adapted to receive current time and date information from an external source of the current time and date, said receiver being coupled to said real time clock such that the time and date information thereof is updated from said receiver.”**

206. *Rosen* in combination with *Cacciatore* and *Williamson* discloses element 11[k]. The '825 Patent acknowledges that the use of receivers adapted to receive time and date information from an external source and use such information to update the real time clock in a thermostat was “well known in the art.” EX1001, 6:13-24 (“a wireless ***receiver 50 is tuned to a source of precision time*** such as WWVB which operates at 60 khz. Such receivers are ***well known in the art and ... can readily be incorporated into a thermostat. ... The output from the receiver 50 is ... the exact time ... and date. This information is used to periodically update the time and date information running in the real time clock 30.***”) (emphasis added).

207. As discussed above with respect to element 1[j], *Rosen* discloses a programmable thermostat system with a settable real-time clock. *Supra*, § VII.C.2.vii; *see also* EX1004, Abstract, ¶0020. *Rosen*, however, does not expressly disclose “a receiver adapted to receive current time and date information from an external source of the current time and date, said receiver being coupled to said real time clock such that the time and date information thereof is updated from said receiver.” EX1001, Claim 11. *Williamson* discloses this aspect of element 11[k].

208. *Williamson* “relates to [the] configuration of an appliance network” such that a “synchronization automatically ... assures all clocks report the correct time.” EX1010, 1:16-19, 2:12-13. The *Williamson* system discloses a receiver: an

intelligent controller that receives time messages from a web server. *Id.*, 2:8-12. *Williamson*'s intelligent controller is "in communication with a web server 104 via a modem (or via a broadband connection)" and may "connect[] through an internet service provider and may even use a cable modem or DSL router to connect with the Internet" such that the intelligent controller receives information from an external source. *Id.*, 4:4-6, 4:38-40; *see also id.*, 10:27-31 ("The minimum functionality required in the intelligent controller 102 is to convert ***data received over an external network*** to the internal network."), 2:2-5, 4:4-7, Figure 1.

209. *Williamson* explains that time messages are specifically received at the modem in the intelligent controller. *Id.*, 8:36-40 ("a synchronization signal (time message) being received at modem 206."). The intelligent controller includes a controller, a real-time clock, and a modem all coupled to each other. *Id.*, Figure 3, 8:36-37 ("A real-time clock 308 ... is connected to the controller 210.").

210. The real-time clock disclosed in *Williamson* "receives time messages from the information controller 102, periodically ... [and] then synchronizes to the time maintained by the intelligent controller 102." *Id.*, 24:10-15; *see also id.*, 8:36-40 ("The real-time clock 308 is a digital chip that is programmable by the controller 210 in response to ***a synchronization signal (time message) being received at modem 206.***") (emphasis added).

211. As seen in annotated Figure 3 of *Williamson* below, the real-time clock is coupled to the intelligent controller and modem. *Id.*, 7:16-23 (“The intelligent controller 102 has a controller 210 that is connected by a bus 302 to the modem 206, the memory 208, and the local network communication link 220. The intelligent controller 102 may also include the ... real-time clock 308.”).

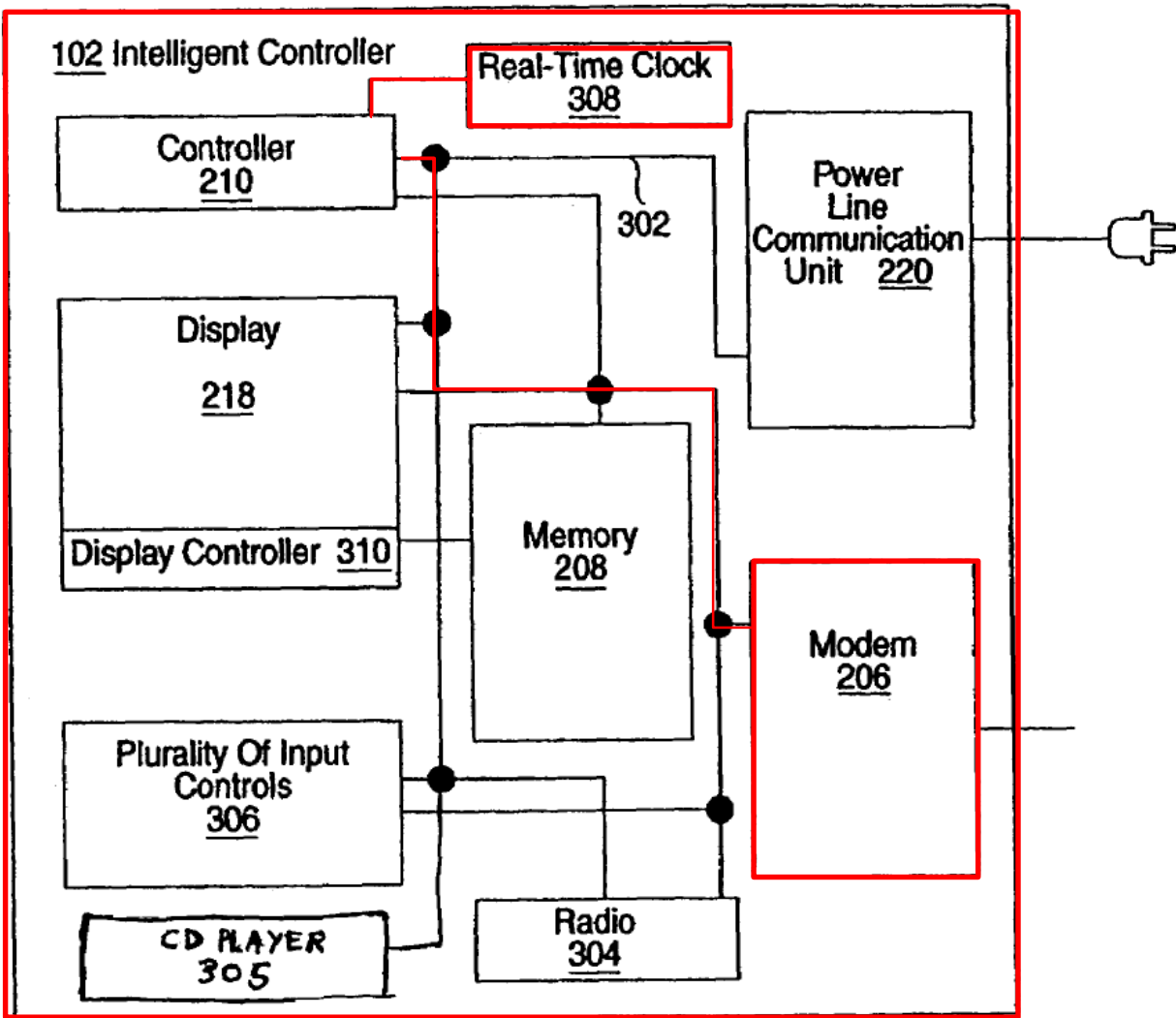


Fig. 3

Id., Figure 3 (annotated).

212. A POSITA would understand that the time and date information received by the *Williamson* modem is current date and time information. Indeed, the “synchronization automatically corrects for time changes and ***assures all clocks report the correct time***. The user profile also contains a time zone identifier that enables the clocks ... to ***report the proper time*** for a specified time zone.” *Id.*, 2:12-16; *see also id.*, 8:46-48.

213. *Williamson*’s receiver (e.g., intelligent controller 102 including modem 206) is adapted to receive current time and date information (e.g., time messages received at intelligent controller) from an external source of the current time and date (e.g., the Internet), said receiver (e.g., intelligent controller 102 including modem 206) being coupled to said real time clock (e.g., the intelligent controller 102 includes real-time clock 308) such that the time and date information thereof is updated from said receiver (the real-time clock is programmed in response to the time messages so that time is correctly maintained). *Compare* EX1010 and EX1001, Claim 11.

214. Accordingly, based on my current analysis, the *Rosen* system modified by *Williamson* discloses each and every element of 11[k], including a receiver adapted to receive current time and date information from an external source of the

current time and date, said receiver being coupled to said real time clock such that the time and date information thereof is updated from said receiver.

(a) Rationale and motivation for combining *Rosen* and *Williamson*

215. It would have been obvious to a POSITA to combine *Williamson*'s receiver with *Rosen*'s programmable thermostat system. Indeed, modifying *Rosen* to incorporate the receiver of *Williamson* would merely involve the simple addition of a known element (a means for connecting to an external network such as the modem disclosed by *Williamson*) for a generally known function (receiving time information from an external source) to obtain predictable results (a thermostat system with a receiver adapted to receive current time and date information from an external source to update the time and date of the thermostat system). As a POSITA would understand, connecting thermostats to the Internet provides various known improvements, including improving upon the protocol to reset the time in the case of a power outage. EX1020, 9 n.10 ("A very different segment of the media coverage of "Internet appliances" concerns the notion of connecting traditional household appliances . . . to the Internet. . . . Some of these concepts make sense (e.g. connecting thermostats so you can program them through a Web site, not to have to reset time when power blinks, perform remote diagnostics on large appliances, etc.)").

216. *Rosen* and *Williamson* are in the same field of endeavor and are therefore analogous art to the '825 Patent and each other. Both *Rosen* and *Williamson* relate to programmable home appliances that contain real-time clocks. EX1004, ¶0001 (“A programmable thermostat system ... includ[ing] ... a real time clock”); EX1010, 1:15-16, 2:8-12 (“The invention relates to configuration of an appliance network” and “a clock [that] is periodically synchronized to a time message that the web server transmits to ... appliances that are capable of receiving the power line communications.”); EX1001, Title (“Programmable Thermostat Employing a Fail Safe Real Time Clock”).

217. *Rosen* explains that a user of its system may wish to set the present time in order to set temperatures for certain time periods ahead of time, and it discloses a multi-step process for setting the real-time clock. EX1004, ¶0034. *Williamson* explains the problems with appliances that include clocks, the “clocks [] must be initially set and reset after a power outage” and “it is often impossible to change the configuration or programming of an appliance ... once the appliance has left the factory.” EX1010, 1:44-46, 1:27-30.

218. However, *Williamson* discloses a system that provides an advantage “by maintaining the correct time synchronization of real-time clock 308 with the correct time maintained at the web server 104.” *Id.*, 8:46-48. A POSITA would have been motivated to incorporate *Williamson*’s known time synchronization from

an external source technique in order to improve upon the *Rosen* thermostat. Incorporating the aforementioned technique of *Williamson*'s thermostat system would improve *Rosen*'s thermostat system by (a) automatically setting the clock for the user, thus saving the user time, and (b) automatically resetting the clock after a power outage thus maintaining the correct time shortly after power was restored. EX1004, ¶0034. Use of *Williamson*'s technique streamlines the programming of the *Rosen* thermostat and would "assure[that] all clocks report the correct time." EX1010, 2:13.

219. A POSITA would have had a reasonable expectation of success in making the combination. As an initial matter, implementing the known technique of *Williamson* would only require the addition of conventional, well-known components, e.g., a modem, to connect *Rosen*'s thermostat system to the Internet. Compare EX1010, Figure 3 and EX1004, Figure 1; EX1013, 44:24-45:20.

220. Moreover, a POSITA would understand that devices that use the Internet to set the time on a clock were commonly known in the art, and particularly, were included in thermostat systems prior to the invention on the '825 Patent. EX1013, 123:6-124:2 (Testimony from the inventor of the '825 Patent confirming that he was aware of devices prior to his invention that used the Internet to set the time on a clock); EX1020, 9 n.10 ("A very different segment of the media coverage of "Internet appliances" concerns the notion of connecting traditional household

appliances . . . to the Internet. . . . Some of these concepts make sense (e.g. connecting thermostats so you can program them through a Web site, not to have to reset time when power blinks, perform remote diagnostics on large appliances, etc.)”). Using such known hardware to receive time from the Internet and update time and date information is a conventional technique commonly known to a POSITA and used in thermostat systems and analogous devices in the prior art.

221. A POSITA would have recognized that the systems described in *Rosen* and *Williamson* are complementary and include many similar elements. The teachings of *Williamson* are directed towards a system for synchronizing the clocks of various appliances through communication with a web server so that the “clocks report the correct time.” EX1010, 4:58-64, 2:12-13. *Rosen*’s programmable thermostat system includes a technique for users to set the present time on the thermostat system so that the display will “show the correct current time.” EX1004, ¶0034; *see also id.*, Abstract. Given the similarities of the systems, a POSITA would have understood that *Williamson*’s techniques were suitable for application with *Rosen*’s thermostat system. Moreover, *Williamson* discloses the technique as applied to a wide range of home appliances including, for example, a coffeemaker, a breadmaker, a microwave oven, a conventional type oven. EX1010, 4:44-51. Thus, a POSITA would have understood that *Williamson*’s receiver and technique for updating time could be readily incorporated into the thermostat system of *Rosen*.

It would have been well within the abilities of a POSITA to modify *Rosen*'s thermostat system to include the receiver of *Williamson* and to couple the receiver of *Williamson* to the already-present processor of *Rosen*.

222. Moreover, a POSITA would have had a reasonable expectation of success in making the combination because, *Rosen* explains that “integrated circuit chips including all the processor components with all the necessary interface conditioning circuits are available off-the-shelf” and that “[t]he subject invention only requires the capabilities of such a processor, and off-the-shelf integrated circuit processor chips may be used to advantage in the subject thermostat system.” EX1004, ¶0023. Additionally, *Williamson* elaborates that its time updating technique could be accomplished by connecting to the Internet through a variety of methods a POSITA would have been familiar with at the time. EX1010, 4:24-44. For instance, *Williamson* explains that Internet connection could be accomplished over an Internet Protocol connection, through an Internet service provider, by a cable modem, by a DSL router. *Id.*, 4:37-40. *Williamson* also teaches “a different communication protocol may be used.” *Id.*, 4:40-42. It would at once be obvious to a POSITA to use the well known Network Time Protocol (NTP) to connect to a server and obtain the time. As described in the introduction to IETF RFC 958, NTP is “a protocol for synchronizing a set of network clocks using a set of distributed clients and servers.” See EX1024, 1. It is common knowledge of a POSITA that

devices connected to the Internet can set their clocks using a time service available on the Internet called NTP. This service was available for at least 15-20 years before the '825 Patent was filed and is a well known way to handle keeping devices on the Internet set to a correct time.

223. Because the systems of *Rosen* and *Williamson* utilize commercially available, off-the-shelf components, and known techniques to connect to the Internet it would have been well within the abilities of a POSITA to modify *Rosen*'s thermostat system to include the receiver of *Williamson* and its associated functionality (namely, the receiver adapted to receive current time and date information from an external source of the current time and date, said receiver being coupled to said real time clock such that the time and date information thereof is updated from said receiver).

2. Claim 14

(i) 14: "The thermostat of claim 11 in which said receiver receives signals via the Internet from said external source."

224. *Rosen* in combination with *Cacciatore* and *Williamson* discloses Claim 14. This combination discloses the elements of Claim 11 as set forth above in Section VII.E.1. As discussed above with respect to element 11[k] above, *Rosen* modified by *Williamson* discloses a receiver adapted to receive current time and date information from an external source over the Internet. *Supra*, § VII.E.1.ii.

225. The system disclosed in *Williamson* includes a receiver that “connect[s] with the Internet” and maintains the correct time. EX1010, 4:36-40, 5:34-36, 7:38-42. Thus, the receiver in *Williamson* receives signals via the Internet from an external source, thereby disclosing the new limitation of Claim 14. *Williamson*’s modem may “connect[] to the external network by wireless means, such as wireless Ethernet connection, 900 MHz in home network, or cellular connection.” *Id.*, 7:38-42. “The web device 112” of *Williamson* “communicates with the server 104 over an Internet Protocol connection. In an alternate embodiment, the intelligent controller 102 may connected through an internet service provider and may even use a cable modem or DSL router to connect with the Internet.” *Id.*, 4:36-41. *Williamson* also teaches “a different communication protocol may be used.” *Id.*, 4:40-42. It would at once be obvious to a POSITA to use the well known NTP to connect to a server and obtain the time. As described in the introduction to IETF RFC 958, NTP is “a protocol for synchronizing a set of network clocks using a set of distributed clients and servers.” See EX1024. The *Rosen-Williamson* system receives current time and date information from the Internet, thus satisfying the limitations of Claim 14.

226. Accordingly, based on my current analysis, the thermostat systems in *Williamson* and *Rosen* together disclose each additional limitation of Claim 14.

3. Claim 15

(i) **15: “The thermostat of claim 14 which includes a vacation mode of operation.”**

227. *Rosen* discloses Claim 15. The '825 Patent admits that this additional element of Claim 15 was known in the prior art. EX1001, 1:60-61 (“The operation of programmable thermostats in the vacation mode is straightforward and well known.”).

228. The *Rosen-Cacciatore-Williamson* combination discloses the elements of Claim 14 as discussed in Section VII.E.2. *Rosen* discloses a thermostat with a vacation mode of operation as set forth in Section VII.C.3. Thus, the *Rosen-Cacciatore-Williamson* combination discloses all elements of Claim 15.

229. Indeed, *Rosen* discloses a program that “may [] include a ‘vacation’ mode which employs different set points when the conditioned space is not occupied for an extended period.” EX1004, ¶0003. Thermostats that include a vacation mode of operation are well known in the art. *See, id.*, ¶0004 (“Typically, prior art programmable thermostat system[s] ... may include a ***vacation mode***.”) (emphasis added). In the annotated figures below *Rosen* illustrates how users can start, stop, or adjust vacation mode, and identifies the interface indicator present when the *Rosen* system is operating in vacation mode:

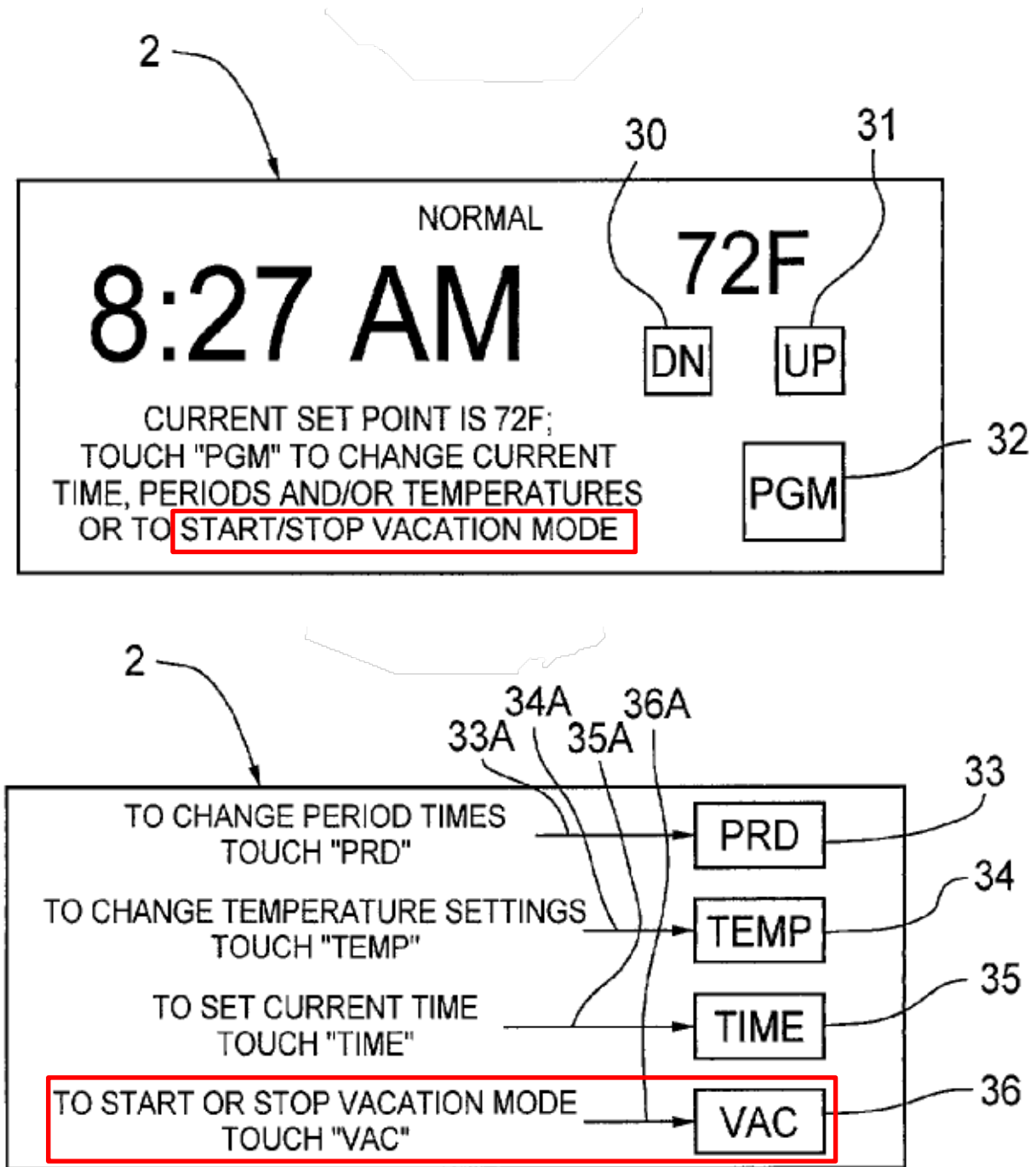
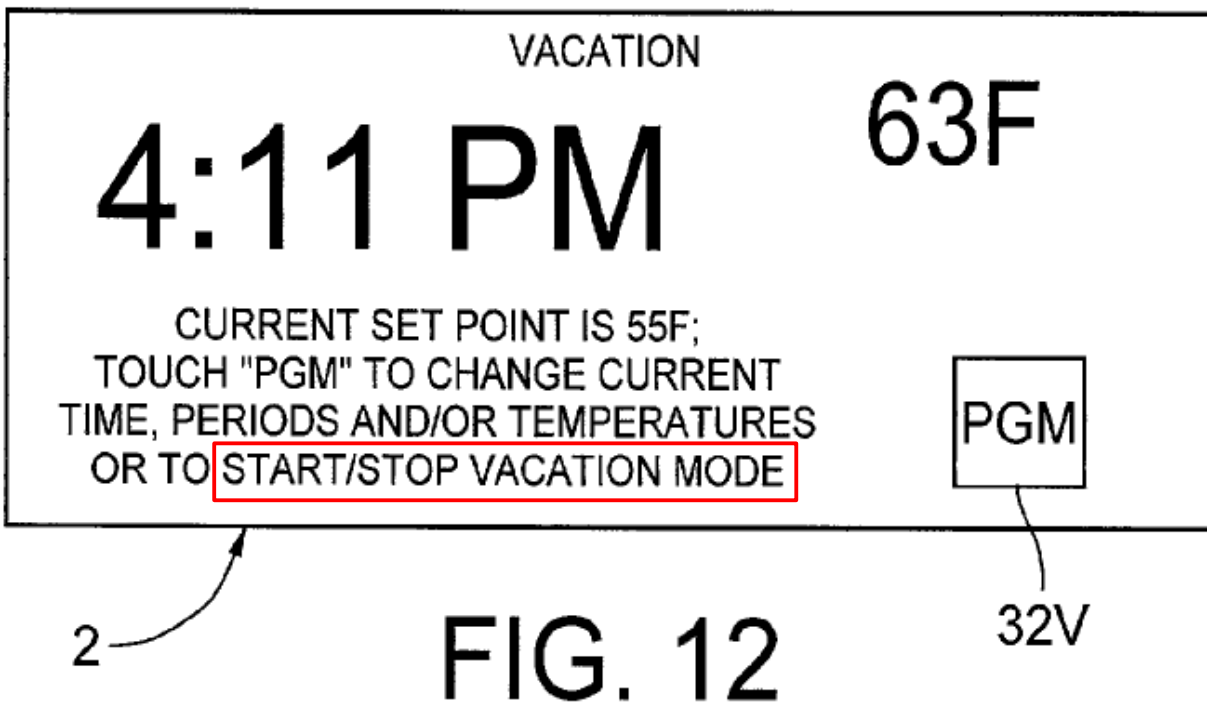
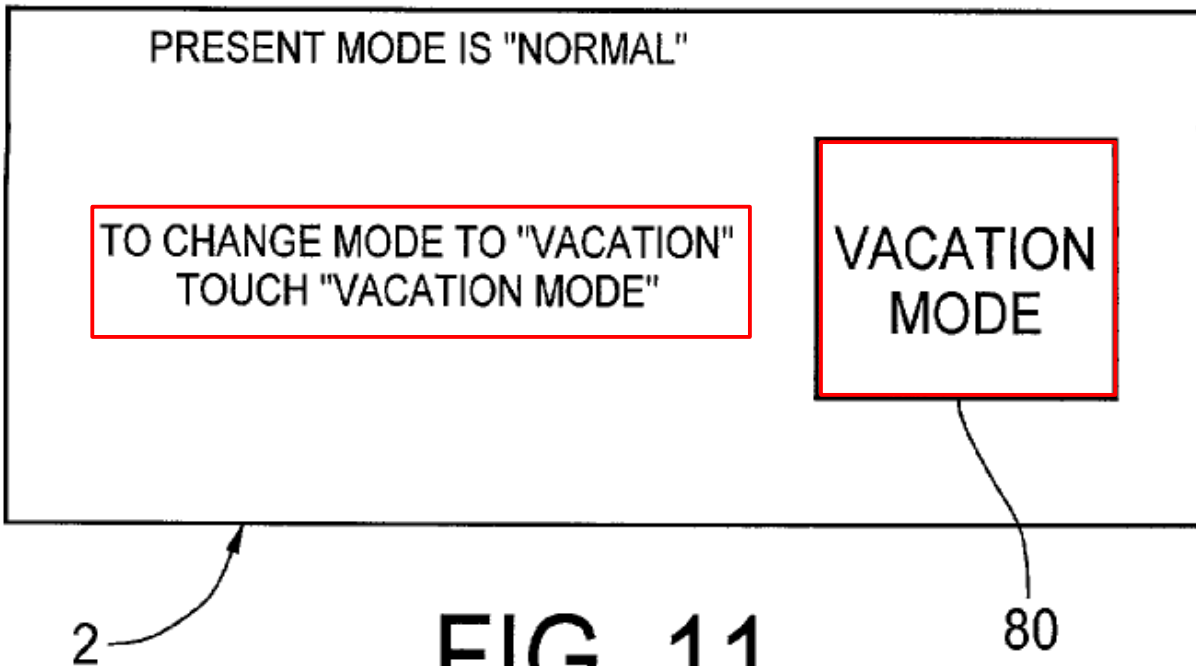
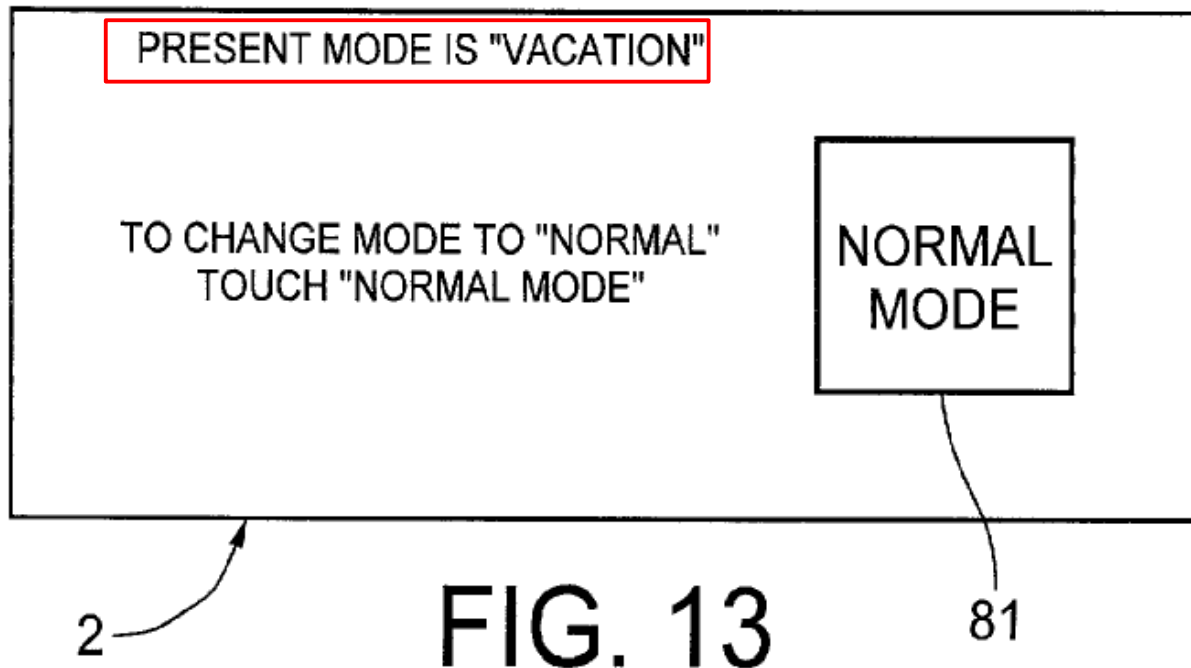


FIG. 4





Id., Figures 3-4, 11-13 (annotated); *see also id.*, ¶0035. *Rosen* thus discloses each additional limitation of Claim 15.

4. Claim 16

- (i) **16: “The thermostat of claim 11 which includes a vacation mode of operation.”**

230. Claim 16 includes each and every element disclosed in Claim 15 and is thus disclosed in the same manner as described in Section VII.E.3 for Claim 15.

F. Ground 4: Claim 1 is obvious over *Shamoon* in view of *Cacciatore*, and *Shigeaki*

231. Based on the following analysis, I conclude that a POSITA at the relevant time (June 24, 2004) would have understood the limitations of Claim 1 were expressly disclosed, taught, or suggested by *Shamoon* in combination with *Cacciatore* and *Shigeaki*.

1. Motivation to Combine

(i) Rationale and motivation for combining *Shamoon* with *Cacciatore*

232. I provide *Cacciatore* in grounds involving *Shamoon* with reference to the “means coupling suitable power for energizing said thermostat from said space conditioning equipment to said thermostat” element of Claim 1/11. In my opinion, this element would be obvious in light of admissions in the specification of the ’825 Patent as discussed above. EX1001, 5:3-5. To the extent the Board disagrees, then *Cacciatore* supplies this element. While *Shamoon* teaches the ability to remote control a thermostat, it indicates “[t]he wall thermostat controller of the invention uses the same operating system as the handheld controller, has similar hardware, and performs pretty much the same.” EX1008, ¶0040.

233. Thermostats have traditionally been powered by using wiring (a power line) to connect a source of power in the space conditioning equipment to the thermostat. The ’825 Patent teaches that power is supplied “in accordance with the prior art.” EX1001, 5:3. Power is “conventionally supplied from the space condition equipment 3 via a line 30 through an isolation diode 33.” *Id.*, 5:3-5. Given this admission that it is conventional to supply power from space conditioning equipment via a “line,” this element is within the general knowledge of a POSITA and it would be obvious to use a conventional method of supplying power in the context of Claims 1 and 11.

234. Thus, it would be obvious to use what is admitted as “conventional” in the specification to supply power to the wall thermostat of *Shamoon*. While *Shamoon* teaches a different method of supplying power, it is obvious that the conventional method could be used. It is merely one design choice that a thermostat designer could choose to use.

235. If the Board disagrees or determines that an “isolation diode” to protect the backup battery is part of the corresponding structure, then it would be obvious to use a line to connect the thermostat to the power source and protect the backup battery with an isolation diode. Again, the ’825 Patent, in the passage quoted above, teaches that the power is “conventionally supplied” using a power line and an isolation diode to protect the battery. EX1001, 5:3-5. Inventor Rosen agrees that the isolation diode to protect the battery is prior art. EX1013, 96:9-97:6. Thus, it is obvious to use this prior art method of supplying power.

236. But if the Board disagrees with all of the above, then the power line and a diode to protect the battery (an isolation diode) is obvious to use given the teachings of *Cacciatore*. As an initial matter, *Shamoon* and *Cacciatore* are in the same field of endeavor and are therefore analogous art to the ’825 Patent and each other. A POSITA would have been motivated to combine *Cacciatore* with *Shamoon*.

237. *Shamoon* discloses the use of an X10 interface—a common home automation interface—an therefore accesses home power. EX1008, ¶0071, Figure 6. For users where home automation is not desired, a POSITA would look to prior art methods of accomplishing obtaining power from the space conditioning equipment. *Cacciatore* is one such reference. As discussed in Sections VII.C.1.i and VII.C.2.iii above, *Cacciatore* teaches both connection via a power line (wiring) to space conditioning equipment and protecting a backup battery via an isolation diode.

238. Based on *Cacciatore*'s disclosure that the configuration it describes provides a means for “simply and effectively providing” operating power to a thermostat system, a POSITA would have been motivated to modify *Shamoon* to use the power line and isolation diode taught by *Cacciatore* to supply energizing power to *Shamoon*'s wall thermostat system from space conditioning equipment. Modifying *Shamoon* to incorporate the *Cacciatore*'s teachings would merely involve the application of a known technique (supplying power to a thermostat system from space conditioning equipment using a power line and protecting a battery with an isolation diode as taught by *Cacciatore*) to a known device (the thermostat system of *Shamoon*) to obtain predictable results (a thermostat system that receives energizing power from space conditioning equipment via a power line employs an isolation diode to protect a backup battery). It is obvious to use this

method of supplying power because it is a conventional method and one design choice for doing so. EX1001, 5:3-5.

239. A POSITA would have had a reasonable expectation of success in making the combination. It was conventional to supply power using such structure so a POSITA would just be using prior art structure to supply power. EX1004, ¶0020; EX1001, 5:3-5; EX1013, 96:9-97:6.

(ii) Rationale and motivation for combining *Shamoon* with *Shigeaki*

240. *Shamoon* suggests but does not explicitly disclose the limitations of Claim 1 concerning the storage of time in a nonvolatile memory and putting that stored time into the real time clock after power is restored. *Shigeaki* explicitly discloses these limitations and it would be obvious to combine *Shigeaki* with *Shamoon*. Specifically, *Shigeaki* discloses the precise method claimed in Claim 1 to reset the real time clock after a power outage: “When a power outage occurs, the time data pertaining to the current time is stored in E²PROM 2, and when power is restored, the time data is read from E²PROM 2, and the time is resumed from the current time corresponding to the retrieved time data.” EX1006, ¶0061. A POSITA would understand that E²PROM means EEPROM, and EEPROM stands for electronically erasable programmable read-only memory as confirmed by Webster’s Dictionary of Computer Terms. See EX1026, 3 (Defining EEPROM as an “[a]cronym for Electrical Erasable Programmable Read-Only Memory. A type of

read-only memory (ROM) that can be erased and reprogrammed by applying an electrical current to the memory chips and then writing new instructions to them.”). EEPROM is a type of nonvolatile memory that can be electronically (via a processor) programmed with new data, i.e., the old data can be “erased.” *Id.*

241. *Shamoon* and *Shigeaki* are in the same field of endeavor and are therefore analogous art to the ’825 Patent and each other. Both *Shamoon* and *Shigeaki* relate to programmable devices with real-time clocks that store time information. EX1008, Abstract; EX1006, ¶0002.

242. As discussed in Section VII.C.1.ii above, *Shigeaki* provides two motivations to use its time restoration technique in a thermostat. “When the power outage of the commercial power source is restored, the clock is delayed only by the time of the power outage. Therefore, short power outage time means that the clock device requires less time and effort to adjust the clock when the power is restore. The clock device does not require a power supply for backup, saving the cost of parts.” EX1006, ¶¶0025-0026. The second motivation of eliminating the need for a backup power supply is mentioned again: “Because a backup power source, such as a capacitor, is unnecessary** to keep the control circuit 1 in operation during a power outage, part costs can be saved, and there is no need to replace the battery.” *Id.*, ¶0063. Eliminating the need for a capacitor or backup battery is precisely what the ’825 Patent discloses as an advantage of the invention. *E.g.* EX1001, 3:30-31.

Those same two motivations would motivate a POSITA to use *Shigeaki*'s technique in *Shamoon* just like in *Rosen* as discussed above. *Supra*, VII.C.1.ii. In addition, a POSITA would be motivated to use known techniques available to restore time as accurately as possible for the same reasons discussed in Section VII.C.1.ii. This was just a matter of design choice and the same reasoning as to obviousness in Section VII.C.1.ii is applicable here. Thus, a POSITA would have been motivated to use the method of restoring the clock after a power outage both to make the clock easier to reset and to eliminate the need for a backup power source to avoid costs.

243. Keeping the clock of a thermostat as accurate as possible when power is restored after a power outage was a recognized problem for thermostats. EX1001, 2:18-55. Inventor Rosen acknowledged that prior art thermostats addressed the issue of keeping the correct time during a power outage. EX1013, 75:8-25. Thus, the problem of keeping the clock as correct as possible after a power outage was a recognized problem for thermostats. The '825 Patent discloses several prior art solutions to this problem—use of battery to power the clock or use of a capacitor to power the clock during a power outage. EX1001, 2:18-55. A POSITA would consider all available prior art methods to address that problem of keeping the clock as accurate as possible in the event of a power outage and thus would turn to *Shigeaki* as one design choice to solve the problem. Inventor Rosen agreed that a POSITA had various methods to choose from to keep the time as accurate as possible after a

power failure. EX1013, 76:11-18. Given that *Shigeaki* provides a method to do so with identified advantages, it would be obvious to use the method of *Shigeaki* in the thermostat of *Shamoon*.

244. A POSITA would have had a reasonable expectation of success in making the combination for the same reasons discussed above in Section VII.C.1.ii. As an initial matter, non-volatile memory and random access memory are conventional, well known components, and their use in thermostat systems as well as circuit chips is well-known. Writing data into and reading data from non-volatile memory is also a conventional technique commonly known to a POSITA and used in thermostat systems and analogous devices in the prior art.

245. Nonvolatile memories, such as EEPROMs or Flash PROMs, are available off the shelf and had been used in the thermostats for a few years prior to the filing of the '825 Patent. EX1018, 16:4, Figure 22b (Disclosing flash memory in an integrated thermostat system as early as October 22, 2002); EX1006, p. 30 (EEPROMS are nonvolatile memories); EX1008, ¶0060 (Flash PROM); EX1019, 7:29-32 ("The non-volatile RAM 108 may be an electrically erasable PROM or a 'flash' PROM which saves its contents even when power is lost."). Because the systems of *Shamoon* and *Shigeaki* utilize commercially available, off-the-shelf components, and known techniques it would have been well within the abilities of a POSITA to modify *Shamoon*'s thermostat system to include *Shigeaki*'s control

program functionality (namely, periodically reading the current time and date information into non-volatile memory and reading such data from the non-volatile memory into the real time clock upon restoration of power after failure). EX1013, 97:21-99:9 (inventor of '825 Patent admitting that all of the hardware components in Claim 1 are off-the-shelf components available in the prior art). This could have been done either using the Flash PROM of *Shamoon* or EEPROM or *Shigeaki* as options for the non-volatile memory. Either were off-the-shelf options.

2. Claim 1

246. Each of the eleven elements 1[pre]-1[j] are disclosed by *Shamoon*, as discussed below. Each of these elements is also common knowledge of a POSITA as admitted by the '825 Patent and discussed above in Section VII.C.2.i.

(i) 1[Pre]: “A programmable thermostat for controlling space conditioning equipment comprising:”

247. If the preamble is limiting, *Shamoon* discloses it. The '825 Patent does not purport to have invented a programmable thermostat for controlling space conditioning equipment or improved upon existing programmable thermostats for controlling space conditioning equipment. Moreover, programmable thermostats for controlling space conditioning equipment were well known in the art, as acknowledged by the '825 Patent. EX1001, 5:28-35 (“Many modern thermostat[s] ... run a process control program ... to send control signals to the heating and/or cooling equipment to closely control the temperature of the conditioned space.”).

248. *Shamoon* discloses an “***an intelligent thermostat which can control, monitor and communicate to a HVAC system and a thermostat and remote controller apparatus.***” EX1008, ¶0025 (emphasis added). It is programmable. *Id.*, ¶¶0040, 0057, 0060, 0065, 0067, 0074. “The thermostat 260 and temperature probe 265” of *Shamoon* “are the controlling devices for a user’s heating and air conditioning equipment.” *Id.*, ¶0057; *see also id.*, ¶0040. The system disclosed in *Shamoon* includes “***programmable*** memory (such as RAM, PROM and flash PROM) as well as prepackaged software (not shown) that runs the hardware and other components of the thermostat and remote control apparatus 10. This software is known to those skilled in the related art.” *Id.*, ¶0060 (emphasis added).

249. Figure 6 of *Shamoon*, reproduced below, depicts a programmable thermostat for controlling space conditioning equipment.

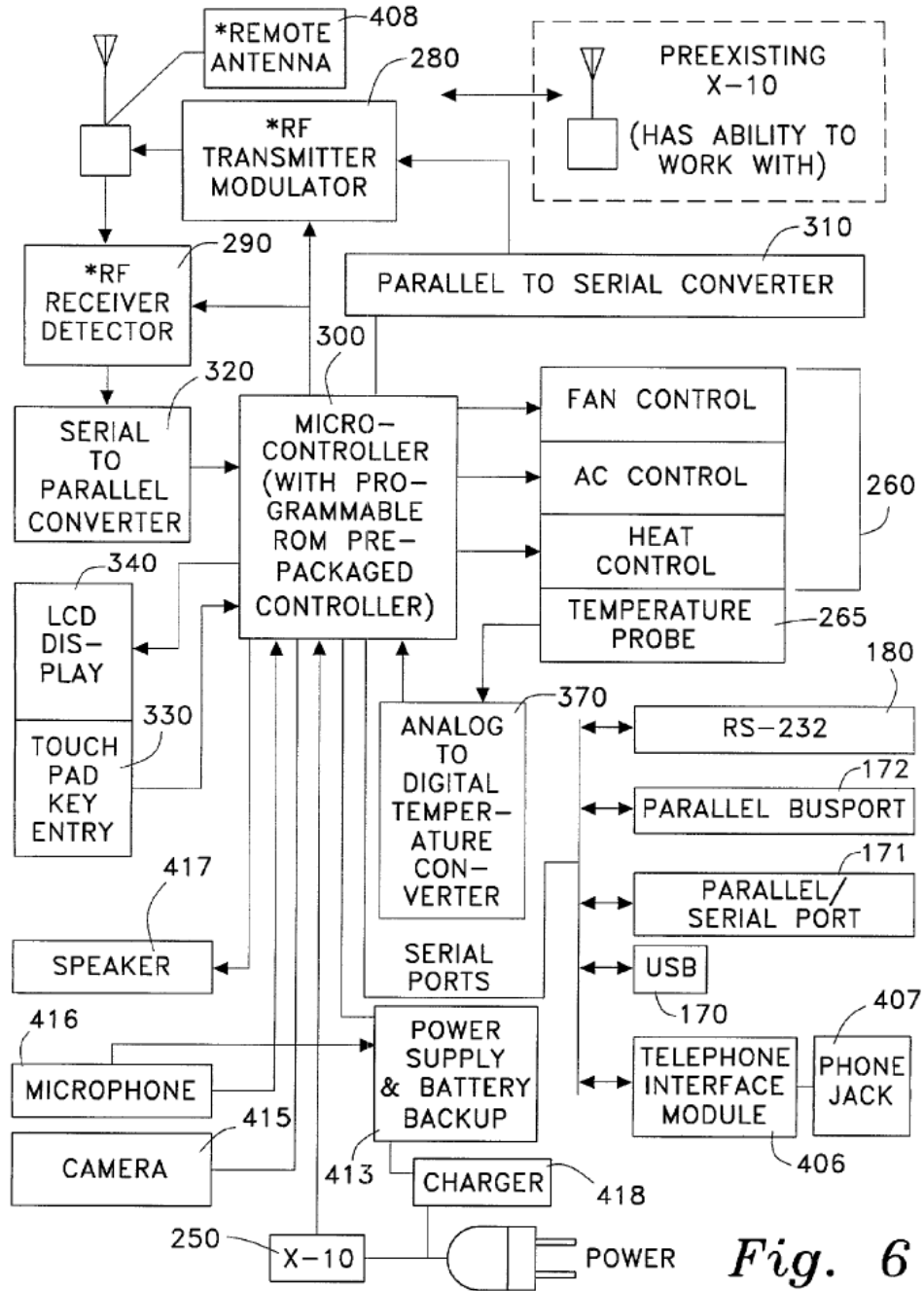


Fig. 6

Id., Figure 6. Accordingly, based on my current analysis, *Shamoon* discloses preamble 1[Pre].

- (ii) “1[a]: “A) means coupling suitable power for energizing said thermostat from said space conditioning equipment to said thermostat;”

250. *Shamoon* coupled with the general knowledge of a POSITA, or *Shamoon* in combination with *Cacciatore* discloses element 1[a]. As discussed above, this claim element is governed by 35 U.S.C. § 112, ¶6. *Supra*, § V.F.1. The function is “coupling suitable power for energizing said thermostat from said space conditioning equipment to said thermostat,” and the corresponding structure is a (power) line and any equivalents. *Id.* The disclosure of this claim element is discussed above in Sections VII.C.1.i and VII.C.2.iii. That discussion is incorporated by reference here. Accordingly, based on my current analysis, the combination of *Shamoon*, *Cacciatore* and the admitted prior art disclose and suggest to a POSITA each limitation of element 1[a].

251. It was well known in the prior art to use space conditioning equipment to provide energizing power to a thermostat. Indeed, the '825 Patent acknowledges that the use of space conditioning equipment to supply power to a thermostat system was “conventional[.]” EX1001, 5:3-5 (“In accordance with the prior art, power to the processor 1 is conventionally supplied from the space conditioning equipment 3 via a line 30 through an isolation diode 33”); *see also id.*, Figure 1, 2:18-19, 5:43-46; *see also* EX1013, 98:16-18 (“Q. There's no new isolation diode disclosed in the '825 Patent, correct? A. Correct.”).

(iii) 1[b]: “B) an interactive interface for a user to enter programming information into said thermostat;”

252. *Shamoon* also discloses element 1[b]. The '825 Patent does not purport to have invented an interactive interface for a user to enter programming information into said thermostat or improved upon existing interactive interfaces for a user to enter programming information into said thermostat. Moreover, it was well known in the art that thermostat systems include memory, as acknowledged by the '825 Patent. EX1001, Figure 1.

253. *Shamoon* discloses its “user interface includes both the hardware and the software via which a user interacts with a control system.” EX1008, ¶0012. *Shamoon* further discloses “an interface disposed in said housing; a plurality of icons on the interface, which correspond to a set of controls for items that are controlled by the apparatus.” *Id.*, Claim 40. *Shamoon* discloses a “thermostat and remote control apparatus 10 [that] has [a] ‘Program\Enter’ button 130 that allows a user to enter and activate a setting on the touchpad 330 display such as temperature settings to the thermostat 260.” *Id.*, ¶0074; *see also id.*, ¶0019.

254. Figure 2 of *Shamoon* illustrates buttons to enter various programming information into the thermostat system, such as temperature settings:

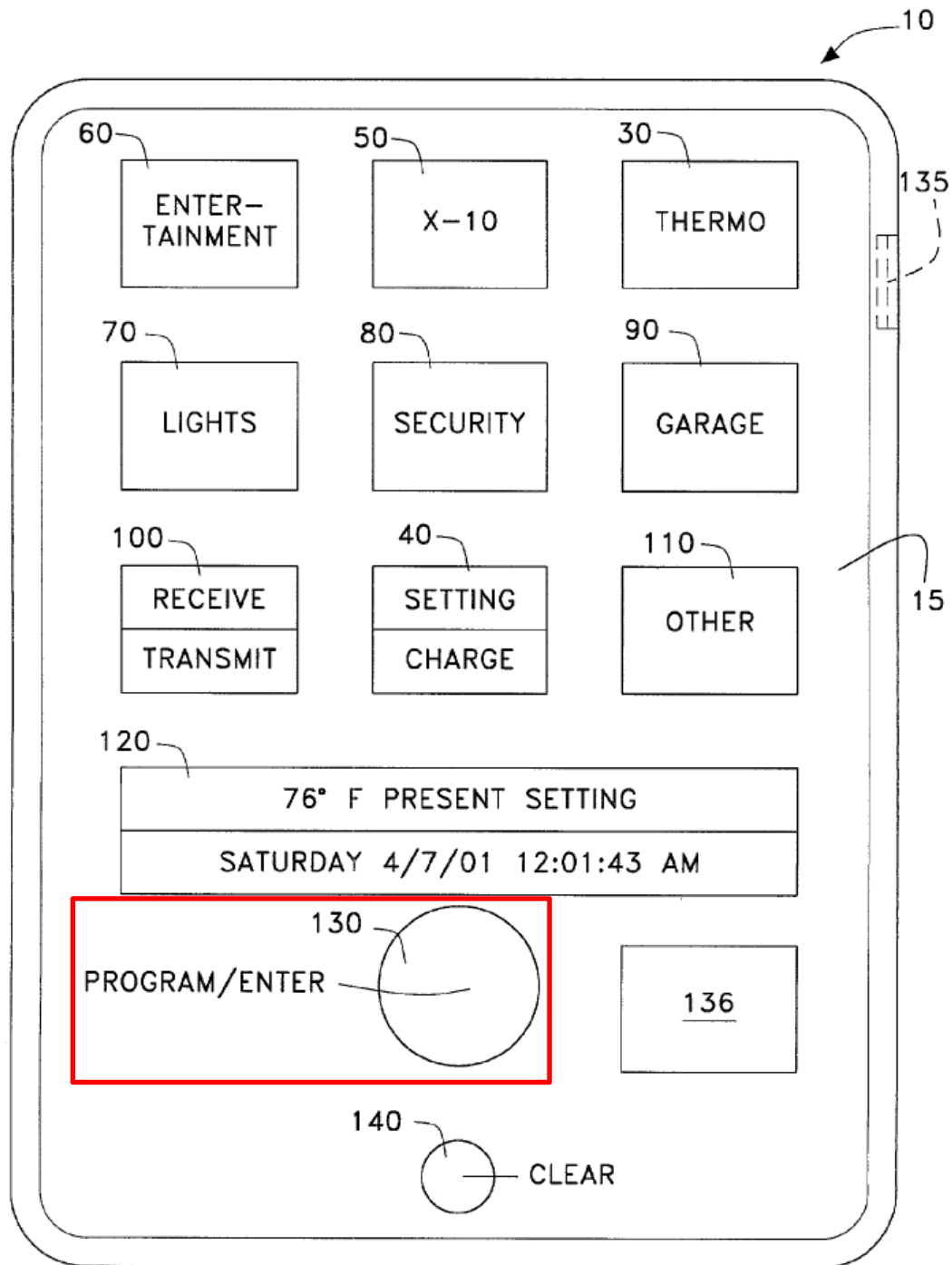


Fig. 2

Id., Figure 2 (annotated), ¶0074.

255. Users of the *Shamoon* system can also “enter[] desired information from a touchpad 330,” shown in annotated Figure 6 of *Shamoon* below:

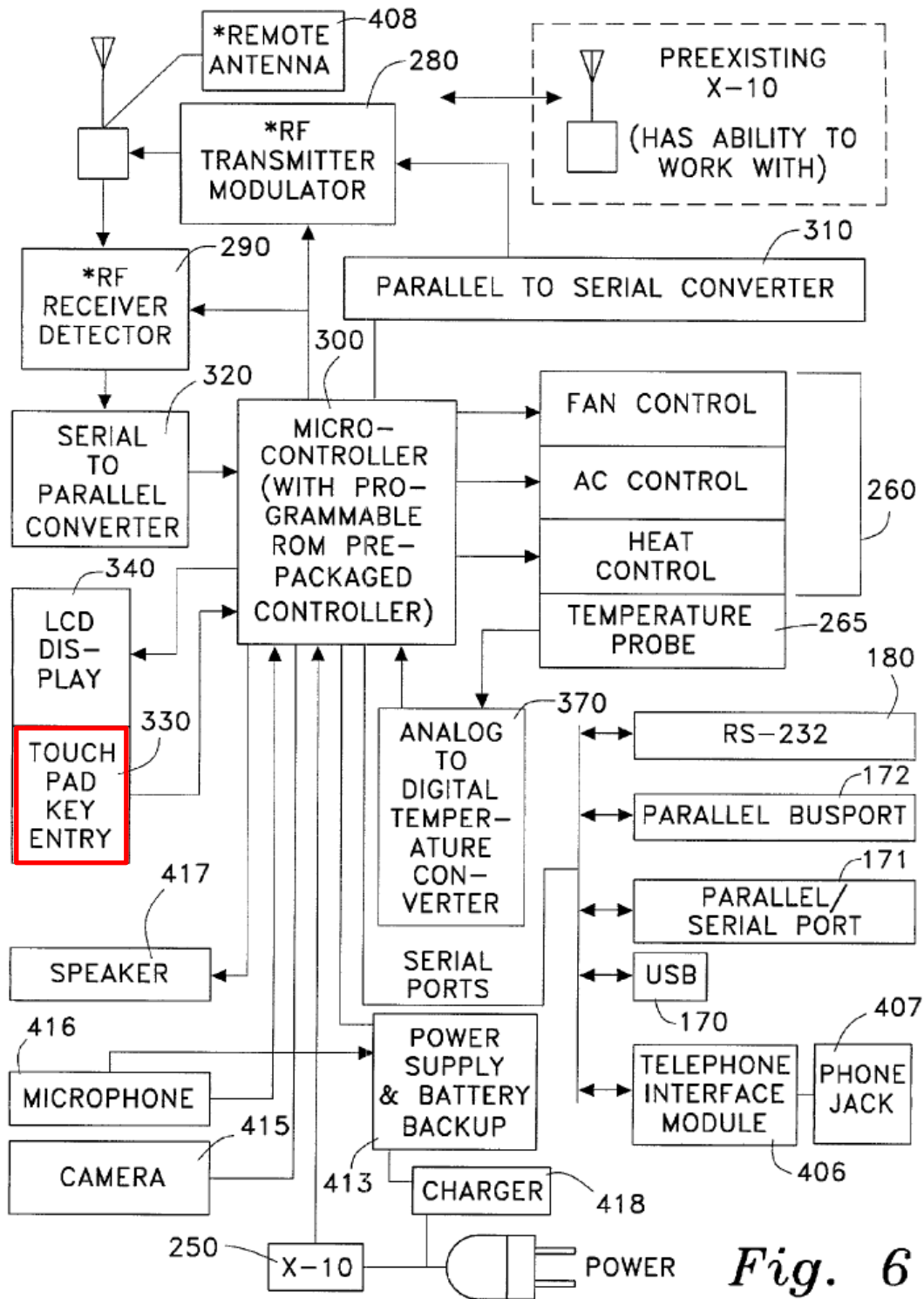


Fig. 6

Id., Figure 6 (annotated), ¶¶0070, 0087. Accordingly, based on my current analysis, *Shamoon* discloses element 1[b].

- (iv) 1[c]: “C) a temperature sensor for providing an electrical signal indicative of the temperature of a conditioned space in which the temperature sensor is situated;”

256. *Shamoon* or *Shamoon* in combination with the general knowledge of a POSITA discloses element 1[c]. The '825 Patent does not purport to have invented a temperature sensor for providing an electrical signal indicative of the temperature of a conditioned space in which the temperature sensor is situated or improved upon existing temperature sensors for providing an electrical signal indicative of the temperature of a conditioned space in which the temperature sensor is situated. Moreover, it was well known in the art that thermostat systems include temperature sensors to measure the temperature of a conditioned space, as acknowledged by the '825 Patent. EX1001, Figure 1, 5:28-35 (“Many modern thermostat include a real time clock, a memory and a data processor to run a process control program stored in the memory to accurately measure the temperature of a **temperature sensor disposed in the conditioned space** and to send control signals to the heating and/or cooling equipment to closely control the temperature of the conditioned space.”).

257. The use of temperature sensors with thermostat systems was well known before the priority date of the '825 Patent. *See, e.g.*, EX1004, ¶0002 (“Thermostats have been used for many years as a temperature sensitive switch

which controls heating and/or cooling equipment for conditioning a space in which the thermostat, or a temperature sensor connected to the thermostat, is placed.”), and ¶0003 (explaining that “[m]any modern thermostat systems include . . . a data processor to run a process control program stored in the memory to accurately measure the temperature of a temperature sensor disposed in the conditioned space”).

258. *Shamoon*’s thermostat system includes a “temperature probe 265” that “sends a signal to an analog to digital temperature converter 370, which sends a signal to the microcontroller 300.” *Id.*, ¶0071. It is shown in Figure 6:

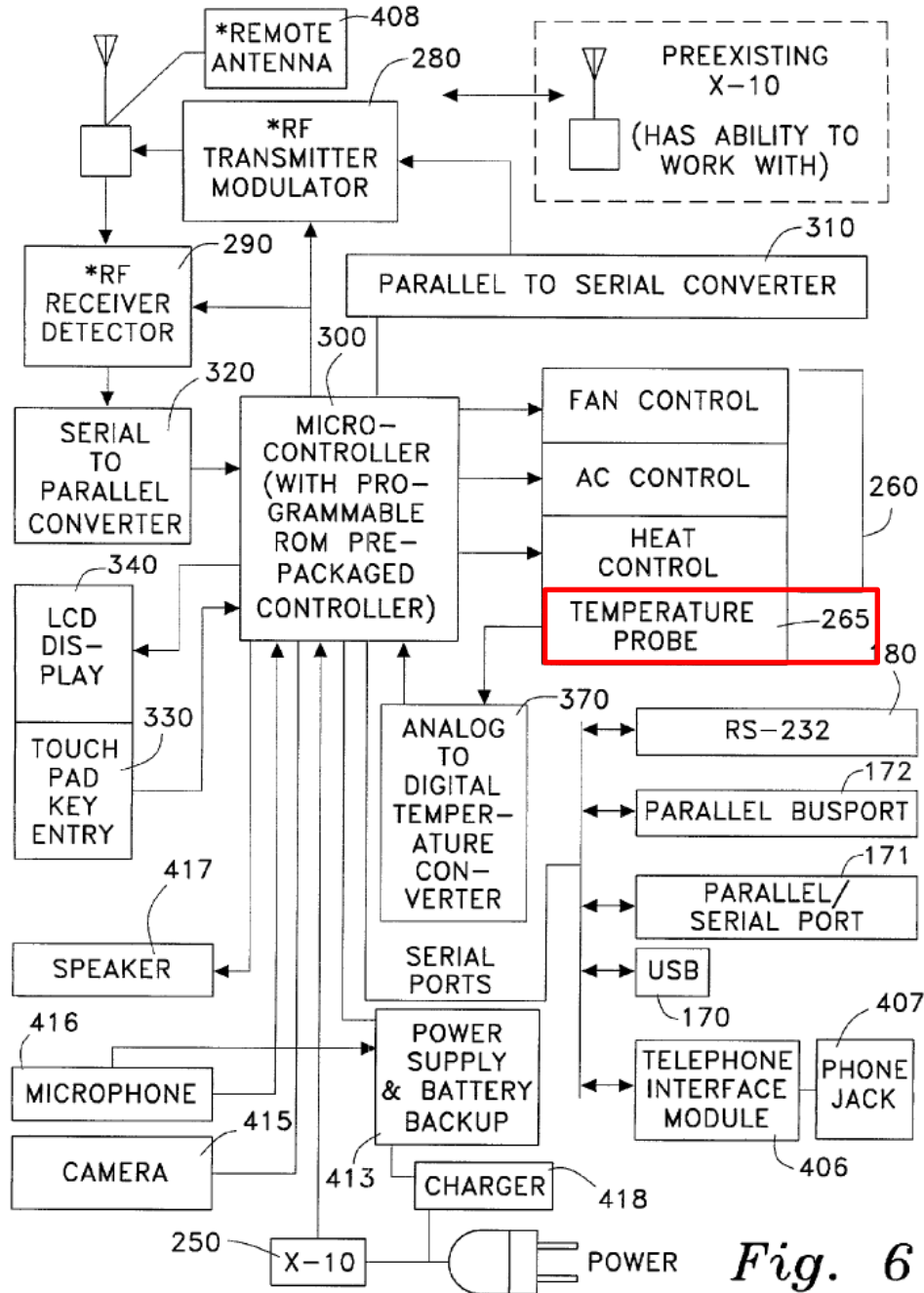


Fig. 6

Id., Figure 6 (annotated). This meets the limitations of element 1[c].

259. It was within the general knowledge of a POSITA that many modern thermostat systems include a temperature sensor for providing an electrical signal indicative of the temperature of a conditioned space, as acknowledged by the '825

Patent. EX1001, Figure 1, 1:28-35. The '825 Patent discloses 1[c] as a prior art element. EX1001, Figure 1, 3:54-57, 4:37-5:2. To the extent Patent Owner contends this element is missing from *Shamoon* or not obvious, the admissions in the Patent demonstrate that this element is within the general knowledge of a POSITA and would be obvious to use in a thermostat.

260. Thus, *Shamoon* discloses element 1[c].

(v) Elements 1[d]-1[g]:

1[d]: “D) a processor, said processor including:”

1[e]: “1) a central processing unit;”

1[f]: “2) a first memory coupled to said central processing unit for storing program and data information; and”

1[g]: “3) an input/output unit including:”

261. *Shamoon* or *Shamoon* in combination with the general knowledge of a POSITA also discloses elements 1[d]-1[g]. Annotated Figure 6 of *Shamoon* below shows the processor as microcontroller 300.

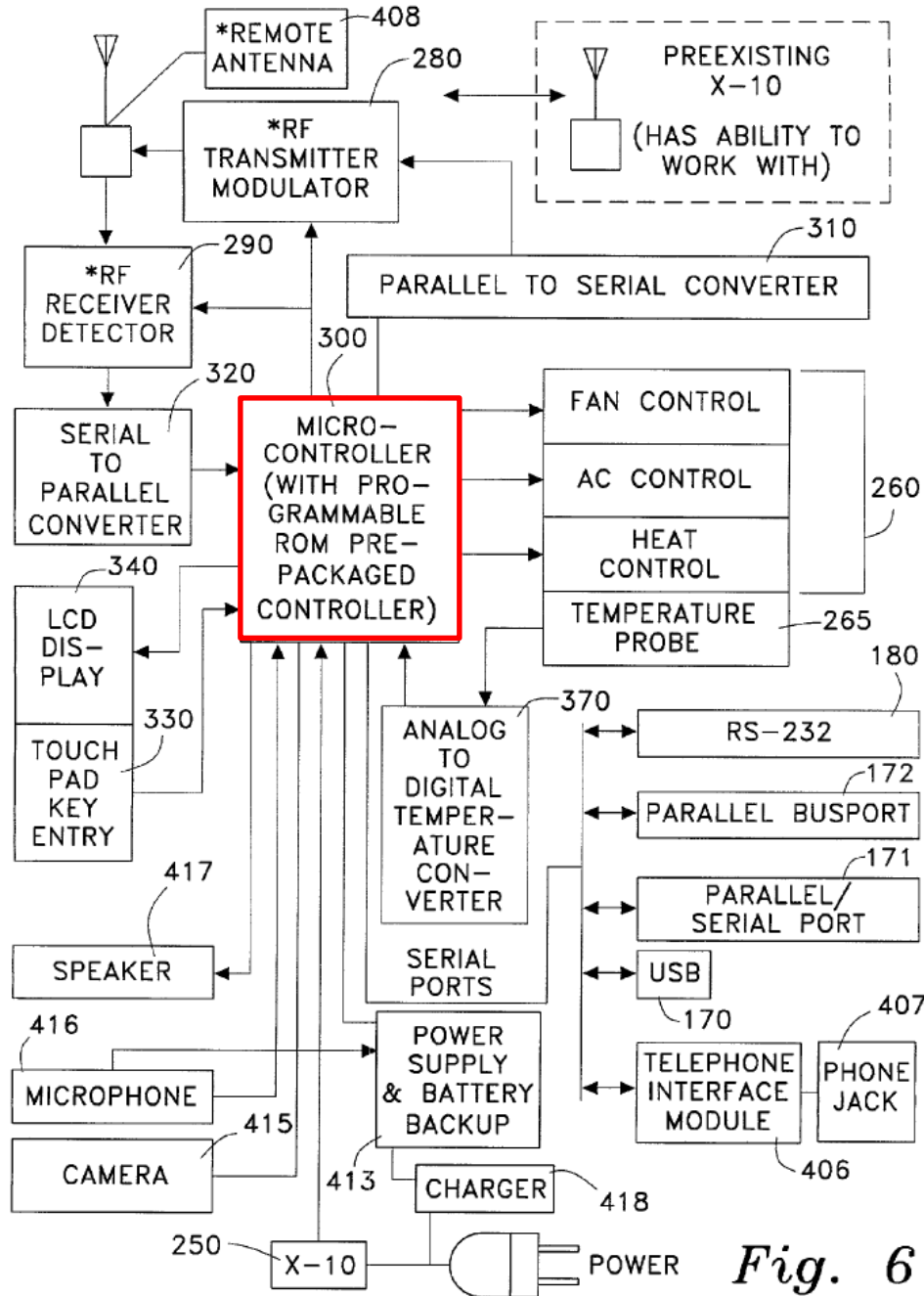
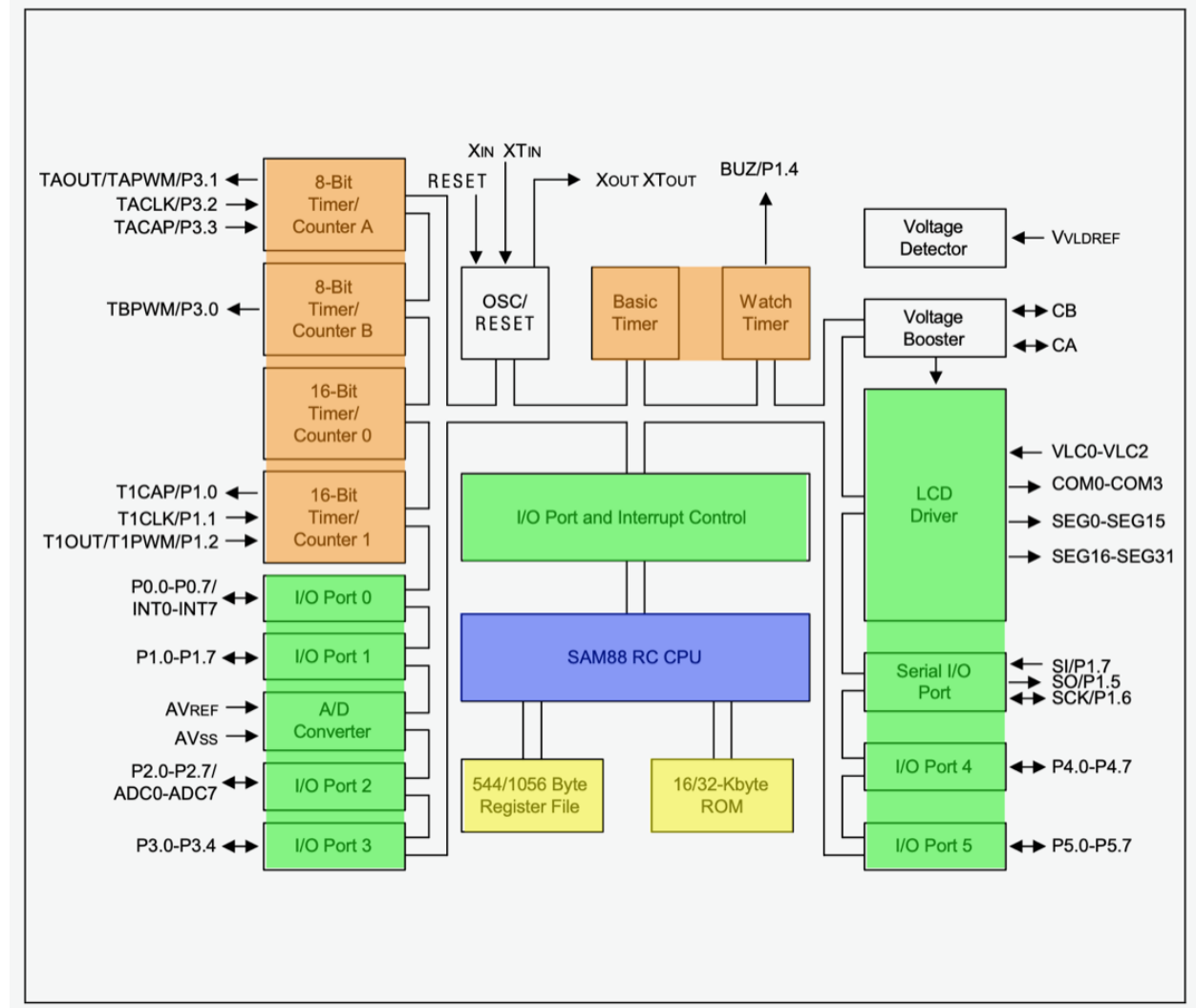


Fig. 6

EX1008, Figure 6 (annotated). Dictionaries in the relevant field of art define a microcontroller as a “highly integrated chip that contains all the components making up a controller. Typically this includes a **CPU**, **RAM**, some form of **ROM**, **I/O ports**, and timers.” EX1027, 3 (emphasis added). A POSITA would understand that

“CPU” is a central processing unit, “RAM” is random access memory, “ROM” is read-only memory, and “I/O” is input/output as these terms have been and continue to be commonly known, established and used in the art.

262. As a representative example of a microcontroller, *Carey* discloses that its programmable thermostat includes a “microprocessor 20 [that]... is preferably a 32Kb microprocessor S3C8249XZZ-OWR9 manufactured by Samsung.” EX1007, ¶0008. The data sheet for the S3C8249 microprocessor includes a block diagram that is annotated below to highlight the CPU (blue), memory (yellow), I/O unit (green) and timers (orange) included in the microprocessor.



EX1025, 3 (annotated).

263. Accordingly, a microcontroller, including *Shamoon's* microcontroller 300, is a processor and contains a central processing unit to run computer programs and perform mathematical operations. EX1013, 121:14-22. Thus, *Shamoon* discloses elements 1[d] and 1[e].

264. Further, *Shamoon* discloses memory that is part of the microcontroller that runs programs to control the thermostat. EX1008, ¶0060 (“The microcontroller

300 is also provided with programmable memory (such as RAM, PROM and flash PROM)"). A POSITA would understand that the memory stores data because *Shamoon* indicates that the microcontroller processes data. EX1008, Abstract, ¶0019. Inventor Rosen agrees that a prior art microcontroller could include the CPU, memory, and communications interface. EX1013, 101:6-20, 121:14-22.

265. The '825 Patent does not purport to have invented any of these elements or improved upon existing versions of these elements. Moreover, it was well known in the art that thermostat systems include these elements, as acknowledged by the '825 Patent. EX1001, Figure 1, 3:54-57, 4:10-5:17.

266. *Shamoon* further discloses an input/output unit. *Id.*, ¶0066. The "software internally of apparatus 10 which provides the interface between control, communications and software functions, and the LCD display, touch screen and I/O port data. The software also allows the apparatus 10 to accept and process the various I/O stimuli received for controlling, monitoring and processing information." *Id.* The microcontroller receives electrical signals from a temperature sensor 265 through analog to digital converter 370. EX1008, ¶0071. The circuitry within the microcontroller that receives the signal and/or that circuitry in combination with converter 370 are a sensor input that forms part of the input/output unit. The microcontroller outputs electrical signals to control space conditioning equipment.

Id. Thus, the microcontroller contains an input/output unit with a sensor input and control output.

267. It was within the general knowledge of a POSITA that many modern thermostat systems include a memory and a processor to run a control program stored in the memory. EX1001, Figure 8, 1:29-35. The '825 Patent discloses elements 1[d]-1[g] as prior art elements. EX1001, Figure 1, 3:54-57, 4:22-29; EX1013, 165:18-166:25. These admissions demonstrate these elements are within the general knowledge of a POSITA and would be obvious to use in a thermostat.

268. *Shamoon*'s microcontroller (element 1[d]) includes a central processing unit (element 1[e]), a memory for storing program and data information (element 1[f]), and an input/output unit (element 1[g]).

(vi) Elements 1[h]-1[j]

1[h]: “a) a sensor input coupled to said temperature sensor for receiving said electrical signal therefrom; and”

1[i]: “b) a control output coupled to the space conditioning equipment for issuing control signals thereto;”

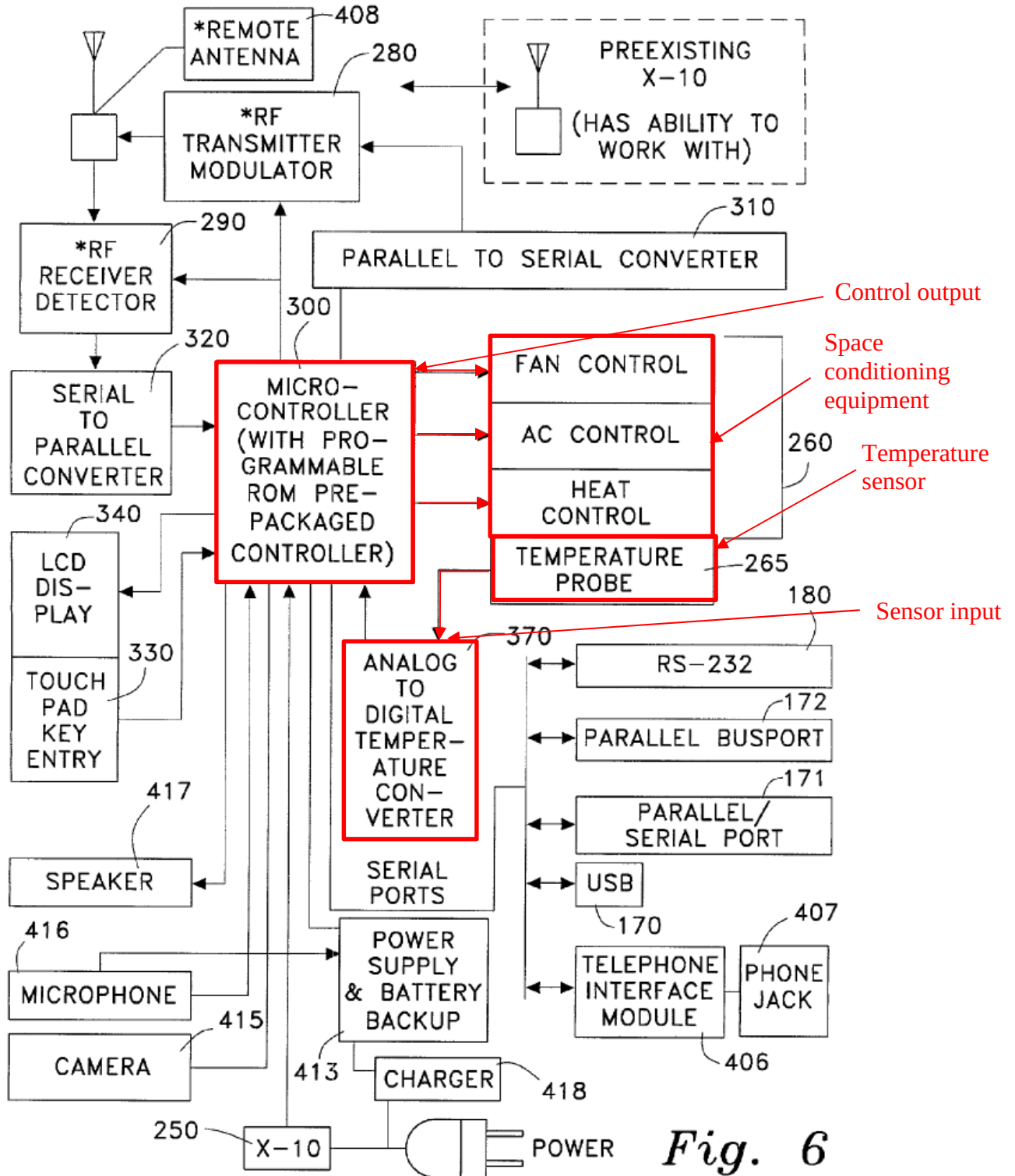
1[j]: “4) a real time clock;”

269. *Shamoon* or *Shamoon* in combination with the general knowledge of a POSITA discloses elements 1[h]-1[j]. The '825 Patent does not purport to have invented any of these elements or improved upon existing versions of these elements. Moreover, it was well known in the art that thermostat systems include

these elements, as acknowledged by the '825 Patent. EX1001, Figure 1, 5:28-35 (“Many modern thermostat include a ***real time clock***, ... a data processor to run a process control program ... to accurately ***measure the temperature of a temperature sensor*** disposed in the conditioned space and to ***send control signals to the heating and/or cooling equipment.***”) (emphasis added).

270. As discussed above for element 1[g], *Shamoon* discloses the claimed input/output unit. *Supra*, §VII.F.2.v; EX1008, ¶0066. As is typical for microtrollers, *Shamoon*'s microcontroller comprise a CPU, memory, and I/O unit. The existence of the input/output unit within *Shamoon*'s microcontroller is evidenced by the interfaces on and connection to the microcontroller itself. For example in Figure 6 below, *Shamoon*'s microcontroller is connected to a speaker, microphoner, camera, LCD, touchpad, RF receiver via a parallel interface, RF transmitter via parallel interface, X-10 powerline communications system, a fan, AC unit, heat unit, and temperature sensor via a digital interface. Thus, the knowledge of a POSITA as to microcontrollers comprising an I/O unit and/or *Shamoon*'s disclosure of a microcontroller with numerous interfaces discloses a processor with an I/O unit to a POSITA. That input/output unit of *Shamoon* includes the features recited in elements 1[h]-1[j]. For instance, *Shamoon* discloses an “intelligent thermostat which can control, monitor and communicate to a HVAC system and a thermostat and remote controller apparatus.” EX1008, ¶0025; *see also id.*, ¶¶0040, 0042.

271. Figure 6 of *Shamoon* illustrates “a remote control apparatus and its thermostat and X-10 components according to the present invention.”



Id., Figure 6 (annotated), ¶34.

272. As discussed above with respect to element 1[c], *Shamoon's* temperature probe 265 is a temperature sensor. *Supra*, § VII.F.2.iv. The temperature sensor connects to an analog to digital converter where the temperature sensor analog signal is converted to a digital signal sent to the microcontroller. EX1008, ¶0071; Figure 6. The circuitry within the microcontroller that receives the digital signal and/or that circuitry in combination with converter 370 constitutes a sensor input that forms part of the input/output unit. That circuitry is coupled to the temperature sensor as shown in Figure 6 and receives an electrical signal therefrom as required by element 1[i]. *Id.*

273. *Shamoon* also has a control output coupled to the space conditioning equipment for issuing control signals. *Shamoon's* thermostat includes “fan control,” “AC [Air Conditioning] Control,” and “heat control,” as illustrated above in Figure 6 of *Shamoon*. *Id.*, Figure 6. The fan, air conditioning and heat as controlled by *Shamoon's* system are examples of space conditioning equipment as claimed. EX1013, 96:5-8 (Testimony from the inventor of the '825 Patent confirming that “space conditioning equipment can refer to a furnace, an air conditioner, a heat pump, an emergency heater or a fan.”). *Shamoon's* “microcontroller 300 [] sends a signal to the fan control, air conditioning control and heat control of the thermostat 260,” and thus, the circuitry that does so within the microcontroller is a control

output for issuing control signals to the space conditioning equipment of *Shamoon*. EX1008, ¶0071. A POSITA would understand that circuitry within the microcontroller that generates these signals for control qualifies as the claim control output of element 1[i]. As illustrated in Figure 6 of *Shamoon* above, the control output (microcontroller) is coupled to the space conditioning equipment (fan, AC, heat) for issuing control signals thereto. *Id.*, Figure 6.

274. *Shamoon* also discloses element 1[j]. *Shamoon* discloses a “***built-in clock on the thermostat*** and remote control apparatus 10 that is synchronized to the thermostat 260.” EX1008, ¶0074; *see also id.*, Claim 18. *Shamoon* discloses, suggests, and makes obvious a real time clock as shown in Figure 2 below:

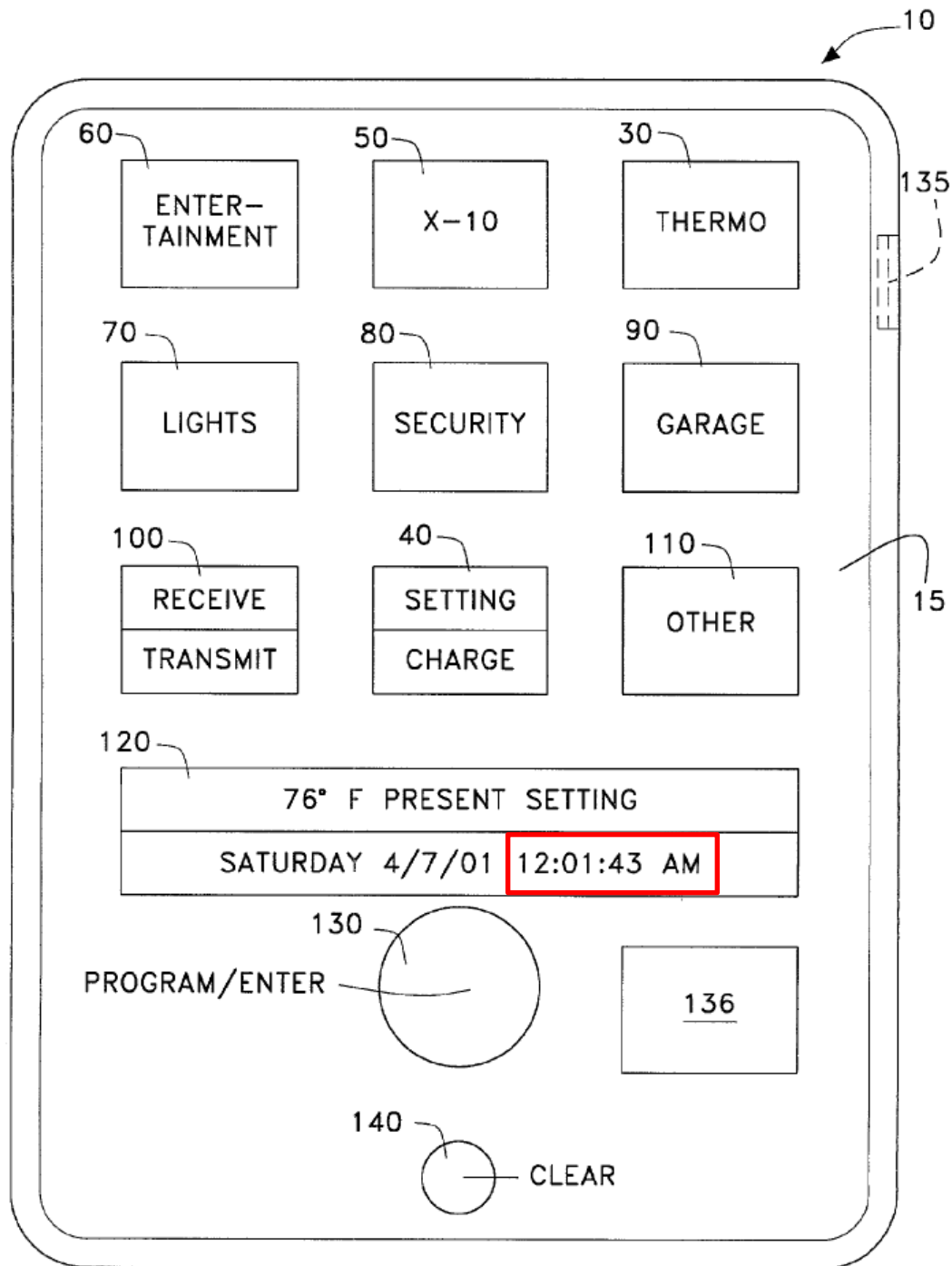


Fig. 2

Id., Figure 2 (annotated). *Shamoon's* "thermostat and remote control apparatus 10 can provide ... the time ... for the HVAC." *Id.*, ¶0059. Accordingly, based on my

current analysis, *Shamoon* discloses each limitation of claim 1[j].

275. It was within the general knowledge of a POSITA that many modern thermostat systems include items such as a real time clock and a processor to measure temperature from a sensor and to send control signals to control space conditioning equipment. EX1001 Figure 1, 1:29-35. The '825 Patent discloses elements 1[h]-1[j] as prior art elements. EX1001, Figure 1, 3:54-57, 4:22-5:2; EX1013, 93:6-94:2. These admissions demonstrate these elements are within the general knowledge of a POSITA and would be obvious to use in a thermostat.

(vii) 1[k]: “5) a non-volatile random access memory; and”

276. *Shamoon* or *Shamoon* in combination with *Shigeaki* discloses element 1[k]. The '825 Patent does not purport to have invented a non-volatile random access memory or improved upon existing non-volatile random access memory. Moreover, it was well known in the art that thermostat systems include memory, as acknowledged by the '825 Patent. EX1001, 1:29-30 (“Many modern thermostat[s] include ... **a memory.**”) (emphasis added); *see also id.*, Figure 1. *Shamoon* in combination with *Shigeaki* also discloses element 1[k].

277. *Shamoon*’s “microcontroller 300 is also provided with programmable memory (such as RAM, PROM and **flash PROM**).” EX1008, ¶0060 (emphasis added). Flash PROM is a non-volatile random access memory, satisfying element 1[k]. EX1019, 7:29-32 (“The non-volatile RAM 108 may be an electrically erasable

PROM or a ‘flash’ PROM which saves its contents even when power is lost.”).

Shamoon’s “auxiliary memory may include ... random access memory (RAM).”

EX1008, ¶0054. *Shamoon* suggests a non-volatile random access memory.

278. For the same reasons disclosed in Section VII.C.2.viii with respect to Ground 1, *Shigeaki* explicitly discloses element 1[k]. Non-volatile memory was well known in the art well before the priority date of the ’825 Patent. EX1013, 103:4-14. It was known to a POSITA prior to the claimed invention that the purpose of a non-volatile memory is to retain the contents of the memory even when no power is supplied to the memory. *Id.*, 104:14-25. It is not surprising that *Shamoon* and *Shigeaki* disclose this aspect of Claim 1.

279. *Shigeaki* relates to “a clock device in which power for operation is supplied via a commercial power source.” EX1006, ¶0001. *Shigeaki* discloses “a semiconductor non-volatile memory capable of storing data and electrically rewriting the stored data” as well as a “data reading means [that] reads time data and power outage data from the semiconductor non-volatile memory” when power is recovered after a power outage. EX1006, Claim 1, ¶0014; *see also id.*, Claim 2, ¶¶0007-0008. Specifically, *Shigeaki* discloses an EEPROM for this purpose. EX1006, ¶¶0030, 0061 (referred to as E²PROM).

280. When *Shigeaki’s* teachings are applied to *Shamoon*, in the combined system a non-volatile random access memory as taught by *Shigeaki* is used to store

the clock information and retain it during a power outage. As described above in Section VII.F.1.ii, it would have been obvious to a POSITA to combine *Shigeaki*'s teachings of using non-volatile memory and its method of handling time during a power outage with *Shamoon*'s programmable thermostat system to arrive at the claimed invention. *Supra*, § VII.F.1.ii.

281. Indeed, modifying *Shamoon* to incorporate the non-volatile memory disclosed in *Shigeaki* would merely involve the application of a known technique (the use of non-volatile memory as taught by *Shigeaki*) to a known device (*Shamoon*'s thermostat system) ready for improvement to yield predictable results (a thermostat system with improved functionality in the case of power outages). Moreover, non-volatile random access memory was commonly used in thermostat systems before the priority date of the '825 Patent for other purposes such as retaining data such as the temperature setting and schedules for automatically changing the thermostat so those are not lost during a power outage. A POSITA would be motivated to include nonvolatile memory in a thermostat for that reason as well.

282. Accordingly, based on my current analysis, *Shigeaki* and *Shamoon* both disclose element 1[k].

(viii) Elements 1[l]-1[n]

1[l]: “6) a control program stored in said first memory directing:”

1[m]: “a) said real time clock to periodically read its current time and date information into said non-volatile memory; and”

1[n]: “b) upon restart after a loss and then return of power from said space conditioning equipment, read the time and date information stored in said non-volatile memory into said real time clock.”

283. *Shamoon* in combination with *Shigeaki* discloses elements 1[l] -1[n]. It was well known in the art that thermostat systems include a control program stored in memory, as acknowledged by the '825 Patent. EX1001, 1:29-31. *Shamoon* discloses a control program—“prepackaged software [] that runs the hardware and other components of the thermostat and remote control apparatus 10.” EX1008, ¶0060. *Shigeaki* discloses a control program 1[l] with the capabilities of elements 1[m]-1[n].

284. As discussed above for element 1[j], the thermostat system of *Shamoon* includes a “real time clock. *See supra*, § VII.F.2.vi. As discussed above for element 1[k] both *Shamoon* and *Shigeaki* disclose a nonvolatile memory. *Supra*, § VII.F.2.vii.

285. *Shigeaki* discloses a “semiconductor non-volatile memory capable of storing data and electrically rewriting the stored data.” EX1006, Claims 1, 2, ¶¶0007-0008. The “data storage means,” non-volatile memory, of *Shigeaki* “stores the current time and the fact of the occurrence of the power outage in the semiconductor non-volatile memory as the current time data and power outage data.”

Id., ¶0013. *Shigeaki* further discloses “a data storage means for allowing the timekeeping means to **store the following data in the semiconductor nonvolatile memory ... the data of the current time** being measured by the remaining power and the fact that the power outage has occurred.” *Id.*, Claims 1, 2, ¶¶0007-0008 (emphasis added). Moreover, the “data storage means” of *Shigeaki* “stores the current time measured [by] the timekeeping means ... as the current time data.” *Id.*, ¶¶0013, 0039. A POSITA would understand that these steps occur due to action by a control program (or that is at least obvious) because a microprocessor running a control program typically causes data to be stored into memory and read from memory.

286. *Shigeaki* further discloses that when “a power outage of the commercial power supply is restored, ... the data reading means reads time data and power outage data from the semiconductor non-volatile memory.” EX1006, ¶0014. When the system disclosed in *Shigeaki* detects that power has been restored, it reads the power failure data and time data from the non-volatile memory to set the time of the clock. *Id.*, ¶0014-0015. “The data reading means reads the current time data and the power outage data from E²PROM 2 when power is restored after a power outage has occurred.” *Id.*, ¶0040.

287. The summary of what the control program of *Shigeaki* does is synonymous with elements 1[m]-1[n]. “When a power outage occurs, the time data

pertaining to the current time is stored in E²PROM 2, and when power is restored, the time data is read from E²PROM 2, and the time is resumed from the current time corresponding to the retrieved time data.” EX1006, ¶0061. A POSITA would understand that it is a control program storing the time/date data in nonvolatile memory and reading that data from the memory after a power outage and then resetting the clock using the stored data.

288. As described above in Section VII.F.1.ii, it would have been obvious to a POSITA to combine *Shigeaki*’s teachings of periodically storing time data into non-volatile memory and restoring the clock to that time after a power outage with *Shamoon*’s programmable thermostat system. *Supra*, § VII.F.1.ii. Accordingly, based on my current analysis, the combination of *Shigeaki* and *Shamoon* discloses and suggests to a POSITA elements 1[l]-1[n].

G. Ground 5: Claim 4 is obvious over *Shamoon* in view of *Cacciatore*, *Shigeaki* and *Toth*

1. Motivation to Combine

(i) Rationale and motivation for combining *Shamoon* and *Toth*

289. I provide *Toth* in grounds involving *Shamoon* with respect to the “vacation” elements of Claims 4, 13 and 16. These elements would be obvious in light of admissions in the specification of the ’825 Patent. As recognized by the inventor of the ’825 Patent, “[s]ome programmable thermostat systems incorporate a vacation mode in which different temperature set points for the several periods are

desirable in order to economize on the energy costs associated with conditioning the temporarily unoccupied space 4.” EX1004, ¶0035. “Typically, a programmable thermostat ... may include both normal and vacation modes.” EX1001, 1:44-50. Given these admissions, this element is within the general knowledge of a POSITA and it would be obvious to include a vacation mode of operation that is admitted as “typical[]” in the system of *Shamoon*.

290. The benefit of a vacation mode of operation is evident to a POSITA—it allows special thermostat settings to be easily invoked by a user of the thermostat when they are going on vacation in order to save energy while they are gone.

291. A vacation mode of operation is also obvious to use given the teachings of *Toth*. As an initial matter, *Shamoon* and *Toth* are in the same field of endeavor and are therefore analogous art to the ’825 Patent and each other. A POSITA would have been motivated to combine *Toth* with *Shamoon*.

292. *Shamoon* discloses the use of a thermostat and remote control apparatus for transmitting a signal to household appliances. EX1008, ¶0055, Figure 6. *Toth* similarly discloses that its “invention relates to thermostats, and in particular, to electronic programmable thermostats having different modes of operation.” EX1012, 1:5-9.

293. Based on *Toth*’s disclosure that the configuration it describes provides a means for “enter[ing] and configure[ing] a vacation mode of operation, such as

when a user leaves his home for a period of time and cannot view and program the thermostat 20 daily,” a POSITA would have been motivated to modify *Shamoon* to incorporate the vacation mode taught by *Toth* to improve the operation of *Shamoon*’s thermostat system. Modifying *Shamoon* to incorporate *Toth*’s teachings would merely involve the application of a known technique (a vacation mode of operation as taught by *Toth*) to a known device (the thermostat system of *Shamoon*) to obtain predictable results (a thermostat system that includes a vacation mode of operation). A POSITA would understand that a vacation mode is desirable to allow the user of a thermostat to save energy while on vacation and maintain control over the schedule of heating/cooling during the vacation. It is obvious to include this method of operation because it is a conventional method of controlling thermostat systems. EX1004, ¶0004.

294. A POSITA would have had a reasonable expectation of success in making the combination. It was conventional to include a vacation mode of operation in a thermostat system so a POSITA would just be using prior art structure/software to implement a known function. *Id.*, ¶¶0004, 0035; EX1001, 2:10-16; EX1013, 71:9-24. Including a vacation mode of operation would include simple modification of the thermostat software to incorporate the vacation mode.

2. Claim 4: “The thermostat of claim 1 which includes a vacation mode of operation.”

295. The *Shamoon-Cacciatore-Shigeaki-Toth* combined system discloses all elements in Claim 1 for the reasons discussed above for Claim 1. *Toth* discloses the new elements of Claim 4 as does the common knowledge of a POSITA. The '825 Patent does not purport to have invented a vacation mode of operation. Moreover, it was well known in the art that thermostat systems include vacation mode of operation, as acknowledged by the '825 Patent. EX1001, 1:60-61 (“The operation of programmable thermostats in the vacation mode is straightforward and well known.”). Thus, it would be obvious to use a vacation mode of operation because it is within the general knowledge of a POSITA.

296. Indeed, *Toth* discloses a “vacation mode of operation.” EX1012, 4:55-56. Thermostats that include a vacation mode of operation are well known in the art. See EX1004, ¶0004 (“Typically, prior art programmable thermostat system[s] ... may include a ***vacation mode***.”) (emphasis added). In the annotated figure below *Toth* illustrates how users can start, stop, or adjust vacation mode:

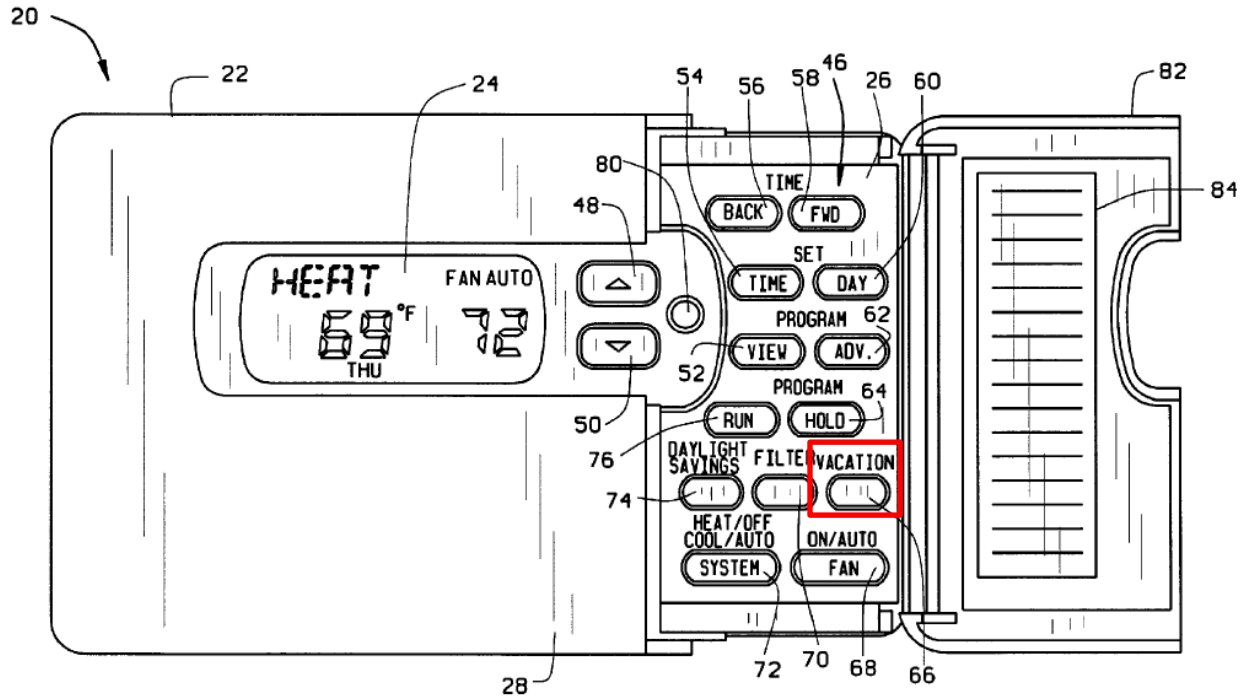


FIG. 1

EX1012, Figure 1 (annotated); *see also id.*, 4:1-7, 4:28-36, 4:51-58. *Toth* thus discloses each additional limitation of Claim 4. As discussed in Section § VII.G.1.i, a POSITA would have been motivated to incorporate *Toth*'s vacation mode of operation in order to improve upon the *Shamoon* thermostat. The motivation to combine *Toth* and *Shamoon* is discussed above, that discussion is incorporated by reference here. *Supra*, § VII.G.1.i.

H. Ground 6: Claims 11 and 12 are obvious over *Shamoon* in view of *Cacciatore*, *Shigeaki* and *Carey*

297. Based on the following analysis, I conclude that a POSITA at the relevant time (June 24, 2004) would have understood the limitations of Claims 11

and 12 were expressly disclosed, taught, or suggested by *Shamoon* in combination with *Cacciatore*, *Shigeaki* and *Carey*.

1. Claim 11

(i) Elements 11[pre]-11[j]

11[pre]: “A programmable thermostat for controlling space conditioning equipment comprising:”

11[a]: “A) means coupling suitable power for energizing said thermostat from said space conditioning equipment to said thermostat;”

11[b]: “B) an interactive interface for a user to enter programming information into said thermostat;”

11[c]: “C) a temperature sensor for providing an electrical signal indicative of the temperature of a conditioned space in which the temperature sensor is situated;”

11[d]: “D) a processor, said processor including:”

11[e]: “1) a central processing unit;”

11[f]: “2) a first memory coupled to said central processing unit for storing program and data information; and”

11[g]: “3) an input/output unit including:”

11[h] “a) a sensor input coupled to said temperature sensor for receiving said electrical signal therefrom; and”

11[i] “b) a control output coupled to the space conditioning equipment for issuing control signals thereto;”

11[j]: “4) a real time clock; and”

298. The analysis for elements 11[pre]-11[j] is identical to the analysis for Ground 4 as set forth in Sections VII.F.2.i-vi above. For clarity, each of these elements is also common knowledge of a POSITA as admitted in the '825 Patent as explained in the introduction to Claim 1 above. *Supra*, § VII.C.2.i.

- (ii) **11[k]: “5) a receiver adapted to receive current time and date information from an external source of the current time and date, said receiver being coupled to said real time clock such that the time and date information thereof is updated from said receiver.”**

299. *Shamoon* in combination with *Carey* together discloses element 11[k]. Claim 11 is directed to a thermostat with a second method to try to maintain the time as accurately as possible in the event of a power outage. The second method, however is also disclosed in the prior art—e.g., by *Carey*. The '825 Patent acknowledges that the use of receivers adapted to receive time and date information from an external source and use such information to update the real time clock was “well known in the art.” EX1001, 6:13-24 (“a wireless **receiver 50 is tuned to a source of precision time** such as WWVB which operates at 60 khz. Such receivers are **well known in the art and ... can readily be incorporated into a thermostat**. For example, a single chip WWVB receiver is available from Micro Analog Systems of Espoo, Finland, and is designated by part number MAS9178 in data sheet DA9178.000. **The output from the receiver 50 is ... the exact time ... and date.**

This information is used to periodically update the time and date information running in the real time clock 30.) (emphasis added).

300. As discussed above with respect to element 1[j], *Shamoon* discloses a “a built-in clock on the thermostat and remote control apparatus 10 that is synchronized to the thermostat 260.” EX1008, ¶0074; *Supra*, § VII.F.2.vi; *see also* EX1008, ¶0059, Figure 2. This is a real time clock. *Shamoon* also discloses a “RF [radio frequency] antenna and a IR [infrared] receiver.” EX1008, ¶64; *see also id.*, Figure 6. *Shamoon*, however, does not expressly disclose “a receiver adapted to receive current time and date information from an external source of the current time and date, said receiver being coupled to said real time clock such that the time and date information thereof is updated from said receiver.” EX1001, Claim 11.

301. *Carey* discloses this aspect of element 11[k] for the same reasons discussed above with respect to Ground 2. *Supra*, § VII.D.1.vii. Accordingly, based on my current analysis, the combination of *Carey* and *Shamoon* disclose element 11[k].

**(a) Rationale and motivation for combining
Shamoon and *Carey***

302. It would have been obvious to a POSITA to combine *Carey*’s receiver with *Shamoon*’s thermostat. Indeed, modifying *Shamoon* to incorporate the receiver of *Carey* would merely involve the simple addition of a known element (the receiver integrated circuit of *Carey*) for a disclosed and generally known function

(synchronizing time information) to obtain predictable results (a thermostat system with a receiver adapted to receive current time and date information from an external source to update the time and date of the thermostat system).

303. *Shamoon* and *Carey* are in the same field of endeavor and are therefore analogous art to the '825 Patent and each other. Both *Shamoon* and *Carey* relate to thermostats with real-time clocks. EX1008, ¶0074 (a “built-in clock on the thermostat and remote control apparatus 10 that is synchronized to the thermostat 260.”); EX1007, Abstract (“A digital programmable thermostat ... [that] can [] automatically set the current time and date.”). The reasoning discussed in Ground 2 for using *Carey* to keep the clock as accurate as possible, especially due to the stated advantages, applies equally to the combination with *Shamoon*. *Supra*, VII.D.1.ii.a.

304. Keeping the clock of a thermostat as accurate as possible when power is restored after a power outage was a recognized problem for thermostats. EX1001, 2:18-55. Inventor Rosen acknowledged that prior art thermostats addressed the issue of keeping the correct time during a power outage. EX1013, 75:8-25, 76:11-16. Thus, the problem of keeping the clock as correct as possible after a power outage was a recognized problem for thermostats. The '825 Patent discloses several prior art solutions to this problem—use of battery to power the clock or use of a capacitor to power the clock during a power outage. EX1001, 2:18-55. A POSITA would consider all available prior art methods to address that problem of keeping the clock

as accurate as possible in the event of a power outage and thus would turn to *Carey* as one design choice to solve the problem. Inventor Rosen agreed that a POSITA had various methods to choose from to keep the time as accurate as possible after a power failure. EX1013, 76:11-18. Given that *Carey* provides a method to keep time as accurate as possible after a power outage with identified advantages, it would be obvious to use the method of *Carey* in the thermostat of *Shamoon*. A POSITA would further understand from *Carey* that if the WWVB receiver was used, the receiver could be used to automatically reset the time after a power failure.

305. *Carey* explains a problem with thermostat programs is that they “require[] the user to complete a complex series of steps.” EX1007, ¶0001. *Carey* discloses a technique to “simplif[y] programming by setting the time for the user.” *Id.*, ¶0003. A POSITA would have been motivated to incorporate *Carey*’s known updating time and date from an external source technique in order to improve upon the *Shamoon* thermostat by making it easier to set the time.

306. Incorporating the aforementioned technique of *Carey*’s thermostat system would provide a better experience to the users of *Shamoon*’s thermostat system because they would not have to engage in the multi-step process *Carey* improves upon. *Id.*, ¶0001. This streamlines the programming of the *Shamoon* thermostat and would “allow a user to easily initiate a single set back program without having to set the current time and date.” *Id.*, ¶0004.

307. A POSITA would have had a reasonable expectation of success in making the combination. As an initial matter, implementing the known technique of *Carey* to reset a clock would only require the modification of conventional, well-known components, e.g., antenna and receiver, already present in the *Shamoon* system and the use of a WWVB receiver, which the '825 Patent teaches can be readily incorporated into a thermostat. *Compare id.*, Figure 1 and EX1008, Figure 6 (*Shamoon's* system includes a remote antenna and a receiver detector"); *see also* EX1001, 6:12-17 ("a wireless receiver 50 is tuned to a source of precision time such as WWVB which operates at 60 khz. ***Such receivers are well known in the art*** and may be implemented in small integrated circuits ***which can readily be incorporated into a thermostat.***") (emphasis added). Moreover, a POSITA would understand that antennas and receivers were commonly known in the art, and particularly, were included in thermostat systems. *See also* EX1007, ¶0009 ("WWVB's low frequency signal can cover the entire continental United States and much of Canada, and ***a small and relatively simple antenna and receiver can reliably decode the time code signal*** from any location in the continental United States."). Using such well-known hardware to receive WWVB signals and update time and date information is a conventional technique that was commonly known to a POSITA and known to be used in thermostat systems and analogous devices in the prior art.

308. A POSITA would have recognized that the systems described in *Shamoon* and *Carey* are remarkably similar as they are both thermostats with a real time clock. EX1008, ¶0073; EX1007, Abstract. The teachings of *Carey* are directed towards a “thermostat [that] can [] automatically set the current time and date”. EX1007, Abstract. While *Shamoon*’s thermostat and control apparatus periodically updates the time and date settings. EX1008, ¶0073. Given the similarities of the systems, a POSITA would have understood that *Carey*’s techniques were suitable for application with *Shamoon*’s thermostat system. Thus, a POSITA would have understood that *Carey*’s receiver and technique for updating time could be readily incorporated into the thermostat system of *Shamoon*. It would have been well within the abilities of a POSITA to modify the antenna and receiver in *Shamoon*’s thermostat to receive time code signal broadcasts from station WWVB as taught by *Carey*.

309. A POSITA would have had a reasonable expectation of success in making the combination. As an initial matter, it was well known to use receivers to receive time and date information from an external source and use such information to update the real time clock in a thermostat, as admitted by the ’825 Patent. EX1001, 6:13-24. Additionally, *Carey* elaborates that its antenna is “preferably a 60kHz LC tuned ferrite core antenna made by HKW Elektronik GmbH,” its receiver integrated circuit “is preferably an Atmel T4227 time code receiver chip,” and its

microprocessor “is preferably a 32Kb microprocessor S3C8249XZZ-OWR9 manufactured by Samsung.” EX1007, ¶0008.

310. Because the *Carey* system utilizes commercially available, off-the-shelf components, and known techniques it would have been well within the abilities of a POSITA to modify *Shamoon*’s thermostat system to include the antenna and receiver of *Carey* and its associated functionality (namely, the WWVB receiver adapted to receive current time and date information from an external source of the current time and date, said receiver being coupled to said real time clock such that the time and date information thereof is updated from said receiver).

2. Claim 12

(i) 12: “The thermostat of claim 11 in which said receiver receives wireless signals from said external source.”

311. The *Shamoon-Cacciatore-Carey* combined system discloses Claim 11 for the reasons discussed in Section VII.H.1 for Claim 11. As discussed above with respect to element 11[k] above, *Shamoon* modified by *Carey* discloses a receiver adapted to receive current time and date information from an external source of the current time and date. *Supra*, § VII.H.1.ii. The system disclosed in *Carey* discloses this element for the same reason discussed for Ground 2 (VII.D.1.ii) and includes a receiver that receives a “60kHz time code signal broadcast from station WWVB in Fort Collins.” EX1007, ¶0008. As a POSITA would understand, *Carey*’s WWVB

signals are wireless signals. Thus, *Carey* discloses the additional element of Claim 12.

312. The '825 Patent does not purport to have invented a receiver that receives wireless signals from said external source or improved upon existing receivers that receive wireless signals from said external source. Moreover, it was well known in the art that wireless receivers, like those disclosed in *Carey*, received wireless signals, as acknowledged by the '825 Patent. EX1001, 6:13-24 (“a **wireless receiver 50** is tuned to a source of precision time such as WWVB which operates at 60 khz. *Such receivers are well known in the art and ... can readily be incorporated into a thermostat.*”) (emphasis added).

I. Ground 7: Claims 13 and 16 are obvious over *Shamoon* in view of *Cacciatore*, *Carey*, and *Toth*

1. Claim 13

(i) 13: “The thermostat of claim 12 which includes a vacation mode of operation.”

313. *Toth* discloses Claim 13. The '825 Patent does not purport to have invented a vacation mode of operation or improved upon existing vacation modes of operation. Moreover, it was well known in the art that thermostat systems include a vacation mode of operation, as acknowledged by the '825 Patent. EX1001, 1:60-61 (“The operation of programmable thermostats in the vacation mode is straightforward and well known.”). Thus, Claim 13 is obvious because Claim 12 is

obvious and all that is added is something that is in the general knowledge of a POSITA, as admitted by the '825 Patent.

314. The *Shamoon-Cacciatore-Carey* combined system discloses Claim 12 for the reasons discussed above for Claim 12. *Toth* discloses the new limitations of Claim 13 as discussed above in Section § VII.I.1. As discussed in Section § VII.G.1.i, a POSITA would have been motivated to incorporate *Toth*'s vacation mode of operation in order to improve upon the *Shamoon* thermostat. The motivation to combine *Toth* and *Shamoon* is discussed above, that discussion is incorporated by reference here. *Supra*, § VII.G.1.i. Thus, the *Shamoon-Cacciatore-Carey-Toth* combined system discloses each and every element of Claim 13.

2. Claim 16

(i) 16: "The thermostat of claim 11 which includes a vacation mode of operation."

315. Claim 11 is disclosed for the reasons described above in Section § VII.H.1. The new limitations of Claim 16 are disclosed by *Toth* and Claim 16 is obvious for the same reasons as described in Section VII.I.1.i for Claim 13.

J. Ground 8: Claims 11 and 14 are obvious over *Shamoon* in view of *Cacciatore*, and *Williamson*

316. Based on the following analysis, I conclude that a POSITA at the relevant time (June 24, 2004) would have understood the limitations of Claims 11 and 14 were expressly disclosed, taught, or suggested by *Shamoon* in combination with *Cacciatore*, and *Williamson*.

1. Claim 11

(i) Elements 11[pre]-11[j]

11[pre]: “A programmable thermostat for controlling space conditioning equipment comprising:”

11[a]: “A) means coupling suitable power for energizing said thermostat from said space conditioning equipment to said thermostat;”

11[b]: “B) an interactive interface for a user to enter programming information into said thermostat;”

11[c]: “C) a temperature sensor for providing an electrical signal indicative of the temperature of a conditioned space in which the temperature sensor is situated;”

11[d]: “D) a processor, said processor including:”

11[e]: “1) a central processing unit;”

11[f]: “2) a first memory coupled to said central processing unit for storing program and data information; and”

11[g]: “3) an input/output unit including:”

11[h] “a) a sensor input coupled to said temperature sensor for receiving said electrical signal therefrom; and”

11[i] “b) a control output coupled to the space conditioning equipment for issuing control signals thereto;”

11[j]: “4) a real time clock; and”

317. The analysis for elements 11[pre]-11[j] is identical to the analysis for Ground 6 as set forth in Section VII.H.1.i above.

- (ii) **11[k]: “5) a receiver adapted to receive current time and date information from an external source of the current time and date, said receiver being coupled to said real time clock such that the time and date information thereof is updated from said receiver.”**

318. *Shamoon* in combination with *Cacciatore and Williamson* discloses element 11[k]. The '825 Patent acknowledges that the use of receivers adapted to receive time and date information and use such information to update the real time clock in a thermostat was “well known in the art.” EX1001, 6:13-24 (“a wireless *receiver 50 is tuned to a source of precision time* such as WWVB which operates at 60 khz. Such receivers are *well known in the art and ... can readily be incorporated into a thermostat. ... The output from the receiver 50 is ... the exact time ... and date. This information is used to periodically update the time and date information running in the real time clock 30.*”) (emphasis added).

319. As discussed above with respect to element 1[j], *Shamoon* discloses a real time clock. *Supra*, § VII.F.2.vi; *see also* EX1008, ¶0074. *Shamoon*, however, does not expressly disclose “a receiver adapted to receive current time and date information from an external source of the current time and date, said receiver being coupled to said real time clock such that the time and date information thereof is updated from said receiver.” EX1001, Claim 11. For the reasons discussed above in Section VII.E.1.ii in connection with Ground 3, *Williamson* discloses element 11[k].

**(a) Rationale and motivation for combining
Shamoon and *Williamson***

320. It would have been obvious to a POSITA to combine *Shamoon*'s programmable thermostat system with the connections of *Williamson*'s intelligent controller to an Internet service provider as suggested by the prior art. Modifying *Shamoon* to incorporate the Internet connectivity of *Williamson* would merely involve the simple addition of a known element (the Internet service provider connection, e.g., the cable modem or DSL router of *Williamson*) for a generally known function (receiving time information) to obtain predictable results (a thermostat system with a receiver adapted to receive current time and date information from an external source to update the time and date of the thermostat system). Moreover, *Shamoon* contemplates a "web-based thermostat." EX1008, ¶0083.

321. *Shamoon* and *Williamson* are in the same field of endeavor and are therefore analogous art to the '825 Patent and each other. Both *Shamoon* and *Williamson* relate to programmable home appliances that contain real-time clocks. EX1004, ¶0001; EX1007, ¶0001. Based on the teachings of *Shamoon*, a POSITA would have been motivated to modify *Shamoon* to incorporate the receiver of *Williamson* to improve upon *Shamoon*'s thermostat system. The intelligent controller of *Williamson* is a thermostat because it controls the heat in an oven. EX1010, 24:45-67.

322. Incorporating the aforementioned technique of *Williamson*'s thermostat system would improve *Shamoon*'s thermostat system by (a) automatically setting the clock for the user, thus saving the user time, and (b) automatically resetting the clock after a power outage thus maintaining the correct time shortly after time was restored. Use of *Williamson*'s technique would "assure[that] all clocks report the correct time." EX1010, 2:13.

323. As discussed above, *Shamoon* explains that "[d]ate, time and thermostat settings are updated from the thermostat 260 to the thermostat and remote control apparatus 10 periodically." EX1008, ¶0073. *Williamson*'s system includes such an arrangement. For example, *Williamson*'s thermostat system includes a "real-time clock 308 [that] is a digital chip that is programmable by the controller 210 in response to a synchronization signal (time message) being received at modem 206." EX1010, 8:37-40. However, *Williamson* further discloses "maintaining the correct time by synchronization of the real-time clock 308 with the correct time maintained at the web server 104." *Id.*, 8:45-48. *Williamson* also teaches "a different communication protocol may be used." *Id.*, 4:40-42. It would at once be obvious to a POSITA to use the well known NTP to connect to a server and obtain the time. As described in the introduction to IETF RFC 958, NTP is "a protocol for synchronizing a set of network clocks using a set of distributed clients and servers." See EX1024. As a POSITA would understand, connecting thermostats to the

Internet provides various known improvements, including improving upon the protocol to reset the time in the case of a power outage. EX1020, 9 n.10 (“A very different segment of the media coverage of “Internet appliances” concerns the notion of connecting traditional household appliances . . . to the Internet. . . . Some of these concepts make sense (e.g. connecting thermostats so you can program them through a Web site, not to have to reset time when power blinks, perform remote diagnostics on large appliances, etc.)”).

324. A POSITA would have had a reasonable expectation of success in making the combination of *Shamoon’s* thermostat system with *Williamson’s* receiver. As an initial matter, a POSITA would have recognized that the systems described in *Shamoon* and *Williamson* have remarkably similar functionalities relating to the real time clock elements. Thus, a POSITA would have understood that the receiver of *Williamson* could be readily incorporated into the thermostat system of *Shamoon*. In addition, *Williamson* teaches standard methods of connecting to the Internet. It would have been well within the abilities of a POSITA to modify *Shamoon’s* thermostat system to include any of the standard hardware needed for these methods of connection to receive the time over the Internet.

2. Claim 14

- (i) **14: “The thermostat of claim 11 in which said receiver receives signals via the Internet from said external source.”**

325. *Shamoon* in combination with *Cacciatore* and *Williamson* discloses the added elements of Claim 14. This combination discloses the elements of Claim 11 as set forth above in Section VII.J.1. As discussed above with regards to element 11[k], *Shamoon* modified by *Williamson* discloses a thermostat system that synchronizes and updates the real-time clock based on current time and date information received from an external source over the Internet.

326. The system disclosed in *Williamson* includes a receiver that “connect[s] with the Internet” and maintains the correct time. EX1010, 4:36-40, 5:34-36. Thus, the receiver in *Williamson* receives signals via the Internet from an external source, thereby disclosing the new limitation of Claim 14. “The web device 112” of *Williamson* “communicates with the server 104 over an Internet Protocol connection. In an alternate embodiment, the intelligent controller 102 may connected [sic] through an internet service provider and may even use a cable modem or DSL router to connect with the Internet.” *Id.*, 4:36-41; *see also* EX1020, 9 n.10. *Williamson* also teaches “a different communication protocol may be used.” EX1010, 4:40-42. It would at once be obvious to a POSITA to use the well known NTP to connect to a server and obtain the time. As described in the introduction to IETF RFC 958, NTP is “a protocol for synchronizing a set of network clocks using a set of distributed clients and servers.” *See* EX1024, 1. The *Shamoon-Williamson*

system receives current time and date information from the Internet, thus satisfying the limitations of Claim 14.

K. Ground 9: Claims 15 and 16 are obvious over *Shamoon* in view of *Cacciatore*, *Williamson*, and *Toth*

1. Claim 15

(i) 15: “The thermostat of claim 14 which includes a vacation mode of operation.”

327. *Toth* discloses Claim 15. The ’825 Patent admits that this additional element of Claim 15 was known in the prior art. EX1001, 1:60-61 (“The operation of programmable thermostats in the vacation mode is straightforward and well known.”). Thus, Claim 15 is obvious in light of the general knowledge of a POSITA.

328. The *Shamoon-Cacciatore-Williamson* combination discloses the elements of Claim 14 as discussed in Section VII.J.2. *Toth* discloses a thermostat with a vacation mode of operation as set forth in Section VII.I.1.i. Thus, the *Shamoon-Cacciatore-Williamson-Toth* combination discloses all elements of Claim 15.

329. The motivation to combine *Toth* and *Shamoon* is discussed above, that discussion is incorporated by reference here. *Supra*, § VII.G.1.i.

2. Claim 16

(i) 16: “The thermostat of claim 11 which includes a vacation mode of operation.”

330. Claim 11 is disclosed for the reasons described above in Section VII.J.1. The new limitations of Claim 16 are disclosed by *Toth* and Claim 16 is obvious for the same reasons as described in Section VII.I.1 for Claim 13.

L. SECONDARY CONSIDERATIONS

331. During prosecution of the '825 Patent, the applicant did not identify any evidence of secondary considerations of non-obviousness tied to the claimed invention of the '825 Patent. I understand from counsel for Petitioner that Patent Owner in the co-pending district court litigation has not yet identified any evidence with respect to secondary considerations of non-obviousness. I am also unaware of any secondary considerations that would suggest non-obviousness.

332. Accordingly, based on my current analysis, there is no objective evidence of non-obviousness that might warrant a finding that Claims 1, 4 and 11-16 are patentable. To the extent the Patent Owner at a later date cites or provides any other evidence regarding secondary considerations, including any expert opinions, I reserve the right to supplement my analysis and opinions to address it.

VIII. CONCLUSION

333. For at least the above-described reasons, in my opinion Claims 1, 4 and 11-16 of the '825 Patent would have been obvious to a POSITA based on the prior art references that I have cited and analyzed above.

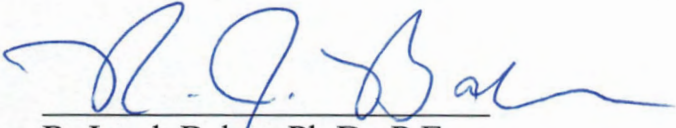
334. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, upon request with reasonable notice to allow me to manage my professional schedule including other obligations to federal courts, the ITC, and the Board, I will appear for cross-examination within the United States during the time allotted for cross-examination.

335. I reserve the right to supplement my opinions in the future to respond to any arguments raised by Patent Owner and to consider any new information that becomes available to me.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed this 28th day of March 2023, in LAS VEGAS, NV.

Respectfully submitted,



R. Jacob Baker, Ph.D., P.E.

APPENDIX A

R. JACOB (JAKE) BAKER, PH.D., P.E.

Professor Pristinus of Electrical and Computer Engineering
Independent Consultant

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Las Vegas, NV 89120

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PROFESSIONAL SUMMARY

Russel Jacob (Jake) Baker, Ph.D., P.E. (IEEE Student Member 1983, Member 1988, Senior Member 1997, and Fellow 2013) was born in Ogden, Utah, on October 5, 1964. He received the B.S. and M.S. degrees in electrical engineering from the University of Nevada, Las Vegas, in 1986 and 1988. He received the Ph.D. degree in electrical engineering from the University of Nevada, Reno in 1993. His Google Scholar profile is [here](#) and his ResearchGate profile is [here](#).

From 1981 to 1987 he served in the United States Marine Corps (from September of 1982 in the Reserves, Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division). From 1985 to 1993 he worked for E. G. & G. Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapons tests at the Nevada Test Site. During this time, he designed, and oversaw the fabrication and manufacture of, over 30 electronic and electro-optic instruments including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame- and bit-syncs, data converters, streak-camera sweep circuits, Pockels cell drivers, micro-channel plate gating circuits, and analog oscilloscope electronics. From 1991-1992 he was an adjunct faculty member in the department of electrical engineering at the University of Nevada, Las Vegas (UNLV). From 1993 to 2000 he served on the faculty in the department of electrical engineering at the University of Idaho (UI), first as an untenured Assistant Professor and then from 1998 as a tenured Associate Professor. In 2000 he joined a new electrical and computer engineering (ECE) program at Boise State University (BSU) where he was promoted to Full Professor in 2002. He then served as the ECE department chair at BSU from 2004 to 2007. At BSU he helped establish graduate programs in ECE including, in 2006, the university's second PhD degree. In 2012 he re-joined the faculty at UNLV as a tenured Full Professor of ECE. During his service at the UI, BSU, and UNLV he has been the major professor to more than [100 graduate students](#). In addition to this industry and academic experience, he has done consulting, both technical and expert witness, for over [200 companies](#).

Over the last 35+ years his [research/development interests](#) and [publications](#) have been, or currently are, focused on: analog-to-digital/digital-to-analog data conversion and transmission, optoelectronics (imagers, displays, LIDARs, APDs, SiPMs, and associated electronics), analog and digital integrated circuit design and fabrication, design of diagnostic electrical and electro-optic instrumentation for scientific research, integrated electrical/biological circuits and systems, array (memory, imagers, and displays) fabrication and design, CAD tool development and online tutorials, low-power interconnect and packaging (electrical and optical) techniques, design of wired/wireless communication and interface circuits, circuit design for the use and storage of renewable energy, power electronics and power supply design, and the delivery of [online engineering education](#).

Dr. Baker is the named inventor on over [150 US patents](#). He is a member of the honor societies Eta Kappa Nu and Tau Beta Pi, a licensed Professional Engineer, a popular lecturer that has delivered over [50 invited talks](#) around the world, an IEEE Fellow, and the author of the books CMOS Circuit Design, Layout, and Simulation, CMOS Mixed-Signal Circuit Design, and a coauthor of DRAM Circuit Design: Fundamental and High-Speed Topics. He received the 2000 Best Paper Award from the IEEE Power Electronics Society, the 2007 Frederick Emmons Terman Award,

the 2011 IEEE Circuits and Systems Education Award and the 2021 Wiley-IEEE Press Textbook Award for the 4th Edition of his book CMOS Circuit Design, Layout, and Simulation.

His service activities include the IEEE Press Editorial Board (1999-2004), editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018), the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015), the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), Distinguished Lecturer for the SSCS (2012-2015), Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for the IEEE Solid-State Circuits Magazine, IEEE Kirchhoff Award Committee (2020-2023), and advisor for the student branch of the IEEE at UNLV (2013-2023).

INDUSTRY EXPERIENCE

2008 - present: Expert witness in intellectual property disputes in electrical, electro-optic, and computer engineering matters for: 1) district court and ITC patent disputes, 2) inter partes reviews at the PTAB, and 3) arbitrations and mediations.

2013 - 2022: Worked with Freedom Photonics, Santa Barbara, CA, on the integration, fabrication and design, of optoelectronics with CMOS integrated circuits. Work includes the design of compact optical transceivers for range finding applications, high-efficiency integrated silicon avalanche photodetectors for quantum key receivers, Geiger mode SiGe receivers for long-range communications, cryptography, and the fabrication of near-infrared focal plane arrays. Packaging and testing of numerous chips fabricated in both CMOS and SiGe technologies using LEDs, ILDs, PIN, APDs, and ROICs.

2017 - 2019: Worked with Vorpil Research Systems, Las Vegas, NV on the design of integrated circuit electronics and optoelectronics for optical transceivers used in LIDARs/LADARs.

2016 - 2019: Worked with Attollo Engineering on the design of transient digitizers for the capture of high-speed signals for range finders using LEDs and lasers in compact optical transceivers.

2013 - 2018: Working with Mission Support and Test Services, LLC (MSTS, formerly National Security Technologies, LLC, [NSTec]) on the Design and Fabrication of Integrated electrical/photonics application specific integrated circuit (ASIC) design for use in the implementation of diagnostic instrumentation.

2013 - 2015: Consultant for OmniVision. Working on integrating CMOS image sensors (CIS) with memory for very high-speed consumer imager products. Design specialty DRAM, high-speed interfaces between CIS and DRAM, packaging techniques to pair the CIS with DRAM.

2010 - 2013: Worked with Arete' Associates on the design of high-speed compressive transimpedance amplifiers for LADAR projects and the design of ROIC unit cells. Work funded by the U. S. Air Force.

2013: Cirque, Inc. Consulting on the design of analog-to-digital interfaces for capacitive touch displays and pads.

2012: Consultant at Lockheed-Martin Santa Barbara Focal Plane Array. CMOS circuit design and fabrication for the development and manufacture of infrared components and imaging systems with an emphasis on highest sensitivity Indium Antimonide (InSb) focal plane arrays (FPAs) in linear through large staring formats. Product groups include FPAs, integrated dewar assemblies (IDCAs), camera heads, high-speed interfaces between image processors and imaging systems, and infrared imaging systems.

2010 - 2012: Working with Aerius Photonics (and then FLIR Inc. when Aerius was purchase by FLIR) on the design of Focal Plane Arrays funded (SBIRs and STTRs) by the U.S. Air Force, Navy, and Army. Experience with readout integrated circuits (ROICs) and the design/layout of photodetectors in standard CMOS.

2009 - 2010: Sun Microsystems, Inc. (and then Oracle) VLSI research group. Provided consulting on memory circuit design/fabrication and proximity connection (PxC) interfaces to DRAMs and SRAMs for lower power, 3D packaging, for memory modules and controllers implemented with FPGAs and custom ASICs.

2009 - 2010: Contour Semiconductor, Inc. Design of NMOS voltage and current references as well as the design of a charge pump for an NMOS memory chip.

1994 - 2008: Affiliate faculty (Senior Designer), Micron Technology. Designed CMOS circuits for DRAMs including DLLs, PLLs for embedded graphics chips, voltage references and regulators, data converters, field-emitting display drivers, sensing for MRAM (using delta-sigma data conversion topologies), SRAMs, RFIDs, CMOS active pixel imagers and sensors, power supply design (linear and switching), input buffers, etc. Worked on a joint research

project between Micron and HP labs in magnetic memory fabrication and design using the MTJ memory cell. Worked on numerous technologies ranging from LED lighting to medical imaging using CMOS image sensors (too many to list) resulting in numerous US patents (see following list). Considerable experience working with product engineering to ensure high-yield from the production line from fabrication to test. Co-authored a book on DRAM circuit design through the support of Micron. Gained knowledge in the entire memory design process from fabrication to packaging. Developed, designed, and tested circuit design techniques for multi-level cell (MLC) Flash memory using signal processing.

January 2008: Consultant for Nascentric located in Austin, TX. Provide directions on circuit operation (DRAM, memory, and mixed-signal) for fast SPICE circuit simulations.

May 1997 - May 1999: Consultant for Tower Semiconductor, Haifa, Israel. Designed CMOS integrated circuit cells for various modem chips, interfaces, and serial buses including USB circuits, charging circuits based upon power up/down circuits using an MOS or bandgap reference, pre-amplifiers, comparators, etc.

Summer 1998: Consultant for Amkor Wafer Fabrication Services, Micron Technology, and Rendition, Inc., Design PLLs and DLLs for custom ASICs and a graphics controller chip.

Summers 1994 - 1995: Micron Display Inc. Designing phase locked loop for generating a pixel clock for field emitting displays and a NTSC to RGB circuit on chip in NMOS. These displays are miniature color displays for camcorder and wrist watch size color television. Worked on the fabrication and design of video peripheral circuits for these displays.

September - October 1993: Lawrence Berkeley Laboratory. Designed and constructed a 40 A, 2 kV power MOSFET pulse generator with a 3 ns rise-time and 8 ns fall-time for driving Helmholtz coils.

Summer 1993: Lawrence Livermore National Laboratory, Nova Laser Program. Researched picosecond instrumentation, including time-domain design for impulse radar and imaging.

December 1985 - June 1993: (from July 1992 to June 1993 employed as a consultant while finishing up my Ph.D.), E.G.&G. Energy Measurements Inc., Nevada, Senior Electronics Design Engineer. Responsible for the design and manufacturing of instrumentation used in support of Lawrence Livermore National Laboratory's Nuclear Test Program. Responsible for designing and fabricating over 30 electronic and electro-optic instruments including: CCD camera design, communication networks, fiber optic transmitters employing high speed laser drive electronics, receivers employing envelop tracking for DC voltage restoration and regeneration of received information, receiver low noise amplifier design, frame synchronizers for re-assembling transmitted images, high-speed SRAM memory system design with battery back-up, calibration equipment design such as a tunnel diode pulse generator for testing compensation of oscilloscopes and DAC design for calibrating CCD readout electronics, power supply and battery charger designs, sweep circuits for streak cameras, Pockel's cell drive electronics, vertical amplifier design using HBTs for analog oscilloscopes used at the Nevada Test Site, and 10 kV ramp designs using a planar triode to name some of the designs.

This position provided considerable fundamental grounding in EE with a broad exposure ranging from the design of PC boards to, for example, the design of cable equalizers. Summarizing, gained experience in circuit design technologies including: bipolar, vacuum tubes (planar triodes for high voltages), hybrid integrated circuit fabrication and design, GaAs (high speed logic and HBTs), Mach-Zehnder interferometers, Pockels cells, krytrons, power MOSFETs, microwave techniques, power supplies, fiber optic transmitters/receivers, etc.

Summer 1985: Reynolds Electrical Engineering Company, Las Vegas, Nevada. Gained hands on experience in primary and secondary power system design, installation and trouble-shooting electric motors on mining equipment.

ACADEMIC EXPERIENCE

January 1991 – present: Professor of Electrical and Computer Engineering at the **University of Nevada, Las Vegas** from August 2012 to present. From January 2000 to July 2012 held various positions at **Boise State University** including: Professor (2003 – 2012), Department Chair (2004 - 2007), and tenured Associate Professor (2000 - 2003). From August 1993 to January 2000 was a tenured/tenure track faculty member at the **University of Idaho:** Assistant Professor (1993 - 1998) and then tenured Associate Professor (1998 - 2000). Lastly, from January 1991 to May 1993 held adjunct faculty positions in the departments of Electrical Engineering at the University of Nevada, Las Vegas and Reno. Additional details:

- Research is focused on analog and mixed-signal integrated circuit fabrication and design. Worked with multi-disciplinary teams (civil engineering, biology, materials science, etc.) on projects that have been funded by EPA, DARPA, NASA, Army, DMEA, Navy, and the AFRL.
- Current and past research and development interests are:
 - Design and packaging of electrical/optical systems (e.g., LiDARs/LADARs) using LEDs, semiconductor lasers, lens for focusing and directing light, integrated circuits, and associated control and communication systems/circuits.
 - Capacitive sensing techniques using delta-sigma modulation and interfacing to sensors
 - Design of high-voltage and energy switching circuits
 - Circuit design and fabrication for the control, use, and storage of renewable energy using thermoelectric generators
 - Design of electrical/biological/optical circuits and systems using electrowetting on dielectric for automating and controlling biological experiments
 - Design of readout integrated circuits (ROICs) for use with focal plane arrays (FPAs)
 - Heterogeneous integration of III-V photonic devices (e.g., FPAs and VCSELs) with CMOS
 - Methods (e.g., 3D packaging and capacitive interconnects) to reduce power consumption in semiconductor memories, memory modules, and digital systems using custom and non-custom (e.g., FPGAs) implementations
 - Analog and mixed-signal circuit fabrication and design for communication systems, synchronization, energy storage, data conversion, and interfaces
 - The design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g., magnetic, chalcogenide)
 - Reconfigurable electronics design and fabrication using nascent memory technologies such as the memristor to implement FPGAs
 - Finding an electronic, that is, no mechanical component, replacement for the hard disk drive using nascent fabrication technologies
 - Power electronics circuit design for consumers and consumer electronics including power management and adaptive control to reduce power consumption
 - Design of bandpass delta-sigma modulators for IQ demodulation in wireless communication systems in OFDM, WiFi, 802.11, Bluetooth, 3G, 4G, etc.
 - University prototyping, fabricating, and packaging of integrated circuits
- Led, as chair, the department in graduate curriculum (MS and PhD), program development, and ABET accreditation visits.
- Worked with established and start-up companies to provide technical expertise and identify employment opportunities for students.
- Held various leadership and service positions including: ECE chair, graduate coordinator, college curriculum committee (chair), promotion and tenure committee, scholarly activities committee, faculty search committee, university level search committees, etc. Collaborate with College of Engineering faculty on joint research projects.
- Taught courses in circuits, analog IC design, digital VLSI design and fabrication, fiber optics, and mixed-signal integrated circuit design to both on- and, via the Internet, off-campus students. Research emphasis in integrated circuit design using nascent technologies.

EDUCATION

- Ph.D. in Electrical Engineering; December 1993; University of Nevada, Reno, GPA 4.0/4.0. Dissertation Title: *Applying power MOSFETs to the design of electronic and electro-optic instrumentation.*
- M.S. and B.S. in Electrical Engineering; May 1986 and May 1988; University of Nevada, Las Vegas. Thesis Title: *Three-dimensional simulation of a MOSFET including the effects of gate oxide charge.*

MEMBERSHIPS IN PROFESSIONAL AND SCHOLARLY ORGANIZATIONS

IEEE (student, 1983; member, 1988; senior member, 1997; Fellow, 2013)
Member of the honor societies Eta Kappa Nu and Tau Beta Pi
Licensed Professional Engineer

HONORS AND AWARDS

- Consolidated Students of the University of Nevada, Las Vegas (CSUN) Faculty Award, 2017
- Tau Beta Pi UNLV Outstanding Professor of the Year in 2013, 2014, 2015 and 2016
- UNLV ECE Department Distinguished Professor of the Year in 2015
- IEEE Fellow for contributions to the design of memory circuits - 2013
- Distinguished Lecturer for the IEEE Solid-State Circuits Society, 2012 - 2015
- IEEE Circuits and Systems (CAS) Education Award - 2011
- Twice elected to the Administrative Committee of the Solid-State Circuits Society, 2011 - 2016
- Frederick Emmons Terman Award from the American Society of Engineering Education - 2007
- President's Research and Scholarship Award, Boise State University - 2005
- Honored Faculty Member - Boise State University Top Ten Scholar/Alumni Association 2003
- Outstanding Department of Electrical Engineering faculty, Boise State 2001
- Recipient of the IEEE Power Electronics Society's Best Paper Award in 2000
- University of Idaho, Department of Electrical Engineering outstanding researcher award, 1998-99
- University of Idaho, College of Engineering Outstanding Young Faculty award, 1996-97

SERVICE

Reviewer for IEEE transactions on solid-state circuits, circuits and devices magazine, education, instrumentation, nanotechnology, VLSI, etc. Reviewer for several American Institute of Physics journals as well (Review of Scientific Instruments, Applied Physics letters, etc.) Board member of the IEEE press (reviewed dozens of books and book proposals). Reviewer for the National Institutes of Health. Technology editor and then Editor-in-Chief for the Solid-State Circuits Magazine.

Led the Department on ABET visits, curriculum and policy development, and new program development including the PhD in electrical and computer engineering. Provided significant University and College service in infrastructure development, Dean searches, VP searches, and growth of academic programs. Provided university/industry interactions including starting the ECE department's advisory board. Held positions as the ECE department Master's graduate coordinator and coordinator for the Sophomore Outcomes Assessment Test (SOAT).

Also currently serves, or has served, on the IEEE Press Editorial Board (1999-2004), as a member of the first Academic Committee of the State Key Laboratory of Analog and Mixed-Signal VLSI at the University of Macau, as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018), on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), as an Advisory Professor to the School of Electronic and Information Engineering at Beijing Jiaotong University, as a Distinguished Lecturer for the SSCS (2012-2015), as the Technical Program Chair for the IEEE 58th 2015 International Midwest Symposium on Circuits and Systems, MWSCAS 2015, as advisor for the student branch of the IEEE at UNLV (2013-2023), and as the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for the *IEEE Solid-State Circuits Magazine*, and IEEE Kirchhoff Award Committee (2020-2023).

ARMED FORCES

From 1981 to 1987 served in the United States Marine Corps (from September of 1982 in the Reserves, Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division), Honorable Discharge. Military Occupational Specialty (MOS) was Machine Gunner (MOS 0331)

TEXTBOOKS AUTHORED

Baker, R. J., "CMOS Circuit Design, Layout and Simulation, Fourth Edition" *Wiley-IEEE Press*, 1234 pages. ISBN 9781119481515 (2019) **Over 50,000 copies of this book in print.** (Third Edition published in 2010, Revised Second Edition published in 2008, and Second Edition Published in 2005)

Baker, R. J., "CMOS Mixed-Signal Circuit Design," *Wiley-IEEE*, 329 pages. ISBN 978-0470290262 (second edition, 2009) and ISBN 9780471227540 (First Edition published in 2002)

Keeth, B., Baker, R. J., Johnson, B., and Lin, F., "DRAM Circuit Design: Fundamental and High-Speed Topics", *Wiley-IEEE*, 2008, 201 pages. ISBN: 9780470184752

Keeth, B. and Baker, R. J., "DRAM Circuit Design: A Tutorial", *Wiley-IEEE*, 2001, 201 pages. ISBN 0780360141

Baker, R. J., Li, H.W., and Boyce, D.E. "CMOS Circuit Design, Layout and Simulation," *Wiley-IEEE*, 1998, 904 pages. ISBN 9780780334168

BOOKS, OTHER (edited, chapters, etc.)

Saxena, V. and Baker, R. J., "Analog and Digital VLSI," chapter in the CRC Handbook on Industrial Electronics, edited by J. D. Irwin and B. D. Wilamowski, *CRC Press*, 2009 second edition.

Baker, R. J., "CMOS Analog Circuit Design," (A self-study course with study guide, videos, and tests.) IEEE Education Activity Department, 2000. ISBN 0-7803-4822-2 (with textbook) and ISBN 0-7803-4823-0 (without textbook)

Baker, R. J., "CMOS Digital Circuit Design," (A self-study course with study guide, videos, and tests.) *IEEE Education Activity Department*, 2000. ISBN 0-7803-4812-5 (with textbook) and ISBN 0-7803-4813-3 (without textbook)

Li, H.W., Baker, R. J., and Thelen, D., "CMOS Amplifier Design," chapter 19 in the CRC VLSI Handbook, edited by Wai-kai Chen, *CRC Press*, 1999 (ISBN 0-8493-8593-8) and the second edition in 2007 (ISBN 978-0-8493-4199-1)

INVITED TALKS AND SEMINARS

Have given over 50 invited talks and seminars at the following locations: AMD (Fort Collins), AMI semiconductor, Arizona State University, Beijing Jiaotong University, Boise State University, Carleton University, Carnegie Mellon, Columbia University, Dublin City University (Ireland), E.G.&G. Energy Measurements, Foveon, the Franklin Institute, Georgia Tech, Gonzaga University, Hong Kong University of Science and Technology, ICSEng Keynote, ICySSS keynote, IEEE Computing and Communication Workshop (CCWC), IEEE Electron Devices Conference (NVMETS), IEEE Workshop on Microelectronics and Electron Devices (WMED), Indian Institute of Science (Bangalore, India), Instituto de Informatica (Brazil), Instituto Tecnológico y de Estudios Superiores de Monterrey (ITESM, Mexico), Iowa State University, Lawrence Livermore National Laboratory, Lehigh University, Lockheed-Martin, Micron Technology, Nascentric, National Semiconductor, Princeton University, Rendition, Saintgits College (Kerala, India), Southern Methodist University, Sun Microsystems, Stanford University, ST Microelectronics (Delhi, India), Temple University, Texas A&M University, Tower Semiconductor (Israel), University of Alabama (Tuscaloosa), University of Arkansas, University of Buenos Aires (Argentina), University of Houston, University of Idaho, University of Illinois (Urbana-Champaign), Université Laval (Québec City, Québec), University of Macau, University of Maryland, Université de Montréal (École Polytechnique de Montréal), Xilinx (Ireland), University of Nevada (Las Vegas), University of Nevada (Reno), University of Toronto, University of Utah, Utah State University, and Yonsei University (Seoul, South Korea).

RESEARCH FUNDING (LAST 5 YEARS AS A PROFESSOR)

Recent funding listed below. In-kind, equipment, and other non-contract/grant funding [e.g., MOSIS support, money for travel for invited talks, etc.] not listed.

- Baker, R. Jacob, (2017-2023) "Tiled Silicon Photomultiplier Array Read-Out Integrated Circuit," NASA, \$29,999 (Phase I), \$225,238 (Phase II), and \$79,697 (Phase IIE)
- Goldman, J., Menezes, J., and Baker, R. J., (2021-2022) "Monitored Compression Therapy: Using Smart Technology to Optimize the Treatment of Lower Extremity Swelling," UNLV Sports Research & Innovation Initiative. Proof of Concept Grant Program, \$50,000
- Baker, R. Jacob, (2019-2021) "Dual-Mode, Extended Near-Infrared, Focal Plane Arrays Fabricated with CMOS Compatible GeSiSn Alloy Materials," DARPA, \$149,998
- Baker, R. Jacob, (2018-2020) "Geiger Mode SiGe Receiver for Long-Range Optical Communications," NASA, \$99,996
- Baker, R. Jacob, (2019) "Improved Quantum Efficiency Photo-Detector," Navy, \$29,999

- Baker, R. Jacob, (2018-2019) "Tiled Silicon Photomultiplier Array Read-Out Integrated Circuit – Phase I," NASA, \$29,999
- Baker, R. Jacob, (2017-2019) "Quantum Cryptography Detector Chip," Defense MicroElectronics Activity (DMEA), \$266,029
- Baker, R. Jacob, (2017-2019) "Advanced Printed Circuit Board Design Methods for Compact Optical Transceiver," U.S. Army/DOD, \$299,605
- Baker, R. Jacob, (2016-2018) "High-Sensitivity Monolithic Silicon APD and ROIC," U.S. Air Force/DOD, \$299,665
- Baker, R. Jacob, (2017-2018) "Transimpedance Amplifier Integrated Circuit Collaboration," Department of Energy, National Security Technologies, LLC, \$100,436
- Baker, R. Jacob, (2017) "Geiger Mode SiGe Receiver for Long-Range Optical Communications," NASA, \$30,000
- Baker, R. Jacob, (2016-2017) "Testing and development of BiCMOS photodetectors and diagnostic instrumentation," Department of Energy, National Security Technologies, LLC, \$181,605
- Baker, R. Jacob, (2016-2017) "Dual-Mode, Extended Near Infrared, Focal Plane Arrays fabricated with a Commercial SiGe BiCMOS Process," DARPA, \$41,892

DOCTORAL STUDENT SUPERVISION

11. Mario Valles Montenegro (underway)
10. Sachin Namboodiri – A Multi-channel MCP-PMT based Readout Integrated Circuit for LiDAR Applications (2020)
9. Wenlan Wu – High-Speed Radhard Mega-Pixel CIS Camera for High-Energy Physics (2019)
8. Kostas Moutafis – A Highly-Sensitive Global-Shutter CMOS Image Sensor with On-Chip Memory for Hundreds of kilo-frames per second Scientific Experiments (2019)
7. Yiyan Li – Portable High Throughput Digital Microfluidics and On-Chip Bacteria Cultures (2016)
6. Yacouba Moumouni – Designing, Building, and Testing a Solar Thermoelectric Generation, STEG, for Energy Delivery to Remote Residential Areas in Developing Regions (2015)
5. Qawi IbnZayd Harvard – Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design (2011)
4. Vishal Saxena – K-Delta-1-Sigma Modulators for Wideband Analog-to-Digital Conversion (2010)
3. Robert Russell Hay – Digitally-Tunable Surface Acoustic Wave Resonator (2009)
2. Xiangli Li (the first Boise State University College of Engineering PhD graduate) – MOSFET Modulated Dual Conversion Gain CMOS Image Sensors (2008)
1. Feng Lin, Research and Design of Low Jitter, Wide Locking-Range Phase-Locked and Delay-Locked Loops (2000)

MASTERS STUDENT SUPERVISION

93. Abraham Lopez (underway)
92. David Santiago (underway)
91. Khulan Tsogt (underway)
90. Jazmin Bolor (underway)
89. Chris Barr (underway)
88. Minsung Cho – Studies of Forward Projection Algorithms and Implementation on PC and FPGA (2023)
87. Armani Alvarez – A Control Integrated Circuit for a Hysteretic Flyback Power Converter (2022)
86. Francisco Mata-carlos – A Wearable Electronic Monitoring Device for Low Pressure Garment Applications and Temperature Analysis for Prevention of Ulceration and Infection (2022)
85. Daniel Senda – Designs and Outcomes of Transcranial Magnetic Stimulation (TMS) and Repetitive Transcranial Magnetic Stimulation (rTMS) Circuits (2021)
84. James Skelly – Monitored Compression Therapy: Using Smart Technology to Optimize the Treatment of Lower Extremity Swelling (2021)
83. Gonzalo Arteaga – Current-mode photon-counting circuit with SiGe BiCMOS input stage (2020)
82. Jason Silic – Design and Fabrication of a 6-bit Current-Mode ADC for Lidar and High-Speed Applications (2020)
81. Brandon Wade (2020)
80. Mario Valles Montenegro – Front-End CMOS Transimpedance Amplifiers on a Silicon Photomultiplier Resistant to Fast Neutron Fluence (2020)
79. Jonathan DeBoy (2018)
78. Dane Gentry – Design, Layout, and Testing of SiGe APDs Fabricated in a BiCMOS Process (2018)

77. James Mellot – Variable Transition Time Inverters in a Digital Delay Line with Analog Storage for Processing Fast Signals and Pulses (2018)
76. Eric Monahan – High Speed Fast Transient Digitizer Design and Simulation (2018)
75. Shada Sharif – Design and Analysis of First and Second Order K-Delta-1-Sigma Modulators in Multiple Fabrication Processes (2018)
74. Vikas Vinayaka – Analysis and Design of Analog Front-End Circuitry for Avalanche Photodiodes (APD) and Silicon Photo-Multipliers (SiPM) in Time-of-Flight Applications (2018)
73. Claire Tsagkari – Design, Fabrication and Testing of a Capacitive Sensor Using Delta-Sigma Modulation (2017)
72. Kevin Buck – Fast Transient Digitizer and PCB Interface (2015)
71. Marzieh Sharbat Maleki (2015)
70. Angsuman Roy – Design, Fabrication and Testing of Monolithic Low-Power Passive Sigma-Delta Analog-to-Digital Converters (2015)
69. Daniel Anderson – Design and Implementation of an Instruction Set Architecture and Instruction Execution Unit for the RZ9 Coprocessor System (2014)
68. Jared Gordon – Design and Fabrication of an Infrared Optical Pyrometer ASIC (2013)
67. Justin Butterfield (2012)
66. Adam Johnson – Methods and Considerations for Testing Resistive Memories (2012)
65. Ben Millemon – CMOS Characterization, Modeling, and Circuit Design in the Presence of Random Local Variation (2012)
64. Justin Wood (2012)
63. Chamunda Ndinawe Chamunda (2011)
62. Gary VanAckern – Design Guide for CMOS Process On-Chip 3D Inductors using Thru-Wafer Vias (2011)
61. Lucien Jan Bissey – High-Voltage Programmable Delta-Sigma Modulation Voltage-Control Circuit (2010)
60. Kaijun Li (2010)
59. Yingting Li (co-supervised with Maria Mitkova) (2010)
58. Lael Matthews (co-supervised with Said Ahmed-Zaid) (2010)
57. Priyanka Mukeshbhai Parikh (2010)
56. Todd Plum (co-supervised with Jeff Jessing) – Design and Fabrication of a Chemicapacitive Sensor for the Detection of Volatile Organic Compounds (2010)
55. Rahul Srikonda (2010)
54. Avani Falgun Trivedi (2010)
53. Kuang Ming Yap – Gain and Offset Error Correction for CMOS Image Sensors using Delta-Sigma Modulation (2010)
52. Mahesh Balasubramanian – Phase Change Memory - Array Development and Sensing Circuits using Delta-Sigma Modulation (2009)
51. Lincoln Bollschweiler (2009)
50. Shantanu Gupta (2009)
49. Qawi Harvard – Wide I_O DRAM Architecture Utilizing Proximity Communication (2009)
48. Avinash Rajagiri (2009)
47. Ramya Ramarapu (2009)
46. Harikrishna Rapole (2009)
45. Aruna Vadla (2009)
44. Hemanth Ande (2008)
43. Curtis Cahoon – Low-Voltage CMOS Temperature Sensor Design using Schottky Diode-Based References (2008)
42. Prashanth Busa (2008)
41. John McCoy III (2008)
40. Dennis Montierth – Using Delta-Sigma-Modulation for Sensing in a CMOS Imager (2008)
39. Rudi Rashwand (2008)
38. Barsha Shrestha (co-supervised with Zhu Han) – Wireless Access in Vehicular Environments using Bit Torrent and Bargaining (2008)
37. Eric Becker – Design of an Integrated Half-Cycle Delay Line Duty Cycle Corrector Delay Locked Loop (2007)

36. Matthew Leslie – Noise-Shaping Sense Amplifier for Cross-Point Arrays (2007)
35. Jose Monje (2007)
34. Sanghyun Park (2007)
33. Vishal Saxena – Indirect Feedback Compensation Techniques for Multi-Stage Operational Amplifiers (2007)
32. Meshack Appikarla (2006)
31. Eric Booth – Wide Range, Low Jitter Delay-Locked Loop Using a Graduated Digital Delay Line and Phase Interpolator (2006)
30. Sucheta Das (2006)
29. Krishna Duvvada – High Speed Digital CMOS Input Buffer Design (2006)
28. Krishnamraju Kurra (2006)
27. Soumya Narasimhan (2006)
26. Roger Porter (2006)
25. David Butler – Low-Voltage Bandgap Reference Design Utilizing Schottky Diodes (2005)
24. Dragos Dimitriu (2005)
23. Surendranath Eruvuru – Sensing Circuit Design for an Ion Mobility Spectrometer (2005)
22. Sandhya Sandireddy (2005)
21. Harish Singidi (2005)
20. Indira Vemula – Delta-Sigma Modulator Used in CMOS Imagers (2005)
19. Bhavana Kollimarla – A 1-Bit Analog-to-Digital Converter Using Delta Sigma Modulation for Sensing in CMOS Imagers (2004)
18. Sandeep Pemmaraju – High Voltage Charge Pump Circuit for an Ion Mobility Spectrometer (2004)
17. Ravindra Puthumbaka – Circuit Design for an Ion Mobility Spectrometer (2004)
16. Brandon Roth – Comparison of Asynchronous vs. Synchronous Design Technologies using a 16-bit Binary Adder (2004)
15. Jennifer Taylor – Reading and Writing Flash Memory Using Delta-Sigma Modulation (2004)
14. Jing Plaisted – Methods for Memory Testing (2003)
13. Murugesh Subramaniam – Flash Memory Sensing Using Averaging (2003)
12. Brian Johnson – Application of an Asynchronous FIFO in a DRAM Data Path (2002)
11. Scott Ward – Electrostatic Discharge (ESD) Protection in CMOS (2002)
10. Tyler Gomm – Design of a Delay-Locked Loop with a DAC-Controlled Analog Delay Line (2001)
9. Gexin Huang (2001)
8. Chris Atkins (2000)
7. Thaddeus Black (2000)
6. Zuxu Qin (2000)
5. Hao Chen (1999)
4. Doug Hackler (co-supervised with Steve Parke) – TMOS: A Novel Design for MOSFET Technology (1999)
3. Song Liu – Design of a CMOS 6-bit Folding and Interpolating Analog-to-Digital Converter (1999)
2. Ben Ba (1997)
1. Brent Keeth – A Novel Architecture for Advanced High Density Dynamic Random Access Memories (1996)

GRANTED US PATENTS

152. Baker, R. J., "Quantizing circuits having improved sensing," **10,658,018**, May 19, 2020.
151. Baker, R. J., "Quantizing circuits having improved sensing," **10,403,339**, September 3, 2019.
150. Baker, R. J., "Digital Filters with Memory," **10,366,744**, July 30, 2019.
149. Baker, R. J., "Quantizing circuits having improved sensing," **10,127,954**, November 13, 2018.
148. Baker, R. J. and Parkinson, W., "NMOS regulated voltage reference," **9,753,481**, September 5, 2017.
147. Baker, R. J., "Digital Filters with Memory," **9,734,894**, August 15, 2017.
146. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **9,697,883**, July 7, 2017
145. Baker, R. J., "Comparators for delta-sigma modulators," **9,641,193**, May 2, 2017.
144. Baker, R. J., "Quantizing circuits having improved sensing," **9,449,664**, September 20, 2016.
143. Baker, R. J., "Error detection for multi-bit memory," **9,336,084**, May 10, 2016.
142. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **9,299,423**, March 29, 2016.

141. Baker, R. J., "Methods for sensing memory elements in semiconductor devices," **9,299,405**, March 29, 2016.
140. Baker, R. J., "Comparators for delta-sigma modulators," **9,135,962**, September 15, 2015.
139. Baker, R. J., "Resistive memory element sensing using averaging," **9,081,042**, July 14, 2015.
138. Baker, R. J., "Digital Filters with Memory," **9,070,469**, June 30, 2015.
137. Baker, R. J., "Reference current sources," **8,879,327**, November 4, 2014.
136. Baker, R. J. and Beigel, K. D., "Multi-resistive integrated circuit memory," **8,878,274**, November 4, 2014.
135. Baker, R. J., "Methods for sensing memory elements in semiconductor devices," **8,854,899**, October 7, 2014.
134. Baker, R. J., "Quantizing circuits with variable parameters," **8,830,105**, September 9, 2014.
133. Baker, R. J., "Integrators for delta-sigma modulators," **8,754,795**, June 17, 2014.
132. Baker, R. J., "Methods of quantizing signals using variable reference signals," **8,717,220**, May 6, 2014.
131. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **8,712,249**, April 29, 2014.
130. Baker, R. J., "Resistive memory element sensing using averaging," **8,711,605**, April 29, 2014.
129. Baker, R. J., "Memory with correlated resistance," **8,681,557**, March 25, 2014.
128. Baker, R. J., "Reference current sources," **8,675,413**, March 18, 2014.
127. Baker, R. J., "Methods for sensing memory elements in semiconductor devices," **8,582,375**, November 12, 2013.
126. Linder, L. F., Renner, D., MacDougall, M., Geske, J., and Baker, R. J., "Dual well read-out integrated circuit (ROIC)," **8,581,168**, November 12, 2013.
125. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **8,516,292**, August 20, 2013.
124. Baker, R. Jacob, "Resistive memory element sensing using averaging," **8,441,834**, May 14, 2013.
123. Qawi, Q. I., Drost, R. J., and Baker, R. Jacob, "Increased DRAM-array throughput using inactive bitlines," **8,395,947**, March 12, 2013.
122. Baker, R. Jacob, "Memory with correlated resistance," **8,289,772**, October 16, 2012.
121. Lin, F. and Baker, R. Jacob, "Phase splitter using digital delay locked loops," **8,218,708**, July 10, 2012.
120. Baker, R. Jacob, "Subtraction circuits and digital-to-analog converters for semiconductor devices," **8,194,477**, June 5, 2012.
119. Baker, R. J., "Digital Filters for Semiconductor Devices," **8,149,646**, April 3, 2012.
118. Baker, R. J., "Error detection for multi-bit memory," **8,117,520**, February 14, 2012.
117. Baker, R. J., "Integrators for delta-sigma modulators," **8,102,295**, January 24, 2012.
116. Baker, R. J., "Devices including analog-to-digital converters for internal data storage locations," **8,098,180**, January 17, 2012.
115. Baker, R. J. and Beigel, K. D., "Multi-resistive integrated circuit memory," **8,093,643**, January 10, 2012.
114. Baker, R. J., "Quantizing circuits with variable parameters," **8,089,387**, January 3, 2012.
113. Baker, R. J., "Reference current sources," **8,068,367**, November 29, 2011.
112. Baker, R. J., "Methods of quantizing signals using variable reference signals," **8,068,046**, November 29, 2011.
111. Baker, R. J., "Systems and devices including memory with built-in self-test and methods of making using the same," **8,042,012**, October 18, 2011.
110. Baker, R. J., "Memory with correlated resistance," **7,969,783**, June 28, 2011.
109. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **7,941,056**, May 10, 2011.
108. Baker, R. J., "K-delta-1-sigma modulator," **7,916,054**, March 29, 2011.
107. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **7,877,623**, January 25, 2011.
106. Lin, F. and Baker, R. J., "Phase splitter using digital delay locked loops," **7,873,131**, January 18, 2011.
105. Hush, G. and Baker, R. J., "Complementary bit PCRAM sense amplifier and method of operation," **7,869,249**, January 11, 2011.
104. Baker, R. J., "Subtraction circuits and digital-to-analog converters for semiconductor devices," **7,839,703**, November 23, 2010.
103. Baker, R. J., "Digital Filters with Memory" **7,830,729**, November 9, 2010.
102. Baker, R. J., "Systems and devices including memory with built-in self test and methods of making using the same," **7,818,638**, October 19, 2010.
101. Baker, R. J., "Integrators for delta-sigma modulators," **7,817,073**, October 19, 2010.

100. Baker, R. J., "Digital filters for semiconductor devices," **7,768,868**, August 3, 2010.
99. Baker, R. J., "Quantizing circuits with variable reference signals," **7,733,262**, June 8, 2010.
98. Baker, R. J., "Quantizing circuits for semiconductor devices," **7,667,632**, February 23, 2010.
97. Baker, R. J., and Beigel, K. D., "Multi-resistive integrated circuit memory," **7,642,591**, January 5, 2010.
96. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **7,616,474**, November 10, 2009.
95. Baker, R. J., "Resistive memory element sensing using averaging," **7,577,044**, Aug. 18, 2009.
94. Baker, R. J., "Quantizing circuits with variable parameters," **7,538,702**, May 26, 2009.
93. Baker, R. J., "Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors," **7,528,877**, May 5, 2009.
92. Baker, R. J., "Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors," **7,515,188**, April 7, 2009.
91. Taylor, J. and Baker, R. J., "Method and apparatus for sensing flash memory using delta-sigma modulation," **7,495,964**, February 24, 2009.
90. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **7,489,575**, February 10, 2009.
89. Baker, R. J., "Per column one-bit ADC for image sensors," **7,456,885**, November 25, 2008.
88. Staples, T. and Baker, R. J., "Input buffer design using common-mode feedback," **7,449,953**, November 11, 2008.
87. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **7,421,607**, September 2, 2008.
86. Baker, R. J., "Methods for resistive memory element sensing using averaging," **7,372,717**, May 13, 2008.
85. Taylor, J. and Baker, R. J., "Method and apparatus for sensing flash memory using delta-sigma modulation," **7,366,021**, April 29, 2008.
84. Hush, G. and Baker, R. J., "Method of operating a complementary bit resistance memory sensor and method of operation," **7,366,003**, April 29, 2008.
83. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **7,330,390**, February 12, 2008.
82. Baker, R. J., "Input and output buffers having symmetrical operating characteristics and immunity from voltage variations," **7,319,620**, January 15, 2008.
81. Staples, T. and Baker, R. J., "Method and apparatus providing input buffer design using common-mode feedback," **7,310,018**, December 18, 2007.
80. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **7,286,428**, October 23, 2007.
79. Baker, R. J., and Cowles, T. B., "Method and apparatus for reducing duty cycle distortion of an output signal," **7,271,635**, September 18, 2007.
78. Baker, R. J., and Cowles, T. B., "Method and apparatus for reducing duty cycle distortion of an output signal," **7,268,603**, September 11, 2007.
77. Hush, G., Baker, R. J., and Moore, J., "Skewed sense AMP for variable resistance memory sensing," **7,251,177**, July 31, 2007.
76. Hush, G. and Baker, R. J., "Method of operating a complementary bit resistance memory sensor," **7,242,603**, July 10, 2007.
75. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **7,237,136**, June 26, 2007.
74. Moore, J. and Baker, R. J., "Rewrite prevention in a variable resistance memory," **7,224,632**, May 29, 2007.
73. Baker, R. J., "Integrated charge sensing scheme for resistive memories," **7,151,698**, December 19, 2006.
72. Baker, R. J., "Adjusting the frequency of an oscillator for use in a resistive sense amp," **7,151,689**, December 19, 2006.
71. Baker, R. J., "Resistive memory element sensing using averaging," **7,133,307**, Nov. 7, 2006.
70. Lin, F. and Baker, R. J., "Phase detector for all-digital phase locked and delay locked loops," **7,123,525**, October 17, 2006.
69. Baker, R. J., and Beigel, K. D., "Integrated circuit memory with offset capacitor," **7,109,545**, September 19, 2006.
68. Baker, R. J., "Input and output buffers having symmetrical operating characteristics and immunity from voltage variations," **7,102,932**, September 5, 2006.
67. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **7,095,667**, August 22, 2006.

66. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **7,082,045**, July 25, 2006.
65. Baker, R. J., "System and method for sensing data stored in a resistive memory element using one bit of a digital count," **7,009,901**, March 7, 2006.
64. Hush, G. and Baker, R. J., "Complementary bit resistance memory sensor and method of operation," **7,002,833**, February 21, 2006.
63. Lin, F. and Baker, R. J., "Phase detector for all-digital phase locked and delay locked loops," **6,987,701**, January 17, 2006.
62. Baker, R. J., "Adjusting the frequency of an oscillator for use in a resistive sense amp," **6,985,375**, January 10, 2006.
61. Baker, R. J., "Method for reducing power consumption when sensing a resistive memory," **6,954,392**, October 11, 2005.
60. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **6,954,391**, October 11, 2005.
59. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **6,954,390**, October 11, 2005.
58. Lin, F. and Baker, R. J., "Phase splitter using digital delay locked loops," **6,950,487**, September 27, 2005.
57. Baker, R. J., "Method and apparatus for measuring current as in sensing a memory cell," **6,930,942**, August 16, 2005.
56. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **6,917,534**, July 12, 2005.
55. Baker, R. J., "Dual loop sensing scheme for resistive memory elements," **6,914,838**, July 5, 2005.
54. Baker, R. J., "High speed low power input buffer," **6,914,454**, July 5, 2005.
53. Baker, R. J., and Beigel, K. D., "Method for stabilizing or offsetting voltage in an integrated circuit," **6,913,966**, July 5, 2005.
52. Moore, J. and Baker, R. J., "PCRAM rewrite prevention," **6,909,656**, June 21, 2005.
51. Baker, R. J., "Integrated charge sensing scheme for resistive memories," **6,901,020**, May 31, 2005.
50. Hush, G., Baker, R. J., and Moore, J., "Skewed sense AMP for variable resistance memory sensing," **6,888,771**, May 3, 2005.
49. Baker, R. J., "Method for reducing power consumption when sensing a resistive memory," **6,885,580**, April 26, 2005.
48. Moore, J. and Baker, R. J., "PCRAM rewrite prevention," **6,882,578**, April 19, 2005.
47. Baker, R. J., "Integrated charge sensing scheme for resistive memories," **6,870,784**, March 22, 2005.
46. Baker, R. J., "Sensing method and apparatus for a resistive memory device," **6,859,383**, February 22, 2005.
45. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **6,856,564**, February 15, 2005.
44. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **6,856,532**, February 15, 2005.
43. Baker, R. J., "Dual loop sensing scheme for resistive memory elements," **6,829,188**, Dec. 7, 2004.
42. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **6,826,102**, Nov. 30, 2004.
41. Baker, R. J., "Resistive memory element sensing using averaging," **6,822,892**, Nov. 23, 2004.
40. Baker, R. J., "System and method for sensing data stored in a resistive memory element using one bit of a digital count," **6,813,208**, Nov. 2, 2004.
39. Baker, R. J., "Wordline driven method for sensing data in a resistive memory array," **6,809,981**, Oct. 26, 2004.
38. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **6,798,705**, Sept. 28, 2004.
37. Baker, R. J., "Methods and apparatus for measuring current as in sensing a memory cell," **6,795,359**, Sept. 21, 2004.
36. Hush, G. and Baker, R. J., "Complementary bit PCRAM sense amplifier and method of operation," **6,791,859**, Sept. 14, 2004.
35. Baker, R. J., "Method and apparatus for sensing resistance values of memory cells," **6,785,156**, August 31, 2004.
34. Lin, F. and Baker, R. J., "Phase detector for all-digital phase locked and delay locked loops," **6,779,126**, August 17, 2004.
33. Baker, R. J., and Lin, F. "Digital dual-loop DLL design using coarse and fine loops," **6,774,690**, August 10, 2004.
32. Hush, G., Baker, R. J., and Voshell, T., "Producing walking one pattern in shift register," **6,771,249**, August 3, 2004.
31. Baker, R. J., "Sensing method and apparatus for resistance memory device," **6,741,490**, May 25, 2004.

30. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **6,704,881**, March 9, 2004.
29. Baker, R. J., "Method and system for writing data in an MRAM memory device," **6,687,179**, February 3, 2004.
28. Baker, R. J., "High speed digital signal buffer and method," **6,683,475**, January 27, 2004.
27. Baker, R. J., "High speed low power input buffer," **6,600,343**, July 29, 2003.
26. Baker, R. J., "Offset compensated sensing for magnetic random access memory," **6,597,600**, July 22, 2003.
25. Baker, R. J., "Sensing method and apparatus for resistive memory device," **6,577,525**, June 10, 2003.
24. Baker, R. J., "Method and apparatus for sensing resistance values of memory cells," **6,567,297**, May 20, 2003.
23. Baker, R. J., "High-speed digital signal buffer and method," **6,538,473**, March 25, 2003.
22. Baker, R. J. and Beigel, K. D., "Electronic device with interleaved portions for use in integrated circuits," **6,509,245**, January 21, 2003.
21. Baker, R. J., "Resistive memory element sensing using averaging," **6,504,750**, January 7, 2003.
20. Baker, R. J., "High-speed digital signal buffer and method," **6,483,347**, November 19, 2002.
19. Baker, R. J., and Lin, F., "Digital dual-loop DLL design using coarse and fine loops," **6,445,231**, September 3, 2002.
18. Baker, R. J., "Method and apparatus for receiving synchronous data," **6,424,684**, July 23, 2002.
17. Baker, R. J. and Beigel, K. D., "Comb-shaped capacitor for use in integrated circuits," **6,410,955**, June 25, 2002.
16. Baker, R. J., "High-speed, low-power input buffer," **6,407,588**, June 18, 2002.
15. Miller, J., Schoenfeld, A., Ma, M., and Baker, R. J., "Method and apparatus for improving the performance of digital delay locked loop circuits," **6,316,976**, Nov. 13, 2001.
14. Keeth, B. and Baker, R. J., "Low skew differential receiver with disable feature," **6,256,234**, July 3, 2001.
13. Keeth, B. and Baker, R. J., "Low skew differential receiver with disable feature," **6,104,209**, August 15, 2000.
12. Miller, J., Schoenfeld, A., Ma, M., and Baker, R. J., "Method and apparatus for improving the performance of digital delay locked loop circuits," **6,069,506**, May 30, 2000.
11. Keeth, B. and Baker, R. J., "Low skew differential receiver with disable feature," **6,026,051**, February 15, 2000.
10. Baker, R. J., and Manning, T. A., "Method and apparatus for adaptively adjusting the timing of a clock signal used to latch digital signals, and memory device using same," **6,026,050**, February 15, 2000.
9. Baker, R. J., and Manning, T. A., "Method and apparatus for adaptively adjusting the timing of a clock signal used to latch digital signals, and memory device using same," **5,953,284**, September 14, 1999.
8. Baker, R. J., "Fully-differential amplifier," **5,953,276**, September 14, 1999.
7. Hush, G., Baker, R. J., and Voshell, T., "Timing Control for a Matrixed Scanned Array," **5,909,201**, June 1, 1999.
6. Hush, G. and Baker, R. J., "Field emission display having pulsed capacitance current control," **5,894,293**, April 13, 1999.
5. Baker, R. J., "Adaptively biased voltage regulator and operating method," **5,874,830**, February 23, 1999.
4. Hush, G. Baker, R. J., and Voshell, T., "Serial to Parallel Conversion with a Phase-Locked Loop," **5,818,365**, October 1, 1998.
3. Hush, G., Baker, R. J., and Voshell, T., "Timing Control for a Matrixed Scanned Array," **5,638,085**, June 10, 1997.
2. Wilson, A. J., Baker, R. J., and Schoenfeld, A., "Waveshaping circuit generating two rising slopes for a sense amplifier pulldown device," **5,614,856**, March 25, 1997.
1. Hush, G., Baker, R. J., and Voshell, T., "Serial to Parallel Conversion with a PLL," **5,598,156**, January 28, 1997.

INVITED TALKS (PARTIAL LISTING)

- Harvard, Q. I. and Baker, R. J., "Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design," a presentation covering semiconductor packaging, DRAM architectures, and I/O circuits. The goal of this work is to investigate replacing the currently used dual in-line memory modules (DIMMs) with a smaller and a lower power memory module, a "Nano-Module."
- Baker, R. J., and Campbell, K. A., "Reconfigurable Analog Electronics using the Memristor."
- Baker, R. J., and Saxena, V., "A K-Delta 1-Sigma Modulator for Wideband Analog-to-Digital Conversion."
- Li, K., Saxena, V., and Baker, R. J., "The Baker ADC: An Overview,"
- Saxena, V., and Baker, R. J., "High-Speed Op-Amp Design: Compensation and Topologies for Two and Three Stage Designs,"
- Baker, R. J., "Circuit Design for MLC Flash: Towards a Semiconductor Replacement for the Hard Disk Drive."

- Baker, R. J., Terman Award Acceptance Speech, given at the Frontiers in Education Conference (FIE 2007), Milwaukee, WI, October 11, 2007.
- Baker, R. J., "The One-Transistor, One-Capacitor (1T1C) Dynamic Random Access Memory (DRAM), and its Impact on Society," presented at the Franklin Institute, in the symposium honoring Dr. Robert H. Dennard and his receipt of the 2007 Benjamin Franklin Medal in Electrical Engineering, April 25, 2007.
- Baker, R. J. and Saxena, V., "Design of Bandpass Delta-Sigma Modulators: Avoiding Common Mistakes."
- Baker, R. J., "Sensing Circuits for Resistive Memory."
- Hadrick, M. and Baker, R. J., "Sensing in CMOS Imagers using Delta-Sigma Modulation."
- Baker, R. J., "Design of High-Speed CMOS Op-Amps for Signal Processing," IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED), April, 2005
- Baker, R. J., "Delta-Sigma Modulation for Sensing," IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED), April, 2004
- Rivera, B. and Baker, R. J., "Design and Layout of Schottky Diodes in a Standard CMOS Process," MURI Review, November, 2001.

REFEREED JOURNAL PAPERS

26. Lopez, A., Strong, H. N., McGlothen, K. I., Hines, D. J., and Baker, R. J., "A compact avalanche-transistor based pulse generator for transcranial infrared light stimulation (TILS) experiments," *Instruments*, 2022, 6, 20.
25. Senda, D., Strong, H., Hines, D., Hines, R., and Baker, R. J., "A Compact 1200V, 700A, IGBT-Based Pulse Generator for Repetitive Transcranial Magnetic Stimulation In Vivo Laboratory Experiments," *Review of Scientific Instruments*, Vol. 92, Issue 8, August 30, 2021.
24. Wu, W., Baker, R. J., Bikkina, P., Long, Y., Levy, A., and Mikkola, E., "Design and Analysis of a Feedback Time Difference Amplifier with Linear and Programmable Gain," *Analog Integrated Circuits and Signal Processing, Springer*, 16 October, 2017.
23. Moumouni, Y. and Baker, R. J., "Modeling, Simulation, and Implementation of a Solar Thermoelectric Energy Harvesting System," *Journal of Energy and Power Engineering*, vol. 10, pp. 296-312, 2016.
22. Li, Y., Baker, R. J., and Raad, D., "Improving the Performance of Electrowetting on Dielectric Microfluidics Using Piezoelectric Top Plate Control," *Sensors and Actuators B: Chemical*, vol. 229, pp. 63-74, 2016.
21. Li, Y., Li, H., and Baker, R. J., "A Low-Cost and High-Resolution Droplet Position Detector for an Intelligent Electrowetting on Dielectric Device," *Journal of Laboratory Automation*, Vol. 20, No. 6, pp. 663-669, 2015.
20. Moumouni, Y., Ahmad, S., and Baker, R. J., "A System Dynamics Model for Energy Planning in Niger," *International Journal of Power and Energy Engineering*, Vol. 3, No. 6, pp. 308-322, 2014.
19. Estrada, D., Ogas, M. L., Southwick III, R. G., Price, P. M., Baker, R. J., and Knowlton, W. B., *Impact of Single pMOSFET Dielectric Degradation on NAND Circuit Performance*, Microelectronics Reliability, Vol. 48, No. 3, pp 354-363, 2008.
18. Leslie, M. B., and Baker, R. J., "Noise-Shaping Sense Amplifier for MRAM Cross-Point Arrays," *IEEE Journal of Solid-State Circuits*, Vol. 41, No. 3, pp. 699-704, 2006.
17. Hess, H. L., and Baker, R. J., "Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOS Devices," *IEEE Transactions on Power Electronics*, Vol. 15, No. 5, pp. 923-930, 2000.
16. Lin, F., Miller, J., Schoenfeld, A., Ma, M., and Baker, R. J., "A Register-Controlled Symmetrical DLL for Double-Data-Rate DRAM," *IEEE Journal of Solid-State Circuits*, Vol. 34, No. 4, pp. 565-568, 1999.
15. Bruce, J. D., Li, H. W., Dallabetta, M. J., and Baker, R. J., "Analog layout using ALAS!" *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 2, pp. 271-274, 1996.
14. Li, H. W., Dallabetta, M. J., and Baker, R. J., "An interactive impulse response extraction system," *Review of Scientific Instruments* 66(10), 5092-5095, 1995.
13. Ward, S. T., Baker, R. J., and Li, H. W., "A microchannel plate image intensifier gating circuit capable of pulse widths from 30 ns to 10 us," *Measurement Science and Technology*, Vol. 6, No. 11, pp. 1631-1633, 1995.
12. Keith, B., Baker, R. J., and Li, H. W., "CMOS transistor VCO with adjustable operating and center frequencies," *Electronics Letters*, 31(17), 1397-98, 1995.
11. Baker, R. J., "Time domain operation of the TRAPATT diode for picosecond-kilovolt pulse generation," *Review of Scientific Instruments*, 65(10), 3286-88, 1994.

10. Baker, R. J. and Ward, S. T., "Designing nanosecond high voltage pulse generators using power MOSFETs," *Electronics Letters*, 30(20), 1634-35, 1994.
9. Baker, R. J. and Johnson, B. P., "Sweep circuit design for a picosecond streak camera," *Measurement Science and Technology*, 5(4). 1994.
8. Baker R. J., Hodder, D. J., Johnson, B. P., Subedi, P. C., and Williams, D. C., "Generation of kilovolt-subnanosecond pulses using a nonlinear transmission line" *Measurement Science and Technology*, 4(8), 893-95, 1993.
7. Baker R. J., and Johnson, B. P., "Series operation of power MOSFETs for high speed, high voltage switching applications," *Review of Scientific Instruments* 65(6), 1993.
6. Baker R. J., and Johnson, B. P., "Applying the Marx bank circuit configuration to power MOSFETs," *Electronics Letters* 29(1), 56-57. 1993.
5. Baker R. J., and Johnson, B. P., "Stacking power MOSFETs for use in high speed instrumentation," *Review of Scientific Instruments*, 63(12), 5799-5801, 1992.
4. Baker R. J., and Johnson, B. P., "A 500 Volt nanosecond pulse generator using cascode connected power MOSFETs," *Measurement Science and Technology*, 3(8), 775-77, 1992.
3. Baker R. J., Perryman, G. T., and Watts, P. W., "A fiber-optically triggered avalanche transistor," *IEEE Transactions on Instrumentation and Measurement*, 40(3), 649-52, 1991.
2. Baker R. J., "High voltage pulse generation using current mode second breakdown in a bipolar junction transistor," *Review of Scientific Instruments*, 62(4), 1031-1036, 1991.
1. Baker R. J., and Pocha, M. D. "Nanosecond switching using power MOSFETs," *Review of Scientific Instruments* 61(8), 2211-2213, 1990.

REFERRED CONFERENCE PAPERS AND MAGAZINE ARTICLES

85. Strong, H., Senda, D., Baker, R. J., and Hines, D., "Focal Stimulation of Movement Related Cortical Potentials in Mice using a Novel TMS Circuit Design," *Brain Stimulation*, Vol. 14, Issue 6, November, 2021.
84. Arteaga, G., Namboodiri, S. P., Roy, A., and Baker, R. J., "Current Comparator with SiGe BiCMOS Input Stage for Photon-Counting LiDAR Applications," *IEEE 64th International Midwest Symposium on Circuits and Systems*, August 9-11, pp. 420-423, 2021.
83. Namboodiri, S. P. and Baker, R. J., "Incorporation of Chopping in Continuous Time K-Delta-1-Sigma Modulator," *IEEE 19th IEEE Interregional NEWCAS Conference*, June 13-16, 2021.
82. Namboodiri, S. P., Arteaga, G., Skelly, J., Mata-carlos, F., Roy, A., and Baker, R. J., "A Current-Mode Photon Counting Circuit for Long-Range LiDAR Applications," *IEEE 63rd International Midwest Symposium on Circuits and Systems*, August 9-12, pp. 146-149, 2020.
81. Vinayaka, V., Namboodiri, S. P., Roy, A., and Baker, R. J., "Segmented Digital SiPM," *IEEE 62nd International Midwest Symposium on Circuits and Systems*, August 4-7, pp. 1118-1121, 2019.
80. Mellott, J. K., Monahan, E., Vinayaka, V., Namboodiri, S. P., Roy, A., and Baker, R. J., "Variable Fast Transient Digitizer," *IEEE 62nd International Midwest Symposium on Circuits and Systems*, August 4-7, pp. 125-128, 2019.
79. Vinayaka, V., Namboodiri, S. P., Abdalla, Kerstetter, B., Mata-Carlos, F., Senda, D., Skelly, J., Roy, A., and Baker, R. J., "Monolithic 8x8 SiPM with 4-bit Current-Mode Flash ADC with Tunable Dynamic Range," *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 57-62, Tysons Corner, VA, May 9-11, 2019.
78. Woodson, M., Estrella, S., Hay, K., Roy, A., Sun, K., Morgan, J., Beling, A., Baker, R. J., Renner, D., and Mashanovitch, M., "Photodetection at or below 1 micron wavelengths," *Proc. SPIE 10912, Physics and Simulation of Optoelectronic Devices XXVII*, 1091210, March 8, 2019.
77. Buck, K. and Baker, R. J., "Fast Transient Digitizer Chip for Capturing Single-Shot Events," *Proceedings of 12th IEEE Dallas Circuits and Systems Conference*, October 9-10, 2016.
76. Wu, W., Baker, R. J., Kumar, P., Garcia, F., and Mikkola, E., "A Linear High Gain Time Difference Amplifier Using Feedback Gain Control," *Proceedings of 12th IEEE Dallas Circuits and Systems Conference*, October 9-10, 2016.
75. Moumouni, Y. and Baker, R. J., "Analysis of a Residential 5kW Grid-tied Photovoltaic System," *Proceedings of the 2016 Clemson University Power Systems Conference*, March 8-11, 2016.
74. Moumouni, Y. and Baker, R. J., "LTspice Model of a Solar Thermoelectric Generation System," *Proceedings of the 2016 Clemson University Power Systems Conference*, March 8-11, 2016.

73. Li, Y. and Baker, R. J., "Computer Vision Assisted Measurement of the Displacements of a Bimorph Piezoelectric Cantilever Beam," *Proceedings of the IEEE Biomedical Circuits and Systems (BioCAS 2015) Conference*, October 22-24, 2015.
72. Li, Y. and Baker, R. J., "A Highly Efficient and Reliable Electrowetting on Dielectric Device for Point-of-Care Diagnostics," *Proceedings of 11th IEEE Dallas Circuits and Systems Conference*, October 12-13, 2015.
71. Roy, A. and Baker, R. J., "A Low-Power Switched-Capacitor Passive Sigma-Delta Modulator," *Proceedings of 11th IEEE Dallas Circuits and Systems Conference*, October 12-13, 2015.
70. Li, Y. and Baker, R. J., "Precise EWOD Top Plate Positioning Using Inverse Preisach Model Based Hysteresis Compensation," *Proceedings of 11th IEEE Dallas Circuits and Systems Conference*, October 12-13, 2015.
69. Moumouni, Y. and Baker, R. J., "Buffer Sizing of Concentrated Photovoltaic Batteries: An Economic Analysis," *IEEE 58th International Midwest Symposium on Circuits and Systems*, pp. 704-707, August 2-5, 2015.
68. Moumouni, Y. and Baker, R. J., "Application of Used Electric Vehicle Batteries to Buffer Photovoltaic Output Transients," *IEEE 58th International Midwest Symposium on Circuits and Systems*, pp. 700-703, August 2-5, 2015.
67. Roy, A., Meza, M., Yurgelon, J., and Baker, R. J., "An FPGA Based Passive K-Delta-1-Sigma Modulator," *IEEE 58th Midwest Symposium on Circuits and Systems*, pp. 121-124, August 2-5, 2015.
66. Moumouni, Y. and Baker, R. J., "Concise Thermal to Electrical Parameters Extraction of Thermoelectric Generator for Spice Modeling," *IEEE 58th International Midwest Symposium on Circuits and Systems*, pp. 596-599, August 2-5, 2015.
65. Moumouni, Y. and Baker, R. J., "Improved SPICE Modeling and Analysis of a Thermoelectric Module," *IEEE 58th International Midwest Symposium on Circuits and Systems*, pp. 600-603, August 2-5, 2015.
64. Li, Y., Li, H., and Baker, R. J., "Volume and Concentration Identification by Using an Electrowetting on Dielectric Device," *Proceedings of 10th IEEE Dallas Circuits and Systems Conference*, October 12-13, 2014.
63. Li, Y., Chen, R., and Baker, R. J., "A Fast Fabricating Electro-wetting Platform to Implement Large Droplet Manipulation," *Proceedings of the IEEE 57th International Midwest Symposium on Circuits and Systems*, pp. 326-329, August 3-6, 2014.
62. Roy, A. and Baker, R. J., "A Passive 2nd-Order Sigma-Delta Modulator for Low-Power Analog-to-Digital Conversion," *Proceedings of the IEEE 57th International Midwest Symposium on Circuits and Systems*, pp. 595-598, August 3-6, 2014.
61. Baker, R. J., "Massive Open Online Courses for Educating Circuit Designers: What Works and What Doesn't," *IEEE Solid-State Circuits Magazine*, Vol. 6, No. 2, pp. 63-65, 2014.
60. Montierth, D., Strand, T., Leatham, J., Linder, L., and Baker, R. J., "Performance and Characteristics of Silicon Avalanche Photodetectors in the C5 Process," *IEEE 55th International Midwest Symposium on Circuits and Systems*, August 5-8, 2012.
59. VanAckern, G., Baker, R. J., Moll, A. J., and Saxena, V., "On-Chip 3D Inductors using Thru-Wafer Vias," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, April 20, 2012.
58. Yap, K. and Baker, R. J., "Two Techniques to Reduce Gain and Offset Errors in CMOS Image Sensors using Delta-Sigma Modulation," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, April 20, 2012.
57. Labaziewicz, A. and Baker, R. J., "A 2 GHz Effective Sampling Frequency K-Delta-1-Sigma Analog-to-Digital Converter," *Proceedings of the IEEE 54th International Midwest Symposium on Circuits and Systems*, August 7-10, 2011.
56. Saxena, V., Balagopal, S., and Baker, R. J., "Systematic Design of Three-Stage Op-amps using Split Length Compensation," *Proceedings of the IEEE 54th International Midwest Symposium on Circuits and Systems*, August 7-10, 2011.
55. Harvard, Q. and Baker, R. J., "A Scalable I/O Architecture for Wide I/O DRAM," *Proceedings of the IEEE 54th International Midwest Symposium on Circuits and Systems*, August 7-10, 2011.
54. Wald, S., Baker, R. J., Mitkova, M., and Rafla, N., "A Non-Volatile Memory Array Based on Nano-Ionic Conductive Bridge Measurements," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 43-46, April 22, 2011.

53. Saxena, V. and Baker, R. J., "Synthesis of Higher-Order K-Delta-1-Sigma Modulators for Wideband ADCs," *Proceedings of the IEEE 53rd International Midwest Symposium on Circuits and Systems*, August 1-4, 2010.
52. Saxena, V. and Baker, R. J., "Indirect Compensation Techniques for Three-Stage Fully-Differential Op-Amps," (invited) *Proceedings of the IEEE 53rd International Midwest Symposium on Circuits and Systems*, August 1-4, 2010.
51. Harvard, Q., Baker, R. J., and Drost, R., "Main Memory with Proximity Communication: A Wide I/O DRAM Architecture," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 40-43, April 16, 2010.
50. Yap, K. M. and Baker, R. J., "Gain Error Correction for CMOS Image Sensor using Delta-Sigma Modulation," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 52-55, April 16, 2010.
49. Gagliano, C. and Baker, R. J., "A Compact Delay-Locked Loop for Multi-Phase Non-Overlapping Clock Generation," *Proceedings (poster) of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, April 16, 2010.
48. Montierth, D., Yap, K. M., and Baker, R. J., "CMOS Image Sensor using Delta-Sigma Modulation," *4th Annual Austin Conference on Integrated Circuits & Systems*, Oct. 26-27, 2009.
47. Saxena, V. and Baker, R. J., "Synthesis of Higher-Order K-Delta-1-Sigma Modulators for Wideband Analog to Digital Conversion," *4th Annual Austin Conference on Integrated Circuits & Systems*, Oct. 26-27, 2009.
46. Li, K., Saxena, V., Zheng, G., and Baker, R. J., "Full Feed-Forward K-Delta-1-Sigma Modulator," *4th Annual Austin Conference on Integrated Circuits & Systems*, Oct. 26-27, 2009.
45. Bollschweiler, L., English, A., Baker, R. J., Kuang, W., Chang, Z.-C., Shih, M.-H., Knowlton, W.B., Hughes, W.L., Lee, J., Yurke, B., Cockerham, N. S., and Tyree, V. C., "Chip-Scale Nanophotonic Chemical and Biological Sensors using CMOS Process," *Proceedings of the IEEE 52nd Midwest Symposium on Circuits and Systems*, pp. 413-416, August 2-5, 2009.
44. Saxena, V., Li, K., Zheng, G., and Baker, R. J., "A K-Delta 1-Sigma Modulator for Wideband Analog to Digital Conversion," *Proceedings of the IEEE 52nd International Midwest Symposium on Circuits and Systems*, pp. 411-415, August 2-5, 2009.
43. Saxena, V. and Baker, R. J., "Indirect Compensation Techniques for Three-Stage CMOS Op-amps," *Proceedings of the IEEE 52nd International Midwest Symposium on Circuits and Systems*, pp. 9-12, August 2-5, 2009.
42. Regner, J., Balasubramanian, M., Cook, B., Li, Y., Kassayebetre, H., Sharma, A., Baker, R. J., and Campbell, K. A., "Integration of IC Industry Feature Sizes with University Back-End-of-Line Post Processing: Example Using a Phase-Change Memory Test Chip," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 28-31, April, 2009.
41. Gupta, S. Saxena, V., Campbell, K. A., and Baker, R. J., "W-2W Current Steering DAC for Programming Phase Change Memory," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 59-62, April, 2009.
40. Rapole, H., Rajagiri, A., Balasubramanian, M., Campbell, K. A., and Baker, R. J., "Resistive Memory Sensing Using Delta-Sigma Modulation," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 63-66, April, 2009.
39. Kassayebetre, H., Regner, J., Rajagiri, A., Sharma, A., Hay, R. R., Baker, R. J., and Campbell, K.A., "Surface Acoustic Wave Device Fabrication using Zinc Oxide and Chalcogenide Thin Films," poster presentation at the *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, April, 2009.
38. Ande, H. K., Busa, P., Balasubramanian, M., Campbell, K. A., and Baker, R. J., "A New Approach to the Design, Fabrication, and Testing of Chalcogenide-Based Multi-State Phase-Change Nonvolatile Memory," *Proceedings of the IEEE 51st International Midwest Symposium on Circuits and Systems*, pp. 570-573, August 10-13, 2008.
36. Saxena, V., and Baker, R. J., "Compensation of CMOS Op-Amps using Split-Length Transistors," *Proceedings of the IEEE 51st Midwest Symposium on Circuits and Systems*, pp. 109-112, August 10-13, 2008.
36. Saxena, V., and Baker, R. J., "Indirect Compensation Technique for Low-Voltage Op-Amps," *Proceedings of the 3rd Annual Austin Conference on Integrated Systems and Circuits (ACISC)*, May 7-9, 2008.

35. Cahoon, C., and Baker, R. J., "Low-Voltage CMOS Temperature Sensor Design using Schottky Diode-Based References," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 16-19, April, 2008.
34. Knowlton, W. B., Araujo, D., Price, P.M., Brotherton, J., Coonse, K., Hendricks, K., Southwick III, R. G., Henderson, J., Oxford, J., Moll, A., Kuang, W., and Baker, R. J., "Progress Towards a Biomolecular Nanowire Sensor Array for Biomedical Applications," invited talk presented at the 6th Annual INBRE/COBRE Research Conference, Moscow, ID, August 6, 2007
33. Knowlton, W. B., Araujo, D., Price, P.M., Brotherton, J., Coonse, K., Southwick III, R.G., Oxford, J., Moll, A., Baker, R. J., and Kuang, W., "Development of Biomolecular Nanostructure Sensor Arrays," presented at the Sensors and Sensor Technology session for the program of the 88th annual meeting of the AAAS, Pacific Division, June 2007, Boise, ID
32. Knowlton, W. B., Kuang, W., Araujo D., Price, P. M., Brotherton, J., Coonse, K. Bollschweiler, L., Southwick, R., Oxford, J. Moll, A., and Baker, R. J., "Nanofabrication of 3D Sensor Arrays for Detection," Advanced Fuel Cycle Workshop, May 8-9, 2007, Boise, ID
31. Loo, S. M., Cole, J., Youngberg, R., Baker, R. J., Gribb, M. M., "Field-programmable gate array in a miniature ion mobility spectrometer sensor system," *Proceedings of the 2006 International Conference on Embedded Systems & Applications*, June 26-29, 2006, Las Vegas, NV.
30. Saxena, V., and Baker, R. J., "Indirect Feedback Compensation of CMOS Op-Amps," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 3-4, April, 2006.
29. Duvvada, K., Saxena, V., and Baker, R. J., High Speed Digital Input Buffer Circuits, *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 11-12, April, 2006.
28. Saxena, V., Plum, T. J., Jessing, J. R., and Baker, R. J., "Design and Fabrication of a MEMS Capacitive Chemical Sensor System," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 17-18, April, 2006.
27. Gorseth, T. L., Estrada, D., Kiepert, J., Ogas, M. L., Cheek, B. J., Price, P. M., Baker, R. J., Bersuker, G., and Knowlton, W.B., "Preliminary Study of NOR Digital Response to Single pMOSFET Dielectric Degradation," presented at the *Workshop on Microelectronic Devices* (Boise, Idaho; April 14, 2006)
26. Sevier, D., Gribb, M., Plumlee, D., Moll, A. J., Hill, H. H., Hong, F., Baker, R. J., Loo, S. M., Walters, R. and Imonigie, J., "An In-Situ Ion Mobility Spectrometer Sensor System for Detecting Gaseous VOCs in the Vadose Zone," *Fourth International Conference on Unsaturated Soils (UNSAT '06) Conference, April 2-6, 2006, Carefree, AZ.*
25. Gribb, M., Hill, H. H., Baker, R. J., Loo, S. M., and Moll, A. J., "Ion Mobility Spectrometer (IMS) Sensor Project," presented at the *Environmental & Subsurface Science Symposium*, Inland Research Alliance, Sept. 19-21, 2005, Big Sky, Montana.
24. Ogas, M. L., Price, P. M., Kiepert J., Baker R. J., Bersuker G., and Knowlton W.B., *Degradation of Rise Time in NAND Gates Using 2.0 nm Gate Dielectrics*, oral presentation and publication at the 2005 IEEE Integrated Reliability Workshop, October 2005.
23. Butler, D. L. and Baker, R. J., *Low-Voltage Bandgap Reference Design Utilizing Schottky Diodes*, *Proceedings of the IEEE 48th International Midwest Symposium on Circuits and Systems*, Aug. 7-10, 2005.
22. Cheek, B. J., Southwick III, R. G., Ogas, M. L., Nagler, P. E., Whelchel, D., Kumar, S., Baker, R. J., and Knowlton, W. B., "Preliminary Soft Breakdown (SBD) Effects In CMOS Building Block Circuits," poster presentation at *2004 IEEE International Integrated Reliability Workshop*, Oct. 18-21, 2004.
21. Ogas, M., Southwick, R. G., Cheek, B. J., Lawrence, C. E., Kumar, S., Haggag, A., Baker, R. J., and Knowlton, W. B., "Multiple Waveform Pulse Voltage Stress Technique for Modeling Noise in Ultra-Thin Oxides," poster presentation at the *Workshop on Microelectronics and Electron Devices*, Boise, Idaho, April 16, 2004.
20. Ogas, M. L., Southwick III, R. G., Cheek, B. J., Baker, R. J., Bersuker, G., and Knowlton, W. B., "Survey of Oxide Degradation in Inverter Circuits Using 2.0nm MOS Devices," in *Proceedings of the 2004 IEEE International Integrated Reliability Workshop*, pp. 32-36.
19. Cheek, B. J., Stutzke, N., Santosh, K., Baker, R. J., Moll, A. J., and Knowlton, W. B., Investigation of Circuit-Level Oxide Degradation and its Effect on CMOS Inverter Operation Performance and MOSFET Characteristics, *2004 IEEE International Reliability Physics Symposium*, April, 25-29.

18. Stutzke, N., Cheek, B. J., Wiscombe, M., Lowman, T., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., *Effects of Circuit-Level Stress on Inverter Performance and MOSFET Characteristics*, 2003 IEEE International Integrated Reliability Workshop, Oct, 20-23.
17. Ogas, M. L., Southwick, R. G., Cheek, B. J., Lawrence, C. E., Kumar, S., Haggag, A., Baker, R. J., and Knowlton, W. B., *Investigation of Multiple Waveform Pulse Voltage Stress (MWPVS) Technique in Ultra-Thin Oxides*, poster presentation at the 2003 IEEE International Integrated Reliability Workshop Oct, 20-23.
16. Baker, R. J., *Mixed-Signal Design in the Microelectronics Curriculum*, IEEE University/Government/Industry Microelectronics (UGIM) Symposium, June 30 - July 2.
15. Hartman, J. A., Baker, R. J., Gribb, M., Hill, H. H., Jessing, J., Moll, A. J., Prouty, and Russell, D., *A Miniaturized Ion Mobility Spectrometer (IMS) Sensor for Wireless Operation*, FAME (Frontiers in Assessment Methods for the Environment) Symposium, Sponsored by NSF, Minneapolis, Minnesota, August 10-13, 2003.
14. Lawrence, C.E., Cheek, B. J., Lawrence, T. E., Kumar, S., Haggag, A., Baker, R. J., and Knowlton, W. B., *Gate Dielectric Degradation Effects on nMOS Devices Using a Noise Model Approach*, IEEE University/Government/Industry Microelectronics (UGIM) Symposium, June 30 - July 2, 2003.
13. Cheek, B., Lawrence, C., Lawrence, T., Gomez, J., Caldwell, T., Kiri, D., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., *Gate Dielectric Degradation Effects on nMOS Devices and Simple IC Building Blocks (SICBBs)*, IEEE Electron Devices Society Boise Meeting, Boise, ID Oct. 25, 2002.
12. Lawrence, C., Cheek, B., Caldwell, T., Lawrence, T., Kiri, D., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., *Pulse voltage stressing of ultrathin gate oxides in NMOS devices*, poster session at IEEE International Integrated Reliability Workshop, October 21-24, 2002.
11. Cheek, B., Lawrence, C., Lawrence, T., Caldwell, T., Kiri, D., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., *Circuit level reliability of ultrathin gate oxides for SICBBs: Preliminary study concentrated on the effect of stress on the NMOSFET of an inverter*, poster session at the IEEE International Integrated Reliability Workshop, October 21-24, 2002.
10. Baker, R. J., "Sensing Circuits for Resistive Memory," *IEEE Electron Devices Society Meeting*, Boise, Idaho October 25, 2002.
9. Rivera, B., Baker, R. J., Melngailis, J., "Design and Layout of Schottky Diodes in a Standard CMOS Process," 2001 International Semiconductor Device Research Symposium, Washington DC, Dec. 2001.
8. Hess, H. and Baker, R. J., "Easier Method to Simultaneously Trigger Series-Connected MOS Devices," *Power Systems World Conference 2000*, Boston, Massachusetts, September 2000.
7. Baker, R. J., and Hess, H., "Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices." *International Electric Machines and Drives Conference*, Seattle, Washington, May 1999, pp. 673-676.
6. Baker, R. J., "A windows based integrated circuit design tool for distance education," *International Conference on Simulation and Multimedia in Engineering Education*."
5. Chen, H. and Baker, R. J., "A CMOS Standard-Cell Library for the PC-based LASI Layout System," *Proceedings of the 41st International Midwest Symposium on Circuits and Systems*, August 9-12, 1998.
4. Liu, S. and Baker, R. J., "Process and temperature performance of a CMOS beta-multiplier voltage reference," *Proceedings of the 41st International Midwest Symposium on Circuits and Systems*, August 9-12, 1998.
3. Boyce, D.E. and Baker, R. J., "A Complete Layout System for the PC," *IEEE 40th International Midwest Symposium on Circuits and Systems*, 1997.
2. Baker, R. J., and Blair, J. J., "Step response considerations and the design of a suitable step generator for high speed digitizer testing," *LLNL's Third Annual Workshop on High Speed Digitizers*, April 3-4, Las Vegas, Nevada, 1991.
1. Baker, R. J., "Step-recovery diodes sharpen pulses," *Engineering Design News Magazine*, pp. 154-156, May 10, 1990.

EXPERT WITNESS EXPERIENCE (LAST 4 YEARS)

The law firms and clients (underlined) whom I have provided expert witness services in electrical and computer engineering are listed below. I have been deposed 94 times, given expert testimony at 12 trials (7 USITC, 2 D. Del., 1 Arbitr., 1 S.D. Cal., and 1 E.D. Tex.), and participated in 1 mediation.

Bracewell LLP (New York, NY and Seattle, WA)

Case – Kioxia America, Inc. and Kioxia Corporation v. BitMICRO LLC

Case Numbers – IPR2023-00741, IPR2023-00742, and IPR2023-00743. Petitions filed on March 23, 2023.

Case Subject Matter – Solid-state storage devices utilizing multi-profile memory controllers. Optimizing memory operations in a memory system suitable for use in an electronic storage device. Supplying energy to a cache memory using a supercapacitor.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Bookoff McAndrews, PLLC (Washington, DC)

Case – Lenovo Inc. and Motorola Mobility LLC v. Theta IP, LLC

Case Numbers – IPR2023-00694, IPR2023-00697, and IPR2023-00698. Petitions filed on March 7, 2023.

Case Subject Matter – Power in wireless communication circuits.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

McDermott Will & Emery LLP (Chicago, IL and Austin, TX)

Case – Xilinx, Inc. v. Polaris Innovations Limited

Case Numbers – IPR2023-00513 and IPR2023-00514. Petitions filed on February 6, 2023.

Case Subject Matter – Methods for terminating a memory chip with various termination resistances and output drivers for integrated circuits.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Norton Rose Fulbright LLP (Austin, TX and Dallas, TX)

Case – Current Lighting Solutions, LLC d/b/a GE Current v. Jiaxing Super Lighting Electric Appliance Co., Ltd.

Case Number – IPR2023-00270. Petition filed on December 19, 2022.

Case Number – IPR2023-00271. Petition filed on December 14, 2022.

Case Subject Matter – LED lighting, lamps, tube lamps, assembly, and associated circuits and electronics.

Work Performed – Provided expert consulting services and wrote declarations for inter partes review.

Paul Hastings LLP (Washington, DC)

Case – Ex Parte Reexaminations

Case Numbers – 90/015155 and 90/015156. Requests filed on November 7, 2022.

Case Number – 90/015134. Request filed on October 14, 2022.

Case Number – 90/015130. Request filed on September 30, 2022.

Case Subject Matter – Packaging and fabrication of light emitting diodes (LEDs).

Work Performed – Provided expert consulting services and wrote declaration.

Sheppard, Mullin, Richter & Hampton LLP (Menlo Park, CA)

Case – Bell Semiconductor, LLC v. NXP, SMC, Micron, Nvidia, Advanced Micro Devices (AMD), Acer, Infineon, Qualcomm, Motorola Mobility, and Western Digital

Case Number – ITC Investigation No. 337-TA-1340. Complaint filed October 6, 2022.

Case Subject Matter – Electronic devices, semiconductor devices, and components.

Work Performed – Provided expert consulting services.

O'Melveny & Myers LLP (Los Angeles, CA)

Case – Daedalus Prime LLC v. Samsung Electronics and TSMC

Case Number – ITC Investigation No. 337-TA-1335. Complaint filed September 12, 2022.

Case Subject Matter – Semiconductor devices, mobile devices, and components.

Work Performed – Provided expert consulting services.

DLA Piper (Chicago, IL and Washington, DC)

Case – Ampt, LLC v. SolarEdge Technologies, Inc.

Case Number – ITC Investigation No. 337-TA-1327. Complaint filed July 28, 2022.

Case Subject Matter – Solar power optimizers, inverters, and components.

Work Performed – Provided expert consulting services including writing declarations for claim construction, expert reports, and was deposed.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – Samsung Electronics Co., Ltd. v. Scramoge Technology Ltd.

Case Numbers – IPR2022-01052, IPR2022-01053, and IPR2022-01058. Petitions filed on May 26, 2022.

Case Numbers – IPR2022-01054, IPR2022-01055, IPR2022-01056, and IPR2022-01057. Petitions filed on May 24, 2022.

Case Number – IPR2022-00939. Petition filed on April 29, 2022.

Case Subject Matter – An antenna that supports wireless charging.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – Ex Parte Reexaminations

Case Number – 90/015020. Request filed on May 2, 2022.

Case Number – 90/014906. Request filed on November 12, 2021.

Case Number – 90/014899. Request filed on November 10, 2021.

Case Number – 90/014888. Request filed on October 21, 2021.

Case Numbers – 90/014886 and 90/014887. Requests filed on October 20, 2021.

Case Number – 90/014885. Request filed on October 19, 2021.

Case Subject Matter – Universal Serial Bus (USB) for charging.

Work Performed – Provided expert consulting services and wrote declarations.

DLA Piper (Chicago, IL, Austin, TX, and Washington, DC)

Case – SolarEdge Technologies, Inc. v. Fronius International GMBH

Case Number – IPR2022-00849. Petition filed on April 14, 2022.

Case Subject Matter – Mechanical assembly and enclosure whereby an upper housing part is detached from a lower housing part using a “rotate-and-lift” feature.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Kirkland & Ellis LLP (New York, NY)

Case – Samsung Electronics Co. v. Sonrai Memory Ltd.

Case Numbers – IPR2022-00305 and IPR2022-00306. Petitions filed on December 10, 2021.

Case Subject Matter – USB devices and circuits for saving power.

Work Performed – Provided expert consulting services including writing declarations for inter partes reviews.

Haynes and Boone, LLP (Washington, DC)

Case – Unified Patents, LLC v. Arigna Technology Limited

Case Number – IPR2022-00285. Petition filed on December 9, 2021.

Case Subject Matter – High voltage driver circuit for driving power devices such as insulated gate bipolar transistors (IGBTs).

Work Performed – Provided expert consulting services, wrote declaration for inter partes review and was deposed.

Paul Hastings LLP (Washington, DC)

Case – Samsung Electronics Co., Ltd. v. Lynk Labs, Inc.

Case Numbers – IPR2022-00149 and IPR2022-00150. Petitions filed on November 12, 2021

Case Numbers – IPR2022-00100 and IPR2022-00101. Petitions filed on October 28, 2021.

Case Numbers – IPR2022-00051, IPR2022-00052, and IPR2022-00098. Petitions filed on October 27, 2021.

Case Numbers – IPR2021-01575 and IPR2021-01576. Petitions filed on October 1, 2021.

Case Numbers – IPR2021-01299, IPR2021-01300, IPR2021-01345, IPR2021-01346, and IPR2021-01347. Petitions filed on September 7, 2021.

Case Subject Matter – Circuit design, including switching power supply design, rectifiers, power factor correction, etc. for lighting and displays using light emitting diodes (LEDs).

Work Performed – Provided expert consulting services, wrote declarations, and was deposed ten times.

Haynes and Boone, LLP (Plano, TX)

Case – Pure Storage, Inc. v. Digital Cache, LLC

Case Number – IPR2022-00121. Petition filed on October 29, 2021.

Case Subject Matter – Non-volatile memory (NVM) devices capable of retaining stored data in case of a power failure.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Banner Witcoff (Washington, DC)

Case – SolarEdge Technologies Ltd. v. Koolbridge Solar, Inc.

Case Numbers – IPR2022-00007, IPR2022-00008, IPR2022-00009, IPR2022-00010, IPR2022-00011, and IPR2022-00012. Petitions filed on October 11, 2021.

Case Numbers – IPR2022-00013, IPR2022-00014, and IPR2022-00015. Petitions filed on October 8, 2021.

Case Subject Matter – DC-to-AC converters using full-bridges, multi-level conversion for power systems, and other electronics for harvesting solar energy.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – Samsung Electronics Co., Ltd. v. LED Wafer Solutions LLC

Case Number – IPR2021-01554. Petition filed on September 20, 2021.

Case Number – IPR2021-01526. Petition filed on September 10, 2021.

Case Number – IPR2021-01506. Petition filed on September 7, 2021.

Case Number – IPR2021-01491. Petition filed on September 3, 2021.

Case Subject Matter – Packaging of light emitting diodes (LEDs).

Work Performed – Provided expert consulting services and wrote declarations.

Paul Hastings, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/014,846. Request filed on August 30, 2021.

Case Subject Matter – Wireless power transmission and ways to wirelessly charge and/or discharge a battery.

Work Performed – Provided expert consulting services and wrote declaration.

Jones Day (San Diego, CA and Pittsburgh, PA)

Case – SOLiD, Inc. v. CommScope Technologies LLC

Case Numbers – IPR2021-01390, IPR2021-01391, IPR2021-01392, IPR2021-01393, and IPR2021-01394. Petitions filed on August 12, 2021.

Case Subject Matter – Digital antenna system that enables extension of radio frequency (RF) analog signals from base stations to areas (e.g., inside of buildings) where access to such signals is inhibited.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declaration.

Unified Patents, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/019,015. Request filed on July 20, 2021.

Case Subject Matter – Voltage-controlled oscillator (VCO) temperature compensation.

Work Performed – Provided expert consulting services and wrote declaration.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC v. Unification Technologies LLC

Case Numbers – IPR2021-00940, IPR2021-00941, and IPR2021-00942. Petitions filed on June 4, 2021.

Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declarations.

Hill, Kertscher & Wharton, LLP (Atlanta, GA)

Case – Kaijet Technology v. Sanho Corporation

Case Number – IPR2021-00886. Petition filed on April 30, 2021.

Case Subject Matter – Port extension apparatus for headphone jack, USB (Universal Serial Bus or Type-C ports), and video ports such as VGA (Video Graphics Array), DVI (Digital Visual Interface), HDMI (High-Definition Multimedia Interface), DP (Display Port), and mini-DP.

Work Performed – Provided expert consulting services for inter partes review, wrote declaration, was deposed.

O'Melveny & Myers LLP (Los Angeles, CA and New York, NY)

Case – Solas OLED LTD. v. Samsung Electronics Co. LTD.

Case Number – Texas, ED (Marshall) 2:21-cv-00105. Complaint filed March 22, 2021.

Case Subject Matter – Touch-sensors for gesture recognition and signal processing for capacitive touch displays.

Work Performed – Provided expert consulting services including writing declaration for claim construction.

O'Melveny & Myers LLP (San Francisco, CA)

Case – Super Interconnect Technologies LLC v. Google LLC

Case Number – Texas, ED (Marshall) 2:18-cv-00463 (complaint filed November 2, 2018) and Texas, WD (Waco) 6:21-cv-00259 (complaint filed March 15, 2021).

Case Subject Matter – Transmission of data and clock signals. Serial signals such as transition minimized differential signaling. Communications between processors and non-volatile storage such as Universal Flash Storage (UFS) and embedded MultiMedia Controller (eMMC).

Work Performed – Provided expert consulting services and wrote expert reports.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, and Irvine, CA)

Case – Fundamental Innovation Systems International LLC v. Anker Innovations and Fantasia Trading LLC d/b/a Ankerdirect

Case Number – Delaware, 1:21-cv-00339. Complaint filed on March 5, 2021.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – TCT Mobile Inc. and TCL Communication, Inc. v. Fundamental Innovation Systems International LLC

Case Numbers – IPR2021-00597, IPR2021-00598, and IPR2021-00599. Petitions filed on February 26, 2021.

Case Number – IPR2021-00428. Petition filed on January 13, 2021.

Case Number – IPR2021-00410. Petition filed on January 11, 2021.

Case Number – IPR2021-00395. Petition filed on December 31, 2020.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services including writing declarations for inter partes reviews. Was deposed twice.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – Samsung, Inc. v. Pictos Technologies, Inc.

Case Number – IPR2021-00557. Petition filed on February 18, 2021.

Case Number – IPR2021-00436. Petition filed on January 19, 2021.

Case Numbers – IPR2021-00437 and IPR2021-00438. Petitions filed on January 15, 2021.

Case Subject Matter – Solid-state imaging devices including red, green, and blue pixels, data conversion circuits, and interpolation circuits. CMOS imagers including fabrication and design, active pixels, and semiconductor physics.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

O'Melveny & Myers LLP (San Francisco, CA) and DLA Piper (New York, NY)

Case – Solas OLED Ltd. v. BOE Technology Group Co. Ltd. and Samsung Electronics

Case Number – ITC Investigation No. 337-TA-1243. Complaint filed January 5, 2021.

Case Subject Matter – Active matrix OLED display devices and components

Work Performed – Provided expert consulting services, wrote expert reports, was deposed, and testified at trial.

Paul Hastings LLP (Washington, DC)

Case – Samsung, Inc. v. Garrity Power Services LLC

Case Number – IPR2021-00389. Petition filed on December 31, 2020.

Case Subject Matter – Power electronics including full-bridge PWM modules for wireless power transmission using magnetic coupling via antennas and transformers. Design of inductors and coils.

Work Performed – Provided expert consulting services and wrote declaration for inter partes reviews.

Morgan, Lewis & Bockius LLP (Palo Alto, CA and Shanghai, CN)

Case – Monolithic Power Systems, Inc. v. Meraki Integrated Circuit Technology, Inc. and Promate Electronic Company, LTD.

Case Number – Texas, WD (Waco) 6:20-cv-00876. Complaint filed on December 24, 2020.

Case Subject Matter – Design of switching power supplies including synchronous rectification.

Work Performed – Provided expert consulting services including declaration for claim construction, trade secret analysis and declaration, and Markman tutorial.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC; Dell Technologies Inc.; Dell Inc.; and HP Inc. v. Unification Technologies LLC

Case Numbers – IPR2021-00343, IPR2021-00344, and IPR2021-00345. Petitions filed on December 22, 2020.

Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services for inter partes reviews, wrote declarations, and was deposed.

Jones Day (Chicago, IL and Dallas, TX)

Case – WSOU Investments, LLC d/b/a Brazos Licensing and Development v. Xilinx, Inc.

Case Numbers – Delaware, 1:20-cv-01231 and Delaware, 1:20-cv-01233. Complaints filed on November 23, 2020 and September 16, 2020.

Case Subject Matter – Controlling power cycles in communication devices and transferring multiple asynchronous clock signals.

Work Performed – Provided expert consulting services, wrote claim construction declaration, wrote expert reports, and was deposed.

O'Melveny & Myers LLP (Los Angeles, CA)

Case – Cosemi Technologies, Inc. v. EverPro Technologies, Fibbr Technologies, Logitech, Inc., and Facebook Technologies

Case Number – ITC Investigation No. 337-TA-1233. Complaint filed October 28, 2020.

Case Subject Matter – Data cables, including HDMI, Display Port, and USB Type A, USB Type C and USB Type A/C data cables.

Work Performed – Provided expert consulting services.

Kirkland & Ellis LLP (Boston, MA and New York, NY)

Case – Pictos Technologies, Inc. v. Samsung Electronics Co., LTD. and Samsung Semiconductor, Inc.

Case Number – ITC Investigation No. 337-TA-1231. Complaint filed September 25, 2020.

Case Subject Matter – Solid-state imaging devices including red, green, and blue pixels, correction of bad pixels, data conversion circuits, and interpolation circuits. CMOS imagers including fabrication and design, active pixels, and semiconductor physics.

Work Performed – Provided expert consulting services and wrote expert report.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – Fundamental Innovation Systems International LLC v. TCT Mobile Inc. and TCL Communication, Inc.

Case Number – Delaware, 1:20-cv-00552. Complaint filed on September 11, 2020.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services including writing declarations, expert report on invalidity, and was deposed.

Walters Wilson LLP (Redwood City, CA)

Case – Western Digital Corporation and SanDisk, LLC v. Martin Kuster

Case Numbers – IPR2020-01410 and IPR2020-01411. Petitions filed on August 3, 2020.

Case Subject Matter – Computer connectors such as universal serial bus (USB) that connect to peripheral devices such as mice, keyboards, displays, printers, external storage, etc.

Work Performed – Provided expert consulting services for inter partes review, wrote declarations and was deposed.

O'Melveny & Myers LLP (Los Angeles, CA)

Case – Advanced Micro Devices, Inc. v. Monterey Research, LLC

Case Number – IPR2020-01315. Petition filed on July 16, 2020.

Case Number – IPR2020-00985. Petition filed on May 26, 2020.

Case Subject Matter – Reading and writing to semiconductor memory such as SRAM and double data rate (DDR) DRAM. Buffer circuits with variable current supplies for controlling the rise and fall times of output signals.

Work Performed – Provided expert consulting services for inter partes review, wrote declarations and was deposed twice.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – Unification Technologies LLC v. Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC

Case Number – Texas, WD (Waco) 6:20-cv-00500. Complaint filed June 5, 2020.

Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services, wrote declaration for claim construction, and was deposed.

Ari Law, P.C. (Palo Alto, CA) and Hill, Kertscher & Wharton, LLP (Atlanta, GA)

Case – Sanho Corporation v. Kaijet Technology, Magic Control Technology, and Star View Global

Case Numbers – Georgia, ND (Atlanta) 1:18-cv-05385 (third amended complaint filed November 14, 2019) and Georgia, ND (Atlanta) 1:20-cv-02150 (filed May 19, 2020).

Case Subject Matter – Port extension apparatus for headphone jack, USB (Universal Serial Bus or Type-C ports), and video ports such as VGA (Video Graphics Array), DVI (Digital Visual Interface), HDMI (High-Definition Multimedia Interface), DP (Display Port), and mini-DP.

Work Performed – Provided expert consulting services, wrote declaration for claim construction, and expert reports. Was deposed.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – Fundamental Innovation Systems International LLC v. Coolpad Group Limited, Coolpad Technologies, Inc., and Yulong Computer Telecommunication Scientific Co. Ltd.

Case Number – Texas, ED (Marshall) 2:20-cv-00117. Complaint filed on April 23, 2020.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services including writing declaration for claim construction.

Pillsbury Winthrop Shaw Pittman LLP (San Francisco, CA and Shanghai, China)

Case – SMIC, Americas v. Innovative Foundry Technologies LLC

Case Numbers – IPR2020-00837 and IPR2020-00839. Petitions filed on April 14, 2020.

Case Subject Matter – Methods of manufacturing a semiconductor component, such as a short-channel MOS device, including forming graded-junctions using spacers along the sidewalls of a transistor's gate.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declarations.

Russ August & Kabat (Los Angeles, CA)

Case – Oyster Optics, LLC v. Ciena Corporation

Case Number – California, ND (Oakland) 3:20-cv-02354. Complaint filed on April 7, 2020.

Case Subject Matter – Fiber optic telecommunication systems.

Work Performed – Provided expert consulting services, wrote claim construction declaration, and was deposed.

Russ August & Kabat (Los Angeles, CA)

Case – Seoul Semiconductor Co., Ltd. v. Document Security Systems, Inc.

Case Number – IPR2020-00938. Petition filed on May 18, 2020.

Case – Nichia Corporation v. Document Security Systems, Inc.

Case Number – IPR2020-00908. Petition filed on May 18, 2020.

Case – Cree, Inc. v. Document Security Systems, Inc.

Case Number – IPR2020-00557. Petition filed on February 11, 2020.

Case Subject Matter – Light emitting diodes (LEDs) as a light source, extraction of light.

Work Performed – Provided expert consulting services, wrote declaration for inter partes reviews, and was deposed three times.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – Flex Logix Technologies, Inc. v. Konda Technologies Inc.

Case Numbers – IPR2020-00260, IPR2020-00261, and IPR2020-00260. Petitions filed on December 16, 2019.

Case Numbers – PGR2019-00037, PGR2019-00040, and PGR2019-00042. Petitions filed on March 18, 2019.

Case Subject Matter – FPGA layout routing for integrated circuits and networks, electrical and computer engineering.

Work Performed – Provided expert consulting services and wrote declarations for post grant and inter partes reviews.

DLA Piper (Chicago, IL, Houston, TX, and Washington, DC) and White & Case LLP (New York, NY and Washington, DC)

Case – M-Red Inc. v. Panasonic Corporation

Case Number – Texas, ED (Marshall) 2:19-cv-00251. Complaint filed on July 16, 2019.

Case Subject Matter – Integrated circuit electronics adjustment, such as ring oscillators, using auto calibration.
Evaluating a known good die using both wire and flip-chip interconnects.

Work Performed – Provided expert consulting services and wrote declaration for claim construction.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – Samsung, Inc. v. NuCurrent, Inc.

Case Number – IPR2019-01217. Petition filed on June 19, 2019.

Case Numbers – PGR2019-00049 and PGR2019-00050. Petitions filed on May 28, 2019.

Case Numbers – IPR2019-00858, IPR2019-00859, IPR2019-00860, IPR2019-00861, IPR2019-00862, and IPR2019-00863. Petitions filed on March 22, 2019.

Case Subject Matter – Wireless power transmission using magnetic coupling via antennas and transformers.
Design of inductors and coils.

Work Performed – Provided expert consulting services and wrote declarations for post grant and inter partes reviews. Was deposed five times.

DLA Piper (East Palo Alto, CA)

Case – Invensas Corporation and Tessera Advanced Technologies, Inc. v. NVIDIA Corporation

Case Number – Delaware, 1:19-cv-00861. Complaint filed on May 8, 2019.

Case Subject Matter – Reference voltage circuits (programmable bandgaps) having a substantially zero temperature coefficient using bipolar and MOS transistors.

Work Performed – Provided expert consulting services.

Irell & Manella LLP (Los Angeles, CA)

Case – VLSI Technology LLC v. Intel Corporation

Case Number – Texas, WD (Waco) 6:19-cv-00256. Complaint filed on April 11, 2019.

Case Subject Matter – Static Random Access Memory (SRAM) having a variable power supply using charge-sharing capacitors, methods for designing digital systems, and hardware managed interrupt control.

Work Performed – Provided expert consulting services, wrote expert reports, declaration, and was deposed.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – Samsung, Inc. v. ProMOS Technologies, Inc.

Case Numbers – IPR2019-00779, IPR2019-00780, IPR2019-00781, IPR2019-00784, and IPR2019-00785. Petitions filed on March 5, 2019.

Case Subject Matter – Programmable latches that include non-volatile programmable elements, digital delay elements, and decoders for memory chips.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed four times.