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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/848,246	02/20/2007	7180403	038P0401	4526

7590

01/31/2007

Rodney F. Brown
3365 Baltimore Street
San Diego, CA 92117

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 340 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Ralph W. Quan, Broomfield, CO;

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated in Block 1, or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee payments.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Rodney F. Brown
 3365 Baltimore Street
 San Diego, CA 92117

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Rodney F. Brown (Depositor's name)
 (Signature)
 January 8, 2007 (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/848,246	05/18/2004	Ralph W. Quan	038P0401	4526

TITLE OF INVENTION:

RFID Reader Utilizing an Analog to Digital Converter for Data Acquisition and Power Monitoring Functions

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$300	\$0	\$1700	02/20/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
Au, Scott D.	2612	340-010300

01/08/2007 TBESHAH2 00000030 024245 10848246
 01 FC:1501 1400.00 DA
 02 FC:1504 300.00 DA

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. Rodney F. Brown

2.

3.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

Assa Abloy Identification Technology Group AB

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Stockholm, Sweden

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card, Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 02-4245 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature

Rodney F. Brown

Date January 8, 2007

Typed or printed name Rodney F. Brown

Registration No. 30,450

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

7590

11/17/2006

Rodney F. Brown
3365 Baltimore Street
San Diego, CA 92117

EXAMINER

AU, SCOTT D

ART UNIT

PAPER NUMBER

2612

DATE MAILED: 11/17/2006

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/848,246

05/18/2004

Ralph W. Quan

038P0401

4526

TITLE OF INVENTION: RFID READER UTILIZING AN ANALOG TO DIGITAL CONVERTER FOR DATA ACQUISITION AND POWER MONITORING FUNCTIONS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$300	\$0	\$1700	02/20/2007

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590

11/17/2006

Rodney F. Brown
3365 Baltimore Street
San Diego, CA 92117

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/848,246	05/18/2004	Ralph W. Quan	038P0401	4526

TITLE OF INVENTION: RFID READER UTILIZING AN ANALOG TO DIGITAL CONVERTER FOR DATA ACQUISITION AND POWER MONITORING FUNCTIONS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$300	\$0	\$1700	02/20/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
AU, SCOTT D	2612	340-010300

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card: Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/848,246	05/18/2004	Ralph W. Quan	038P0401	4526

7590

11/17/2006

Rodney F. Brown
3365 Baltimore Street
San Diego, CA 92117

EXAMINER

AU, SCOTT D

ART UNIT	PAPER NUMBER
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2612

DATE MAILED: 11/17/2006

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 340 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 340 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability

Application No.

10/848,246

Examiner

Scott Au

Applicant(s)

QUAN, RALPH W.

Art Unit

2612

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 9/29/2006.
2. ☒ The allowed claim(s) is/are 1-43.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
 - * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____

Allowable Subject Matter

This communication is in response to applicant's Amendment which filed September 29, 2006 in the application of Quan for a "RFID reader utilizing an analog to digital converter for data acquisition and power monitoring functions" filed May 18, 2004.

The amendment has been entered and made of record.

Claims 44-46 are cancelled.

Claims 1-43 are allowed as evident by applicant's amendment.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submission should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Au whose telephone number is (571) 272-3063. The examiner can normally be reached on Mon-Fri, 8:30AM – 5:00PM.

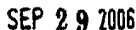
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Hofsass can be reached at (571) 272-2981. The fax phone numbers for the organization where this application or proceeding is assigned are (571)-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-305-3900.

SA

JEFFERY HOFSSASS
SUPERVISORY PATENT EXAM.
TECHNOLOGY CENTER 260

WAVELYNX EX. 1002, Pg. 7



Approved for use through 03/31/2007. OMB 0651-0031

U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449/PTO

(Use as many sheets as necessary)

Complete if Known

Application Number	10/848.246
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Filing Date	05/18/2004
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First Named Inventor	Ralph W. Quan
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Art Unit	2612
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Examiner Name	Scott Au
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Attorney Docket Number	038P0401
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Sheet	1	of	1
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U. S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T*
		Country Code ³ -Number ⁴ -Kind Code ⁶ (if known)				
SA		GB-2305074-A	03/26/1997	Howell et al.	Fig. 6 p.15,1.26-p.16,1.23	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Issue Classification 	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/848,246	QUAN, RALPH W.	
	Examiner	Art Unit	
	Scott Au	2612	

ISSUE CLASSIFICATION										
ORIGINAL				CROSS REFERENCE(S)						
CLASS	SUBCLASS			CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
340	10.3			340	572.4	825	572	447	10.34	10.4
INTERNATIONAL CLASSIFICATION										
H04	A	5122								
G08	B	1314								
G06	F	1342								
		1								
		1								

Scott Au 11/6/06 (Assistant Examiner) (Date)	JEFFERY WOFSAEC SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2600 (Primary Examiner) (Date) 11/9/06	Total Claims Allowed: 43
[Signature] 11-5-06 (Legal Instruments Examiner) (Date)		O.G. Print Claim(s) 1 O.G. Print Fig. 1

☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	31	31	61	91	121	151	181	
2	2	32	32	62	92	122	152	182	
3	3	36	33	63	93	123	153	183	
4	4	37	34	64	94	124	154	184	
12	5	38	35	65	95	125	155	185	
19	6	41	36	66	96	126	156	186	
20	7	39	37	67	97	127	157	187	
22	8	43	38	68	98	128	158	188	
23	9	40	39	69	99	129	159	189	
24	10	42	40	70	100	130	160	190	
5	11	33	41	71	101	131	161	191	
6	12	34	42	72	102	132	162	192	
7	13	35	43	73	103	133	163	193	
8	14		44	74	104	134	164	194	
13	15		45	75	105	135	165	195	
14	16		46	76	106	136	166	196	
16	17		47	77	107	137	167	197	
17	18		48	78	108	138	168	198	
18	19		49	79	109	139	169	199	
21	20		50	80	110	140	170	200	
15	21		51	81	111	141	171	201	
9	22		52	82	112	142	172	202	
10	23		53	83	113	143	173	203	
11	24		54	84	114	144	174	204	
25	25		55	85	115	145	175	205	
26	26		56	86	116	146	176	206	
27	27		57	87	117	147	177	207	
28	28		58	88	118	148	178	208	
29	29		59	89	119	149	179	209	
30	30		60	90	120	150	180	210	

Search Notes



Application/Control No.

10/848,246

Examiner

Scott Au

Applicant(s)/Patent under Reexamination

QUAN, RALPH W.

Art Unit

2612

SEARCHED

Class	Subclass	Date	Examiner
340	10.3	5/31/06	SA
	572.4		
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	572		
	447		
	10.34		
	10.4	6/2/06	
	updated		
	Search	11/6/06	SA

INTERFERENCE SEARCHED

Class	Subclass	Date	Examiner
Same as above			SA

SEARCH NOTES (INCLUDING SEARCH STRATEGY)

	DATE	EXMR
Search EAST	5/31/06	
	SA	SA
Keywords:		
analog, digital		
reader, interrogation		
excitation		
tag, transponder		
resistor, capacitors		
diode, level		
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Bib Data Sheet

CONFIRMATION NO. 4526

SERIAL NUMBER 10/848,246	FILING OR 371(c) DATE 05/18/2004 RULE	CLASS 340	GROUP ART UNIT 2612	ATTORNEY DOCKET NO. 038P0401	
APPLICANTS Ralph W. Quan, Broomfield, CO; ** CONTINUING DATA ***** NO ** FOREIGN APPLICATIONS ***** NO <i>Sau 11/6/06</i> IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 07/16/2004					
Foreign Priority claimed ☐ yes ☒ no 35 USC 119 (a-d) conditions ☐ yes ☒ no ☐ Met after met <i>Allowance</i> Verified and <i>Scott</i> <i>11/6/06</i> Acknowledged <i>Examiner's Signature</i> <i>Initials</i>		STATE OR COUNTRY CO	SHEETS DRAWING 3	TOTAL CLAIMS 46	INDEPENDENT CLAIMS 3
ADDRESS Rodney F. Brown 3365 Baltimore Street San Diego, CA92117					
TITLE RFID reader utilizing an analog to digital converter for data acquisition and power monitoring functions					
FILING FEE RECEIVED 1838	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

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September 26, 2006
DATE

Rodney F. Brown
RODNEY F. BROWN

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No. : 10/848,246
Applicant : Ralph W. Quan
Filed : May 18, 2004
Title : RFID Reader Utilizing an Analog to Digital Converter for Data Acquisition and Power Monitoring Functions

Art Unit : 2612
Examiner : Scott D. Au

Docket No. : 038P0401

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR RECONSIDERATION WITH AMENDMENT UNDER 37 C.F.R. §1.111

Sir:

In response to the Office Action of June 26, 2006, please amend the above-captioned patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks / Arguments begin on page 13 of this paper.

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The following listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A reader for an RFID system comprising:

- a signal generator for generating a detection signal containing analog data and for generating an excitation signal;
- a transmitting antenna coupled with said signal generator for transmitting said detection signal and said excitation signal into a space surrounding said transmitting antenna;
- a receiving antenna for receiving a transponder data signal at a voltage value containing received digital data from a transponder in said space;
- receiver electronics coupled with said receiving antenna for conditioning said transponder data signal to ~~place said~~ a conditioned transponder data signal ~~in a condition for reading~~ including said received digital data;
- an internal power source for supplying electrical operating power to said reader, said internal power source having a declining power level as a function of use; and
- a single-chip microcontroller coupled with said internal power source and said receiver electronics, said single-chip microcontroller including an analog to digital converter to acquire said analog data from said detection signal and said received digital data from said conditioned transponder data signal and to convert said analog data from said detection signal to converted digital data, wherein said microcontroller further includes a detection means for evaluating said converted digital data to detect a transponder presence in the space surrounding said transmitting antenna and said microcontroller further includes a reading means for demodulating said conditioned transponder data signal to read said received digital data.

Claim 2 (original): The reader of claim 1, wherein said receiver electronics includes a receiver electronics input from said receiving antenna, a receiver electronics output to

said single-chip microcontroller, and a plurality of relatively low-cost simple electrical components selected from the group consisting of resistors, diodes, capacitors, and electrical switches, and excludes relatively high-cost complex multi-stage band pass amplifiers.

Claim 3 (currently amended): The reader of claim 1, wherein said ~~single-chip microcontroller further includes~~ reading means is a software and/or firmware-based demodulator ~~for demodulating said transponder data signal to read said digital data from said transponder data signal.~~

Claim 4 (original): The reader of claim 1, wherein said receiving antenna and said transmitting antenna are both included in a single dual-function antenna.

Claim 5 (currently amended): ~~The reader of claim 2~~ A reader for an RFID system comprising:

a signal generator for generating a detection signal containing analog data and for generating an excitation signal;

a transmitting antenna coupled with said signal generator for transmitting said detection signal and said excitation signal into a space surrounding said transmitting antenna;

a receiving antenna for receiving a transponder data signal at a voltage value containing digital data from a transponder in said space;

receiver electronics coupled with said receiving antenna for conditioning said transponder data signal to place said transponder data signal in a condition for reading said digital data;

an internal power source for supplying electrical operating power to said reader, said internal power source having a declining power level as a function of use; and

a single-chip microcontroller coupled with said internal power source and said receiver electronics, said single-chip microcontroller including an analog to digital converter to acquire said analog data from said detection signal and said digital data from said transponder data signal and to convert said analog data from said detection signal to

converted digital data, wherein said receiver electronics includes a resistor divider section comprising first and second series resistors at said receiver electronics input forming a voltage divider to reduce said voltage value of said transponder data signal and third and fourth series resistors downstream of said first and second series resistors positioned between ground and said power supply and a blocking capacitor positioned in parallel with the second series resistor upstream of said third and fourth series resistors to maintain said transponder data signal at said receiver electronics output in a voltage range between about ground and said power supply, inclusive.

Claim 6 (currently amended): ~~The reader of claim 2~~ A reader for an RFID system comprising:

a signal generator for generating a detection signal containing analog data and for generating an excitation signal;

a transmitting antenna coupled with said signal generator for transmitting said detection signal and said excitation signal into a space surrounding said transmitting antenna;

a receiving antenna for receiving a transponder data signal at a voltage value containing digital data from a transponder in said space;

receiver electronics coupled with said receiving antenna for conditioning said transponder data signal to place said transponder data signal in a condition for reading said digital data;

an internal power source for supplying electrical operating power to said reader, said internal power source having a declining power level as a function of use; and

a single-chip microcontroller coupled with said internal power source and said receiver electronics, said single-chip microcontroller including an analog to digital converter to acquire said analog data from said detection signal and said digital data from said transponder data signal and to convert said analog data from said detection signal to converted digital data, wherein said receiver electronics includes a peak detector section comprising a rectifier at said receiver electronics input to rectify said voltage value of said

transponder data signal and a pair of series resistors downstream of said rectifier positioned between ground and said power supply and a blocking capacitor positioned between said rectifier and said pair of series resistors to maintain said transponder data signal at said receiver electronics output in a voltage range between about ground and said power supply, inclusive.

Claim 7 (original): The reader of claim 6, wherein said rectifier includes a diode and said peak detector section further comprises a detector capacitor and a detector resistor, said detector capacitor and detector resistor positioned in parallel with one another and in parallel with said blocking capacitor downstream of said diode and upstream of said pair of series resistors.

Claim 8 (currently amended): ~~The reader of claim 2~~ A reader for an RFID system comprising:

a signal generator for generating a detection signal containing analog data and for generating an excitation signal;

a transmitting antenna coupled with said signal generator for transmitting said detection signal and said excitation signal into a space surrounding said transmitting antenna;

a receiving antenna for receiving a transponder data signal at a voltage value containing digital data from a transponder in said space;

receiver electronics coupled with said receiving antenna for conditioning said transponder data signal to place said transponder data signal in a condition for reading said digital data;

an internal power source for supplying electrical operating power to said reader, said internal power source having a declining power level as a function of use; and

a single-chip microcontroller coupled with said internal power source and said receiver electronics, said single-chip microcontroller including an analog to digital converter to acquire said analog data from said detection signal and said digital data from said transponder data signal and to convert said analog data from said detection signal to

converted digital data, wherein said receiver electronics includes an integrator section comprising a rectifier and an integrator in series at said receiver electronics input and coupled with said receiver electronics output, said receiver electronics output coupled with said analog to digital converter.

Claim 9 (original): The reader of claim 8, wherein said rectifier includes a diode and said integrator includes an integrator resistor and integrator capacitor in series with said diode, said integrator section further comprising a paired grounding switch resistor and grounding switch in series with one another and in parallel with said integrator capacitor downstream of said integrator resistor, said paired grounding switch resistor and grounding switch coupling said integrator capacitor with ground when said grounding switch is closed and coupling said integrator capacitor with said analog to digital converter when said grounding switch is open.

Claim 10 (original): The reader of claim 8, wherein said rectifier includes a diode and said integrator includes an integrator resistor and integrator capacitor in series with said diode, said integrator section further comprising a charging switch in series with said integrator capacitor and ground, said charging switch coupling said integrator capacitor with said receiving antenna when said charging switch is closed and decoupling said integrator capacitor from said receiving antenna when said charging switch is open.

Claim 11 (currently amended): The reader of claim 1, wherein said reader further comprises a sample and hold circuit having one or more sample times for isolating points on said detection signal where said analog data is to be acquired and for isolating points on said transponder data signal where said received digital data is to be acquired.

Claim 12 (original): The reader of claim 11, wherein said sample and hold circuit is included in said analog to digital converter of said single-chip microcontroller.

Claim 13 (original): The reader of claim 11, wherein said microcontroller controls said one or more sample times of said sample and hold circuit and adjusts said one or more sample times in response to different values of carrier frequency, data rate, and/or modulation type of said transponder data signal.

Claim 14 (original): The reader of claim 11, wherein said microcontroller controls said one or more sample times of said sample and hold circuit and adjusts said one or more sample times to enable detection of a transponder from a limited sampling of detection signals.

Claim 15 (original): The reader of claim 5, wherein said receiver electronics further includes a peak detector section comprising a rectifier at said receiver electronics input to rectify said voltage value of said transponder data signal and a pair of series resistors downstream of said rectifier positioned between ground and said power supply and a blocking capacitor positioned between said rectifier and said pair of series resistors to maintain said transponder data signal at said receiver electronics output in a voltage range between about ground and said power supply, inclusive.

Claim 16 (original): The reader of claim 15, wherein said rectifier includes a diode and said peak detector section further comprises a detector capacitor and a detector resistor, said detector capacitor and detector resistor positioned in parallel with one another and in parallel with said blocking capacitor downstream of said diode and upstream of said pair of series resistors.

Claim 17 (original): The reader of claim 5, wherein said receiver electronics further includes an integrator section comprising a rectifier and an integrator in series at said receiver electronics input and coupled with said receiver electronics output, said receiver electronics output coupled with said analog to digital converter.

Claim 18 (original): The reader of claim 17, wherein said rectifier includes a diode and said integrator includes an integrator resistor and integrator capacitor in series with said diode, said integrator section further comprising a paired grounding switch resistor and grounding switch in series with one another and in parallel with said integrator capacitor downstream of said integrator resistor, said paired grounding switch resistor and grounding switch coupling said integrator capacitor with ground when said grounding switch is closed and coupling said integrator capacitor with said analog to digital converter when said grounding switch is open.

Claim 19 (original): The reader of claim 17, wherein said rectifier includes a diode and said integrator includes an integrator resistor and integrator capacitor in series with said diode, said integrator section further comprising a charging switch in series with said integrator capacitor and ground, said charging switch coupling said integrator capacitor with said receiving antenna when said charging switch is closed and decoupling said integrator capacitor from said receiving antenna when said charging switch is open.

Claim 20 (original): The reader of claim 6, wherein said receiver electronics further includes an integrator section comprising an integrator at said receiver electronics input and coupled with said receiver electronics output, said receiver electronics output coupled with said analog to digital converter.

Claim 21 (original): The reader of claim 15, wherein said receiver electronics further includes an integrator section comprising an integrator at said receiver electronics input and coupled with said receiver electronics output, said receiver electronics output coupled with said analog to digital converter.

Claim 22 (original): The reader of claim 1 further comprising a transmitting tuning capacitor paired with said transmitting antenna and a receiving tuning capacitor paired with said receiving antenna.

Claim 23 (original): The reader of claim 22, wherein said receiving tuning capacitor and said transmitting tuning capacitor are both included in a single dual-function tuning capacitor.

Claim 24 (original): The reader of claim 22, wherein said transmitting tuning capacitor and/or said receiving tuning capacitor is a first tuning capacitor for tuning a first reader antenna to a higher carrier frequency, said reader further comprising a second tuning capacitor for tuning a second reader antenna to a lower carrier frequency,

Claim 25 (currently amended): A reader for an RFID system comprising:
a signal generator for generating a detection signal containing analog data and for generating an excitation signal;
a transmitting antenna coupled with said signal generator for transmitting said

detection signal and said excitation signal into a space surrounding said transmitting antenna;

a receiving antenna for receiving a transponder data signal at a voltage value containing received digital data from a transponder in said space;

receiver electronics coupled with said receiving antenna for conditioning said transponder data signal to ~~place said~~ a conditioned transponder data signal ~~in a condition for reading~~ including said received digital data; and

a single-chip microcontroller coupled with said receiver electronics, said single-chip microcontroller including an analog to digital converter to acquire said analog data from said detection signal and said received digital data from said transponder data signal and to convert said analog data from said detection signal to converted digital data, said single-chip microcontroller further including a demodulator for demodulating said conditioned transponder data signal to read said received digital data ~~from said transponder data signal~~ and still further including a detection means for evaluating said converted digital data to detect a transponder presence in the space surrounding said transmitting antenna.

Claim 26 (original): The reader of claim 25, wherein said receiver electronics includes a receiver electronics input from said receiving antenna, a receiver electronics output to said single-chip microcontroller, and a plurality of relatively low-cost simple electrical components selected from the group consisting of resistors, diodes, capacitors, and electrical switches, and excludes one or more relatively high-cost complex multi-stage band pass amplifiers.

Claim 27 (original): The reader of claim 25, wherein said receiving antenna and said transmitting antenna are both included in a single dual-function antenna.

Claim 28 (currently amended): A method for operating a reader for an RFID system comprising:

generating a detection signal containing analog data ~~in a detection mode of operation~~;

transmitting said detection signal from a transmitting antenna into a space

surrounding said transmitting antenna ~~to detect a proximal transponder;~~

acquiring said analog data from said detection signal with an analog to digital converter included within a single-chip microcontroller and coupled with receiver electronics;

converting said analog data to converted digital data with said analog to digital converter;

evaluating said converted digital data with said microcontroller to detect a proximal transponder in said space surrounding said transmitting antenna;

generating an excitation signal ~~in an excitation mode of operation;~~

transmitting said excitation signal from said transmitting antenna into said space to power up said proximal transponder;

generating a transponder data signal at said proximal transponder in response to said excitation signal and propagating said transponder data signal through said space from said proximal transponder;

receiving said transponder data signal with a receiving antenna, wherein said transponder data signal is at a voltage value and contains received digital data;

conditioning said transponder data signal with said receiver electronics ~~coupled with said receiving antenna to place said to a conditioned~~ transponder data signal ~~in a condition for reading said digital data;~~

~~coupling an analog to digital converter in a single-chip microcontroller with an internal power source supplying electrical operating power to said reader, said internal power source having a declining power level as a function of use and with said receiver electronics;~~

~~coupling said analog to digital converter with said receiver electronics;~~

~~acquiring said analog data from said detection signal with said analog to digital converter for use in said detection mode; and~~

acquiring said received digital data from said conditioned transponder data signal with said analog to digital converter ~~for use in a signal reading mode of operation; and~~

demodulating said conditioned transponder data signal with said microcontroller to read said received digital data.

Claim 29 (original): The method of claim 28, wherein said receiver electronics includes a plurality of relatively low-cost simple electrical components selected from the group consisting of resistors, diodes, capacitors, and electrical switches, and excludes one or more relatively high-cost complex multi-stage band pass amplifiers.

Claim 30 (currently amended): The method of claim 28 ~~further comprising demodulating, wherein said conditioned transponder data signal is demodulated~~ with software and/or firmware contained in said single-chip microcontroller ~~to read said digital data from said transponder data signal in said signal-reading mode.~~

Claim 31 (original): The method of claim 28, wherein said receiving antenna and said transmitting antenna are both included in a single dual-function antenna.

Claim 32 (original): The method of claim 28, wherein said transponder data signal is conditioned with said receiver electronics by reducing said voltage value of said transponder data signal and maintaining said transponder data signal in a voltage range between about ground and a power supply for said reader, inclusive.

Claim 33 (original): The method of claim 28, wherein said transponder data signal is conditioned with said receiver electronics by rectifying said voltage value of said transponder data signal and maintaining said transponder data signal in a voltage range between about ground and a power supply for said reader, inclusive.

Claim 34 (original): The method of claim 28, wherein said transponder data signal is conditioned with said receiver electronics by rectifying said voltage value of said transponder data signal and integrating said transponder data signal over one or more cycles of a carrier frequency of said transponder data signal.

Claim 35 (original): The method of claim 28, further comprising isolating points on said detection signal where said analog data is to be acquired with a sample and hold circuit having one or more sample times.

Claim 36 (currently amended): The method of claim 28, further comprising isolating

points on said transponder data signal where said received digital data is to be acquired with a sample and hold circuit having one or more sample times.

Claim 37 (original): The method of claim 35, wherein said sample and hold circuit is included in said analog to digital converter of said single-chip microcontroller.

Claim 38 (original): The method of claim 36, wherein said sample and hold circuit is included in said analog to digital converter of said single-chip microcontroller.

Claim 39 (original): The method of claim 35, wherein said microcontroller controls said one or more sample times of said sample and hold circuit and adjusts said one or more sample times to enable detection of said proximal transponder from a limited sampling of detection signals.

Claim 40 (original): The method of claim 36, wherein said microcontroller controls said one or more sample times of said sample and hold circuit and adjusts said one or more sample times in response to different values of carrier frequency, data rate, and/or modulation type of said transponder data signal.

Claim 41 (original): The method of claim 32, wherein said transponder data signal is conditioned with said receiver electronics by rectifying said voltage value of said transponder data signal and maintaining said transponder data signal in a voltage range between about ground and a power supply for said reader, inclusive.

Claim 42 (original): The method of claim 41, wherein said transponder data signal is conditioned with said receiver electronics by rectifying said voltage value of said transponder data signal and integrating said transponder data signal over one or more cycles of a carrier frequency of said transponder data signal.

Claim 43 (original): The method of claim 32, wherein said transponder data signal is conditioned with said receiver electronics by rectifying said voltage value of said transponder data signal and integrating said transponder data signal over one or more cycles of a carrier frequency of said transponder data signal.

Claims 44-46 are canceled without prejudice.

REMARKS / ARGUMENTS

Claims 1-46 were pending in the above-captioned patent application at the time of the Office Action. Claims 1-4, 11-14, and 22-46 are rejected. Claims 5-10 and 15-21 are objected to but would be allowable if rewritten in independent form. In response to the objections and rejections, applicant amends claims 1, 3, 5, 6, 8, 11, 25, 28, 30, and 36 and cancels claims 44-46. Each specific ground of rejection is addressed below.

Rejections Under 35 U.S.C. §103

Claims 1, 3, 4, 11-14, 25, 27, 28, and 30-46 have been rejected under 35 U.S.C. §103(a) as being unpatentably obvious over U.S. Patent 6,467,708 to Johnson in view of U.S. Patent 5,347,263 to Carroll et al. In particular, the Office Action asserts that Johnson discloses every limitation of claim 1, 25, or 28 with the exception of a single-chip microcontroller including an analog to digital converter to acquire analog data from the detection signal and digital data from the transponder data signal and convert the analog data to converted digital data. However, the Office Action asserts that Carroll et al. discloses the above-recited microcontroller limitations at col. 7, lines 1-8 and col. 9, lines 14-39. Thus, the Office Action concludes that the teaching of Carroll et al. in combination with Johnson renders claims 1, 25, and 28 obvious.

It is respectfully submitted that claim 1 as amended traverses the instant ground of rejection. Amended claim 1 requires that the single-chip microcontroller include an analog to digital converter (ADC), a detection means and a reading means. The ADC requires the capability to acquire both the analog data from the detection signal and the received digital data from the conditioned transponder data signal and to convert the analog data to converted digital data. The detection means requires the capability to evaluate the converted digital data to detect a transponder presence in the space surrounding the transmitting antenna. The reading means requires the capability to demodulate the conditioned transponder data signal to read the received digital data.

Carroll et al. discloses a prior art single-chip microprocessor 31 at Figure 2 and col.

7, lines 1-26. The microprocessor 31 is positioned downstream of a band pass amplifier 29 and detector 30 to receive an output signal from the detector 30. It is apparent from the disclosure of Carroll et al. that the band pass amplifier 29 functions as a conditioner to condition (in this case, filter and amplify) the transponder data signal received from the transponder which includes digital data to be read by the reader. The band pass amplifier 29 outputs a conditioned transponder data signal (termed the received signal and characterized as a raw carrier signal) to the detector 30. The detector 30 functions as a demodulator to convert the conditioned transponder data signal to a digital bit stream, thereby "reading" the digital data contained in the transponder data signal. The detector 30 outputs the digital data to the microprocessor 31 for further processing before outputting the digital data as a serial bit stream to peripheral equipment. The microprocessor output directs some appropriate action by the peripheral equipment, such as opening a door, triggering an alarm, enabling a piece of machinery, etc.

Col. 7 of Carroll et al. only contains teaching with respect to processing the transponder data signal. There is no teaching at col. 7 of Carroll et al. with respect to processing a detection signal as recited in the instant claim 1. Accordingly, col. 7 of Carroll et al. lacks teaching of an ADC in the reader microcontroller having the capability of acquiring analog data from the detection signal and converting the analog data to converted digital data. Col. 7 of Carroll et al. also lacks teaching of a detection means in the microcontroller having the capability to evaluate the converted digital data to detect a transponder presence in the space surrounding the transmitting antenna. Furthermore, col. 7 of Carroll et al. lacks teaching of a reading means in the microcontroller having the capability to demodulate the conditioned transponder data signal to read the received digital data. Instead col. 7 of Carroll et al. teaches demodulation of the transponder data signal in the detector 30 rather than the microcontroller as required by claim 1.

Carroll et al. discloses certain inventive features of a microprocessor 42 at Figures 3 and 5 and col. 8, line 50 through col. 9, line 39. The microprocessor 42 has a number of parallel I/O pin circuits 50 and associated I/O pins 52 wired directly to the antenna coil

43 of the reader 40. However, the above-cited section of Carroll et al. only discloses the output function of the I/O pin circuits 50 and associated I/O pins 52. In particular, the microprocessor 42 outputs signals through the parallel I/O pin circuits 50 and associated I/O pins 52 to the antenna coil 43, which in combination function as drivers for the excitation signals on the antenna coil 43. Carroll et al. claims to achieve significant savings in circuit complexity by using the microprocessor 42 to drive the excitation signals on the antenna coil 43 rather than using a separate driver circuit as is commonly done in the prior art. See col. 9, lines 14-39.

As such, cols. 8 and 9 of Carroll et al. only contain teaching with respect to generating excitation signals for transmission by the reader into the space surrounding the antenna coil. Cols. 8 and 9 of Carroll et al. lack any teaching with respect to processing a detection signal as recited in the instant claim 1. Accordingly, cols. 8 and 9 of Carroll et al. lack teaching of an ADC in the reader microcontroller having the capability of acquiring analog data from the detection signal and converting the analog data to converted digital data. Cols. 8 and 9 of Carroll et al. also lack the required teaching of a detection means in the microcontroller having the capability to evaluate the converted digital data to detect a transponder presence in the space surrounding the transmitting antenna. Furthermore, cols. 8 and 9 of Carroll et al. lack the required teaching of a reading means in the microcontroller having the capability to demodulate the conditioned transponder data signal to read the received digital data. Thus, the teaching of Carroll et al. in combination with Johnson is insufficient to render claim 1 obvious and claim 1 is allowable over the references.

Amended claim 25 includes similar limitations to claim 1 with respect to the microcontroller. In particular, amended claim 25 requires that the single-chip microcontroller include an analog to digital converter (ADC), a detection means and a reading means. The ADC requires the capability to acquire both the analog data from the detection signal and the received digital data from the conditioned transponder data signal and to convert the analog data to converted digital data. The detection means requires the

capability to evaluate the converted digital data to detect a transponder presence in the space surrounding the transmitting antenna. The reading means requires the capability to demodulate the conditioned transponder data signal to read the received digital data. Accordingly, it is respectfully submitted that claim 25 is allowable over the cited references for substantially the same reasons as set forth above with respect to claim 1.

Amended claim 28 is a process claim which requires a number of limitations with respect to operation of the microcontroller. In particular, claim 28 recites the steps of transmitting a detection signal from the transmitting antenna of the reader into a space surrounding said transmitting antenna. The analog to digital converter included within the microcontroller acquires the analog data from the detection signal and converts it to converted digital data. The microcontroller evaluates the converted digital data to detect a proximal transponder in the space surrounding the transmitting antenna.

Claim 28 further recites the steps of receiving the transponder data signal containing received digital data with the receiving antenna of the reader. The receiver electronics condition the transponder data signal to a conditioned transponder data signal. The analog to digital converter acquires the received digital data from the conditioned transponder data signal and the microcontroller demodulates the conditioned transponder data signal to read the received digital data.

Claims 3, 4, 11-14, 27, and 30-43 are likewise allowable as depending directly or indirectly on allowable claim 1, 25, or 28. Claims 44-46 are canceled without prejudice and are no longer at issue.

Claims 2, 26, and 29 have been rejected under 35 U.S.C. §103(a) as being unpatentably obvious over U.S. Patent 6,467,708 to Johnson in view of U.S. Patent 5,347,263 to Carroll et al. and further in view of U.S. Patent 6,367,697 to Turner et al. Claims 2, 26, and 29 are allowable as depending directly or indirectly on allowable claim 1, 25, or 28.

Claims 22-24 have been rejected under 35 U.S.C. §103(a) as being unpatentably obvious over U.S. Patent 6,467,708 to Johnson in view of U.S. Patent 5,347,263 to Carroll

et al. and further in view of U.S. Patent 6,354,468 to Riek et al. Claims 22-24 are allowable as depending directly or indirectly on allowable claim 1.

Objectionable claims 5, 6, and 8 have been amended to recite all the limitations of original claim 1. Although claims 5, 6, and 8 as filed depended on original claim 2 which in turn depended on original claim 1, it is respectfully submitted that the patentability of claims 5, 6, and 8 is not contingent on any limitations recited in original claim 2. Accordingly, the limitations of original claim 2 have been omitted from amended claims 5, 6, and 8. Nevertheless, it is respectfully submitted that amended claims 5, 6, and 8 traverse the objection and are allowable as amended. Claims 7, 9, and 10 are likewise allowable as depending directly on allowable claim 6 or 8. Objectionable claims 15-21 are likewise allowable as depending directly or indirectly on allowable claim 5 or 6.

The remaining prior art references made of record and not relied upon have been considered by applicant, but are not deemed sufficient to render the instant pending claims unpatentably obvious. The newly cited references in the Supplemental Information Disclosure Statement filed concurrently herewith disclose some additional limitations of claims 1, 25, and 28 which are not disclosed by the earlier references of record. The newly cited references, nevertheless, lack sufficient disclosure to render the present claims unpatentably obvious. For example, U.S. Patent Application Publication 2004/0256460 to Charrat discloses a detection mode for a reader at Fig. 10 and 11 and paragraphs 0083-0085, wherein analog data is acquired from a detection signal (termed an envelop pulse) and converted to digital data by an ADC distinctly separate from the downstream microcontroller MP of the reader. The microcontroller MP receives the digital data output by the ADC (DETC3) via the microcontroller input ports PT and evaluates the digital data to detect a transponder presence in the space surrounding the transmitting antenna of the reader.

Charrat, as noted above, lacks disclosure of an ADC integrated within the single-chip microcontroller. Charrat further lacks disclosure of an ADC having the capability to acquire the received digital data from the conditioned transponder data signal. Charrat still

Application No. 10/848,246
Amendment dated September 26, 2006
Reply to Office Action of June 26, 2006

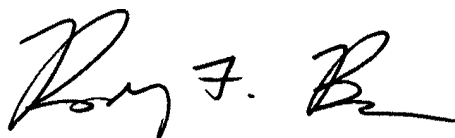
further lacks disclosure of the reading means integrated within the microcontroller having the capability to demodulate the conditioned transponder data signal to read the received digital data.

Applicant's claimed integration of the ADC within the single-chip microcontroller is not an obvious design choice to reduce the number of discrete circuit components in the reader merely for purposes of economy and simplicity. Microcontrollers in general have a relatively high level of internal digital noise. Therefore, one skilled in the art would expect the digital noise level of the microcontroller to disrupt operation of an integral ADC which could in turn undesirably reduce the operating range of the reader. As such, the current state of the art teaches the skilled artisan to design away from the present invention of *inter alia* integrating the ADC within the microcontroller.

Conclusion

In conclusion, applicant respectfully asserts that all pending claims 1-43 in the instant patent application are allowable for the reasons set forth above. Accordingly, an early notice of allowance is earnestly solicited. The Examiner is requested to call the undersigned at (858) 272-8705 for any reason that would advance the instant application to issue.

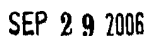
Respectfully submitted,



Rodney F. Brown
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Registration No. 30,450

3365 Baltimore Street
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Telephone: (858) 272-8705

RFB:038P0401A



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Sheet	1	of	1
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Complete if Known

Application Number	10/848,246
Filing Date	05/18/2004
First Named Inventor	Ralph W. Quan
Art Unit	2612
Examiner Name	Scott Au
Attorney Docket Number	038P0401

U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ *Number ⁴ *Kind Code ⁵ (if known)				
		GB-2305074-A	03/26/1997	Howell et al.	Fig. 6	
					p.15,I.26-p.16,I.23	

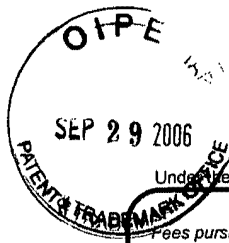
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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND

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Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL

For FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT (\$) 780

Complete if Known

Application Number	10/848,246
Filing Date	May 18, 2004
First Named Inventor	Ralph W. Quan
Examiner Name	Scott Au
Art Unit	2612
Attorney Docket No.	038P0401

METHOD OF PAYMENT (check all that apply)

☒ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☐ Deposit Account Deposit Account Number: 02-4245 Deposit Account Name: Rodney F. Brown

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee (\$)	Small Entity Fee (\$)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180
Total Claims	Extra Claims	Fee (\$)
43 - 20 or HP = 0	x	=
HP = highest number of total claims paid for, if greater than 20.		
Indep. Claims	Extra Claims	Fee (\$)
6 - 3 or HP = 3	x	= 200
HP = highest number of independent claims paid for, if greater than 3.		

3. APPLICATION SIZE FEE

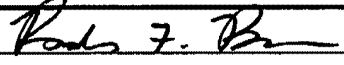
If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fee Paid (\$)
- 100 =	/ 50 =	(round up to a whole number) x	=	

4. OTHER FEE(S)

Non-English Specification, \$130 fee (no small entity discount)	
Other (e.g., late filing surcharge): Submission of Information Disclosure Statement under 1.17p	180

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 30,450	Telephone 858-272-8705
Name (Print/Type)	Rodney F. Brown		Date September 26, 2006

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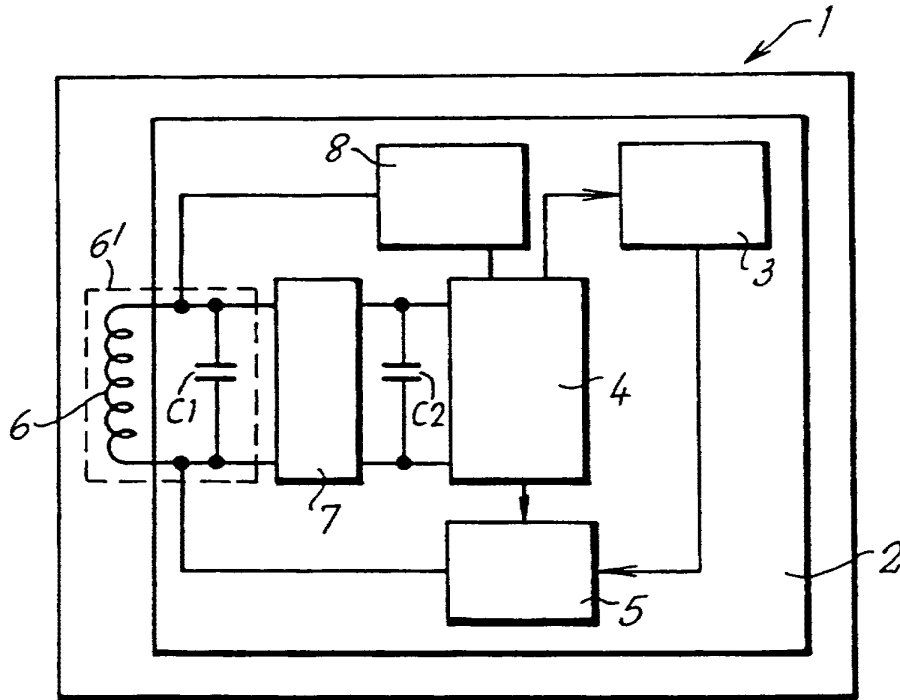


FIG. 1

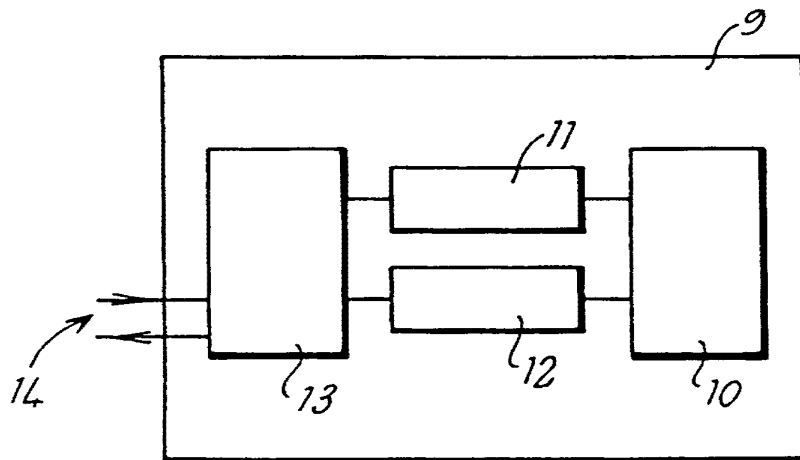
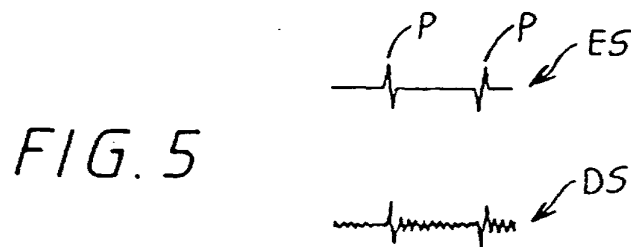
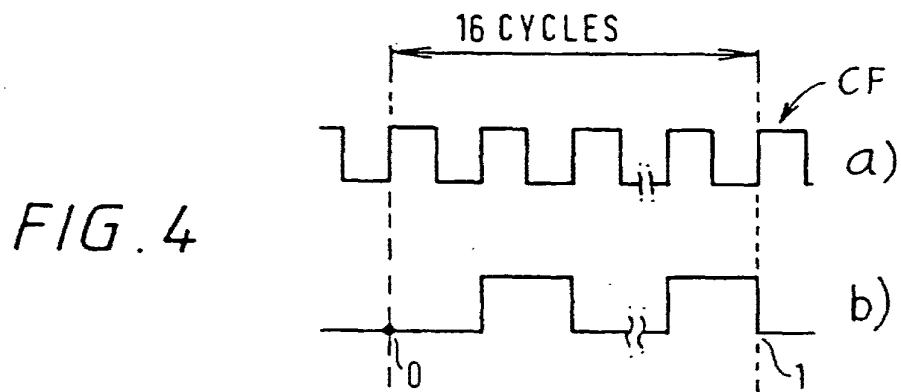
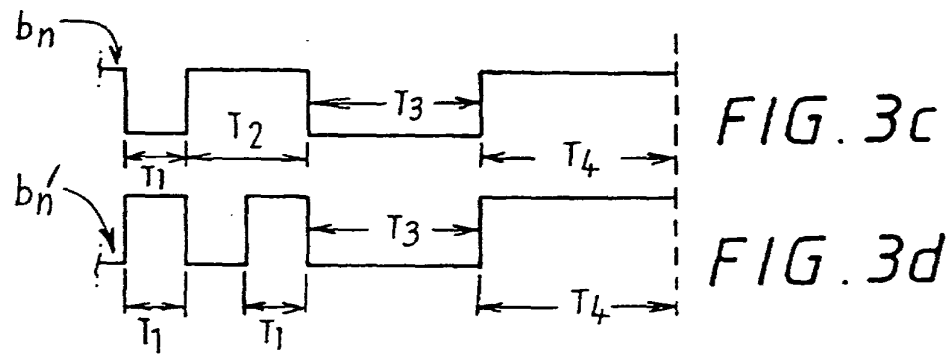
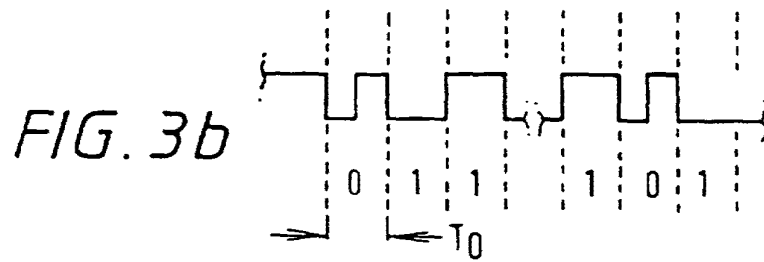
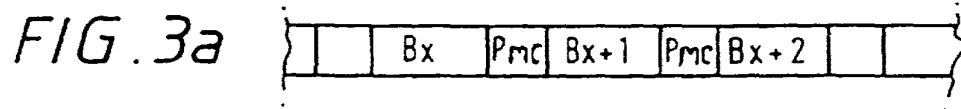
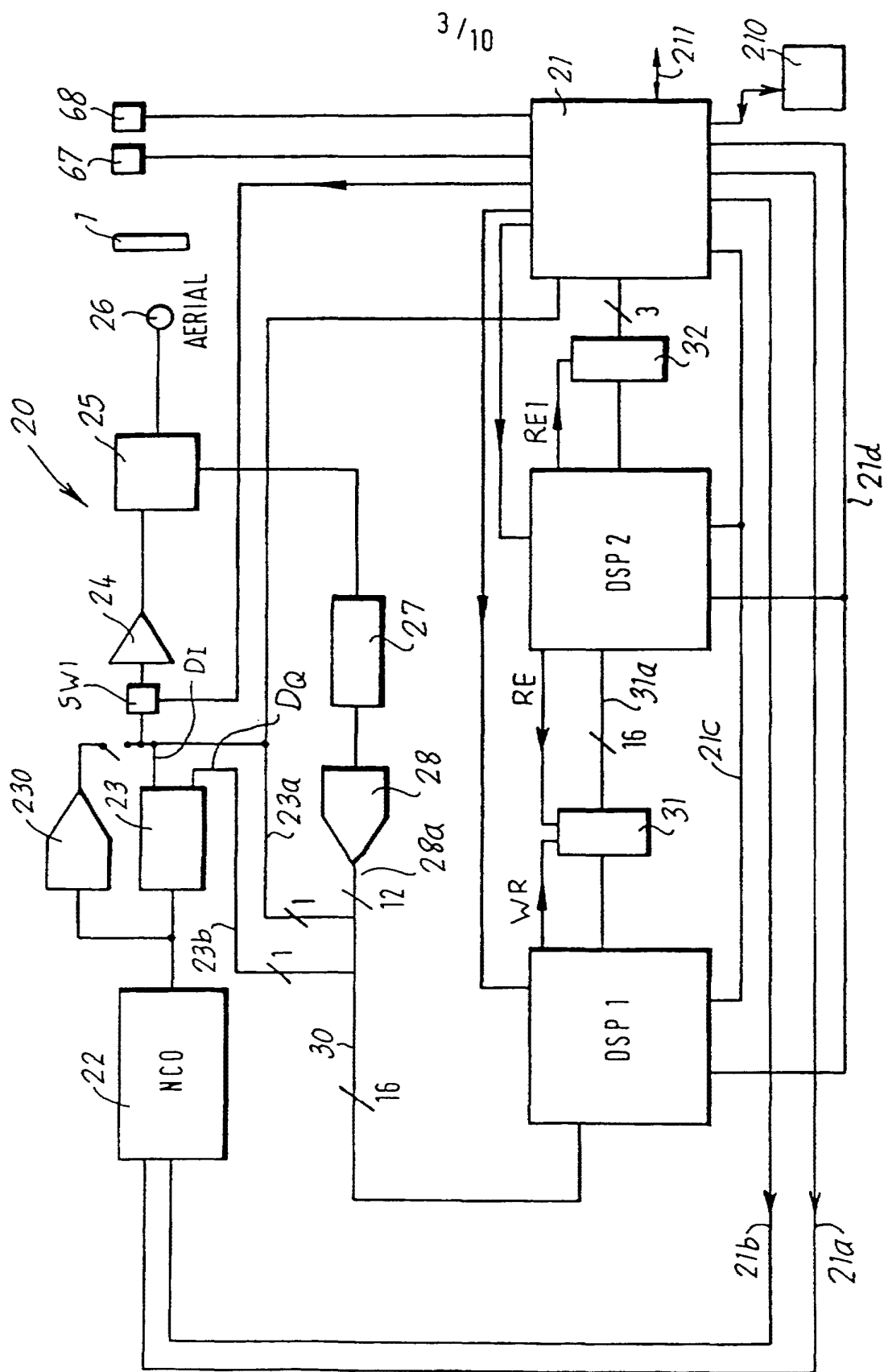
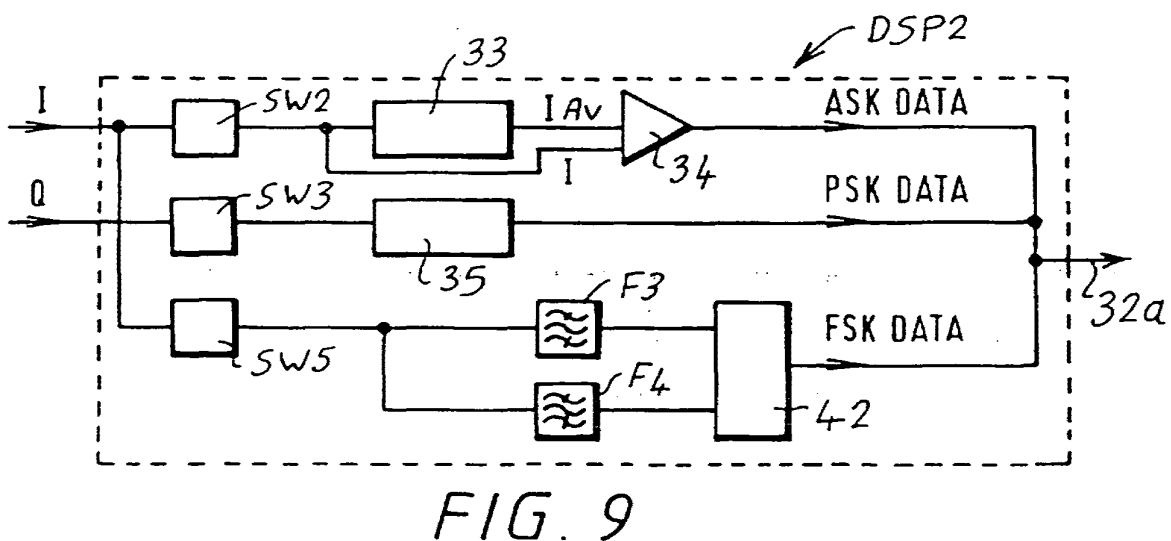
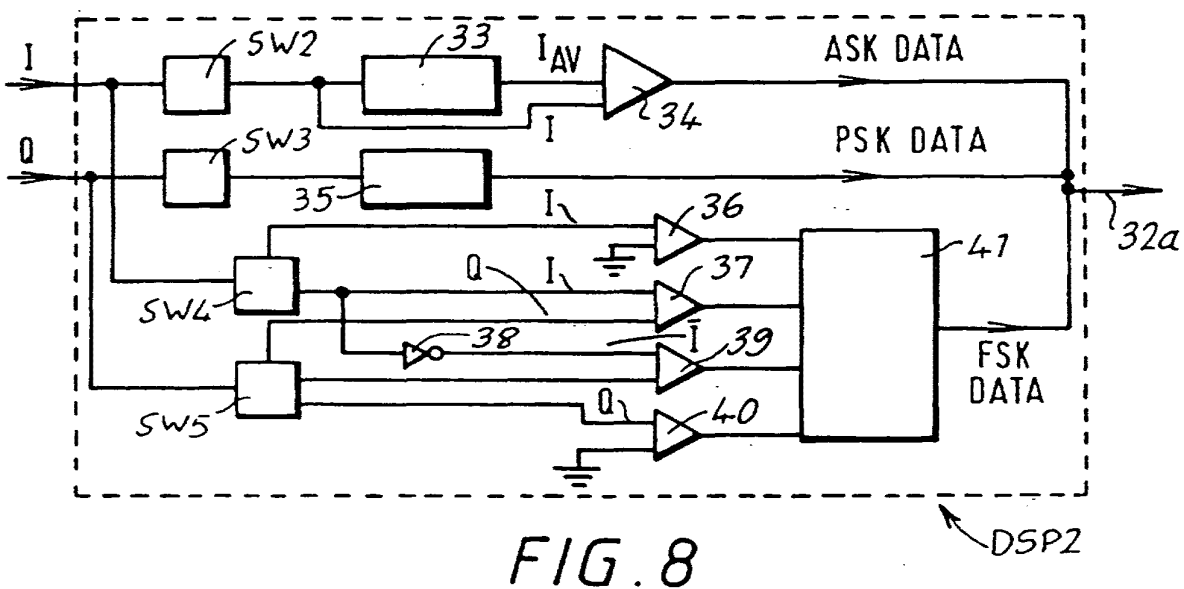
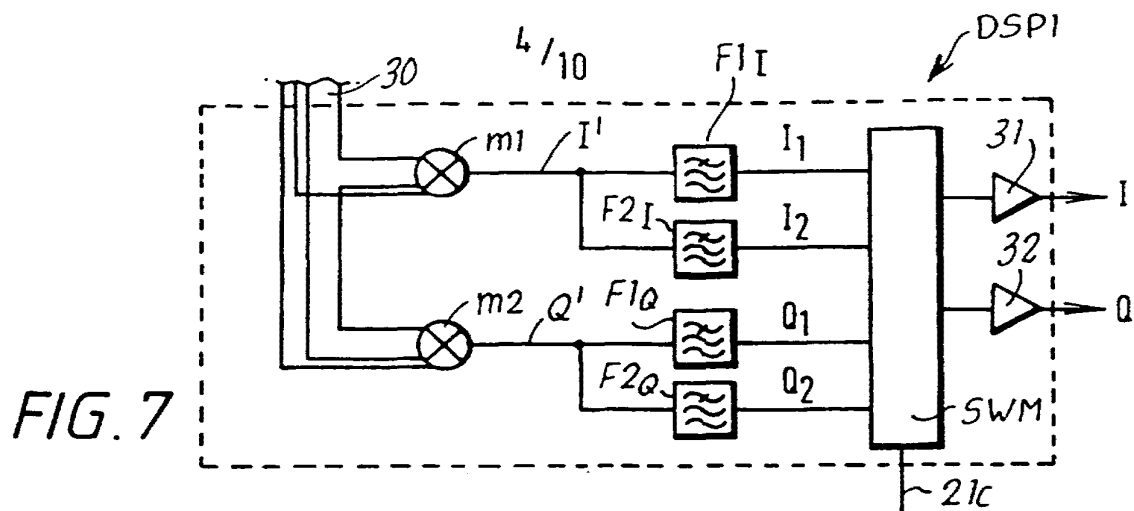
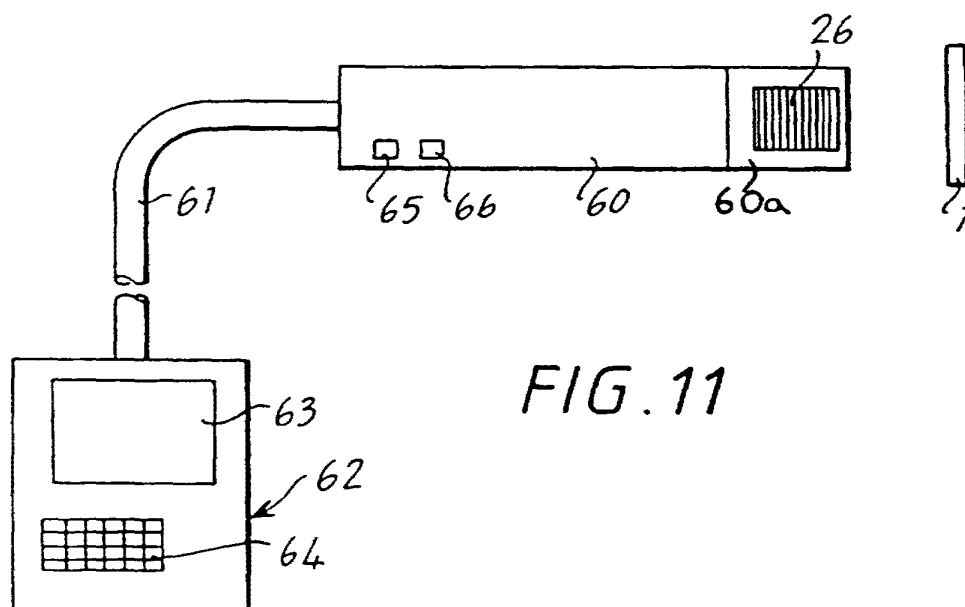
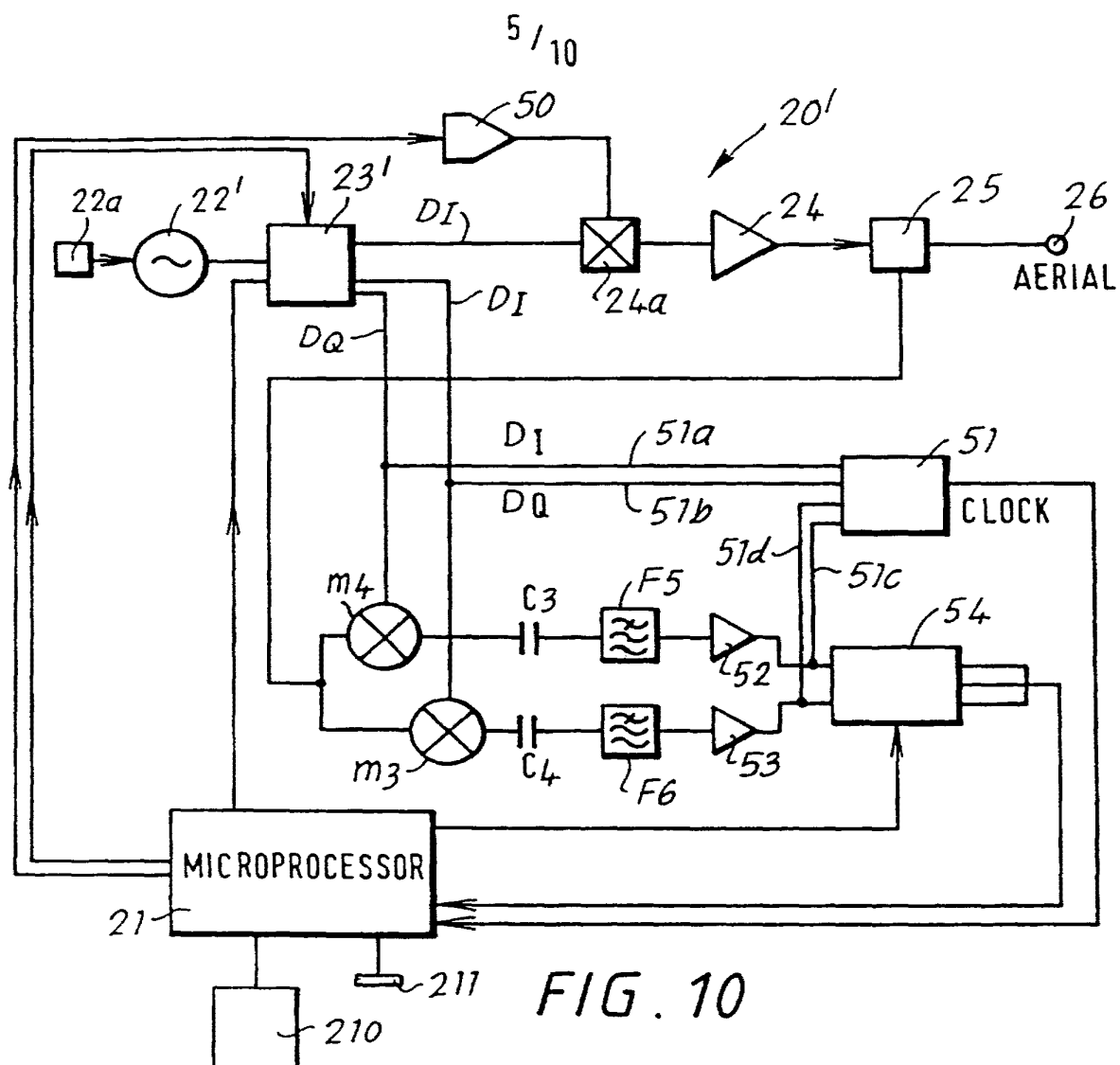


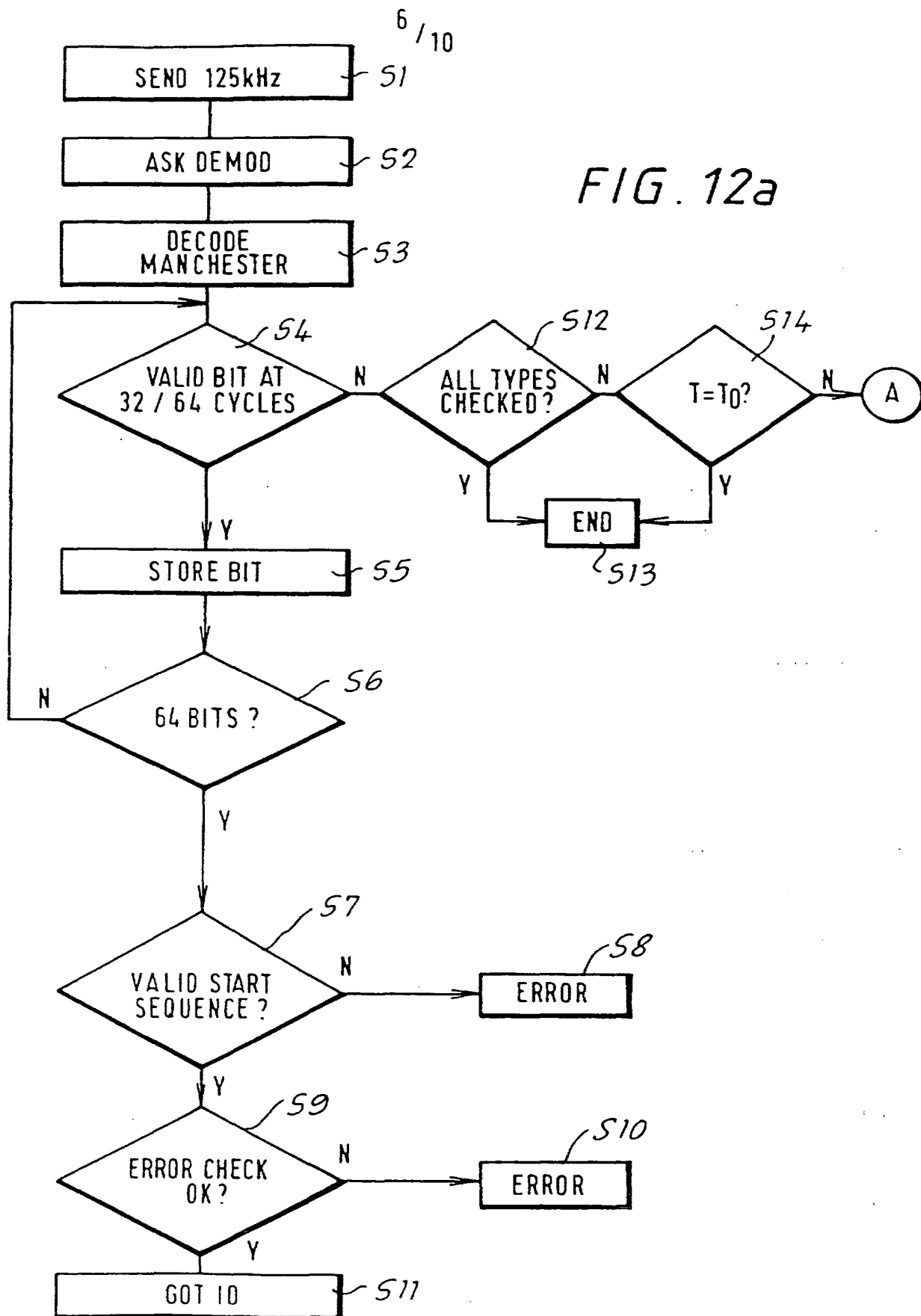
FIG. 2











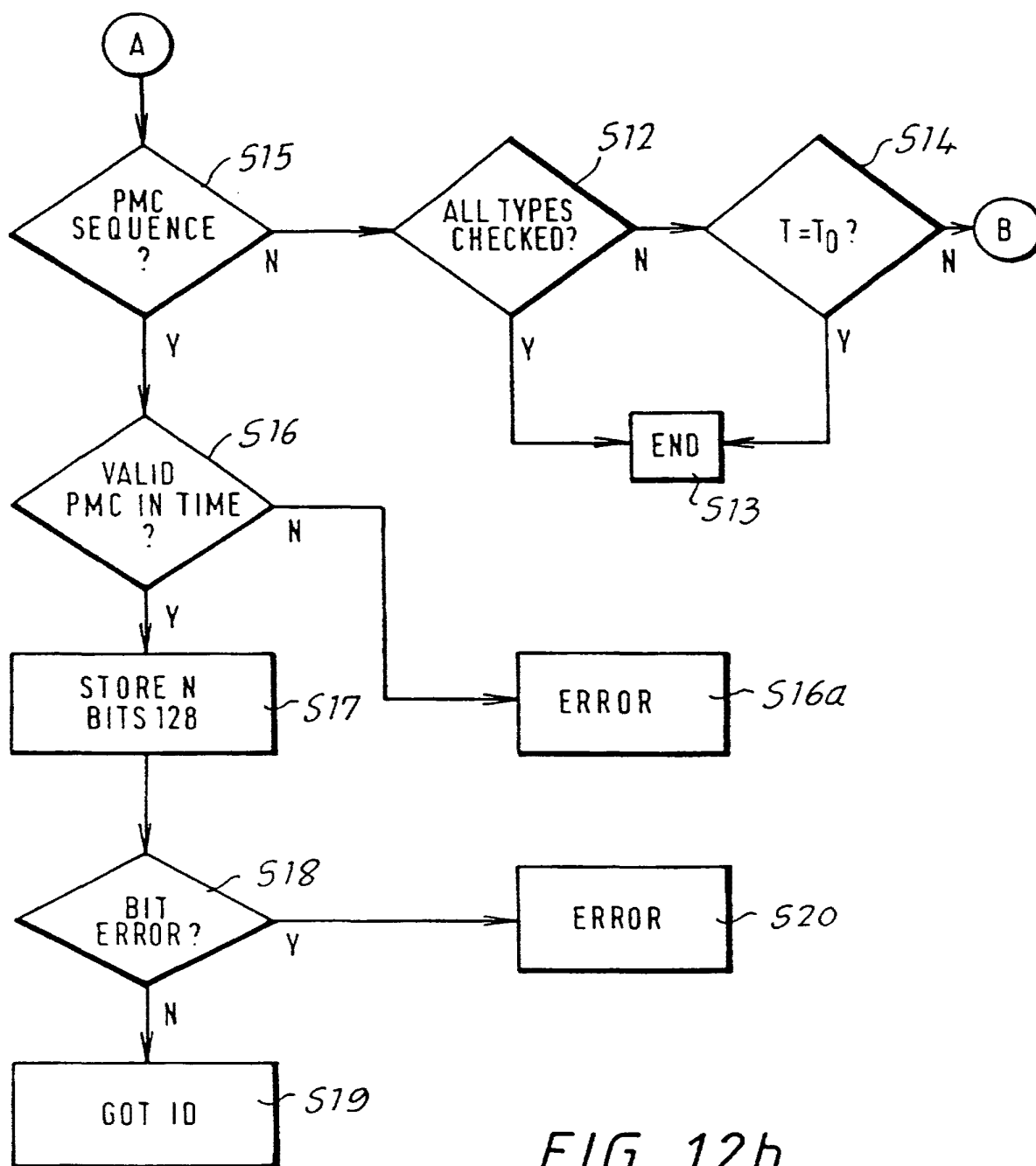


FIG. 12b

FIG. 12c

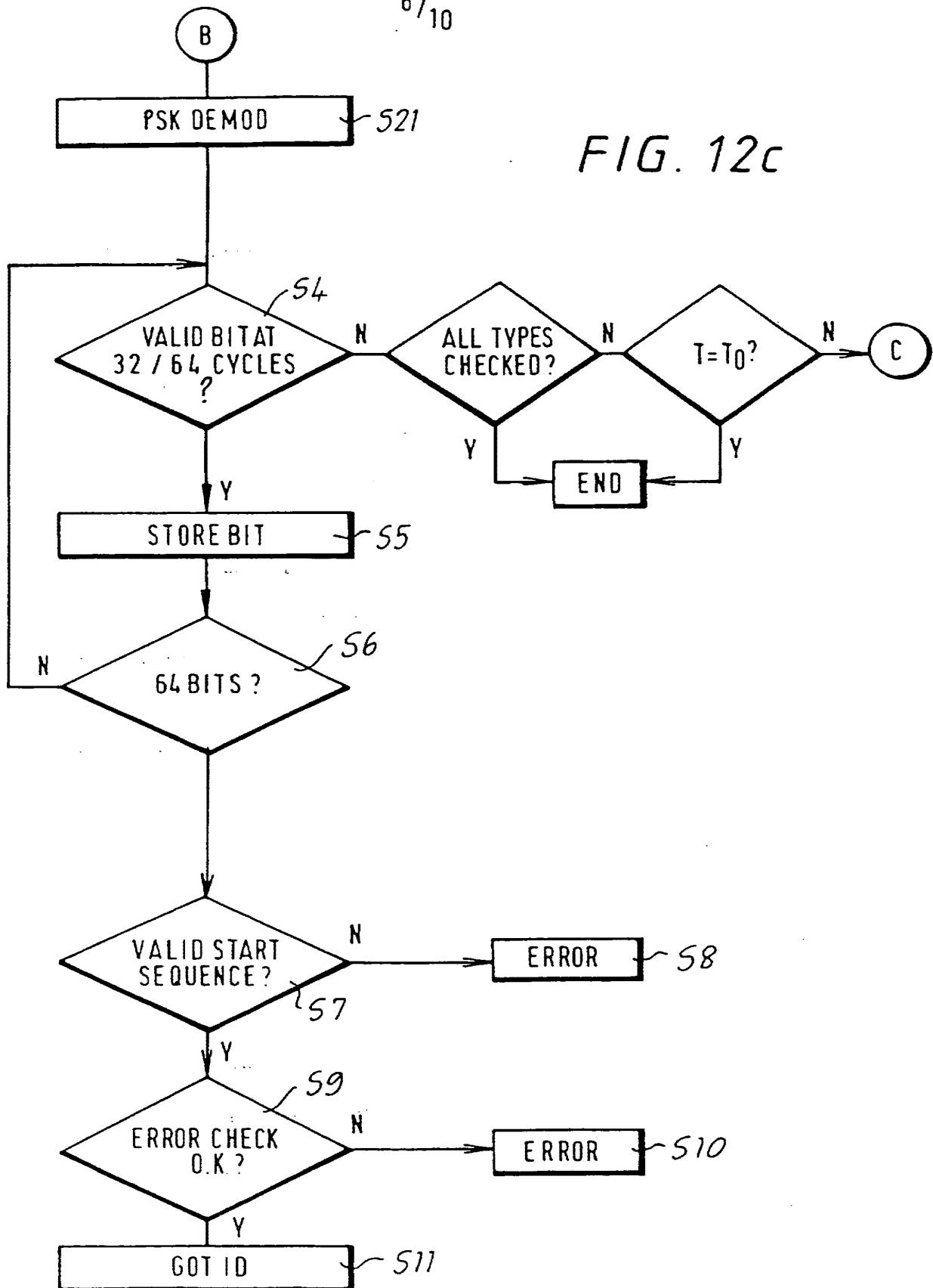
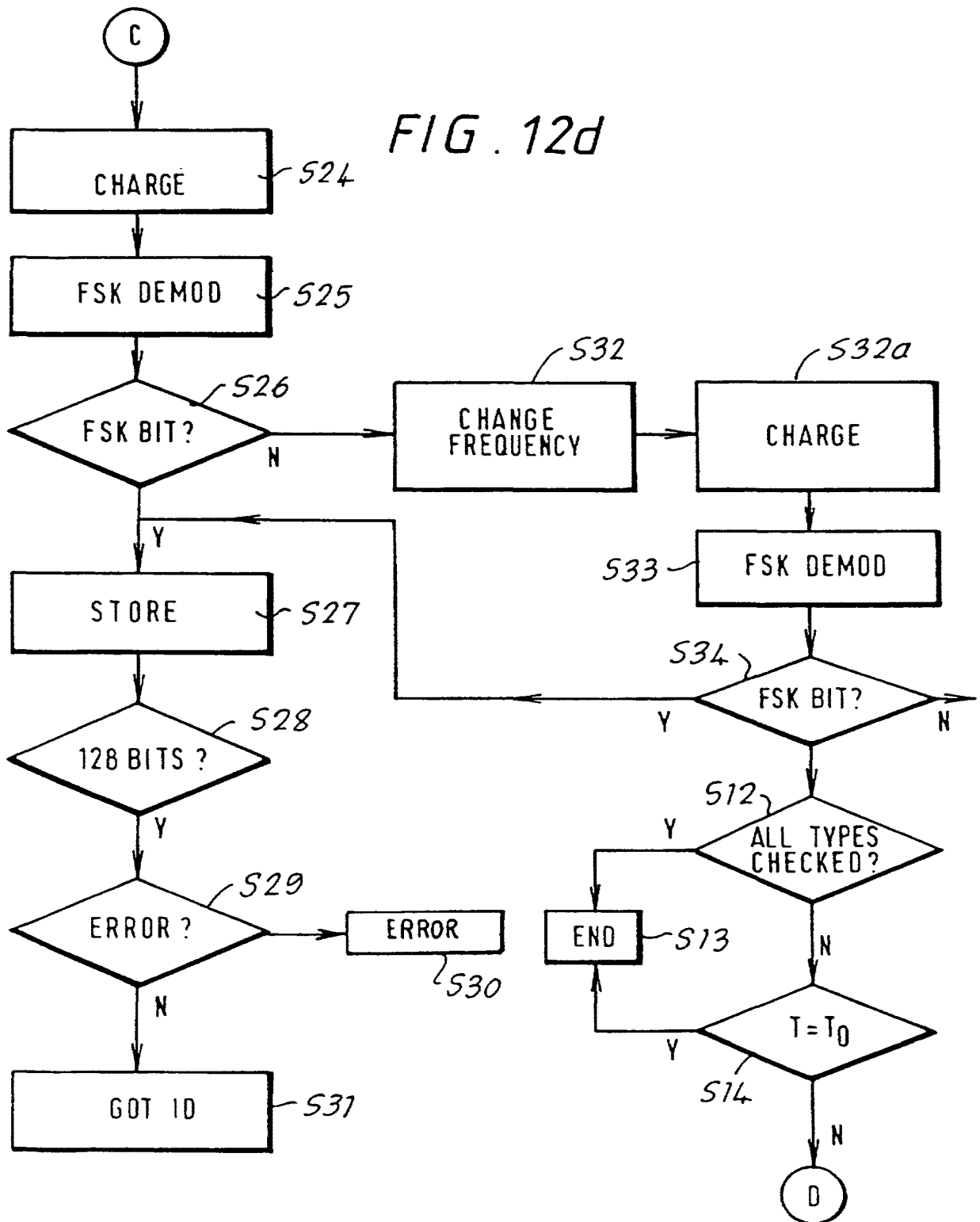


FIG. 12d



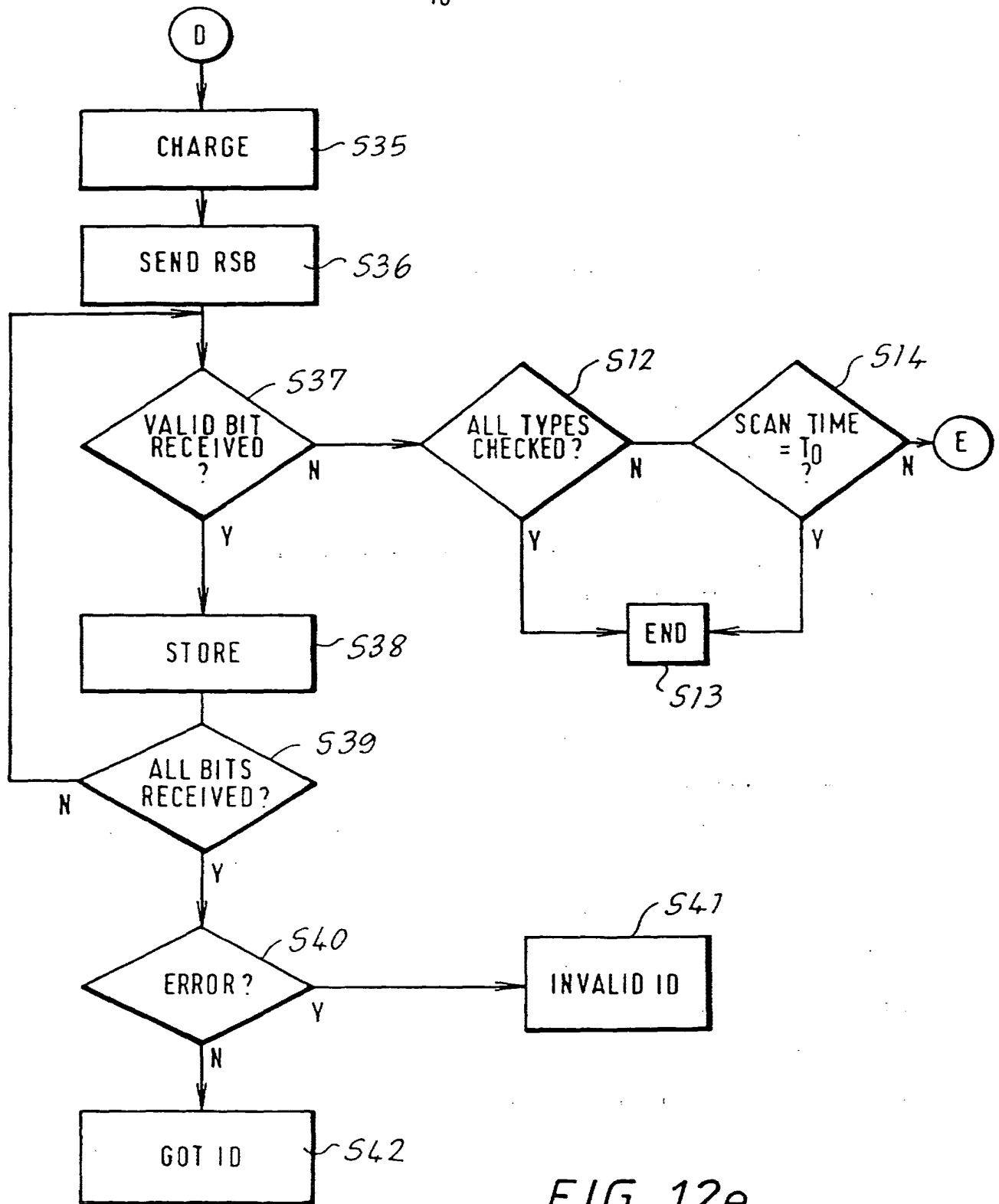


FIG. 12e

- 1 -

APPARATUS AND METHOD FOR REMOTELY READING

DATA STORAGE DEVICES

This invention relates to an apparatus and method
5 for remotely reading data storage devices.

Remotely readable data storage devices are particularly attractive for use in enabling identification and tracking of items to which the data storage devices are attached, either permanently or
10 temporarily. One recently developed system for enabling remote reading or interrogation of a data storage device is a radio frequency identification (RF/ID) system in which the data storage device is in the form of a low (LF) or high (HF) frequency tag or transponder with which
15 a reader or interrogator communicates via low frequency radio signals. These tags are passive devices (that is they have no internal power source) and rely on the interrogator or reader to supply the necessary energy to enable operation of the tag.

20 Figure 1 of the accompanying drawings illustrates a schematic block diagram of a typical example of a tag or transponder 1. The transponder 1 comprises an integrated circuit 2 which is generally formed of silicon. The integrated circuit 2 comprises a non-
25 volatile memory 3, generally a read only memory (ROM) or a non-volatile random access memory (RAM) or FRAM (ferro-electric RAM), for storing data. The memory 3 is

security purposes.

Figure 2 is a block diagram illustrating very schematically the main functional components of a reader or interrogator 9 for reading data stored in the transponder 1. The reader 9 comprises an RF antenna 10 coupled via an RF modulator 11 and a demodulator 12 to a microprocessor control unit 13 which itself may be coupled via an appropriate interface 14 (for example an RS232 interface) to a host computer (not shown). In order to enable data to be read from the tag or transponder 1, the tag or transponder 1 should be placed within a given distance of the antenna 10 of the reader 9 with its RF coil or receiver 6 in an appropriate orientation. The distance depends upon the precise characteristics of the transponder, the strength of the transmitted RF signal and the environment in which it is placed. Typically, this distance may range from about 1-2mm (millimetres) to 1-2 metres. The reader 9 transmits an RF signal of the appropriate frequency which induces an alternating current in the resonant circuit 6' (which as shown by the dashed box consists of the RF coil 6 and the capacitor C1) of the transponder 1 causing the charge storage capacitor C2 to be charged via the rectifier 7. Charging of the charge storage capacitor C2 causes the logic control unit 4 to reset itself and to initiate transmission of an RF signal carrying the data stored in the memory 3 via the modulating circuit

connected to a sequencer or logic control unit 4 which controls the reading or writing of data from the memory 3 and also controls operation of a radio frequency modulation unit 5 for modulating the data for transmission via an RF transmitter in the form of a coil 6 coupled to the integrated circuit 2. The coil 6 also forms the receiver of the transponder 1 and is generally connected to a capacitor C1 to form a parallel resonant circuit tuned to a transmission frequency of a reader compatible with the tag or transponder 1. The output of the resonant circuit 6 is coupled to a rectifier 7 which provides a rectified output for charging a charge storage capacitor C2. The charge storage capacitor C2 is coupled between the positive and negative power supply lines of the integrated circuit. The capacitors C1 and C2 may be integrated in or on the integrated circuit 2 or may be separate components. The RF coil 6 is also coupled to a clock extraction circuit 8 which extracts from an RF signal transmitted to the RF coil a clock control signal for the logic control unit 4. The transponder 1 is provided within an insulating, generally plastics or glass, encapsulation. Typically, the transponder 1 has dimensions ranging from several centimetres down to a few millimetres and may even be as small as, for example, a grain of rice. Such a transponder 1 may easily be incorporated into the packaging or outer casing of products which require identification for stocktaking or

5 and the RF coil 6 for reception by the reader antenna 10.

Currently, there is no common carrier modulation and data transmission system agreed between manufacturers for such transponders and the systems chosen by different manufacturers of tags and readers vary widely and are generally incompatible with one another. This incompatibility means that a reader made by one manufacturer for reading a particular type of tag or transponder will not normally be able to read tags or transponders manufactured by another supplier. This incompatibility is hindering the widespread adoption of the technology because, currently, it is necessary for a customer who wishes to incorporate the tags or transponders into his products to rely on a single source for the transponders and readers. Thus, if the customer's requirements subsequently change or there are commercial reasons for changing to transponders or tags available from different sources, then a severe cost penalty will be incurred in duplicating the reader hardware and software support. In addition, there are many applications for such transponders or tags where it may not be possible to predict in advance the type of tag which will be required to be read by the reader. Such applications include, for example, the identification of lost or stolen property by the police or the tracking or identification of luggage or goods in transit, for

example at airports or across borders.

According to one aspect of the present invention, there is provided apparatus for remotely reading data from a number of data storage devices such as radio
5 frequency identification transponders, which apparatus comprises means for determining the modulation system and/or data transmission system of a data storage device thereby allowing data stored by the data storage device to be read by the apparatus.

10 In another aspect, the present invention provides a method of remotely reading data from a number of data storage devices such as radio frequency identification transponders which determines the modulation system and/or data transmission system of a data storage device
15 thereby allowing data stored by different manufacturer's data storage devices to be read.

As used herein the term "data transmission system" refers to, for example, the format of the data transmission by the data storage device, that is whether,
20 for example, the data is divided into blocks of data, the relationship between the data and the carrier frequency, the actual carrier frequency and any modulation frequencies where a frequency modulation system is used, whether the data includes headers, parity check bits,
25 block separators and so on and possibly also to any encoding of the data.

Means may be provided for identifying whether the

response signal uses any one of a number of different types of carrier modulation systems by, for example, processing the response signal as if it were using a given one of the different modulation systems and then
5 deciding from the processed signal whether that modulation system was in fact used. If not, the process may be repeated. The decision as to whether a particular modulation system was used may be based on whether or not the processed signal represents a binary data stream of
10 one of the possible carrier modulation and data transmission systems, possibly after suitable decoding. Specific features of the possible data transmission systems may be looked for to enable identification of the actual data transmission system of the data storage
15 device. If no response signal has been received, a signal may be transmitted by the apparatus to the data storage device for a predetermined period to charge the data storage device to see if the data storage device is of a type which requires full charging before it can be
20 read. Also, the frequency of the transmission means may be changed if no response is received at the end of the predetermined period and a determination then made as to whether there is a response from the data storage device to the new frequency. In order to check for data storage
25 devices which require a separate exciter signal after charging, periodic exciter signal bursts may be generated if there is no response after the charging period and a

determination then made as to whether a response signal is received in response to an exciter signal burst.

The apparatus may be housed within a hand-holdable casing. A communications interface may be provided for communication with a host computer. A bar code reader
5 may be incorporated in the apparatus.

Embodiments of apparatus and a method in accordance with the present invention enable a number of different data storage devices, each using a different modulation
10 and/or data transmission system, to be interrogated and read using the response signal transmitted by the data storage device in response to an interrogation signal from the apparatus to identify the modulation and data transmission system of the data storage device and thus
15 enable retrieval of the data transmitted by the data storage device.

Embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

20 Figure 1 is a block schematic diagram of a typical radio frequency identification tag or transponder;

Figure 2 is a block schematic diagram of a typical radio frequency identification tag reader;

Figure 3a is a block schematic diagram for
25 illustrating the data format for one particular modulation and data transmission system and Figures 3b to 3d are wave form diagrams for that particular

modulation and data transmission system for enabling transmission of data from one type of radio frequency identification tag;

Figure 4 illustrates wave form diagrams for another modulation and data transmission system for transmitting data from another type of radio frequency identification tag or transponder;

Figure 5 illustrates wave form diagrams of another modulation and data transmission system for transmitting data from another type of radio frequency identification transponder;

Figure 6 shows a block schematic diagram of one example of apparatus in accordance with the invention;

Figure 7 shows a functional block diagram for illustrating the operation of a first digital signal processor of the apparatus shown in Figure 6;

Figure 8 shows a functional block diagram for illustrating the operation of one example of a second digital signal processor of the apparatus shown in Figure 6;

Figure 9 shows a functional block diagram for illustrating the operation of another example of the second digital signal processor of the apparatus shown in Figure 6;

Figure 10 shows a block diagram of another example of apparatus in accordance with the invention;

Figure 11 is a diagrammatic view of one possible

form of apparatus in accordance with the invention;

Figures 12a to 12e are flow charts for explaining the operation of an embodiment of apparatus in accordance with the invention.

5 It should, of course, be understood that the drawings are only schematic and are not to scale. Like reference numerals are used throughout to refer to like components.

Referring now to the drawings, Figures 3a to 3d
10 illustrate schematically components of the modulation and coding scheme used by Philips Semiconductors (a division of Philips Electronics NV of the Netherlands) in its PIT family of radio frequency identification tags or transponders. In the carrier modulation and data
15 transmission system shown in Figures 3a to 3d, the radio frequency identification tag or transponder is responsive to a radio frequency signal at 125kHz and transmits a response signal at the same frequency using amplitude shift key (ASK) modulation. The data is encoded by a
20 diphas coding technique as illustrated schematically in Figure 3b where the interval T_0 represents 16 cycles of the 125kHz carrier signal. As shown in Figure 3b, a binary zero is represented by a change of phase half way through the interval T_0 while a binary 1 is represented
25 by no change of phase within the interval T_0 . The data is transmitted in blocks B_x , B_{x+1} , B_{x+2} etc. separated by

program mode check (PMC) sections. Each of the PMC sections incorporates a unique PMC code. There are two types of PMC code depending on whether the last bit of the previous block was of high or low amplitude. Figure 3c shows the situation where the last bit b_n of the previous block ended on a high amplitude. In this case, the PMC code is low for a period T_1 representing 16 cycles of the carrier frequency, is then high for a period T_2 representing 32 cycles of the carrier frequency is then low for a period T_3 representing 128 cycles of the carrier frequency and is then high for a period T_4 representing $127 + 16$ cycles of the carrier frequency. As shown in Figure 3d, where the last bit b'_n is or terminates on a low amplitude, the PMC code is high for a period T_1 , then low for a period T_1 , high again for a period T_1 , then low for a period T_3 and high again for the period T_4 .

The H4000 ASK family of radio frequency identification transponders manufactured by the Swiss company EM Microelectronic Marin SA also uses an ASK modulation system with a carrier frequency of 125kHz. In this case, however, each bit of the data stream is represented by 64 cycles of the carrier frequency and the data is encoded using Manchester coding so that a logical 1 is represented by modulating the amplitude of the 64 cycles representing the bit so that the amplitude is high

for 32 cycles and then low for 32 cycles and a logical zero is represented by modulating the carrier frequency so that the amplitude is low for 32 cycles and then high for 32 cycles.

5 The H4000 PSK series of transponders manufactured by EM Microelectronic Marin SA also uses 125kHz carrier frequency but uses a phase shift key (PSK) modulation scheme rather than an ASK modulation scheme. Figure 4 shows wave forms illustrating this modulation scheme.

10 In this case, a bit of the data stream is represented by 16 cycles of the carrier frequency CF shown as waveform a in Figure 4. A 180° change in phase at the end of the 16 cycle period represents, as shown, at b in Figure 4, a logical zero while no change in phase at the end of the

15 16 cycles represents a logical 1.

 In the EM Microelectronic Marin SA modulation and coding systems, the data is represented as 64 bits with a 9 bit header consisting only of logical ones and 40 bits of data arranged as ten columns and four rows with

20 ten row parity check bits, four column parity check bits and one stop bit.

 AEG of Germany also produce two families of radio frequency identification (RF/ID) transponders, using 180° PSK and ASK modulation respectively, with the ASK version

25 adopting a Manchester coding system. AEG use a similar scheme data coding to the above-described EM Microelectronic Marin SA system.

Texas Instruments of the United States use a different modulation and coding system which operates on a frequency shift key (FSK) modulation scheme. In this case, the transponder responds to the reader or
5 interrogator only when the transponder detects that its charge storage capacitor has been fully charged. Typically, this takes from 15 to 50 milliseconds. Once the charge storage capacitor has been charged, the transponder transmits its data using a frequency of
10 typically 123.2kHz to represent a logical zero and typically 134.4kHz to represent a logical 1. Each bit is represented by 16 cycles and the identification code carried by the transponder is a 64 bit identification (ID) plus an error check code.

15 Another transponder which uses an FSK modulation system is manufactured by the Finnish company IDESCO. The data communication system used by this transponder differs from those discussed above in that the transponder must first be charged and then requires a
20 separate exciter signal to be supplied by the reader or interrogator before it will transmit its data. Figure 5a shows the exciter signal ES which consists of a, generally, eight microsecond pulse P which is repeated every 50 microseconds with a 180° phase change in the
25 carrier signal every other pulse. The 180° phase change in the pulse instructs the transponder to send the part of the data bit. Each data bit is thus represented by

a signal supplied by the transponder in response to each of two successive exciter pulses. A logical 1 is represented by a high frequency (300kHz) response to one exciter pulse followed by a low frequency (250kHz) response to the next exciter pulse while a logical zero is represented by a low frequency response to one exciter pulse followed by a high frequency response to the next exciter pulse. The data may be provided as a 64 or 256 bit stream. Figure 5b illustrates part of a data signal DS. The same number of cycles of the high and the low frequency modulation is provided.

Figure 6 illustrates one example of apparatus 20 in accordance with the present invention which is capable of reading at least the transponders described above with reference to Figures 3 to 5.

As shown in Figure 6 the apparatus 20 comprises a microprocessor or microcontroller 21 with associated memory 210 (for example ROM and/or RAM) which controls the overall operation of the apparatus and stores information relating to the carrier modulation and data transmission systems of the various tags or transponders which the apparatus is designed to read.

The apparatus 20 comprises a numerically controlled oscillator (NCO) 22 which, under the control of the microprocessor 21, outputs a digital signal which has a frequency four times that of the desired carrier frequency. The output of the NCO 22 is supplied to a

programmable logic device or scaler 23 which has first and second outputs D_I and D_Q . The first output D_I is a binary digital signal which changes state (i.e. changes between 0 and 1) at the leading (or trailing) edge of every fourth pulse from the NCO 22 to provide a digital binary signal of the required carrier frequency. The second output D_Q of the scaler 23 similarly changes state at the same frequency. However, the change of state of the output D_Q is 90° out of phase with the output D_I , that is the second output D_Q changes phase on the leading (or trailing) edges of the first, fifth, ninth, etc. output pulses from the NCO 22. The outputs D_I and D_Q are supplied by respective one bit data buses 23a and 23b to a 16 bit data bus 30. The data bus 23a is also coupled to the microprocessor to provide to the microprocessor a signal representing the clock frequency of the tag or transponder. The output D_I of the scaler 23 is also supplied via a switch SW1 to a power amplifier 24 which is coupled via an RF directional coupler 25 to an RF antenna 26.

The antenna 26 may comprise a single RF coil with an inductance of, typically, 186 milli Henrys. Although not shown, as another possibility, the antenna 26 may consist of a number of RF coils (which may be provided by connecting tap points to a single coil) with the particular coil or combination of coils being selected

by switches controlled by the microprocessor 21. This enables the RF coil characteristics to be optimised for transmission of signals to and reception of signals from different transponders or tags 1.

5 The power amplifier 24 and RF antenna 26 provide a resonant circuit for generating an RF sinusoidal signal from the binary digital signal supplied via the scaler 23. As an alternative to using the scaler 23 to provide the RF signal for transmission by the transmitter 26, a
10 digital to RF converter 230 may be coupled between the NCO 22 and the switch SW1 to convert the digital output signal from the NCO 22 into an RF sinusoidal signal of a quarter the frequency.

 As indicated above, the actual frequency supplied
15 by the NCO 22 is controlled by the microprocessor 21 via data and clock lines 21a and 21b. The microprocessor 21 may also enable switching on or off of the NCO for power saving reasons.

 The RF directional coupler 25 prevents, as is known
20 in the art, an RF signal received by the antenna 26 from being supplied back to the power amplifier 24. This enables the same antenna 26 to be used for both transmission and reception of RF signals. Of course, if desired, separate transmission and reception aerials
25 could be provided.

 An RF signal received via the antenna 26 is supplied via the directional coupler 25 to an analog-to-digital

converter (ADC) 28 via a conditioning circuit 27 which comprises conventional filters for removing noise components from the received RF signals. The analog-to-digital converter (ADC) 28 has a 12 bit parallel output data bus 28a which is coupled to the 16 bit parallel data bus 30 with the one bit data buses 23a and 23b. The data bus 30 is coupled to the input of a first digital signal processing unit DSP1. As will be explained below, the first DSP1 serves to mix or multiply each of the binary digital output signals D_I and D_Q with the data carrying digital output signal of the ADC 28 to provide an in-phase data carrying signal I and a quadrature out-of-phase data carrying signal Q. The data carrying digital signals I and Q are supplied one after another to a first latch or FIFO buffer 31 which is coupled via a 16 parallel bit data bus 31a to a second digital signal processor DSP2 which, as will be explained below, affects appropriate demodulation processing of the I and Q data carrier signals to enable data extraction. The output of DSP2 is coupled via a second latch 32 to the microprocessor 21. Typically, the DSPs may be TMS 320C 52 or possibly TMS 320C 25 DSPs produced by Texas Instruments.

Figure 7 is a functional block diagram for explaining the operation of the DSP1.

As shown in Figure 7, the 16 bit parallel data bus 30 is divided upon input into the DSP1 so that the 12 bit

data carrying digital signal from the DAC 28 is mixed by the in-phase binary digital signal D_I and the quadrature out-of-phase binary digital signal D_Q , respectively. This process is illustrated by mixers M1 and M2 in Figure 7. The mixing process represented by the mixer M1 provides an in-phase data carrying signal I' while the mixing process illustrated by the mixer M2 provides a quadrature out-of-phase data carrying signal Q' . The data carrying signals I' and Q' are then low-pass filtered by finite impulse response filter functions of the DSP1 which are designed to remove the carrier frequency and would, in the absence of any data signal, output a signal of constant amplitude representing the amplitude of the carrier frequency. Although the filter functions applied to each of the signals I' and Q' will be the same, the particular filter required to remove the carrier frequency may depend upon the particular type of transponder being read. For this reason, Figure 7 shows each of the signals I' and Q' as being coupled to the input of two low-pass filters $F1_I$ and $F2_I$ for the signal I' and $F1_Q$ and $F2_Q$ for the signal Q' . The filters produce output signals I_1 , I_2 , Q_1 and Q_2 which are selectable under the control of signals input to the DSP1 via a control line 21c of the microprocessor. This function of the DSP1 is represented by a multiplexing switch SWM in Figure 7 which provides, via amplifiers 31

and 32, an in-phase data carrying signal I and a quadrature out-of-phase data carrying signal Q selected from the signals I_1 and I_2 and Q_1 and Q_2 , respectively.

As explained above, the in-phase and quadrature out-of-phase signals I and Q are supplied one after another via the latch 31 to the second DSP2. The latch 31 is provided to control the data flow rate between DSP1 and DSP2 to enable DSP2 to carry out its data processing. If, however, the DSP2 is capable of operating sufficiently quickly, then it may be possible to dispense with the latch 31. The flow of data between DSP1 and DSP2 and the microprocessor 20 may also be controlled by signals from the microprocessor on line 21d.

The DSP2 is programmed to extract the data from the in-phase and quadrature out-of-phase data carrying signals I and Q and to provide the microprocessor, via the latch 32, with a demodulated digital data stream of noughts and ones which the microprocessor can then identify or decode as will be described below with reference to Figure 12.

Figure 8 is a block diagram for illustrating one way in which the DSP2 may be programmed so as to obtain the raw binary data (which may or may not be coded) from the in-phase and quadrature out-of-phase data carrying signals I and Q which may be ASK, PSK or FSK modulated. The DSP2 carries out different data extraction routines depending upon whether the incoming data carrying signals

are assumed to be ASK, PSK or FSK modulated. Selection of the data extraction routine of the DSP2 is under microprocessor control via the control line 21c and this is illustrated functionally in Figure 8 by means of
5 microprocessor-controlled switches SW2 to SW5 which control supply of the input data carrying signals I and Q to the various data extraction routines of the DSP2.

In order to extract the raw binary data from an ASK modulated data carrying signal, the DSP2 performs a
10 running average (over, for example, 50 milliseconds) of the in-phase data carrying signal I (as illustrated functionally in Figure 8 by the averaging circuit 33) to provide an average signal I_{AV} . The DSP2 then compares this average signal I_{AV} with each bit of the input in-
15 phase data carrying signal I as represented by the comparator 34 in Figure 8 and provides an output signal which is 1 when the bit of the input data carrying signal I is greater than the average I_{AV} and is zero when the bit of the input data carrying signal I is smaller than
20 the average I_{AV} . The average I_{AV} is constantly updated by the DSP2 and a hysteresis circuit is included so as to avoid hunting or cycling. ASK demodulated data is output on output line 32a to the latch or FIFO buffer 32 for supply to the microprocessor. As another possibility,
25 the DSP2 may also perform the averaging and comparison steps on the quadrature out-of-phase data carrying signal

Q to provide the ASK demodulated binary data. This may be done additionally or in place of the processing of the in-phase data carrying signal I. If the averaging and subsequent comparison are carried out on both the in-phase and the quadrature out-of-phase data carrying signals I and Q, the DSP2 may then select whichever of the two ASK demodulated binary data streams is less noisy or otherwise provides the stronger signal or may vectorally add them.

Where the modulation used to transmit the data is the 180° PSK system discussed above with reference to Figure 4, then the effect of mixing the output of the ADC 28 with the quadrature out-of-phase digital signal D_Q is to provide a signal which goes positive or negative depending upon whether the PSK modulated carrier undergoes a 180° phase shift or not. The raw binary data can therefore be derived from the quadrature out-of-phase data carrying signal Q simply by appropriate threshold and level detecting as indicated by the circuit 35 in Figure 8 to provide an output which is 0 when the quadrature out-of-phase data carrying signal Q is high and 1 when the quadrature out-of-phase data carrying signal is low. Again, the PSK demodulated binary data is supplied from the DSP2 to the latch 32 on output line 32a. The in-phase data carrying signal I could also be used to extract PSK modulated data but is less sensitive

because the signal changes only between zero and a positive value in accordance with the PSK modulated data.

Figure 8 illustrates by functional components one possible data extraction routine which may be used by the DSP2 to demodulate FSK modulated data. As discussed above, in the FSK modulated data, zeros and ones are represented by different frequency modulations of the carrier signals. Where the carrier signal frequency is intermediate to modulation frequencies or, as will be described below, the frequency supplied by the scaler 23 for mixing with the output of the ADC 28 is adjusted so as to be between the two modulation frequencies, then the fact that the phase difference between the carrier frequency and the higher modulation frequency will change in one direction with time whereas the phase difference between the carrier frequency and the lower frequency modulation signal will change in the other direction with time means that the modulation frequency can be detected by determining the direction of phase change in the I and Q data carrier signals. Thus, by comparing, as indicated functionally in Figure 8 by the comparators 36 and 40, the amplitudes of the in-phase and quadrature data carrying signals I and Q with zero (indicated by the earth or ground symbols in Figure 8) output signals can be obtained which increase or decrease with time depending upon the direction in which the phase is changing. To increase the accuracy of this approach, the

in-phase data carrying signal may be compared with the quadrature data carrying signal as illustrated by the comparator 37 in Figure 8 and the inverted (as indicated functionally in Figure 8 by the inverter 38) in-phase data carrying signal $\bar{I}$ may be compared with the quadrature out-of-phase data carrying signal Q as indicated by the comparator 39. The results of these comparisons are used by the DSP2 to determine whether the phase is increasing or decreasing with time and so to determine whether the modulation frequency is higher or lower than the carrier frequency. DSP2 outputs a logical 1 when the modulation frequency is higher than the carrier frequency and a logical zero when the modulation frequency is lower than the carrier frequency. This function is illustrated in Figure 8 by logic circuitry 41.

Figure 9 illustrates a functional block diagram for illustrating different possible data extraction processes for the DSP2. The functional block diagram shown in Figure 9 differs from that shown in Figure 8 only in respect of the data processing routine used to extract the FSK binary data. In the example shown in Figure 8, when the microprocessor 21 instructs the DSP2 to carry out FSK modulated data extraction, the in-phase data carrying signal I is supplied to two band pass filters $F3$ and $F4$ which may be implemented using Goetzal's algorithm in the DSP2. The filters $F3$ and $F4$ each pass

one of the two modulation frequencies. The DSP2 outputs, as indicated by logic circuitry 42 in Figure 9, a logical zero when there is an output from one of the filters F3 and F2 and a logical 1 when there is an output from the other of the filters F3 and F4. Although this approach
5 may be simpler in terms of processing complexity than the arrangements shown in Figure 8, it does require that the filters F3 and F4 have narrow well-defined band pass regions.

10 In the example described above with reference to Figures 6 to 7, the apparatus is implemented as a digital circuit. It is, however, possible to implement at least some of the components of the apparatus as analog circuits. Figure 10 is a block diagram illustrating
15 apparatus embodying the invention which is implemented at least in part by analog circuits.

As shown in Figure 10, in this example the apparatus
20' comprises a conventional voltage controlled tunable oscillator 22' in which the operating frequency is
20 controlled by voltage variable capacitors (varactors) with the voltages applied to the varactors from a controllable voltage source 22a being controlled by the microprocessor 21. The output of the oscillator 22' is
25 applied to a digital signal processor 23' which performs similar functions to the scaler 23 in the apparatus shown in Figure 6. Thus, the oscillator 22' is controlled to provide a frequency four times that of the desired

carrier frequency and the digital processor 23' provides the in-phase and quadrature out-of-phase digital signals D_I and D_Q at the carrier frequency. The in-phase digital signal D_I is supplied via a variable gain amplifier stage 5 24a to the power amplifier 24 as in Figure 6. The gain of the variable gain amplifier stage 24a may be controlled by a digital-to-analog converter 50 which is controlled by the microprocessor 21. The variable gain amplifier stage 24a may be used to boost or reduce the 10 power of the carrier frequency signal if the microprocessor determines that a tag or transponder is not responding correctly.

As in the example described with reference to Figure 6, the output of the power amplifier 24 is supplied to 15 the RF antenna 26 via an RF directional coupler 25. When an incoming data carrying RF signal is received by the antenna 26, the directional coupler 25 supplies the data carrying signal to each of first and second mixers M3 and M4. The first mixer M3 also receives the in-phase 20 digital signal D_I while the second mixer M4 also receives the quadrature out-of-phase digital signal D_Q . In this example, the mixers M3 and M4 may be in the form of comparators or differential amplifiers with one of the positive and negative inputs of each comparator receiving 25 the data carrying RF signal from the antenna 26 and the other receiving the appropriate one of the digital

signals D_I and D_Q . The outputs of the mixers M3 and M4 are supplied to respective programmable filters F5 and F6 via decoupling capacitors C3 and C4 which act to remove reader transmit signal leakage appearing as DC at the output of the mixers. Although not described above with reference to Figures 6 to 9, the DSP1 may include functions analogous to the decoupling capacitors C3 and C4. The filters F5 and F6 are arranged to pass the modulated data without the carrier signal. That is, if no data were present on the signal received by the antenna 26, the outputs of the band-pass filters F5 and F6 would have a constant level dependent upon the amplitude of the carrier. Although not shown in Figure 10, as in the example described with reference to Figure 6, each of the filters F5 and F6 may comprise a number of separate individual filters with the actual filters used to filter the outputs of the mixers M3 and M4 being determined in accordance with instructions from the microprocessor 21. The outputs of the filters F5 and F6 are supplied via amplifiers 52 and 53 to a data extraction circuit 54. The data extraction circuit may comprise respective analog-to-digital converters (not shown) for the outputs of the amplifiers 52 and 53 together with a digital signal processor similar to the DSP2 shown in Figures 6 and 8 or 9.

The binary in-phase and quadrature out-of-phase signals D_I and D_Q and the in-phase and quadrature out-of-

phase data carrying signals I and Q may also be supplied on respective lines 51a, 51b, 51c and 51d to a clock extraction circuit 51 which is in the form of a digital signal processor which determines from these signals the clock frequency of the transponder 1. This circuit may, although not shown, also be provided in the apparatus shown in Figure 6. The clock extraction circuit 51 is generally not needed except in the cases of transponders such as the Texas family of TIRIS transponders in which the clock frequency changes with the high and low frequency modulation so as to enable the high and low frequency modulation sections of a bit each to consist of the same number of cycles.

The apparatus 20 shown in Figure 6 or the apparatus 20' shown in Figure 10 would generally be mounted onto a single printed circuit board using surface mounted components where available.

The apparatus may, as shown in Figure 11, be mounted in a compact plastics case 60 which, as shown in Figure 11, is preferably in the form of a tube so that the apparatus can be handled conveniently. Indeed, the apparatus 20 may, as illustrated schematically in Figure 6, be provided with a light emitting device (generally a laser) 67 and a photosensitive device 68 to enable, by incorporation of suitable software into the microprocessor's programming, the apparatus also to be used to read conventional bar codes. The bar code

reading may be carried out simultaneously with the RF tag reading by using time share processing or an interrupt protocol, for example.

The microprocessor or microcontroller is provided
5 with a serial interface 211 generally an RS232 interface. Power supply to the apparatus and connection of serial data to the RS232 interface is by way of a flexible cable
61 coupling the apparatus to a commercially available portable computer for example a laptop or palmtop
10 personal computer or a portable data terminal (that is a small hand held computer which has been made rugged for use in industrial environments) such as a Psion organiser
62 with a liquid crystal or similar display screen 63 and an input or input devices in the form of a keyboard 64
15 and possibly also a track ball or similar pointing device. Such an arrangement allows the apparatus to be fully portable enabling it to be moved to the location of the tag or transponders to be identified. This should be of particular advantage where, for example, it is
20 necessary to check the tags or transponders carried by a large consignment of goods or to check the tags or transponders of heavy or bulky items which are difficult to move.

Of course, the apparatus may be connected via the
25 RS232 interface to other suitable host computers, for example a desktop personal computer in appropriate circumstances. Also, the apparatus may be built into a

portal or like device through which a conveying belt carrying items to be identified or luggage to be checked passes.

As shown in Figure 11, the antenna 26 of the apparatus is provided at one end of the housing 60 and might be of any suitable conventional design. In addition, the housing 60 carries a green LED 65 and a red LED 66, both of which are actuable by the microprocessor. The green LED is designed to be lit to indicate that power is being supplied to the apparatus 1 while the red LED may be illuminated to indicate that a tag has been read. One or both of the LEDs or a separate LED may be actuated or caused to flash by the microprocessor 21 in the event of a fault condition such as a short or open circuit in the antenna.

The portion 60a of the housing carrying the antenna 26 is detachable and may be replaced by an electrically equivalent antenna of smaller physical dimensions to allow more versatile searching in confined spaces.

In use of the apparatus shown in Figure 11, a tag or transponder 1 to be read and the antenna 26 should be positioned so as to be a maximum distance of 50mm apart where the tag has a nominal diameter of 25mm. The wand is designed so that optimum coupling should occur when, in the case of a disk-like tag, the major surfaces of the tag are parallel to the end of the cylindrical housing 60 as shown in Figure 1. The user may then operate the

keyboard 64 to instruct the microprocessor 21 via the RS232 interface that it is desired to read the data stored in the tag or transponder 1. Alternatively, the microprocessor 21 may be programmed or instructed to
5 search or seek for tags or transponders. This latter option is particularly suitable for use where the tags or transponders are carried by goods conveyed past a station at which the apparatus is located.

The following description relates to the digital
10 implementation of the apparatus shown in Figures 6 to 9. However, it will be appreciated by those skilled in the art that the operation of the apparatus shown in Figure 10 is similar.

Once the microprocessor has been instructed via the
15 RS232 interface that a tag or transponder 1 is to be read or has been instructed to search or seek for tags, the microprocessor 21 sends signals via the control lines 21a and 21b to switch on the numerically controlled oscillator 22 and to cause the numerically controlled
20 oscillator to generate a signal with a frequency of four times 125kHz so that the scaler 23 provides a 125kHz digital signal to the amplifier 24 via the switch SW1. The antenna 26 therefore transmits a sinusoidal RF signal at 125kHz to the tag or transponder 1 as indicated at
25 step S1 in Figure 12a. As indicated above, where the antenna 26 comprises a selectable RF coil arrangement, the microprocessor 21 will also select the RF coil or

coils most suitable for transmitting signals to and receiving signals from the particular tag or transponder 1 which the microprocessor initially assumes is present.

Any return signal transmitted by the tag or
5 transponder 1 is supplied via the antenna 26, directional coupler 25, conditioning circuit 27 and ADC 28 to the DSP1 which is controlled by the microprocessor 21 produce the in-phase and quadrature out-of-phase data carrying signals I and Q from which the 125kHz carrier frequency
10 has been filtered out. The in-phase and quadrature out-of-phase data carrying signals I and Q are written into the latch 31 under the control of write signals supplied via a write line WR from the DSP1. Data is supplied from the latch 31 up to the DSP2 on the 16 parallel bit data
15 bus 31a in response to a read instruction received from the DSP2 along the read line RE. The microprocessor 21 first assumes that the data transmitted by the tag or transponder 1 is ASK modulated and therefore controls the DSP2 to process the incoming in-phase data carrying
20 signal I as ASK modulated data at step S2. The ASK demodulated binary data is supplied via the DSP2 to the latch 32 under control of a read signal RE1 from the DSP2 and thence to the microprocessor 21. The microprocessor initially assumes, in this example, that the tag or
25 transponder being read is produced by EM Microelectronic Marin SA and therefore assumes that the digital data stream supplied by the DSP2 is Manchester code encoded.

The microprocessor thus decodes the received data as if it were Manchester encoded data at step S3 and then checks to see if a valid 0 or 1 data bit at a frequency of 32 or 64 cycles per second has been received at step
5 S4. If the answer is yes, the microprocessor stores the bit in RAM (not shown) at step S5 and then checks to see whether 64 bits of data have been received at step S6. If the answer is no, the microprocessor repeats steps S4, S5 and S6 until 64 bits of data have been received. The
10 microprocessor then looks at step S7 for a valid start sequence in the 64 bits of received data. That is, the microprocessor looks for the characteristic 9 logical 1 bits header of the EM Microelectronic Marin SA data storage format. If a valid start sequence is not
15 detected, the microprocessor indicates at step S8 that an error has occurred and may cause one or both of the LEDs on the wand to flash. In addition, the microprocessor may supply signals via the RS232 interface to cause an error message to be displayed on the LCD
20 of the host computer 62. Assuming a valid start sequence is detected, the microprocessor then checks the parity bits at step S9 in accordance with the stored information regarding this type of tag to determine whether there are any errors in the received data. If the error check is
25 not OK, that is if an error is detected, the microprocessor causes an error message to be generated. Again, for example, one or more of the LEDs 65 and 66 may

be caused to flash and a message may be displayed on the LCD screen 63. Assuming the error check does not indicate any errors in the data, the microprocessor determines that the tag or transponder 1 was indeed of
5 the EM Microelectronic Marin SA ASK modulated family and transmits the decoded data or ID at step S11 to the host computer 62 for display on the screen 63.

If the microprocessor does not detect receipt of a valid bit at step S4, a check is carried out step S12 to
10 determine whether the received data has been analysed on the basis of all types of tag or transponders known to the microprocessor. If the answer is yes, then the microprocessor determines that the tag or transponder 1 cannot be identified and the identification process is
15 terminated at step S13. The microprocessor 21 may also instruct the host computer to display a message indicating that the tag could not be identified. If it is determined at step S12 that the apparatus has not checked for all possible types of tag or transponder
20 known to the apparatus, then the microprocessor first checks at step S14 whether a maximum time T_0 set for the identification process by the user has been exceeded. If the answer is yes, then the microprocessor proceeds to step S13 and indicates that the tag or transponder 1
25 could not be identified. If the answer at step S14 is no, the microprocessor then checks whether the tag or transponder 1 is another type of tag or transponder 1

using ASK modulation. If desirable, where the antenna
26 has a selectable RF coil arrangement, the
microprocessor 21 may modify the RF coil selection to
optimise transmission of signals to and reception of
5 signals from the next type of transponder. In
particular, in the example shown in Figure 12b, the
microprocessor 21 checks the data received from the DSP2
to determine whether it can identify the PMC sequence
unique to the Philips PIT family of transponders. If the
10 answer is yes at step S15 and it is determined that a
valid PMC was received in the requisite time at step S16,
then the microprocessor stores the 128 bits of a block
of the PIT data format at step S17 and checks at step S18
to determine whether there is any bit error in accordance
15 with the information stored in its memory concerning this
particular type of tag. If the answer is no, the
microprocessor 21 determines that the tag has been
identified at step S19 and proceeds to decode the data
from the DSP2 assuming that the tag is a Philips PIT
20 family tag and supplies the decoded data via the RS232
interface to the host computer to enable the tag ID to
be displayed. If a bit error is detected at step S19
then an error signal is generated at step S20 by the
microprocessor and an error message displayed on the
25 display 63.

If the answer at step S15 is no, the microprocessor
then carries out steps S12 and S14 again to see if the

received data signal has been analysed for all known types of tags or transponders and if not to determine whether the maximum time T_0 allowed for the identification process has been exceeded. Again, if the answer to either of those questions is yes, the microprocessor proceeds to step S13. If the answer to both questions is no, then the microprocessor proceeds to analyse the incoming data stream in accordance with the modulation and data transmission system of the next known type of tag or transponder stored in the memory of the microprocessor. Again, the microprocessor 21 may adjust the selection of RF coil or coils where the antenna 26 comprises a microprocessor selectable RF coil arrangement. In this example, as shown in Figure 12c, the microprocessor 21 then checks to see if the transponder or tag is an EM Microelectronic Marin SA tag in which a 180° PSK rather than ASK modulation is used. Thus, the microprocessor controls the DSP2 at step S21 to provide PSK demodulated binary data. The microprocessor then carries out the same steps as S4 to S11 in Figure 12a and, if the tag or transponder is correctly identified as a PSK modulated tag or transponder produced by EM Microelectronic Marin SA, the decoded data is supplied to the host computer to enable the ID to be displayed. Again, if the answer at step S4 is no, the microprocessor repeats steps S12 and S14 to determine whether the incoming data stream has been

analysed according to the characteristics of all tags or transponders known to the microprocessor and, if not, whether the maximum time limit set for the interrogation has been exceeded. If the answer is in both cases no, the microprocessor assumes, in this example, that the tag or transponder is of the TIRIS family produced by Texas Instruments and supplies the 125kHz signal to the tag or transponder for the time known from the information stored in its memory to be required to charge the TIRIS tag, that is for a period of up to 50 milliseconds, at step S24. Again, where a microprocessor selectable RF coil arrangement is provided for the antenna, the microprocessor 21 may adjust the RF coil selection to optimise communication with the Texas TIRIS tag family. After a period of 50 milliseconds has expired, the microprocessor 21 controls the DSP2 to cause the incoming in-phase and quadrature data carrying signals to be processed as if they were FSK modulated in accordance with the TIRIS modulation and data transmission system. The FSK demodulation may be carried out at step S25 either by the filtering method described above with reference to Figure 9 in which, effectively, one of the in-phase or quadrature out-of-phase data carrying signals is filtered so as to pass only signals at the two modulation frequencies of the TIRIS tag or transponder or by using the comparison process described with reference to Figure 8. The microprocessor then checks

at step S26 to see if a valid FSK demodulated bit of the TIRIS data format has been received. If the answer is yes, the microprocessor stores the received bit at step S27. Steps S26 and S27 are repeated until the
5 microprocessor determines at step S28 that 128 bits have been received. Once this is the case, the microprocessor checks to see if the received data contains any error in accordance with the error determining protocol of the TIRIS tag or transponder modulation and coding system.
10 If the answer is yes at step S29, the microprocessor outputs an error message at step S30 to be displayed on the LCD of the host computer. If the answer is no at step S29, the microprocessor determines at step S31 that the tag or transponder is indeed a TIRIS type tag or
15 transponder and transmits the decoded identification to the host computer.

If the answer at step S26 is no, the microprocessor may optionally change the interrogation frequency at step S32 by controlling the output frequency of the NCO 22.
20 In particular, although it should be possible to charge a TIRIS tag or transponder using a 125kHz RF signal, the RF signal may be changed to the optimum charging frequency for the TIRIS tag system, namely 134.2kHz. Also, in this example, the microprocessor may control the
25 clock extraction circuit 51, if provided, to enable extraction of the clock frequencies from the data carrying signals I and Q. Once the frequency has been

changed at step S32, the microprocessor waits for 50
milliseconds at step S32a to ensure that the tag or
transponder is charged and then instructs the DSP2 to
carry out the FSK demodulating procedure as discussed
5 above at step S33. If the microprocessor determines that
a valid FSK bit has been received at step S34, the
process proceeds to step S27 and continues as discussed
above. If, however, the microprocessor does not detect
an FSK bit at step S34, steps S12 and S14 are again
10 carried out. If the microprocessor determines that
either all known types of tag have been checked for or
the maximum time limit allowed for the interrogation has
been exceeded, then the microprocessor determines that
the interrogation is at an end at step S13 and supplies
15 data to the host computer indicating that the tag cannot
be identified. If the answers at steps S12 and S14 are
no, the microprocessor 21 then proceeds to check for the
next type of tag, in this example the IDESCO MICROLOG
type of tag or transponder. Thus, the microprocessor 21
20 controls the NCO 22 to cause the antenna 26 to transmit
the exciter pulses for the charging time known from the
information stored in its memory to be required by the
IDESCO tag or transponder at step S35. Again, the
microprocessor 21 may adjust the RF coil selection to
25 optimise communication between the antenna 26 and the tag
1 where the antenna comprises a microprocessor-selectable
RF coil arrangement. Once the maximum required charging

time has expired, the microprocessor looks for a response to the exciter pulses (RSB) as described above with reference to Figure 5, as indicated by step S36 in Figure 12e. The DSP2 processes the in-phase and quadrature phase data carrier signals I and Q as if they were FSK modulated. If the DSP2 operates in the manner described above with reference to Figure 9, then the microprocessor controls the DSP2 to adjust the band-pass frequencies of the filters F3 and F4 to the two modulation frequencies used by the IDESCO modulation and coding system. The microprocessor then checks at step S37 whether a valid bit has been received. If the answer is yes, the bit is stored at step S38 and steps S37 and S38 repeated until the microprocessor determines at step S39 that all the bits known to be required for the IDESCO identification have been received. The microprocessor then checks at step S40 to see if there is any error in the received data in accordance with the IDESCO error checking procedure. If so, the microprocessor supplies a signal at step S41 to the host computer to indicate that the ID is invalid. If no error is detected, then the microprocessor determines at step S42 that the ID has been identified and supplies the ID to the host computer for display on the LCD display.

Although not shown in Figure 12e, if the microprocessor determines at step S37 that a valid bit has not been received, optionally the microprocessor may

operate the switch SW1 to prevent transmission of any RF signal between the exciter pulses and then control the NCO 22 to provide a substitute carrier frequency for the scaler 23 which is intermediate to the two modulation
5 frequencies of the IDESCO tag and then instruct and DSP2 to repeat the FSK data processing routine.

If the answer at step S37 is no even after the above optional steps have been carried out, the microprocessor again carries out steps S12 and S14. If the answer at
10 both steps S12 and S14 is no, then the microprocessor will proceed to analyse the incoming data for characteristics unique to the next type of tag stored in its memory. Alternatively, if the answer at either of steps S12 and S14 is yes, then the microprocessor sends
15 a signal to the host computer indicating that the identification process has ended without the tag being identified and, if the user does not instruct the host computer that another tag is to be checked within a predetermined time limit, the microprocessor will power
20 down the apparatus.

Of course, the order in which the apparatus checks for the various different types of tags or transponders may be now modified as desired.

Although particular examples of existing available
25 transponders or tags have been described above, it should be appreciated that the present invention can be applied to any commercially available transponders or tags using

ASK or 180° PSK and responsive to an RF frequency within the range available to the apparatus which may be, for example, from 50 to 250kHz, depending upon the characteristics of the NCO 22 and possibly also of the antenna 26, although the use of a microprocessor-controllable RF coil arrangement would increase the flexibility of the apparatus. In addition, if the FSK data processing routine shown in Figure 8 is used, then tags or transponders using FSK modulation with different frequencies from those described above may also be identified. Of course, if the band-pass of the filtering in the example shown in Figure 9 can be controlled by the microprocessor, then the filtering processing could also be used to analyse for FSK modulation schemes using other frequencies. Also, the PSK demodulation process may be adaptable to other PSK modulation schemes. Similarly, by reprogramming the DSPs in the apparatus shown in Figure 6, other modulation schemes may be accommodated as and when their use becomes known, for example, QPSK or spread spectrum modulation schemes may be incorporated. In addition, other methods for trying to identify a particular tag may be used. For example, a digital signal processor may be programmed to carry out a Fast Fourier Transform (FFT) on the response signal from the transponder 1 and the microprocessor 21 may then compare the resulting spectrum with stored data, for example the microprocessor 21 may be provided with a look

up table containing information on characteristic features of the spectrum of different tags or transponders 1 and may then compare the FFT spectrum from the DSP with the information in the look up table to
5 identify the particular tag, so as to enable its data to be decoded, if necessary, and retrieved.

It should be appreciated that the above described types of tags or transponders are only examples and that the present invention could also be applied to other
10 types of tags with different modulation and data transmission systems provided that the microprocessor has access to the information necessary to enable characteristic features of a tag's modulation and data transmission system, for example characteristic features
15 of its data format, to be identified and the identified tag then to be read. As new types of tag or transponder become known the programming of the DSPs, the microprocessor and the information stored in memory may be changed or updated by coupling the apparatus to a host
20 computer. Updating may even, for example, be carried out by a user installing updated software and information supplied on a suitable data carrier by the supplier of the apparatus via a host computer coupled to the apparatus. The digital signal processors may, where
25 necessary, be modified to cope with different carrier modulation and data transmission systems as these arise. It may also be possible for the apparatus microprocessor

to have access to information regarding common carrier modulation techniques and data format/coding systems not currently used for tags or transponders to allow the apparatus to attempt to read an unknown tag by using its
5 information regarding commonly known carrier modulation techniques and format/coding systems.

Although in the examples described above, digital signal processors have been used to increase the speed with which a tag can be read, where speed is not
10 essential or when faster more powerful microprocessors become available, it may be possible to replace the digital signal processors with microprocessors to facilitate modification of the processing operations.

Although the above description has been directed to
15 passive data storage tags in the form of low radio frequency identification tags or transponders, it should be appreciated that the present invention may be applied to, for example, passive data storage tags which operate at other electromagnetic frequencies, for example
20 frequencies in the Megahertz and Gigahertz (for example 2.45GHz) ranges and including microwave frequencies, with appropriate modification of the antenna structure and operating frequencies. It may also be possible to apply the present invention to passive data storage devices
25 where activation and data transmission is carried out by some form of opto-electronic coupling. In addition, the present invention could be applied to remotely readable

data storage devices such as so-called active tags which have some form of internal power source, for example a battery backed up RAM.

Also, once the data storage device has been
5 identified as described above apparatus embodying the present invention may be used to enable data to be written to a data storage device where the data storage device is designed to allow data to be written to the device.

10 Other modifications and variations will be apparent to those skilled in the art.

CLAIMS:

1. Apparatus for remotely reading data from a number of different manufacturer's data storage devices such as
5 radio frequency identification transponders, which apparatus comprises means for determining the modulation system used by such a data storage device to transmit data and for checking for features characteristic of the data transmission system of a particular manufacturer's
10 data storage devices in a response signal transmitted by the data storage device to the apparatus and means for analysing the response signal in accordance with the identified features to determine the data stored by the data storage device.

15

2. Apparatus for remotely reading data from a number of data storage devices each designed to communicate data to a corresponding compatible reader in response to an interrogation signal from that reader and using a carrier
20 modulation and data transmission system designed for that data storage device and corresponding reader, the apparatus comprising means for storing information relating to different possible carrier modulation and data transmission systems, means for interrogating a data
25 storage device by transmitting a signal to the data storage device, means for receiving a response signal from the data storage device, means for determining using

information stored by the storing means and the response signal the particular carrier modulation and data transmission system of the data storage device, and means for analysing the response signal in accordance with the identified carrier modulation and data transmission system to determine the data stored by the data storage device.

3. Apparatus according to claim 1 or 2, wherein the determining means comprises means for identifying whether the response signal uses any one of a number of different types of carrier modulation systems.

4. Apparatus according to claim 3, wherein the identifying means comprises means for processing the response signal as if it were using a given one of the different modulation systems to produce a processed signal, means for deciding from the processed signal whether the response signal used that modulation system and means for causing the processing means to repeat the processing for another of the different modulation systems if the deciding means decides that modulation system was not used.

5. Apparatus according to claim 4, wherein the processing means comprises a digital signal processor.

6. Apparatus according to claim 4 or 5, wherein the deciding means comprises a microprocessor.

7. Apparatus according to claim 4, 5 or 6, wherein the
5 deciding means comprises means for checking whether the processed signal represents a binary data stream of one of the possible carrier modulation and data transmission systems.

10 8. Apparatus according to claim 7, wherein the deciding means comprises means for decoding the processed signal in accordance with a coding system used by one of the possible different carrier modulation and data transmission systems having the given modulation scheme.

15

9. Apparatus according to any one of claims 4 to 8, wherein the deciding means comprises data format comparison means for comparing the processed signal with information stored by the storing means relating to
20 possible data format systems of the different possible carrier modulation and data transmission systems to determine whether the processed signal has a valid data format.

25 10. Apparatus according to any one of claims 4 to 9, wherein the identifying means comprises means for mixing a response signal received by the receiving means with

an in-phase carrier signal and with a quadrature out-of-phase carrier signal to provide in-phase and quadrature out-of-phase data carrying signals.

5 11. Apparatus according to claim 10, further comprising analog-to-digital conversion means for converting the response signal to a digital response signal and wherein the generating means are adapted to provide binary in-phase carrier and quadrature out-of-phase carrier signals
10 for mixing with the digital response signal.

12. Apparatus according to claim 10 or 11, wherein the identifying means comprises means for filtering the in-phase and quadrature out-of-phase data carrying signals
15 to remove the carrier signal.

13. Apparatus according to any one of claims 10 to 12, wherein the identifying means comprises means for comparing one of the in-phase and quadrature out-of-phase
20 signals with an average over time of the one of the in-phase and quadrature out-of-phase signals to provide an amplitude modulation demodulated output signal to the deciding means.

25 14. Apparatus according to any one of claims 10 to 13, wherein the identifying means comprises means for supplying the waveform of the quadrature out-of-phase

data carrying signal to the deciding means.

15. Apparatus according to any one of claims 10 to 14,
wherein the identifying means comprises first and second
5 band pass filtering means for each filtering one of the
in-phase and quadrature out-of-phase signals and
supplying an output signal to the deciding means.

16. Apparatus according to any one of claims 10 to 15,
10 wherein the identifying means comprises comparing means
for providing outputs dependent on the change of
amplitude of the in-phase and quadrature out-of-phase
signals with time to the deciding means.

15 17. Apparatus according to any one of the preceding
claims, further comprising control means for causing,
when the determining means determines that no response
signal has been received by the receiving means, the
transmitting means to send a signal for a predetermined
20 period to charge the data storage device and for causing
the determining means to determine whether a response
signal has been received at the end of the predetermined
period.

25 18. Apparatus according to claim 17, wherein the control
means is adapted to change the frequency of the
transmission means if no response is received at the end

of the predetermined period and then to cause the determining means to determine whether a response signal is received within another predetermined period.

5 19. Apparatus according to claim 17 or 18, wherein, when no response is received within the predetermined or a further predetermined period, the control means causes the transmitting means to generate periodic excitor signal bursts and causes the determining means to
10 determine whether a response signal is received in response to an excitor signal burst.

20. Apparatus according to any one of the preceding claims, wherein the apparatus is housed within a hand-
15 holdable casing.

21. Apparatus according to any one of the preceding claims, further comprising a communications interface for communicating with a host computer.

20

22. Apparatus according to any one of the preceding claims, further comprising means for reading bar codes.

23. Apparatus according to any one of the preceding
25 claims, further comprising means for modifying the signal transmitted to the data storage device.

24. Apparatus according to any one of claims 1 to 22 adapted to read data remotely from radio frequency identification tags or transponders.

5 25. Apparatus according to claim 24, wherein the transmitting means comprises an RF coil arrangement and means for selecting an RF coil or coil combination.

26. A method for remotely reading data from a number of
10 different manufacturer's data storage devices such as radio frequency identification transponders, which method comprises determining the modulation system used by such a data storage device to transmit data and checking for features characteristic of the data transmission system
15 of a particular manufacturer's data storage devices in a response signal transmitted by the data storage device to the apparatus and analysing the response signal in accordance with the identified features to determine the data stored by the data storage device.

20

27. A method for remotely reading data from a number of data storage devices each designed to communicate data to a corresponding compatible reader in response to an interrogation signal from that reader and using a carrier
25 modulation and data transmission system designed for that data storage device and corresponding reader, the method comprising storing information relating to different

possible carrier modulation and data transmission systems, interrogating a data storage device by transmitting a signal to the data storage device, receiving a response signal from the data storage device, 5 determining using stored information and the response signal the particular carrier modulation and data transmission system of the data storage device, and analysing the response signal in accordance with the identified carrier modulation and data transmission 10 system to determine the data stored by the data storage device.

28. A method according to claim 26 or 27, which comprises identifying whether the response signal uses 15 any one of a number different types of carrier modulation systems.

29. A method according to claim 28, which comprises identifying the modulation system by processing the 20 response signal as if it were using a given one of the different modulation systems to produce a processed signal, deciding from the processed signal whether the response signal used that modulation system and repeating the processing for another of the different modulation 25 systems if that modulation system was not used.

30. A method according to claim 29, wherein the deciding step comprises checking whether the processed signal represents a binary data stream of one of the possible carrier modulation and data transmission systems.

5

31. A method according to claim 30, wherein the deciding step comprises decoding the processed signal in accordance with a coding system used by one of the possible different carrier modulation and data
10 transmission system having the given modulation scheme.

32. A method according to any one of claims 29 to 31, wherein the deciding step comprises comparing the processed signal with information stored by the storing
15 means relating to possible data format systems of the different possible carrier modulation and data transmission systems to determine whether the processed signal has a valid data format.

20 33. A method according to any one of claims 26 to 32, which comprises, when no response is received within a predetermined period, continuing transmission of a signal to the data storage device for a predetermined time to charge the device and then determining whether a response
25 is received.

34. A method according to claim 33, which comprises, after the predetermined period, if no response signal is received, generating periodic excitor signal bursts and determining whether a response signal is received in response to an excitor signal burst.

35. A method according to any one of claims 26 to 32 for reading data remotely from radio frequency identification tags or transponders.

10

36. Apparatus for remotely reading data from a number of data storage devices substantially as hereinbefore described with reference to the accompanying drawings.

15 37. A method for remotely reading data from a number of data storage devices substantially as hereinbefore described.

54

Relevant Technical Fields

(i) UK Cl (Ed.N) G4H (HNLB, HNNC); H4L
(LACA, LASS)

(ii) Int Cl (Ed.6) G01S 13/02, 13/76, 13/82; G06K 7/00, 7/08, 7/10

Date of completion of Search
4 DECEMBER 1995

Databases (see below)

(i) UK Patent Office collections of GB, EP, WO and US patent specifications.

Documents considered relevant following a search in respect of Claims :-
1-37

(ii) ONLINE: WPI

X: Document indicating lack of novelty or of inventive step.

P: Document published on or after the declared priority date but before the filing date of the present application.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

A: Document indicating technological background and/or state of the art.

&: Member of the same patent family; corresponding document.

Databases:The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).

Continuation page

Category	Identity of document and relevant passages	Relevant to claim(s)
X	US 5329104 (ALPS) see whole document	1, 2, 22, 26, 27 at least

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 2003

Application or Docket Number

10848246

CLAIMS AS FILED - PART I

(Column 1)

(Column 2)

TOTAL CLAIMS	46	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	46 minus 20 =	26
INDEPENDENT CLAIMS	9 minus 3 =	0
MULTIPLE DEPENDENT CLAIM PRESENT ☐		

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT A	10/5/06	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	43	Minus	46	=
	Independent	6	Minus	3	= 3
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

(Column 1)

(Column 2)

(Column 3)

AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	*	Minus	**	=
	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

(Column 1)

(Column 2)

(Column 3)

AMENDMENT C		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	*	Minus	**	=
	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SMALL ENTITY

TYPE ☐

OTHER THAN

SMALL ENTITY

RATE	FEE
BASIC FEE	385.00
XS 9=	
X43=	
+145=	
TOTAL	

RATE	FEE
BASIC FEE	770.00
XS18=	468
X86=	
+290=	
TOTAL	1238

SMALL ENTITY

OR

OTHER THAN

SMALL ENTITY

RATE	ADDITIONAL FEE
XS 9=	
X43=	
+145=	
TOTAL	
ADDIT. FEE	

RATE	ADDITIONAL FEE
XS18=	
X86=	600
+290=	
TOTAL	600
ADDIT. FEE	

RATE	ADDITIONAL FEE
XS 9=	
X43=	
+145=	
TOTAL	
ADDIT. FEE	

RATE	ADDITIONAL FEE
XS18=	
X86=	
+290=	
TOTAL	
ADDIT. FEE	

RATE	ADDITIONAL FEE
XS 9=	
X43=	
+145=	
TOTAL	
ADDIT. FEE	

RATE	ADDITIONAL FEE
XS18=	
X86=	
+290=	
TOTAL	
ADDIT. FEE	



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/848,246

05/18/2004

Ralph W. Quan

038P0401

4526

7590

06/26/2006

Rodney F. Brown
3365 Baltimore Street
San Diego, CA 92117

EXAMINER

AU, SCOTT D

ART UNIT

PAPER NUMBER

2612

DATE MAILED: 06/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/848,246

Applicant(s)

QUAN, RALPH W.

Examiner

Scott Au

Art Unit

2612

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 May 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-46 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 11-14 and 22-46 is/are rejected.
- 7) ☒ Claim(s) 5-10 and 15-21 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 May 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) ☐ Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) ☐ Other: _____ |

DETAILED ACTION

The application of Quan for a "RIFD reader utilizing an analog to digital converter for data acquisition and power monitoring functions" filed May 18, 2004 has been examined.

Claims 1-46 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1,3-4,11-14,25,27-28, and 30-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson (US# 6,476,708) in view of Carroll et al. (US# 5,347,263).

Referring to claims 1, 25 and 28, Johnson discloses a reader for an RFID system and method comprising:

a signal generator (16) (i.e. excitation signal generator circuit) for generating a detection signal containing analog data and for generating an excitation signal;

a transmitting antenna (28) (i.e. transmitting antenna) coupled with said signal generator for transmitting said detection signal and said excitation signal into a space surrounding said transmitting antenna;

a receiving antenna (30) (i.e. receiving antenna) for receiving a transponder data signal at a voltage value containing data from a transponder in said space;

receiver electronics (22) (i.e. response signal conditioner circuit) coupled with said receiving antenna for conditioning said transponder data signal to place said transponder data signal in a condition for reading said digital data;

an internal power source (26) (i.e. power source) for supplying electrical operating power to said reader,
said internal power source having a declining power level as a function of use; and

a microcontroller (24) (i.e. demodulation circuit and detection circuit) coupled with said internal power source and receiver electronics (col. 3 lines 35-63).

However, Johnson did not explicitly disclose a single-chip microcontroller including an analog to digital converter to acquire said analog data from said detection signal and said digital data from said transponder data signal and to convert said analog data from said detection signal to converted digital data.

In the same field of endeavor of communication system, Carroll et al. disclose a single-chip microcontroller (42) (i.e. single chip) including an analog to digital converter to acquire said analog data from said detection signal and said digital data from said

transponder data signal and to convert said analog data from said detection signal to converted digital data (col. 7 lines 1-8 and col. 9 lines 14-39).

One ordinary skill in the art understands that a single-chip microcontroller (42) (i.e. single chip) including an analog to digital converter to acquire said analog data from said detection signal and said digital data from said transponder data signal and to convert said analog data from said detection signal to converted digital data of Carroll et al. is desirable in the communication system of Johnson because Johnson teaches circuit 24 for demodulating and detecting the signal is received from the receiving circuit 22 (col. 3 lines 35-64) and Carroll et al. teach the single microprocessor 42 processes the signal into digital signal in order to identify the transponder.

Referring to claims 3 and 30, Johnson in view of Carroll et al. disclose the system and method of claims 1 and 28, Carroll et al. disclose wherein said single-chip microcontroller further includes a software and/or firmware-based demodulator for demodulating said transponder data signal to read said digital data from said transponder data signal (col. 10 lines 3-19).

Referring to claims 4, 27 and 31, Johnson in view of Carroll et al. disclose the system and method of claims 1, 25 and 28, Carroll et al. disclose wherein said receiving antenna and said transmitting antenna are both included in a single dual-function antenna (col. 9 lines 8-12 and 40-45).

Referring to claims 11-14, and 35-40, Johnson in view of Carroll et al. disclose the system and method of claims 1 and 28, it is conventional in the art that the single-chip microcontroller having utility herein is Model MSP430 available from Texas Instruments, Inc., 12500 TI Boulevard, Dallas, Tex. 75243-4136. The reader microcontroller 28 also contains an analog to digital converter (ADC) module 42, which preferably includes a conventional sample and hold circuit as disclose by the applicant specification paragraph 47, and also see Johnson, col. 6 line 62 to col. 7 line 19.

Referring to claim 32, Johnson in view of Carroll et al. disclose the method of claim 28, Johnson discloses wherein said transponder data signal is conditioned with said receiver electronics by reducing said voltage value of said transponder data signal and maintaining said transponder data signal in a voltage range between about ground and a power supply for said reader, inclusive (col. 10 lines 1-23).

Referring to claim 41, Johnson in view of Carroll et al. disclose the method of claim 32, Johnson discloses wherein said transponder data signal is conditioned with said receiver electronics by rectifying said voltage value of said transponder data signal and maintaining said transponder data signal in a voltage range between about ground and a power supply for said reader, inclusive (col. 10 lines 1-23).

Referring to claim 42, Johnson in view of Carroll et al. disclose the method of claim 41, Johnson discloses wherein said transponder data signal is conditioned with said receiver electronics by rectifying said voltage value of said transponder data signal and integrating said transponder data signal over one or more cycles of a carrier frequency of said transponder data signal (col. 9 lines 22-45 and col. 10 lines 1-23).

Referring to claim 43, Johnson in view of Carroll et al. disclose the method of claim 32, Johnson discloses wherein said transponder data signal is conditioned with said receiver electronics by rectifying said voltage value of said transponder data signal and integrating said transponder data signal over one or more cycles of a carrier frequency of said transponder data signal (col. 9 lines 22-45 and col. 10 lines 1-23).

Referring to claim 33, Johnson in view of Carroll et al. disclose the method of claim 28, Johnson discloses wherein said transponder data signal is conditioned with said receiver electronics by rectifying said voltage value of said transponder data signal and maintaining said transponder data signal in a voltage range between about ground and a power supply for said reader, inclusive (col. 10 lines 1-23).

Referring to claim 34, Johnson in view of Carroll et al. disclose the method of claim 28, Johnson discloses wherein said transponder data signal is conditioned with said receiver electronics by rectifying said voltage value of said transponder data signal

and integrating said transponder data signal over one or more cycles of a carrier frequency of said transponder data signal (col. 9 lines 22-45 and col. 10 lines 1-23).

Referring to claim 44, Johnson in view of Carroll et al. disclose the method of claim 28, further comprising terminating said detection mode and initiating said excitation mode when said proximal transponder is detected (col. 4 lines 44-51) in order to reduce the used of power.

Referring to claim 45, Johnson in view of Carroll et al. disclose the method of claim 28, Johnson discloses wherein said detection mode of operation has a reduced power state and said excitation mode of operation has an increased power state (col. 4 lines 44-51).

Referring to claim 46, Johnson in view of Carroll et al. disclose the method of claim 28, Carroll et al. disclose measuring said declining power level of said internal power source with said analog to digital converter (col. 9 lines 14-39).

Claims 2, 26 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson (US# 6,476,708) in view of Carroll et al. (US# 5,347,263) as applied to claims 1, 25 and 28 above, and further in view of Turner et al. (US# 6,367,697).

Referring to claims 2, 26 and 29, Johnson in view of Carrol et al. disclose the system and method of claims 1, 25 and 28, Johnson in view of Carroll et al. disclose said receiver electronics includes a receiver electronics input from said receiving antenna, a receiver electronics output to said single-chip microcontroller. However, Johnson in view of Carroll et al. did not explicitly disclose wherein the reader includes a plurality of relatively low-cost simple electrical components selected from the group consisting of resistors, diodes, capacitors, and electrical switches, and excludes relatively high-cost complex multi-stage band pass amplifiers.

In the same field of endeavor of communication system, Turner et al. teach wherein the reader includes a plurality of relatively low-cost simple electrical components selected from the group consisting of resistors, diodes, capacitors, and electrical switches, and excludes relatively high-cost complex multi-stage band pass amplifiers (col. 5 lines 13-23; see Figure 4).

One ordinary skill in the art understands that the reader includes a plurality of relatively low-cost simple electrical components selected from the group consisting of resistors, diodes, capacitors, and electrical switches, and excludes relatively high-cost complex multi-stage band pass amplifiers of Turner et al. is desirable in the reader system of Johnson in view of Carroll et al. because Johnson and Turner et al. teach interrogating transponders system and Turner et al. teach the used of components from the group consisting of resistors, diodes, capacitors, and electrical switches, is obvious of low costs.

Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson (US# 6,476,708) in view of Carroll et al. (US# 5,347,263).

Referring to claim 22, Johnson in view of Carroll et al. disclose the system of claim 1. However, Johnson in view of Carroll et al. did not explicitly disclose a transmitting tuning capacitor paired with said transmitting antenna and a receiving tuning capacitor paired with said receiving antenna.

In the same field of endeavor of communication system, Riek teaches a transmitting tuning capacitor paired with said transmitting antenna and a receiving tuning capacitor paired with said receiving antenna (col. 5 line 51 to col. 6 line 3; see Figure 5).

One ordinary skill in the art understands that the transmitting tuning capacitor paired with said transmitting antenna and the receiving tuning capacitor paired with said receiving antenna of Riek is desirable in the reader of Johnson in view of Carroll et al. because Johnson et al. teach the transmitting and receiving antennas (28,30) of the reader 12 (i.e. see Figure 1A) and Riek teaches the transmitting tuning capacitor paired with said transmitting antenna and the receiving tuning capacitor paired with said receiving antenna in order to communicate with the transponders (col. 5 line 51 to col. 6 line 3; see Figure 5).

Referring to claim 23, Johnson in view of Carroll et al. and Riek disclose the system of claim 22, Carroll et al. discloses a dual function antenna 43 (col. 9 lines 8-12 and 40-45) and Riek teaches the transmitting tuning capacitor paired with said transmitting antenna and the receiving tuning capacitor paired with said receiving antenna in order to communicate with the transponders (col. 5 line 51 to col. 6 line 3; see Figure 5). It is obvious one skill in the art understands that one can combine the idea of Carroll et al. and Riek in order to produce the receiving tuning capacitor and said transmitting tuning capacitor are both included in a single dual-function tuning capacitor.

Referring to claim 24, Johnson in view of Carroll et al. and Riek disclose the system of claim 22, Johnson teaches wherein said transmitting tuning capacitor and/or said receiving tuning capacitor is a first tuning capacitor for tuning a first reader antenna to a higher carrier frequency, said reader further comprising a second tuning capacitor for tuning a second reader antenna to a lower carrier frequency (col. 9 lines 30-45).

Claim Objections

Claims 5-10 and 15-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Referring to claim 5, the following is a statement of reasons for the indication of allowable subject matter: the prior art fail to suggest limitations that wherein said

receiver electronics includes a resistor divider section comprising first and second series resistors at said receiver electronics input forming a voltage divider to reduce said voltage value of said transponder data signal and third and fourth series resistors downstream of said first and second series resistors positioned between ground and said power supply and a blocking capacitor positioned in parallel with the second series resistor upstream of said third and fourth series resistors to maintain said transponder data signal at said receiver electronics output in a voltage range between about ground and said power supply, inclusive

Referring to claim 6, the following is a statement of reasons for the indication of allowable subject matter: the prior art fail to suggest limitations that wherein said receiver electronics includes a peak detector section comprising a rectifier at said receiver electronics input to rectify said voltage value of said transponder data signal and a pair of series resistors downstream of said rectifier positioned between ground and said power supply and a blocking capacitor positioned between said rectifier and said pair of series resistors to maintain said transponder data signal at said receiver electronics output in a voltage range between about ground and said power supply, inclusive.

Referring to claim 8, the following is a statement of reasons for the indication of allowable subject matter: the prior art fail to suggest limitations that wherein said receiver electronics includes an integrator section comprising a rectifier and an

integrator in series at said receiver electronics input and coupled with said receiver electronics output, said receiver electronics output coupled with said analog to digital converter.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ueda (US# 6,731,199) discloses an interrogation system.

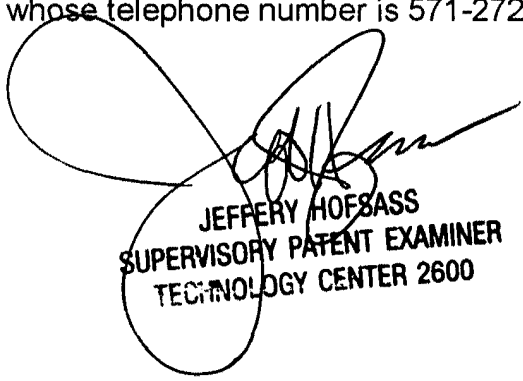
Bradin (US# 6,650,227) discloses a reader for a reader for a radio frequency identification system having automatic tuning capability.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Au whose telephone number is (571) 272-3063. The examiner can normally be reached on Mon-Fri, 8:30AM – 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Hofsass can be reached at (571) 272-2981. The fax phone numbers for the organization where this application or proceeding is assigned are (571)-272-1817.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-3050.

Scott Au



JEFFERY HOFBASS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Notice of References Cited	Application/Control No. 10/848,246	Applicant(s)/Patent Under Reexamination QUAN, RALPH W.	
	Examiner Scott Au	Art Unit 2612	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,367,697	04-2002	Turner et al.	235/440
*	B	US-6,354,468	03-2002	Riek, Jan C.	222/129.3
*	C	US-6,650,227	11-2003	Bradin, John P.	340/10.3
*	D	US-6,731,199	05-2004	Ueda, Takashi	340/10.4
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

FORM PTO-1449

Docket No:
038P0401INFORMATION DISCLOSURE
STATEMENT BY APPLICANTApplicant:
Ralph W. Quan

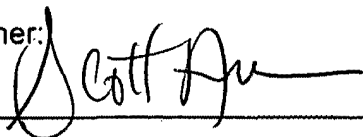
U.S. PATENT DOCUMENTS

Exam. Initial	Pat./App. Number	Issue/Pub. Date	Inventor	Class	Sub- Class
<u>SA</u>	4,730,188	3/8/88	Milheiser	340	825.0
<u>SA</u>	5,347,263	9/13/94	Carroll et al.	340	572
<u>SA</u>	5,541,574	7/30/96	Lowe et al.	340	447
<u>SA</u>	6,476,708	11/5/02	Johnson	340	10.34
<u>SA</u>	20030090367	5/15/03	Carroll et al.	340	10.4

FOREIGN PATENT DOCUMENTS

Exam. Initial	Document Number	Publication Date	Country	Class	Translation Yes No
<u>SA</u>	GB 2 278 631	12/7/94	UK	E06B 49/00	

Examiner:



Date Considered:

5/31/06

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP §609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[illegible]

Scott Au

2612

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INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
Search EAST		
Keywords: analog, digital reader, Interrogation excitation tag, transponder resistor, capacitors diode, level		

Index of Claims



Application/Control No.

10/848,246

Examiner

Scott Au

Applicant(s)/Patent under Reexamination

QUAN, RALPH W.

Art Unit

2612

✓	Rejected
=	Allowed

-	(Through numeral) Cancelled
+	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claim		Date									
Final	Original										
1	✓										
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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	"20050258940".pn.	US-PGPUB; USPAT	OR	OFF	2006/06/02 13:31
S2	1	"5945906".pn.	US-PGPUB; USPAT	OR	OFF	2006/05/29 22:05
S3	1	"5561420".pn.	US-PGPUB; USPAT	OR	OFF	2006/05/29 22:18
S4	12	((("4,178,549") or ("4,219,812") or ("4,482,947") or ("4,529,980") or ("4,665,397") or ("4,706,299") or ("4,912,463") or ("5,085,062") or ("5,193,210") or ("5,412,379") or ("5,471,668") or ("5,528,230"))).PN.	USPAT	OR	OFF	2006/05/29 22:21
S5	1	"20050258940".pn. and (transmit\$4)	US-PGPUB; USPAT	OR	OFF	2006/05/31 09:22
S6	1	"20050258940".pn. and (receiv\$4)	US-PGPUB; USPAT	OR	OFF	2006/05/31 09:32
S7	1	"20050258940".pn. and (pair)	US-PGPUB; USPAT	OR	OFF	2006/05/31 09:34
S8	1	"20050258940".pn. and (tuning with capacitor)	US-PGPUB; USPAT	OR	OFF	2006/06/01 19:32
S9	1	"4730188".pn.	USPAT	OR	OFF	2006/05/31 10:05
S10	1	"5347263".pn.	USPAT	OR	OFF	2006/05/31 10:16
S11	1	"5541574".pn.	USPAT	OR	OFF	2006/05/31 10:20
S12	1	"6476708".pn.	USPAT	OR	OFF	2006/05/31 10:22
S13	1	"20030090367".pn.	US-PGPUB; USPAT	OR	OFF	2006/05/31 10:26
S14	9012	scott.xa.	USPAT	OR	OFF	2006/05/31 10:26
S15	269	S14 and au	USPAT	OR	OFF	2006/05/31 10:27
S16	44	S15 and horabik	USPAT	OR	OFF	2006/05/31 10:27
S17	9	("3983487" "4264980" "4393514" "4786903" "5630216" "5710993" "5742902" "6094147" "6288629").PN. OR ("7046122").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/05/31 10:28
S18	4	("5926110" "6100603" "6218932" "6307471").PN. OR ("6950008").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/05/31 10:32
S19	12	("3859624" "4471343" "4730188" "4752776" "5523746" "5973611").PN. OR ("6476708").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/05/31 10:56

EAST Search History

S20	12	("3859624" "4471343" "4730188" "4752776" "5523746" "5973611").PN. OR ("6476708").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/05/31 10:56
S21	0	("2003/0090367").URPN.	USPAT	OR	OFF	2006/05/31 10:58
S22	117	("3859624" "3878528" "4095214" "4129855" "4354099" "4475481" "4549264" "4672375" "4688036" "4724427" "4739328" "4857893" "4893118" "5023887" "5070500" "5235326" "5266926").PN. OR ("5347263"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/05/31 10:59
S23	117	("3859624" "3878528" "4095214" "4129855" "4354099" "4475481" "4549264" "4672375" "4688036" "4724427" "4739328" "4857893" "4893118" "5023887" "5070500" "5235326" "5266926").PN. OR ("5347263"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/05/31 14:01

EAST Search History

S24	154	("3022492" "3128744" "3137847" "3144017" "3299424" "3313301" "3369525" "3427614" "3440633" "3541995" "3545405" "3557758" "3689885" "3739279" "3752960" "3757035" "3803571" "3816709" "3820545" "3859624" "3878322" "3890581" "3898619" "3933612" "3944928" "3964024" "4040053" "4053836" "4065753" "4068232" "4075632" "4079414" "4087791" "4114151" "4129855" "4187509" "4196418" "4209783" "4233964" "4242663" "4262632" "4313033" "4333072" "4345253" "4350883" "4368439" "4388524" "4447909" "4463353" "4485347" "4494553" "4510495" "4517563" "4525713" "4556883" "4596985" "4602253" "4630044").PN. OR ("4730188").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/05/31 14:25
S25	1	"4826581".pn.	USPAT	OR	OFF	2006/05/31 14:25
S26	6	("4233109" "4406765" "4687753" "4695357").PN. OR ("4826581").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/05/31 14:25

EAST Search History

S27	154	("3022492" "3128744" "3137847" "3144017" "3299424" "3313301" "3369525" "3427614" "3440633" "3541995" "3545405" "3557758" "3689885" "3739279" "3752960" "3757035" "3803571" "3816709" "3820545" "3859624" "3878322" "3890581" "3898619" "3933612" "3944928" "3964024" "4040053" "4053836" "4065753" "4068232" "4075632" "4079414" "4087791" "4114151" "4129855" "4187509" "4196418" "4209783" "4233964" "4242663" "4262632" "4313033" "4333072" "4345253" "4350883" "4368439" "4388524" "4447909" "4463353" "4485347" "4494553" "4510495" "4517563" "4525713" "4556883" "4596985" "4602253" "4630044").PN. OR ("4730188").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/05/31 15:31
S28	170	340/10.3.ccls.	USPAT	OR	OFF	2006/05/31 18:35
S29	331	340/572.4.ccls.	USPAT	OR	OFF	2006/05/31 18:35
S30	0	S29 and (analog same excitation same (reader interrogat\$4))	USPAT	OR	OFF	2006/05/31 18:37
S31	2	340/825\$.ccls. and (analog same excitation same (reader interrogat\$4))	USPAT	OR	OFF	2006/05/31 18:38
S32	3	340/572\$.ccls. and (analog same excitation same (reader interrogat\$4))	USPAT	OR	OFF	2006/05/31 18:40
S33	0	340/447\$.ccls. and (analog same excitation same (reader interrogat\$4))	USPAT	OR	OFF	2006/05/31 18:40
S34	2	340/10.34.ccls. and (analog same excitation same (reader interrogat\$4))	USPAT	OR	OFF	2006/05/31 18:42
S35	1	340/10.4.ccls. and (analog same excitation same (reader interrogat\$4))	USPAT	OR	OFF	2006/05/31 18:42

EAST Search History

S36	17	"340"/\$.ccls. and (analog same excitation same (reader interrogat\$4))	USPAT	OR	OFF	2006/05/31 18:47
S37	1	(transponder same power same level same analog same excitation same (reader interrogat\$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/31 18:48
S38	1	"5347263".pn.	US-PGPUB; USPAT	OR	OFF	2006/06/01 14:07
S39	1	"6476708".pn.	US-PGPUB; USPAT	OR	OFF	2006/06/01 16:02
S40	1	"6208235".pn.	US-PGPUB; USPAT	OR	OFF	2006/06/01 16:03
S41	1	"7049958".pn.	US-PGPUB; USPAT	OR	OFF	2006/06/01 16:05
S42	470	"340"/\$.ccls. and (resistor\$2 same diode\$2 same capacitor\$2) and (reader interrogator)	US-PGPUB; USPAT	OR	OFF	2006/06/01 16:07
S43	1530	"340"/\$.ccls. and (resistor\$2 same diode\$2 same capacitor\$2 same (reader receiv\$4 interrogator))	US-PGPUB; USPAT	OR	ON	2006/06/01 16:08
S44	762	"340"/\$.ccls. and ((resistor\$2 with diode\$2 with capacitor\$2) same (reader receiv\$4 interrogator))	USPAT	OR	ON	2006/06/01 16:09
S45	23	"340"/\$.ccls. and ((resistor\$2 with diode\$2 with capacitor\$2) same (reader interrogator))	USPAT	OR	ON	2006/06/01 16:43
S46	5	"340"/\$.ccls. and ((resistor\$2 same voltage same divider same reduc\$ same series) same (reader interrogator receiver receiving))	USPAT	OR	ON	2006/06/01 16:46
S47	71	"340"/\$.ccls. and (resistor\$2 same voltage same divider same reduc\$ same series) and (reader interrogator receiver receiving)	USPAT	OR	ON	2006/06/01 16:47
S48	2	"340"/\$.ccls. and (resistor\$2 same voltage same divider same reduc\$ same series) and (reader interrogator receiver receiving) and (transponder\$2 tag\$2)	USPAT	OR	ON	2006/06/01 16:48
S49	9	(resistor\$2 same voltage same divider same reduc\$ same series) and (reader interrogator receiver receiving) and (transponder\$2 tag\$2)	USPAT	OR	ON	2006/06/01 17:12

EAST Search History

S50	154	((peak with detect\$4) same (rectifier with resistor\$2))	USPAT	OR	OFF	2006/06/01 17:13
S51	1	S50 and (reader same transponder)	USPAT	OR	ON	2006/06/01 17:13
S52	0	("2005/0258940").URPN.	USPAT	OR	OFF	2006/06/01 18:19
S53	9	"340"/\$.ccls. and (reader same transponder) and (((diode\$2 rectifier) with (integrator resistor)) same (output and input))	USPAT	OR	OFF	2006/06/01 18:41
S54	2	"340"/\$.ccls. and (reader same transponder) and (((diode\$2 rectifier) with (integrator resistor)) same (output and input) same receiv\$4)	USPAT	OR	OFF	2006/06/01 19:24
S55	9012	scott.xa.	USPAT	OR	OFF	2006/06/01 19:25
S56	44	S55 and au and horabik	USPAT	OR	OFF	2006/06/01 19:25
S57	9	("20020024422" "5231273" "5406297" "5751570" "5777561" "5940006" "5966083" "6104279" "6661336").PN. OR ("7053755"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/06/01 19:27
S58	9	("3983487" "4264980" "4393514" "4786903" "5630216" "5710993" "5742902" "6094147" "6288629").PN. OR ("7046122"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/06/01 19:28
S59	0	"20050258940".pn. and (holding and tim\$4)	US-PGPUB; USPAT	OR	OFF	2006/06/01 19:33
S60	1	"20050258940".pn. and (hold and tim\$4)	US-PGPUB; USPAT	OR	OFF	2006/06/01 19:57
S61	1	"6354468".pn.	US-PGPUB; USPAT	OR	OFF	2006/06/01 19:57
S62	1	"20050258940".pn. and (single with dual with capacitor)	US-PGPUB	OR	ON	2006/06/02 13:59
S63	0	"6354468".pn. and (low and high)	US-PGPUB	OR	ON	2006/06/02 13:57
S64	0	"6476708".pn. and (low and high)	US-PGPUB	OR	ON	2006/06/02 16:31
S65	0	"5347263".pn. and (low and high)	US-PGPUB	OR	ON	2006/06/02 13:54
S66	1	"5347263".pn. and (low and high)	USPAT	OR	ON	2006/06/02 13:55
S67	1	"6476708".pn. and (low and high)	USPAT	OR	ON	2006/06/02 13:56
S68	0	"6354468".pn. and (low and high)	USPAT	OR	ON	2006/06/02 13:57
S69	0	"6354468".pn. and (low\$3 and high\$3)	USPAT	OR	ON	2006/06/02 13:57

EAST Search History

S70	1	"20050258940".pn. and (high\$4 same low\$4)	US-PGPUB	OR	ON	2006/06/02 14:00
S71	1	"6476708".pn. and (detect\$4)	USPAT	OR	ON	2006/06/02 16:31

EXPRESS MAIL LABEL NO: ER 782612292 US

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Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Docket No:038P0401

NON-PROVISIONAL PATENT APPLICATION FEE TRANSMITTAL

Sir:

Transmitted herewith for filing is the non-provisional patent application of

Inventor: Ralph W. Quan

Entitled: RFID Reader Utilizing an Analog to Digital Converter for Data Acquisition and Power Monitoring Functions

Including the specification having 34 pages and a title page, and the formal drawings having 3 sheets.

Also enclosed are:

Glossary of Drawing Terms;

Combined Declaration and Power of Attorney for Patent Application;

Assignment and Recordation Form Cover Sheet for Patents; and

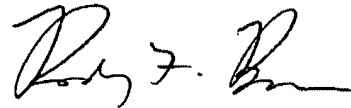
Information Disclosure Statement, Form PTO-1449, and copies of listed references.

The filing fee has been calculated as shown below:

	Number Filed		Number Extra		Rate			Fee	
					Small Entity	Other Entity		Small Entity	Other Entity
Total Claims	46 - 20	=	26	X	\$9	\$18	=	\$--	\$288
Independent Claims	3 - 3	=	0	X	\$43	\$86	=	\$--	\$0
Multiple Dependent Claims Presented: ___ Yes <u>X</u> No					\$145	\$290		\$--	\$0
					BASIC FEE			\$385	\$770
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I hereby authorize the charge of \$1058.00 for the total fees indicated above to my deposit account number 02-4245. Also charge any deficiency or credit any overpayment in the total fees indicated above to my deposit account. A duplicate copy of this document is enclosed for fee payment purposes.

Respectfully submitted,



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UNITED STATES NON-PROVISIONAL PATENT APPLICATION

of

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for

RFID Reader Utilizing an Analog to Digital Converter

for Data Acquisition and Power Monitoring Functions

**RFID READER UTILIZING AN ANALOG TO DIGITAL CONVERTER
FOR DATA ACQUISITION AND POWER MONITORING FUNCTIONS**

TECHNICAL FIELD

5 The present invention relates generally to RFID systems, and more particularly to the construction and operation of a reader in an RFID system.

BACKGROUND OF THE INVENTION

10 Radio frequency identification (RFID) systems generally consist of at least one host reader and a plurality of transponders, which are commonly termed credentials. The transponder is an active or passive radio frequency communication device, which is directly attached to or embedded in an article to be identified or otherwise characterized by the reader, or which is alternatively embedded in a portable substrate, such as a card, keyfob, tag, or the like, carried by a person or an article to be identified
15 or otherwise characterized by the reader.

 A passive transponder is dependent on the host reader as its power supply. The host reader "excites" or powers up the passive transponder by transmitting high voltage excitation signals into the space surrounding the reader, which are received by the transponder when it is near, but not necessarily in contact with, the reader. The
20 excitation signals from the reader provide the operating power for the circuitry of the recipient transponder. In contrast, an active transponder is not dependent on the reader as its power supply, but is instead powered up by its own internal power source, such as a battery. Once the transponder is powered up, the transponder communicates information, such as identity data or other characterizing data stored in
25 the memory of the transponder, to the reader and the reader can likewise communicate information back to the transponder without the reader and transponder coming in contact with one another.

 The powered up transponder communicates with the reader by generating transponder data signals within the circuitry of the transponder and transmitting the
30 transponder data signals in the form of electromagnetic waves into the surrounding

space occupied by the reader. The reader contains its own circuitry to “read” the data contained in the transponder data signals received from the transponder. Exemplary RFID systems communicating in this manner are disclosed in U.S. Patents 4,730,188 to Milheiser (the ‘188 Patent), 5,541,574 to Lowe et al. (the ‘574 Patent), and 5,347,263 to Carroll et al. (the ‘263 Patent), all of which are incorporated herein by reference.

RFID systems are generally characterized by a number of parameters relating to transmission and processing of the data signals. Such parameters include the carrier frequency of the data signals, the transfer rate of the data in the data signals, and the type of modulation of the data signals. In particular, data signals communicated between the transponder and reader of a given RFID system are usually at a specified standard carrier frequency, which is characteristic of the given RFID system. For example, RFID systems, which employ transponders of the type conventionally termed proximity cards or proximity tags, typically communicate by means of data signals at a carrier frequency within a range of 100 to 150 kHz. This carrier frequency range is nominally referred to herein as 125 kHz carrier frequency and is deemed a low frequency. In contrast, RFID systems, which employ transponders of the type conventionally termed smart cards, typically communicate by means of data signals at a higher frequency of 13.56 MHz.

The transfer rate of digital data communicated between the transponder and reader of a given RFID system via the data signals is commonly at one of a number of specified standard data rates, which is also characteristic of the given RFID system. The specified data rates are usually a function of the carrier frequency for the given RFID system. For example, RFID systems operating at the 125 kHz carrier frequency typically employ a relatively low data rate on the order of a few kilobits per second. For RFID systems operating at the 13.56 MHz carrier frequency, one particular industry standard specifies a low data rate of about 6 kilobits per second and a high data rate of about 26 kilobits per second. Another industry standard specifies an even higher data rate of 106 kilobits per second for RFID systems operating at the 13.56 MHz carrier frequency.

Finally, the type of modulation applied to data signals in a given RFID system

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is also characteristic of the given RFID system. Among the different modulation types available to RFID systems are frequency shift keying (FSK), phase shift keying (PSK) and amplitude shift keying (ASK).

As a rule, the circuitry of the reader is more extensive and complex than the circuitry of the transponder because the reader requires a higher degree of functionality relative to the transponder, particularly in the case of a passive transponder. Whereas most of the functionality of the transponder can normally be contained within a single integrated circuit, the diverse functionality of the reader typically requires a plurality of separate and discrete non-integrated (i.e., external) electronic components. For example, Figures 1-3 and 6 and the associated text of the '188 Patent disclose separate specific hardware for generating an excitation signal transmitted into the surrounding space from a reader antenna which enables powering up of nearby passive transponders. The '188 Patent also discloses separate specific hardware for detecting transponder data signals from among the signals received from the surrounding space on the reader antenna, for conditioning the transponder data signals received from the surrounding space when detected, and for demodulating the resulting conditioned transponder data signals, respectively, to read the data contained in the transponder signal.

The '263 Patent refines the reader circuitry of the '188 Patent by integrating certain electronic components of the reader circuitry of the '188 Patent, such as decoders and drivers, into a single-chip microcontroller. In accordance with the '263 Patent, operation of the reader comprises receiving a transponder data signal on the reader antenna and feeding the transponder data signal to a multi-stage band pass amplifier downstream of the reader antenna and upstream of the microcontroller. The multiple stages of the band pass amplifier condition, i.e., filter and amplify, the transponder data signal. The resulting conditioned transponder data signal is passed to the microcontroller where the data contained in the transponder data signal is read.

Although the design of the reader disclosed in the '263 Patent realizes some economies of size and cost over the prior art by integrating a plurality of electronic components and their functionalities into the microcontroller of the reader, the use of

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an external multi-stage band pass amplifier limits the practicality of the reader for universal applications. In order to universally adapt the reader of the '263 Patent to the multiplicity of different available carrier frequencies, data rates, and modulation types recited above, the reader would require a separate external multi-stage receiver for each variation of carrier frequency, data rate, and modulation type, respectively. It is readily apparent that a universal reader based on the reader design of the '263 Patent would require many additional external receiver components, thereby offsetting any advantage gained by integrating other reader components and functionalities into the reader microcontroller.

The present invention disclosed hereafter recognizes the particular desirability of eliminating the external multi-stage band pass amplifier in the circuitry of the reader or at least reducing the number of stages of the band pass amplifier so that the reader more efficiently accommodates a range of carrier frequencies, data rates, and modulation types for signals received by the reader. The present invention also recognizes the desirability of integrating the functionalities of other electrical components into the microcontroller of the reader in addition to or in the alternative to those disclosed in the '263 Patent. For example, the present invention recognizes the specific desirability of integrating power conservation functionalities into the microcontroller of the reader.

U.S. Patent 6,476,708 to Johnson (the '708 Patent) discloses a reader having relatively low power consumption requirements. Low power consumption is a particularly advantageous characteristic for a reader, which is powered by a self-contained portable power source within the reader, such as a small disposable or rechargeable battery. Use of the self-contained power source enables a user to position the reader in a remote location which lacks access to an ac power line or an ac power outlet. A battery, however, has a finite life necessitating replacement of the battery in the reader at the end of its useful life, which is both costly and time consuming. Accordingly, it is desirable to reduce the power demands on the battery during operation, thereby extending the useful life of the battery.

The reader of the '708 Patent includes an excitation signal generator circuit,

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transponder detection circuit coupled to the excitation signal generator circuit, and a power source in the form of a small portable battery. The excitation signal generator circuit unit initially operates in a reduced power state effected by drawing reduced electrical current from the power source. The excitation signal generator circuit
5 generates ring signals containing analog data in response to the reduced electrical current. The ring signals are transmitted from a reader antenna and the ring signals propagate into the space surrounding the reader, but are insufficient to power operation of any transponders residing in the surrounding space.

The transponder detection circuit consists of hardware which monitors the level
10 of a transponder detection parameter embodied in the analog data of the ring signals. When the transponder detection circuit determines that the transponder detection parameter has passed a threshold level due to the presence of a transponder in the surrounding space, the transponder detection circuit switches the excitation signal generator circuit from the reduced power state to an increased power state and
15 generation of the ring signals is terminated. The excitation signal generator circuit draws increased electrical current from the power source in the increased power state to generate an excitation signal which is sufficient to power the transponder. The excitation signal is transmitted by the reader and received by the transponder to power the transponder circuitry. The transponder circuitry in turn generates a transponder
20 data signal containing digital data, which is transmitted to the reader. The reader reads the digital data contained in the transponder data signal and the excitation signal generator circuit switches back to the reduced power state, resuming generation of the ring signals while terminating generation of the excitation signal. It is apparent that the duty cycle of the excitation signal generator circuit is significantly lower when operating
25 in the reduced power state than when operating in the increased power state. As a result, the life of the power source is greatly extended and more electrical power is available to the other operations of the reader.

As such, the present invention recognizes a need for a reader which integrates many reader functionalities, including reader power conservation and other analog and
30 digital data acquisition and processing, into a reader microcontroller to realize

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economies of size and/or cost while maintaining or enhancing reader performance. Accordingly, it is generally an object of the present invention to integrate a plurality of reader functionalities into a reader microcontroller. It is generally another object of the present invention to realize economies of size and/or cost over prior art reader designs while maintaining or enhancing reader performance. More particularly, it is an object of the present invention to integrate certain power conservation functionalities of the reader into a reader microcontroller. It is a further object of the present invention to integrate other analog and digital data acquisition and processing functionalities of the reader into a reader microcontroller. It is another object of the present invention to eliminate the external multi-stage band pass amplifier altogether or to at least reduce the number of stages of the external multi-stage band pass amplifier in the circuitry of the reader. It is yet another object of the present invention to substitute lower cost and simpler electronics for the external multi-stage band pass amplifier in the circuitry of the reader, which produce suitable input signals for processing by an integrated microcontroller of the reader. It is a still further object of the present invention to readily accommodate a range of carrier frequencies, data rates, and modulation types for signals received by the reader. These objects and others are accomplished in accordance with the invention described hereafter.

SUMMARY OF THE INVENTION

The present invention is a reader for an RFID system. The reader includes a signal generator for generating a detection signal containing analog data, preferably when operating in a reduced power state, and for generating an excitation signal, preferably when operating in an increased power state. A transmitting antenna is coupled with the signal generator for transmitting the detection signal and the excitation signal into a space surrounding the transmitting antenna. A receiving antenna is provided for receiving a transponder data signal from a transponder in the space, wherein the transponder data signal is at a voltage value and contains digital data. The receiving antenna and the transmitting antenna can both be included in a single dual-

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function antenna if desired.

The reader preferably further includes a transmitting tuning capacitor paired with the transmitting antenna and a receiving tuning capacitor paired with the receiving antenna to tune the respective paired antenna to a predetermined carrier frequency.

5 When the receiving antenna and transmitting antenna are both included in a single dual-function antenna, the receiving tuning capacitor and transmitting tuning capacitor are likewise both preferably included in a single dual-function tuning capacitor paired with the single dual-function antenna.

10 In accordance with one embodiment, two or more receiving and transmitting antenna pairs or dual-function antennas are provided in the reader. Each antenna pair or dual-function antenna has a corresponding receiving and transmitting tuning capacitor pair or dual-function tuning capacitor, respectively, which tunes the associated antenna pair or dual-function antenna to a carrier frequency different than the carrier frequencies to which the remaining antenna pairs or dual-function antennas are tuned.

15 Receiver electronics are coupled with the receiving antenna for conditioning the transponder data signal to place the transponder data signal in a condition for reading the digital data. An internal power source, which has a declining power level as a function of use, is provided for supplying electrical operating power to the reader. The reader further includes a single-chip microcontroller coupled with the internal power source and the receiver electronics. The single-chip microcontroller includes an analog to digital converter to measure the declining power level of the internal power source, to acquire the analog data from the detection signal and the digital data from the transponder data signal and to convert the analog data from the detection signal to converted digital data. The single-chip microcontroller preferably further includes a demodulator, which is more preferably software and/or firmware based, for demodulating the transponder data signal to read the digital data from the transponder data signal.

25 The reader preferably further includes a sample and hold circuit having one or more sample times for isolating points on the detection signal where the analog data

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is to be acquired and for isolating points on the transponder data signal where the digital data is to be acquired. In accordance with one embodiment, the sample and hold circuit is included in the analog to digital converter of the single-chip microcontroller. The microcontroller controls the one or more sample times of the sample and hold circuit and adjusts the one or more sample times in response to different values of carrier frequency, data rate, and/or modulation type of the transponder data signal. The microcontroller also adjusts the one or more sample times to enable transponder detection from a limited sampling of detection signals.

The receiver electronics preferably includes a receiver electronics input from the receiving antenna, a receiver electronics output to the single-chip microcontroller, and a plurality of relatively low-cost simple electrical components selected from the group consisting of resistors, diodes, capacitors, and electrical switches, and preferably excludes relatively high-cost complex multi-stage band pass amplifiers. In accordance with a first embodiment, the receiver electronics includes a resistor divider section comprising first and second series resistors at the receiver electronics input forming a voltage divider to reduce the voltage value of the transponder data signal. The resistor divider section also comprises third and fourth series resistors downstream of the first and second series resistors positioned between ground and the power supply and a blocking capacitor positioned in parallel with the second series resistor upstream of the third and fourth series resistors to maintain the transponder data signal at the receiver electronics output in a voltage range between about ground and the power supply, inclusive.

In accordance with a second embodiment, the receiver electronics includes a peak detector section comprising a rectifier at the receiver electronics input to rectify the voltage value of the transponder data signal. The peak detector section further comprises a pair of series resistors downstream of the rectifier, which are positioned between ground and the power supply, and a blocking capacitor, which is positioned between the rectifier and the pair of series resistors, to maintain the transponder data signal at the receiver electronics output in a voltage range between about ground and the power supply, inclusive. The rectifier preferably includes a diode. The peak

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detector section preferably further comprises a detector capacitor and a detector resistor, wherein the detector capacitor and detector resistor are positioned in parallel with one another and in parallel with the blocking capacitor downstream of the diode and upstream of the pair of series resistors.

5 In accordance with a third embodiment, the receiver electronics includes an integrator section comprising a rectifier and an integrator in series at the receiver electronics input and coupled with the receiver electronics output. The receiver electronics output is coupled with the analog to digital converter. The rectifier preferably includes a diode. The integrator preferably includes an integrator resistor and integrator capacitor in series with the diode. The integrator section preferably further comprises a paired grounding switch resistor and a grounding switch in series with one another and in parallel with the integrator capacitor downstream of the integrator resistor. The paired grounding switch resistor and grounding switch couple the integrator capacitor with ground when the grounding switch is closed and couple the integrator capacitor with the analog to digital converter when the grounding switch is open. The integrator section preferably still further comprises a charging switch in series with the integrator capacitor and ground. The charging switch couples the integrator capacitor with the receiving antenna when the charging switch is closed and decouples the integrator capacitor from the receiving antenna when the charging switch is open.

20 All three of the above-recited embodiments can be utilized together in combination as the reader receiver electronics. Alternatively, any two selected embodiments can be utilized in combination as the reader receiver electronics while excluding the remaining embodiment from the receiver electronics. In yet another alternative, only one selected embodiment can be utilized as the reader receiver electronics while excluding the remaining two embodiments from the receiver electronics.

25 The present invention is also a method for operating a reader for an RFID system. The method is initiated by generating a detection signal containing analog data during a detection mode of operation which preferably has a reduced power state. The

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detection signal is transmitted from a transmitting antenna into a space surrounding the transmitting antenna to detect a proximal transponder. The detection mode is preferably terminated when the proximal transponder is detected and an excitation mode of operation is initiated which preferably has an increased power state. An excitation signal is generated in the excitation mode and transmitted from the transmitting antenna into the surrounding space to power up the proximal transponder. A transponder data signal is generated by the proximal transponder in response to the excitation signal and propagated through the space from the proximal transponder. The transponder data signal is received at the reader with a receiving antenna. The transponder data signal is at a voltage value and contains digital data.

The transponder data signal is conditioned with receiver electronics coupled with the receiving antenna to place the transponder data signal in a condition for reading the digital data. The receiving antenna and transmitting antenna can both be included in a single dual-function antenna.

An analog to digital converter in a single-chip microcontroller is coupled with the receiver electronics and with an internal power source supplying electrical operating power to the reader. The analog to digital converter measures the power level of the internal power source, which is declining as a function of use. The analog to digital converter additionally acquires the analog data from the detection signal and converts the analog data to converted digital data for use in the detection mode. The analog to digital converter also acquires the digital data from the transponder data signal for use in a signal reading mode of operation. The single-chip microcontroller preferably contains specific software and/or firmware to demodulate the transponder data signal and read the digital data from the transponder data signal in the signal reading mode of operation.

In accordance with a first embodiment, the transponder data signal is conditioned with the receiver electronics by reducing the voltage value of the transponder data signal and maintaining the transponder data signal in a voltage range between about ground and a power supply for the reader, inclusive. In accordance with a second embodiment, the transponder data signal is conditioned with the receiver

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electronics by rectifying the voltage value of the transponder data signal and maintaining the transponder data signal in a voltage range between about ground and a power supply for the reader, inclusive. In accordance with a third embodiment, the transponder data signal is conditioned with the receiver electronics by rectifying the voltage value of the transponder data signal and integrating the transponder data signal over one or more cycles of a carrier frequency of the transponder data signal.

The method may further include isolating points on the detection signal where the analog data is to be acquired from the detection signal with a sample and hold circuit having one or more sample times. The sample and hold circuit can also isolate points on the transponder data signal where the digital data is to be acquired. The sample and hold circuit is preferably included in the analog to digital converter of the single-chip microcontroller. The microcontroller controls the one or more sample times of the sample and hold circuit and adjusts the one or more sample times to enable transponder detection from a limited sampling of detection signals. The microcontroller also adjusts the one or more sample times in response to different values of carrier frequency, data rate, and/or modulation type of the transponder data signal.

The present invention will be further understood from the drawings and the following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of an RFID system employing the reader of the present invention.

Figure 2 is a schematic view of a first conditioning circuit having utility in the receiver electronics of the reader of Figure 1.

Figure 3 is a schematic view of a second conditioning circuit having utility in the receiver electronics of the reader of Figure 1.

Figure 4 is a schematic view of a third conditioning circuit having utility in the receiver electronics of the reader of Figure 1.

DESCRIPTION OF PREFERRED EMBODIMENTS

Referring initially to Figure 1, a conceptualized embodiment of an RFID system is shown and generally designated 10. The RFID system 10 comprises a transponder 12 and a reader 14. The reader 14 is a preferred embodiment of a reader of the present invention and is described in greater detail hereafter.

The embodiment of the transponder shown herein is a passive device. As such, the transponder 12 is not physically coupled with an electrical power supply. The electrical power required to operate the transponder 12 is indirectly supplied to the transponder 12 by electromagnetic waves, which are periodically propagated through open space 16 to the transponder 12 from the reader 14. The transponder 12 is only operational when it is receiving electromagnetic waves from the reader 14 of a specific frequency and of sufficient strength to power up the transponder 12.

The transponder 12 includes a transponder integrated circuit (IC) 18 and a transponder antenna 20 coupled with the transponder IC 18. The transponder antenna 20 is a single conventional coil which performs both the receiving and transmitting functions of the transponder 12. Thus, the transponder antenna 20 is termed a “dual-function antenna.” However, the present invention is not limited to an RFID system having a transponder with a single dual-function transponder antenna. The present invention alternately encompasses an RFID system having a transponder with separate receiving and transmitting antennas, which separately perform the receiving and transmitting functions of the transponder.

The transponder IC 18 is preferably a custom IC which satisfies essentially all remaining required transponder functionalities, such as disclosed in the '188 and '574 Patents. The transponder 12 may optionally include an external transponder tuning capacitor 22 coupled with the transponder IC 18 and transponder antenna 20. The term “external” is used herein to designate electronic components which are not physically or functionally included within an integrated circuit. The transponder antenna 20, in cooperation with the transponder tuning capacitor 22, if present, determines the carrier frequency of the transponder 12. In particular, the practitioner sets the carrier

frequency of the transponder 12 by selecting an antenna and optionally a tuning capacitor for the transponder 12, which are tuned to either 125 kHz or 13.56 MHz.

The present transponder 12 is but one example of a type of transponder having utility in the RFID system 10. It is understood that the present invention is not limited to any one specific type of transponder, but is generally applicable to most conventional types of transponders having utility in RFID systems including the different transponder types shown and described in the '188, '574, and '263 Patents. Thus, for example, the transponder 12 can be selected from proximity cards, proximity tags, smart cards, or the like. It is further understood that the RFID system 10 is not limited to RFID systems having only one transponder and one reader as shown. The present RFID system 10 is shown as such primarily for ease of description. In practice, RFID systems having utility in the present invention typically include any number of compatible transponders and can also include a plurality of compatible readers.

The reader 14 comprises a reader signal generator 24, reader receiver electronics 26, a reader microcontroller 28, a reader input/output (I/O) interface 30, and a reader power supply 32. The reader 14 further comprises a reader low frequency antenna 34 and correspondingly paired reader low frequency tuning capacitor 36 and a reader high frequency antenna 38 and correspondingly paired reader high frequency tuning capacitor 40.

The reader power supply 32 is preferably a finite electrical power source which is self-contained (i.e., internal) within the reader 14, such as a relatively small portable battery consisting of one or more disposable dry cells or rechargeable cells. It is noted that the reader 14 is alternatively operable with a power supply which is hard wired to an essentially infinite remote electrical power source, such as an electric utility.

The signal generator 24 includes conventional electronic components similar to those disclosed in the '188 Patent and the '708 Patent for generating relatively low energy electromagnetic waves termed "ring signals" or "detection signals" and for generating relatively high energy electromagnetic waves termed "excitation signals". The signal generator 24 preferably includes electronic components for generating low frequency detection and excitation signals having a frequency of 125 kHz and high

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frequency detection and excitation signals having a frequency of 13.56 MHz.

The signal generator 24 is coupled with the reader low frequency antenna and paired low frequency tuning capacitor 34, 36 to transmit low frequency detection and excitation signals from the signal generator 24 through the open space 16 for reception
5 by any nearby transponders which are tuned to 125 kHz. The signal generator 24 is similarly coupled with the reader high frequency antenna and paired high frequency tuning capacitor 38, 40 to transmit high frequency detection and excitation signals from the signal generator 24 through the open space 16 for reception by any nearby transponders which are tuned to 13.56 MHz.

10 The excitation signals transmitted from the reader 14 typically have a limited range due to size and power constraints of the reader 14. Thus, the reader 14 and transponder 12 of the RFID system 10 are simultaneously operational only when the transponder 12 is within the range of the reader 14 and, more particularly, when the reader 14 and transponder 12 are positioned in relative proximity to one another such
15 that the transponder 12 receives excitation signals of sufficient strength and an appropriate frequency from the reader 14 to power up the transponder 12.

In most conventional RFID systems, the position of the reader is stationary (i.e., constant) relative to the surrounding environment, while the position of the transponder is portable (i.e., variable) within the surrounding environment. In such cases, the user
20 of the RFID system moves the portable transponder into relative proximity with the stationary reader to enable simultaneous operation of the both the transponder and reader. In some conventional RFID systems, however, the position of the reader may be portable relative to the surrounding environment, while the position of the transponder is either portable or stationary. In the case of a portable reader and a
25 stationary transponder, the user moves the portable reader into relative proximity with the stationary transponder to enable simultaneous operation of the both the transponder and reader. In the case of a portable reader and a portable transponder, the user may move both the portable reader and the portable transponder into relative proximity with one another to enable simultaneous operation of the both the
30 transponder and reader. The present invention is not limited to any one of the above-

recited RFID system configurations.

5 The signal generator 24 initially operates in a transponder detection mode. The transponder detection mode is a reduced power state of operation which is effected by periodically drawing reduced electrical current from the reader power supply 32 under the direction of the reader microcontroller 28. The signal generator 24 periodically generates both 125 kHz and 13.56 MHz detection signals containing analog data in response to the reduced electrical current. The 125 KHz detection signals are periodically transmitted from the reader 14 on the reader low frequency antenna 34 and the 13.56 MHz detection signals are periodically transmitted from the reader 14 on the reader high frequency antenna 38. The detection signals are of insufficient strength to power operation of any transponders 12 residing in the surrounding open space 16, but nevertheless propagate into the open space 16 surrounding the reader 14. Propagated detection signals returned to the reader 14 via the reader low and/or high frequency antennas 34, 38 are monitored and evaluated by the reader 14 when operating in the transponder detection mode.

15 The monitoring and evaluating functionalities are integrated into the reader microcontroller 28, which is preferably a single-chip device. An exemplary single-chip microcontroller having utility herein is Model MSP430 available from Texas Instruments, Inc., 12500 TI Boulevard, Dallas, TX 75243-4136. The reader microcontroller 28 also contains an analog to digital converter (ADC) module 42, which preferably includes a conventional sample and hold circuit (not shown). The ADC module 42 has a first ADC input 44 and a second ADC input 46. The first ADC input 44 couples the ADC module 42 with the reader power supply 32. The second ADC input 46 couples the ADC module 42 with the reader receiver electronics 26. The reader receiver electronics 26 are in turn coupled with the reader low frequency antenna and paired low frequency tuning capacitor 34, 36 and with the reader high frequency antenna and paired high frequency tuning capacitor 38, 40 via first and second receiver electronics inputs 48 and 50, respectively.

25 The transponder detection mode functionalities are enabled at least in part by the ADC module 42 and specific software and/or firmware included in the reader

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microcontroller 28. In particular, the ADC module 42 is used to convert the analog data of the detection signals to digital data. The firmware included in the reader microcontroller 28 is then used to identify changes in degree and/or changes in kind within the digital data. The firmware further recognizes which changes in the digital data correspond to changes in one or more selected detection parameters, such as the decay rate or voltage of the detection signals. Changes in one or more of the selected detection parameters indicates the presence of a transponder 12 having a given frequency in the open space 16. It is noted that the firmware of the reader microcontroller 28 preferably does not utilize the relation between analog values of a single detection parameter embodied in the detection signals and a fixed threshold value of the detection parameter as the criteria for determining the presence of a transponder. Instead, the firmware, in cooperation with the ADC module 42 of the reader microcontroller 28, preferably utilizes data trends over time in the digital data extracted from the detection signals, which can correlate to one or more detection parameters, to more efficiently determine the presence of a transponder. Thus, the firmware monitors digital data changes with reference to the preceding digital data to detect a transponder rather than with reference to a fixed threshold value of a detection parameter.

When the reader microcontroller 28 detects a transponder 12 in the above-recited manner, the reader microcontroller 28 switches the signal generator 24 from the transponder detection mode at the reduced power state to a transponder excitation mode at an increased power state of operation. Switching the signal generator 24 to the excitation mode terminates periodic generation of the detection signals of the given frequency and causes the signal generator 24 to draw increased electrical current from the reader power supply 32. The increased draw of electrical current in the excitation mode enables the signal generator 24 to generate an excitation signal of the given frequency under the direction of the reader microcontroller 28. The excitation signal is in the form of an electromagnetic wave, which has sufficient strength to power up the transponder 12.

The transponder antenna 20 has an excitation signal reception range which is

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generally about 4 to 5 inches when the reader and transponder antennas are coaxially aligned. When the transponder 12 and/or reader 14 is moved to a proximal position such that the distance between reader 14 and transponder 12 is within the excitation signal reception range of the transponder antenna 20, the transponder antenna 20
5 receives the excitation signal at a sufficient strength to power up the transponder IC 18, thereby activating the transponder 12.

Upon activation, the transponder IC 18 generates a communication signal termed a transponder data signal, which contains readable information (i.e., digital data) copied or otherwise derived from the memory of the transponder IC 18. The
10 transponder data signal is in the form of an electromagnetic wave like the excitation signal. It is noted that communication signals of RFID systems (i.e., excitation and transponder data signals) are typically termed radio frequency signals. However, the excitation and transponder data signals of the present invention are not limited exclusively to signals having specific frequencies within the narrow "radio frequency"
15 range, as "radio frequency" is commonly defined for the radio communication industry. The transponder 12 transmits the transponder data signal into the open space 16 of the external environment via the transponder antenna 20.

Each of the reader antennas 34, 38 shown is a conventional coil acting as a single dual-function antenna, which performs both the receiving and transmitting
20 functions of the reader 14. In particular, the reader antennas 34, 38 receive the low and high frequency detection signals and the low and high frequency transponder data signals, respectively, from the open space 16 and transmit the low and high frequency detection and excitation signals into the open space 16. However, the present invention is not limited to an RFID system having a reader with dual-function antennas.
25 The present invention alternately encompasses an RFID system having a reader with separate receiving and transmitting antennas, which separately perform the transponder data signal and detection signal receiving functions of the reader and the detection signal and excitation signal transmitting functions of the reader, respectively. In yet another alternative, where a reader is provided with separate receiving and
30 transmitting antennas, the reader transmitting antennas are capable of being adapted

to act as dual-function antennas (i.e., receiving and transmitting) only with respect to the detection signals while the reader transmitting and receiving antennas function separately with respect to the transponder data signals.

Transponder data signal reading components and their corresponding functionality are integrated into the reader microcontroller 28 along with the transponder detection components and the components for activating the excitation mode and their corresponding functionalities described above. The transponder data signal reading functionalities are enabled in part by specific firmware included in the reader microcontroller 28. The receiver electronics receive the low and high frequency transponder data signals for any of a plurality of data rates and modulation types, from the reader antennas 34, 38, via the first and second receiver electronics inputs 48, 50, respectively. The reader receiver electronics 26 "condition" the low and high frequency transponder data signals and thereafter convey them to the ADC module 42 via the second ADC input 46.

The reader microcontroller 28 demodulates the conditioned transponder data signals in accordance with the respective modulation type of the signal to read the data on the signals. The demodulator which performs the demodulation step within the reader microcontroller 28 is preferably based in the firmware and/or software of the reader microcontroller 28 rather than being hardware-based. The resulting data can then be sent to an external device (not shown), such as a central host computer, via the reader I/O interface 30.

The signal conditioning function of the reader receiver electronics 26 places the signals containing analog and digital data of differing carrier frequencies, data rates and modulation types as recited above into a form which enables the integrated reader microcontroller 28 to properly process the entire range of signals. Specific embodiments of the reader receiver electronics 26 are shown and described hereafter with reference to Figures 2-4, which perform the signal conditioning function.

Referring initially to Figure 2, a first conditioning circuit termed a resistor divider section is shown and generally designated 60. The first conditioning circuit 60 has an input node 62 which is coupled with the reader low frequency antenna and paired low

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frequency tuning capacitor 34, 36 via the first receiver electronics input 48 or with the reader high frequency antenna and paired high frequency tuning capacitor 38, 40 via the second receiver electronics input 50 for receiving transponder data signals. The first conditioning circuit 60 also has an output node 64, which is coupled directly with the second ADC input 46 for conveying transponder data signals from the first conditioning circuit 60 to the sample and hold circuit of the ADC module 42, if the sample and hold circuit of the ADC module 42 is fast enough to capture the peak of a 125 kHz or 13.56 MHz transponder data signal. If the sample and hold circuit of the ADC module 42 is not sufficiently fast, an additional sample and hold circuit (not shown) of sufficient speed is provided in series between the output node 64 and the ADC module 42.

The first conditioning circuit 60 contains first and second series resistors 66, 68, third and fourth series resistors 70, 72, and a blocking capacitor 74. The first and second series resistors 66, 68 in combination form a voltage divider which reduces the high voltage of the transponder data signal on the low or high frequency antenna and paired tuning capacitor 34, 36 or 38, 40 to a lower voltage level, which can be input to the ADC module 42 of the reader microcontroller 28. The third and fourth series resistors 70, 72 are positioned in series between ground 76 (0 volts) and the reader power supply 32, which is, for example, 3 volts. The third and fourth series resistors 70, 72 in combination with the blocking capacitor 74, which is in parallel with the second series resistor 68, function to maintain the voltage of the transponder data signal input to the ADC module 42 in a voltage range between ground (i.e., 0 volts in the present example) and the voltage of the reader power supply 32 (i.e., 3 volts in the present example), inclusive.

In a preferred embodiment, a separate first conditioning circuit 60 is provided for each reader receiving antenna and paired tuning capacitor, which are coupled with the first conditioning circuit 60. Since the first conditioning circuit 60 contains only four resistors and one capacitor, while avoiding use of a multi-stage band pass amplifier, the first conditioning circuit 60 is a simple yet effective means for conditioning the transponder data signal. In many cases, the resulting transponder data signal has an

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acceptable voltage for inputting to the ADC module 42 of the reader microcontroller 28 and for processing by the reader microcontroller 28 in the manner recited herein.

As stated above, the first conditioning circuit 60 is effective for its intended purpose. However, in some cases the voltage reduction of the transponder data signal by the voltage divider can be disadvantageous. Referring to Figure 3, a second conditioning circuit is shown and generally designated 80, which is an alternate embodiment or a supplemental embodiment of the reader receiver electronics 26 relative to the above-recited embodiment of the reader receiving electronics designated as the first conditioning circuit 60. The second conditioning circuit 80 avoids voltage reduction of the transponder data signal.

Components which are common to both the first and second conditioning circuits 60, 80 are designated in Figures 2 and 3 by the same reference characters. The second conditioning circuit 80, termed a peak detector section, differs from the first conditioning circuit 60 by only a few components. In particular, the first series resistor 66 of the first conditioning circuit 60 is replaced in the second conditioning circuit 80 with a diode 82 and a second capacitor 84 in parallel with the second series resistor 68. In all other respects, the first and second conditioning circuits 60, 80 are identical. The diode 82 rectifies the voltage of the transponder data signal obtained from the low or high frequency antenna and paired tuning capacitor 34, 36 or 38, 40 and functions in combination with the second capacitor 84 as a peak voltage detector for the transponder data signal. Although only a single diode 82 is shown in the present embodiment of the second conditioning circuit 80, it is understood that in practice the second conditioning circuit 80 can employ multiple diodes for the rectifying and peak voltage detection functions.

In a preferred embodiment, a separate second conditioning circuit 80 is provided for each reader receiving antenna and paired tuning capacitor, which are coupled with the second conditioning circuit 80. Like the first conditioning circuit 60, the second conditioning circuit 80 avoids use of a multi-stage band pass amplifier, while providing a simple yet effective means for conditioning the transponder data signal. In many cases, the resulting transponder data signal is acceptable for inputting to the ADC

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module 42 of the reader microcontroller 28 and for processing by the reader microcontroller 28 in the manner recited herein.

In some cases, the reader microcontroller 28 is relatively slow running, i.e., is not fast enough to keep pace with a high frequency transponder data signal. Referring to Figure 4, a third conditioning circuit is shown and generally designated 90, which provides a solution to this problem. The third conditioning circuit 90 is termed an integrator section because the third conditioning circuit 90 integrates the transponder data signal over one or more cycles of the carrier frequency before inputting the resulting integrated transponder data signal to the ADC module 42 of the reader microcontroller 28.

Components which are common to the first, second and third conditioning circuits 60, 80, 90 are designated in Figures 2-4 by the same reference characters. As such, the third conditioning circuit 90 has an input node 62 which is coupled with the reader low frequency antenna and paired low frequency tuning capacitor 34, 36 via the first receiver electronics input 48 or with the reader high frequency antenna and paired high frequency tuning capacitor 38, 40 via the second receiver electronics input 50 for receiving transponder data signals. The third conditioning circuit 90 further comprises in series a diode 82 and an integrator resistor 94 downstream of the input node 62. An integrator capacitor 96, a charging switch 98, a grounding switch 100, and a grounding switch resistor 102 are provided downstream of the integrator resistor 94. The integrator capacitor 96 and charging switch 98 are in series with one another and the grounding switch 100 and grounding switch resistor 102 are in series with one another, respectively. However, the series paired integrator capacitor and charging switch 96, 98 are in parallel with the series paired grounding switch and grounding switch resistor 100, 102. Both the charging switch 98 and grounding switch 100 are preferably electronic switches.

The charging switch 98 couples the integrator capacitor 96 with the input node 62 when the charging switch 98 is closed and decouples the integrator capacitor 96 from the input node 62 when the charging switch 98 is open. The grounding switch 100 couples the integrator capacitor 96 with ground 76 when the grounding switch 100 is

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closed and couples the integrator capacitor 96 with the output node 64 when the grounding switch 100 is open. As recited above, the output node 64 is coupled directly with the second ADC input 46 for conveying integrated transponder data signals from the integrator capacitor 96 to the ADC module 42.

5 The diode 82 rectifies the voltage of the transponder data signal obtained from the reader low or high frequency antenna and paired tuning capacitor 34, 36 or 38, 40. Although only a single diode 82 is shown in the present embodiment of the third conditioning circuit 90, it is understood that in practice the third conditioning circuit 90 can employ multiple diodes for the rectifying function. The integrator resistor 94 and
10 integrator capacitor 96 in combination form an integrator which integrates the transponder data signal over one or more cycles of the carrier frequency. After the sample and hold circuit of the ADC module 42 has sampled and held a voltage on the integrator capacitor 96, the grounding switch 100 is closed to remove the charge from the integrator capacitor 96 through the relatively small grounding switch resistor 102
15 and initialize the integrator 94, 96. The grounding switch 100 is then opened for the next integration and the cycle is repeated.

 The charging switch 98 controls over which cycles of the carrier frequency the integration is performed. The integrator capacitor 96 can only be charged when the charging switch 98 is closed. Accordingly, the charging switch 98 is closed for cycles
20 of the carrier frequency over which it is desired to perform the integration and is opened for cycles of the carrier frequency over which it is not desired to perform the integration. Although not shown, it is within the scope of the present invention to alternatively position the charging switch 98 between the input node 62 and the diode 82, between the diode 82 and the integrator resistor 94, or between the integrator resistor 94 and
25 the integrator capacitor 96. Any of these alternate positions of the charging switch 98 will not modify its function as recited above.

 In a preferred embodiment, a separate third conditioning circuit 90 is provided for each reader receiving antenna and paired tuning capacitor, which are coupled with the third conditioning circuit 90. Like the first and second conditioning circuits 60, 80,
30 the third conditioning circuit 90 avoids use of a multi-stage band pass amplifier, while

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providing a simple yet effective means for conditioning the transponder data signal. In many cases the resulting transponder data signal is acceptable for inputting to the ADC module 42 of the reader microcontroller 28 and for processing by the reader microcontroller 28 in the manner recited herein.

5 All three types of conditioning circuits, i.e., the first, second and third conditioning circuits 60, 80, 90, can be utilized together in combination as the reader receiver electronics 26. Alternatively, any two types of the conditioning circuits can be utilized in combination as the reader receiver electronics 26 while excluding the remaining type of conditioning circuit from the reader receiver electronics 26. In yet another
10 alternative, only one type of conditioning circuit can be utilized as the reader receiver electronics 26 while excluding the remaining two types of conditioning circuits from the reader receiver electronics 26. Selection of the specific conditioning circuits recited herein for use in the reader receiver electronics 26 is within the purview of the skilled artisan, being a function of the particular requirements of the reader microcontroller 28 and the character of the signals received by the reader antennas 34, 38.
15

Use of one or more of the above-recited conditioning circuits 60, 80, 90 in combination with the integrated reader microcontroller 28 as recited herein enables the reader 14 to effectively acquire and process analog data from detection signals having a plurality of different frequency characteristics during a transponder detection mode
20 of operation; while simultaneously effectively acquiring and processing digital data from transponder data signals having a plurality of different carrier frequency, data rate and modulation characteristics during a signal reading mode of operation.

In accordance with the transponder detection mode, nearby transponders are detected when specified digital data extracted from the detection signals, which are
25 transmitted from the reader antennas 34, 38, changes, as measured by the ADC module 42 at a set sampling time or times. The transponder detection mode is optimized by careful selection or adjustment of the sampling time or times of the ADC module 42 of the reader microcontroller 28 to enable transponder detection from only a limited sampling of detection signals.

30 The signal reading mode is also optimized by careful selection or adjustment of

the sampling time or times of the ADC module 42 of the reader microcontroller 28 in accordance with the carrier frequencies, data rates, and modulation types. Efficient microcontroller firmware instructions are then used to locate bit transitions in the data of the ADC module 42 and recover the bits transmitted to the reader 14 from the transponder 12. A specific sequence of bits stored in a specific location in the transponder 12 is received by the reader 14 and used to assist in synchronization of the reader microcontroller 28 with bit transitions from the transponder 12. For example, a specific bit sequence transmitted by the transponder 12 to the reader 14 is the sequence 00110101, wherein the leftmost bit is transmitted first by the transponder 12.

As noted, all of the above-recited conditioning circuits advantageously contain only simple and low-cost electronic components such as diodes, resistors, capacitors, electronic switches and the like. Use of the specific reader receiver electronics 26 disclosed herein in combination with the ADC module 42 of the reader microcontroller 28 and its associated firmware enables the practitioner to preferably avoid the inclusion of costly and complex multi-stage band pass amplifiers in the reader design or at least reduce the number of stages in the band pass amplifiers, if a band pass amplifier is retained.

The conditioning circuits and integrated reader microcontroller recited herein further enable the above-recited reader operations while efficiently conserving reader power. Reduced power consumption is effected by reducing the number of electronic components in the reader design and by directing the powering off of certain reader modules or components during periods of non-use. An efficient instruction set from the reader microcontroller 28 can also reduce power consumption by minimizing the oscillator frequency used to process data in real time.

Another functional feature of the reader 14 is the capability of monitoring the status of the reader power supply 32 simultaneous with the data acquisition and processing functions so that the user can estimate the time of reliable reader operation remaining before it is necessary to replace or recharge the power supply 32. This feature is enabled by the ADC module 42 of the reader microcontroller 28, which periodically measures the voltage of the reader power supply 32. The measured

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voltage value or a status message is subsequently communicated to the user or to an external device via the reader I/O interface 30.

While the forgoing preferred embodiments of the invention have been described and shown, it is understood that alternatives and modifications, such as those suggested and others, may be made thereto and fall within the scope of the invention.

5

**GLOSSARY OF DRAWING TERMS
ATTORNEY DOCKET NO. 038P0401**

10 RFID system
12 transponder
14 reader
16 open space
18 transponder integrated circuit (IC)
20 transponder antenna
22 transponder tuning capacitor
24 reader signal generator
26 reader receiver electronics
28 reader microcontroller
30 reader input/output (I/O) interface
32 reader power supply
34 reader low frequency antenna
36 reader low frequency tuning capacitor
38 reader high frequency antenna
40 reader high frequency tuning capacitor
42 analog to digital converter (ADC) module
44 first ADC input
46 second ADC input
48 first receiver electronics input
50 second receiver electronics input

60 first conditioning circuit
62 input node
64 output node
66 first resistor
68 second resistor
70 third resistor
72 fourth resistor
74 blocking capacitor
76 ground

80 second conditioning circuit
82 diode
84 second capacitor

90 third conditioning circuit
94 integrator resistor
96 integrator capacitor
98 charging switch
100 grounding switch
102 grounding switch resistor

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I claim:

1. A reader for an RFID system comprising:

a signal generator for generating a detection signal containing analog data and for generating an excitation signal;

5 a transmitting antenna coupled with said signal generator for transmitting said detection signal and said excitation signal into a space surrounding said transmitting antenna;

a receiving antenna for receiving a transponder data signal at a voltage value containing digital data from a transponder in said space;

10 receiver electronics coupled with said receiving antenna for conditioning said transponder data signal to place said transponder data signal in a condition for reading said digital data;

an internal power source for supplying electrical operating power to said reader, said internal power source having a declining power level as a function of use; and

15 a single-chip microcontroller coupled with said internal power source and said receiver electronics, said single-chip microcontroller including an analog to digital converter to acquire said analog data from said detection signal and said digital data from said transponder data signal and to convert said analog data from said detection signal to converted digital data.

20 2. The reader of claim 1, wherein said receiver electronics includes a receiver electronics input from said receiving antenna, a receiver electronics output to said single-chip microcontroller, and a plurality of relatively low-cost simple electrical components selected from the group consisting of resistors, diodes, capacitors, and electrical switches, and excludes relatively high-cost complex multi-stage band pass
25 amplifiers.

3. The reader of claim 1, wherein said single-chip microcontroller further includes a software and/or firmware-based demodulator for demodulating said transponder data signal to read said digital data from said transponder data signal.

30 4. The reader of claim 1, wherein said receiving antenna and said transmitting antenna are both included in a single dual-function antenna.

5 5. The reader of claim 2, wherein said receiver electronics includes a resistor divider section comprising first and second series resistors at said receiver electronics input forming a voltage divider to reduce said voltage value of said transponder data signal and third and fourth series resistors downstream of said first and second series resistors positioned between ground and said power supply and a blocking capacitor positioned in parallel with the second series resistor upstream of said third and fourth series resistors to maintain said transponder data signal at said receiver electronics output in a voltage range between about ground and said power supply, inclusive.

10 6. The reader of claim 2, wherein said receiver electronics includes a peak detector section comprising a rectifier at said receiver electronics input to rectify said voltage value of said transponder data signal and a pair of series resistors downstream of said rectifier positioned between ground and said power supply and a blocking capacitor positioned between said rectifier and said pair of series resistors to maintain said transponder data signal at said receiver electronics output in a voltage range
15 between about ground and said power supply, inclusive.

20 7. The reader of claim 6, wherein said rectifier includes a diode and said peak detector section further comprises a detector capacitor and a detector resistor, said detector capacitor and detector resistor positioned in parallel with one another and in parallel with said blocking capacitor downstream of said diode and upstream of said pair of series resistors.

25 8. The reader of claim 2, wherein said receiver electronics includes an integrator section comprising a rectifier and an integrator in series at said receiver electronics input and coupled with said receiver electronics output, said receiver electronics output coupled with said analog to digital converter.

30 9. The reader of claim 8, wherein said rectifier includes a diode and said integrator includes an integrator resistor and integrator capacitor in series with said diode, said integrator section further comprising a paired grounding switch resistor and grounding switch in series with one another and in parallel with said integrator capacitor downstream of said integrator resistor, said paired grounding switch resistor and grounding switch coupling said integrator capacitor with ground when said grounding

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switch is closed and coupling said integrator capacitor with said analog to digital converter when said grounding switch is open.

10. The reader of claim 8, wherein said rectifier includes a diode and said integrator includes an integrator resistor and integrator capacitor in series with said diode, said integrator section further comprising a charging switch in series with said integrator capacitor and ground, said charging switch coupling said integrator capacitor with said receiving antenna when said charging switch is closed and decoupling said integrator capacitor from said receiving antenna when said charging switch is open.

11. The reader of claim 1, wherein said reader further comprises a sample and hold circuit having one or more sample times for isolating points on said detection signal where said analog data is to be acquired and for isolating points on said transponder data signal where said digital data is to be acquired.

12. The reader of claim 11, wherein said sample and hold circuit is included in said analog to digital converter of said single-chip microcontroller.

13. The reader of claim 11, wherein said microcontroller controls said one or more sample times of said sample and hold circuit and adjusts said one or more sample times in response to different values of carrier frequency, data rate, and/or modulation type of said transponder data signal.

14. The reader of claim 11, wherein said microcontroller controls said one or more sample times of said sample and hold circuit and adjusts said one or more sample times to enable detection of a transponder from a limited sampling of detection signals.

15. The reader of claim 5, wherein said receiver electronics further includes a peak detector section comprising a rectifier at said receiver electronics input to rectify said voltage value of said transponder data signal and a pair of series resistors downstream of said rectifier positioned between ground and said power supply and a blocking capacitor positioned between said rectifier and said pair of series resistors to maintain said transponder data signal at said receiver electronics output in a voltage range between about ground and said power supply, inclusive.

16. The reader of claim 15, wherein said rectifier includes a diode and said

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peak detector section further comprises a detector capacitor and a detector resistor, said detector capacitor and detector resistor positioned in parallel with one another and in parallel with said blocking capacitor downstream of said diode and upstream of said pair of series resistors.

5 17. The reader of claim 5, wherein said receiver electronics further includes an integrator section comprising a rectifier and an integrator in series at said receiver electronics input and coupled with said receiver electronics output, said receiver electronics output coupled with said analog to digital converter.

10 18. The reader of claim 17, wherein said rectifier includes a diode and said integrator includes an integrator resistor and integrator capacitor in series with said diode, said integrator section further comprising a paired grounding switch resistor and grounding switch in series with one another and in parallel with said integrator capacitor downstream of said integrator resistor, said paired grounding switch resistor and grounding switch coupling said integrator capacitor with ground when said grounding
15 switch is closed and coupling said integrator capacitor with said analog to digital converter when said grounding switch is open.

19. The reader of claim 17, wherein said rectifier includes a diode and said integrator includes an integrator resistor and integrator capacitor in series with said diode, said integrator section further comprising a charging switch in series with said
20 integrator capacitor and ground, said charging switch coupling said integrator capacitor with said receiving antenna when said charging switch is closed and decoupling said integrator capacitor from said receiving antenna when said charging switch is open.

20. The reader of claim 6, wherein said receiver electronics further includes an integrator section comprising an integrator at said receiver electronics input and
25 coupled with said receiver electronics output, said receiver electronics output coupled with said analog to digital converter.

21. The reader of claim 15, wherein said receiver electronics further includes an integrator section comprising an integrator at said receiver electronics input and
30 coupled with said receiver electronics output, said receiver electronics output coupled with said analog to digital converter.

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22. The reader of claim 1 further comprising a transmitting tuning capacitor paired with said transmitting antenna and a receiving tuning capacitor paired with said receiving antenna.

23. The reader of claim 22, wherein said receiving tuning capacitor and said transmitting tuning capacitor are both included in a single dual-function tuning capacitor.

24. The reader of claim 22, wherein said transmitting tuning capacitor and/or said receiving tuning capacitor is a first tuning capacitor for tuning a first reader antenna to a higher carrier frequency, said reader further comprising a second tuning capacitor for tuning a second reader antenna to a lower carrier frequency,

25. A reader for an RFID system comprising:

a signal generator for generating a detection signal containing analog data and for generating an excitation signal;

a transmitting antenna coupled with said signal generator for transmitting said detection signal and said excitation signal into a space surrounding said transmitting antenna;

a receiving antenna for receiving a transponder data signal at a voltage value containing digital data from a transponder in said space;

receiver electronics coupled with said receiving antenna for conditioning said transponder data signal to place said transponder data signal in a condition for reading said digital data; and

a single-chip microcontroller coupled with said receiver electronics, said single-chip microcontroller including an analog to digital converter to acquire said analog data from said detection signal and said digital data from said transponder data signal and to convert said analog data from said detection signal to converted digital data, said single-chip microcontroller further including a demodulator for demodulating said transponder data signal to read said digital data from said transponder data signal.

26. The reader of claim 25, wherein said receiver electronics includes a receiver electronics input from said receiving antenna, a receiver electronics output to said single-chip microcontroller, and a plurality of relatively low-cost simple electrical

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components selected from the group consisting of resistors, diodes, capacitors, and electrical switches, and excludes one or more relatively high-cost complex multi-stage band pass amplifiers.

27. The reader of claim 25, wherein said receiving antenna and said transmitting antenna are both included in a single dual-function antenna.

28. A method for operating a reader for an RFID system comprising:
generating a detection signal containing analog data in a detection mode of operation;

transmitting said detection signal from a transmitting antenna into a space surrounding said transmitting antenna to detect a proximal transponder;

generating an excitation signal in an excitation mode of operation;

transmitting said excitation signal from said transmitting antenna into said space to power up said proximal transponder;

generating a transponder data signal at said proximal transponder in response to said excitation signal and propagating said transponder data signal through said space from said proximal transponder;

receiving said transponder data signal with a receiving antenna, wherein said transponder data signal is at a voltage value and contains digital data;

conditioning said transponder data signal with receiver electronics coupled with said receiving antenna to place said transponder data signal in a condition for reading said digital data;

coupling an analog to digital converter in a single-chip microcontroller with an internal power source supplying electrical operating power to said reader, said internal power source having a declining power level as a function of use and with said receiver electronics;

coupling said analog to digital converter with said receiver electronics;

acquiring said analog data from said detection signal with said analog to digital converter for use in said detection mode; and

acquiring said digital data from said transponder data signal with said analog to digital converter for use in a signal reading mode of operation.

29. The method of claim 28, wherein said receiver electronics includes a plurality of relatively low-cost simple electrical components selected from the group consisting of resistors, diodes, capacitors, and electrical switches, and excludes one or more relatively high-cost complex multi-stage band pass amplifiers.

5 30. The method of claim 28 further comprising demodulating said transponder data signal with software and/or firmware contained in said single-chip microcontroller to read said digital data from said transponder data signal in said signal reading mode.

31. The method of claim 28, wherein said receiving antenna and said transmitting antenna are both included in a single dual-function antenna.

10 32. The method of claim 28, wherein said transponder data signal is conditioned with said receiver electronics by reducing said voltage value of said transponder data signal and maintaining said transponder data signal in a voltage range between about ground and a power supply for said reader, inclusive.

15 33. The method of claim 28, wherein said transponder data signal is conditioned with said receiver electronics by rectifying said voltage value of said transponder data signal and maintaining said transponder data signal in a voltage range between about ground and a power supply for said reader, inclusive.

20 34. The method of claim 28, wherein said transponder data signal is conditioned with said receiver electronics by rectifying said voltage value of said transponder data signal and integrating said transponder data signal over one or more cycles of a carrier frequency of said transponder data signal.

35. The method of claim 28, further comprising isolating points on said detection signal where said analog data is to be acquired with a sample and hold circuit having one or more sample times.

25 36. The method of claim 28, further comprising isolating points on said transponder data signal where said digital data is to be acquired with a sample and hold circuit having one or more sample times.

37. The method of claim 35, wherein said sample and hold circuit is included in said analog to digital converter of said single-chip microcontroller.

30 38. The method of claim 36, wherein said sample and hold circuit is included

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in said analog to digital converter of said single-chip microcontroller.

39. The method of claim 35, wherein said microcontroller controls said one or more sample times of said sample and hold circuit and adjusts said one or more sample times to enable detection of said proximal transponder from a limited sampling of detection signals.

40. The method of claim 36, wherein said microcontroller controls said one or more sample times of said sample and hold circuit and adjusts said one or more sample times in response to different values of carrier frequency, data rate, and/or modulation type of said transponder data signal.

41. The method of claim 32, wherein said transponder data signal is conditioned with said receiver electronics by rectifying said voltage value of said transponder data signal and maintaining said transponder data signal in a voltage range between about ground and a power supply for said reader, inclusive.

42. The method of claim 41, wherein said transponder data signal is conditioned with said receiver electronics by rectifying said voltage value of said transponder data signal and integrating said transponder data signal over one or more cycles of a carrier frequency of said transponder data signal.

43. The method of claim 32, wherein said transponder data signal is conditioned with said receiver electronics by rectifying said voltage value of said transponder data signal and integrating said transponder data signal over one or more cycles of a carrier frequency of said transponder data signal.

44. The method of claim 28, further comprising terminating said detection mode and initiating said excitation mode when said proximal transponder is detected.

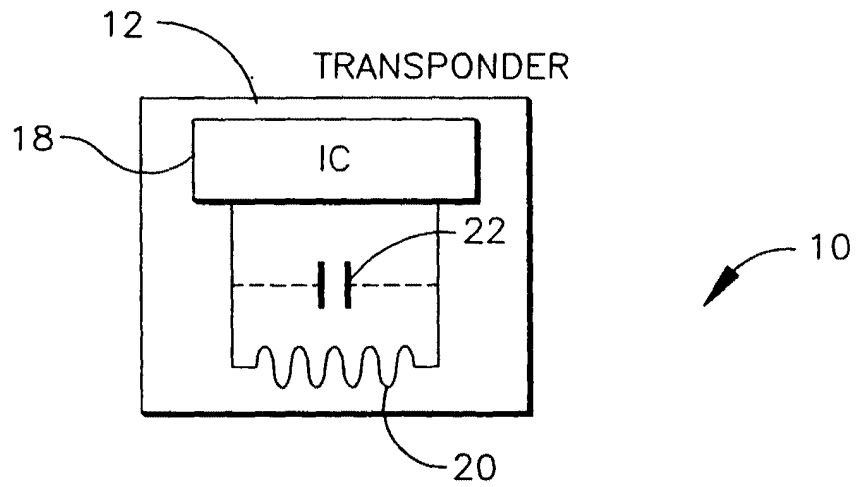
45. The method of claim 28, wherein said detection mode of operation has a reduced power state and said excitation mode of operation has an increased power state.

46. The method of claim 28, further comprising measuring said declining power level of said internal power source with said analog to digital converter.

ABSTRACT

A reader for an RFID system includes an internal power source, a signal generator for generating a detection signal containing analog data and an excitation signal, a transmitting antenna for transmitting the detection and excitation signals, and a receiving antenna for receiving a transponder data signal from a transponder containing digital data. Receiver electronics are coupled with the receiving antenna for conditioning the transponder data signal before reading the digital data. The reader further includes a single-chip microcontroller coupled with the internal power source and the receiver electronics. The single-chip microcontroller has an analog to digital converter to measure the declining power level of the internal power source and to acquire the analog data from the detection signal and the digital data from the transponder data signal. The single-chip microcontroller also includes a firmware and/or software-based demodulator for demodulating the transponder data signal to read the digital data.

1/3



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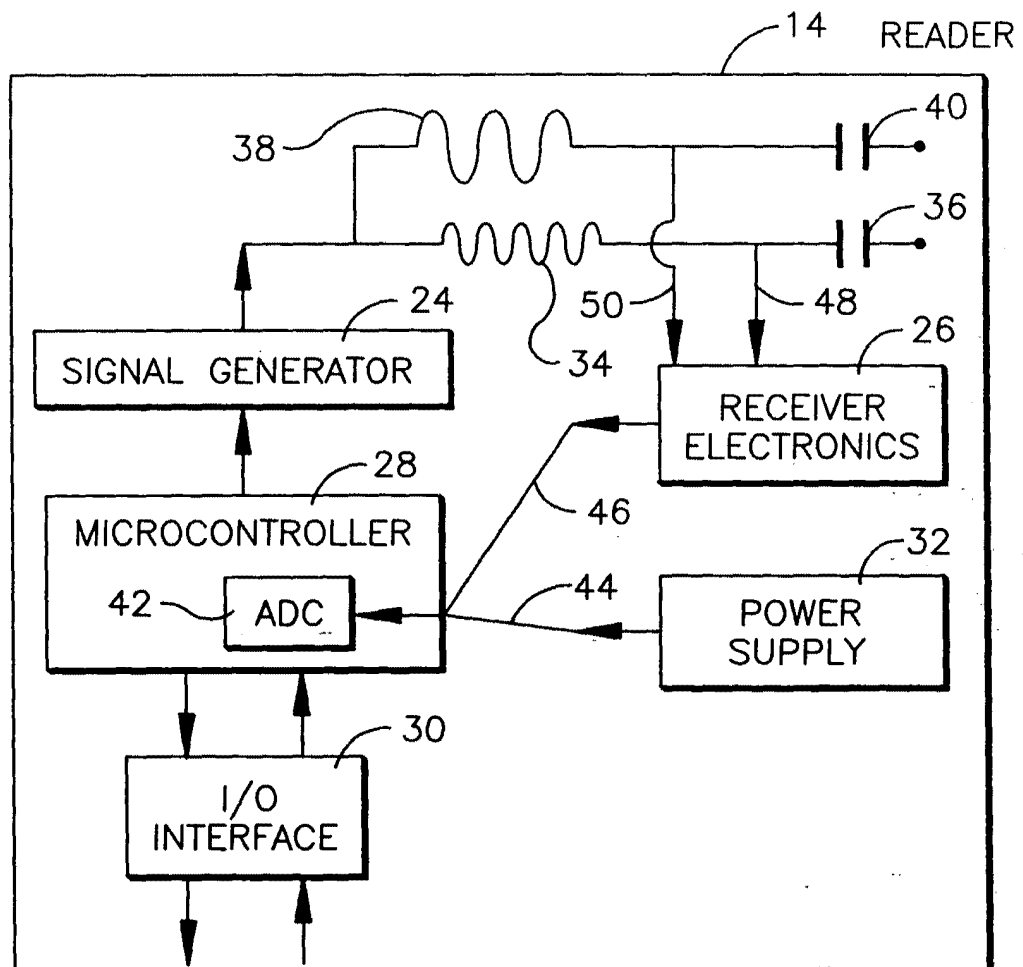


Fig. 1

Fig.2

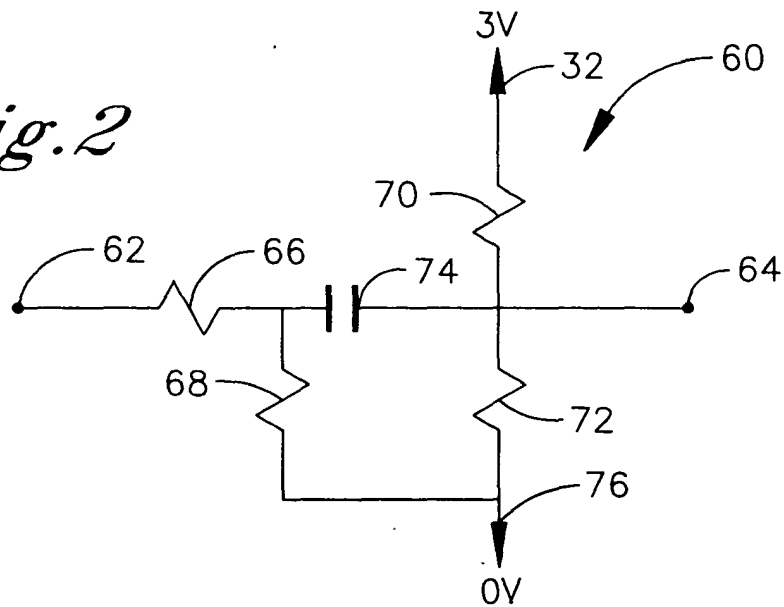


Fig. 3

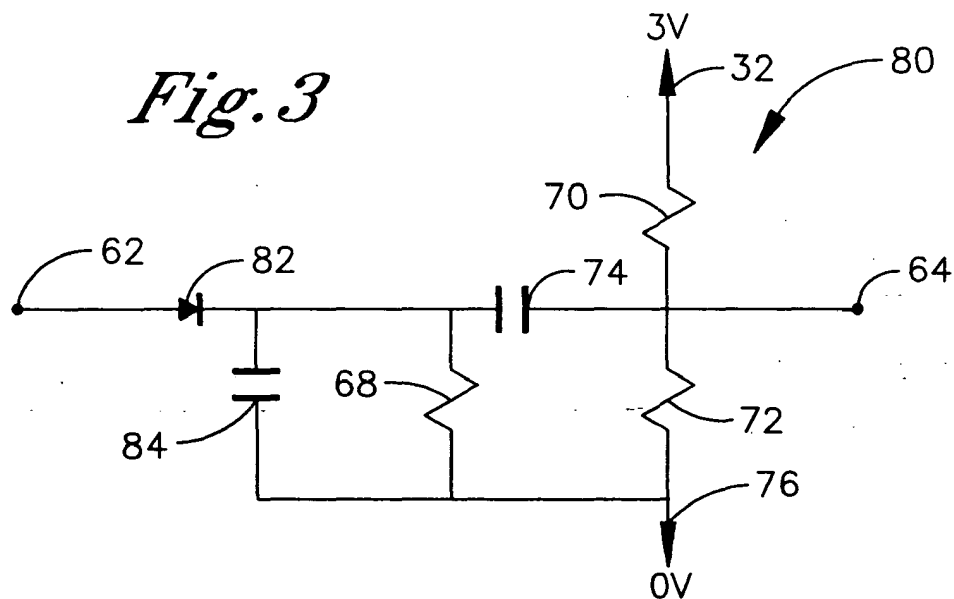
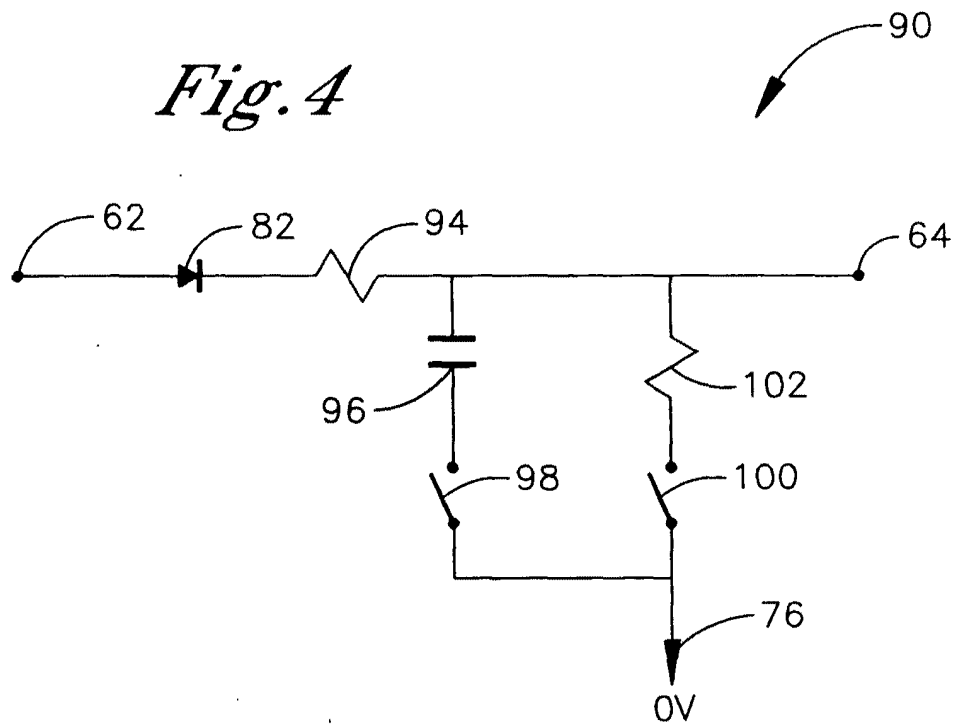


Fig. 4

**COMBINED DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION**

As below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first, and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

RFID Reader Utilizing an Analog to Digital Converter for Data Acquisition and Power Monitoring Functions

the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR §1.56.

As named inventor, I hereby appoint the following practitioner with full power of substitution and revocation to prosecute this application and transact all business in the United States Patent and Trademark Office connected therewith:

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Address all correspondence to: Rodney F. Brown
3365 Baltimore Street
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Phone: (858) 272-8705
Fax: (858) 581-1282

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Full Name of Inventor

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Ralph W. Quan
Title : RFID Reader Utilizing an Analog to Digital Converter for Data Acquisition and Power Monitoring Functions

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P.O. Box 1450
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §1.97 AND §1.98**

Sir:

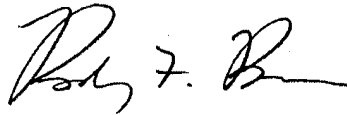
The references listed on the accompanying Form PTO-1449 may be material to the examination of the above-captioned patent application and are therefore disclosed by the applicant in compliance with the duty of disclosure defined in 37 CFR §1.56.

This Information Disclosure Statement, which is submitted in accordance with 37 CFR §§1.97 and 1.98, is not to be construed as a representation that a search has been made, that additional matter material to the examination of this application does not exist, or that any one or more of the references listed on Form PTO-1449 constitutes prior art under 35 U.S.C. §102.

It is requested that the listed references be made of record, if appropriate, in the prosecution of this application.

Copies of all listed references are enclosed.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Rodney F. Brown". The signature is fluid and cursive, with the first name "Rodney" being more prominent.

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RFB:0514d.038
enclosure

FORM PTO-1449

Docket No:
038P0401INFORMATION DISCLOSURE
STATEMENT BY APPLICANTApplicant:
Ralph W. Quan

U.S. PATENT DOCUMENTS

<u>Exam.</u> <u>Initial</u>	<u>Pat./App.</u> <u>Number</u>	<u>Issue/Pub.</u> <u>Date</u>	<u>Inventor</u>	<u>Class</u>	<u>Sub-</u> <u>Class</u>
_____	4,730,188	3/8/88	Milheiser	340	825.0
_____	5,347,263	9/13/94	Carroll et al.	340	572
_____	5,541,574	7/30/96	Lowe et al.	340	447
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_____	20030090367	5/15/03	Carroll et al.	340	10.4

FOREIGN PATENT DOCUMENTS

<u>Exam.</u> <u>Initial</u>	<u>Document</u> <u>Number</u>	<u>Publication</u> <u>Date</u>	<u>Country</u>	<u>Class</u>	<u>Translation</u> <u>Yes</u> <u>No</u>
_____	GB 2 278 631	12/7/94	UK	E06B 49/00	

Examiner:

Date Considered:

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP §609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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(54) Title of Invention

An identification system

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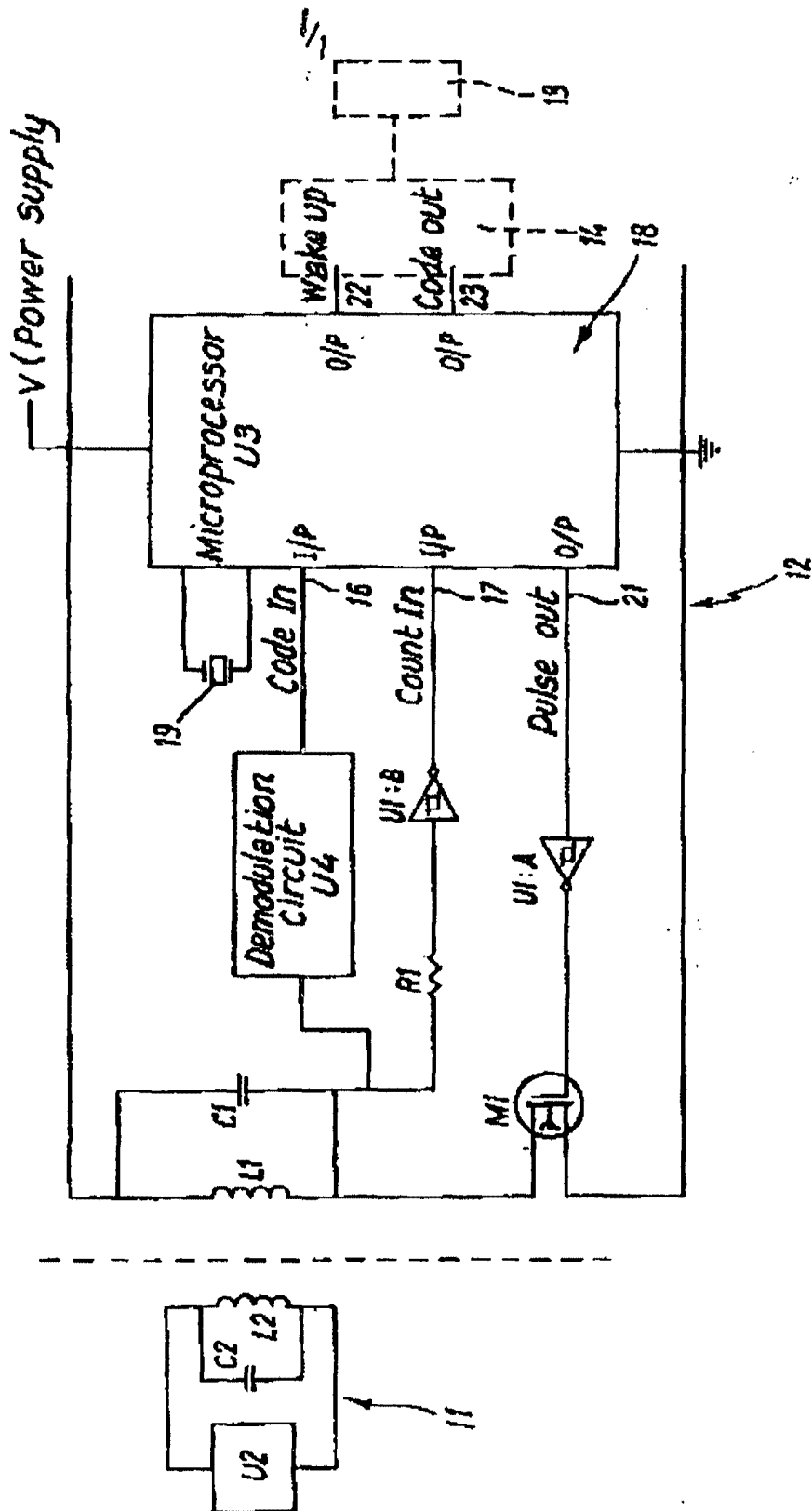
(52) Domestic classification
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(56) Documents cited
EP0227589 A2
US4864292 A
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(58) Field of search

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G4T TCA
INT CL: E05B 49/00
Online databases: WPI
updated as appropriate

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2278631

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AN IDENTIFICATION SYSTEM

Technical Field

This invention relates to a non-contact identification system for use in particular, although not exclusively, for personnel access control.

Background Art

It is common for doors or other closures to be secured by an electrically operated lock which can be opened by presenting a token in the form of a card or key to a reader associated with the lock. The reader verifies that the key carries a code which is acceptable to allow opening of the door and, if it is acceptable, the reader actuates opening of the door by release of the lock. Commonly the reader and token are of the kind which require no contact between them and therefore such a system is commonly known as a proximity reading system.

The problem arises with such systems at the present time in that in order to allow for reading of a token at any time for access control purposes it is necessary to ensure that the reader is continuously powered. This means that a significant amount of power is wasted during non-operative periods. Furthermore it is necessary for current systems of this type to be hardwired into a mains circuit to ensure that adequate power is supplied for reliable operation over sustained time periods.

Disclosure of the invention

It is an object of the present invention to provide an identification system of the abovementioned type which can be operated by a low voltage

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on-board power supply in such a manner as to substantially reduce the amount of power used in operation.

Thus, and in accordance with one aspect of the present invention therefore there is provided an identification system comprising an identification device and a reader, said reader including a power supply, said reader being normally in a first state in which it generates low power pulses from said supply, said reader being switchable into a second state upon sensing a modification to said pulses caused by the i.d. device being in proximity thereto, in said second state said reader being capable of generating sufficient power to read the i.d. device.

With this arrangement it is possible to provide an identification system which can read an i.d. device presented to it and yet utilise a much reduced amount of power in operation. A low voltage power supply can be used.

Preferably said i.d. device includes a first coupling device and said reader includes a second coupling device, said first and second coupling devices being inductively linked when said i.d. device is in proximity to said reader whereby power from the power supply can be transferred to said identification device via said inductively linked coupling devices. Preferably said first and second coupling devices comprise inductive coil elements which can be energised by way of an alternating or fluctuating current. The first and/or second coupling devices may form part of a tuned resonant circuit and in a preferred embodiment both said coupling devices form part of separate such circuits, one on the i.d. device end and one on the reader.

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With regard to the identification device this may be a token and may comprise a thin plastics member having electrical circuitry embedded therein so as to insulate or shield the circuitry from the environment. Said circuitry may include rectification circuitry to rectify an incoming alternating current, a code memory and clock circuitry to control the generation of codes from the memory.

With regard to the reader, this may be mounted in or adjacent to the controlled device and may be adapted to control operation of the device directly or indirectly via actuating means. The reader may include a micro-processor to control generation of said low power pulses and to read and interpret incoming codes from said key and to operate said controlled device in accordance therewith.

With regard to the modification of the low power pulses that are detected by the reader, this may comprise a change in the decaying oscillations of a tuned circuit in response to successive pulses and the reader may detect such change by detecting the difference in number of oscillations beyond a predetermined threshold. Said reader may detect the difference in number of oscillations by comparison of stored oscillation counts between successive single or multiple pulses. Alternatively the pulses may be integrated over time to provide a voltage level for comparison with successive levels.

Preferably, and in accordance with a second aspect of the present invention there is provided a reading system comprising a reader and a

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device to be read, said reader comprising a tuned circuit, an actuating device arranged periodically to apply an actuating pulse to the tuned circuit to produce a low power signal derived from a decaying oscillation in a first operational state of the reader, and a detection circuit connected to the tuned circuit to detect modification of the decaying oscillation caused by the said device when in proximity with the reader and to switch the reader to a second operational state in which a higher power signal is produced. The higher power signal may be derived from continuous operation of the tuned circuit or otherwise.

The second aspect of the invention may be used in conjunction with the first aspect of the present invention.

Typically the pulses may be at the rate of 10 per second at a duration of $2\mu\text{s}$. Operating at 3V, this can draw only $5\mu\text{A}$ current from the power source (roughly 16000 times less than that required for continuous duty). The rate of the pulses is chosen only to fulfil the required system response time for the particular application. Preferably the tuned circuit is actuated or 'ringed' so as to oscillate for a natural decaying period (i.e. so that oscillations terminate) before the next pulse is applied.

The detection circuit preferably operates by counting the number of decaying oscillations.

In so far as the system is looking only for a change to the number of decaying oscillations, then it is not important what the actual number is, as long as it is stable over time. This attribute can be utilised to reduce the

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emphasis on production component tolerances and also to allow the system to automatically adjust for the effect of metallic materials which may be present or subsequently introduced in proximity with the reader. In the latter respect, the detection circuit can act to determine the number of oscillations or other parameter over a period of time during a period of stability to arrive at a 'normal' count or reference parameter for the particular environment.

Brief description of the drawings

The invention will now be described further by way of example only and with reference to the accompanying drawing, the single figure of which shows one embodiment of identification system according to the present invention.

Best mode of carrying out the invention

Referring now to the figure, there is shown a key or token 11 and reader 12 adapted to control operation of a lock mechanism for a security door shown schematically at 13 via an actuating mechanism 14.

The key 11 comprises a thin rectangular plastics plate which can be conveniently carried in a persons pocket. The plate incorporates electronic circuitry embedded in the plate so as to be electrically insulated and physically sealed from the environment by the plastics material of the plate. The circuitry includes a key inductive coil L2 connected in parallel to a capacitive element C2 to form a resonant circuit and an integrated circuit device U2 which includes rectifying circuitry, a non-volatile code store memory and clock circuitry to control the generation of the codes from the

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memory in operation (not shown).

The reader 12 comprises a reader coil L1 connected in parallel to a capacitor C1. The output from the coil L1 is connected to a demodulation circuit U4 and to a threshold detection element U1:B via a current limit resistor R1. The output of the demodulation circuit U4 and the threshold detection element U1:B are connected to inputs 16 and 17 of a microprocessor 18 respectively. The microprocessor is connected to a low voltage d.c. power supply integral with the reader and is clocked by crystal 19. A first output 21 of the microprocessor 18 connects the microprocessor to the reader coil L1 via an inverting buffer U1:A and MOS field effect transistor M1. Second and third outputs of the microprocessor 22, 23 provide the output via the actuating means to operate the lock mechanism 13 in a manner to be hereinafter described.

In use, the reader is normally in a dormant state in which the microprocessor 18 feeds pulses to the reader coil L1 at a frequency of one $2\mu\text{s}$ pulse per 100ms via the inverting buffer U1:A and the MOS transistor M1. The voltage pulses applied to the gate of the MOSFET M1 cause current pulses to be applied to the reader coil L1 at the same rate. Thus the reader coil L1 radiates pulses of energy for the period that the reader is in its dormant mode. Thus it will be appreciated that in its dormant mode the reader is consuming a minimum of power due to the fact that short frequent low power pulses are being applied to the reader coil L2 as opposed to the continuous current or continuous stream of pulses of conventional systems

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of this type. Thus in the dormant mode the reader coil L1 is providing an intermittent magnetic field.

When a key or token 11 is brought into close proximity with the reader 12, the coil L2 links the intermittent magnetic field generated by the reader 12 and this inductive coupling of the two coils L1 and L2 causes a modification of the pulses applied to the reader coil L1 in the form of a damping thereof. The modified pulses are applied via a current limit resistor R1 to a threshold detection element U1:B which detects that part of the pulse above a threshold limit caused by the aforementioned damping and provides an output to input 17 of the microprocessor 18, if the pulses are of sufficient amplitude. The output signal applied to the microprocessor in these circumstances by the threshold detection element U1:B is counted by the microprocessor and if the count has changed, causes the microprocessor to switch out of its dormant mode and into an active mode in which mode the output field of reader coil L1 is made continuous rather than intermittent.

The inductive coupling of the two coils L1 and L2 when the key or token 11 is in close proximity to the reader 12 also provides the necessary power to drive the circuitry of the integrated circuit device U2 which provides a signal indicative of the code identifying the key or token 11, or person carrying the key or token 11, to the coil L1 via coil L2 as a modulation of the pulses. These modulated pulses are fed back to the microprocessor 18 via a demodulated circuit to input 16 of the micro-

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processor in order that the microprocessor can read the code stored on the key or token 11. The code stored on the key or token 11 can then be compared with a store of acceptable codes in the microprocessor, or indirectly via a separate store of acceptable codes, and if verified as an acceptable code, the microprocessor 18 will generate a signal to cause actuation of the lock mechanism 13 and opening of the door via the actuating circuitry 14.

Furthermore, it will be appreciated that whilst the present invention has been described in terms of the operation of a lock mechanism 13, the key or token 11 and reader system of the invention can be utilised to control operation of any device which requires to be controlled or operated on presentation of a suitable authority.

The present invention has a number of advantages over conventional systems of this type, in so far as, since the reader only uses short pulses, the power consumption is significantly reduced and furthermore, since the reader includes its own on-board d.c. power supply or battery which is capable of controlling operation of the lock mechanism 13, there is no need for the device to be hardwired into a mains circuit, rendering it simple and convenient to fit the system to all types of existing locks and other controlled mechanisms. The token need have no on-board battery since it derives all necessary power from the inductive linkage as described.

It is of course to be understood that the invention is not intended to be restricted to the details of the above embodiment which are described by

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way of example only.

In order further to minimise power consumption, the clock of the reader preferably operates at two rates - a slow (low power) rate during the deactuated mode and a higher (higher power) rate on "wake up". For example, the slow speed may be 32 KHz, and the high speed may be 2.5 MHz.

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CLAIMS

1. An identification system comprising an identification device (11) and a reader (12); said reader (12) including a power supply, said reader (12) being normally in a first state in which it generates low power pulses from said supply, said reader (12) being switchable into a second state upon sensing a modification to said pulses caused by the i.d. device (11) being in proximity thereto, in said second state said reader being capable of generating sufficient power to read the i.d. device.

2. A system according to claim 1 characterised in that preferably said i.d. device (11) includes a first coupling device (L2) and said reader (12) includes a second coupling device (L1), said first and second coupling devices (L1, L2) being inductively linked when said i.d. device (11) is in proximity to said reader (12) whereby power from the power supply can be transferred to said identification device via said inductively linked coupling devices (L1, L2).

3. A system according to claim 2 characterised in that preferably said first and second coupling devices (L1, L2) comprise inductive coil elements which can be energised by way of an alternating or fluctuating current.

4. A system according to claim 3 characterised in that at least one of the first and second coupling devices (L1, L2) form part of a tuned resonant circuit.

5. A system according to claim 4 characterised in that both said coupling devices (L1, L2) form part of separate such circuits.

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6. A system according to any one of claims 1 to 5 characterised in that the identification device (11) is a token which comprises a thin plastics member having electrical circuitry embedded therein so as to insulate or shield the circuitry from the environment.

7. A system according to any one of claims 1 to 6 characterised in that the identification device (11) comprises electrical circuitry including rectification circuitry to rectify an incoming alternating current, a code memory and clock circuitry to control the generation of codes from the memory.

8. A system according to any one of claims 1 to 7 characterised in that the modification of the low power pulses which are detected by the reader comprise a change in the decaying oscillations of a tuned circuit in response to successive pulses.

9. A system according to claim 8 characterised in that the reader (12) detects said change by detecting the difference in number of oscillations beyond a predetermined threshold.

10. A system according to claim 9 characterised in that the reader detects the difference in number of oscillations by comparison of stored oscillation counts between successive single or multiple pulses.

11. A system according to claim 9 characterised in that the pulses are integrated over time to provide a voltage level for comparison with successive levels.

12. A reading system comprising a reader (12) and a device (11) to be
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WaveLynx Technologies v. ASSA Abloy, IPR2023-00730

read, said reader (12) comprising a tuned circuit (L1,C1), an actuating device (U1:A,M1) arranged periodically to apply an actuating pulse to the circuit (L1,C1) to produce a low power signal derived from a decaying oscillation in a first operational state of the reader, and a detection circuit (U1:B) connected to the tuned circuit (L1,C1) to detect modification of the decaying oscillation caused by the said device when in proximity with the reader and to switch the reader to a second operational state in which a higher power signal is produced capable of powering the reader (12) and the identification device.

13. A reading system according to claim 12 characterised in that the higher power signal is derived from continuous operation of the tuned circuit (L1,C1).

14. A reading system according to claim 12 to 13 characterised in that the tuned circuit (L1,CL) is ringed so as to oscillate for a natural decaying period before the next pulse is applied.

15. A reading system according to any one of claims 12 to 13 characterised in that the detection circuit (U1:B) counts the number of decaying oscillations.

16. A reading system according to any one claims 12 to 15 characterised in that the detection circuit (U1:B) derives a reference parameter for the decaying oscillation and responds to changes therein, said reference parameter being derived from multiple oscillations occurring over a period of time during a period of stability.

17. An identification system according to any one of claims 1 to 11 in which the reader (12) comprises a reading system in accordance with any one of claims 12 to 16.

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system of any one of claims 1 to 15.

18. A system according to any one of claims 1 to 11 or 17 when used to control operation of a door lock.

19. A system substantially as hereinbefore described with reference to the accompanying drawings.

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 2003

Application or Docket Number

10848246

CLAIMS AS FILED - PART I

(Column 1)

(Column 2)

TOTAL CLAIMS	46	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	46 minus 20 =	* 26
INDEPENDENT CLAIMS	3 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT ☐		

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	*	Minus	**	=
	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

(Column 1)

(Column 2)

(Column 3)

AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	*	Minus	**	=
	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

(Column 1)

(Column 2)

(Column 3)

AMENDMENT C		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	*	Minus	**	=
	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SMALL ENTITY TYPE ☐

OR OTHER THAN SMALL ENTITY

RATE	FEE
BASIC FEE	385.00
XS 9=	
X43=	
+145=	
TOTAL	

RATE	FEE
BASIC FEE	770.00
XS18=	468
X86=	
+290=	
TOTAL	1238

SMALL ENTITY

OR OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE
XS 9=	
X43=	
+145=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
XS18=	
X86=	
+290=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
XS 9=	
X43=	
+145=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
XS18=	
X86=	
+290=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
XS 9=	
X43=	
+145=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
XS18=	
X86=	
+290=	
TOTAL ADDIT. FEE	

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

05/20/2004 HLE333 00000058 024245 10848246

01 FC:1001 770.00 DA
02 FC:1202 468.00 DA

PTO-1556
(5/87)

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