



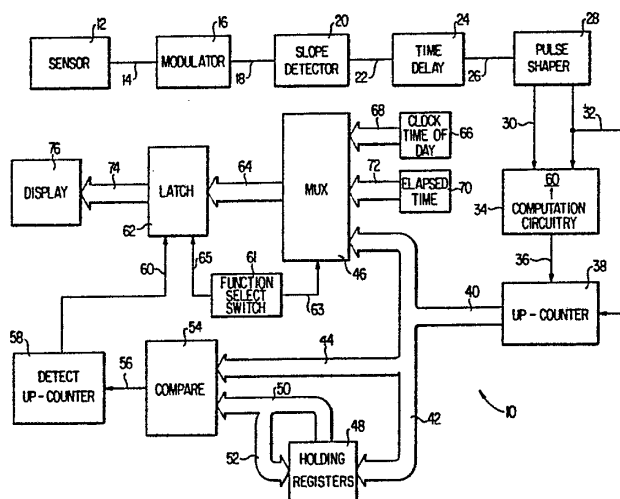
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(54) Title: CARDIOTACHOMETER USING AUTOCORRELATION TECHNIQUES

(57) Abstract

A cardi tachometer for indicating heart rate of a user in beats per minute. The cardi tachometer comprises a sensor (12), placed on the body of the user, for producing an electrical signal indicative of the heart rate of the user. Circuitry (28) is provided for converting the electrical signal into first and second digital signals. 60/t computation circuitry (34) responds to the first and second digital signals and produces a third digital signal having a varying frequency representative of the number of heart beats per minute. An up-counter (38) converts the third digital signal into a plurality of binary number signals, each bit of which is stored in a series of shift registers (48). A compare (54) using a plurality of exclusive OR gates, compares each of the stored binary number signals with the most recent binary number signal, from the up-counter, to determine if a plurality of compared signals are within a predetermined percentage of each other. Finally, a display (76) is provided for displaying the most recent binary number signal, when the plurality of compared signals are within the predetermined percentage of each other. Further provision is made for display of both elapsed time and time of day.



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DescriptionCardiotachometer Using Autocorrelation TechniquesTechnical Field

The present invention relates to pulse
5 monitors with visual readout, in general, and to a
cardiotachometer which performs a comparison between
selected heartbeat intervals such that when any
plurality of the intervals are within a predetermined
percentage of each other, the plurality of intervals
10 are averaged, read out and held in the display until
the next update.

Background Art

Heart rate is the basic parameter used to
evaluate and determine the condition of the human
15 body. In carrying out its action, the heart produces
three wave complexes, designated as P, QRS, and T,
each of which corresponds to a particular electrical
event within the heart. It has long been known that
the R wave produces the greatest electrical activity,
20 and for this reason the R-R interval has been used
as a way of measuring the time between heartbeats.
By knowing the time between heartbeats, it is easy
to determine the number of beats per minute.

The contraction, or period of contraction,
25 of the heart, is referred to as a systole. It
coincides with the interval between first and second
heart sounds, during which blood is forced into the
aorta and the pulmonary trunk. In the same way the
R-R interval may be used as a way of measuring the
30 time between heartbeats, the interval between systoles
may be used for the same purpose.



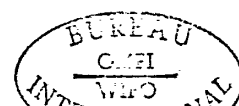
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During a systole, the heart contracts and forces blood through the arteries, which respond by expanding. Thus, a systole may be detected by placing an appropriate transducer or sensor against
5 any of the well known pressure points on the human body or in an area where blood flow is occurring.

The transducer may be in the form of a pressure transducer, such as a piezoelectric crystal or a photo-transducer in the form of a light emitting
10 diode and a photocell.

There are any number of prior art pulse monitors which detect the R-R interval or the systolic rate, compute the heart rate in beats per minute and, then, display every update as an instantaneous
15 beat-by-beat readout. An undesirable feature of this procedure is that movements of the transducer by the user are not distinguished from actual heart pulses by the transducer and thus a false reading occurs. Another cause of false readings is the
20 detection by the transducer of normal respiratory fluctuation or psychomotor responses. These readings manifest themselves in a constantly changing display.

To avoid such false readings, electronic
25 pulse rate measuring devices have been designed to average the time interval over 4, 8, 10, or 16 beats to get an average heart beat. Each of these averaging techniques has its own drawback. In the case of the 4 beat average, there is still some jumping of the
30 readout. The problem with the 8, 10 or 16 beat average is the long time interval between updates. Probably the most important drawback found in all averaging systems is that any error occurring during the period under consideration is also averaged into
35 the final readout.



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There is thus a need for a cardi tachometer or a pulse monitor which produces a continuous update and display, and which is not plagued by the problems of inconsistent readout, and the introduction of error from any source, such as, muscle tremor, poor sensor contact, and inappropriate use, to name a few. The present invention is directed toward filling that need.

Disclosure of Invention

10 In accordance with the subject invention, there is provided a miniature, totally self-contained cardi tachometer to be worn or held by a user for numerically displaying a continuous readout of the user's heart beat rate. The device, which may be
15 housed in a wrist watch or a compact hand-held unit, basically comprises a sensor in the form of a light emitting diode and a photocell which is placed on the finger of the user. The photocell responds to the variations in light intensity reflected off the
20 capillary bed within the finger to produce an analog voltage signal representative of the systolic beats. This signal is received by a slope detector where it is amplified and converted into a digital signal.

The digital signal is delayed for a predetermined time and then fed into a pulse shaper to
25 produce a pair of clean pulse trains. One pulse train is used to reset an up-counter and a 60/t computation block, while the other pulse train is used to latch data within the 60/t computation
30 block.

The 60/t computation circuitry produces an output signal which has a frequency representative of the heart rate in beats per minute. This signal is used to cause an up-counter to produce a binary



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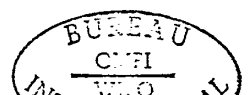
number equal to the number of beats per minute.
This number is fed to a latch and held.

The binary number from the up-counter,
with the two least significant bits excluded, is
5 simultaneously fed to a comparator and a series of
holding registers.

In the preferred embodiment the holding
registers typically comprise a plurality of 10-bit
shift registers, one being associated with each
10 binary bit from the up-counter. The binary numbers
from the up-counter are placed into the holding
registers on a first-in first-out (FIFO) basis.
Thus, the eleventh number placed into the holding
registers will replace the first number previously
15 stored therein. If the bits of the current number
from the up-counter are the same as the bits of one
of the numbers in the holding registers, a compare
signal is issued and fed to a detect up-counter.
This comparison continues with the remaining numbers
20 stored in the holding registers. When at least one
more valid comparison is made, the detect up-counter
is advanced to produce a latch signal. The latch
responds to this signal by causing the data stored
therein to be transferred to a display where the
25 data is converted into an array of integers in eye
readable format.

Provision is also made for an elapsed time
indicator and a conventional time-of-day clock, each
of which have their readout on the same display as
30 the cardiometer.

It is thus an object of the present invention
to provide a cardiometer for producing a numerical
indication of pulse rate with an extremely high
degree of accuracy.



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It is another object of the present invention to provide a totally unified, self-contained, sensor-electronic-display pulse monitor.

It is still an object of the present invention to provide a simple, inexpensive pulse monitor not plagued by readout error.

It is yet an object of the present invention to provide a pulse monitor not plagued by movements of the sensor at the detection site by the user.

It is a further object of the present invention to provide a pulse monitor in which beat-by-beat read unsteadiness, due to normal respiratory fluctuation or psychomotor responses, is ameliorated.

Additional objects of the present invention will become apparent from a reading of the appended specification and claims in which preferred but not necessarily the only forms of the invention will be described in detail, taken in connection with the drawings accompanying and forming a part of the application.

Brief Description of Drawings

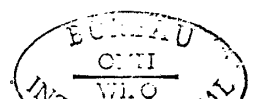
Figure 1 is a functional block diagram for a preferred embodiment of the subject invention;

Figure 2 is block circuit diagram showing examples of the sensor, the modulator and the slope detector;

Figure 3 is a block circuit diagram showing examples of the time delay and the pulse shaper;

Figure 4 is a block circuit diagram showing examples of the 60/t computation circuit and the up-counter;

Figure 5 is a block circuit diagram showing the holding registers and the compare;



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Figure 6 is a perspective view of the hand-held embodiment of the subject cardiometer.

Figure 7 is a perspective view of the subject cardiometer in the form of a wrist watch.

Figure 8 is a schematic rear view of the cardiometer of Figure 7.

Best Mode for Carrying Out the Invention

With reference to Figure 1, the cardiometer of the subject invention is generally noted as 10. In a preferred embodiment of the subject invention, the cardiometer 10 is a totally self-contained unit in the form of a wrist watch or a hand-held device.

A sensor 12, which may be a conventional pressure transducer or a light emitting diode/photocell combination, measures the systolic beats of the user. In the case of the wrist watch embodiment, the beats are sensed at the wrist of the user in a conventional manner. In the case of the hand held device, the beats are sensed through a finger of the user in a conventional manner. The electrical signal produced by the sensor is fed into a modulator 16 via leads 14. The modulator 16 converts the incoming signal into a digital signal for interpretation by the slope detector 20. The output of the slope detector 20 appears on line 22 and is fed to a time delay 24. The output of the time delay appearing on leads 26 is fed to a pulse shaper 28 which produces two pulse trains on lines 30 and 32.

The signals appearing on lines 30 and 32 are fed into 60/t computation circuitry 34. The signals on lines 30 and 32 cause the 60/t circuit 34 to produce at its output 36, a digital signal having



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a frequency equal to the number of heart beats per minute.

5 An up-counter 38 responds to the signal on line 36 by producing an output signal 40 which is a digital representation in binary form of the number of beats per minute. The signal appearing on line 32 is used to reset the up-counter 38 between detected beats.

10 The output of the up-counter is typically a 12-bit number, D11-D0, which is fed to a multiplexer 46. The multiplexer 46 also receives the output of a time of day clock 66 on lines 68, and an elapsed time indicator 70 on lines 72.

15 At the same time, 6 bits, D7-D2, from the output of the up-counter are fed to holding registers 48 on lines 42 and to a compare 54 via lines 44. The holding registers 48 typically comprise a series of 10-bit shift registers, although shift registers having a capacity for a greater or lesser number of bits can be used. The holding registers are clocked at a rate such that the entire contents of the registers are presented to the compare 54 before the output of the up-counter is changed. The output of the holding registers 48 is also reinserted into the registers on a first-in first-out basis, along with the output of the up-counter so that the oldest piece of data is replaced by the output of the up-counter.

25 The compare 54 contrasts the data from the up-counter 40, appearing on lines 44, with the data samples contained in the holding registers 48, appearing on lines 50. When the bits on line 44 are the same as the bits on line 50, the compare 54 issues a compare signal on line 56.



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The detect up-counter which is typically a conventional up-counter, is caused to advance or count one unit by the compare signal 56. When the detect up-counter has advanced at least two, but typically three, units, a latch pulse is issued on line 60.

A function select switch 61, which is typically a multiposition switch or a series of push button switches located external to the device, provides a means for selecting between three functions for display, namely, time of day, elapsed time, or heart rate. When heart rate is selected the multiplexer 46 feeds the output of the up-counter 38 to the latch 62. The signal appearing on line 60 from the detect up-counter 58 causes the latch 62 to issue appropriate signals on lines 74 to cause a conventional display 76 to display in eye readable form the heart rate of the user in beats per minute.

When the user wishes to display the time of day or the elapsed time, the function select switch 61 also activates the latch 62 to produce the appropriate display in eye readable format on display 76.

A detailed description of the sensor 12, the modulator 16, and the slope detector 20 will now be presented with reference to Figure 2. The sensor 12 comprises a light emitting diode (LED) 100 in series with a resistor 102 between a source of potential Vcc and ground. There is also provided a photocell in the form of a phototransistor 104 in series with a resistor 106 between a source of potential Vcc and ground. The photocell senses the light from the LED bouncing off the capillary bed within the skin of the wearer as a beam of varying intensity caused by the systolic beats. The photocell

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responds by producing a varying voltage which is fed into the positive term of a comparator 110.

The output of the comparator 110 is fed to the D input of flip-flop 122 via inverters 112 through 114. The flip-flop 122 produces a pulse train at its Q output which is fed back through resistor 118 to the negative input of the comparator 110. A capacitor 120 is connected between the negative input and ground. As the capacitor charges, it will trail the upgoing pulse from the phototransistor. When it catches the pulse, the output of the comparator 110 will be low, otherwise the output will be high. Therefore, the Q output of the flip-flop 122 will produce a series of logic ones when the slope of the output of the phototransistor is positive and will produce a series of logic zeros at all other times.

The Q output of the flip-flop 122 is fed into a 16 bit shift register 126, although shift registers having a greater bit capacity can be used. The outputs of the shift registers are fed into a NAND gate 128 and then inverted by an inverter 134 to produce a signal on line 22. Should any of the outputs of the shift register become a logic zero then the output of the inverter 134 will be a logic zero, thus indicating that a pulse has not been detected. When the shift register is filled with logic ones, the output of the inverter 134 will also be a logic one, thus indicating that a pulse has been detected. The capacity of the shift register 126 as well as the clocking rate for the flip-flop 122 and the shift register 126 is chosen so that base line noise, including 60 and 120 Hz noise, at the sensor is not detected as a pulse. In other words, for a pulse to be detected it must have a



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fairly high slope, such as that caused by a systolic beat.

With reference to Figure 3, the time delay 24 and the pulse shaper 28 will be described in detail. The output of the slope detector 20 appearing on line 22 is fed into a NAND gate 140. The other input to the NAND gate is received from the $\bar{Q}$ output of a flip-flop 142. The output of the NAND gate 140 provides a clock signal to the flip-flop 142 on line 148. The Q output of flip-flop 142 is fed to the D input of an up-counter 144 which has its reset grounded. The up-counter issues a signal every 16th pulse to reset the flip-flop 142. In this way, a time-delayed signal is issued on line 26 and fed into the pulse shaper 28. This time delay serves the purpose of providing a "dead time" interval where no spurious pulses, whether electronic or mechanical in origin, can be counted.

The pulse shaper 28 which is used to provide a pair of synchronized pulses on lines 30 and 32, comprises three flip-flops 150-152. Flip-flop 150 has its D input held high and is clocked by the signal on line 26. The Q output of flip-flop 150 is fed to the D input of flip-flop 151. The Q output of flip-flop 151 is fed to the D input of flip-flop 152 and also provides a signal on line 30. The Q output of the flip-flop 152 provides a signal on line 32 as well as a reset signal for flip-flop 150. Thus, the signals appearing on lines 30 and 32 are synchronized to further provide that no spurious pulses, electronic or mechanical, are allowed into the computation.

With reference to Figure 4, a detailed description of the 60/t circuit 34 and the up-counter 38 will be provided. A conventional 12-bit up-counter

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160 is enabled and reset by the signal on line 32. The output of the up-counter is a 12-bit number chosen to represent the time interval between reset times. This number is fed via lines 162 into a
5 latch 164 which is clocked at a rate determined by the signal on line 30. The latch has its reset high so as to dump its contents into the divide-by-N ($\div N$) 168.

The divide-by-N is reset by the signal
10 appearing on line 32 and is appropriately clocked by a signal on line 167 to produce at its output, a digital signal having a frequency equal to the number of heart beats per minute. Thus, it can be seen that the $60/t$ circuitry takes the time interval
15 between systolic beats, and converts this time interval into a digital signal indicative of the number of heart beats per minute. This signal, which appears on line 36, is used to clock an up-counter 38 which is reset between detected beat
20 intervals by the signal on line 32. The output of the up-counter is a 12-bit binary number, D11 through D0, which appears on lines 40. The output of the up-counter is fed via lines 40 to the multiplexer 46. At the same time bits D7 through D2 from the
25 up-counter are fed into the holding registers 48 and the compare 54.

With reference to Figure 5, the details of the holding registers 48 and the compare 54 will now be described. Bits D7-D2 from the output of the
30 up-counter 38 are simultaneously fed into the inputs A_0 through F_0 of a multiplexer 180 and a series of exclusive OR gates 190 through 195 via lines 44-1 through 44-6. The outputs, A through F, of the multiplexer 180 are fed into a series of 10-bit
35 shift registers 170 through 175. The outputs of the



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shift registers are fed to inputs of the exclusive OR gates 190 through 195 via lines 51-56, and to the inputs A_1 through F_1 of the multiplexer 180 via lines 52-1 through 52-6.

5 The shift registers 170 through 175 shift the incoming data received from the multiplexer 180 on a first-in first-out (FIFO) basis. The data is shifted through the shift registers at such a rate so that each of the data samples is presented for
10 comparison by the compare 54 with the selected bits D7 through D2 from the up-counter 38.

 The outputs of the exclusive OR gates 190 through 192 are fed to a NOR gate 196 the output of which is fed to the input of a NAND gate 204. The
15 outputs of exclusive OR gates 193 through 195 are fed to the inputs of NAND gate 204 via inverters 198 through 200, respectively.

 The exclusive OR gates 190 through 195 each issue a logic 1 when the inputs to those gates
20 are different and issue a logic 0 when the inputs are the same. When the outputs of all of the exclusive OR gates 190 through 195 are low, the output of the NAND gate 204 is high, indicating that a valid comparison has been made. If any of the outputs
25 from the exclusive OR gates is high then the output of the NAND gate 204 will be low, indicating that a valid comparison has not been made.

 By way of example, assume that the output from the up-counter 38 is a binary number indicating
30 that the heart rate is 72 beats per minute. The output, D11-D0, of the up-counter 38 in binary notation is 0000, 0100, 1000. As stated before, only bits D7-D2 are fed into the exclusive OR gates. In this case, binary bits 010010 will be fed, respec-
35 tively, to the inputs 41-1 through 44-6 of the

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exclusive OR gates. Since the two least significant bits of the output from the up-counter 38 have been excluded from the comparison, the output of the up-counter 38 will compare favorably to samples
5 stored in the shift registers which are in the range between 72 and 75 beats per minute. This is due to the fact that the bits D7 through D2 for each of those numbers are the same as bits D7 through D2 for the number 72. A specific comparison range, obtained
10 by excluding the two least significant bits, has been described. It is to be understood that the comparison range as well as the percentage difference between the numbers within the range may be increased by excluding a greater number of least significant
15 bits. Further, the comparison range and the percentage difference may be narrowed by not excluding any least significant bits so that the percentage difference between samples is reduced to zero.

Returning now to Figure 1, the compare
20 signal on line 56 indicates that a valid comparison has been made. This signal provides a pulse to advance the up-counter 58. When the up-counter advances at least two, but typically three, units, it issues a latch signal on line 60 to latch the
25 data previously stored in the latch 62, to appear on display 76. The multiplexer 46 is of conventional design, and may include a series of multiplexers designated as model number 4053 and manufactured by National Semiconductor, Inc., Santa Clara, California.
30 Likewise the latch is of conventional design and may include a number of BCD-to-seven segment conversion devices. One such device is model number 4543, again, manufactured by National Semiconductor, Inc. The display 76 is typically of the type which converts
35 the output of the latch 62 to an eye-readable array

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of integers. One such device is model number 741 manufactured by Beckman Instruments, Inc., Fullerton, California. Although there are numerous variations in the timing scheme used to clock the various components of the subject invention, excellent results have been obtained using the following clock rates:

512 Hz for the flip-flop 122 in the modulator and shift register 126 in the slope detector.
16 Hz to the up-counter 144 in the time delay.

32,768 Hz to the flip-flop 151 in the pulse shaper.

128 Hz to the up-counter 160 and 7680 Hz to the divide-by-N 168 in the 60/T circuit 34.

16,384 Hz to the shift registers 170-175 in the holding registers 48.

With reference to Figure 6, a hand-held version of the unified, self-contained cardiotochometer with digital readout is generally designated as 200. The device comprises a unitized housing 202 shaped for convenient placement within the palm of the user. The light emitting diode 100 and the phototransistor 104 are positioned on the housing so as to receive the thumb of the user. In this way systoles are detected. The cardiotochometer circuitry, described hereinbefore, is mounted within the housing 200. The output of the phototransistor 104 is fed to the cardiotochometer circuitry, wherein it is processed and read out on the display 76 which is positioned on the housing for easy reading by the user.

The cardiotochometer of the subject invention being mounted in a wrist watch is shown in Figures 7 and 8. In this embodiment the cardiotochometer

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circuitry is mounted in a watch housing 210 which is secured to the wrist of the user by straps 212. The sensor, which is a piezoelectric transducer 214, is secured to the back of the housing 210 and detects
5 systoles through the wrist of the user. A push button switch 216 is provided to select the function (heart rate, time of day, or elapsed time) to be displayed on the display 76.

Obviously many modifications and variations
10 of the present invention are possible in light of the above teachings, and it is contemplated that the subject invention may be implemented through the use of discrete components or an integrated circuit chip. It is further contemplated that an integrated
15 circuit chip having complimentary-metal-oxide-silicon (CMOS) circuits may be used to configure the present invention, and that a remote sensor may be contained in a housing separate from that containing the remainder of the device. It is, therefore, to be
20 understood that within the scope of the appended claims, the invention may be practiced otherwise and as specifically described.



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Claims

1. A cardiometer for indicating heart rate of a user in beats per minute, said cardiometer comprising:

- 5 means, responsive to the heart beats of said user for producing a heart rate signal having portions representative of the beats per minute of said user's heart;
- means for storing the portions of said heart rate signal;
- 10 means for comparing each of said stored portions with the most recent portion of said heart rate signal;
- means for issuing a display signal when at least two of the comparisons in said comparing means is made between portions within a predetermined comparison range; and
- 15 means, responsive to said display signal, for displaying said most recent portion of said heart rate signal in eye-readable format wherein heart rate in beats per minute is indicated.
- 20

2. The cardiometer of claim 1, wherein said at least two is three.

3. The cardiometer of claim 1 further including time delay means for removing spurious pulses.

25

4. A cardiometer for indicating heart rate of a user in beats per minute, said cardiometer comprising:

- 30 interval means, responsive to the heart beats of said user, for producing an interval signal having portions indicative of the time interval between said beats;



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means for converting each portion of said interval signal into a heart rate signal having portions representative of the beats per minute of said user's heart;

5 means for storing the portions of said heart rate signal;

means for comparing each of said stored portions with the most recent portion of said heart rate signal;

10 means for issuing a display signal when at least two of the comparisons in said comparing means are made between portions within a pre-determined percentage of each other; and

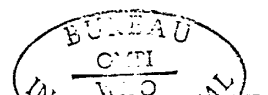
15 means, responsive to said display signal, for displaying said most recent one of said plurality of signals in eye-readable format wherein heart rate in beats per minute is indicated.

5. The cardiometer of claim 4, further comprising sensor means, adapted to contact the skin of said user, for producing an electrical signal indicative of the heart beats of said user, and interconnect means for conveying said electrical signal for use by said interval means.

25 6. The cardiometer of claim 4 further including time delay means for removing spurious pulses.

30 7. The cardiometer of claim 4, further comprising means for producing a signal indicative of time-of-day for display by said displaying means.

35 8. The cardiometer of claim 4, further comprising means for producing a signal indicative of elapsed time for display by said displaying means.



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9. A cardi tachometer for indicating heart rate in beats per minute of a user, said cardi tachometer comprising:

5 sensor means, adapted to contact the skin of said user, for producing an electrical signal indicative of the heart rate of said user;

means for converting said electrical signal into first and second digital signals;

10 means responsive to said first and second digital signals for producing a third digital signal having a varying frequency representative of the number of heart beats per minute;

15 converting means for converting said third digital signal into a plurality binary number signals;

storing means for storing each of said binary number signals;

20 means for comparing each of said stored binary number signals with the most recent binary number signal from said converting means to determine if a plurality of compared signals are within a predetermined comparison range of each other; and

25 means for displaying said most recent binary number signal when said plurality of compared signals are within said predetermined percentage of each other.

30 10. The cardi tachometer of claim 9, wherein said comparison range is determined by the number of least significant bits excluded from each of said stored and most recent binary number signals.

35 11. The cardi tachometer of claim 9, wherein said sensor means comprises a pressure transducer.



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12. The cardiometer of claim 9,
wherein said sensor means comprises a light source,
and a photocell responsive to variations in light
intensity reflected off of the capillary bed within
5 the skin of said user, for producing a voltage
signal representative of the heart rate of said
user.

13. The cardiometer of claim 9,
wherein said sensor means detects systolic beats in
10 order to produce said electrical signal.

14. The cardiometer of claim 9,
wherein said third digital signal producing means
comprises counting means for producing an interval
signal representing the time interval between heart
15 beats, and dividing means responsive to said interval
signal for producing said third digital signal.

15. The cardiometer of claim 14,
wherein said producing means includes a latch for
holding said interval signal before it is fed to
20 said dividing means.

16. The cardiometer of claim 15,
wherein said dividing means is a divide-by-N device.

17. The cardiometer of claim 9,
wherein said converting means comprises an up-counter.

25 18. The cardiometer of claim 9,
wherein said storing means comprises shift register
means.

19. The cardiometer of claim 9,
wherein said plurality of binary number signals each
30 comprises a plurality of bits, and said storing
means comprises a plurality of shift registers, each
for receiving a particular bit of each binary number
signal.

20. The cardiometer of claim 9,
35 wherein said comparing means includes an exclusive

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OR gate for receiving said stored binary number signals and said most recent binary number signal.

21. The cardiometer of claim 19, wherein said comparing means further includes means for excluding at least one of the least significant bits of each of said binary number signals from being compared.

22. The cardiometer of claim 9, wherein said comparing means includes means for issuing a compare signal each time said compared signals are within a predetermined percentage of each other, and wherein said displaying means includes means for issuing a display signal after receiving a plurality of said compare signals.

23. The cardiometer of claim 22, wherein said plurality of compare signals is three.

24. The cardiometer of claim 9, wherein said displaying means includes latch means for holding said most recent binary number signal prior to display, and means for displaying the contents of said latch means as an array of integers.



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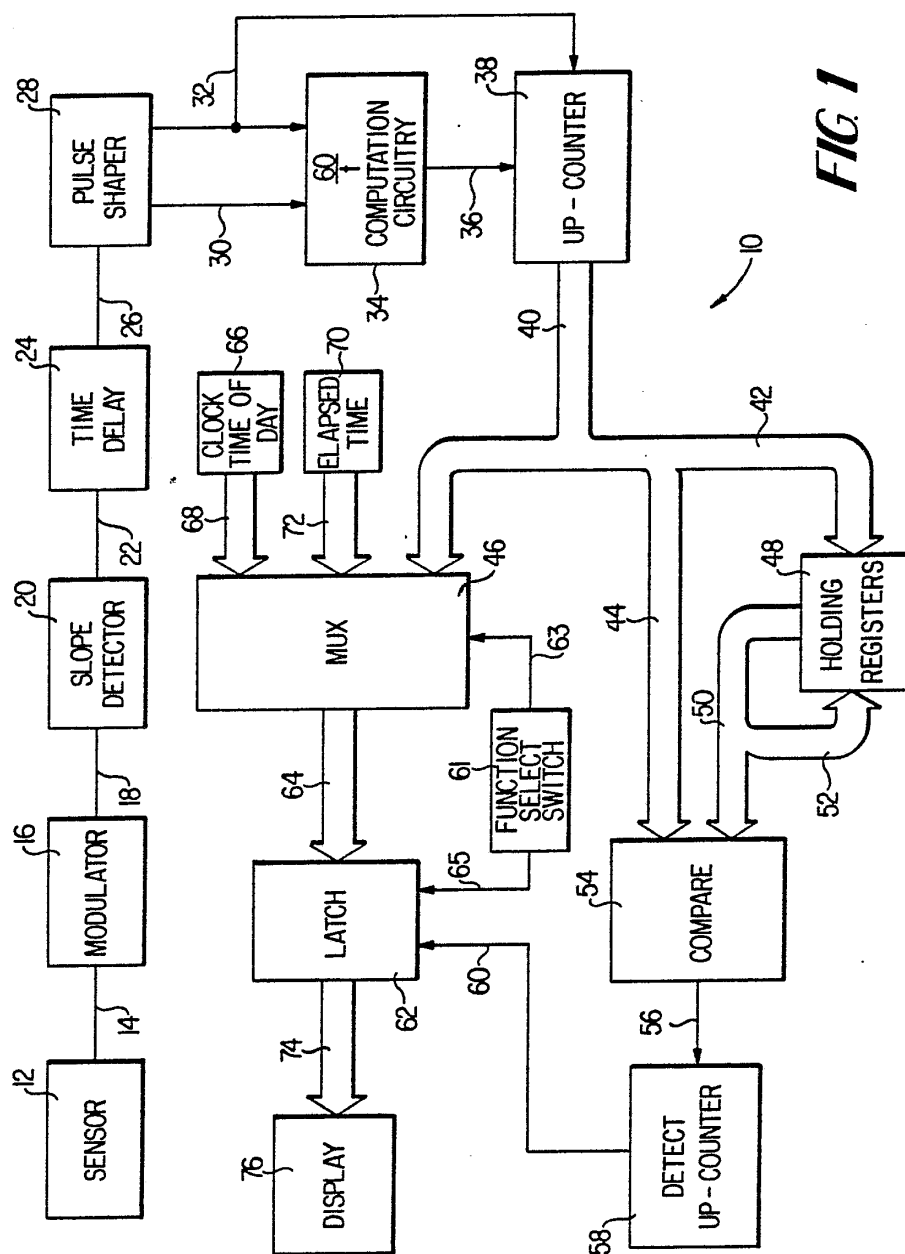
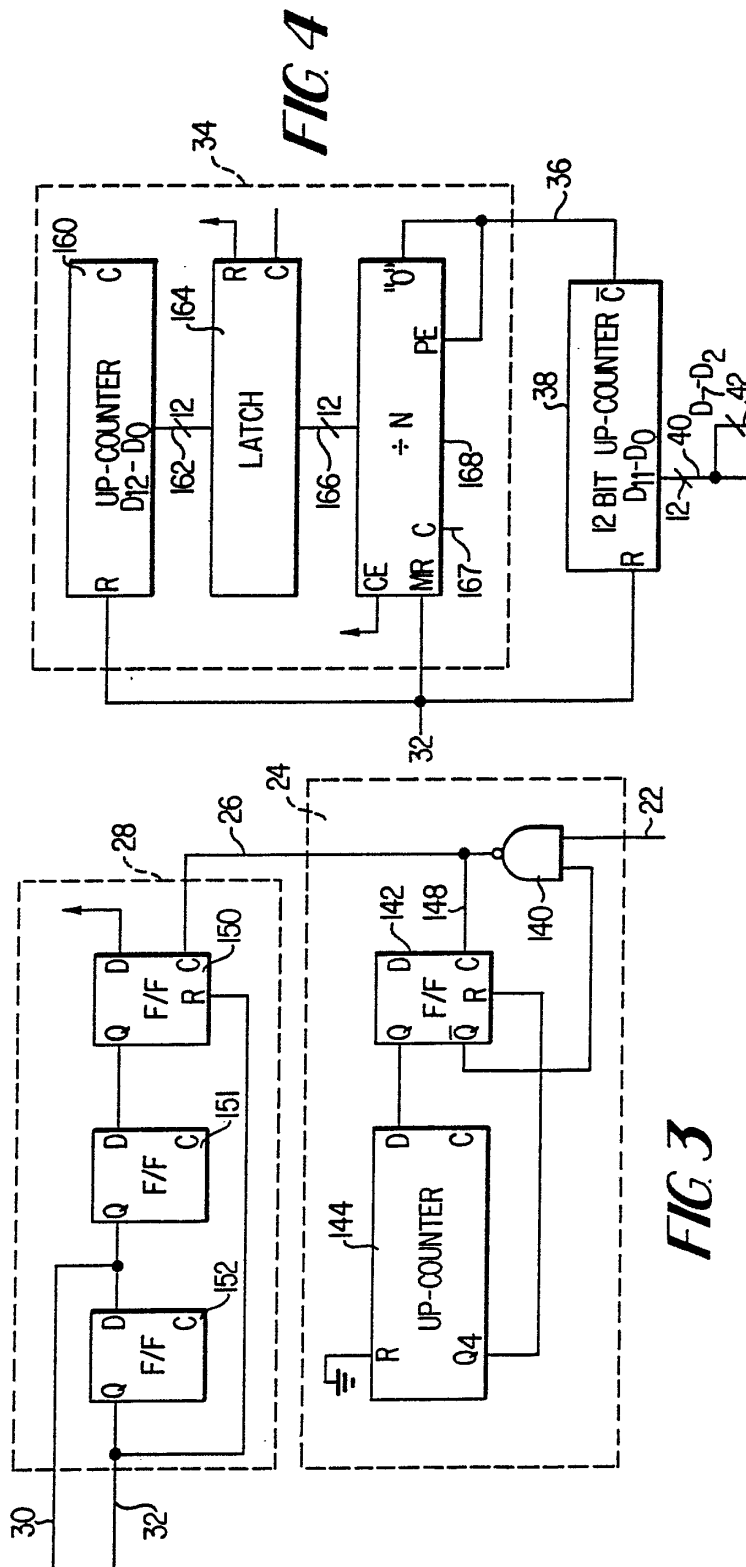
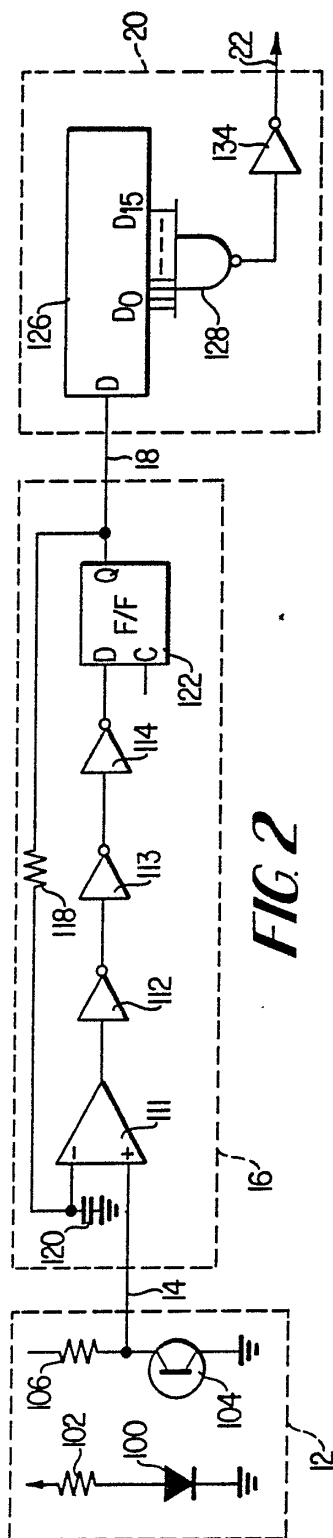


FIG 1



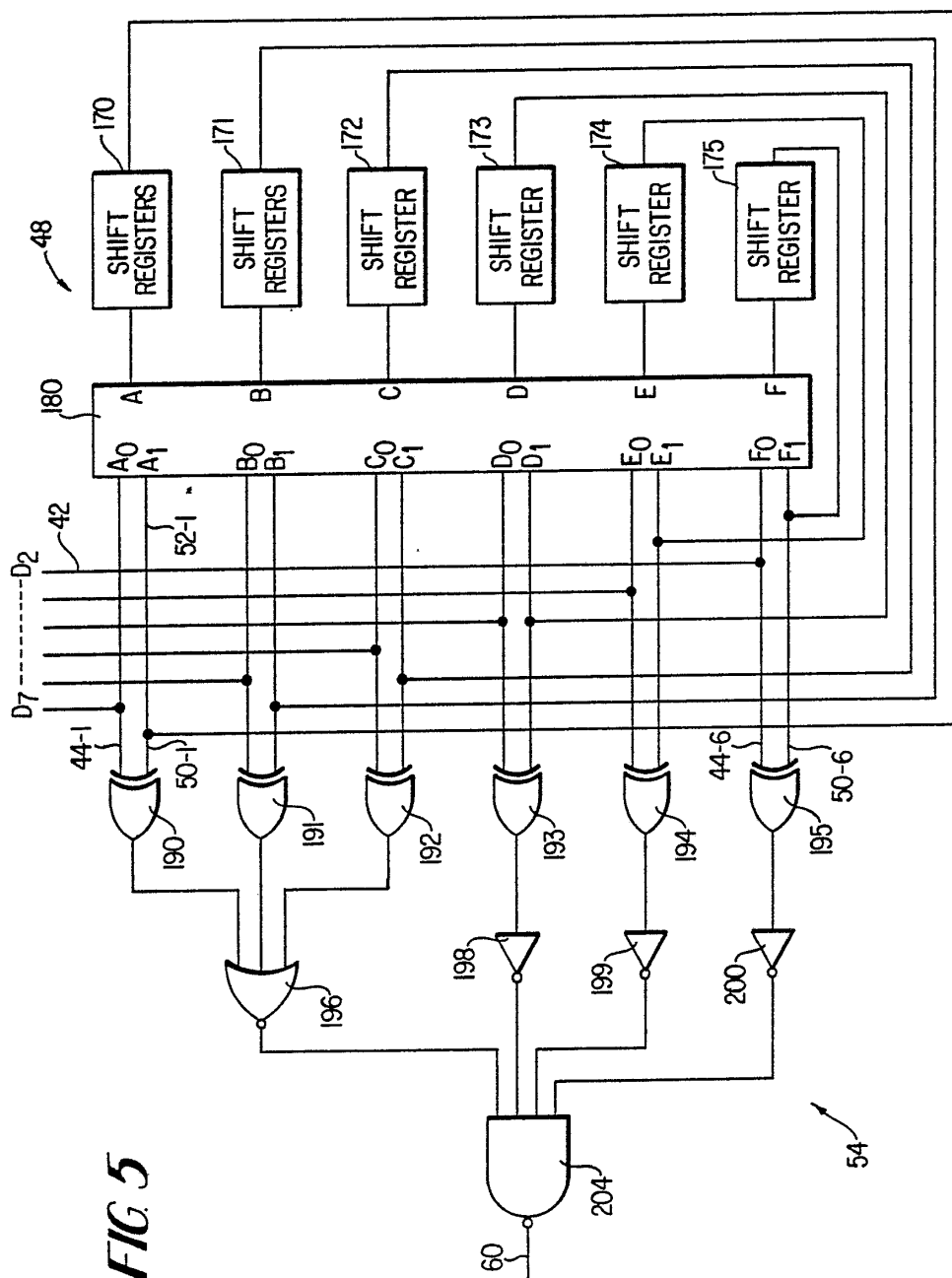


FIG. 5

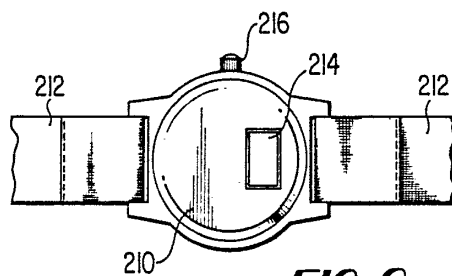
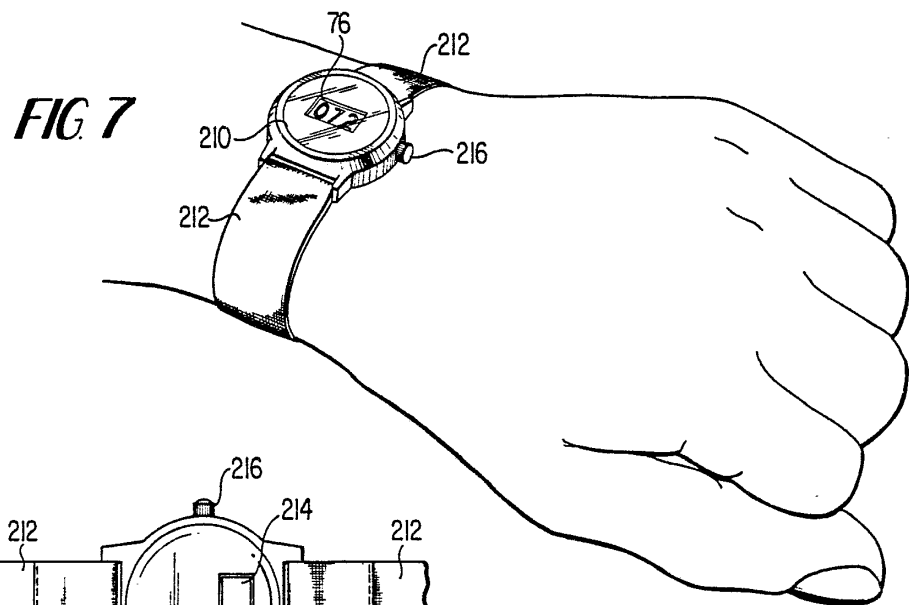
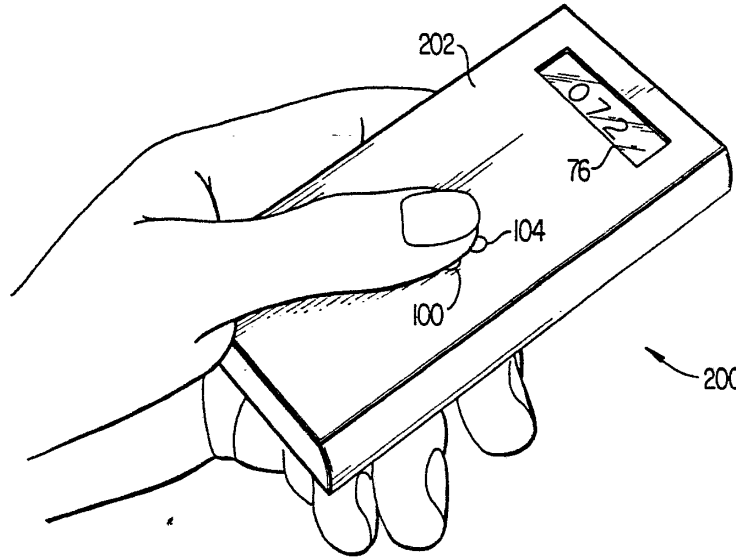


FIG 8

INTERNATIONAL SEARCH REPORT

International Application No PCT/US80/00839

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) ³		
According to International Patent Classification (IPC) or to both National Classification and IPC		
Int. Cl. ³	A61B 5/02	
U.S. Cl.	128/666,690	
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁴		
Classification System	Classification Symbols	
U.S.	128/666,687,689,690,706,707	
Documentation Searched other than Minimum Documentation to the extent that such Documents are included in the Fields Searched ⁵		
III. DOCUMENTS CONSIDERED TO BE RELEVANT ¹⁴		
Category ⁶	Citation of Document, ¹⁵ with indication, where appropriate, of the relevant passages ¹⁷	Relevant to Claim No. ¹⁸
X,E	US,A, 4,248,244 Published February 03, 1981 CHARNITSKI et al	1-2,4-5,9-10 21-24
X	US,A, 3,837,333 Published September 24, 1974 BRUCKHEIM	1-2,4-5,9-10 21-24
X	US,A, 4,022,192 Published May 10, 1977 LAUKIEN	1-2,4-5,9-10 21-24
X	US,A, 4,096,854 Published June 27, 1978 PERICA et al	8,11
X,E	US,A, 4,224,948 Published September 30, 1980 CRAMER, et al	7,8
X	US,A, 4,166,454 Published September 4, 1979 MEIJER	12,13
X	US,A, 3,613,670 Published October 19, 1971 EDENHOFER	3,6
X	US,A, 4,058,118 Published November 15, 1977 STUPAY et al	3,6
X	US,A, 3,908,636 Published September 30, 1975 PAGE	12
X	US,A, 3,858,574 Published January 7, 1975 PAGE	12
X	US,A, 4,030,483 Published June 21, 1977 STEVENS	12
X	US,A, 4,015,595 Published April 5, 1977 BENJAMIN Jr.	12
(Cont. On Suppl. Sheet 2)		
¹⁶ Special categories of cited documents: "A" document defining the general state of the art "E" earlier document but published on or after the international filing date "L" document cited for special reason other than those referred to in the other categories "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but on or after the priority date claimed "T" later document published on or after the international filing date or priority date and not in conflict with the application, but cited to understand the principle or theory underlying the invention "X" document of particular relevance		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search ¹⁹	Date of Mailing of this International Search Report ²⁰	
19 May 1981	02 JUN 1981	
International Searching Authority ¹	Signature of Authorized Officer ²⁰	
ISA/US	John Hanley <i>JCH</i> <i>C. Mitchell</i>	

Form PCT/ISA/210 (second sheet) (October 1977)

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

III

- | | | |
|---|-----------------|--|
| A | US,A, 3,717,140 | Published February 20, 1973
GREENWOOD |
| A | US,A, 4,018,219 | Published April 19, 1977
HOJAIBAN |
| A | US,A, 4,120,294 | Published October 17, 1978
WOLFE |

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE ¹⁰

This International search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers because they relate to subject matter ¹² not required to be searched by this Authority, namely:

2. ☐ Claim numbers because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out ¹³, specifically:

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING ¹¹

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.
2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:
3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

Remark on Protest

- ☐ The additional search fees were accompanied by applicant's protest.
- ☐ No protest accompanied the payment of additional search fees.

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