IN THE CLAIMS

We claim:

1. A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising:

addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

using attributes from said first and second device profiles.

2. The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device.

3. The method of claim 1, wherein said difference between said first and second device profiles includes different attributes; and said addressing said first memory location is made in response to a first memory transaction request; and

further including addressing said second memory location.

4. The method of claim 1, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

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said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes.

5. The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

6. The method of claim 5, wherein said different attribute qualifiers include different attribute values.

7. The method of claim 5, wherein said different attribute qualifiers include different attribute types.

8. The method of claim 5, wherein said shared attributes include a memory device type attribute.

9. The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

10. The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

11. The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

12. The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

13. The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of

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attributes that differs in value from a second page size attribute from said second set of attributes.

14. The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes.

15. The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device, and said second memory device interface attribute corresponds to a DRAM device interface.

16. The method of claim 2, wherein said using attributes from said first and second device profile further includes using a first partial page size attribute from said first set of attributes that differs in value from a second partial page size attribute from said second set of attributes.

17. The method of claim 16:

said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute; and

further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute.

18. The method of claim 8, wherein said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

19. The method of claim 8, wherein said first memory device type attribute corresponds to a NAND flash memory device and said second memory device type attribute corresponds to a NOR flash memory device.

20. The method of claim 2, further including:

using an address corresponding to a memory location from said first memory device and transferring a first data set, and

using an address corresponding to a memory location from said second memory device and transferring a second data set.

21. The method of claim 20, wherein:

said first set of attributes includes a first page size attribute, and said first data set includes a first data set size; and

if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size.

22. The method of claim 20, wherein:

said second set of attributes includes a second page size attribute, and said second data set includes a second data set size; and

if said second data set size is greater than said second page size attribute, said transferring said second data set includes:

performing a set of write operations on said second memory device that includes using a second transfer size equal to said second page size attribute until a remaining portion of said second data set that has not yet been written to said second device is less than said second page size attribute, and

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

23. The method of claim 20, wherein:

said first set of attributes includes a page size attribute and a block size attribute;

said first data set includes a first data set size;

if said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes:

performing a set of write operations on said first memory device that includes using a second transfer size equal to said page size attribute until a remaining portion of said first data set that has not yet been written to said first device is less than said page size attribute,

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size; and

said second device profile.

24. The method of claim 1, wherein said using attributes from said first and second device profile further includes:

performing respective write operations on said first and second memory devices by at least using a transfer size at least equal to a partial page size attribute from said first set of attributes and performing at least one write operation on said second memory device by at least using a transfer size at least equal to a partial page size attribute value from said second set of attributes; and

said attribute difference includes different attribute values of said first and second partial page size attributes.

25. The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size attribute of said first memory device.

26. The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a block size attribute value that corresponds to a block size attribute of said first memory device.

27. The method of claim 26, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

28. The method of claim 2, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

29. A computer readable medium comprising computer executable instructions adapted to cause a method of performing memory transactions on a first memory location and a second memory location, said method comprising:

addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory device, and said second device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles; and

using attributes from said first and second device profiles.

30. The computer readable medium of claim 29, wherein:

said first memory location is part of a memory space associated with a first memory device;

said second memory location is part of a memory space associated with a second memory device; and

said first and second memory devices comprise at least a portion of a memory store.

31. The computer readable medium of claim 30, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

32. The computer readable medium of claim 30, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

33. The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

34. The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes.

35. The computer readable medium of claim 29, wherein said means for addressing further includes:

said first and second device profiles having at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

36. The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

37. The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values.

38. The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types.

39. The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute.

40. The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

41. The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

42. The computer readable medium of claim 36, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

43. The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes.

44. The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device.

45. A memory controller for performing memory transactions, said memory controller comprising:

a means for addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said means for addressing uses attributes from said first and second device profiles.

46. The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

47. The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

48. The memory controller of claim 46, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said use of said attributes from said first and second device profiles by said means for addressing includes using said different attribute qualifiers for said shared attributes.

49. The memory controller of claim 46, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

50. The memory controller of claim 45, wherein said means for addressing further includes addressing said second memory location.

51. The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

52. The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values.

53. The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types.

54. The memory controller of claim 51, wherein said shared attributes include a memory device type attribute.

55. The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

56. The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

57. The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

58. The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device.

59. A memory controller comprising:

an interface controller coupled to a memory device interface and an IO device interface;

said interface controller disposed to perform a memory transaction by addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile;

said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said addressing of said first memory location includes using said attributes from said first device profile.

60. The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile.

61. The memory controller of claim 59, wherein said interface controller includes:

a main control device coupled to said memory device interface and to said data path;

a first memory bus controller coupled to said control device and said memory device interface; and

an IO bus controller coupled to said IO device interface and said control device.

62. The memory controller of claim 61, wherein said IO bus controller is disposed to respond to said memory transaction request by acknowledging said request and providing status to said main control device.

63. The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction, coordinates the operation of said memory device interface, and manages the transfer of memory transaction data between said IO device interface and said memory device interface through a data path.

64. The memory controller of claim 59, wherein said buffer is a FIFO and said data path includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface.

65. The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots.

66. The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a plurality of queue slots that buffer data from said IO device interface to said memory device interface.

67. The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from said memory device interface to said IO device interface.

68. The memory controller of claim59, further including a second memory bus controller coupled to said main control device and said memory device interface.

69. The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes.

70. The memory controller of claim 59, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

71. The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

72. The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute.

73. The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values.

74. The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values.

75. The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type.

76. The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values.

77. The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types.

78. The memory controller of claim 71, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

79. The memory controller of claim 71, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

80. An electronic storage device, comprising:

a memory controller disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said memory controller using attributes from said first and second device profiles.

81. The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that

differs in attribute value from a second block size attribute from said second set of attributes.

82. The electronic storage device of claim 80, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

83. The electronic storage device of claim 80, said memory controller further disposed to:

perform a write operation on said first memory device, if said memory transaction request is associated with a write request;

perform a read operation on said first memory device, if said memory transaction request is associated with a read request; and

wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using said second device profile in response to receiving a second memory transaction request.

84. The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

85. The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values.

86. The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute.

87. The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types.

88. The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said shared attributes.

89. The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device.

90. The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

91. The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

92. The electronic storage device of claim 84, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

93. The electronic storage device of claim 80, wherein said memory controller is further adapted to:

use a first partial page size attribute by performing a write operation on said first memory device and using a transfer size at least equal to said partial page size attribute; and

use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute.

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2187	

NOTIFICATION DATE	DELIVERY MODE
12/21/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	12/876,113	BRUCE ET AL.	
	Examiner	Art Unit	
	JARED RUTZ	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-93* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-93* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *04 September 2010* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-93, as originally filed on 9/4/2010, are pending in the instant application. Of these, there are 5 independent and 88 dependent claims.

Double Patenting

2. Applicant is advised that should claim 31 be found allowable, claim 32 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Objections

3. **Claim 68** is objected to because of the following informalities:

   a. **Claim 68** recites “The memory controller of claim59", the Examiner respectfully submits that there should be a space between claim and 59.

4. Appropriate correction is required.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. **Claims 29-44** are rejected under 35 U.S.C. 101 because they are directed to non-statutory subject matter.

7. As per **claims 29-44**, they are rejected because the applicant has provided evidence that the applicant intends the term "computer-readable storage medium" to include non-statutory matter. The applicant describes a computer-readable storage medium as including open ended language and thus it is reasonable to interpret it to include all possible mediums, including non-statutory mediums (see paragraph 0045). The words "storage" and/or "recording" are insufficient to convey only statutory embodiments to one of ordinary skill in the art absent an explicit and deliberate limiting definition or clear differentiation between storage media and transitory media in the disclosure. As such, the claim(s) is/are drawn to a form of energy. Energy is not one of the four categories of invention and therefore this/these claim(s) is/are not statutory. Energy is not a series of steps or acts and thus is not a process. Energy is not a physical article or object and as such is not a machine or manufacture. Energy is not a combination of substances and therefore not a composition of matter.

8. The Examiner suggests amending the claim(s) to read as a “non-transitory machine-readable storage medium”.

Claim Rejections - 35 USC § 112

9. The following is a quotation of 35 U.S.C. 112(a):
(a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), first paragraph:
The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. **Claims 45-58** are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 45 recites “a means for addressing”, and recites further details of said means. Claim 45 is a single means claim. As per MPEP 2164.08(a), a means recitation which does not appear in combination with another recited element of means is subject to an undue breadth rejection under 35 USC 112 first paragraph. A single means claim which covers every conceivable means for achieving the stated purpose is non-enabling for the scope of the claim because the specification discloses at most only those means known to the inventor. See *In re Hyatt*, 708 F.2d 712, 714-715, 218 USPQ 195, 197 (Fed. Cir. 1983). Claims 46-58 do not recite additional elements, and accordingly are rejected for the same reasons as claim 45.

11. The following is a quotation of 35 U.S.C. 112(b):

(B) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. **Claims 23, 31, 32, 35, 50, 61-64, 68, and 83** are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

13. **Claim 23** recites “and second device profile” in lines 12-13. The Examiner respectfully notes that this limitation has no apparent relationship to the rest of the claim, and its meaning in the claim is unclear.

14. **Claims 31 and 32** each recite the limitation "*said at least one attribute*" in line 1. There is insufficient antecedent basis for this limitation in the claim.

15. **Claim 35** recites the limitation "*said means for addressing*" in line 1. There is insufficient antecedent basis for this limitation in the claim.

16. **Claim 50** recites the limitation “*wherein said means for addressing further includes addressing said second memory location*”. It is unclear how a means for addressing, which is a structure, can include addressing, which is an action.

17. **Claim 61** recites the limitation "*said data path*" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

18. **Claims 62 and 63** depend from claim 61, and are rejected for the same reasons as claim 61.

19. **Claim 62** recites the limitation "*said memory transaction request*" in line 2. There is insufficient antecedent basis for this limitation in the claim.

20. **Claim 63** depends from claim 62, and is rejected for the same reason as claim 62.

21. **Claim 64** recites the limitation "*said buffer is a FIFO*" in line 1. There is insufficient antecedent basis for this limitation in the claim.

22. **Claim 64** recites the limitation "*said data path*" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

23. **Claim 68** recites the limitation "*said main control device*" in line 2. There is insufficient antecedent basis for this limitation in the claim.

24. **Claim 83** recites the limitation "*said memory transaction request*" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

25. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

26. **Claims 1-14, 20, 21, 25, 45-60, and 69-92** are rejected under 35 U.S.C. 102(e) as being anticipated by Falik et al. (US 8,200,879).

Claim 1 is taught by Falik as:

A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising: addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 2 is taught by Falik as:

The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 3 is taught by Falik as:

The method of claim 1, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

And said addressing said first memory location is made in response to a first memory transaction request. Column 18 lines 24-34 shows that applications on the main die 100 issue read and program commands.

And further including addressing said second memory location. Figure 6 shows that both sections can be addressed.

Claim 4 is taught by Falik as:

The method of claim 1, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 5 is taught by Falik as:

The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 6 is taught by Falik as:

The method of claim 5, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 7 is taught by Falik as:

The method of claim 5, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 8 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a memory device type attribute. Column 20 lines 30-36 shows that the registers can indicate if the device is self timed type flash memory or not.

Claim 9 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 10 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line

61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 11 is taught by Falik as:

The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 12 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 13 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of attributes that differs in value from a second page size attribute from

said second set of attributes. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 14 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 20 is taught by Falik as:

The method of claim 2, further including: using an address corresponding to a memory location from said first memory device and transferring a first data set. Column 16 lines 53-62 shows that an address and data are sent for a programming operation.

And using an address corresponding to a memory location from said second memory device and transferring a second data set. Column 14 lines 51-65 show that the standard address space is mapped to the logical sections into

which the arrays are grouped, showing that the second memory device is accessed using an address corresponding to the second memory device.

Claim 21 is taught by Falik as:

The method of claim 20, wherein: said first set of attributes includes a first page size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

And said first data set includes a first data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

And if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size. Column 27 lines 9-24 shows that when the number of bytes to be transferred to the FD have been transferred, the transfer process ends by setting the bus to a HiZ state.

Claim 25 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size

attribute of said first memory device. As discussed at column 27 lines 33-60, the program buffer corresponds to the batch size, which is the amount of data which can be programmed into the flash array at once.

Claim 45 is taught by Falik as:

A memory controller for performing memory transactions, said memory controller comprising: a means for addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14

lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And said means for addressing uses attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 46 is taught by Falik as:

The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 47 is taught by Falik as:

The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 48 is taught by Falik as:

The memory controller of claim 46, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said use of said attributes from said first and second device profiles by said means for addressing includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 49 is taught by Falik as:

The memory controller of claim 46, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 50 is taught by Falik as:

The memory controller of claim 45, wherein said means for addressing further includes addressing said second memory location. Figure 6 shows that both sections can be addressed.

Claim 51 is taught by Falik as:

The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 52 is taught by Falik as:

The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 53 is taught by Falik as:

The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 54 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 55 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 56 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 57 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 58 is taught by Falik as:

The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

Claim 59 is taught by Falik as:

A memory controller comprising: an interface controller coupled to a memory device interface and an IO device interface. Figure 4B shows interface controller 110 connected to bus 90 and internal bus 140.

Said interface controller disposed to perform a memory transaction by addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities

registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And said addressing of said first memory location includes using said attributes from said first device profile. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 60 is taught by Falik as:

The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile. Figure 6 shows that both sections can be addressed.

Claim 69 is taught by Falik as:

The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

Claim 70 is taught by Falik as:

The memory controller of claim 59, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 71 is taught by Falik as:

The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 72 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 73 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 74 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column

20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 75 is taught by Falik as:

The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 76 is taught by Falik as:

The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 77 is taught by Falik as:

The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20

line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 78 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 79 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 80 is taught by Falik as:

An electronic storage device, comprising: a memory controller disposed to address a first memory location and a second memory location which are

respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And said memory controller using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 81 is taught by Falik as:

The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command. Column 9 lines 5-18 shows that the interface performs appropriate requests for erasure.

Claim 82 is taught by Falik as:

The electronic storage device of claim 80, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 83 is taught by Falik as:

The electronic storage device of claim 80, said memory controller further disposed to: perform a write operation on said first memory device, if said memory transaction request is associated with a write request. Column 16 lines 53-64 shows that write transactions may be performed.

Perform a read operation on said first memory device, if said memory transaction request is associated with a read request. Column 16 lines 53-64 shows that read transactions may be performed.

And wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using said second device profile in response to receiving a second memory transaction request. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used for accesses to the groups of memory arrays.

Claim 84 is taught by Falik as:

The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 85 is taught by Falik as:

The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 86 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20

line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 87 is taught by Falik as:

The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 88 is taught by Falik as:

The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 89 is taught by Falik as:

The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

Claim 90 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 91 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 92 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim Rejections - 35 USC § 103

27. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

28. **Claims 15, 18, and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Nangle (US 7,330,954).

Claim 15 is taught by Falik as:

The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device. Column 21 lines 7-10 shows that the information can correspond to a flash device FD.

Although Falik column 21 lines 7-10 shows that other memory technologies such as SRAM may be used, it does not expressly teach that the second memory device attribute corresponds to a DRAM device interface.

With respect to claim 15, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 lines 51-67 shows that the memory devices may be flash memory and DRAM.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include flash memory and DRAM in the system of Falik.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 15**.

Claim 18 is taught by Falik as shown supra with respect to claim 8.

Falik does not expressly teach that said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

With respect to claim 18, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 line 51 through column 5 line 4 shows that the memory devices may be volatile memory that have a battery backup.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a volatile memory disposed to receive backup power from a portable power source.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 18**.

Claim 19 is taught by Falik as shown supra with respect to claim 8.

Falik does not expressly teach that said first memory device type attribute corresponds to a NAND flash memory device and said second memory device type attribute corresponds to a NOR flash memory device.

With respect to claim 19, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 lines 51-65 shows that the memory devices may be NAND or NOR type flash memories.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a volatile memory disposed to receive backup power from a portable power source.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 19**.

29. **Claims 16, 17, 22-24, and 93** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Sinclair et al. (US 2006/0184723).

Claim 16 if taught by Falik as shown supra with respect to claim 2.

Although Falik teaches that the width of the array is the minimum programming size of the array at column 20 lines 62-65, and that the width of the array is stored at column 20 lines 49-52, Falik does not expressly teach that a first and second partial page size attribute is stored and used.

With respect to claim 16, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claims 16 and 17**.

Claim 17 is taught by Falik and Sinclair as:

The method of claim 16: said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute. Sinclair paragraph 0168 shows that in a flash memory that supports

partial page programming, when sufficient data is transferred to the buffer, it is programmed to the page. Falik column 14 lines 51-60 and figure 3 shows that the first memory device group can be accessed.

And further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute. Sinclair paragraph 0168 shows that in a flash memory that supports partial page programming, when sufficient data is transferred to the buffer, it is programmed to the page. Falik column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

Claim 22 is taught by Falik as:

The method of claim 20, wherein: said second set of attributes includes a second page size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

And said second data set includes a second data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

And if said second data set size is greater than said second page size attribute, said transferring said second data set includes: performing a set of

write operations on said second memory device that includes using a second transfer size equal to said second page size attribute. Column 16 lines 48-52 shows that program buffer 19 may be a double buffer, allowing the programming of one chunk of data while another chunk of data is received. As discussed at column 27 lines 33-60, the program buffer corresponds to the batch size, which is the amount of data which can be programmed into the flash array at once.

Falik does not expressly teach that the transaction is made using a transfer size equal to the page size until a remaining portion of said second data set that has not yet been written to said second device is less than said second page size attribute and using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

With respect to claim 22, Sinclair teaches Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times. As discussed in paragraph 0168, when the end of the data group is received in the buffer and it is smaller than a full page of data, a partial page programming operation may be performed.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 22**.

Claim 23 is taught by Falik as:

The method of claim 20, wherein: said first set of attributes includes a page size attribute and a block size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Said first data set includes a first data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

If said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes: performing a set of write operations on said first memory device that includes using a second transfer size equal to said page size attribute […]. Column 27 lines 14-24 shows that bytes of data are sent until all the bytes have been sent.

And said second device profile. Column 14 lines 4-20 shows that each group of arrays has characteristics stored in the control, status, and capabilities registers 12.

Falik does not expressly teach that the transaction is made using a transfer size equal to the page size until a remaining portion of said first data set that has not yet been written to said first device is less than said first page size attribute and using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

With respect to claim 23, Sinclair teaches Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times. As discussed in paragraph 0168, when the end of the data group is received in the buffer and it is smaller than a full page of data, a partial page programming operation may be performed.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 23**.

Claim 24 is taught by Falik as shown supra with respect to claim 1, and further as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes: performing respective write operations on

said first and second memory devices by at least using a transfer size at least equal to a […] *page size attribute from said first set of attributes*. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations.

And performing at least one write operation on said second memory device by at least using a transfer size at least equal to a […] *page size attribute value from said second set of attributes*. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations. Column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

And said attribute difference includes different attribute values of said first and second […] *page size attributes*. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Although Falik teaches storing a page size attribute, it does not expressly teach storing a partial page size attribute.

With respect to claim 24, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 24**.

Claim 93 is taught by Falik as shown supra with respect to claim 80, and further as:

The electronic storage device of claim 80, wherein said memory controller is further adapted to: use a first partial page size attribute by performing a write operation on said first memory device and using a transfer size at least equal to said partial page size attribute. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations.

And use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations. Column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

Although Falik teaches storing a page size attribute, it does not expressly teach storing a partial page size attribute.

With respect to claim 93, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 93**.

30. **Claims 26-28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Lakhani et al. (US 6,961,805).

Claim 26 is taught by Falik as shown supra with respect to claim 1.

Falik further teaches, at column 20 lines 60-65, that Page Size Block1 stores the size of the minimal segment of a flash array erasable upon a single erase command. Additionally, column 16 line 53 through column 17 line 24 shows that data can be

written to a block of addresses by designating the starting address and performing a series of program continue operations.

Falik does not expressly teach using the block size attribute in performing a write operation that uses a transfer size that corresponds to the block size.

With respect to claim 26, Lakhani teaches, at column 18 lines 19-46, that predecoder 50 asserts sets of multiblock selection bits in response to control bits from the controller, which allows a designated number of blocks to be selected for writing at the same time.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to perform a write operation that uses a transfer size equal to the a block size attribute value that corresponds to a block size attribute of the first memory device.

The motivation for doing so would have been to reduce the time used to test the memory cells of the block, Lakhani column 8 lines 21-32.

Therefore, it would have been obvious to combine Lakhani with Falik to obtain the invention as specified in **claims 26 and 27**.

Claim 27 is taught by Lakhani as:

> *The method of claim 26, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value*. Column 13 lines 25-38 shows that a plurality of blocks can be selected at the same time.

Claim 28 is taught by Falik as shown supra with respect to claim 2.

Falik further teaches, at column 20 lines 60-65, that Page Size Block1 stores the size of the minimal segment of a flash array erasable upon a single erase command. Additionally, column 16 line 53 through column 17 line 24 shows that data can be written to a block of addresses by designating the starting address and performing a series of program continue operations.

Falik does not expressly teach using the block size attribute in performing a write operation that uses a transfer size that is equal to a multiple of the block size.

With respect to claim 28, Lakhani teaches, at column 18 lines 19-46, that predecoder 50 asserts sets of multiblock selection bits in response to control bits from the controller, which allows a designated number of blocks to be selected for writing at the same time.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to perform a write operation that uses a transfer size equal to the a block size attribute value that corresponds to a block size attribute of the first memory device.

The motivation for doing so would have been to reduce the time used to test the memory cells of the block, Lakhani column 8 lines 21-32.

Therefore, it would have been obvious to combine Lakhani with Falik to obtain the invention as specified in **claim 28**.

31. **Claims 29-44** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Rubinstein et al. (US 5,913,215).

Claim 29 is taught by Falik as:

Said method comprising: addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said first device profile representing a first set of attributes of said first memory device, and said second device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Falik does not expressly teach that the methods may be implemented using a computer readable medium comprising computer executable instructions.

With respect to claim 29, Rubinstein teaches at column 10, lines 3-15, that computer methods may be performed either by a series of instructions, or by specific hardware components that contain hard-wired logic for performing the method, or by any combination of the two.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a computer readable medium comprising computer executable instructions.

The rationale for doing so would have been that it is a known technique to implement methods in computer systems using a computer readable medium comprising computer executable instructions.

Therefore, it would have been obvious to combine Rubinstein with Falik to obtain the invention as recited in **claims 29-44**.

Claim 30 is taught by Falik as:

The computer readable medium of claim 29, wherein: said first memory location is part of a memory space associated with a first memory device, said second memory location is part of a memory space associated with a second

memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

And said first and second memory devices comprise at least a portion of a memory store. Figure 3 shows that the address space is mapped to the memory devices.

Claim 31 is taught by Falik as:

The computer readable medium of claim 30, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 32 is taught by Falik as:

The computer readable medium of claim 30, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 33 is taught by Falik as:

The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 34 is taught by Falik as:

The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

Claim 35 is taught by Falik as:

The computer readable medium of claim 29, wherein said means for addressing further includes: said first and second device profiles having at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 36 is taught by Falik as:

The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 37 is taught by Falik as:

The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 38 is taught by Falik as:

The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 39 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 40 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 41 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 42 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 43 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 44 is taught by Falik as:

The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

32. **Claims 61 and 64-68** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Chin et al. (US 2001/0010066).

Claim 61 is taught by Falik as shown supra with respect to claim 59.

Falik further teaches:

The memory controller of claim 59, wherein said interface controller includes: A first memory bus controller coupled to said control device and said memory device interface. Falik figure 4b item 116.

And an IO bus controller coupled to said IO device interface and said control device. Falik figure 4b item 117.

With respect to claim 61, Chin figure 2 teaches a bridge unit 104, which connects to a CPU bus 108 and a memory bus 110, including control logic 242, shown in paragraph 0037 to direct the operations of the queue storage elements through a network of control signals. Figure 2 also illustrates a data path between the CPU bus 108 and memory bus 110 through queues 250 and 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a main control device coupled to the memory device interface and data path as taught by Chin in the interface controller of Falik.

The motivation for doing so would have been to provide a means to manage the transfer of data through the interface performed by the system of Falik, see Chin paragraph 0037.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as specified in **claim 61**.

Claim 64 is taught by Falik as shown supra with respect to claim 59.

Falik does not expressly teach that a buffer is a FIFO or that a data path includes a plurality of queue slots.

With respect to claim 64, Chin teaches:

Wherein said buffer is a FIFO. Paragraph 0052 shows that queue 250 is a FIFO.

And said data path includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory. Figure 2 also shows read queue 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a FIFO and a data path including a plurality of queue slots in the system of Falik.

The motivation for doing so would have been to provide an interface that provides all devices in a computer system fair access to memory, Chin paragraph 0012.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as recited in **claim 64**.

Claim 65 is taught by Falik as shown supra with respect to claim 59.

Falik does not expressly teach that a data path includes a buffer having a plurality of queue slots.

With respect to claim 65, Chin teaches:

The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a FIFO and a data path including a plurality of queue slots in the system of Falik.

The motivation for doing so would have been to provide an interface that provides all devices in a computer system fair access to memory, Chin paragraph 0012.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as recited in **claims 65-67**.

Claim 66 is taught by Chin as:

The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a plurality of queue slots that buffer data from said IO device interface to said memory device interface. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory.

Claim 67 is taught by Chin as:

The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from

said memory device interface to said IO device interface. Figure 2 also shows read queue 252.

Claim 68 is taught by Falik as shown supra with respect to claim 1.

Falik further teaches a memory bus controller, figure 4b item 116, coupled to bus 90.

Falik does not expressly teach that the memory bus controller is coupled to a main control device.

With respect to claim 68, Chin teaches:

A second memory bus controller coupled to said main control device and said memory device interface. Figure 2 teaches a bridge unit 104, which connects to a CPU bus 108 and a memory bus 110, including control logic 242, shown in paragraph 0037 to direct the operations of the queue storage elements through a network of control signals. Figure 2 also illustrates a data path between the CPU bus 108 and memory bus 110 through queues 250 and 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a main control device coupled to the memory device interface and data path as taught by Chin in the interface controller of Falik.

The motivation for doing so would have been to provide a means to manage the transfer of data through the interface performed by the system of Falik, see Chin paragraph 0037.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as specified in **claim 68**.

33. **Claims 62 and 63** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Chin et al. (US 2001/0010066) as applied to claim 61 above, and further in view of Tsuruta (US 2007/0174506).

Claim 62 is taught by the combination of Falik and Chin as shown supra with respect to claim 61.

The combination of Falik and Chin does not expressly teach that the IO bus controller is disposed to respond to said memory transaction request by acknowledging said request and providing status to said main control device.

With respect to claim 62, Tsuruta teaches:

Wherein said IO bus controller is disposed to respond to said memory transaction request by acknowledging said request and providing status to said main control device. Paragraph 0183 shows that in response to a read req from the CPU, MEM-DMAC 232 issues a read ack signal. Paragraph 0186 shows that after the read operation is performed, a sequencer in the memory controller 231 issues ack to a sequencer in the MEM-DMAC 232.

At the time of the invention, it would have been obvious to use the acknowledgement system of Tsuruta in the combination of Falik and Chin.

The motivation for doing so would have been to provide coordination between the CPU interface and the read/write queues to perform the requested memory operations.

Therefore, it would have been obvious to combine Tsuruta with Falik and Chin to obtain the invention as specified in **claims 62 and 63**.

Claim 63 is taught by Chin as:

The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction. Paragraph 0052 shows that control logic provides control signals to the input and output selectors 351 and 353 that determine the values of the enable and select signals in response to a memory request from the CPU.

Coordinates the operation of said memory device interface. Paragraph 0052 shows that the data and address of each request is sent to the memory controller 200.

And manages the transfer of memory transaction data between said IO device interface and said memory device interface through a data path. Paragraph 0052 shows that data is transferred through the queue 250.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JARED RUTZ whose telephone number is (571)272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Christian Chace can be reached on (571)272-4190. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jared I Rutz
Primary Examiner
Art Unit 2187

/Jared I Rutz/
Primary Examiner, Art Unit 2187

REMARKS/ARGUMENTS

Double Patenting

Claim 31 is being amended to depend on claim 29. Accordingly, the double-patenting rejection is no longer applicable. The withdrawal of the double-patenting rejection to claims 31 and 32 is respectfully requested.

Claim Objections

A clerical correction is made on claim 68. Accordingly, the claim objection to claim 68 is no longer applicable. The withdrawal of the objection to claim 68 is respectfully requested.

Claim Rejections 35 USC 101

Claim 29 is being amended to recite the language, "non-transitory computer readable medium" in the preamble. Accordingly, the claim rejection to claims 29-44 is no longer applicable. The withdrawal of the rejection to claims 29-44 is respectfully requested.

Claim Rejections 35 USC 112

Claim 45 is being amended as shown above. Support for this claim amendment is found in, for example, paragraph [0029] of the filed application. Accordingly, the claim rejection to claims 45-58 is no longer applicable. The withdrawal of the rejection to claims 45-58is respectfully requested.

35 USC 102

Claims 1-14, 20, 21, 25, 45-60, and 69-92

Claims 1-11 and 16-33 are rejected under 35 U.S.C. 102(e) as allegedly being anticipated by US 8,200,879 to Falik et al. ("Falik"). Claims 1, 45, 59, and 80 are independent claims. Applicants respectfully traverse this rejection.

Applicants respectfully contend that independent claim 1 recites the following limitations that are not disclosed within the four corners of Falik: addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile; said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and using attributes from said first and second device profiles.

The Office implies that information in the registers 12 disclose the first and second set of attributes of claim 1 (Office Action: page 7). Applicants respectfully disagree with the Office based on at least the reasons presented below.

Falik discloses the device and status control register (Falik: Figure 5A) which provides status and control information for an entire memory device (Falik: column 19, lines 4-8). Falik also discloses a flash device capabilities register (Falik: Figure 5B) that provides

capabilities and properties information on the same entire memory device (Falik: column 19, lines 49-53). Therefore, these registers contain information directed to the same entire memory device and not directed to different memory locations. These registers do not contain a first set of attributes of a first memory location and also do not contain a second set of attributes of a second memory location.

Falik also discloses section properties registers that provide information on structural properties of sections of a flash device (Falik: column 20, lines 49-55). However, Falik discloses these sections as logical sections which are not memory locations (Falik: column 14, lines 51-60 and column 20, lines 49-56). These registers do not contain a first set of attributes of a first memory location and also do not contain a second set of attributes of a second memory location.

Based on at least the above discussion, Falik does not disclose and does not teach "said first memory location and a second memory location respectively associated with a first device profile and a second device profile; said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles" as required in claim 1.

Since Falik does not disclose and does not teach all the limitations of claim 1, claim 1 is not anticipated by the cited reference. Claim 1 is otherwise allowable.

Claims 2-14, 20, 21, and 25 depend from allowable claim 1; as such, they are also allowable for at least the same reasons as claim 1.

The withdrawal of the rejections to claims 1-14, 20, 21, and 25 is respectfully requested.

Independent claims 45, 59, and 80 recite at least some limitations similar to that as claim 1. Although claims 45, 59, and 80 are different, Applicants respectfully argue that in this case the above arguments regarding the patentability of claim 1 apply with equal force with respect to claims 45, 59, and 80. Since Falik does not disclose and does not teach all the limitations of claims 45, 59, and 80, claims 45, 59, and 80 are not anticipated by the cited reference. Claims 45, 59, and 80 are otherwise allowable.

Claims 46-58 depend from allowable claim 45; as such, they are also allowable for at least the same reasons as claim 45.

Claims 60 and 69-79 depend from allowable claim 59; as such, they are also allowable for at least the same reasons as claim 59.

Claims 81-92 depend from allowable claim 80; as such, they are also allowable for at least the same reasons as claim 80.

The withdrawal of the rejection to claims 45-60 and 69-92 is respectfully requested.

Claims 15, 18, and 19

Claims 15, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 7,330,954 to Nangle.

Claims 15, 18, and 19 depend from allowable claim 1; as such, they are also allowable for at least the same reasons a claim 1.

The withdrawal of the rejection of claims 15, 18, and 19 is respectfully requested.

Claims 16, 17, 22-24, and 93

Claims 16, 17, 22-24, and 93 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 2006/0184723 to Sinclair.

Claims 16, 17, and 22-24 depend from allowable claim 1; as such, they are also allowable for at least the same reasons a claim 1.

Claim 93 depends from allowable claim 80; as such, claim 93 is also allowable for at least the same reasons a claim 1.

The withdrawal of the rejection of claims 16, 17, 22-24, and 93 is respectfully requested.

Claims 26-28

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 6961,805 to Lakhani et al.

Claims 26-28 depend from allowable claim 1; as such, they are also allowable for at least the same reasons a claim 1.

The withdrawal of the rejection of claims 26-28 is respectfully requested.

Claims 29-44

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 5,913,215 to Rubinstein.

The Office admits that Falik does not expressly teach that the methods may be implemented using a computer readable medium comprising computer executable instructions. In order to supply the missing limitations, the Office combines Falik with Rubinstein. The Office argues it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a computer readable medium comprising computer executable instructions (Office Action: page 44). The Applicants respectfully disagree with the assertions of the Office.

Independent claim 29 recite at least some limitations similar to that as claim 1. Although claim 29 is different, Applicants respectfully argue that in this case the above arguments regarding the patentability of claim 1 apply with equal force with respect to claim 29.

Since Falik and Rubinstein, considered individually or in combination, do not disclose and does not teach all the limitations of claim 29, claim 29 is not rendered obvious in view the cited references. Claim 29 is otherwise allowable.

Claims 30-44 depend from allowable claim 29; as such, they are also allowable for at least the same reasons a claim 29.

The withdrawal of the rejection of claims 29-44 is respectfully requested.

Claims 61 and 64-68

Claims 61 and 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 2001/0010066 to Chin et al.

Claims 61 and 64-68 depend from allowable claim 59; as such, they are also allowable for at least the same reasons a claim 59.

The withdrawal of the rejection of claims 61 and 64-68 is respectfully requested.

Claims 62 and 63

Claims 61 and 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of Chin as applied to claim 61 above, and further in view of US 2007/0174506 to Tsuruta.

Claims 62 and 63 depend from allowable claim 59; as such, they are also allowable for at least the same reasons a claim 59.

The withdrawal of the rejection of claims 62 and 63 is respectfully requested.

New dependent claims 94-97

New dependent claims 94-97 are being added. The new claims are supported in the filed application, for example, in Figures 1, 2A, 2B, and 2C, and accompanying text, and in paragraph [0015]. Applicants respectfully request the allowance of these claims.

Applicants respectfully request the allowance of the claims.

Conclusion

Claims 1-97 herein are allowable, and a timely Notice of Allowance is respectfully requested.

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (408) 256-0244.

Date: March 21, 2013

Respectfully submitted,

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising:

addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

using attributes from said first and second device profiles.

2. (original) The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device.

3. (original) The method of claim 1, wherein said difference between said first and second device profiles includes different attributes; and said addressing said first memory location is made in response to a first memory transaction request; and

further including addressing said second memory location.

4. (original) The method of claim 1, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes.

5. (original) The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

6. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute values.

7. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute types.

8. (original) The method of claim 5, wherein said shared attributes include a memory device type attribute.

9. (original) The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

10. (original) The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

11. (original) The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

12. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

13. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of attributes that differs in value from a second page size attribute from said second set of attributes.

14. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes.

15. (original) The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device, and said second memory device interface attribute corresponds to a DRAM device interface.

16. (original) The method of claim 2, wherein said using attributes from said first and second device profile further includes using a first partial page size attribute from said first set of attributes that differs in value from a second partial page size attribute from said second set of attributes.

17. (original) The method of claim 16:

said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute; and

further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute.

18. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

19. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a NAND flash memory device and said second memory device type attribute corresponds to a NOR flash memory device.

20. (original) The method of claim 2, further including:

using an address corresponding to a memory location from said first memory device and transferring a first data set, and

using an address corresponding to a memory location from said second memory device and transferring a second data set.

21. (original) The method of claim 20, wherein:

said first set of attributes includes a first page size attribute, and said first data set includes a first data set size; and

if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size.

22. (original) The method of claim 20, wherein:

said second set of attributes includes a second page size attribute, and said second data set includes a second data set size; and

if said second data set size is greater than said second page size attribute, said transferring said second data set includes:

performing a set of write operations on said second memory device that includes using a second transfer size equal to said second page size attribute until a remaining portion of said second data set that has not yet been written to said second device is less than said second page size attribute, and

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

23. (currently amended) The method of claim 20, wherein:

said first set of attributes includes a page size attribute and a block size attribute;

said first data set includes a first data set size;

if said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes:

performing a set of write operations on said first memory device that includes using a second transfer size

equal to said page size attribute until a remaining portion of said first data set that has not yet been written to said first device is less than said page size attribute,

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size; [[and

said second device profile]].

24. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes:

performing respective write operations on said first and second memory devices by at least using a transfer size at least equal to a partial page size attribute from said first set of attributes and performing at least one write operation on said second memory device by at least using a transfer size at least equal to a partial page size attribute value from said second set of attributes; and

said attribute difference includes different attribute values of said first and second partial page size attributes.

25. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size attribute of said first memory device.

26. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a block size attribute value that corresponds to a block size attribute of said first memory device.

27. (original) The method of claim 26, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

28. (original) The method of claim 2, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

29. (currently amended) A non-transitory computer readable medium comprising computer executable instructions adapted to cause a method of performing memory transactions on a first memory location and a second memory location, said method comprising:

addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory device, and said second

device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles; and

using attributes from said first and second device profiles.

30. (original) The computer readable medium of claim 29, wherein:

said first memory location is part of a memory space associated with a first memory device;

said second memory location is part of a memory space associated with a second memory device; and

said first and second memory devices comprise at least a portion of a memory store.

31. (currently amended) The computer readable medium of claim [[30]]29, wherein [[said]] at least one attribute of said attributes includes a block size and said difference includes a block size value of [[said]]a first memory device and a block size value of [[said]]a second memory device.

32. (currently amended) The computer readable medium of claim 30, wherein [[said]] at least one attribute of said attributes includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

33. (original) The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

34. (original) The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes.

35. (currently amended) The computer readable medium of claim 29, wherein said [[means for]] addressing further includes:

said first and second device profiles having at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

36. (original) The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

37. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values.

38. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types.

39. (original) The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute.

40. (original) The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

41. (original) The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

42. (original) The computer readable medium of claim 36, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

43. (original) The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes.

44. (original) The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device.

45. (currently amended) A memory controller for performing memory transactions, said memory controller comprising:

a means for addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile;

wherein said means for addressing includes an interface controller means for processing memory transaction requests;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said means for addressing uses attributes from said first and second device profiles.

46. (original) The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

47. (original) The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute

value from a second block size attribute from said second set of attributes.

48. (original) The memory controller of claim 46, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said use of said attributes from said first and second device profiles by said means for addressing includes using said different attribute qualifiers for said shared attributes.

49. (original) The memory controller of claim 46, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

50. (currently amended) The memory controller of claim 45, wherein said means for addressing further includes a means for addressing said second memory location.

51. (original) The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

52. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values.

53. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types.

54. (original) The memory controller of claim 51, wherein said shared attributes include a memory device type attribute.

55. (original) The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

56. (original) The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

57. (original) The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

58. (original) The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device.

59. (original) A memory controller comprising:

an interface controller coupled to a memory device interface and an IO device interface;

said interface controller disposed to perform a memory transaction by addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile;

said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said addressing of said first memory location includes using said attributes from said first device profile.

60. (original) The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile.

61. (currently amended) The memory controller of claim 59, wherein said interface controller includes:

a main control device coupled to said memory device interface and to [[said]]a data path;

a first memory bus controller coupled to said control device and said memory device interface; and

an IO bus controller coupled to said IO device interface and said control device.

62. (currently amended) The memory controller of claim 61, wherein said IO bus controller is disposed to respond to [[said]]a memory transaction request by acknowledging said request and providing status to said main control device.

63. (original) The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction, coordinates the operation of said memory device interface, and manages the transfer of memory transaction data between said IO device interface and said memory device interface through a data path.

64. (currently amended) The memory controller of claim 59, [[wherein]]further including [[said]]a buffer [[is]]comprising a FIFO and [[said]]a data path that includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface.

65. (original) The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots.

66. (original) The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a

plurality of queue slots that buffer data from said IO device interface to said memory device interface.

67. (original) The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from said memory device interface to said IO device interface.

68. (currently amended) The memory controller of [[claim59]]claim 59, further including a second memory bus controller coupled to [[said]]a main control device and said memory device interface.

69. (original) The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes.

70. (original) The memory controller of claim 59, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

71. (original) The memory controller of claim 59, wherein said difference includes different attribute qualifiers for

at least one set of shared attributes from said first and second device profiles.

72. (original) The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute.

73. (original) The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values.

74. (original) The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values.

75. (original) The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type.

76. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values.

77. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types.

78. (original) The memory controller of claim 71, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

79. (original) The memory controller of claim 71, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

80. (original) An electronic storage device, comprising:

a memory controller disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said memory controller using attributes from said first and second device profiles.

81. (original) The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

82. (original) The electronic storage device of claim 80, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

83. (currently amended) The electronic storage device of claim 80, said memory controller further disposed to:

perform a write operation on said first memory device, if [[said]]a memory transaction request is associated with a write request;

perform a read operation on said first memory device, if said memory transaction request is associated with a read request; and

wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using said second device profile in response to receiving a second memory transaction request.

84. (original) The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

85. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values.

86. (original) The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute.

87. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types.

88. (original) The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said shared attributes.

89. (original) The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device.

90. (original) The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

91. (original) The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

92. (original) The electronic storage device of claim 84, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

93. (original) The electronic storage device of claim 80, wherein said memory controller is further adapted to:

use a first partial page size attribute by performing a write operation on said first memory device and using a

transfer size at least equal to said partial page size attribute; and

use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute.

94. (new) The method of claim 1, wherein the first memory location and the second memory location are addressable memory locations.

95. (new) The memory controller of claim 45, wherein the first memory location and the second memory location are addressable memory locations.

96. (new) The memory controller of claim 59, wherein the first memory location and the second memory location are addressable memory locations.

97. (new) The electronic device of claim 80, wherein the first memory location and the second memory location are addressable memory locations.

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EXAMINER	
RUTZ, JARED IAN	
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NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 12/876,113	Applicant(s) BRUCE ET AL.	
	Examiner JARED RUTZ	Art Unit 2187	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2013*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-97* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-97* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some * c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Interim copies:

a)☐ All b)☐ Some c)☐ None of the: Interim copies of the priority documents have been received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-97, as amended on 3/26/2013, are pending in the instant application. Applicant's arguments submitted 3/26/2013 have been carefully and fully considered, but are not found fully persuasive. The instant Office action is made **FINAL**.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-97** are rejected under 35 U.S.C. 102(e) as being anticipated by Falik et al. (US 8,200,879).

Claim 1 is taught by Falik as:

A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising: addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and

capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 2 is taught by Falik as:

The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 3 is taught by Falik as:

The method of claim 1, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

And said addressing said first memory location is made in response to a first memory transaction request. Column 18 lines 24-34 shows that applications on the main die 100 issue read and program commands.

And further including addressing said second memory location. Figure 6 shows that both sections can be addressed.

Claim 4 is taught by Falik as:

The method of claim 1, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 5 is taught by Falik as:

The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 6 is taught by Falik as:

The method of claim 5, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 7 is taught by Falik as:

The method of claim 5, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 8 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a memory device type attribute. Column 20 lines 30-36 shows that the registers can indicate if the device is self timed type flash memory or not.

Claim 9 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 10 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 11 is taught by Falik as:

The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size,

memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 12 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 13 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of attributes that differs in value from a second page size attribute from said second set of attributes. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 14 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 20 is taught by Falik as:

The method of claim 2, further including: using an address corresponding to a memory location from said first memory device and transferring a first data set. Column 16 lines 53-62 shows that an address and data are sent for a programming operation.

And using an address corresponding to a memory location from said second memory device and transferring a second data set. Column 14 lines 51-65 show that the standard address space is mapped to the logical sections into which the arrays are grouped, showing that the second memory device is accessed using an address corresponding to the second memory device.

Claim 21 is taught by Falik as:

The method of claim 20, wherein: said first set of attributes includes a first page size attribute. Column 20 lines 62-65 shows that the minimum

programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

And said first data set includes a first data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

And if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size. Column 27 lines 9-24 shows that when the number of bytes to be transferred to the FD have been transferred, the transfer process ends by setting the bus to a HiZ state.

Claim 25 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size attribute of said first memory device. As discussed at column 27 lines 33-60, the program buffer corresponds to the batch size, which is the amount of data which can be programmed into the flash array at once.

Claim 45 is taught by Falik as:

A memory controller for performing memory transactions, said memory controller comprising: a means for addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Wherein said means for addressing includes an interface controller means for processing memory transaction requests. Figure 4B, flash bus transactions state machine 116.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And said means for addressing uses attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 46 is taught by Falik as:

The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 47 is taught by Falik as:

The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 48 is taught by Falik as:

The memory controller of claim 46, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows

that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said use of said attributes from said first and second device profiles by said means for addressing includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 49 is taught by Falik as:

The memory controller of claim 46, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 50 is taught by Falik as:

The memory controller of claim 45, wherein said means for addressing further includes a means for addressing said second memory location. Figure 6 shows that both sections can be addressed.

Claim 51 is taught by Falik as:

The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 52 is taught by Falik as:

The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 53 is taught by Falik as:

The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 54 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6

shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 55 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 56 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 57 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size,

block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 58 is taught by Falik as:

The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

Claim 59 is taught by Falik as:

A memory controller comprising: an interface controller coupled to a memory device interface and an IO device interface. Figure 4B shows interface controller 110 connected to bus 90 and internal bus 140.

Said interface controller disposed to perform a memory transaction by addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column

16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And said addressing of said first memory location includes using said attributes from said first device profile. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 60 is taught by Falik as:

The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile. Figure 6 shows that both sections can be addressed.

Claim 69 is taught by Falik as:

The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-

48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

Claim 70 is taught by Falik as:

The memory controller of claim 59, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 71 is taught by Falik as:

The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 72 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 73 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 74 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 75 is taught by Falik as:

The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 76 is taught by Falik as:

The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 77 is taught by Falik as:

The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 78 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block

size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 79 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 80 is taught by Falik as:

An electronic storage device, comprising: a memory controller disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the

standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And said memory controller using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 81 is taught by Falik as:

The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command. Column 9 lines 5-18 shows that the interface performs appropriate requests for erasure.

Claim 82 is taught by Falik as:

The electronic storage device of claim 80, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 83 is taught by Falik as:

The electronic storage device of claim 80, said memory controller further disposed to: perform a write operation on said first memory device, if a memory transaction request is associated with a write request. Column 16 lines 53-64 shows that write transactions may be performed.

Perform a read operation on said first memory device, if said memory transaction request is associated with a read request. Column 16 lines 53-64 shows that read transactions may be performed.

And wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using said second device profile in response to receiving a second memory transaction request. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used for accesses to the groups of memory arrays.

Claim 84 is taught by Falik as:

The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 85 is taught by Falik as:

The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 86 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 87 is taught by Falik as:

The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20

line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 88 is taught by Falik as:

The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 89 is taught by Falik as:

The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

Claim 90 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 91 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 92 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 94 is taught by Falik as:

The method of claim 1, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 95 is taught by Falik as:

The memory controller of claim 45, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 96 is taught by Falik as:

The memory controller of claim 59, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 97 is taught by Falik as:

The electronic device of claim 80, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which

may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 15, 18, and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Nangle (US 7,330,954).

Claim 15 is taught by Falik as:

The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device. Column 21 lines 7-10 shows that the information can correspond to a flash device FD.

Although Falik column 21 lines 7-10 shows that other memory technologies such as SRAM may be used, it does not expressly teach that the second memory device attribute corresponds to a DRAM device interface.

With respect to claim 15, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 lines 51-67 shows that the memory devices may be flash memory and DRAM.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include flash memory and DRAM in the system of Falik.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 15**.

Claim 18 is taught by Falik as shown supra with respect to claim 8.

Falik does not expressly teach that said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

With respect to claim 18, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 line 51 through column 5 line 4 shows that the memory devices may be volatile memory that have a battery backup.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a volatile memory disposed to receive backup power from a portable power source.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 18**.

Claim 19 is taught by Falik as shown supra with respect to claim 8.

Falik does not expressly teach that said first memory device type attribute corresponds to a NAND flash memory device and said second memory device type attribute corresponds to a NOR flash memory device.

With respect to claim 19, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 lines 51-65 shows that the memory devices may be NAND or NOR type flash memories.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a volatile memory disposed to receive backup power from a portable power source.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 19**.

6. **Claims 16, 17, 22-24, and 93** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Sinclair et al. (US 2006/0184723).

Claim 16 if taught by Falik as shown supra with respect to claim 2.

Although Falik teaches that the width of the array is the minimum programming size of the array at column 20 lines 62-65, and that the width of the array is stored at column 20 lines 49-52, Falik does not expressly teach that a first and second partial page size attribute is stored and used.

With respect to claim 16, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claims 16 and 17**.

Claim 17 is taught by Falik and Sinclair as:

The method of claim 16: said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute. Sinclair paragraph 0168 shows that in a flash memory that supports partial page programming, when sufficient data is transferred to the buffer, it is programmed to the page. Falik column 14 lines 51-60 and figure 3 shows that the first memory device group can be accessed.

And further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute. Sinclair paragraph 0168 shows that in a flash memory that supports partial page programming, when sufficient data is transferred to the buffer, it is programmed to the page. Falik column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

Claim 22 is taught by Falik as:

The method of claim 20, wherein: said second set of attributes includes a second page size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

And said second data set includes a second data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

And if said second data set size is greater than said second page size attribute, said transferring said second data set includes: performing a set of write operations on said second memory device that includes using a second transfer size equal to said second page size attribute. Column 16 lines 48-52 shows that program buffer 19 may be a double buffer, allowing the programming of one chunk of data while another chunk of data is received. As discussed at column 27 lines 33-60, the program buffer corresponds to the batch size, which is the amount of data which can be programmed into the flash array at once.

Falik does not expressly teach that the transaction is made using a transfer size equal to the page size until a remaining portion of said second data set that has not yet been written to said second device is less than said second page size attribute and using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

With respect to claim 22, Sinclair teaches Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times. As discussed in paragraph 0168, when the end of the data group is received in the buffer and it is smaller than a full page of data, a partial page programming operation may be performed.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 22**.

Claim 23 is taught by Falik as:

The method of claim 20, wherein: said first set of attributes includes a page size attribute and a block size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Said first data set includes a first data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

If said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes: performing a set of write

operations on said first memory device that includes using a second transfer size equal to said page size attribute [...]. Column 27 lines 14-24 shows that bytes of data are sent until all the bytes have been sent.

Falik does not expressly teach that the transaction is made using a transfer size equal to the page size until a remaining portion of said first data set that has not yet been written to said first device is less than said first page size attribute and using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

With respect to claim 23, Sinclair teaches Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times. As discussed in paragraph 0168, when the end of the data group is received in the buffer and it is smaller than a full page of data, a partial page programming operation may be performed.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 23**.

Claim 24 is taught by Falik as shown supra with respect to claim 1, and further as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes: performing respective write operations on said first and second memory devices by at least using a transfer size at least equal to a […] *page size attribute from said first set of attributes*. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations.

And performing at least one write operation on said second memory device by at least using a transfer size at least equal to a […] *page size attribute value from said second set of attributes*. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations. Column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

And said attribute difference includes different attribute values of said first and second […] *page size attributes*. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Although Falik teaches storing a page size attribute, it does not expressly teach storing a partial page size attribute.

With respect to claim 24, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 24**.

Claim 93 is taught by Falik as shown supra with respect to claim 80, and further as:

The electronic storage device of claim 80, wherein said memory controller is further adapted to: use a first partial page size attribute by performing a write operation on said first memory device and using a transfer size at least equal to said partial page size attribute. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations.

And use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing

address locations. Column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

Although Falik teaches storing a page size attribute, it does not expressly teach storing a partial page size attribute.

With respect to claim 93, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 93**.

7. **Claims 26-28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Lakhani et al. (US 6,961,805).

Claim 26 is taught by Falik as shown supra with respect to claim 1.

Falik further teaches, at column 20 lines 60-65, that Page Size Block1 stores the size of the minimal segment of a flash array erasable upon a single erase command.

Additionally, column 16 line 53 through column 17 line 24 shows that data can be written to a block of addresses by designating the starting address and performing a series of program continue operations.

Falik does not expressly teach using the block size attribute in performing a write operation that uses a transfer size that corresponds to the block size.

With respect to claim 26, Lakhani teaches, at column 18 lines 19-46, that predecoder 50 asserts sets of multiblock selection bits in response to control bits from the controller, which allows a designated number of blocks to be selected for writing at the same time.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to perform a write operation that uses a transfer size equal to the a block size attribute value that corresponds to a block size attribute of the first memory device.

The motivation for doing so would have been to reduce the time used to test the memory cells of the block, Lakhani column 8 lines 21-32.

Therefore, it would have been obvious to combine Lakhani with Falik to obtain the invention as specified in **claims 26 and 27**.

Claim 27 is taught by Lakhani as:

> *The method of claim 26, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a*

transfer size equal to a multiple of said block size attribute value. Column 13 lines 25-38 shows that a plurality of blocks can be selected at the same time.

Claim 28 is taught by Falik as shown supra with respect to claim 2.

Falik further teaches, at column 20 lines 60-65, that Page Size Block1 stores the size of the minimal segment of a flash array erasable upon a single erase command. Additionally, column 16 line 53 through column 17 line 24 shows that data can be written to a block of addresses by designating the starting address and performing a series of program continue operations.

Falik does not expressly teach using the block size attribute in performing a write operation that uses a transfer size that is equal to a multiple of the block size.

With respect to claim 28, Lakhani teaches, at column 18 lines 19-46, that predecoder 50 asserts sets of multiblock selection bits in response to control bits from the controller, which allows a designated number of blocks to be selected for writing at the same time.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to perform a write operation that uses a transfer size equal to the a block size attribute value that corresponds to a block size attribute of the first memory device.

The motivation for doing so would have been to reduce the time used to test the memory cells of the block, Lakhani column 8 lines 21-32.

Therefore, it would have been obvious to combine Lakhani with Falik to obtain the invention as specified in **claim 28**.

8. **Claims 29-44** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Rubinstein et al. (US 5,913,215).

Claim 29 is taught by Falik as:

Said method comprising: addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said first device profile representing a first set of attributes of said first memory device, and said second device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14

lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Falik does not expressly teach that the methods may be implemented using a non-transitory computer readable medium comprising computer executable instructions.

With respect to claim 29, Rubinstein teaches at column 10, lines 3-15, that computer methods may be performed either by a series of instructions, or by specific hardware components that contain hard-wired logic for performing the method, or by any combination of the two.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a computer readable medium comprising computer executable instructions.

The rationale for doing so would have been that it is a known technique to implement methods in computer systems using a non-transitory computer readable medium comprising computer executable instructions.

Therefore, it would have been obvious to combine Rubinstein with Falik to obtain the invention as recited in **claims 29-44**.

Claim 30 is taught by Falik as:

The computer readable medium of claim 29, wherein: said first memory location is part of a memory space associated with a first memory device, said

second memory location is part of a memory space associated with a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

And said first and second memory devices comprise at least a portion of a memory store. Figure 3 shows that the address space is mapped to the memory devices.

Claim 31 is taught by Falik as:

The computer readable medium of claim 29, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of a first memory device and a block size value of a second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 32 is taught by Falik as:

The computer readable medium of claim 30, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 33 is taught by Falik as:

The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 34 is taught by Falik as:

The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

Claim 35 is taught by Falik as:

The computer readable medium of claim 29, wherein said addressing further includes: said first and second device profiles having at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 36 is taught by Falik as:

The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 37 is taught by Falik as:

The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 38 is taught by Falik as:

The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 39 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 40 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 41 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 42 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 43 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 44 is taught by Falik as:

The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

9. **Claims 61 and 64-68** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Chin et al. (US 2001/0010066).

Claim 61 is taught by Falik as shown supra with respect to claim 59.

Falik further teaches:

The memory controller of claim 59, wherein said interface controller includes: A first memory bus controller coupled to said control device and said memory device interface. Falik figure 4b item 116.

And an IO bus controller coupled to said IO device interface and said control device. Falik figure 4b item 117.

With respect to claim 61, Chin figure 2 teaches a bridge unit 104, which connects to a CPU bus 108 and a memory bus 110, including control logic 242, shown in paragraph 0037 to direct the operations of the queue storage elements through a network of control signals. Figure 2 also illustrates a data path between the CPU bus 108 and memory bus 110 through queues 250 and 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a main control device coupled to the memory device interface and data path as taught by Chin in the interface controller of Falik.

The motivation for doing so would have been to provide a means to manage the transfer of data through the interface performed by the system of Falik, see Chin paragraph 0037.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as specified in **claim 61**.

Claim 64 is taught by Falik as shown supra with respect to claim 59.

Falik does not expressly teach that a buffer is a FIFO or that a data path includes a plurality of queue slots.

With respect to claim 64, Chin teaches:

Further including a buffer comprising a FIFO. Paragraph 0052 shows that queue 250 is a FIFO.

And a data path that includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory. Figure 2 also shows read queue 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a FIFO and a data path including a plurality of queue slots in the system of Falik.

The motivation for doing so would have been to provide an interface that provides all devices in a computer system fair access to memory, Chin paragraph 0012.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as recited in **claim 64**.

Claim 65 is taught by Falik as shown supra with respect to claim 59.

Falik does not expressly teach that a data path includes a buffer having a plurality of queue slots.

With respect to claim 65, Chin teaches:

The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a FIFO and a data path including a plurality of queue slots in the system of Falik.

The motivation for doing so would have been to provide an interface that provides all devices in a computer system fair access to memory, Chin paragraph 0012.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as recited in **claims 65-67**.

Claim 66 is taught by Chin as:

The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a plurality of queue slots that buffer data from said IO device interface to said memory device interface. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory.

Claim 67 is taught by Chin as:

The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from

said memory device interface to said IO device interface. Figure 2 also shows read queue 252.

Claim 68 is taught by Falik as shown supra with respect to claim 1.

Falik further teaches a memory bus controller, figure 4b item 116, coupled to bus 90.

Falik does not expressly teach that the memory bus controller is coupled to a main control device.

With respect to claim 68, Chin teaches:

A second memory bus controller coupled to said main control device and said memory device interface. Figure 2 teaches a bridge unit 104, which connects to a CPU bus 108 and a memory bus 110, including control logic 242, shown in paragraph 0037 to direct the operations of the queue storage elements through a network of control signals. Figure 2 also illustrates a data path between the CPU bus 108 and memory bus 110 through queues 250 and 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a main control device coupled to the memory device interface and data path as taught by Chin in the interface controller of Falik.

The motivation for doing so would have been to provide a means to manage the transfer of data through the interface performed by the system of Falik, see Chin paragraph 0037.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as specified in **claim 68**.

10. **Claims 62 and 63** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Chin et al. (US 2001/0010066) as applied to claim 61 above, and further in view of Tsuruta (US 2007/0174506).

Claim 62 is taught by the combination of Falik and Chin as shown supra with respect to claim 61.

The combination of Falik and Chin does not expressly teach that the IO bus controller is disposed to respond to said memory transaction request by acknowledging said request and providing status to said main control device.

With respect to claim 62, Tsuruta teaches:

Wherein said IO bus controller is disposed to respond to a memory transaction request by acknowledging said request and providing status to said main control device. Paragraph 0183 shows that in response to a read req from the CPU, MEM-DMAC 232 issues a read ack signal. Paragraph 0186 shows that after the read operation is performed, a sequencer in the memory controller 231 issues ack to a sequencer in the MEM-DMAC 232.

At the time of the invention, it would have been obvious to use the acknowledgement system of Tsuruta in the combination of Falik and Chin.

The motivation for doing so would have been to provide coordination between the CPU interface and the read/write queues to perform the requested memory operations.

Therefore, it would have been obvious to combine Tsuruta with Falik and Chin to obtain the invention as specified in **claims 62 and 63**.

Claim 63 is taught by Chin as:

The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction. Paragraph 0052 shows that control logic provides control signals to the input and output selectors 351 and 353 that determine the values of the enable and select signals in response to a memory request from the CPU.

Coordinates the operation of said memory device interface. Paragraph 0052 shows that the data and address of each request is sent to the memory controller 200.

And manages the transfer of memory transaction data between said IO device interface and said memory device interface through a data path. Paragraph 0052 shows that data is transferred through the queue 250.

Response to Arguments

2. Applicant's arguments, see the first paragraph beginning on page 24 of the remarks filed 3/26/2013, with respect to the double patenting objection to claims 31 and

32 have been fully considered and are persuasive. The double patenting objection to claims 31 and 32 has been withdrawn.

3. Applicant's arguments, see the second paragraph beginning on page 24 of the remarks filed 3/26/2013, with respect to the objection to claim 68 have been fully considered and are persuasive. The objection to claim 68 has been withdrawn.

4. Applicant's arguments, see the third paragraph beginning on page 24 of the remarks filed 3/26/2013, with respect to the rejection of claims 29-44 under 35 USC 101 have been fully considered and are persuasive. The rejection of claims 29-44 under 35 USC 101 has been withdrawn.

5. Applicant's arguments, see the fourth paragraph beginning on page 24 of the remarks filed 3/26/2013, with respect to the rejection of claims 45-58 under 35 USC 112 second paragraph have been fully considered and are persuasive. The rejection of claims 45-58 under 35 USC 112 second paragraph has been withdrawn.

6. In the fourth paragraph beginning on page 25 and continuing in the first paragraph beginning on page 26, with respect to the teachings of Falik, Applicant argues:

> "Falik discloses the device and status control register (Falik: Figure 5A) which provides status and control information for an entire memory device (Falik: column 19, lines 4-8). Falik also discloses a flash device capabilities register (Falik: Figure 5B), that provides capabilities and properties information on the same entire memory device (Falik: column 19, lines 49-53). Therefore, these registers contain information directed to the same entire memory device and not

directed to different memory locations. These registers do not contain a first set of attributes of a first memory location and also do not contain a second set of attributes of a second memory location.

Falik also discloses section properties registers that provide information on structural properties of sections of a flash device (Falik: column 20, lines 49-55). However, Falik discloses these sections as logical sections which are not memory locations (Falik: column 14, lines 51-60 and column 20, lines 49-56). These registers do not contain a first set of attributes of a first memory location and also do not contain a second set of attributes of a second memory location."

7. The Examiner respectfully disagrees. As noted at column 19 lines 49-55, the flash device capabilities register stores information on the capabilities and properties of the flash device. As noted at column 6 lines 11-19, the flash device may have multiple arrays, each having different parameters. As shown at column 14 lines 40-65, the arrays having identical structure are logically grouped into sections, and that the address space of each logical block is divided into a plurality of sections that correspond to the logical groups. As the sections are included in the address map, each section includes a plurality of addressable memory locations. Column 15 lines 63-67 shows that characteristics of each section 57, in the information block and its assignment to a sub-block, are stored in a corresponding Section Capabilities Register. As noted at column 20 lines 49-56, there is a section properties register that stores structural properties of each of the sections of the device. Column 20 lines 60-67 shows that the section properties register includes PageSizeBlock1 which indicates the size of the

minimum segment of the array which may be erased with a single erase command, which is specifically mentioned in the specification of the instant application at paragraph 0015 as an example of an attribute of a memory region.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JARED RUTZ whose telephone number is (571)272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Christian Chace can be reached on (571)272-4190. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jared I Rutz
Primary Examiner
Art Unit 2187

/Jared I Rutz/
Primary Examiner, Art Unit 2187

REMARKS/ARGUMENTS

Claim Rejections

35 USC 102

Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-97

Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-97 are rejected under 35 U.S.C. 102(e) as allegedly being anticipated by US 8,200,879 to Falik et al. ("Falik"). Claims 1, 45, 59, and 80 are independent claims. Applicants respectfully traverse this rejection.

Applicants respectfully disagree with this rejection, but to expedite allowance of the claims, Applicants amend independent claim 1 herein to recite: addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile, wherein a memory read transaction or a memory write transaction is performed on at least one of the first memory location or second memory location, wherein data is transferred to the first memory location or second memory location for a memory write transaction, wherein data is transferred from the first memory location or second memory location for a memory read transaction. Support for the amendment in claim 1 is found in the filed application in, for example, Figures 1 and 2 and accompanying text, and paragraphs [0029], [0030], and [0031]. In contrast, Falik does not disclose associating any device profiles with a memory location used for a memory read or memory write transaction.

Applicants further respectfully contend that independent claim 1 recites the following limitations that are not disclosed within the four corners of Falik: addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile; said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and using attributes from said first and second device profiles. In contrast, Falik discloses characteristics of each logical section 57 (Falik: column 15, line 63), and these logical sections contain logical blocks (and these logical blocks are Main Block 51 and Information Block 52) (Falik: column 14, line 51-56). Therefore, Falik discloses logical sections as associated with these characteristics. However, these logical blocks in these logical sections are for storing data used by any application in a Main Device, or for storing auxiliary data (e.g., configuration data or control data) used by the Main Device or application programs (Falik: column 14, lines 21-31 and lines 51-58). Therefore, these logical blocks (and logical sections that contain these logical blocks) are not addressable sections used for a memory read or memory write transaction. Therefore, Falik does not disclose these logical sections as memory locations that are addressed. Accordingly, Falik does not disclose all the limitations of claim 1.

Falik further discloses the device and status control register (Falik: Figure 5A) which provides status and control information for an entire memory device (Falik: column 19, lines 4-8). Falik also discloses a flash device capabilities register (Falik: Figure 5B) that provides capabilities and properties information on the same entire memory device (Falik: column 19, lines 49-53). Therefore, these registers contain information directed to the same entire memory device and not directed to different memory locations. These registers do not contain a first set of attributes of a first memory location and also do not contain a second set of attributes of a second memory location.

Based on at least the above discussion, Falik does not disclose and does not teach "addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile" and "said first memory location and a second memory location respectively associated with a first device profile and a second device profile; said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles" as required in claim 1.

Since Falik does not disclose and does not teach all the limitations of claim 1, claim 1 is not anticipated by the cited reference. Claim 1 is otherwise allowable.

Claims 2-14, 20, 21, and 25 depend from allowable claim 1; as such, they are also allowable for at least the same reasons as claim 1.

The withdrawal of the rejections to claims 1-14, 20, 21, 25 and 94 is respectfully requested.

Independent claims 45, 59, and 80 recite at least some limitations similar to that as claim 1. Although claims 45, 59, and 80 are different, Applicants respectfully argue that in this case the above arguments regarding the patentability of claim 1 apply with equal force with respect to claims 45, 59, and 80. Since Falik does not disclose and does not teach all the limitations of claims 45, 59, and 80, claims 45, 59, and 80 are not anticipated by the cited reference. Claims 45, 59, and 80 are otherwise allowable.

Claims 46-58 and 95 depend from allowable claim 45; as such, they are also allowable for at least the same reasons as claim 45.

Claims 60, 69-79, and 96 depend from allowable claim 59; as such, they are also allowable for at least the same reasons as claim 59.

Claims 81-92 and 97 depend from allowable claim 80; as such, they are also allowable for at least the same reasons as claim 80.

The withdrawal of the rejection to claims 45-60, 69-92, and 95-97 is respectfully requested.

Claims 15, 18, and 19

Claims 15, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 7,330,954 to Nangle.

Claims 15, 18, and 19 depend from allowable claim 1; as such, they are also allowable for at least the same reasons a claim 1.

The withdrawal of the rejection of claims 15, 18, and 19 is respectfully requested.

Claims 16, 17, 22-24, and 93

Claims 16, 17, 22-24, and 93 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 2006/0184723 to Sinclair.

Claims 16, 17, and 22-24 depend from allowable claim 1; as such, they are also allowable for at least the same reasons a claim 1.

Claim 93 depends from allowable claim 80; as such, claim 93 is also allowable for at least the same reasons a claim 1.

The withdrawal of the rejection of claims 16, 17, 22-24, and 93 is respectfully requested.

Claims 26-28

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 6961,805 to Lakhani et al.

Claims 26-28 depend from allowable claim 1; as such, they are also allowable for at least the same reasons a claim 1.

The withdrawal of the rejection of claims 26-28 is respectfully requested.

Claims 29-44

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 5,913,215 to Rubinstein.

The Office admits that Falik does not expressly teach that the methods may be implemented using a computer readable medium comprising computer executable instructions. In order to supply the missing limitations, the Office combines Falik with Rubinstein. The Office argues it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a computer readable medium comprising computer executable instructions (Office Action: page 44). The Applicants respectfully disagree with the assertions of the Office.

Independent claim 29 recite at least some limitations similar to that as claim 1. Although claim 29 is different, Applicants respectfully argue that in this case the above arguments regarding the patentability of claim 1 apply with equal force with respect to claim 29.

Since Falik and Rubinstein, considered individually or in combination, do not disclose and does not teach all the limitations of claim 29, claim 29 is not rendered obvious in view the cited references. Claim 29 is otherwise allowable.

Since 14 October 2013 falls on a Federal Holiday, this Response is timely filed on 15 October 2013.

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, the Applicants are not conceding in this application that previously pending claims are not patentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application.

Claims 30-44 depend from allowable claim 29; as such, they are also allowable for at least the same reasons a claim 29.

The withdrawal of the rejection of claims 29-44 is respectfully requested.

Claims 61 and 64-68

Claims 61 and 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 2001/0010066 to Chin et al.

Claims 61 and 64-68 depend from allowable claim 59; as such, they are also allowable for at least the same reasons a claim 59.

The withdrawal of the rejection of claims 61 and 64-68 is respectfully requested.

Claims 62 and 63

Claims 61 and 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of Chin as applied to claim 61 above, and further in view of US 2007/0174506 to Tsuruta.

Claims 62 and 63 depend from allowable claim 59; as such, they are also allowable for at least the same reasons a claim 59.

The withdrawal of the rejection of claims 62 and 63 is respectfully requested.

Applicants respectfully request the allowance of the claims. Applicant respectfully requests and petitions for a two-months extension of time to file this response.

Conclusion

Claims 1-97 herein are allowable, and a timely Notice of Allowance is respectfully requested.

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (408) 256-0244.

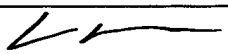
Date: October 15, 2013

Respectfully submitted,



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Typed or Printed Name:	Arnold de Guzman	Dated:	Oct. 15, 2013
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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising:

addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile, wherein a memory read transaction or a memory write transaction is performed on at least one of the first memory location or second memory location, wherein data is transferred to the first memory location or second memory location for a memory write transaction, wherein data is transferred from the first memory location or second memory location for a memory read transaction;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

using attributes from said first and second device profiles.

2. (original) The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device.

3. (original) The method of claim 1, wherein said difference between said first and second device profiles includes different attributes; and said addressing said first memory location is made in response to a first memory transaction request; and

further including addressing said second memory location.

4. (original) The method of claim 1, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes.

5. (original) The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

6. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute values.

7. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute types.

8. (original) The method of claim 5, wherein said shared attributes include a memory device type attribute.

9. (original) The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

10. (original) The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

11. (original) The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

12. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

13. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of attributes that differs in value from a second page size attribute from said second set of attributes.

14. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes.

15. (original) The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device, and said second memory device interface attribute corresponds to a DRAM device interface.

16. (original) The method of claim 2, wherein said using attributes from said first and second device profile further includes using a first partial page size attribute from said first set of attributes that differs in value from a second partial page size attribute from said second set of attributes.

17. (original) The method of claim 16:

said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute; and

further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute.

18. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

19. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a NAND flash memory device and said second memory device type attribute corresponds to a NOR flash memory device.

20. (original) The method of claim 2, further including:

using an address corresponding to a memory location from said first memory device and transferring a first data set, and

using an address corresponding to a memory location from said second memory device and transferring a second data set.

21. (original) The method of claim 20, wherein:

said first set of attributes includes a first page size attribute, and said first data set includes a first data set size; and

if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size.

22. (original) The method of claim 20, wherein:

said second set of attributes includes a second page size attribute, and said second data set includes a second data set size; and

if said second data set size is greater than said second page size attribute, said transferring said second data set includes:

performing a set of write operations on said second memory device that includes using a second transfer size equal to said second page size attribute until a remaining portion of said second data set that has not yet been written to said second device is less than said second page size attribute, and

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

23. (currently amended) The method of claim 20, wherein:

said first set of attributes includes a page size attribute and a block size attribute;

said first data set includes a first data set size;

if said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes:

performing a set of write operations on said first memory device that includes using a second transfer size equal to said page size attribute until a remaining portion of said first data set that has not yet been written to said first device is less than said page size attribute,

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size[[;]].

24. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes:

performing respective write operations on said first and second memory devices by at least using a transfer size at least equal to a partial page size attribute from said first set of attributes and performing at least one write operation on said second memory device by at least using a transfer size at least equal to a partial page size attribute value from said second set of attributes; and

said attribute difference includes different attribute values of said first and second partial page size attributes.

25. (original) The method of claim 1, wherein said using attributes from said first and second device profile

further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size attribute of said first memory device.

26. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a block size attribute value that corresponds to a block size attribute of said first memory device.

27. (original) The method of claim 26, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

28. (original) The method of claim 2, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

29. (previously presented) A non-transitory computer readable medium comprising computer executable instructions adapted to cause a method of performing memory transactions on a first memory location and a second memory location, said method comprising:

addressing a first memory location, said first memory location and a second memory location are respectively

associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory device, and said second device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles; and

using attributes from said first and second device profiles.

30. (original) The computer readable medium of claim 29, wherein:

said first memory location is part of a memory space associated with a first memory device;

said second memory location is part of a memory space associated with a second memory device; and

said first and second memory devices comprise at least a portion of a memory store.

31. (previously presented) The computer readable medium of claim 29, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of a first memory device and a block size value of a second memory device.

32. (previously presented) The computer readable medium of claim 30, wherein at least one attribute of said

attributes includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

33. (original) The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

34. (original) The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes.

35. (previously presented) The computer readable medium of claim 29, wherein said addressing further includes:

said first and second device profiles having at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

36. (original) The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

37. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values.

38. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types.

39. (original) The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute.

40. (original) The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

41. (original) The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

42. (original) The computer readable medium of claim 36, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

43. (original) The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes.

44. (original) The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device.

45. (previously presented) A memory controller for performing memory transactions, said memory controller comprising:

a means for addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile;

wherein said means for addressing includes an interface controller means for processing memory transaction requests;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said means for addressing uses attributes from said first and second device profiles.

46. (original) The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

47. (original) The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

48. (original) The memory controller of claim 46, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said use of said attributes from said first and second device profiles by said means for addressing includes using said different attribute qualifiers for said shared attributes.

49. (original) The memory controller of claim 46, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

50. (previously presented) The memory controller of claim 45, wherein said means for addressing further includes a means for addressing said second memory location.

51. (original) The memory controller of claim 45, wherein said difference includes different attribute qualifiers for

at least one set of shared attributes from said first and second device profiles.

52. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values.

53. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types.

54. (original) The memory controller of claim 51, wherein said shared attributes include a memory device type attribute.

55. (original) The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

56. (original) The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

57. (original) The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

58. (original) The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device.

59. (original) A memory controller comprising:

an interface controller coupled to a memory device interface and an IO device interface;

said interface controller disposed to perform a memory transaction by addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile;

said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said addressing of said first memory location includes using said attributes from said first device profile.

60. (original) The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile.

61. (previously presented) The memory controller of claim 59, wherein said interface controller includes:

a main control device coupled to said memory device interface and to a data path;

a first memory bus controller coupled to said control device and said memory device interface; and

an IO bus controller coupled to said IO device interface and said control device.

62. (previously presented) The memory controller of claim 61, wherein said IO bus controller is disposed to respond to a memory transaction request by acknowledging said request and providing status to said main control device.

63. (original) The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction, coordinates the operation of said memory device interface, and manages the transfer of memory transaction data between said IO device interface and said memory device interface through a data path.

64. (previously presented) The memory controller of claim 59, further including a buffer comprising a FIFO and a data path that includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface.

65. (original) The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots.

66. (original) The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a plurality of queue slots that buffer data from said IO device interface to said memory device interface.

67. (original) The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from said memory device interface to said IO device interface.

68. (previously presented) The memory controller of claim 59, further including a second memory bus controller coupled to a main control device and said memory device interface.

69. (original) The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes.

70. (original) The memory controller of claim 59, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

71. (original) The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

72. (original) The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute.

73. (original) The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values.

74. (original) The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values.

75. (original) The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type.

76. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values.

77. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types.

78. (original) The memory controller of claim 71, wherein said shared attributes include a block size attribute, and

said different attribute qualifiers include different block size values.

79. (original) The memory controller of claim 71, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

80. (original) An electronic storage device, comprising:

a memory controller disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said memory controller using attributes from said first and second device profiles.

81. (original) The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

82. (original) The electronic storage device of claim 80, wherein said first memory location is located in a first

memory device and said second memory location is located in a second memory device.

83. (previously presented) The electronic storage device of claim 80, said memory controller further disposed to:

perform a write operation on said first memory device, if a memory transaction request is associated with a write request;

perform a read operation on said first memory device, if said memory transaction request is associated with a read request; and

wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using said second device profile in response to receiving a second memory transaction request.

84. (original) The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

85. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values.

86. (original) The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute.

87. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types.

88. (original) The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said shared attributes.

89. (original) The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device.

90. (original) The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

91. (original) The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

92. (original) The electronic storage device of claim 84, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

93. (original) The electronic storage device of claim 80, wherein said memory controller is further adapted to:

use a first partial page size attribute by performing a write operation on said first memory device and using a

transfer size at least equal to said partial page size attribute; and

use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute.

94. (previously presented) The method of claim 1, wherein the first memory location and the second memory location are addressable memory locations.

95. (previously presented) The memory controller of claim 45, wherein the first memory location and the second memory location are addressable memory locations.

96. (previously presented) The memory controller of claim 59, wherein the first memory location and the second memory location are addressable memory locations.

97. (previously presented) The electronic device of claim 80, wherein the first memory location and the second memory location are addressable memory locations.

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EXAMINER	
RUTZ, JARED IAN	
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NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 12/876,113	Applicant(s) BRUCE ET AL.	
	Examiner JARED RUTZ	Art Unit 2187	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/5/2014*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-97* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-97* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *2/5/2014*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

KIOXIA Ex-1002, Page 193

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

2. Claims 1-97, as amended on 10/21/2013, are pending in the instant application. Applicant's arguments submitted 10/21/2013 have been carefully and fully considered, but are not found persuasive. The instant Office action is made **FINAL**.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/21/2013 has been entered.

4. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Information Disclosure Statement

5. The information disclosure statement (IDS) submitted on 2/5/2014 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. **Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-97** are rejected under 35 U.S.C. 102(e) as being anticipated by Falik et al. (US 8,200,879).

Claim 1 is taught by Falik as:

A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising: addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Wherein a memory read transaction or a memory write transaction is performed on at least one of the first memory location or second memory location, wherein data is transferred to the first memory location of second memory location for a memory write transaction, wherein data is transferred from the first memory location or second memory location for a memory read transaction. Column 22 lines 16-20 shows that reading of data from memory and

modifying contents of the memory (i.e. erasing and programming) are carried out as transactions, initiated by appropriate commands and affected by the contents of the specified registers. Column 16 line 53 through column 17 line 24 further discusses the use of addresses to read and write data from the memory. Column 6 is an illustration of reads and writes to different addresses in different sections of the memory.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 2 is taught by Falik as:

The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 3 is taught by Falik as:

The method of claim 1, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

And said addressing said first memory location is made in response to a first memory transaction request. Column 18 lines 24-34 shows that applications on the main die 100 issue read and program commands.

And further including addressing said second memory location. Figure 6 shows that both sections can be addressed.

Claim 4 is taught by Falik as:

The method of claim 1, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 5 is taught by Falik as:

The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 6 is taught by Falik as:

The method of claim 5, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 7 is taught by Falik as:

The method of claim 5, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 8 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a memory device type attribute. Column 20 lines 30-36 shows that the registers can indicate if the device is self timed type flash memory or not.

Claim 9 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 10 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 11 is taught by Falik as:

The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size,

memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 12 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 13 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of attributes that differs in value from a second page size attribute from said second set of attributes. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 14 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 20 is taught by Falik as:

The method of claim 2, further including: using an address corresponding to a memory location from said first memory device and transferring a first data set. Column 16 lines 53-62 shows that an address and data are sent for a programming operation.

And using an address corresponding to a memory location from said second memory device and transferring a second data set. Column 14 lines 51-65 show that the standard address space is mapped to the logical sections into which the arrays are grouped, showing that the second memory device is accessed using an address corresponding to the second memory device.

Claim 21 is taught by Falik as:

The method of claim 20, wherein: said first set of attributes includes a first page size attribute. Column 20 lines 62-65 shows that the minimum

programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

And said first data set includes a first data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

And if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size. Column 27 lines 9-24 shows that when the number of bytes to be transferred to the FD have been transferred, the transfer process ends by setting the bus to a HiZ state.

Claim 25 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size attribute of said first memory device. As discussed at column 27 lines 33-60, the program buffer corresponds to the batch size, which is the amount of data which can be programmed into the flash array at once.

Claim 45 is taught by Falik as:

A memory controller for performing memory transactions, said memory controller comprising: a means for addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Wherein said means for addressing includes an interface controller means for processing memory transaction requests. Figure 4B, flash bus transactions state machine 116.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And said means for addressing uses attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 46 is taught by Falik as:

The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 47 is taught by Falik as:

The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 48 is taught by Falik as:

The memory controller of claim 46, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows

that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said use of said attributes from said first and second device profiles by said means for addressing includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 49 is taught by Falik as:

The memory controller of claim 46, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 50 is taught by Falik as:

The memory controller of claim 45, wherein said means for addressing further includes a means for addressing said second memory location. Figure 6 shows that both sections can be addressed.

Claim 51 is taught by Falik as:

The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 52 is taught by Falik as:

The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 53 is taught by Falik as:

The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 54 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6

shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 55 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 56 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 57 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size,

block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 58 is taught by Falik as:

The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

Claim 59 is taught by Falik as:

A memory controller comprising: an interface controller coupled to a memory device interface and an IO device interface. Figure 4B shows interface controller 110 connected to bus 90 and internal bus 140.

Said interface controller disposed to perform a memory transaction by addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column

16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And said addressing of said first memory location includes using said attributes from said first device profile. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 60 is taught by Falik as:

The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile. Figure 6 shows that both sections can be addressed.

Claim 69 is taught by Falik as:

The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-

48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

Claim 70 is taught by Falik as:

The memory controller of claim 59, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 71 is taught by Falik as:

The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 72 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 73 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 74 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 75 is taught by Falik as:

The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 76 is taught by Falik as:

The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 77 is taught by Falik as:

The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 78 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block

size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 79 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 80 is taught by Falik as:

An electronic storage device, comprising: a memory controller disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the

standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And said memory controller using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 81 is taught by Falik as:

The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command. Column 9 lines 5-18 shows that the interface performs appropriate requests for erasure.

Claim 82 is taught by Falik as:

The electronic storage device of claim 80, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 83 is taught by Falik as:

The electronic storage device of claim 80, said memory controller further disposed to: perform a write operation on said first memory device, if a memory transaction request is associated with a write request. Column 16 lines 53-64 shows that write transactions may be performed.

Perform a read operation on said first memory device, if said memory transaction request is associated with a read request. Column 16 lines 53-64 shows that read transactions may be performed.

And wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using said second device profile in response to receiving a second memory transaction request. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used for accesses to the groups of memory arrays.

Claim 84 is taught by Falik as:

The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 85 is taught by Falik as:

The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 86 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 87 is taught by Falik as:

The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20

line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 88 is taught by Falik as:

The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 89 is taught by Falik as:

The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

Claim 90 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 91 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 92 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 94 is taught by Falik as:

The method of claim 1, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 95 is taught by Falik as:

The memory controller of claim 45, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 96 is taught by Falik as:

The memory controller of claim 59, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 97 is taught by Falik as:

The electronic device of claim 80, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which

may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claims 15, 18, and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Nangle (US 7,330,954).

Claim 15 is taught by Falik as:

The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device. Column 21 lines 7-10 shows that the information can correspond to a flash device FD.

Although Falik column 21 lines 7-10 shows that other memory technologies such as SRAM may be used, it does not expressly teach that the second memory device attribute corresponds to a DRAM device interface.

With respect to claim 15, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 lines 51-67 shows that the memory devices may be flash memory and DRAM.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include flash memory and DRAM in the system of Falik.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 15**.

Claim 18 is taught by Falik as shown supra with respect to claim 8.

Falik does not expressly teach that said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

With respect to claim 18, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 line 51 through column 5 line 4 shows that the memory devices may be volatile memory that have a battery backup.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a volatile memory disposed to receive backup power from a portable power source.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 18**.

Claim 19 is taught by Falik as shown supra with respect to claim 8.

Falik does not expressly teach that said first memory device type attribute corresponds to a NAND flash memory device and said second memory device type attribute corresponds to a NOR flash memory device.

With respect to claim 19, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 lines 51-65 shows that the memory devices may be NAND or NOR type flash memories.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a volatile memory disposed to receive backup power from a portable power source.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 19**.

10. **Claims 16, 17, 22-24, and 93** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Sinclair et al. (US 2006/0184723).

Claim 16 if taught by Falik as shown supra with respect to claim 2.

Although Falik teaches that the width of the array is the minimum programming size of the array at column 20 lines 62-65, and that the width of the array is stored at column 20 lines 49-52, Falik does not expressly teach that a first and second partial page size attribute is stored and used.

With respect to claim 16, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claims 16 and 17**.

Claim 17 is taught by Falik and Sinclair as:

The method of claim 16: said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute. Sinclair paragraph 0168 shows that in a flash memory that supports partial page programming, when sufficient data is transferred to the buffer, it is programmed to the page. Falik column 14 lines 51-60 and figure 3 shows that the first memory device group can be accessed.

And further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute. Sinclair paragraph 0168 shows that in a flash memory that supports partial page programming, when sufficient data is transferred to the buffer, it is programmed to the page. Falik column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

Claim 22 is taught by Falik as:

The method of claim 20, wherein: said second set of attributes includes a second page size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

And said second data set includes a second data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

And if said second data set size is greater than said second page size attribute, said transferring said second data set includes: performing a set of write operations on said second memory device that includes using a second transfer size equal to said second page size attribute. Column 16 lines 48-52 shows that program buffer 19 may be a double buffer, allowing the programming of one chunk of data while another chunk of data is received. As discussed at column 27 lines 33-60, the program buffer corresponds to the batch size, which is the amount of data which can be programmed into the flash array at once.

Falik does not expressly teach that the transaction is made using a transfer size equal to the page size until a remaining portion of said second data set that has not yet been written to said second device is less than said second page size attribute and using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

With respect to claim 22, Sinclair teaches Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times. As discussed in paragraph 0168, when the end of the data group is received in the buffer and it is smaller than a full page of data, a partial page programming operation may be performed.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 22**.

Claim 23 is taught by Falik as:

The method of claim 20, wherein: said first set of attributes includes a page size attribute and a block size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Said first data set includes a first data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

If said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes: performing a set of write

operations on said first memory device that includes using a second transfer size equal to said page size attribute [...]. Column 27 lines 14-24 shows that bytes of data are sent until all the bytes have been sent.

Falik does not expressly teach that the transaction is made using a transfer size equal to the page size until a remaining portion of said first data set that has not yet been written to said first device is less than said first page size attribute and using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

With respect to claim 23, Sinclair teaches Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times. As discussed in paragraph 0168, when the end of the data group is received in the buffer and it is smaller than a full page of data, a partial page programming operation may be performed.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 23**.

Claim 24 is taught by Falik as shown supra with respect to claim 1, and further as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes: performing respective write operations on said first and second memory devices by at least using a transfer size at least equal to a […] *page size attribute from said first set of attributes*. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations.

And performing at least one write operation on said second memory device by at least using a transfer size at least equal to a […] *page size attribute value from said second set of attributes*. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations. Column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

And said attribute difference includes different attribute values of said first and second […] *page size attributes*. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Although Falik teaches storing a page size attribute, it does not expressly teach storing a partial page size attribute.

With respect to claim 24, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 24**.

Claim 93 is taught by Falik as shown supra with respect to claim 80, and further as:

The electronic storage device of claim 80, wherein said memory controller is further adapted to: use a first partial page size attribute by performing a write operation on said first memory device and using a transfer size at least equal to said partial page size attribute. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations.

And use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing

address locations. Column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

Although Falik teaches storing a page size attribute, it does not expressly teach storing a partial page size attribute.

With respect to claim 93, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 93**.

11. **Claims 26-28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Lakhani et al. (US 6,961,805).

Claim 26 is taught by Falik as shown supra with respect to claim 1.

Falik further teaches, at column 20 lines 60-65, that Page Size Block1 stores the size of the minimal segment of a flash array erasable upon a single erase command.

Additionally, column 16 line 53 through column 17 line 24 shows that data can be written to a block of addresses by designating the starting address and performing a series of program continue operations.

Falik does not expressly teach using the block size attribute in performing a write operation that uses a transfer size that corresponds to the block size.

With respect to claim 26, Lakhani teaches, at column 18 lines 19-46, that predecoder 50 asserts sets of multiblock selection bits in response to control bits from the controller, which allows a designated number of blocks to be selected for writing at the same time.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to perform a write operation that uses a transfer size equal to the a block size attribute value that corresponds to a block size attribute of the first memory device.

The motivation for doing so would have been to reduce the time used to test the memory cells of the block, Lakhani column 8 lines 21-32.

Therefore, it would have been obvious to combine Lakhani with Falik to obtain the invention as specified in **claims 26 and 27**.

Claim 27 is taught by Lakhani as:

> *The method of claim 26, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a*

transfer size equal to a multiple of said block size attribute value. Column 13 lines 25-38 shows that a plurality of blocks can be selected at the same time.

Claim 28 is taught by Falik as shown supra with respect to claim 2.

Falik further teaches, at column 20 lines 60-65, that Page Size Block1 stores the size of the minimal segment of a flash array erasable upon a single erase command. Additionally, column 16 line 53 through column 17 line 24 shows that data can be written to a block of addresses by designating the starting address and performing a series of program continue operations.

Falik does not expressly teach using the block size attribute in performing a write operation that uses a transfer size that is equal to a multiple of the block size.

With respect to claim 28, Lakhani teaches, at column 18 lines 19-46, that predecoder 50 asserts sets of multiblock selection bits in response to control bits from the controller, which allows a designated number of blocks to be selected for writing at the same time.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to perform a write operation that uses a transfer size equal to the a block size attribute value that corresponds to a block size attribute of the first memory device.

The motivation for doing so would have been to reduce the time used to test the memory cells of the block, Lakhani column 8 lines 21-32.

Therefore, it would have been obvious to combine Lakhani with Falik to obtain the invention as specified in **claim 28**.

12. **Claims 29-44** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Rubinstein et al. (US 5,913,215).

Claim 29 is taught by Falik as:

Said method comprising: addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said first device profile representing a first set of attributes of said first memory device, and said second device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14

lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Falik does not expressly teach that the methods may be implemented using a non-transitory computer readable medium comprising computer executable instructions.

With respect to claim 29, Rubinstein teaches at column 10, lines 3-15, that computer methods may be performed either by a series of instructions, or by specific hardware components that contain hard-wired logic for performing the method, or by any combination of the two.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a computer readable medium comprising computer executable instructions.

The rationale for doing so would have been that it is a known technique to implement methods in computer systems using a non-transitory computer readable medium comprising computer executable instructions.

Therefore, it would have been obvious to combine Rubinstein with Falik to obtain the invention as recited in **claims 29-44**.

Claim 30 is taught by Falik as:

The computer readable medium of claim 29, wherein: said first memory location is part of a memory space associated with a first memory device, said

second memory location is part of a memory space associated with a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

And said first and second memory devices comprise at least a portion of a memory store. Figure 3 shows that the address space is mapped to the memory devices.

Claim 31 is taught by Falik as:

The computer readable medium of claim 29, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of a first memory device and a block size value of a second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 32 is taught by Falik as:

The computer readable medium of claim 30, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 33 is taught by Falik as:

The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 34 is taught by Falik as:

The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

Claim 35 is taught by Falik as:

The computer readable medium of claim 29, wherein said addressing further includes: said first and second device profiles having at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 36 is taught by Falik as:

The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 37 is taught by Falik as:

The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 38 is taught by Falik as:

The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 39 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 40 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 41 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 42 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 43 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 44 is taught by Falik as:

The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

13. **Claims 61 and 64-68** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Chin et al. (US 2001/0010066).

Claim 61 is taught by Falik as shown supra with respect to claim 59.

Falik further teaches:

The memory controller of claim 59, wherein said interface controller includes: A first memory bus controller coupled to said control device and said memory device interface. Falik figure 4b item 116.

And an IO bus controller coupled to said IO device interface and said control device. Falik figure 4b item 117.

With respect to claim 61, Chin figure 2 teaches a bridge unit 104, which connects to a CPU bus 108 and a memory bus 110, including control logic 242, shown in paragraph 0037 to direct the operations of the queue storage elements through a network of control signals. Figure 2 also illustrates a data path between the CPU bus 108 and memory bus 110 through queues 250 and 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a main control device coupled to the memory device interface and data path as taught by Chin in the interface controller of Falik.

The motivation for doing so would have been to provide a means to manage the transfer of data through the interface performed by the system of Falik, see Chin paragraph 0037.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as specified in **claim 61**.

Claim 64 is taught by Falik as shown supra with respect to claim 59.

Falik does not expressly teach that a buffer is a FIFO or that a data path includes a plurality of queue slots.

With respect to claim 64, Chin teaches:

Further including a buffer comprising a FIFO. Paragraph 0052 shows that queue 250 is a FIFO.

And a data path that includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory. Figure 2 also shows read queue 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a FIFO and a data path including a plurality of queue slots in the system of Falik.

The motivation for doing so would have been to provide an interface that provides all devices in a computer system fair access to memory, Chin paragraph 0012.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as recited in **claim 64**.

Claim 65 is taught by Falik as shown supra with respect to claim 59.

Falik does not expressly teach that a data path includes a buffer having a plurality of queue slots.

With respect to claim 65, Chin teaches:

The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a FIFO and a data path including a plurality of queue slots in the system of Falik.

The motivation for doing so would have been to provide an interface that provides all devices in a computer system fair access to memory, Chin paragraph 0012.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as recited in **claims 65-67**.

Claim 66 is taught by Chin as:

The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a plurality of queue slots that buffer data from said IO device interface to said memory device interface. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory.

Claim 67 is taught by Chin as:

The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from

said memory device interface to said IO device interface. Figure 2 also shows read queue 252.

Claim 68 is taught by Falik as shown supra with respect to claim 1.

Falik further teaches a memory bus controller, figure 4b item 116, coupled to bus 90.

Falik does not expressly teach that the memory bus controller is coupled to a main control device.

With respect to claim 68, Chin teaches:

A second memory bus controller coupled to said main control device and said memory device interface. Figure 2 teaches a bridge unit 104, which connects to a CPU bus 108 and a memory bus 110, including control logic 242, shown in paragraph 0037 to direct the operations of the queue storage elements through a network of control signals. Figure 2 also illustrates a data path between the CPU bus 108 and memory bus 110 through queues 250 and 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a main control device coupled to the memory device interface and data path as taught by Chin in the interface controller of Falik.

The motivation for doing so would have been to provide a means to manage the transfer of data through the interface performed by the system of Falik, see Chin paragraph 0037.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as specified in **claim 68**.

14. **Claims 62 and 63** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Chin et al. (US 2001/0010066) as applied to claim 61 above, and further in view of Tsuruta (US 2007/0174506).

Claim 62 is taught by the combination of Falik and Chin as shown supra with respect to claim 61.

The combination of Falik and Chin does not expressly teach that the IO bus controller is disposed to respond to said memory transaction request by acknowledging said request and providing status to said main control device.

With respect to claim 62, Tsuruta teaches:

Wherein said IO bus controller is disposed to respond to a memory transaction request by acknowledging said request and providing status to said main control device. Paragraph 0183 shows that in response to a read req from the CPU, MEM-DMAC 232 issues a read ack signal. Paragraph 0186 shows that after the read operation is performed, a sequencer in the memory controller 231 issues ack to a sequencer in the MEM-DMAC 232.

At the time of the invention, it would have been obvious to use the acknowledgement system of Tsuruta in the combination of Falik and Chin.

The motivation for doing so would have been to provide coordination between the CPU interface and the read/write queues to perform the requested memory operations.

Therefore, it would have been obvious to combine Tsuruta with Falik and Chin to obtain the invention as specified in **claims 62 and 63**.

Claim 63 is taught by Chin as:

The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction. Paragraph 0052 shows that control logic provides control signals to the input and output selectors 351 and 353 that determine the values of the enable and select signals in response to a memory request from the CPU.

Coordinates the operation of said memory device interface. Paragraph 0052 shows that the data and address of each request is sent to the memory controller 200.

And manages the transfer of memory transaction data between said IO device interface and said memory device interface through a data path. Paragraph 0052 shows that data is transferred through the queue 250.

Response to Arguments

15. Applicant's arguments filed 10/21/2013 have been carefully and fully considered but they are not persuasive.

16. In the second paragraph beginning on page 24 of the remarks submitted 10/21/2013, Applicant argues:

> "In contrast, Falik does not disclose associating any device profiles with a memory location used for a memory read or memory write transaction."

17. The Examiner respectfully disagrees. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

18. In the first paragraph beginning on page 25 of the remarks submitted 10/21/2013, Applicant argues:

> "In contrast, Falik discloses characteristics of each logical section 57 (Falik: column 15, line 63), and these logical sections contain logical blocks (and these logical blocks are Main Block 51 and Information Block 52) (Falik: column 14, line 51-56). Therefore, Falik discloses logical sections as associated with these characteristics. However, these logical blocks in these logical sections are for storing data used by any application in a Main Device, or for storing auxiliary data (e.g., configuration data or control data) used by the Main Device or application programs (Falik: column 14, lines 21-31 and lines 51-58). Therefore, these logical blocks (and logical sections that contain these logical blocks) are not addressable sections used for a memory read or memory write transaction. Therefore, Falik does not disclose these logical sections as memory locations that are addressed. Accordingly, Falik does not disclose all the limitations of claim 1."

19. The Examiner respectfully disagrees. Initially, the Examiner respectfully notes that Applicant has provided no rational support for the statement that data used by a device is not read or written. Further, the Examiner respectfully notes that Falik column 22 lines 16-20 expressly states that reading of data from memory and modifying contents of the memory (i.e. erasing and programming) are carried out as transactions, initiated by appropriate commands and affected by the contents of the specified

registers. Column 16 line 53 through column 17 line 24 further discusses the use of addresses to read and write data from the memory.

20. In the first paragraph beginning on page 26 of the remarks submitted 10/21/2013, Applicant argues:

> "Falik further discloses the device and status control register (Falik: Figure 5A) which provides status and control information for an entire memory device (Falik: column 19, lines 4-8). Falik also discloses a flash device capabilities register (Falik: Figure 5B) that provides capabilities and properties information on the same entire memory device (Falik: column 19, lines 49-53). Therefore, these registers contain information directed to the same entire memory device and not directed to different memory locations. These registers do not contain a first set of attributes of a first memory location and also do not contain a second set of attributes of a second memory location."

21. The Examiner respectfully disagrees. Falik column 20 lines 49-55 states: Section Properties Register 'i' (FIG. 5C) is a read-only register, of double-word length, that provides to the MD (By means of the Section Properties Read command) information on the structural properties of Section 'i' of the flash device. There is one such register for each of the sections in the device..." Accordingly, there are a first set of attributes of a first memory location and a second set of attributes of a second memory location.

22. In the fourth paragraph beginning on page 29 of the remarks submitted 10/21/2013, Applicant argues:

> "The Office admits that Falik does not expressly teach that the methods may be implemented using a computer readable medium comprising computer executable instructions. In order to supply the missing limitations, the Office combines Falik with Rubinstein. The Office argues it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a computer readable medium comprising computer executable instructions (Office Action: page 44). The Applicants respectfully disagree with the assertions of the Office."

23. The Examiner respectfully disagrees, and notes that as shown by Rubinstein, the implementation of methods in software stored in computer readable media is well known to one of ordinary skill in the art.

Conclusion

24. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JARED RUTZ whose telephone number is (571)272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, April Blair can be reached on (571)270-1014. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jared I Rutz
Primary Examiner
Art Unit 2187

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REMARKS/ARGUMENTS

Claim Rejections

35 USC 102

Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-97

Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-97 are rejected under 35 U.S.C. 102(e) as allegedly being anticipated by US 8,200,879 to Falik et al. ("Falik"). Claims 1, 45, 59, and 80 are independent claims. Applicants respectfully traverse this rejection.

Applicants respectfully disagree with this rejection, but to expedite allowance of the claims, Applicants amend independent claim 1 herein to recite the above-noted features. Support for the amendment in claim 1 is found in the filed application in, for example, Figures 1 and 2 and accompanying text, and paragraphs [0015], [0016], [0017], [0018], [0019], [0025], and [0029].

The Office equates the first device profile and second device profile of claim 1 with the structure tables (Falik: Figures 5A-5F) of various registers 12 (Falik: Figure 4A) in the flash interface controller 10 of Falik (Final Office Action: page 5).

However, Applicants respectfully argue that the structure tables in Figures 5A-5F of Falik are properties of registers 12, wherein the registers 12 are not disposed within memory devices in a memory store and the registers 12 of Falik are instead disposed within the flash interface controller 10. Thus, Falik discloses the structure tables

(of Figures 5A-5F) as stored into the controller 10 (Falik: Figure 4A) and not stored in the flash memory arrays 70. Therefore, Falik does not disclose and does not teach the "first device profile and second device profile are each stored in the memory store" as required in claim 1. Additionally, Falik does not disclose and does not teach "wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location" as required in claim 1.

Since Falik does not disclose and does not teach all the limitations of claim 1, claim 1 is not anticipated by the cited reference. Claim 1 is otherwise allowable.

Claims 2-14, 20, 21, 25, and 94 depend from allowable claim 1; as such, they are also allowable for at least the same reasons as claim 1.

The withdrawal of the rejections to claims 1-14, 20, 21, 25, and 94 is respectfully requested.

Independent claims 45, 59, and 80 recite at least some limitations similar to that as claim 1. Although claims 45, 59, and 80 are different, Applicants respectfully argue that in this case the above arguments regarding the patentability of claim 1 apply with equal force with respect to claims 45, 59, and 80. Since Falik does not disclose and does not teach all the limitations of claims 45, 59, and 80, claims 45, 59, and 80 are not anticipated

by the cited reference. Claims 45, 59, and 80 are otherwise allowable.

Claims 46-58 and 95 depend from allowable claim 45; as such, they are also allowable for at least the same reasons as claim 45.

Claims 60, 69-79, and 96 depend from allowable claim 59; as such, they are also allowable for at least the same reasons as claim 59.

Claims 81-92 and 97 depend from allowable claim 80; as such, they are also allowable for at least the same reasons as claim 80.

The withdrawal of the rejection to claims 45-60, 69-92, and 95-97 is respectfully requested.

Claims 15, 18, and 19

Claims 15, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 7,330,954 to Nangle.

Claims 15, 18, and 19 depend from allowable claim 1; as such, they are also allowable for at least the same reasons as claim 1.

The withdrawal of the rejection of claims 15, 18, and 19 is respectfully requested.

Claims 16, 17, 22-24, and 93

Claims 16, 17, 22-24, and 93 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 2006/0184723 to Sinclair.

Claims 16, 17, and 22-24 depend from allowable claim 1; as such, they are also allowable for at least the same reasons as claim 1.

Claim 93 depends from allowable claim 80; as such, claim 93 is also allowable for at least the same reasons as claim 1.

The withdrawal of the rejection of claims 16, 17, 22-24, and 93 is respectfully requested.

Claims 26-28

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 6961,805 to Lakhani et al.

Claims 26-28 depend from allowable claim 1; as such, they are also allowable for at least the same reasons as claim 1.

The withdrawal of the rejection of claims 26-28 is respectfully requested.

Claims 29-44

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 5,913,215 to Rubinstein.

The Office admits that Falik does not expressly teach that the methods may be implemented using a computer readable medium comprising computer executable instructions. In order to supply the missing limitations, the Office combines Falik with Rubinstein. The Office argues it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a

computer readable medium comprising computer executable instructions (Office Action: page 44). The Applicants respectfully disagree with the assertions of the Office.

Independent claim 29 recite at least some limitations similar to that as claim 1. Although claim 29 is different, Applicants respectfully argue that in this case the above arguments regarding the patentability of claim 1 apply with equal force with respect to claim 29.

Since Falik and Rubinstein, considered individually or in combination, do not disclose and does not teach all the limitations of claim 29, claim 29 is not rendered obvious in view the cited references. Claim 29 is otherwise allowable.

Claims 30-44 depend from allowable claim 29; as such, they are also allowable for at least the same reasons as claim 29.

The withdrawal of the rejection of claims 29-44 is respectfully requested.

Claims 61 and 64-68

Claims 61 and 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 2001/0010066 to Chin et al.

Claims 61 and 64-68 depend from allowable claim 59; as such, they are also allowable for at least the same reasons a claim 59.

The withdrawal of the rejection of claims 61 and 64-68 is respectfully requested.

Claims 62 and 63

Claims 61 and 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of Chin as applied to claim 61 above, and further in view of US 2007/0174506 to Tsuruta.

Claims 62 and 63 depend from allowable claim 59; as such, they are also allowable for at least the same reasons a claim 59.

The withdrawal of the rejection of claims 62 and 63 is respectfully requested.

Applicant also maintain the arguments presented in the amendment filed on 15 October 2013 for this application.

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, the Applicants are not conceding in this application that previously pending claims are unpatentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application.

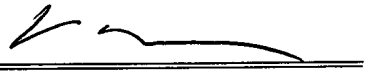
Conclusion

Claims 1-97 herein are allowable, and a timely Notice of Allowance is respectfully requested.

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (805) 569-1600.

Date: June 13, 2014

Respectfully submitted,



Arnold de Guzman
Attorney for Applicant(s)
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CERTIFICATE OF TRANSMISSION OR MAILING 37 C.F.R. 1.8			
I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office in accordance with 37 C.F.R. § 1.6(d), or is being transmitted via the Office electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4), or is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below:			
Signature:			
Typed or Printed Name:	Arnold de Guzman	Dated:	**June 13, 2014**
Express Mail Mailing Number (*optional*):			

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising:

addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile, wherein said second memory location is in a second memory device in the memory store, wherein a memory read transaction or a memory write transaction is performed on at least one of the first memory location or second memory location, wherein data is transferred to the first memory location or second memory location for a memory write transaction, wherein data is transferred from the first memory location or second memory location for a memory read transaction;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;

wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location;

wherein the memory store is coupled by at least one memory bus to a controller, and wherein the controller performs the memory transactions on the memory store;

wherein the first device profile and second device profile are each stored in the memory store; and

using attributes from said first and second device profiles.

2. (original) The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device.

3. (original) The method of claim 1, wherein said difference between said first and second device profiles includes different attributes; and said addressing said first memory location is made in response to a first memory transaction request; and

further including addressing said second memory location.

4. (original) The method of claim 1, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes.

5. (original) The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

6. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute values.

7. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute types.

8. (original) The method of claim 5, wherein said shared attributes include a memory device type attribute.

9. (original) The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

10. (original) The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

11. (original) The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

12. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

13. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of attributes that differs in value from a second page size attribute from said second set of attributes.

14. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes.

15. (original) The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device, and said second memory device interface attribute corresponds to a DRAM device interface.

16. (original) The method of claim 2, wherein said using attributes from said first and second device profile further includes using a first partial page size attribute from said first set of attributes that differs in value from a second partial page size attribute from said second set of attributes.

17. (original) The method of claim 16:

said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute; and

further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute.

18. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

19. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a NAND flash memory device and said second memory device type attribute corresponds to a NOR flash memory device.

20. (original) The method of claim 2, further including:

using an address corresponding to a memory location from said first memory device and transferring a first data set, and

using an address corresponding to a memory location from said second memory device and transferring a second data set.

21. (original) The method of claim 20, wherein:

said first set of attributes includes a first page size attribute, and said first data set includes a first data set size; and

if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size.

22. (original) The method of claim 20, wherein:

said second set of attributes includes a second page size attribute, and said second data set includes a second data set size; and

if said second data set size is greater than said second page size attribute, said transferring said second data set includes:

performing a set of write operations on said second memory device that includes using a second transfer size equal to said second page size attribute until a remaining

portion of said second data set that has not yet been written to said second device is less than said second page size attribute, and

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

23. (previously presented) The method of claim 20, wherein:

said first set of attributes includes a page size attribute and a block size attribute;

said first data set includes a first data set size;

if said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes:

performing a set of write operations on said first memory device that includes using a second transfer size equal to said page size attribute until a remaining portion of said first data set that has not yet been written to said first device is less than said page size attribute,

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

24. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes:

performing respective write operations on said first and second memory devices by at least using a transfer size at least equal to a partial page size attribute from said first set of attributes and performing at least one write operation on said second memory device by at least using a transfer size at least equal to a partial page size attribute value from said second set of attributes; and

said attribute difference includes different attribute values of said first and second partial page size attributes.

25. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size attribute of said first memory device.

26. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a block size attribute value that corresponds to a block size attribute of said first memory device.

27. (original) The method of claim 26, wherein said using attributes from said first and second device profile

further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

28. (original) The method of claim 2, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

29. (currently amended) A non-transitory computer readable medium comprising computer executable instructions adapted to cause a method of performing memory transactions on a first memory location and a second memory location, said method comprising:

addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile, wherein said second memory location is in a second memory device in the memory store;

said first device profile representing a first set of attributes of said first memory device, and said second device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles;

wherein each attribute in the first set of attributes and second set of attributes is associated with a

respective attribute qualifier that qualifies a respective memory location;

wherein the memory store is coupled by at least one memory bus to a controller, and wherein the controller performs the memory transactions on the memory store;

wherein the first device profile and second device profile are each stored in the memory store; and

using attributes from said first and second device profiles.

30. (original) The computer readable medium of claim 29, wherein:

said first memory location is part of a memory space associated with a first memory device;

said second memory location is part of a memory space associated with a second memory device; and

said first and second memory devices comprise at least a portion of a memory store.

31. (previously presented) The computer readable medium of claim 29, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of a first memory device and a block size value of a second memory device.

32. (previously presented) The computer readable medium of claim 30, wherein at least one attribute of said

attributes includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

33. (original) The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

34. (original) The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes.

35. (previously presented) The computer readable medium of claim 29, wherein said addressing further includes:

said first and second device profiles having at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

36. (original) The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

37. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values.

38. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types.

39. (original) The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute.

40. (original) The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

41. (original) The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

42. (original) The computer readable medium of claim 36, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

43. (original) The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes.

44. (original) The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device.

45. (currently amended) A memory controller for performing memory transactions, said memory controller comprising:

a means for addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile, wherein said second memory location is in a second memory device in the memory store;

wherein said means for addressing includes an interface controller means for processing memory transaction requests;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;

wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location;

wherein the memory store is coupled by at least one memory bus to the interface controller means, and wherein

the interface controller means performs the memory transactions on the memory store;

wherein the first device profile and second device profile are each stored in the memory store; and

said means for addressing uses attributes from said first and second device profiles.

46. (original) The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

47. (original) The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

48. (original) The memory controller of claim 46, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said use of said attributes from said first and second device profiles by said means for addressing includes using

said different attribute qualifiers for said shared attributes.

49. (original) The memory controller of claim 46, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

50. (previously presented) The memory controller of claim 45, wherein said means for addressing further includes a means for addressing said second memory location.

51. (original) The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

52. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values.

53. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types.

54. (original) The memory controller of claim 51, wherein said shared attributes include a memory device type attribute.

55. (original) The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

56. (original) The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

57. (original) The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

58. (original) The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device.

59. (currently amended) A memory controller comprising:

an interface controller coupled to a memory device interface and an IO device interface;

said interface controller disposed to perform a memory transaction by addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile, wherein said second memory location is in a second memory device in the memory store;

said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;

wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location;

wherein the memory store is coupled by at least one memory bus to the interface controller, and wherein the interface controller performs the memory transactions on the memory store;

wherein the first device profile and second device profile are each stored in the memory store; and

said addressing of said first memory location includes using said attributes from said first device profile.

60. (original) The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile.

61. (previously presented) The memory controller of claim 59, wherein said interface controller includes:

a main control device coupled to said memory device interface and to a data path;

a first memory bus controller coupled to said control device and said memory device interface; and

an IO bus controller coupled to said IO device interface and said control device.

62. (previously presented) The memory controller of claim 61, wherein said IO bus controller is disposed to respond to a memory transaction request by acknowledging said request and providing status to said main control device.

63. (original) The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction, coordinates the operation of said memory device interface, and manages the transfer of memory transaction data between said IO device interface and said memory device interface through a data path.

64. (previously presented) The memory controller of claim 59, further including a buffer comprising a FIFO and a data path that includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface.

65. (original) The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots.

66. (original) The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a plurality of queue slots that buffer data from said IO device interface to said memory device interface.

67. (original) The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from said memory device interface to said IO device interface.

68. (previously presented) The memory controller of claim 59, further including a second memory bus controller coupled to a main control device and said memory device interface.

69. (original) The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes.

70. (original) The memory controller of claim 59, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

71. (original) The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

72. (original) The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute.

73. (original) The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values.

74. (original) The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values.

75. (original) The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type.

76. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values.

77. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types.

78. (original) The memory controller of claim 71, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

79. (original) The memory controller of claim 71, wherein said shared attributes include a page size attribute and

said different attribute qualifiers include different page size values.

80. (currently amended) An electronic storage device, comprising:

a memory controller disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile;

wherein the first memory location is in a first memory device in a memory store;

wherein the second memory location is in a second memory device in the memory store;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;

wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location;

wherein the memory store is coupled by at least one memory bus to the memory controller, and wherein the memory controller performs the memory transactions on the memory store;

wherein the first device profile and second device profile are each stored in the memory store; and

said memory controller using attributes from said first and second device profiles.

81. (original) The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

82. (original) The electronic storage device of claim 80, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

83. (previously presented) The electronic storage device of claim 80, said memory controller further disposed to:

perform a write operation on said first memory device, if a memory transaction request is associated with a write request;

perform a read operation on said first memory device, if said memory transaction request is associated with a read request; and

wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using

said second device profile in response to receiving a second memory transaction request.

84. (original) The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

85. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values.

86. (original) The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute.

87. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types.

88. (original) The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said shared attributes.

89. (original) The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device.

90. (original) The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

91. (original) The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

92. (original) The electronic storage device of claim 84, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

93. (original) The electronic storage device of claim 80, wherein said memory controller is further adapted to:

use a first partial page size attribute by performing a write operation on said first memory device and using a transfer size at least equal to said partial page size attribute; and

use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute.

94. (previously presented) The method of claim 1, wherein the first memory location and the second memory location are addressable memory locations.

95. (previously presented) The memory controller of claim 45, wherein the first memory location and the second memory location are addressable memory locations.

96. (previously presented) The memory controller of claim 59, wherein the first memory location and the second memory location are addressable memory locations.

97. (previously presented) The electronic device of claim 80, wherein the first memory location and the second memory location are addressable memory locations.

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12/876,113	09/04/2010	Ricardo H. BRUCE	6005.042	1607

64180 7590 07/11/2014

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EXAMINER	
RUTZ, JARED IAN	
ART UNIT	PAPER NUMBER
2187	

NOTIFICATION DATE	DELIVERY MODE
07/11/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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labid@uriartelaw.com
arnold@uriartelaw.com

Office Action Summary	Application No. 12/876,113	Applicant(s) BRUCE ET AL.	
	Examiner JARED RUTZ	Art Unit 2187	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/19/2014*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-97* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-97* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

2. Claims 1-97, as amended on 6/19/2014, are pending in the instant application. Applicant' arguments submitted 6/19/2014 have been carefully and fully considered, but are not found persuasive. The instant Office action is made **FINAL**.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/19/2014 has been entered.

4. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-97** are rejected under 35 U.S.C. 102(e) as being anticipated by Falik et al. (US 8,200,879).

Claim 1 is taught by Falik as:

A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising: addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Wherein said second memory location is in a second memory device in the memory store. Column 6 lines 11-16 shows that the different parameters correspond to different memory arrays. Accordingly, the address corresponding to a different section may be in a second memory device.

Wherein a memory read transaction or a memory write transaction is performed on at least one of the first memory location or second memory location, wherein data is transferred to the first memory location of second memory location for a memory write transaction, wherein data is transferred from the first memory location or second memory location for a memory read

transaction. Column 22 lines 16-20 shows that reading of data from memory and modifying contents of the memory (i.e. erasing and programming) are carried out as transactions, initiated by appropriate commands and affected by the contents of the specified registers. Column 16 line 53 through column 17 line 24 further discusses the use of addresses to read and write data from the memory. Column 6 is an illustration of reads and writes to different addresses in different sections of the memory.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

Wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location. Column 20 line 49 through column 21 line 15 shows that the section properties register stores values representing the section of the flash device, and that there is a section properties register for each section of the flash device.

Wherein the memory store is coupled by at least one memory bus to a controller, and wherein the controller performs the memory transactions on the

memory store. Figure 1 shows that main die interface controller connects to the flash die via bus 90, as discussed at column 10 lines 5-15. Column 27 lines 8-32 shows that the MD sends commands to the FD.

Wherein the first device profile and second device profile are each stored in the memory store. Column 18 lines 53-64 show that the control, status and capabilities registers 12 and 112 are located on the flash device, and can be kept in the flash device's own memory.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 2 is taught by Falik as:

The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 3 is taught by Falik as:

The method of claim 1, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

And said addressing said first memory location is made in response to a first memory transaction request. Column 18 lines 24-34 shows that applications on the main die 100 issue read and program commands.

And further including addressing said second memory location. Figure 6 shows that both sections can be addressed.

Claim 4 is taught by Falik as:

The method of claim 1, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 5 is taught by Falik as:

The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second

device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 6 is taught by Falik as:

The method of claim 5, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 7 is taught by Falik as:

The method of claim 5, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 8 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a memory device type attribute. Column 20 lines 30-36 shows that the registers can indicate if the device is self timed type flash memory or not.

Claim 9 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 10 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 11 is taught by Falik as:

The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 12 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 13 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of attributes that differs in value from a second page size attribute from said second set of attributes. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 14 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes. Column 19 lines 56-59

shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 20 is taught by Falik as:

The method of claim 2, further including: using an address corresponding to a memory location from said first memory device and transferring a first data set. Column 16 lines 53-62 shows that an address and data are sent for a programming operation.

And using an address corresponding to a memory location from said second memory device and transferring a second data set. Column 14 lines 51-65 show that the standard address space is mapped to the logical sections into which the arrays are grouped, showing that the second memory device is accessed using an address corresponding to the second memory device.

Claim 21 is taught by Falik as:

The method of claim 20, wherein: said first set of attributes includes a first page size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

And said first data set includes a first data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

And if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size. Column 27 lines 9-24 shows that when the number of bytes to be transferred to the FD have been transferred, the transfer process ends by setting the bus to a HiZ state.

Claim 25 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size attribute of said first memory device. As discussed at column 27 lines 33-60, the program buffer corresponds to the batch size, which is the amount of data which can be programmed into the flash array at once.

Claim 45 is taught by Falik as:

A memory controller for performing memory transactions, said memory controller comprising: a means for addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is

addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Wherein said means for addressing includes an interface controller means for processing memory transaction requests. Figure 4B, flash bus transactions state machine 116.

Wherein said second memory location is in a second memory device in the memory store Column 6 lines 11-16 shows that the different parameters correspond to different memory arrays. Accordingly, the address corresponding to a different section may be in a second memory device.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

Wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location. Column 20 line 49 through column 21 line 15 shows that the section properties register stores values representing the section of the flash device, and that there is a section properties register for each section of the flash device.

Wherein the memory store is coupled by at least one memory bus to the interface controller means, and wherein the interface controller means performs the memory transactions on the memory store. Figure 1 shows that main die interface controller connects to the flash die via bus 90, as discussed at column 10 lines 5-15. Column 27 lines 8-32 shows that the MD sends commands to the FD.

Wherein the first device profile and second device profile are each stored in the memory store. Column 18 lines 53-64 show that the control, status and capabilities registers 12 and 112 are located on the flash device, and can be kept in the flash device's own memory.

And said means for addressing uses attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 46 is taught by Falik as:

The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 47 is taught by Falik as:

The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 48 is taught by Falik as:

The memory controller of claim 46, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said use of said attributes from said first and second device profiles by said means for addressing includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 49 is taught by Falik as:

The memory controller of claim 46, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 50 is taught by Falik as:

The memory controller of claim 45, wherein said means for addressing further includes a means for addressing said second memory location. Figure 6 shows that both sections can be addressed.

Claim 51 is taught by Falik as:

The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths

Support indicates the logical bus width values that a particular flash device supports.

Claim 52 is taught by Falik as:

The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 53 is taught by Falik as:

The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 54 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 55 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 56 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 57 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 58 is taught by Falik as:

The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

Claim 59 is taught by Falik as:

A memory controller comprising: an interface controller coupled to a memory device interface and an IO device interface. Figure 4B shows interface controller 110 connected to bus 90 and internal bus 140.

Said interface controller disposed to perform a memory transaction by addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Wherein said second memory location is in a second memory device in the memory store. Column 6 lines 11-16 shows that the different parameters

correspond to different memory arrays. Accordingly, the address corresponding to a different section may be in a second memory device.

Said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

Wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location. Column 20 line 49 through column 21 line 15 shows that the section properties register stores values representing the section of the flash device, and that there is a section properties register for each section of the flash device.

Wherein the memory store is coupled by at least one memory bus to the interface controller, and wherein the interface controller performs the memory transactions on the memory store. Figure 1 shows that main die interface controller connects to the flash die via bus 90, as discussed at column 10 lines 5-15. Column 27 lines 8-32 shows that the MD sends commands to the FD.

Wherein the first device profile and second device profile are each stored in the memory store. Column 18 lines 53-64 show that the control, status and

capabilities registers 12 and 112 are located on the flash device, and can be kept in the flash device's own memory.

And said addressing of said first memory location includes using said attributes from said first device profile. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 60 is taught by Falik as:

The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile. Figure 6 shows that both sections can be addressed.

Claim 69 is taught by Falik as:

The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

Claim 70 is taught by Falik as:

The memory controller of claim 59, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows

that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 71 is taught by Falik as:

The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 72 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 73 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 74 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 75 is taught by Falik as:

The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 76 is taught by Falik as:

The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 77 is taught by Falik as:

The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 78 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 79 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 80 is taught by Falik as:

An electronic storage device, comprising: a memory controller disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Wherein the first memory location is in a first memory device in a memory store; wherein the second memory location is in a second memory device in the

memory store. Column 6 lines 11-16 shows that the different parameters correspond to different memory arrays. Accordingly, the first location may be in a different memory device than the second location.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

Wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location. Column 20 line 49 through column 21 line 15 shows that the section properties register stores values representing the section of the flash device, and that there is a section properties register for each section of the flash device.

Wherein the memory store is coupled by at least one memory bus to the memory controller, and wherein the memory controller performs the memory transactions on the memory store. Figure 1 shows that main die interface controller connects to the flash die via bus 90, as discussed at column 10 lines 5-15. Column 27 lines 8-32 shows that the MD sends commands to the FD.

Wherein the first device profile and second device profile are each stored in the memory store. Column 18 lines 53-64 show that the control, status and capabilities registers 12 and 112 are located on the flash device, and can be kept in the flash device's own memory.

And said memory controller using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 81 is taught by Falik as:

The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command. Column 9 lines 5-18 shows that the interface performs appropriate requests for erasure.

Claim 82 is taught by Falik as:

The electronic storage device of claim 80, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 83 is taught by Falik as:

The electronic storage device of claim 80, said memory controller further disposed to: perform a write operation on said first memory device, if a memory transaction request is associated with a write request. Column 16 lines 53-64 shows that write transactions may be performed.

Perform a read operation on said first memory device, if said memory transaction request is associated with a read request. Column 16 lines 53-64 shows that read transactions may be performed.

And wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using said second device profile in response to receiving a second memory transaction request. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used for accesses to the groups of memory arrays.

Claim 84 is taught by Falik as:

The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 85 is taught by Falik as:

The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 86 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 87 is taught by Falik as:

The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 88 is taught by Falik as:

The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said

shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 89 is taught by Falik as:

The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

Claim 90 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 91 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash

device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 92 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 94 is taught by Falik as:

The method of claim 1, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 95 is taught by Falik as:

The memory controller of claim 45, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address

into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 96 is taught by Falik as:

The memory controller of claim 59, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 97 is taught by Falik as:

The electronic device of claim 80, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 15, 18, and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Nangle (US 7,330,954).

Claim 15 is taught by Falik as:

The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device. Column 21 lines 7-10 shows that the information can correspond to a flash device FD.

Although Falik column 21 lines 7-10 shows that other memory technologies such as SRAM may be used, it does not expressly teach that the second memory device attribute corresponds to a DRAM device interface.

With respect to claim 15, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 lines 51-67 shows that the memory devices may be flash memory and DRAM.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include flash memory and DRAM in the system of Falik.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 15**.

Claim 18 is taught by Falik as shown supra with respect to claim 8.

Falik does not expressly teach that said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

With respect to claim 18, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 line 51 through column 5 line 4 shows that the memory devices may be volatile memory that have a battery backup.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a volatile memory disposed to receive backup power from a portable power source.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 18**.

Claim 19 is taught by Falik as shown supra with respect to claim 8.

Falik does not expressly teach that said first memory device type attribute corresponds to a NAND flash memory device and said second memory device type attribute corresponds to a NOR flash memory device.

With respect to claim 19, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 lines 51-65 shows that the memory devices may be NAND or NOR type flash memories.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a volatile memory disposed to receive backup power from a portable power source.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 19**.

9. **Claims 16, 17, 22-24, and 93** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Sinclair et al. (US 2006/0184723).

Claim 16 if taught by Falik as shown supra with respect to claim 2.

Although Falik teaches that the width of the array is the minimum programming size of the array at column 20 lines 62-65, and that the width of the array is stored at column 20 lines 49-52, Falik does not expressly teach that a first and second partial page size attribute is stored and used.

With respect to claim 16, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claims 16 and 17**.

Claim 17 is taught by Falik and Sinclair as:

The method of claim 16: said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute. Sinclair paragraph 0168 shows that in a flash memory that supports

partial page programming, when sufficient data is transferred to the buffer, it is programmed to the page. Falik column 14 lines 51-60 and figure 3 shows that the first memory device group can be accessed.

And further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute. Sinclair paragraph 0168 shows that in a flash memory that supports partial page programming, when sufficient data is transferred to the buffer, it is programmed to the page. Falik column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

Claim 22 is taught by Falik as:

The method of claim 20, wherein: said second set of attributes includes a second page size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

And said second data set includes a second data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

And if said second data set size is greater than said second page size attribute, said transferring said second data set includes: performing a set of

write operations on said second memory device that includes using a second transfer size equal to said second page size attribute. Column 16 lines 48-52 shows that program buffer 19 may be a double buffer, allowing the programming of one chunk of data while another chunk of data is received. As discussed at column 27 lines 33-60, the program buffer corresponds to the batch size, which is the amount of data which can be programmed into the flash array at once.

Falik does not expressly teach that the transaction is made using a transfer size equal to the page size until a remaining portion of said second data set that has not yet been written to said second device is less than said second page size attribute and using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

With respect to claim 22, Sinclair teaches Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times. As discussed in paragraph 0168, when the end of the data group is received in the buffer and it is smaller than a full page of data, a partial page programming operation may be performed.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 22**.

Claim 23 is taught by Falik as:

The method of claim 20, wherein: said first set of attributes includes a page size attribute and a block size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Said first data set includes a first data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

If said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes: performing a set of write operations on said first memory device that includes using a second transfer size equal to said page size attribute […]. Column 27 lines 14-24 shows that bytes of data are sent until all the bytes have been sent.

Falik does not expressly teach that the transaction is made using a transfer size equal to the page size until a remaining portion of said first data set that has not yet been written to said first device is less than said first page size attribute and using a last

transfer size equal to said remaining portion if said remaining portion is less than said page size.

With respect to claim 23, Sinclair teaches Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times. As discussed in paragraph 0168, when the end of the data group is received in the buffer and it is smaller than a full page of data, a partial page programming operation may be performed.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 23**.

Claim 24 is taught by Falik as shown supra with respect to claim 1, and further as:

> *The method of claim 1, wherein said using attributes from said first and second device profile further includes: performing respective write operations on said first and second memory devices by at least using a transfer size at least equal to a* […] *page size attribute from said first set of attributes.* Column 16

lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations.

And performing at least one write operation on said second memory device by at least using a transfer size at least equal to a […] *page size attribute value from said second set of attributes*. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations. Column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

And said attribute difference includes different attribute values of said first and second […] *page size attributes*. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Although Falik teaches storing a page size attribute, it does not expressly teach storing a partial page size attribute.

With respect to claim 24, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 24**.

Claim 93 is taught by Falik as shown supra with respect to claim 80, and further as:

> *The electronic storage device of claim 80, wherein said memory controller is further adapted to: use a first partial page size attribute by performing a write operation on said first memory device and using a transfer size at least equal to said partial page size attribute*. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations.
>
> *And use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute*. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations. Column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

Although Falik teaches storing a page size attribute, it does not expressly teach storing a partial page size attribute.

With respect to claim 93, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 93**.

10. **Claims 26-28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Lakhani et al. (US 6,961,805).

Claim 26 is taught by Falik as shown supra with respect to claim 1.

Falik further teaches, at column 20 lines 60-65, that Page Size Block1 stores the size of the minimal segment of a flash array erasable upon a single erase command. Additionally, column 16 line 53 through column 17 line 24 shows that data can be written to a block of addresses by designating the starting address and performing a series of program continue operations.

Falik does not expressly teach using the block size attribute in performing a write operation that uses a transfer size that corresponds to the block size.

With respect to claim 26, Lakhani teaches, at column 18 lines 19-46, that predecoder 50 asserts sets of multiblock selection bits in response to control bits from the controller, which allows a designated number of blocks to be selected for writing at the same time.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to perform a write operation that uses a transfer size equal to the a block size attribute value that corresponds to a block size attribute of the first memory device.

The motivation for doing so would have been to reduce the time used to test the memory cells of the block, Lakhani column 8 lines 21-32.

Therefore, it would have been obvious to combine Lakhani with Falik to obtain the invention as specified in **claims 26 and 27**.

Claim 27 is taught by Lakhani as:

> *The method of claim 26, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value*. Column 13 lines 25-38 shows that a plurality of blocks can be selected at the same time.

Claim 28 is taught by Falik as shown supra with respect to claim 2.

Falik further teaches, at column 20 lines 60-65, that Page Size Block1 stores the size of the minimal segment of a flash array erasable upon a single erase command. Additionally, column 16 line 53 through column 17 line 24 shows that data can be written to a block of addresses by designating the starting address and performing a series of program continue operations.

Falik does not expressly teach using the block size attribute in performing a write operation that uses a transfer size that is equal to a multiple of the block size.

With respect to claim 28, Lakhani teaches, at column 18 lines 19-46, that predecoder 50 asserts sets of multiblock selection bits in response to control bits from the controller, which allows a designated number of blocks to be selected for writing at the same time.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to perform a write operation that uses a transfer size equal to the a block size attribute value that corresponds to a block size attribute of the first memory device.

The motivation for doing so would have been to reduce the time used to test the memory cells of the block, Lakhani column 8 lines 21-32.
Therefore, it would have been obvious to combine Lakhani with Falik to obtain the invention as specified in **claim 28**.

11. **Claims 29-44** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Rubinstein et al. (US 5,913,215).

Claim 29 is taught by Falik as:

Said method comprising: addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Wherein said second memory location is in a second memory device in the memory store. Column 6 lines 11-16 shows that the different parameters correspond to different memory arrays. Accordingly, the address corresponding to a different section may be in a second memory device.

Said first device profile representing a first set of attributes of said first memory device, and said second device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14

lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

Wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location. Column 20 line 49 through column 21 line 15 shows that the section properties register stores values representing the section of the flash device, and that there is a section properties register for each section of the flash device.

Wherein the memory store is coupled by at least one memory bus to a controller, and wherein the controller performs the memory transactions on the memory store. Figure 1 shows that main die interface controller connects to the flash die via bus 90, as discussed at column 10 lines 5-15. Column 27 lines 8-32 shows that the MD sends commands to the FD.

Wherein the first device profile and second device profile are each stored in the memory store. Column 18 lines 53-64 show that the control, status and capabilities registers 12 and 112 are located on the flash device, and can be kept in the flash device's own memory.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Falik does not expressly teach that the methods may be implemented using a non-transitory computer readable medium comprising computer executable instructions.

With respect to claim 29, Rubinstein teaches at column 10, lines 3-15, that computer methods may be performed either by a series of instructions, or by specific hardware components that contain hard-wired logic for performing the method, or by any combination of the two.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a computer readable medium comprising computer executable instructions.

The rationale for doing so would have been that it is a known technique to implement methods in computer systems using a non-transitory computer readable medium comprising computer executable instructions.

Therefore, it would have been obvious to combine Rubinstein with Falik to obtain the invention as recited in **claims 29-44**.

Claim 30 is taught by Falik as:

> *The computer readable medium of claim 29, wherein: said first memory location is part of a memory space associated with a first memory device, said second memory location is part of a memory space associated with a second memory device*. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.
>
> *And said first and second memory devices comprise at least a portion of a memory store*. Figure 3 shows that the address space is mapped to the memory devices.

Claim 31 is taught by Falik as:

The computer readable medium of claim 29, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of a first memory device and a block size value of a second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 32 is taught by Falik as:

The computer readable medium of claim 30, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 33 is taught by Falik as:

The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 34 is taught by Falik as:

The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

Claim 35 is taught by Falik as:

The computer readable medium of claim 29, wherein said addressing further includes: said first and second device profiles having at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 36 is taught by Falik as:

The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from

said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 37 is taught by Falik as:

The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 38 is taught by Falik as:

The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 39 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 40 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 41 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 42 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 43 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 44 is taught by Falik as:

The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

12. **Claims 61 and 64-68** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Chin et al. (US 2001/0010066).

Claim 61 is taught by Falik as shown supra with respect to claim 59.

Falik further teaches:

The memory controller of claim 59, wherein said interface controller includes: A first memory bus controller coupled to said control device and said memory device interface. Falik figure 4b item 116.

And an IO bus controller coupled to said IO device interface and said control device. Falik figure 4b item 117.

With respect to claim 61, Chin figure 2 teaches a bridge unit 104, which connects to a CPU bus 108 and a memory bus 110, including control logic 242, shown in paragraph 0037 to direct the operations of the queue storage elements through a network of control signals. Figure 2 also illustrates a data path between the CPU bus 108 and memory bus 110 through queues 250 and 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a main control device coupled to the memory device interface and data path as taught by Chin in the interface controller of Falik.

The motivation for doing so would have been to provide a means to manage the transfer of data through the interface performed by the system of Falik, see Chin paragraph 0037.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as specified in **claim 61**.

Claim 64 is taught by Falik as shown supra with respect to claim 59.

Falik does not expressly teach that a buffer is a FIFO or that a data path includes a plurality of queue slots.

With respect to claim 64, Chin teaches:

Further including a buffer comprising a FIFO. Paragraph 0052 shows that queue 250 is a FIFO.

And a data path that includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory

device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory. Figure 2 also shows read queue 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a FIFO and a data path including a plurality of queue slots in the system of Falik.

The motivation for doing so would have been to provide an interface that provides all devices in a computer system fair access to memory, Chin paragraph 0012.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as recited in **claim 64**.

Claim 65 is taught by Falik as shown supra with respect to claim 59.

Falik does not expressly teach that a data path includes a buffer having a plurality of queue slots.

With respect to claim 65, Chin teaches:

The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a FIFO and a data path including a plurality of queue slots in the system of Falik.

The motivation for doing so would have been to provide an interface that provides all devices in a computer system fair access to memory, Chin paragraph 0012.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as recited in **claims 65-67**.

Claim 66 is taught by Chin as:

The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a plurality of queue slots that buffer data from said IO device interface to said memory device interface. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory.

Claim 67 is taught by Chin as:

The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from said memory device interface to said IO device interface. Figure 2 also shows read queue 252.

Claim 68 is taught by Falik as shown supra with respect to claim 1.

Falik further teaches a memory bus controller, figure 4b item 116, coupled to bus 90.

Falik does not expressly teach that the memory bus controller is coupled to a main control device.

With respect to claim 68, Chin teaches:

A second memory bus controller coupled to said main control device and said memory device interface. Figure 2 teaches a bridge unit 104, which connects to a CPU bus 108 and a memory bus 110, including control logic 242, shown in paragraph 0037 to direct the operations of the queue storage elements through a network of control signals. Figure 2 also illustrates a data path between the CPU bus 108 and memory bus 110 through queues 250 and 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a main control device coupled to the memory device interface and data path as taught by Chin in the interface controller of Falik.

The motivation for doing so would have been to provide a means to manage the transfer of data through the interface performed by the system of Falik, see Chin paragraph 0037.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as specified in **claim 68**.

13. **Claims 62 and 63** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Chin et al. (US 2001/0010066) as applied to claim 61 above, and further in view of Tsuruta (US 2007/0174506).

Claim 62 is taught by the combination of Falik and Chin as shown supra with respect to claim 61.

The combination of Falik and Chin does not expressly teach that the IO bus controller is disposed to respond to said memory transaction request by acknowledging said request and providing status to said main control device.

With respect to claim 62, Tsuruta teaches:

Wherein said IO bus controller is disposed to respond to a memory transaction request by acknowledging said request and providing status to said main control device. Paragraph 0183 shows that in response to a read req from the CPU, MEM-DMAC 232 issues a read ack signal. Paragraph 0186 shows that after the read operation is performed, a sequencer in the memory controller 231 issues ack to a sequencer in the MEM-DMAC 232.

At the time of the invention, it would have been obvious to use the acknowledgement system of Tsuruta in the combination of Falik and Chin.

The motivation for doing so would have been to provide coordination between the CPU interface and the read/write queues to perform the requested memory operations.

Therefore, it would have been obvious to combine Tsuruta with Falik and Chin to obtain the invention as specified in **claims 62 and 63**.

Claim 63 is taught by Chin as:

The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction. Paragraph 0052 shows that control logic provides control signals to the input and output

selectors 351 and 353 that determine the values of the enable and select signals in response to a memory request from the CPU.

Coordinates the operation of said memory device interface. Paragraph 0052 shows that the data and address of each request is sent to the memory controller 200.

And manages the transfer of memory transaction data between said IO device interface and said memory device interface through a data path. Paragraph 0052 shows that data is transferred through the queue 250.

Response to Arguments

14. Applicant's arguments filed 6/19/2014 have been fully considered but they are not persuasive.

15. In the fourth paragraph beginning on page 27, Applicant argues:

> "However, Applicants respectfully argue that the structure tables in Figures 5A-5F of Falik are properties of registers 12, Wherein the registers 12 are not disposed within memory devices in a memory store and the registers 12 of Falik are instead disposed within the flash interface controller 10. Thus, Falik discloses the structure tables (of Figures 5A-5F) as stored into the controller 10 (Falik: Figure 4A) and not stored in the flash memory arrays 70. Therefore, Falik does not disclose and does not teach the "first device profile and second device profile are each stored in the memory store" as required in claim 1. Additionally, Falik does not disclose and does not teach "wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location" as required in claim 1."

16. The Examiner respectfully disagrees. Falik column 18 lines 53-64 show that the information in control, status, and capabilities registers 12 may be echoed in in registers 112 on the memory device, and that the contents of registers 12 may be stored in

locations in the memory of the flash device. Column 15 line 63 through column 16 line 19 shows that the section capabilities register stored data for a section of the memory, including main block size and page size. Paragraph 0016 of the specification of the instant application shows that an attribute qualifier is a value or type that indicates a characteristic related to the memory attribute. Column 20 line 49 through column 21 line 15 of Falik shows that values representing the main block size, page size, among others, are stored in the section properties register.

17. In the eighth paragraph beginning on page 30, Applicant argues:

> "The Office admits that Falik does not expressly teach that the methods may be implemented using a computer readable medium comprising computer executable instructions. In order to supply the missing limitations, the Office combines Falik with Rubinstein. The Office argues it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a computer readable medium comprising computer executable instructions (Office Action: page 44). The Applicants respectfully disagree with the assertions of the Office."

18. The Examiner respectfully disagrees. The Examiner notes that Applicant has provided no explanation as to why it would not have been obvious to one of ordinary skill in the art to implement a method in a computer using a computer readable medium comprising computer executable instructions. The Examiner does not find this assertion persuasive, as the use of a computer readable medium storing instructions to implement a method in a computer is a well-known technique to one of ordinary skill in the art, as shown by Rubinstein.

Conclusion

19. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JARED RUTZ whose telephone number is (571)272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, April Blair can be reached on (571)270-1014. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jared I Rutz
Primary Examiner
Art Unit 2187

/JARED RUTZ/
Primary Examiner, Art Unit 2187

REMARKS/ARGUMENTS

New Claims

Claims 98-101 are being added and are supported in the filed application in, for example, Figures 1, 2A, 2B, 2C, 4, 5, and 6 and accompanying text. New claims 98-101 recite at least some features that are not disclosed and are not suggested in the cited references in the final office action dated 11 July 2014.

Since the cited references do not disclose and do not teach all the limitations of claims 98-101, claims 98-101 are not rendered obvious in view of the cited references. Claims 98-101 are each otherwise allowable.

Applicant respectfully requests the allowance of claims 98-101.

Claim Rejections

35 USC 102

Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-97

Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-97 are rejected under 35 U.S.C. 102(e) as allegedly being anticipated by US 8,200,879 to Falik et al. ("Falik"). Claims 1, 45, 59, and 80 are independent claims. Applicants respectfully traverse this rejection.

Applicants respectfully disagree with this rejection, but to expedite allowance of the claims, Applicants amend independent claim 1 herein to recite various features as shown above. Support for the amendment in claim 1 is found

in the filed application in, for example, Figures 1, 2A, 2B, 2C, 4, 5, and 6 and accompanying text.

Falik discloses a dual-controllers configuration having a main die controller 110 in a semiconductor main die 110, a flash die controller in a flash die 80, and a bus 90 directly coupled between the controller 110 and controller 10 (Falik: Figures 1, 4A, and 4B). Falik's dual-controllers configuration permits the semiconductor main die 10 to communicate with the flash die 80.

In contrast, claim 1 recites the features of, for example, a controller that is directly coupled by at least one memory bus to a memory store and the controller is also directly coupled to a host as the controller performs a memory transaction. The recited features in claim 1 are not disclosed in Falik. The recited features in claim 1 also advantageously avoids, for example, the complex circuitries (and increased die area and increased power requirements) of the dual-controllers configuration of Falik. Such advantages provided by the recited features of claim 1 are neither disclosed nor suggested in Falik, and it would be unreasonable to impart such advantageous limitations of claim 1 into Falik. Therefore, claim 1 recites limitations that are distinguishable from Falik based on at least the above-discussed advantages and/or based on the above-discussed claim 1 limitations that are absent in Falik.

Accordingly, Falik does not disclose all the limitations of claim 1. Since Falik does not disclose and does not teach all the limitations of claim 1, claim 1 is

not anticipated by the cited reference. Claim 1 is otherwise allowable.

Claims 2-14, 20, 21, and 25 depend from allowable claim 1; as such, they are also allowable for at least the same reasons as claim 1.

The withdrawal of the rejections to claims 1-14, 20, 21, 25 and 94 is respectfully requested.

Independent claims 45, 59, and 80 recite at least some limitations similar to that as claim 1. Although claims 45, 59, and 80 are different, Applicants respectfully argue that in this case the above arguments regarding the patentability of claim 1 apply with equal force with respect to claims 45, 59, and 80. Since Falik does not disclose and does not teach all the limitations of claims 45, 59, and 80, claims 45, 59, and 80 are not anticipated by the cited reference. Claims 45, 59, and 80 are otherwise allowable.

Claims 46-58 and 95 depend from allowable claim 45; as such, they are also allowable for at least the same reasons as claim 45.

Claims 60, 69-79, and 96 depend from allowable claim 59; as such, they are also allowable for at least the same reasons as claim 59.

Claims 81-92 and 97 depend from allowable claim 80; as such, they are also allowable for at least the same reasons as claim 80.

The withdrawal of the rejection to claims 45-60, 69-92, and 95-97 is respectfully requested.

Claims 15, 18, and 19

Claims 15, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 7,330,954 to Nangle.

Claims 15, 18, and 19 depend from allowable claim 1; as such, they are also allowable for at least the same reasons a claim 1.

The withdrawal of the rejection of claims 15, 18, and 19 is respectfully requested.

Claims 16, 17, 22-24, and 93

Claims 16, 17, 22-24, and 93 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 2006/0184723 to Sinclair.

Claims 16, 17, and 22-24 depend from allowable claim 1; as such, they are also allowable for at least the same reasons a claim 1.

Claim 93 depends from allowable claim 80; as such, claim 93 is also allowable for at least the same reasons a claim 1.

The withdrawal of the rejection of claims 16, 17, 22-24, and 93 is respectfully requested.

Claims 26-28

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 6961,805 to Lakhani et al.

Claims 26-28 depend from allowable claim 1; as such, they are also allowable for at least the same reasons a claim 1.

The withdrawal of the rejection of claims 26-28 is respectfully requested.

Claims 29-44

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 5,913,215 to Rubinstein.

The Office admits that Falik does not expressly teach that the methods may be implemented using a computer readable medium comprising computer executable instructions. In order to supply the missing limitations, the Office combines Falik with Rubinstein. The Office argues it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a computer readable medium comprising computer executable instructions (Office Action: page 44). The Applicants respectfully disagree with the assertions of the Office.

Independent claim 29 recite at least some limitations similar to that as claim 1. Although claim 29 is different, Applicants respectfully argue that in this case the above arguments regarding the patentability of claim 1 apply with equal force with respect to claim 29.

Since Falik and Rubinstein, considered individually or in combination, do not disclose and does not teach all the limitations of claim 29, claim 29 is not rendered obvious in view the cited references. Claim 29 is otherwise allowable.

Claims 30-44 depend from allowable claim 29; as such, they are also allowable for at least the same reasons a claim 29.

The withdrawal of the rejection of claims 29-44 is respectfully requested.

Claims 61 and 64-68

Claims 61 and 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 2001/0010066 to Chin et al.

Claims 61 and 64-68 depend from allowable claim 59; as such, they are also allowable for at least the same reasons a claim 59.

The withdrawal of the rejection of claims 61 and 64-68 is respectfully requested.

Claims 62 and 63

Claims 61 and 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of Chin as applied to claim 61 above, and further in view of US 2007/0174506 to Tsuruta.

Claims 62 and 63 depend from allowable claim 59; as such, they are also allowable for at least the same reasons a claim 59.

The withdrawal of the rejection of claims 62 and 63 is respectfully requested.

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, the Applicants are not conceding in this application that previously pending claims are unpatentable over the cited references. Rather, any alterations or characterizations

are being made to facilitate expeditious prosecution of this application.

Conclusion

Claims 1-101 herein are allowable, and a timely Notice of Allowance is respectfully requested.

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (805) 569-1600.

Date: October 7, 2014

Respectfully submitted,

__/Arnold de Guzman/__
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805-569-1600

Please send correspondence to:
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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising:

addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile, wherein said second memory location is in a second memory device in the memory store, wherein a memory read transaction or a memory write transaction is performed on at least one of the first memory location or second memory location, wherein data is transferred to the first memory location or second memory location from a host for a memory write transaction, wherein data is transferred from the first memory location or second memory location to the host for a memory read transaction;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;

wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location;

wherein the memory store is directly coupled [[by]]to at least one memory bus and wherein the at least one memory bus is directly coupled to a controller, and wherein the controller performs the memory read transaction and memory write transaction on the memory [[sore]]store;

wherein the host is directly coupled to the controller by a communication path as the controller performs the memory read transaction or memory write transaction;

wherein the first device profile and second device profile are each stored in the memory store; and

using attributes from said first and second device profiles.

2. (original) The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device.

3. (original) The method of claim 1, wherein said difference between said first and second device profiles includes different attributes; and said addressing said first memory location is made in response to a first memory transaction request; and

further including addressing said second memory location.

4. (original) The method of claim 1, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes.

5. (original) The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

6. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute values.

7. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute types.

8. (original) The method of claim 5, wherein said shared attributes include a memory device type attribute.

9. (original) The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

10. (original) The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

11. (original) The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

12. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

13. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of attributes that differs in value from a second page size attribute from said second set of attributes.

14. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes.

15. (original) The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device, and said second memory device interface attribute corresponds to a DRAM device interface.

16. (original) The method of claim 2, wherein said using attributes from said first and second device profile further includes using a first partial page size attribute from said first set of attributes that differs in value from a second partial page size attribute from said second set of attributes.

17. (original) The method of claim 16:

said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute; and

further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute.

18. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

19. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a NAND flash

memory device and said second memory device type attribute corresponds to a NOR flash memory device.

20. (original) The method of claim 2, further including:

using an address corresponding to a memory location from said first memory device and transferring a first data set, and

using an address corresponding to a memory location from said second memory device and transferring a second data set.

21. (original) The method of claim 20, wherein:

said first set of attributes includes a first page size attribute, and said first data set includes a first data set size; and

if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size.

22. (original) The method of claim 20, wherein:

said second set of attributes includes a second page size attribute, and said second data set includes a second data set size; and

if said second data set size is greater than said second page size attribute, said transferring said second data set includes:

performing a set of write operations on said second memory device that includes using a second transfer size equal to said second page size attribute until a remaining

portion of said second data set that has not yet been written to said second device is less than said second page size attribute, and

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

23. (previously presented) The method of claim 20, wherein:

said first set of attributes includes a page size attribute and a block size attribute;

said first data set includes a first data set size;

if said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes:

performing a set of write operations on said first memory device that includes using a second transfer size equal to said page size attribute until a remaining portion of said first data set that has not yet been written to said first device is less than said page size attribute,

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

24. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes:

performing respective write operations on said first and second memory devices by at least using a transfer size at least equal to a partial page size attribute from said

first set of attributes and performing at least one write operation on said second memory device by at least using a transfer size at least equal to a partial page size attribute value from said second set of attributes; and

said attribute difference includes different attribute values of said first and second partial page size attributes.

25. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size attribute of said first memory device.

26. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a block size attribute value that corresponds to a block size attribute of said first memory device.

27. (original) The method of claim 26, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

28. (original) The method of claim 2, wherein said using attributes from said first and second device profile

further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

29. (previously presented) A non-transitory computer readable medium comprising computer executable instructions adapted to cause a method of performing memory transactions on a first memory location and a second memory location, said method comprising:

addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory device, and said second device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles; and

using attributes from said first and second device profiles.

30. (original) The computer readable medium of claim 29, wherein:

said first memory location is part of a memory space associated with a first memory device;

said second memory location is part of a memory space associated with a second memory device; and

said first and second memory devices comprise at least a portion of a memory store.

31. (previously presented) The computer readable medium of claim 29, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of a first memory device and a block size value of a second memory device.

32. (previously presented) The computer readable medium of claim 30, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

33. (original) The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

34. (original) The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes.

35. (previously presented) The computer readable medium of claim 29, wherein said addressing further includes:

said first and second device profiles having at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

36. (original) The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

37. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values.

38. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types.

39. (original) The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute.

40. (original) The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

41. (original) The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

42. (original) The computer readable medium of claim 36, wherein said shared attributes includes any one of the

following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

43. (original) The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes.

44. (original) The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device.

45. (currently amended) A memory controller for performing memory transactions, said memory controller comprising:

a means for addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile;

said means for addressing is directly coupled to the first memory location and second memory location;

wherein said means for addressing includes an interface controller means for processing memory transaction requests;

said means for addressing is directly coupled to a host as said means for addressing addresses the first memory location or second memory location;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of

said second memory location, and a difference exists between said first and second device profiles; and

said means for addressing uses attributes from said first and second device profiles.

46. (original) The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

47. (original) The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

48. (original) The memory controller of claim 46, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said use of said attributes from said first and second device profiles by said means for addressing includes using said different attribute qualifiers for said shared attributes.

49. (original) The memory controller of claim 46, wherein said at least one attribute includes a block size and said

difference includes a block size value of said first memory device and a block size value of said second memory device.

50. (previously presented) The memory controller of claim 45, wherein said means for addressing further includes a means for addressing said second memory location.

51. (original) The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

52. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values.

53. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types.

54. (original) The memory controller of claim 51, wherein said shared attributes include a memory device type attribute.

55. (original) The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

56. (original) The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

57. (original) The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

58. (original) The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device.

59. (currently amended) A memory controller comprising:

an interface controller coupled to a memory device interface and an input/output (IO) device interface;

a memory store;

wherein the memory device interface is directly coupled to the memory store;

said interface controller disposed to perform a memory transaction by addressing a first memory location in the memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile;

said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said addressing of said first memory location includes using said attributes from said first device profile.

60. (original) The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile.

61. (previously presented) The memory controller of claim 59, wherein said interface controller includes:

a main control device coupled to said memory device interface and to a data path;

a first memory bus controller coupled to said control device and said memory device interface; and

an IO bus controller coupled to said IO device interface and said control device.

62. (previously presented) The memory controller of claim 61, wherein said IO bus controller is disposed to respond to a memory transaction request by acknowledging said request and providing status to said main control device.

63. (original) The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction, coordinates the operation of said memory device interface, and manages the transfer of memory transaction data between said IO device interface and said memory device interface through a data path.

64. (previously presented) The memory controller of claim 59, further including a buffer comprising a FIFO and a data path that includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface.

65. (original) The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots.

66. (original) The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a plurality of queue slots that buffer data from said IO device interface to said memory device interface.

67. (original) The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from said memory device interface to said IO device interface.

68. (previously presented) The memory controller of claim 59, further including a second memory bus controller coupled to a main control device and said memory device interface.

69. (original) The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes.

70. (original) The memory controller of claim 59, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

71. (original) The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

72. (original) The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute.

73. (original) The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values.

74. (original) The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values.

75. (original) The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type.

76. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values.

77. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types.

78. (original) The memory controller of claim 71, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

79. (original) The memory controller of claim 71, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

80. (currently amended) An electronic storage device, comprising:

a memory controller directly coupled to and disposed to address a first memory location and a second memory

location which are respectively associated with a first device profile and a second device profile;

said memory controller directly coupled to a host as said memory controller addresses the first memory location or second memory location;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said memory controller using attributes from said first and second device profiles.

81. (original) The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

82. (original) The electronic storage device of claim 80, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

83. (previously presented) The electronic storage device of claim 80, said memory controller further disposed to:

perform a write operation on said first memory device, if a memory transaction request is associated with a write request;

perform a read operation on said first memory device, if said memory transaction request is associated with a read request; and

wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using said second device profile in response to receiving a second memory transaction request.

84. (original) The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

85. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values.

86. (original) The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute.

87. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types.

88. (original) The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said shared attributes.

89. (original) The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device.

90. (original) The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

91. (original) The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

92. (original) The electronic storage device of claim 84, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

93. (original) The electronic storage device of claim 80, wherein said memory controller is further adapted to:

use a first partial page size attribute by performing a write operation on said first memory device and using a transfer size at least equal to said partial page size attribute; and

use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute.

94. (previously presented) The method of claim 1, wherein the first memory location and the second memory location are addressable memory locations.

95. (previously presented) The memory controller of claim 45, wherein the first memory location and the second memory location are addressable memory locations.

96. (previously presented) The memory controller of claim 59, wherein the first memory location and the second memory location are addressable memory locations.

97. (previously presented) The electronic device of claim 80, wherein the first memory location and the second memory location are addressable memory locations.

98. (new) An electronic storage device, comprising:

a memory controller directly coupled to and disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile;

wherein the memory controller is directly coupled to a host as the memory controller addresses the first memory location or the second memory location;

the first device profile representing a first set of attributes of the first memory location, and the second device profile representing a second set of attributes of the second memory location; and

wherein said memory controller uses attributes from the first and second device profiles.

99. (new) The electronic devices of claim 98, wherein the memory controller comprises:

an interface controller;

a memory device interface directly coupled to the first memory location and to the second memory location and coupled to the interface controller;

an input/output (IO) device interface coupled to the interface controller and directly coupled to the host as the memory controller addresses the first memory location or the second memory location.

100. (new) A method for performing memory transactions, the method comprising:

addressing a first memory location in a first memory device in a memory store, the first memory location and a second memory location respectively associated with a first device profile and a second device profile;

the first device profile representing a first set of attributes of the first memory location, and the second device profile representing a second set of attributes of the second memory location;

wherein the memory store is directly coupled to a memory controller, and wherein the memory controller performs a memory transaction;

wherein the host is directly coupled to the memory controller as the memory controller performs the memory transaction; and

using attributes from the first and second device profiles.

101. (new) The method of claim 100, wherein the memory controller comprises:

an interface controller;

a memory device interface directly coupled to the first memory location and to the second memory location and coupled to the interface controller;

an input/output (IO) device interface coupled to the interface controller and directly coupled to the host as the memory controller addresses the first memory location or the second memory location.

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EXAMINER	
EDOUARD, JEAN C	

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NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 12/876,113	Applicant(s) BRUCE ET AL.	
	Examiner JEAN EDOUARD	Art Unit 2133	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/17/2014*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-101* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-101* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *09/04/2010* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *11/17/2014, 11/04/2014*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

The present application is being examined under the pre-AIA first to invent provisions

Claims 1-101 are presented for examination.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/17/2014 has been entered.

4. Response to Arguments

5. Applicant's arguments filed on 10/07/2014 have been fully considered but they are not persuasive. Applicant argues on pages 2-3 in regards to claim 1, that "Falik does not all the limitation of claim 1"

Examiner respectfully disagrees. Estakhri is relied upon for that limitations. Falik teaches *first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and*

***second device profiles*. Col. 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.**

Claim Rejections - 35 USC § 112

4. The following is a quotation of 35 U.S.C. 112(b):
(b) CONCLUSION—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 100 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Regarding claim 100; the citation “the host” lacks antecedent basis.

Subsequently, claim 101 are also rejected because they inherit the deficiencies stated above.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1-14, 20, 21, 25, 45-60, 69-92 and 94-101** are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri et al. (U.S. Pub. 20110167204) in view of Falik et al. (US 8,200,879).

Claim 1 is taught by Estakri as:

A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising: addressing a first memory location in a first memory device in a memory store. Estakri fig. 3 mass storage device 302 contains a volatile memory 100 with multiple locations and a non-volatile memory 104 with multiple locations and paragraph [0039]-[0041] wherein memory location are being addressed.

said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Estakri paragraph [0038]-[0040] a first memory location and a second memory location associated with multiple device profile

Wherein said second memory location is in a second memory device in the memory store. Estakri fig. 1-2 and paragraph [0032], [0037]-[0038] shows non-volatile memory104 with multiple locations in the mass storage device 302. Wherein a memory read transaction or a memory write transaction is performed on at least one of the first memory location or second memory location. Estakri paragraph [0020], [0039]-[0040] shows memory read transaction is performed in the non-volatile memory 104 by controller 304.

wherein data is transferred to the first memory location or second memory location from a host for a memory write transaction. Estakri fig. 3 and paragraph [0036], [0041] shows data is transferred from the external signal system which is equivalent to a host to the volatile 100 and the non-volatile memory 104 via the controller and interfaces 140, 306 and 308 for a memory write transaction. wherein data is transferred from the first memory location or second memory location to the host for a memory read transaction. Estakri fig. 3 and paragraph [0039]-[0041] *shows data is transferred from the external signal system which is equivalent to a host to the volatile 100 and the non-volatile memory 104 via the controller and interfaces 140, 306 and 308 for a memory read transaction.*

Wherein the memory store is directly coupled to at least one memory bus and wherein the at least one memory bus is directly coupled to a controller, and wherein the controller performs the memory read transaction and memory write transaction on the memory store. Estakhri fig. 3 shows the volatile memory 100 connects to controller 304

via bus 140 and paragraph [0010], [0036], [0040] wherein controller 304 interacts in read and write transactions in the memory.

Wherein the host is directly coupled to the controller by a communication path as the controller performs the memory read transaction or memory write transaction; Estakhri fig. 3 shows the external digital signal 300 which is equivalent to host connects directly to controller 304 via interface 306 and 308 and the controller also connects to volatile memory 100 and nonvolatile memory 104 via interface 140 to perform read and write transaction.

Estakri does not explicitly teach Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location. Wherein the first device profile and second device profile are each stored in the memory store. And using attributes from said first and second device profiles.

However, Falik teaches Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Col. 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-

45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

Wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location. Column 20 line 49 through column 21 line 15 shows that the section properties register stores values representing the section of the flash device, and that there is a section properties register for each section of the flash device.

Wherein the first device profile and second device profile are each stored in the memory store. Column 18 lines 53-64 show that the control, status and capabilities registers 12 and 112 are located on the flash device, and can be kept in the flash device's own memory.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Falik does not explicitly teach Wherein the memory store is directly coupled to at least one memory bus and wherein the at least one memory bus is directly coupled to a controller, and wherein the controller performs the memory read transaction and memory write transaction on the memory store. Wherein the host is directly coupled to the controller by a communication path as the controller performs the memory read transaction or memory write transaction.

It would have been obvious to one of an ordinary skill in the art at the time the invention was made to have incorporated the teaching of *Said first device profile representing a first set of attributes of said first memory location, and said second*

device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location. Wherein the first device profile and second device profile are each stored in the memory store. And using attributes from said first and second device profiles as suggested in Falik into Estakri's system because both of the system are addressing the need of managing and controlling the access to memory locations, and by incorporating the teaching of Falik into Estakhri would perform the benefit of avoiding program buffer being full by using the double buffer empty status bit in the device status and control register (Falik paragraph [0134].

Claim 2 is taught by Estakhri and Falik as:

The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device. Col. 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 3 is taught by Estakhri and Falik as:

The method of claim 1, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when

different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

And said addressing said first memory location is made in response to a first memory transaction request. Column 18 lines 24-34 shows that applications on the main die 100 issue read and program commands.

And further including addressing said second memory location. Figure 6 shows that both sections can be addressed.

Claim 4 is taught by Estakhri and Falik as:

The method of claim 1, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 5 is taught by Estakhri and Falik as:

The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 6 is taught by Estakhri and Falik as:

The method of claim 5, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 7 is taught by Estakhri and Falik as:

The method of claim 5, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 8 is taught by Estakhri and Falik as:

The method of claim 5, wherein said shared attributes include a memory device type attribute. Column 20 lines 30-36 shows that the registers can indicate if the device is self-timed type flash memory or not.

Claim 9 is taught by Estakhri and Falik as:

The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 10 is taught by Estakhri and Falik as:

The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 11 is taught by Estakhri and Falik as:

The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 12 is taught by Estakhri and Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 13 is taught by Estakhri and Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of attributes that differs in value from a second page size attribute from said second set of attributes. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 14 is taught by Estakhri and Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes. Column 19 lines 56-59 shows that the Bus Widths

Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 20 is taught by Estakhri and Falik as:

The method of claim 2, further including: using an address corresponding to a memory location from said first memory device and transferring a first data set. Column 16 lines 53-62 shows that an address and data are sent for a programming operation.

And using an address corresponding to a memory location from said second memory device and transferring a second data set. Column 14 lines 51-65 show that the standard address space is mapped to the logical sections into which the arrays are grouped, showing that the second memory device is accessed using an address corresponding to the second memory device.

Claim 21 is taught by Estakhri and Falik as:

The method of claim 20, wherein: said first set of attributes includes a first page size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

And said first data set includes a first data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

And if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size. Column 27 lines 9-24 shows that when the number of bytes to be transferred to the FD have been transferred, the transfer process ends by setting the bus to a HiZ state.

Claim 25 is taught by Estakhri and Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size attribute of said first memory device. As discussed at column 27 lines 33-60, the program buffer corresponds to the batch size, which is the amount of data which can be programmed into the flash array at once.

Claim 45 is taught by Falik as:

A memory controller for performing memory transactions, said memory controller comprising: a means for addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that

arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Wherein said means for addressing includes an interface controller means for processing memory transaction requests. Figure 4B, flash bus transactions state machine 116.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Col. 20 line 49 through col. 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And said means for addressing uses attributes from said first and second device profiles. Col. 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Falik does not explicitly teach Said means for addressing is directly coupled to the first memory location and second memory location; Said means for addressing is directly coupled to a host as said means for addressing addresses the first memory location or second memory location.

However, Estakhri teaches Said means for addressing is directly coupled to the first memory location and second memory location; estakri fig. 3 paragraph [0033],

[0039], [0054] shows the controller 304, for addressing is connected directly to volatile memory 100 and nonvolatile memory 104 via interface 140.

Said means for addressing is directly coupled to a host as said means for addressing addresses the first memory location or second memory location. Estakhri fig. 3 and paragraph [0033], [0040]-[0041] shows controller 304 connects directly to external digital signal (host) via interface 306 and 308 wherein volatile memory 100 and nonvolatile memory 104 are addressable by the controller via interface 140.

It would have been obvious to one of an ordinary skill in the art at the time the invention was made to have incorporated the teaching of *Said means for addressing is directly coupled to the first memory location and second memory location*; Said means for addressing is directly coupled to a host as said means for addressing addresses the first memory location or second memory location as suggested in Estakhri into Talik's system because both of the system are addressing the need of managing and controlling the access to memory locations, and by incorporating the teaching of Talik into Estakhri would improve the performance system (Estakhri et al, paragraph [0051]]).

Claim 46 is taught by Estakhri and Falik as:

The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second

memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 47 is taught by Estakhri and Falik as:

The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 48 is taught by Estakhri and Falik as:

The memory controller of claim 46, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said use of said attributes from said first and second device profiles by said means for addressing includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 49 is taught by Estakhri and Falik as:

The memory controller of claim 46, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 50 is taught by Estakhri and Falik as:

The memory controller of claim 45, wherein said means for addressing further includes a means for addressing said second memory location. Figure 6 shows that both sections can be addressed.

Claim 51 is taught by Estakhri and Falik as:

The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 52 is taught by Estakhri and Falik as:

The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths

Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 53 is taught by Estakhri and Falik as:

The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 54 is taught by Estakhri and Falik as:

The memory controller of claim 51, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 55 is taught by Estakhri and Falik as:

The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 56 is taught by Estakhri and Falik as:

The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 57 is taught by Estakhri and Falik as:

The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 58 is taught by Estakhri and Falik as:

The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

Claim 59 is taught by Estakri as:

A memory store. Estakri fig. 3 storage device 302.

teaches wherein the memory device interface is directly coupled to the memory store. See Estakhri fig. 3 controller 304 connected directly memory 100 via interface 140.

Estakri does not explicitly teach *a memory controller comprising: an interface controller coupled to a memory device interface and an input/output (IO) device interface. Said interface controller disposed to perform a memory transaction by addressing a first memory location in a first memory device in the memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Said addressing of said first memory location includes using said attributes from said first device profile.*

However, Falik teaches a memory controller comprising: an interface controller coupled to a memory device interface and an input/output (IO) device interface. Figure 4B shows interface controller 110 connected to bus 90 and internal bus 140.

Wherein the memory device interface is directly coupled to the memory store. See Estakhri fig. 3 controller 304 connected directly memory 100 via interface 140.

Said interface controller disposed to perform a memory transaction by addressing a first memory location in a first memory device in the memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory

location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

Said addressing of said first memory location includes using said attributes from said first device profile. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

It would have been obvious to one of an ordinary skill in the art at the time the invention was made to have incorporated the teaching of *a memory controller comprising: an interface controller coupled to a memory device interface and an input/output (IO) device interface. Said interface controller disposed to perform a memory transaction by addressing a first memory location in a first memory device in*

the memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Said addressing of said first memory location includes using said attributes from said first device profile as suggested in Falik into Estakhri's system because both of the system are addressing the need of managing and controlling the access to memory locations, and by incorporating the teaching of Talik into Estakhri would perform the benefit of reducing overall time for finishing a flash programming task (Falik paragraph [0082]).

Claim 60 is taught by Estakhri and Falik as:

The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile. Figure 6 shows that both sections can be addressed.

Claim 69 is taught by Estakhri and Falik as:

The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

Claim 70 is taught by Estakhri and Falik as:

The memory controller of claim 59, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 71 is taught by Estakhri and Falik as:

The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 72 is taught by Estakhri and Falik as:

The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that

Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 73 is taught by Estakhri and Falik as:

The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 74 is taught by Estakhri and Falik as:

The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 75 is taught by Estakhri and Falik as:

The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type.

Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 76 is taught by Estakhri and Falik as:

The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 77 is taught by Estakhri and Falik as:

The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 78 is taught by Estakhri and Falik as:

The memory controller of claim 71, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 79 is taught by Estakhri and Falik as:

The memory controller of claim 71, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 80 is taught by Estakhri as:

a memory controller directly coupled to and disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile. Estakhri fig. 1, 3 and paragraph [0033], [0036], [0054] shows controller 304 connects directly to memory 100 for addressing and wherein memory 100 contains multiple locations.

Said memory controller directly coupled to a host as said memory controller addresses the first memory location or second memory location. Estakhri fig. 3 and paragraph [0033], [0041], [0094] shows controller 304 directly coupled to memory 100 for addressing and wherein memory 100 has multiple locations.

Estakhri does not explicitly teach *an electronic storage device, comprising: Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Said memory controller using attributes from said first and second device profiles*.

However, Falik teaches an electronic storage device, comprising: Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

Said memory controller using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

It would have been obvious to one of an ordinary skill in the art at the time the invention was made to have incorporated the teaching of *an electronic storage device, comprising: Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Said memory controller using attributes from said first and second device profiles* as suggested in Falik into Estakhri's system because both of the system are addressing the need of managing and controlling the access to memory locations, and by incorporating the teaching of Talik into Estakhri would perform the benefit of reducing overall time for finishing a flash programming task (Falik paragraph [0082]).

Claim 81 is taught by Estakhri and Falik as:

The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command. Column 9 lines 5-18 shows that the interface performs appropriate requests for erasure.

Claim 82 is taught by Estakhri and Falik as:

The electronic storage device of claim 80, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 83 is taught by Estakhri and Falik as:

The electronic storage device of claim 80, said memory controller further disposed to: perform a write operation on said first memory device, if a memory transaction request is associated with a write request. Column 16 lines 53-64 shows that write transactions may be performed.

Perform a read operation on said first memory device, if said memory transaction request is associated with a read request. Column 16 lines 53-64 shows that read transactions may be performed.

And wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using said second device profile in response to receiving a second memory transaction request. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used for accesses to the groups of memory arrays.

Claim 84 is taught by Estakhri and Falik as:

The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 85 is taught by Estakhri and Falik as:

The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 86 is taught by Estakhri and Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that

Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 87 is taught by Estakhri and Falik as:

The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 88 is taught by Estakhri and Falik as:

The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 89 is taught by Estakhri and Falik as:

The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

Claim 90 is taught by Estakhri and Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 91 is taught by Estakhri and Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 92 is taught by Estakhri and Falik as:

The electronic storage device of claim 84, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 94 is taught by Estakhri and Falik as:

The method of claim 1, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 95 is taught by Estakhri and Falik as:

The memory controller of claim 45, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 96 is taught by Estakhri and Falik as:

The memory controller of claim 59, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 97 is taught by Estakhri and Falik as:

The electronic device of claim 80, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 98 is taught by Estakhri as:

teaches a memory controller directly coupled to and disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile. Estakhri fig. 1, 3 and paragraph [0033], [0036], [0054] shows controller 304 connects directly to memory 100 for addressing and wherein memory 100 contains multiple locations.

Wherein the memory controller directly coupled to a host as said memory controller addresses the first memory location or second memory location. Estakhri fig. 3 and paragraph [0033], [0041], [0094] shows controller 304 directly coupled to memory 100 for addressing and wherein memory 100 has multiple locations.

Estakhri does not explicitly teach an electronic storage device, comprising:

The first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device

profiles. And wherein Said memory controller using attributes from said first and second device profiles.

However, Falik teaches an electronic storage device, comprising:

The first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And wherein Said memory controller using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

It would have been obvious to one of an ordinary skill in the art at the time the invention was made to have incorporated the teaching of *a memory controller directly coupled to and disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile. Said memory controller directly coupled to a host as said memory controller addresses the first memory location or second memory location* as suggested in Estakhri into Falik's system because both of the system are addressing the need of managing and controlling the access to memory locations, and by incorporating the

teaching of Falik into Estakhri would perform the benefit of reducing overall time for finishing a flash programming task (Falik paragraph [0082]).

Claim 99 is taught by Estakhri and Falik as:

The electronic device of claim 98, wherein the memory controller comprises: an interface controller. Falik interface controller 110;

A memory controller comprising: an interface controller coupled to a memory device interface and an input/output (IO) device interface. Figure 4B shows interface controller 110 connected to bus 90 and internal bus 140.

A memory store. Falik fig. 4A flash memory 70, wherein *the memory device interface is directly coupled to the memory store*. Falik fig. 4A-4B bus 90 interacts with flash memory 70

Said interface controller disposed to perform a memory transaction by addressing a first memory location in a first memory device in the memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having

identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

Said addressing of said first memory location includes using said attributes from said first device profile. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 100 is taught by Estakhri as:

A method of performing memory transactions, the method comprising: addressing a first memory location in a first memory device in a memory store. Estakri fig. 3 mass storage device 302 contains a volatile memory 100 with multiple locations and a non-volatile memory 104 with multiple locations and paragraph [0039]-[0041] wherein memory location are being addressed.

Said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Estakri paragraph [0038]-[0040] a first memory location and a second memory location associated with multiple device profile.

Wherein the host is directly coupled to a memory controller performs a memory r transaction. Estakhri fig. 3 and [0039]-[0041] shows the external digital signal 300 which is equivalent to host connects directly to controller 304 via interface 306 and 308 and the controller also connects to volatile memory 100 and nonvolatile memory 104 via interface 140 to perform transactions.

Estakhri does not explicitly teach *the first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location. And using attributes from said first and second device profiles*.

However, Falik teaches the first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location. Col. 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

It would have been obvious to one of an ordinary skill in the art at the time the invention was made to have incorporated the teaching of *the first device profile*

representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location. And using attributes from said first and second device profiles as suggested in Falik into Estakhri's system because both of the system are addressing the need of managing and controlling the access to memory locations, and by incorporating the teaching of Talik into Estakhri would perform the benefit of reducing overall time for finishing a flash programming task (Falik paragraph [0082]).

Claim 101 is taught by Falik and Estakhri as:

The method of claim 100, wherein the memory controller comprises: an interface controller. Falik fig. 4B interface controller 110.

A memory device interface directly coupled to the first memory location and the second memory location and coupled to the interface controller. Falik fig. 4A-4B Bus interface 90 connects to interface controller 110 and the memory.

An input/output (IO) device interface coupled to the interface coupled to the interface controller. Falik fig. 4B bus 90 connects to interface controller 110; and directly coupled to the host as the memory controller addresses the first memory location or the second memory location. Estakhri fig. 3 and paragraph [0033], [0036], [0041] wherein bus 90 will connect directly to the external digital system (host) as controller 304 addresses.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 15, 18, and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri et al. (U.S. 20110167204) in view of Falik et al. (US 8,200,879) in further view of Nangle (US 7,330,954).

Claim 15 is taught by Estakhri and Falik as:

The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device. Column 21 lines 7-10 shows that the information can correspond to a flash device FD.

Although Falik column 21 lines 7-10 shows that other memory technologies such as SRAM may be used, it does not expressly teach that the second memory device attribute corresponds to a DRAM device interface.

With respect to claim 15, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 lines 51-67 shows that the memory devices may be flash memory and DRAM.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include flash memory and DRAM in the system of Falik.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 15**.

Claim 18 is taught by Estakhri and Falik as shown supra with respect to claim 8.

Falik does not expressly teach that said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

With respect to claim 18, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 line 51 through column 5 line 4 shows that the memory devices may be volatile memory that have a battery backup.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a volatile memory disposed to receive backup power from a portable power source.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 18**.

Claim 19 is taught by Estakhri and Falik as shown supra with respect to claim 8.

Estakhri and Falik does not expressly teach that said first memory device type attribute corresponds to a NAND flash memory device and said second memory device type attribute corresponds to a NOR flash memory device.

With respect to claim 19, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 lines 51-65 shows that the memory devices may be NAND or NOR type flash memories.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a volatile memory disposed to receive backup power from a portable power source.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 19**.

9. **Claims 16, 17, 22-24, and 93** are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri et al. (U.S. 20110167204) in view of Falik et al. (US 8,200,879) in further view of Sinclair et al. (US 2006/0184723).

Claim 16 if taught by Estakhri and Falik as shown supra with respect to claim 2.

Although Falik teaches that the width of the array is the minimum programming size of the array at column 20 lines 62-65, and that the width of the array is stored at column 20 lines 49-52, Falik does not expressly teach that a first and second partial page size attribute is stored and used.

With respect to claim 16, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claims 16 and 17**.

Claim 17 is taught by Estakhri, Falik and Sinclair as:

The method of claim 16: said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute. Sinclair paragraph 0168 shows that in a flash memory that supports partial page programming, when sufficient data is transferred to the buffer, it is programmed to the page. Falik column 14 lines 51-60 and figure 3 shows that the first memory device group can be accessed.

And further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute. Sinclair paragraph 0168 shows that in a flash memory that supports partial page programming, when sufficient data is transferred to the buffer, it is programmed to the page. Falik column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

Claim 22 is taught by Estakhri and Falik as:

The method of claim 20, wherein: said second set of attributes includes a second page size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

And said second data set includes a second data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

And if said second data set size is greater than said second page size attribute, said transferring said second data set includes: performing a set of write operations on said second memory device that includes using a second transfer size equal to said second page size attribute. Column 16 lines 48-52 shows that program buffer 19 may be a double buffer, allowing the programming of one chunk of data while another chunk of data is received. As discussed at column 27 lines 33-60, the program buffer corresponds to the batch size, which is the amount of data which can be programmed into the flash array at once.

Falik does not expressly teach that the transaction is made using a transfer size equal to the page size until a remaining portion of said second data set that has not yet been written to said second device is less than said second page size attribute and using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

With respect to claim 22, Sinclair teaches Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times. As discussed in paragraph 0168, when the end of the data group is received in the buffer and it is smaller than a full page of data, a partial page programming operation may be performed.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 22**.

Claim 23 is taught by Estakhri and Falik as:

The method of claim 20, wherein: said first set of attributes includes a page size attribute and a block size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Said first data set includes a first data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

If said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes: performing a set of write operations on

said first memory device that includes using a second transfer size equal to said page size attribute […]. Column 27 lines 14-24 shows that bytes of data are sent until all the bytes have been sent.

Falik does not expressly teach that the transaction is made using a transfer size equal to the page size until a remaining portion of said first data set that has not yet been written to said first device is less than said first page size attribute and using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

With respect to claim 23, Sinclair teaches Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times. As discussed in paragraph 0168, when the end of the data group is received in the buffer and it is smaller than a full page of data, a partial page programming operation may be performed.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 23**.

Claim 24 is taught by Estakhri and Falik as shown supra with respect to claim 1, and further as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes: performing respective write operations on said first and second memory devices by at least using a transfer size at least equal to a […] *page size attribute from said first set of attributes*. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations.

And performing at least one write operation on said second memory device by at least using a transfer size at least equal to a […] *page size attribute value from said second set of attributes*. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations. Column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

And said attribute difference includes different attribute values of said first and second […] *page size attributes*. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Although Estakhri and Falik teaches storing a page size attribute, it does not expressly teach storing a partial page size attribute.

With respect to claim 24, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 24**.

Claim 93 is taught by Estakhri and Falik as shown supra with respect to claim 80, and further as:

The electronic storage device of claim 80, wherein said memory controller is further adapted to: use a first partial page size attribute by performing a write operation on said first memory device and using a transfer size at least equal to said partial page size attribute. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations.

And use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute. Column 16 lines 53-62 shows that programming is carried out

in a block to be stored in sequentially increasing address locations. Column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

Although Estakhri and Falik teach storing a page size attribute, it does not expressly teach storing a partial page size attribute.

With respect to claim 93, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 93**.

10. **Claims 26-28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri et al. (U.S. 20110167204) in view of Falik et al. (US 8,200,879) in further view of Lakhani et al. (US 6,961,805).

Claim 26 is taught by Estakhri and Falik as shown supra with respect to claim 1.

Falik further teaches, at column 20 lines 60-65, that Page Size Block1 stores the size of the minimal segment of a flash array erasable upon a single erase command. Additionally, column 16 line 53 through column 17 line 24 shows that data can be written to a block of addresses by designating the starting address and performing a series of program continue operations.

Estakhri and Falik does not expressly teach using the block size attribute in performing a write operation that uses a transfer size that corresponds to the block size.

With respect to claim 26, Lakhani teaches, at column 18 lines 19-46, that predecoder 50 asserts sets of multiblock selection bits in response to control bits from the controller, which allows a designated number of blocks to be selected for writing at the same time.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to perform a write operation that uses a transfer size equal to the a block size attribute value that corresponds to a block size attribute of the first memory device.

The motivation for doing so would have been to reduce the time used to test the memory cells of the block, Lakhani column 8 lines 21-32.

Therefore, it would have been obvious to combine Lakhani with Falik to obtain the invention as specified in **claims 26 and 27**.

Claim 27 is taught by Lakhani as:

The method of claim 26, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value. Column 13 lines 25-38 shows that a plurality of blocks can be selected at the same time.

Claim 28 is taught by Falik as shown supra with respect to claim 2.

Falik further teaches, at column 20 lines 60-65, that Page Size Block1 stores the size of the minimal segment of a flash array erasable upon a single erase command. Additionally, column 16 line 53 through column 17 line 24 shows that data can be written to a block of addresses by designating the starting address and performing a series of program continue operations.

Falik does not expressly teach using the block size attribute in performing a write operation that uses a transfer size that is equal to a multiple of the block size.

With respect to claim 28, Lakhani teaches, at column 18 lines 19-46, that predecoder 50 asserts sets of multiblock selection bits in response to control bits from the controller, which allows a designated number of blocks to be selected for writing at the same time.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to perform a write operation that uses a transfer size equal to the a block size attribute value that corresponds to a block size attribute of the first memory device.

The motivation for doing so would have been to reduce the time used to test the memory cells of the block, Lakhani column 8 lines 21-32.

Therefore, it would have been obvious to combine Lakhani with Falik to obtain the invention as specified in **claim 28**.

11. **Claims 29-44** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Rubinstein et al. (US 5,913,215).

Claim 29 is taught by Falik as:

Said method comprising: addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Wherein said second memory location is in a second memory device in the memory store. Column 6 lines 11-16 shows that the different parameters

correspond to different memory arrays. Accordingly, the address corresponding to a different section may be in a second memory device.

Said first device profile representing a first set of attributes of said first memory device, and said second device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

Wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location. Column 20 line 49 through column 21 line 15 shows that the section properties register stores values representing the section of the flash device, and that there is a section properties register for each section of the flash device.

Wherein the memory store is coupled by at least one memory bus to a controller, and wherein the controller performs the memory transactions on the memory store. Figure 1 shows that main die interface controller connects to the flash die via bus 90, as discussed at column 10 lines 5-15. Column 27 lines 8-32 shows that the MD sends commands to the FD.

Wherein the first device profile and second device profile are each stored in the memory store. Column 18 lines 53-64 show that the control, status and

capabilities registers 12 and 112 are located on the flash device, and can be kept in the flash device's own memory.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Falik does not expressly teach that the methods may be implemented using a non-transitory computer readable medium comprising computer executable instructions.

With respect to claim 29, Rubinstein teaches at column 10, lines 3-15, that computer methods may be performed either by a series of instructions, or by specific hardware components that contain hard-wired logic for performing the method, or by any combination of the two.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a computer readable medium comprising computer executable instructions.

The rationale for doing so would have been that it is a known technique to implement methods in computer systems using a non-transitory computer readable medium comprising computer executable instructions.

Therefore, it would have been obvious to combine Rubinstein with Falik to obtain the invention as recited in **claims 29-44**.

Claim 30 is taught by Falik as:

The computer readable medium of claim 29, wherein: said first memory location is part of a memory space associated with a first memory device, said second memory

location is part of a memory space associated with a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

And said first and second memory devices comprise at least a portion of a memory store. Figure 3 shows that the address space is mapped to the memory devices.

Claim 31 is taught by Falik as:

The computer readable medium of claim 29, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of a first memory device and a block size value of a second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 32 is taught by Falik as:

The computer readable medium of claim 30, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 33 is taught by Falik as:

The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 34 is taught by Falik as:

The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

Claim 35 is taught by Falik as:

The computer readable medium of claim 29, wherein said addressing further includes: said first and second device profiles having at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40

shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 36 is taught by Falik as:

The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 37 is taught by Falik as:

The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 38 is taught by Falik as:

The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 39 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 40 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 41 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 42 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size,

block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 43 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 44 is taught by Falik as:

The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

12. **Claims 61 and 64-68** are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri et al. (U.S. 20110167204) in view of Falik et al. (US 8,200,879) in view of Chin et al. (US 2001/0010066).

Claim 61 is taught by Estakhri and Falik as shown supra with respect to claim 59.

Falik further teaches:

The memory controller of claim 59, wherein said interface controller includes: A first memory bus controller coupled to said control device and said memory device interface. Falik figure 4b item 116.

And an IO bus controller coupled to said IO device interface and said control device. Falik figure 4b item 117.

With respect to claim 61, Chin figure 2 teaches a bridge unit 104, which connects to a CPU bus 108 and a memory bus 110, including control logic 242, shown in paragraph 0037 to direct the operations of the queue storage elements through a network of control signals. Figure 2 also illustrates a data path between the CPU bus 108 and memory bus 110 through queues 250 and 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a main control device coupled to the memory device interface and data path as taught by Chin in the interface controller of Falik.

The motivation for doing so would have been to provide a means to manage the transfer of data through the interface performed by the system of Falik, see Chin paragraph 0037.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as specified in **claim 61**.

Claim 64 is taught by Estakhri and Falik as shown supra with respect to claim 59.

Falik does not expressly teach that a buffer is a FIFO or that a data path includes a plurality of queue slots.

With respect to claim 64, Chin teaches: *Further including a buffer comprising a FIFO*. Paragraph 0052 shows that queue 250 is a FIFO.

And a data path that includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory. Figure 2 also shows read queue 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a FIFO and a data path including a plurality of queue slots in the system of Falik.

The motivation for doing so would have been to provide an interface that provides all devices in a computer system fair access to memory, Chin paragraph 0012.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as recited in **claim 64**.

Claim 65 is taught by Estakhri and Falik as shown supra with respect to claim 59.

Falik does not expressly teach that a data path includes a buffer having a plurality of queue slots.

With respect to claim 65, Chin teaches: *The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots*.

Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a FIFO and a data path including a plurality of queue slots in the system of Falik.

The motivation for doing so would have been to provide an interface that provides all devices in a computer system fair access to memory, Chin paragraph 0012.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as recited in **claims 65-67**.

Claim 66 is taught by Chin as:

The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a plurality of queue slots that buffer data from said IO device interface to said memory device interface. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory.

Claim 67 is taught by Chin as:

The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from said memory device interface to said IO device interface. Figure 2 also shows read queue 252.

Claim 68 is taught by Estakhri and Falik as shown supra with respect to claim 1.

Falik further teaches a memory bus controller, figure 4b item 116, coupled to bus 90.

Falik does not expressly teach that the memory bus controller is coupled to a main control device.

With respect to claim 68, Chin teaches:

A second memory bus controller coupled to said main control device and said memory device interface. Figure 2 teaches a bridge unit 104, which connects to a CPU bus 108 and a memory bus 110, including control logic 242, shown in paragraph 0037 to direct the operations of the queue storage elements through a network of control signals. Figure 2 also illustrates a data path between the CPU bus 108 and memory bus 110 through queues 250 and 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a main control device coupled to the memory device interface and data path as taught by Chin in the interface controller of Falik.

The motivation for doing so would have been to provide a means to manage the transfer of data through the interface performed by the system of Falik, see Chin paragraph 0037.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as specified in **claim 68**.

13. **Claims 62 and 63** are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri et al. (U.S. 20110167204) in view of Falik et al. (US 8,200,879) in view of Chin et al. (US 2001/0010066) as applied to claim 61 above, and further in view of Tsuruta (US 2007/0174506).

Claim 62 is taught by the combination of Falik and Chin as shown supra with respect to claim 61.

The combination of Falik and Chin does not expressly teach that the IO bus controller is disposed to respond to said memory transaction request by acknowledging said request and providing status to said main control device.

With respect to claim 62, Tsuruta teaches:

Wherein said IO bus controller is disposed to respond to a memory transaction request by acknowledging said request and providing status to said main control device. Paragraph 0183 shows that in response to a read req from the CPU, MEM-DMAC 232 issues a read ack signal. Paragraph 0186 shows that after the read operation is performed, a sequencer in the memory controller 231 issues ack to a sequencer in the MEM-DMAC 232.

At the time of the invention, it would have been obvious to use the acknowledgement system of Tsuruta in the combination of Falik and Chin.

The motivation for doing so would have been to provide coordination between the CPU interface and the read/write queues to perform the requested memory operations.

Therefore, it would have been obvious to combine Tsuruta with Falik and Chin to obtain the invention as specified in **claims 62 and 63**.

Claim 63 is taught by Chin as:

The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction. Paragraph 0052 shows that control logic provides control signals to the input and output selectors 351 and 353 that determine the values of the enable and select signals in response to a memory request from the CPU.

Coordinates the operation of said memory device interface. Paragraph 0052 shows that the data and address of each request is sent to the memory controller 200.

And manages the transfer of memory transaction data between said IO device interface and said memory device interface through a data path. Paragraph 0052 shows that data is transferred through the queue 250.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Solan et al. (U.S Patent 5850566) discloses Method for Storing Multiple Files without Header Information and for Each Storage Medium Maintaining a Separate Stored Index Including Header Information for Each File and Methods for its use.

Kern al. (U.S Publication 2009/0158085) discloses Power Safe Translation Table Operation in Flash Memory and methods for its use.

Que (U.S Publication 2009/0094411) discloses Nand Flash Controller and Data Exchange Method between Nand Flash Memory and Nand Flash Controller.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEAN EDOUARD whose telephone number is (571)270-1683. The examiner can normally be reached on 8:30-4:30

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rutz Jared can be reached on5712725535. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JEAN EDOUARD/
Examiner, Art Unit 2133

/Aimee Li/
Supervisory Patent Examiner, Art Unit 2137

REMARKS/ARGUMENTS

Claim 100 is amended to remove the lack of antecedent basis. Accordingly, the rejection to claim 100 is no longer applicable. Claim 100 is otherwise allowable.

Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-101 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Estakhri et al. (US 2011/0167204) in view of Falik et al. (US 8,200,879).

Applicants respectfully disagree with thi.s rejection, but to expedite allowance of the claims, Applicants amend independent claim 1 herein to recite various features as shown above. Support for the amendment in claim 1 is found in the filed application in, for example, Figures 1, 2A, 2B, 2C, 4, 5, and 6 and accompanying text.

The Office admits that Estakri does not disclose first and second device profiles as required in claim 1. Falik discloses reading tables in the registers 12 of the flash interface controller 10 (Falik: Figure 4A). However, Falik fails to disclose, fails to teach, and fails to suggest various features such as "wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type; said performing the memory transaction further comprising identifying command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device", "after identifying the command details, obtaining the first set of attributes", and "selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes" as required in claim 1. Accordingly, Estakhri and Falik do not disclose all the limitations of claim 1. Since Estakhri and Falik, considered individually or in combination do not disclose and do not teach and do not suggest all the limitations of claim 1, claim 1 is not rendered obvious by the cited references. Claim 1 is otherwise allowable.

Claims 2-14, 20, 21, and 25 depend from allowable claim 1; as such, they are also allowable for at least the same reasons as claim 1.

The withdrawal of the rejections to claims 1-14, 20, 21, 25 and 94 is respectfully requested.

Independent claims 29, 45, 59, 80, 98, and 100 recite at least some limitations similar to that as claim 1. Although claims 29, 45, 59, 80, 98, and 100 are different, Applicants respectfully argue that in this case the above arguments regarding the patentability of claim 1 apply with equal force with respect to claims 29, 45, 59, 80, 98, and 100. Since Estakhri and Falik and other cited references, considered individually or in combination, do not disclose, do not teach, and do not suggest all the limitations of claims 29, 45, 59, 80, 98, and 100, claims 29, 45, 59, 80, 98, and 100 are not rendered obvious by the cited references. Claims 29, 45, 59, 80, 98, and 100 are otherwise allowable.

Various dependent claims depend from the above allowable claims; as such, the dependent claims are also allowable for at least the same reasons as their respective independent claims.

Applicant hereby petitions and requests for a two-months extension of time to file this response. A payment of for the two-months extension of time petition is being included herewith in the signed and dated form PTO-2038.

Claims 1-101 herein are allowable, and a timely Notice of Allowance is respectfully requested.

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, the Applicants are not conceding in this application that previously pending claims are unpatentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application.

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (805) 569-1600.

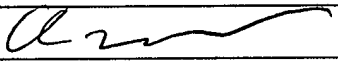
Date: May 5, 2015

Respectfully submitted,



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Please send correspondence to:
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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising:

performing a memory transaction comprising addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile, wherein said second memory location is in a second memory device in the memory store, wherein a memory read transaction or a memory write transaction is performed on at least one of the first memory location or second memory location, wherein data is transferred to the first memory location or second memory location from a host for a memory write transaction, wherein data is transferred from the first memory location or second memory location to the host for a memory read transaction;

wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type;

said performing the memory transaction further comprising identifying command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;

after identifying the command details, obtaining the first set of attributes;

wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location;

wherein the memory store is directly coupled to at least one memory bus and wherein the at least one memory bus is directly coupled to a controller, and wherein the controller performs the memory read transaction and memory write transaction on the memory store;

wherein the host is directly coupled to the controller by a communication path as the controller performs the memory read transaction or memory write transaction;

wherein the first device profile and second device profile are each stored in the memory store; and

using attributes from said first and second device profiles; and

selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

2. (original) The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device.

3. (original) The method of claim 1, wherein said difference between said first and second device profiles includes different attributes; and said addressing said first memory location is made in response to a first memory transaction request; and

further including addressing said second memory location.

4. (original) The method of claim 1, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes.

5. (original) The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

6. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute values.

7. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute types.

8. (original) The method of claim 5, wherein said shared attributes include a memory device type attribute.

9. (original) The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

10. (original) The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

11. (original) The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

12. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

13. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of attributes that differs in value from a second page size attribute from said second set of attributes.

14. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes.

15. (original) The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device, and said second memory device interface attribute corresponds to a DRAM device interface.

16. (original) The method of claim 2, wherein said using attributes from said first and second device profile further includes using a first partial page size attribute from said first set of attributes that differs in value from a second partial page size attribute from said second set of attributes.

17. (original) The method of claim 16:

said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute; and

further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute.

18. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

19. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a NAND flash memory device and said second memory device type attribute corresponds to a NOR flash memory device.

20. (original) The method of claim 2, further including:

using an address corresponding to a memory location from said first memory device and transferring a first data set, and

using an address corresponding to a memory location from said second memory device and transferring a second data set.

21. (original) The method of claim 20, wherein:

said first set of attributes includes a first page size attribute, and said first data set includes a first data set size; and

if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size.

22. (original) The method of claim 20, wherein:

said second set of attributes includes a second page size attribute, and said second data set includes a second data set size; and

if said second data set size is greater than said second page size attribute, said transferring said second data set includes:

performing a set of write operations on said second memory device that includes using a second transfer size equal to said second page size attribute until a remaining portion of said second data set that has not yet been written to said second device is less than said second page size attribute, and

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

23. (previously presented) The method of claim 20, wherein:

said first set of attributes includes a page size attribute and a block size attribute;

said first data set includes a first data set size;

if said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes:

performing a set of write operations on said first memory device that includes using a second transfer size equal to said page size attribute until a remaining portion of said first data set that has not yet been written to said first device is less than said page size attribute,

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

24. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes:

performing respective write operations on said first and second memory devices by at least using a transfer size at least equal to a partial page size attribute from said first set of attributes and performing at least one write operation on said second memory device by at least using a transfer size at least equal to a partial page size attribute value from said second set of attributes; and

said attribute difference includes different attribute values of said first and second partial page size attributes.

25. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size attribute of said first memory device.

26. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a block size attribute value that corresponds to a block size attribute of said first memory device.

27. (original) The method of claim 26, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

28. (original) The method of claim 2, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

29. (currently amended) A non-transitory computer readable medium comprising computer executable instructions adapted to cause a method of performing memory transactions on a first memory location and a second memory location, said method comprising:

performing a memory transaction comprising addressing a first memory location, said first memory location and a

second memory location are respectively associated with a first device profile and a second device profile;

wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type;

said performing the memory transaction further comprising identifying command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;

said first device profile representing a first set of attributes of said first memory device, and said second device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles;

after identifying the command details, obtaining the first set of attributes; and

using attributes from said first and second device profiles; and

selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

30. (original) The computer readable medium of claim 29, wherein:

said first memory location is part of a memory space associated with a first memory device;

said second memory location is part of a memory space associated with a second memory device; and

said first and second memory devices comprise at least a portion of a memory store.

31. (previously presented) The computer readable medium of claim 29, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of a first memory device and a block size value of a second memory device.

32. (previously presented) The computer readable medium of claim 30, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

33. (original) The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

34. (original) The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes.

35. (previously presented) The computer readable medium of claim 29, wherein said addressing further includes:

said first and second device profiles having at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

36. (original) The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

37. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values.

38. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types.

39. (original) The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute.

40. (original) The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

41. (original) The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

42. (original) The computer readable medium of claim 36, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

43. (original) The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes.

44. (original) The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device.

45. (currently amended) A memory controller for performing memory transactions, said memory controller comprising:

means for performing a memory transaction comprising a means for addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile;

said means for addressing is directly coupled to the first memory location and second memory location;

wherein said means for addressing includes an interface controller means for processing memory transaction requests;

said means for addressing is directly coupled to a host as said means for addressing addresses the first memory location or second memory location;

wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type;

said performing the memory transaction further comprising identifying command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;

said means for addressing obtains the first set of attributes after identifying the command details; and

said means for addressing uses attributes from said first and second device profiles and selects a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

46. (original) The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

47. (original) The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

48. (original) The memory controller of claim 46, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said use of said attributes from said first and second device profiles by said means for addressing includes using said different attribute qualifiers for said shared attributes.

49. (original) The memory controller of claim 46, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

50. (previously presented) The memory controller of claim 45, wherein said means for addressing further includes a means for addressing said second memory location.

51. (original) The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

52. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values.

53. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types.

54. (original) The memory controller of claim 51, wherein said shared attributes include a memory device type attribute.

55. (original) The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

56. (original) The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

57. (original) The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

58. (original) The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device.

59. (currently amended) A memory controller comprising:

an interface controller coupled to a memory device interface and an input/output (IO) device interface;

a memory store;

wherein the memory device interface is directly coupled to the memory store;

said interface controller disposed to perform a memory transaction by addressing a first memory location in the memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile;

wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said

data type comprises one of a random data type or a sequential data type;

said interface controller identifies command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;

said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;

said interface controller obtaining the first set of attributes after identifying the command details; and

said addressing of said first memory location includes using said attributes from said first device profile; and

said addressing of said first memory location includes selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

60. (original) The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile.

61. (previously presented) The memory controller of claim 59, wherein said interface controller includes:

a main control device coupled to said memory device interface and to a data path;

a first memory bus controller coupled to said control device and said memory device interface; and

an IO bus controller coupled to said IO device interface and said control device.

62. (previously presented) The memory controller of claim 61, wherein said IO bus controller is disposed to respond to a memory transaction request by acknowledging said request and providing status to said main control device.

63. (original) The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction, coordinates the operation of said memory device interface, and manages the transfer of memory transaction data between said IO device

interface and said memory device interface through a data path.

64. (previously presented) The memory controller of claim 59, further including a buffer comprising a FIFO and a data path that includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface.

65. (original) The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots.

66. (original) The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a plurality of queue slots that buffer data from said IO device interface to said memory device interface.

67. (original) The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from said memory device interface to said IO device interface.

68. (previously presented) The memory controller of claim 59, further including a second memory bus controller coupled to a main control device and said memory device interface.

69. (original) The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes.

70. (original) The memory controller of claim 59, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

71. (original) The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

72. (original) The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute.

73. (original) The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values.

74. (original) The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values.

75. (original) The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type.

76. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values.

77. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types.

78. (original) The memory controller of claim 71, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

79. (original) The memory controller of claim 71, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

80. (currently amended) An electronic storage device, comprising:

a memory controller directly coupled to and disposed to address a first memory location and a second memory

location which are respectively associated with a first device profile and a second device profile;

said memory controller directly coupled to a host as said memory controller addresses the first memory location or second memory location;

wherein said first device profile is optimal for a data type subject to a memory transaction, wherein said data type comprises one of a random data type or a sequential data type;

said memory controller identifies command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;

said memory controller obtaining the first set of attributes after identifying the command details; and

said memory controller using attributes from said first and second device profiles; and

said memory controller selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

81. (original) The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

82. (original) The electronic storage device of claim 80, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

83. (previously presented) The electronic storage device of claim 80, said memory controller further disposed to:

perform a write operation on said first memory device, if a memory transaction request is associated with a write request;

perform a read operation on said first memory device, if said memory transaction request is associated with a read request; and

wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using said second device profile in response to receiving a second memory transaction request.

84. (original) The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

85. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values.

86. (original) The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute.

87. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types.

88. (original) The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said shared attributes.

89. (original) The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device.

90. (original) The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

91. (original) The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

92. (original) The electronic storage device of claim 84, wherein said shared attributes includes any one of the

following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

93. (original) The electronic storage device of claim 80, wherein said memory controller is further adapted to:

use a first partial page size attribute by performing a write operation on said first memory device and using a transfer size at least equal to said partial page size attribute; and

use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute.

94. (previously presented) The method of claim 1, wherein the first memory location and the second memory location are addressable memory locations.

95. (previously presented) The memory controller of claim 45, wherein the first memory location and the second memory location are addressable memory locations.

96. (previously presented) The memory controller of claim 59, wherein the first memory location and the second memory location are addressable memory locations.

97. (previously presented) The electronic device of claim 80, wherein the first memory location and the second memory location are addressable memory locations.

98. (previously presented) An electronic storage device, comprising: a memory controller directly coupled to and disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile;

wherein the memory controller is directly coupled to a host as the memory controller addresses the first memory location or the second memory location;

wherein said first device profile is optimal for a data type subject to a memory transaction, wherein said data type comprises one of a random data type or a sequential data type;

said memory controller identifies command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;

the first device profile representing a first set of attributes of the first memory location, and the second device profile representing a second set of attributes of the second memory location;

said memory controller obtaining the first set of attributes after identifying the command details; and

wherein said memory controller uses attributes from the first and second device profiles;

wherein said memory controller selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

99. (previously presented) The electronic devices of claim 98, wherein the memory controller comprises:

an interface controller;

a memory device interface directly coupled to the first memory location and to the second memory location and coupled to the interface controller;

an input/output (IO) device interface coupled to the interface controller and directly coupled to the host as the memory controller addresses the first memory location or the second memory location.

100. (currently amended) A method for performing memory transactions, the method comprising:

performing a memory transaction comprising addressing a first memory location in a first memory device in a memory store, the first memory location and a second memory location respectively associated with a first device profile and a second device profile;

wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type;

said performing the memory transaction further comprising identifying command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;

the first device profile representing a first set of attributes of the first memory location, and the second device profile representing a second set of attributes of the second memory location;

after identifying the command details, obtaining the first set of attributes;

wherein the memory store is directly coupled to a memory controller, and wherein the memory controller performs a memory transaction;

wherein [[the]] a host is directly coupled to the memory controller as the memory controller performs the memory transaction; and

using attributes from the first and second device profiles; and

selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

101. (previously presented) The method of claim 100, wherein the memory controller comprises:

an interface controller;

a memory device interface directly coupled to the first memory location and to the second memory location and coupled to the interface controller;

an input/output (IO) device interface coupled to the interface controller and directly coupled to the host as the memory controller addresses the first memory location or the second memory location.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

64180 7590 06/22/2015

URIARTE LAW
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EXAMINER
EDOUARD, JEAN C

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/22/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/876,113	09/04/2010	Ricardo H. BRUCE	6005.042	1607

TITLE OF INVENTION: MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	09/22/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

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(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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nonprovisional	SMALL	$480	$0	$0	$480	09/22/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
EDOUARD, JEAN C	2133	711-103000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

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Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

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- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
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EXAMINER	
EDOUARD, JEAN C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/22/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 12/876,113	Applicant(s) BRUCE ET AL.	
	Examiner JEAN EDOUARD	Art Unit 2133	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *05/08/2015*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-101*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 11/17/2014, 02/05/2014
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/JARED RUTZ/
Supervisory Patent Examiner, Art Unit 2133

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Response to Amendment

The amendments filed on 05/08/2015, have been and made of record. In response to the most recent office action, dated 12/05/2014:

Claims 1-101 have been considered.

Reasons for Allowance

Claims 1-101are allowed.

The prior art does not teach or fairly suggest:

Claim 1 recites the limitations " Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; after identifying the command details, obtaining the first set of attributes; wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location; Wherein the first device profile and second device profile are each stored in the memory store; and using attributes from said first and second device profiles; and selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes".

Claim 29 recites the limitations " Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; after identifying the command details, obtaining the first set of attributes; and using attributes from said first and second device profiles; and selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attribute".

Claim 45 recites the limitations " Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles Said means for addressing obtains the first set of attributes after identifying the command details; and said means for addressing uses attributes from said first and second device profiles and selects a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes".

Claim 59 recites the limitations " said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; said interface controller obtaining the first set of attributes after identifying the command details; and said addressing of said first memory location includes using said attributes from said first device profile; and said addressing of said first memory location includes

selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

Claim 80 recites the limitations " said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; said memory controller obtaining the first set of attributes after identifying the command details; and said memory controller using attributes from said first and second device profiles; and said memory controller selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes".

Claim 98 recites the limitations "the first device profile representing a first set of attributes of the first memory location, and the second device profile representing a second set of attributes of the second memory location; said memory controller obtaining the first set of attributes after identifying the command details; and wherein said memory controller uses attributes from the first and second device profiles, wherein said memory controller selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes".

Claim 100 recites the limitations "the first device profile representing a first set of attributes of the first memory location, and the second device profile representing a second set of attributes of the second memory location; after identifying the command details, obtaining the first set of attributes; memory transaction; and using attributes from the first and second device profiles; and selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes".

Said limitations are taught by the specification as originally filed at least at paragraphs {0015]-[0019 and [0033].

Claims 2-28, 30-44, 46-59, 60-80, 99 and 101 depend from claims 1, 29, 45, 59, 80, 98 and 100 and are considered allowable for at least the same reasons as claims 1, 29, 45, 59, 80, 98 and 100.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEAN EDOUARD whose telephone number is (571)270-1683. The examiner can normally be reached on 8:30 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jared Rutz can be reached on 5712725535. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JEAN EDOUARD/
Examiner, Art Unit 2133

/JARED RUTZ/
Supervisory Patent Examiner, Art Unit 2133