

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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KIOXIA AMERICA, INC. and  
KIOXIA CORPORATION,  
Petitioners,

v.

BiTMICRO, LLC,  
Patent Owner.

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Case IPR2023-00741  
Patent 9,135,190

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**PATENT OWNER'S PRELIMINARY RESPONSE**

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**Rules**

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Pursuant to 37 C.F.R. § 42.107, Patent Owner BiTMICRO, LLC (“BiTMICRO” or “Patent Owner”) files this preliminary response to the Petition, setting forth reasons why the Petition for *inter partes* review (“IPR”) of claims 1, 5-6, 29, 36-37, 45, 51-52, 59, 71, 76, 80, 84-85, and 98 of U.S. Patent No. 9,135,190 (the “’190 Patent”), as requested by Kioxia America, Inc. and Kioxia Corporation (“Petitioners”), should be denied.<sup>1</sup> As discussed below, none of the asserted references in the Petition discloses every claimed feature of the challenged claims, and each ground presented by Petitioners is deficient. The Petition should be denied.

## I. INTRODUCTION

The ’190 Patent discloses a multi-profile memory controller “that can operate with memory locations, memory devices, or both which are associated with different memory attributes, different attribute qualifiers, or the like,” while improving on shortcomings of prior memory controllers. ’190 Pat., Abst. As the ’190 Patent discloses, “[m]ulti-profile memory controllers have been traditionally designed to operate with memory stores or modules that comprise of memory devices which use the *same* memory device characteristics, such as block size.” ’190 Pat., 1:20-24 (emphasis added). For example, the ’190 Patent describes a

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<sup>1</sup> By submitting this Preliminary Response, no waiver of any argument is intended by Patent Owner. Patent Owner will have a right to file a complete response to the Petition, should the Board institute *inter partes* review. 37 C.F.R. § 42.120(a).

legacy multi-profile memory controller specifically designed to operate with memory devices that use flash memory cells having “relatively large block sizes.”

’190 Pat., 1:24-27. While relatively large block sizes pose some advantages for the memory density and cost efficiency of a device, the ’190 Patent also explains some associated disadvantages, including “higher read-modify-write cycle latency, higher random memory access latency and lower random IOPS (input/output operations per second).” ’190 Pat., 1:31-43.

The ’190 Patent’s invention “pertains to a multi-profile memory controller and related methods and systems that can operate with memory locations, memory devices, or both which are associated with different memory attributes, different attribute qualifiers, or the like, while minimizing or avoiding some or all of the disadvantages of the prior art.” ’190 Pat., 1:52-60. To further explain these features, the ’190 Patent discloses an exemplary storage device 15 having a multi-profile memory controller 2 and a memory store 4. ’190 Pat., Fig. 1. The memory store 4 includes a first memory device 10 having a first memory location 9, and a second memory device 12 having a second memory location 11. *Id.* These features are shown in FIG. 1, reproduced below:

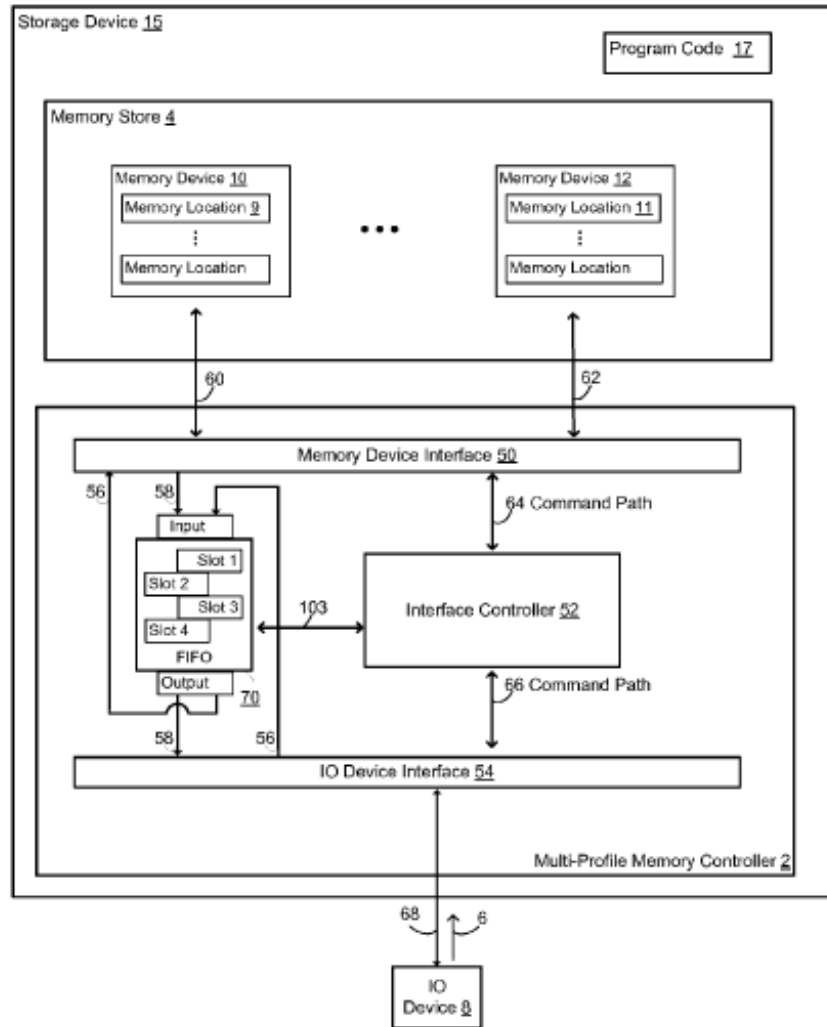


**FIG. 1**

Each memory location may have a set of memory attributes, with an attribute defined in the '190 Patent as “a characteristic of a memory location that is related to accessing or addressing the memory location.” '190 Pat., 2:65-3:2. Attributes may be represented in a device profile 14, such as shown in FIG. 2A.

|                             |                           |
|-----------------------------|---------------------------|
| Page Size <u>16</u>         | (# of pages)              |
| Block Size <u>18</u>        | (# of blocks)             |
| Memory Protocol <u>20</u>   | (Protocol Type Supported) |
| Mem. Dev. Type <u>22</u>    | (Mem. Type)               |
| Partial Page Size <u>23</u> | (# of pages)              |

**FIG. 2A**

As described in the '190 Patent, a device profile may include attributes including page size 16, block size 18, memory protocol 20, memory device type 22, and partial page size 23. The page size 16 “corresponds to an attribute value in bytes per page,” block size 18 “corresponds to an attribute value in pages per block,” memory protocol 20 “corresponds to a memory device specification or protocol supported by the memory device associated with the memory location,” memory device type 22 “corresponds to a memory device type of the memory device associated with the memory location,” and partial page size 23 “corresponds to an attribute value in bytes per partial page.” '190 Pat., 3:30-39.

In the memory store 4 of FIG. 1, first memory location 9 and second memory location 11 may have different attributes as reflected on their respective device profiles. As disclosed in FIG. 2B, first memory location 9 may have a device profile 26 with a page size of 1024 bytes per page, a block size of 2048

pages, and a partial page size of 512 bytes per partial page. This device profile 26 is shown in FIG. 2B:

26

|                   |           |            |
|-------------------|-----------|------------|
| Page Size         | <u>28</u> | 1024       |
| Block Size        | <u>30</u> | 2048       |
| Memory Protocol   | <u>32</u> | ONFi       |
| Mem. Dev. Type    | <u>34</u> | NAND Flash |
| Partial Page Size | <u>36</u> | 512        |

**FIG. 2B**

As disclosed in FIG. 2C, second memory location 11 may have a device profile 38 with a page size of 512 bytes per page, a block size of 8192 pages, and a partial page size of 256 bytes per partial page. This device profile 38 for second memory location 11 is shown in FIG. 2C:

38

|                   |           |            |
|-------------------|-----------|------------|
| Page Size         | <u>40</u> | 512        |
| Block Size        | <u>42</u> | 8192       |
| Memory Protocol   | <u>44</u> | ONFi       |
| Mem. Dev. Type    | <u>46</u> | NAND Flash |
| Partial Page Size | <u>48</u> | 256        |

**FIG. 2C**

As disclosed, multi-profile memory controller 2 serves as a memory controller for both the first memory location 9 and the second memory location 11,

which respectively have different page sizes, block sizes, and partial page sizes from each other.

Consistent with this disclosure, the challenged claims are directed generally to a solid-state storage device having a memory controller able to operate with memory devices with different attributes. This enables the memory controller to perform a variety of memory transactions that were previously not performed by a single memory controller. Claim 1’s “method of performing transactions on a set of memory locations” includes, in relevant part, the step of “selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.”<sup>2</sup> Independent claims 29, 45, 59, 80, and 98 each recite substantially similar features. For example, claim 98 is directed to an “electronic storage device,” and includes in relevant part “wherein said memory controller selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.”

Petitioners assert two comparable grounds against these challenged claims. In Ground 1, Petitioners contend that each of the challenged claims is obvious over

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<sup>2</sup> Claim 1 also recites that “each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location.”

the Cornwell<sup>3</sup> reference in view of a POSITA’s knowledge. Similarly, in Ground 2, Petitioners contend that each of the challenged claims is obvious over the Ware<sup>4</sup> reference in view of a POSITA’s knowledge.

However, in each ground, Petitioners fail to explain how Cornwell and Ware allegedly disclose every relied-upon feature of the challenged claims. In particular, Petitioners fail to explain how Cornwell and Ware allegedly disclose selecting a transfer size for a memory transaction as a function of the claimed factors in the challenged claims. Indeed, Petitioners fail to explain how the functions disclosed by Cornwell and Ware constitute a selection of transfer size. Rather, the Petition’s arguments amount to nothing more than a conclusory assertion that these features are disclosed, and the Declaration of Dr. Baker (Ex. 1003) offers no further analysis sufficient to support the challenges.

As such, each ground presented in the Petition is deficient, and the Petition should be denied without institution.

## **II. THE BOARD NEED NOT REACH ANY CLAIM CONSTRUCTION ISSUES TO DENY THE PETITION**

In the Petition, Petitioners submit proposed constructions for three terms appearing in claim 45: “means for performing a memory transaction,” “interface

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<sup>3</sup> U.S. Patent Application Publication No. 2007/0180186 (“Cornwell”).

<sup>4</sup> U.S. Patent No. 7,269,708 (“Ware”).

controller means for processing memory transaction requests,” and “means for addressing a first memory location.” Pet., 5-8. Without expressly agreeing to Petitioners’ proposed constructions, and without waiving its right to submit its proposed constructions in a Patent Owner Response, Patent Owner submits that the Board need not engage in any pre-institution claim construction of these terms from claim 45. For the reasons presented in Section III below, Petitioners’ grounds each include fundamental flaws and fail to establish the disclosure of every claimed element in each independent claim. These findings do not require the Board to conduct any construction of the above-identified terms of claim 45.

### **III. PETITIONER’S CHALLENGES FAIL ON THE MERITS**

#### **A. The Challenged Claims Require Selecting a Transfer Size for a Memory Transaction**

Claim 1’s “method of performing transactions on a set of memory locations” includes, in relevant part, the step of “selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.” This “selecting” step is identified by Petitioners as [Claim 1o] in the Petition. *See* Pet., ix. Independent claims 29, 45, 59, 80, and 98 each recite substantially similar features as charted and identified below.

| Claim number | Claimed feature and Petition's Identifier                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Claim 29     | <p>A non-transitory computer readable medium comprising computer executable instructions adapted to cause a method of performing memory transactions on a first memory location and a second memory location, said method comprising:</p> <p>...</p> <p>selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.</p> <p>([Claim 29g] per the Petition)</p> |
| Claim 45     | <p>A memory controller for performing memory transactions, said memory controller comprising:</p> <p>...</p> <p>and said means for addressing uses attributes from said first and second device profiles and selects a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.</p> <p>([Claim 45i] per the Petition)</p>                                              |
| Claim 59     | <p>A memory controller comprising:</p> <p>...</p> <p>said addressing of said first memory location includes selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.</p> <p>([Claim 59k] per the Petition)</p>                                                                                                                                             |
| Claim 80     | <p>An electronic storage device, comprising:</p> <p>...</p> <p>said memory controller selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.</p> <p>([Claim 80h] per the Petition)</p>                                                                                                                                                                   |

|          |                                                                                                                                                                                                                                                                                                                 |
|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Claim 98 | <p>An electronic storage device, comprising:</p> <p>...</p> <p>wherein said memory controller selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.</p> <p>([Claim 98h] per the Petition)</p> |
|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

Providing support for these claimed features, the ’190 Patent discloses that the “[m]ulti-profile memory controller 2 also determines the transfer sizes to use when causing a memory transaction to be performed on the target memory device.” ’190 Pat., 8:4-6. In an embodiment, “the transfer size selected is a function of the data size of the subject to memory transaction request 6, and the attributes in a device profile associated with a target memory location.” ’190 Pat., 8:39-42. The ’190 Patent discloses exemplary attributes, including “any combination of the following: the page size attribute, the block size attribute, and the partial page size attribute in device profile 26 of memory location 9 ... .” ’190 Pat., 8:42-47. Further discussion of the selection of transfer size is provided in the ’190 Patent. *See, e.g.*, ’190 Pat., 8:47-9:6.

As already introduced above, the ’190 Patent also discloses that the term “memory attribute” or “attribute” “is defined to include a characteristic of a memory location that is related to accessing or addressing the memory location.”

'190 Pat., 2:63-3:2. A device profile can include attributes of a memory location.

'190 Pat., 3:40-49.

**B. Cornwell Fails to Disclose any Selection of Transfer Size**

As introduced above, claim 1 recites, in relevant part, “selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.” Petitioners refer to this element as [Claim 1o], and assert that Cornwell teaches this claimed feature. Pet., ix, 27. Contrary to Petitioners' assertions, there is no basis for Petitioners to contend that this feature is disclosed or suggested in Cornwell.

In the challenge based on Cornwell, Petitioners point to “non-volatile memory devices 106” as the claimed “first memory location in a first memory device” and the “second memory location ... in a second memory device.” Pet., 13-17. Looking to [Claim 1d], Petitioners argue that “Cornwell discloses that a memory read or write transaction is performed on at least one memory location,” pointing to read or write operations performed by memory devices 106. Pet., 18. Petitioners then rely on Cornwell to disclose that “each device profile (device data 312) includes a variety of information ‘associated with attributes, properties or characteristics of the memory device ... .’” Pet., 22-23 (citing Cornwell, [0042]).

Focusing on [Claim 1o], Petitioners rely on Cornwell's Example Page Program Operation and argue that “Cornwell teaches that ‘the controller 308,

programs the page into the memory array 304 ... .” Pet., 27 (citing Cornwell, [0039]). Petitioners also assert that a page has a “page size.” Pet., 27 (citing Cornwell, ¶¶ [0042], [0048], [0050]). Based on these disclosures, and without identifying any selection of transfer size in Cornwell, Petitioners contend that “Cornwell therefore teaches selecting a transfer size for the memory transaction.” Pet., 27 (citing Ex. 1003, ¶ 151). Petitioners also assert that “page size” is a “function of device density ... and the IDE/ATA bus standard.” Pet., 27 (citing Cornwell, [0042]). Finally, without citing to any support from Cornwell and without explaining the basis for their assertion, Petitioners contend that “Cornwell also teaches that the transfer size is selected by the controller.” Pet., 27 (citing Ex. 1003, ¶¶ 153-55).

Notwithstanding Petitioners’ conclusions to the contrary, Petitioners fail to point to any “selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes” in Cornwell. Based on the disclosures cited to and discussed by Petitioners, Cornwell programs a page into the memory array without disclosing or suggesting any selecting step. According to Cornwell, “[d]uring a page program operation, the controller 308 receives a ‘page program’ command input from the I/O bus 110 ... and stores it in the command register 316.” Cornwell, [0039]. “Several bus cycles ... are then used to input a memory address into address

register 314.” *Id.* Then, “data stored in I/O buffers and latches 322 is loaded into the page buffer 306.” *Id.* The “controller 308 programs the page into the memory array 304 at the address stored in address register 314 ... .” *Id.* In this process, Cornwell teaches no selecting step associated with the page program operation.

Further, Petitioners incorrectly rely on Cornwell’s paragraph [0042] for disclosures relevant to [Claim 1o]. As Cornwell discloses, a “page size (1k, 2K, etc.)” can be included in the chip data 312 for a memory device 106. Cornwell, [0042]. However, this does not mean that there is a selection of page size. Rather, as Cornwell describes it, the page size in the chip data 312 is fixed as an attribute, and is not selected as part of the transfer size for the memory transaction.

Similarly, Cornwell’s paragraphs [0048]-[0050] disclose the policy of “block defining,” which involves tailoring “the size of files such that the average file size is proportional to the block size.” However, tailoring a file size is also not sufficient to disclose selecting a transfer size. Rather, as disclosed in Cornwell, setting a file system structure and file size based on an average file size simply defines the relationship of an average file size in relation to a block size. Importantly, this process disclosed in Cornwell makes no mention of how to adapt to varying block sizes, i.e. different attributes between a first memory device and a second memory device. Petitioners’ discussion of [Claim 1o] completely misses the point of the ’190 Patent’s invention, which includes the step of selecting a

transfer size precisely because not every memory device needs to possess identical attributes. Indeed, Petitioners chose not to discuss these Cornwell paragraphs [0048]-[0050] in its incorrect assertion that Cornwell discloses the features of [Claim 1o]. This confirms that Petitioners could not tie Cornwell’s disclosure of “block defining” to the claimed feature of “selecting a transfer size.”

Dr. Baker’s Declaration offers no further support for why Cornwell allegedly discloses this claimed feature, and simply parrots the conclusory and unsupported assertions from the Petition. *See* Ex. 1003, ¶¶ 151-155. These conclusory statements should be disregarded. *See* 37 C.F.R. § 42.65(a); *Samsung Electronics Co., Ltd. v. Rightquestion, LLC*, IPR2022-00251, Paper 17 at 25 (PTAB June 9, 2022) (declining to credit testimony where “declarant makes these same statements verbatim, without more, and with no additional citations to evidence”).

Finally, just as the Petition fails to substantiate its reliance on Cornwell to disclose [Claim 1o], it fails to substantiate its assertion that Cornwell discloses the corresponding features of claims 29 ([claim 29g]), 45 ([claim 45i]), 59 ([claim 59k]), 80 ([claim 80h]), and 98 ([claim 98h]). Rather than address these other features, Petitioners simply refer back to their incorrect analysis for [claim 1o]. *See* Pet., 30, 38, 45, 51, 52-53. For the same reasons presented above for [Claim 1o], each challenge of these independent claims fails.

For these reasons, the challenged independent claims have not been shown to be obvious over Cornwell, which fails to disclose or suggest at least these claimed features.

**C. Like Cornwell, Ware Fails to Disclose any Selection of Transfer Size Based on the Claimed Features**

Ground 2, based on Ware, includes similar failures as Ground 1. Petitioners introduce Ware as disclosing a “memory controller for a ‘non-homogenous memory system’ in which the main memory is comprised of two or more memory ‘portions’ or device types, such as DRAM and Flash.” Pet., 11 (quoting Ware, 2:18-25, 3:57-4:11). According to Petitioners, DRAM and Flash have different attributes, and Ware allegedly “utilizes these different attributes to distribute data among the different memory devices ‘in a manner designed to provide fast access to the data and programs that are most frequently used.’” Pet., 11 (quoting Ware, 3:64-67). But like Cornwell, Ware also fails to disclose every claimed element, including [Claim 1o]—“selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes”—as well as the corresponding claimed elements of the other challenged independent claims, claims 29 ([claim 29g]), 45 ([claim 45i]), 59 ([claim 59k]), 80 ([claim 80h]), and 98 ([claim 98h]).

As introduced above, Petitioners rely on Ware to disclose non-homogeneous main memory 101 having DRAM 104 and Flash 106. Pet., 55. Addressing [Claim

1n] (“using attributes from said first and second device profiles”), Petitioners contend that “Ware also teaches a device granularity attribute, noting that different devices have ‘different granularity for read and write operations.’” Pet., 73 (citing Ware, 5:65-66). Petitioners are misquoting Ware, however, because Ware does not teach whether DRAM 104 and Flash 106 have different granularities. Instead, this quotation in Ware is describing the granularity for read and write operations of a NOR Flash memory device only. Ware’s 5:65-66 discloses that “NOR Flash memory devices typically have different granularity for read and write operations.” Ware then clarifies that it is *only* describing the differences in granularity based on whether the operation performed on a NOR Flash memory device is a “read” or a “write” operation. Ware teaches that “the minimum unit for reading data from Flash memory may be a word (e.g., 16 bits) while the minimum unit for writing data to Flash memory is typically significantly larger than the minimum unit for reading, and is called either a block or a group of memory cells.” Ware, 5:66-6:4. Thus, these statements only compare the granularity for a read vs. a write operation for a Flash memory. Contrary to Petitioners’ erroneous assertion, these statements do not teach whether DRAM 104 and Flash 106 have different granularities from each other.

Addressing [Claim 1o] next, without ever having established whether DRAM 104 and Flash 106 have different granularities from each other, Petitioners

assert that a “POSITA would have understood that granularity is the minimum unit for read and write operations, thus resulting in *the need* to use the device granularity attribute in a memory transaction.” Pet., 73 (emphasis added). Petitioners then contend that because “Ware teaches that different devices have different granularity, [there is a] need to select a transfer size for read/write transactions.” Pet., 73 (citing Pet., § IX.B.1.o., directed to [Claim 1n]). This contention fails for numerous reasons.

First, as already noted, Petitioners fail to point to any disclosure in Ware to establish “different devices hav[ing] different granularity.” Therefore, the fundamental premise underlying Petitioners’ conclusion is not established. Second, simply having a granularity characteristic for a device does not mean that Ware inherently or necessarily requires a selection of transfer size in order to perform a read/write transaction. For example, a default transfer size that is larger than the granularity does not create a “need to select a transfer size for read/write transactions,” as Petitioners incorrectly contend. See Pet., 73. Petitioners’ analysis is clearly tainted by improper hindsight in an effort to read the claimed elements into a prior art reference that does not disclose them. Further, Dr. Baker’s declaration repeats the erroneous misinterpretation of Ware presented in the Petition (see Ex. 1003, ¶463), and similarly fails to establish any “need to select a transfer size (granularity) for the memory transaction.” Ex. 1003, ¶463.

Also addressing [Claim 1o], Petitioners state that “flash memory can be written in pages, ... and that a page is the number of bits in a row of data in flash memory that can be transferred during a memory transaction, and that page size is an attribute.” Pet., 73. Even if these statements are accepted as true, Petitioners point to no disclosure of any selection of transfer size or even a page selection in Ware. Rather, like in the first Ground based on Cornwell, Petitioners treat the existence of a page size as either tantamount to the claimed “selecting,” or requiring a “selecting step” without ever pointing to a disclosure of any selecting of transfer size. Simply put, Petitioners have no basis to allege that Ware expressly or even inherently discloses this feature of claim 1, and cannot prevail in their second Ground.

Finally, just as the Petition fails to substantiate its reliance on Ware to disclose [Claim 1o], it fails to substantiate its assertion that Ware discloses the corresponding features of claims 29 ([29g]), 45 ([45i])<sup>5</sup>, 59 ([59k]), 80 ([80h]), and 98 ([98h]). Once again, Petitioners refer back to their incorrect analysis for [Claim

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<sup>5</sup> Addressing claim 45 ([45i]), Petitioners also argue that “decoding bits of a physical address to ‘determine whether the first or second portion of main memory will receive a memory access transaction’” discloses the claimed “selects a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.” Pet., 85-86 (citing Ware, 7:46-54). Not so. Petitioners fail to explain how decoding an address for a memory operation discloses or suggests this claimed feature [Claim 45i]. This incomplete argument also fails.

1o]. *See* Pet., 77, 85-86, 93, 99, 101. For the same reasons presented above for [claim 1o], each challenge of these independent claims fails.

For these reasons, the challenged independent claims have not been shown to be obvious over Ware, which fails to disclose or suggest at least these claimed features.

#### **IV. CONCLUSION**

For the reasons presented above, no *inter partes* review should be instituted.

Dated: July 26, 2023

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**CERTIFICATE OF WORD COUNT**

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word-processing system's word count, the brief contains 3,870 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(a).

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**CERTIFICATE OF SERVICE**

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