

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KIOXIA AMERICA, INC. and KIOXIA CORPORATION,
Petitioners,

v.

BiTMICRO LLC,
Patent Owner.

IPR2023-00741
Patent 9,135,190 B1

Before KEN B. BARRETT, TERRENCE W. McMILLIN, and
KEVIN C. TROCK, *Administrative Patent Judges*.

McMILLIN, *Administrative Patent Judge*.

DECISION

Denying Institution of *Inter Partes* Review
35 U.S.C. § 314, 37 C.F.R. § 42.4

I. INTRODUCTION

KIOXIA Corporation and KIOXIA America, Inc. (“Petitioners”) filed a Petition to institute an *inter partes* review of claims 1, 5, 6, 29, 36, 37, 45, 51, 52, 59, 71, 76, 80, 84, 85, and 98 (“the challenged claims”) of U.S. Patent No. 9,135,190 B1 (Ex. 1001, “the ’190 patent”) pursuant to 35 U.S.C. § 311 *et seq.* Paper 3 (“Petition” or “Pet.”). BiTMICRO, LLC (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Preliminary Response” or “Prelim. Resp.”).

We have authority under 35 U.S.C. § 314, which provides that an *inter partes* review may not be instituted unless the information presented in the Petition and the Preliminary Response shows that “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). For the reasons discussed below, we deny institution.

A. Related Matters

The parties identify the following related proceedings: *Certain Solid State Storage Drives, Stacked Electronics Components, and Products Containing Same*, Inv. No. 337-TA-1097 (Int’l Trade Comm’n); *SK Hynix Inc., et al. v. BiTMICRO, LLC*, Case No. 3:18-cv-03505 (N.D. Cal.); *Samsung Semiconductor, Inc. et al. v. BiTMICRO, LLC et al.*, Case No. 3:18-cv-03502 (N.D. Cal.); *BiTMICRO LLC v. KIOXIA Am. Inc., et al.*, Case No. 6:22-cv-00331 (W.D. Tex. 2022); *BiTMICRO LLC v. Intel Corp.*, Case No. 5:23-cv-00625 (N.D. Cal.). Pet. 103; Paper 5, 2–3.

Patent Owner further identifies the following *inter partes* review petition challenging the ’190 patent: *Intel Corporation v. BiTMICRO, LLC*, IPR2023-00780. Paper 5, 3.

Although not identified by either party, there is an additional *inter partes* review challenging the '190 patent: *Intel Corporation v. BiTMICRO, LLC*, IPR2023-00779.¹

B. The '190 Patent

The '190 patent is titled “Multi-Profile Memory Controller for Computing Devices.” Ex. 1001, code (54). The '190 patent is directed to a “a multi-profile memory controller . . . that can operate with memory locations, memory devices, or both which are associated with different memory attributes, different attribute qualifiers, or the like.” *Id.* at code (57).

Figure 1 of the '190 patent, reproduced below, “illustrates a multi-profile memory controller.” *Id.* at 1:64.

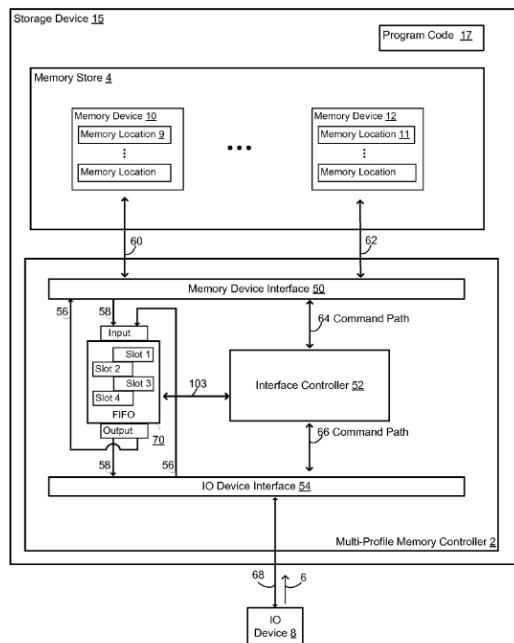


FIG. 1

¹ The parties are reminded of the obligation to update their mandatory notices within 21 days of a change of information including identifying related matters. 37 C.F.R. § 42.8.

Figure 1 depicts an exemplary storage device 15 having a multi-profile memory controller 2 and a memory store 4 that includes a first memory device 10 having a first memory location 9 and a second memory device 12 having a second memory location 11. *Id.* at 2:50–65, 3:7–8. Each memory location is “associated with a set of at least one memory attribute,” which “is defined to include a characteristic of a memory location that is related to accessing or addressing the memory location.” *Id.* at 2:63–3:2. “[E]xamples of an attribute of a memory location may include . . . the block size used by the memory device, the page size used by the memory device, the memory protocol or specification supported by the memory device, and the partial page size used by the memory device.” *Id.* at 3:8–13.

Figure 2A of the ’190 patent, reproduced below, illustrates a device profile for use with the multi-profile memory controller. *Id.* at 2:1–3.

24		25	14
Page Size	16	(# of pages)	
Block Size	18	(# of blocks)	
Memory Protocol	20	(Protocol Type Supported)	
Mem. Dev. Type	22	(Mem. Type)	
Partial Page Size	23	(# of pages)	

FIG. 2A

Figure 2A depicts a device profile 14, which “may be used to represent at least one attribute 24 of a memory location, and each attribute respectively corresponds to an attribute qualifier 25.” *Id.* at 3:22–25. “These attributes include a page size 16, a block size 18, a memory protocol 20 supported by the memory device in which the memory location is addressable, a memory device type 22, and a partial page size 23,” and the “[a]ttribute qualifier 25 is in the form of a value or type.” *Id.* at 3:25–30.

The ’190 patent discloses that the “[m]ulti-profile memory controller 2 can perform memory transactions using different device profiles,” and

“memory locations 9 and 11 [can] have different device profiles.” *Id.* at 3:61–64.

C. Challenged Claims

Petitioners challenge claims 1, 5, 6, 29, 36, 37, 45, 51, 52, 59, 71, 76, 80, 84, 85, and 98 of the '190 patent. Pet. 1. Challenged claims 1, 29, 45, 59, 80, and 98 are independent claims. Ex. 1001, 12:57–13:42, 15:59–16:21, 17:19–53, 18:34–65, 20:14–44, 21:49–22:11. Claim 1 recites:

1. A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising:
performing a memory transaction comprising addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile, wherein said second memory location is in a second memory device in the memory store, wherein a memory read transaction or a memory write transaction is performed on at least one of the first memory location or second memory location, wherein data is transferred to the first memory location or second memory location from a host for a memory write transaction, wherein data is transferred from the first memory location or second memory location to the host for a memory read transaction;
wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type;
said performing the memory transaction further comprising identifying command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;
said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second

memory location, and a difference exists between said first and second device profiles;
after identifying the command details, obtaining the first set of attributes;
wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location;
wherein the memory store is directly coupled to at least one memory bus and wherein the at least one memory bus is directly coupled to a controller, and wherein the controller performs the memory read transaction and memory write transaction on the memory store;
wherein the host is directly coupled to the controller by a communication path as the controller performs the memory read transaction or memory write transaction;
wherein the first device profile and second device profile are each stored in the memory store; and
using attributes from said first and second device profiles; and
selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

Id. at 12:57–13:42 (emphasis added to disputed limitation).

D. The Asserted Grounds

Petitioners challenge claims 1, 5, 6, 29, 36, 37, 45, 51, 52, 59, 71, 76, 80, 84, 85, and 98 of the '190 patent based on the grounds set forth in the table below.

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 5, 6, 29, 36, 37, 45, 51, 52, 59, 71, 76, 80, 84, 85, 98	103(a)	Cornwell ²
1, 5, 6, 29, 36, 37, 45, 51, 52, 59, 71, 76, 80, 84, 85, 98	103(a)	Ware ³

² US 2007/0180186 A1, published Aug. 2, 2007 (Ex. 1005).

³ US 7,269,708 B2, issued Sep. 11, 2007 (Ex. 1006).

II. ANALYSIS

A. *Legal Standards*

A patent claim is unpatentable as obvious if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of obviousness or non-obviousness.⁴ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). Petitioners cannot satisfy their burden of proving obviousness by employing “mere conclusory statements.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

B. *Level of Ordinary Skill in the Art*

With regard to the level of ordinary skill in the art, Petitioners contend “a person of ordinary skill in the art . . . would have had at least a Bachelor’s degree in electrical or computer engineering, or a similar field, and at least

⁴ The parties do not submit objective evidence of obviousness or non-obviousness. *See generally* Pet.; Prelim. Resp.

two years of work experience in the computer memory or data storage industry.” Pet. 4–5 (citing Ex. 1003 ¶¶ 66–69). Petitioners further contend “less formal education” can be “substituted . . . with additional relevant work experience, and vice versa.” *Id.* at 5 (citing Ex. 1003 ¶¶ 66–69). Patent Owner does not address the level of ordinary skill in the art. *See generally* Prelim. Resp.

For purposes of this Decision, we adopt Petitioners’ definition of the level of ordinary skill in the art because it is consistent with the ’190 patent and the asserted prior art.

C. Claim Construction

In an *inter partes* review for a petition filed on or after November 13, 2018, “[claims] of a patent . . . shall be construed using the same claim construction standard that would be used to construe the [claims] in a civil action under 35 U.S.C. § 282(b), including construing the [claims] in accordance with the ordinary and customary meaning of such claims as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b) (2018); *see also Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–14 (Fed. Cir. 2005). “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). There is a “heavy presumption,” however, that a claim term carries its ordinary and customary meaning. *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002) (citation omitted).

The Petition submits constructions for certain purported means-plus-function terms in claim 45. Pet. 5–8. Petitioners construe the claimed “means for performing a memory transaction” to have a recited function of “performing a memory transaction” and a structure “as a ‘multi-profile memory controller or similar structure configured to perform a memory transaction.’” *Id.* at 6. Petitioners construe the claimed “interface controller means for processing memory transaction requests” to have a recited function of “processing memory transaction requests” and a structure “as an ‘interface controller or similar structure configured to process memory transaction requests.’” *Id.* at 7. Petitioners construe the claimed “means for addressing a first memory location” to have a recited function of “addressing a first memory location” and a structure “as a ‘a memory device interface, a host interface, an interface controller or similar structure configured to process memory transaction requests, and associated communication pathways.’” *Id.* Patent Owner states that “the Board need not engage in any pre-institution claim construction of these terms from claim 45.” Prelim. Resp. 8.

We determine that no terms require express construction for purposes of this Decision. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Ltd.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). In this Decision, we give the claim terms their ordinary and customary meanings.

D. Summaries of Cited Art

In the challenges to the claims, Petitioners rely on Cornwell (Ex. 1005) and Ware (Ex. 1006). Summaries of these references are provided below.

1. Cornwell

Cornwell is titled “Non-Volatile Memory Management.” Ex. 1005, code (54). Cornwell discloses a memory management system comprising “a memory controller [that] is operatively coupled to the one or more non-volatile memory devices and configurable to access the one or more non-volatile memory devices in accordance with a memory management policy.” *Id.* ¶ 7. The “device data,” used to identify each memory device and its manufacturer, “can include an electronic signature or serial number that includes a manufacturer code and/or device code,” “device type,” “device density,” “page size,” “spare area size,” “sequential access time,” “block size,” “bus width,” “bad block identification, and any other information that is associated with attributes, properties or characteristics of the memory device.” *Id.* ¶ 42.

Figure 1 of Cornwell, reproduced below, illustrates an exemplary non-volatile memory management system. *Id.* ¶ 11.

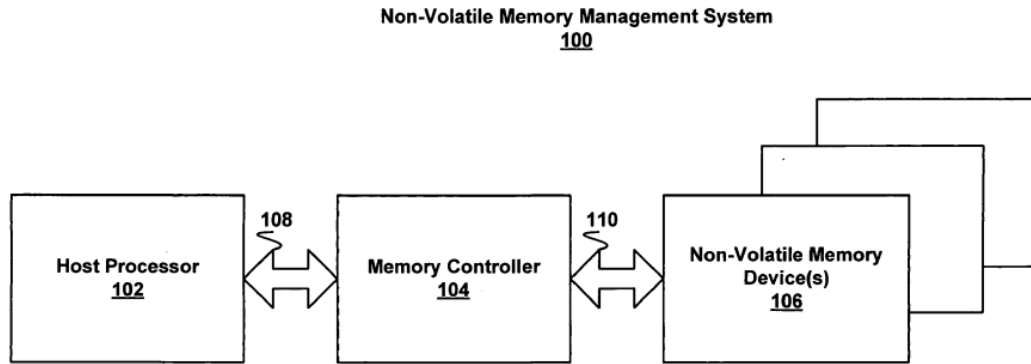


Figure 1

Figure 1 depicts a memory controller 104 coupled to one or more non-volatile memory devices 106.

Figure 3 of Cornwell, reproduced below, illustrates a non-volatile memory device. *Id.* ¶ 13.

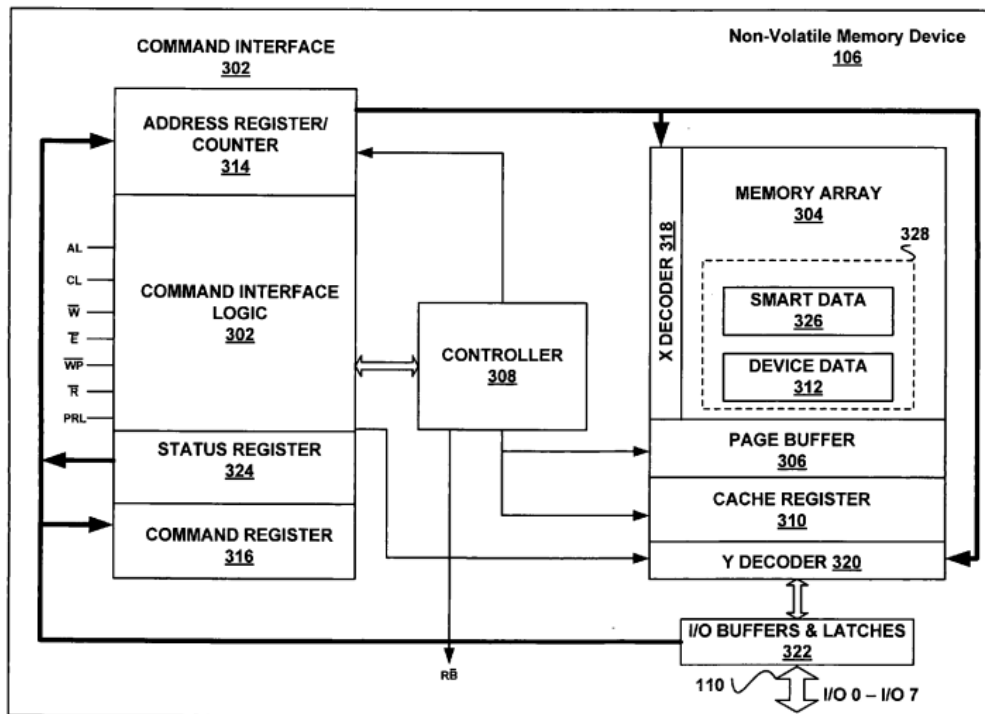


Figure 3

Figure 3 depicts the device data contained in each memory device.

2. *Ware*

Ware is titled “Memory Controller for Non-Homogenous Memory System.” Ex. 1006, code (54). Ware discloses a “memory controller for a non-homogenous memory system,” where the “memory devices, which collectively form the main memory of a computer or computer controlled device, include two or more memory device types (e.g., DRAM, Flash) with different attributes.” *Id.* at 2:18–25. These attributes, that are different for the “memory devices in portion 104” from the “memory devices in portion 106,” include “the ratio of write access time to read access time, volatility, and endurance.” *Id.* at 4:6–11.

Figure 1 of Ware, reproduced below, illustrates “a system having non-homogenous main memory.” *Id.* at 2:58–29.

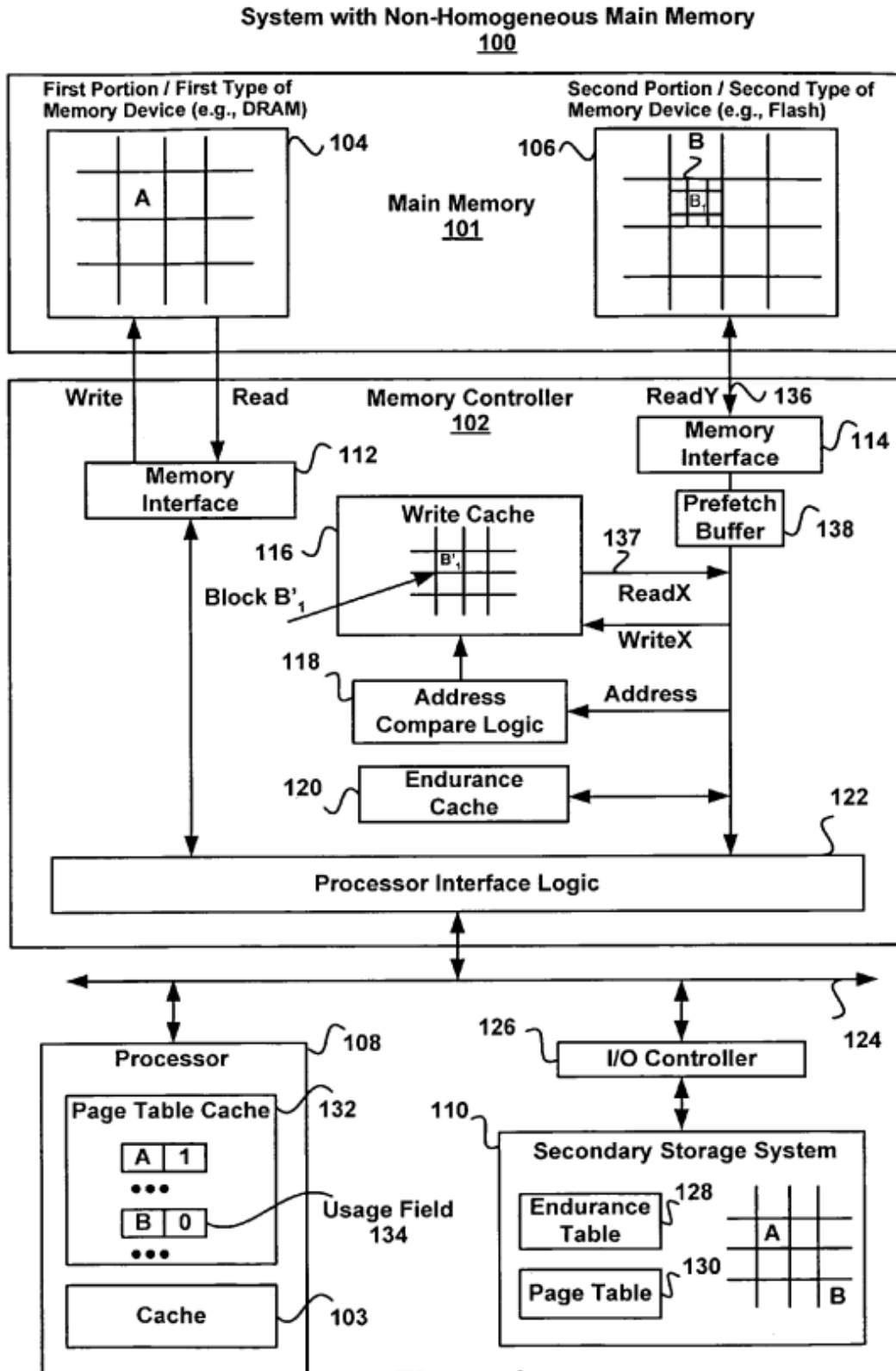


Figure 1 depicts a computer system 100 having a main memory 101 that “includes a first portion 104 implemented with one or more memory devices of a first type (e.g., DRAM), and a second portion 106 implemented with one or more memory devices of a second type (e.g., . . . Flash memory).” *Id.* at 3:39–40, 3:57–61.

E. Discussion of Challenges to the Claims

Patent Owner opposes institution on the basis that Petitioners have failed to establish that the cited art teaches or suggests all the limitations of the challenged claims. Prelim. Resp. 1 (“[N]one of the asserted references in the Petition discloses every claimed feature of the challenged claims, and each ground presented by Petitioners is deficient. The Petition should be denied.”). More specifically, Patent Owner argues:

Petitioners fail to explain how Cornwell and Ware allegedly disclose selecting a transfer size for a memory transaction as a function of the claimed factors in the challenged claims. Indeed, Petitioners fail to explain how the functions disclosed by Cornwell and Ware constitute a selection of transfer size. Rather, the Petition’s arguments amount to nothing more than a conclusory assertion that these features are disclosed, and the Declaration of Dr. Baker (Ex. 1003) offers no further analysis sufficient to support the challenges.

Id. at 7. Accordingly, we consider whether the Petition establishes that either Cornwell or Ware teaches or suggests “selecting a transfer size for the memory transaction, wherein the transfer size is a function of the data size of the memory transaction and the first set of attributes” as recited in claim 1 of the ’190 patent (Ex. 1001, 13:40–42) and as similarly recited in the additional challenged independent claims. *Id.* at 16:19–21 (claim 29), 17:50–53 (claim 45), 18:63–65 (claim 59), 20:41–44 (claim 80), 22:9–11

(claim 98); *see also* Prelim. Resp. 9–10 (chart showing the “selecting” limitation in challenged independent claims 29, 45, 59, 80, and 98).

For its first ground, Petitioners rely on Cornwell (Ex. 1005) for allegedly disclosing the “selecting” limitation as recited in each of the challenged independent claims of the ’190 patent. *See* Pet. 27 (claim 1), 30 (claim 29), 38–39 (claim 45), 45 (claim 59), 51 (claim 80), 52–53 (claim 98). With regard to the “selecting” limitation and Cornwell, the entire presentation in the Petition is:

Cornwell teaches that “the controller 308, *programs the page* into the memory array 304” Ex-1005, ¶ [0039] (emphasis added). Each page has a specific “page size (1k, 2k, etc.).” *Id.*, ¶¶ [0042]; [0048]; [0050]. Cornwell therefore teaches selecting a transfer size for the memory transaction. Ex-1003, ¶ 151.

Cornwell also discloses that page size is a function of device density, which may vary, and the IDE/ATA bus standard, which is used as the communication between the host and the command interface 302. Ex-1005, [0042]; *supra*, §§ IX.A.1.i-IX.A.1.k. Further, a POSITA would have understood that page size is the length of a row (i.e., the number of columns) in the memory, which varies with the device density, and that the data size information (e.g., the number of logical sectors to be transferred), which is referred by the controller for the communication between the controller and the memory store, is included in the ATA command from the host. Ex-1003, ¶¶ 151-152. Cornwell thus teaches that the transfer size is also a function of the first set of attributes, such as the device density. *Id.* Cornwell also teaches that the transfer size is selected by the controller. *Id.*, ¶¶ 153-155.

Id. at 27.⁵ The contention in the Petition is that because “Cornwell teaches that ‘the controller 308, *programs the page* into the memory array 304’ and

⁵ The “selecting” limitation of claim 1 (referred to as “Claim 1o”) is discussed on page 27 of the Petition. For the “selecting” limitations of the

“[e]ach page has a specific ‘page size (1k, 2k, etc.)’” that “Cornwell therefore teaches [the controller] selecting a transfer size for the memory transaction.” *Id.* There is no explanation as to how or why programming a page with a specific size into memory as described in Cornwell is selecting a transfer size for the memory transaction.

Petitioners rely on paragraph 39 of Cornwell for allegedly teaching “selection a transfer size for the memory transaction” as recited in claim 1. *See id.* (quoted above). Paragraph 39 of Cornwell states:

An example page program operation will now be described. During a page program operation, the controller 308 receives a "page program" command input from the I/O bus 110 in a first bus cycle and stores it in the command register 316. Several bus cycles (e.g., 4 cycles) are then used to input a memory address into address register 314. Next, data stored in I/O buffers & latches 322 is loaded into the page buffer 306. When the page buffer 306 is loaded with data, the controller 308 programs the page into the memory array 304 at the address stored in address register 314 using x-decoder logic 318 and y-decoder logic 320 for row and column address decoding, respectively.

Ex. 1005 ¶ 39. Petitioners do not explain and we do not discern how or why this passage in Cornwell teaches or suggests that the controller selects a transfer size for the memory transaction.

Patent Owner argues that Cornwell fails to disclose any selection of transfer size for the memory transaction. Prelim. Resp. 11–15. With specific regard to paragraph 39 of Cornwell, Patent Owner contends that “Cornwell programs a page into the memory array without disclosing or

other challenged independent claims, the Petition relies on the discussion of claim 1. *See* Pet. 30 (“Claim 29g”), 38 (“Claim 45i”), 45 (“Claim 59k”), 51 (“Claim 80h”), 52–53 (“Claim 98h”).

suggesting any selecting step.” *Id.* at 12. We agree with Patent Owner that Cornwell does not disclose or suggest the controller selecting a transfer size for the memory transaction. The cited and quoted sentence from Cornwell in the Petition (Pet. 27 (“the controller 308, *programs the page* into the memory array 304”)) does not teach or suggest a step of “selecting a transfer size for a memory transaction.”

The Petition describes “memory transactions” as “read or write requests.”⁶ *See* Pet. 13 (“Cornwell discloses . . . memory transactions in the form of ‘read or write requests’”), 18 (“Cornwell discloses that a memory read or write transaction is performed on at least one memory location”); *see also* Ex. 1003 ¶ 98 (“Cornwell discloses a method of performing transactions, i.e., read and write operations, on a set of memory locations.”). The Declaration of Dr. Baker in paragraph 154 refers to an example of such a request or memory transaction as being provided in paragraph 25 of Cornwell. Ex. 1003 ¶ 154 (“Cornwell teaches an example in which a media player sends a request to an operating system on a host.” (citing Ex. 1005 ¶ 25)). In this example, the memory transaction request is “a request to save a song to memory.” Ex. 1005 ¶ 25 (“In some implementations, an application running on the host processor 102 can request access to data stored on one or more memory devices 106. For example, a user of a media

⁶ The ’190 patent describes “memory transactions” in a similar fashion. The ’190 patent states, “The term ‘IO device’ is intended to cover a broad range of devices that can request a memory transaction, such as a read or write transaction” (Ex. 1001, 5:9–11) and “The addressing of this memory location may be part of the memory read or write transaction indicated in memory transaction request 114. Main control device 78 interprets memory transaction request 114 by determining whether the memory transaction involves a memory read or a memory write transaction” (*id.* at 11:17–23).

player/recorder may request to save a song to memory.”). We find no allegation in the Petition that Cornwell teaches or suggests selecting a transfer size for a read or write request.

The Petitioners have not shown a reasonable likelihood of establishing that Cornwell teaches or suggests “selection [of] a transfer size for the memory transaction” as recited in the independent claims of the ’190 patent.

For its second ground, Petitioners rely on Ware (Ex. 1006) for allegedly disclosing “selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes” as recited in each of the challenged independent claims of the ’190 patent. *See* Pet. 73–74 (claim 1), 77 (claim 29), 85–86 (claim 45), 93 (claim 59), 99 (claim 80), 101 (claim 98). With regard to the “selecting” limitation and Ware, the entire presentation in the Petition is:

As explained above, Ware teaches that different devices have different granularity, resulting in the need to select a transfer size for read/write transactions. *Supra* § IX.B.1.o.^[7] For example, a POSITA would have understood that flash memory can be written in pages, Ex-1006 at 6:9-12, and that a page is the number of bits in a row of data in flash memory that can be transferred during a memory transaction, and that page size is an attribute. Ex-1003, ¶¶ 463-464. Ware further teaches that a page may be “of a different size than a block in a Flash memory device” and thus may be stored in a plurality of blocks, or one block could store multiple pages, or each page could be stored in a single block.” Ex-1006 at 6:9-14 (emphasis

⁷ Section IX.B.1.o is the immediately preceding section of the Petition at pages 72–73 relating to the immediately preceding limitation in claim 1 (limitation “Claim 1n” which is “using attributes from said first and second device profiles” (Ex. 1001, 13:38)). There is no discussion in Section IX.B.1.o of the Petition of “selecting a transfer size for the memory transaction.”

added). As a result, a POSITA would understand that the transfer size (granularity) would be a function of the data size of the transaction and the first set of attributes. Ex-1003, ¶ 464.

Id. at 73–74. Petitioner does not explain adequately how this passage shows that Ware teaches or suggests “selecting a transfer size for the memory transaction” as recited.⁸

The only passage in Ware cited in the Petition’s sole paragraph relating to the “selecting” limitation (quoted above) is column 6, lines 9–14, which states:

Furthermore, it may be noted that a page, which is the basic unit of data or storage in a virtual memory system is typically, but not necessarily, of a different size than a block in a Flash memory device. Thus, a page may be stored in a plurality of blocks, or one block could store multiple pages, or each page could be stored in a single block.

Ex. 1006, 6:9–14. Petitioner does not explain adequately how or why this passage teaches or suggests “selecting a transfer size for the memory transaction” as recited (and Petitioners never assert that it does (*see* Pet. 73–74 (quoted above))).

Patent Owner argues that the Petition fails to show that Ware teaches or suggests the “selecting” limitation. Prelim. Resp. 15–19. We agree.

Patent Owner also challenges Petitioners’ assertion that “Ware teaches that different devices have different granularity, resulting in the need to

⁸ Petitioners rely on this alleged showing for claim 1 for the similar “selecting” limitations in the other challenged independent claims. *See* Pet. 77 (“Claim 29g”), 85 (“Claim 45i”), 93 (“Claim 59k”), 99 (“Claim 80h”), 101 (“Claim 98h”).

select a transfer size for read/write transactions.” *Id.* at 15–16. The Preliminary Response states:

Petitioners rely on Ware to disclose non-homogeneous main memory 101 having DRAM 104 and Flash 106. Pet., 55. Addressing [Claim 1n] (“using attributes from said first and second device profiles”), Petitioners contend that “Ware also teaches a device granularity attribute, noting that different devices have ‘different granularity for read and write operations.’” Pet., 73 (citing Ware, 5:65-66). Petitioners are misquoting Ware, however, because Ware does not teach whether DRAM 104 and Flash 106 have different granularities. Instead, this quotation in Ware is describing the granularity for read and write operations of a NOR Flash memory device only. Ware’s 5:65-66 discloses that “NOR Flash memory devices typically have different granularity for read and write operations.” Ware then clarifies that it is *only* describing the differences in granularity based on whether the operation performed on a NOR Flash memory device is a “read” or a “write” operation. Ware teaches that “the minimum unit for reading data from Flash memory may be a word (e.g., 16 bits) while the minimum unit for writing data to Flash memory is typically significantly larger than the minimum unit for reading, and is called either a block or a group of memory cells.” Ware, 5:66-6:4. Thus, these statements only compare the granularity for a read vs. a write operation for a Flash memory. Contrary to Petitioners’ erroneous assertion, these statements do not teach whether DRAM 104 and Flash 106 have different granularities from each other.

Id. Patent Owner’s position is well-taken. The sentence cited in the Petition for the proposition that “Ware teaches that different devices have different granularity” relates only to NOR Flash memory devices or one type of device. *See* Pet. 73 (citing Ex. 1006, 5:65–66).

The Petition does not provide a persuasive showing that Ware teaches or suggests selecting a transfer size for a memory transaction. Petitioners have not shown a reasonable likelihood of establishing that Ware teaches or

suggests the “selecting” limitation as recited in the independent claims of the ’190 patent.

III. CONCLUSION

On the record before us, we conclude that there is not a reasonable likelihood that the Petitioners would prevail with respect at least one of the claims challenged in the Petition. Therefore, we do not institute *inter partes* review on any claims or any challenge to the claims of the ’190 patent.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that the Petition is *denied* and we do not institute *inter partes* review of any challenged claim of U.S. Patent No. 9,135,190 B1.

IPR2023-00741
Patent 9,135,190 B1

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