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URIARTE LAW Attn: Stephen R. Uriarte 2021 The Alameda Suite 225 San Jose, CA 95126			EXAMINER FARROKH, HASHEM	
			ART UNIT 2187	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 12/323,461	Applicant(s) ARCEDERA ET AL.	
	Examiner HASHEM FARROKH	Art Unit 2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 November 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-40 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 November 2008 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) | 5) ☐ Notice of Informal Patent Application |
| 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>01/27/09</u> . | 6) ☐ Other: _____ |

The instant application having application No. 12/323,461 has a total of 40 claims pending in the application; there are 3 independent claim and 37 dependent claims, all of which are ready for examination by the examiner.

INFORMATION CONCERNING IDS:

The information disclosure statement (IDS) submitted on 01/27/09 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner.

INFORMATION CONCERNING CLAIMS:

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-40 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

1. *Lines 16-18 of the independent claim1 recite the limitation(s): "...said mapping table causes the storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA..." The*

Art Unit: 2187

specification does not describe how the mapping table causes the storage device to perform optimized memory operation on memory location in such a way that is understood by one having ordinary skill in the related art. The independent claims 22 and 32 recite a similar limitation(s) and are rejected based on the same ground of rejection. The dependent claims 2-21, 23-31, and 33-40 are rejected under 35 U.S.C. 112, first paragraph, by virtue of their dependency from their respected independent claims.

Conclusion

The prior art made of record and not relied upon are as follows:

- 1. U. S. Patent Publication No. 2009/0300318 A1 to Allen et al. describes ADDRESS CACHING STORED TRANSLATION.*
- 2. U. S. Patent Publication No. 2005/0114587 A1 to Chou et al. describes ExpressCard with On-Card Flash Memory with Shared Flash-Control Bus but Separate Ready Lines.*
- 3. U. S. Patent Publication No. 2003/0217202 A1 to Zilberman et al. describes Method for improving performance of a flash-based storage system using specialized flash controllers.*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached on 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin L. Ellis can be reached on (571)272-4205. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

*/Hashem Farrokh/
Examiner, Art Unit 2187*

Amendment(s) to the Specification

In the Specification, please enter the amendments shown with respect to the replacement paragraphs identified below. Text in underline indicates new text, while text in strike-out format or between a pair of double brackets indicates deletion of text. No new matter has been added.

Please replace paragraph **[003]** on page 2 with the following replacement paragraph.

[0003] Electronic storage devices that respectively employ a memory system that includes memory devices, memory chips, or modules that use non-volatile memory cells are commonly known and are sometimes referred to as solid state storage devices. The computer device industry has increased the adoption of these solid state storage devices due to certain advantages offered by these types of storage devices over other forms of storage devices, such as rotational drives. The adoption of solid state storage devices as an enhancement or even as ~~[[a]]~~ replacements ~~replacement~~ to rotational drives is not without some difficulty because many conventional computer devices, sometimes referred to as "hosts", use host operating systems, file systems, or both that are optimized for use with rotational drives rather than solid state storage devices. For example, unlike rotational drives, solid state storage devices that use NAND flash memory, also referred to as "flash drives", suffer from write cycle limitations and to a certain degree, bad blocks. In addition, flash drives use block addressing rather than byte addressing, and these flash drives use block addresses that are usually much larger than the block address used by the host. Block addressing may impose an

additional level of complexity and additional processing cycles when performing a write operation, and which in turn, may increase write operation latency. This additional level of complexity may include performing a read-modify-write transaction to complete the write operation.

Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (ORIGINAL) A mapping table for optimizing memory operations performed by an electronic storage device in response to receiving an I/O transaction request initiated by a host, said mapping table comprising:

a set of logical fields, including a first logical field and a second logical field, and said logical fields respectively disposed for representing a plurality of LBA sets, including said first logical field disposed for representing a first LBA set and said second logical field disposed for representing a second LBA set, said first and second LBA sets each representing a set of consecutive LBAs;

a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for representing a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs; and

wherein, in response to receiving the I/O transaction request, said mapping table causes-the storage device to perform optimized memory operations on memory locations respectively associated with said first PBA

and said second PBA, if the I/O transaction request is associated with said first and second LBA sets.

2. (ORIGINAL) The mapping table of claim 1, wherein:

said first and second LBA sets are adjacent LBA sets;

said first and second access parameters are different; and

said LBAs from said first and second LBA sets are logical block addresses used by the host for addressing said data.

3. (ORIGINAL) The mapping table of claim 1, wherein an LBA having the lowest LBA value from said second LBA set is consecutive with an LBA having the highest LBA value from said first LBA set.

4. (ORIGINAL) The mapping table of claim 1, wherein an LBA having the lowest LBA value from said second LBA set is not consecutive with an LBA having the highest LBA value from said first LBA set.

5. (ORIGINAL) The mapping table of claim 1, wherein:

data stored at a first physical memory location, which is addressable using said first PBA, is transferred to a second physical memory location, which is addressable using said second PBA, said data transferred in portions equal to a section size.

6. (ORIGINAL) The mapping table of claim 5, wherein:

said first and second LBA sets respectively have an LBA set size equal to said section size.

7. (ORIGINAL) The mapping table of claim 5, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size; and

said section size is at least equal to a product of a positive integer multiplied by said native page size, and said integer is at least equal to one.

8. (ORIGINAL) The mapping table of claim 5, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size and a plurality of flash blocks, and that supports more than one page write that can be performed on a page from one of said flash blocks before requiring an erase cycle to be performed on said one of said flash blocks; and

said section size is at least equal to a quotient resulting from dividing said native page size by said more than one page write.

9. (ORIGINAL) The mapping table of claim 1, wherein said set of access parameters includes a bus identifier, an FDE identifier and a group identifier.

10. (ORIGINAL) The mapping table of claim 9, wherein said first and second PBA include different bus identifiers, different FDE identifiers and different group identifiers.

11. (ORIGINAL) The mapping table of claim 9, wherein said first and second PBA respectively include different combinations of said bus identifiers, said FDE identifiers, and said group identifiers.

12. (ORIGINAL) The mapping table of claim 1, wherein said first and second PBA include different bus identifiers.

13. (ORIGINAL) The mapping table of claim 1, wherein said first and second PBA include different FDE identifiers.

14. (ORIGINAL) The mapping table of claim 1, wherein said first and second PBAs respectively include a first group identifier and a second group identifier.

15. (ORIGINAL) The mapping table of claim 1:

wherein said memory store includes a set of solid state memory devices that are coupled to a set of buses and that are controlled by a set of FDEs; and

wherein said access parameter includes a group identifier for identifying at least a portion of said set of memory devices that are respectively controlled by different FDEs from said set of FDEs.

16. (ORIGINAL) The mapping table of claim 1, wherein:

said memory store includes a first set of memory devices controlled by a first FDE and a second set of memory devices controlled by a second FDE; and

said first and second sets of memory devices associated with a plurality of group identifiers in which no two of said group identifiers is the same, and each memory device from said first set of memory devices is respectively associated with different group identifiers from said plurality of group identifiers.

17. (ORIGINAL) The mapping table of claim 1, wherein:

said electronic storage device includes a storage device controller, said memory store, and a memory system;

said memory system includes a flash buffer controller, a first set of FDEs, a second set of FDEs, and a set of buses that includes a first bus and a second bus;

said memory store includes a first set of memory devices and a second set of memory devices, said first and second set of memory devices respectively coupled to said first and second buses;

said first set of FDEs disposed to control said first set of memory devices through said flash buffer controller and said first bus, said first set of FDEs including a first FDE and a second FDE;

said second set of FDEs disposed to control said second set of memory devices through said flash buffer controller and said second bus, said second set of FDEs including a third FDE and a fourth FDE;

said first and second set of memory devices are associated with a plurality of memory device groups, including a first group and a second group;

wherein said first and second groups corresponding respectively to said first and second group identifiers; and

wherein said first and second PBAs respectively include said first and second group identifiers.

18. (ORIGINAL) The mapping table of claim 17, wherein said first and third memory devices are associated with a first group identifier and said second and fourth memory devices are associated with a second group identifier.

19. (ORIGINAL) The mapping table of claim 17, wherein said first and second memory devices include non-volatile solid state memory cells.

20. (ORIGINAL) The mapping table of claim 17, wherein each memory device from said first set of memory devices are respectively associated with different group identifiers.

21. (ORIGINAL) The mapping table of claim 1, wherein said first PBA further disposed to represent a memory index.

22. (ORIGINAL) A memory system for optimizing memory operations in an electronic storage device responsive to an I/O transaction request initiated by a host, said electronic storage device including a memory store having a set of memory devices including a first memory device, a second memory device, a third memory device and a fourth memory device, said memory system comprising:

a flash buffer controller, a set of FDEs, and a set of buses, wherein said set of FDEs including a first FDE, a second FDE, a third FDE, and a fourth FDE and wherein said buses including a first bus and a second bus, said first bus coupled to the first and second memory devices, and the second bus coupled to said third and fourth memory devices;

said first and second FDEs coupled to said first bus through said first buffer controller, and said third and fourth FDEs coupled to said second bus through said first buffer controller;

said set of memory devices are partitioned into memory device groups, including a first group and a second group;

a mapping table that includes:

a set of logical fields, including a first logical field and a second logical field, and said logical fields respectively disposed for representing a plurality of LBA sets, including said first logical field disposed for representing a first LBA set and said second logical field disposed for representing a second LBA set, said first and second LBA sets each representing a set of consecutive LBAs;

a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for holding a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs; and

wherein, in response to receiving the I/O transaction request, said mapping table causes the storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second set of consecutive LBAs.

23. (ORIGINAL) The memory system of claim 22, wherein an LBA having the lowest LBA value in said second LBA set is consecutive with an LBA having the highest LBA value from said first LBA set.

24. (ORIGINAL) The memory system of claim 22, wherein said first and third memory devices correspond to a first group identifier and said second and fourth memory devices correspond to a second group identifier.

25. (ORIGINAL) The memory system of claim 22, wherein said optimized memory operations include a first memory operation performed using said first PBA and a second memory operation performed using said second PBA; said first and second PBAs respectively associated with a first set of access parameters and a second set of access parameters, and said set of first and second set of access parameters differing by at least one access parameter.

26. (ORIGINAL) The memory system of claim 25, wherein said first and second set of access parameters respectively including a bus identifier, an FDE identifier and a group identifier.

27. (ORIGINAL) The memory system of claim 26, wherein said first and second PBAs respectively include said first and second group identifiers.

28. (ORIGINAL) The memory system of claim 22, wherein said PBA further includes a memory index.

29. (ORIGINAL) The memory system of claim 22, wherein:

data stored at said first physical memory location is moved to said second physical memory location using a minimum transfer size granularity that is equal to a section size; and

said first and second LBA sets respectively have an LBA set size equal to said section size.

30. (ORIGINAL) The mapping table of claim 29, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size; and

said section size is at least equal to a product of a positive integer multiplied by said native page size, and said integer is at least equal to one.

31. (ORIGINAL) The mapping table of claim 29, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size and a plurality of flash blocks, and that permit a number of write operations to be performed on a page from one of said flash blocks before requiring an erase cycle to be performed on said flash block, said number of write operations equal to at least two; and

said section size is at least equal to said native page size divided by said number of write operations.

32. (ORIGINAL) An electronic storage device that includes a memory system that uses a memory table for increasing the likelihood that an operational load imposed on the storage apparatus during the processing of an I/O transaction request will be optimally distributed across storage device resources, said I/O transaction request received by said storage device from a requesting host, said electronic storage device comprising:

a mapping table which maps a first LBA set to a first PBA, and a second LBA set to a second PBA, said first and second LBA sets including respective sets of consecutive LBAs;

a memory store that includes a set of flash devices, said set of flash devices includes a first physical memory location and a second physical memory location that are addressable by said first and second PBAs respectively;

a memory system coupled to said memory store and disposed to use said mapping table during a memory operation;

wherein said first PBA includes a first set of access parameters and said second PBA includes a second set of access parameters, and at least one difference between said first and second PBAs; and

wherein said mapping table increases the likelihood that that the operational load imposed on the storage apparatus during the processing of

the I/O transaction request will be optimally distributed across storage device resources.

33. (ORIGINAL) The electronic storage device of claim 32, wherein an LBA having the lowest LBA value in said second LBA set is consecutive with an LBA having the highest LBA value from said first LBA set.

34. (ORIGINAL) The electronic storage device of claim 32, wherein the processing of the I/O transaction request includes a first memory operation performed using said first PBA and a second memory operation performed using said second PBA; said first and second PBAs respectively associated with a first set of access parameters and a second set of access parameters, and said set of first and second set of access parameters differing by at least one access parameter.

35. (ORIGINAL) The memory system of claim 34, wherein said first and second set of access parameters respectively including a bus identifier, an FDE identifier, and a group identifier.

36. (ORIGINAL) The memory system of claim 35, wherein said first and second PBAs respectively include said first and second group identifiers.

37. (ORIGINAL) The electronic storage device of claim 32, wherein said PBA further includes a memory index.

38. (ORIGINAL) The electronic storage device of claim 32, wherein:

data stored at said first physical memory location is moved to said second physical memory location using a minimum transfer size granularity that is equal to a section size; and

said first and second LBA sets respectively have an LBA set size equal to said section size.

39. (ORIGINAL) The mapping table of claim 38, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size; and

said section size is at least equal to a product of a positive integer multiplied by said native page size, and said integer is at least equal to one.

40. (ORIGINAL) The mapping table of claim 38, wherein:

said memory store includes a plurality of flash memory devices that each have a native page size and a plurality of flash blocks, and that permit a number of write operations to be performed on a page from one of said flash blocks before requiring an erase cycle to be performed on said flash block, said number of write operations equal to at least two; and

said section size is at least equal to said native page size divided by said number of write operations.

Remarks

The specification has been amended to correct minor errors, improve readability, or otherwise. These corrections are of a clerical nature and do not add "new matter".

The First Paragraph Section 112 Rejection

The Examiner rejects claims 1-40 under 35 USC §112, first paragraph, as allegedly failing to comply with the written description requirement. More particularly, the Examiner asserts that the "specification does not describe how the mapping table causes the storage device to perform optimized memory operations on a memory location". Applicants respectfully traverse this rejection because the Specification describes embodiment(s) of the present invention in a manner that allows one of ordinary skill in the art how to make and use without undue experimentation the invention as claimed. See, MPEP 2164.01.

Independent Claims 1, 22 and 32 Meet the Statutory Requirements

Claim 1

Claim 1 recites in part:

"wherein, in response to receiving the I/O transaction request, said mapping table **causes** the storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second LBA sets." (Emphasis Added.)

The above limitation in claim 1 is supported by the Specification because the Specification teaches how a “mapping table” causes a “storage device to perform optimized memory operations”. For example, paragraphs [0023]-[0025], [0034], and [0036] (see also, FIGS. 1-2) disclose a mapping table, that when used by a storage device, **causes** the storage device to perform optimized memory operations.

“[0023] In FIG. 2, mapping table 9 reflects the embodiment disclosed in FIG. 1. PBA 46 and PBA 50 include access parameters that are associated with the same group identifier of 15-0 but pertain to physical memory locations within different flash memory devices in memory store 6. ***These access parameters are associated with different FDE identifiers, such as FDE identifiers 22-01 and 22-11 and with different bus identifiers 8-0 and 8-1, respectively.*** (Emphasis added.) Using their respective access parameters, PBA 46 is associated with a physical memory location that is within a flash memory device 12-01 coupled to bus 8-0, controlled by FDE 22-01, and in group 15-0, while PBA 50 is associated with another physical memory location that is within a flash memory device 12-01 coupled to bus 8-1, controlled by FDE 22-11, and in group 15-0 in FIG. 1.

[0024] The term “LBA”, which may also be referred to herein as a logical block address, is intended to represent an address that is part of a logical addressing system (not shown) used by a host, such as host 18, and this host may use one or more LBAs in an I/O transaction request, such as I/O transaction request 20. Mapping table 9 associates LBAs from this host logical addressing system to the device addressing system used by storage

device 2. This device addressing system may include using a mapping table that includes the functionality described herein, such as mapping table 9. These LBAs may be grouped into ***sets of consecutive LBAs, named "LBA sets"***. (Emphasis added.) These LBA sets may then be represented using logical fields 26 from mapping table 9, where each logical field in set of logical fields 26 is respectively disposed to represent a LBA set. For example, LBA sets 40, 42, 44, and 45 may be used to respectively represent consecutive LBAs used by host 18, such as LBAs 00 through 07, LBAs 08 through 15, LBAs 16 through 23, and LBAs 24-31, respectively.

[0025] *Logical fields in mapping table 9 may be initialized to represent LBA sets that are serially arranged in mapping table 9 so that LBAs from adjacent LBA sets are contiguous.* (Emphasis added.)

In the example shown in FIG. 2, LBA sets 40, 42, 42, 44 and 45 represent serially arranged LBAs since the highest LBA in one LBA set is contiguous with the lowest LBA in an adjacent LBA set. Specifically, LBA sets 40 and 42 are disposed in adjacent rows and thus are adjacent to each other. These adjacent LBA sets are also contiguous because LBA 7, which corresponds to the highest LBA in LBA set 40, is contiguous with LBA 8, which is the lowest LBA in LBA set 42. Similarly, LBA sets 42 and 44 are also contiguous because LBA 15, which corresponds to the highest LBA in LBA set 42, is contiguous with LBA 16, which is the lowest LBA in LBA set 44. LBA set 44 is also contiguous with LBA set 45.

[0034] During operation and after initialization of mapping table 9, if storage device controller 22 receives an I/O transaction request 20 from host 18, *storage device controller 22 processes I/O transaction request by*****

transferring it to DMA controller 10. After receiving I/O transaction request 20, DMA controller 10 uses mapping table 9 to determine which PBAs are mapped to LBAs used in I/O transaction request 20. DMA controller 10 uses the PBAs to determine which addressable physical memory locations to use when performing memory operations requested by host 18 through I/O transaction request 20.

Mapping table 9 associates LBA sets to PBAs in a manner that increases the likelihood *that memory operations resulting from I/O transaction request 20 will be **optimized by distributing these memory operations across different storage device resources that are associated with these PBAs**, such as across **different FDEs, different buses, different flash** memory devices, or **any combination of these**.* (Emphasis added.)

[0036] Using different group identifiers, such as group identifiers 15-0 and 15-1 in mapping table 9, enables the ***interleaving*** of memory operations across flash devices that are controlled by the same FDE. (Emphasis added.) Stated another way, using different group identifiers enables interleaving memory operations across flash devices that belong to the same flash array bank interleave. Using different FDE identifiers in mapping table 9 enables interleaving memory operations across flash memory devices that are controlled by different FDEs, while using different bus identifiers enables interleaving memory operations across flash memory devices that are coupled to different flash bus interfaces.”

Thus, by the example discussed above, the Specification describes “how the mapping table causes the storage device to perform optimized memory operations” (See, Office Action) in a manner that meets the requirements in Section 112, first

paragraph, rendering claim 1 and its respective dependent claims statutory.

Claim 22

Claim 22 recites in part:

“wherein, in response to receiving the I/O transaction request, said mapping table causes the storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second set of consecutive LBAs.”

The above limitation in claim 22 is also supported by the Specification because the Specification teaches how a “mapping table” causes a “storage device to perform optimized memory operations”. See, Specification at paragraphs [0023]-[0025], [0034], and [0036] and FIGS. 1-2. Thus, claim 22 also meets the requirements in 35 USC Section 112, first paragraph, rendering claim 22 and its respective dependent claims statutory.

Claim 32

Claim 32 recites in part:

“wherein said mapping table increases the likelihood that that the operational load imposed on the storage apparatus during the processing of the I/O transaction request will be optimally distributed across storage device resources.”

The above limitation in claim 32 is supported by the Specification because the

Specification teaches how a “mapping table increases the likelihood that the operational load imposed on the storage apparatus”...“will be optimally distributed across storage device resources” as recited in claim 32. See for example, paragraphs [0034] and [0036] (see also, FIGS. 1-2) which disclose the following:

“[0034] During operation and after initialization of mapping table 9, if storage device controller 22 receives an I/O transaction request 20 from host 18, storage device controller 22 processes I/O transaction request by transferring it to DMA controller 10. *After receiving I/O transaction request 20, DMA controller 10 **uses mapping table 9 to determine which PBAs are mapped to LBAs used in I/O transaction request 20.** DMA controller 10 uses the PBAs to determine which addressable physical memory locations to use when performing memory operations requested by host 18 through I/O transaction request 20. Mapping table 9 associates LBA sets to PBAs in a manner that **increases the likelihood that memory operations resulting from I/O transaction request 20 will be optimized by distributing these memory operations across different storage device resources that are associated with these PBAs,** such as across **different FDEs, different buses, different flash** memory devices, or **any combination of these.** (Emphasis added.)*

[0036] Using different group identifiers, such as group identifiers 15-0 and 15-1 in mapping table 9, **enables the interleaving** of memory operations across flash devices that are controlled by the same FDE. Stated another way, using different group identifiers enables interleaving memory operations across flash devices that belong to the same flash array bank interleave. Using different FDE identifiers in mapping table 9 enables interleaving

memory operations across flash memory devices that are controlled by different FDEs, while using different bus identifiers enables interleaving memory operations across flash memory devices that are coupled to different flash bus interfaces. (Emphasis added.)”

Thus, claim 32 also meets the requirements in 35 USC Section 112, first paragraph, rendering claim 32 and its respective dependent claims statutory.

Request for Allowance

It is believed that this Response places this Application into condition for allowance. Early favorable consideration of this Amendment is earnestly solicited.

Respectfully submitted,

Dated: 25 February 2011

/Stephen R. Uriarte/

Stephen R. Uriarte, Reg. No. 40,854

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2021 The Alameda, Suite 225
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Email: mail@uriartelaw.com



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

64180 7590 04/13/2011
URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

EXAMINER

FARROKH, HASHEM

ART UNIT

PAPER NUMBER

2187

DATE MAILED: 04/13/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/323,461

11/25/2008

Mark Ian ARCEDERA

6005.007CIP

7802

TITLE OF INVENTION: OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$755	\$300	\$0	\$1055	07/13/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

64180 7590 04/13/2011
URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/323,461 11/25/2008 Mark Ian ARCEDERA 6005.007CIP 7802

TITLE OF INVENTION: OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$755	\$300	\$0	\$1055	07/13/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
FARROKH, HASHEM	2187	711-103000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s); (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/323,461	11/25/2008	Mark Ian ARCEDERA	6005.007/CIP	7802

64180 7590 04/13/2011
URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

EXAMINER

FARROKH, HASHEM

ART UNIT	PAPER NUMBER
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2187

DATE MAILED: 04/13/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 242 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 242 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability

Application No.

12/323,461

Examiner

HASHEM FARROKH

Applicant(s)

ARCEDERA ET AL.

Art Unit

2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 02/25/2011.
2. ☒ The allowed claim(s) is/are 1-40.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
- (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
- 1) ☐ hereto or 2) ☐ to Paper No./Mail Date ____.
- (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|---|
| 1. ☐ Notice of References Cited (PTO-892) | 5. ☐ Notice of Informal Patent Application |
| 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date ____. |
| 3. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date ____ | 7. ☐ Examiner's Amendment/Comment |
| 4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 8. ☒ Examiner's Statement of Reasons for Allowance |
| | 9. ☐ Other ____. |

PART I **THE EXAMINER'S EVALUATION OF THE APPLICATION**

SECTION A **RELEVANT ART CITED BY THE EXAMINER**

1. U. S. Patent Publication No. 2009/0300318 A1 to Allen et al. describes ADDRESS CACHING STORED TRANSLATION.
2. U. S. Patent Publication No. 2005/0114587 A1 to Chou et al. describes Express Card with On-Card Flash Memory with Shared Flash-Control Bus but Separate Ready Lines.
3. U. S. Patent Publication No. 2003/0217202 A1 to Zilberman et al. describes Method for improving performance of a flash-based storage system using specialized flash controllers.

SECTION B **DISTINGUISHING FEATURES RECITED IN THE CLAIMS**

The following is an **Examiner's Statement of Reasons for Allowance** See **MPEP 1302.14**

4. The primary reasons for allowance of claims 1-31 in the instant application is the combination with the inclusion of the following limitations: **a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for representing a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical**

fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs; and wherein, in response to receiving the I/O transaction request, said mapping table causes-the storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second LBA sets.

5. *The primary reasons for allowance of claims 32-40 in the instant application is the combination with the inclusion of the following limitations: **a mapping table which maps a first LBA set to a first PBA, and a second LBA set to a second PBA, said first and second LBA sets including respective sets of consecutive LBAs; wherein said first PBA includes a first set of access parameters and said second PBA includes a second set of access parameters, and at least one difference between said first and second PBAs; and wherein said mapping table increases the likelihood that that the operational load imposed on the storage apparatus during the processing of he I/O transaction request will be optimally distributed across storage device resources.***

The prior art of record including the disclosures of Allen et al. (2009/0300318 A1), Chou et al. (2005/0114587 A1), and Zilberman et al. (2003/0217202 A1) neither anticipates nor renders obvious the above-recited combination.

Art Unit: 2187

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays should be clearly labeled

"Comments on Statement of Reasons for Allowance"

SECTION C RESPONSE TO REMARKS

Applicant arguments regarding rejection of claims 1-40 under 35 U.S.C. 112, first paragraph is persuasive. Hence, rejection under 35 U.S.C. 112, first paragraph is withdrawn.

PART II THE ATTENTION OF FUTURE CORRESPONDENT

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached on 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Ellis can be reached on (571)272-4205. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2187

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

*/HASHEM FARROKH/
Primary Examiner, Art Unit 2187*