IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

BITMICRO LLC, *Plaintiff,*	§	
-v-	§	**6:22-CV-00331-ADA**
KIOXIA AMERICA, INC., KIOXIA CORPORATION, *Defendants.*	§	

CLAIM CONSTRUCTION ORDER AND MEMORANDUM IN SUPPORT THEREOF

Before the Court are the Parties' claim construction briefs: Defendants KIOXIA America, Inc. and KIOXIA Corporation's Opening and Reply briefs (ECF Nos. 33and 43, respectively) and Plaintiff BiTMICRO LLC's Response and Sur-Reply briefs (ECF Nos. 38 and 42, respectively). The Court provided preliminary constructions for the disputed terms one day before the hearing. The parties informed the Court that they did not choose to argue against any of the preliminary constructions. The Court now enters its preliminary constructions as its final constructions.

I. DESCRIPTION OF THE ASSERTED PATENTS

Plaintiff asserts U.S. Patent Nos. 6,496,939 ("'939 Patent"), 8,010,740 ("'740 Patent"), and 9,135,190 ("'190 Patent").

A. The '939 Patent

The '939 Patent is entitled "Method and system for controlling data in a computer system in the event of a power failure" and relates to "a system and method for controlling data in such a system when the system loses external power.." '939 Patent at 1:9–11.

In the event of loss of power to a computer system, to prevent the loss of data written to volatile memory, the '939 Patent discloses using "super-capacitors" as a temporary power source

to allow data to be safely written from volatile memory (which does not retain data after a loss of power) to non-volatile memory (which does retain data after a loss of power). *Id.* at 2:33–37. Figure 1 depicts an embodiment of the invention:

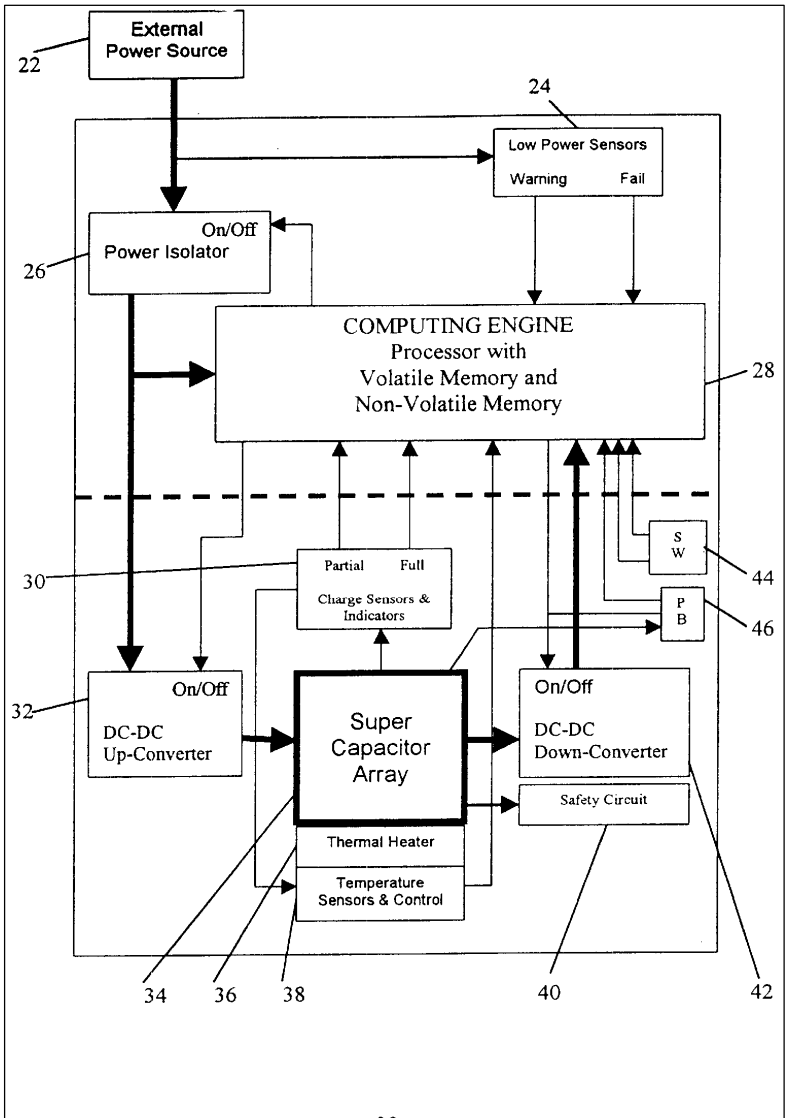


FIGURE 1

The specification describes that when there is power, *i.e.*, external power source 22 is providing power to the computer system, upconverter 32 charges super capacitor array 34. *Id.* at 3:39–41. When there is a loss of power, upconverter 32 deactivates and down-converter 42 activates, which allows super capacitor array 34 to provide power to compute engine 28. *Id.* at 5:19–22. The

specification describes that once the super capacitors discharge to a "predetermined level," the down converter has insufficient voltage differential to continue proper operation and shuts down. *Id.* at 6:40–44.

B. The '740 Patent

The '740 Patent is entitled "Optimizing memory operations in an electronic storage device" and relates to "solutions for optimizing memory operations in a memory system suitable for use in an electronic storage device." '740 Patent at 1:16–18. The '740 Patent describes using a "improved mapping table" to "increase[e] the likelihood that, in response to an I/O transaction initiated by a host, the operational load imposed on the storage device by these memory operations will be optimally distributed across different storage device resources, such as by interleaving or parallel memory operations, reducing memory operation latency, increasing operational device efficiency, or both." *Id.* at 2:14–21. Figure 2 depicts an exemplary mapping table. *Id.* at 5:27–30.

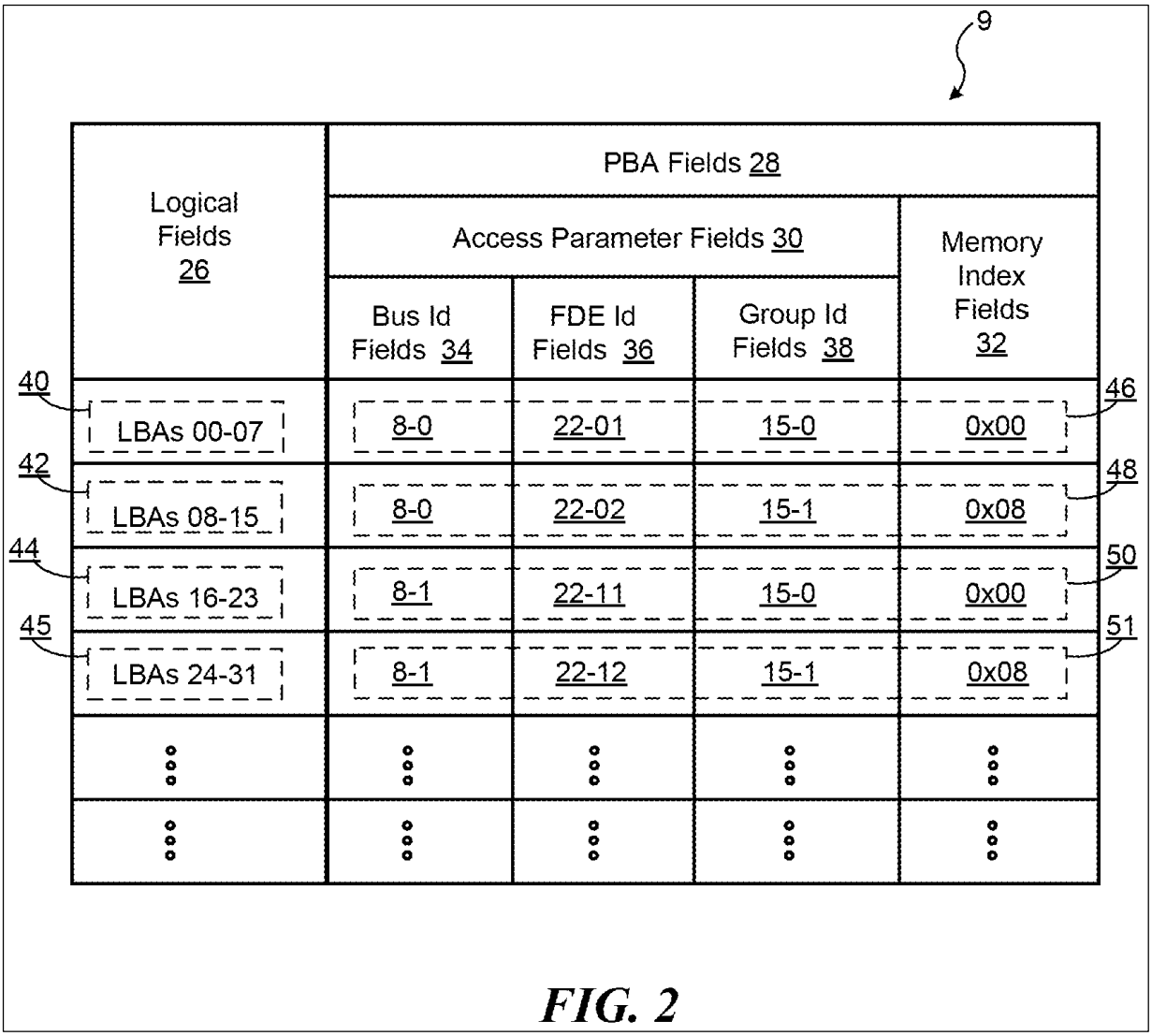


FIG. 2

The specification uses the acronyms LBA and PBA for logical block address, which is the address that is part of a logical addressing system used by a host, and physical block address, which is a unique addressable physical memory location, respectively. *Id.* at 6:37–40, 5:30–33. The specification describes that each row of the mapping table contains the LBA field and PBA fields (access parameter fields 30: bus identifier field 34, FDE identifier fields 36, and group identifier field 38; and memory index field 32). *Id.* at 5:29–38. The specification describes that the "mapping association among LBA sets and PBAs increases the likelihood that memory operations resulting from an I/O transaction request will be optimized because if these memory operations

involve data accesses associated with contiguous LBA sets these data accesses will in likelihood occur on different PBAs." *Id.* at 7:9–14.

C. The '190 Patent

The '190 Patent is entitled "Multi-profile memory controller for computing devices" and relates to "multi-profile memory controllers and computing devices, such as solid-state storage devices, that use these multi-profile memory controllers.." '190 Patent at 1:17–19. The memory controller disclosed in the '190 Patent varied how reads and writes were performed on different memory locations or devices, which was an improvement over the prior art. *Id.* at 1:54–60. To accomplish this, the specification describes that the multi-profile memory controller uses different device profiles to perform memory transactions. *Id.* at 2:44–47. Figure 2A depicts an exemplary device profile.

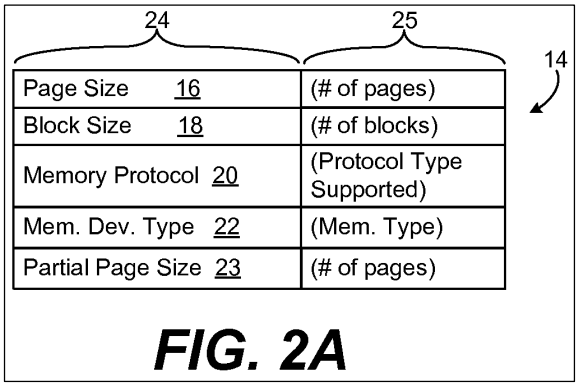


FIG. 2A

II. LEGAL STANDARD

A. General principles

The general rule is that claim terms are generally given their plain-and-ordinary meaning. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*); *Azure Networks, LLC v. CSR PLC*, 771 F.3d 1336, 1347 (Fed. Cir. 2014), *vacated on other grounds*, 575 U.S. 959, 959 (2015) ("There is a heavy presumption that claim terms carry their accustomed meaning in the

relevant community at the relevant time.") (internal quotation omitted). The plain-and-ordinary meaning of a term is the "meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Phillips*, 415 F.3d at 1313.

The "only two exceptions to [the] general rule" that claim terms are construed according to their plain-and-ordinary meaning are when the patentee (1) acts as his/her own lexicographer or (2) disavows the full scope of the claim term either in the specification or during prosecution. *Thorner v. Sony Computer Ent. Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012). The Federal Circuit has counseled that "[t]he standards for finding lexicography and disavowal are exacting." *Hill-Rom Servs., Inc. v. Stryker Corp.*, 755 F.3d 1367, 1371 (Fed. Cir. 2014). To act as his/her own lexicographer, the patentee must "clearly set forth a definition of the disputed claim term" and "'clearly express an intent' to [define] the term." *Thorner,* 669 F.3d at 1365.

"Like the specification, the prosecution history provides evidence of how the PTO and the inventor understood the patent." *Phillips*, 415 F.3d at 1317. "[D]istinguishing the claimed invention over the prior art, an applicant is indicating what a claim does not cover." *Spectrum Int'l, Inc. v. Sterilite Corp.*, 164 F.3d 1372, 1379 (Fed. Cir. 1998). The doctrine of prosecution disclaimer precludes a patentee from recapturing a specific meaning that was previously disclaimed during prosecution. *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1323 (Fed. Cir. 2003). "[F]or prosecution disclaimer to attach, our precedent requires that the alleged disavowing actions or statements made during prosecution be both clear and unmistakable." *Id.* at 1325–26. Accordingly, when "an applicant's statements are amenable to multiple reasonable interpretations, they cannot be deemed clear and unmistakable." *3M Innovative Props. Co. v. Tredegar Corp.*, 725 F.3d 1315, 1326 (Fed. Cir. 2013).

A construction of "plain and ordinary meaning" may be inadequate when a term has more than one "ordinary" meaning or when reliance on a term's "ordinary" meaning does not resolve the parties' dispute. *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co*., 521 F.3d 1351, 1361 (Fed. Cir. 2008). In that case, the Court must describe what the plain-and-ordinary meaning is. *Id.*

"Although the specification may aid the court in interpreting the meaning of disputed claim language . . ., particular embodiments and examples appearing in the specification will not generally be read into the claims." *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1571 (Fed. Cir. 1988). "[I]t is improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004).

Although extrinsic evidence can be useful, it is "less significant than the intrinsic record in determining 'the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317 (quoting *C.R. Bard, Inc. v. United States Surgical Corp.*, 388 F.3d 858, 862 (Fed. Cir. 2004)). Technical dictionaries may be helpful, but they may also provide definitions that are too broad or not indicative of how the term is used in the patent. *Id.* at 1318. Expert testimony may also be helpful, but an expert's conclusory or unsupported assertions as to the meaning of a term are not. *Id.*

B. Claim differentiation

Under the doctrine of claim differentiation, a court presumes that each claim in a patent has a different scope. *Phillips*, 415 F.3d at 1314-15. The presumption is rebutted when, for example, the "construction of an independent claim leads to a clear conclusion inconsistent with a

dependent claim." *Id.* The presumption is also rebutted when there is a "contrary construction dictated by the written description or prosecution history." *Seachange Int'l., Inc. v. C-COR, Inc.*, 413 F.3d 1361, 1369 (Fed. Cir. 2005). The presumption does not apply if it serves to broaden the claims beyond their meaning in light of the specification. *Intellectual Ventures I LLC v. Motorola Mobility LLC*, 870 F.3d 1320, 1326 (Fed. Cir. 2017).

C. Indefiniteness

"[I]ndefiniteness is a question of law and in effect part of claim construction." *ePlus, Inc. v. Lawson Software, Inc.*, 700 F.3d 509, 517 (Fed. Cir. 2012). Patent claims must particularly point out and distinctly claim the subject matter regarded as the invention. 35 U.S.C. § 112, ¶ 2. A claim, when viewed in light of the intrinsic evidence, must "inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 910 (2014). If it does not, the claim fails § 112, ¶ 2 and is therefore invalid as indefinite. *Id.* at 901. Whether a claim is indefinite is determined from the perspective of one of ordinary skill in the art as of the time the application was filed. *Id.* at 911.

In the context of a claim governed by § 112, ¶ 6, the claim is indefinite if the claim fails to disclose adequate corresponding structure to perform the claimed functions. *Williamson*, 792 F.3d at 1351–52. The disclosure is inadequate when one of ordinary skill in the art "would be unable to recognize the structure in the specification and associate it with the corresponding function in the claim." *Id.* at 1352. Computer-implemented means-plus-function claims are indefinite unless the specification discloses an algorithm to perform the function associated with the limitation. *Noah Sys., Inc. v. Intuit Inc.*, 675 F.3d 1302, 1319 (Fed. Cir. 2012).

D. Means-Plus-Function Claiming

A patent claim may be expressed using functional language. *See* 35 U.S.C. § 112 ¶ 6.[1] *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1347–49 (Fed. Cir. 2015). In particular, § 112, ¶ 6 provides that a structure may be claimed as a "means . . . for performing a specified function" and that an act may be claimed as a "step for performing a specified function." *Masco Corp. v. United States*, 303 F.3d 1316, 1326 (Fed. Cir. 2002).

The presumption is that terms reciting "means" are subject to § 112, ¶ 6. *Williamson*, 792 F.3d at 1348. But if the term does not use the word "means," then it is presumed not to be subject to § 112, ¶ 6. *Id.* "That presumption can be overcome, but only if the challenger demonstrates that the claim term fails to recite sufficiently definite structure or else recites function without reciting sufficient structure for performing that function." *Samsung Elecs. Am., Inc. v. Prisua Eng'g Corp.*, 948 F.3d 1342 (Fed. Cir. 2020) (internal quotations removed) (citing *Williamson*, 792 F.3d at 1349). "The correct inquiry, when 'means' is absent from a limitation, is whether the limitation, read in light of the remaining claim language, specification, prosecution history, and relevant extrinsic evidence, has sufficiently definite structure to a person of ordinary skill in the art." *Apple Inc. v. Motorola, Inc.*, 757 F.3d 1286 (Fed. Cir. 2014), *overruled on other grounds by Williamson*, 792 F.3d at 1349.

When § 112 ¶ 6 applies, it limits the scope of the functional term "to only the structure, materials, or acts described in the specification as corresponding to the claimed function and equivalents thereof." *Williamson*, 792 F.3d at 1347. Construing a means-plus-function limitation involves multiple steps. "The first step . . . is a determination of the function of the means-plus-

[1]The American Invents Act of 2011 changed the numbering of the relevant subsection from § 112, ¶ 6 to § 112(f). Because the substance of the subsection did not change, the undersigned will refer to the relevant subsection as § 112, ¶ 6 in keeping with the numeration at the time of the patent filing.

function limitation." *Medtronic, Inc. v. Advanced Cardiovascular Sys., Inc.*, 248 F.3d 1303, 1311 (Fed. Cir. 2001). "[T]he next step is to determine the corresponding structure disclosed in the specification and equivalents thereof." *Id.* A "structure disclosed in the specification is 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim." *Id.* The focus of the "corresponding structure" inquiry is not merely whether a structure is capable of performing the recited function, but rather whether the corresponding structure is "clearly linked or associated with the [recited] function." *Id.* The corresponding structure "must include all structure that actually performs the recited function." *Default Proof Credit Card Sys. v. Home Depot U.S.A., Inc.*, 412 F.3d 1291, 1298 (Fed. Cir. 2005). However, § 112, ¶ 6 does not permit "incorporation of structure from the written description beyond that necessary to perform the claimed function." *Micro Chem., Inc. v. Great Plains Chem. Co.*, 194 F.3d 1250, 1258 (Fed. Cir. 1999).

III. LEGAL ANALYSIS

A. Term #1: "predetermined level"

Term	Plaintiff's Proposed Construction	Defendant's Proposed Construction
"predetermined level" U.S. Patent No. 6,496,939, Claims 1, 10	Plain and ordinary meaning.	"a preset minimum operating voltage necessary for proper operation, in which the super capacitors are not fully discharged"

<u>The Parties' Positions:</u>

Defendants contend that its construction is correct because (1) the patentee acted as its own lexicographer and (2) the patentee relied on this specific meaning during prosecution to differentiate the invention from the prior art. Opening at 4.

With respect to the former, Defendants contend that the specification "explains that the 'predetermined level' is a preset minimum operating voltage at which 'the down-converter has ***insufficient voltage differential to continue proper operation*** and shuts down.'" *Id.* at 3 (quoting '939 patent at 5:39–43 (emphasis in Defendants' brief); citing '939 Patent at 6:40–44, 5:44–48, 5:48–52, 6:49–53). Defendants contend that the specification explains that if the predetermined voltage level were allowed to fall below the minimum operating voltage of the computer system, the computer system might run with "***unpredictable and potentially serious results***." *Id.* (quoting '939 Patent at 5:44–48 (emphasis in Defendants' brief); citing '939 Patent at 6:45–49). Defendants contend that this would undermine one of the goals of the invention (to correctly store large amounts of newly written and modified data) and also has the advantage of reducing the time needed to recharge the super-capacitor. *Id.* (citing '939 Patent at 2:33–41, 5:48–52, 6:49–53).

With respect to the latter, Defendants contend that Applicant stated that setting the predetermined voltage level above the minimum operative voltage of the computer system improves the "performance and reliability of the computer system" and decreases the time needed to recharge the super capacitor. *Id.* at 3–4 (quoting Opening, Ex. I at 7 (amend. Filed on May 8, 2002)).

Defendants contend that Plaintiff's proposed construction of plain-and-ordinary meaning is incorrect in light of the patentee's lexicography and reliance on a critical feature that differentiated the prior art during prosecution. *Id.* at 4.

In its response, Plaintiff contends that "predetermined level" is an "ordinary term that both laypersons and POSITAs readily understand." Response at 3 (citing *Ferguson Beauregard/Logic Controls, Div. of Dover Res., Inc. v. Mega Sys., LLC*, 350 F.3d 1327, 1340 (Fed. Cir. 2003)). Plaintiff contends that the claims uses the term consistent with its plain meaning. *Id.* at 3–4.

Plaintiff contends that Defendants have not provided any reason for diverging from that plain meaning. *Id.* at 4 (citing cases). With respect to Defendants' lexicography argument, Plaintiff contends that "there is no definition of 'predetermined level' in the portions of the specification cited in [Defendants'] brief" nor do any of the passages cited by Defendants rise to the level of a clear and unmistakable disclaimer. *Id.* at 5.

With respect to Defendants' history argument, Plaintiff contends that the statements cited by Defendants only distinguished a prior art reference cited by Examiner. *Id.* Plaintiff further contends that Applicant's statements were "exemplary," *e.g.*, "can be set," which further indicates that Applicant did not disavow any claim scope. *Id.*

Plaintiff finally contends that "predetermined level" is used in contemporary patents in the same subject matter. *Id.* (citing Intel's patents).

In their reply, Defendants contend that Plaintiff does not dispute that (1) the "specification describes a predetermined level as a preset minimum operating voltage at which the down-converter has insufficient voltage differential to continue proper operation and shuts down," (2) "the specification establishes the importance of setting the predetermined level at a voltage necessary for proper operation," and (3) "a threshold set below a minimum operating voltage necessary for proper operation would fatally undermine the '939 patent's stated goals." Reply at 1 (citing'939 patent at 5:39,–43, 5:44–48, 6:45–49, 2:33–41). Based on those assertions, Defendants contend that the patentee acted as their own lexicographer. *Id.* Defendants further contend that specification "establishes the critical importance of having the predetermined level fixed at a preset minimum operating voltage necessary for proper operation confirms Defendants' proposed construction." *Id.* at 1-2 (citing '939 Patent at 5:44–48, 6:45–49; citing cases).

With respect to the prosecution history, Defendants contend that Plaintiff admits that it distinguished prior art from the claimed invention based on the limitations described in Defendants' proposed construction. *Id.* at 2.

With respect to the other patents Plaintiff cites to, Defendants contend that those are unrelated patents which merit "little consideration." *Id.*

In its sur-reply, Plaintiff contends that Defendants have not identified anything that "compels the import of the two limitations in their construction" nor anything in the specification or prosecution history that is lexicography. Sur-Reply at 1. Plaintiff contends that Defendants' proposed construction improperly attempts to limit the claim scope to a single embodiment. *Id.* at 1–2 (citing cases). With respect to Defendants' argument that its proposed construction accomplishes the stated goals of the '939 Patent, Plaintiff contends that Defendants mischaracterize the goals of the patent. *Id.* at 2. More specifically, Plaintiff contends that the passage that discusses the goals of the patent does not mention "minimum operating voltage necessary for proper operation." *Id.*

<u>The Court's Analysis:</u>

After reviewing the parties' arguments and considering the applicable law, the Court agrees with Plaintiff and finds that the proper construction is plain-and-ordinary meaning for the reasons that follow. ***First***, the "heavy presumption" is that terms should be construed according to their plain-and-ordinary meaning. *Azure Networks*, 771 F.3d at 1347.

Second, the Court disagrees with Defendants that the patentees acted as their own lexicographer as the evidence that Defendants provide does not meet the "exacting" standard necessary for finding lexicography. *Hill-Rom Servs.*, 755 F.3d at 1371. More specifically, this

term appears in the specification twice, but neither time does it recite any of the language in Defendants' proposed construction. '939 Patent at 5:39–43 ("Finally, once the super-capacitors discharge to a predetermined level, the down-converter has insufficient voltage differential to continue proper operation and shuts down, thus turning off the power to the computer system, via step 110."), 6:40–44 ("Finally, once the super-capacitors discharge to a predetermined level, the down-converter has insufficient voltage differential to continue proper operation and shuts down, thus turning off the power to the computer system, via step 310."). Accordingly, the Court concludes that the patentee did not act as their own lexicographer as the patentee did not "clearly set forth a definition of the disputed claim term other than its plain and ordinary meaning" nor "clearly express[ed] an intent to redefine the term." *Hill-Rom Servs.*, 755 F.3d at 1371.

Third, the Court disagrees with Defendants that Applicant disclaimed claim scope during prosecution. A disclaimer needs to be clear and unambiguous. *Liebel-Flarsheim*, 358 F.3d at 900. But here, the passages from the prosecution history that Defendants cite to merely describes that the prior art does not disclose various limitations of the claimed invention. *Computer Docking Station Corp. v. Dell, Inc.*, 519 F.3d 1366, 1375 (Fed. Cir. 2008) ("Prosecution disclaimer does not apply, for example, if the applicant simply describes features of the prior art and does not distinguish the claimed invention based on those features.").

Fourth, the Court concludes that "predetermined level" is a simple, non-technical claim term that is easily understood by a lay jury. By contrast, the Court concludes that Defendants' proposed construction—"a preset minimum operating voltage necessary for proper operation, in which the super capacitors are not fully discharged"—is both more technical and more complicated, and thus it is unlikely to help a lay jury understand the meaning of this claim term. *Sulzer Textil A.G. v. Picanol N.V.*, 358 F.3d 1356, 1366 (Fed. Cir. 2004) ("The district court simply

must give the jury guidance that can be understood and given effect by the jury once it resolves the issues of fact which are in dispute.”).

Therefore, for the reasons described above, the Court’s final construction for “predetermined level” is plain-and-ordinary meaning.

B. Term #2: “means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level”

Term	Plaintiff’s Proposed Construction	Defendant’s Proposed Construction
“means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level” U.S. Patent No. 6,496,939, Claim 10	**Function**: deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level. **Structure**: Col. 3:3-12, 3:28-4:8, 5:35-42, 6:37-44, Figs. 1, 3, 5, of the ’939 Patent, and equivalents thereof.	Indefinite under 35 U.S.C. § 112: Lacks corresponding structure.

The Parties’ Positions:

Defendants contend that because the specification does not “clearly link” any structure to the recited function of “deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level,” the term is indefinite. Opening at 5. Defendants contend that the specification describes “deactivating” using “generic functional language,” but that does not describe structure. *Id.* at 6 (citing cases). Defendants further contend that the specification does not disclose a structure that “deactivates” a plurality of super capacitors, but only discusses “deactivating” an up-converter and

a down-converter. *Id.* at 6–7. Defendants contend that the specification does not link deactivation an up-converter and a down-converter with the deactivation of a plurality of super capacitors. *Id.* at 7. Accordingly, Defendants contend that the specification does not "clearly link" any structure to the recited function. *Id.* at 8.

Defendants contend that Plaintiff's proposed construction is a "laundry list of figures and paragraphs, which is an "absurdly overinclusive designation fails to identify a sufficiently definite structure that corresponds to the claimed function." *Id.* (quoting *Bell N. Research, LLC v. Coolpad Techs.*, Inc., No. 18-CV-1783-CAB-BLM, 2019 WL 3766688, at *6 (S.D. Cal. Aug. 9, 2019)). Defendants contend that Plaintiff's citations either make "no mention of 'deactivating' anything, much less a super capacitor," or discuss the deactivation of other components, *e.g.*, up-converter or down-converter. *Id.* at 9.

In its response, Plaintiff contends that because "activating" and "deactivating" are "two sides of the same coin," disclosures of structure, acts, and methods relevant to "activating" are relevant to "deactivating." Response at 6, 8 n.4. Plaintiff contends that Defendants did not challenge the "activating" limitation in Claim 10 given this disclosure. *Id.* at 6–7.

Plaintiff contends that the specification discloses circuity (charge level sensors 30, up-converter 32, thermal heater 36, temperature sensors & control 38, and down-converter 42) that is the corresponding structure. *Id.* at 7–8. More specifically, Plaintiff contends that once the down-super capacitors have discharged to a predetermined level, the down converter shuts down, thus turning off power to the computer system. *Id.* (quoting '939 Patent at 5:17–43). Plaintiff contends that once the down-converter turns off, other circuit elements may turn on. *Id.* at 8. Based on this, Plaintiff contends that Defendants cannot meet their burden of showing by clear and convincing

evidence that the specification lacks "disclosure of structure sufficient to be understood by one skilled in the art as being adequate to perform the cited function." *Id.* (citing cases).

Plaintiff contends that the above disclosures contradict Defendants' argument that the specification does not disclose the corresponding structure. *Id.* at 8–9. Plaintiff further contends that it is not clear what Defendants think "deactivating" capacitors means in this context and what structure satisfies that functionality. *Id.* at 9.

Plaintiff contends that the claim language explains that deactivating a capacitor means to cut off power to the computing engine. *Id.*

Plaintiff contends that Defendants do not provide expert evidence regarding indefiniteness which is "fatal" to their case. *Id.* at 8.

In their reply, Defendants contend that the passages Plaintiff cites does not describe deactivating any component, let alone the super capacitor. Reply at 3. Defendants contend that Plaintiff never explains what "deactivating a plurality of supercapacitors" means and that Plaintiff is not able to do so because the patent does not address this issue, let alone identify any structure that performs this function. *Id.* Defendants contend that the specification only indicate that charge level sensors 30 "inform the computer system that the super-capacitor voltage has fallen below the fully charged and partially charged levels," but does not indicate that they "deactivate" the super-capacitors. *Id.* at 4 (quoting '939 patent at 5:36–39, 6:37–40). Defendants contend that down-converter simply converts a high voltage into a lower voltage and that there is nothing to indicate that the down-converter "deactivates" the super capacitors. *Id.* Defendants contend that Plaintiff does not point to any structure that is "clearly linked" to the claimed function and thus the claim is indefinite. *Id.* (citing cases).

Defendants contend that Plaintiff's argument that "means for activating" and "means for deactivating" are two sides of the same coin is flawed because different terms are presumed to have different meanings. *Id.* at 4–5 (*Bd. of Regents of the Univ. of Tex. Sys. v. BENQ Am. Corp.*, 533 F.3d 1362, 1371 (Fed. Cir. 2008)). Defendants further contend that the claim language describes that "activating" describes power being removed from the computer system while "deactivating" describes the super capacitor discharging (into the computer system). *Id.* at 5.

Defendants contend that Plaintiff's suggestion that expert testimony is required for a finding of indefiniteness "misstates the applicable law." *Id.* (citing cases).

In its sur-reply, Plaintiff contends that the plain meaning of "deactivating the plurality of super capacitors" is to make them electrically inactive. Sur-Reply at 3. Plaintiff contends that a construction would not help a POSITA or jury. *Id.* Plaintiff contends that

> structure consists of the "charge level sensors 30," which informs the computer system whether the plurality of capacitors have discharged to a predetermined level, the "down converter DC 42," which turns off or shuts down thereby disconnecting the plurality of super capacitors from the rest of the system and accordingly "cut[ting] off power to the computing engine," and other related circuitry (like the power isolator and up converter that revert to their original states).

Id. at 4. Plaintiff contends that Defendants have not identified what structure would be required to activate a super capacitor. *Id.* Plaintiff contends that "a 1:1 mapping of structure and claim is clearly evident." *Id.*

<u>The Court's Analysis:</u>

Because the parties do not dispute that the term is governed by § 112, ¶ 6 and because the term contains the word "means," the Court concludes that this term is subject to § 112, ¶ 6.

The parties appear to agree that the claimed function is "deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level," and the Court concurs.

With respect to the corresponding structure, the Court concludes that a POSITA would understand that "deactivating" a capacitor means that the capacitor is electrically disconnected such that it is not discharging current to a load, *e.g.*, the computing engine, for at least two reasons. ***First***, the claim language describes that "deactivating the plurality of super capacitors" electrically disconnects the super capacitors from the computing engine ("to cut off power to the computing engine"). ***Second***, the specification describes that the super capacitor down-converter is "deactivated" once when the computer system determines the external power system has risen back to normal levels. *See, e.g.*, '939 Patent at 5:52–57. And by "activating" the up-converter, the computer system recharges the super capacitor. *Id.* But in order to prevent the down-converter continuing to discharge the super capacitor, the down-converter needs to be electrically disconnected (*i.e.*, "deactivated") from the super capacitor. *Id.* at 5:39–43 ("Finally, once the super-capacitors discharge to a predetermined level, the down-converter has insufficient voltage differential to continue proper operation ***and shuts down, thus turning off the power to the computer system***, via step 110.") (emphasis added).

Although the Court agrees with Defendants that the specification does not expressly describe "deactivating" a super capacitor, the claimed function describes that "deactivating a super-capacitor" "cuts off power to the computing engine." The Court concludes that because deactivating a down-converter also electrically disconnects a super capacitor from the down-converter such that power is cut-off to the computing engine, a POSITA would understand that is equivalent to "deactivating a super-capacitor."

Based on the aforementioned analysis, the Court concludes that the specification "clearly links" down-converter 42 to the claimed function of "means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level." In addition, the Court concludes that other circuit elements, *e.g.*, switches, transistors, gates, *etc.*, could be corresponding structure as they are generally known in the art. *Apple*, 757 F.3d at 1299 ("A limitation has sufficient structure when it recites a claim term with a structural definition that is either provided in the specification or generally known in the art.").

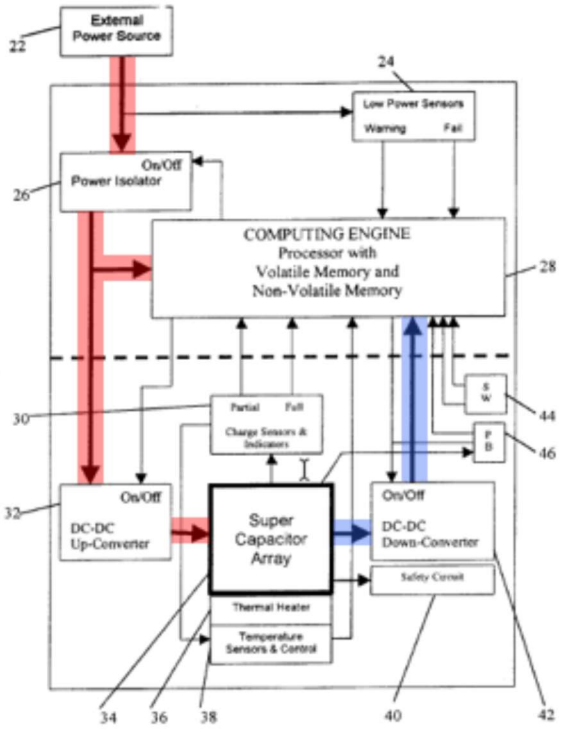
Therefore, for the reasons described above, the Court concludes that this term is subject to § 112, ¶ 6, the claimed function is "deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level," and the corresponding structure is down-converter 42 in Figure 1 (and corresponding text), and equivalents thereof, and switches, transistors, gates, *etc.* that are generally known in the art.

C. Term #3: "reversing the flow of current between the computing engine and the plurality of super capacitors"

Term	Plaintiff's Proposed Construction	Defendant's Proposed Construction
"reversing the flow of current between the computing engine and the plurality of super capacitors" U.S. Patent No. 6,496,939, Claim 6	Plain and ordinary meaning; not indefinite.	Indefinite.

The Parties' Positions:

Defendants contend that the term is indefinite because it is "inconsistent with the description of the alleged invention in the specification[.]" Opening at 9 (citing cases). Defendants contend that the specification describes that current only flows in one direction—between the external power source to the super capacitors to the computing engine. *Id.* at 10. More specifically, Defendants annotate Figure 1 to show that current flows in a unidirectional way between external power source 22 to super capacitor array 34 via the power isolator 26 and up-converter 32 (red) and from super capacitor array 34 to computing engine 28 via down-converter 42 (blue). *Id.* at 10–11.



Defendants contends that the specification does not teach otherwise; although they contend that 6:27–28 is "clearly an error" as the patent does not otherwise suggest or disclose that current can flow from the volatile memory (in the computing engine) to the super capacitors. *Id.* at 9–10 (citing '939 patent at 5:24–26).

In its response, Plaintiff contends that the specification makes clear that "reversing" the current refers to the "change in the flow of current in the system from the normal state (when power is supplied by the EPS to the computing engine and to the capacitors to charge them) and backup state (when power is supplied from the capacitors to the computer engine)." Response at 11. Plaintiff contends that the external power supply, power isolator, and computing engine exists on one "power plane" while the super capacitor exists on another power plane, therefore, the current flow "reverses" from one power plane to another. *Id.*

In their reply, Defendants contend that claim language requires that the current be reversed between computing engine and the super capacitors, but the specification describes that current flows in the opposite direction. *Id.* at 6. Defendants contend that to truly be reverse current, the current needs to flow from the computing engine to the super capacitors along the same path. *Id.* at 7. But because Plaintiff's argument relies on two different paths, that means that there is no "reverse" current. *Id.*

In its sur-reply, Plaintiff contends that Defendants do not provide an expert declaration in support of its indefiniteness position. Sur-Reply at 4. Plaintiff contends that the dotted line in Figure 1 separates the external power source and computing engine from the super capacitor, which indicates that the former and latter are in different power planes. *Id.* Plaintiff contends that "Defendants' admission that current flows in one direction when external power is supplied, and another direction when power is supplied by the capacitors, is entirely consistent with how a POSITA and jury would understand the claim." *Id.*

Plaintiff contends that "Defendants' fallback argument–that the claim language requires the 'computing engine' to provide power to super capacitors when external power is being

supplied—is technical to a fault," but rather that the claims should be understood in light of the specification. *Id.* at 5.

The Court's Analysis:

After reviewing the parties' arguments and considering the applicable law, the Court agrees with Plaintiff that this term is not indefinite and should be construed according to its plain-and-ordinary meaning for at least the reasons that follow. ***First***, there does not appear to be any dispute that "reversing the flow of current between the computing engine and the plurality of super capacitors" simply means that the current flows in the opposite direction, *i.e.*, from the super capacitors to the computing engine instead of the other way around. This indicates that the parties understand what the claim term means and thus it is not indefinite.

Second, the Court disagrees with Defendants that "reversing the flow of current" requires that current flow in the opposite direction on the same path. Rather, the claim language recites that the "flow of current" is reversed between the computing engine and plurality of super capacitors. The plain meaning of that claim language appears to be broad enough to include one path or multiple paths, so long as the current flow goes in the opposite direction between the computing engine and plurality of super capacitors. Additionally, Defendants have not identified any disclosure in the specification that describes that requires that "reverse" current flow be on the same path as the "forward" current.

Third, with respect to Defendants' argument that this claim term is inconsistent with the description of the alleged invention in the specification as the specification only discloses unidirectional paths, the Court disagrees. Defendants' argument relies on the current flowing forward and in reverse on the same path. But, as described immediately above, the "reversing the

flow of current" is not limited to a single path. Furthermore, even if the specification only describes unidirectional paths, the Court concludes that Defendants' argument presupposes limiting the claim term to the disclosed embodiments that utilize unidirectional paths. But it is improper to limit a claim scope, let alone to presuppose that a claim term is limited to a disclosed embodiment, in order to find that its indefinite. *Liebel-Flarsheim*, 358 F.3d at 913 ("[I]t is improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited."). Finally, even if the specification only discloses unidirectional paths, at most, the Court concludes that is a written description issue and not a claim construction one.

Construction: Because the "heavy presumption" is that terms should be construed according to their plain-and-ordinary meaning and because Defendants does not allege lexicography or disclaimer, which are the only two exceptions to the general rule that a term should be construed as having its plain-and-ordinary meaning, the Court concludes that the term should be construed as having its plain-and-ordinary meaning. *Azure Networks*, 771 F.3d at 1347; *Thorner*, 669 F.3d at 1365.

Therefore, for the reasons described above, the Court finds that the term is not indefinite and should be construed according to its plain-and-ordinary meaning.

D. Term #4: "means for reversing the flow of current between the computing engine and the plurality of super-capacitors"

Term	Plaintiff's Proposed Construction	Defendant's Proposed Construction
"means for reversing the flow of current between the computing engine and the plurality of super-capacitors" U.S. Patent No. 6,496,939, Claim 15	**Function**: reversing the flow of current between the computing engine and the plurality of super capacitors. **Structure**: Col. 3:3-12, 3:28-4:8, 6:22-28, Figs. 1, 3, 5, of the '939 Patent, and equivalents thereof.	Indefinite under 35 U.S.C. § 112(6): Lacks corresponding structure.

The Parties' Positions:

Defendants contend that the term is indefinite for (1) failing to disclosing the recited function (as was explained with respect to Term #3) and (2) failing to disclose "sufficient" corresponding structure. Opening at 12. Defendants contend that Plaintiff fails to identify specific structure that allegedly corresponds to the recited "reversing" function. *Id.*

In its response, Plaintiff contends that "[t]his term is not indefinite for the same reasons as discussed with respect to the previous term. And the disclosures recited with respect to that term and the 'deactivating' term above also identify the corresponding structure, *i.e.*, the 'circuit[r]y' in the cited passages of the specification." Response at 12.

In their reply, Defendants contend that the specification does not teach this functionality and that Plaintiff does not identify any structure other than "generic circuitry." Reply at 7.

In its sur-reply, Plaintiff contends that this term is not indefinite for the same reasons that Term #3 is not indefinite. Sur-Reply at 5. Plaintiff contends that passages recited with respect to this term and the "deactivating" term identify the corresponding structure. *Id.*

The Court's Analysis:

Because the parties do not dispute that the term is governed by § 112, ¶ 6 and because the term contains the word "means," the Court concludes that this term is subject to § 112, ¶ 6.

The parties appear to agree that the claimed function is "reversing the flow of current between the computing engine and the plurality of super-capacitors," and the Court concurs.

With respect to the corresponding structure, as described above, there does not appear to be any dispute that "reversing the flow of current between the computing engine and the plurality of super capacitors" simply means that the current flows from the super capacitors to the computing engine instead of the other way around. The specification describes that activating the down-converter and deactivating the up-converter causes current to flow in the reverse direction, *i.e.*, from the super capacitor to the computing engine. *See, e.g.*, '939 Patent at 5:19–24, 5:52–57. Therefore, the specification discloses that down-converter 42 and up-converter 42 are corresponding structure.

Therefore, for the reasons described above, the Court concludes that this term is subject to § 112, ¶ 6, the claimed function is "reversing the flow of current between the computing engine and the plurality of super-capacitors," and the corresponding structure is down-converter 42 and up-converter 42 in Figure 1 (and corresponding text), and equivalents thereof.

E. Term #5: "optimized memory operations"

Term	Plaintiff's Proposed Construction	Defendant's Proposed Construction
"optimized memory operations" U.S. Patent No. 8,010,740, Claim 1	Plain and ordinary meaning; not indefinite.	Indefinite.

The Parties' Positions:

Defendants contend that this term is indefinite because the claim and specification do not provide any criteria for assessing whether the memory operations have been optimized. Opening at 19. Defendants contend that the only way that the specification "teaches only one way to 'optimally distribute' operational load and thus optimize memory transactions—*i.e.*, to map LBA sets to PBA fields such that memory transactions across multiple LBA sets can be conducted in parallel." *Id.* at 20.

Defendants contend that the specification teaches that "[f]or memory transactions across two or more LBA sets to be conducted in parallel, one or more of the access parameters associated with the LBA sets must be different." *Id.* (citing '740 Patent at 2:14–22; 7:9–18, 9:19–25). Defendants contend that Claim 1 does not require that the first and second LBA sets must be different, but that Claim 2 does require that difference. *Id.* at 21. Defendants contend that given that the specification teaches that LBA sets must be different to be optimized, that collapses the difference between Claims 1 and 2, which renders Claim 1 indefinite.

In its response, Plaintiff contends that "optimized" is not indefinite as it is readily understandable to both a layperson and a POSITA. Response at 21.

Plaintiff contends that during prosecution Examiner rejected the draft claims pursuant to § 112, ¶ 1 but ultimately withdrew the rejection based on Plaintiff's response that "the specification teaches how a 'mapping table' causes a 'storage device to perform optimized memory operations,'" and Applicant's citation to specific paragraphs disclosing different examples of such optimized memory operations. *Id.* Plaintiff contends that a POSITA would understand that this term has a definite meaning in light of the arguments Applicant presented during prosecution and Examiner's acceptance of those arguments. *Id.* at 21-22.

Plaintiff contends that Defendants are incorrect that the specification only teaches only one way to "optimally distribute" operational load and thus optimize memory transactions, but rather that the specification teaches multiple optimizations including "contiguous arrangement of LBA sets (6:46-54, 6:63-7:2), adjacency between LBA sets (6:55-62), and adjacent PBAs differing by at least one access parameter (7:3-6). *Id.* at 22. As such, given that the specification describes multiple ways to perform "optimized memory operations." Plaintiff contends that there is no claim differentiation problem between Claims 1 and 2. *Id.*

Plaintiff contends that Defendants' claim differentiation argument also fails because Claim 2 recites another limitation ("said first and second LBA sets are adjacent LBA sets") not present in Claim 1. *Id.* at 22–23. More specifically, Plaintiff contends that Figure 2 depicts a situation where "[d]istributing memory operations across LBA sets 40 and 45 based on their different access parameters would therefore constitute "optimized memory operations" falling within the scope of claim 1, but not claim 2." *Id.* Plaintiff contends that Claim 2 recites yet another limitation ("said LBAs from said first and second LBA sets are logical block addresses used by the host for addressing said data.") that differentiates it from Claim 1. *Id.* at 23 (citing cases).

Plaintiff finally contends that Defendants do not offer any expert testimony in support of their indefiniteness position, which prevents Defendants from meeting their burden of indefiniteness. *Id.* at 24.

In their reply, Defendants contend that the claim language "provides no performance index and no hint of objective criteria against which to assess memory operations." Reply at 11. Defendants contend that Plaintiff's prosecution history arguments fail because Examiner's rejection was a § 112, ¶ 1 written description rejection and not § 112, ¶ 2 indefiniteness. *Id.* at 12.

Defendants contend that Plaintiff is incorrect that there are multiple disclosed optimizations. *Id.* More specifically, Defendants contend that Claim 1 "requires that memory operations—and not the mapping table—to be optimized," and the optimizations Plaintiff alleges are actually directed towards the mapping table. *Id.*

Defendants contend that Plaintiff "erroneously" argues that non-adjacent LBA sets 40 and 45 in Figure 2 could be an example of Claim 1, but not Claim 2, as Claim 2 requires adjacent sets. *Id.* at 12–13. Defendants contend that Figure 2 shows that LBA sets 40 and 42 which are recited in claim 2 and that any time there are more 3 or more LBA sets, there will be non-adjacent LBA sets. *Id.* at 13.

Defendants finally contend that an additional limitation that allegedly differentiates Claims 1 and 2 ("are logical block addresses used by the host for addressing said data") does not differentiate the two claims because the specification defines "LBA" in that manner. *Id.* (quoting '740 Patent at 6:37–40 ("The term 'LBA'. . . is intended to represent an address that is part of a logical addressing system … used by a host.").

In its sur-reply, Plaintiff contends that Defendants have not shown by clear and convincing evidence that this term is indefinite. Sur-Reply at 8.

With respect to the prosecution history, Plaintiff contends that it does not matter what type of rejection Applicant was responding to, as it matters only that Applicant made certain statements that would help a POSITA understand the scope of that term with reasonable certainty. *Id.* at 8–9.

Plaintiff finally contends that Defendants do not offer any expert testimony in support of their indefiniteness position, which prevents Defendants from meeting their burden of indefiniteness. *Id.* Plaintiff contends that the cases that Defendants cite in support of the

proposition that expert testimony is not required, Plaintiff contends that all those cases are inapposite. *Id.*

With respect to Defendants' arguments regarding adjacent LBA sets, Plaintiff contends that Defendants' argument makes "no sense." *Id.* at 10. More specifically, Plaintiff contends that the issue is not whether a mapping table contains LBA sets that are adjacent to another LBA set, but rather which of the LBA sets are involved in the optimized memory operations. *Id.* Plaintiff contends that Claim 1 "covers optimized memory operations where the I/O transaction request is associated with any two LBA sets in the mapping table, regardless of whether they are adjacent or non-adjacent." Plaintiff contends that Claim 2, by contrast, is limited to optimized memory operations where the I/O transaction request is associated with adjacent LBA sets. *Id.*

The Court's Analysis:

After reviewing the parties' arguments and considering the applicable law, the Court agrees with Plaintiff that this term is not indefinite and should be construed according to its plain-and-ordinary meaning for at least the reasons that follow. ***First***, the Court agrees with Plaintiff that the specification discloses multiple optimizations, including contiguous LBA sets, adjacent LBA sets, adjacent PBAs differing by at least one access parameter. '740 Patent at 6:55–7:19. Because the specification teaches that there are other methods of optimizing memory operations (apart from "mapping LBA sets to PBA fields such that memory transactions across multiple LBA sets can be conducted in parallel"—which Defendants allege is the only way to optimize memory operations), Defendants' argument that there is no difference in claim scope between Claims 1 and 2 is incorrect. Accordingly, because there is a difference in claim scope, Defendants' argument that Claim 1 is indefinite because it has the same claim scope as Claim 2 is also incorrect.

Second, the Court agrees with Plaintiff that Defendants' claim differentiation argument also fails because Claim 2 contains additional limitations that Claim 1 does not. More specifically, Claim 2 includes a limitation that requires "said first and second LBA sets are adjacent LBA sets[.]" '740 Patent, Claim 2 (emphasis added).

With respect to Defendants' argument that Figure 2 depicts adjacent sets and that there will be adjacent LBA sets whenever there are more than three LBA sets in the mapping table, the Court does not find Defendants' argument to be persuasive as the optimized memory operations is not based on whether there are any adjacent LBA sets, but rather which adjacent LBA sets are involved in the optimized memory operations.

Third, even if Defendants are correct that Claim 1 and Claim 2 has the same scope, Defendants do not appear to explain why Claim 1—and not Claim 2—is indefinite for having the same claim scope.

Based on the above, the Court concludes that Defendants have not shown that this term is indefinite by clear and convincing evidence.

Construction: Because the "heavy presumption" is that terms should be construed according to their plain-and-ordinary meaning and because Defendants does not allege lexicography or disclaimer, which are the only two exceptions to the general rule that a term should be construed as having its plain-and-ordinary meaning, the Court concludes that the term should be construed as having its plain-and-ordinary meaning. *Azure Networks*, 771 F.3d at 1347; *Thorner*, 669 F.3d at 1365.

Therefore, for the reasons described above, the Court finds that the term is not indefinite and should be construed according to its plain-and-ordinary meaning.

F. Term #6: "optimally distributed"

Term	Plaintiff's Proposed Construction	Defendant's Proposed Construction
"optimally distributed" U.S. Patent No. 8,010,740, Claim 32	Plain and ordinary meaning; not indefinite.	Indefinite.

<u>The Parties' Positions:</u>

Defendants contend that this term is also indefinite for "similar" reasons as for Term #5. Opening at 22. Defendants contend that Claim 32 requires "at least one difference between the first and second PBAs, but does not recite that the "I/O transaction is associated with two LBA sets." *Id.* But Defendants contend that Claim 34 does require that the I/O transaction is associated with two LBA sets. *Id.* (quoting '740 Patent, Claim 34 ("wherein the processing of the I/O transaction request includes a first memory operation performed using said first PBA and a second memory operation performed using said second PBA")). Defendants contend that Claim 32 "covers optimal distribution in the case where there is only a single set of LBAs[,]" but because "the patent provides no guidance as to how that is possible, [it] leav[es] the scope of the claim indefinite." *Id.*

In its response, Plaintiff contends that Defendants' indefiniteness argument fails for the "same reasons" as their indefiniteness arguments failed for Term #5. Response at 24. More specifically, Plaintiff contends that the specification discloses "multiple examples of optimally distributing data operations across storage device resources based on[.]" *Id.* Plaintiff also contends that during prosecution, Applicant pointed out passages from the specification where "optimally distributed" was taught. *Id.*

Plaintiff contends that Defendants are wrong to argue that Claim 32 is indefinite because it could cover an "optimal distribution where there is only a single set of LBAs." *Id.* at 24–25. More specifically, Plaintiff contends that Claim 32 on its face requires two LBAs. *Id.* at 25 (citing '740 Patent at 13:36–39 ("a mapping table which maps a first LBA set to a first PBA, and a second LBA set to a second PBA, said first and second LBA sets including respective sets of consecutive LBAs.")). Plaintiff contends that there is no claim differentiation issue between Claims 32 and 34 as the latter "simply specifies that the memory operations to be performed are 'using said first PBA and . . . said second PBA,'" while the former "leaves open the possibility that the mapping table is used for optimally distributing memory operations over other PBAs." *Id.*

In their reply, with respect to Plaintiff's argument that Defendants argue that Claim 32 covers a mapping table with just one LBA set, Defendants contend that Plaintiff "mischaracterizes" Defendants actual argument. Reply at 13. Rather, Defendants contend that Claim 32 does not limit I/O transaction requests with memory operations that use just one PBA, but dependent Claim 34 requires using two PBAs. *Id.* Defendants contend that because the '740 Patent "says nothing about how to achieve that outcome with an I/O transaction using just one PBA, leaving the scope of the 'optimally distributed' limitation indefinite." *Id.* at 14.

Defendants also contend that expert testimony is not required for an indefiniteness finding. *Id.* at 14 n.4.

In its sur-reply, Plaintiff contends that Defendants' arguments for this term fail for the same reason they failed for Term #5. Sur-Reply at 10. Plaintiff contends that, contrary to Defendants' allegation that Claim 32 does encompasses memory operations that use just one PBA, Claim 32's recitation that the operational load is "distributed across storage device resources" necessarily requires that multiple PBAs are involved in order to be "optimally distributed." *Id.* at 10–11

(quoting '740 Patent at 9:19–25). Plaintiff finally contends that that Claim 32 does not specify which PBAs are used for memory operations while Claim 34 identifies memory operations using "said first PBA" and "said second PBA." *Id.* at 11.

The Court's Analysis:

After reviewing the parties' arguments and considering the applicable law, the Court agrees with Plaintiff that this term is not indefinite and should be construed according to its plain-and-ordinary meaning for at least the reasons that follow. ***First***, the parties' make the same arguments for this term as for Term #5, so the Court's analysis and reasoning also apply to this term. ***Second***, with respect to Defendants' argument that this term is indefinite because '740 Patent "says nothing about how to achieve that outcome with an I/O transaction using just one PBA," the Court disagrees because Claim 32 necessarily requires that multiple PBAs. More specifically, Claim 32 recites that "the processing of the I/O transaction request will be optimally distributed ***across storage device resources***," which requires at least one PBA for each of the storage device resources. (emphasis added).

Construction: Because the "heavy presumption" is that terms should be construed according to their plain-and-ordinary meaning and because Defendants does not allege lexicography or disclaimer, which are the only two exceptions to the general rule that a term should be construed as having its plain-and-ordinary meaning, the Court concludes that the term should be construed as having its plain-and-ordinary meaning. *Azure Networks*, 771 F.3d at 1347; *Thorner*, 669 F.3d at 1365.

Therefore, for the reasons described above, the Court finds that the term is not indefinite and should be construed according to its plain-and-ordinary meaning.

G. Term #7: "memory store"

Term	Plaintiff's Proposed Construction	Defendant's Proposed Construction
"memory store" U.S. Patent No. 8,010,740, Claims 1, 15, 32	"non-volatile, solid-state storage, e.g., flash"	Plain and ordinary meaning.

<u>The Parties' Positions:</u>

Defendants contend that the plain-and-ordinary meaning of this term is not "non-volatile, solid-state storage, e.g., flash," which is Plaintiff's proposed construction. Opening at 23. Defendants contend that Claims 7, 8, and 15—which depend on Claim 1—specifically recite that the "memory store" comprises either a "plurality of flash devices or a "set of solid state memory devices." *Id.* Defendants contend that Claim 17 recite that a "memory store" includes " a first and second set of memory devices," and that Claim 19, which depends on Claim 17, further recites that the "first and second set of memory devices" includes "non-volatile solid state memory cells." *Id.* Defendants contend that because the dependent claims expressly limits the "memory store" to solid state and flash devices, based on the doctrine of claim differentiation, these limitations cannot be read into the broader construction of "memory store." *Id.*

Defendants contend that this conclusion is further confirmed by asserted claims 15 and 32. *Id.* at 24. More specifically, Defendants contend that because which these claims recite that the claimed "memory store" "***includes*** a set of [solid state memory devices / flash devices]," the use

of the word "includes" indicates that "memory is not limited to solid state memory devices and flash devices. *Id.* (emphasis in Defendants' brief).

Defendants contend that the specification also refutes Plaintiff's narrow construction. *Id.* More specifically, Defendants contend that "nothing in the specification expressly disclaims the use of devices other than solid-state storage devices." *Id.* Defendants contend that, by contrast, the specification describes "[m]emory store 6 ***may be configured to include*** a set of solid state memory devices that are coupled to a set of buses and that are controlled by a set of FDEs." *Id.* (citing '740 Patent at 4:54–56) (emphasis in Defendants' brief). Defendants contend that "may be configured to include" confirms that solid state memory devices are permitted, but not required. *Id.* Defendants contend that the specification also recites that "[t]he term 'flash memory device,' which constitutes one example of a memory store, 'is intended to include any form of non-volatile memory, including those that use blocks of non-volatile memory cells, named flash blocks.'" *Id.* (quoting '740 Patent at 4:59–62).

Defendants contend that Plaintiff's complaint in a related case filed with this Court demonstrates that it understood that the plain-and-ordinary meaning of "memory store" is not limited to non-volatile, solid state storage. *Id.* at 25. Defendants contend that Plaintiff's complaint in that related case recites "the Optane Persistent Memory product ***includes both DRAM memory and persistent memory modules***, ***which separately*** or in combination ***are a memory store***." *Id.* (quoting 6:22-cv-00335, ECF No. 1 at ¶ 106).

Defendants finally contend that extrinsic evidence (dictionary definitions) indicates that plain-and-ordinary meaning of "memory store" is not limited to non-volatile, solid state storage. *Id*. at 25–26.

In its response, Plaintiff contends that its proposed construction is consistent with the specification as the specification "equates 'memory store' with solid-state storage, with flash as one example of such storage." Response at 25.

> Memory store 6 may be configured to include a set of solid state memory devices that are coupled to a set of buses and that are controlled by a set of FDEs. In FIG. 1, these memory devices, buses, and FDEs are implemented in the form of flash memory devices 12-01 and 12-02; buses 8-0 and 8-1; and FDEs 22-01, 22-02, 22-11, and 22-12, respectively. The term "flash memory device" is intended to include any form of non-volatile memory, including those that use blocks of nonvolatile memory cells, named flash blocks.

'740 Patent at 4:54–62. Plaintiff contends that "may be configured" in the above passage describes configuring busses and FED control, and not configuring different types of memory stores that are not solid state memory devices. Response at 25. Plaintiff contends that Claims 15 and 32 do not support Defendants' argument because the "includes a set of [solid state memory devices / flash devices]" in those claims is actually directed towards configurations apart from the solid state memory devices and flash devices. *Id.* at 26.

With respect to Defendants' argument that the specification's description that "flash memory device" "is intended to include any form of non-volatile memory," Plaintiff contends that that argument "makes no sense" as the specification uses the term "solid state storage" interchangeably with "non-volatile memory." *Id.* (quoting '740 Patent at 1:28–32 ("Electronic storage devices . . . that use non-volatile memory cells are commonly known and are sometimes referred to as solid state storage devices.")).

Plaintiff contends that Defendants' claim differentiation arguments with respect to Claims 7, 8, 15, 17, and 19 lack merit because those claims include multiple additional limitations, but claim differentiation is inapplicable" where a dependent claim adds multiple limitations. *Id.* (citing cases).

In their reply, with respect to Plaintiff's arguments regarding the above block quote, Defendants contend that the passage describes that a memory store "'may be configured to ***include*** a set of solid state memory devices' and is not focused on the manner of coupling." Reply at 14.

Defendants contend that Plaintiff is wrong that additional limitations in a dependent claim does not implicate claim differentiation. *Id.* at 14–15 (citing *Pisony v. Commando Constr., Inc.*, No. W-17-CV-00055-ADA, 2019 WL 928406, at *3 (W.D. Tex. Jan. 23, 2019)).

Defendants contend that if "memory stores" were limited to "solid state memory devices," then Claim 15 would redundantly recite "wherein said memory store includes a set of ~~solid state memory devices~~ [memory stores]…" *Id.* (alterations in Defendants' brief).

With respect to Plaintiff's contention that the specification "equates" "solid state storage" with "non-volatile memory," Defendants disagrees. *Id.* (quoting'740 Patent at 1:28–32 ("Electronic storage devices that respectively employ a memory system that includes memory devices, memory chips, or modules that use non-volatile memory cells are commonly known and are sometimes referred to as solid state storage devices.")). More specifically, Defendants contend that the passage actually describes that "electronic storage devices"—and not "non-volatile memory"–are sometimes referred to as "solid state storage devices." *Id.* Defendants contend, in fact, that because Claim 19 recites "non-volatile solid state memory cells," a "non-volatile memory device need not be a solid state storage device[]." *Id.*

In its sur-reply, Plaintiff again contends that the "may be configured" language in the specification does not open the possibility that the memory store includes memory devices other than solid state memory devices, as Defendants contend, but rather opens the possibility of different configurations in which the "solid state memory devices can be connected in the memory store." Sur-Reply at 11.

Plaintiff contends that Figure 1 depicts Flash Buffer Controller 16. *Id.* at 11–12. Plaintiff contends that the Background section of the patent is focused on describing the state of the art in "solid state storage devices" and "flash drives." *Id.* at 12.

With respect to Defendants' claim differentiation arguments, Plaintiff contends that claim differentiation is "most applicable" when there is a dispute whether the limitation in the dependent claim is the "only meaningful difference" between the two claims. *Id.* (citing *RF Delaware, Inc. v. Pacific Keystone Techs., Inc.*, 326 F.3d 1255, 1263 (Fed. Cir. 2003)). Plaintiff contends that none of the dependent claims fit this description and thus claim differentiation is inapplicable here.

The Court's Analysis:

After reviewing the parties' arguments and considering the applicable law, the Court agrees with Plaintiff and finds that the proper construction is plain-and-ordinary meaning for the reasons that follow. ***First***, the "heavy presumption" is that terms should be construed according to their plain-and-ordinary meaning. *Azure Networks*, 771 F.3d at 1347. ***Second***, Defendants do not expressly allege lexicography or disclaimer, which are the only two exceptions to the general rule that a term should be construed as having its plain-and-ordinary meaning. *Thorner*, 669 F.3d at 1365.

Third, the claim language indicates that "memory store" is not coextensive with "non-volatile, solid-state storage." For example, Claims 7 and 8 recite that the "memory store includes a flash memory devices that each have a native page size," while Claim 15 recites that the "memory store includes a set of solid state memory devices." Claims 17 and 19 collectively recite that the "memory store includes a first set of memory devices and a second set of memory devices," wherein "said first and second memory devices include non-volatile solid state memory cells."

Claim 32 recites that "a memory store that includes a set of flash devices[.]" The plain language of these claims indicates that "memory store" includes, but is not limited to, "flash memory devices" (Claims 7, 8, and 32), "a set of solid state memory devices" (Claim 15), or "non-volatile solid state memory cells" (Claims 17 and 19).

Fourth, the Court agrees with Defendants that if "memory stores" were limited to "solid state memory devices," as Plaintiff contends, then Claim 15 would redundantly recite "wherein said memory store includes a set of [memory stores]." The circular nature of Plaintiff's proposed construction inserted in Claim 15 indicates that "memory stores" are not limited to "solid state memory devices."

Fifth, the Court agrees with Defendants that the specification does not equate "memory store" with "solid-state storage." The disputed passage recites that "[m]emory store 6 may be configured to include a set of solid state memory devices that are coupled to a set of buses and that are controlled by a set of FDEs," describes that the "solid state memory devices" are one type of "memory store." But the Court agrees with Defendants that the passage describes that "memory store 6 may … include a set of solid state memory devices," *i.e.*, memory stores include, but are not limited to, non-volatile, solid-state storage. Rather, at most, the passage describes that "memory store 6" may comprise of a specific type of memory ("a set of solid state memory devices") that is arranged in a specific manner ("coupled to a set of buses and that are controlled by a set of FDEs"), which does not equate "memory store" with "solid-state storage."

Sixth, the Court agrees with Defendants that the passage "[e]lectronic storage devices . . . that use non-volatile memory cells are commonly known and are sometimes referred to as solid state storage devices," describes that "electronic storage devices"—and not "non-volatile memory cells" "are sometimes referred to as solid state devices."

Seventh, in a related case, Plaintiff's complaint recites "the Optane Persistent Memory product includes both ***DRAM memory and persistent memory modules***, which ***separately*** or in combination ***are a memory store***." 6:22-cv-00335, ECF No. 1 at ¶ 106. This statement from Plaintiff's complaint indicates that Plaintiff understood that memory store is not coextensive with non-volatile, solid-state storage.

Plaintiff's argument that this statement was made without the benefit of discovery does not persuade the Court. Evidence produced in discovery is extrinsic evidence, which is "less significant than the intrinsic record," which was available at the time of the filing of the complaint. *Phillips*, 415 F.3d at 1318.

Eighth, extrinsic evidence confirms that the plain-and-ordinary meaning of "memory store" is not limited to non-volatile, solid state storage. Opening, Exs. G, H.

Ninth, the Court is not persuaded by Plaintiff's argument that Figure 1 depicts a flash buffer controller and thus the proper construction of "memory store" should be "non-volatile, solid-state storage." The Court concludes that Figure 1 is merely an embodiment and that it would be improper to limit the scope of this claim term to this embodiment. *Liebel-Flarsheim*, 358 F.3d at 913 ("[I]t is improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited.").

Therefore, for the reasons described above, the Court's final construction for "memory store" is plain-and-ordinary meaning.

H. Term #8: "optimal"

Term	Plaintiff's Proposed Construction	Defendant's Proposed Construction
"optimal" U.S. Patent No. 9,135,190, Claims 1, 29, 45, 59, 80, 98	Plain and ordinary meaning; not indefinite.	Indefinite.

<u>The Parties' Positions:</u>

Defendants contend that it is unclear from the specification what criteria would make a device profile optimal for a particular data type. Opening at 28. Defendants contend that, "at most," the specification provides three examples of potentially optimal device profiles, but does not explain which example to use. *Id.* at 28–29 (citing '190 Patent at 9:16–26 (data type is sequential), 9:27–35 (data type is random), 9:35–43 (data type is random and "data size of the data subject to the write transaction is at most equal to the partial page size attribute value")).

Defendants contend that the facts of this case are similar to those in *Intellectual Ventures I LLC v. T Mobile USA, Inc.*, No. 2:17-CV-00577-JRG, 2018 WL 5809267, at *4-5 (E.D. Tex. Nov. 6, 2018) where the court found "optimal" to be indefinite because the specification did not provide boundaries on what was optimal, despite providing two definitions of what constituted optimal performance. *Id.* at 29.

In its response, Plaintiff contends that "optimal" is an "ordinary" word that both laypersons and POSITA understand. Response at 28. Plaintiff contends that the claim language describes that "the attributes of the first memory location are better for a data type than the second memory location, where the data type is either random or sequential." *Id.*

Plaintiff contends that the plain meaning of this term is consistent with the specification; namely, that the multi-profile controller can support memory locations that have different device

profiles that are optimal for different data types. *Id.* (citing '190 Patent at 9:7–16). Plaintiff contends that the specification also provides examples of how that determination could be made; namely, "'the largest available' block size attribute for sequential data types, the 'smallest available' block size attribute for random data types, and 'partial page size attribute' 'at most equal' to "the data size of the data' being written for random data types." *Id.* (citing '190 Patent at 9:16–43). Plaintiff further contends that the specification recites that "[f]lash memory devices that have a relatively large block size generally provide better sequential memory access performance than flash memory devices that use smaller block sizes." *Id.* at 29 (quoting 1:27–31). Based on that, Plaintiff contends that "a larger block size attribute is more 'optimal' for sequential data than random data, and vice versa." *Id.*

With respect to Defendants argument that the specification does not provide a comprehensive list of examples, Plaintiff contends that "comprehensiveness is not a requirement for definiteness." *Id.*

In their reply, Defendants contend that the term is indefinite because the patent "does not explain how a memory device would select an optimal device profile based on a data type in the innumerable situations the device might encounter." Reply at 16. Defendants contend that the examples in the specification "do not address the full scope of the claims, which extend to device profile optimization in all events." *Id.*

In its sur-reply, with respect to Defendants' "innumerable" argument, Plaintiff contends the claims only use "optimal" with respect to random and sequential data types. Sur-Reply at 13. Based on that, Plaintiff contends that "optimal" "simply means that the first device profile is better for either random or sequential data" and that the specification provides guidance for "at least three different examples of device profiles that are better for handling random or sequential data

depending on how the attributes in the device profile are set." *Id.* (citing'190 Patent at 9:16–43). Plaintiff finally contends that Defendants' argument that three examples is not enough guidance for a POSITA is pure attorney argument.

The Court's Analysis:

After reviewing the parties' arguments and considering the applicable law, the Court agrees with Plaintiff that this term is not indefinite and should be construed according to its plain-and-ordinary meaning for at least the reasons that follow. ***First***, the Court agrees with Plaintiff that rather there being "innumerable situations that the device might encounter," the claim language focuses on whether the device profile is "optimal" for the random or sequential data types only. *See, e.g.*, '190 Patent, Claim 1, Limitation [b] ("wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type"). ***Second***, the three examples that the specification provides are directed towards random data type or a sequential data type; namely, the specification recites: (1) a device profile that includes a block size attribute value that is the largest available from the other device profiles when the data type is sequential (*id.* at 9:16–26), (2) a device profile that includes a block size attribute value that is the smallest available from the other device profiles" when the data type is random (*id.* at 9:27–35), and (3) a device profile that includes a partial page size attribute value when the data type is random and the data size of the data subject to the write transaction is at most equal to the partial page size attribute value (*id.* at 9:35–43).

Therefore, based on the fact that the claim language focuses on whether the device profile is "optimal" for the random or sequential data types and because specification provides guidance on which device profile to use for the random or sequential data types in the form of three

examples, the Court concludes that Defendants have not carried their burden of showing the claim term is indefinite by clear and convincing evidence.

Construction: Because the "heavy presumption" is that terms should be construed according to their plain-and-ordinary meaning and because Defendants does not allege lexicography or disclaimer, which are the only two exceptions to the general rule that a term should be construed as having its plain-and-ordinary meaning, the Court concludes that the term should be construed as having its plain-and-ordinary meaning. *Azure Networks*, 771 F.3d at 1347; *Thorner*, 669 F.3d at 1365.

Therefore, for the reasons described above, the Court finds that the term is not indefinite and should be construed according to its plain-and-ordinary meaning.

IV. CONCLUSION

In conclusion, for the reasons described herein, the Court adopts the below constructions as its final constructions.

SIGNED this 16th day of February 2023.

ALAN D ALBRIGHT
UNITED STATES DISTRICT JUDGE

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Preliminary Construction
#1: "predetermined level" U.S. Patent No. 6,496,939, Claims 1, 10	Plain and ordinary meaning.	"a preset minimum operating voltage necessary for proper operation, in which the super capacitors are not fully discharged"	Plain-and-ordinary meaning
#2: "means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level" U.S. Patent No. 6,496,939, Claim 10	**Function**: deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level. **Structure**: Col. 3:3-12, 3:28-4:8, 5:35-42, 6:37-44, Figs. 1, 3, 5, of the '939 Patent, and equivalents thereof.	Indefinite under 35 U.S.C. § 112: Lacks corresponding structure.	Subject to § 112, ¶ 6, **Function**: deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level **Structure:** down-converter 42 in Figure 1 (and corresponding text), and equivalents thereof, and switches, transistors, gates, *etc.* that are generally known in the art.
#3: "reversing the flow of current between the computing engine and the plurality of super capacitors" U.S. Patent No. 6,496,939, Claim 6	Plain and ordinary meaning; not indefinite.	Indefinite.	Not indefinite. Plain-and-ordinary meaning.

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Preliminary Construction
#4: "means for reversing the flow of current between the computing engine and the plurality of super-capacitors" U.S. Patent No. 6,496,939, Claim 15	**Function**: reversing the flow of current between the computing engine and the plurality of super capacitors. **Structure**: Col. 3:3-12, 3:28-4:8, 6:22-28, Figs. 1, 3, 5, of the '939 Patent, and equivalents thereof.	Indefinite under 35 U.S.C. § 112(6): Lacks corresponding structure.	Subject to § 112, ¶ 6, **Function**: : reversing the flow of current between the computing engine and the plurality of super capacitors **Structure:** down-converter 42 and up-converter 42 in Figure 1 (and corresponding text), and equivalents thereof.
#5: "optimized memory operations" U.S. Patent No. 8,010,740, Claim 1	Plain and ordinary meaning; not indefinite.	Indefinite.	Not indefinite. Plain-and-ordinary meaning.
#6: "optimally distributed" U.S. Patent No. 8,010,740, Claim 32	Plain and ordinary meaning; not indefinite.	Indefinite.	Not indefinite. Plain-and-ordinary meaning.
#7: "memory store" U.S. Patent No. 8,010,740, Claims 1, 15, 32	"non-volatile, solid-state storage, e.g., flash"	Plain and ordinary meaning.	Plain-and-ordinary meaning

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Preliminary Construction
#8: "optimal" U.S. Patent No. 9,135,190, Claims 1, 29, 45, 59, 80, 98	Plain and ordinary meaning; not indefinite.	Indefinite.	Not indefinite. Plain-and-ordinary meaning.