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11/450,005

06/08/2006

Mark Arcedera

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7174

64180

7590

03/17/2008

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EXAMINER

FARROKH, HASHEM

ART UNIT

PAPER NUMBER

2187

MAIL DATE

DELIVERY MODE

03/17/2008

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

|                              |                                      |                                        |  |
|------------------------------|--------------------------------------|----------------------------------------|--|
| <b>Office Action Summary</b> | <b>Application No.</b><br>11/450,005 | <b>Applicant(s)</b><br>ARCEDERA ET AL. |  |
|                              | <b>Examiner</b><br>HASHAM FARROKH    | <b>Art Unit</b><br>2187                |  |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 08 June 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 is/are rejected.
- 7) ☒ Claim(s) 2-8 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 January 2008 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |                                                                                      |                                                                   |
|--------------------------------------------------------------------------------------|-------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____                                                          | 6) <input type="checkbox"/> Other: _____                          |

*The instant application having application No. 11/450,005 has a total of 8 claims pending in the application; there are 1 independent claim and 7 dependent claims, all of which are ready for examination by the examiner.*

**INFORMATION CONCERNING CLAIMS:**

***Claim Objections***

*Claim 3 is objected to because of the following informalities: claim 3 has a “;” as a claim terminator, a claim must be terminated with a period”.*

*Appropriate correction is required.*

***Claim Rejections - 35 USC § 102***

*The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:*

*A person shall be entitled to a patent unless –*

*(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.*

*Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,822,251 to Bruce et al. (hereinafter Bruce).*

1. *In regard to claim 1 Bruce teaches:*

**“An apparatus (e.g., Fig. 2) for data storage comprising:”**

**“a plurality of flash buses;” (e.g., Flash Bus-A 10 and Flash Bus-B 18 in Fig. 2).**

“a plurality of DMA Engines coupled to at least two of the plurality of flash buses;” **(e.g., Flash Specific DMA 12 and 16 in Fig. 2).**

“a plurality of flash devices coupled to at least two of the plurality of DMA Engines;” **(e.g., Flash Chips 14 in Fig. 2).**

“wherein data access performance is improved by bus interleaving wherein one or more data is transferred to or from the plurality of flash devices using at least two flash buses;” **(e.g., see column 6, lines 59-60; column 17, lines 33-35).** *A plurality of chips or devices is accessed (e.g., for data transfer) by two DMA controller using two flash buses (see definition of interleaving in page 9, lines 12-19 of the instant specification).*

“wherein data access performance is improved by flash array bank interleaving wherein one or more data is transferred to or from the plurality of flash devices using at least two DMA Engines;” **(e.g., see column 17, lines 23-25; column 6, lines 57-58).**

“and wherein data access performance is improved by group interleaving wherein one or more data is transferred to or from the plurality of flash devices using at least two flash devices.” **(e.g., see column 6, lines 59-60).** *A plurality of chips or devices is accessed by a DMA controller using one flash bus.*

***Allowable Subject Matter***

*Claims 2-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.*

2. *The primary reason for allowance of claims 2-8 in instant application is the combination of claim limitations with inclusion of the following limitation: **wherein each of the plurality of flash devices further comprises a plurality of sections; wherein each section in the apparatus is operable to be accessed using a physical block address comprising a least significant portion, a second least significant portion, a third least significant portion, and a fourth least significant portion; wherein the least significant portion comprises an order according to the plurality of flash buses, the second least significant portion comprises an order according to a plurality of DMA Engines each coupled to a same flash bus, the third least significant portion comprises an order according to a plurality of flash devices each coupled to a same DMA Engine, and the fourth least significant portion comprises an order according to the plurality of sections in a same flash device;***

### **Conclusion**

*The prior art made of record and not relied upon are as follows:*

1. *U. S. Patent Publication No. 2004/0073721 A1 to Goff et al. describes DMA Controller for USB and like applications.*
2. *U. S. Patent Publication No. 2002/0141244 A1 to Bruce et al. describes Parallel erase operations in memory systems.*

3. *U. S. Patent Publication No. 2003/0217202 A1 to Zilberman et al.*  
*describes Method for improving performance of a flash-based storage system using specialized flash controllers.*

*Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached on 8-5.*

*If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571)272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.*

*Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.*

*/Hashem Farrokh/  
Patent Examiner  
Art Unit 2187*

3/02/08

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

|                                           |   |                          |
|-------------------------------------------|---|--------------------------|
| In re Application of: ARCEDERA, et al.    | ) | Group Art Unit: 2187     |
|                                           | ) |                          |
| Serial No.: 11/450,005                    | ) | Examiner: Hashem Farrokh |
|                                           | ) |                          |
| Application Filing Date: 08 June 2006     | ) |                          |
|                                           | ) |                          |
| For: OPTIMIZED PLACEMENT POLICY FOR SOLID | ) |                          |
| STATE STORAGE DEVICES                     | ) |                          |
| <hr/>                                     |   |                          |

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**AMENDMENT AND REPLY TO FIRST OFFICE ACTION**

Dear Sir:

In response to the Office Action, mailed 17 March 2008, please kindly amend this Application as follows and consider the remarks set forth below.

Amendments to the specification begin on page 2;

A listing of claims begins on page 3; and

Remarks begin on page 6 of this paper.

### **Amendment(s) to the Specification**

In the specification, please enter the following amendments.

Please replace the paragraph on pages 8, lines 19 through page 9, line 2, with the following replacement paragraph:

The flash array organization comprises a set of Flash DMA Engines controlling multiple flash devices across a set of flash buses. The set of flash devices assigned to a particular flash bus is called a “flash array bank”. Each bank can be partitioned into any number of flash array banks with the Flash DMA Engines sharing a flash bus. For example in Figure 1, it is shown that a group of n number of Flash DMA Engines, such as group 105, shares ~~is sharing~~ a single Flash Bus0 106.

Please replace the paragraph on page 9, lines 4 through 10, with the following replacement paragraph:

Each Flash DMA Engine[[s]] is assigned to control a set of flash devices. This set of flash devices is said to belong to a flash array bank interleave. In addition, each flash device within this interleave is said to belong to a different flash group. From Figure 1, all flash chips labeled ‘A0’ within flash array bank interleave 107 is controlled by Flash DMA Engine A0 and each of the flash device within this interleave belongs to a different group. For example, the first flash device A0 108 belongs to Group 0, second flash device A0 109 belongs to Group 1, and so on.

**Listing of Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (CANCELLED): An apparatus for data storage comprising:  
  
a plurality of flash buses;  
  
a plurality of DMA Engines coupled to at least two of the plurality of flash buses; and  
  
a plurality of flash devices coupled to at least two of the plurality of DMA Engines;  
  
wherein data access performance is improved by bus interleaving wherein one or more data is transferred to or from the plurality of flash devices using at least two flash buses;  
  
wherein data access performance is improved by flash array bank interleaving wherein one or more data is transferred to or from the plurality of flash devices using at least two DMA Engines; and  
  
wherein data access performance is improved by group interleaving wherein one or more data is transferred to or from the plurality of flash devices using at least two flash devices.
2. (CURRENTLY AMENDED): [[The apparatus of claim1]] An apparatus for data storage comprising:  
  
a plurality of flash buses;  
  
a plurality of DMA Engines coupled to at least two of the plurality of flash buses;  
  
a plurality of flash devices coupled to at least two of the plurality of DMA Engines;  
  
wherein data access performance is improved by bus interleaving wherein one or more data is transferred to or from the plurality of flash devices using at least two flash buses;

wherein data access performance is improved by flash array bank interleaving wherein one or more data is transferred to or from the plurality of flash devices using at least two DMA Engines;

wherein data access performance is improved by group interleaving wherein one or more data is transferred to or from the plurality of flash devices using at least two flash devices;

wherein each of the plurality of flash devices further comprises a plurality of sections;

wherein each section in the apparatus is operable to be accessed using a physical block address comprising a least significant portion, a second least significant portion, a third least significant portion, and a fourth least significant portion;

wherein the least significant portion comprises an order according to the plurality of flash buses, the second least significant portion comprises an order according to a plurality of DMA Engines each coupled to a same flash bus, the third least significant portion comprises an order according to a plurality of flash devices each coupled to a same DMA Engine, and the fourth least significant portion comprises an order according to the plurality of sections in a same flash device; and

wherein a logical block address for host data access is mapped to a physical block address according to a placement algorithm whereby host data access performance is improved.

3. (CURRENTLY AMENDED) The apparatus of claim 2:

wherein at least one section in at least one of the plurality of flash devices is designated as a free section; and

wherein at least one free section is pre-erased as target for at least one data relocation wherein [whereby] flash write performance and bad block replacement performance are improved according to the placement algorithm.

4. (PREVIOUSLY PRESENTED) The apparatus of claim 3:

wherein the placement algorithm maps each logical block address to a physical block address in a linear mapping prior to the at least one data relocation; and

wherein the placement algorithm designates a plurality of free sections evenly to each of the plurality of flash devices.

5. (CURRENTLY AMENDED) The apparatus of claim 4, wherein the placement algorithm locates a target for each of the at least one data relocation for write operation according to a current load represented in a system queue based on a priority comprising firstly locating a free section corresponding to a different flash bus, secondly locating a free section corresponding to a different DMA Engine coupled to a same flash bus, and thirdly locating a free section corresponding to a different flash device coupled to a same DMA Engine.
6. (CURRENTLY AMENDED) The apparatus of claim 4, wherein the placement algorithm locates a target for each of the at least one data relocation for bad block management based on a priority comprising firstly locating a free section corresponding to a same flash device, secondly locating a free section corresponding to a different flash device coupled to a same DMA Engine, and thirdly locating a section corresponding to a different DMA Engine coupled to a same flash bus.
7. (PREVIOUSLY PRESENTED) The apparatus of claim 4:  
  
wherein each section further comprises a plurality of stripes; and  
  
wherein the linear mapping further comprises one or more flash device interleaves.
8. (PREVIOUSLY PRESENTED). The apparatus of claim 7:  
  
wherein data striping occurs in more than one flash device.

### **Remarks**

The specification has been amended to correct minor grammatical errors. These corrections are of a clerical nature and do not add "new matter".

Claim 1 has been cancelled without prejudice.

Claims 2, 3, 5 and 6 have been amended to particularly point out and distinctly claim subject matter regarded as the invention. The text of claims 4, 7 and 8 is unchanged from the respective previous versions of these claims, but the meaning of these claims is changed because they depend from amended claims.

### **Correction of Inadvertent Omission of Markings Necessary for Showing Inclusion of New Text in Amended Claims**

Claims 2, 5 and 6 include amendments that correct the inadvertent omission of markings necessary to show the addition of new text in an amended claim. In the preliminary amendment filed on behalf of the Applicants on 2 January 2008, the proposed amendment, "DMA [[e]]Engines", was proposed for claims 1, 2, 5 and 6, among others. The inclusion of the capitalized character "E" in the proposed amendment, however, was inadvertently shown without underlining in the Listing of Claims of the preliminary amendment. Consequently, in this amendment, claims 2, 5, and 6 have been amended in this response to include the underlining of the capitalized form of the character "E" in all locations in the claims where underlying was inadvertently omitted. Since claim 1 has been cancelled, the correction to claim 1 has not been made in this response. It is believed that these amendments do not add new matter or otherwise necessitate a new search by the Examiner.

### **Informal Objections by the Examiner**

The Examiner objects to claim 3 by asserting that it contains "the following informalities: claim 3 has a ".,," as a claim terminator, a claim must be terminated with a period ".,," "

Claim 3 has been amended as shown: "wherein at least one section in at least one of the plurality of flash devices is designated as a free section; and".

With this amendment it is respectfully submitted that claim 3 satisfies the statutory

requirements.

In addition, claim 3 has been further amended as shown: “wherein at least one free section is pre-erased as target for at least one data relocation wherein [whereby] flash write performance and bad block replacement performance are improved according to the placement algorithm. This further amendment is of a clerical nature and does not add new matter.

#### The Section 102(b) Rejection

The Examiner rejected claim 1 by asserting that it is anticipated by Bruce et al. in United States patent 5,822,251. This rejection is now rendered moot since Claim 1 has been cancelled without prejudice.

#### Dependent Claims 2-8

The Examiner objected to claims 2-8 by asserting they depend upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

Claims 2-8 have been so amended, rendering these claims allowable.

#### Request for Allowance

It is believed that this Amendment places this Application into condition for allowance. Early favorable consideration of this Amendment is earnestly solicited.

Respectfully submitted,

Dated: 27 June 2008

/Stephen R. Uriarte/  
Stephen R. Uriarte, Reg. No. 40,854

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