

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KIOXIA AMERICA, INC. and
KIOXIA CORPORATION,
Petitioners,

v.

BiTMICRO, LLC,
Patent Owner.

Case IPR2023-00742
Patent 8,010,740

PATENT OWNER'S PRELIMINARY RESPONSE

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Pursuant to 37 C.F.R. § 42.107, Patent Owner BiTMICRO, LLC (“BiTMICRO” or “Patent Owner”) files this preliminary response to the Petition, setting forth reasons why the Petition for *inter partes* review (“IPR”) of claims 1, 9-15, 32, and 34 of U.S. Patent No. 8,010,740 (the “’740 Patent”), as requested by Kioxia America, Inc. and Kioxia Corporation (“Petitioners”), should be denied.¹

I. INTRODUCTION

The ’740 Patent is entitled “OPTIMIZING MEMORY OPERATIONS IN AN ELECTRONIC STORAGE DEVICE” and relates to “solutions for optimizing memory operations in a memory system suitable for use in an electronic storage device.” See ’740 Pat., 1:16–18. As an example of such a solution, the ’740 Patent describes and claims an improved “mapping table” that may increase “the likelihood that, in response to an I/O transaction initiated by a host, the operational load imposed on the storage device by these memory operations will be optimally distributed across different storage device resources” by “interleaving or [performing] parallel memory operations, reducing memory operation latency, increasing operational device efficiency,” or a combination thereof. ’740 Pat., 2:14–21.

¹ By submitting this Preliminary Response, no waiver of any argument is intended by Patent Owner. Patent Owner will have a right to file a complete response to the Petition, should the Board institute *inter partes* review. 37 C.F.R. § 42.120(a).

A. The ’740 Patent Discloses a Mapping Table Designed to Correlate Logical Block Addresses and Physical Block Addresses

The ’740 Patent illustrates an exemplary “mapping table for an electronic storage device” in FIG. 2, also reproduced below. ’740 Pat., 2:58-60.

Logical Fields 26	PBA Fields 28			
	Access Parameter Fields 30			Memory Index Fields 32
	Bus Id Fields 34	FDE Id Fields 36	Group Id Fields 38	
LBAs 00-07	8-0	22-01	15-0	0x00
LBAs 08-15	8-0	22-02	15-1	0x08
LBAs 16-23	8-1	22-11	15-0	0x00
LBAs 24-31	8-1	22-12	15-1	0x08
⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮

FIG. 2

The physical block address (PBA) Fields 28 illustrated in the mapping table of FIG. 2 include Access Parameter Fields 30 and Memory Index Fields 32. The illustrated Access Parameter Fields 30 include Bus ID Fields 34, FDE ID Fields 36, and Group ID Fields 38. These Access Parameter Fields 30 illustrated in the mapping table of FIG. 2 are explained further with reference to FIG. 1, which illustrates an exemplary electronic storage device using the mapping table of FIG. 2. This electronic storage device of FIG. 1 is reproduced below:

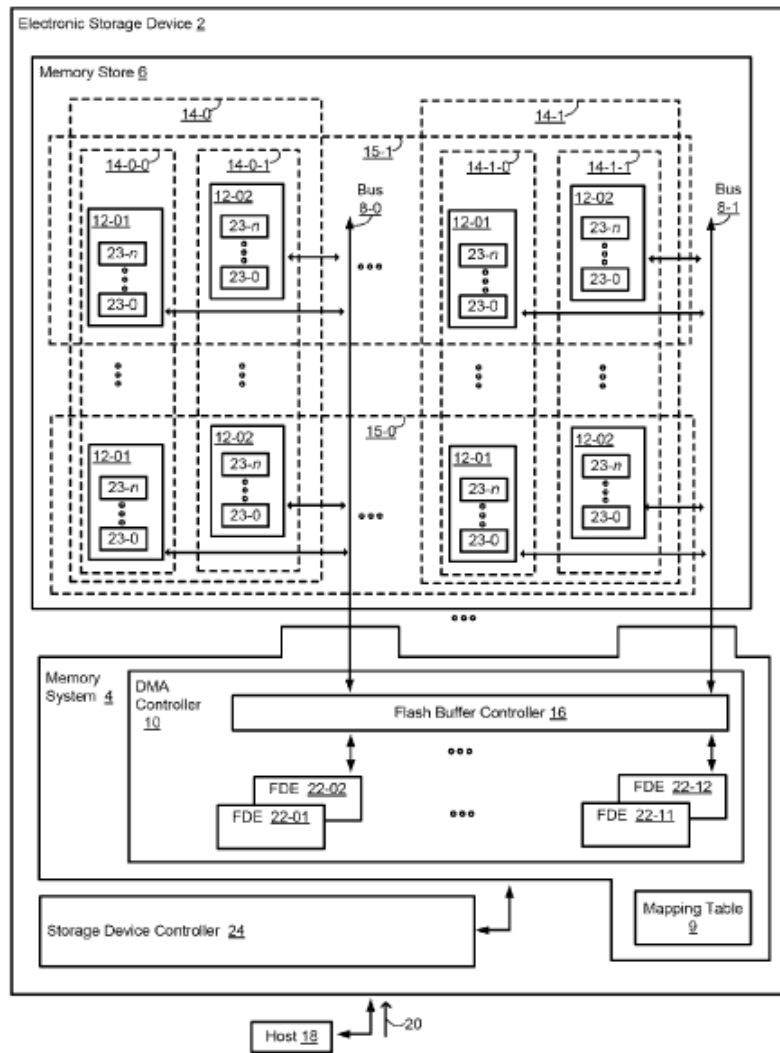


FIG. 1

The electronic storage device 2 of FIG. 1 includes direct memory access engines (FDEs) 22-01, 22-02, 22-11, and 22-12 to control flash memory devices 12-01 and 12-02 and perform DMA (direct memory access) operations on the flash memory devices 12-01 and 12-02. Flash memory devices 12-01 and 12-02 are arranged into flash array banks 14-0 and 14-1, and also into flash array bank interleaves 14-0-0, 14-0-1, 14-1-0, and 14-1-1. FDEs 22-01 and 22-02 control and

communicate with selected flash array bank interleaves 14-0-0 and 14-0-1 of flash array bank 14-0 via bus 8-0. Similarly, FDEs 22-11 and 22-12 control and communicate with selected flash array bank interleaves 14-1-0 and 14-1-1 of flash array bank 14-1 via bus 8-1. As shown in FIG. 1, the '740 Patent also assigns different group identifiers 15-0 and 15-1 to flash memory devices 12-01 and 12-02. As the '740 Patent explains, two flash memory devices 12-01 and 12-02 accessed via a common bus, such as bus 8-0, can share a common group number 15-0 or 15-1 if “these flash devices are controlled by different FDEs, such as FDEs 22-01 or 22-02, respectively.” '740 Pat., 6:15-21.

Returning to the mapping table of FIG. 2, the Access Parameter Fields 30, including Bus ID Fields, FDE ID Fields, and Group ID Fields, associate LBAs (logical block addresses) with corresponding PBAs (physical block addresses). By mapping consecutive LBAs to adjacent PBAs that “differ by at least one access parameter,” the mapping table of FIG. 2 “increases the likelihood that memory operations resulting from an I/O transaction request will be optimized because if these memory operations involve data accesses associated with contiguous LBA sets these data accesses will in [all] likelihood occur on different PBAs.” '740 Pat., 7:3-15. For example, a memory operation resulting from an I/O transaction request and involving data accesses associated with consecutive LBAs 40 and 42

shown in FIG. 2 would access different memory devices in different FDE ID Fields and different Group ID Fields, as shown below.

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Logical Fields 26	PBA Fields 28			
	Access Parameter Fields 30			Memory Index Fields 32
	Bus Id Fields 34	FDE Id Fields 36	Group Id Fields 38	
LBAs 00-07	8-0	22-01	15-0	0x00
LBAs 08-15	8-0	22-02	15-1	0x08
LBAs 16-23	8-1	22-11	15-0	0x00
LBAs 24-31	8-1	22-12	15-1	0x08
⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮

FIG. 2

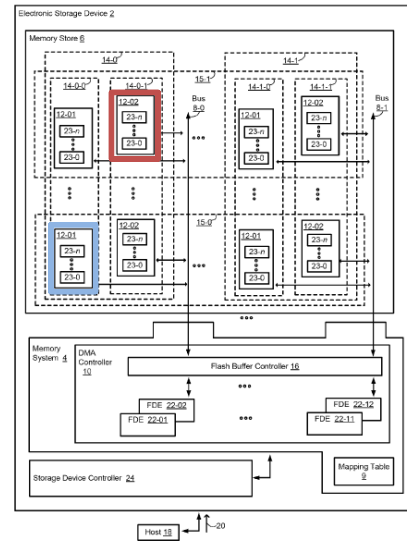


FIG. 1

B. Introduction to the Challenged Claims and Petitioners' Deficient Challenges

Consistent with this disclosure, the challenged claims each recite in relevant part a “mapping table,” and recite additional features and relationships consistent with those described in the '740 Patent specification and discussed above.

Independent claim 1 is specifically directed to a “mapping table for optimizing memory operations performed by an electronic storage device,” while independent claim 32 is directed to an “electronic storage device” comprising, *inter alia*, a “mapping table” having specifically claimed features. Claim 1 recites in full:

1. A mapping table for optimizing memory operations performed by an electronic storage device in response to receiving an I/O transaction request initiated by a host, said mapping table comprising:

a set of logical fields, including a first logical field and a second logical field, and said logical fields respectively disposed for representing a plurality of LBA sets, including said first logical field disposed for representing a first LBA set and said second logical field disposed for representing a second LBA set, said first and second LBA sets each representing a set of consecutive LBAs;

a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for representing a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs; and

wherein, in response to receiving the I/O transaction request, said mapping table causes the electronic storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second LBA sets.

'740 Pat., 9:63-10:24. Challenged claims 9-15 each depend directly or indirectly from claim 1. Independent claim 32 recites in full:

32. An electronic storage device that includes a memory system that uses a memory table for increasing the likelihood that an operational load imposed on the storage apparatus during the processing of an I/O transaction request will be optimally distributed across storage device

resources, said I/O transaction request received by said storage device from a requesting host, said electronic storage device comprising:
a mapping table which maps a first LBA set to a first PBA, and a second LBA set to a second PBA, said first and second LBA sets including respective sets of consecutive LBAs;
a memory store that includes a set of flash devices, said set of flash devices includes a first physical memory location and a second physical memory location that are addressable by said first and second PBAs respectively;
a memory system coupled to said memory store and disposed to use said mapping table during a memory operation;
wherein said first PBA includes a first set of access parameters and said second PBA includes a second set of access parameters, and at least one difference between said first and second PBAs;
and wherein said mapping table increases the likelihood that the operational load imposed on the storage apparatus during the processing of the I/O transaction request will be optimally distributed across storage device resources.

'740 Pat., 13:29-14:5. Claim 34 depends from claim 32.

Petitioners assert four grounds against challenged claims 1, 9-15, 32, and 34. In Ground 1, Petitioners contend that challenged claims 1, 32, and 34 are anticipated by the Sukegawa² reference. However, in this challenge, Petitioners

² U.S. Patent No. 5,572,466 ("Sukegawa").

fail to address every claimed feature, including the claim 1 requirement that the “I/O transaction request is associated with said first and second LBA sets.”

In Ground 2, Petitioners contend that challenged claims 9-15 are obvious over Sukegawa in view of the Bruce³ reference. However, Petitioners’ proposed reasons for combining Sukegawa and Bruce do not stand up to scrutiny and are clearly hindsight-based. For example, Petitioners propose to add table entries to Sukegawa from Bruce based on Bruce’s memory structure despite the fact that Sukegawa already includes table entries describing its own memory structure. Further, in a classic case of the tail wagging the dog, Petitioners use the addition of Bruce’s table entries into Sukegawa as the reason for engaging in an unwarranted wholesale redesign of Sukegawa’s memory structure in a manner that destroys Sukegawa’s purposeful correlation of its mapping table to its memory structure. Petitioners’ wholesale redesign of Sukegawa guts Sukegawa’s address conversion table, and the alleged “mapping table” relied on for claim 1 no longer exists in the combination asserted in Petitioners’ challenge of dependent claims 9-15. As Petitioners look to Bruce’s memory structure to reverse-engineer the “mapping table” of claims 9-15, each of which depend directly or indirectly from claim 1, their analysis is not guided by Bruce’s or Sukegawa’s teachings, but by hindsight.

³ U.S. Patent No. 5,822,251 (“Bruce”).

In Ground 3, Petitioners contend that challenged claims 1 and 32 are anticipated by the Bennett⁴ reference. However, Bennett lacks every feature of the challenged claims, including the claimed “set of access parameters” recited as part of the claimed “mapping table” in each claim. Rather than including any “set of access parameters” as required, Bennett identifies a physical memory group (*i.e.*, a metablock) by a number and nothing more.

Finally, in Ground 4, Petitioners contend that challenged dependent claims 9-15 and 34 are obvious over Bennett in view of Bruce. Once again, Petitioners’ proposed modification of a primary reference—here, Bennett—in view of Bruce is supported only by improper hindsight-based reasoning. As in Petitioners’ Ground 2, Petitioners propose an extensive redesign of Bennett’s memory structure and table data without justification. Further, just as the challenges of independent claims 1 and 32 in Ground 3 are deficient, so are the challenges against their dependent claims.

As such, and as discussed in more detail in Section III below, each ground presented in the Petition is deficient.

⁴ U.S. Patent No. 7,139,864 (“Bennett”).

II. THE BOARD NEED NOT REACH ANY CLAIM CONSTRUCTION ISSUES TO DENY THE PETITION

In the Petition, Petitioners submit the following proposed constructions for five terms appearing in the challenged claims.

Term	Petitioners’ Proposed Construction
Claims 1 and 32: “optimal”	Plain and ordinary meaning
Claims 1 and 32: “LBA” (logical block address)	“an address that is part of a logical addressing system used by a host”
Claims 1 and 32: “PBA” (physical block address)	“unique addressable physical memory location”
Claims 9-11, 13, and 15: “FDE” / “FDE Identifier”	“FDE”: “a component that controls multiple flash devices and facilitates high speed data transfers to and from a group of flash memory devices.” “FDE Identifier”: “an identifier for a component that controls multiple flash devices and facilitates high speed data transfers to and from a group of flash memory devices.”

Claims 9-11 and 14: “group identifier”	“an identifier for identifying one flash memory device from another flash memory device from a set of flash devices that are controlled by the same FDE”
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See Pet., 6-9. Without expressly agreeing to Petitioners’ constructions, and without waiving its right to submit its proposed constructions in a Patent Owner Response, Patent Owner submits that the Board need not engage in any pre-institution claim construction. For the reasons presented in Section III below, Petitioners’ grounds each include fundamental flaws and fail to establish the unpatentability of every challenged claim. The Board does not need to conduct any construction of the above-identified claim terms in order to deny this Petition on the merits.

III. PETITIONER’S CHALLENGES FAIL ON THE MERITS

A. Petitioners’ Ground 1 Challenges based on Sukegawa Fail to Address Every Feature as Recited in the Challenged Claims

Petitioners assert that Sukegawa anticipates claim 1. Pet., 24-45. However, in their challenge of both claims 1 and 32, Petitioners fail to address every claimed feature and therefore fail to establish anticipation of these claims. These challenges fail.

Claim 1 recites, in relevant part, “in response to receiving the I/O transaction request, said mapping table causes the electronic storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request [initiated by a host] is associated with said first and second LBA sets.” Petitioners’ challenge fails to address every feature of this claimed limitation. In particular, Petitioners provide no analysis and point to no instance in Sukegawa directed to the claimed feature of an I/O transaction request initiated by a host being “associated with said first and second LBA sets.” Petitioners state that the alleged “optimization” occurs in response to an I/O transaction request, but fails to discuss any characteristic in Sukegawa of the alleged I/O transaction request. Petitioners assert that:

Sukegawa further explains that this optimization occurs in response to receiving an I/O transaction request, explaining that the controller accesses memory for read and write transactions “in response to an [sic] disk access request supplied from a host CPU.” Ex.-1005 at 7:28-32; *see also id.* at 11:3-6 (explaining that “[w]hen a write access request for a specified address (logical address) occurs, the block corresponding to the specified address is accessed on the basis of the address conversion table 121”); Ex-1003, ¶ 114.

Pet., 31. This is the entirety of the Petition's discussion of the alleged I/O transaction request disclosed by Sukegawa, and no mention is made of how Sukegawa allegedly discloses "the I/O transaction request is associated with said first and second LBA sets." In light of Petitioners' failure to address this element, Sukegawa fails to anticipate claim 1.

Similarly, Petitioners fail to address every claimed feature of claim 32. Claim 32 recites, in relevant part, an "electronic storage device that includes a memory system that uses a memory table for increasing the likelihood that an operational load imposed on the storage apparatus during the processing of an I/O transaction request will be optimally distributed across storage device resources, said I/O transaction request received by said storage device from a requesting host ..., " and "wherein said mapping table increases the likelihood that [the] operational load imposed on the storage apparatus during the processing of the I/O transaction request will be optimally distributed across storage device resources."

Addressing the preamble, the Petition contends that Sukegawa discloses flash EEPROMS "accessed parallelly." Pet., 34 (quoting Sukegawa). However, Petitioners fail to address the "likelihood" feature of claim 32's preamble. *Id.* Indeed, aside from quoting the "accessed parallelly" language from Sukegawa, Petitioners' analysis of the claimed characteristics of claim 32 ("the memory table increases the likelihood that an operational load imposed on the storage apparatus

will be optimally distributed across storage device resources”), or the effect of Sukegawa’s address conversion table on such “likelihood” is neither discussed nor explained. *Id.* Further, while addressing element [32e]—“wherein said mapping table increases the likelihood ...”—Petitioners state “[a]s explained above, Sukegawa’s mapping table increases the likelihood that an operational load will be optimally distributed across on the storage apparatus by ‘enabling parallel write operations’ on different sectors in response to a request from a host.” Pet., 41-42 (citing Sec. IX.A.1.d). However, Section IX.A.1.d of the Petition, appearing on pp. 30-31, does not address any “likelihood” term either.

Absent Petitioners’ failure to address this element, Sukegawa also fails to anticipate claim 32.

B. Ground 2 Warrants Denial Both Because the Petition Fails to Support the Proposed Combination of References, and Because the Proposed Combination Fails to Disclose or Suggest Every Claimed Feature

For at least three reasons, Petitioners’ argument for combining Sukegawa and Bruce is nonsensical and fails to support Petitioners’ proposed combination of these references. First, Petitioners unnecessarily propose to incorporate Bruce’s physical access parameters—which are unique to Bruce’s memory structure—into Sukegawa’s mapping table even though Sukegawa’s address conversion table already possesses access parameters for Sukegawa’s memory structure. Second, Bruce’s physical access parameters only make sense for Bruce’s memory structure

architecture, and cannot simply be dropped into Sukegawa's address conversion table without undertaking a wholesale redesign of Sukegawa's memory structure. As an afterthought, Petitioners propose to combine Bruce's and Sukegawa's memory structure, but with no credible reason to do so. Further, such a redesign is incompatible with Sukegawa's purposeful memory structure design. Last, the purported benefit that Petitioners seek to incorporate into Sukegawa by the proposed combination is a benefit that Sukegawa already possesses. Therefore, the combination of these two references as presented in the Petition is not supportable and would not have been undertaken by a person of ordinary skill in the art absent impermissible hindsight.

Additionally, Petitioners' proposed combination of Sukegawa and Bruce, including their reliance on Bruce for the claimed "set of access parameters," fails to disclose or suggest every claimed feature of the challenged claims.

As explained in more detail below, Petitioners' ground 2 challenge fails for at least these reasons.

i. Petitioners' Proposed Reason for Combining Sukegawa and Bruce is Driven By Hindsight-based Reasoning

Petitioners' proposed combination of Sukegawa and Bruce is fundamentally flawed first because Petitioners propose to incorporate Bruce's physical access parameters, which identify Bruce's physical memory structure, into Sukegawa's mapping table even though Sukegawa's address conversion table already possesses

access parameters for Sukegawa’s own memory structure. As stated in the Petition, Petitioners assert that “a POSITA would have been motivated to incorporate Bruce’s physical access parameters into Sukegawa’s mapping table, *which already contains access parameters ...*” Pet., 20 (emphasis added). There is no reason why a POSITA would have modified Sukegawa’s address conversion table to include access parameters for a memory structure that does not exist in Sukegawa.

Indeed, Bruce’s identifiers are meaningless without Bruce’s architecture because Bruce’s identifiers specifically provide mapping for Bruce’s specific memory architecture. Petitioners tacitly acknowledge this while proposing to “incorporate Bruce’s physical access parameters into Sukegawa’s” address conversion table. Pet., 20. Specifically, Petitioners state that “incorporating Bruce’s additional access parameters into Sukegawa’s mapping table would require only the modification of adding additional physical access parameters to account for *limited additional hardware* in an expandable system, such as distinct buses, DMA engines, and flash chip groups.” Pet., 20 (emphasis added). In essence, Petitioners propose to add Bruce’s entire memory structure—“distinct buses, DMA engines, and flash chip groups”—into Sukegawa in order to justify their addition of Bruce’s identifiers to Sukegawa’s address conversion table. Absurdly, this combination results in two different memory structures in

Sukegawa, with each memory structure being addressed using different identifiers. Considered in full, these changes proposed to Sukegawa go far beyond simply adding additional identifiers to Sukegawa's address conversion table, and Petitioners propose no alleged motivation or reason why a POSITA would implement this wide-sweeping redesign of Sukegawa's memory architecture.

Moreover, Petitioners fail to address that this addition to Sukegawa's architecture is fundamentally inconsistent with Sukegawa's teaching that consecutive sector numbers are used in the same track. Sukegawa teaches that sectors to be accessed sequentially are assigned to the same track: "access speed of the semiconductor memory system can therefore be increased when the system is controlled by the existing disk access method in which the sectors to be accessed sequentially are assigned to the same track." Sukegawa, Abst. This feature is a primary object of Sukegawa's disclosed invention: "It is therefore a **primary object** of the present invention to provide a semiconductor memory system which is designed to permit parallel access to a plurality of flash EEPROMs **when consecutive sector numbers in the same track** are designated" Sukegawa, 4:52-56 (emphasis added). Petitioners' combination of Bruce and Sukegawa constitutes a wholesale redesign of Sukegawa's memory structure without regard for Sukegawa's track structure, in violation of Sukegawa's "primary object" of the invention. In particular, Petitioners propose to add Bruce's architecture to

Sukegawa in order to include Bruce's identifiers as access parameters, but there is nothing in the Petition to support that the resulting address conversion table would still satisfy Sukegawa's teaching "to permit parallel access to a plurality of flash EEPROMs when consecutive sector numbers in the same track are designated."

Last, Petitioners concede that Sukegawa already possesses the benefits proposed to be added through the incorporation of Bruce. Petitioners state that the combination of Bruce and Sukegawa "would have allowed Sukegawa's mapping table to utilize the benefits of solid-state, non-volatile memory connected to a host system while maintaining and enhancing parallel memory operations." Pet., 20. But Petitioners also contend that Sukegawa's address conversion table "improves performance by 'enabling parallel write operations' on different physical memory sectors in response to a request from a host." Pet., 13 (citing Sukegawa, 8:39-43, 10:20-21, 12:36-41, 4:51-57). Additionally, while addressing claim 32's preamble against Sukegawa, Petitioners contend that Sukegawa's address conversion table "increases the likelihood that an operational load imposed on the storage apparatus will be optimally distributed across storage device resources by enabling flash EEPROMS to be 'accessed parallelly.'" Pet., 34. Petitioners even compare the features of Sukegawa and Bruce, stating that "[l]ike Sukegawa and Bennett, Bruce explains that it provides '[a] high-performance flash-memory system performing flash operations in parallel ... even when expansion flash chips are added,'"

Pet., 18. As such, Petitioners offer no credible reason why a POSITA, faced with Sukegawa’s address conversion table that already possesses access parameters to allegedly enable parallel memory operations, would have been motivated to incorporate additional access parameters for a different memory structure—and as result, need to redesign the memory structure—in Sukegawa.

Thus, Petitioners’ proposed combination of Sukegawa and Bruce requires a wholesale and complicated redesign of Sukegawa’s memory structure without adding any purported benefits. This combination is not driven by any real motivation or added benefit to Sukegawa, but rather by Petitioners’ hindsight-driven attempt to reinvent the challenged claims. This proposed combination should be rejected as unsupported by evidence and logic.

ii. Petitioners’ Proposed Combination of Sukegawa and Bruce Fails to Disclose Every Feature of Claims 9-15

For very similar reasons, Petitioners’ proposed combination of Sukegawa and Bruce fails to disclose every feature of dependent claims 9-15, including at least a “mapping table of claim 1, wherein said set of access parameters includes a bus identifier, an FDE identifier, and a group identifier” as claimed in dependent claim 9. Per claim 1, the claimed “mapping table” also must satisfy, in relevant part, “wherein, in response to receiving the I/O transaction request, said mapping table causes the electronic storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second

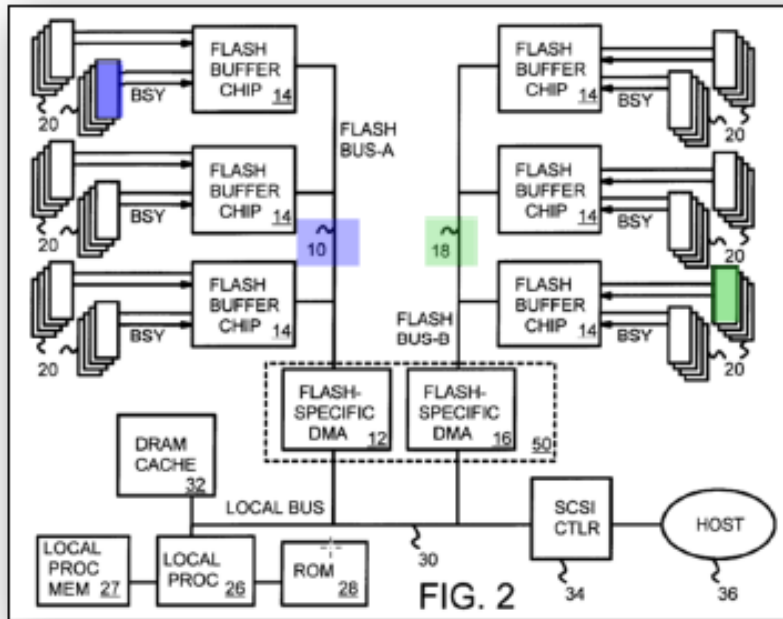
PBA, if the I/O transaction request is associated with said first and second LBA sets.”

In challenging claim 1, Petitioners rely on Sukegawa's address conversion table, and Sukegawa's "parallel write operations" that result from Sukegawa's features of the address conversion table, to allegedly disclose features of claim 1's "mapping table." Pet., 31. As discussed in Section III.B.i above, Sukegawa requires that sectors to be accessed sequentially are assigned to the same track: "access speed of the semiconductor memory system can therefore be increased when the system is controlled by the existing disk access method in which the sectors to be accessed sequentially are assigned to the same track." Sukegawa, Abst. Sukegawa teaches that this feature is a primary object of the disclosed invention. Sukegawa, 4:52-56. However, as also discussed in Section III.B.i above, Petitioners' proposed combination of Sukegawa and Bruce for the purpose of challenging claims 9-15 disregards Sukegawa's access parameters and memory structure in favor of Bruce's. As a result, Petitioners have discarded the very features of Sukegawa that were relied upon for teaching the "mapping table" of claim 1.

Indeed, the challenge of claim 9 consists of Petitioners spending pages discussing Bruce's architecture, and based on that architecture, asserting that "it would have been obvious to a POSITA to modify Sukegawa's mapping table to

include the identifiers disclosed by Bruce.” Pet., 50. But as discussed above, Bruce’s identifiers are meaningless without Bruce’s architecture, and adopting Bruce’s architecture into Sukegawa discards Sukegawa’s primary objective that consecutive sector numbers are used in the same track. In particular, once Sukegawa’s memory structure has been replaced with Bruce’s architecture in order to include a bus identifier, an FDE identifier, and a group identifier as access parameters, there is nothing in the Petition to support that the resulting mapping table would still meet all elements of claim 1.

Dependent claim 10 reinforces how Petitioners’ theory based on a combination of Sukegawa and Bruce falls short. According to claim 10, the “said first and second PBA include different bus identifiers, different FDE identifiers and different group identifiers.” However, Sukegawa’s teaching requires that the sectors to be accessed sequentially are assigned to the same track. There is no reason or theory advanced by Petitioners how a first and second PBA [having] different bus identifiers, different FDE identifiers and different group identifiers” would still be arranged in the same track as required by Sukegawa. This defect is made apparent in Petitioners’ annotated version of Bruce’s FIG. 2, indicating what Petitioners contend are a “PBA ... for a first memory chip” in purple and a “PBA for a second memory chip” in green:



Pet., 51. It is not sufficient for the purpose of this challenge for Petitioners to simply identify an architecture, such as in Bruce, with chips that are accessed via separate DMAs and busses. Petitioners must also establish that Bruce's architecture is compatible with the relied-upon features of Sukegawa in challenging claim 1, including Sukegawa's teaching that sectors to be accessed sequentially are assigned to the same track in order to enable parallel operations. Petitioners' calculated decision to assign different identifiers for Bruce's flash chips confirms the absurdity of their position, namely that identifying two random chips in Bruce's FIG. 2 would still meet all claimed elements of base claim 1:

	Access Parameters		
	Bus Identifier	FDE Identifier	Group Identifier
First unique physical location (PBA)	Bus 10/Bus-A	Bank0 SM	Specific address of first chip
Second unique physical location (PBA)	Bus 18/Bus-B	Bank3 SM	Specific address of second chip

Pet., 53.

Petitioners’ strategy of identifying a reference that allegedly discloses a portion of the challenged claims in isolation cannot prevail. Petitioners’ theory goes no further than this level of superficial detail, and therefore fails to establish obviousness of any dependent claim based on the alleged combination of Sukegawa and Bruce.

C. Ground 3 Based on Bennett Fails to Disclose Every Claimed Feature as Recited in the Challenged Claims

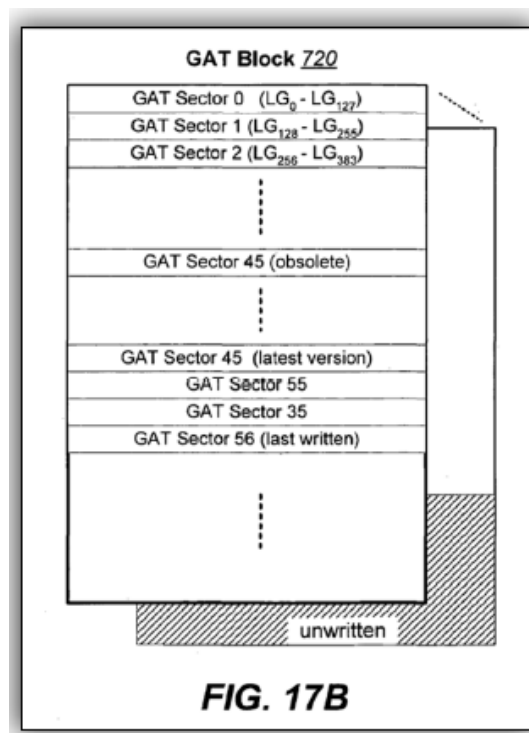
Petitioners assert that Bennett anticipates claims 1 and 32. Pet., 58-79.

Patent Owner disagrees, as Bennett fails to disclose every feature of these challenges claims, including any “set of access parameters” representing a physical block address.

Claim 1 is directed to a “mapping table” comprising, in relevant part, “a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for representing a set of PBAs, including a first PBA

disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store.”

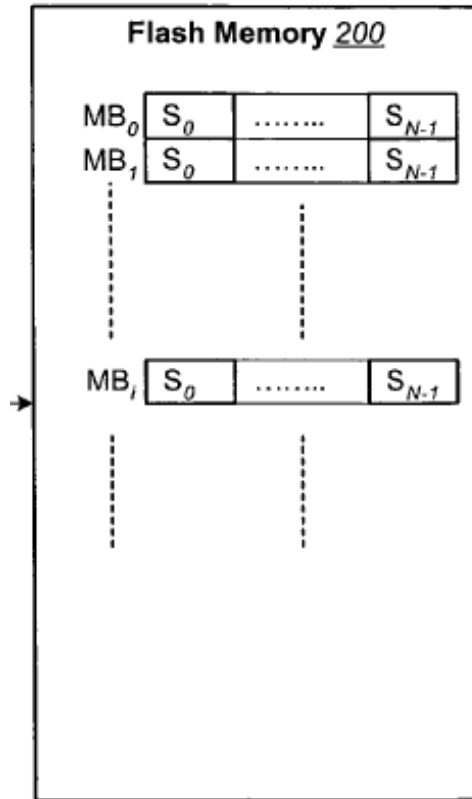
Petitioners rely on Bennett to disclose a GAT (Group Access Table) as the claimed “mapping table” of claim 1, and Petitioners look to the GAT to disclose “a list of metablock addresses for all logical groups of host data in the memory system.” Pet., 58 (quoting Bennett, 24:19-21). Petitioners also contend that the GAT “contains one entry for each logical group, ordered sequentially according to logical address.” Pet., 58 (quoting Bennett, 24:21-22). This is indicated in Bennett’s FIG. 17B, reproduced below:



Additionally, while addressing the claimed “set of PBA fields” of claim 1, Petitioners contend that Bennett’s “metablocks are therefore PBAs—or unique addressable memory locations.” Pet., 63.

However, while Petitioners rely on Bennett’s “metablocks” to disclose the claimed “PBAs—or unique addressable memory locations,” Petitioners fail to identify any claimed first and second “set of access parameters” stored in Bennett’s GAT, as required by claim 1. In particular, claim 1 requires that the claimed “mapping table” comprise a “set of PBA fields respectively disposed for representing a set of PBAs, *including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters*, said PBAs each associated with a physical memory location in a memory store.” (emphasis added).

Bennett introduces Flash Memory 200 as including “metablocks, where each metablock is a group of physical sectors $S_0, \dots, S_{N-1}$ that are erasable together.” Bennett, 6:50-52. Per Bennett, each metablock is identified by metablock number, as shown in Bennett’s FIG. 2 below.



Attempting to establish the claimed “set of access parameters” to identify first and second metablocks in Bennett, Petitioners point to the data fields of a GAT sector, which include a GAT entry for each metablock. Pet., 64-65 (arguing that “the specific metablock number and relinked flag[] exemplify access parameters for representing the physical memory location of the PBA.” This is incorrect. Each GAT entry, which Bennett refers to as an “address,” includes “the metablock number, the page tag ... , and a flag indicating whether the metablock has been relinked.” Bennett, 24:33-36, 24:39-42. But of this information, a page tag and relinked flag do not represent a PBA, or physical block address. Only a metablock number in Bennett is used to identify a metablock. See Bennett, 24:23-

24 (“The nth entry in the GAT contains the metablock address for the logical group with address n.”). A single metablock number does not disclose a “set of access parameters” as claimed. For at least this reason, Bennett’s GAT fails to disclose or suggest every feature of claim 1, and Bennett therefore fails to anticipate claim 1.

Similar to claim 1, claim 32 recites, in relevant part, “wherein said first PBA includes a first set of access parameters and said second PBA includes a second set of access parameters, and at least one difference between said first and second PBAs.” Petitioners assert that a difference in a “set of access parameters” is satisfied by “a different metablock number (e.g., MB₀ and MB₂).” Pet., 76. However, for the same reasons identified for claim 1, Bennett’s metablock number does not disclose a “set of access parameters” as claimed in claim 32. Bennett’s GAT fails to disclose or suggest every feature of claim 32, and Bennett therefore fails to anticipate claim 32.

Petitioners fall short in establishing other features of claim 32 in Bennett. Claim 32 also recites, in relevant part, “a memory store that includes a set of flash devices, said set of flash devices includes a first physical memory location and a second physical memory location that are addressable by said first and second PBAs respectively.” Petitioners contend that the claimed “first physical memory location and a second physical memory location” are satisfied by a single metablock in Bennett. Pet., 73. This is incorrect. Petitioners also assert that

Bennett’s metablock includes “a group of memory locations,” and contend that “the first physical memory location would be addressable by a first PBA and a second memory location would be addressable by a second PBA.” Pet., 73 (citing Bennett, 8:15-16). This is also wrong. First, Bennett clarifies that the “group of memory locations” described at 8:15-16 refers to “sectors that are erasable together,” and this group of sectors is Bennett’s metablock. Bennett, 8:18-19 (“a metablock being the minimum unit of erasure”). Second, as already discussed above with respect to claims 1 and 32, Bennett clearly discloses only a single address—a metablock number—for a metablock, and does not disclose a “PBA” for each sector of a metablock. As such, a single metablock in Bennett cannot be relied upon by Petitioners to fully disclose two physical locations, namely the claimed “first physical memory location and a second physical memory location that are addressable by said first and second PBAs respectively.”

Petitioners also fail to address the “likelihood” feature of claim 32’s preamble and element [32e]. Petitioners state that “Bennett further teaches that the memory table increases the likelihood that an operational load imposed on the storage apparatus will be optimally distributed across storage device resources by enabling parallel memory operations.” Pet., 69. But this statement includes no analysis, and the effect of Bennett’s GAT on any such “likelihood” is neither discussed nor explained. *Id.* Instead, Petitioners rely on the district court’s

examples of optimized memory operations without explaining the role of Bennett’s GAT on such memory operations. At most, Petitioners contend that Bennet’s GAT “optimizes memory operations in response to processing of an I/O transaction with a host” by performing such actions as accessing the memory and reading or writing in logical clusters. Pet., 70. But these actions have no relationship to whether a memory operation is optimized, and do not support Petitioners’ assertion.

And while addressing element [32e]—“wherein said mapping table increases the likelihood ...”—Petitioners identify Bennett’s teaching to exploit “parallelism ... as much as possible” without addressing how Bennett’s GAT allegedly increases the likelihood of parallelism. Pet., 78. And once again, Petitioners contend that Bennet’s GAT “optimizes memory operations in response to processing of an I/O transaction with a host” by performing such actions as accessing the memory and reading or writing in logical clusters. Pet., 70. As already noted, these actions have no relationship to whether a memory operation is optimized, and do not support Petitioners’ assertion.

For at least these reasons, Petitioners’ challenges against claims 1 and 32 based on Bennett fail.

D. Ground 4 Based on Bennett in view of Bruce Suffers From the Same Defects As Ground 3, and the Combination is Unsupported

i. Petitioners' Proposed Reason for Combining Bennett and Bruce is Driven By Hindsight-based Reasoning

Similar to the reasons presented above in Section III.C.i, Petitioners' argument for combining Bennett and Bruce is once again nonsensical and driven by hindsight-based logic. Petitioners again propose to incorporate Bruce's physical access parameters into Bennett's GAT even though Bennett's GAT already possesses a metablock number to identify each metablock in Bennett's memory structure. Pet., 23. Specifically, just as with Petitioners' unsupported combination of Sukegawa and Bruce, Petitioners assert that "a POSITA would have been motivated to incorporate Bruce's physical access parameters into Bennett's mapping table because doing so would have allowed Bennett's mapping table to cover an expandable solid state storage system with parallel memory access." Pet., 23. But Bennett already possesses a GAT having a scheme for identifying its own metablock numbers, and there is no reason to add Bruce's parameters into Bennett, where those parameters would be meaningless.

Second, Bruce's physical access parameters only make sense for Bruce's memory structure architecture, and cannot simply be dropped into Bennett's GAT without undertaking a wholesale redesign of Bennett's memory structure. While Petitioners contend that adding Bruce's access parameters to Bennett's GAT would

be “very minor changes” (see Pet., 23-24), the wholesale redesign of Bennett’s memory structure is not very minor. This proposed change is also unsupported by any credible reason beyond impermissible hindsight. Petitioners claim that the proposed changes to Bennett are made to provide “parallel memory access.” Pet., 23. But according to Petitioners, Bennett’s GAT “optimizes memory operations by enabling parallel memory operations.” Pet., 59. Therefore, they propose combining Bennett and Bruce in a manner that requires an extensive redesign of Bennett’s memory structure without any corresponding benefit. This combination of references cannot be maintained.

In summary, Petitioners have offered no credible reason why a POSITA would have been motivated to incorporate Bruce’s access parameters to Bennett’s GAT, thus requiring a wholesale redesign of Bennett’s memory structure to achieve a purported benefit that Bennett already possesses. Only hindsight-based reasoning supports such a combination. This is improper, and fails to establish obviousness of any challenged claim in Ground 4.

ii. Petitioners’ Proposed Combination of Bennett and Bruce Also Fails to Disclose Every Feature of Claims 9-15 and 34

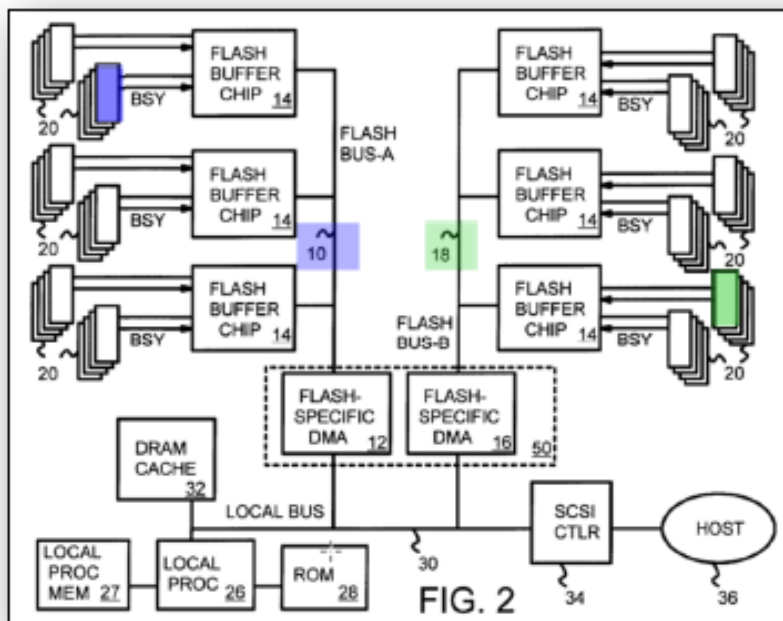
Petitioners’ proposed combination of Bennett and Bruce also fails to disclose every feature of claim 9, namely a “mapping table of claim 1, wherein said set of access parameters includes a bus identifier, an FDE identifier, and a group identifier” as claimed in dependent claim 9. Petitioners refer back to their

Ground 2 challenge and discussion of Bruce's architecture (Pet., 79), and based on that architecture assert that it "would have been obvious to include Bruce's access parameters in Bennett's table." Pet., 79. Indeed, the entirety of Petitioners' analysis of claims 9-15 in Ground 4 is limited to the conclusory statement that it would have been obvious to "include Bruce's access parameters in Bennett's table." Pet., 79-82. But as explained above in Section III.D, Petitioners failed to show that Bennett anticipates claim 1. Specifically, Petitioners failed to establish that Bennett discloses a "mapping table" having every feature of claim 1. See Sec. III.D, *supra*. Further, in Ground 4, Petitioners do not rely upon Bruce to remedy this shortcoming of Bennett. Therefore, claim 1 necessarily survives Petitioners' challenge, as do dependent claims 9-15.

Petitioners' theory against dependent claim 34 based on Bennett in view of Bruce also fails. According to claim 34, "the processing of the I/O transaction request [of claim 32] includes a first memory operation performed using said first PBA and a second memory operation performed using said second PBA." Further, "said first and second PBAs respectively associated with a first set of access parameters and a second set of access parameters, and said set of first and second set of access parameters differing by at least one access parameter." Petitioners reuse the manufactured chart from page 53 of the Petition to contend that "a first and second PBA can be identified using the following access parameters:

	Access Parameters		
	Bus Identifier	FDE Identifier	Group Identifier
First unique physical location (PBA)	Bus 10/Bus-A	Bank0 SM	Specific address of first chip
Second unique physical location (PBA)	Bus 18/Bus-B	Bank3 SM	Specific address of second chip

Pet., 83-84. The PBAs identified in this chart correspond to the memory chips shown in Petitioners’ annotation of Bruce’s FIG. 2:



Pet., 51. But Petitioners have no basis to contend that the purple memory chip on BUS-A and the green memory chip on BUS-B would ever be the subject of memory operations occurring as a result of “the processing of an I/O transaction request” as required by challenged claim 34. Petitioners simply point to Bruce’s

architecture without ever establishing how or why the processing of an I/O transaction request would result in a memory operation on both the purple memory chip on BUS-A and the green memory chip on BUS-B, particularly as Petitioners have effectively discarded Bennett's memory structure for the purpose of its challenge of claim 34. Bennett and Bruce, whether considered alone or in Petitioners' asserted combination, fail to disclose every feature of claim 34 as arranged in the claim. Petitioners have pieced those references together in an attempt to recreate the challenged claim, but without showing that all claimed features are present in the combination. This challenge of claim 34 also fails.

IV. CONCLUSION

For the reasons presented above, no *inter partes* review should be instituted.

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The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word-processing system's word count, the brief contains 6,449 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(a).

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CERTIFICATE OF SERVICE

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