

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KIOXIA AMERICA, INC. and KIOXIA CORPORATION,
Petitioners,

v.

BiTMICRO LLC,
Patent Owner.

IPR2023-00742
Patent 8,010,740 B2

Before KEN B. BARRETT, TERRENCE W. McMILLIN, and
KEVIN C. TROCK, *Administrative Patent Judges*.

McMILLIN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background and Summary

KIOXIA Corporation and KIOXIA America, Inc. (“Petitioners”)¹ filed a Petition to institute an *inter partes* review of claims 1, 9–15, 32, and 34 (the “challenged claims”) of U.S. Patent 8,010,740 B2 (Ex. 1001, the “’740 patent”) pursuant to 35 U.S.C. § 311 *et seq.* Paper 3 (“Petition” or “Pet.”). BiTMICRO, LLC (“Patent Owner”)² filed a Preliminary Response. Paper 7 (“Preliminary Response” or “Prelim. Resp.”).

We have authority under 35 U.S.C. § 314, which provides that an *inter partes* review may not be instituted unless the information presented in the Petition and the Preliminary Response shows that “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). For the reasons discussed below, we determine that this standard has been met and institute *inter partes* review on the grounds presented in the Petition.

B. Related Proceedings

The parties identify the following related proceedings: *BiTMICRO LLC v. KIOXIA Am. Inc., et al.*, 6:22-cv-00331 (W.D. Tex. 2022); and *BiTMICRO LLC v. Intel Corp.*, 5:23-cv-00625 (N.D. Cal.). Pet. 91; Paper 5, 2.

Patent Owner further identifies the following *inter partes* review petition challenging the ’740 patent: *Intel Corporation v. BiTMICRO, LLC*, IPR2023-00782. Paper 5, 2.

¹ Petitioners identify KIOXIA Corporation and KIOXIA America, Inc. as the real parties-in-interest. Pet. 91.

² Patent Owner identifies BitMicro, LLC as the real party-in-interest. Paper 5, 2.

C. The '740 patent

The '740 patent is titled “Optimizing Memory Operations in an Electronic Storage Device.” Ex. 1001, code (54). The '740 patent explains that the “increased . . . adoption of . . . solid state storage devices due to certain advantages of these types of storage devices over other forms of storage devices, such as rotational drives” can be difficult “because many conventional computer devices, sometimes referred to as ‘hosts,’ use host operating systems, file systems, or both that are optimized for use with rotational drives rather than solid state storage devices.” *Id.* at 1:32–41. A “need exists for a solution that optimizes memory operations performed by or in an electronic storage device with a relatively minimal increase in device complexity and costs” and “include[s] increasing the likelihood that, in response to an I/O transaction initiated by a host, the operational load imposed on the storage device by these memory operations will be optimally distributed across different storage device resources, such as by interleaving or parallel memory operations, reducing memory operation latency, increasing operational device efficiency, or both.” *Id.* at 2:11–21.

The '740 patent “relates to solutions for increasing the likelihood that the operational load imposed on the memory system by these memory operations, performed in response to an I/O transaction request, will be optimally distributed across resources used by the memory system, increasing operational efficiency, reducing memory operation latency or both.” *Id.* at 1:16–24. The '740 patent provides this solution using a “mapping table.” *See id.* at 2:25–49.

Figure 2, reproduced below, illustrates “a mapping table for an electronic storage device” in accordance to the '740 patent. *Id.* at 2:58–61.

9

Logical Fields 26	PBA Fields 28			
	Access Parameter Fields 30			Memory Index Fields 32
	Bus Id Fields 34	FDE Id Fields 36	Group Id Fields 38	
40 LBAs 00-07	8-0	22-01	15-0	46 0x00
42 LBAs 08-15	8-0	22-02	15-1	48 0x08
44 LBAs 16-23	8-1	22-11	15-0	50 0x00
45 LBAs 24-31	8-1	22-12	15-1	51 0x08
⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮

FIG. 2

Figure 2 depicts “Mapping table 9,” which “includes a set of fields, named logical fields 26, and a set of PBA fields 28.” *Id.* at 5:27–30.

Figure 1, reproduced below, illustrates “an electronic storage device that includes a memory system which uses a memory table” such as the mapping table illustrated in Figure 2. *Id.* at 2:53–57.

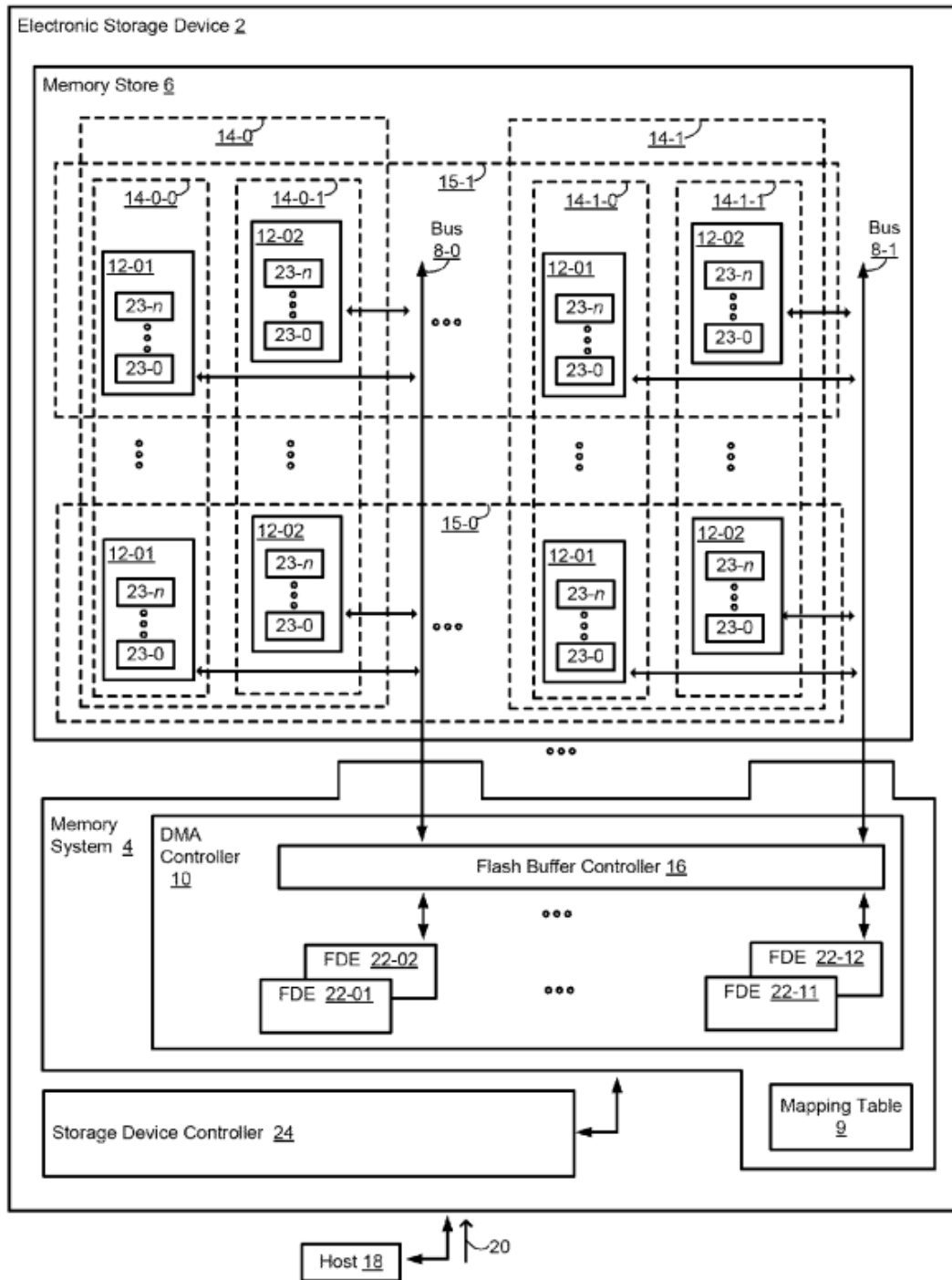


FIG. 1

Figure 1 depicts an electronic storage device with a “memory system 4” that “is coupled to a memory store 6 via a set of buses, such as buses 8-0 and 8-1,

and uses a mapping table 9” and that “also includes a DMA controller 10 that includes a flash buffer controller 16 and a set of direct memory access engines.” *Id.* at 3:25–30. These “direct memory access engines may be . . . referred to as FDEs,” which “represent[] a device that is capable of controlling a flash memory device and performing DMA operations on the flash memory device in response to commands generated by storage device 2 through storage device controller 24.” *Id.* at 3:32–39. “These DMA operations include facilitating high speed data transfers to and from memory devices that are included as part of memory store 6, such as flash memory devices 12-01 and 12-02,” and “[b]uses 8-0 and 8-1 respectively function as a bus interface that is used by an FDE to control and communicate with selected flash memory devices in memory store 6.” *Id.* at 3:39–45.

The ’740 patent discloses that “storage device 2 initializes mapping table 9 by creating an association between . . . LBA [(logical block address)] sets and PBAs [(physical block addresses)] so that adjacent LBA sets are mapped to PBAs, and any two adjacent PBAs differ by at least one access parameter.” *Id.* at 7:3–6. “This mapping association among LBA sets and PBAs increases the likelihood that memory operations resulting from an I/O transaction request will be optimized because if these memory operations involve data accesses associated with contiguous LBA sets these data accesses will in likelihood occur on different PBAs,” which “results in the likelihood that different storage resources will be used, such as different buses, different FDEs, different groups or any combination of these, which provides a form of interleaving by bus, FDE, flash memory device group or any combination of these.” *Id.* at 7:9–19.

D. Challenged Claims

Petitioners challenge claims 1, 9–15, 32, and 34 of the '740 patent. Pet. 1, 2–3. Of the challenged claims, claims 1 and 32 are independent claims. Ex. 1001, 9:64–10:24, 13:29–14:5. Claim 1 recites:

1. A mapping table for optimizing memory operations performed by an electronic storage device in response to receiving an I/O transaction request initiated by a host, said mapping table comprising:
 - a set of logical fields, including a first logical field and a second logical field, and said logical fields respectively disposed for representing a plurality of LBA sets, including said first logical field disposed for representing a first LBA set and said second logical field disposed for representing a second LBA set, said first and second LBA sets each representing a set of consecutive LBAS;
 - a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for representing a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAS each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs; and
- wherein, in response to receiving the I/O transaction request, said mapping table causes the electronic storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second LBA sets.

Id. at 9:64–10:24.

E. The Asserted Grounds

Petitioners challenge claims 1, 9–15, 32, and 34 of the '740 patent based on the grounds set forth in the table below.

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 32, 34	102(b) ³	Sukegawa ⁴
9–15	103(a)	Sukegawa, Bruce ⁵
1, 32	102(a)	Bennett ⁶
9–15, 34	103(a)	Bennett, Bruce

Pet. 2–3. Petitioners support their showing of unpatentability of the challenged claims of the '740 patent with Exhibits 1001–1016 including the Declaration of R. Jacob Baker, Ph.D., P.E. (Ex. 1003). Patent Owner did not file any exhibits in support of the Preliminary Response. As such, there is no testimony in the record to contradict that provided in the Declaration of Dr. Baker.

II. ANALYSIS

A. Legal Standards

In order for a prior art reference to serve as an anticipatory reference, it must disclose every limitation of the claimed invention, either explicitly or inherently. *In re Schreiber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997).

Anticipation “requires that every element and limitation of the claim was previously described in a single prior art reference, either expressly or inherently, so as to place a person of ordinary skill in possession of the invention.” *Sanofi-Synthelabo v. Apotex, Inc.*, 550 F.3d 1075, 1082 (Fed. Cir. 2008) (citing *Schering Corp. v. Geneva Pharms., Inc.*, 339 F.3d 1373,

³ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 285–88 (2011), revised 35 U.S.C. §§ 102 and 103 effective March 16, 2013. Because the challenged patent claims priority to applications filed before March 16, 2013, we refer to the pre-AIA version of §§ 102 and 103. Our opinions on the present record would not change if the AIA version of §§ 102 and 103 were to apply.

⁴ US 5,572,466, issued Nov. 5, 1996 (Ex. 1005).

⁵ US 5,822,251, issued Oct. 13, 1998 (Ex. 1006).

⁶ US 7,139,864 B2, issued Nov. 21, 2006 (Ex. 1007).

1379 (Fed. Cir. 2003); *Continental Can Co. USA v. Monsanto Co.*, 948 F.2d 1264, 1267–69 (Fed. Cir. 1991)). Anticipation also requires that a reference discloses “all of the limitations arranged or combined in the same way as recited in the claim.” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008).

A patent claim is unpatentable as obvious if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of non-obviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). Petitioners cannot satisfy their burden of proving obviousness by employing “mere conclusory statements.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

B. Level of Ordinary Skill in the Art

With regard to the level of ordinary skill in the art, Petitioners contend a person of ordinary skill in the art “would have had at least a Bachelor’s

degree in electrical or computer engineering, or a similar field, and at least two years of work experiences in the computer memory or data storage industry.” Pet. 5–6 (citing Ex. 1003 ¶¶ 57–59). Petitioners further contend “less formal education” could be “substituted . . . with additional relevant work experience, and vice versa.” *Id.* at 6. Patent Owner does not address the level of ordinary skill in the art. *See generally* Prelim. Resp.

For purposes of this Decision, we adopt Petitioners’ definition of the level of ordinary skill in the art because it is consistent with the ’740 patent and the asserted prior art.

C. Claim Construction

In an *inter partes* review for a petition filed on or after November 13, 2018, “[claims] of a patent . . . shall be construed using the same claim construction standard that would be used to construe the [claims] in a civil action under 35 U.S.C. § 282(b), including construing the [claims] in accordance with the ordinary and customary meaning of such claims as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b) (2018); *see also Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–14 (Fed. Cir. 2005). We shall construe only terms that are in controversy and then only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999). “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). There is a “heavy presumption,” however, that a

claim term carries its ordinary and customary meaning. *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002) (citation omitted).

Petitioners submit constructions for five claim terms which they apply for purposes of the Petition. Pet. 6–9. However, for the claim term “optimal,”⁷ the Petition provides that, “[i]n the co-pending litigation, the Court held that ‘optimal’ had a plain and ordinary meaning.” *Id.* at 7 (citing Ex. 1008, 42–45). Petitioners apply this construction but do not state the “plain and ordinary meaning” of “optimal.” *Id.*

The other four terms discussed in the Petition and the proposed constructions are:

LBA	an address that is part of a logical addressing system used by a host
PBA	unique addressable physical memory location
FDE ⁸	a component that controls multiple flash devices and facilitates high speed data transfers to and from a group of flash memory devices
group identifier	an identifier for identifying one flash memory device from another flash memory device from a set of flash devices that are controlled by the same FDE

⁷ The Petition states “Claims 1 and 32 recite the term ‘optimal.’” Pet. 7. However, the term “optimal” does not appear in either claim 1 or 32 although both of these claims use a form of this term. Claim 1 uses “optimizing” and “optimized” and claim 32 uses “optimally” twice.

⁸ For the related term “FDE Identifier,” Petitioners propose “an identifier for a component that controls multiple flash devices and facilitates high speed data transfers to and from a group of flash memory devices.” Pet. 8.

Id. at 7–9. Petitioners support these constructions with citations to the Specification of the '740 patent. *See id.*

Patent Owner proposes that we not engage in any claim construction at this stage of this proceeding. Prelim. Resp. 11. Patent Owner contends that “Petitioners’ grounds each include fundamental flaws and fail to establish the unpatentability of every challenged claim” and states, “The Board does not need to conduct any construction of the above-identified claim terms in order to deny this Petition on the merits.” *Id.* Patent Owner does not say what we should do as far as claim construction if we institute *inter partes* review. *See id.* Patent Owner does not argue that Petitioners proposed constructions are incorrect or flawed in any respect.

Based on this record, we adopt the uncontested constructions proposed by Petitioners. If Patent Owner contests any of these constructions or believes any claim construction is necessary for purposes of the final written decision, the Patent Owner should so indicate in its response filed pursuant to 37 C.F.R. § 42.120.

D. *Summaries of Cited Art*⁹

1. *Sukegawa (Ex. 1005)*

Sukegawa is titled “Flash Memory Chips.” Ex. 1005, code (54). Sukegawa discloses a “plurality of consecutive sector numbers are assigned to a plurality of flash EEPROM chips in a semiconductor memory system,” and the “results of assigning the consecutive sector numbers are held in an address conversion table as address conversion information.” *Id.* at code

⁹ Petitioners contend that the cited art qualifies as prior art under applicable law. *See* Pet. 1–2. Patent Owner does not dispute the prior art status of the cited art. *See generally* Prelim. Resp. Pursuant to our independent analysis as set forth in the body, we determine that the cited art is prior art.

(57). Sukegawa discloses an “address conversion table” or mapping table, which is used by an access controller to define “the correspondence between the logical addresses (the track numbers and the sector numbers) from the host CPU and the real addresses for accessing the flash EEPROM chips.” *Id.* at 7:47–52. The “logical addresses” are specified as “track numbers and sector numbers,” and the “real memory addresses” are specified as “chip numbers, block 10 numbers, and page numbers.” *Id.* at 9:14–19.

Sukegawa was filed on October 6, 1993, and issued on November 5, 1996. *Id.* at codes (22), (45). The earliest priority date claimed for the ’740 patent is June 8, 2006. Ex. 1001, code (63), 1:7–12. Sukegawa is prior art to the ’740 patent.

2. *Bruce (Ex. 1006)*

Bruce is titled “Expandable Flash-Memory Mass-Storage Using Shared Buddy Lines and Intermediate Flash-Bus Between Device-Specific Buffers and Flash-Intelligent DMA Controllers.” Ex. 1006, code (54). Bruce discloses an “expandable” flash-memory system” that uses “flash buffer chips” instead of “directly connecting individual flash-memory chips to a controller.” *Id.* at code (57). “Each flash buffer chip can connect to four banks of flash-memory chips,” enabling “individual chips in a bank [to be] generated from an address sent to the flash buffer chips.” *Id.* The use of “[t]wo flash-specific DMA controllers . . . each with four DMA state machines for controlling the four banks of flash-memory chips attached to a flash buffer chip . . . allows for four-way interleaving,” and “[t]wo flash buses connect the two DMA controllers to flash buffer chips.” *Id.* As a result, “[t]he data can be interleaved among the four banks for each flash buffer chip, and also interleaved among chips connected to the two flash

busses.” *Id.* at 6:57–60. Because, “[e]ach bank can be separately accessed, . . . many flash operations [can] be performed in parallel.” *Id.* at 5:21–23.

Bruce was filed on September 29, 1997, and issued on October 13, 1998. *Id.* at codes (22), (45). The earliest priority date claimed for the ’740 patent is June 8, 2006. Ex. 1001, code (63), 1:7–12. Bruce is prior art to the ’740 patent.

3. *Bennett (Ex. 1007)*

Bennett is titled “Non-Volatile Memory and Method with Block Management System.” Ex. 1007, code (54). Bennett discloses a “non-volatile memory system [that] is organized in physical groups of physical memory locations,” and that “allows for update of a logical group of data by allocating a metablock [physical group] dedicated to recording the update data of the logical group.” *Id.* at code (57). Bennett’s disclosure “allows multiple logical groups to be updated concurrently,” which “increase efficiency and reduces overheads.” *Id.* at 4:50–52. Specifically, “[i]n order to maximize programming speed and erase speed, parallelism is exploited as much as possible by arranging for multiple pages of information, located in multiple MEUs [(minimum erase units)], to be programmed in parallel, and for multiple MEUs to be erased in parallel.” *Id.* at 8:27–31.

Bennett was filed on December 30, 2003. *Id.* at code (22). The earliest priority date claimed for the ’740 patent is June 8, 2006. Ex. 1001, code (63), 1:7–12. Bennett is prior art to the ’740 patent.

E. Claims 1, 32, and 34: Consideration of Alleged Anticipation Over Sukegawa

We begin our analysis with a consideration of Petitioners’ allegation that Sukegawa anticipates claims 1, 32, and 34. *See* Pet. 24–45.

1. Element-by-Element Analysis of Claim 1

Our element-by-element analysis of Petitioners' challenge to claim 1 based on Sukegawa is set forth below.

A mapping table for optimizing memory operations performed by an electronic storage device in response to receiving an I/O transaction request initiated by a host, said mapping table comprising:

Petitioners do not take a position as to whether the preamble of claim 1 is limiting. The presentation in the Petition with regard to the preamble begins with, “[t]o the extent the preamble is limiting, Sukegawa discloses . . .” Pet. 25. The Petition goes on to present a showing that all the elements of the preamble are taught by Sukegawa. *Id.* at 25–26. Patent Owner also fails to take a position as to whether the preamble of claim 1 is limiting. *See generally* Prelim. Resp. As the showing in the Petition that Sukegawa discloses the preamble is undisputed (*see id.*), we determine that it is unnecessary for us to determine, at least at this stage, whether the preamble of claim 1 is limiting. We shall proceed to consider the showing in the Petition as to the preamble of claim 1.

Petitioners rely on Sukegawa's disclosure of an “address conversion table” as disclosing a “mapping table” as recited in the preamble. Pet. 25–26. The Petition states, “Sukegawa discloses an ‘address conversion table’ that converts logical addresses specified by a host into ‘real memory addresses’ in flash EEPROM chips. . . . Sukegawa's address conversion table is thus a ‘mapping table.’” *Id.* at 25 (citing Ex. 1003 ¶¶ 96–97; Ex. 1005, 7:48–52, 10:14–19, Fig. 11). Figure 11 of Sukegawa is reproduced below.

ADDRESS
CONVERSION
TABLE

121

LOGICAL ADDRESS		REAL MEMORY ADDRESS			
TRACK No.	SECTOR No.	CHIP No.	BLOCK No.	PAGE No.	
0	0	#10	0	(0, 1)	
	7	↓		(14, 15)	
	8	#11		(0, 1)	
	15	↓		(14, 15)	
	32	#14		(0, 1)	
	39	↓		(14, 15)	
1	0	#10	1	(0, 1)	
	7	↓		(14, 15)	
	8	#11		(0, 1)	
	15	↓		(14, 15)	
	32	#14		(0, 1)	
	39	↓		(14, 15)	
2	0	#10	3	(0, 1)	
	7	↓		(14, 15)	
	8	#11		(0, 1)	

FIG. 11

Figure 11 depicts “address conversion table 121.” The detailed description of Sukegawa states, “In the address conversion table 121, the correspondence between the logical addresses (the track numbers and the sector numbers) from the host CPU and the real addresses for accessing the flash EEPROM chips 11-0 through 11-4 is defined.” Ex. 1005, 7:48–52.

With regard to the remaining elements of the preamble (*optimizing memory operations performed by an electronic storage device in response to receiving an I/O transaction request initiated by a host*), the Petition provides:

Sukegawa’s mapping table also enables optimized memory operations by allowing flash EEPROMS to be “accessed parallelly.” Ex-1005 at 12:35-40, 4:51-57, 5:8-13, 10:10-13, 10:20-21; Ex-1003, ¶ 98. The district court’s claim construction order also identifies “contiguous LBA sets, adjacent LBA sets, [and] adjacent PBA’s differing by at least

one parameter” as examples of optimization. Ex-1008 at 30; Ex-1003, ¶ 99. Sukegawa teaches each of these examples. *Infra* §§ IX.A.1.b, IX.A.1.c; Ex-1003, ¶ 99.

Sukegawa also states that these optimized memory operations are performed in response to receiving an I/O transaction request initiated by a host, explaining that the controller accesses memory for read and write transactions “in response to [a] disk access request supplied from a host CPU.” Ex-1005 at 7:28-32, 11:3-6; Ex-1003, ¶ 100.

Pet. 25–26 (alterations in original, footnote omitted).

As noted above, Patent Owner does not dispute Petitioners’ showing as to the preamble of claim 1. *See generally* Prelim. Resp.

We determine that, on the current record, Petitioners have met their burden to show the preamble of claim 1 of the ’740 patent is disclosed in Sukegawa.

a set of logical fields, including a first logical field and a second logical field, and said logical fields respectively disposed for representing a plurality of LBA sets, including said first logical field disposed for representing a first LBA set and said second logical field disposed for representing a second LBA set, said first and second LBA sets each representing a set of consecutive LBAs;

In support of Petitioners’ contention that Sukegawa discloses this limitation, the Petition provides an annotated version of Figure 11 of Sukegawa, an excerpted portion of which is reproduced below. Pet. 27.¹⁰

¹⁰ Any coloration shown in the depicted figures or quoted passages is reproduced from the Petition.

ADDRESS
CONVERSION
TABLE 121

LOGICAL ADDRESS		REAL MEMORY ADDRESS			
TRACK No.	SECTOR No.	CHIP No.	BLOCK No.	PAGE No.	
0 ↓ ↓ ↓	0 ↓ 7	#10 ↓	0 ↓	(0, 1) ↓ (14, 15)	
	8 ↓ 15	#11 ↓		(0, 1) ↓ (14, 15)	
	32 ↓ 39	#14 ↓		(0, 1) ↓ (14, 15)	

This excerpted portion of the annotated version of Figure 11 depicts “Sukegawa’s **first logical field** and **second logical field**, each of which are disposed to represent **a set of consecutive LBAs.**” *Id.* The Petition states:

Sukegawa discloses “sectors” that are part of “a logical address designated by a host system.” Ex-1005 at 4:67-5:4, 9:14-19, 4:30-35, 8:48-49. These logical sectors thus constitute LBAs, or addresses that are part of a logical addressing system used by a host, under Petitioners’ proposed construction. *Supra*, § VII.B; Ex-1003, ¶ 102.

Sukegawa also discloses logical fields that are disposed to represent a plurality of LBA sets, including, for example, a first LBA set comprising eight consecutive LBAs from 0-7, a second LBA set comprising eight consecutive LBAs from 8-15, etc. Ex-1005 at 8:66-9:8, 8:36-39; Ex-1003, ¶ 103.

Id. at 26. The cited passages in Sukegawa support Petitioners’ contentions regarding this limitation of claim 1.

Patent Owner does not dispute Petitioners’ showing as to this limitation of claim 1. *See generally* Prelim. Resp.

We determine that, on the current record, Petitioners have met their burden to show this limitation of claim 1 of the '740 patent is disclosed in Sukegawa.

a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for representing a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs; and

In support of Petitioners' contention that Sukegawa discloses this limitation, the Petition provides an annotated version of Figure 11 of Sukegawa, an excerpted portion of which is reproduced below. Pet. 30.

ADDRESS
CONVERSION
TABLE

121

LOGICAL ADDRESS		REAL MEMORY ADDRESS		
TRACK No.	SECTOR No.	CHIP No.	BLOCK No.	PAGE No.
0 ↓ ↓ ↓	0 ↓ 7	#10 ↓	0	(0, 1) ↓ (14, 15)
	8 ↓ 15	#11 ↓		(0, 1) ↓ (14, 15)
	~~~~~			
	32 ↓ 39	#14 ↓		(0, 1) ↓ (14, 15)

This excerpted portion of the annotated version of Figure 11 depicts:

a set of **PBA fields** that includes a first and second PBA field (e.g., chip number and block number), which represent a **first PBA** and a **second PBA**. Annotated Figure 11 also illustrates the **first logical field** associated with the **first PBA**, and the **second logical field** associated with the **second PBA**.

*Id.* at 29. The Petition states:

Sukegawa discloses “real memory addresses,” which correspond to physical memory locations illustrated by identifiers for a chip number, block number, and page number. Ex-1005 at 9:14-21, 4:30-35, Fig. 11; Ex-1003, ¶ 106. Each of these “real memory addresses” thus constitute a PBA, or a unique addressable physical memory location, pursuant to Petitioner’s proposed construction. *Supra* § VII.C; Ex-1003, ¶ 106.

Sukegawa also discloses sets of PBA fields disposed for representing a set of PBAs. For example, Sukegawa teaches fields such as “Chip No.” and “Block No.” that represent a set of PBAs (real memory addresses). Ex-1005 at 9:14-32; 7:5-45[.] Sukegawa also teaches identifiers for these fields (e.g., Chip No. 10 and Block No. 0 for the first PBA), which exemplify access parameters representing the physical location of the PBA. *Id.*; Ex-1003, ¶ 107.

In addition, Sukegawa discloses that the address conversion table is disposed to associate the first and second LBA sets with first and second PBA, explaining that the table provides “a correspondence between the logical addresses . . . specified by the host CPU and the real memory addresses.” Ex-1005 at 9:14-19, 10:14-19, 5:46-51; Ex-1003, ¶ 108.

*Id.* at 28–29 (second alteration in original). The cited passages in Sukegawa support Petitioners’ contentions regarding this limitation of claim 1.

Patent Owner does not dispute Petitioners’ showing as to this limitation of claim 1. *See generally* Prelim. Resp. Indeed, in the Preliminary Response, Patent Owner acknowledges that “Sukegawa’s address conversion table . . . possesses access parameters for Sukegawa’s memory structure.” *Id.* at 14.

We determine that, on the current record, Petitioners have met their burden to show this limitation of claim 1 of the ’740 patent is disclosed in Sukegawa.

*wherein, in response to receiving the I/O transaction request, said mapping table causes the electronic storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second LBA sets.*

In support of Petitioners' contention that Sukegawa discloses this limitation, the Petition states:

Sukegawa teaches that the mapping table causes an electronic storage device to perform optimized memory operations by "enabling parallel write operations" in response to a request from a host. Ex-1005 at 8:39-43; 10:14-21; 4:51-57. As explained above, parallel memory operations are an example of optimized memory operations. *Supra* Footnote 2; Ex-1003, ¶¶ 111-112.

The district court's claim construction order also identifies "contiguous LBA sets, adjacent LBA sets, [and] adjacent PBA's differing by at least one parameter" as examples of optimization. Ex-1008 at 30; Ex-1003, ¶ 113. As explained above, Sukegawa teaches each of these examples as well. *Supra* §§ IX.A.1.b, IX.A.1.c.

Sukegawa further explains that this optimization occurs in response to receiving an I/O transaction request, explaining that the controller accesses memory for read and write transactions "in response to an [sic] disk access request supplied from a host CPU." Ex.-1005 at 7:28-32; *see also id.* at 11:3-6 (explaining that "[w]hen a write access request for a specified address (logical address) occurs, the block corresponding to the specified address is accessed on the basis of the address conversion table 121"); Ex-1003, ¶ 114.

Pet. 31 (alterations in original). The cited passages in Sukegawa support Petitioners' contentions regarding this limitation of claim 1.

Patent Owner disputes whether Petitioners have shown Sukegawa discloses this limitation. *See* Prelim Resp. 11–13. Patent Owner contends, "In particular, Petitioners provide no analysis and point to no instance in

Sukegawa directed to the claimed feature of an I/O transaction request initiated by a host being ‘associated with said first and second LBA sets.’”  
*Id.* at 12.

Contrary to Patent Owner’s contention, Petitioners do show that Sukegawa discloses that “if an I/O request is associated with first and second LBA sets,” the “mapping table causes the electronic storage device to perform optimized memory operations on memory locations respectively associated with a first PBA and a second PBA” as recited. As noted above, the Petition states:

Sukegawa . . . states that these optimized memory operations are performed in response to receiving an I/O transaction request initiated by a host, explaining that the controller accesses memory for read and write transactions “in response to [a] disk access request supplied from a host CPU.” Ex-1005 at 7:28-32, 11:3-6; Ex-1003, ¶ 100.

* * *

Sukegawa discloses that the address conversion table is disposed to associate the first and second LBA sets with first and second PBA, explaining that the table provides “a correspondence between the logical addresses . . . specified by the host CPU and the real memory addresses.” Ex-1005 at 9:14-19, 10:14-19, 5:46-51; Ex-1003, ¶ 108.

Pet. 26, 28–29 (alterations in original). And, in the “Overview of Sukegawa,” the Petition states:

Sukegawa’s solution is a semiconductor memory system that converts read and write requests from a host, using logical addresses, to “real memory addresses”—or unique addressable physical memory locations—in a flash EEPROM memory store. [Ex. 1005,] 4:51-5:13, 9:14-19, 10:14-19. More particularly, Sukegawa discloses an “address conversion table,” or mapping table, which is used by an access controller to associate logical addresses from a host with physical addresses

in the memory store during a read or write operation. *Id.* at 7:26-40; 7:46-51; 8:17-19. . . .

Sukegawa further teaches that the address conversion table maps the LBAs to “real memory addresses,” or PBAs, which correspond to physical memory locations in the flash EEPROM. . . .

As shown . . . in . . . Figure 11 from Sukegawa, a **first set of LBAs** is associated with a **first PBA**, and a **second set of LBAs** is associated with a **second PBA**.

*Id.* at 10–12. The cited passages in Sukegawa support these contentions in the Petition.

We determine that, on the current record, Petitioners have met their burden to show this limitation of claim 1 of the ’740 patent is disclosed in Sukegawa. Based on our determination that Petitioners have established that Sukegawa discloses all the limitations of claim 1 of the ’740 patent, we also determine that there is a reasonable likelihood that Petitioners will prevail with respect to establishing that Sukegawa anticipates claim 1.¹¹

## 2. Analysis of Claim 32

The Petition includes an element-by-element analysis showing that Sukegawa discloses all the limitations of claim 32. Pet. 31–42. Patent Owner disputes Petitioners’ showing as to claim 32. Prelim. Resp. 13–14. Patent Owner argues:

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¹¹ Thus, we have determined that there is a reasonable likelihood that the Petitioner will prevail with respect to at least one of the claims challenged in the Petition pursuant to 35 U.S.C. § 314. Accordingly, we institute *inter partes* review as to all the challenged claims and all the challenges raised in the Petition. 37 C.F.R. §42.108(a) (“When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.”).

Petitioners fail to address every claimed feature of claim 32. Claim 32 recites, in relevant part, an “electronic storage device that includes a memory system that uses a memory table for increasing the **likelihood** that an operational load imposed on the storage apparatus during the processing of an I/O transaction request will be optimally distributed across storage device resources, said I/O transaction request received by said storage device from a requesting host ...,” and “wherein said mapping table increases the **likelihood** that [the] operational load imposed on the storage apparatus during the processing of the I/O transaction request will be optimally distributed across storage device resources.”

*Id.* at 13 (emphasis added; alterations in original). Patent Owner contends that Petitioners fail to address the “likelihood” feature or term of claim 34.

*Id.* at 13–14.

This contention is contradicted by the Petition. The Petition’s showing as to claim 32 states, “Sukegawa discloses that the memory table increases the **likelihood** that an operational load imposed on the storage apparatus will be optimally distributed across storage device resources by enabling flash EEPROMS to be ‘accessed parallelly’” (Pet. 34 (citing Ex. 1003 ¶ 177; Ex. 1005, 4:51–57, 5:8–13, 10:10–13, 10:20–21, 12:35–40) (emphasis added)) and “Sukegawa’s mapping table increases the **likelihood** that an operational load will be optimally distributed across on [sic] the storage apparatus by ‘enabling parallel write operations’ on different sectors in response to a request from a host” (*id.* at 41–42 (citing Ex. 1003 ¶ 196; Ex. 1005, 4:51–57, 8:39–43, 10:20–21, 12:36–41) (emphasis added)). We reject Patent Owner’s argument.

We determine that, on the current record, Petitioners have met their burden to show the limitations of claim 32 of the ’740 patent are disclosed in Sukegawa. Based on our determination that Petitioners have established that

Sukegawa discloses all the limitations of claim 32 of the '740 patent, we also determine that there is a reasonable likelihood that Petitioners will prevail with respect to establishing that Sukegawa anticipates claim 32.

### *3. Analysis of Claim 34*

Petitioners also challenges dependent claim 34 as anticipated by Sukegawa. *See* Pet. 2, 42–45. The Petition includes an element-by-element analysis showing that Sukegawa discloses all the limitations of claim 34. *Id.* Patent Owner does not dispute Petitioners' showing as to claim 34. *See generally* Prelim. Resp.

We determine that, on the current record, Petitioners have met their burden to show the limitations of claim 34 of the '740 patent are disclosed in Sukegawa. Based on our determination that Petitioners have established that Sukegawa discloses all the limitations of claim 34 of the '740 patent, we also determine that there is a reasonable likelihood that Petitioners will prevail with respect to establishing that Sukegawa anticipates claim 34.

### *F. Dependent Claims 9–15: Consideration of Alleged Obviousness Over Sukegawa and Bruce*

Petitioners provide an element-by-element showing that the combination of Sukegawa and Bruce teaches all the limitations of dependent claims 9–15. Pet. 46–58. Petitioners also contend that it would have been obvious to a skilled artisan to combine Sukegawa and Bruce. *Id.* at 19–22. Patent Owner disputes that the combination of Sukegawa and Bruce teaches all the limitations of claims 9 and 10, but does not dispute Petitioners' showing as to the additional limitations recited in claims 11–15. Prelim. Resp. 19–23. Patent Owner also disputes Petitioners' showing as to motivation to combine Sukegawa and Bruce. *Id.* at 14–19.

Claim 9 recites:

*The mapping table of claim 1, wherein said set of access parameters includes a bus identifier, an FDE identifier and a group identifier.*

Ex. 1001, 10:65–67. Claim 10 recites:

*The mapping table of claim 9, wherein said first and second PBA include different bus identifiers, different FDE identifiers and different group identifiers.*

Ex. 1001, 11:1–3. With regard to claim 9, Petitioners contend that “Sukegawa discloses all elements of claim 1” and “Bruce teaches that access parameters representing a physical memory location include the identifiers recited in claim 9.” Pet. 46. With regard to claim 10, Petitioners rely on the showing as to claim 9 and contend that “Bruce further teaches that the bus identifiers, FDE identifiers, and group identifiers taught therein may be different.” *Id.* at 50.

Patent Owner argues that “Petitioners’ proposed combination of Sukegawa and Bruce fails to disclose every feature of dependent claims 9–15, including at least a ‘mapping table of claim 1, wherein said set of access parameters includes a bus identifier, an FDE identifier, and a group identifier’ as claimed in dependent claim 9.” Prelim Resp. 19. But Patent Owner does not argue that Bruce does not teach the access parameters recited in claims 9 and 10. *See id.* at 19–22. Instead, Patent Owner’s argument is that Sukegawa and Bruce use incompatible architecture. *See id.* The Preliminary Response states:

It is not sufficient for the purpose of this challenge for Petitioners to simply identify an architecture, such as in Bruce, with chips that are accessed via separate DMAs and busses. Petitioners must also establish that Bruce’s architecture is compatible with the relied-upon features of Sukegawa in challenging claim 1, including Sukegawa’s teaching that sectors

to be accessed sequentially are assigned to the same track in order to enable parallel operations.

*Id.* at 22. However, Petitioners’ contentions with regard to claims 9 and 10 and combining the relevant teachings of Sukegawa and Bruce are supported by the testimony of Dr. Baker. *See* Pet. 19–22 (addressing combining Sukegawa and Bruce) (citing Ex. 1003 ¶¶ 116–126), 46–53 (addressing claims 9 and 10) (citing Ex. 1003 ¶¶ 128–145); *see also* Ex. 1003 ¶ 146 (“[I]t is my opinion that it would have been obvious for a person of ordinary skill in the art in to combine Sukegawa with Bruce, and to include Bruce’s bus identifiers, FDE identifiers, and group identifiers in the mapping table disclosed by Sukegawa.”). In contrast, Patent Owner relies on unsupported attorney argument. *See* Prelim. Resp. 19–22. Such unsupported attorney argument is entitled to little probative value. *See In re Geisler*, 116 F.3d 1465, 1470 (Fed. Cir. 1997); *In re De Blauwe*, 736 F.2d 699, 705 (Fed. Cir. 1984). Petitioners’ contentions are relatively well-supported by citations to Sukegawa and Bruce and the Declaration of Dr. Baker. *See* Pet. 19–22, 46–58. We, therefore, determine that, on the current record, the weight of the evidence supports Petitioners’ contentions that the combination of Sukegawa and Bruce teach all the elements of claims 9–15.

With specific regard to motivation to combine Sukegawa and Bruce, Patent Owner similarly argues that Sukegawa and Bruce have incompatible architecture “and would not have been undertaken by a person of ordinary skill in the art absent impermissible hindsight.” Prelim. Resp. 15. Patent Owner argues that “[t]here is no reason why a POSITA would have modified Sukegawa’s address conversion table to include access parameters for a memory structure that does not exist in Sukegawa” and “Bruce’s

identifiers are meaningless without Bruce’s architecture because Bruce’s identifiers specifically provide mapping for Bruce’s specific memory architecture.” *Id.* at 16. As noted above, Petitioners’ contentions with regard to combining the relevant teachings of Sukegwa and Bruce are supported by the testimony of Dr. Baker. *See* Pet. 19–22 (citing Ex. 1003 ¶¶ 116–126). And again, in contrast, Patent Owner relies on unsupported attorney argument. *See* Prelim. Resp. 15–19.

In support of Petitioners’ contention that a skilled artisan would have been motivated to combine the relevant teachings of Sukegawa and Bruce, the Petition states, “[a]s explained in the attached declaration of Dr. R. Jacob Baker, a POSITA^[12] would have been motivated to combine Bruce with Sukegawa.” Pet. 19 (citing Ex. 1003 ¶ 116). The Petition goes on to provide a detailed explanation as to why it would have been obvious to a skilled artisan to combine Sukegawa and Bruce supported by citations to Sukegawa (Ex. 1005) and Bruce (Ex. 1006) and the Declaration of Dr. Baker (Ex. 1003), including:

These references both recognize disadvantages related to spinning disk drives, as well as the benefits of solid-state non-volatile storage. Ex-1005 at 1:21-28, 52-58; Ex-1006, 1:35-42; Ex-1003, ¶ 117. They also recognize that existing solid-state nonvolatile storage suffered from drawbacks related to data management, host addressing schemes, and the erasure and programming of information. Ex-1005 at 4:26-57; Ex-1006, 1:45-52; Ex-1003, ¶ 117. The references are both directed to resolving these issues and improving the function of solid-state non-volatile memory to optimize memory performance. Ex-1005, 4:51-6:5; Ex-1006, 2:40-3:18; Ex-1003, ¶ 117. For example, both references disclose the use of interleaving and

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¹² POSITA is an acronym commonly used in patent cases for “person of ordinary skill in the art.”

parallel memory operations to optimize memory operations. *See* Ex-1005 at 4:51-57, 10:20-21, 5:8-13; Ex-1006, 2:44-46, 13:32-35, 13:45-46; Ex-1003, ¶ 118.

Because Sukegawa and Bruce are from the same field and have interrelated teachings, a POSITA would have been motivated to combine them. Ex-1003, ¶ 119. Specifically, a POSITA would have been motivated to incorporate Bruce's physical access parameters into Sukegawa's mapping table, which already contains access parameters, because doing so would have allowed Sukegawa's mapping table to utilize the benefits of solid-state, non-volatile memory connected to a host system while maintaining and enhancing parallel memory operations. *Id.*

The combination of these references also involves combining well-known prior art elements and techniques, according to known methods, to yield the predictable result of a mapping table that accounts for an expandable solid state storage device. *Id.*, ¶ 120. Indeed, Sukegawa teaches a mapping table comprising fields for access parameters, and Bruce teaches certain types of access parameters that can be used in such a table. *Id.* Moreover, Bruce's teachings rely on well-known techniques that can be readily applied to expand Sukegawa's mapping table. *Id.*

Further, the combination of the references would have been straightforward and predictable, requiring minimal modification. *Id.*, ¶ 121. For example, incorporating Bruce's additional access parameters into Sukegawa's mapping table would require only the modification of adding additional physical access parameters to account for limited additional hardware in an expandable system, such as distinct buses, DMA engines, and flash chip groups. *Id.*

Pet. 19–20. And, as Petitioners point out, Sukegawa is cited in Bruce. *Id.* at 21 (“Further underscoring the motivation for a POSITA to combine these references is the fact that Sukegawa is explicitly referenced on the face of Bruce.”); *see also* Ex. 1006, code (56).

We determine that, on the current record, Petitioners have met their burden to show the limitations of claims 9–15 of the '740 patent are disclosed in Sukegawa and Bruce and that a skilled artisan would have been motivated to combine the relevant teachings of Sukegawa and Bruce. We also determine that there is a reasonable likelihood that Petitioners will prevail with respect to establishing that the combination of Sukegawa and Bruce renders obvious claims 9–15.

*G. Claims 1 and 32: Consideration of Alleged Anticipation Over Bennett*

The Petition includes an element-by-element analysis showing that Bennett discloses all the limitations of claims 1 and 32. Pet. 58–79. Patent Owner disputes Petitioners' showings as to claims 1 and 32. Prelim. Resp. 23–29.

First, with regard to both claims 1 and 32, Patent Owner argues that Petitioners fail to show that Bennett discloses any “set of access parameters.” *See id.* at 23 (“Bennett fails to disclose every feature of these challenge[d] claims, including any ‘set of access parameters’ representing a physical block address.”). The relevant limitation containing this element in claim 1 recites:

*a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for representing a set of PBAs, including a first PBA disposed for representing a first **set of access parameters** and a second PBA disposed for representing a second **set of access parameters**, said PBAs each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs.*

Ex. 1001, 10:8–17 (emphasis added). This limitation is addressed on pages 62–66 of the Petition. The relevant limitation containing this element in

claim 32 recites:

*wherein said first PBA includes a first set of access parameters and said second set of access parameters, and at least one difference between said first and second PBAs.*

*Id.* at 13:47–50 (emphasis added). This limitation is addressed on pages 75–77 of the Petition.

In the Petition, the Group Access Table (“GAT”) of Bennett is relied on for disclosing the mapping table of claim 1 and the memory table of claim 32. *See, e.g.*, Pet. 58, 68. Bennett states, “The Group Address Table (GAT) is a list of metablock addresses for all logical groups of host data in the memory system” and is “compris[ed of] a set of sectors (referred to as GAT sectors) with entries defining metablock addresses for every logical group in the memory system.” Ex. 1007, 24:19–27. With specific regard to disclosing the disputed elements of claims 1 and 32 (“set of access parameters”), the Petition relies on the data fields for the GAT entry depicted in Figure 17A of Bennett. Pet. 64–65 (“[T]he identifiers in these fields for each PBA (e.g., the specific metablock number and relinked flag) exemplify access parameters for representing the physical memory location of the PBA.”), 76–77 (“[T]he specific identifiers in these fields (e.g., the specific metablock number and relinked flag) exemplify access parameters for representing the physical memory location of the PBA.”). Figure 17A of Bennett is reproduced below.

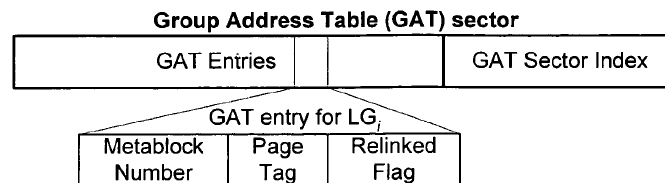


**FIG. 17A**

Figure 17A depicts GAT (Group Address Table) entry for a logical group including three data fields. Bennett describes these data fields as “a set of GAT entries for the metablock address of each logical group within a range” which “contains information for locating the metablock associated with the logical address.” Ex. 1007, 24:34–37.

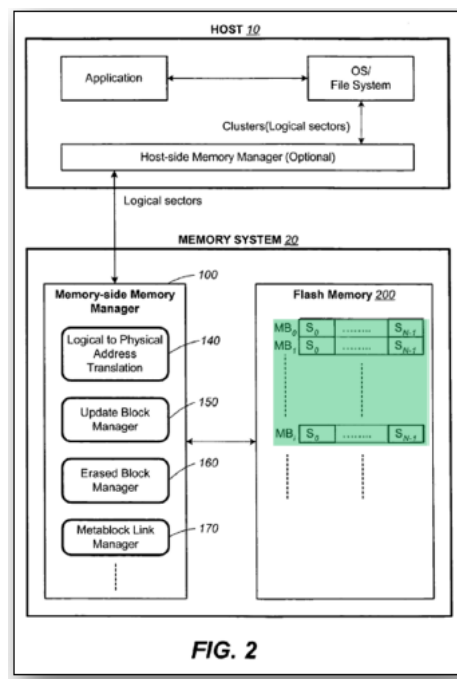
Patent Owner argues “Only a metablock number in Bennett is used to identify a metablock” and “[a] single metablock number does not disclose a ‘set of access parameters’ as claimed.” Prelim. Resp. 26–27. This argument is not explained. *See id.* Patent Owner does not explain why the “Relinked Flag” as depicted in Figure 17A and described in Bennett as “a flag indicating whether the metablock has been relinked” (Ex. 1007, 24:41–42) is not an access parameter. Moreover, even if we disregard the other data fields disclosed in Bennett, Patent Owner does not explain why the disclosed metablock number does not constitute a “set of access parameters” with a single element in each set. At least at this stage of this proceeding, after considering the arguments of the parties on this issue, we determine that Bennett does disclose a “set of access parameters” as recited in claims 1 and 32.

With further regard to claim 32, Patent Owner argues that Petitioners fail to establish that Bennett discloses “a memory store that includes a set of flash devices, said set of flash devices includes a first physical memory location and a second physical memory location that are addressable by said first and second PBAs respectively.” Prelim. Resp. 27–28. Specifically, Patent Owner argues that “Petitioners contend that the claimed ‘first physical memory location and a second physical memory location’ are satisfied by a single metablock in Bennett.” *Id.* at 27 (citing Pet. 73). Patent

Owner's argument is based on a misrepresentation of Petitioners' showing as to this limitation. *See* Pet. 72–74. Petitioners do not make the contention that Patent Owner attributes to Petitioners. *See id.* On page 73 with regard to this limitation, the Petition states:

Bennett further teaches that the first and second physical locations are addressable by first and second PBAs (i.e., physical sectors). “The physical address space of the flash memory is treated as a set of metablocks,” *id.* 8:17-19, and each metablock represents “a group of memory locations, e.g., sectors that are erasable together.” *Id.* at 8:15-16, 6:50-52. Thus, the first physical memory location would be addressable by a first PBA and a second memory location would be addressable by a second PBA. Ex-1003, ¶ 301.

*Id.* at 73. And, the Petition provides an annotated version of Figure 2 of Bennett which is reproduced below.



*Id.* at 74. The Petition states, “Annotated Figure 2 from Bennett shows Bennett’s memory store with physical memory locations represented by **metablocks (MB₀ . . . MB_i)**.” *Id.* at 73. As noted in the Petition, Bennett

clearly discloses a memory store with multiple physical memory locations addressable by multiple PBAs. We reject Patent Owner’s argument and determine that Petitioners have shown that this limitation is disclosed in Bennett.

Finally, Patent Owner argues that “Petitioners also fail to address the ‘likelihood’ feature of claim 32’s preamble and [last] element.” Prelim.

Resp. 28. This is also untrue. The preamble of claim 32 recites:

*An electronic storage device that includes a memory system that uses a memory table for increasing the **likelihood** that an operational load imposed on the storage apparatus during the processing of an I/O transaction request will be optimally distributed across storage device resources, said I/O transaction request received by said storage device from a requesting host, said electronic storage device comprising.*

Ex. 1001, 13:29–35 (emphasis added). With regard to the preamble of claim 32, the Petition states:

Bennett further teaches that the memory table increases the **likelihood** that an operational load imposed on the storage apparatus will be optimally distributed across storage device resources by enabling parallel memory operations. [Ex. 1007], 8:26-30, 2:57-59; Ex-1003, ¶ 288. As explained above, parallel memory operations are an example of optimized memory operations. *Supra* Footnote 2; Ex-1003, ¶ 288. Bennett also discloses “contiguous LBA sets, adjacent LBA sets, [and] adjacent PBA’s differing by at least one parameter,” *infra* §§ IX.C.2.b, IX.C.2.c, IX.C.2.e, which the district court has identified as examples of optimized memory operations. Ex-1008 at 30; Ex-1003, ¶ 290.

Pet. 69 (emphasis added) (second alteration in original). This passage from the Petition addresses the “likelihood” as recited in the preamble.

The last limitation of claim 32 recites:

*wherein said mapping table increases the **likelihood** that that [sic] the operational load imposed on the storage apparatus during the processing of the I/O transaction request will be optimally distributed across storage device resources.*

Ex. 1001, 14:1–5 (emphasis added). With regard to the last limitation of claim 32, the Petition states:

Bennett teaches that “[i]n order to maximize programming speed and erase speed, parallelism is exploited as much as possible by arranging for multiple pages of information . . . to be programmed in parallel, and for multiple MEUs [minimum erasable units] to be erased in parallel.” Ex-1007 at 8:26-30, 2:57-59. As explained above, parallel memory operations are an example of optimized memory operations. *Supra* Footnote 2; Ex-1003, ¶ 309. Likewise, Bennett explains that the mapping table provides a more “efficient use of system resources” by allowing “multiple logical groups to be updated concurrently,” which “increases efficiency and reduces overhead.” Ex-1007 at 4:50-52.

The district court’s claim construction order also identifies “contiguous LBA sets, adjacent LBA sets, [and] adjacent PBA’s differing by at least one parameter” as examples of optimization. Ex-1008 at 30. As explained above, Bennett teaches each of these examples as well. *Supra* §§ IX.C.2.b, IX.C.2.c, IX.C.2.e; Ex-1003, ¶ 309 & n.16.

In addition, Bennett explains that the mapping table optimizes memory operations in response to processing of an I/O transaction with a host, including, for example, that the host “accesses the memory” and reads or writes “to the memory system in unit[s] of logical clusters, each consisting of one or more logical sectors.” Ex-1007 at 6:53-59, 6:61-65; Ex-1003, ¶ 310.

Pet. 78–79 (alterations in original). Although not using the word “likelihood,” this passage from the Petition addresses “likelihood” as recited in the last limitation of claim 32 and we determine that this limitation is disclosed in Bennett. Accordingly, we reject Patent Owner’s argument.

We determine that, on the current record, Petitioners have met their burden to show the limitations of claims 1 and 32 of the '740 patent are disclosed in Bennett. Based on our determination that Petitioners have established that Bennett discloses all the limitations of claims 1 and 32 of the '740 patent, we also determine that there is a reasonable likelihood that Petitioners will prevail with respect to establishing that Bennett anticipates claims 1 and 32.

*H. Dependent Claims 9–15 and 34: Consideration of Alleged Obviousness Over Bennett and Bruce*

Petitioners provide an element-by-element showing that the combination of Bennett and Bruce teaches all the limitations of dependent claims 9–15 and 34. Pet. 79–84. Petitioners also contend that it would have been obvious to a skilled artisan to combine Bennett and Bruce. *Id.* at 22–24. Patent Owner disputes that the combination of Bennett and Bruce teaches all the limitations of claims 9 and 34, but does not dispute Petitioners' showing as to the additional limitations recited in claims 10–15. Prelim. Resp. 31–34. Patent Owner also disputes Petitioners' showing as to motivation to combine Bennett and Bruce. *Id.* at 30–31.

With regard to claim 9, Patent Owner argues that Petitioners' challenge based on the combination of Bennett and Bruce fails because "Petitioners failed to show that Bennett anticipates claim 1. Specifically, Petitioners failed to establish that Bennett discloses a 'mapping table' having every feature of claim 1." *Id.* at 32. To the extent that Patent Owner argues that Petitioners have not shown that Bennett anticipates claim 1 including by disclosing a 'mapping table,' we analyzed Patent Owner's arguments and determined to the contrary. *See* Section II.G. above. As Patent Owner provides no additional reasoning (*see* Prelim. Resp. 31–32), we determine

that Petitioners have shown that Bennett and Bruce teach all the limitations of claim 1.

With regard to claim 34, Patent Owner argues that Petitioners fail to show that the combination of Bennett and Bruce teaches “the processing of the I/O transaction request includes a first memory operation performed using said first PBA and a second memory operation performed using said second PBA.” *Id.* at 32–34. In this regard, the Petition states:

Bennett discloses all elements of claim 32 as explained above. *Supra*, § IX.C.2; Ex-1003, ¶ 313. As also explained above, Bruce teaches uniquely addressable memory locations (or PBAs) within different memory banks, which are associated with different FDEs, different buses, and different device addresses, as explained above. *Supra*, §§ IX.D.2, IX.D.3, IX.C.2.e. Ex-1003, ¶ 314. The banks of flash-memory chips “can be separately accessed, allowing many flash operations to be performed in parallel.” Ex-1006, 5:21-23, 6:55-57, 10:17-19. **This simultaneous or parallel access to different unique memory locations (PBAs) illustrates a first memory operation using a first PBA and second memory operation using a second PBA.** Ex-1003, ¶ 314.

Pet. 82–83 (emphasis added). As indicated, Petitioner supports its contention with regard to this limitation with citations to the Declaration of Dr. Baker (Ex. 1003). *See id.*; *see also* Ex. 1003 ¶ 315 (“[I]t is my opinion that Bennett in combination with Bruce renders obvious the ‘electronic storage device of claim 32, wherein the processing of the I/O transaction request includes a first memory operation performed using said first PBA and a second memory operation performed using said second PBA.’”). In contrast, Patent Owner relies on unsupported attorney argument. *See* Prelim. Resp. 32–34. On this record, we credit Dr. Baker’s uncontradicted

testimony and determine that this limitation is taught by the asserted combination of references.

With regard to motivation to combine Bennett and Bruce, Patent Owner's arguments are similar to its arguments with regard to claims 9–15 and motivation to combine Sukegawa and Bruce which were discussed above (Section II.F.). *Compare* Prelim. Resp. 15–19 *with id.* at 30–31. Patent Owner argues that the memory architecture of Bennett and Bruce are incompatible and Petitioners' incorporation of Bruce's access parameters into Bennett's mapping table are "nonsensical and driven by hindsight-based logic." *Id.* at 30–31. The Preliminary Response states, "In summary, Petitioners have offered no credible reason why a POSITA would have been motivated to incorporate Bruce's access parameters to Bennett's GAT." *Id.* at 31. This is inaccurate. The Petition states, "a POSITA would have been motivated to incorporate Bruce's physical access parameters into Bennett's mapping table because doing so would have allowed Bennett's mapping table to cover an expandable solid state storage system with parallel memory access." Pet. 23 (citing Ex. 1003 ¶ 233). The cited paragraph in Dr. Baker's Declaration provides:

Because Bennett and Bruce are in the same field, teach analogous solutions to the same issues, and have the same purpose of enabling and improving parallel memory operations, a POSITA would have been motivated to combine these references. In particular, a POSITA would have been motivated to incorporate Bruce's physical access parameters—which enable an expandable system architecture—into Bennett's mapping table to provide the benefit of a mapping table covering an expandable solid state storage system capable of improving parallel memory access. This motivation stems from the references themselves, which are both directed to improving and increasing parallel memory operations. For

example, Bruce explains the addition of flash memory chips in a memory device increases busy signals. Ex-1006 at 2:9-11. Moreover, connecting busy signals “can limit performance as parallel flash operations driving the same busy line can interfere with each other” and can also “limit[] parallelism by not providing separate indications of when each flash-memory chip has completed an operation.” *Id.* at 2:12-21; *see also* Ex-1007 at 3:31-37 (noting that the initialization and preparation of directory information takes time, “all the more so with ever increasing flash memory capacity.”). Accordingly, the benefits provided by Bruce align directly with the purpose of Bennett. Thus, a POSITA would have been motivated to combine Bruce’s additional access parameters with Bennett’s mapping table, which already contains access parameters as explained above, as this would have allowed Bennett’s mapping table to further leverage the benefits of solid state non-volatile memory connected to a host system while maintaining and enhancing parallel memory operations.

Ex. 1003 ¶ 233 (alteration in original). The Petition (Pet. 22–24) and the Declaration of Dr. Baker (Ex. 1003 ¶¶ 230–232, 234–239) provide substantial, additional reasoning supporting combining Bennett and Bruce. In contrast, Patent Owner’s argument is relatively conclusory and consists of unsupported attorney argument. *See* Prelim. Resp. 30–31. On this record, we determine that a skilled artisan would have been motivated to combine the relevant teachings of Bennett and Bruce.

We determine that, on the current record, Petitioners have met their burden to show the limitations of claims 9–15 and 34 of the ’740 patent are disclosed in Bennett and Bruce and that a skilled artisan would have been motivated to combine the relevant teachings of Bennett and Bruce. We also determine that there is a reasonable likelihood that Petitioners will prevail with respect to establishing that the combination of Bennett and Bruce renders obvious claims 9–15 and 34.

*I. Conclusion*

For the reasons discussed above, we determine that Petitioners have demonstrated a reasonable likelihood of showing at least one of the claims challenged in the Petition is unpatentable and institute *inter partes* review of claims 1, 9–15, 32, and 34 of the '740 patent on the grounds set forth in the Petition. *See* Pet. 2–3.

III. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of the '740 patent is instituted with respect to the challenged claims and the grounds set forth in the Petition; and

FURTHER ORDERED pursuant to 35 U.S.C. § 314(a) and 37 C.F.R. § 42.4(b), *inter partes* review of the '740 patent shall commence on the entry date of this Order, and notice is hereby given of the institution of a trial.

IPR2023-00742  
Patent 8,010,740 B2

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