

(FACE)

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

10/04/1999 TRADE1 00000001 022120 09399908
01 FC:201 380.00 OP

PTO-1556
(5/87)

*U.S. GPO: 1998-433-214/80404

Printed 06/07/20

APPLICATION NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO
09/399,908	09/21/1999	713	2182	1457P

APPLICANT
ROLAND F PORTMAN, PLEASANTON, CALIFORNIA; RICARDO H BRUCE, UNION CITY,
CALIFORNIA.

CONTINUING DOMESTIC DATA***
VERIFIED
NONE (HOD)

371 (NAT'L STAGE) DATA***
VERIFIED
NONE (HOD)

FOREIGN APPLICATIONS***
VERIFIED
NONE (HOD)

FOREIGN FILING LICENSE GRANTED 10/14/1999

SMALL ENTITY

Foreign priority claimed 35 USC 119 (a-d) conditions met. ☐ yes ☒ no	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
Verified and acknowledged <u>thd</u> <u>thd</u> Examiner's Name Initials	CA	5	18	2

ADDRESS
JOSEPH A SAWYER JR
SAWYER AND ASSOCIATES
POST OFFICE BOX 51418
PALO ALTO , CA 94303

TITLE
~~METHOD AND SYSTEM FOR CONTROLLING DATA IN A COMPUTER SYSTEM~~
Title Changed: see Paper # 7/A

FILING FEE RECEIVED \$**380	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT NO. _____ for the following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit
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1 of 2

THE COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, DC 20231

Attorney Docket: 1457P
PATENT

Sir:

Transmitted herewith for filing is the Patent Application of

Inventor: **Roland F. Portman and Ricardo H. Bruce**

For: **METHOD AND SYSTEM FOR CONTROLLING DATA IN A COMPUTER SYSTEM**

Enclosed with the Patent Application are:

- ☒ Five (5) sheet(s) of informal drawings
- ☒ Combined Declaration/Power of Attorney by Inventor(s)
- ☒ Declaration Claiming Small Entity Status
- ☒ Assignment and Recordation Form
- ☐ Information Disclosure Statement (PTO Form 1449)
- ☐ A certified copy of a _____ application.
- ☒ Self Addressed, Stamped Postcard

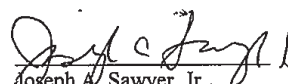
The filing fee has been calculated as shown below:

(Col. 1)		(Col. 2)	SMALL ENTITY	
FOR:	NO. FILED	NO. EXTRA	RATE	FEE
BASIC FEE				\$ 380.00
TOTAL CLAIMS	18 - 20	= 0	x 9 =	\$ 0.00
INDEP. CLAIMS	2 - 3	= 0	x 39 =	\$ 0.00
MULTIPLE DEPENDENT CLAIM PRESENTED			+125 =	\$ 0.00
*If the difference in Col. 1 is less than "0", enter "0" in Col. 2			TOTAL	\$ 380.00

☒ Please find enclosed check no. 11709 in the amount of **\$380.00** for payment of application filing fees.

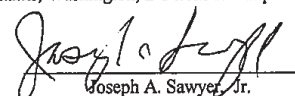
Respectfully submitted,

SAWYER AND ASSOCIATES
P.O. BOX 51418
Palo Alto, California 94303
(650) 493-4540


Joseph A. Sawyer, Jr.
Sawyer & Associates
Attorney for Applicants
Reg. No. 30,801

EXPRESS MAIL CERTIFICATE

I hereby certify that the above paper/fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated below and is addressed to the Commissioner of Patents and Trademarks, Washington, DC 20231. "Express Mail" no.: EL272673452US. Date of Deposit: September 21, 1999. Signature of person mailing paper/fee:


Joseph A. Sawyer, Jr.

UNITED STATES PATENT APPLICATION

FOR

~~METHOD AND SYSTEM FOR CONTROLLING DATA IN A COMPUTER SYSTEM~~

Inventors:
Roland F. Portman
Ricardo H. Bruce

Sawyer & Associates
2465 East Bayshore Road, Suite 406
Palo Alto, California 94303

METHOD AND SYSTEM FOR CONTROLLING DATA IN A COMPUTER SYSTEM

FIELD OF INVENTION

The present invention relates generally to computer systems and more particularly to a system and method for controlling data in such a system when the system loses external power.

BACKGROUND OF THE INVENTION

Most modern computer systems utilize various types of memory for handling data. A typical computer system consists of a central processing unit (CPU), cache memory, main memory, and long-term data storage such as a hard disk drive (HDD). Cache memory is significantly faster than main memory but has much less data capacity and more costly. Similarly main memory is significantly faster than a HDD, but also stores significantly less data and is more costly. Cache memory is very high speed memory designed to hold upcoming to-be-accessed and/or recently-accessed data. Data retrieved from the relatively slow HDD may be still be resident in the cache or in the main memory, thus the CPU can re-access that data from the cache many times faster than from main memory and hundreds of times faster than from the HDD. However, cache memory and main memory are characterized as volatile memory. Volatile memory (VM) is memory that contains data that is subject to erasure when the external power supply is shut down. A HDD is characterized as a non-volatile storage.

Consequently, the first problem that is encountered in this environment is that when there is an sudden loss of external power there is insufficient time to safely write all the

newly written and modified data from the VM to the HDD before the computer system shuts down. This poses a significant risk on the customer's data contained in the VM. Perhaps a very small amount of data could be safely saved to the HDD during the limited time available from detection to shutdown. However this would place a severe restriction on the amount of newly written and modified data that could be held in the VM which would basically eliminate the performance gains achieved by using the VM.

A battery could be coupled to the internal power system, however the use of batteries pose significant problems. Batteries have a limited number of charge-drain cycles, have a large internal resistance, and are physically very large and heavy. Additionally a HDD consumes significant amounts of power. The size and capacity of the batteries needed to supply power to the CPU, VM and HDD make them impractical. Alternatively a battery-backed uninterruptible power supply (UPS) could be connected in series with the external power source to provide power to the entire computer system in the event of a loss of external power. However, an UPS is physically large, heavy and relatively expensive.

Another significant problem associated with conventional computer technology is the ability to erase data from a HDD. Erasing all data from a disk, rapidly, and without the possibility of retrieval, is a mandatory requirement as an action of last resort for many applications. For example, if the data being stored is particularly valuable or otherwise sensitive and imminent access by hostile parties cannot be avoided, then the data must be destroyed instantaneously and irretrievably.

Normally when data is erased from a HDD, only the information to track the location of the files on the physical disk media is removed. This means that it is possible to retrieve the data by reconstructing the File Allocation Table (FAT). Some HDD erase utilities

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Accordingly, what is needed is a method for providing power to the computer system in the event of a sudden loss of power such that all newly written and modified data in the VM will be correctly stored in the non-volatile storage. What is further needed is method for rapidly erasing all data from a large non-volatile storage without the possibility of retrieval even in the event of a sudden loss of power. The method should be affordable and consume minimal space and weight. The present invention addresses such a need.

SUMMARY OF THE INVENTION

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automatically, in the event of a sudden loss of external power or manually. This capability consumes minimal space and weight and is implemented in an affordable manner.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a system in accordance with the present invention.

Figure 2 is a high-level flowchart of the first aspect of the method in accordance with the present invention.

Figure 3 is a flowchart of the operation of the first aspect of the method in accordance with the present invention.

Figure 4 is a high-level flowchart of the second aspect of the method in accordance with the present invention.

Figure 5 is a flowchart of the operation of the first aspect of the method in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides a method and system for controlling data in a computer system. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment will be readily apparent to those skilled in the art and the generic principles herein may be applied to other embodiments shown but it is to be accorded the widest scope consistent with the principles and features described herein.

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The method and system in accordance with the present invention contemplates the use of super-capacitors as a short term power source. With the advent of low cost super-capacitors available in values to over 10 Farads, large amounts of energy can be affordably stored internally in a very small space to use as a short term power source to extend operations well beyond a detected loss of external system power. The extended length of time can range from a few hundred milliseconds to tens of seconds depending on the value, quantity and configuration of the super-capacitors.

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To further understand the method and system in accordance with the present invention please refer to the formula $I = C \, dv/dt$ (Current in amperes is equal to the Capacitance in Farads times the change in voltage in Volts divided by the change in time in seconds), or $dt = C \, dv / I$. In order to increase the time, one can reduce the current, increase the amount of capacitance, or increase the change in voltage across the super-capacitor. The amount of capacitance is limited by the physical space of the enclosure and the current draw is fixed based on the operations that are taking place when the system in accordance with the present invention is activated. However, by increasing the voltage change of the capacitors, the amount of time available for the computer system to complete those operations is increased accordingly.

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To more specifically understand the method and system of the present invention refer now to the following detailed description of a preferred embodiment of a system 20 in accordance with the present invention along with the accompanying Figure 1. The computing engine CE 28 containing the processor, volatile and non-volatile memory, is supplied power from the external power source EPS 22 through the power isolator PI 26. The PI 26 isolates the CE 28 from the EPS 22. Power sensors 24 are implemented to notify the CE

26 of any sudden loss of power from the EPS 22.

An up-converter 32 is coupled to a plurality of super-capacitors SC 34 in order to convert the voltage supplied by the EPS 22 and charge the super-capacitors 34. Two charge level sensors 30 inform the CE 28 when the SC 34 are partially and fully charged. Once the SC 34 are fully charged, the demand for current is minimal and the charging circuit goes into trickle charge mode to keep the SC 34 at their peak charge value. A down converter DC 42 is also coupled to the SC 34 to convert the voltage from the SC 34 to supply power to the CE 28.

Preferably, the SC 34 chosen have an operating temperature range from -40C to +85C since many computer systems have an operating temperature range from -40C to +85C. If the SC 34 chosen have a higher minimum operating temperature, temperature sensors and controls 38 are utilized to activate thermal heaters 36 once the temperature falls below 0C to keep the SC 34 from becoming too cold. The heaters 36 are powered by the SC 34, but once the SC 34 fall below full charge, the temperature control circuit 38 is overridden and the heaters 36 are turned off to preserve the power stored in the super-capacitors 34. Additionally, a signal from the temperature sensors and controls 38 is sent to CE 28 warning that the SC 34 are below their minimum operating temperature.

If the SC 34 and the associated circuitry 30, 32, 36, 38, 42 are configured as a removable option to the system 20 a safety circuit 40 is necessary to automatically and fully discharge the super-capacitors 34 into a load resistor when they are removed. This will prevent injury to the technician and also prevent damage to SC 34 and the associated circuitry 30, 32, 36, 38, 42.

Although this invention is described in the context of utilizing three voltage converters, one of ordinary skill in the art will readily recognize that a variety of voltages could be used in

this system. Accordingly, the number of converters utilized could vary without departing from the spirit and scope of the present invention.

The method and system in accordance with the present invention is now disclosed in the context of a preferred embodiment. A first aspect of the preferred embodiment ensures that all data in the volatile memory are stored into the non-volatile memory without being lost or corrupted for all instances of power loss. A second aspect of the preferred embodiment of the method and system in accordance with the present invention allows a user to securely erase all the data in the non-volatile memory quickly and irretrievably either automatically or manually regardless of the availability of external power.

The method and system in accordance with the present invention preferably incorporates a three position manual switch 44, preferably located on the mechanical assembly containing the super capacitors and the associated circuitry, which allows the user to select 1 of 3 modes of operation, save mode, erase mode, and standby mode. Furthermore, a pushbutton 46 may be incorporated to permit the user to utilize the super-capacitor power source and command the CE 28 to erase all data from the non-volatile memory.

Although this invention is described in the context of utilizing a switch and pushbutton, one of ordinary skill in the art will readily recognize that a variety of methods to accomplish the same tasks could be used in this system. Accordingly, the switch and or pushbutton could be mounted externally from the system without departing from the spirit and scope of the present invention.

If the system is operating in save mode, the first aspect of the present invention is implemented wherein all data is automatically transferred from volatile memory to the non-volatile memory in the event of a sudden power loss from the external power source.

If the system is in erase mode, the second aspect of the present invention is implemented wherein all data is completely and irretrievably erased from the non-volatile memory in the event of a sudden power loss from the external power source.

In the save and erase modes, the super-capacitors will continue to discharge and power the computer system even after all the data has been transferred until the down-converter has insufficient voltage differential to continue proper operation and shuts down thus turning off the computer system. This will typically be only a few seconds.

Finally, if the system is in standby mode, the system will shut down when external power source is shut down, however the charge is maintained in the super-capacitors after the power is removed from the system. This mode incorporates a pushbutton which when depressed, will activate the super-capacitors to power up the system while simultaneously activating an erase command. This standby mode permits the system to be removed from the external power source and transported for an extended amount of time, while maintaining the ability to erase all the non-volatile memory if the pushbutton is depressed.

Although this invention is described in the context of the utilization of a manual switch and pushbutton, one of ordinary skill in the art will readily recognize that a variety of methods could be utilized while staying within the spirit and scope of the invention. For example, the concept of a manual pushbutton can easily be extended to a wireless pushbutton wherein a system fitted with the present invention containing a wireless receiver can be commanded to erase from a separate location.

To more particularly describe the "save mode" feature of the method in accordance with the present invention, please refer to flowchart of Figure 2. If a system is in "save mode" and is subsequently subjected to a sudden power loss, first, the super-capacitors are activated to maintain the internal power of the system, via step 50. Finally, data from the volatile memory is transferred to the non-volatile memory, via step 52. Through the use of the method in accordance with the present invention, a user is able to quickly and correctly transfer all data from volatile memory to non-volatile memory in the event of a sudden power loss.

To better understand the operation of the "save mode" feature of the method in accordance with the present invention, please refer to the flowchart of Figure 3. First, once the computer system detects that the external system power has fallen below a certain threshold amount via the power sensors, the up-converter is deactivated, via step 100. Next, the down-converter is activated to maintain the internal power of the system, via step 102. This reverses the flow of current between the computer system and the super-capacitors. The super-capacitors then begin to slowly discharge current to the computer system through the down-converter, via step 104. Then the computer system is isolated from the external power source, via step 105. This prevents any contention between the external power source and the down-converter. The rate of discharge depends on the amount of capacitance and the amount of current needed by the computer system. While the computer system is receiving current from the super-capacitors, data is transferred from the volatile memory to the non-volatile memory, via step 106. Next, the two charge level sensors inform the computer system that the super-capacitor voltage has fallen below the fully charged and partially charged levels, via step 108. Finally, once the super-capacitors discharge to a

predetermined level, the down-converter has insufficient voltage differential to continue proper operation and shuts down, thus turning off the power to the computer system, via step 110.

This has two positive side effects. First, if the output voltage from the down-converter were allowed to fall below the minimum operating voltage of the computer system, the computer system could continue to run with unpredictable and potentially serious results. Also, by not fully discharging the super-capacitors they will take only a few seconds to recharge once the external system power is restored, whereas the initial charge of super-capacitors may take up to 5 minutes. If, after all the data has been saved, the computer system detects the external power system is risen back to normal levels, the computer system is reconnected to the external power system, the super-capacitor down-converter is deactivated, and the up-converter is activated to recharge the super-capacitors. Accordingly, through the use of a system and method in accordance with the present invention, a user is able to accurately transfer all data from volatile storage to non-volatile memory in the event of a sudden power loss.

The "erase mode" of the method and system in accordance with the present invention is the second aspect of the present invention and is now described in the context of a preferred embodiment. The second aspect of the present invention focuses on a computer systems ability to securely erase all data even in event of a sudden power loss. The method and system in accordance with the present invention has the ability to irretrievably erase the entire contents of a large non-volatile memory hundreds of times faster than a conventional rotational hard disk drive. This is accomplished by erasing many non-volatile memory chips in

parallel. Consequently, the speed at which an entire non-volatile memory can be erased is only limited by the available power to the non-volatile memory chips.

To more particularly describe the "erase mode" feature of the method in accordance with the present invention, please refer to flowchart of Figure 4. If a system is in "erase mode" and is subsequently subjected to a sudden power loss, first, the super-capacitors are activated to maintain the internal power of the system, via step 200. Then an erase command is executed until completed, via step 202. Since the super-capacitors are preferably able to provide a significant amount of power to the computer system for a sufficient period of time, the method and system in accordance with the present invention has the ability to complete the entire erase operation in the event of a external system power loss.

To further understand the operation of the "erase mode" feature of the method in accordance with the present invention, please refer to the flowchart of Figure 5. First, once the computer system detects that the external system power has fallen below a certain threshold amount, the up-converter is deactivated, via step 300. Next, the down-converter is activated to maintain the internal power of the system, via step 302. This reverses the flow of current between the volatile memory and the super-capacitors. The super-capacitors then begin to slowly discharge current to the computer system through the down-converter, via step 304. The computer system is then isolated from the external power source, via step 305. This prevents any contention between the external power source and the down-converter. The rate of discharge depends on the amount of capacitance and the amount of current needed by the computer system. While the computer system is receiving current from the super-capacitors, all traces of data in the volatile memory is completely erased, via step 306. Next, the two charge level sensors inform the computer system that the super-capacitor voltage has fallen

below the fully charged and partially charged levels, via step 308. Finally, once the super-capacitors discharge to a predetermined level, the down-converter has insufficient voltage differential to continue proper operation and shuts down, thus turning off the power to the computer system, via step 310.

5 This has two positive side effects. First, if the output voltage from the down-converter were allowed to fall below the minimum operating voltage of the computer system, the computer system could continue to run with unpredictable and potentially serious results. Also, by not fully discharging the super-capacitors they will take only a few seconds to recharge once the external system power is restored, whereas the initial charge of super-capacitors may take up to 5 minutes.

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A significant feature of the second aspect of the present invention is the "standby mode" which provides the ability to erase data manually while the system is removed from the system. This is preferably done with the incorporation of a pushbutton. Once the super-capacitors are fully charged, the system may be removed from external system power and the super-capacitors will retain a sufficient charge for all modes of operation preferably for up to 60 minutes. Thus, if a system containing sensitive data is being transported, the erase command can be activated by depressing the external pushbutton connected to the system, at which time the system will be powered up and the entire contents of the non-volatile memory will be rapidly and irretrievably erased.

20 Through the use of a system and method in accordance with the present invention, a user is able to accurately transfer all data from volatile memory to non-volatile memory in the event of a sudden external system power loss. Furthermore, the user of a system and method in accordance with the present invention will be able to rapidly and irretrievably

erase all data from the non-volatile memory manually or automatically in the event of a sudden external system power loss. These features consume minimal space and are implemented in an affordable manner.

5 Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.

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CLAIMS

What is claimed is:

- 1 *Sub* 1. ~~A method for controlling data in a computer system when the computer~~
2 ~~system loses power, the computer system comprising a computing engine, comprising the~~
3 ~~steps of:~~
4 ~~(a) activating a plurality of super capacitors to supply power to the~~
5 ~~computing engine based upon power being removed from the computer system; and~~
6 ~~(b) reconfiguring the data in the computing engine.~~
- 1 2. The method of claim 1 wherein the computing engine comprises a least one
2 volatile memory and at least one non-volatile memory.
- 1 3. The method of claim 2 wherein the reconfiguring step (b) further comprises:
2 (b1) allowing all data to be transferred from the at least one volatile
3 memory to the at least one non-volatile memory.
- 1 4. The method of claim 2 wherein the reconfiguring step (b) further comprises:
2 (b1) allowing all data in the at least one volatile memory to be erased.
- 1 5. The method of claim 4 wherein the reconfiguring step (b) further comprises:
2 (b2) allowing all data in the at least one non-volatile memory to be erased.

1 6. The method of claim 3 wherein the activating step (a) further comprises:
2 (a1) reversing the flow of current between the computing engine and the
3 plurality of super capacitors; and

4 (a2) discharging current from the plurality of super capacitors to the
5 computing engine.

1 7. The method of claim 4 wherein the activating step (a) further comprises:

2 (a1) reversing the flow of current between the computing engine and the
3 plurality of super capacitors; and

4 (a2) discharging current from the plurality of super capacitors to the
5 computing engine.

1 8. The method of claim 5 wherein the allowing step (b2) is initiated based upon a
2 user interaction.

1 9. The method of claim 8 wherein the user interaction is the depressing of a
2 button.

1 ~~10. A system for controlling data in a computer system when the computer system~~
2 ~~loses power, the computer system comprising a computing engine, comprising:~~
3 ~~means for activating a plurality of super capacitors to supply power to the~~
4 ~~computing engine based upon power being removed from the computer system; and~~
5 ~~means for reconfiguring the data in the computing engine.~~

1 11. The system of claim 10 wherein the computing engine comprises a least one
2 volatile memory and at least one non-volatile memory.

1 12. The system of claim 11 wherein the reconfiguring means further comprises:
2 means for allowing all data to be transferred from the at least one volatile
3 memory to the at least one non-volatile memory.

1 13. The system of claim 11 wherein the reconfiguring means further comprises:
2 means for allowing all data in the at least one volatile memory to be erased.

1 14. The system of claim 13 wherein the allowing means further comprises:
2 means for allowing all data in the at least one non-volatile memory to be
3 erased.

1 15. The system of claim 12 wherein the activating means further comprises:
2 means for reversing the flow of current between the computing engine and the
3 plurality of super capacitors; and
4 means for discharging current from the plurality of super capacitors to the
5 computing engine.

1 16. The system of claim 13 wherein the activating means further comprises:
2 means for reversing the flow of current between the computing engine and the

3 plurality of super capacitors; and
4 means for discharging current from the plurality of super capacitors to the
5 computing engine.
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1 17. The system of claim 14 wherein the allowing means is initiated based upon a
2 user interaction.

1 18. The system of claim 17 wherein the user interaction is the depressing of a
2 button.

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ABSTRACT

See ~~The present invention discloses a method and system for controlling data in a~~
computer system when the computer system loses power, the computer system comprising a
computing engine. The method and system comprises activating a plurality of super
capacitors to supply power to the computing engine based upon power being removed from
the computer system and reconfiguring the data in the computing engine. Through the use of
a system and method in accordance with the present invention, a user is able to correctly
store large amounts of newly written and modified data from the volatile memory to the non-
volatile memory in the event of a sudden external system power loss. Furthermore, the user
of a system and method in accordance with the present invention will be able to rapidly and
irretrievably erase data from the non-volatile memory automatically, in the event of a sudden
loss of external power or manually. This capability consumes minimal space and weight and
~~is implemented in an affordable manner.~~

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DECLARATION AND POWER OF ATTORNEY FOR UTILITY PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name,

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD AND SYSTEM FOR CONTROLLING DATA IN A COMPUTER SYSTEM

the specification of which

X is attached hereto.
_____ was filed on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I do not know and do not believe that the same was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and said invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application.

I acknowledge the duty to disclose information which is material to the examination and patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56 (a).

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119, of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

Priority Claimed

(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status -- patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status -- patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such wilful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number).

Joseph A. Sawyer, Jr. Reg. No. 30,801
Stephen G. Sullivan, Reg. No. 38,329

Janyce R. Mitchell, Reg. No. 40,095
Michele Liu, Reg. No. P44,875

as my attorney with full power of substitution and revocation to transact all business in the United States Patent and Trademark Office connected herewith.

Send all correspondence to:

Joseph A. Sawyer, Jr.
SAWYER & ASSOCIATES
Post Office Box 51418
Palo Alto, California 94303

Direct all telephone calls to:

Joseph A. Sawyer, Jr. at (650) 493-4540

Full Name of first Inventor:

Roland F. Portman

Residence Address:

3001 Warrenton Court
Pleasanton Alameda California 94588
City County State Zip

Post Office Address:

SAME

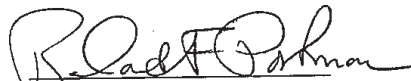
Citizenship:

United States of America

Date

Sept 15, 1999

Signature of Inventor



Full Name of second Inventor:

Ricardo H. Bruce

Residence Address:

33041 Regents Boulevard
Union City Alameda California 94587
City County State Zip

Post Office Address:

SAME

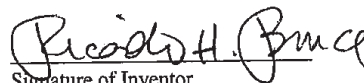
Citizenship:

United States of America

Date

Sept 15, 1999

Signature of Inventor



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Portman et al.

Serial No.:

Filed: **Herewith**

For: **METHOD AND SYSTEM FOR CONTROLLING DATA IN A COMPUTER SYSTEM**

**DECLARATION CLAIMING SMALL ENTITY
STATUS UNDER 37 CFR 1.9(f) and 1.27(c)
SMALL BUSINESS CONCERN**

0370900-09219
56720-00550

I hereby declare that I am

- ☐ the owner of the small business concern identified below:
☒ an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN
ADDRESS OF CONCERN

BiT Microsystems, INC.
48499 Milmont Drive
Fremont, California 94538

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal years, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention entitled **METHOD AND SYSTEM FOR CONTROLLING DATA IN A COMPUTER SYSTEM** by inventor(s) Roland F. Portman and Ricardo H. Bruce, described in the application filed herewith.

The rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(d) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

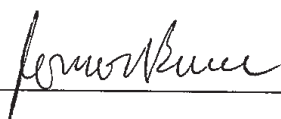
*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

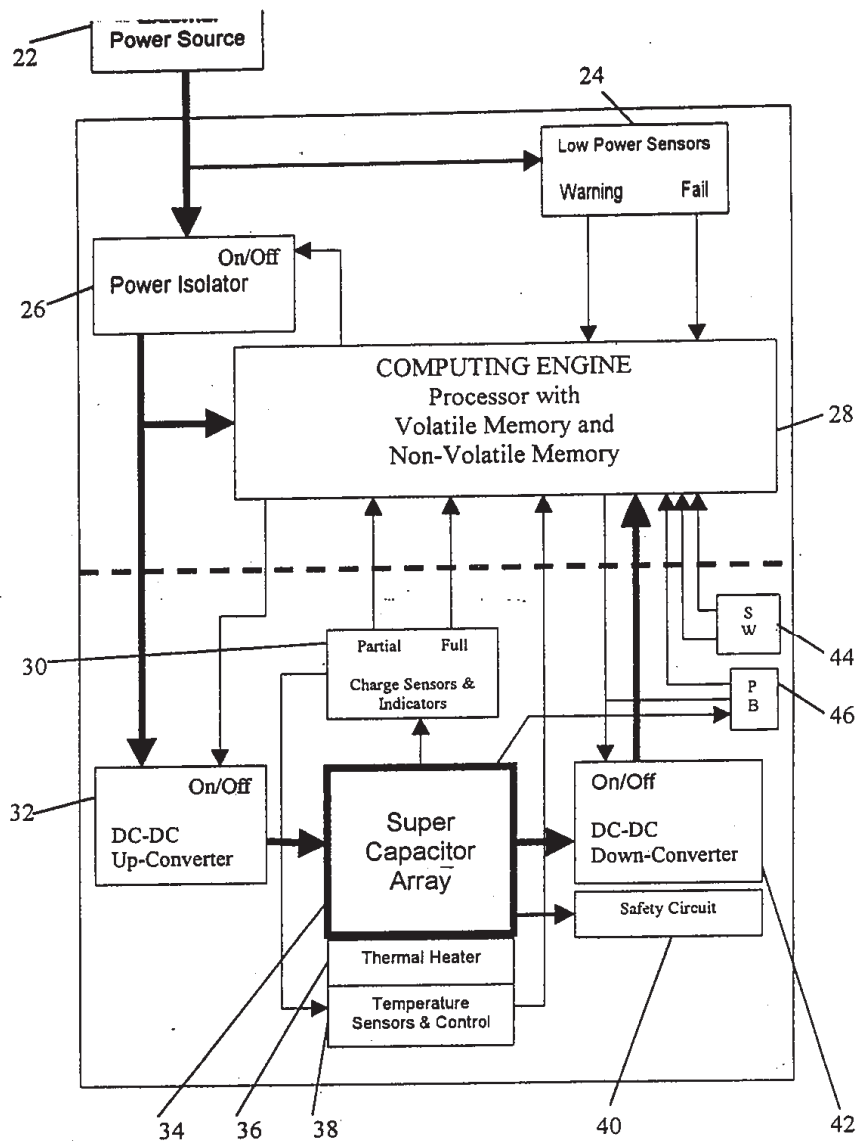
I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this declaration is directed.

NAME OF PERSON SIGNING:
TITLE OF PERSON OTHER THAN OWNER:
ADDRESS OF PERSON SIGNING:

Romeo H. Bruce
President
48499 Milmont Drive
Fremont, California 94538

SIGNATURE: 

DATE: 9/15/99



20

FIGURE 1

00399908-092199

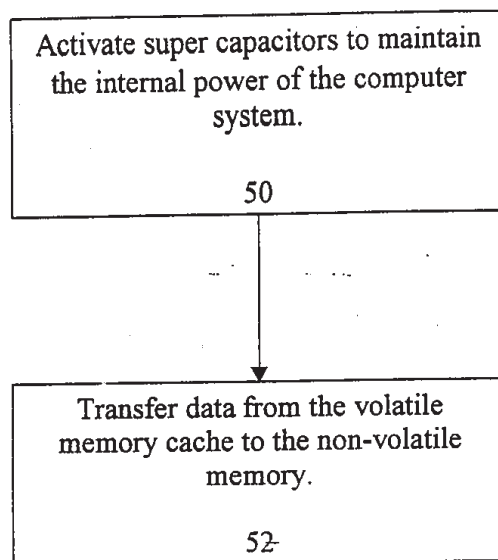


FIGURE 2

09399900-091499

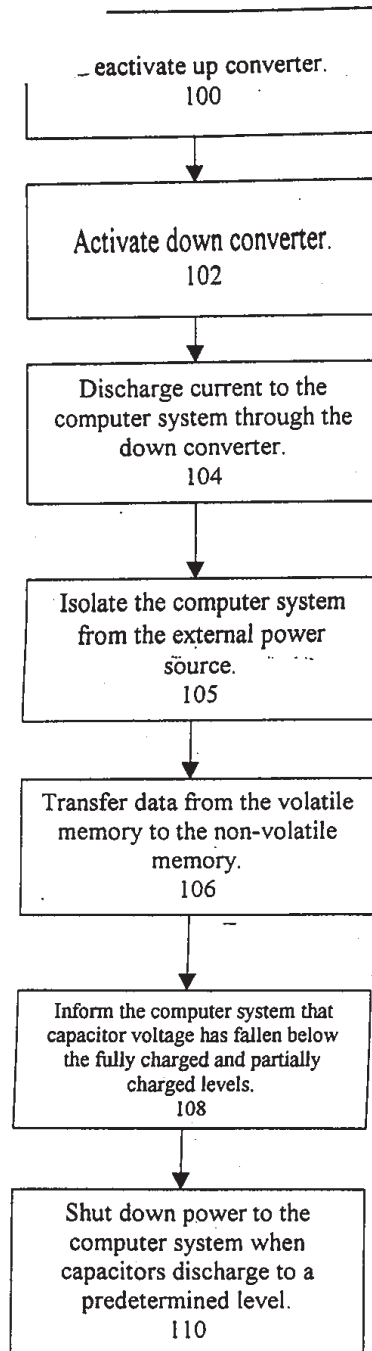


FIGURE 3

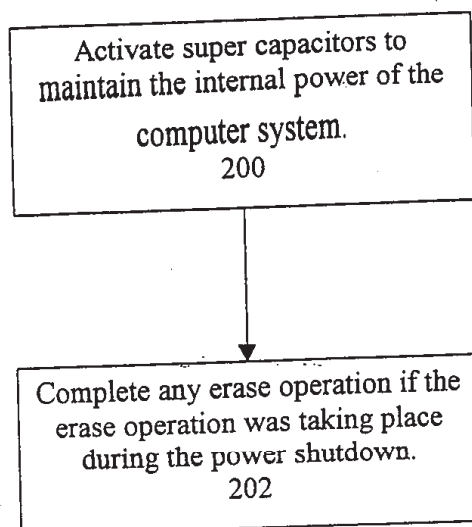


FIGURE 4

651250-90666560

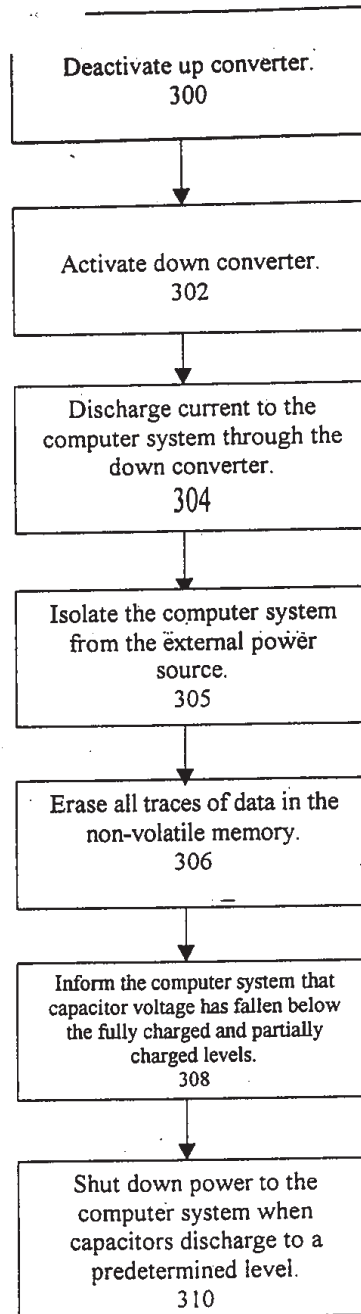
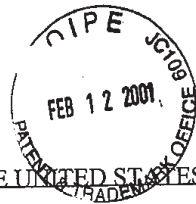


FIGURE 5



Attorney Docket: 1457P

2787
2/17/01
2188m

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Date: February 9, 2001

Portman et al.

Serial No.: 09/399,908

Group Art Unit: 2787

Filed: September 21, 1999

Examiner: Unknown

For: METHOD AND SYSTEM FOR CONTROLLING DATA IN A COMPUTER
SYSTEM

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

MAILED

FEB 16 2001

Technology Center 2100

TRANSMITTAL LETTER

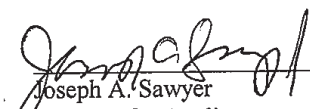
Sir:

Please find enclosed the following documents relating to the above-mentioned patent application:

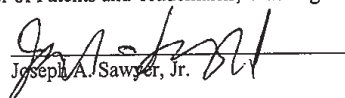
- 1) Information Disclosure Statement: Form PTO-1449 and four (4) references
- 2) Transmittal Letter (original and two copies)
- 3) Post card.

If any unresolved issues remain, please contact Applicant's attorney at the telephone number indicated below.

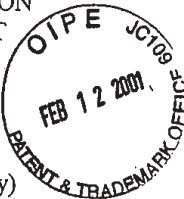
Respectfully submitted,


Joseph A. Sawyer
Attorney for Applicant
Reg. No. 30,801
(650) 493-4540

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner of Patents and Trademarks, Washington, D.C. 20231, on February 9, 2001.


Joseph A. Sawyer, Jr.

FORM PTO-1449 (Modified)

LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANT'S INFORMATION
DISCLOSURE STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.

1457P

SERIAL NO.

09/399,908

APPLICANT:

Portman et al

FILING DATE:

9/21/1999

GROUP:

2787

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
<i>MD</i>	5 7 9 9 2 0 0	Aug 25 1998	Brant et al	—	—	
<i>MD</i>	5 5 4 2 0 4 2	Jul 30 1996	Manson	—	—	

MAILED
FEB 16 2001
Technology Center 2100

FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation
<i>MD</i>	EP 0 4 5 8 5 1 0	Nov 27 1991	Europe	—	—	YES NO
<i>MD</i>	EP 0 9 6 4 3 6 0	Dec 15 1999	Europe	—	—	

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER

Myal She S

DATE CONSIDERED

6/13/2001

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/399,908 09/21/99 PORTMAN

R 1457P

EXAMINER

TM01/0615

JOSEPH A SAWYER JR
SAWYER AND ASSOCIATES
POST OFFICE BOX 51418
PALO ALTO CA 94303

DHARIA, R

ART UNIT

PAPER NUMBER

2181

DATE MAILED:

06/15/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/399,908	PORTMAN ET AL.	
	Examiner	Art Unit	
	Rupal D. Dharla	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 September 1999.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

- 15) ☒ Notice of References Cited (PTO-892)
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 18) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other:

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 250 words. It is important that the abstract not exceed 250 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 6, 7, 10-13, 15, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Manson (5,542,042).

a. As per claims 1 and 10, Manson teaches a system and method for controlling data in a computer system when the system loses power; comprising a computing engine; and activating a plurality of super capacitors to supply power to the computing engine based

upon power being removed from the computer system and reconfiguring the data in the computing engine (Fig. 4; col. 1, lines 11-35; col. 3, line 19 thru col. 4, line 65).

b. As per claims 2 and 11, Manson discloses the claimed invention as described above and furthermore teaches at least one volatile memory and at least one non-volatile memory (Fig. 4; col. 1, lines 11-35; col. 3, line 19 thru col. 4, line 65).

c. As per claims 3 and 12, Manson discloses the claimed invention as described above and furthermore teaches allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory (Fig. 4; col. 1, lines 11-35; col. 3, line 19 thru col. 4, line 65).

d. As per claims 4 and 13, Manson discloses the claimed invention as described above and furthermore teaches allowing all data in the at least one volatile memory to be erased (Fig. 4; col. 1, lines 11-35; col. 3, line 19 thru col. 4, line 65).

e. As per claims 6 and 15, Manson discloses the claimed invention as described above and furthermore teaches reversing the flow of current between the computing engine and the plurality of super capacitors; and discharging current from the plurality of super capacitors to the computing engine (Fig. 4; col. 1, lines 11-35; col. 3, line 19 thru col. 4, line 65).

f. As per claims 7 and 16, Manson discloses the claimed invention as described above and furthermore teaches reversing the flow of current between the computing engine and the plurality of super capacitors; and discharging current from the plurality of super capacitors to the computing engine (Fig. 4; col. 1, lines 11-35; col. 3, line 19 thru col. 4, line 65).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 5, 8, 9, 14, 17, and 18, are rejected under 35 U.S.C. 103(a) as being unpatentable over Manson (5,542,042) in view of Bruwer et al. (5,768,208).

g. As per claims 5 and 14, Manson discloses the claimed invention as described above. Manson does not explicitly teach erasing the non-volatile memory. Bruwer teaches a super capacitor system and that it is known to erase a non-volatile memory (Fig. 2B; col. 1 thru col. 8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the above as taught by Bruwer in the system of Manson because to prevent "soft writes" as taught by Bruwer (col. 1, lines 13-67).

h. As per claims 8, 9, 17, and 18, Manson and Bruwer disclose the claimed invention as described above. However, Manson and Bruwer do not explicitly teach a user interaction and a pressing of a button. Official notice is taken in that both the concept and advantages of a user interaction of pressing a button to cause an event to occur is well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the above in the system of Manson and Bruwer, because the system can be controlled by software or hardware and the user interaction could give specific control to the user when to erase a memory.

Application/Control Number: 09/399,908
Art Unit: 2181

Page 5

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rupal D. Dharia whose telephone number is (703) 305-4003.

The examiner can normally be reached on M-F 7:00AM-3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoleil can be reached on (703) 305-9713. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-6296 for regular communications and (703) 308-6296 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3600.


Rupal D. Dharia
Primary Examiner
Art Unit 2181

RDD
June 13, 2001

FORM PTO-892		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		SERIAL NO. 09/399,908	GROUP ART UNIT 2181	ATTACHMENT TO PAPER NO.	3
NOTICE OF REFERENCES CITED				APPLICANT(S) Portman et al.			
U.S. PATENT DOCUMENTS							
*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	A	5,768,208	6/1998	Bruwer et al	365	228	
	B	4,449,205	5/1984	Hoffman	365	185.08	
	C	4,807,141	2/1989	Muller			
	D	4,965,828	10/1990	Ergott Jr. et al.	380	50	
	E	4,999,575	3/1991	Germer	324	142	
	F						
	G						
	H						
	I						
	J						
	K						
FOREIGN PATENT DOCUMENTS							
*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS
	L						
	M						
	N						
	O						
	P						
	Q						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)							
	R						
	S						
	T						
	U						
EXAMINER Rupal Dharja		DATE June 13, 2001					
* A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05(a).)							

Form892ccs2106b

L Number	Hits	Search Text	DB	Time stamp
1	2183	((713/300-340).CCLS.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/07/24 08:42
2	564	((714/2) or (714/14) or (714/22)).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/07/24 08:42
3	2646	((713/300-340).CCLS.) or ((714/2) or (714/14) or (714/22)).CCLS.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/07/24 08:42
4	15975	capacitor adj discharg\$	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/07/24 08:43
5	27	(capacitor adj discharg\$) and ((713/300-340).CCLS.) or ((714/2) or (714/14) or (714/22)).CCLS.))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/07/24 08:43
6	20	(capacitor adj discharg\$) same (volatile or non-volatile)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/07/24 08:43
7	280	capacitor adj2 supply adj2 power	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/07/24 08:44
8	65	erase adj (volatile or non-volatile)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/07/24 08:44
9	1	(capacitor adj2 supply adj2 power) and (erase adj (volatile or non-volatile)) and ((713/300-340).CCLS.) or ((714/2) or (714/14) or (714/22)).CCLS.))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/07/24 08:44
10	4	(capacitor adj2 supply adj2 power) and (erase adj (volatile or non-volatile))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/07/24 08:44

Search History 7/24/02 8:44:45 AM Page 1

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-	2130	((713/300-340).CCLS.) or ((714/2) or (714/14) or (714/22)).CCLS.)	USP&T; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2002/07/24 08:42
-	0	portman-roland\$.in.	USP&T; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/06/07 15:05
-	4	bruce-ricardo\$.in.	USP&T; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/06/07 15:06
-	15154	capacitor adj discharg\$	USP&T; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2002/07/24 08:42
-	24	(capacitor adj discharg\$) and ((713/300-340).CCLS.) or ((714/2) or (714/14) or (714/22)).CCLS.)	USP&T; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/06/07 15:07
-	16	(capacitor adj discharg\$) same (volatile or non-volatile)	USP&T; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/06/07 15:14
-	243	capacitor adj2 supply adj2 power	USP&T; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2002/07/24 08:43
-	55	erase adj (volatile or non-volatile)	USP&T; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2002/07/24 08:43

-	1	((capacitor adj2 supply adj2 power) and (erase adj (volatile or non-volatile))) and (((713/300-340).CCLS.) or ((714/2) or (714/14) or (714/22).CCLS.))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/06/07 15:15
-	4	(capacitor adj2 supply adj2 power) and (erase adj (volatile or non-volatile))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2002/07/24 08:44

EAST - [399908.wsp:1]

File View Edit Tools Window Help

☒ Drafts
☐ Pending
☒ Active

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L4: (0) portman-roland\$.in.
L5: (4) bruce-ricardo\$.in.
L6: (15154) capacitor adj discharg\$
L7: (24) 6 and 3
L8: (16) 6 same (volatile or non-volatile)
L9: (243) capacitor adj2 supply adj2 power
L10: (55) erase adj (volatile or non-volatile)
L11: (1) 11 and 3
L12: (4) 9 and 10

☐ Failed
☐ Saved
☐ Favorites
☐ Tagged

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9 and 10

SPS form SAR form Image Text

	U	A	Document ID	Issue Date	Pages	Title	Current OP	Current Wd
1	☐	☐	US 5768208 A	19980616	8	Fail safe non-volatile memory programming system	365/228	365/185.04 ; 365/185.0
2	☐	☐	US 4673872 A	19870616	19	Packaging for electronic demand register	324/103R	235/1D ; 361/659
3	☐	☐	US 4631476 A	19861223	18	Memory programmer interface for electronic demand	324/103R	324/157
4	☐	☒	US 4627000 A	19861202	9	Apparatus and method for copying data from one	713/300	324/103R ; 324/116

Ready

NUM

EAST - [default.wsp:1]

File View Edit Tools Window Help

☐ Drafts
☒ Pending
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☐ Failed
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☐ Favorites
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☐ Queue
☐ Trash

L1: (1736) ("713/300-340").CCLS.
 L2: (480) (("714/2") or ("714/14") or ("714/22")).CCL
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 L4: (0) portman-roland\$.in.
 L5: (4) bruce-ricardo\$.in.
 L6: (15154) capacitor adj discharg\$
 L7: (24) 6 and 3
 L8: (16) 6 same (volatile or non-volatile)

DBs: USPAT,USPGPUB,EPU,JPT
 Default operator: OR
 Highlight all hit terms in hit

6 same (volatile or non-volatile)

BRS form S&R form Image Text

	U	Document ID	Issue Date	Pages	Title	Current OR	Current X
☐	☒	US 4999575 A	19910312	17	Power supply and monitor for controlling an electrical	324/142	324/103R ; 324/116
☐	☒	US 4965828 A	19901023	21	Non-volatile semiconductor memory with SCRAM hold cycle	713/193	307/64 ; 365/229
☐	☒	US 4807141 A	19890221	13	Postage meter with microprocessor controlled	705/405	
☐	☒	US 4449205 A	19840515	13	Dynamic RAM with non-volatile back-up storage	365/185.08	365/185.19 ; 365/200

☒ Hits ☐ Details

Ready

NUM

DOCUMENT-IDENTIFIER: US 5768208 A
TITLE: Fail safe non-volatile memory programming system and
method therefor

DEPR:

A high voltage charging capacitor 16 is coupled to the non-volatile memory device 12. The high voltage charging capacitor 16 is used for storing a charge that must be sufficient before the non-volatile memory 12 is to be programmed (i.e, write to or erase the non-volatile memory device 12). The high voltage charging capacitor 16 is then used for supplying a programming voltage to the non-volatile memory device 12.

DEPR:

The control unit 26 and the latching device 28 are powered by an analog voltage supply AV.sub.dd. In the preferred embodiment of the present invention, the analog voltage supply AV.sub.dd provides a 5 volt charge. If the analog voltage supply AV.sub.dd is interrupted, a low voltage charging capacitor 30 is provided to supply the required power to the control unit 26 and the latching device 28 in order to complete the programming cycle. In another embodiment of the present invention, the high voltage charging capacitor 16 is also coupled to a latching device 28. The high voltage charging capacitor 16 thus is able to supply power to the latching device 28 so that the latching device 28 does not have to depend on the analog voltage source AV.sub.dd. In such an implementation, the high voltage charging capacitor 16 will normally be connected to an external voltage source V.sub.DD while the high voltage generator 18 is not functioning.

06/07/2001, EAST Version: 1.02.0008

DOCUMENT-IDENTIFIER: US 4807141 A
TITLE: Postage meter with microprocessor controlled reset
inhibiting means

BSPR:

An early, typical, system for protecting data in the event of a power failure condition in an electronic postage meter is shown in U.S. Pat. No. 3,978,457 for MICROCOMPUTERIZED ELECTRONIC POSTAGE METER SYSTEM. In this system, when the supply voltage drops below a threshold level, a shut down signal is generated which causes the postage meter's microcomputer to initiate a shut down routine. As part of the shut down routine, the contents of a working, random access, memory are transferred to a non-volatile memory. Power is made available during the time period needed to detect the shut down signal and to transfer the register contents from the working memory to the non-volatile memory by providing the power supply with at least one large filter capacitor which discharges during a time interval of sufficient length to maintain a working voltage range during the time period.

DOCUMENT-IDENTIFIER: US 4449205 A
TITLE: Dynamic RAM with non-volatile back-up storage and method
of operation
thereof

BSPR:

Further in accordance with the invention, there is provided a method for operating such a memory cell. To transfer data from the volatile dynamic element to the non-volatile cell, the floating gate is driven first positive and then negative. In the positive state, a positive charge is stored on the floating gate if the data at the data node is a data 0. Otherwise, during the negative state, a negative charge is stored on the floating gate if the data of the data node is a data 1. In either case, the potential of the floating gate is changed by current flowing through the DEIS material layer. To recover data stored on the floating gate, that is, to transfer the data stored on the floating gate in the non-volatile element of a memory cell to the dynamic portion of the cell, the data node of the dynamic cell is first forced to a data 1 state. Then, the second control gate of the dual gate FET is taken to a positive level. The floating gate, if it is then charged with a positive charge, will, in cooperation with the positive level on the second control gate, turn on the channel of the dual gate FET, and hence the charge on the data storage capacitor is discharged through the dual gate FET to ground. If the floating gate is charged negatively, the channel region under the floating gate of the second FET will be off so that the data storage capacitor is not discharged, and hence the data node will remain at the data 1 level. The second control gate voltage is then returned to ground to allow normal operations to commence.

06/07/2001, EAST Version: 1.02.0008

DOCUMENT-IDENTIFIER: US 4627000 A
TITLE: Apparatus and method for copying data from one electronic demand register to another

DEPR:

In summary, when a momentary power outage on lines 26 and 28 causes the voltage of the unregulated DC voltage to fall below a first threshold value, a timer is started. If the unregulated DC voltage does not rise above a second threshold, slightly higher than the first threshold before the timer times out, processor 52 is commanded to transfer billing data and programmed constants to non-volatile memory 64. A capacitor in power supply and power monitor 66 stores sufficient energy to maintain operation of demand register 46 for the duration of the timer delay, and to then have sufficient energy remaining therein to write the billing data and programmed constants to non-volatile memory 64.

DEPR:

After the data read out from non-volatile memory 64 into temporary storage in temporary storage 78 has been copied into a replacement non-volatile memory 64', the ground signal on processor reset hold signal line 72 may be removed. This permits processor reset generator 71 to generate a reset signal which, among other things, reads the copied contents of non-volatile memory 64 into processor 52 in order to enable testing of demand register 46. When demand register 46 is physically removed from non-volatile memory copy programmer 74 and power is thereby cut off from demand register 46, the apparent power outage is effective in the manner described to erase non-volatile memory 64 and store the data therein. When demand register 46 is installed in an electric meter, and the voltage applied thereto rises above a predetermined

value, the stored
content of non-volatile memory 64 is returned to processor 52.

CCOR:
713/300



Attorney Docket: 1457P

4
12-28-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Date: December 17, 2001

Portman, et al.

Serial No.: 09/399,908

Group Art Unit: 2181

Filed: September 21, 1999

Examiner: Dharia, R.

For: METHOD AND SYSTEM FOR CONTROLLING DATA IN A COMPUTER
SYSTEM

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

**PETITION FOR EXTENSION OF TIME
UNDER 37 C.F.R. § 1.136**

RECEIVED
DEC 26 2001
Technology Center 2100

Sir:

In response to the Office Action dated June 15, 2001, Applicant petitions the Commissioner of Patents and Trademarks to extend the deadline for filing a response by three (3) months from September 15, 2001 to December 17, 2001.

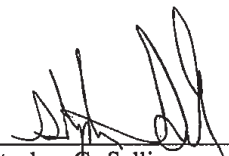
Enclosed is check no. 3797 in the amount of \$ 460.00 for payment of the three month extension of time fee.

Respectfully submitted,

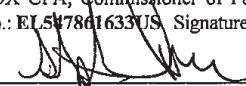
12/26/2001 AWONDAF1 00000048 09399908

01 FC:217

460.00 OP


Stephen G. Sullivan
Sawyer Law Group LLP
Attorney for Applicant (s)
Reg. No. 38,329
(650) 493-4540

I hereby certify that this correspondence is being deposited with the United States Postal Service "Express Mail to Addressee" service under 37 CFR 1.10, and is addressed to BOX CPA, Commissioner of Patents and Trademarks, Washington, D.C. 20231, on December 17, 2001, Express Mail No.: EI 547861633 US. Signature of Person mailing paper or fee:


Stephen G. Sullivan



12-21-01

Attorney Docket: 1457P

CPA/27
5
12-3

CONTINUED PROSECUTION APPLICATION TRANSMITTAL

218)

Prior Application:

Serial No.: 09/399,908
Inventor: Portman, et al.
Filing Date: September 21, 1999
Examiner: Dharia, R.
Group Art: 2181
Assignee: Bit Microsystems, Inc.

Title: Method and System for Controlling
Data in a Computer System

Box CPA
Commissioner of Patents and Trademarks
Washington, D.C. 20231

RECEIVED
DEC 26 2001
Technology Center 2100

This is a request to file a Continued-Prosecution Application

☒ continuation
☐ divisional

under 37 CFR 1.53(d) for the above-identified application.

- ☒ This communication is a request for filing an application under 1.53(d). Please utilize the file jacket and contents of the prior application, including the specification, drawings and oath or declaration from the prior application, to constitute the new application.
- ☒ For identification purposes, please assign the serial number of the prior application to that of the continuation application in accordance with 37 CFR 1.53(d)(2)(iv).
- ☒ Please abandon the prior application as of the filing date of this request for a continued prosecution application under 37 CFR 1.53(d)(2)(v).

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service "Express Mail to Addressee" service under 37 CFR 1.10, and is addressed to BOX CPA, Commissioner of Patents and Trademarks, Washington, D.C. 20231, on December 17, 2001, Express Mail No.: EL547861633US. Signature of Person mailing paper or fee:

Stephen G. Sullivan

EL547861633US

12/26/2001 AMNDPFI 00000047 09399908
370.00 DP
01 FC:231

CLAIMS AND FILING FEES

- ☒ Amendment is not enclosed.
- ☐ Cancel in this application claim(s) _____ of the prior application before calculating the filing fee.
- ☐ Cancel in this application all claims of the prior application and substitute the claims contained in the attached Amendment prior to calculating the filing fee.
- ☐ Add the additional claims in the attached Amendment prior to calculating the filing fee.
- ☐ Enter all amendments requested pursuant to 37 CFR 1.116 but unentered in the prior application.

THE FILING FEE IS CALCULATED AS FOLLOWS:

FOR	NUMBER FILED	NUMBER EXTRA		RATE	FEE
Small Entity				\$370.00	\$ 370.00
Total Claims	18 - 20	= 0	x	\$ 9.00	\$ 0.00
Indep. Claims	2 - 3	= 0	x	\$ 42.00	\$ 0.00
1+ Multiple dependent Claim				\$140.00	\$ 0.00
TOTAL FILING FEE					<u>\$ 370.00</u>

- ☒ A check in the amount of \$ 370.00 for payment of continuation application filing fees is enclosed.
- ☒ A check in the amount of \$ 460.00 for payment of a THREE (3) month Extension of Time in Prior Application is enclosed.

The Commissioner is hereby authorized to charge any additional fees which may be required or credit any overpayment to Deposit Account No. 02-2120 (Sawyer Law Group LLP):

In accordance with 37 CFR 1.53(d)(8), the following information relating to the prior application is the same for the purposes of the continued-prosecution application filed under 37 CFR 1.53(d):

Title: METHOD AND SYSTEM FOR CONTROLLING DATA IN A COMPUTER SYSTEM

Applicant(s): Roland F. Portman
3001 Warrenton Court
Pleasanton, California 94588

Ricardo H. Bruce
33041 Regents Blvd.
Union City, California 94587

Citizenship: USA USA

Assignee: Bit Microsystems, Inc.
48499 Millmont Drive
Fremont, California 94538

Recordation Date: September 21, 1999
Reel/Frame: 010280/0764

Attorney/Agent of Record:

Joseph A. Sawyer, Jr.
Reg. No. 30,801

Janyce R. Mitchell
Reg. No. 40,095

Stephen G. Sullivan
Reg. No. 38,329

Michele Liu
Reg. No. 44,875

Joyce Tom
Reg. No. 48,681

Address future correspondence to:

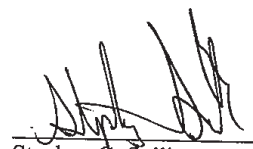
Sawyer Law Group LLP
P.O. Box 51418
Palo Alto, California 94303

Facsimile: (650) 493-4549

Direct all telephone calls to:

Joseph A. Sawyer, Jr.
(650) 493-4540

Respectfully submitted,



Stephen G. Sullivan
Sawyer Law Group LLP
Attorney for Applicants
Reg. No. 38,329

12/17/01

Date

8



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/399,908	09/21/1999	ROLAND F. PORTMAN	1457P	2827

7590 01/28/2002

JOSEPH A SAWYER JR
SAWYER AND ASSOCIATES
POST OFFICE BOX 51418
PALO ALTO, CA 94303

EXAMINER

DHARIA, RUPAL

ART UNIT PAPER NUMBER

2181

DATE MAILED: 01/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s) <u>H. G.</u>	
	09/399,908	PORTMAN ET AL.	
	Examiner	Art Unit	
	Rupal D. Dharja	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 17 December 2001.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-18 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____

4) ☐ Interview Summary (PTO-413) Paper No(s). _____

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other:

U.S. Patent and Trademark Office
PTO-326 (Rev. 04-01)

Office Action Summary

Part of Paper No. 6

DETAILED ACTION

Conclusion

1. This is a final rejection of applicant's earlier Application No. 09/399,908. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rupal D. Dharia whose telephone number is (703) 305-4003. The examiner can normally be reached on M-F 7:00AM-3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoleil can be reached on (703) 305-9713. The fax phone numbers for

Application/Control Number: 09/399,908

Art Unit: 2181

Page 3

the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3600.


Rupal D. Dharia
Primary Examiner
Art Unit 2181

rdd
January 24, 2002

COPY OF PAPERS
ORIGINALLY FILED

Attorney Docket: 1457CPA
Page 1 of 2

2181#

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to the Commissioner for Patents and Trademarks, Washington, D.C. 20231, on April 26, 2002.

Grace Alicea



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the name of:

Date: April 26, 2002

Portman, et al.

Serial No.: 09/399,908

Group Art Unit: 2181

Filing Date: Sept. 21, 1999

Examiner: Dharia, R.

Title: METHOD AND SYSTEM FOR CONTROLLING DATA
IN A COMPUTER SYSTEM

Assistant Commissioner of Patents
Washington, D.C. 20231

RECEIVED

MAY 13 2002

Technology Center 2100

TRANSMITTAL LETTER

Sir:

In response to the Office Action dated January 28, 2002, please find enclosed the following:

- 1) Amendment responsive to the Office Action dated January 28, 2002;
- 2) Transmittal Letter; and
- 3) Postcard.

- 4) The fee for claims has been calculated as shown below:

<u>Large Entity</u> ☐ <u>Small Entity</u> ☒					
Fee Items	Claims remaining after Amendment	Highest number of Claims previously paid for	Present extra Claims	Fee Rate	TOTAL
Total Claims	28	- 20 =	8	x 9.00	\$ 72.00
Independent	8	- 3 =	5	x 42.00	210.00
Multiple Dependent Claim fee (one or more, first added by this amendment)				140.00	0.00
Total Fees					\$ 282.00

A

5) **Extension of Term:** Pursuant to 37 CFR 1.136, Applicant petitions the Commissioner to extend the time for response from _____ to _____.

☐ _____ (X) Month Extension of Time, \$ 0.00 is submitted herewith.

☒ No extension of time is required.

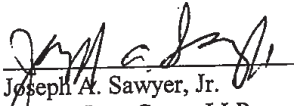
6) **Payment of Fees:**

☒ Check No. 4309 in the amount of \$282.00 is enclosed for payment of excess claim fees.

7) ☒ The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to Deposit Account 02-2120 (Sawyer Law Group).

If any unresolved issues remain, please contact Applicant's attorney at the telephone number indicated below.

Respectfully submitted,


Joseph A. Sawyer, Jr.
Sawyer Law Group LLP
Attorney for Applicant(s)
Reg. No. 30,801
(650) 493-4540

COPIES OF PAPERS
ORIGINALLY FILED

Attorney Docket No: 1457CPA



CERTIFICATE OF MAIL

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to the Assistant for Patents and Trademarks, Washington, D.C. 20231, on April 26, 2002.

Grace Alicea
Grace Alicea

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Date: April 26, 2002

Portman, et al.

Serial No. 09/399,908

Group Art Unit: 2181

Filed: Sept. 21, 1999

Examiner: Dharia, R.

For: METHOD AND SYSTEM FOR CONTROLLING DATA IN A
COMPUTER SYSTEM

RECEIVED

MAY 13 2002

Assistant Commissioner for Patents
Washington, D.C. 20231

Technology Center 210

AMENDMENT

Sir:

In response to the Final Office Action dated January 28, 2002, please amend the above-identified application in the following manner:

IN THE SPECIFICATION:

Please replace the title with: "METHOD AND SYSTEM FOR CONTROLLING DATA IN A
COMPUTER SYSTEM IN THE EVENT OF A POWER FAILURE"

In the Abstract (Page 18, line 2):

A method and system for controlling data in a computer system when the computer system loses power is disclosed. The method and system comprises activating a plurality of super capacitors to supply power to the computing engine based upon power being removed

Q1 from the computer system and reconfiguring the data in the computing engine. Through the use of a system and method, large amounts of newly written and modified data can be stored from the volatile memory to the non-volatile memory in the event of a sudden external system power loss. The system and method allows data to be rapidly and irretrievably erased from the non-volatile memory automatically, in the event of a sudden loss of external power, or manually. This capability consumes minimal space and weight and is implemented in an affordable manner.

IN THE CLAIMS:

Q2 1. (Amended) A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:

- (a) activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;
- (b) reconfiguring the data in the computing engine; and
- (c) deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.

Q3 10. (Amended) A system for controlling data in a computer system when the computer system loses power, the computer system comprising a computer engine, comprising:

- means for activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;
- means for reconfiguring the data in the computing engine; and
- means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.

Please add claims:

19. A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:

- (a) allowing the computer system to be placed in an erase mode;
- (b) activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system; and
- (c) securely erasing data in the computing engine to prevent access to the data each time power is removed from the computing engine and the system is in the erase mode.

20. The method of claim 19 wherein the allowing step (a) further includes the step of:

- (a1) allowing the computer system to be placed in the erase mode or in a save mode.

21. The method of claim 20 further comprising the step of:

- (d) saving the data in the computing engine in a nonvolatile storage in each time power is removed from the computing engine and the system is in the save mode.

22. A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:

- (a) activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;
- (b) placing the computer system in a standby mode based upon power being removed from the computer system;
- (c) providing power to the computer system using the plurality of super capacitors in response to a user interaction after the computer system has entered standby mode; and

- (d) erasing data in the computing engine based upon the user interaction.

23. A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:

- (a) activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;
- (b) reconfiguring the data in the computing engine; and
- (c) ensuring that the plurality of super capacitors is maintained in a desired temperature range.

24. A system for controlling data in a computer system when the computer system loses power, the computer system comprising a computer engine, comprising:

means for activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system; and

means for reconfiguring the data in the computing engine, the reconfiguring means being capable of being placed in an erase mode;

wherein the reconfiguring means further securely erase data in the computing engine to prevent access to the data each time each time power is removed from the computing engine and the system is in the erase mode.

25. The system of claim 24 wherein the reconfiguring means can further be placed in the erase mode or in a save mode.

26. The system of claim 25 wherein the reconfiguring means further save the data in the computing engine in a nonvolatile storage in each time power is removed from the computing engine and the system is in the save mode.

27. A system for controlling data in a computer system when the computer system loses power, the computer system comprising a computer engine, comprising:

means for activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system, for placing the computer system in a standby mode based upon power being removed from the computer system, providing power to the computer system based upon a user interaction after the computer system has entered standby mode;

means for reconfiguring the data in the computing engine, the reconfiguring means further including means for erasing a portion of the data in the computing engine based upon the user interaction.

28. A system for controlling data in a computer system when the computer system loses power, the computer system comprising a computer engine, comprising:

means for activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;

means for reconfiguring the data in the computing engine; and

means for ensuring that the plurality of super capacitors is maintained in a desired temperature range.

REMARKS

Claims 1-18 are pending in the present Application. Applicant has amended claims 1 and 10. Applicant has added claims 19-28. Consequently, claims 1-28 remain pending in the present Application.

Applicant has amended claims 1 and 10 to recite that the super capacitors are deactivated when their charge reach a predetermined level. Support for the amendments to claims 1 and 10 can be found in the specification, page 9, line 23-page 10, line 3. Support for new claims 19-21 and 24-26 can be found in the specification, page 8, lines 1-6 and page 11, lines 3-10. Support for new claims 22 and 27 can be found in the specification, page 12, lines 11-19. Support for new claims 23 and 28 can be found in the specification, page 6, lines 8-16. Accordingly, Applicant respectfully submits that no new matter is added.

In the above-identified Office Action, the Examiner objected to portions of the present application and rejected the claims for the same reasons as in a previous Office Action in the parent case ("previous Office Action") dated June 15, 2001. In the previous Office Action, the Examiner objected to the Abstract and the title. Applicant has amended the Abstract in accordance with the Examiner's suggestion. In addition, Applicant has changed the title to: METHOD AND SYSTEM FOR CONTROLLING DATA IN A COMPUTER SYSTEM IN THE EVENT OF A POWER FAILURE, which Applicant believes is descriptive of the present invention as recited in varying scope in claims 1-26. Accordingly, Applicant respectfully submits that the Examiner's objection to the specification and the title has been overcome.

In the previous Office Action, the Examiner also rejected claims 1-4, 6, 7, 10-13, 15 and 16 under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 5,542,042 ("Manson"). The Examiner also rejection claims 5, 8, 9, 14, 17 and 18 under 35 U.S.C. § 103 as being obvious in light of Manson in view of U.S. Patent No. 5,768,208 ("Bruwer").

The Examiner has rejected claims 1-4, 6, 7, 10-13, 15 and 16 as being anticipated by Manson. The Examiner indicated that Manson transferring data from volatile to nonvolatile memory, and erasing the volatile memory.

Applicant respectfully traverses the Examiner's rejection. Claim 1 recites a method for controlling data in a computer system, which includes a computing system, when the computer system loses power. Claim 1 recites the steps of activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system and reconfiguring the data in the computing engine. Claim 1 further recites the step of deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level. Claim 10 recites an analogous system that includes means for performing the steps recited in claim 1.

Because the method and system of claims 1 and 10, respectively, teach that power is cut off to the computing engine when the super capacitors reach a predetermined level, performance and reliability of the computer system are improved. The predetermined level can be set above the minimum operating voltage of the computer system, preventing the computer system from running with unpredictable results. Specification, page 12, lines 5-8. Furthermore, the predetermined level can be set above a zero level of power for the computer system. When the super capacitors are not fully discharged, it may take only a few seconds to recharge the super capacitors, rather than several minutes, rapidly providing protection against power loss. Specification, page 12, lines 8-10.

Claims 1 and 10 are neither taught nor suggested by Manson. Similarly, claims 1 and 10 are neither taught nor suggested by Manson in view of Bruwer.

In contrast to the present invention as recited in varying scope in claims 1 and 10, Manson fails to teach or suggest the combination of elements recited in claims 1 and 10

including deactivating the super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level. Manson teaches a system which stores "critical" data upon a power loss. In particular, when a power loss is detected, the "critical" data is copied to an accumulator, then complemented. Manson, col. 3, lines 24-40. The complemented data is thus stored. Upon power on reset of the computer system, the complemented data is checked. Manson, col. 2, lines 29-30, 46-55. If the comparison indicates that the complemented data matches data generated after power is turned back on, then operation continues. However, if the comparison indicates that there was a memory loss during the power outage, then the memory is initialized. Manson, col. 2, lines 55-61.

Bruwer describes a system that is used to provide fail safe non-volatile memory programming, even in the event of a power loss. Bruwer, Abstract. Bruwer teaches that "soft writes" are a problem. Bruwer, col. 1, lines 23-28. A soft write occurs when an attempt is made to change the state of information in a cell of the memory, but the attempt is not completed due to some type of interrupt, such as a power failure. Bruwer, col. 1, lines 19-23. Bruwer also teaches that a standard write operation first erases a cell by writing a one, then changes the value in the cell from a 1 to a zero or leaves the cell unchanged, depending upon the desired data for the cell. Bruwer, col. 1, lines 29-34. The system of Bruwer determines whether sufficient charge exists in a bank of capacitors to program a non-volatile memory. Bruwer, col. 4, lines 51-60. If not, then the system of Bruwer does not operate upon a power loss. Bruwer, col. 4, lines 60-67. If the capacitors have sufficient charge, Bruwer completes a programming cycle interrupted by a power loss. Bruwer, col. 4, line 67-col. 5, line 4.

Although both Manson and Bruwer discuss operations performed in the event of a power failure, Applicant can find no mention in either Manson or Bruwer of any mechanism for cutting off power supplied by the capacitors. More specifically, Manson and Bruwer are devoid of

mention of deactivating super capacitors when the super capacitors are discharged to a predetermined level to cut power off to the computer system. Any combination of Manson and Bruwer, therefore, would not deactivate super capacitors when the super capacitors are discharged to a predetermined level to cut off power to the computer system. Consequently, Manson and Bruwer, separately or in combination, cannot teach or suggest the method and system recited in claims 1 and 10, respectively. Accordingly, Applicant respectfully submits that claims 1 and 10 are allowable over the cited references.

Claim 2-4, 6, and 7 depend upon independent claim 1. Similarly, claims 11-13, 15 and 16 depend upon independent claim 10. Consequently, the arguments herein apply with full force to claims 2-4, 6, 7, 11-13, 15 and 16. Accordingly, Applicant respectfully submits that claims 2-4, 6, 7, 11-13, 15 and 16 are allowable over cited references.

The Examiner also rejected claims 5, 8, 9, 14, 17 and 18 under 35 U.S.C. § 103 as being obvious in light of Manson in view of Bruwer. The Examiner cited Bruwer as teaching that it is known to erase a non-volatile memory and that one of ordinary skill in the art would have incorporated the teachings of Bruwer in the system of Manson to prevent the "soft writes" described by Bruwer.

Claims 5, 8 and 9 depend on independent claim 1. Claims 14, 17 and 18 depend on independent claim 10. Consequently, the arguments herein apply with full force to claims 2, 5-11, and 13-17. Accordingly, Applicant respectfully submits that claims 2-5, and 13-17 are also allowable over the cited references.

New claims 19 and 24 recite a method and system, respectively, for controlling data in a computer system when the computer system loses power. The method recited in claim 19 allows a user to place the computer system in an erase mode and activates a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer

system. The method recited in claim 19 also securely erases data in the computing engine to prevent access to the data each time power is removed from the computing engine and the system is in erase mode. Claim 23 recites a system analogous to the method recited in claim 19. The method and system recited in claims 19 and 23, respectively, securely erase data to prevent access to the data in response to power being removed from the computing engine. As a result, it can be ensured that sensitive data on the computer system cannot be accessed after power is removed from the computer system.

In contrast, neither Manson nor Bruwer, separately or in combination, teach or suggest the combination of elements in claims 19 and 23 including erasing data each time power is removed from the computer system and the computer system is in the erase mode. As described above, Manson teaches that "critical" data are saved in the event that power is removed from the computer system. It is only upon power on reset of the computer system that data might be erased only if a comparison indicates that there was a memory loss during the power outage. Manson, col. 2, lines 55-61. Applicant can find no mention in Manson of erasing data for any other reason. More specifically, Applicant can find no mention in Manson of erasing data in response to power being removed from the computer system and the computer system being in an erase mode. Manson also fails to mention an erase mode. Consequently, Manson cannot teach or suggest the method and system recited in claims 19 and 23, respectively.

Similarly, Bruwer teaches that a programming cycle is completed upon a power loss. In order to do so, data may be erased as part of the programming cycle if the data had not been erased prior to the power loss. Thus, data would only be erased if the programming cycle had not completed the erasing data in the computer system. Consequently, Bruwer would not erase data each time the computer system loses power and the computer system is in an erase mode. Furthermore, Bruwer fails to mention the existence of an erase mode in the computer system.

Consequently, Bruwer also fails to teach or suggest erasing data each time power is removed from a computer system and the computer system is in erase mode.

Neither Manson nor Bruwer discusses an erase mode or erasing data each time power is removed from a computer system and the computer system is in erase mode. As a result, any combination of Manson and Bruwer cannot teach or suggest this feature. Accordingly, claims 19 and 23 are allowable over the cited references.

Claims 20-21 and 25-26 depend upon claims 19 and 24, respectively. Therefore, the arguments herein apply with full force to claims 20-21 and 25-26. Accordingly, Applicant respectfully submits that claims 20-21 and 25-26 are allowable over the cited references. Furthermore, Applicant can find no mention in either Manson or Bruwer of having both a save mode and an erase mode available on the computer system. Manson and Bruwer also fail to discuss any mechanism for saving data in nonvolatile storage in the save mode, while erasing data in the computing engine in the erase mode. Thus, Manson and Bruwer, separately or in combination, cannot teach or suggest the method and system recited in claims 20-21 and 25-26, respectively. Accordingly, Applicant respectfully submits that claims 20-21 and 25-26 are each separately allowable over the cited references.

New claims 22 and 27 recite a method and system, respectively, for controlling data in a computer system when the computer system loses power. The computer system includes a computing engine. The method recited in claim 22 includes the steps of activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system and placing the computer system in a standby mode based upon power being removed from the computer system. The method recited in claim 22 also includes the steps of providing power to the computer system using the plurality of super capacitors in response to a user interaction after the computer system has entered standby mode and erasing data in the

computing engine based upon the user interaction. Claim 27 recites an analogous system. Thus, using the method and system recited in claims 22 and 27, respectively, a user can select to erase data while the computer system is disconnected from a power.

In contrast, both Manson and Bruwer describe providing power to the computer system to keep the computer system operating and performing functions with computer system after power is removed. Neither Manson nor Bruwer describe placing the computer system in a standby mode based upon power being removed from the computer system. Neither Manson nor Bruwer describe providing power to the computer system using super capacitors in response to a user interaction after the computer system has entered standby mode. Furthermore, both Manson and Bruwer fail to mention erasing data in the computing engine based upon the user interaction. Consequently, any combination of Manson and Bruwer cannot teach or suggest placing the computer system in a standby mode based upon power being removed from the computer system, providing power to the computer system using the super capacitors in response to a user interaction after the computer system has entered standby mode and erasing data in the computing engine based upon the user interaction. Manson and Bruwer, separately or in combination, thus cannot teach or suggest the method and system recited in claims 22 and 27. Accordingly, Applicant respectfully submits that claims 22 and 27 are allowable over the cited references.

New claims 23 and 28 recite a method and system for controlling data in a computer system when the computer system loses power. The computer system includes a computing engine. The method recited in claim 23 includes the steps of activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system and reconfiguring the data in the computing engine. The method recited in claim 23 also includes the step of ensuring that the plurality of super capacitors is maintained in

a desired temperature range. Claim 28 recites an analogous system. As a result, the super capacitors can be maintained in their operating temperature range, ensuring their ability to provide power to the computer system in the event of power being removed from the computer system.

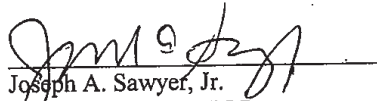
In contrast, Applicant can find no mention in either Bruwer or Manson of any mechanism for ensuring that the capacitors used to provide power to the computer system are maintained in a particular temperature range. Consequently, any combination of Manson and Bruwer would also fail to teach or suggest this feature. Manson and Bruwer, separately or in combination, therefore, cannot teach or suggest the method and system recited in claims 23 and 28. Accordingly, Applicant respectfully submits that claims 23 and 28 are allowable over the cited references.

Accordingly, for the above-mentioned reasons, Applicant respectfully submits that the claims are allowable over the cited reference. Consequently, Applicant respectfully requests reconsideration and allowance of the claims as currently presented.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "Version with markings to show changes made".

Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issue remain, the Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,


Joseph A. Sawyer, Jr.
Sawyer Law Group LLP
Attorney for Applicant(s)
Reg. No. 30,801
(650) 493-4540

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Please replace the title with: "METHOD AND SYSTEM FOR CONTROLLING DATA IN A COMPUTER SYSTEM IN THE EVENT OF A POWER FAILURE"

In the Abstract (Page 18, line 2):

[The present invention discloses] A method and system for controlling data in a computer system when the computer system loses power[, the computer system comprising a computing engine] is disclosed. The method and system comprises activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system and reconfiguring the data in the computing engine. Through the use of a system and method[in accordance with the present invention, a user is able to correctly store], large amounts of newly written and modified data can be stored from the volatile memory to the non-volatile memory in the event of a sudden external system power loss. [Furthermore, the user of a]The system and method [in accordance with the present invention will be able to]allows data to be rapidly and irretrievably erased [data]from the non-volatile memory automatically, in the event of a sudden loss of external power, or manually. This capability consumes minimal space and weight and is implemented in an affordable manner.

IN THE CLAIMS:

1. (Amended) A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:
 - (a) activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system; [and]

- (b) reconfiguring the data in the computing engine; and
- (c) deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.

10. (Amended) A system for controlling data in a computer system when the computer system loses power, the computer system comprising a computer engine, comprising:
means for activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system; [and]
means for reconfiguring the data in the computing engine; and
means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.

Please add claims:

19. A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:

- (a) allowing the computer system to be placed in an erase mode;
- (b) activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system; and
- (c) securely erasing data in the computing engine to prevent access to the data each time power is removed from the computing engine and the system is in the erase mode.

20. The method of claim 19 wherein the allowing step (a) further includes the step of:
(a1) allowing the computer system to be placed in the erase mode or in a save mode.

21. The method of claim 20 further comprising the step of:
- (d) saving the data in the computing engine in a nonvolatile storage in each time power is removed from the computing engine and the system is in the save mode.
22. A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:
- (a) activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;
- (b) placing the computer system in a standby mode based upon power being removed from the computer system;
- (c) providing power to the computer system using the plurality of super capacitors in response to a user interaction after the computer system has entered standby mode; and
- (d) erasing data in the computing engine based upon the user interaction.
23. A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:
- (a) activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;
- (b) reconfiguring the data in the computing engine; and
- (c) ensuring that the plurality of super capacitors is maintained in a desired temperature range.
24. A system for controlling data in a computer system when the computer system loses power, the computer system comprising a computer engine, comprising:

means for activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system; and

means for reconfiguring the data in the computing engine, the reconfiguring means being capable of being placed in an erase mode;

wherein the reconfiguring means further securely erase data in the computing engine to prevent access to the data each time each time power is removed from the computing engine and the system is in the erase mode.

25. The system of claim 24 wherein the reconfiguring means can further be placed in the erase mode or in a save mode.

26. The system of claim 25 wherein the reconfiguring means further save the data in the computing engine in a nonvolatile storage in each time power is removed from the computing engine and the system is in the save mode.

27. A system for controlling data in a computer system when the computer system loses power, the computer system comprising a computer engine, comprising:

means for activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system, for placing the computer system in a standby mode based upon power being removed from the computer system, providing power to the computer system based upon a user interaction after the computer system has entered standby mode;

means for reconfiguring the data in the computing engine, the reconfiguring means further including means for erasing a portion of the data in the computing engine based upon the user interaction.

28. A system for controlling data in a computer system when the computer system loses power, the computer system comprising a computer engine, comprising:

means for activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;

means for reconfiguring the data in the computing engine; and

means for ensuring that the plurality of super capacitors is maintained in a desired temperature range.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/399,908	09/21/1999	ROLAND F. PORTMAN	1457P	2827

7590 05/17/2002
JOSEPH A SAWYER JR
SAWYER AND ASSOCIATES
POST OFFICE BOX 51418
PALO ALTO, CA 94303

EXAMINER	
DHARIA, RUPAL	
ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 05/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No. 09/399,908	Applicant(s) PORTMAN ET AL.	
	Examiner Rupal D. Dharja	Art Unit 2181	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 08 May 2002 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☐ The period for reply expires _____ months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☒ The proposed amendment(s) will not be entered because:

(a) ☒ they raise new issues that would require further consideration and/or search (see NOTE below);

(b) ☐ they raise the issue of new matter (see Note below);

(c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

(d) ☒ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: The newly added limitations would require further consideration and/or search.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☐ The a) ☐ affidavit, b) ☐ exhibit, or c) ☐ request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☒ For purposes of Appeal, the proposed amendment(s) a) ☒ will not be entered or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: _____.

Claim(s) objected to: _____.

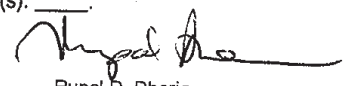
Claim(s) rejected: 1-18.

Claim(s) withdrawn from consideration: _____.

8. ☐ The proposed drawing correction filed on _____ is a) ☐ approved or b) ☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____.

10. ☐ Other: _____


 Rupal D. Dharja
 Primary Examiner
 Art Unit: 2181

COPY OF PAPERS
ORIGINAL ED

PTO/SB/30 (10-01)

Approved for use through 10/31/2002, OMB 0651-0031
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REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL	
 Address to: Commissioner for Patents Box RCE Washington DC 20231	Application Number
	Filing Date
	First Named Inventor
	Art Unit
	Examiner Name

09/399,906
09/27/1999
PORTMAN, et al.
2181
Dharla, Rupal
Attorney Docket Number
1457CPA

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. **Submission required under 37 CFR 1.114**

a. ☒ Previously submitted

i. ☒ Consider the amendment(s)/reply under 37 CFR 1.116 previously filed on **April 26, 2002**.
(Any unentered amendment(s) referred to above will be entered).

ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

iii. ☐ Other _____

b. ☐ Enclosed

i. ☐ Amendment/Reply

ii. ☐ Affidavit(s)/Declaration(s)

iii. ☐ Information Disclosure Statement (IDS)

iv. ☐ Other _____

2. **Miscellaneous**

a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

b. ☐ Other _____

3. **Fees** The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

a. ☐ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. _____

i. ☐ RCE fee required under 37 CFR 1.17(e)

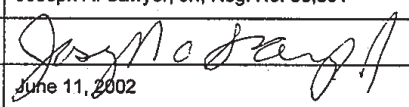
ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)

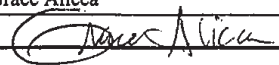
iii. ☐ Other _____

b. ☒ Check No. **4759** in the amount of **\$370.00** enclosed

c. ☐ Payment by credit card (Form PTO-2038 enclosed)

06/25/2002 AMONDAF1 00000104 09399908
01 FC:279 370.00 DP

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Attorney Name	Joseph A. Sawyer, Jr., Reg. No: 30,801
Signature	
Date	June 11, 2002

CERTIFICATE OF MAILING	
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231 on this date: June 11, 2002 .	
Type or printed name	Grace Alicea
Signature	

pa

Notice of Allowability	Application No.	Applicant(s)	
	09/399,908	PORTMAN ET AL.	
	Examiner	Art Unit	
	Rupal D. Dharla	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment filed 5/8/2002.
2. ☒ The allowed claim(s) is/are 1-28.
3. ☒ The drawings filed on 21 September 1999 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.
5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 - (a) ☐ The translation of the foreign language provisional application has been received.
6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
8. ☐ CORRECTED DRAWINGS must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No. _____.
 - (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
 - (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the top margin (not the back) of each sheet. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.
9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1 ☐ Notice of References Cited (PTO-892) 3 ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5 ☐ Information Disclosure Statements (PTO-1449), Paper No. _____ 7 ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	2 ☐ Notice of Informal Patent Application (PTO-152) 4 ☐ Interview Summary (PTO-413), Paper No. _____ 6 ☐ Examiner's Amendment/Comment 8 ☐ Examiner's Statement of Reasons for Allowance 9 ☐ Other
---	--

Rupal D. Dharla
 Primary Examiner
 Art Unit: 2181

09/399,908

NOTICE OF DRAFTSPERSON'S
PATENT DRAWING REVIEWThe drawing(s) filed (insert date) 9-21-99 are:A. ☒ approved by the Draftsperson under 37 CFR 1.84 or 1.152.B. ☐ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 for the reasons indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawing must be submitted according to the instructions on the back of this notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings: Black ink. Color: _____ Color drawings are not acceptable until petition is granted. Fig(s) _____ Pencil and non black ink not permitted. Fig(s) _____ 2. PHOTOGRAPHS. 37 CFR 1.84(b) 1 full-tone set is required. Fig(s) _____ Photographs not properly mounted (must use bryistol board or photographic double-weight paper). Fig(s) _____ Poor quality (half-tone). Fig(s) _____ 3. TYPE OF PAPER. 37 CFR 1.84(e) Paper not flexible, strong, white, and durable. Fig(s) _____ Erasures, alterations, overwritings, interlineations, folds, copy machine marks not accepted. Fig(s) _____ Mylar, velum paper is not acceptable (too thin). Fig(s) _____ 4. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable sizes: 21.0 cm by 29.7 cm (DIN size A4) 21.6 cm by 27.9 cm (8 1/2 x 11 inches) All drawing sheets not the same size. Sheet(s) _____ Drawings sheets not an acceptable size. Fig(s) _____ 5. MARGINS. 37 CFR 1.84(g): Acceptable margins: Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm SIZE: A4 Size Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm SIZE: 8 1/2 x 11 Margins not acceptable. Fig(s) _____ Top (T) _____ Left (L) Right (R) _____ Bottom (B) 6. VIEWS. 37 CFR 1.84(h) REMINDER: Specification may require revision to correspond to drawing changes. Partial views. 37 CFR 1.84(h)(2) Brackets needed to show figure as one entity. Fig(s) _____ Views not labeled separately or properly. Fig(s) _____ Enlarged view not labeled separately or properly. Fig(s) _____ 7. SECTIONAL VIEWS. 37 CFR 1.84 (h)(3) Hatching not indicated for sectional portions of an object. Fig(s) _____ Sectional designation should be noted with Arabic or Roman numbers. Fig(s) _____	8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i) Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s) _____ 9. SCALE. 37 CFR 1.84(k) Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction. Fig(s) _____ 10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(j) Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (poor line quality). Fig(s) _____ 11. SHADING. 37 CFR 1.84(m) Solid black areas pale. Fig(s) _____ Solid black shading not permitted. Fig(s) _____ Shade lines; pale, rough and blurred. Fig(s) _____ 12. NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.84(p) Numbers and reference characters not plain and legible. Fig(s) _____ Figure legends are poor. Fig(s) _____ Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(1) Fig(s) _____ English alphabet not used. 37 CFR 1.84(p)(2) Fig(s) _____ Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3) Fig(s) _____ 13. LEAD LINES. 37 CFR 1.84(q) Lead lines cross each other. Fig(s) _____ Lead lines missing. Fig(s) _____ 14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t) Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Sheet(s) _____ 15. NUMBERING OF VIEWS. 37 CFR 1.84(u) Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s) _____ 16. CORRECTIONS. 37 CFR 1.84(w) Corrections not made from prior PTO-948 dated _____ 17. DESIGN DRAWINGS. 37 CFR 1.152 Surface shading shown not appropriate. Fig(s) _____ Solid black shading not used for color contrast. Fig(s) _____
COMMENTS	

REVIEWER

DATE

11-19-99

TELEPHONE NO.

ATTACHMENT TO PAPER NO.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities--37 CFR 1.85

File new drawings with the changes incorporated therein. The application number or the title of the invention, inventor's name, docket number (if any), and the name and telephone number of a person to call if the Office is unable to match the drawings to the proper application, should be placed on the back of each sheet of drawings in accordance with 37 CFR 1.84(c). Applicant may delay filing of the new drawings until receipt of the Notice of Allowability (PTOL-37). Extensions of time may be obtained under the provisions of 37 CFR 1.136. The drawing should be filed as a separate paper with a transmittal letter addressed to the Drawing Processing Branch.

2. Timing for Corrections

Applicant is required to submit **acceptable** corrected drawings within the three-month shortened statutory period set in the Notice of Allowability (PTOL-37). If a correction is determined to be unacceptable by the Office, applicant must arrange to have acceptable corrections resubmitted within the original three-month period to avoid the necessity of obtaining an extension of time and paying the extension fee. Therefore, applicant should file corrected drawings as soon as possible.

Failure to take corrective action within set (or extended) period will result in **ABANDONMENT** of the Application.

3. Corrections other than Informalities Noted by the Drawing Review Branch on the Form PTO-948

All changes to the drawings, other than informalities noted by the Drawing Review Branch, **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.



UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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Washington, D.C. 20231
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NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 07/24/2002

JOSEPH A SAWYER JR
SAWYER AND ASSOCIATES
POST OFFICE BOX 51418
PALO ALTO, CA 94303

EXAMINER

DHARIA, RUPAL

ART UNIT

CLASS-SUBCLASS

2181

713-340000

DATE MAILED: 07/24/2002

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/399,908	09/21/1999	ROLAND F. PORTMAN	1457P	2827

TITLE OF INVENTION: METHOD AND SYSTEM FOR CONTROLLING DATA IN A COMPUTER SYSTEM IN THE EVENT OF A POWER FAILURE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$640	\$300	\$940	10/24/2002

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. **PROSECUTION ON THE MERITS IS CLOSED.** THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN **THREE MONTHS** FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. **THIS STATUTORY PERIOD CANNOT BE EXTENDED.** SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above. If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is changed, pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above and notify the United States Patent and Trademark Office of the change in status, or

B. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check the box below and enclose the PUBLICATION FEE and 1/2 the ISSUE FEE shown above.

☐ Applicant claims SMALL ENTITY status.
See 37 CFR 1.27.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Box ISSUE FEE
Commissioner for Patents
Washington, D.C. 20231
Fax (703)746-4000

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)
7590 07/24/2002

JOSEPH A SAWYER JR
SAWYER AND ASSOCIATES
POST OFFICE BOX 51418
PALO ALTO, CA 94303

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above, or being facsimile transmitted to the USPTO, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/399,908	09/21/1999	ROLAND F. PORTMAN	1457P	2827

TITLE OF INVENTION: METHOD AND SYSTEM FOR CONTROLLING DATA IN A COMPUTER SYSTEM IN THE EVENT OF A POWER FAILURE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$640	\$300	\$940	10/24/2002

EXAMINER	ART UNIT	CLASS-SUBCLASS
DHARIA, RUPAL	2181	713-340000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent)

☐ individual ☐ corporation or other private group entity ☐ government

4a. The following fee(s) are enclosed:

4b. Payment of Fee(s):

- ☐ Issue Fee
☐ Publication Fee
☐ Advance Order - # of Copies _____

- ☐ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Commissioner is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

Commissioner for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature)

(Date)

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/399,908	09/21/1999	ROLAND F. PORTMAN	1457P	2827
7590 07/24/2002			EXAMINER	
JOSEPH A SAWYER JR SAWYER AND ASSOCIATES POST OFFICE BOX 51418 PALO ALTO, CA 94303			DHARIA, RUPAL	
			ART UNIT	PAPER NUMBER
			2181	

DATE MAILED: 07/24/2002

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The patent term adjustment to date is 0 days. If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the term adjustment will be 0 days.

If a continued prosecution application (CPA) was filed in the above-identified application, the filing date that determines patent term adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) system. (<http://pair.uspto.gov>)



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/399,908	09/21/1999	ROLAND F. PORTMAN	1457P	2827
EXAMINER				
DHARIA, RUPAL				
ART UNIT		PAPER NUMBER		
2181				

DATE MAILED: 07/24/2002

Notice of Fee Increase on October 1, 2002

If a reply to a "Notice of Allowance and Fee(s) Due" is filed in the Office on or after October 1, 2002, then the amount due may be higher than that set forth in the "Notice of Allowance and Fee(s) Due" since there will be an increase in fees effective on October 1, 2002. See Revision of Patent and Trademark Fees for Fiscal Year 2003: Notice of Proposed Rulemaking, 67 Fed. Reg. 30634, 30636 (May 7, 2002). Although a change to the amount of the publication fee is not currently proposed for October 2002, if the issue fee or publication fee is to be paid on or after October 1, 2002, applicant should check the USPTO web site for the current fees before submitting the payment. The USPTO Internet address for the fee schedule is: <http://www.uspto.gov/main/howtofees.htm>.

If the issue fee paid is the amount shown on the "Notice of Allowance and Fee(s) Due," but not the correct amount in view of the fee increase, a "Notice to Pay Balance of Issue Fee" will be mailed to applicant. In order to avoid processing delays associated with mailing of a "Notice to Pay Balance of Issue Fee," if the response to the Notice of Allowance and Fee(s) due form is to be filed on or after October 1, 2002 (or mailed with a certificate of mailing on or after October 1, 2002), the issue fee paid should be the fee that is required at the time the fee is paid. If the issue fee was previously paid, and the response to the "Notice of Allowance and Fee(s) Due" includes a request to apply a previously-paid issue fee to the issue fee now due, then the difference between the issue fee amount at the time the response is filed and the previously paid issue fee should be paid. See Manual of Patent Examining Procedure, Section 1308.01 (Eighth Edition, August 2001).

Effective October 1, 2002, 37 CFR 1.18 is proposed to be revised to change the patent issue fees as set forth below. As stated above, the final fees may be a different amount, and applicant should check the web site given above when paying the fee.

(a) Issue fee for issuing each original or reissue patent, except a design or plant patent:

By a small entity (Sec. 1.27(a))--\$655.00
By other than a small entity--\$1,310.00

(b) Issue fee for issuing a design patent:

By a small entity (Sec. 1.27(a))--\$235.00
By other than a small entity--\$470.00

(c) Issue fee for issuing a plant patent:

By a small entity (Sec. 1.27(a))--\$315.00
By other than a small entity--\$630.00

Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

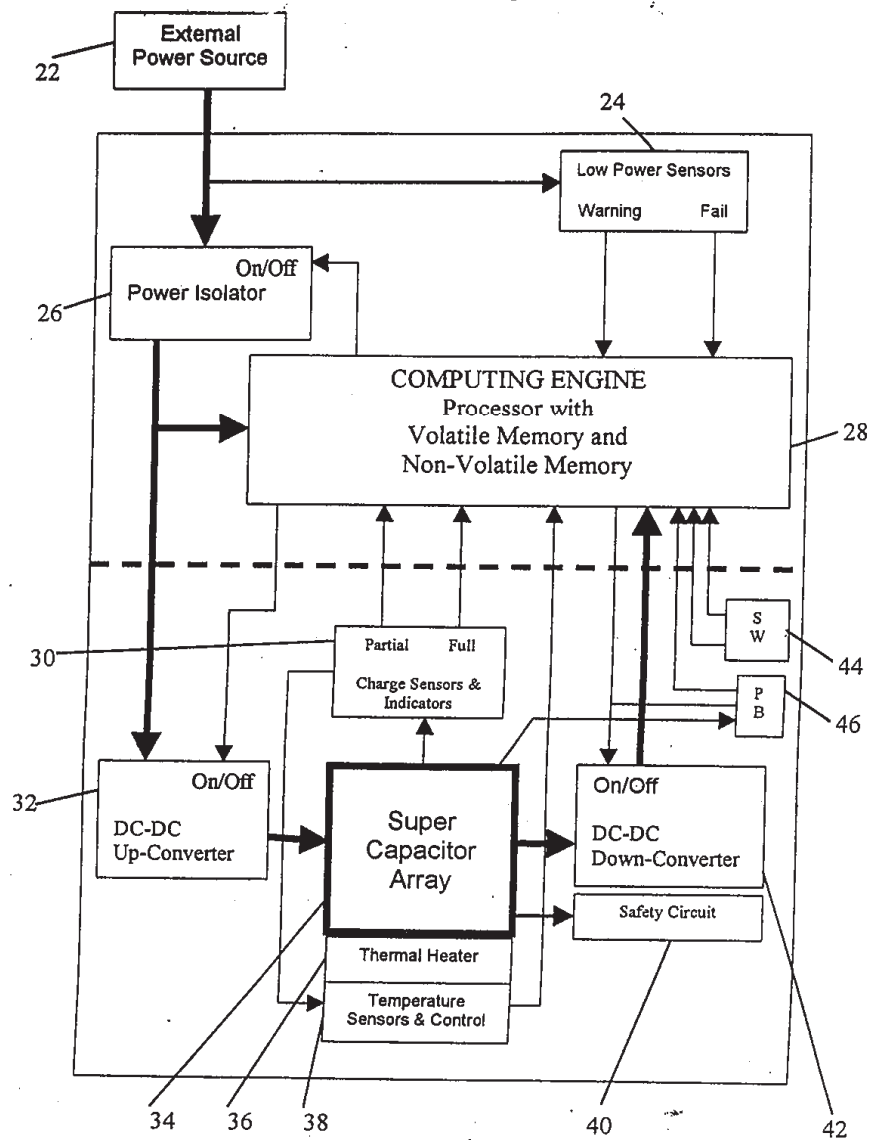
Page 4 of 4

PTOL-85 (REV. 04-02) Approved for use through 01/31/2004.

APPROVED	O.G. FIG. 1	
BY	CLASS	SUBCLASS
DRAFTSMAN	713	340

6496939

6496939-2066660



20

FIGURE 1

APPROVED	O.G. FIG. 1	
BY	CLASS	SUBCLASS
DRAFTSMAN	713	340

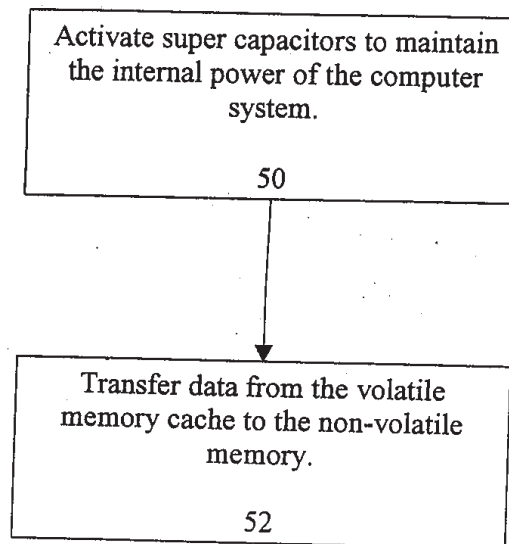


FIGURE 2

APPROVED	O.G. FIG. 1	
BY	CLASS	SUBCLASS
DRAFTSMAN	713	340

0930908-09199

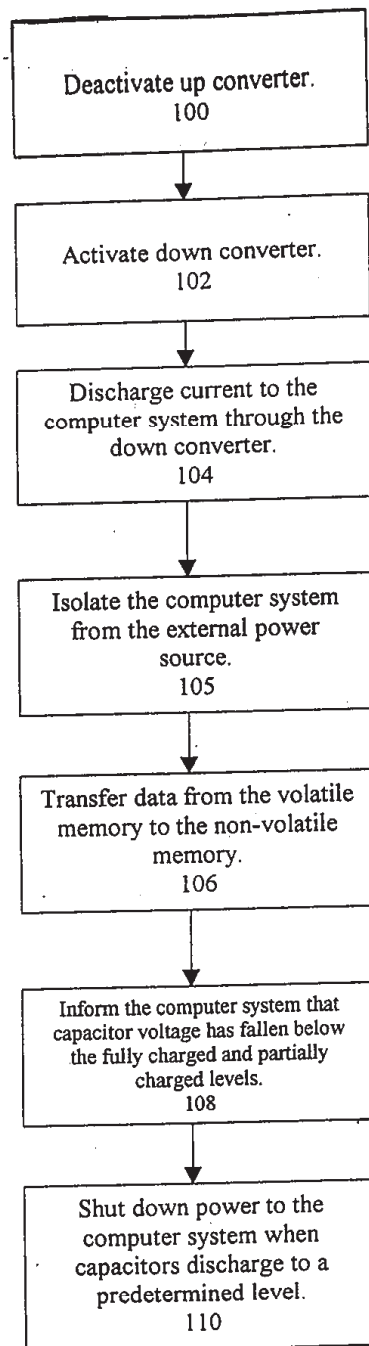


FIGURE 3

APPROVED	D.G. FIG. 1	
BY	CLASS	SUBCLASS
DRAFTSMAN	713	340

66T250-8055550

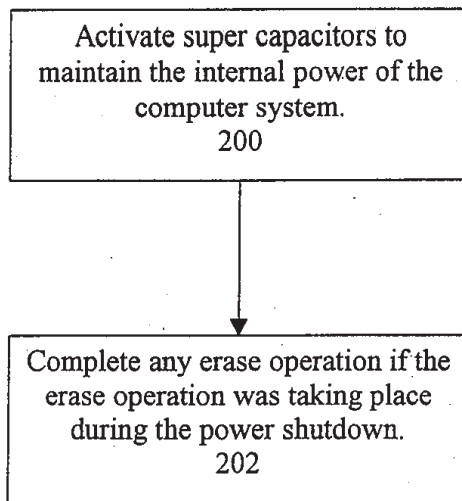


FIGURE 4

APPROVED	O.O. FIG. 1	
BY	CLASS	SUBCLASS
DRAFTSMAN	713	340

09190808-26165

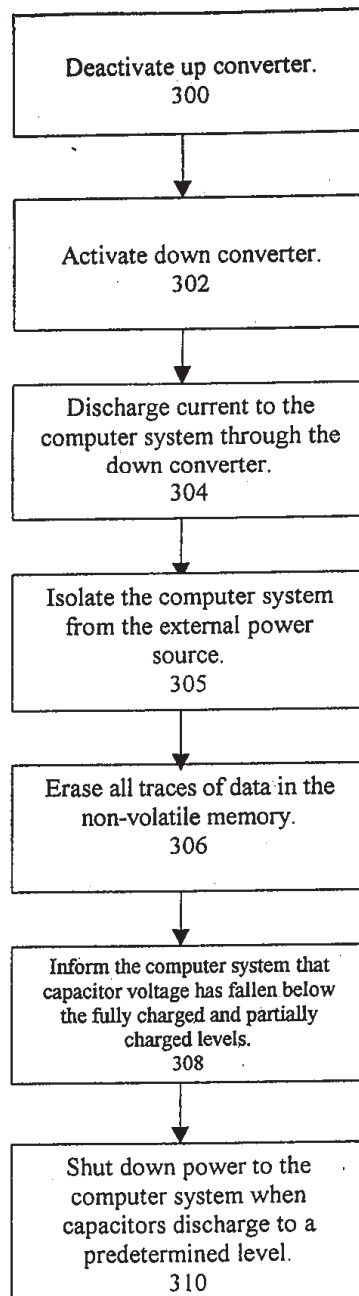


FIGURE 5



PART B - FEE(S) TRANSMITTAL

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Commissioner for Patents
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Fax (703)746-4000

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CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

7590

01/24/2002

JOSEPH A SAWYER JR
SAWYER AND ASSOCIATES
POST OFFICE BOX 51418
PALO ALTO, CA 94303

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Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above, or being facsimile transmitted to the USPTO, on the date indicated below.

Grace Alicea (Depositor's name)
Grace Alicea (Signature)
October 23, 2002 (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/399,908	09/21/1999	ROLAND F. PORTMAN	1457P	2827

TITLE OF INVENTION: METHOD AND SYSTEM FOR CONTROLLING DATA IN A COMPUTER SYSTEM IN THE EVENT OF A POWER FAILURE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$640	\$300	\$940	10/24/2002

EXAMINER	ART UNIT	CLASS-SUBCLASS
DHARIA, RUPAL	2181	713-340000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.563).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. Sawyer Law Group LLP

2. _____

3. _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY AND STATE OR COUNTRY)

Bit Microsystems, Inc.

Fremont, California

Please check the appropriate assignee category or categories (will not be printed on the patent)

☐ Individual ☒ corporation or other private group entity ☐ government

4a. The following fee(s) are enclosed:

4b. Payment of Fee(s):

☒ Issue Fee

☒ A check in the amount of the fee(s) is enclosed.

☒ Publication Fee

☐ Payment by credit card. Form PTO-2038 is attached.

☒ Advance Order - # of Copies 5

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Commissioner for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature)

(Date)

10-23-02

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

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10/30/2002 MBIZUNEZ 00000244 09399908

01 FC:1504

300.00 OP

02 FC:2501

640.00 OP

03 FC:8001

15.00 OP

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PTOL-85 (REV. 04-02) Approved for use through 01/31/2004. OMB 0651-0033

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

2

POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION	T.D.		9/28/95
O.I.P.E. CLASSIFIER		48	10/5/99
FORMALITY REVIEW		70008	10-14-09

INDEX OF CLAIMS

✓ Rejected N Non-elected
 = ... Allowed I Interference
 - (Through numeral)... Canceled A Appeal
 ÷ Restricted O Objected

Claim	Final	Original	Date
1	✓	✓	
2	✓	✓	
3	✓	✓	
4	✓	✓	
5	✓	✓	
6	✓	✓	
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10	✓	✓	
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Claim	Final	Original	Date
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If more than 150 claims or 10 actions
staple additional sheet here

(LEFT INSIDE)

SEARCHED

Class	Sub.	Date	Exmr.
713	300-340	6/13/01	PAD
714	2 14 22		
update above		7/24/02	PAD

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.
713	300-340	7/24/02	PAD
714	2 14 22		

SEARCH NOTES (INCLUDING SEARCH STRATEGY)

	Date	Exmr.
EAST	6/13/01	PAD
EAST update	7/24/02	PAD

PATENT APPLICATION FEE DETERMINATION RECORD Effective November 10, 1998

Application or Docket Number

09/399908

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE		
TOTAL CLAIMS	18 minus 20 = *	
INDEPENDENT CLAIMS	2 minus 3 = *	
MULTIPLE DEPENDENT CLAIM PRESENT		

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	* 18	Minus ** 20	=
Independent	* 2	Minus *** 3	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM			

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SMALL ENTITY TYPE ☒ OR

OTHER THAN SMALL ENTITY

RATE	FEE
	380.00
X\$ 9=	
X39=	
+130=	
TOTAL	380

OR

RATE	FEE
	760.00
X\$18=	
X78=	
+260=	
TOTAL	

SMALL ENTITY OR

OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE
X\$ 9=	
X39=	
+130=	
TOTAL ADDIT. FEE	380

OR

RATE	ADDITIONAL FEE
X\$18=	
X78=	
+260=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$ 9=	
X39=	
+130=	
TOTAL ADDIT. FEE	

OR

RATE	ADDITIONAL FEE
X\$18=	
X78=	
+260=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$ 9=	
X39=	
+130=	
TOTAL ADDIT. FEE	

OR

RATE	ADDITIONAL FEE
X\$18=	
X78=	
+260=	
TOTAL ADDIT. FEE	

PATENT APPLICATION



09399908

U.S. PTO

09/399908

09/12/99

INITIALS 10/5/99 12

CONTENTS

Date received
(Incl. C. of M.)
or
Date Mailed

Date received
(Incl. C. of M.)
or
Date Mailed

1. Application 5 pgs papers.
2. IDS
3. rej 3 mos.
4. Extraj time
5. CPA
6. 1-28-02 Trial Rejection (GNE)
7. Amot A
8. 5/11/02 advisory action
9. Request for RCE
10. Notice of allowability

2/12/01
6-15-01
12-17-01
12-17-01
1-28-02
5/8/02
5/17/02
6-24-02
7-24-02

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