

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KIOXIA AMERICA, INC. and KIOXIA CORPORATION,

Petitioners,

v.

BITMICRO LLC, LLC,

Patent Owner.

Case No.: IPR2023-00743

U.S. Patent No. 6,496,939

DECLARATION OF R. JACOB BAKER, PH.D., P.E.

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I, Dr. R. Jacob Baker, declare as follows:

I. INTRODUCTION

1. I have been retained by KIOXIA Corporation and KIOXIA America, Inc. (“Petitioners”) as an independent expert in this *inter partes* review before the United States Patent and Trademark Office (“PTO”) regarding U.S. Patent No. 6,496,939 (“the ’939 patent”), Ex-1001. Specifically, I have been asked to consider whether certain references disclose or suggest the features recited in claims 1-3, 6, 10-12, and 15 of the ’939 patent (“challenged claims”). As explained below, it is my opinion that the challenged claims are invalid as anticipated and/or obvious in view of the prior art references discussed in this Declaration and the accompanying Petition.

2. I am being compensated at my ordinary consulting rate of \$655.00 per hour. No part of my compensation is dependent on the outcome of this proceeding or any other proceeding involving the ’939 patent or any of its related patents. I have no other interests in this proceeding.

II. QUALIFICATIONS

3. My qualifications are generally set forth in my Curriculum Vitae, which is attached as Ex-1004. My Curriculum Vitae also includes a list of the publications I have authored and a list of the other cases in which I have testified during the last

four years.

4. I have been working as an Engineer since 1985 and have been teaching Electrical and Computer Engineering courses since 1991. I am currently a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas (“UNLV”).

5. I received B.S. and M.S. degrees in Electrical Engineering from UNLV in 1986 and 1988, respectively. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno, in 1993.

6. My doctoral research, culminating in the award of a Ph.D., investigated the use of power MOSFETs in the design of very high peak power, and high-speed, instrumentation. I developed techniques to reliably stack power MOSFETs to switch higher voltages, that is, greater than 1,000 volts and 100 amps of current with nanosecond switching times. This work was reported in the paper entitled “Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices,” published in the IEEE Transactions on Power Electronics. The paper received the Best Paper Award in 2000.

A. Industry Experience

7. I have done technical and expert witness consulting for over 200 companies and their subsidiaries since I started working as an engineer in 1985,

which included design experience with circuits employing capacitors. This experience ranged from designing computer memory employing a one-transistor, one-capacitor memory (DRAM, dynamic random access memory) to the design of power supply circuits where capacitors are used for filtering. I've also worked on the design of capacitors to supply power to a modem in the event of a power failure. From 1985 to 1993, I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapon tests at the Nevada test site. During this time, I designed, and oversaw the fabrication of, over 30 electronic and electro-optic instruments, including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame and bit-syncs, data converters, streak-camera sweep circuits, Pockel's cell drivers, micro-channel plate gating circuits, charging circuits for battery backup of equipment for recording test data, and analog oscilloscope electronics.

8. My work during this time, as one example, had a direct impact on my doctoral research work using power MOSFETs, subsequent publishing efforts, and industry designs. In addition to the 2000 Best Paper Award from the IEEE Power Electronics Society, I published several other papers in related areas while working in industry. I hold a patent, US Patent No. 5,874,830, in the area of power supply design, titled, "Adaptively biased voltage regulator and operating method," which

was issued on February 23, 1999. I have designed dozens of linear and switching power supplies for commercial products and scientific instrumentation.

9. I am a licensed Professional Engineer and have extensive industry experience in circuit design, fabrication, and manufacture of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, Phase-Change Random Access Memory (PCRAM) chips, and CMOS Image Sensors (CISs) at Micron Technology, Inc. (“MTI”) in Boise, Idaho. I spent considerable time working on the development of flash memory chips while at MTI. My efforts resulted in more than a dozen patents relating to flash memory. One of my projects at MTI included the development, design, and testing of circuit design techniques for a multi-level cell (MLC) flash memory using signal processing. This effort resulted in higher-density memories for use in solid-state drives and flash memory cards having an ATA interface that are ubiquitous in consumer electronics, including cameras and data storage systems. Further, the use of higher-density memory can result in fewer changes in the flash translation layer for logical-to-physical addressing, less need for garbage collection, and larger data segments that can improve a computing system’s performance.

10. Another project I worked on at MTI focused on the design of buffers for high-speed double-data rate DRAM, which resulted in around 10 U.S. patents in

buffer design. Among many other experiences, I led the development of the delay locked loop (DLL) in the late 1990s so that MTI DRAM products could transition to the DDR memory protocol, used in mobile and non-mobile (server, desktop, cell phones, tablets, etc.) computing systems as main computer memory, for addressing and controlling accesses to memory via interprocess communications (IPC) with the memory controller (MC). I provided technical assistance with MTI's acquisition of Photobit during 2001 and 2002, including transitioning the manufacture of CIS products into MTI's process technology. Further, I did consulting work at Sun Microsystems and then Oracle on the design of memory modules during 2009 and 2010. This work entailed the design of low-power, high-speed, and wide interconnection methods with the goal of transmitting data to/from the memory module and the MC at higher speeds.

11. I have extensive experience in the development of instrumentation and commercial products in a multitude of areas including: integrated electrical/biological circuits and systems, array (memory, imagers, and displays) circuit design, CMOS analog and digital circuit design, diagnostic electrical and electro-optic instrumentation for scientific research, CAD tool development and online tutorials, low-power interconnect and packaging techniques, design of communication/interface circuits (to meet commercial standards such as USB,

firewire, DDR, PCIe, SPI, etc.), circuit design for the use and storage of renewable energy, and power electronics. For example, a part of my research at Boise State, for many years, focused on the use of Thru-Silicon-Vias (TSVs), aka Thru-Wafer Vias (TWVs), for high-density packaging. These packaging techniques were utilized in the memory module development work I did with Sun Microsystems and Oracle. As another example, I designed circuitry for use in implementing Universal Serial Bus (USB) interface circuits while consulting at Tower Semiconductor. I designed PCI communication circuits for IPC between a Graphics Processor Unit (GPU) and memory while consulting for Rendition, Inc.

12. My current research work is focused in part on the design of integrated circuits for wireless sensing using LIDAR (Light Detection And Ranging). I have worked with several companies in the development of these circuits and systems including Freedom Photonics, Aerius Photonics, and FLIR. In the early 1990s, I worked on wireless systems for wideband impulse radar while at Lawrence Livermore Laboratory. Further, part of my research for several years focused on the digitization of IQ channels using delta-sigma modulation. The knowledge and experience gained from this effort are reflected in my textbook *CMOS Mixed-Signal Circuit Design* and a presentation, which I have presented at several universities and companies, http://cmosedu.com/jbaker/papers/talks/BP_DSM_talk.pdf.

B. Academic Experience

13. I was an adjunct faculty member in the Electrical Engineering departments of UNLV and UNR from 1991-1993. From 1993 to 2000, I served on the faculty at the University of Idaho as an Assistant Professor and then as a tenured Associate Professor of Electrical Engineering. In 2000, I joined a new Electrical and Computer Engineering program at Boise State University (“BSU”), where I served as department chair from 2004 to 2007. At BSU, I helped establish graduate programs in Electrical and Computer Engineering including, in 2006, the university’s second Ph.D. degree. In 2012, I re-joined the faculty at UNLV. Over the course of my career as a professor, I have advised more than 100 masters and doctoral students.

14. I have been recognized for my contributions as an educator in the field. While at Boise State University, I received the President’s Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001). In 2007, I received the Frederick Emmons Terman Award (the “Father of Silicon Valley”), which is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator’s contributions to the profession. In 2011, I received the IEEE Circuits and Systems Education Award. I received the

Tau Beta Pi Outstanding Electrical and Computer Engineering Professor Award every year it was awarded while I have been back at UNLV.

15. I have authored several books and papers in the electrical and computer engineering area. My published books include *CMOS Circuit Design, Layout, and Simulation* (Baker, R.J., Wiley-IEEE, ISBN: 9781119481515 (4th ed., 2019)) and *CMOS Mixed-Signal Circuit Design* (Baker, R.J., Wiley-IEEE, ISBN: 9780470290262 (2nd ed., 2009) and ISBN: 9780471227540 (1st ed., 2002)). I co-authored *DRAM Circuit Design: Fundamental and High-Speed Topics* (Keeth, B., Baker, R.J., Johnson, B., and Lin, F., Wiley-IEEE, ISBN: 9780470184752 (2008)), *DRAM Circuit Design: A Tutorial* (Keeth, B. and Baker, R.J., Wiley-IEEE, ISBN: 0-7803-6014-1 (2001)), and *CMOS Circuit Design, Layout and Simulation* (Baker, R.J., Li, H.W., and Boyce, D.E., Wiley - IEEE, ISBN: 9780780334168 (1998)). I contributed as an editor and co-author on several other electrical and computer engineering books.

C. Other Relevant Experience

16. I have performed technical and expert witness consulting for more than 200 companies and their subsidiaries and given more than 50 invited talks at conferences, companies, and universities. Further, I am the author or co-author of more than 100 papers and presentations in the areas of electrical and computer

engineering design, fabrication, and packaging.

17. I currently serve, or have served, as a volunteer on the IEEE Press Editorial Board (1999-2004); as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018); as the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015); on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016); as a Distinguished Lecturer for the SSCS (2012-2015); the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for IEEE Solid-State Circuits Magazine; IEEE Kirchhoff Award Committee (2020-2023); and advisor for the student branch of the IEEE at UNLV (2013-present). These meetings, groups, and publications are intended to allow researchers to share and coordinate research. My active participation in these meetings, groups, and publications allowed me to see what other researchers in the field have been doing.

18. In addition to the above, I am an IEEE Fellow for contributions to semiconductor memory design and a member of the honor societies Eta Kappa Nu and Tau Beta Pi.

III. MATERIALS CONSIDERED

19. My opinions, as set forth in this Declaration, are based on the documents I have reviewed, my experience and background, and my knowledge and

professional judgment. In forming these opinions, I have reviewed the '939 patent (Ex-1001), the prosecution history for the '939 patent (Ex-1002), the prior art discussed below, and any other material and information identified in this Declaration. I have also relied on my experience and knowledge in the field of computer memory and data storage devices.

20. In particular, my opinions regarding the invalidity of the challenged claims are based on the following prior art references, as informed by my knowledge in the field of computer memory and data storage devices.

Exhibit	Description
1005	U.S. Patent No. 4,559,616 (“Bruder”). It is my understanding that Bruder issued on December 17, 1985. Petitioners’ counsel has informed me that Bruder is prior art under pre-AIA 35 U.S.C. § 102(b). <i>See infra</i> § VI.B for a more detailed description regarding my understanding of this category of prior art.
1006	U.S. Patent No. 5,596,708 (“Weber”). It is my understanding that Weber issued on January 21, 1997. Petitioners’ counsel has informed me that Weber is prior art under pre-AIA 35 U.S.C. § 102(b). <i>See infra</i> § VI.B for a more detailed description regarding my understanding of this category of prior art.

Declaration of R. Jacob Baker
Inter Partes Review of U.S. Patent No. 6,496,939

Exhibit	Description
1007	U.S. Patent No. 4,591,782 (“Germer”). It is my understanding that Germer issued on May 27, 1986. Petitioners’ counsel has informed me that Germer is prior art pursuant to 35 U.S.C. § 102(b). <i>See infra</i> § VI.B for a more detailed description regarding my understanding of this category of prior art.
1008	U.S. Patent No. 5,414,861 (“Horning”). It is my understanding that Horning issued on May 9, 1995. Petitioners’ counsel has informed me that Horning is prior art pursuant to 35 U.S.C. § 102(b). <i>See infra</i> § VI.B for a more detailed description regarding my understanding of this category of prior art.
1009	Claim Construction Order and Memorandum in Support Thereof, <i>BiTMicro LLC v. KIOXIA Am., Inc.</i> , WDTX-6-22-00331-ADA, Dkt. No. 54 (WDTX, Feb. 16, 2023).
1010	U.S. Patent No. 3,980,935 (“Worst”). It is my understanding that Worst issued on September 14, 1976. Petitioners’ counsel has informed me that Worst is prior art pursuant to 35 U.S.C. § 102(b). <i>See infra</i> § VI.B for a more detailed description regarding my understanding of this category of prior art.

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Inter Partes Review of U.S. Patent No. 6,496,939

Exhibit	Description
1011	U.S. Patent No. 4,306,299 (“Check”). It is my understanding that Check issued on December 15, 1981. Petitioners’ counsel has informed me that Check is prior art pursuant to 35 U.S.C. § 102(b). <i>See infra</i> § VI.B for a more detailed description regarding my understanding of this category of prior art.
1012	U.S. Patent No. 4,431,134 (“Hendricks”). It is my understanding that Hendricks issued on February 14, 1984. Petitioners’ counsel has informed me that Hendricks is prior art pursuant to 35 U.S.C. § 102(b). <i>See infra</i> § VI.B for a more detailed description regarding my understanding of this category of prior art.
1013	U.S. Patent No. 4,701,858 (“Stokes”). It is my understanding that Stokes issued on October 20, 1987. Petitioners’ counsel has informed me that Stokes is prior art pursuant to 35 U.S.C. § 102(b). <i>See infra</i> § VI.B for a more detailed description regarding my understanding of this category of prior art.
1014	U.S. Patent No. 4,453,117 (“Elms”). It is my understanding that Elms issued on June 5, 1984. Petitioners’ counsel has informed me that Elms is prior art pursuant to 35 U.S.C. § 102(b). <i>See infra</i> § VI.B for

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Exhibit	Description
	a more detailed description regarding my understanding of this category of prior art.
1015	U.S. Patent No. 4,412,284 (“Kerforne”). It is my understanding that Kerforne issued on October 25, 1983. Petitioners’ counsel has informed me that Kerforne is prior art pursuant to 35 U.S.C. § 102(b). <i>See infra</i> § VI.B for a more detailed description regarding my understanding of this category of prior art.
1016	U.S. Patent No. 3,562,555 (“Ahrons”). It is my understanding that Ahrons issued on February 9, 1971. Petitioners’ counsel has informed me that Ahrons is prior art pursuant to 35 U.S.C. § 102(b). <i>See infra</i> § VI.B for a more detailed description regarding my understanding of this category of prior art.
1017	U.S. Patent No. 4,636,963 (“Nakajima”). It is my understanding that Nakajima issued on January 13, 1987. Petitioners’ counsel has informed me that Nakajima is prior art pursuant to 35 U.S.C. § 102(b). <i>See infra</i> § VI.B for a more detailed description regarding my understanding of this category of prior art.

IV. TECHNOLOGY BACKGROUND

21. I understand that the '939 patent issued on December 17, 2002 and was filed on September 21, 1999. The '939 patent purportedly relates to controlling data in a computer system in the event of a power failure. *See, e.g.*, Ex-1001, Abstract. In particular, the '939 patent discusses using super-capacitors to power the transfer of data from volatile to non-volatile memory during a power failure. *Id.*

22. Using capacitors as back-up power to enable the preservation of data stored in volatile memory during an external power loss predates the September 1999 filing date of the '939 patent by many years. As early as the 1960's, it was known to use capacitors to provide back-up power for memory devices. For example, Ahrons—which was filed in 1967—describes a “memory protecting circuit” utilizing a capacitor as an “emergency power source to supply the current requirements” for memory. Ex-1016 at 3:21-24. And by the early 1980s, it was common to find a variety of devices and systems that employed capacitors as back-up power systems for preserving data in volatile memory, including in the context of microprocessor controlled motors (Ex-1014, filed on Apr. 14, 1983); postage meters (Ex-1011, filed on November 13, 1979); thermostats (Ex-1012, filed on Nov. 8, 1982); electric utility meters (Ex-1013, filed on Dec. 31, 1984); and even household appliances such as washing machines (Ex-1015, filed on March 20, 1981).

These devices employed back-up power, stored on capacitors, to ensure that data written into volatile memory was preserved until power could be restored.

23. Similarly, preserving data by using capacitors to power the transfer of data from volatile to non-volatile memory was well-known long before the filing of the '939 patent. For example, Check, which was filed in 1979 and claims priority to an application filed in 1974, discloses an electronic postage meter that uses capacitors as a backup power supply to preserve data stored in volatile memory. *See, e.g.*, Ex-1011 at Abstract; *id.* at 18:36-47; claim 18. As Check explains, postage meters contain “critical information” and “crucial accounting functions,” such as postage balances and credits, that must be preserved in non-volatile memory when external power is lost. *Id.* at 6:58-7:4; *see also id.* at 2:4-11 (explaining that the use of non-volatile memory is important to ensure that “the remaining balance in the postal meter” and the “continuous accumulation of charges thereto” is “permanently stored in the nonvolatile memory when the system is de-energized.”). Accordingly, Check describes a method for preserving this crucial data during a power failure by using capacitors to power the transfer of data “from the [volatile] working memory to the non-volatile memory.” *See e.g., id.*, Abstract; 10:55-58; 18:36-47; claim 1; claim 18.

24. Likewise, Germer, which was filed on April 12, 1984, describes an

electronic register in an electric meter. Ex-1007, Abstract. As Germer explains, electric meters include volatile memory to store electric usage data, which may be lost in the event of a power outage *Id.* at 1:62-2:5. Germer thus teaches the use of capacitors as a temporary power store. *Id.*, Abstract. In the event of a power loss, energy from the capacitors is used by a processor to power the transfer of data from the volatile memory to non-volatile memory, where it will be preserved. *Id.* at 5:49-57, 5:64-6:10.

25. Super capacitors were also well-known in the art for providing back up power for memory well before the priority date of the '939 patent. For example, Stokes, which issued in 1987, discloses super capacitors for use as backup power in a volatile memory system. Ex-1013 at 2:57-3:61. Likewise, Nakajima, which also issued in 1987, teaches a system comprising memory “whose power source is backed-up by an electric cell or an electric double layer capacitor (a capacitor generally referred to as a super capacitor having a great capacitance and with very low leaking current).” Ex-1017 at 3:65-4:3.

26. In conclusion, well before the September 1999 priority date of the '939 patent, there was a long history of using capacitors and super capacitors to supply back-up power in order to preserve data in devices in the case of a sudden loss of power.

V. OVERVIEW OF THE '939 PATENT

A. Specification of the '939 Patent

27. As explained above, I understand that the '939 patent issued on December 17, 2002, from an application filed on September 21, 1999. Counsel has informed me that the '939 patent expired on September 21, 2019. Claim 1 of the '939 patent is an independent claim, while claims 2, 3, and 6 depend from claim 1. Likewise, claim 10 is an independent claim, while claims 11, 12, and 15 depend from claim 10.

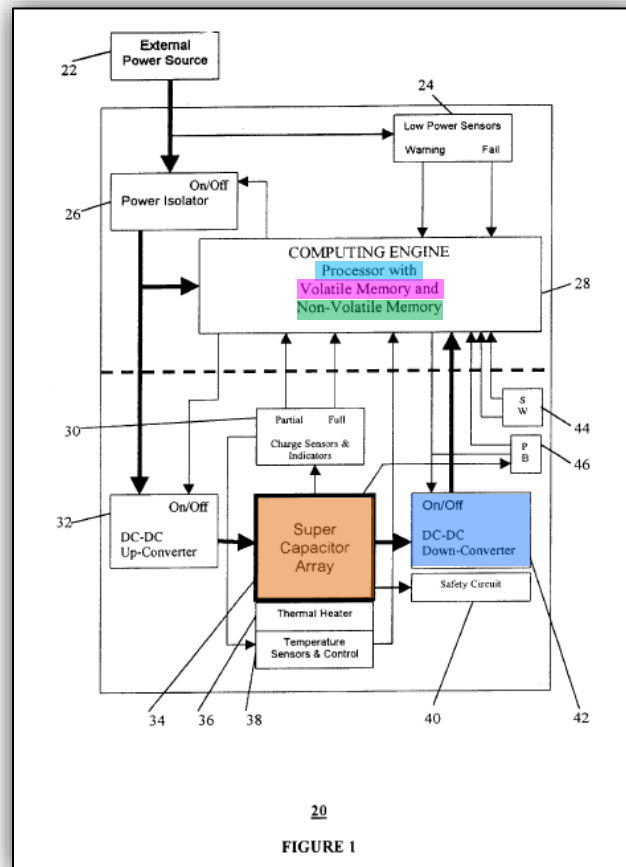
28. The '939 patent describes well known systems and methods for controlling data in a computer system when the computer system loses power. Ex-1001 at 1:8-11. According to the '939 patent, computer systems typically comprise two types of memory: volatile “cache” memory, which is erased when power is removed, and non-volatile memory, which preserves data even when power is removed. *Id.* at 1:15-33. Since volatile cache memory is much faster than non-volatile memory, data is typically written to cache memory before being transferred to non-volatile memory. *Id.* However, the '939 patent explains that, when external power is suddenly lost, there is insufficient time to transfer all newly written data from volatile cache memory to non-volatile memory. *Id.* at 1:34-39. This creates a risk that data will be lost. *Id.* Accordingly, the '939 patent identifies an alleged need

to ensure that all newly written data to the volatile memory is safely transferred to non-volatile memory in the event of a sudden power loss. *Id.* at 2:13-16.

29. The '939 patent purports to address this need by using a “computing engine” comprising a processor, volatile memory, and non-volatile memory ... all commonplace, well-known components. *Id.* at 3:33-36; Figure 1. The '939 patent also discloses an array of “super capacitors” as a “short term power source” for the computing engine ... components that were also well-known at the time of invention. *Id.* at 2:27-31; 3:3-5. Upon a sudden loss of external power, the super capacitors are purportedly “activated” to maintain internal power to the system. *Id.* at 5:8-11. Using the stored charge on the super capacitors, data in volatile memory is transferred to non-volatile memory. *Id.* at 5:33-36. Once the super-capacitors have discharged to a predetermined level, the super-capacitors are purportedly “deactivated” to cut off power to the computer system. *Id.* at 5:39-43; 5:48-52; 6:49-53. According to the specification, the super-capacitors are activated and deactivated by a “down-converter,” which converts the high-voltage stored on the super-capacitors to a lower voltage that can be utilized by the computing engine. *Id.* at 5:8-29; 5:39-43; 6:11-31; 6:40-44.

30. Figure 1 of the '939 patent, annotated below, illustrates this system. In particular, annotated Figure 1 illustrates the computing engine, which comprises a

processor, volatile memory, and non-volatile memory, as well as a super capacitor array and voltage down-converter.



31. However, as explained below, systems comprising the disclosed “computing engine,” capacitors, and voltage down-converters were well known before the priority date of the ’939 patent. Likewise, reconfiguring data by using energy stored in the capacitors to facilitate data transfer from volatile to non-volatile memory upon a sudden loss of power was equally well known before the priority date of the ’939 patent. As explained below, Horning, Stokes, Bruder, Weber, and

Germer all disclose such systems. Accordingly, nothing about the claims of the '939 patent would have been novel or non-obvious to a person of ordinary skill in the art ("POSITA") at the time the application for the '939 patent was filed.

B. Prosecution History

32. I understand that claim 1, as originally filed, was similar to issued claim 1 except that it did not recite a step for deactivating the plurality of super capacitors. Specifically, I understand that originally filed claim 1 recited the following:

1. A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:

(a) activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system; and

(b) reconfiguring the data in the computing engine.

Ex-1002 at 19.

33. Similarly, I understand that claim 10, as originally filed, recited means for activating a plurality of super capacitors and means for reconfiguring data in the computing engine but did not recite means for deactivating the plurality of super-capacitors. *Id.* at 20.

34. I understand that, on June 15, 2001, the Patent Office issued a non-final

Office Action rejecting the claims. *Id.* at 35-40. In particular, the Examiner stated that the prior art references of record taught “a system and method for controlling data in a computer system when the system loses power; comprising a computing engine; and activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computing system and reconfiguring data in the computing engine.” *Id.* at 36-37. The Examiner further stated that the prior art “teaches at least one volatile memory and at least one non-volatile memory” and “teaches allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory.” *Id.* at 38. In addition, the Examiner stated that the prior art “teaches reversing the flow of current between the computing engine and the plurality of super-capacitors; and discharging current from the plurality of super capacitors to the computing engine.” *Id.* at 38.

35. I understand that, in response to the Office Action, the applicant did not challenge the Examiner’s conclusions regarding these prior arts teachings. Instead, the applicant amended claim 1 to include an additional step for deactivating the capacitors as stated below:

- c. A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:
- (c) activating a plurality of super capacitors to supply

power to the computing engine based upon power being removed from the computer system;

(b) reconfiguring the data in the computing engine, and

© deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.

Ex-1002 at 75-76.

36. The applicant similarly amended claim 10 to recite a means for deactivating the capacitors, as stated below:

10. A system for controlling data in a computer system when the computer system loses power, the computer system comprising a computer engine, comprising:

means for activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;

means for reconfiguring the data in the computing engine; and

means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.

Id. at 76.

37. In its response, the applicant argued that the “deactivation” limitation was “neither taught nor suggested” by the prior art of record. *Id.* at 67-74. The applicant also alleged that reliability is improved when “power is cut off to the computing engine when the super capacitors reach a predetermined level.” *Id.* at 68. According to the applicant, this predetermined level “can be set above the minimum

operating voltage of the computer system.” *Id.* The applicant further argued that cutting off power from the capacitors at a predetermined level is advantageous because “it may take only a few seconds to recharge the super capacitors, rather than several minutes, rapidly providing protection against power loss.” *Id.*

38. The Examiner subsequently issued a Notice of Allowability based on the applicant’s arguments. *Id.* at 83. As explained below, however, deactivating capacitors to cut off power to a computing engine upon discharging to a predetermined level was well known before the priority date of the ’939 patent. Accordingly, it is my opinion that nothing about this limitation was novel or non-obvious to a POSITA at the time the application for the ’939 patent was filed.

VI. LEGAL PRINCIPLES USED IN ANALYSIS

39. I am not an attorney and I offer no opinions on the law. I have been advised by Petitioners’ counsel of certain legal principles relevant to an invalidity analysis, as summarized below. I have conducted my analysis in accordance with these principles.

A. Prior Art

40. I understand that a patent or other publication must qualify as prior art before it can be used to invalidate a patent claim.

41. I understand that a U.S. or foreign patent qualifies as prior art to a

challenged claim if the patent was issued prior to the invention date of the challenged claim. I also understand that a U.S. or foreign patent or published patent application qualifies as prior art to a challenged claim if it was published before the invention date of the challenged claim.

B. Anticipation

42. I understand that a prior art reference “anticipates” an asserted claim, thereby rendering the claim invalid, if all elements of the claim are disclosed in the reference, either expressly or inherently. I understand that an element is disclosed inherently in a prior art reference if it is necessarily present in the prior art reference or is the natural result flowing from the disclosure of the prior art reference. I have been informed that a prior art reference does not need to use the same words as the challenged claim in order to anticipate the claim.

43. Petitioners’ counsel informs me that the application for the ’939 patent was filed before the America Invents Act (“AIA”) was enacted. Accordingly, I have been informed that pre-AIA 35 U.S.C. § 102 defines the types of references that can be used as prior art against the challenged claims.

44. I understand that under pre-AIA 35 U.S.C. § 102(a), a challenged claim is anticipated if it was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention

thereof by the patent applicant.

45. I also understand that under pre-AIA 35 U.S.C. § 102(b), a challenged claim is anticipated if was patented or described in a printed publication in this or a foreign country, or in public use or on sale in this country, more than one year prior to the date of the patent application in the United States.

C. Obviousness

46. I also understand that a patent is invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the pertinent art at the time the invention was made. I understand that a POSITA provides a reference point from which the prior art and claimed invention should be viewed. This reference point prevents one from using his or her own personal insight or hindsight in deciding whether a claim is obvious.

47. I understand that an obviousness determination includes the consideration of various factors, such as (1) the scope and content of the prior art, (2) the differences between the prior art and the asserted claims, (3) the level of ordinary skill in the pertinent art, and (4) the existence of secondary considerations such as commercial success, long-felt but unresolved needs, failure of others, etc.

48. I understand that an obviousness evaluation can be based on a

combination of multiple prior art references. I understand that the prior art references themselves may provide a suggestion, motivation, or reason to combine, which does not need to be explicit. I further understand that any need or problem known in the field and addressed by the patent can provide a reason for combining the elements in the manner claimed. To determine whether there was an apparent reason to combine the known elements in the way a patent claims, I have been informed that I may look to interrelated teachings of multiple patents, to the effects of demands known to the relevant community or present in the marketplace, and to the background knowledge possessed by a POSITA. I also understand that practical and common-sense considerations should guide a proper obviousness analysis because familiar items may have obvious uses beyond their primary purposes. I further understand that a POSITA looking to overcome a problem will often be able to fit together the teachings of multiple publications. I understand that an obviousness analysis therefore accounts for the inferences and creative steps that a POSITA would employ under the circumstances.

49. I understand that the nexus linking two or more prior art references can also be simple common sense. I further understand that the obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references may be supplied by the

direction of the marketplace.

50. I understand that if a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

51. I understand that a particular combination may be proven obvious merely by showing that it was obvious to try the combination. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a POSITA has good reason to pursue the known options within his or her technical grasp because the result is likely not the product of innovation, but of ordinary skill and common sense.

52. I understand that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different field. If a POSITA can implement a predictable variation, the patent claim is likely obvious.

53. As noted above, I understand that a proper obviousness analysis focuses on what was known or obvious to a POSITA, not just the patentee. Accordingly, I

understand that any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.

54. I understand that a claim can be obvious in light of a single reference, without the need to combine references, if the elements of the claim that are not found explicitly or inherently in the reference can be supplied by the common sense or knowledge of one of skill in the art.

55. I also understand that secondary indicia of non-obviousness may include: (1) a long-felt but unmet need in the prior art that was satisfied by the invention of the patent; (2) commercial success of processes covered by the patent; (3) unexpected results achieved by the invention; (4) praise of the invention by others skilled in the art; (5) taking of licenses under the patent by others; (6) deliberate copying of the invention; (7) failure of others to find a solution to the long-felt need; and (8) skepticism by experts.

56. I also understand that there must be a relationship between any such secondary considerations and the invention. I further understand that contemporaneous and independent invention by others is a secondary consideration

supporting an obviousness determination.¹

¹ In this case, I am not aware of any such secondary considerations that would support the conclusion that the claims of the '939 patent are not obvious. To the contrary, it does not appear that there was any long-felt but unmet need for the alleged invention; as noted below, data preservation systems that used capacitors to power the transfer of data from volatile to non-volatile memory were well known. I am also not aware of any evidence that Bit Microsystems Inc. (the original patentee) had commercial success marketing any product covered by the '939 patent. I am also unaware of any unexpected results achieved by the alleged invention; to the contrary, as described below, numerous systems used energy stored in capacitors to ensure that data stored in volatile memory was preserved in non-volatile memory in the event of a power loss. Likewise, systems that used power from capacitors to transfer data from volatile to non-volatile memory, thereby safeguarding data and increasing the ease by which it can be secured and recovered, were used well before the priority date of the '939 patent. I am also unaware any of any praise of the '939 patent by those skilled in the art, any deliberate copying of the '939 patent, any failure of others to find a solution, or any skepticism by experts regarding the methods of the '939 patent.

57. In sum, it is my understanding that prior art teachings are properly combined where a POSITA—having the understanding and knowledge reflected in the prior art and being motivated by the general problem facing the inventor—would have been led to make the combination of elements recited in the claims. Under this analysis, the prior art references themselves, or any need or problem known in the field of endeavor at the time of the invention, can provide a reason for combining the elements of multiple prior art references in the claimed manner.

D. Claim Construction

58. I understand that, before an invalidity analysis can be performed, the scope and meaning of the challenged claims must be determined. It is my understanding that this is accomplished through the process of claim construction.

59. I have been informed and understand that claims are generally construed from the perspective of a POSITA at the time of the invention, which I have been asked to assume is the '939 patent's priority date of September 21, 1999. More specifically, I understand that the claims should be afforded a meaning in accordance with the ordinary and customary meaning of the claim, as understood by a POSITA at the time of the invention.

60. I have been advised that, in construing a claim term, one must first look to the “intrinsic” patent evidence, which includes the claims themselves, the patent

specification, and the prosecution history of the patent. I have also been informed that “extrinsic” evidence, which is outside the patent and prosecution history, may be useful in construing patent claims. It is my understanding that such extrinsic evidence may include dictionaries, textbooks, treatises, and similar sources of information.

61. I have been advised that a claim may recite a function to be performed rather than a structure for performing the function. I have been informed that such claim terms are known as “means-plus-function” claim terms. I understand that a term introduced by the phrase “means for” is presumed to be a means-plus-function claim term. I have also been informed that a claim term may be construed as a means-plus-function term where it fails to recite sufficiently definite structure, or else recites function without reciting sufficient structure for performing that function.

62. I have been advised that the construction of a means-plus-function claim term is a two-step process. I understand that the first step requires an identification of the function recited in the claim. I understand that the second step requires determining what structure is disclosed in the specification for performing the recited function. I have been advised that a structure disclosed in the patent specification qualifies as corresponding structure if the intrinsic evidence clearly links or associates that structure to the function recited in the claim. I have been

advised that the proper construction for a means-plus-function term is restricted to the corresponding structure identified in the specification and equivalents thereof.

63. I understand that claims must be construed in an *inter partes* review using the same claim construction standard that would be used to construe the claim in a civil action before a district court.

VII. LEVEL OF ORDINARY SKILL IN THE ART

64. My opinions have been guided by my appreciation of how a POSITA (described below) would have understood the claims of the '939 patent as of the invention date, which I have been asked to assume is the patent's priority date, September 21, 1999.

65. It is my understanding that a POSITA is one who is presumed to be aware of all pertinent art and is a person of ordinary creativity. I further understand that the following factors may be considered in establishing the level of ordinary skill in the art in the relevant field: the type of problems encountered in the art; the prior art solutions to those problems; the rapidity with which innovations are made; sophistication of the technology; and the educational level of active workers in the field.

66. Based on the above factors, the materials and information I have reviewed, and my extensive experience with the subject matter of the '939 patent

around the time of the invention date, it is my opinion that a POSITA related to the technology of the '939 patent would have had at least a bachelor's degree in electrical engineering or related field, and at least two years of work experience in the computer memory or data storage industry that includes experience with using batteries or capacitors to supply power. Someone with less technical education but more experience, or more technical education but less experience, would also meet this standard.

67. Based on my education and experience in the fields of electrical engineering, computer memory, and data storage, I believe that I am well qualified to provide opinions about how a POSITA would have interpreted and understood the claims of the '939 patent and the prior art discussed below.

VIII. CLAIM CONSTRUCTION

68. I have set forth my understanding of relevant claim construction principles above, which I have followed in my analysis. Below I discuss Petitioners' constructions of seven claim terms. In my view, the remaining claim terms should be given their plain and ordinary meaning.

A. "predetermined level"

69. Counsel informs me that the district court has construed the term "predetermined level" as having a plain and ordinary meaning. Ex-1009. For the

purposes of this declaration, I have been asked to adopt this construction in my analysis.

B. “computing engine”/“computer engine”

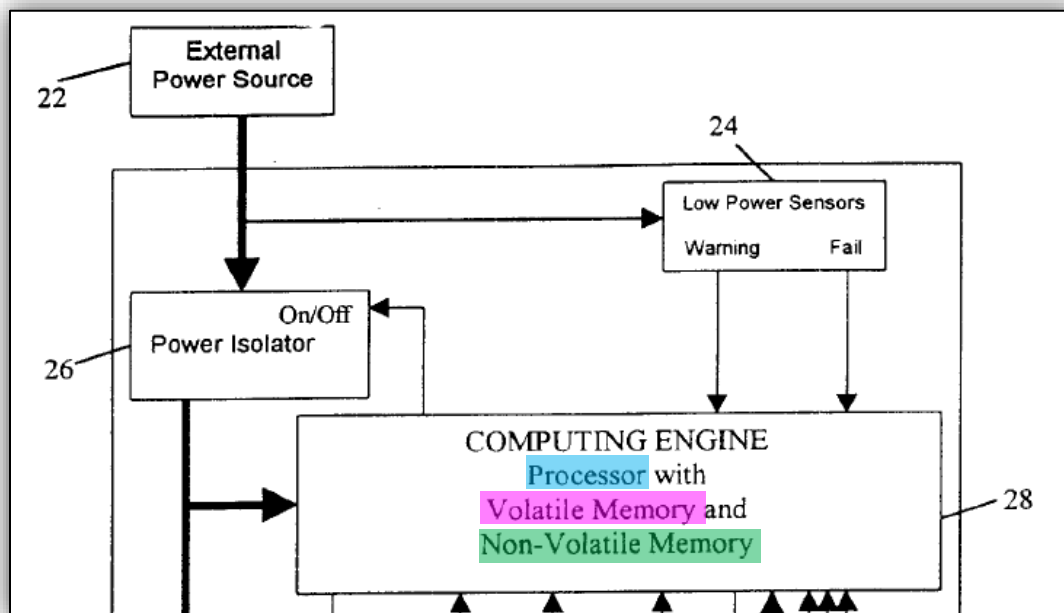
70. Independent claim 1 recites a method for controlling data in a computing system, in which “the computer system compris[es] a computing engine.” Ex-1001, claim 1. Independent claim 1 further recites “activating a plurality of super capacitors to supply power to the computing engine,” “reconfiguring the data in the computing engine,” and “deactivating the plurality of super capacitors to cut off power to the computing engine.” *Id.* Likewise, the dependent claims further recite: that “the computing engine comprises a [sic] least one volatile memory and at least one non-volatile memory”; “reversing the flow of current between the computing engine and the plurality of Super capacitors”; and “discharging current from the plurality of super capacitors to the computing engine.” *Id.* at claims 2, 6. Claims 10, 11, and 15 contain similar recitations in mean-plus-function format.”²

71. I understand that Petitioners have proposed that the “computing engine” should be construed as comprising a processor or similar structure for directing the

² The preamble of claim 10 recites a “computer engine”, but the individual elements of claim 10 recite a “computing engine.”

transfer and storage of data in memory, volatile memory, and non-volatile memory. Based on my review of the intrinsic record, together with the knowledge of a POSITA, I agree with this construction.

72. The specification explicitly states that the computing engine “contain[s] the processor, volatile and non-volatile memory.” *Id.* at 3:33-36. This is confirmed by the excerpt of annotated Figure 1 shown below, which illustrates the computing engine as containing a **processor**, **volatile memory**, and **non-volatile memory**:



73. Moreover, a POSITA would have understood that the processor is a structure that controls the memory and sends signals and instructions to direct the transfer and storage of data in the volatile and non-volatile memory. Accordingly, based on the description in the specification, together with the knowledge of a

POSITA, I agree that the term “computing engine” should be construed as comprising a processor or similar structure for directing the transfer and storage of data in memory, volatile memory, and non-volatile memory.

C. “means for activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system”

74. Independent claim 10 recites a computer system comprising a “means for activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system.” This term is introduced by the phrase “means for,” which I am informed creates a presumption that it is a means-plus-function term. It is also my opinion that this phrase does not connote any particular structure. Accordingly, I have been asked to assume that this is a means-plus-function element and conduct my analysis in accordance with the two-step process for a means-plus-function term set forth above. *Supra* ¶¶ 61-62.

1. Step 1 – Recited Function

75. I understand that Petitioners have proposed that the recited function is “activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system.” This function is recited verbatim in the language of claim 10. Accordingly, I agree with the Petitioners that “activating a plurality of super capacitors to supply power to the

computing engine based upon power being removed from the computer system” is the recited function.

2. Step 2 – Corresponding Structure

76. I understand that the district court did not directly construe “means for activating,” but the court did construe “means for reversing the flow of current between the computing engine and the plurality of super capacitors” in the context of claim 15. As recited in claim 15, the “activating means . . . comprises: means for reversing the flow of current” Accordingly, because the “means for activating” includes the “means for reversing,” I have been asked to adopt the court’s construction of “means for reversing” for this claim element as well.

77. I understand that the district court construed the structure for the “means for reversing” element as a “down-converter 42 and up-converter 42³ in Figure 1 (and corresponding text), and equivalents thereof.” Ex-1009 at 26, 47.

³ The court’s recitation of an “up-converter **42**” appears to be an error, as the ’939 patent does not disclose an up-cover with this numerical designation. Instead, the ’939 patent discloses an “up-converter **32**.” Ex-1001 at 3:39-41 (emphasis added); Figure 1. Accordingly, I have applied the structure for up-converter 32 in my analysis.

Petitioners have proposed that the structure for the “means for activating” include the structure identified by the district court with respect to the “means for reversing” as well as associated circuit components. As a result, I have incorporated this construction for the “means for activating” claim element.

D. “means for reconfiguring the data in the computing engine”

78. Independent claim 10 recites a computer system comprising “means for reconfiguring the data in the computing engine.” This term is introduced by the phrase “means for,” which I am informed creates a presumption that it is a means-plus-function term. It is also my opinion that this phrase does not connote any particular structure. Accordingly, I have been asked to assume that this is a means-plus-function element and conduct my analysis in accordance with the two-step process for a means-plus-function term set forth above. *Supra* ¶¶ 61-62.

1. Step 1 – Recited Function

79. I understand that Petitioners have identified the recited function as “reconfiguring the data in the computing engine.” This function is recited verbatim in the language of claim 10. Accordingly, I agree with the Petitioners that “reconfiguring the data in the computing engine” is the recited function.

2. Step 2 – Corresponding Structure

80. I understand that Petitioners have proposed that the structure disclosed in the specification as corresponding to the recited function is a “processor or

equivalent structure that directs the transfer and storage of data in memory.” Based on my review of the intrinsic record, together with the knowledge of a POSITA, I agree with this construction.

81. As explained above, the ’939 patent states that the computing engine comprises a processor, volatile memory, and non-volatile memory. Ex-1001 at 3:33-36; Figure 1; *supra* ¶¶ 70-73. A POSITA would also understand that the processor is a structure that controls the volatile and non-volatile memory in the computing engine by sending signals and instructions to direct the transfer and storage of data in the volatile and non-volatile memory. *See also, e.g.*, Ex-1001 at 5:33-36; 6:35-37; *supra* ¶¶ 70-73.

82. Accordingly, I agree that this claim term recites the function of “reconfiguring the data in the computing engine.” Based on the description in the specification and the knowledge of a POSITA, I further agree that the corresponding structure linked to this function is a “processor or equivalent structure that directs the transfer and storage of data in memory.”

E. “means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level”

83. Independent claim 10 recites a computer system comprising “means for deactivating the plurality of super capacitors to cut off power to the computing

engine based upon the plurality of super capacitors discharging to a predetermined level.” I am informed by that the district court has construed this term as a means-plus-function term, and for the purposes of this declaration have adopted the district court’s construction in my analysis, as discussed below.

1. Step 1 – Recited Function

84. I understand that the district court has identified the recited function as “deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.” Ex-1009 at 20, 46. This function is recited verbatim in the language of claim 10 and, for the purposes of this declaration, I have adopted the district court’s construction in my analysis.

2. Step 2 – Corresponding Structure

85. I understand that the district court has identified the structure corresponding to the recited function as a “down-converter 42 in Figure 1 (and corresponding text) and equivalents thereof, and switches, transistors, gates, *etc.* that are generally known in the art.” Ex-1009 at 20, 46. For the purposes of this declaration, I have adopted the district court’s construction in my analysis.

F. “means for allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory”

86. Dependent claim 12 recites the system of claim 11 wherein the

reconfiguring means further comprises “means for allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory.” This term is introduced by the phrase “means for,” which I am informed creates a presumption that it is a means-plus-function term. It is also my opinion that this phrase does not connote any particular structure. Accordingly, I have been asked to assume that this is a means-plus-function element and conduct my analysis in accordance with the two-step process for a means-plus-function term set forth above. *Supra* ¶¶ 61-62.

1. Step 1 – Recited Function

87. I understand that Petitioners have identified the recited function as “allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory.” This function is recited verbatim in the language of claim 12. Accordingly, I agree with the Petitioners that “allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory” is the recited function.

2. Step 2 – Corresponding Structure

88. I understand that Petitioners have proposed that the structure corresponding to the recited function is a “processor or equivalent structure that directs the transfer and storage of data in memory and is configured to transfer all

data from volatile to non-volatile memory.” Based on my review of the intrinsic record, together with the knowledge of a POSITA, I agree with this construction.

89. As stated in the claim language, dependent claim 12 further limits the “means for reconfiguring” claim element. For the reasons explained above, it is my opinion that the structure corresponding to the “means for reconfiguring” claim element is a “processor or equivalent structure that directs the transfer and storage of data in memory.” *Supra* ¶¶ 80-82. Claim 12 illustrates that this structure must further be configured such that it “allow[s] all data to be transferred from the at least one volatile memory to the at least one non-volatile memory.”

90. Accordingly, I agree that this claim term recites the function of “allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory.” Based on the description in the specification, I further agree that the corresponding structure linked to this function is a “processor or equivalent structure that directs the transfer and storage of data in memory and is configured to transfer all data from volatile to non-volatile memory.”

G. “reversing the flow of current between the computing engine and the plurality of super capacitors”

91. Claim 6 recites “reversing the flow of current between the computing engine and the plurality of super capacitors.” I am informed by counsel that the district court has construed this term as having a plain and ordinary meaning. Ex-

1009 at 23-24, 46. I have been asked by counsel to adopt this construction in my analysis for the purposes of this declaration.

H. “means for reversing the flow of current between the computing engine and the plurality of super capacitors”

92. Dependent claim 15 recites the system of claim 12 wherein the activating means further comprises “means for reversing the flow of current between the computing engine and the plurality of super capacitors.” I am informed by counsel that the district court has construed this term as a means-plus-function term, and for the purposes of this declaration I have adopted the district court’s construction, as discussed below.

1. Step 1 – Recited Function

93. I understand that the district court has identified the recited function as “reversing the flow of current between the computing engine and the plurality of super capacitors.” Ex-1009 at 26, 47. This function is recited verbatim in the language of claim 15, and for the purposes of this declaration, I have adopted the district court’s construction in my analysis.

2. Step 2 – Corresponding Structure

94. I understand that the district court has identified “down-converter 42 and up-converter 42 in Figure 1 (and corresponding text), and equivalents thereof” as the corresponding structure for performing the recited function. Ex-1009 at 26,

47. For the purposes of this declaration, I have adopted the district court's construction in my analysis.

I. “means for discharging current from the plurality of super capacitors to the computing engine”

95. Dependent claim 15 also recites the system of claim 12 wherein the activating means further comprises “means for discharging current from the plurality of super capacitors to the computing engine.” This term is introduced by the phrase “means for,” which I am informed creates a presumption that it is a means-plus-function term. It is also my opinion that this phrase does not connote any particular structure. Accordingly, I have been asked to assume that this is a means-plus-function element and conduct my analysis in accordance with the two-step process for a means-plus-function term set forth above. *Supra* ¶¶ 61-62.

1. Step 1 – Recited Function

96. I understand that Petitioners have proposed that the recited function is “discharging current from the plurality of super capacitors to the computing engine.” This function is recited verbatim in the language of claim 15. Accordingly, I agree with the Petitioners that “discharging current from the plurality of super capacitors to the computing engine” is the recited function.

2. Step 2 – Corresponding Structure

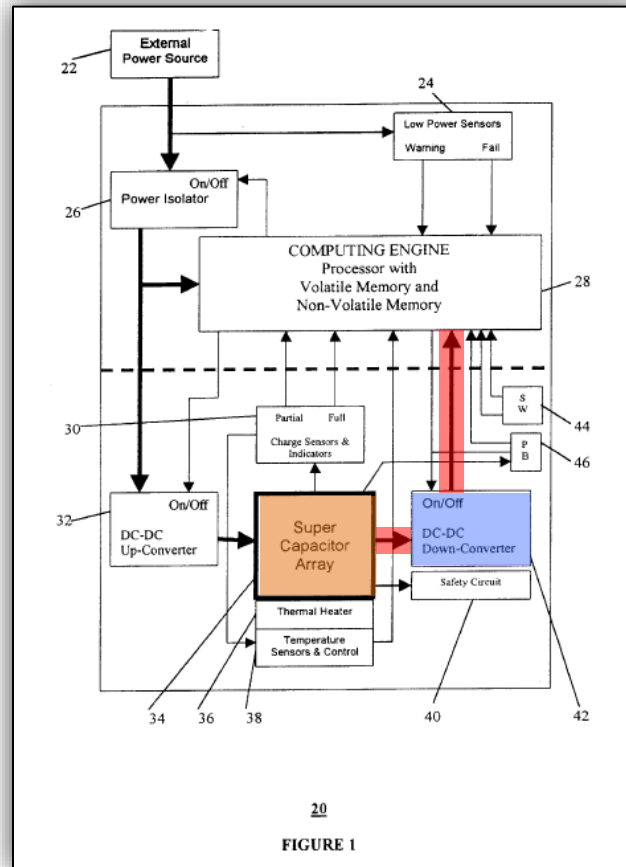
97. I understand that Petitioners have proposed that the structure disclosed

in the specification as corresponding to the recited functionality is a “voltage down-converter that converts a high voltage signal to a lower voltage signal and is configured to discharge current from the capacitors to the computing engine.” Based on my review of the intrinsic record, together with the knowledge of a POSITA, I agree with this construction.

98. As stated in the claim language, dependent claim 15 further limits the “means for activating the plurality of super-capacitors” claim element. As explained above, I have been asked to adopt the following construction for the “means for activating” element: a “down-converter 42 and up-converter 42 in Figure 1 (and corresponding text), and equivalents thereof.” It is my opinion that the portion of this structure corresponding to “discharging current from the plurality of super capacitors to the computing engine,” is a down-converter configured to discharge current from the plurality of super capacitors to the computing engine.

99. This is confirmed by the specification, which states that, once the down-converter has been activated and current has been reversed, “[t]he super capacitors then begin to *slowly discharge current* to the computer system *through the down-converter.*” Ex-1001 at 5:26-28 (emphasis added); 6:28-31; Figures 3 and 5 (stating that current is discharged “to the computer system through the down converter”). Annotated Figure 1, shown below, further illustrates that **current** from the

capacitors is discharged through the **down-converter** to the computing engine:



100. Accordingly, I agree that this claim term recites functionality for “discharging current from the plurality of super capacitors to the computing engine.” Based on the description in the specification, I further agree that the corresponding structure linked to this function is a “voltage down-converter or equivalent structure that converts a high voltage signal to a lower voltage signal and is configured to discharge current from the capacitors to the computing engine.”

IX. OVERVIEW OF THE PRIOR ART

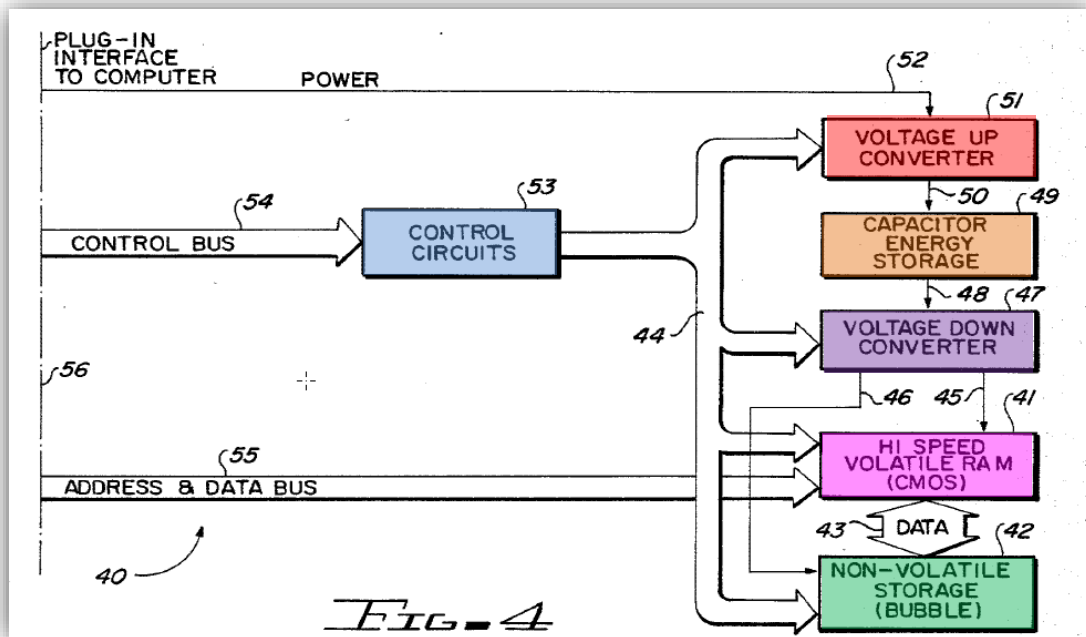
A. Bruder Discloses Systems and Methods for Storing Data in a Computer System When Power Is Lost

101. Bruder is directed to systems and methods for utilizing non-volatile memory that retains data upon a loss of external power. Ex-1005 at 1:8-13. As the specification explains, low power semiconductor memory has replaced many other types of memory previously utilized in computer systems. *Id.* at 1:14-18. However, Bruder notes that semiconductor memory suffers from “one drawback” in that it loses stored data if the power is interrupted, even momentarily. *Id.* at 1:18-21. Despite this fact, the lower costs of semiconductor memory make it “increasingly attractive” for a variety of applications. *Id.* at 1:32-38. As a result, Bruder cites the need for a “practical, inexpensive, non-volatile, high speed, low power semiconductor memory” for use in such applications. *Id.* at 1:39-42.

102. To meet this need, Bruder discloses a method and system for securely storing data when power is interrupted. This system includes volatile CMOS RAM and non-volatile “bubble memory.” *Id.* at 7:52-60. While the volatile memory is used by the computer during normal operations, the entire contents of the volatile memory can be “rapidly transfer[red]” to the non-volatile memory upon a power failure. *Id.* The power needed to facilitate this data transfer is supplied by a bank of storage capacitors containing sufficient energy to allow the transfer of data from

volatile to non-volatile memory. *Id.* at 7:60-66. Power from these capacitors is routed through a “voltage down converter,” which maintains the proper operating voltage for each of the system’s components. *Id.* at 8:2-10. Bruder teaches that control circuitry directs the transfer of data from volatile to non-volatile memory. *Id.* at 8:37-45.

103. Annotated Figure 4 of Bruder, shown below, illustrates the **control circuits**, **capacitor bank**, **volatile memory**, **non-volatile memory**, **voltage up converter**, and **voltage down converter** in this system.



104. As Bruder explains, this system provides a “very efficient design” with enough power to effectuate a complete transfer of data from volatile memory to non-

volatile memory in the event of a power interruption. *Id.* at 10:54-64. As a result, this system “mak[es] the entire memory system non-volatile, in effect.” *Id.*

B. Weber Discloses a Transfer Memory Backup System To Safeguard Data When Power Is Lost

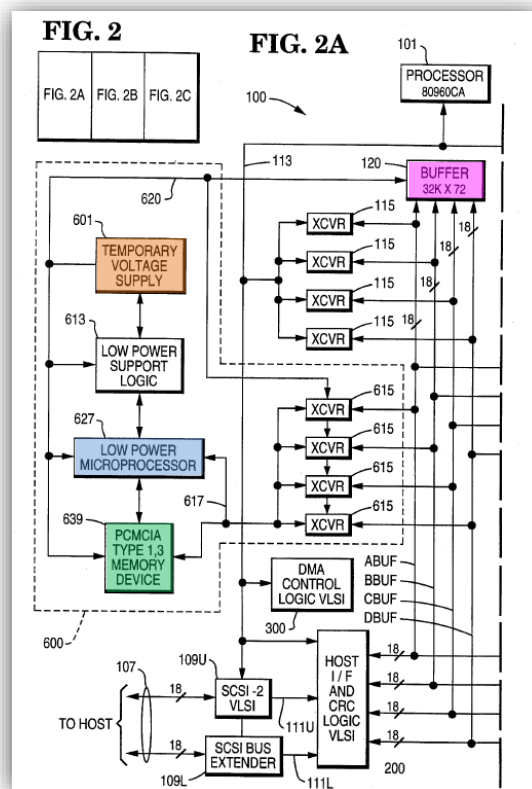
105. Weber is directed to systems and methods for safeguarding data in disk array systems during disk write operations. Ex-1006 at 1:7-9; *see also id.* at Abstract. Weber explains that these systems perform early write operations in which write data received from a host is written to a volatile transfer buffer, after which a write complete status signal is sent to the host. *Id.* at 2:44-47. However, if a power failure occurs after the issuance of the write command signal is sent to the host—but before the data has been written from the volatile transfer buffer to a disk—the data could be lost. *Id.* at 3:5-8. Accordingly, Weber cites the need for a “method and structure for safeguarding disk array early write operations . . . to prevent the data loss resulting from the occurrence of a power failure” prior to the completion of write procedures to a disk. *Id.* at 3:24-27.

106. To meet this need, Weber discloses a “transfer memory backup system” for use with a computer data storage system. *Id.* at 3:51-57. This transfer memory backup system comprises volatile memory in the form of a transfer buffer, together with non-volatile PCMCIA flash card memory. *Id.* at Abstract; 3:38-43; 4:16-20; 5:13-20. The system also includes a low power microprocessor, which controls data

transfer from volatile to non-volatile memory. *Id.* at 4:13-16; 6:65–7:8; 7:22-36.

Weber’s transfer memory backup system also comprises a temporary voltage source, which may include a “high capacitance gold capacitor,” to power the transfer of data from volatile to non-volatile memory upon a loss of external power. *Id.* at Abstract; 4:5-10; 6:65–7:8; 7:17-21.

107. Annotated Figure 2A of Weber, shown below, illustrates the **low power microprocessor**, **capacitor** (temporary voltage supply), **volatile memory** (buffer), and **non-volatile memory** (PCMCIA memory):



C. Germer Discloses an Electronic Register That Preserves Data

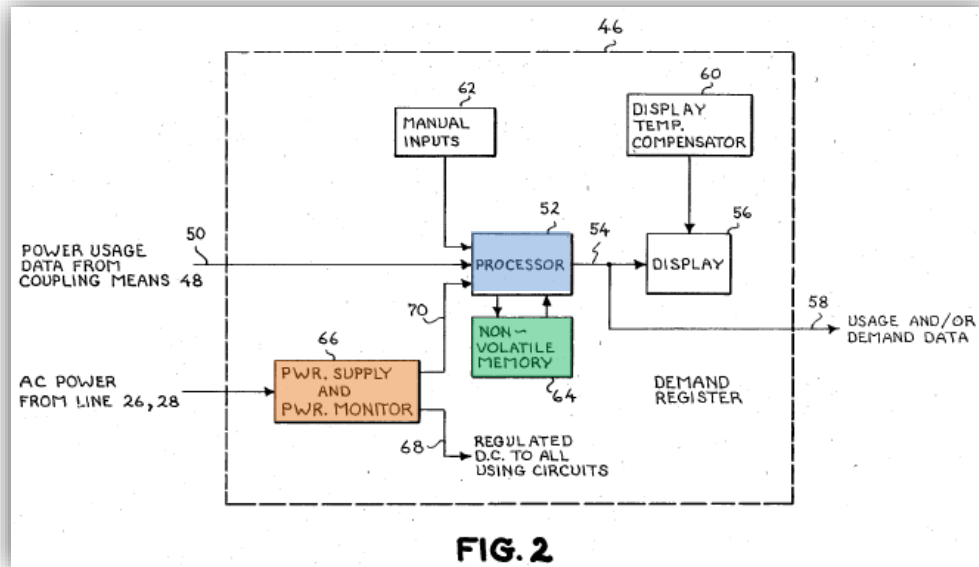
When Power Is Lost

108. Germer is directed to an electronic register, which can be used in an electric meter, into which data is written in the event of a power outage. Ex-1007 at Abstract. As Germer explains, some electric meters have computerized systems that include volatile random access memory to store electric usage data. *Id.* at 1:62-2:1. In the event of a power outage, the contents of the volatile memory may be erased, leading to the loss of such data. *Id.* at 2:1-5. Germer states that “[t]his is, of course, unacceptable.” *Id.* at 2:5. Accordingly, Germer identifies the need for a system to store this data in non-volatile memory when a power outage occurs. *Id.* at 2:6-8.

109. To address this need, Germer discloses an electronic register that preserves data upon a power outage. *Id.* at 2:27-30. This system includes volatile random access memory and non-volatile memory, a processor, and capacitors to store power. *Id.* at Abstract; 5:39-57. In the event of a power outage, the capacitors provide energy—through a regulator that converts a high-voltage signal to a low-voltage regulated signal appropriate for the electronic components—to power the transfer of data from volatile to non-volatile memory. *Id.* at 5:64-6:10. Using this power, the processor directs and controls the transfer of data from volatile memory to non-volatile memory. *Id.* at 5:49-57.

110. Annotated Figure 2 of Germer, shown below, illustrates the **processor**,

which contains volatile memory, **non-volatile memory**, and a power supply and power monitor, which contains **capacitors**, for power storage and use.



D. Horning Discloses A Data Protection System That Uses Reserve Power To Maintain Data in Volatile Memory

111. Horning is directed to a data protection system that uses different levels of reserve power to preserve data in volatile memory systems in the event of a power failure. Ex-1008 at Abstract. As Horning explains, while volatile memory arrays are capable of storing large amounts of data and are relatively compact and inexpensive, the loss of electrical power to the memory array can result in total data loss. *Id.* at 1:26-45. Horning goes on to explain that replacing or reconstructing this lost data can be difficult and time consuming, or even impossible. *Id.* at 1:46-52. Horning discusses several data protection systems, *id.* at 1:64-3:55, and identifies a

need for a data protection system that allows for a user configurable power sequence to allow a user to tailor the operation of the data protection system based on the capacity of the backup power source. *See id.* at 3:56-4:6.

112. To meet this need, Horning describes an intelligent data protection system that includes a power subsystem for providing backup power to a volatile memory that is preferably a solid state disk drive (SSD). *See id.* at 5:51-60. The backup power is supplied by a power subsystem that includes a reserve power supply maintained at an energy level sufficient to power the data transfer process between the volatile memory and a non-volatile memory. *See id.* at 8:9-24; 9:5-27. A control subsystem manages backup power and the data transfer process. *See id.* at 9:20-27. After the data transfer process is completed, power is removed from the memory arrays and the data protection system is deactivated. *Id.* Horning describes the power supply and reserve power supply for the data protection system as having “sufficient capacity” to power the control subsystem, non-volatile memory, and volatile memory, and can be any circuit “well known in the art” recognized as suitable by persons having ordinary skill in the art. *See id.* at 12:1-11.

113. Annotated Figure 1 of Horning below, illustrates the **control subsystem**, **power subsystem**, **volatile memory**, and **non-volatile memory**.

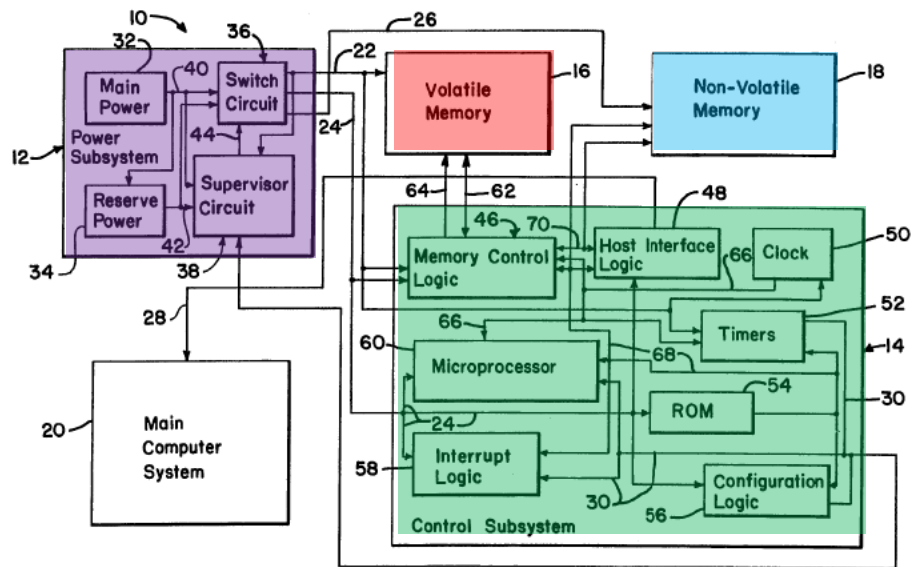


FIG. 1

E. Stokes Discloses a Super Capacitor-Based Backup Power System for a Nonvolatile Realtime Clock Calendar Module

114. Stokes is directed towards a circuit module that utilizes a super capacitor to maintain power to a nonvolatile memory in the event of power loss. *See* Ex-1013 at Abstract; 2:57-3:27. As Stokes explains, in the event of a power loss, there is a need for a backup power source to non-volatile memory that can maintain data without degradation for periods up to and exceeding 12 hours without the use of a backup battery. *See id.* at 2:27-36.

115. To meet this need, Stokes discloses a “super capacitor” in the form of

a “Double Layer Capacitor (DLC).” *Id.* at 2:57-3:27. These super capacitors offer the advantage of reduced physical volume and cost per farad of capacitance. *Id.* at 3:7-10. Stokes explains that super capacitors are also quickly rechargeable, upon restoration of the primary power source. *See id.* at 4:28-32.

X. THE PRIOR ART RENDERS ALL OF THE CLAIMED ELEMENTS OF THE '939 PATENT OBVIOUS

A. Claims 1-3 Are Rendered Obvious by Horning in View of Stokes

116. It is my opinion that Horning in view of Stokes teaches, and therefore renders obvious, every element of claims 1-3 of the '939 patent. In particular, a POSITA would have been motivated to combine the intelligent data protection system disclosed in Horning, which comprises a reserve power supply, with the super capacitors disclosed in Stokes to provide more reserve power in a more compact form factor.

117. Both Horning and Stokes recognize significant drawbacks and issues with reserve power supplies, such as batteries, in data preservation systems. For example, Horning teaches that a “major drawback” in reserve power supplies utilizing batteries is that they the batteries are readily exhausted. Ex-1008 at 2:13-18. The use of larger batteries also leads to additional drawbacks, such as the use of “large capacity battery chargers and associated components, which increase the overall costs, complexities, and sizes” of data protections systems. *Id.* at 2:22-25.

Likewise, Stokes recognizes that “[f]or the past thirty years, batteries have been the weakest link in electronic system design.” Ex-1013 at 1:39-40. For example, Stokes notes that the chemical nature of batteries “in general leads to significant design problems, including corrosion, leakage, temperature limitations, poor reliability, and short life.” *Id.* at 1:40-45. Horning and Stokes thus recognize the need for improved backup power supplies to preserve data in memory systems when external power has been lost.

118. Because Horning and Stokes are in the same field, teach analogous solutions to the same issues, and have the same purpose of improving a backup power supply for data preservation systems, a POSITA would have been motivated to combine these references. In particular, a POSITA would have been motivated to incorporate Stokes’ well-known super capacitors, which enable additional power to be stored in a more compact form, into Horning’s reserve power supply to provide the benefit of a more compact and efficient reserve power supply. This motivation is provided by the references themselves. For example, Horning explicitly states that the reserve power supply may comprise “other energy storage devices” besides batteries. Ex-1008 at 11:60-64. Horning further notes that “*persons having ordinary skill in the art could easily provide a* suitable main power supply [] and *reserve power supply* [] with sufficient capacity to power the control subsystem [],

volatile memory array [], and non-volatile memory array [], depending on the configuration of the computer system.” *Id.* at 12:1-9 (emphasis added). And Stokes not only teaches the drawbacks of batteries (similar to Horning), but also teaches the benefits of super capacitors, noting their “significance” because they can be “packaged in one cubic inch, a two order of magnitude reduction in volume of prior technology.” Ex-1013 at 3:7-10. As a result, Stokes explicitly identifies the potential for using super capacitors or “Double layer Capacitor (DLC) to sustain” operation of electronic devices and memory during power outages. *Id.* at 3:11-15. The benefits provided by Stokes thus directly align with Horning’s purpose. Accordingly, a POSITA would have been motivated to combine Stokes’ super capacitors with Horning’s data protection system, as this would have allowed Horning’s data protection system to leverage the benefits of Stokes’ super-capacitors and avoid the drawbacks of batteries.

119. Design and market incentives would have also motivated a POSITA to combine these references. As noted above, Horning teaches that larger batteries “increase the overall costs” of a data protection system, in addition to its size. Ex-1008 at 2:22-25. In contrast, Stokes makes clear that super-capacitors provide “reasonable cost” while reducing the volume of reserve storage by two orders of magnitude. Ex-1013 at 3:7-10. Accordingly, design and market incentives such as

reduced size and a lower or reasonable cost would have led a POSITA to combine these references.

120. Including Stokes' capacitors in Horning's data protection system would have also been straightforward, led to predictable results, and required minimal modification. Both Stokes and Horning recognize the benefits of having a reserve power system in a small form factor and as noted above, Stokes explains that super capacitors can be "packaged in one cubic inch, a two order of magnitude reduction in volume of prior technology." Ex-1013 at 3:7-10. Accordingly, incorporating Stokes' super capacitors, with a smaller form factor, into Horning's data protection system, would have involved minimal changes.

121. A POSITA would have also had every expectation of success in incorporating super capacitors into Horning's data protection system, as Stokes demonstrates that super capacitors were already well-known for use in reserve power systems for preserving data in volatile memory when external power has been lost. Ex-1013 at 2:57-3:61. Likewise, given the smaller form factor for super-capacitors, a POSITA would have understood that no significant changes would have been required to use a super capacitor in place of another type of reserve power supply.

122. Accordingly, it is my opinion that a POSITA would have applied combined Stokes' super capacitors in Horning's data preservation system, which

teaches a reserve power supply, to improve the functionality of the system. As a result, it is my opinion that it would have been obvious to a POSITA to combine Horning with Stokes.

1. Claim 1 Is Rendered Obvious by Horning in View of Stokes

123. As explained below, it is my opinion that Horning in view of Stokes teaches, and therefore renders obvious, every element of claim 1.

a. [Claim 1 Pre]: “A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:”

124. To the extent the preamble is limiting, it is my opinion that Horning discloses this claim element. Horning is directed to a data protection system and methods that uses different levels of reserve power to preserve data in volatile memory in the event of a power failure. *See* Ex-1008, Abstract (“The data protection system also includes data transfer apparatus to transfer data from the volatile memory into a non-volatile memory upon command from the control apparatus.”); *id.* at 5:1-8 (describing a method of intelligent data protection).

125. To achieve this, Horning discloses a control subsystem (including a memory control logic, a host interface logic, and a microprocessor), a volatile memory, and a non-volatile memory. *Id.* at Figure 1; 5:51-6:60; Abstract. In the event of a power loss, the control subsystem will transfer the data from the volatile

memory array to the non-volatile memory array. *Id.* at 9:20-28. Thus, in my opinion, Horning's control subsystem is a "processor or similar structure for directing the transfer and storage of data in memory" under Petitioners' proposed construction. Accordingly, Horning's control subsystem, volatile memory, and non-volatile memory, comprise a computing engine—i.e., "a processor or similar structure for directing the transfer and storage of data in memory, volatile memory, and non-volatile memory"—pursuant to Petitioner's proposed construction of this term.

126. Annotated Figure 1 of Horning, shown below, illustrates the **control subsystem**, **volatile memory**, and **non-volatile memory**.

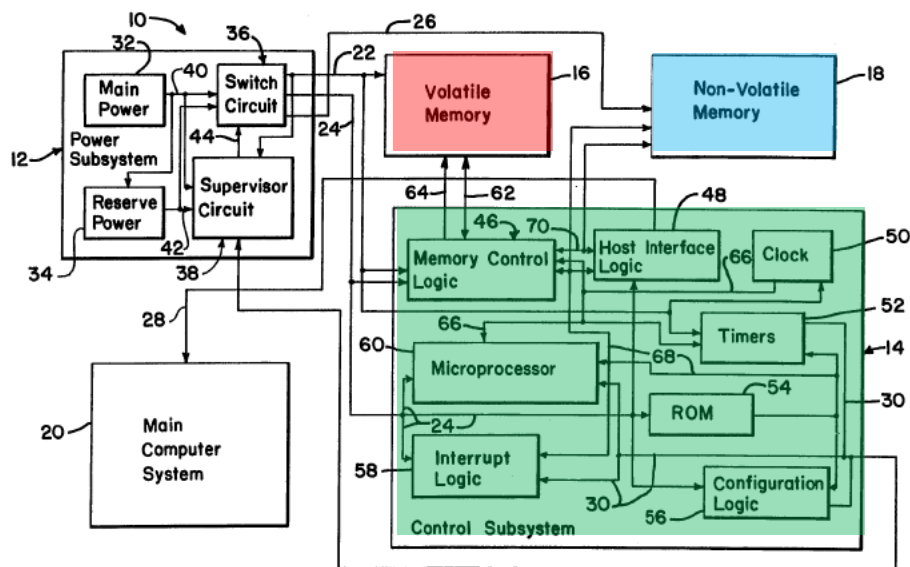


FIG. 1

127. For at least these reasons, it is my opinion that Horning discloses "[a] method for controlling data in a computer system when the computer system loses

power, the computer system comprising a computing engine.”

b. [Claim 1a]: “activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;”

128. Horning in view of Stokes renders this claim element obvious. Horning discloses a power subsystem that includes main power and reserve power components. Ex-1008, Figure 1; 6:9-37. Upon interruption of power to the main power supply component, the reserve power supply component is connected to maintain power to the memory arrays and prevent data loss. *See id.* at 6:27-37; 8:25-33; Abstract. As a result, Horning discloses activating a reserve power to supply to supply power upon power being removed from the computer system.

129. While Horning describes an embodiment in which the reserve power supply comprises batteries, *see, e.g., id.* at 13:16-25, it also states that “persons having ordinary skill in the art could easily provide a suitable main power supply [] and reserve power supply [] with sufficient capacity to power the control subsystem [], volatile memory array [], and non-volatile memory array [], depending on the configuration of the computer system.” *Id.* at 12:1-9; *see also id.* at 11:60-63 (stating that the reserve power supply may comprise “other energy storage devices”). A POSITA would thus readily understand that such a reserve power supply could include super capacitors.

130. For example, Stokes teaches a circuit module that utilizes a super capacitor to maintain power to a nonvolatile memory in the event of power loss. *See* Ex-1013 at Abstract; 2:57-3:27. In particular, Stokes discloses a “super capacitor” in the form of a “Double Layer Capacitor (DLC).” *Id.* As Stokes explains, these super capacitors offer the advantage of reduced physical volume and cost per farad of capacitance. *Id.* at 3:7-10. Super capacitors are also quickly rechargeable, upon restoration of the primary power source. *See id.* at 4:28-32. In addition, Stokes discloses that multiple DLCs—i.e., a plurality of DLCs—can be used to power a nonvolatile memory. *See id.* at 3:15-24.

131. As explained above, it is my opinion that it would have been obvious to a POSITA to combine Horning with Stokes, including using a plurality of super capacitors as described by Stokes in the power subsystem of Horning in order to benefit from these stated advantages. *Supra* § X.A. For at least these reasons, it is my opinion that Horning in view of Stokes renders obvious “activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system.”

c. [Claim 1b]: “reconfiguring the data in the computing engine;”

132. It is my opinion that Horning discloses this claim element. Horning discloses that, in the event of prolonged external power loss, the data stored in the

volatile memory array is transferred to the non-volatile memory array. Ex-1008 at Abstract (“The data protection system also includes data transfer apparatus to transfer data from the volatile memory into a non-volatile memory upon command from the control apparatus”); 7:19-23 (“... the data protection system [] will begin transferring data from the volatile memory array [] to the non-volatile memory array [] while there is still enough power in the reserve power supply [] to accomplish this data transfer.”); 9:20-24 (“... the control subsystem 14 will now immediately begin transferring data from the volatile memory array 16 to the non-volatile memory array 18.”); 11:9-17 (“If the power control sequence is in power sequence ... the microprocessor ... will begin saving the data from the volatile memory into the non-volatile memory. The program will execute this process until the save is complete ...”). This transfer of data from volatile to non-volatile memory is an example of “reconfiguring data” in the computing engine.

133. For at least these reasons, it is my opinion that Horning discloses “reconfiguring the data in the computing engine.”

- d. **[Claim 1c]: “deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.”**

134. Horning in view of Stokes renders this claim element obvious. Horning describes user programmable power control sequences that can be tailored to

accommodate a wide variety of capacities of reserve power supplies. *See* Ex-1008 at 7:60-8:8. Horning also discloses conserving reserve power by discharging the reserve power supply only to the point where there is only enough energy to accomplish the data transfer task. *Id.* at 8:13-17. At that point, once all data has been transferred from volatile to non-volatile memory, Horning teaches that power is cut off to the computing engine by a circuit that “**removes power** from the primary, secondary, and tertiary power conductors 22, 24, and 26, respectively, thereby **deactivating the entire data protection system 10.**”⁴ *Id.* at 9:20-27 (emphasis added); *see also id.* at 7:23-27 (“After all the data has been transferred, the **reserve power supply 34 is disconnected** from all the power conductors and **the system 10 will remain in this power off state**”) (emphasis added). In this manner, Horning teaches deactivating a reserve power supply to cut off power to the computing engine upon the reserve power system discharging to a predetermined level—i.e., a level where there is only enough energy left for the data transfer.

135. Annotated Figure 1 from Horning illustrates that conductors 22, 24, and 26 are the only lines that supply power to the control subsystem. Thus, when power

⁴ The reserve power supply is part of, and thus is deactivated with, “data protection system 10.” Ex-1008, Figure 1.

is removed from conductors 22, 24, and 26, power is removed from the entire system.

136. As discussed above, it would have been obvious to a POSITA to

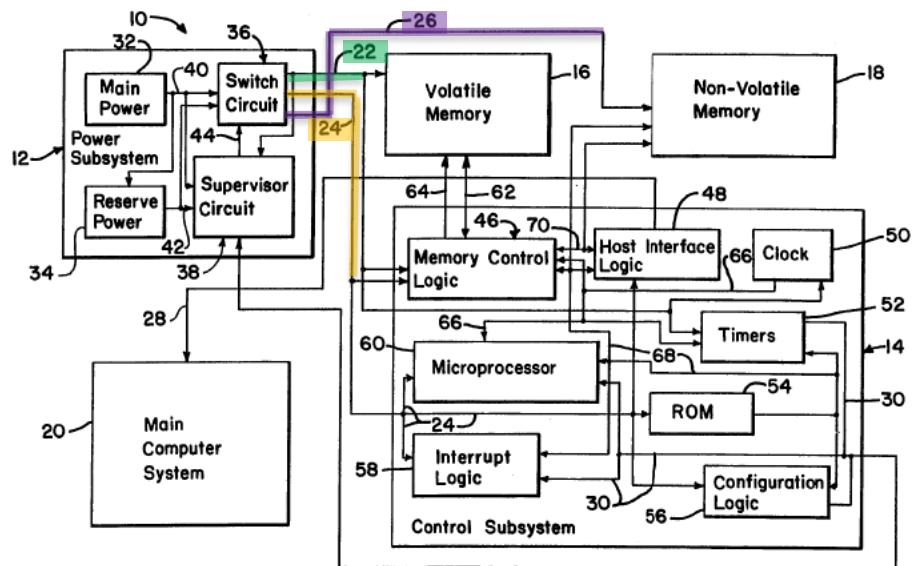


FIG. 1

combine Horning and Stokes, and to include a plurality of super capacitors as taught by Stokes in the power subsystem of Horning. *See* § X.A *supra*. As a result, it would have also been obvious to discharge the super capacitors to a predetermined level at which there is enough charge to complete the data transfer task, and then disconnect those super capacitors upon completion of data transfer, as taught by Horning.

137. For at least these reasons, it is my opinion that Horning in view of Stokes renders obvious “deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors

discharging to a predetermined level.”

2. Claim 2 Is Rendered Obvious by Horning in View of Stokes

138. As explained below, it is my opinion that Horning in view of Stokes renders obvious every element of claim 2.

- a. **[Claim 2 pre]: “The method of claim 1 wherein the computing engine comprises a least one volatile memory and at least one non-volatile memory.”**

139. It is my opinion that Horning in view of Stokes renders obvious the method of claim 1 for the reasons discussed above. *Supra* § X.A.1. It is also my opinion that Horning and Stokes render obvious the method recited in claim 2.

140. As discussed above, Horning discloses that the computing engine comprises both a volatile memory and non-volatile memory. *See supra* X.A.1.a, X.A.1.c.. Accordingly, it is my opinion that Horning in view of Stokes renders obvious the method of claim 1 “wherein the computing engine comprises a least one volatile memory and at least one non-volatile memory.”

3. Claim 3 Is Rendered Obvious by Horning in View of Stokes

141. As explained below, it is my opinion that Horning in view of Stokes renders obvious every element of claim 3.

- a. **[Claim 3]: “The method of claim 2 wherein the reconfiguring step (b) further comprises: (b1) allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory.”**

142. It is my opinion that Horning in view of Stokes renders obvious the method of claim 2 for the reasons discussed above. *Supra* § X.A.2. It is also my opinion that Horning and Stokes render obvious the method recited in claim 3.

143. Horning discloses that the data transfer task allows for all the data from the volatile memory array to be transferred to the non-volatile memory array. Ex-1008 at 7:30-34 (“If the first recovery mode is selected, the system [] will continue the data transfer process until ***all the data*** [has] been transferred into the non-volatile memory.”) (emphasis added). Horning further confirms that the power is not removed from the data protection system until after “***all the data*** [has] been transferred.” *Id.* at 9:23-27 (emphasis added).

144. Accordingly, it is my opinion that Horning in view of Stokes renders obvious the method of claim 2 wherein the reconfiguration step further comprises “allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory.”

B. Claims 1-3 Are Rendered Obvious by Germer in View of Horning Further in View of Stokes

145. It is my opinion that Germer in view of Horning **further in view of Stokes** teaches, and therefore renders obvious, every element of claims 1-3 of the '939 patent. In particular, a POSITA would have been motivated to combine the power supply and power monitor for the electric meter disclosed in Germer with the

intelligent data protection system disclosed in Horning and the super capacitors of Stokes. Furthermore, a POSITA would have been motivated to combine Horning's functionality for deactivating a reserve power supply to cut off power, within Germer's data protection system, to provide optimal utilization and management of Germer's reserve power supply. Additionally, a POSITA would have been motivated to combine the super capacitors described by Stokes into the combination of Germer and Horning in order to provide low cost-per-farad of capacitance with a reduced physical volume that is also quickly rechargeable. *See supra* § X.A.

146. Both Germer and Horning recognize the importance of preserving data in systems using volatile memory by incorporating reserve power systems to power data transfer from volatile memory to non-volatile memory when external power has been lost. Germer and Horning also recognize the need to manage the reserve power supply. For example, Germer states that it would be "unacceptable" to allow critical data, such as billing data, to be erased from a volatile RAM in the event of power loss. Ex-1007 at 2:1-9. Thus, Germer teaches a data protection system using reserve power system, in the form of capacitors, to provide a "sufficient quantity of energy" to "complete the writing of data to the non-volatile storage" when power is lost. *Id.* at 2:30-34. Once all data has been transferred and the power in the capacitors has dropped to a specific threshold at which the processor can no longer reliably

maintain its operating conditions, a reset signal is produced. *Id.* at 6:25-31. Below this threshold, a switching transistor cut off is maintained. *Id.* at 9:3-6; claim 1.

147. Similarly, Horning recognizes that replacing or reconstructing data lost from volatile memory due to a power outage can be difficult and time consuming, or even impossible. Ex-1008 at 1:46-52. Thus, Horning also teaches a data protection system that uses a reserve power supply to enable “transferring data from the volatile memory array [] to the non-volatile memory array.” *Id.* at 9:20-24; *see also id.* at 6:27-37; 8:25-33; Abstract. Horning also recognizes that allowing the reserve power system to continue providing power has drawbacks. For example, providing a large enough reserve power system to energize components for the duration of a power outage “is just not practical.” *Id.* at 3:32-35. Accordingly, once all data has been transferred to non-volatile memory, Horning’s data protection system “removes power from the primary, secondary, and tertiary power conductors 22, 24, and 26, respectively, thereby deactivating the entire data protection system 10.” *Id.* at 9:20-27. Horning teaches many advantages to such an intelligent data protection system, including optimal utilization of the reserve power supply regardless of the capacity of the reserve power supply. *Id.* at 8:6-8; 8:19-24.

148. Thus, because Germer and Horning are in the same field, teach analogous solutions to the same issues, and have the same purpose of improving data

protection and preservation systems, it is my opinion that a POSITA would have been motivated to combine these references. The motivation to combine is provided by the reference themselves. For example, as noted above, Germer teaches that, once reserve power has dropped below the level where the processor can properly function, a reset signal is produced and a switching transistor “*cut off*” is maintained. Ex-1007 at 6:25-31; 9:3-6; claim 1. Likewise, Horning teaches that teaches that power is cut off to the computing engine by a circuit that “*removes power* from the primary, secondary, and tertiary power conductors 22, 24, and 26, respectively, thereby *deactivating the entire data protection system 10.*” Ex-1008 at 9:20-27 (emphasis added); *see also id.* at 7:23-27 (“After all the data has been transferred, the *reserve power supply 34 is disconnected* from all the power conductors and *the system 10 will remain in this power off state*”) (emphasis added). Accordingly, the power optimization benefits taught by Horning directly align with Germer’s purpose. As a result, a POSITA would have been motivated to combine Germer’s data protection system with Horning’s teaching of deactivating and cutting off power from a reserve power system, as this would have allowed Germer’s data protection system to leverage the benefits of Horning’s power optimization and utilization scheme.

149. Including Horning’s functionality for deactivating a reserve power

supply to cut off power, within Germer's data protection system, would have also been straightforward, led to predictable results, and required minimal modification. Both Germer and Horning recognize the drawbacks of using a reserve power system below a minimum threshold, and discuss components, such as switches, transistors and circuits, that could accomplish this function. Ex-1007 at 6:25-31; Ex-1008 at 9:20-27. Accordingly, incorporating Horning's teachings regarding deactivating the reserve power supply, into Germer's data protection system, would have involved minimal changes. Likewise, incorporating a plurality of Stokes' super capacitors into the combination of Germer and Horning would have involved minimal changes, as it would have been a direct substitution of a plurality of Stokes' super capacitors for the plurality of capacitors in Germer.

150. A POSITA would have also had an expectation of success in incorporating Horning's functionality for deactivating the reserve power supply to cut off power into Germer's data protection system. As Germer teaches, a processor would need to be reset once power falls below a predetermined level, and Horning demonstrates the benefits of deactivating a capacitor to cut off power at such a level. Accordingly, a POSITA would have understood that incorporating Horning's teaching of deactivation into Germer's data preservation system would have been simple and yielded expected results. Similarly, substituting a plurality of Stokes'

super capacitors into the combination of Germer and Horning would be a simple substitution and yield the expected results of higher capacitance at a reduced physical volume.

151. As a result, it is my opinion that the combined teachings of these references, the knowledge, creativity, and common sense of a POSITA, and the nature of the problem to be solved as a whole would have led a POSITA to the claimed combination and would have indicated a reasonable likelihood of success in making the above-referenced combination.

1. Claim 1 Is Rendered Obvious by Germer in View of Horning Further in View of Stokes

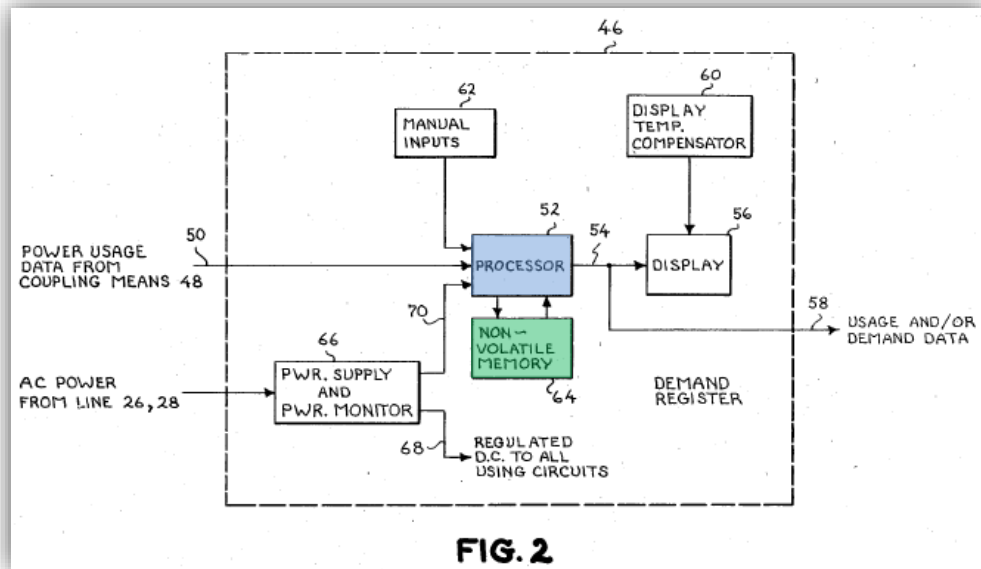
152. As explained below, it is my opinion that Germer in view of Horning further in view of Stokes teaches, and therefore renders obvious, every element of claim 1.

- a. [Claim 1 Pre]: “A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:”**

153. To the extent the preamble is limiting, it is my opinion that Germer discloses this claim element. Germer is directed to an electronic register that saves data when a computer system loses power, together with methods for using the same. Ex-1007 at 2:18-4; 2:66-3:16; claim 15 (“A method for controlling and electronic

register . . .”). To achieve this, Germer discloses a computing engine that comprises a processor, which contains volatile random access memory, and non-volatile memory. *Id.* at Abstract; 2:55-60; 3:7-13; 5:6-9 (noting that the processor “employs volatile random access memory elements which lose any data stored in them in the event of a power outage”); 5:12-15 (noting that non-volatile memory “is well known for use with [a] processor”); 5:64-6:3 (explaining that data is transferred from “the volatile random access . . . to safe storage in non-volatile memory” in the event of a power outage). In the event of a power outage, the processor controls the transfer of data from the volatile memory to the non-volatile memory. *Id.* at 5:50-57. In my opinion, Germer’s processor is a “processor or similar structure for directing the transfer and storage of data in memory” under Petitioners’ proposed construction. Thus, Germer’s processor, volatile memory, and non-volatile memory, comprise a computing engine—i.e. “a processor or similar structure for directing the transfer and storage of data in memory, volatile memory, and non-volatile memory”—pursuant to Petitioner’s proposed construction of this term

154. Annotated Figure 2 of Germer, shown below, illustrates the **processor**, which comprises volatile memory, as well as **non-volatile memory**:



155. For at least these reasons, it is my opinion that Germer renders obvious “[a] method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine.”

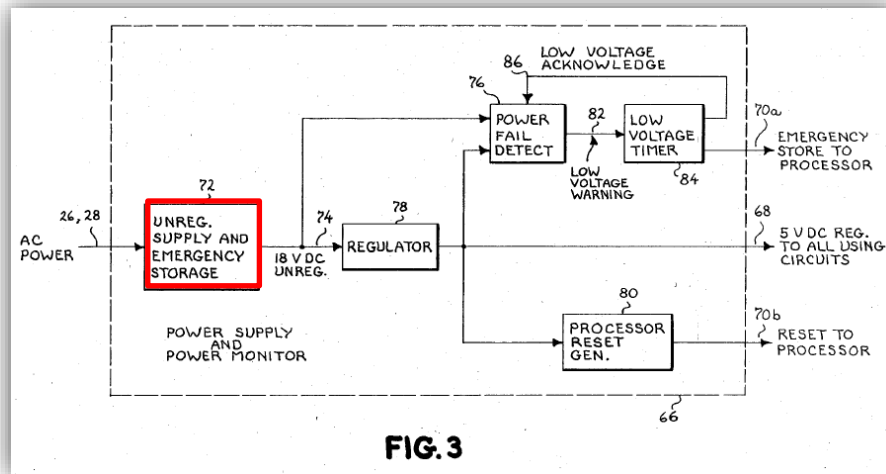
- b. **[Claim 1a]: “activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;”**

156. It is my opinion that Germer renders this claim element obvious in view of Stokes. Germer discloses an “unregulated supply and emergency storage” component, which comprises a capacitor for storing power. Ex-1007 at Abstract; 2:30-34; 7:41-55. Germer further claims an electronic register that “includes *a* capacitor having a capacitance.” *Id.* at claim 3. As noted above, I have been informed that use of the indefinite article “a” in a patent claim means “one or more.”

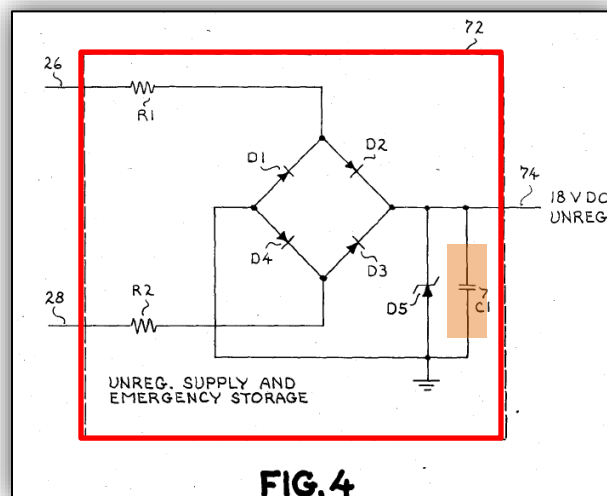
As a result, it is my opinion that, by claiming “*a* capacitor,” Germer discloses “one or more”—i.e., a plurality—of capacitors.

157. Germer also discloses that, in the event of a power outage, the capacitor is activated to “maintain power to critical circuits” for long enough “to permit transfer of billing data and programmed constants from the volatile random access memory . . . to safe storage in non-volatile memory.” *Id.* at 5:64-6:3; *see also id.* at 6:18-31 (noting that “[t]he energy stored in unregulated supply and emergency storage 72 is sufficient to maintain operation of all functions in demand register” and ensure that “all data is safely stored in non-volatile memory 62 before a reset signal may be generated”). Germer thus teaches activating the capacitors to supply power to the computing engine based upon power being removed from the computer system.

158. A diagram illustrating the unregulated supply and emergency storage structure is provided in annotated Figure 3, below:



159. A more detailed diagram of the unregulated supply and emergency storage component, illustrating a **capacitor**, is shown in annotated Figure 4, below:



160. While Germer does not refer to the capacitors as “super capacitors,” it is my opinion that the use of super-capacitors would have been obvious in view of

Stokes.⁵ At the time that the '939 patent was filed, a POSITA would have known of super-capacitors. Stokes teaches the use of super-capacitors in electronic systems more a decade before the '939 patent was filed. *Supra* § IX.E. As Stokes also teaches, super-capacitors provide more capacitance in a smaller form factor, making them very attractive as reserve power source in electronic systems. *See id.* Germer similarly teaches the importance of higher capacitance, noting that the disclosed systems must have sufficient capacitance “to feed energy to the succeeding circuits” for a period of time to preserve the data within volatile memory, “*plus* the energy required to write the data into non-volatile memory.” Ex-1007 at 7:41-45 (emphasis added). Thus, Germer expressly contemplates that the disclosed systems and methods may require “more . . . energy to safely perform their functions,” necessitating a “larger . . . value of capacitance.” *Id.* at 7:46-52. As a result, Germer explains that “[o]ne skilled in the art with the present disclosure before him *would*

⁵ I note that the '939 patent does not define a super-capacitor, nor does it differentiate a super-capacitor from a “capacitor.” Instead, the specification, simply states that “with the advent of low cost super-capacitors available in values of over 10 farads, large amounts of energy can be affordably stored in a very small space.” Ex-1001 at 3:5-10.

be fully enabled to select an appropriate value of capacitance . . . without requiring experimentation.” *Id.* at 7:52-55 (emphasis added). Accordingly, because the benefits provided by Stokes directly align with Germer’s purpose, and because Stokes and Germer are in the same field, teach analogous solutions to the same issues, and have the same purpose of improving a backup power supply for data preservation systems, a POSITA would have been motivated to combine these references. This motivation is provided by the references themselves. *See id.* (explaining that a POSITA would have known use capacitors having higher capacitance); *supra* § IX.E (teaching that super-capacitors provide the benefit of higher capacitance). A POSITA would have also had every expectation of success in incorporating super-capacitors into Germer’s data protection system, as Stokes demonstrates that super-capacitors were already well-known for use in reserve power systems that provide energy for preserving data in volatile memory. Ex-1013 at 2:57-3:61. Including Stokes’ super-capacitors in Germer’s data protection system would have also been straightforward, led to predictable results, and required minimal modification as Stokes explains that super-capacitors have a small form factor and were already known, and ideal, for use in data preservation systems. *Id.* at 2:57-3:61. Thus, replacing Germer’s capacitors with Stokes’ super-capacitors would have been obvious based on the advantages taught by Stokes and a POSITA

would have been motivated to make that replacement in order to increase the reserve power without increasing the size of the capacitor. This is particularly true, given Germer's critical function of ensuring sufficient capacity to power the computing engine, and ensure the complete transfer of data to non-volatile memory, in the event of power loss. *See, e.g., IX.E supra* (discussing characteristics of super capacitors).

161. For at least these reasons, it is my opinion that Germer in view of Stokes renders obvious "activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system."

c. [Claim 1b]: "reconfiguring the data in the computing engine;"

162. It is my opinion that Germer discloses this claim element. Germer discloses that data in the computing engine is reconfigured by transferring the data "from the volatile random access memory in processor 52 to safe storage in non-volatile memory 64." Ex-1007 at 5:64-6:3; *see also id.* at 5:49-57 (explaining that the processor "controls the transfer of data from the processor 52 to non-volatile memory 64 in the event of a power outage"); 2:59-62 (noting that the stored electric energy is "sufficient to maintain the data in the volatile data storage and to transfer the data to the non-volatile data storage in the absence of the electric power"); claim 15 (reciting a method comprising the step of "writing at least some data from said volatile data storage into said non-volatile data storage").

163. For at least these reasons, it is my opinion that Germer renders obvious “reconfiguring the data in the computing engine.”

d. [Claim 1c]: “deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.”

164. Germer in view of Horning further in view of Stokes renders this claim element obvious. Germer discloses a number of thresholds, including a specific threshold (e.g., a “third threshold”) at which the processor “is no longer able to reliably maintain its operating conditions” and a reset signal is generated. Ex-1007 at 6:25-31. For example, Germer explains that when the regulated voltage 68, the output of regulator circuit seen in Fig. 5, powering the processor decreases “from its nominal value of 5 volts to a threshold value of about 3.9 volts,” a reset to processor signal is generated. *Id.* at 9:9-13.

165. As explained above, Horning discloses a system and method of data protection that includes discharging a reserve power supply to a predetermined level at which it can supply enough power to the computing engine so that it can transfer all the data from the volatile memory array to the non-volatile memory array. *Supra* § X.A.1; Ex-1008 at 8:13-17. As Horning teaches, discharging the reserve power supply to such a level, followed by cutting off power from the reserve power supply, allows the user to obtain “optimum utilization of the reserve power supply

regardless of the capacity of the reserve power supply. *Id.* at 8:6-8; 8:19-24. Horning also discloses that, after all data has been transferred from volatile to non-volatile memory, power is cut off to the computing engine by a circuit that “**removes power** from the primary, secondary, and tertiary power conductors . . . thereby **deactivating the entire data protection system 10.**”⁶ *Id.* at 9:20-27 (emphasis added). As discussed above, it would have been obvious to a POSITA to include the teachings of Horning, including Horning’s functionality for deactivating the reserve power system, in the system and method of Germer in order to achieve the stated optimum utilization of the reserve power capacitor. As discussed above, it would have been obvious to a POSITA to replace Germer’s capacitors with Stokes’ super capacitors in order to supply sufficient reserve power from a reduced physical volume. *See supra* § X.B.

166. For at least these reasons, it is my opinion that Germer in view of Horning further in view of Stokes renders obvious “deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.”

2. Claim 2 Is Rendered Obvious by Germer in View of

⁶ The reserve power supply is part of, and thus is deactivated with, “data protection system 10.” Ex-1008, Figure 1.

Horning Further in View of Stokes

167. As explain below, it is my opinion that Germer in view of Horning further in view of Stokes renders every element of claim 2 obvious.

- a. **[Claim 2 pre]: “The method of claim 1 wherein the computing engine comprises a least one volatile memory and at least one non-volatile memory.”**

168. It is my opinion that Germer in view of Horning further in view of Stokes renders obvious the method of claim 1 for the reasons discussed above. *Supra* § X.B.1.. It is also my opinion that Germer and Horning further in view of Stokes render obvious the method recited in claim 2.

169. As discussed above, Germer discloses that the computing engine comprises both a volatile memory and non-volatile memory. *See supra* §§ X.B.1.a, X.B.1.c. Accordingly, it is my opinion that Germer in view of Horning further in view of Stokes renders obvious the method of claim 1 “wherein the computing engine comprises a least one volatile memory and at least one non-volatile memory.”

3. Claim 3 Is Rendered Obvious by Germer in View of Horning Further in View of Stokes

170. As explained below, it is my opinion that Germer in view of Horning further in view of Stokes renders obvious every element of claim 3.

- a. **[Claim 3]: “The method of claim 2 wherein the reconfiguring step (b) further comprises: (b1) allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory.”**

171. It is my opinion that Germer in view of Horning further in view of Stokes renders obvious the method of claim 2 for the reasons discussed above. *Supra* § X.B.2. It is also my opinion that Germer and Horning further in view of Stokes render obvious the method recited in claim 3.

172. Germer discloses that data in the computing engine is reconfigured by transferring the data “from the volatile random access memory in processor 52 to safe storage in non-volatile memory 64.” Ex-1007 at 5:64-6:3; *see also id.* at 5:49-57 (explaining that the processor “controls the transfer of data from the processor 52 to non-volatile memory 64 in the event of a power outage”); 2:59-62 (noting that the stored electric energy is “sufficient to maintain the data in the volatile data storage and to transfer the data to the non-volatile data storage in the absence of the electric power”). Germer further confirms that the power thresholds for deactivation of the capacitors are set to ensure “that ***all data*** is safely stored in non-volatile memory.” *Id.* at 6:28-31 (emphasis added).

173. Accordingly, it is my opinion that Germer in view of Horning further in view of Stokes renders obvious the method of claim 2 wherein the reconfiguration step further comprises “allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory.”

C. Each of the Challenged Claims Is Rendered Obvious by Bruder in View of Horning Further in View of Stokes

174. It is my opinion that Bruder in view of Horning further in view of Stokes teaches, and therefore makes obvious, every element of claims 1-3, 6, 10-12, and 15 of the '939 patent. In particular, a POSITA would have been motivated to combine Horning's functionality for deactivating a reserve power supply to cut off power, within Bruder's data protection system, to provide optimal utilization and management of Bruder's reserve power supply. Furthermore, a POSITA would have been motivated to combine the super capacitors described by Stokes into the combination of Bruder and Horning in order to provide low cost-per-farad of capacitance with reduced physical volume that is also quickly rechargeable. *See supra* § X.A.

175. Both Bruder and Horning underscore the importance of conserving reserve power in a data preservation system. For example, Bruder teaches a data preservation system in which reserve power, stored in a bank of capacitors, is used to transfer data from volatile to non-volatile memory in the event of an external power failure. *See, e.g.*, Ex-1005 at 7:60-66; 8:2-10; 10:58-64. Bruder also explains that "low overall power dissipation" is important for a data preservation system because it is "necessary to have minimum size back up storage capacitors." *Id.* at 7:40-47. As a result, Bruder teaches that reserve power from capacitors should be supplied temporarily and only for "long enough to allow this transfer of data to be

accomplished.” *Id.* at 7:64-66; 10:58-64 (stating that the capacitors “supply enough power to effectuate a complete transfer of the entire contents” of volatile memory to non-volatile memory); *id.*, Abstract; 2:35-42.

176. Similarly, Horning teaches a data protection system that uses a reserve power supply to enable “transferring data from the volatile memory array [] to the non-volatile memory array” upon the loss of external power. Ex-1008 at 9:20-24; *see also id.* at 6:27-37; 8:25-33; Abstract. Horning also recognizes that failure to manage or conserve reserve power has drawbacks. *See id.* at 3:32-35. Accordingly, Horning teaches that, once all data has been transferred to non-volatile memory, Horning’s data protection system “removes power from the primary, secondary, and tertiary power conductors 22, 24, and 26, respectively, thereby deactivating the entire data protection system 10.” *Id.* at 9:20-27. Horning teaches many advantages to such an intelligent data protection system, including optimal utilization of the reserve power supply regardless of the capacity of the reserve power supply. *Id.* at 8:6-8; 8:19-24.

177. Accordingly, because Bruder and Horning are in the same field, teach analogous solutions to the same issues, and have the purpose of improving data protection and preservation systems, it is my opinion that a POSITA would have been motivated to combine these references. The motivation to combine is provided

directly by the references. For example, as explained above, Bruder teaches that reserve power from capacitors should only be supplied for “long enough to allow this transfer of data [from volatile to non-volatile memory] to be accomplished.” Ex-1005 at 7:64-66. Likewise, Horning teaches optimizing power utilization in a reserve power system using a circuit that “**removes power** from the primary, secondary, and tertiary power conductors . . . thereby **deactivating the entire data protection system 10.**” Ex-1008 at 9:20-27 (emphasis added); *see also id.* at 7:23-27 (“After all the data has been transferred, the **reserve power supply 34 is disconnected** from all the power conductors and **the system 10 will remain in this power off state**”) (emphasis added). Accordingly, the power optimization benefits taught by Horning directly align with Bruder’s goals. As a result, a POSITA would have been motivated to combine Bruder’s data protection system with Horning’s teaching of deactivating and cutting off power from a reserve power system, as this would have allowed Bruder’s data protection system to leverage the benefits of Horning’s power optimization and utilization scheme. Furthermore, a POSITA would have been motivated to incorporate a plurality of Stokes’ super capacitors into the combination of Bruder and Horning in order to provide sufficient power at a reduced physical volume. *See supra* § X.A.

178. Including Horning’s functionality for deactivating a reserve power

supply to cut off power, within Bruder's data protection system, would have also been straightforward, led to predictable results, and required minimal modification. Both Bruder and Horning recognize that a reserve power supply should be conserved, and discuss components, such as switches, transistors and circuits, that could accomplish this function. Ex-1005 at 7:40-47; 7:64-66; Ex-1008 at 9:20-27. Accordingly, incorporating Horning's teachings regarding deactivating the reserve power supply, into Bruder's data protection system, would have involved minimal changes. Likewise, incorporating a plurality of Stokes' super capacitors into the combination of Bruder and Horning would have involved minimal changes, as it would have been a direct substitution of a plurality of Stokes' super capacitors for the plurality of capacitors in Bruder.

179. A POSITA would have also had an expectation of success in incorporating Horning's functionality for deactivating the reserve power supply to cut off power into Bruder's data preservation system. As Bruder teaches, power should only be supplied temporarily to ensure that data is transferred to non-volatile memory, and Horning demonstrates the benefits of deactivating a capacitor to cut off power at that same level. Accordingly, a POSITA would have understood that incorporating Horning's teaching of deactivation into Bruder's data preservation system would have been straightforward and yielded expected results. Similarly,

substituting a plurality of Stokes' super capacitors into the combination of Bruder and Horning would be a simple substitution and yield the expected results of higher capacitance at a reduced physical volume.

180. As a result, it is my opinion that the combined teachings of these references, the knowledge, creativity, and common sense of a POSITA, and the nature of the problem to be solved as a whole would have led a POSITA to the claimed combination and would have indicated a reasonable likelihood of success in making the above-referenced combination.

1. Claim 1 Is Rendered Obvious by Bruder in View of Horning Further in View of Stokes

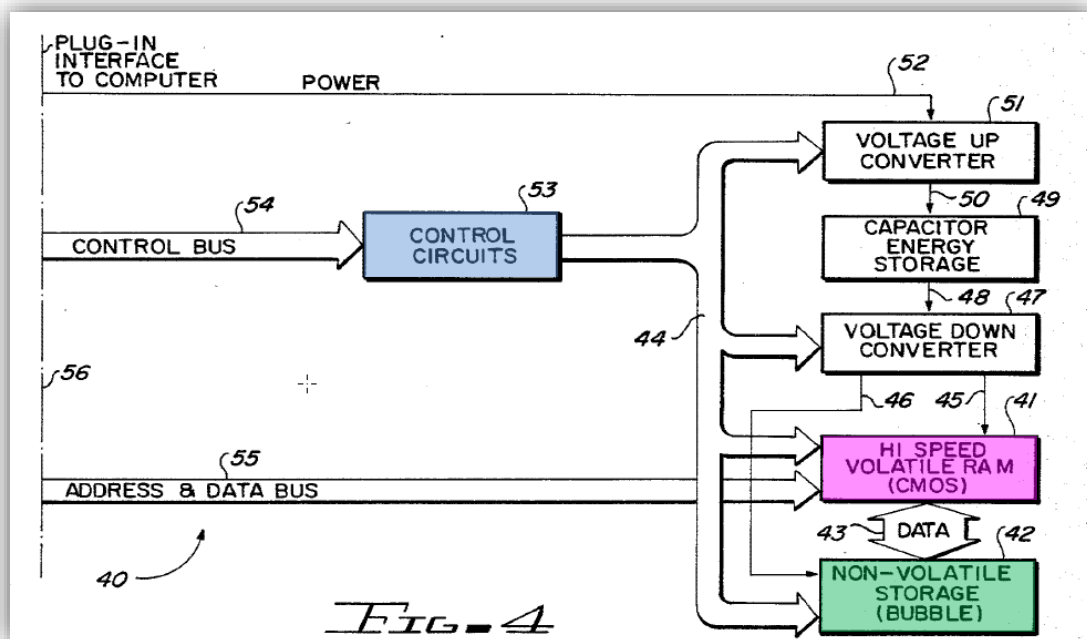
181. As explained below, it is my opinion that Bruder in combination with Horning further in view of Stokes teaches, and therefore renders obvious, every element of claim 1.

- a. [Claim 1 Pre]: “A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:”**

182. To the extent the preamble is limiting, it is my opinion that Bruder teaches this claim element. Bruder is directed to systems and methods for retaining data in a computer system when external power is interrupted. Ex-1005 at 1:8-13; *see also id.* at Abstract. To accomplish this objective, Bruder discloses a computing

engine that comprises both volatile memory (e.g., CMOS RAM) and non-volatile memory (e.g., bubble memory). *Id.* at Abstract; 2:32-42; 7:52-60; Fig. 4. Bruder also teaches control circuits, which control “data transfer between CMOS Ram 41 and bubble memory 42 during a power interruption.” *Id.* at 8:37-45. In my opinion, the “control circuits” comprise a “processor or similar structure for directing the transfer and storage of data in memory” pursuant to Petitioners’ proposed construction of computing engine.

183. The **control circuits**, **volatile memory**, and **nonvolatile memory**, which comprise the claimed “computing engine,” are illustrated in annotated Figure 4, below:



184. For at least these reasons, it is my opinion that Bruder renders obvious “a method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine.”

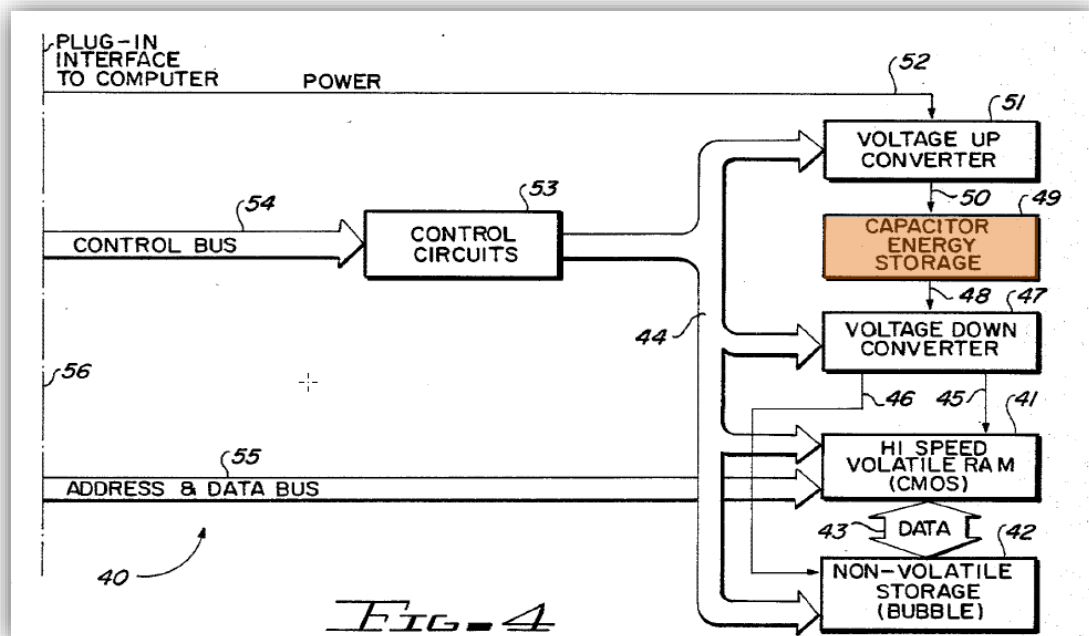
b. [Claim 1a]: “activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;”

185. It is my opinion that Bruder in view of Stokes renders this claim element obvious in view of a POSITA’s knowledge. Bruder discloses a capacitor bank (i.e., a “plurality of capacitors”) that stores and “supplies enough energy to maintain the voltage supply lines” to the memory and other circuitry when external power is interrupted. Ex-1005 at 7:60-66; Abstract (explaining that the “capacitor bank is charged to a high voltage” to provide energy when external power is interrupted); 2:35-38 (same); 8:2-7; Fig. 4.

186. Bruder also teaches activating the capacitors when external power is removed from the computer system. For example, Bruder explains that, when external power to the computing system is interrupted, “low power control circuitry actuates a voltage down converter circuit that produces a regulated output voltage” from the capacitor bank “to temporarily power the control circuitry.” *Id.* at Abstract; 8:2-10 (stating that, when power is lost, the capacitor bank “is coupled by means of conductor 48 to voltage down converter circuit 47,” which “maintains the proper

operating voltages” to ensure data transfer); 2:35-38 (“In the event of a power interruption, temporary power is supplied to the CMOS memory and to the bubble memory system, and also to a low power control circuit by means of a high voltage capacitor bank.”).

187. The **capacitor bank** is illustrated in annotated Figure 4, below.



188. While Bruder does not refer to the capacitors as “super capacitors,” it is my opinion that the use of super-capacitors would have been obvious in view of Stokes.⁷ At the time that the '939 patent was filed, a POSITA would have known of

⁷ I note that the '939 patent does not define a super-capacitor, nor does it differentiate

super-capacitors. Stokes teaches the use of super-capacitors in electronic systems more a decade before the '939 patent was filed. *Supra* § IX.E As Stokes also teaches, super-capacitors provide more capacitance in a smaller form factor, making them very attractive as reserve power source in electronic systems. *See id.* Likewise, Bruder teaches the necessity of a reserve power supply having sufficient capacitance to supply “enough energy to maintain the voltage supply lines of CMOS memory 41, bubble memory 42, and [] other circuitry . . . within a predetermined voltage range long enough to allow this transfer of data [from volatile to non-volatile memory] to be accomplished.” Ex-1005 at 7:60-66; *see also id.* at 10:54-64 (stating that backup capacitors must “supply enough power to effectuate a complete transfer of the entire contents of CMS RAM 41 to bubble memory system 42 . . . thereby making the entire memory system non-volatile, in effect”). Like Stokes, Bruder also teaches the critical importance of a small form factor, noting that reserve capacitors should “be as small as possible.” *Id.* at 3:36-44; *see also id.*, Abstract (explaining that a

a super-capacitor from a “capacitor.” Instead, the specification, simply states that “with the advent of low cost super-capacitors available in values of over 10 farads, large amounts of energy can be affordably stored in a very small space.” Ex-1001 at 3:5-10.

capacitor bank should be “relatively small” and “minimized”); 7:40-47 (noting that “it is necessary to have minimum size back up storage capacitors”). Accordingly, because the benefits provided by Stokes directly align with Bruder’s purpose, and because Stokes and Bruder are in the same field, teach analogous solutions to the same issues, and have the same purpose of improving a backup power supply for data preservation systems, a POSITA would have been motivated to combine these references. This motivation is provided by the references themselves. *See id.* at 3:36-44, 7:40-47 (describing the necessity of a small form factor for capacitors); *supra* § IX.E (teaching that super-capacitors provide a higher capacitance in a small form factor). A POSITA would have also had every expectation of success in incorporating super-capacitors into Bruder’s data protection system, as Stokes demonstrates that super-capacitors were already well-known for use in reserve power systems that provide energy for preserving data in volatile memory. Ex-1013 at 2:57-3:61. Including Stokes’ super-capacitors in Bruder’s data protection system would have also been straightforward, led to predictable results, and required minimal modification as Stokes explains that super-capacitors have a small form factor and were already known, and ideal, for use in data preservation systems. *Id.* at 2:57-3:61. Thus, replacing Bruder’s capacitor with Stokes’ super-capacitors would have been obvious based on the advantages taught by Stokes and a POSITA

would have been motivated to make that replacement in order to increase the reserve power without increasing the size of the capacitor. This is particularly true, given Bruder's critical function of ensuring sufficient capacity to power the computing engine, and ensure the complete transfer of data to non-volatile memory, in the event of power loss. *See, e.g.,* § IX.E *supra* (discussing characteristics of super capacitors).

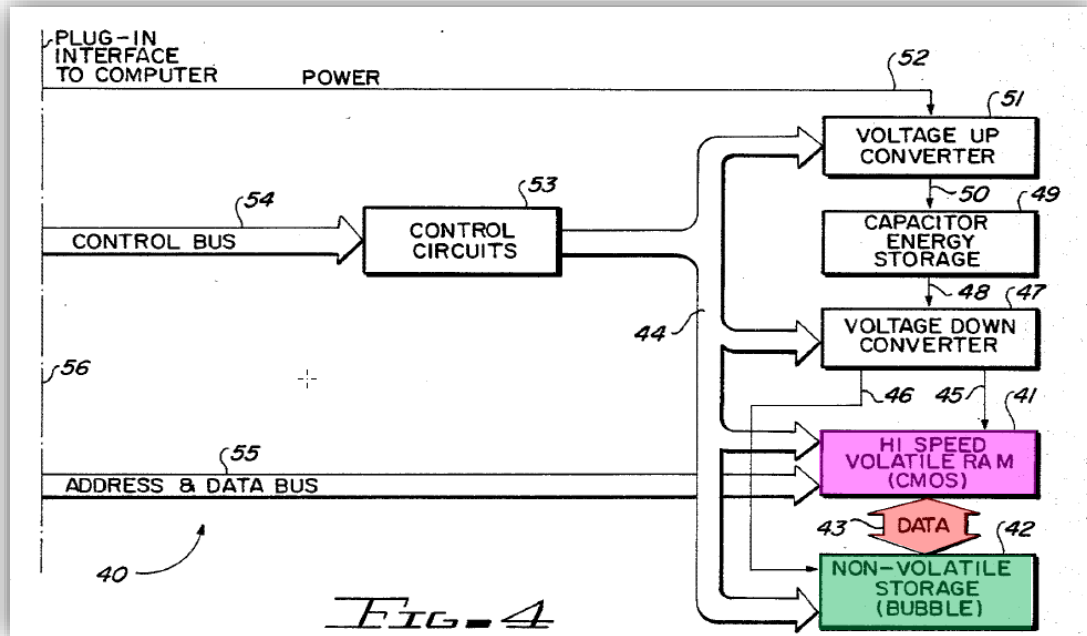
189. For at least these reasons, it is my opinion that Bruder in view of Stokes teaches “activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system.”

c. [Claim 1b]: “reconfiguring the data in the computing engine;”

190. It is my opinion that Bruder teaches this claim element. Bruder discloses that, in the event of a power failure, data is reconfigured in the computing engine by “transfer[ring] the entire contents” of volatile CMOS RAM to non-volatile bubble memory. Ex-1005 at 7:57-60; 8:2-10 (explaining that the capacitors provide sufficient power to “permit complete transfer of data in CMOS RAM 41 to bubble memory 42”); 10:58-64 (stating that the capacitor bank provides power “to effectuate a complete transfer of the entire contents of CMOS RAM 41 to bubble memory system 42 in the event of a power interruption”).

191. As discussed above, Figure 4 depicts the claimed “computing engine.” The transfer—or reconfiguration—of data from **volatile memory** to **non-volatile**

memory via a data bus is illustrated in annotated Figure 4, below:



192. For at least these reasons, it is my opinion that Bruder teaches “reconfiguring the data in the computing engine.”

- d. [Claim 1c]: “deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.”

193. It is my opinion that Bruder in combination with Horning further in view of Stokes teaches this claim element. Bruder teaches that the capacitor bank supplies power to the down converter to “temporarily power the control circuitry” while data is being transferred from volatile to non-volatile memory. Ex-1005 at Abstract; 2:35-42 (“In the event of a power interruption, temporary power is

supplied . . . by means of a high voltage capacitor bank.”); 7:64-66 (noting that the capacitors maintain voltage “long enough to allow this transfer of data to be accomplished”). By teaching that the capacitor bank is only activated “temporarily”—and only for “long enough” to affect a complete data transfer from volatile to non-volatile memory—Bruder teaches deactivating the capacitor bank.

194. Bruder also teaches the importance of regulating and minimizing the power output from the reserve power supply. For example, Bruder teaches that the capacitors maintain voltage “long enough to allow this transfer of data [from volatile to non-volatile memory] to be accomplished.” *Id.* at 7:64-66; *see also id.* at 3:40-44 (explaining that the capacitors have sufficient voltage to “allow[] a complete transfer of all data”); 8:7-10 (same); 10:58-64 (stating that the capacitors “supply enough power to effectuate a complete transfer of the entire contents” of volatile memory to non-volatile memory).

195. As explained above, Horning discloses a system and method of data protection that includes discharging a reserve power supply to a predetermined level at which it can supply enough power to the computing engine so that it can transfer all the data from the volatile memory array to the non-volatile memory array. *Supra* § X.A.1.a, X.A.1.b; *see also id.* at 8:13-17. As Horning teaches, discharging the reserve power supply to such a level, followed by cutting off power from the

reserve power supply, allows the user to obtain “optimum utilization of the reserve power supply regardless of the capacity of the reserve power supply.” *Id.* at 8:6-8; 8:19-24. Horning also discloses that, after all data has been transferred from volatile to non-volatile memory, power is cut off to the computing engine by a circuit that “**removes power** from the primary, secondary, and tertiary power conductors . . . thereby **deactivating the entire data protection system 10.**”⁸ *Id.* at 9:20-27 (emphasis added). Moreover, as discussed above, it would have been obvious to a POSITA to include the teachings of Horning, including Horning’s functionality for deactivating the reserve power system, in Bruder’s data protection system in order to achieve the stated optimum utilization of the reserve power capacitor. *Supra* § X.C. As discussed above, it would have been obvious to a POSITA to replace Bruder’s capacitors with a plurality of Stokes’ super capacitors in order to supply sufficient reserve power from a reduced physical volume. *See supra* §§ X.C.

196. For at least these reasons, it is my opinion that Bruder in combination with Horning further in view of Stokes teaches, and therefore renders obvious “deactivating the plurality of super capacitors to cut off power to the computing

⁸ The reserve power supply is part of, and thus is deactivated with, “data protection system 10.” Ex-1008, Figure 1.

engine based upon the plurality of super capacitors discharging to a predetermined level.”

2. Claim 2 Is Rendered Obvious by Bruder in View of Horning Further in View of Stokes

197. As explained below, it is my opinion that Bruder in view of Horning further in view of Stokes teaches, and therefore renders obvious, every element of claim 2.

a. [Claim 2]: “The method of claim 1 wherein the computing engine comprises a least one volatile memory and at least one non-volatile memory.”

198. It is my opinion that Bruder in view of Horning further in view of Stokes renders obvious the method of claim 1 for the reasons discussed above. *Supra* § X.C.1. It is also my opinion that Bruder and Horning render obvious the method recited in claim 2.

199. As discussed above, Bruder teaches that the computing engine comprises at least one volatile memory (e.g., CMOS RAM) and at least one non-volatile memory (e.g., bubble memory). *See supra* §§ X.C.1.a, X.C.1.c. Accordingly, it is my opinion that Bruder in view of Horning renders obvious the method of claim 1 “wherein the computing engine comprises a least one volatile memory and at least one non-volatile memory,” as recited in claim 2.

3. Claim 3 Is Rendered Obvious by Bruder in View of

Horning Further in View of Stokes

200. As explained below, it is my opinion that Bruder in view of Horning further in view of Stokes teaches, and therefore renders obvious, every element of claim 3.

- a. **[Claim 3]: “The method of claim 2 wherein the reconfiguring step (b) further comprises: (b1) allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory.”**

201. It is my opinion that Bruder in view of Horning further in view of Stokes renders obvious the method of claim 2 for the reasons discussed above. *Supra* § X.C.2. It is also my opinion that Bruder and Horning further in view of Stokes render obvious the method recited in claim 3.

202. Bruder teaches that “the entire contents” of volatile CMOS RAM is transferred to non-volatile bubble memory in the event of a power failure. Ex-1005 at 7:57-60; 8:2-10 (disclosing a “*complete transfer of data*” from volatile CMOS RAM to non-volatile bubble memory” upon a power failure) (emphasis added); 10:58-64 (same). Accordingly, it is my opinion that Bruder in view of Horning further in view of Stokes renders obvious the method of claim 2 wherein the reconfiguring step further comprises “allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory.”

4. Claim 6 Is Rendered Obvious by Bruder in View of

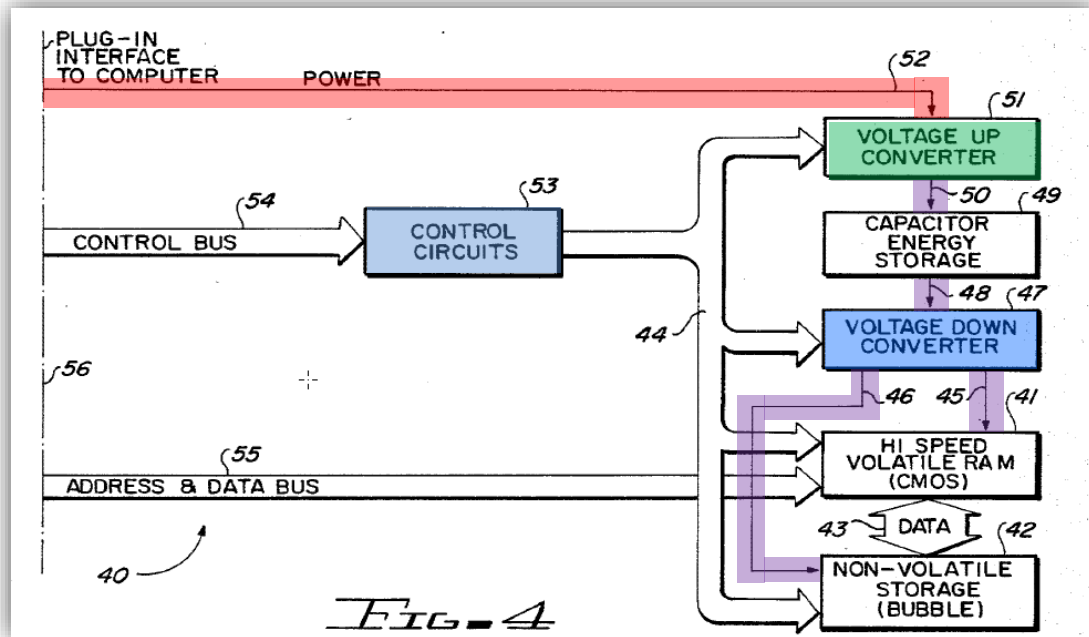
Horning Further in View of Stokes

203. As explained below, it is my opinion that Bruder in view of Horning further in view of Stokes renders obvious, and therefore makes obvious, every element of claim 6.

- a. **[Claim 6a]: “The method of claim 3 wherein the activating step (a) further comprises: reversing the flow of current between the computing engine and the plurality of super capacitors; and”**

204. It is my opinion that Bruder in view of Horning further in view of Stokes renders obvious the method of claim 3 for the reasons discussed above. *Supra* § X.C.3. It is also my opinion that Bruder and Horning further in view of Stokes render obvious the method recited in claim 6.

205. As illustrated in annotated Figure 4 below, Bruder teaches a **single power bus (52)** that provides power to the **control circuits (53)**, **voltage down converter (47)**, **voltage up converter (51)**, and other components through a series of **conductors (45, 46, 48, and 50)**:



See also Ex-1005 at 7:66-8:2 (explaining that the conductors 45 and 46 supply power to the non-volatile and volatile memory, respectively, and “normally receive their operating power from the main power bus”); 8:21-24 (same).

206. Bruder further teaches that, once the capacitor bank is activated, power is “gradually discharged into a down *voltage converter* that produces a constant, regulated output voltage *to the control circuitry*, the CMOS memory, and the bubble memory system.” *Id.* at 2:35-42 (emphasis added); Abstract (confirming that the voltage down converter “produces a regulated output voltage to temporarily *power the control circuitry*”) (emphasis added). As annotated Figure 4 (above) demonstrates, there is no separate power bus to provide power from the down

converter to the control circuitry when the capacitors are activated. Accordingly, for the up converter and down converter to provide “voltage to the control circuitry” as taught in the specification, it would be obvious to a POSITA that the flow of current from the capacitors to the control circuitry would need to be reversed over power bus 52 in order to go to the control circuits. As discussed above, it would have been obvious to a POSITA to replace Bruder’s capacitors with a plurality of Stokes’ super capacitors in order to supply sufficient reserve power from a reduced physical volume. *See supra* § X.C.

207. For at least these reasons, it is my opinion that Bruder in view of Horning further in view of Stokes teaches “reversing the flow of current between the computing engine and the plurality of super capacitors.”

b. [Claim 6b]: “discharging current from the plurality of super capacitors to the computing engine.”

208. Bruder teaches this claim element. Specifically, Bruder teaches that, upon activation, power from the capacitors is “discharged into a down voltage converter that produces a constant, regulated output voltage to the control circuitry, the CMOS memory, and the bubble memory system.” Ex-1005 at 2:35-42; *see also id.* at Abstract (“[i]n the event of a power interruption, low power control circuitry actuates a voltage down converter circuit that produces a regulated output voltage to temporarily power the control circuitry” using the capacitor bank); 8:11-15

(explaining that energy stored in the capacitor bank is “initially at a very high voltage,” but “falls off” as current is discharged to power the transfer of data from volatile to non-volatile memory).

209. For at least these reasons, it is my opinion that Bruder in view of Horning further in view of Stokes teaches “discharging current from the plurality of super capacitors to the computing engine.”

5. Claim 10 Is Rendered Obvious by Bruder in View of Horning Further in View of Stokes

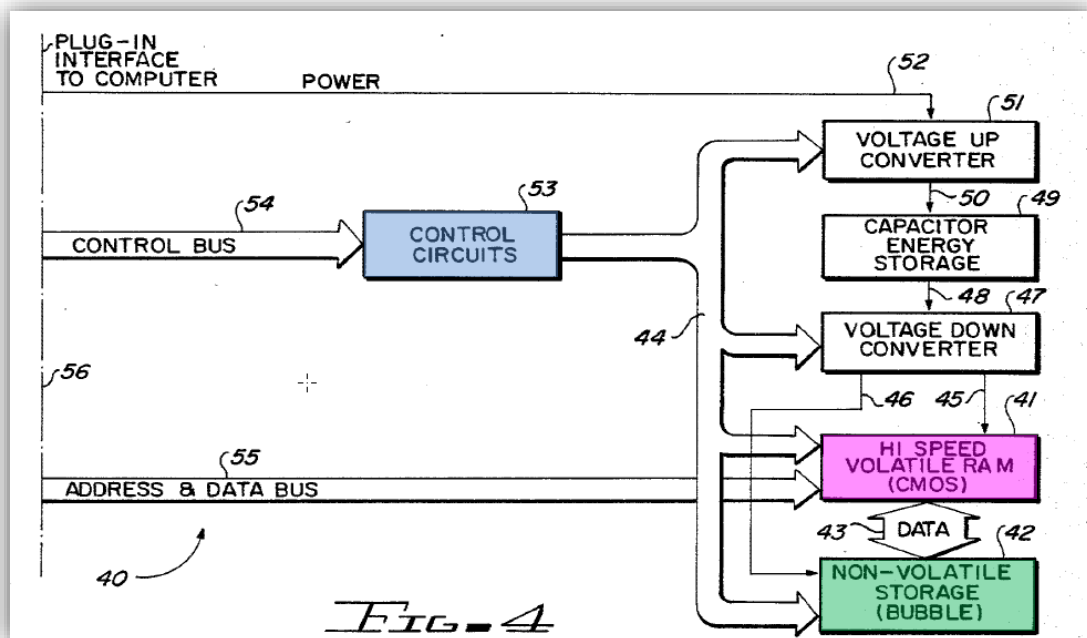
210. As explained below, it is my opinion that Bruder in view of Horning further in view of Stokes teaches, and therefore renders obvious, every element of claim 10.

- a. **[Claim 10 pre]: “A system for controlling data in a computer system when the computer system loses power, the computer system comprising a computer engine, comprising:”**

211. To the extent the preamble is limiting, it is my opinion that Bruder discloses this claim element. Bruder is directed to systems and methods for retaining data in a computer system when external power to the computer system is interrupted. Ex-1005 at 1:8-13; *see also id.* at Abstract. To accomplish this objective, Bruder discloses a computing engine that comprises both volatile memory (e.g., CMOS RAM) and non-volatile memory (e.g., bubble memory) for storing data. *Id.* at

Abstract; 2:32-42; 7:52-60; Fig. 4. Bruder also discloses control circuits, which control “data transfer between CMOS Ram 41 and bubble memory 42 during a power interruption.” *Id.* at 8:37-45. In my opinion, the “control circuits” comprise a “processor or similar structure for directing the transfer and storage of data in memory” under Petitioners’ proposed construction of “computer engine.”

212. The **control circuits**, **volatile memory**, and **nonvolatile memory** are illustrated in annotated Figure 4, below:



213. For at least these reasons, it is my opinion that Bruder in view of Horning further in view of Stokes renders obvious “a system for controlling data in a computer system when the computer system loses power, the computer system

comprising a computer engine.”

- b. **[Claim 10a]: “means for activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;”**

214. It is my opinion that Bruder renders this claim element obvious in view of Stokes. Bruder discloses a capacitor bank (i.e., a “plurality of capacitors”) that stores and “supplies enough energy to maintain the voltage supply lines” to the memory and other circuitry when external power is interrupted. Ex-1005 at 7:60-66; Abstract (explaining that a “capacitor bank is charged to a high voltage” to provide energy when external power is interrupted); *id.* at 2:35-38 (same); 8:2-7; Fig. 4. While Bruder does not refer to the capacitors as “super capacitors,” it is my opinion that the use of super-capacitors would have been obvious in view of Stokes.⁹ At the time that the ’939 patent was filed, a POSITA would have known of super-capacitors. Stokes teaches the use of super-capacitors in electronic systems more a

⁹ I note that the ’939 patent does not define a super-capacitor, nor does it differentiate a super-capacitor from a “capacitor.” Instead, the specification, simply states that “with the advent of low cost super-capacitors available in values of over 10 farads, large amounts of energy can be affordably stored in a very small space.” Ex-1001 at 3:5-10.

decade before the '939 patent was filed. *Supra* § IX.E. As taught by Stokes, a POSITA would have also known that super-capacitors provide more capacitance in a smaller form factor, making them very attractive as reserve power source in electronic systems. *See id.* Likewise, Bruder teaches the necessity of a reserve power supply having sufficient capacitance to supply “enough energy to maintain the voltage supply lines of CMOS memory 41, bubble memory 42, and [] other circuitry . . . within a predetermined voltage range long enough to allow this transfer of data [from volatile to non-volatile memory] to be accomplished.” Ex-1005 at 7:60-66; *see also id.* at 10:54-64 (stating that backup capacitors must “supply enough power to effectuate a complete transfer of the entire contents of CMS RAM 41 to bubble memory system 42 . . . thereby making the entire memory system non-volatile, in effect”). Like Stokes, Bruder also teaches the critical importance of a small form factor, noting that reserve capacitors should “be as small as possible.” *Id.* at 3:36-44; Abstract (explaining that a capacitor bank should be “relatively small” and “minimized”); 7:40-47 (noting that “it is necessary to have minimum size back up storage capacitors”). Accordingly, because the benefits provided by Stokes directly align with Bruder’s purpose, and because Stokes and Bruder are in the same field, teach analogous solutions to the same issues, and have the same purpose of improving a backup power supply for data preservation systems, a POSITA would

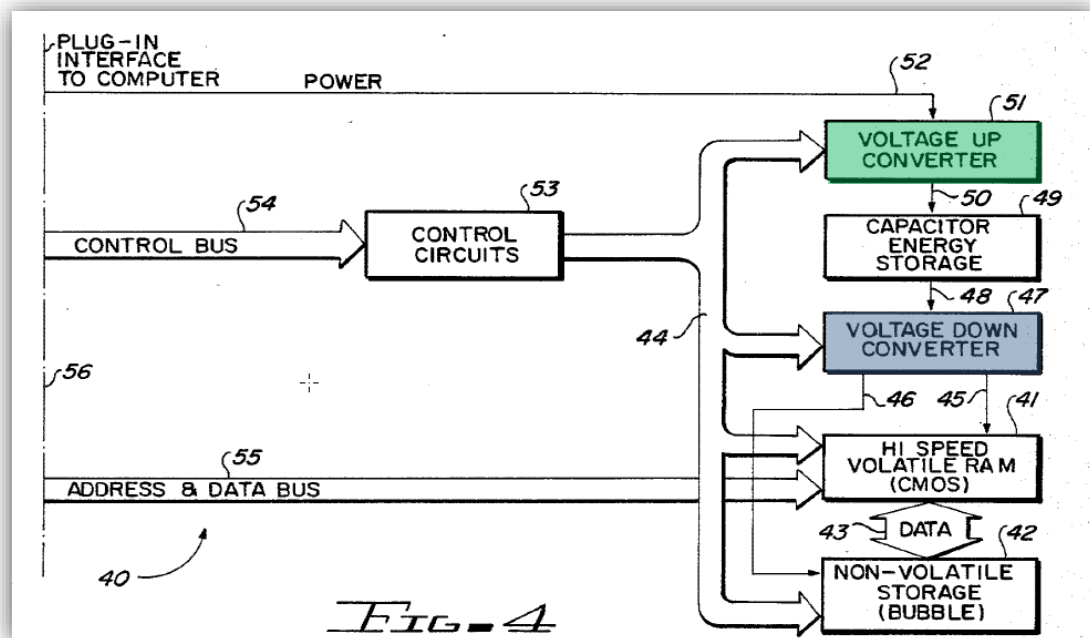
have been motivated to combine these references. This motivation is provided by the references themselves. *See id.* at 3:36-44, 7:40-47 (describing the necessity of a small form factor for capacitors); *supra* § IX.E (teaching that super-capacitors provide a higher capacitance in a small form factor). A POSITA would have also had every expectation of success in incorporating super-capacitors into Bruder's data protection system, as Stokes demonstrates that super-capacitors were already well-known for use in reserve power systems that provide energy for preserving data in volatile memory. Ex-1013 at 2:57-3:61. Including Stokes' super-capacitors in Bruder's data protection system would have also been straightforward, led to predictable results, and required minimal modification as Stokes explains that super-capacitors have a small form factor and were already known, and ideal, for use in data preservation systems. *Id.* at 2:57-3:61. Thus, replacing a capacitor with a super-capacitor would have been obvious based on the advantages taught by Stokes and a POSITA would have been motivated to make the replacement in order to increase the reserve power without increasing the size of the capacitor. This is particularly true, given Bruder's critical function of ensuring sufficient capacity to power the computing engine, and ensure the complete transfer of data to non-volatile memory, in the event of power loss. *See, e.g.,* § IX.E *supra* (discussing characteristics of super capacitors)

215. Bruder also discloses both the function and structure of the means for activating the capacitors when external power is removed from the computer system pursuant to Petitioner's proposed construction. For example, Bruder explains that, when external power to the computing system is interrupted, "low power control circuitry actuates a **voltage down converter circuit** that produces a regulated output voltage to temporarily power the control circuitry" using the capacitor bank. *Id.* at Abstract (emphasis added); *see also id.* at 8:2-10 (stating that, when power is lost, the capacitor bank "is coupled by means of conductor 48 to voltage down converter circuit 47," which "maintains the proper operating voltages" to ensure data transfer). Bruder further teaches that the down converter converts a +100 volt supply from the capacitor bank to a lower voltage supply that can be utilized by the electronic components. *Id.* at 9:35-10:5.

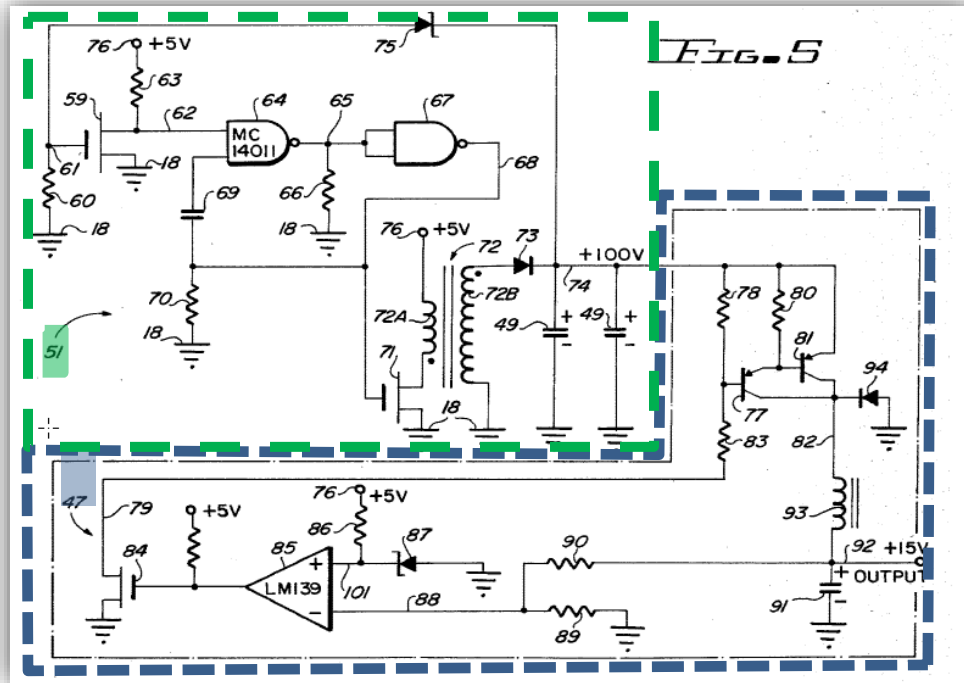
216. Similarly, Bruder discloses that a "**voltage up' converter circuit 51** boosts the normal operating voltage on main power bus 52 to produce the 100 volts needed to charge up capacitor bank 49 and thereby store enough energy in case of a power failure." *Id.* at 8:31-34; 8:37-45 ("Control circuitry 53 receives control inputs such as control and address inputs from the computer and generates the necessary signals on bus 44 to effectuate proper operation of voltage up converter circuit 51 during normal memory operation, and to also effectuate proper operation of voltage

down converter circuit 47 to achieve the desired data transfer between CMOS RAM 41 and bubble memory 42 during a power interruption.”). As a result, Bruder discloses a “down-converter 42 and up-converter 42 in Figure 1 (and corresponding text), and equivalents thereof” as well as associated circuit components under the Petitioner’s proposed construction for this means-plus-function element.

217. A general view of the **voltage down converter (47)** and **voltage up converter (51)** is illustrated in annotated Figure 4, below:



218. A more detailed diagram of voltage **down-converter (47)** and **voltage up converter (51)** is also illustrated in annotated Figure 5, below:



219. For at least these reasons, it is my opinion that Bruder discloses the “means for activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system” under the district court’s construction.

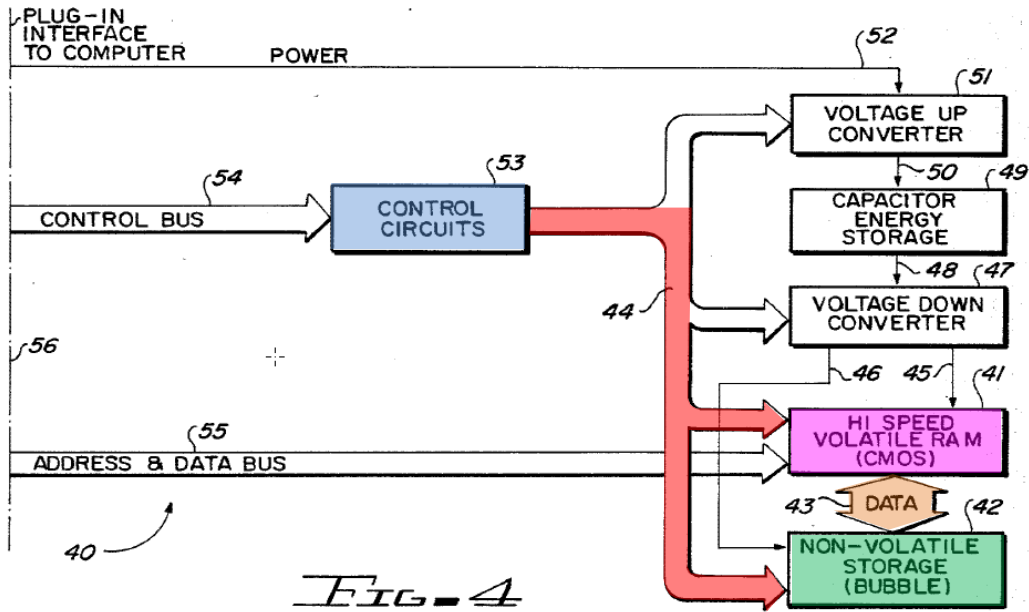
c. [Claim 10b]: “means for reconfiguring the data in the computing engine;” and

220. It is my opinion that Bruder teaches both the function and structure of this claim element. Bruder discloses that, in the event of a power failure, data is reconfigured in the computing engine by “transfer[ring] the entire contents” of volatile CMOS RAM to non-volatile bubble memory. Ex-1005 at 7:57-60; *see also id.* at 8:2-10 (explaining that the capacitors provide sufficient power to “permit

complete transfer of data in CMOS RAM 41 to bubble memory 42”); 10:58-64 (stating that the capacitor bank provides power “to effectuate a complete transfer of the entire contents of CMOS RAM 41 to bubble memory system 42 in the event of a power interruption”).

221. Bruder also discloses that “[c]ontrol circuitry . . . generates the necessary signals on bus 44 to . . . achieve the desired data transfer” from volatile memory to nonvolatile memory. *Id.* at 8:37-45; *see also id.* at Abstract (noting that the temporary power supply “power[s] the control circuitry while the CMOS-RAM is being transferred to the bubble memory”); 10:54-64 (explaining that the control circuitry effectuates a transfer of data from volatile to non-volatile memory). As a result, Bruder’s control circuitry is a “processor or equivalent structure that directs the transfer and storage of data in memory” pursuant to Petitioners’ proposed construction for this means-plus-function element.

222. Annotated Figure 4, below, illustrates the **control signals** provided by the **control circuitry (53)**, which result in a reconfiguration or transfer of data from **volatile memory (41)** to **nonvolatile memory (42)** over a **data bus (43)**.



223. For at least these reasons, it is my opinion that Bruder teaches “means for reconfiguring the data in the computing engine” under Petitioners’ proposed construction.

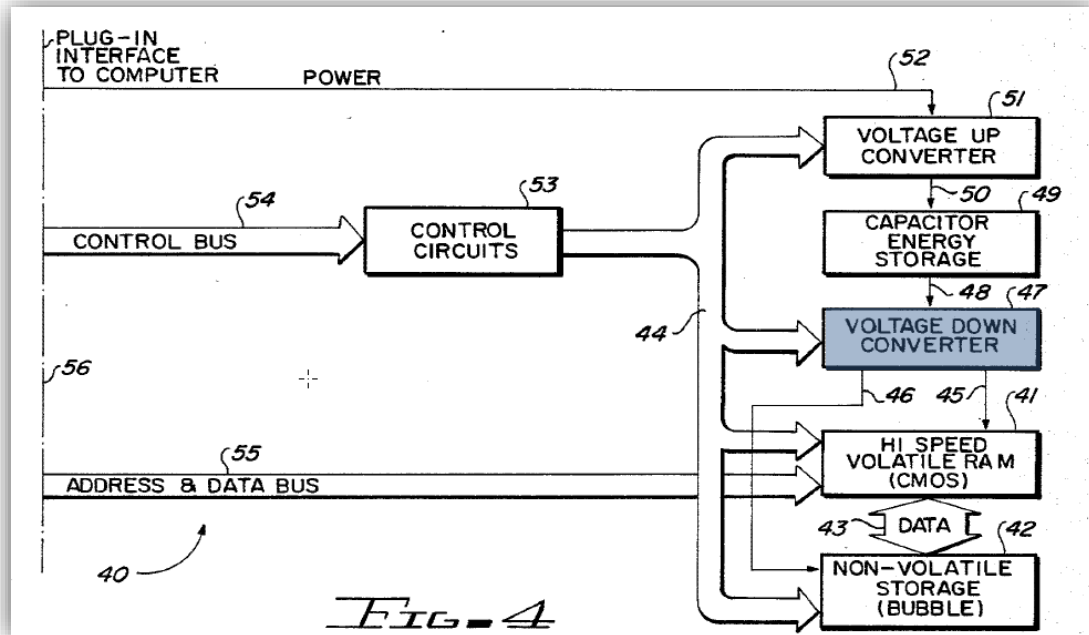
d. [Claim 10c]: “means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.”

224. It is my opinion that Bruder in view of Horning further in view of Stokes discloses this claim element by teaching both the function and structure of this means-plus-function element. Bruder teaches that the capacitor bank supplies power to the down converter to “temporarily power the control circuitry” while data is being transferred from volatile to non-volatile memory. Ex-1005 at Abstract; *see*

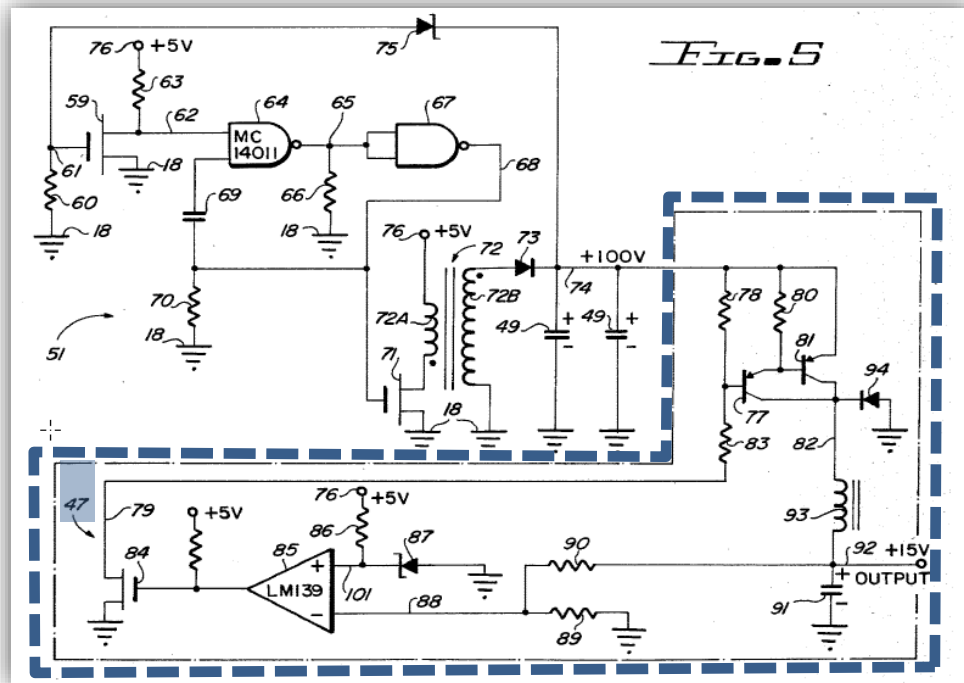
also id. at 2:35-42 (“In the event of a power interruption, temporary power is supplied . . . by means of a high voltage capacitor bank.”); 7:64-66 (noting that the capacitors maintain voltage “long enough to allow this transfer of data to be accomplished.”). By teaching that the capacitor bank is only activated “temporarily”—and only for “long enough” to affect a complete data transfer from volatile to non-volatile memory—Bruder discloses deactivating the capacitor bank.

225. Bruder also discloses the recited “means for deactivating” the capacitor bank, teaching a down converter to cut off power to the computing engine when the capacitors have discharged to a predetermined level. For example, Bruder teaches that the down converter “maintains the proper operating voltages” only for long enough to “permit complete transfer of data” from volatile to non-volatile memory. *Id.* at 8:7-10; *see also id.* at Abstract (noting that the voltage down converter uses power from the capacitors to “produce[] a regulated output voltage to temporarily power the control circuitry” while data is transferred); *id.* at 7:64-66 (explaining that voltage is supplied for “long enough to allow this transfer of data [from volatile to non-volatile memory] to be accomplished.”). Bruder thus discloses a “voltage down-converter or equivalent structure that converts a high voltage signal to a lower voltage signal” under the district court’s construction for this means-plus-function element.

226. An illustration of the voltage **down converter (47)** is provided in annotated Figure 4, below:



227. A more detailed diagram of voltage **down-converter (47)** is illustrated in annotated Figure 5, below:



228. As discussed above, Horning discloses a system and method of data protection that includes discharging a reserve power supply to a predetermined level at which it can supply enough power to the computing engine so that it can transfer all the data from the volatile memory array to the non-volatile memory array. *Supra* §§ X.A.1.a, X.A.1.c; *see also* Ex-1009 at 8:13-17. As Horning teaches, discharging the reserve power supply to such a level, followed by cutting off power from the reserve power supply, allows the user to obtain “optimum utilization of the reserve power supply regardless of the capacity of the reserve power supply. *Id.* at 8:6-8; 8:19-24. Horning also discloses that, after all data has been transferred from volatile to non-volatile memory, power is cut off to the computing engine by a circuit

that “***removes power*** from the primary, secondary, and tertiary power conductors . . . thereby ***deactivating the entire data protection system 10.***”¹⁰ *Id.* at 9:20-27 (emphasis added). As discussed above, it would have been obvious to a POSITA to include the teachings of Horning in the system and method of Bruder in order to achieve the stated optimum utilization of the reserve power capacitor in Bruder. *See* § X.C *supra*. Similarly, A POSITA at the time of invention would have been motivated to combine Bruder with the method and system for data protection of Horning in order to achieve the optimal utilization of the reserve power supply. *Id.* As discussed above, it would have been obvious to a POSITA to replace Bruder’s capacitors with a plurality of Stokes’ super capacitors in order to supply sufficient reserve power from a reduced physical volume. *See supra* § X.C.

229. For at least these reasons, it is my opinion that Bruder in view of Horning renders further in view of Stokes obvious the “means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level” under the district court’s construction.

6. Claim 11 Is Rendered Obvious by Bruder in View of

¹⁰ The reserve power supply is part of, and thus is deactivated with, “data protection system 10.” Ex-1008, Figure 1.

Horning Further in View of Stokes

230. As explained below, it is my opinion that Bruder in view of Horning further in view of Stokes teaches, and therefore makes obvious, each element of claim 11.

- a. **[Claim 11]: “The system of claim 10 wherein the computing engine comprises a least one volatile memory and at least one non-volatile memory.”**

231. It is my opinion that Bruder in view of Horning further in view of Stokes renders obvious the system of claim 10 for the reasons discussed above. *Supra* § X.C.5 It is also my opinion that Bruder and Horning further in view of Stokes render obvious the system recited in claim 11.

232. As discussed above, Bruder teaches that the computing engine comprises at least one volatile memory (e.g., CMOS RAM) and at least one non-volatile memory (e.g., bubble memory). *See supra* §§ X.C.1.a, X.C.1.c. Accordingly, it is my opinion that Bruder in view of Horning further in view of Stokes renders obvious the system of claim 10 “wherein the computing engine comprises a least one volatile memory and at least one non-volatile memory.”

7. Claim 12 Is Rendered Obvious by Bruder in View of Horning Further in View of Stokes

233. As explained below, it is my opinion that Bruder in view of Horning further in view of Stokes teaches, and therefore makes obvious, each element of

claim 12.

- a. **[Claim 12]: “The system of claim 11 wherein the reconfiguring means further comprises: means for allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory.”**

234. It is my opinion that Bruder in view of Horning further in view of Stokes renders obvious the system of claim 11 for the reasons discussed above. *Supra* § X.C.6. It is also my opinion that Bruder and Horning further in view of Stokes render obvious the system recited in claim 12.

235. Bruder teaches both the function and structure for this claim element. For example, Bruder teaches that “the entire contents” of volatile CMOS RAM are transferred to non-volatile bubble memory in the event of a power failure. Ex-1005 at 7:57-60; 8:2-10 (disclosing a “*complete transfer of data*” from volatile CMOS RAM to non-volatile bubble memory” upon a power failure) (emphasis added); 10:58-64 (same).

236. Bruder also teaches that “[c]ontrol circuitry . . . generates the necessary signals on bus 44 to . . . achieve the desired data transfer” from volatile memory to nonvolatile memory. *Id.* at 8:37-45; *see also id.* at Abstract (noting that the temporary power supply “power[s] the control circuitry while the CMOS-RAM is being transferred to the bubble memory”); 10:54-64 (explaining that the control

circuitry effectuates a transfer of data from volatile to non-volatile memory); *supra* §§ X.C.5.a, X.C.5.c. Bruder thus demonstrates that the control circuitry is a “processor or equivalent structure that directs the transfer and storage of data in memory and is configured to transfer all data from volatile to non-volatile memory” under Petitioners’ proposed construction.

237. Accordingly, it is my opinion that Bruder in view of Horning further in view of Stokes renders this claim element obvious.

8. Claim 15 Is Rendered Obvious by Bruder in View of Horning Further in View of Stokes

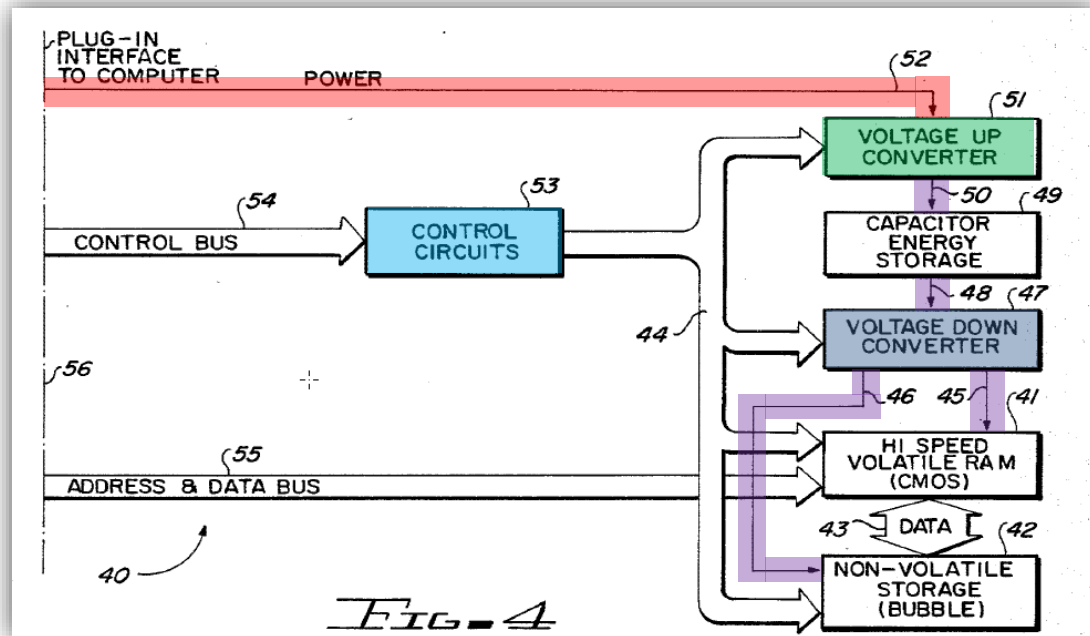
238. As explained below, it is my opinion that Bruder in view of Horning further in view of Stokes teaches, and therefore makes obvious, each element of claim 15.

- a. **[Claim 15 pre]: “The system of claim 12 wherein the activating means further comprises: means for reversing the flow of current between the computing engine and the plurality of super capacitors; and”**

239. It is my opinion that Bruder in view of Horning further in view of Stokes renders obvious the system of claim 12 for the reasons discussed above. *Supra* § X.C.7. It is also my opinion that Bruder and Horning further in view of Stokes renders obvious the system recited in claim 15.

240. As illustrated in annotated Figure 4 below, Bruder teaches a **single**

power bus (52) that provides power to the **control circuits (53)**, voltage **down converter (47)**, voltage **up converter (51)**, and other components through a series of **conductors (45, 46, 48, and 50)**:



See also Ex-1005 at 7:66-8:2 (explaining that the conductors 45 and 46 supply power to the nonvolatile and volatile memory, respectively, and “normally receive their operating power from the main power bus”); 8:21-24 (same).

241. Bruder also discloses both the function and structure of the “means for reversing the flow of current” pursuant to Petitioner’s proposed construction. For example, Bruder teaches “[a] ‘*voltage up*’ *converter circuit* 51 [that] boosts the normal operating voltage on main power bus 52 to produce the 100 volts needed to

charge up capacitor bank 49 and thereby store enough energy in case of a power failure.” *Id.* at 8:31-36; *see also, e.g., id.* at 8:37-45 (noting that “[c]ontrol circuitry 53 . . . generates the necessary signals on bus 44 to effectuate proper operation of voltage up converter circuit 51 during normal memory operation”); *id.* at 8:60-9:10 (discussing structure and operation of voltage up converter”); *id.* at 10:6-25 (same).

242. Likewise, Bruder teaches “a ***down voltage converter*** that produces a constant, regulated output voltage ***to the control circuitry***, the CMOS memory, and the bubble memory system.” *Id.* at 2:35-42 (emphasis added); *see also id.* at Abstract (confirming that the voltage down converter “produces a regulated output voltage to temporarily ***power the control circuitry***”) (emphasis added). Bruder thus discloses a “down-converter 42 and up-converter 42 in Figure 1 (and corresponding text), and equivalents thereof” under the district court’s construction.

243. That this structure reverses power is confirmed by the fact that, as annotated Figure 4 demonstrates, there is no separate power bus to provide power from the down converter to the control circuitry when the capacitors are activated. Accordingly, for the down converter to provide “voltage to the control circuitry” as disclosed in the specification, it would need to reverse the flow of current from the capacitors to the control circuitry over power bus 52 through up-converter 51.

244. Accordingly, it is my opinion that Bruder in view of Horning further in

view of Stokes renders this claim element obvious.

b. [Claim 15b]: “means for discharging current from the plurality of super capacitors to the computing engine.”

245. It is my opinion that Bruder discloses both the function and structure of this claim element. Bruder teaches that, upon activation, power from the capacitors is “discharged into a *down voltage converter that produces a constant, regulated output voltage* to the control circuitry, the CMOS memory, and the bubble memory system.” Ex-1005 at 2:35-42 (emphasis added); *see also id.* at Abstract (“[i]n the event of a power interruption, low power control circuitry actuates a voltage down converter circuit that produces a regulated output voltage to temporarily power the control circuitry” using the capacitor bank); 8:11-15 (explaining that energy stored in the capacitor bank is “initially at a very high voltage,” but “falls off” as current is discharged to power the transfer of data from volatile to non-volatile memory). Bruder thus demonstrates that the disclosed down converter is a “voltage down-converter or equivalent structure that converts a high voltage signal to a lower voltage signal and is configured to discharge current from the capacitors to the computing engine” under Petitioners’ proposed construction.

246. Accordingly, it is my opinion that Bruder in view of Horning further in view of Stokes teaches this claim element.

D. Claims 1-3 and 6 Are Rendered Obvious by Weber in View of

Horning Further in View of Stokes

247. It is my opinion that Weber in view Horning further in view of Stokes teaches, and therefore renders obvious each element of claims 1-3 and 6. In particular, a POSITA would have been motivated to combine Horning's functionality for deactivating a reserve power supply to cut off power, within Weber's data protection system, to provide optimal utilization and management of Weber's reserve power supply. Furthermore, as discussed above, it would have been obvious to a POSITA to replace Weber's capacitors with Stokes' super capacitors in order to supply sufficient reserve power from a reduced physical volume. *See, e.g., supra* § X.A.

248. Both Weber and Horning demonstrate the importance of conserving reserve power in a data preservation system. Weber teaches a data preservation system "for safeguarding disk array write operations." Ex-1006 at 1:7-9. In particular, Weber's teaches the use of high capacitance gold capacitors in a data preservation system to provide energy for "transfer[ring] data residing in the [volatile] transfer buffer to the non-volatile" memory upon a loss of power. *Id.* at 4:1-3. However, Weber acknowledges the need to conserve this power. As a result, Weber teaches that, once "the backup transfer operation has been completed" by transferring all data from volatile to non-volatile memory, the low power

processor “shuts down to conserve power.” *Id.* at 9:34-36.

249. Likewise, Horning teaches a data protection system that uses a reserve power supply to enable “transferring data from the volatile memory array [] to the non-volatile memory array” upon the loss of external power. Ex-1008 at 9:20-24; *see also id.* at 6:27-37; *id.* at 8:25-33; *id.*, Abstract. Horning also recognizes that failure to manage or conserve reserve power has drawbacks. *See id.* at 3:32-35. Accordingly, Horning teaches that, once all data has been transferred to non-volatile memory, Horning’s data protection system “removes power from the primary, secondary, and tertiary power conductors 22, 24, and 26, respectively, thereby deactivating the entire data protection system 10.” *Id.* at 9:20-27. Horning teaches many advantages to such an intelligent data protection system, including optimal utilization of the reserve power supply regardless of the capacity of the reserve power supply. *Id.* at 8:6-8; 8:19-24.

250. Thus, because Weber and Horning are in the same field, teach analogous solutions to the same issues, and have the purpose of improving data protection and preservation systems, it is my opinion that a POSITA would have been motivated to combine these references. The motivation to combine is provided by each of these references themselves. For example, as explained above, Weber teaches that as soon as the backup transfer operation has been completed” by

transferring all data from volatile to non-volatile memory, the low power processor “shuts down to *conserve power*.” Ex-1006 at 9:34-36 (emphasis added). Likewise, Horning teaches optimizing power utilization in a reserve power system using a circuit that “*removes power* from the primary, secondary, and tertiary power conductors . . . thereby *deactivating the entire data protection system 10*.” Ex-1008 at 9:20-27 (emphasis added); *see also id.* at 7:23-27 (“After all the data has been transferred, the *reserve power supply 34 is disconnected* from all the power conductors and *the system 10 will remain in this power off state*”) (emphasis added). Accordingly, the power optimization benefits taught by Horning directly align with Weber’s goals. As a result, a POSITA would have been motivated to combine Weber’s data protection system with Horning’s teaching of deactivating and cutting off power from a reserve power system, as this would have allowed Bruder’s data protection system to leverage the benefits of Horning’s power optimization and utilization scheme. Furthermore, a POSITA would have been motivated to incorporate a plurality of Stokes’ super capacitors into the combination of Weber and Horning in order to provide sufficient power at a reduced physical volume. *See, e.g., supra* § X.A.

251. Including Horning’s functionality for deactivating a reserve power supply to cut off power, within Weber’s data protection system, would have also

been straightforward, led to predictable results, and required minimal modification. Both Weber and Horning recognize that a reserve power supply should be conserved, and discuss components, such as switches, transistors and circuits, that could accomplish this function. Ex-1006 at 7:40-47, 64-66; Ex-1008 at 9:20-27. Accordingly, incorporating Horning's teachings regarding deactivating the reserve power supply, into Weber's data protection system, would have involved minimal changes. Likewise, incorporating a plurality of Stokes' super capacitors into the combination of Weber and Horning would have involved minimal changes, as it would have been a direct substitution of a plurality of Stokes' super capacitors for Weber's capacitors.

252. A POSITA would have also had an expectation of success in incorporating Horning's functionality for deactivating the reserve power supply to cut off power into Weber's data preservation system. As Weber teaches, as soon as data has been transferred to non-volatile memory, power should be conserved. Accordingly, a POSITA would have understood that incorporating Horning's teaching of deactivating a reserve power supply, into Weber's data preservation system, would have been straightforward and yielded expected results. Similarly, substituting a plurality of Stokes' super capacitors into the combination of Weber and Horning would be a simple substitution and yield the expected results of higher

capacitance at a reduced physical volume.

253. As a result, it is my opinion that the combined teachings of these references, the knowledge, creativity, and common sense of a POSITA, and the nature of the problem to be solved as a whole would have led a POSITA to the claimed combination and would have indicated a reasonable likelihood of success in making the above-referenced combinations.

1. Claim 1 Is Rendered Obvious By Weber in View of Horning Further in View of Stokes

254. As explained below, it is my opinion that Weber in view of Horning further in view of Stokes teaches, and therefore renders obvious, every element of claim 1.

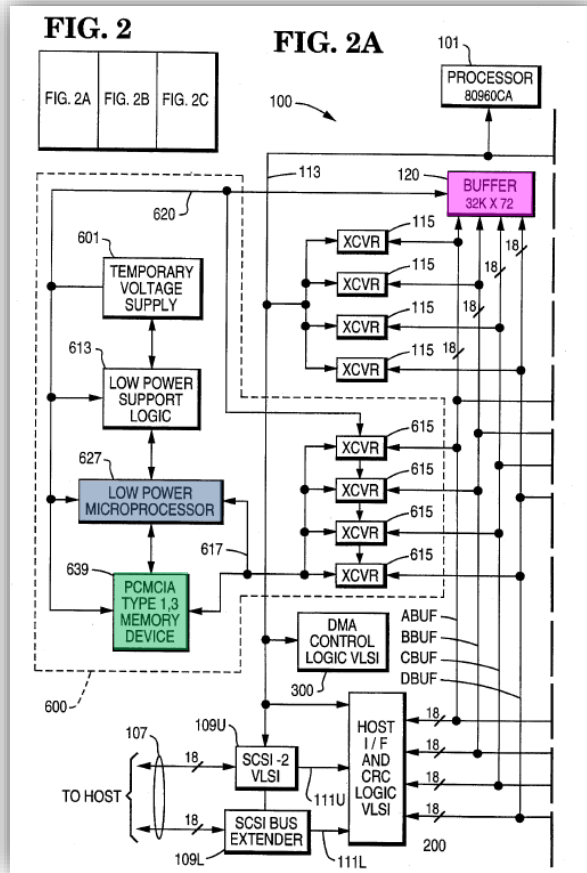
a. [Claim 1 Pre]: “A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:”

255. To the extent the preamble is limiting, it is my opinion that Weber discloses this claim element. Weber is directed to methods and systems for controlling data in a data storage or disk array storage system. Ex-1006 at Abstract; *see also id.* at 3:51-57 (same); 1:7-9 (“The present invention relates to . . . a method for safeguarding disk array write operations.”); 3:31-33 (same); claims 1-9. To achieve this goal, Weber discloses a computing engine comprising volatile memory

(e.g., transfer buffer) as well as non-volatile memory (e.g., PCMCIA flash card or disk drive). *Id.* at Abstract; 3:38-43; 4:16-20; 5:13-20; 7:5-11; 9:15-50; claims 19-20. The computing engine also comprises a low power microprocessor, which may be a “low power CMOS microcomputer” or a “complex CMOS state machine designed to perform memory transfers.” *Id.* at 4:13-16; 7:22-36; 9:25-36. The low power microprocessor “controls the transfer of data” from volatile memory to non-volatile memory. *Id.* at 7:5-8. Weber thus demonstrates that the low power microprocessor is a “processor or equivalent structure that directs the transfer and storage of data in memory and is configured to transfer all data from volatile to non-volatile memory” under Petitioners’ proposed construction.

256. As Weber explains, this system “monitor[s] the voltage provided by the primary voltage source.” *Id.* at 9:15-17. When the system detects a failure, data is transferred from volatile memory to non-volatile memory, thereby ensuring that the data is not erased. *Id.* at 9:59-63 (noting that “the present invention [provides] a method and structure for safeguarding disk array early write operations, thereby preventing the loss of data resulting from the occurrence of a power failure”).

257. The **low power microprocessor**, **volatile memory**, and **nonvolatile memory** are illustrated in annotated Figure 2A below:



258. For at least these reasons, it is my opinion that Weber discloses a “method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine.”

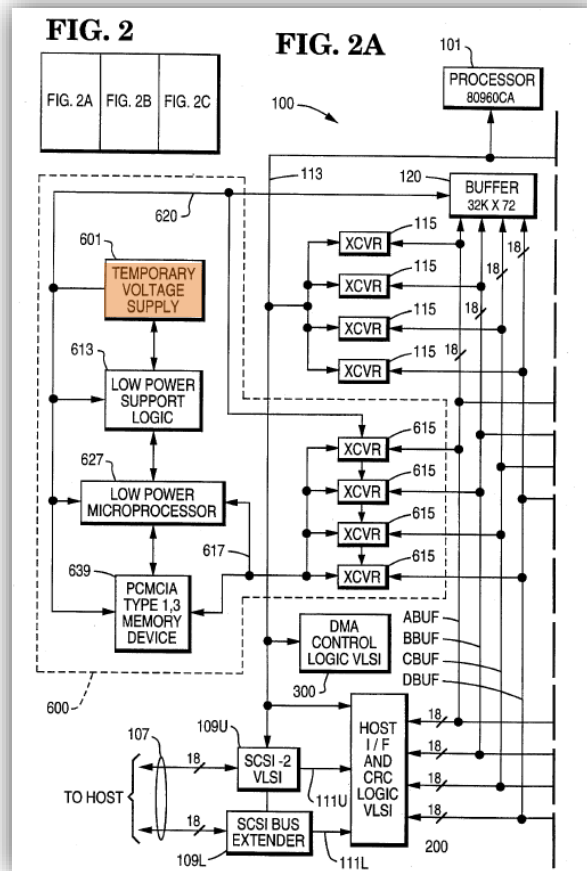
b. [Claim 1a]: “activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;”

259. It is my opinion that Weber renders this claim element obvious in view of Stokes. Weber discloses a “temporary voltage source” in the form of a “high capacitance gold capacitor,” which has “an extremely high capacitance value.” Ex-

1006 at Abstract; *see also id.* at 4:5-10; 6:65-7:2; 7:17-21. Numerous claims also recite that the temporary voltage source “comprises *a* gold capacitor for supplying power.” *See, e.g., id.* at claims 7, 10, and 26 (emphasis added.). I have been informed that use of the indefinite article “a” in a claim means “one or more.” As a result, it is my opinion that, by claiming “*a* gold capacitor,” Weber discloses a plurality of capacitors.

260. When the external voltage drops, Weber also teaches that backup logic, which includes the temporary voltage source (i.e., the capacitor), is activated to “assume control of the disk array system.” *Id.* at 9:14-25; *see also id.* at 3:24-27 (noting that the disclosed methods and structures prevent “data loss resulting from the occurrence of a power failure”); 6:65-7:2 (explaining that backup logic “includes . . . a small, temporary voltage source 601 made up of a small . . . gold capacitor”). As such, Weber teaches activating the capacitors to supply power to the computing engine based upon power being removed from the computer system.

261. The **temporary voltage supply (comprising capacitors)** is illustrated in annotated Figure 2A, below:



262. While Weber does not refer to the capacitors as “super capacitors,” it is my opinion that the use of super-capacitors would have been obvious in view of Stokes.¹¹ At the time that the ’939 patent was filed, a POSITA would have known

¹¹ I note that the ’939 patent does not define a super-capacitor, nor does it differentiate a super-capacitor from a “capacitor.” Instead, the specification, simply states that “with the advent of low cost super-capacitors available in values of over 10 farads, large amounts of energy can be affordably stored in a very small space.”

of super-capacitors. Stokes teaches the use of super-capacitors in electronic systems more a decade before the '939 patent was filed. *Supra* § IX.E. Stokes also teaches that super-capacitors provide more capacitance in a smaller form factor, making them very attractive as reserve power source in electronic systems. *See id.* Weber similarly teaches the use of capacitors “having an ***extremely high capacitance*** value.” Ex-1006 at 7:17-21 (emphasis added); *see also id.*, claims 8, 16, 27 (reciting a gold capacitor that “has a high capacitance value”). This is because the capacitor must “provide continuous power and refresh for the transfer buffer [] as well as power to the components included in backup logic.” *Id.* at 7:2-5. Moreover, Weber teaches that the capacitor must not only have “extremely high capacitance,” but also a “small” form factor. *Id.* at 4:5-10 (explaining that the disclosed systems and devices require “a small, temporary voltage source”); *see also id.* at 6:65-7:2 (same); *id.*, claims 4, 10 (reciting “a small voltage source for temporarily supplying power”). Accordingly, because the benefits provided by Stokes directly align with Weber’s purpose, and because Stokes and Weber are in the same field, teach analogous solutions to the same issues, and have the same purpose of improving a backup power supply for data preservation systems, a POSITA would have been motivated to combine these

Ex-1001 at 3:5-10.

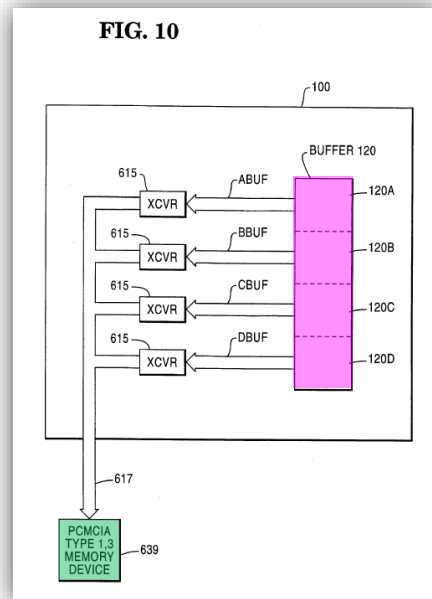
references. This motivation is provided by the references themselves. *See id.* at 6:65-7:2, 7:17-21 (describing the need for an “extremely high capacitance” capacitor with a “small” form factor); *supra* § IX.E (teaching that super-capacitors provide a higher capacitance in a small form factor). A POSITA would have also had an expectation of success in incorporating super-capacitors into Weber’s data protection system, as Stokes demonstrates that super-capacitors were already well-known for use in reserve power systems that provide energy for preserving data in volatile memory. Ex-1013 at 2:57-3:61. Including Stokes’ super-capacitors in Weber’s data protection system would have also been straightforward, led to predictable results, and required minimal modification as Stokes explains that super-capacitors have a small form factor and were already known, and ideal, for use in data preservation systems. *Id.* at 2:57-3:61. Thus, replacing a capacitor with a super-capacitor would have been obvious based on Stokes’ teachings and a POSITA would have been motivated to make such a replacement in order to increase the reserve power without increasing the size of the capacitor. This is particularly true, given Weber’s critical function of ensuring sufficient capacity to power the computing engine, and ensure the complete transfer of data to non-volatile memory, in the event of power loss. *See, e.g.,* § IX.E, *supra* (discussing characteristics of super capacitors).

263. For at least these reasons, it is my opinion that Weber in view of Stokes teaches “activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system.”

c. [Claim 1b]: “reconfiguring the data in the computing engine;”

264. It is my opinion that Weber teaches this claim element. Weber discloses that data in the computing engine is reconfigured by “transfer[ring] data residing in the [volatile] transfer buffer to the non-volatile” memory upon a loss of power. Ex-1006 at 4:1-3; *see also id.* at 3:24-27 (noting that the disclosed methods and structures prevent “data loss resulting from the occurrence of a power failure”); 3:38-43 (explaining that the invention “utilize[es] volatile memory to provide an early write completion signal” and “a low power non-volatile storage device . . . to store the contents of the volatile memory” in the event of a failure); 9:25-28 (explaining that the low power processor “initiates a transfer of data residing in transfer buffer to [non-volatile memory in the] PCMCIA device”).

265. The transfer of data from **volatile memory** (transfer buffer), through a series of data buses, to **non-volatile memory** (e.g., PCMCIA flash card or disk drive) is illustrated in annotated Figure 10, below:



266. For at least these reasons, it is my opinion that Weber teaches “reconfiguring the data in the computing engine.”

d. [Claim 1c]: “deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.”

267. It is my opinion that Weber in view of Horning further in view of Stokes teaches this claim element. Weber teaches that, once “the backup transfer operation has been completed” by transferring all data from volatile to non-volatile memory, the low power processor “shuts down to conserve power.” Ex-1006 at 9:34-36. In my opinion, the fact that the processor “shuts down to conserve power” suggests that the capacitors are deactivated to cut off power to the computing engine.

268. Nonetheless, as explained above, Horning discloses a system and

method of data protection that includes discharging a reserve power supply to a predetermined level at which it can supply enough power to the computing engine so that it can transfer all the data from the volatile memory array to the non-volatile memory array. *Supra* §§ X.A.1.a, X.A.1.b, X.A.1.c; Ex-1008 at 8:13-17. As Horning teaches, discharging the reserve power supply to such a level, followed by cutting off power from the reserve power supply, allows the user to obtain “optimum utilization of the reserve power supply regardless of the capacity of the reserve power supply. Ex-1008 at 8:6-8; 8:19-24. Horning also discloses that, after all data has been transferred from volatile to non-volatile memory, power is cut off to the computing engine by a circuit that “***removes power*** from the primary, secondary, and tertiary power conductors . . . thereby ***deactivating the entire data protection system 10.***”¹² *Id.* at 9:20-27 (emphasis added). As discussed above, it would have been obvious to a POSITA to include the teachings of Horning, including Horning’s functionality for deactivating the reserve power system, in the system and method of Weber in order to achieve the stated optimum utilization of the reserve power capacitor in Weber. Furthermore, as discussed above, it would have been obvious

¹² The reserve power supply is part of, and thus is deactivated with, “data protection system 10.” Ex-1008, Figure 1.

to a POSITA to replace Weber's capacitors with a plurality of Stokes' super capacitors in order to supply sufficient reserve power from a reduced physical volume. *See supra* § X.D.

269. For at least these reasons, it is my opinion that Weber in combination with Horning further in view of Stokes teaches "deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level."

2. Claim 2 Is Rendered Obvious By Weber in View of Horning Further in View of Stokes

270. As explained below, it is my opinion that Weber in view of Horning further in view of Stokes teaches, and therefore renders obvious, every element of claim 2.

a. [Claim 2 pre]: "The method of claim 1 wherein the computing engine comprises a least one volatile memory and at least one non-volatile memory."

271. It is my opinion that Weber in view of Horning further in view of Stokes renders obvious the method of claim 1 for the reasons discussed above. *Supra* § X.D.1. It is also my opinion that Weber and Horning further in view of Stokes renders obvious the method recited in claim 2.

272. As discussed above, Weber discloses that the computing engine comprises at least one volatile memory (e.g., transfer buffer) and one non-volatile

memory (PCMCIA memory). *See supra* §§ X.D.1.a, X.D.1.c. Accordingly, it is my opinion that Weber in view of Horning further in view of Stokes teaches the method of claim 1 “wherein the computing engine comprises a least one volatile memory and at least one non-volatile memory,” as recited in claim 2.

3. Claim 3 Is Rendered Obvious by Weber in View of Horning Further in View of Stokes

273. As explained below, it is my opinion that Weber in view of Horning further in view of Stokes teaches, and therefore renders obvious, every element of claim 3.

- a. [Claim 3]: “The method of claim 2 wherein the reconfiguring step (b) further comprises: (b1) allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory.”**

274. It is my opinion that Weber in view of Horning further in view of Stokes renders obvious the method of claim 2 for the reasons discussed above. *Supra* § X.D.2. It is also my opinion that Weber and Horning further in view of Stokes renders obvious the method recited in claim 3.

275. Weber discloses that the transfer of data from volatile to non-volatile memory “safeguard[s] disk array early write operations, thereby preventing the loss of data resulting from the occurrence of a power failure.” Ex-1006 at 9:59-63; *see also id.* at 3:24-27 (explaining the necessity of methods and structures for

“safeguarding disk array early write operations . . . to prevent the data loss resulting from the occurrence of a power failure”); Claim 1 (reciting a data storage system “for preventing the loss of data residing in said transfer buffer”). A POSITA would readily understand that in order to “prevent the loss of data” and “safeguard” all early write operations, the system disclosed in Weber would need to transfer all data from the volatile memory to the non-volatile memory.

276. As discussed above, Horning also discloses that the data transfer task allows for all the data from the volatile memory array to be transferred to the non-volatile memory array. *Supra* §§ X.A.1.a, X.A.1.b, X.A.1.c; *see also* Ex-1008 at 7:30-34 (“If the first recovery mode is selected, the system [] will continue the data transfer process until ***all the data*** [has] been transferred into the non-volatile memory.”) (emphasis added). Horning further confirms that the power is not removed from the data protection system until after “***all the data*** [has] been transferred.” Ex-1008 at 9:23-27 (emphasis added).

277. Accordingly, it is my opinion that Weber in view of Horning further in view of Stokes teaches the method of claim 2 wherein the reconfiguration step further comprises “allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory,” as recited in claim 3.

**4. Claim 6 Is Rendered Obvious by Weber in View of Horning
Further in View of Stokes**

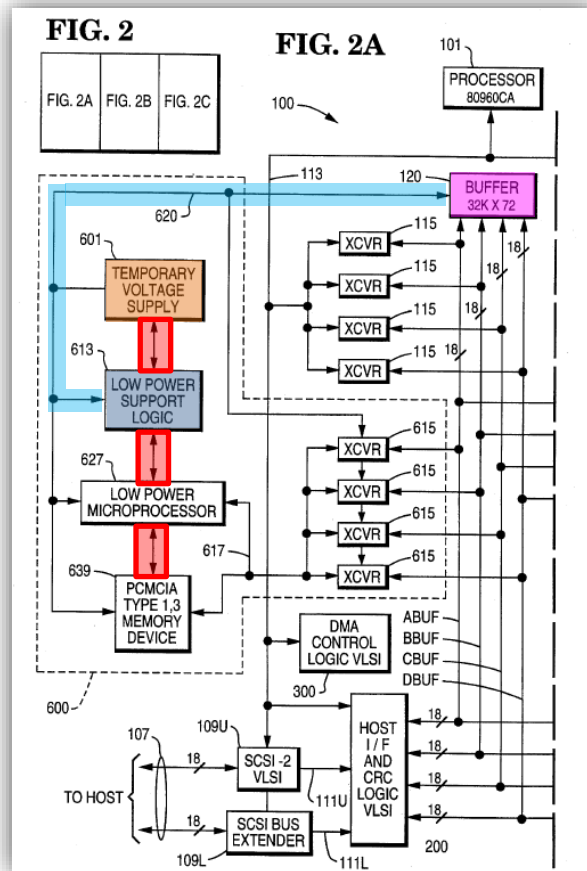
278. As explained below, it is my opinion that Weber in view of Horning further in view of Stokes teaches, and therefore renders obvious, every element of claim 6.

- a. **[Claim 6a]: “The method of claim 3 wherein the activating step (a) further comprises: reversing the flow of current between the computing engine and the plurality of super capacitors; and”**

279. It is my opinion that Weber in view of Horning further in view of Stokes renders obvious the method of claim 3 for the reasons discussed above. *Supra* § X.D.3. It is also my opinion that Weber and Horning further in view of Stokes render obvious the method recited in claim 6.

280. In my opinion, Weber in view of Horning further in view of Stokes teaches this claim element. Weber discloses that, upon loss of power, backup logic “assumes control” of the system. Ex-1006 at 9:17-22. The backup logic includes “low power support logic,” which—together with a power bus 620—provides “continuous power and refresh for the transfer buffer . . . as well as power to the components included in the backup logic.” *Id.* at 7:2-5; *see also id.* at 9:23-25.

281. Annotated Figure 2A, below, illustrates both the **low power support logic**, **temporary voltage supply (capacitors)**, and **volatile memory**:



282. As illustrated in annotated Figure 2A, there is a **bi-directional flow** between the **low power support logic** and the other components, including the **capacitors**, confirming that voltage is reversed between these components. In addition, for the low power support logic and power bus to “provide continuous power and refresh for the transfer buffer” as required by the specification, voltage from the **low power support logic** would necessarily have to be reversed on the **power bus** to the **transfer buffer (volatile memory)**. As discussed above, it would have been obvious to a POSITA to replace Weber’s capacitors with a plurality of

Stokes' super capacitors in order to supply sufficient reserve power from a reduced physical volume. *See supra* § X.D.

283. For at least these reasons, it is my opinion that Weber in view of Horning further in view of Stokes renders obvious "reversing the flow of current between the computing engine and the plurality of super capacitors."

b. [Claim 6b]: "discharging current from the plurality of super capacitors to the computing engine."

284. It is my opinion that Weber discloses this claim element. Weber discloses that voltage stored on the capacitors is discharged to provide "continuous power" to the computing engine, including the transfer buffer and all "other components included in the backup logic." Ex-1006 at 6:65-7:5; *see also id.* at Abstract (explaining that power from the high capacitance gold capacitor is used by the low power logic to "power the components included in the transfer memory backup system"); 9:15-36 (explaining that, once the system detects a drop in the primary voltage source, low power support logic provides power to backup logic components); Fig. 2A (illustrating current discharge from the capacitors); claims 4, 7, and 8 (reciting a voltage source, which may comprise a capacitor, to provide power to the buffer and low power backup transfer circuitry). As discussed above, it would have been obvious to a POSITA to replace Weber's capacitors with a plurality of Stokes' super capacitors in order to supply sufficient reserve power from

a reduced physical volume. *See supra* § X.D.

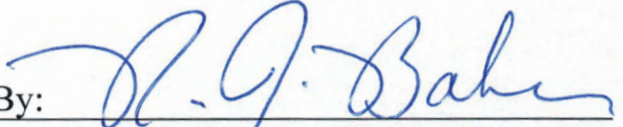
285. For at least these reasons, it is my opinion that Weber in view of Horning teaches “discharging current from the plurality of super capacitors to the computing engine.”

XI. CONCLUSION

286. For the foregoing reasons, it is my opinion that claims 1-3, 6, 10-12, and 15 of the '939 patent are rendered obvious by Horning, Stokes, Germer, Bruder, and Weber.

287. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: March 22, 2023

By: 
Dr. R. Jacob Baker, Ph.D., P.E