UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KIOXIA AMERICA, INC. and KIOXIA CORPORATION,

Petitioners,

v.

BiTMICRO LLC,

Patent Owner.

Case No.: IPR2023-00743
U.S. Patent No. 6,496,939

# PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,496,939

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## LIST OF EXHIBITS

| Ex. No. | Description |
|---|---|
| 1001 | U.S. Patent No. 6,496,939 ("the '939 patent") |
| 1002 | Excerpts of the File History for U.S. Patent No. 6,496,939 |
| 1003 | Declaration of Dr. R. Jacob Baker |
| 1004 | Curriculum Vitae of Dr. R. Jacob Baker |
| 1005 | U.S. Patent No. 4,559,616 ("Bruder"). Bruder issued on December 17, 1985. Thus, Bruder is prior art under pre-AIA 35 U.S.C. § 102(b). |
| 1006 | U.S. Patent No. 5,596,708 ("Weber"). Weber issued on January 21, 1997. Thus, Weber is prior art under pre-AIA 35 U.S.C. § 102(b). |
| 1007 | U.S. Patent No. 4,591,782 ("Germer"). Germer issued on May 27, 1986. Thus, Germer is prior art under 35 U.S.C. § 102(b). |
| 1008 | U.S. Patent No. 5,414,861 ("Horning"). Horning issued on May 9, 1995. Thus, Horning is prior art under 35 U.S.C. § 102(b). |
| 1009 | Claim Construction Order and Memorandum in Support Thereof, *BiTMICRO LLC v. KIOXIA Am., Inc.*, Case No. 6:22-cv-00331-ADA, Dkt. No. 54 (W.D. Tex. Feb. 16, 2023). |
| 1010 | U.S. Patent No. 3,980,935 ("Worst"). Worst issued on September 14, 1976. Thus, Worst is prior art under 35 U.S.C. § 102(b). |
| 1011 | U.S. Patent No. 4,306,299 ("Check"). Check issued on December 15, 1981. Thus, Check is prior art under 35 U.S.C. § 102(b). |
| 1012 | U.S. Patent No. 4,431,134 ("Hendricks"). Hendricks issued on February 14, 1984. Thus, Hendricks is prior art under 35 U.S.C. § 102(b). |
| 1013 | U.S. Patent No. 4,701,858 ("Stokes"). Stokes issued on October 20, 1987. Thus, Stokes is prior art under 35 U.S.C. § 102(b). |

| Ex. No. | Description |
|---|---|
| 1014 | U.S. Patent No. 4,453,117 ("Elms"). Elms issued on June 5, 1984. Thus, Elms is prior art under 35 U.S.C. § 102(b). |
| 1015 | U.S. Patent No. 4,412,284 ("Kerforne"). Kerforne issued on October 25, 1983. Thus, Kerforne is prior art under 35 U.S.C. § 102(b). |
| 1016 | U.S. Patent No. 3,562,555 ("Ahrons"). Ahrons issued on February 9, 1971. Thus, Ahrons is prior art under to 35 U.S.C. § 102(b). |
| 1017 | U.S. Patent No. 4,636,963 ("Nakajima"). Nakajima issued on January 13, 1987. Thus, Nakajima is prior art under 35 U.S.C. § 102(b). |

**Challenged Claims of U.S. Patent No. 6,496,939**

| **Claim element** | **Claim 1** |
|---|---|
| [Claim 1 Pre] | A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of: |
| [Claim 1a] | (a) activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system; |
| [Claim 1b] | (b) reconfiguring the data in the computing engine; and |
| [Claim 1c] | (c) deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level. |
| **Claim element** | **Claim 2** |
| [Claim 2a] | The method of claim 1 wherein the computing engine comprises a least one volatile memory and at least one non-volatile memory. |
| **Claim element** | **Claim 3** |
| [Claim 3a] | The method of claim 2 wherein the reconfiguring step (b) further comprises: |
| [Claim 3b] | (b1) allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory. |
| **Claim element** | **Claim 6** |
| [Claim 6 a] | The method of claim 3 wherein the activating step (a) further comprises: (a1) reversing the flow of current between the computing engine and the plurality of super capacitors; and |
| [Claim 6b] | (a2) discharging current from the plurality of super capacitors to the computing engine. |
| **Claim element** | **Claim 10** |

| | |
|---|---|
| [Claim 10 Pre] | A system for controlling data in a computer system when the computer system loses power, the computer system comprising a computer engine, comprising: |
| [Claim 10a] | means for activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system; |
| [Claim 10b] | means for reconfiguring the data in the computing engine; and |
| [Claim 10c] | means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level. |
| **Claim element** | **Claim 11** |
| [Claim 11] | The system of claim 10 wherein the computing engine comprises a least one volatile memory and at least one non-volatile memory. |
| **Claim element** | **Claim 12** |
| [Claim 12 Pre] | The system of claim 11 wherein the reconfiguring means further comprises: |
| [Claim 12a] | means for allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory. |
| **Claim element** | **Claim 15** |
| [Claim 15 Pre] | The system of claim 12 wherein the activating means further comprises: |
| [Claim 15a] | means for reversing the flow of current between the computing engine and the plurality of super capacitors; and |
| [Claim 15b] | means for discharging current from the plurality of super capacitors to the computing engine. |

# I. INTRODUCTION

KIOXIA Corporation and KIOXIA America, Inc. ("Petitioners") petition for institution of inter partes review ("IPR") of claims 1-3, 6, 10-12, and 15 ("challenged claims") of U.S. Patent No. 6,496,939 ("the '939 patent"). Ex-1001.

# II. GROUNDS FOR STANDING

Petitioners certify that the '939 patent is available for review under 35 U.S.C. § 311(c) and that Petitioners are not estopped from requesting *inter partes* review of the challenged claims on the grounds identified in this Petition.[1]

# III. FEES

The Commissioner is hereby authorized to charge or credit the fee specified by 37 C.F.R. § 42.15(a), and any other additional fees, to Bracewell LLP Deposit Account No. 50-0259.

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[1] The '939 patent expired on September 21, 2019. The Board has jurisdiction over expired patents through *inter partes* review. *See, e.g., See, e.g.*, *Sony Corp. v. Iancu*, 924 F.3d 1235, 1239–41 (Fed. Cir. 2019) (articulating the importance of the Board's review of expired patents because expired patents can be asserted for past infringement); *see also, e.g., Wasica Fin. GmbH v. Cont'l Auto. Sys., Inc.*, 853 F.3d 1272, 1279 (Fed. Cir. 2017) (noting that "[t]he Board construes claims of an expired patent in accordance with *Phillips*").

## IV. PRECISE RELIEF REQUESTED

Petitioners request review of the challenged claims under 35 U.S.C. § 311 and cancellation of the challenged claims under pre-AIA 35 U.S.C. § 103(a) in view of the prior art and grounds described herein.

### A. Prior Art

#### 1. Horning

Petitioners rely on U.S. Patent No. 5,414,861 ("Horning"). Ex-1008. Cornwell was issued on May 9, 1995, more than a year before the alleged priority date for the '939 patent, and qualifies as a prior art printed publication under at least pre-AIA 35 U.S.C. § 102(b).

#### 2. Germer

Petitioners also rely on U.S. Patent No. 4,591,782 ("Germer"). Ex-1007. Germer was issued on May 27, 1986, more than a year before the alleged priority date for the '939 patent, and qualifies as a prior art printed publication under at least pre-AIA 35 U.S.C. § 102(b).

#### 3. Bruder

Petitioners also rely on U.S. Patent No. 4,559,616 ("Bruder"). Ex-1005. Bruder was issued on December 17, 1985, more than a year before the alleged priority date for the '939 patent, and qualifies as a prior art printed publication under

at least pre-AIA 35 U.S.C. § 102(b).

#### 4. Weber

Petitioners rely on U.S. Patent No. 5,596,708 ("Weber"). Ex-1006. Weber was issued on January 21, 1997, more than a year before the alleged priority date for the '939 patent, and qualifies as a prior art printed publication under at least pre-AIA 35 U.S.C. § 102(b).

#### 5. Stokes

Petitioners rely on U.S. Patent No. 4,701,858 ("Stokes"). Ex-1013. Stokes was issued on October 20, 1987, more than a year before the alleged priority date for the '939 patent, and qualifies as a prior art printed publication under at least pre-AIA 35 U.S.C. § 102(b).

## V. IPR GROUNDS

| Ground | Claims | Statutory Basis |
|---|---|---|
| 1 | 1-3 | Horning in view of Stokes under pre-AIA 35 U.S.C. § 103 |
| 2 | 1-3 | Germer in view of Horning further in view of Stokes under pre-AIA 35 U.S.C. § 103 |
| 3 | 1-3, 6, 10-12, 15 | Bruder in view of Horning further in view of Stokes under pre-AIA 35 U.S.C. § 103 |
| 4 | 1-3, 6 | Weber in view of Horning further in view of Stokes under pre-AIA 35 U.S.C. § 103 |

## VI. THE '939 PATENT

### A. Overview of the '939 Patent

The '939 patent describes well known systems and methods for controlling data in a computer system upon power loss. Ex-1001 at 1:8-11. Computer systems typically comprise volatile "cache" memory, which is erased when power is removed, and non-volatile memory, which preserves data when power is removed. *Id*. at 1:15-33. Because volatile cache memory operates much faster than non-volatile memory, data is typically written to cache memory before being transferred to non-volatile memory. *Id*. The '939 patent explains that sudden loss of external power leaves insufficient time to transfer all newly written data from volatile cache memory to non-volatile memory, which risks data loss. *Id*. at 1:34-39. Accordingly, the '939 patent identifies an alleged need to ensure transfer of newly written data in the volatile memory to non-volatile memory in the event of a sudden power loss. *Id*. at 2:13-16.

The '939 patent purports to address this perceived need by using a "computing engine," comprising a processor, volatile memory, and non-volatile memory, *id*. at 3:33-36; Figure 1, and an array of "super capacitors" as a "short term power source" for the computing engine, *id*. at 2:27-31; 3:3-5. Upon a sudden loss of external power, the super-capacitors are purportedly "activated" to maintain internal power to the system. *Id*. at 5:8-11. Using the stored charge on the super-capacitors, data

in volatile memory can be transferred to non-volatile memory. *Id*. at 5:33-36. Once the super-capacitors have discharged "to a predetermined level," the super-capacitors are purportedly "deactivated" to cut off power to the computer system. *Id*. at 5:39-43; 5:48-52; 6:49-53. According to the specification, the super-capacitors are activated and deactivated by a "down-converter," which converts the high voltage stored on the super-capacitors to a lower voltage that can be utilized by the computing engine. *Id*. at 5:8-29; 5:39-43; 6:11-31; 6:40-44.

Figure 1 of the '939 patent, annotated below, illustrates this system, including the computing engine, which comprises a **processor**, **volatile memory**, and **non-volatile memory**, as well as a **super-capacitor array** and voltage **down-converter**.

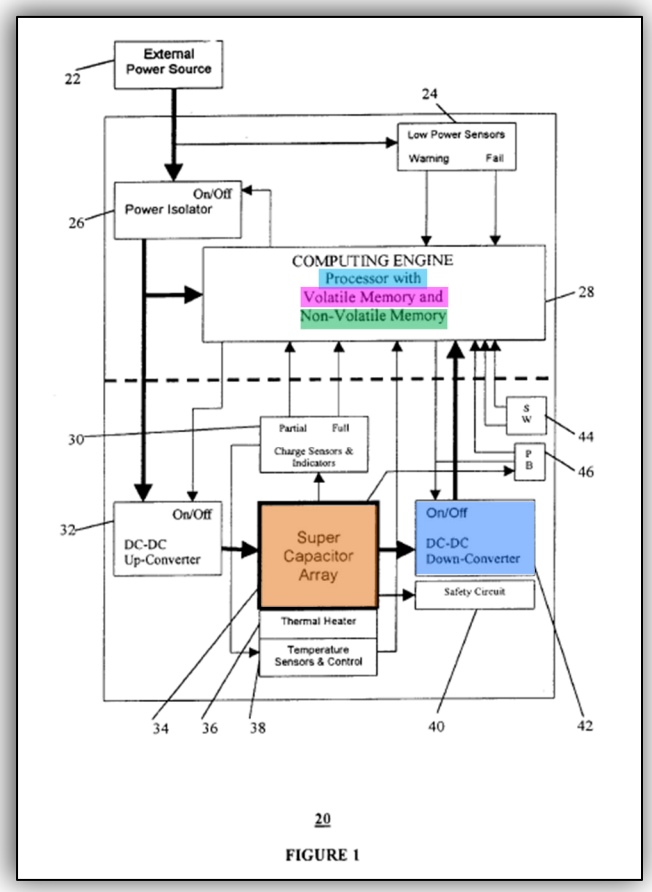


FIGURE 1

However, systems comprising the disclosed "computing engine," super-capacitors, and voltage down-converters were well known before the priority date of the '939 patent. Likewise, reconfiguring data using energy stored in capacitors to facilitate data transfer from volatile to non-volatile memory upon a sudden loss of power was equally well known before the applicable priority date. As explained below, Horning, Stokes, Bruder, Weber, and Germer all disclose such systems. Accordingly, nothing about the claims of the '939 patent would have been novel or non-obvious to a person of ordinary skill in the art ("POSITA") at the time the application for the '939 patent was filed. Ex-1003, ¶ 31.

### B. Prosecution History

The application underlying the ’939 patent was filed on September 21, 1999. In response to a rejection asserting that the applied-for claims were anticipated or rendered obvious by the prior art, the applicant made a number of substantive amendments to the claims. Importantly, neither Horner, Stokes, Germer, Bruder, nor Weber were before the Examiner during prosecution; however, as discussed below, these references disclose the particular claim elements on which the Examiner based the Notice of Allowance. *See* Ex-1003, ¶¶ 32-38.

## VII. LEVEL OF ORDINARY SKILL IN THE ART

As of the priority date, a POSITA would have had at least a Bachelor’s degree in electrical or computer engineering, or a similar field, and at least two years of work experience in the computer memory or data storage industry. Ex-1003, ¶¶ 64-67. A POSITA could have substituted less formal education with additional relevant work experience, and vice versa. *Id*.

## VIII. CLAIM CONSTRUCTION

Claim terms should be construed according to the *Phillips* standard. *See Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); *see also* 37 C.F.R. § 42.100(b). The Board need only construe terms to the extent necessary to resolve a controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor*

*Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

A patent claim that uses the term "means for" invokes a rebuttable presumption that the term is a means-plus-function term that should be construed pursuant to 35 U.S.C. § 112. *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1348 (Fed. Cir. 2015). Construing a means-plus-function term is a two-step process. *Id.* at 1351. First, the claimed function must be identified. *Id.* Second, the structure disclosed in the specification for performing the claimed function must be determined. *Id.*

For purposes of this proceeding only, Petitioners submit constructions for the below terms.[2] Petitioners do not believe that construction of any other term is

[2] While Petitioner proposes these constructions for purposes of this proceeding, Petitioner reserves its right to revise or amend these constructions in any other action or forum. *Western Digital Corp. v. Spex Techs., Inc.*, IPR2018-00084, Paper 14 at 11 (PTAB., April 25, 2018) ("37 C.F.R. § 104(b)(3) does not require [a p]etitioner to express its subjective agreement regarding correctness of its proffered claim constructions or to take ownership of those constructions"). Petitioner also reserves the right to challenge the validity of the challenged claims under 35 U.S.C. § 112 in another other action or forum. *See Target Corp. v. Proxicom Wireless, LLC*, IPR2020- 00904, Paper 11 at 12-13 (PTAB Nov. 10, 2020) (instituting IPR despite

necessary.

### A. Claims 1 and 10: "predetermined level"

The district court construed the term "predetermined level" as having a plain and ordinary meaning, which Petitioners adopt for the purposes of this Petition. *See* Ex-1009.

### B. Claims 1, 2, 6, 10, 11, and 15: "computing engine"/"computer engine"

Independent claim 1 and dependent claims 2 and 6 recite a "computing engine." Ex-1001, claim 1, 2, 6. Claims 10, 11, and 15 contain similar recitations in mean-plus-function format."[3] "Computing engine" should be construed as comprising a processor or similar structure for directing the transfer and storage of data in memory, volatile memory, and non-volatile memory. The specification explicitly states that the computing engine "contain[s] the processor, volatile and non-volatile memory." *Id*. at 3:33-36. Annotated Figure 1, shown below, further illustrates the computing

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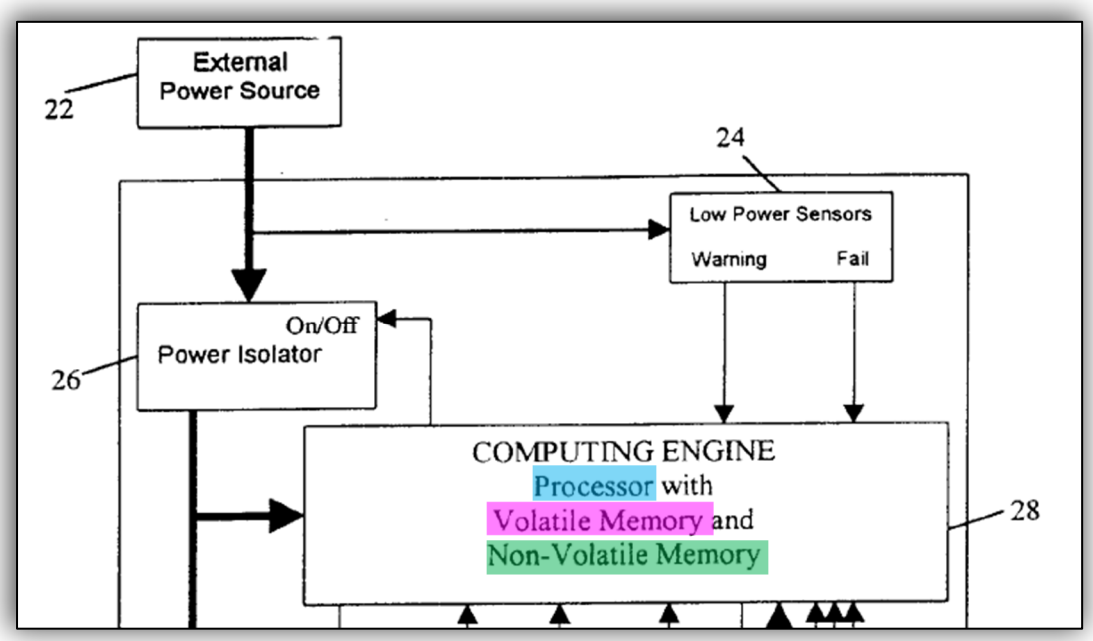
indefiniteness arguments in parallel lawsuit, explaining that this kind of "alternative pleading before a district court is common practice, especially where it concerns issues outside the scope of inter partes review").

[3] The preamble of claim 10 recites a "computer engine," but the individual elements of claim 10 recite a "computing engine."

engine as containing a **processor**, **volatile memory**, and **non-volatile memory**:




Moreover, a POSITA would have understood that the processor is a structure that controls the memory and sends signals and instructions to direct the transfer and storage of data in the volatile and non-volatile memory. Ex-1003, ¶ 73. Accordingly, based on the description in the specification, together with the knowledge of a POSITA, "computing engine" should be construed as comprising a processor or similar structure for directing the transfer and storage of data in memory, volatile memory, and non-volatile memory. *Id.*

### C. Claim 10: "means for activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system"

This term should be construed as a means-plus-function term, with a recited function of "activating a plurality of super capacitors to supply power to the

computing engine based upon power being removed from the computer system." The corresponding structure should be construed as a "down-converter and up-converter, and equivalents thereof, together with associated circuit components."

While the district court did not directly construe "means for activating," in connection with claim 15, the court construed "means for reversing the flow of current between the computing engine and the plurality of super capacitors." Ex-1009 at 26, 47. Per claim 15, the "activating means . . . comprises: means for reversing the flow of current . . . ." Accordingly, because the "means for activating" as construed by the court includes the "means for reversing," Petitioners adopt the court's construction of "means for reversing" for the "means for activating" claim element, which is a "down-converter 42 and up-converter 42[4] in Figure 1 (and corresponding text), and equivalents thereof." *Id*. Therefore, Petitioners propose that the structure for the "means for activating" includes the structure identified by the district court with respect to the "means for reversing," as well as associated circuit components.

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[4] The court's recitation of an "up-converter ***42***" appears to be an error, as the '939 patent does not disclose an up-cover with this numerical designation. Instead, the '939 patent discloses an "up-converter ***32***." Ex-1001 at 3:39-41 (emphasis added); Figure 1.

### D. Claim 10: "means for reconfiguring the data in the computing engine"

This term should be construed as a means-plus-function term, with a recited function of "reconfiguring the data in the computing engine." The corresponding structure should be construed as a "processor or equivalent structure that directs the transfer and storage of data in memory."

As explained above, the '939 patent states that the computing engine comprises a processor, volatile memory, and non-volatile memory. Ex-1001 at 3:33-36; Figure 1; *supra* § VIII.B. A POSITA would understand that the processor is the structure that controls the volatile and non-volatile memory in the computing engine by sending signals and instructions to direct the transfer and storage of data in the volatile and non-volatile memory. *See, e.g.*, Ex-1001 at 5:33-36; 6:35-37; *supra* § VIII.B; Ex-1003, ¶¶ 78-82. Thus, Petitioners applies the foregoing function and structure for this term.

### E. Claim 10: "means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level"

The district court construed this term as a means-plus-function term with the recited function as "deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level" and the corresponding structure as a "down-converter 42 in

Figure 1 (and corresponding text) and equivalents thereof, and switches, transistors, gates, *etc.* that are generally known in the art." Ex-1009 at 18-20, 46. Petitioners apply this construction for purposes of this Petition.

### F. Claim 12: "means for allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory"

This term should be construed as a means-plus-function term, with a recited function of "allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory." The corresponding structure should be construed as a "processor or equivalent structure that directs the transfer and storage of data in memory and is configured to transfer all data from volatile to non-volatile memory."

As stated in the claim language, dependent claim 12 further limits the "means for reconfiguring" claim element. The structure corresponding to the "means for reconfiguring" claim element is a "processor or equivalent structure that directs the transfer and storage of data in memory." *See supra* § VIII.D. Claim 12 illustrates that this structure must further be configured such to allow "all data to be transferred from the at least one volatile memory to the at least one non-volatile memory." For the purposes of this Petition, Petitioner thus applies the foregoing function and structure for this term.

### G. Claim 6: "reversing the flow of current between the computing

**engine and the plurality of super capacitors"**

Claim 6 recites "reversing the flow of current between the computing engine and the plurality of super capacitors." The district court construed this term as having a plain and ordinary meaning. Ex-1009 at 23-24, 46. For the purposes of this Petition, Petitioners apply the court's construction.

### H. Claim 15: "means for reversing the flow of current between the computing engine and the plurality of super capacitors"

The district court construed this term as a means-plus-function term, with the recited function of "reversing the flow of current between the computing engine and the plurality of super capacitors" and the following corresponding structure: "down-converter 42 and up-converter 42 in Figure 1 (and corresponding text), and equivalents thereof." Ex-1009 at 26, 47. Petitioners apply the court's construction for purposes of this Petition.

### I. Claim 15: "means for discharging current from the plurality of super capacitors to the computing engine"

This term should be construed as a means-plus-function term, with a recited function of "discharging current from the plurality of super capacitors to the computing engine." The corresponding structure should be construed as a "voltage down-converter or equivalent structure that converts a high voltage signal to a lower voltage signal and is configured to discharge current from the capacitors to the

computing engine."

As stated in the claim language, dependent claim 15 further limits the "means for activating the plurality of super-capacitors" claim element. As explained above, Petitioners construe the "means for activating" element as including a "down-converter 42 and up-converter 42 in Figure 1 (and corresponding text), and equivalents thereof." The portion of this structure corresponding to "discharging current from the plurality of super capacitors to the computing engine" is a down-converter configured to discharge current from the plurality of super-capacitors to the computing engine.

This is confirmed by the specification, which states that, once the down-converter has been activated and current has been reversed, "[t]he super capacitors then begin to ***slowly discharge current*** to the computer system ***through the down-converter***." Ex-1001 at 5:26-28 (emphasis added); 6:28-31; Figures 3 & 5 (current discharged "to the computer system through the down converter"). Annotated Figure 1, shown below, further illustrates that **current** from the **capacitors** is discharged through the **down-converter** to the computing engine:

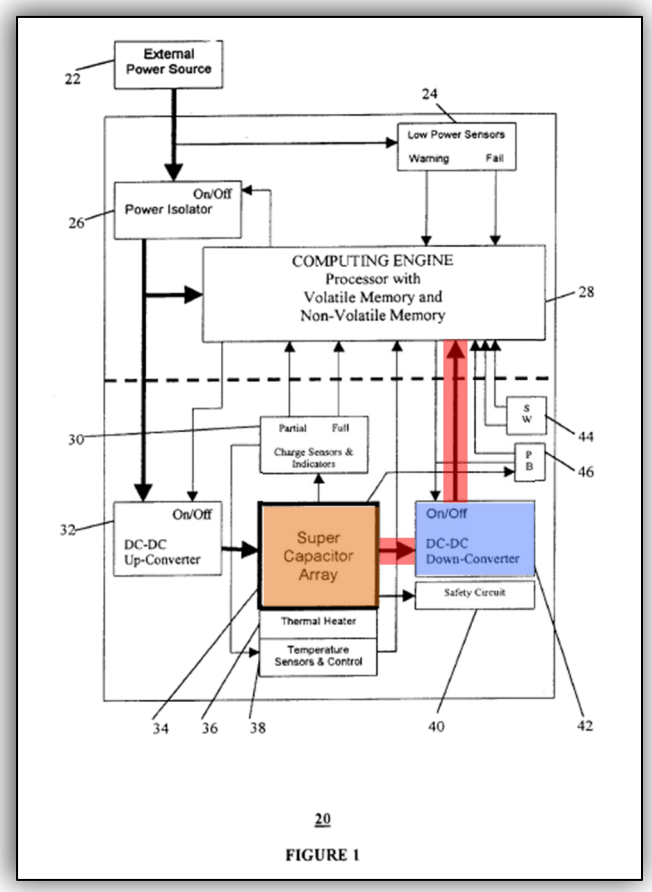


FIGURE 1

For the purposes of this Petition, Petitioners thus apply the foregoing function and structure for this term.

## IX. OVERVIEW OF THE PRIOR ART

### A. Bruder Discloses Systems and Methods for Storing Data in a Computer System When Power Is Lost

Bruder discloses a method and system for securely storing data when power is interrupted. This system includes volatile CMOS RAM and non-volatile "bubble memory." Ex-1005 at 7:52-60. While the volatile memory is used by the computer during normal operations, the entire contents of the volatile memory can be "rapidly

transfer[red]" to the non-volatile memory upon a power failure. *Id*. The power needed to facilitate this data transfer is supplied by a bank of storage capacitors containing sufficient energy to allow the transfer of data from volatile to non-volatile memory. *Id*. at 7:60-66. Power from these capacitors is routed through a "voltage down converter," which maintains the proper operating voltage for each of the system's components. *Id*. at 8:2-10. Bruder also teaches that control circuitry directs the transfer of data from volatile to non-volatile memory. *Id*. at 8:37-45.

### B. Weber Discloses a Transfer Memory Backup System To Safeguard Data When Power Is Lost

Weber discloses a "transfer memory backup system" for use with a computer data storage system. Ex-1006 at 3:51-57. This transfer memory backup system comprises volatile memory in the form of a transfer buffer, together with non-volatile PCMCIA flash card memory. *Id*. at Abstract; 3:38-43; 4:16-20; 5:13-20. The system also includes a low-power microprocessor, which controls data transfer from volatile to non-volatile memory in the event that external power is interrupted. *Id*. at 4:13-16; 6:65–7:8; 7:22-36. The system also comprises a temporary voltage source, which may include a "high capacitance gold capacitor," to power the transfer of data upon a power interruption. *Id*. at Abstract; 4:5-10; 6:65–7:8; 7:17-21.

### C. Germer Discloses an Electronic Register That Preserves Data When Power Is Lost

Germer discloses an electronic register that preserves data upon a power

outage. Ex-1007 at 2:27-30. This system includes volatile random access memory and non-volatile memory, a processor, and capacitors to store power. *Id*. at Abstract; 5:39-57. In the event of a power outage, the capacitors provide energy—through a regulator that converts a high-voltage signal to a low-voltage regulated signal appropriate for the electronic components—to power the transfer of data from volatile to non-volatile memory. *Id*. at 5:64-6:10. Using this power, the processor directs and controls the transfer of data from volatile memory to non-volatile memory. *Id*. at 5:49-57.

### D. Horning Discloses A Data Protection System That Uses Reserve Power To Maintain Data in Volatile Memory

Horning describes an intelligent data protection system that includes a power subsystem for providing backup power to a volatile memory that is preferably a solid state disk drive (SSD). Ex-1008 at 5:51-60. The backup power is supplied by a power subsystem that includes a reserve power supply maintained at an energy level sufficient to power the data transfer process between the volatile memory and a non-volatile memory. *See id*. at 8:9-24; 9:5-27. A control subsystem manages backup power and the data transfer process. *See id*. at 9:20-27. After the data transfer process is completed, power is removed from the memory arrays and the data protection system is deactivated. *Id*. Horning describes the power supply and reserve power supply for the data protection system as having "sufficient capacity"

to power the control subsystem, non-volatile memory, and volatile memory, and can be any circuit "well known in the art" recognized as suitable by persons having ordinary skill in the art. *See id*. at 12:1-11.

### E. Stokes Discloses a Super Capacitor-Based Backup Power System for a Nonvolatile Realtime Clock Calendar Module

Stokes discloses a "super capacitor" in the form of a "Double Layer Capacitor (DLC)" to maintain power to non-volatile memory in the event of power loss. Ex-1013 at 2:57-3:27. These super capacitors offer the advantage of reduced physical volume and cost per farad of capacitance. *Id*. at 3:7-10. Stokes explains that super capacitors are also quickly rechargeable, upon restoration of the primary power source. *See id*. at 4:28-32.

## X. THE CHALLENGED CLAIMS ARE UNPATENTABLE AND SHOULD BE CANCELLED

### A. Ground 1: Claims 1-3 Are Rendered Obvious by Horning in View of Stokes

Horning in view of Stokes teaches, and therefore renders obvious, claims 1-3 of the '939 patent. As explained in the attached declaration of Dr. R. Jacob Baker, Horning and Stokes are in the same field, teach analogous solutions to the same issues, and have the same purpose of improving a backup power supply for data preservation systems. Ex-1003, ¶¶ 116-122. Accordingly, a POSITA would have been motivated to incorporate Stokes' super-capacitors, which enable additional

power to be stored in a more compact form, into Horning's reserve power supply to provide the benefit of a more compact and efficient reserve power supply. *Id*.

This motivation is plain from the references themselves. Ex-1003, ¶¶ 117-118. Horning identifies the problems with the then-current state of battery size and rapid exhaustion, Ex-1008 at 2:13-25, and states that the reserve power supply may comprise "other energy storage devices" besides batteries, *id.* at 11:60-64. Horning further notes that "***persons having ordinary skill in the art could easily provide a*** suitable . . . ***reserve power supply*** [] with sufficient capacity to power the control subsystem [], volatile memory array [], and non-volatile memory array [], depending on the configuration of the computer system." *Id*. at 12:1-9 (emphasis added). Similarly, Stokes not only teaches the drawbacks of batteries (similar to Horning), but also teaches the benefits of super-capacitors, noting their "significance" because they can be "packaged in one cubic inch, a two order of magnitude reduction in volume of prior technology," and used to "sustain" operation of electronic devices and memory during power outages. Ex-1013 at 3:7-15. The benefits provided by Stokes thus directly align with Horning's purpose. Accordingly, a POSITA would have been motivated to combine these references to leverage the benefits of Stokes' super-capacitors and avoid the drawbacks of batteries in Horning's data protection system. Ex-1003, ¶ 119.

A POSITA also would have had every expectation of success in incorporating

super-capacitors into Horning's data protection system, as Stokes demonstrates that super-capacitors were already well-known for use in reserve power systems for preserving data in volatile memory when external power is lost. Ex-1013 at 2:57-3:61; Ex-1003, ¶ 121. Likewise, given the smaller form factor but otherwise interchangeable capability of super-capacitors, a POSITA would have understood that no significant changes would have been required to use a super-capacitor in place of another type of reserve power supply. Ex-1003, ¶ 120.

As a result, it would have been obvious to a POSITA to combine Horning with Stokes to improve the functionality of the system. *See* Ex-1003, ¶ 118.

### 1. Claim 1 Is Rendered Obvious by Horning in View of Stokes

#### a. [Claim 1 Pre]: "A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:"

To the extent the preamble is limiting, Horning discloses this claim element through the disclosure of data protection systems and methods that use different levels of reserve power to preserve data in volatile memory in the event of a power failure. *See* Ex. 1008, Abstract ("The data protection system also includes data transfer apparatus to transfer data from the volatile memory into a non-volatile memory upon command from the control apparatus."); *id*. at 5:1-8 (describing a method of intelligent data protection).

In particular, Horning discloses a control subsystem (including a memory control logic, a host interface logic, and a microprocessor), a volatile memory, and a non-volatile memory. *Id*. at Figure 1; 5:51-6:60; Abstract. In the event of power loss, the control subsystem will transfer the data from the volatile memory array to the non-volatile memory array. *Id*. at 9:20-28. Horning's control subsystem is thus a "processor or similar structure for directing the transfer and storage of data in memory" under Petitioners' proposed construction. Ex-1003, ¶ 125.

Annotated Figure 1 of Horning, shown below, illustrates the **control subsystem**, **volatile memory**, and **non-volatile memory**.

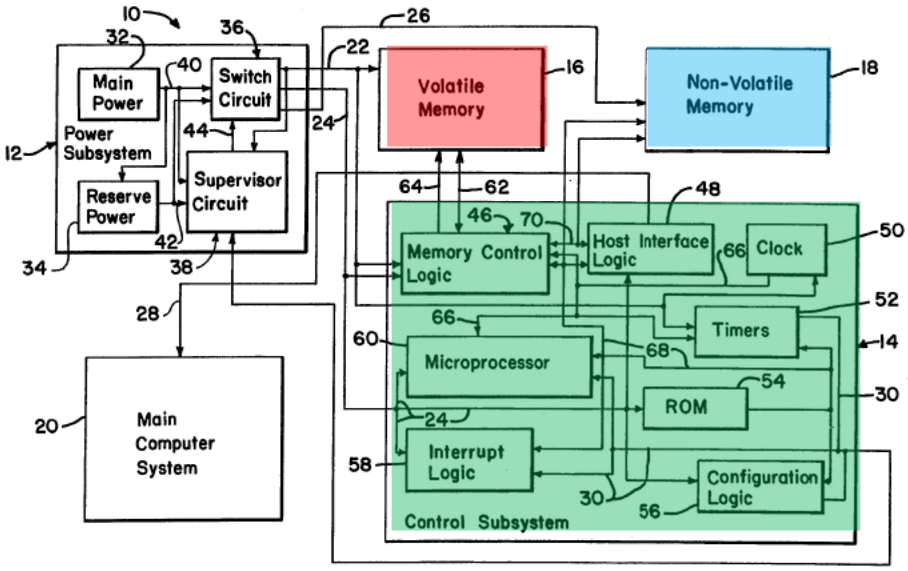


FIG. 1

*Id*., ¶ 126.

**b. [Claim 1a]: "activating a plurality of super capacitors to supply power to the computing engine based upon**

**power being removed from the computer system;"**

Horning in view of Stokes renders this claim element obvious. Horning discloses a power subsystem that includes main power and reserve power components. Ex-1008, Figure 1; 6:9-37. Upon interruption of power to the main power supply component, the reserve power supply is connected to maintain power to the memory arrays and prevent data loss. *See id*. at 6:27-37; 8:25-33; Abstract. As a result, Horning discloses activating a reserve power to supply to supply power upon the main power being removed from the computer system. Ex-1003, ¶ 131.

Horning describes an embodiment in which the reserve power supply comprises batteries, *see, e.g.*, *id*. at 13:16-25, but also states that "persons having ordinary skill in the art could easily provide a suitable main power supply [] and reserve power supply [] with sufficient capacity to power the control subsystem [], volatile memory array [], and non-volatile memory array [], depending on the configuration of the computer system." *Id*. at 12:1-9; 11:60-63 (stating that the reserve power supply may comprise "other energy storage devices"). Ex-1003, ¶ 129.

Stokes teaches a circuit module that utilizes a super-capacitor to maintain power to a nonvolatile memory in the event of power loss. *See* Ex-1013 at Abstract; 2:57-3:27. In particular, Stokes discloses a "super capacitor" in the form of a "Double Layer Capacitor (DLC)." *Id*. Stokes explains that super-capacitors offer

the advantage of reduced physical volume and cost per farad of capacitance. *Id*. at 3:7-10. Super-capacitors are also quickly rechargeable upon restoration of the primary power source. *See id*. at 4:28-32. Stokes also discloses that multiple DLCs—i.e., a plurality of DLCs—can be used to power a nonvolatile memory. *See id*. at 3:15-24. Ex-1003, ¶ 130.

As explained above, it would have been obvious to a POSITA to combine Horning with Stokes, including using a plurality of super-capacitors as described by Stokes in the power subsystem of Horning in order to benefit from the stated advantages. *Supra* § X.A. Ex-1003, ¶ 116-122, 131.

**c. [Claim 1b]: "reconfiguring the data in the computing engine;"**

Horning discloses that, in the event of prolonged external power loss, the data stored in the volatile memory array is transferred to the non-volatile memory array. Ex-1008 at Abstract; 7:19-23; 9:20-24; 11:9-17. This transfer of data from volatile to non-volatile memory is an example of "reconfiguring data" in the computing engine. Ex-1003, ¶¶ 132-133.

**d. [Claim 1c]: "deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level."**

Horning in view of Stokes renders this claim element obvious. Horning describes user programmable power control sequences that can be tailored to

accommodate a wide variety of capacities of reserve power supplies. *See* Ex-1008 at 7:60-8:8. Horning also discloses conserving reserve power by discharging the reserve power supply only to the point where there is enough energy to accomplish the data transfer task. *Id*. at 8:13-17. At that point, once all data has been transferred from volatile to non-volatile memory, Horning teaches that power is cut off to the computing engine by a circuit that "***removes power*** from the primary, secondary, and tertiary power conductors 22, 24, and 26, respectively, thereby ***deactivating the entire data protection system 10***."[5] *Id*. at 9:20-27 (emphasis added); 7:23-27. Horning thus teaches deactivating a reserve power supply to cut off power to the computing engine upon the reserve power system discharging to a predetermined level—i.e., a level where there is only enough energy left for the data transfer. Ex-1003, ¶¶ 134-137.

Annotated Figure 1 from Horning illustrates that conductors **22**, **24**, and **26** are the only lines that supply power to the control subsystem. Thus, when power is removed from conductors **22**, **24**, and **26**, power is removed from the entire system.

[5] The reserve power supply is part of, and thus is deactivated with, "data protection system 10." Ex-1008, Figure 1.

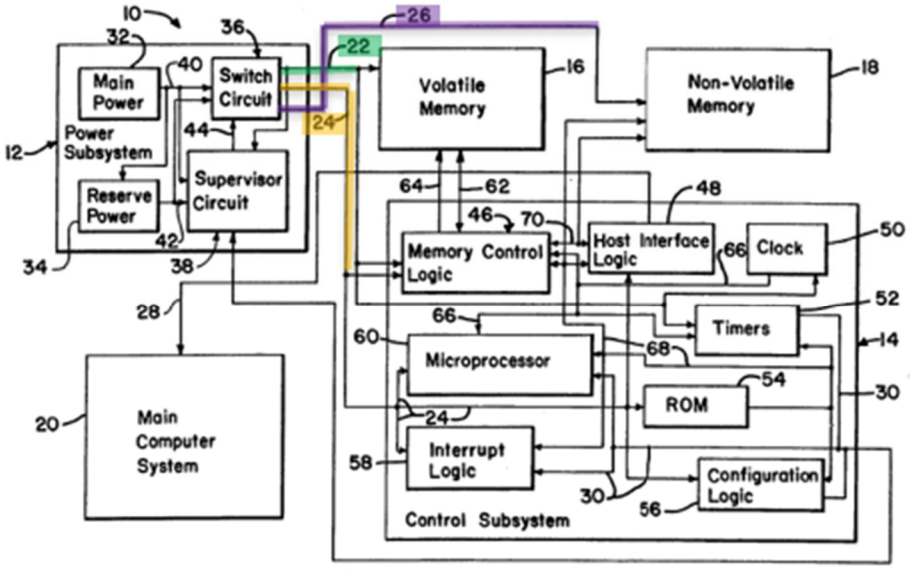


FIG. 1

*Id.*, ¶ 135.

As discussed above, it would have been obvious to a POSITA to combine Horning and Stokes, and to include a plurality of super capacitors as taught by Stokes in the power subsystem of Horning. *Supra* § X.A.; Ex-1003, ¶¶ 116-122, 128-131. As a result, it also would have been obvious to discharge the super-capacitors to a predetermined level at which there is enough charge to complete the data transfer task, and then disconnect those super-capacitors upon completion of data transfer, as taught by Horning. Ex-1003, ¶ 136.

### 2. Claim 2 Is Rendered Obvious by Horning in View of Stokes

#### a. [Claim 2 pre]: "The method of claim 1 wherein the computing engine comprises a least one volatile memory and at least one non-volatile memory."

Horning in view of Stokes renders obvious the method of claim 1 for the reasons discussed above. *Supra* § X.A.1. Horning and Stokes also render obvious the method of claim 2, as Horning discloses that the computing engine comprises both a volatile memory and non-volatile memory. *See supra* §§ X.A.1.a., X.A.1.c; Ex-1003, ¶¶ 124-127, 132-133.

#### 3. Claim 3 Is Rendered Obvious by Horning in View of Stokes

##### a. [Claim 3]: "The method of claim 2 wherein the reconfiguring step (b) further comprises: (b1) allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory."

Horning in view of Stokes renders obvious the method of claim 2 for the reasons discussed above, *supra* § X.A.2, and also render obvious the method of claim 3.

Horning discloses that the data transfer task allows for all the data from the volatile memory array to be transferred to the non-volatile memory array. Ex-1008 at 7:30-34. Horning further confirms that the power is not removed from the data protection system until after "***all the data*** [has] been transferred." *Id*. at 9:23-27 (emphasis added); Ex-1003, ¶¶ 142-144.

### B. Ground 2: Claims 1-3 Are Rendered Obvious by Germer in View of Horning Further in View of Stokes

Germer in view of Horning further in view of Stokes teaches, and therefore

renders obvious, claims 1-3 of the ’939 patent. As Dr. Baker explains, a POSITA would have been motivated to combine the power supply and power monitor for the electric meter disclosed in Germer with the intelligent data protection system disclosed in Horning. Ex-1003, ¶¶ 145-151. A POSITA also would have been motivated to combine Horning’s functionality for deactivating a reserve power supply to cut off power, with Germer’s data protection system, to provide optimal utilization and management of Germer’s reserve power supply. *Id*. Furthermore, a POSITA would have been motivated to combine the super capacitors described by Stokes into the combination of Germer and Horning in order to provide low cost-per-farad of capacitance with a reduced physical volume that is also quickly rechargeable. *Id*., ¶¶ 145, 149, 150.

Germer and Horning are in the same field, teach analogous solutions to the same issues, and have the same purpose of improving data protection and preservation systems. Ex-1003, ¶ 148. Thus, a POSITA would have been motivated to combine these references, which is apparent from the reference themselves. *Id*. Germer teaches that, once reserve power has dropped below the level where the processor can properly function, a reset signal is produced and a switching transistor “***cut off***” is maintained. Ex-1007 at 6:25-31; 9:3-6; claim 1; Ex-1003, ¶ 148. Likewise, Horning teaches that power is cut off to the computing engine by a circuit that “***removes power*** from the primary, secondary, and tertiary power conductors 22,

24, and 26, respectively, thereby ***deactivating the entire data protection system 10***." Ex-1007 at 9:20-27 (emphasis added); 7:23-27. Accordingly, the power optimization benefits taught by Horning directly align with Germer's purpose. As a result, a POSITA would have been motivated to combine Germer's data protection system with Horning's teaching of deactivating and cutting off power from a reserve power system, as this would have allowed Germer's data protection system to leverage the benefits of Horning's power optimization and utilization scheme. Ex-1003, ¶ 148.

A POSITA also would have had an expectation of success in incorporating Horning's functionality for deactivating the reserve power supply to cut off power into Germer's data protection system. Ex-1003, ¶ 150. As Germer teaches, a processor would need to be reset once power falls below a predetermined level, and Horning demonstrates the benefits of deactivating a capacitor to cut off power at such a level. *Id*., ¶ 149. Accordingly, a POSITA would have understood that incorporating Horning's teaching of deactivation into Germer's data preservation system would have been straightforward and yielded expected results. *Id*. Similarly, A POSITA would have understood that substituting a plurality of Stokes' super capacitors into the combination of Germer and Horning would be a simple substitution and yield the expected results of higher capacitance at a reduced physical volume. *Id*.

### 1. Claim 1 Is Rendered Obvious by Germer in View of Horning Further in View of Stokes

#### a. [Claim 1 Pre]: "A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:"

To the extent the preamble is limiting, Germer discloses this claim element. Germer is directed to an electronic register that saves data when a computer system loses power, together with methods for using the same. Ex-1007 at 2:18-4; 2:66-3:16; claim 15. In particular, Germer discloses a computing engine that comprises a processor, which contains volatile random access memory, and non-volatile memory. *Id*. at Abstract; 2:55-60; 3:7-13; 5:6-9; 5:12-15; 5:64-6:3. In the event of a power outage, the processor controls the transfer of data from the volatile memory to the non-volatile memory. *Id*. at 5:50-57. Germer's processor is thus a "processor or similar structure for directing the transfer and storage of data in memory" under Petitioners' proposed construction. Ex-1003, ¶ 153. As a result, Germer discloses "a processor or similar structure for directing the transfer and storage of data in memory, volatile memory, and non-volatile memory" pursuant to Petitioner's construction. *Id*.

Annotated Figure 2 of Germer, shown below, illustrates Germer's **processor**, which comprises volatile memory, as well as **non-volatile memory**:

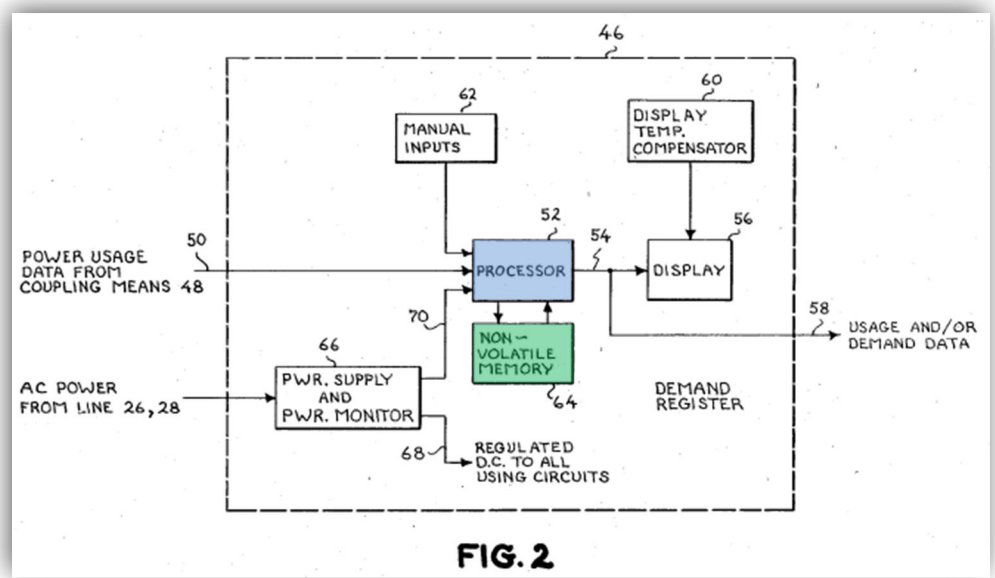

FIG. 2

*Id.*, ¶ 154.

**b. [Claim 1a]: "activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;"**

Germer renders this claim element obvious in view of Stokes. Germer discloses an "unregulated supply and emergency storage" component, which comprises a capacitor for storing power. Ex-1007 at Abstract; 2:30-34; 7:41-55. Germer further claims an electronic register that "includes ***a*** capacitor having a capacitance." *Id*. at claim 3. The use of the indefinite article "a" in a patent claim means "one or more."[6] As a result, by claiming "***a*** capacitor," Germer discloses

[6] *KCJ Corp. V. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2000) ("This court has repeatedly emphasized that an indefinite article 'a' or 'an' in patent

"one or more"—i.e., a plurality—of capacitors. Ex-1003, ¶ 156.

Germer also discloses that, in the event of a power outage, the capacitor is activated to "maintain power to critical circuits" for long enough "to permit transfer of billing data and programmed constants from the volatile random access memory . . . to safe storage in non-volatile memory." *Id.* at 5:64-6:3; 6:18-31. Germer thus teaches activating the capacitors to supply power to the computing engine based upon power being removed from the computer system. Ex-1003, ¶ 157.

A diagram illustrating the unregulated supply and emergency storage structure is provided in annotated Figure 3, below:

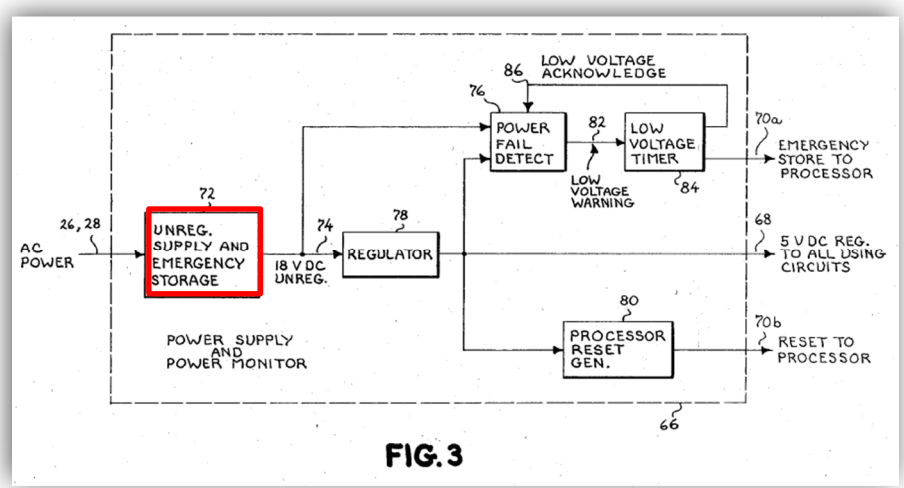

FIG. 3

A more detailed diagram of the unregulated supply and emergency storage

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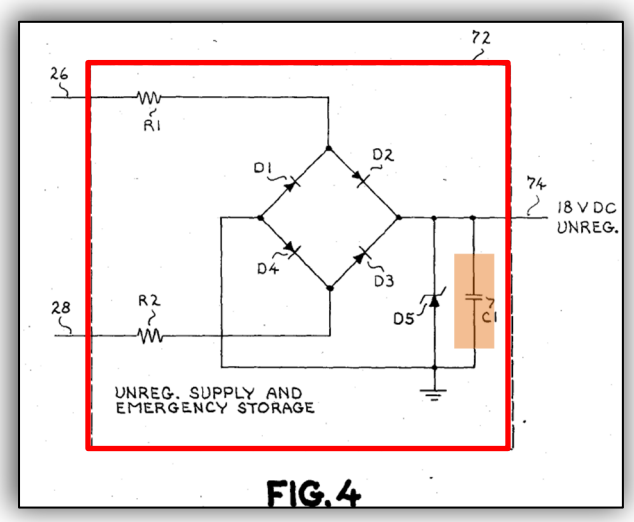
parlance carries the meaning of 'one or more' in open-ended claims containing the transitional phrase 'comprising.'").

component, illustrating a **capacitor**, is shown in annotated Figure 4, below:




Ex-1003, ¶¶ 158-159.

Although Germer does not refer to the capacitors as "super capacitors," use of super-capacitors in Germer's invention would have been obvious in view of Stokes. Ex-1003, ¶ 160.[7] As discussed above, super-capacitors would have been well-known to a POSITA at the time that that '939 patent was filed, and were also known to provide more capacitance in a smaller form factor. *Supra* § IX.E; Ex-1003,

[7] The '939 patent does not define what a super-capacitor, nor does it differentiate a super-capacitor from a "capacitor." Instead, the specification, simply states that "with the advent of low cost super-capacitors available in values of over 10 Farads, large amounts of energy can be affordably stored in a very small space." Ex-1001 at 3:7-10.

¶¶ 114-115, 160. Moreover, as also discussed above, a POSITA would have known that super-capacitors could be used electronic systems and circuits. Ex-1003, ¶¶ 114-115, 160. Thus, using Stokes' "super-capacitor" in place of a "capacitor" would have been obvious to a POSITA, particularly in view of Stokes' teachings and given Germer's disclosure that the capacitors need to have sufficient capacity to power the computing engine, and ensure the complete transfer of data to non-volatile memory, in the event of power loss. *See, e.g.*, IX.E *supra* (discussing characteristics of super capacitors); Ex-1003, ¶¶ 114-115, 160.

**c. [Claim 1b]: "reconfiguring the data in the computing engine;"**

Germer discloses that data in the computing engine is reconfigured by transferring the data "from the volatile random access memory in processor 52 to safe storage in non-volatile memory 64" upon a power interruption. Ex-1008 at 5:64-6:3; 5:49-57; 2:59-62; Claim 15; Ex-1003, ¶ 162.

**d. [Claim 1c]: "deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level."**

Germer in view of Horning further in view of Stokes renders this claim element obvious. Germer discloses a number of thresholds, including a specific threshold (e.g., a "third threshold") at which the processor "is no longer able to reliably maintain its operating conditions" and a reset signal is generated. Ex-1007

at 6:25-31. Germer explains that when the regulated voltage 68 (i.e., the output of regulator circuit seen in Fig. 5) powering the processor decreases "from its nominal value of 5 volts to a threshold value of about 3.9 volts," a reset to processor signal is generated. *Id*. at 9:9-13; Ex-1003, ¶ 164.

Horning also discloses a system and method of data protection that includes discharging a reserve power supply to a predetermined level at which it can supply enough power to the computing engine so that it can transfer all the data from the volatile memory array to the non-volatile memory array. *Supra* § X.A.1; Ex-1008 at 8:13-17. Horning teaches that cutting off power from the reserve power supply at that level allows the user to obtain "optimum utilization of the reserve power supply regardless of the capacity of the reserve power supply." *Id*. at 8:6-8; 8:19-24. Horning also discloses that, after all data has been transferred from volatile to non-volatile memory, power is cut off to the computing engine by a circuit that "***removes power*** from the primary, secondary, and tertiary power conductors . . . thereby ***deactivating the entire data protection system 10***."[8] *Id*. at 9:20-27 (emphasis added); Ex-1003, ¶ 165.

As discussed above, it would have been obvious to a POSITA to include the

[8] The reserve power supply is part of, and thus is deactivated with, "data protection system 10." Ex-1008, Figure 1.

teachings of Horning, including Horning's functionality for deactivating the reserve power system, in the system and method of Germer in order to achieve the stated optimum utilization of the reserve power capacitor. *Supra* § X.B.1.b; Ex-1003, ¶¶ 164-165. As discussed above, it would have been obvious to a POSITA to replace Germer's capacitors with Stokes' super capacitors in order to supply sufficient reserve power from a reduced physical volume. *See supra* § X.B.1.b; Ex-1003, ¶¶ 164-165.

#### 2. Claim 2 Is Rendered Obvious by Germer in View of Horning Further in View of Stokes

##### a. [Claim 2 pre]: "The method of claim 1 wherein the computing engine comprises a least one volatile memory and at least one non-volatile memory."

Germer in view of Horning further in view of Stokes renders obvious the method of claim 1 for the reasons discussed above. *Supra* § X.B.1. Germer and Horning in view of Stokes also render obvious the method of claim 2, as Germer discloses that the computing engine comprises both a volatile memory and non-volatile memory. *See supra* §§ X.B.1.a, X.B.1.c; Ex-1003, ¶¶ 167-169.

#### 3. Claim 3 Is Rendered Obvious by Germer in View of Horning Further in View of Stokes

##### a. [Claim 3]: "The method of claim 2 wherein the reconfiguring step (b) further comprises: (b1) allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory."

Germer in view of Horning further in view of Stokes renders obvious the method of claim 2 for the reasons discussed above, *supra* § X.B.2, and also renders obvious the method of claim 3.

Germer discloses that data in the computing engine is reconfigured by transferring the data "from the volatile random access memory in processor 52 to safe storage in non-volatile memory 64." Ex-1007 at 5:64-6:3; 5:49-57; 2:59-62. Germer further confirms that the power thresholds for deactivation of the capacitors are set to ensure "that ***all data*** is safely stored in non-volatile memory." *Id*. at 6:28-31 (emphasis added); Ex-1003, ¶¶ 172-173.

### C. Ground 3: Each of the Challenged Claims Is Rendered Obvious by Bruder in View of Horning Further in View of Stokes

Bruder in view of Horning further in view of Stokes teaches, and therefore makes obvious, claims 1-3, 6, 10-12, and 15 of the '939 patent. As Dr. Baker explains, a POSITA would have been motivated to combine Horning's functionality for deactivating a reserve power supply to cut off power with Bruder's data protection system to provide optimal utilization and management of Bruder's reserve power supply. Ex-1003, ¶¶ 174-180.

Bruder and Horning are in the same field, teach analogous solutions to the same issues, and have the purpose of improving data protection and preservation systems. Ex-1003, ¶¶ 175-177. Thus, a POSITA would have been motivated to

combine these references. *Id*. Bruder teaches that reserve power from capacitors should only be supplied for "long enough to allow this transfer of data [from volatile to non-volatile memory] to be accomplished." Ex-1005 at 7:64-66; Ex-1003, ¶¶ 175-177. Likewise, Horning teaches optimizing power utilization in a reserve power system using a circuit that "***removes power*** from the primary, secondary, and tertiary power conductors . . . thereby ***deactivating the entire data protection system 10***." Ex-1008 at 9:20-27 (emphasis added); 7:23-27. As a result, a POSITA would have been motivated to combine Bruder's data protection system with Horning's teaching of deactivating and cutting off power from a reserve power system because this would have allowed Bruder's data protection system to leverage the benefits of Horning's power optimization and utilization scheme. Ex-1003, ¶¶ 176-177. Furthermore, a POSITA would have been motivated to combine the super capacitors described by Stokes into the combination of Bruder and Horning in order to provide low cost-per-farad of capacitance with a reduced physical volume that is also quickly rechargeable. Ex-1003, ¶ 177.

A POSITA also would have had an expectation of success in incorporating Horning's functionality for deactivating the reserve power supply to cut off power into Bruder's data preservation system. Ex-1003, ¶ 179. As Bruder teaches, power should only be supplied temporarily to ensure that data is transferred to non-volatile memory, and Horning demonstrates the benefits of deactivating a capacitor to cut

off power at that same level. *Id*. Accordingly, a POSITA would have understood that incorporating Horning's teaching of deactivation into Bruder's data preservation system would have been straightforward and yielded expected results. *Id*. Likewise, a POSITA would have understood that substituting a plurality of Stokes' super capacitors into the combination of Germer and Horning would be a simple substitution and yield the expected results of higher capacitance at a reduced physical volume. *Id*., ¶ 178.

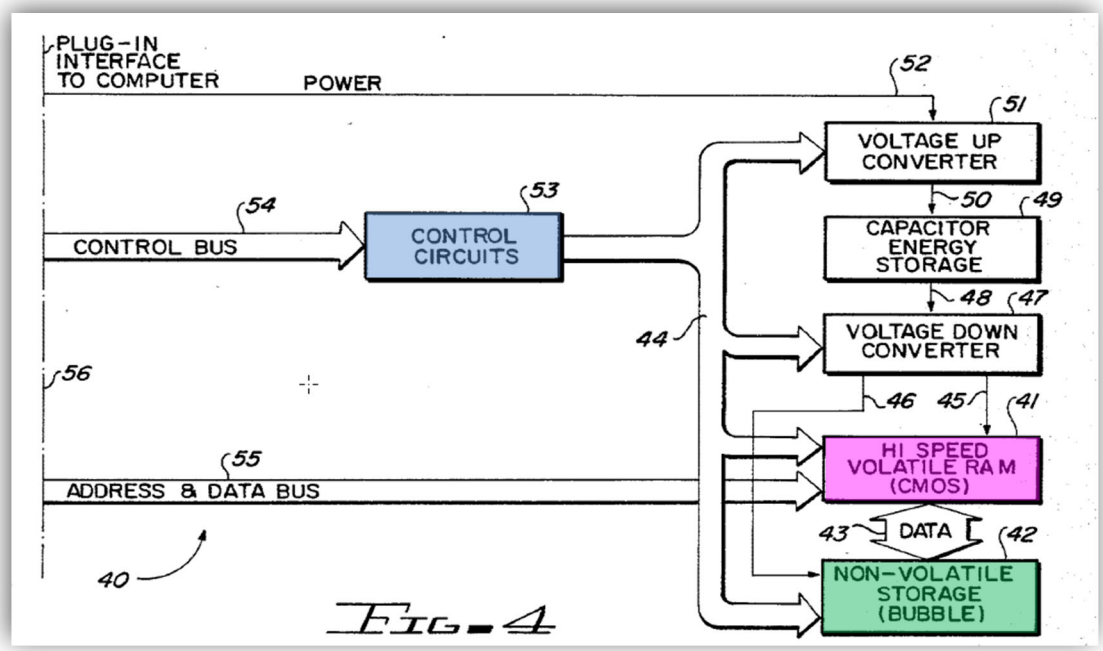
### 1. Claim 1 Is Rendered Obvious by Bruder in View of Horning Further in View of Stokes

#### a. [Claim 1 Pre]: "A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:"

To the extent the preamble is limiting, Bruder teaches this claim element. Bruder is directed to systems and methods for retaining data in a computer system when external power is interrupted. Ex-1005 at 1:8-13; Abstract. Bruder discloses a computing engine that comprises both volatile memory (e.g., CMOS RAM) and non-volatile memory (e.g., bubble memory). *Id*. at Abstract; 2:32-42; 7:52-60; Fig. 4. Bruder also teaches control circuits, which control "data transfer between CMOS Ram 41 and bubble memory 42 during a power interruption." *Id*. at 8:37-45. The "control circuits" comprise a "processor or similar structure for directing the transfer and storage of data in memory" under the Petitioners' proposed construction of

computing engine. Ex-1003, ¶ 182.

Bruder's **control circuits**, **volatile memory**, and **nonvolatile memory**, which comprise the claimed "computing engine," are illustrated in annotated Figure 4, below:




*Id.*, ¶ 183.

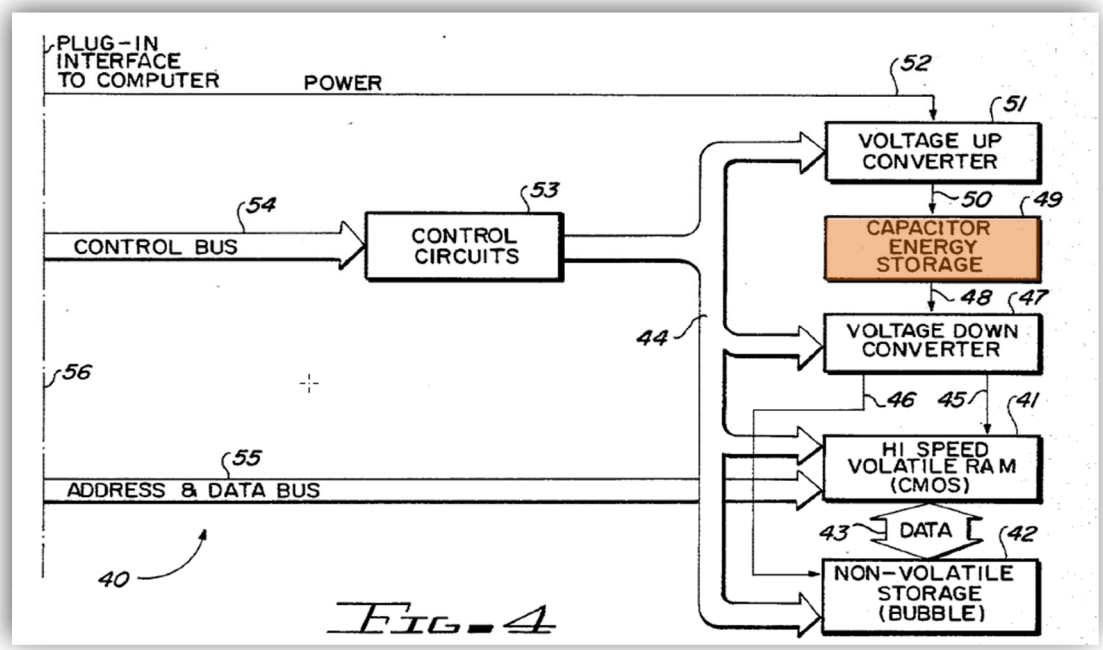
**b. [Claim 1a]: "activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;"**

Bruder renders this claim element obvious in view of Stokes. Bruder discloses a capacitor bank (i.e., a "plurality of capacitors") that stores and "supplies enough energy to maintain the voltage supply lines" to the memory and other circuitry when external power is interrupted. Ex-1005 at 7:60-66; Abstract; 2:35-38; 8:2-7; Fig. 4;

Ex-1003, ¶ 185.

Bruder also teaches activating the capacitors when external power is removed from the computer system. Bruder states that, when external power to the computing system is interrupted, "low power control circuitry actuates a voltage down converter circuit that produces a regulated output voltage" from the capacitor bank "to temporarily power the control circuitry." *Id*. at Abstract; 8:2-10; 2:35-38; Ex-1003, ¶ 186.

The **capacitor bank** is illustrated in annotated Figure 4, below.




Ex-1003, ¶ 187.

Although Bruder does not refer to the capacitors as "super capacitors," use of super-capacitors in Bruder's invention would have been obvious in view of Stokes.

*Id*., ¶ 188.[9] As discussed above, super-capacitors would have been well-known to a POSITA at the time that that '939 patent was filed, and were also known to provide more capacitance in a smaller form factor. *Supra* § IX.E.; Ex-1003, ¶¶ 114-115, 188. Moreover, as also discussed above, a POSITA would have known that super-capacitors could be used electronic systems and circuits. *Id*. Thus, using a "super-capacitor" in place of a "capacitor" would have been obvious to a POSITA based on the advantages taught by Stokes and also given Bruder's disclosure that the capacitors need to have sufficient capacity to power the computing engine, and ensure the complete transfer of data to non-volatile memory, in the event of power loss. *See, e.g.*, § IX.E. *supra* (discussing characteristics of super capacitors); Ex-1003, ¶¶ 114-115, 188.

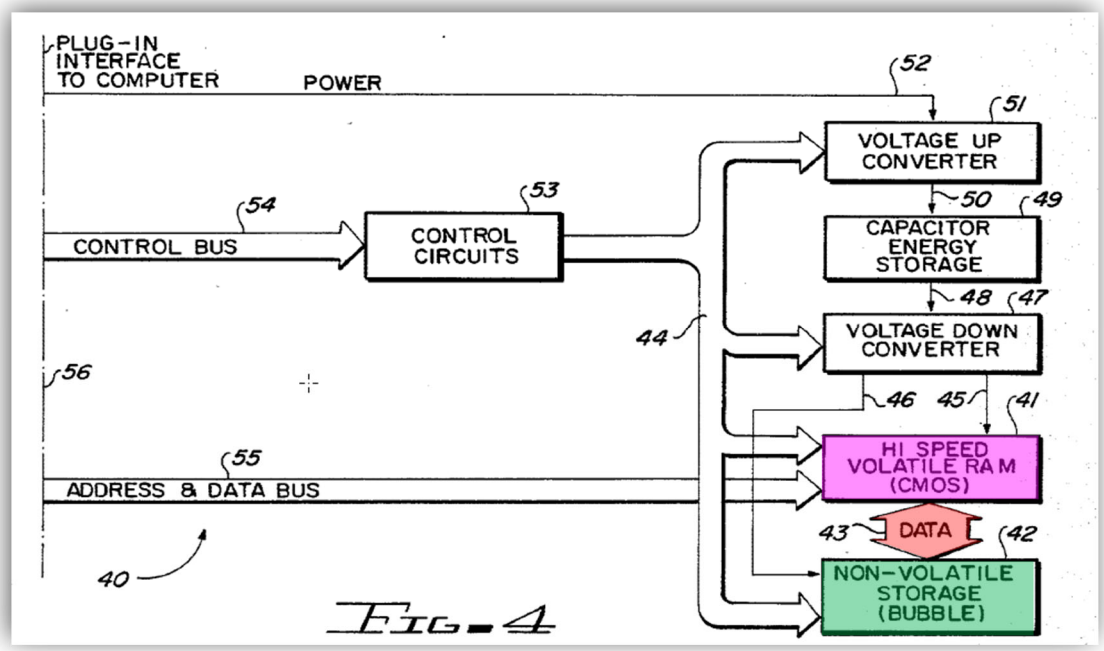
**c. [Claim 1b]: "reconfiguring the data in the computing engine;"**

Bruder discloses that, in the event of a power interruption, data is reconfigured in the computing engine by "transfer[ring] the entire contents" of volatile CMOS RAM to non-volatile bubble memory. Ex-1005 at 7:57-60; 8:2-10; 10:58-64; Ex-1003, ¶ 194.

Annotated Figure 4, below, depicts the transfer—or reconfiguration—of data

[9] The '939 patent does not define what a super-capacitor is. *Supra* Footnote 7.

from **volatile memory** to **non-volatile memory** via a **data bus**:




Ex-1003, ¶ 191.

**d. [Claim 1c]: "deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level."**

Bruder renders this claim element obvious in view of Horning further in view of Stokes. Bruder teaches that the capacitor bank supplies power to the down converter to "temporarily power the control circuitry" while data is being transferred from volatile to non-volatile memory. Ex-1005 at Abstract; 2:35-42; 7:64-66. By teaching that the capacitor bank is only activated "temporarily"—and only for "long enough" to affect a complete data transfer from volatile to non-volatile memory—Bruder indicates that the capacitor bank is deactivated. Bruder also teaches the

importance of regulating the power output from the reserve power supply, noting that the capacitors maintain voltage "long enough to allow this transfer of data [from volatile to non-volatile memory] to be accomplished." *Id.* at 7:64-66; 3:40-44; 8:7-10; 10:58-64; Ex-1003, ¶ 194.

Horning discloses a system and method of data protection that includes discharging a reserve power supply to a predetermined level at which it can supply enough power to the computing engine so that it can transfer all the data from the volatile memory array to the non-volatile memory array. *Supra* § IX.D; Ex-1008 at 8:13-17. Horning teaches that cutting off power from the reserve power supply at that level allows the user to obtain "optimum utilization of the reserve power supply regardless of the capacity of the reserve power supply." *Id*. at 8:6-8; 8:19-24. Horning also discloses that, after all data has been transferred from volatile to non-volatile memory, power is cut off to the computing engine by a circuit that "***removes power*** from the primary, secondary, and tertiary power conductors . . . thereby ***deactivating the entire data protection system 10***."[10] *Id*. at 9:20-27 (emphasis added). Ex-1003, ¶ 195.

As discussed above, it would have been obvious to a POSITA to include the

[10] The reserve power supply is part of, and thus is deactivated with, "data protection system 10." Ex-1008, Figure 1.

teachings of Horning, including Horning's functionality for deactivating the reserve power system, in Bruder's data protection system in order to achieve the stated optimum utilization of the reserve power capacitor. *Supra* § X.C.1.b; Ex-1003, ¶¶ 185-189. Furthermore, as discussed above, it would have been obvious to a POSITA to replace Bruder's capacitors with a plurality of Stokes' super capacitors in order to supply sufficient reserve power from a reduced physical volume. *See supra* § X.C.1.b; Ex-1003, ¶¶ 185-189.

### 2. Claim 2 Is Rendered Obvious by Bruder in View of Horning Further in View of Stokes

#### a. [Claim 2]: "The method of claim 1 wherein the computing engine comprises a least one volatile memory and at least one non-volatile memory."

Bruder in view of Horning further in view of Stokes renders obvious the method of claim 1 for the reasons discussed above. *Supra* § X.C.1. Bruder and Horning also render obvious the method of claim 2, as Bruder teaches that the computing engine comprises at least one volatile memory (e.g., CMOS RAM) and at least one non-volatile memory (e.g., bubble memory). *See supra* §§ X.C.1.a, X.C.1.c; Ex-1003, ¶¶ 198-199.

### 3. Claim 3 Is Rendered Obvious by Bruder in View of Horning Further in View of Stokes

#### a. [Claim 3]: "The method of claim 2 wherein the reconfiguring step (b) further comprises: (b1) allowing

**all data to be transferred from the at least one volatile memory to the at least one non-volatile memory."**

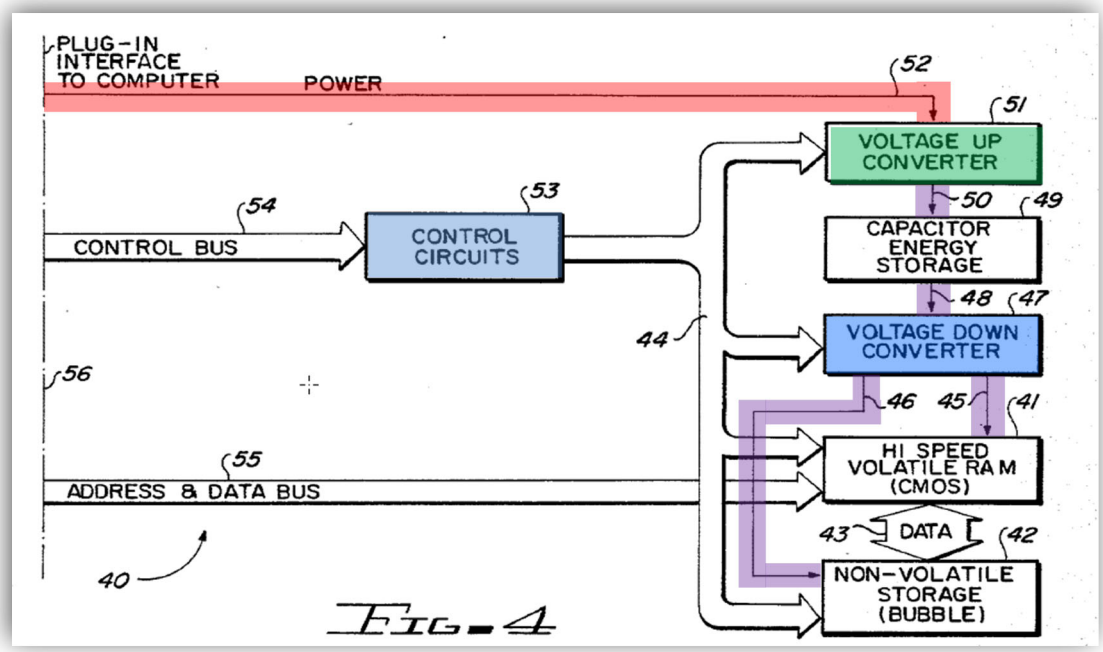
Bruder in view of Horning further in view of Stokes renders obvious the method of claim 2 for the reasons discussed above, *supra* § X.C.2, and also renders obvious the method of claim 3. In particular, Bruder teaches that "the entire contents" of volatile CMOS RAM is transferred to non-volatile bubble memory in the event of a power failure. Ex-1005 at 7:57-60; 8:2-10; 10:58-64; Ex-1003, ¶¶ 201-202.

#### 4. Claim 6 Is Rendered Obvious by Bruder in View of Horning Further in View of Stokes

##### a. [Claim 6a]: "The method of claim 3 wherein the activating step (a) further comprises: reversing the flow of current between the computing engine and the plurality of super capacitors; and"

Bruder in view of Horning further in view of Stokes renders obvious the method of claim 3 for the reasons discussed above, *supra* § X.C.3, and also render obvious the method of claim 6.

As illustrated in annotated Figure 4 below, Bruder teaches a **single power bus (52)** that provides power to the **control circuits (53)**, **voltage down converter (47)**, **voltage up converter (51),** and other components through a series of **conductors (45, 46, 48, and 50)**:




*See also* Ex-1005 at 7:66-8:2 (explaining that the conductors 45 and 46 supply power to the non-volatile and volatile memory, respectively, and "normally receive their operating power from the main power bus"); 8:21-24; Ex-1003, ¶ 205. As discussed above, it would have been obvious to a POSITA to replace Bruder's capacitors with a plurality of Stokes' super capacitors in order to supply sufficient reserve power from a reduced physical volume. *See supra* § X.C.1.b; Ex-1003, ¶ 206.

Bruder further teaches that, once the capacitor bank is activated, power is "gradually discharged into a down ***voltage converter*** that produces a constant, regulated output voltage ***to the control circuitry***, the CMOS memory, and the bubble memory system." Ex-1005 at 2:35-42 (emphasis added); Abstract. As annotated Figure 4 (above) demonstrates, there is no separate power bus to provide power from

the down converter to the control circuitry when the capacitors are activated. Accordingly, for the up-converter and down-converter to provide "voltage to the control circuitry" as taught in the specification, it would be obvious to a POSITA that the flow of current from the capacitors to the control circuitry would need to be reversed over power bus 52 to reach the control circuits. Ex-1003, ¶ 206.

#### b. [Claim 6b]: "discharging current from the plurality of super capacitors to the computing engine."

Bruder teaches that, upon activation, power from the capacitors is "discharged into a down voltage converter that produces a constant, regulated output voltage to the control circuitry, the CMOS memory, and the bubble memory system." Ex-1005 at 2:35-42; Abstract; 8:11-15; Ex-1003, ¶ 208.

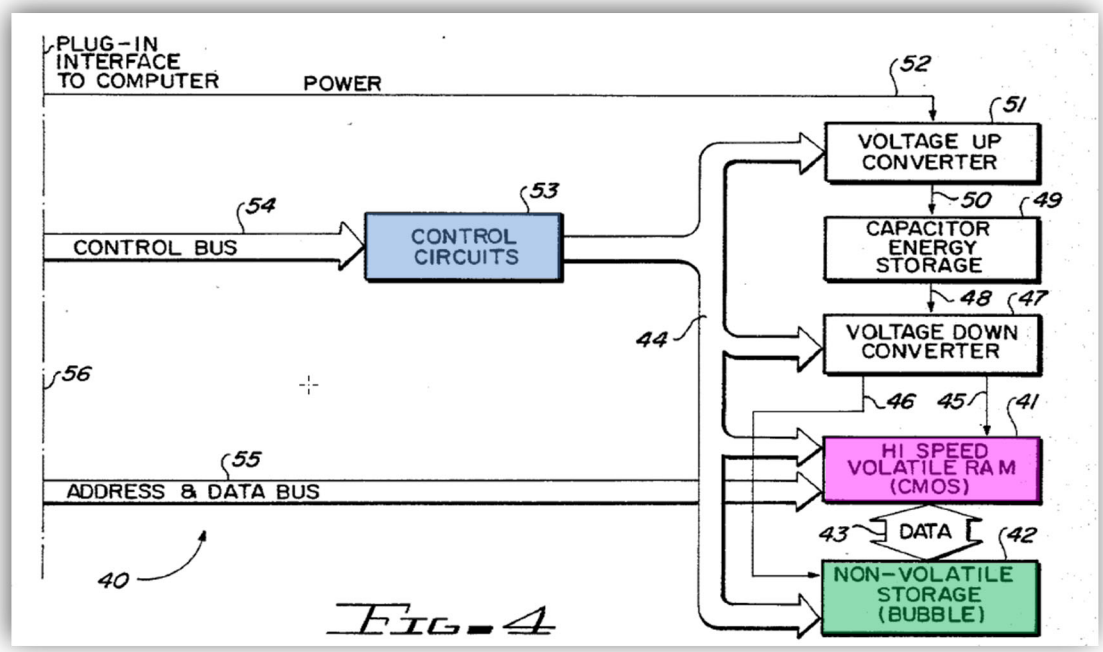
### 5. Claim 10 Is Rendered Obvious by Bruder in View of Horning Further in View of Stokes

#### a. [Claim 10 pre]: "A system for controlling data in a computer system when the computer system loses power, the computer system comprising a computer engine, comprising:"

To the extent the preamble is limiting, Bruder discloses this claim element. Bruder is directed to systems and methods for retaining data in a computer system when external power to the computer system is interrupted. Ex-1005 at 1:8-13; Abstract. Bruder discloses a computing engine that comprises both volatile memory (e.g., CMOS RAM) and non-volatile memory (e.g., bubble memory) for storing data.

*Id*. at Abstract; 2:32-42; 7:52-60; Fig. 4. Bruder also discloses control circuits, which control "data transfer between CMOS Ram 41 and bubble memory 42 during a power interruption." *Id*. at 8:37-45. The "control circuits" comprise a "processor or similar structure for directing the transfer and storage of data in memory" under Petitioners' proposed construction of "computer engine." Ex-1003, ¶ 211.

Bruder's **control circuits**, **volatile memory**, and **nonvolatile memory** are illustrated in annotated Figure 4, below:




Ex-1003, ¶ 212.

**b. [Claim 10a]: "means for activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;"**

Bruder renders this claim element obvious in view of Stokes. Bruder discloses

a capacitor bank (i.e., a "plurality of capacitors") that stores and "supplies enough energy to maintain the voltage supply lines" to the memory and other circuitry when external power is interrupted. Ex-1005 at 7:60-66; Abstract; *id*.; 2:35-38; 8:2-7; Fig. 4. Although Bruder does not refer to the capacitors as "super capacitors," use of super-capacitors in Bruder's invention would have been obvious in view Stokes. Ex-1003, ¶¶ 114-115, 214.[11] As discussed above, super-capacitors would have been well-known to a POSITA at the time that that '939 patent was filed, and were also known to provide more capacitance in a smaller form factor. *Supra* § IX.E; Ex-1003, ¶¶ 114-115, 214. Moreover, as also discussed above, Stokes teaches that super-capacitors could be used in electronic systems and circuits. Ex-1003, ¶¶ 114-115, 214. Thus, using Stokes' "super-capacitor" in place of a "capacitor" would have been obvious to a POSITA, particularly given Bruder's disclosure that the capacitors need to have sufficient capacity to power the computing engine, and ensure the complete transfer of data to non-volatile memory, in the event of power loss. *See, e.g.*, § IX.E *supra* (discussing characteristics of super capacitors); Ex-1003, ¶¶ 114-115, 214.

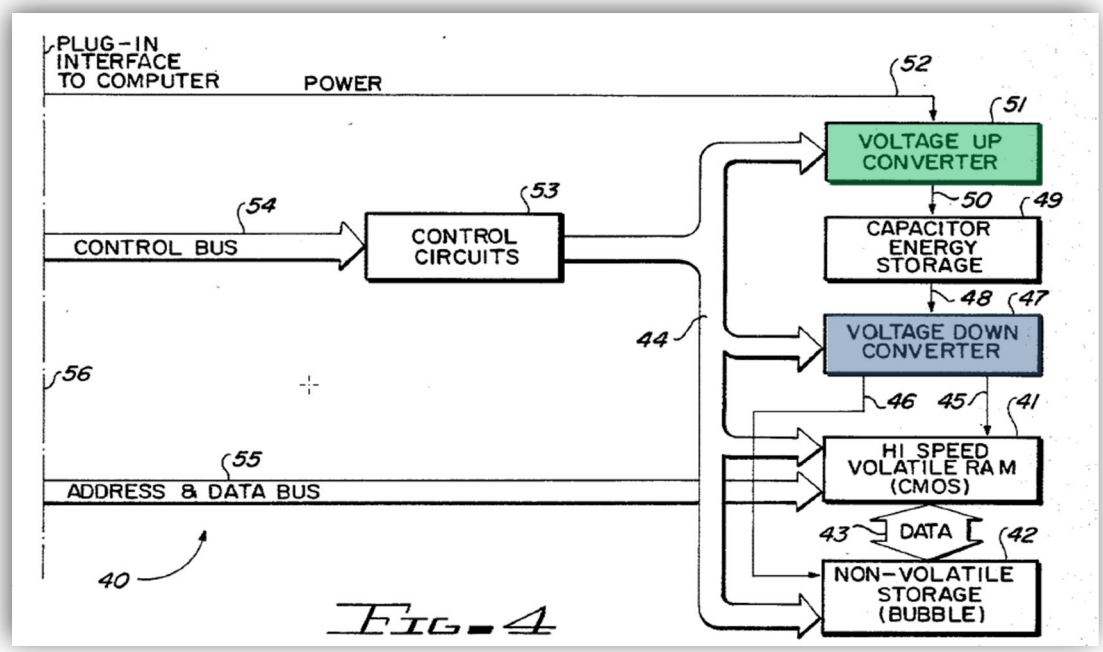
Bruder also discloses both the function and structure for activating the capacitors when external power is removed from the computer system pursuant to

[11] The '939 patent does not define what a super-capacitor is. *Supra* Footnote 7.

Petitioner's proposed construction. Bruder explains that, when external power to the computing system is interrupted, "low power control circuitry actuates a ***voltage down converter circuit*** that produces a regulated output voltage to temporarily power the control circuitry" using the capacitor bank. *Id*. at Abstract (emphasis added); Ex-1005 at 8:2-10. Bruder further teaches that the down-converter converts a +100 volt supply from the capacitor bank to a lower voltage supply that can be utilized by the electronic components. *Id*. at 9:35-10:5; Ex-1003, ¶ 215.

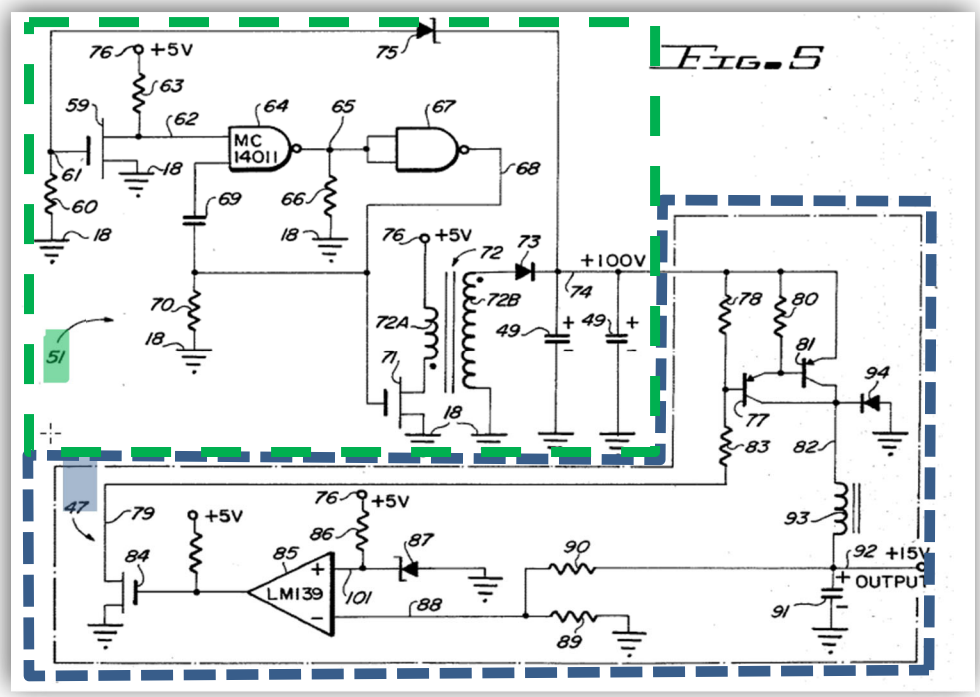
Bruder also discloses that a "'***voltage up' converter circuit*** 51 boosts the normal operating voltage on main power bus 52 to produce the 100 volts needed to charge up capacitor bank 49 and thereby store enough energy in case of a power failure." Ex-1005 at 8:31-34; 8:37-45. As a result, Bruder discloses a "down-converter 42 and up-converter 42 in Figure 1 (and corresponding text), and equivalents thereof" as well as associated circuit components, under the Petitioner's proposed construction for this means-plus-function element; Ex-1003, ¶ 216.

A general view of the **voltage down converter (47)** and **voltage up converter (51)** is illustrated in annotated Figure 4, below:




*Id.*, ¶ 217.

A more detailed diagram of Bruder's voltage **down-converter (47)** and **voltage up converter (51)** and associated circuit components also illustrated in annotated Figure 5, below:




*Id.*, ¶ 218.

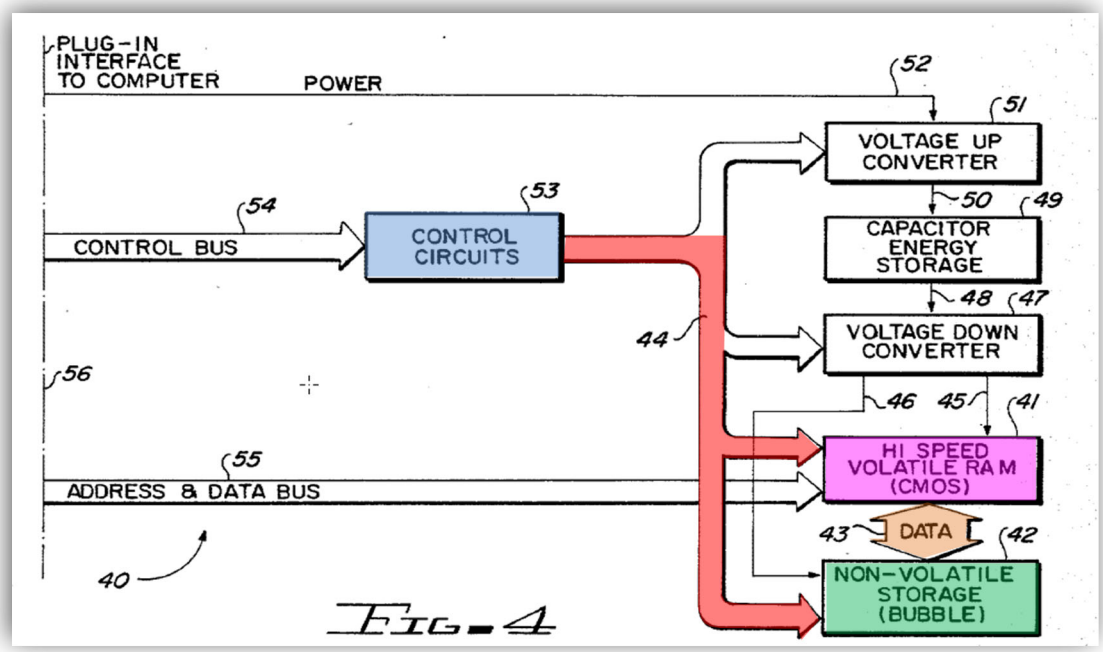
**c. [Claim 10b]: "means for reconfiguring the data in the computing engine;" and**

Bruder discloses both the function of reconfiguring the data in the computing engine, teaching that, in the event of a power failure, data is reconfigured in the computing engine by "transfer[ring] the entire contents" of volatile CMOS RAM to non-volatile bubble memory. Ex-1005 at 7:57-60; 8:2-10; 10:58-64; Ex-1003, ¶ 220.

Bruder also discloses structure for performing this function, explaining that "[c]ontrol circuitry . . . generates the necessary signals on bus 44 to . . . achieve the desired data transfer" from volatile memory to nonvolatile memory. Ex-1005 at 8:37-45; Abstract; 10:54-64. Bruder's control circuitry is a "processor or equivalent

structure that directs the transfer and storage of data in memory" pursuant to Petitioners' proposed construction for this means-plus-function element. Ex-1003, ¶ 221.

Annotated Figure 4, below, illustrates the **control signals** provided by the **control circuity (53),** which result in a reconfiguration or transfer of data from **volatile memory (41)** to **nonvolatile memory (42)** over a **data bus (43)**.




*Id.*, ¶ 222.

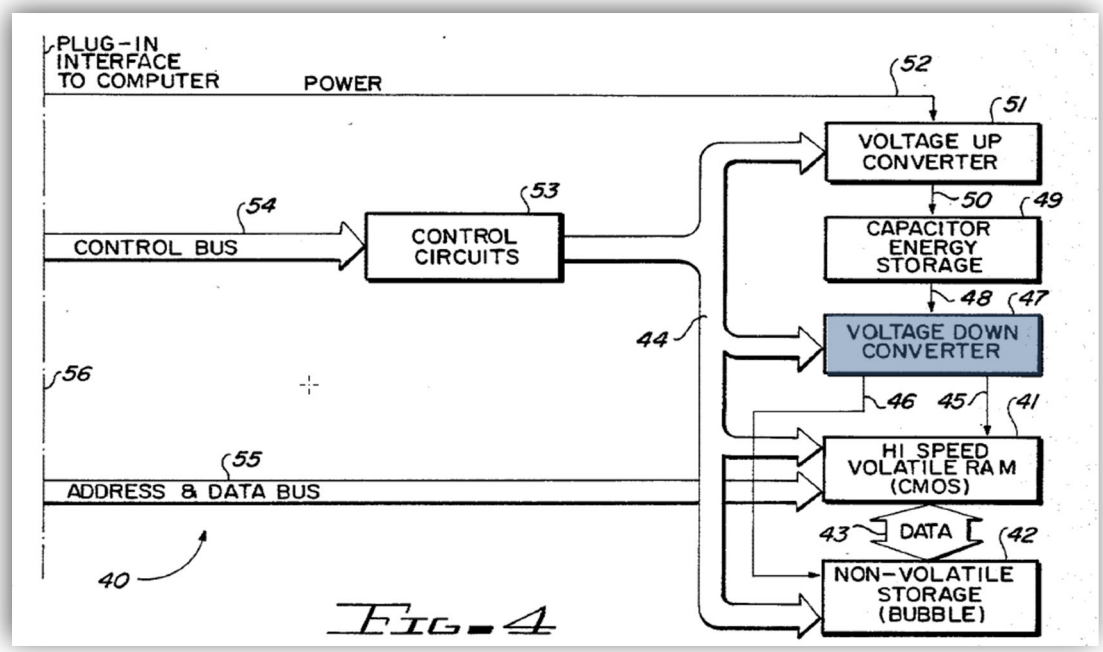
**d. [Claim 10c]: "means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level."**

Bruder renders this claim element obvious in view of Horning further in view of Stokes. Bruder teaches that the capacitor bank supplies power to the down

converter to "temporarily power the control circuitry" while data is being transferred from volatile to non-volatile memory. Ex-1005 at Abstract; 2:35-42; 7:64-66. By teaching that the capacitor bank is only activated "temporarily"—and only for "long enough" to affect a complete data transfer from volatile to non-volatile memory—Bruder indicates that the capacitor bank is deactivated. Bruder also teaches the importance of regulating the power output from the reserve power supply, noting that the capacitors maintain voltage "long enough to allow this transfer of data [from volatile to non-volatile memory] to be accomplished." *Id.* at 7:64-66; 3:40-44; 8:7-10; 10:58-64; Ex-1003, ¶ 224.

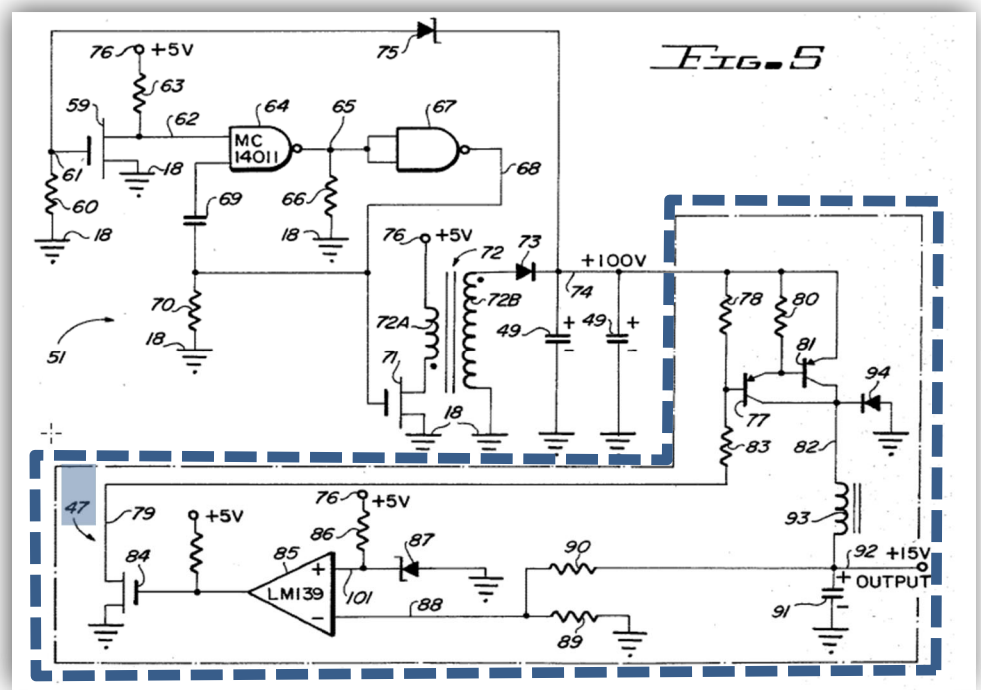
Bruder also discloses the recited "means for deactivating" the capacitor bank, teaching a down-converter to cut off power to the computing engine when the capacitors have discharged to a predetermined level. Bruder teaches that the down-converter "maintains the proper operating voltages" only for long enough to "permit complete transfer of data" from volatile to non-volatile memory. Ex-1005 at 8:7-10; Abstract; 7:64-66. Bruder thus discloses a "voltage down-converter or equivalent structure that converts a high voltage signal to a lower voltage signal" under the Court's construction. Ex-1003, ¶ 225

An illustration of the voltage **down converter (47)** is provided in annotated Figure 4, below:




*Id.*, ¶ 226.

A more detailed diagram of voltage **down-converter (47)** is illustrated in annotated Figure 5, below:




*Id.*, ¶ 227.

As discussed above, Horning discloses a system and method of data protection that includes discharging a reserve power supply to a predetermined level at which it can supply enough power to the computing engine so that it can transfer all the data from the volatile memory array to the non-volatile memory array. *Supra* §§ X.A.1.a, X.A.1.b, X.A.1.c; Ex-1008 8:13-17. Horning teaches that cutting off power from the reserve power supply at that level allows the user to obtain "optimum utilization of the reserve power supply regardless of the capacity of the reserve power supply. *Id.* at 8:6-8; 8:19-24. Horning also discloses that, after all data has been transferred from volatile to non-volatile memory, power is cut off to the computing engine by a circuit that "***removes power*** from the primary, secondary,

and tertiary power conductors . . . thereby ***deactivating the entire data protection system 10***."[12] *Id*. at 9:20-27 (emphasis added); Ex-1003, ¶ 228.

As discussed above, it would have been obvious to a POSITA to include the teachings of Horning, including Horning's functionality for deactivating the reserve power system, in Bruder's data protection system in order to achieve the stated optimum utilization of the reserve power capacitor. *Supra* § X.C.1; Ex-1003, ¶ 228. Furthermore, as discussed above, it would have been obvious to a POSITA to replace Bruder's capacitors with a plurality of Stokes' super capacitors in order to supply sufficient reserve power from a reduced physical volume. *See supra* § X.C.1; Ex.-1003, ¶¶ 228-229.

#### 6. Claim 11 Is Rendered Obvious by Bruder in View of Horning Further in View of Stokes

##### a. [Claim 11]: "The system of claim 10 wherein the computing engine comprises a least one volatile memory and at least one non-volatile memory."

Bruder in view of Horning further in view of Stokes renders obvious the system of claim 10 for the reasons discussed above. *Supra* § X.C.5. Bruder and Horning also render obvious the system of claim 11, as Bruder teaches that the

[12] The reserve power supply is part of, and thus is deactivated with, "data protection system 10." Ex-1008, Figure 1.

computing engine comprises at least one volatile memory (e.g., CMOS RAM) and at least one non-volatile memory (e.g., bubble memory). *See supra* §§ X.C.1.a, X.C.1.c; Ex-1003, ¶ 232.

### 7. Claim 12 Is Rendered Obvious by Bruder in View of Horning Further in View of Stokes

#### a. [Claim 12]: "The system of claim 11 wherein the reconfiguring means further comprises: means for allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory."

Bruder in view of Horning renders obvious the system of claim 11 for the reasons discussed above, *supra* § X.C.6, and also renders obvious the system recited in claim 12. Bruder teaches that "the entire contents" of volatile CMOS RAM are transferred to non-volatile bubble memory in the event of a power failure. Ex-1005 at 7:57-60; 8:2-10; 10:58-64. Bruder also teaches that the control circuitry, which constitutes the means for reconfiguring as explained above, *supra* § X.C.5.c, "generates the necessary signals on bus 44 to . . . achieve the desired data transfer" from volatile memory to nonvolatile memory. *Id*. at 8:37-45; Abstract; 10:54-64; *supra* § X.C.5.c; Ex-1003, ¶¶ 234-237.

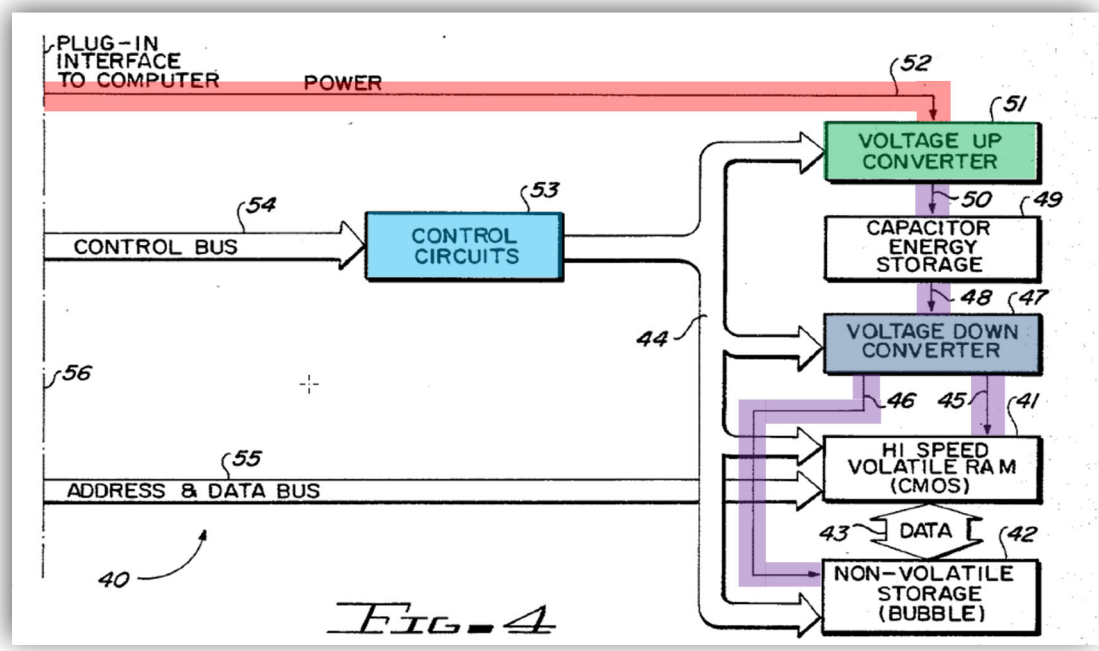
### 8. Claim 15 Is Rendered Obvious by Bruder in View of Horning Further in View of Stokes

#### a. [Claim 15 pre]: "The system of claim 12 wherein the activating means further comprises: means for

**reversing the flow of current between the computing engine and the plurality of super capacitors; and"**

Bruder in view of Horning further in view of Stokes renders obvious the system of claim 12 for the reasons discussed above, *supra* § X.C.7, and also renders obvious the system recited in claim 15.

As illustrated in annotated Figure 4 below, Bruder teaches a **single power bus (52)** that provides power to the **control circuits (53)**, voltage **down converter (47)**, voltage **up converter (51)**, and other components through a series of **conductors (45, 46, 48, and 50)**:




*See also* Ex-1005 at 7:66-8:2; 8:21-24 (explaining that the conductors 45 and 46 supply power to the non-volatile and volatile memory, respectively, and "normally receive their operating power from the main power bus"); 8:21-24; Ex-1003, ¶ 240.

Bruder also discloses both the structure and function for reversing the flow of current pursuant to the district court's construction. Bruder teaches "[a] ***'voltage up' converter circuit*** 51 [that] boosts the normal operating voltage on main power bus 52 to produce the 100 volts needed to charge up capacitor bank 49 and thereby store enough energy in case of a power failure." Ex-1005 at 8:31-36; 8:37-45; 8:60-9:10; 10:6-25. Bruder also teaches "a ***down voltage converter*** that produces a constant, regulated output voltage ***to the control circuitry***, the CMOS memory, and the bubble memory system." *Id*. at 2:35-42 (emphasis added); Abstract. Bruder thus discloses a "down-converter 42 and up-converter 42 in Figure 1 (and corresponding text), and equivalents thereof" under the district court's construction. Ex-1003, ¶ 241.

That this structure reverses power is confirmed by the fact that, as annotated Figure 4 demonstrates, there is no separate power bus to provide power from the down converter to the control circuitry when the capacitors are activated. *Id*., ¶ 243. Accordingly, for the down converter to provide "voltage to the control circuitry" as disclosed in the specification, it would need to reverse the flow of current from the capacitors to the control circuitry over power bus 52 through up-converter 51. *Id*.

**b. [Claim 15b]: "means for discharging current from the plurality of super capacitors to the computing engine."**

Bruder discloses both the function and structure of this claim element. Bruder teaches that, upon activation, power from the capacitors is "discharged into a ***down***

***voltage converter that produces a constant, regulated output voltage*** to the control circuitry, the CMOS memory, and the bubble memory system." Ex-1005 at 2:35-42 (emphasis added); Abstract; 8:11-15. Bruder thus demonstrates that the disclosed down converter is a "voltage down-converter or equivalent structure that converts a high voltage signal to a lower voltage signal and is configured to discharge current from the capacitors to the computing engine" under Petitioners' proposed construction. Ex-1003, ¶ 245.

### D. Ground 4: Claims 1-3 and 6 Are Rendered Obvious by Weber in View of Horning Further in View of Stokes

Weber in view Horning further in view of Stokes teaches, and therefore renders obvious, claims 1-3 and 6 of the '939 patent. As Dr. Baker explains, a POSITA would have been motivated to combine Horning's functionality for deactivating a reserve power supply to cut off power with Weber's data protection system to provide optimal utilization and management of Weber's reserve power supply. Ex-1003, ¶ 247.

Weber and Horning are in the same field, teach analogous solutions to the same issues, and have the purpose of improving data protection and preservation systems. Ex-1003, ¶ 250. Thus, a POSITA would have been motivated to combine these references. *Id*. Weber teaches that as soon as the backup transfer operation has been completed" by transferring all data from volatile to non-volatile memory,

the low-power processor "shuts down to ***conserve power***." Ex-1007 at 9:34-36 (emphasis added). Likewise, Horning teaches optimizing power utilization in a reserve power system using a circuit that "***removes power*** from the primary, secondary, and tertiary power conductors . . . thereby ***deactivating the entire data protection system 10***." Ex-1008 at 9:20-27 (emphasis added); 7:23-27; Ex-1003, ¶ 250. Accordingly, the power optimization benefits taught by Horning directly align with Weber's goals. *Id*. A POSITA would have been motivated to combine Weber's data protection system with Horning's teaching of deactivating and cutting off power from a reserve power system, as this would have allowed Weber's data protection system to leverage the benefits of Horning's power optimization and utilization scheme. *Id*. Furthermore, a POSITA would have been motivated to incorporate a plurality of Stokes' super capacitors into the combination of Weber and Horning in order to provide sufficient power at a reduced physical volume. *See supra* § X.A; Ex-1003, ¶ 250.

### 1. Claim 1 Is Rendered Obvious By Weber in View of Horning Further in View of Stokes

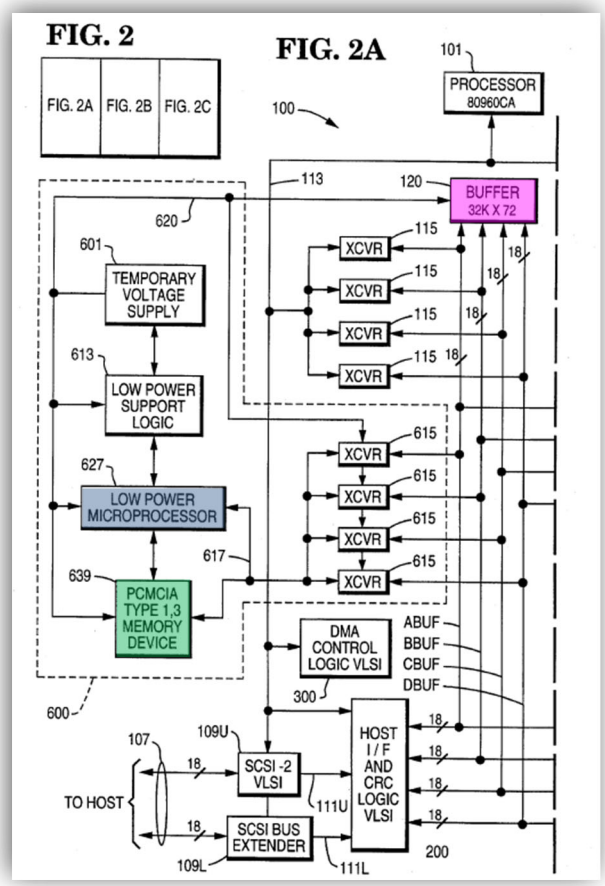
#### a. [Claim 1 Pre]: "A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:"

To the extent the preamble is limiting, Weber discloses this claim element. Weber teaches methods and systems for controlling data in a data storage or disk

array storage system. Ex-1006 at Abstract; 3:51-57; 1:7-9 ("The present invention relates to . . . a method for safeguarding disk array write operations."); 3:31-33 (same); claims 1-9. Weber discloses a computing engine comprising volatile memory (e.g., transfer buffer) as well as non-volatile memory (e.g., PCMCIA flash card or disk drive). *Id*. at Abstract; 3:38-43; 4:16-20; 5:13-20; 7:5-11; 9:15-50; claims 19-20. The computing engine also comprises a low-power microprocessor, which may be a "low power CMOS microcomputer" or a "complex CMOS state machine designed to perform memory transfers." *Id*. at 4:13-16; 7:22-36; 9:25-36. The low-power microprocessor "controls the transfer of data" from volatile memory to non-volatile memory. *Id*. at 7:5-8. Weber's low-power microprocessor is thus a "processor or equivalent structure that directs the transfer and storage of data in memory and is configured to transfer all data from volatile to non-volatile memory" under Petitioners' proposed construction. Ex-1003, ¶ 255.

Weber teaches that this system "monitor[s] the voltage provided by the primary voltage source." *Id*. at 9:15-17. When the system detects a failure, data is transferred from volatile memory to non-volatile memory, thereby ensuring that the data is not erased. *Id*. at 9:59-63. Ex-1003, ¶ 256.

The **low power microprocessor**, **volatile memory**, and **nonvolatile memory** are illustrated in annotated Figure 2A below:




Ex-1003, ¶ 257.

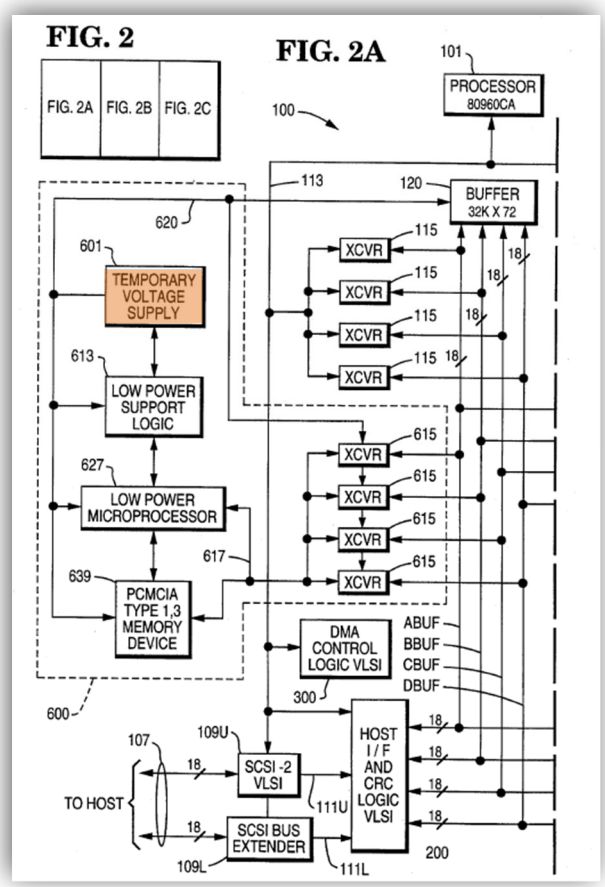
**b. [Claim 1a]: "activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;"**

Weber renders this claim element obvious in view of Stokes. Weber discloses a "temporary voltage source" in the form of a "high capacitance gold capacitor," which has "an extremely high capacitance value." Ex-1006 at Abstract; 4:5-10; 6:65-7:2; 7:17-21. Numerous claims also recite that the temporary voltage source "comprises ***a*** gold capacitor for supplying power." *See, e.g.*, *id*. at claims 7, 10, and 26 (emphasis added.). The use of the indefinite article "a" in a claim means "one or

more." As a result, by claiming "***a*** gold capacitor," Weber discloses a plurality of capacitors. Ex-1003, ¶ 259.

When the external voltage drops, Weber also teaches that backup logic, which includes the temporary voltage source (i.e., the capacitor), is activated to "assume control of the disk array system." *Id*. at 9:14-25; 3:24-27; 6:65-7:2. Weber thus teaches activating the capacitors to supply power to the computing engine based upon power being removed from the computer system. Ex-1003, ¶ 259.

The **temporary voltage supply (comprising capacitors)** is illustrated in annotated Figure 2A, below:




*Id.*, ¶ 261.

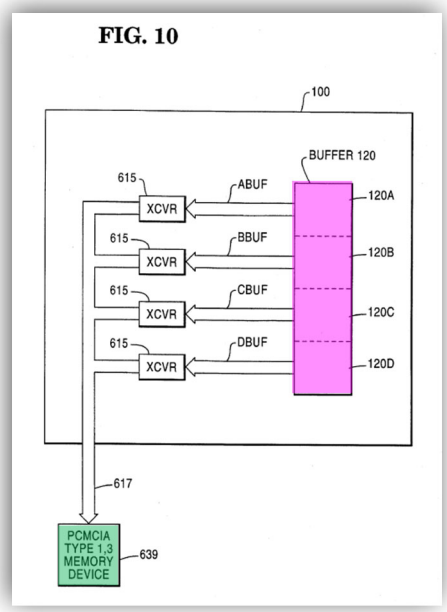
Although Weber does not refer to the capacitors as "super capacitors," use of super-capacitors in Weber's invention would have been obvious in view of Stokes. *Id.*, ¶¶ 114-115, 262.[13] As discussed above, super-capacitors would have been well-known to a POSITA at the time that that '939 patent was filed, and were also known to provide more capacitance in a smaller form factor. *Supra* § IX.E; Ex-1003, ¶¶ 114-115, 262. Moreover, as also discussed above, a POSITA would have known

[13] The '939 patent does not define what a super-capacitor is. *Supra* Footnote 6.

that super-capacitors could be used electronic systems and circuits. Ex-1003, ¶¶ 114-115, 262. Thus, using a "super-capacitor" in place of a "capacitor" would have been obvious to a POSITA based on Stokes' teachings, particularly given Weber's disclosure that the capacitors need to have sufficient capacity to power the computing engine, and ensure the complete transfer of data to non-volatile memory, in the event of power loss. *See, e.g.*, § IX.E *supra* (discussing characteristics of super capacitors); Ex-1003, ¶¶ 114-115, 262.

**c. [Claim 1b]: "reconfiguring the data in the computing engine;"**

Weber discloses that data in the computing engine is reconfigured by "transfer[ring] data residing in the [volatile] transfer buffer to the non-volatile" memory upon a loss of power. Ex-1006 at 4:1-3; 3:24-27; 3:38-43; 9:25-28; Ex-1003, ¶ 264. The transfer of data from **volatile memory** (transfer buffer), through a series of data buses, to **non-volatile memory** (e.g., PCMCIA flash card or disk drive) is illustrated in annotated Figure 10, below:




Ex-1003, ¶ 265.

**d. [Claim 1c]: "deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level."**

Weber in view of Horning further in view of Stokes renders this claim element obvious. Weber teaches that, once "the backup transfer operation has been completed" by transferring all data from volatile to non-volatile memory, the low-power processor "shuts down to conserve power." Ex-1006 at 9:34-36. The processor "shut[ting] down to conserve power" suggests that the capacitors are deactivated to cut off power to the computing engine. Ex-1003, ¶ 267.

As explained above, however, Horning discloses a system and method of data protection that includes discharging a reserve power supply to a predetermined level

at which it can supply enough power to the computing engine so that it can transfer all the data from the volatile memory array to the non-volatile memory array. *Supra* §§ X.A.1.a, X.A.1.b, X.A.1.c; Ex-1008 at 8:13-17. Horning teaches that cutting off power from the reserve power supply at that level allows the user to obtain "optimum utilization of the reserve power supply regardless of the capacity of the reserve power supply. *Id*. at 8:6-8; 8:19-24. Horning also discloses that, after all data has been transferred from volatile to non-volatile memory, power is cut off to the computing engine by a circuit that "***removes power*** from the primary, secondary, and tertiary power conductors . . . thereby ***deactivating the entire data protection system 10***."[14] *Id*. at 9:20-27 (emphasis added); Ex-1003, ¶ 268.

As discussed above, it would have been obvious to a POSITA to include the teachings of Horning, including Horning's functionality for deactivating the reserve power system, in the system and method of Weber in order to achieve the stated optimum utilization of the reserve power capacitor in Weber. Ex-1003, ¶ 268. Furthermore, as discussed above, it would have been obvious to a POSITA to replace Weber's capacitors with a plurality of Stokes' super capacitors in order to supply sufficient reserve power from a reduced physical volume. *See supra* § X.D; Ex-

[14] The reserve power supply is part of, and thus is deactivated with, "data protection system 10." Ex-1008, Figure 1.

1003, ¶ 268.

### 2. Claim 2 Is Rendered Obvious By Weber in View of Horning Further in View of Stokes

#### a. [Claim 2 pre]: "The method of claim 1 wherein the computing engine comprises a least one volatile memory and at least one non-volatile memory."

Weber in view of Horning further in view of Stokes renders obvious the method of claim 1 for the reasons discussed above. *Supra* § X.D.1. Weber and Horning also render obvious the method of claim 2, as Weber discloses that the computing engine comprises at least one volatile memory (e.g., transfer buffer) and one non-volatile memory (PCMCIA memory). *See supra* §§ X.D.1.a, X.D.1.c; Ex-1003, ¶ 271.

### 3. Claim 3 Is Rendered Obvious by Weber in View of Horning Further in View of Stokes

#### a. [Claim 3]: "The method of claim 2 wherein the reconfiguring step (b) further comprises: (b1) allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory."

Weber in view of Horning further in view of Stokes renders obvious the method of claim 2 for the reasons discussed above, *supra* § X.D.2, and also renders obvious the method of claim 3.

Weber discloses that the transfer of data from volatile to non-volatile memory

"safeguard[s] disk array early write operations, thereby preventing the loss of data resulting from the occurrence of a power failure." Ex-1006 at 9:59-63; 3:24-27; Claim 1. A POSITA would readily understand that in order to "prevent the loss of data" and "safeguard" all early write operations, the system disclosed in Weber would need to transfer all data from the volatile memory to the non-volatile memory. Ex-1003, ¶ 275.

As discussed above, Horning also discloses that the data transfer task allows for all the data from the volatile memory array to be transferred to the non-volatile memory array. *Supra* §§ X.A.1.a, X.A.1.b, X.A.1.c; Ex-1008 at 7:30-34. Horning further confirms that the power is not removed from the data protection system until after "***all the data*** [has] been transferred." *Id*. at 9:23-27 (emphasis added); Ex-1003, ¶ 276.

#### 4. Claim 6 Is Rendered Obvious by Weber in View of Horning Further in View of Stokes

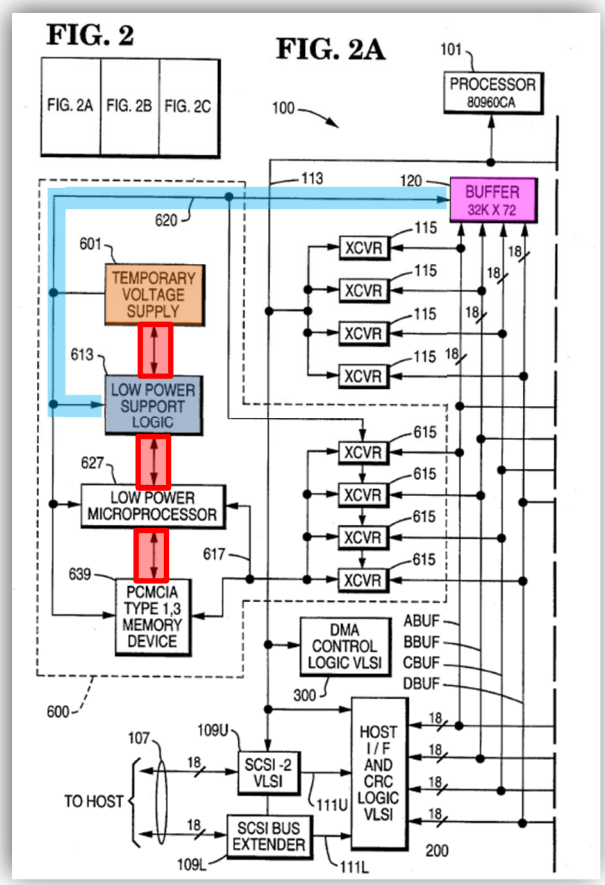
##### a. [Claim 6a]: "The method of claim 3 wherein the activating step (a) further comprises: reversing the flow of current between the computing engine and the plurality of super capacitors; and"

Weber in view of Horning renders obvious the method of claim 3 for the reasons discussed above, *supra* § X.D.3, and also renders obvious the method of claim 6.

Weber discloses that, upon loss of power, backup logic "assumes control" of

the system. Ex-1006 at 9:17-22. The backup logic includes "low power support logic," which—together with a power bus 620—provides "continuous power and refresh for the transfer buffer . . . as well as power to the components included in the backup logic." *Id*. at 7:2-5; 9:23-25; Ex-1003, ¶ 280.

Annotated Figure 2A, below, illustrates both the **low power support logic**, **temporary voltage supply (capacitors)**, and **volatile memory**:




Ex-1003, ¶ 281.

As illustrated in annotated Figure 2A, there is a **bi-directional flow** between the **low power support logic** and the other components, including the **capacitors**,

confirming that voltage is reversed between these components. In addition, for the low power support logic and power bus to "provide continuous power and refresh for the transfer buffer" as required by the specification, voltage from the **low power support logic** would necessarily have to be reversed on the **power bus** to the **transfer buffer (volatile memory)**. Ex-1003, ¶ 282.

#### b. [Claim 6b]: "discharging current from the plurality of super capacitors to the computing engine."

Weber discloses that voltage stored on the capacitors is discharged to provide "continuous power" to the computing engine, including the transfer buffer and all "other components included in the backup logic." Ex-1006 at 6:65-7:5; Abstract; 9:15-36; Fig. 2A; Claims 4, 7, 8; Ex-1003, ¶ 284.

## XI. INSTITUTION SHOULD NOT BE DISCRETIONARILY DENIED

### A. The Board Should Not Exercise Its Discretion Under 35 U.S.C. § 314(a)

Petitioners hereby stipulate that, should the Petition be granted, they will not pursue in the district court the same grounds that are raised or could have reasonably been raised in this Petition pursuant to *Sotera Wireless, Inc., v. Masimo Corp.* IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020) (precedential as to § II.A). Under the June 21, 2022, *Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation*, the Director has stated that "the

PTAB will not discretionarily deny institution of on an IPR" in view of such a stipulation. Interim Procedures at 7; *id*. at 3 and n.3 (discussing *Sotera*).

Accordingly, Petitioners' stipulation is dispositive in establishing that institution should not be discretionarily denied pursuant to 35 U.S.C. § 314(a).

### B. The Board Should Not Exercise Its Discretion under 35 U.S.C. § 325(d)

In evaluating arguments under § 325(d), [the PTAB] use[s] a two-part framework: (1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of the first part of the framework is satisfied, whether the petition has demonstrated that the Office erred in a manner material to the patentability of challenged claims." *The Data Co. Techs., Inc. v. Bright Data Ltd.*, IPR2022-00135, Paper 12 at 15 (PTAB June 1, 2022) (citing *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020).

Here, none of Horning, Stokes, Germer, Bruder, or Weber were presented to the Office during examination of the application that led to the '939 patent. Nor were any other prior art or arguments substantially similar to those presented in this Petition presented to the Office. Thus, the *Advanced Bionics* framework does not apply because the first part is not satisfied. *Id.* at 17 (Where "the first part of the

*Advanced Bionics* framework is not satisfied, [the Board] need not consider the second part of the framework.”).

## XII. MANDATORY NOTICES

### A. Real Parties in Interest—37 C.F.R. § 42.8(b)(1)

The following entities are real parties in interest to this proceeding: KIOXIA Corporation and KIOXIA America, Inc. No other parties had access to or control over this Petition, and no other parties funded this Petition.

### B. Related Matters—37 C.F.R. § 42.8(b)(2)

To the best of Petitioner’s knowledge, the ’939 patent has been or is involved in the following cases:

- *BiTMICRO LLC v. KIOXIA Am. Inc., et al.*, Case NO. 6:22-cv-00331 (W.D. Tex. 2022). This case is ongoing.
- *BiTMICRO LLC v. Intel Corp.*, Case No. 5:23-cv-00625 (N.D. Cal.), which was transferred from the District Court for the Western District of Texas, Case No. 6-22-cv-00335. This case is ongoing.

Petitioner is not aware of any other matters involving the ’939 patent.

### C. Lead and Back-Up Counsel—37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

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### D. Service Information—37 C.F.R. § 42.8(b)(4)

Please address all correspondence and service to the address listed above. Petitioner consents to electronic service by email at Bracewell-IP@bracewell.com

## XIII. CONCLUSION

The prior art references cited herein demonstrate that the challenged claims of the ’939 patent are unpatentable. Petitioners thus request that the PTAB grant this Petition, institute *inter partes* review, and invalidate the challenged claims.

Respectfully Submitted,

Dated: March 23, 2023

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*Counsel for Petitioners*

## CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24, the undersigned certifies that the foregoing Petition for *Inter Partes* Review contains 13,687 words excluding the caption, table of contents, table of authorities, table of exhibits, claim listing, mandatory notices, certificate of service, and certificate of word count. Petitioner has relied on the word count feature of the word processing system used to create this paper in making this certification.

Dated: March 23, 2023

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## CERTIFICATE OF SERVICE

I hereby certify that on March 23, 2023, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review, associated exhibits, and power of attorney to be served via overnight courier upon the following counsel of record for Patent Owner per 37 CFR §§ 42.105(a) and 42.205(a).

| Patent Office Counsel of Record | Litigation Counsel of Record |
|---|---|
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I further certify that I served courtesy copies of the foregoing documents via electronic mail on March 23, 2023, upon Patent Owner's counsel of record as follows:

| Patent Office Counsel of Record | Litigation Counsel of Record |
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