

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KIOXIA AMERICA, INC. and KIOXIA CORPORATION,
Petitioner,

v.

BITMICRO, LLC,
Patent Owner.

IPR2023-00743
Patent 6,496,939 B2

Before KEN B. BARRETT, TERRENCE W. McMILLIN, and
KEVIN C. TROCK, *Administrative Patent Judges*.

TROCK, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

KIOXIA Corporation and KIOXIA America, Inc. (collectively, “Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting *inter partes* review of claims 1–3, 6, 10–12, and 15 (the “challenged claims”) of U.S. Patent No. 6,496,939 B2 (Ex. 1001, “the ’939 patent”). BiTMICRO, LLC (“Patent Owner”) filed a Preliminary Response (Paper 7, “Prelim. Resp.”).

The Board has authority to determine whether to institute *inter partes* review. *See* 35 U.S.C. § 314; 37 C.F.R. § 42.4(a). Under 35 U.S.C. § 314(a), we may not authorize an *inter partes* review unless the information in the petition and the preliminary response “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

For the reasons stated below, we determine that Petitioner has established a reasonable likelihood that it would prevail with respect to at least one claim. We therefore institute *inter partes* review as to all of the challenged claims of the ’939 patent and all of the asserted grounds of unpatentability in the Petition.

II. BACKGROUND

A. Related Matters

The parties identify the following district court proceedings involving the ’939 patent: *BiTMICRO LLC v. KIOXIA Am. Inc., et al.*, No. 6:22-cv-00331 (W.D. Tex.); *BiTMICRO LLC v. Intel Corp.*, No. 5:23-cv-00625 (N.D. Cal.). Pet. 76; Paper 5, 2. Patent Owner also identifies another related USPTO proceeding: IPR2023-00783 (PTAB), involving the ’939 patent. Paper 5, 2.

B. Real Parties-in-Interest

Petitioner identifies KIOXIA Corporation and KIOXIA America, Inc. as the real parties-in-interest. Pet. 76. Patent Owner identifies BiTMICRO, LLC, as the real party-in-interest. Paper 5, 2.

Based on the current record, we determine that Petitioner has established compliance with the statutory requirement under 35 U.S.C. § 312(a)(2) to identify all real parties in interest.

C. The '939 Patent

The '939 patent is entitled “Method and System for Controlling Data in a Computer System in the Event of a Power Failure.” Ex. 1001, code (54). According to the '939 patent, when there is a sudden loss of external power to a computer system there is insufficient time to safely write all the newly written and modified data from the computer's volatile memory to the computer's data storage mechanism before the computer system shuts down. *Id.* at 1:34–38. The '939 patent explains that in accordance with the invention, “if a system is in ‘save mode’ and is subsequently subjected to a sudden power loss, first, the super-capacitors are activated to maintain the internal power of the system.” *Id.* at 5:8–11. The '939 patent goes on to explain that “data from the volatile memory is transferred to the non-volatile memory . . . [so that] a user is able to quickly and correctly transfer all data from volatile memory to non-volatile memory in the event of a sudden power loss.” *Id.* at 5:11–16.

Figure 1, reproduced below, shows a schematic of the '939 patent's system.

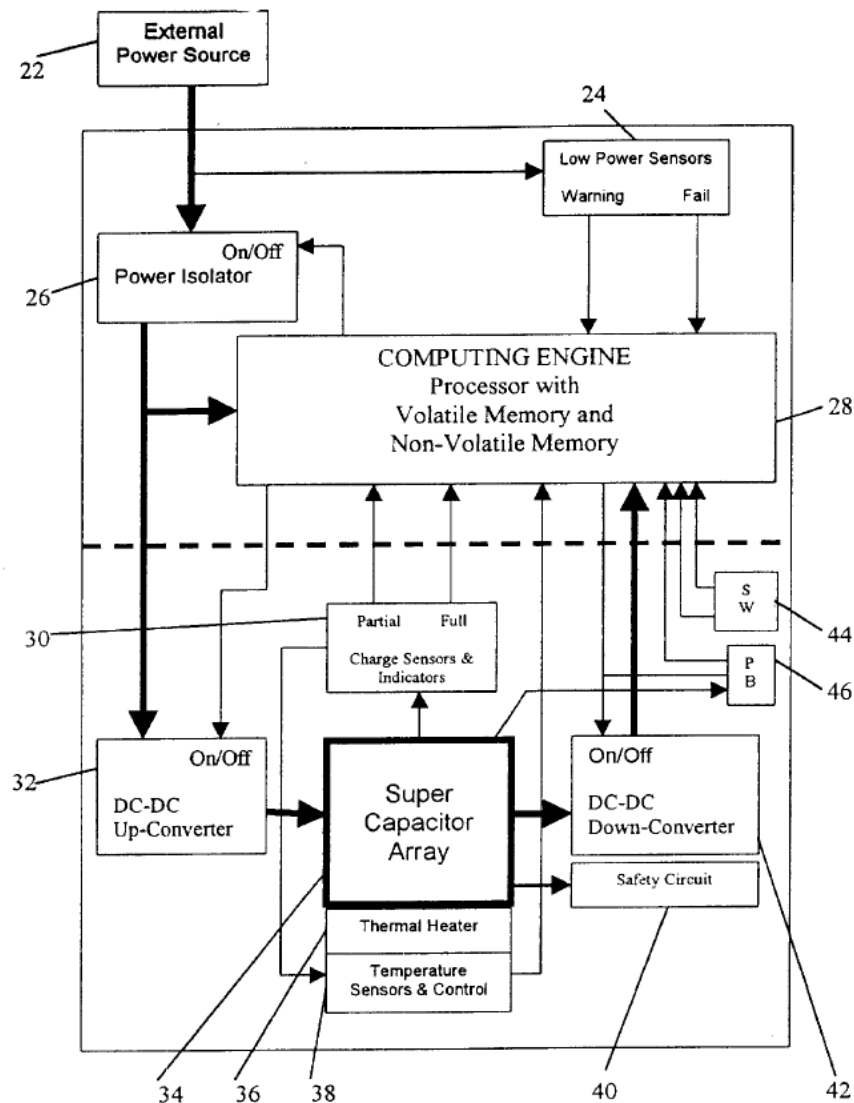


Figure 1, above, shows computing engine 28 comprising a processor with volatile memory and non-volatile memory, external power source 22, power isolator 26, DC-DC up-converter 32, DC-DC down-converter 42, and super capacitor array 34. *Id.* at 3:33–41.

The '939 patent explains that “[w]hile the computer system is receiving current from the super-capacitors, data is transferred from the volatile memory to the non-volatile memory,” but “once the super-capacitors discharge to a pre-determined level, the down-converter has insufficient

voltage differential to continue proper operation and shuts down, thus turning off the power to the computer system.” *Id.* at 5:33–43.

The ’939 patent explains that this shut down has two positive side effects. “First,” the patent explains, “if the output voltage from the down-converter were allowed to fall below the minimum operating voltage of the computer system, the computer system could continue to run with unpredictable and potentially serious results.” *Id.* at 5:44–48. Second, “by not fully discharging the super-capacitors they will take only a few seconds to recharge once the external system power is restored, whereas the initial charge of super-capacitors may take up to 5 minutes.” *Id.* at 5:48–52.

D. Illustrative Claim

The ’939 patent has 28 claims. As noted, claims 1–3, 6, 10–12, and 15 are challenged in the Petition. Pet. 1. Claim 1, a method claim, and claim 10, a system claim, are independent. Ex. 1001, 7:20–10:34. Claim 1 is illustrative of the claimed subject matter and is reproduced below:¹

1. [Pre] A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of:

[1a] activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;

[1b] reconfiguring the data in the computing engine; and

[1c] deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.

Ex. 1001, 7:20–31.

¹ Paragraph references in brackets proposed by Petitioner. See Pet. ix–x.

E. Prior Art References and Other Evidence

Petitioner relies on the following references:

1. Horning, U.S. Patent No. 5,414,861 (May 9, 1995) (Ex. 1008, “Horning”).
2. Stokes et al., U.S. Patent No. 4,701,858 (Oct. 20, 1987) (Ex. 1013, “Stokes”).
3. Germer, U.S. Patent No. 4,591,782 (May 27, 1986) (Ex. 1007, “Germer”).
4. Bruder, U.S. Patent No. 4,559,616 (Dec. 17, 1985) (Ex. 1005, “Bruder”).
5. Weber, U.S. Patent No. 5,596,708 (Jan. 21, 1997) (Ex. 1006, “Weber”).

In addition to these references, Petitioner relies on a Declaration of Dr. R. Jacob Baker. Ex. 1003.

F. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability. Pet. 3.

Claim(s) Challenged	Basis 35 U.S.C. §	Reference(s)
1–3	103(a) ²	Horning, Stokes
1–3	103(a)	Germer, Horning, Stokes
1–3, 6, 10–12, 15	103(a)	Bruder, Horning, Stokes
1–3, 6	103(a)	Weber, Horning, Stokes

² Because the application from which the ’939 patent issued has an effective filing date before March 16, 2013 (Ex. 1001, code (22)), citations to 35 U.S.C. § 103 are to the pre-AIA version. Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29.

III. ANALYSIS OF THE CHALLENGED CLAIMS

A. *Applicable Legal Standards*

A claim is unpatentable as obvious under 35 U.S.C. § 103 “if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains.” 35 U.S.C. § 103 (2011). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) so-called “secondary considerations,” including commercial success, long-felt but unsolved needs, failure of others, and unexpected results. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). At this stage, neither party has presented any evidence on the fourth *Graham* factor.

B. *Level of Ordinary Skill in the Art*

According to Petitioner, a person of ordinary skill in the pertinent art “would have had at least a Bachelor’s degree in electrical or computer engineering, or a similar field, and at least two years of work experience in the computer memory or data storage industry.” Pet. 7 (citing Ex. 1003 ¶¶ 64–67). The ordinary artisan “could have substituted less formal education with additional relevant work experience, and vice versa.” *Id.*

Patent Owner does not address the level of skill of the ordinary artisan. *See generally* Prelim. Resp.

We regard Petitioner’s definition as consistent with the ’939 patent and the prior art before us. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355

(Fed. Cir. 2001) (prior art itself may reflect an appropriate level of skill). Therefore, for the purpose of this decision, we adopt Petitioner’s formulation.

C. Claim Construction

For this *inter partes* review, the Board applies the same claim construction standard as that applied in federal courts. *See* 37 C.F.R. § 42.100(b) (2019). Under this standard, claim terms “are generally given their ordinary and customary meaning” as understood by a person of ordinary skill in the art in question at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc) (citations omitted). “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). Extrinsic evidence is “less significant than the intrinsic record in determining ‘the legally operative meaning of claim language.’” *Phillips*, 415 F.3d at 1317 (citation omitted).

Some of the challenged claims make use of “means-plus-function” claiming. *See* 35 U.S.C. § 112, ¶ 6. Means-plus-function claiming occurs when a claim term is drafted in a manner that invokes 35 U.S.C. § 112, ¶ 6, which states:

An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

See 35 U.S.C. § 112, ¶ 6; *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1347 (Fed. Cir. 2015) (en banc).

On the record before us, we have not been directed to any dispute between the parties that § 112, ¶ 6 does not apply to the “means for” clauses recited in the challenged claims. Where claim language may be construed according to 35 U.S.C. § 112(f) (or its predecessor, § 112, ¶ 6), a petitioner must provide a construction that includes both the claimed function and the specific portions of the specification that describe the structure, material, or acts corresponding to each claimed function. 37 C.F.R. § 42.104(b)(3).

In accordance with these requirements, Petitioner provides specific constructions for all the means-plus-function clauses in the challenged claims. *See* Pet. 7–16. Petitioner also proposes construction for the terms “predetermined level” recited in independent claims 1 and 10, “computing engine” or “computer engine” recited in claims 1, 2, 6, 10, 11, and 15, and “reversing the flow . . . of super capacitors” recited in claim 6. *Id.* Where applicable, Petitioner asserts its proposed constructions are consistent with constructions made by the district court in related litigation. *Id.*; *see also* Ex. 1009.

Patent Owner contends “the Board need not engage in any pre-institution claim construction,” does not substantively address or contest Petitioner’s proposed claim constructions, and does not propose any constructions itself. *See* Prelim. Resp. 6–10.

Based on the record before us, we adopt, for purposes of this Decision, Petitioner’s unopposed proposed claim constructions. “[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’” *Nidec Motor Corp. v. Zhongshan Broad Ocean*

Motor Co. Ltd., 868 F.3d 1013, 1017 (Fed. Cir. 2017) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

This initial claim construction determination does not preclude the parties from arguing their proposed constructions of the claims during trial. Indeed, the parties are hereby given notice that claim construction, in general, is an issue to be addressed at trial. Claim construction will be determined at the close of all the evidence and after any hearing. The parties are expected to assert all their claim construction arguments and evidence in the Petition, Patent Owner’s Response, or otherwise during trial, as permitted by our rules.

1. *“predetermined level”*

Petitioner proposes that “predetermined level,” recited in claims 1 and 10, should be construed consistent with the district court as having a plain and ordinary meaning. Pet. 9 (citing Ex. 1009). Patent Owner does not provide a construction. Prelim. Resp. 6–10.

2. *“computing engine” or “computer engine”*

Petitioner proposes that these terms, recited in claims 1, 2, 6, 10, 11, and 15, “should be construed as comprising a processor or similar structure for directing the transfer and storage of data in memory, volatile memory, and non-volatile memory.” Pet. 9. Patent Owner does not provide a construction. Prelim. Resp. 6–10.

3. *“means for activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system”*

Petitioner proposes that this term, recited in claim 10, should be construed as means-plus-function, with a recited function being “activating a plurality of super capacitors to supply power to the computing engine based

upon power being removed from the computer system,” and the corresponding structure being a “down-converter and up-converter, and equivalents thereof, together with associated circuit components.” Pet. 11. Patent Owner does not provide a construction. Prelim. Resp. 6–10.

4. *“means for reconfiguring the data in the computing engine”*

Petitioner proposes that this term, recited in claim 10, should be construed as means-plus-function, with a recited function being “reconfiguring the data in the computing engine,” with the corresponding structure being a “processor or equivalent structure that directs the transfer and storage of data in memory.” Pet. 12. Patent Owner does not provide a construction. Prelim. Resp. 6–10.

5. *“means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level”*

Petitioner proposes that this term, recited in claim 10, should be construed consistent with the district court construction as means-plus-function, with the recited function being “deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level” and the corresponding structure as “down-converter 42 in Figure 1 (and corresponding text) and equivalents thereof, and switches, transistors, gates, etc. that are generally known in the art.” Pet. 12–13. Patent Owner does not provide a construction. Prelim. Resp. 6–10.

6. *“means for allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory”*

Petitioner proposes that this term, recited in claim 12, should be construed as means-plus-function with the recited function being “allowing all data to be transferred from the at least one volatile memory to the at least one non-volatile memory” and the corresponding structure being a “processor or equivalent structure that directs the transfer and storage of data in memory and is configured to transfer all data from volatile to non-volatile memory.” Pet. 13. Patent Owner does not provide a construction. Prelim. Resp. 6–10.

7. *“reversing the flow of current between the computing engine and the plurality of super capacitors”*

Petitioner proposes that this term, recited in claim 6, should be given its plain and ordinary meaning consistent with the district court construction. Pet. 14 (citing Ex. 1009, 23–24, 46). Patent Owner does not provide a construction. Prelim. Resp. 6–10.

8. *“means for reversing the flow of current between the computing engine and the plurality of super capacitors”*

Petitioner proposes that this term, recited in claim 15, should be construed consistent with the district court construction as means-plus-function with the recited function being “reversing the flow of current between the computing engine and the plurality of super capacitors” and the corresponding structure being “down-converter 42 and up-converter [32] in Figure 1 (and corresponding text), and equivalents thereof.” Pet. 14 (citing Ex. 1009, 26, 47). Patent Owner does not provide a construction. Prelim. Resp. 6–10.

9. “means for discharging current from the plurality of super capacitors to the computing engine”

Petitioner contends that this term, recited in claim 15, should be construed as means-plus-function, with the recited function being “discharging current from the plurality of super capacitors to the computing engine,” and the corresponding structure being a “voltage down-converter or equivalent structure that converts a high voltage signal to a lower voltage signal and is configured to discharge current from the capacitors to the computing engine.” Pet. 14–15. Patent Owner does not provide a construction. Prelim. Resp. 6–10.

D. Prior Art References

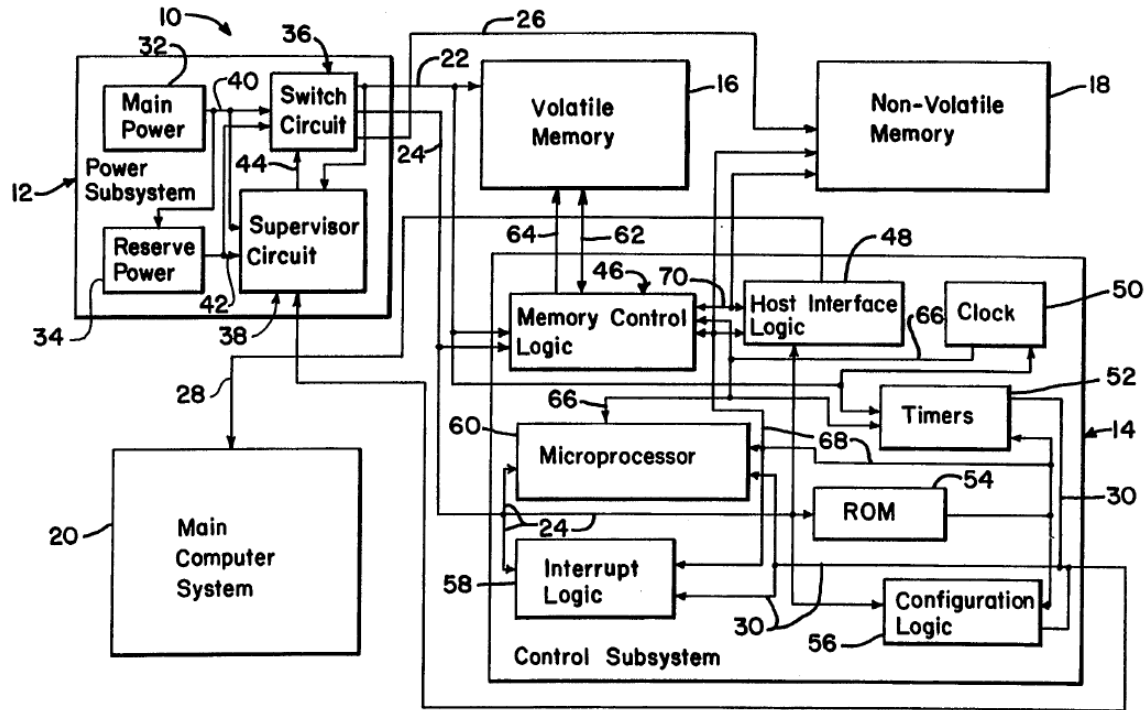
1. *Horning (Ex. 1008)*

Horning is a patent titled “Data Protection System Using Different Levels of Reserve Power to Maintain Data in Volatile Memories for Any Period of Time.” Ex. 1008, code (54). Horning “relates to data protection systems for computer systems in general, and more particularly to a data protection system having user programmable power sequences to efficiently manage the limited power available from a reserve power supply.” *Id.* at 1:9–14.

Horning explains that in computers that use dynamic random-access memory (“DRAM”) chips for temporary data storage, “if the electrical power to the DRAM array and the data refreshing apparatus is interrupted, even momentarily, the data stored in the DRAM array will be lost forever and must be replaced or reconstructed before computer operations can resume.” *Id.* at 1:40–45. Horning indicates a need for “a data protection system [which] should be capable of temporarily powering the volatile memory arrays to allow the computer system to be rapidly restored to

operation following short power outages, and yet ensure full data integrity by storing the data in non-volatile memory in the event the power failure is of long duration.” *Id.* at 3:62–68.

Figure 1, reproduced below, shows a schematic of Horning’s data protection system.



Horning’s Figure 1, above, shows a data protection system that comprises “power subsystem 12 and a control subsystem 14 that are connected to each other and to a volatile memory 16, a non-volatile memory 18, and a main computer system 20.” *Id.* at 5:51–56. “[T]he power subsystem 12 supplies power to certain selected portions of the control subsystem 14, the volatile memory array 16 of the solid-state disk drive system (not shown), and the non-volatile or back-up memory array 18 via primary, secondary, and tertiary power conductors 22, 24, and 26.” *Id.* at 6:9–17.

Horning explains that in a lengthy power outage, its system will “direct the supervisor circuit 38 to connect the reserve power supply 34 to the tertiary power conductor 26 to energize the non-volatile memory 18, such as a magnetic disk drive or tape unit.” *Id.* at 7:14–18. “Then, after these components have been energized, the data protection system 10 will begin transferring data from the volatile memory 16 to the non-volatile memory array 18 while there is still enough power in the reserve power supply 34 to accomplish this data transfer.” *Id.* at 7:18–23. Horning also explains that its system monitors the status of its reserve power system, and if “there is only enough energy to accomplish the data transfer task, the data protection system 10 will automatically initiate the data transfer process to ensure complete data integrity.” *Id.* at 8:9–19. “Then, after all the data have been transferred, the supervisor circuit 38 removes power from the primary, secondary, and tertiary power conductors 22, 24, and 26, respectively, thereby deactivating the entire data protection system 10.” *Id.* at 9:23–27.

According to Horning, “a given battery in the reserve power supply 34 will safely power the system 10 in either power sequence 74 or reduced power sequence 76 until it reaches some safe minimum voltage level, at which point there will only be enough energy left in the battery to just safely complete the data transfer process.” *Id.* at 13:43–48. “The specific safe minimum voltage level will, of course, depend on the particular discharge curve of the battery in the reserve power supply and on the energy required by the various components of the system 10 to complete the data transfer process during power load sequence 78.” *Id.* at 13:49–54.

Horning explains that “the determination of such a safe minimum voltage would be obvious to persons having ordinary skill in this art based

on these factors and such a person could then select the proper values for resistors 214 and 216 to provide the comparator 212 with the safe minimum voltage as a reference voltage.” *Id.* at 13:54–59. Horning further explains that “[i]f the voltage of the reserve power supply falls below the predetermined safe minimum voltage, the output of comparator 212 will be negative, thus turning off transistor 220 and driving the power supply status line 30 ‘high’ (logic level 1).” *Id.* at 13:66–14:3.

2. *Stokes (Ex. 1013)*

Stokes is a patent entitled “Nonvolatile Realtime Clock Calendar Module.” Ex. 1013, code (54). Stokes “relates generally to an electronic module for use with an electronic time-of-use utility meter,” and “computes real-time clock calendar information and maintains the computation function throughout the duration of long-term power outages without the necessity for a backup battery power source.” *Id.* at 1:6–14.

Stokes describes that “microcomputer based systems compute and maintain real-time clock calendar (RTCC) information either as a primary or secondary function. Prevalent examples are microcomputer based digital clocks, digital thermostats, microwave ovens and video cassette recorders.” *Id.* at 1:22–28. Further, the “realtime clock in a time-of-use meter must maintain accurate time data through long term power outages,” sometimes as much as 72 hours. *Id.* at 1:31–33, 2:32–36. Stokes discloses the use of “the Electric Double Layer capacitor commonly called ‘super capacitor’ which is manufactured by NEC Electronics U.S.A., Inc. and Panasonic, Inc.” *Id.* at 2:63–67. Stokes “combines a very low power CMOS integrated circuit dedicated to RTCC computation with a DLC capacitor as a secondary power supply.” *Id.* at 3:30–33.

3. *Germer (Ex. 1007)*

Germer is entitled “Power Supply and Power Monitor for Electric Meter.” Ex. 1007, code (54). Germer relates to “to power supplies and power monitors for electronic demand registers of electric meters.” *Id.* at 1:6–8. Germer describes that

[a]n electronic register for an electric meter includes a non-volatile storage into which data is written upon the detection of an impending power outage. A sufficient quantity of electric energy is normally stored in a capacitor to continue operation of the electronic register for a long enough period of time to complete the writing of data to the non-volatile storage.

Id. at Abstract.

Figure 3, reproduced below, shows a block diagram of Germer’s power supply and power monitor.

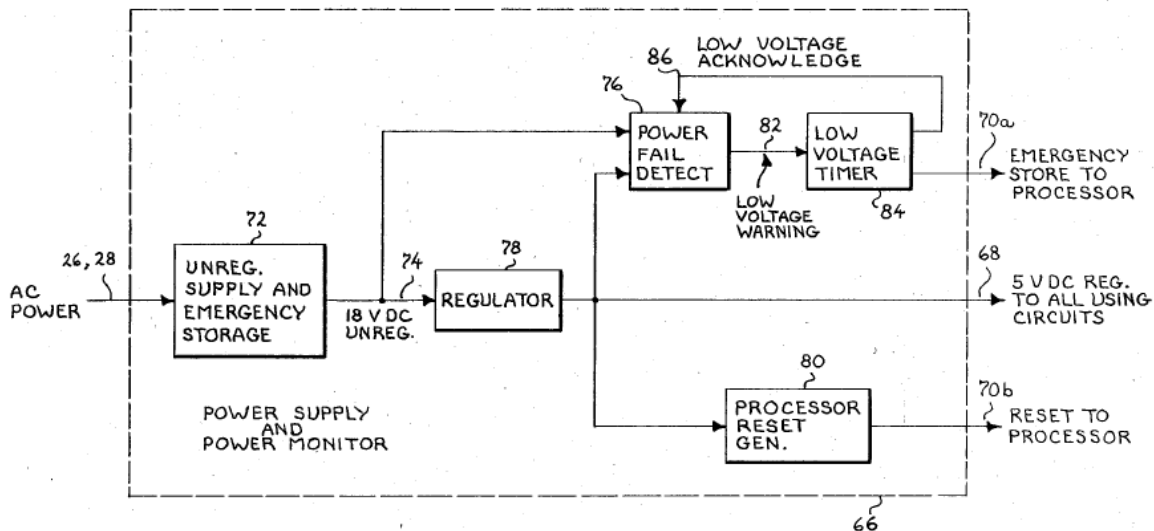


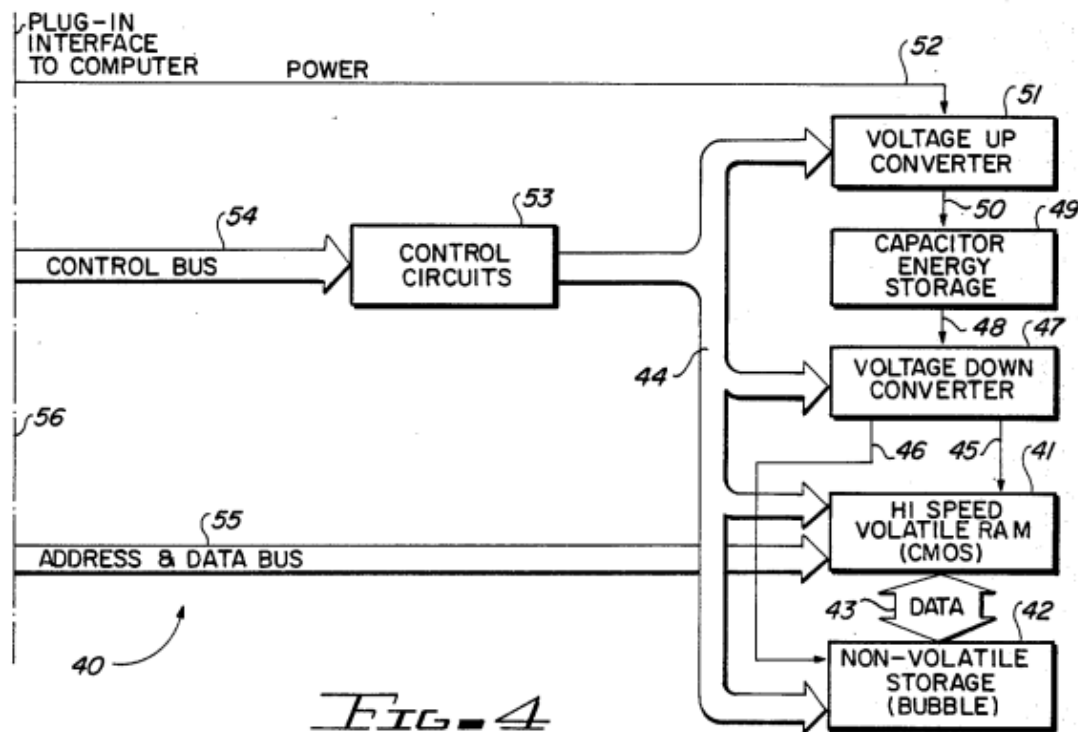
Figure 3 shows unregulated supply and emergency storage 72, which includes “capacitive storage to maintain power to critical circuits in demand register 46 for a long enough period after an apparent power outage is detected to permit transfer of billing data and programmed constants from

the volatile random access memory in processor 52 to safe storage in non-volatile memory 64.” *Id.* at 5:64–6:3.

4. *Bruder (Ex. 1005)*

Bruder is a “system for optimizing the performance of a bubble memory.” Ex. 1005, Abstract. Bruder relates “to non-volatile computer memories of the type which retain their stored data despite an interruption in power that supplies the memory.” *Id.* at 1:8–13. Bruder’s bubble memory is used as a non-volatile back-up memory for a CMOS-RAM. *Id.* at 2:32–42. A capacitor bank is charged to a high voltage during normal operation of the CMOS-RAM by a voltage booster circuit. *Id.* In the event of a power interruption, low power control circuitry actuates a voltage down converter circuit that produces a regulated output voltage to temporarily power the control circuitry while the CMOS-RAM is being transferred to the bubble memory. *Id.*

A diagram of Bruder’s system is shown in Figure 4 below.



Bruder's Figure 4, above, is a block diagram of a hybrid high speed semiconductor random access memory 40, with a non-volatile bubble memory back-up system 42 that can be utilized as a core memory replacement. Figure 4 shows bi-directional data bus 43 coupling CMOS RAM 41 to bubble memory 42. *Id.* at 7:52–54. Because CMOS 41 is volatile, whenever there is a power failure the hybrid memory 40 rapidly transfers the entire contents of CMOS 41 to non-volatile bubble memory 42. *Id.* at 7:57–60. A bank of energy storage capacitors 49 supplies enough energy to maintain the voltage supply lines of CMOS memory 41, bubble memory 42, and the other circuitry within a predetermined voltage range long enough to allow the transfer of data to be accomplished. *Id.* at 7:60–66.

5. *Weber (Ex. 1006)*

Weber, entitled "Method and Apparatus for the Protection of Write Data in a Disk Array," "relates to disk array storage devices for computer

systems and, more particularly, to a method for safeguarding disk array write operations.” Ex. 1006, code (54), 1:7–9.

Weber concerns RAID 4 and RAID 5 disk arrays, in particular, and describes that “[o]ne method for decreasing the RAID level 4 and 5 write penalty is to perform an early write operation wherein write data received from the host is written into a transfer buffer and a write complete status signal provided back to the host.” *Id.* at 2:44–47. One problem with this is that a “power failure following issuance of the write complete status signal to the host, but before completion of write operations to transfer data and parity from the transfer buffer to disk could result in the loss of data.” *Id.* at 3:5–8.

As a way to safeguard disk array write operations, Weber discloses “a low power, non-volatile storage device, such as a PCMCIA flash card device or PCMCIA disk drive, connected to transfer data with the data storage system transfer buffer; a small, temporary voltage source connected to provide power to the transfer buffer and the non-volatile storage device.” *Id.* at 3:58–4:3.

E. Obviousness Based on Bruder, Horning and Stokes

Petitioner contends that all the challenged claims, 1–3, 6, 10–12, and 15, would have been obvious over the combined teachings of Bruder, Horning and Stokes. Pet. 37–62. We begin our analysis by considering Petitioner’s rationale for combining the asserted art.

1. Rationale to Combine Bruder, Horning, and Stokes

Petitioner contends that a person of ordinary skill in the art “would have been motivated to combine Horning’s functionality for deactivating a reserve power supply to cut off power with Bruder’s data protection system

to provide optimal utilization and management of Bruder's reserve power supply." Pet. 37 (citing Ex. 1003 ¶¶ 174–180). Petitioner asserts that "Bruder and Horning are in the same field, teach analogous solutions to the same issues, and have the purpose of improving data protection and preservation systems." Pet. 37 (citing Ex. 1003 ¶¶ 175–177). "Thus," Petitioner concludes, a person of ordinary skill in the art "would have been motivated to combine these references." Pet. 37–38.

Petitioner explains that "Bruder teaches that reserve power from capacitors should only be supplied for 'long enough to allow this transfer of data [from volatile to non-volatile memory] to be accomplished.'" Pet. 38 (alteration in original) (citing Ex. 1005, 7:64–66; Ex. 1003 ¶¶ 175–177). "Likewise," Petitioner explains, "Horning teaches optimizing power utilization in a reserve power system using a circuit that '*removes power* from the primary, secondary, and tertiary power conductors . . . thereby *deactivating the entire data protection system 10*.'" Pet. 38 (citing Ex. 1008, 9:20–27, 7:23–27). "As a result," Petitioner argues, a person of ordinary skill in the art "would have been motivated to combine Bruder's data protection system with Horning's teaching of deactivating and cutting off power from a reserve power system because this would have allowed Bruder's data protection system to leverage the benefits of Horning's power optimization and utilization scheme." Pet. 38 (Ex. 1003 ¶¶ 176–177).

Petitioner also argues that a person of ordinary skill in the art "would have had an expectation of success in incorporating Horning's functionality for deactivating the reserve power supply to cut off power into Bruder's data preservation system." Pet. 38 (citing Ex. 1003 ¶ 179). Petitioner asserts that "[a]s Bruder teaches, power should only be supplied temporarily to ensure

that data is transferred to non-volatile memory, and Horning demonstrates the benefits of deactivating a capacitor to cut off power at that same level.” Pet. 38–39. “Accordingly,” Petitioner argues, a person of ordinary skill in the art “would have understood that incorporating Horning’s teaching of deactivation into Bruder’s data preservation system would have been straightforward and yielded expected results.” Pet. 39.

“Furthermore,” Petitioner argues, a person of ordinary skill in the art “would have been motivated to combine the super capacitors described by Stokes into the combination of Bruder and Horning in order to provide low cost-per-farad of capacitance with a reduced physical volume that is also quickly rechargeable.” Pet. 38 (citing Ex. 1003 ¶ 177).

Petitioner argues that “Horning and Stokes are in the same field, teach analogous solutions to the same issues, and have the same purpose of improving a backup power supply for data preservation systems.” Pet. 19 (citing Ex. 1003 ¶¶ 116–122). “Accordingly,” Petitioner concludes, a person of ordinary skill in the art “would have been motivated to incorporate Stokes’ super-capacitors, which enable additional power to be stored in a more compact form, into Horning’s reserve power supply to provide the benefit of a more compact and efficient reserve power supply.” Pet. 19–20. Petitioner argues that “[t]his motivation is plain from the references themselves,” because “Horning identifies the problems with the then-current state of battery size and rapid exhaustion, and states that the reserve power supply may comprise ‘other energy storage devices’ besides batteries.” Pet. 20 (citing Ex. 1008, 2:13–25, 11:60–64; Ex. 1003 ¶¶ 117–118).

According to Petitioner, “Horning further notes that ‘*persons having ordinary skill in the art could easily provide a suitable . . . reserve power*

supply [] with sufficient capacity to power the control subsystem [], volatile memory array [], and non-volatile memory array [], depending on the configuration of the computer system.” Pet. 20 (citing Ex. 1008, 12:1–9) (alterations in original).

“Similarly,” Petitioner argues,

Stokes not only teaches the drawbacks of batteries (similar to Horning), but also teaches the benefits of super-capacitors, noting their “significance” because they can be “packaged in one cubic inch, a two order of magnitude reduction in volume of prior technology,” and used to “sustain” operation of electronic devices and memory during power outages.

Pet. 20 (citing Ex. 1013, 3:7–15).

According to Petitioner, “[t]he benefits provided by Stokes thus directly align with Horning’s purpose.” Pet. 20. Petitioner concludes that a person of ordinary skill in the art “would have been motivated to combine these references to leverage the benefits of Stokes’ super-capacitors and avoid the drawbacks of batteries in Horning’s data protection system.” *Id.* (citing Ex. 1003 ¶ 119).

Petitioner also asserts that a person of ordinary skill in the art “would have had every expectation of success in incorporating super-capacitors into Horning’s data protection system, as Stokes demonstrates that super-capacitors were already well-known for use in reserve power systems for preserving data in volatile memory when external power is lost.” Pet. 20–21 (citing Ex. 1013, 2:57–3:61; Ex. 1003 ¶ 121). According to Petitioner, a person of ordinary skill in the art “would have understood that no significant changes would have been required to use a super-capacitor in place of another type of reserve power supply.” Pet. 21 (citing Ex. 1003 ¶ 120). “As a result,” Petitioner argues, “it would have been obvious to [a person of

ordinary skill in the art] to combine Horning with Stokes to improve the functionality of the system.” Pet. 21 (citing Ex. 1003 ¶ 118).

Petitioner’s arguments setting out a rationale to combine the teachings of Bruder, Horning, and Stokes is supported by the testimony of Dr. Baker. See Ex. 1003 ¶¶ 116–122, 174–180.

Patent Owner does not appear to offer any evidence or argument challenging Petitioner’s showing of a rationale for combining the teachings of Bruder, Horning, and Stokes.

Petitioner provides a well-reasoned showing of various rationales for combining the teachings of Bruder, Horning, and Stokes. Petitioner’s arguments are also supported by the substantial, unrebutted testimony of Dr. Baker. See Ex. 1003 ¶¶ 116–122, 174–180. In contrast, Patent Owner has not provided any argument or testimonial evidence to challenge Petitioner’s showing. See Prelim. Resp 10–20. At this stage of the proceeding, the evidence is one-sided in favor of Petitioner on the issue of rationale to combine.

Based upon the current record, we are persuaded that Petitioner has demonstrated sufficiently for purposes of institution that a person of ordinary skill in the art at the time of the invention would have had a reasoned basis for combining the teachings of Bruder, Horning, and Stokes in the manner proffered and would have had a reasonable expectation of success in that endeavor.

2. *Independent Claim 1*

Preamble - A method for controlling data in a computer system when the computer system loses power, the

*computer system comprising a computing engine,
comprising the steps of:*

Petitioner contends that “[t]o the extent the preamble is limiting, Bruder teaches this claim element.” Pet. 39. Bruder “relates to computer memories, and more particularly to non-volatile computer memories of the type which retain their stored data despite an interruption in power that supplies the memory.” Ex. 1005, 1:8–11. Petitioner asserts that “Bruder discloses a computing engine that comprises both volatile memory (e.g., CMOS RAM) and non-volatile memory (e.g., bubble memory).” Pet. 39 (citing Ex. 1005, Abstract, 2:32–42, 7:52–60, Fig. 4). Petitioner also asserts that Bruder “teaches control circuits, which control ‘data transfer between CMOS Ram 41 and bubble memory 42 during a power interruption.’” Pet. 39 (citing Ex. 1005, 8:37–5). According to Petitioner, “Bruder’s ‘control circuits’ comprise a ‘processor or similar structure for directing the transfer and storage of data in memory’ under the Petitioners’ proposed construction of computing engine.” Pet. 39–40 (citing Ex. 1003 ¶ 182).

Petitioner asserts that Bruder’s control circuits, volatile memory, and nonvolatile memory, “comprise the claimed ‘computing engine,’” and are illustrated in Bruder’s Figure 4, shown below annotated by Petitioner. *See* Pet. 40 (citing Ex. 1003 ¶ 183).



Bruder explains that Figure 4 “is a block diagram of a hybrid high speed semiconductor random access memory, with a non-volatile bubble memory back-up system that can be utilized as a core memory replacement.” Ex. 1005, 3:3–7. As annotated by Petitioner, Bruder’s Figure 4 shows control circuits 53 highlighted in blue, hi speed volatile RAM (CMOS) 41 highlighted in purple, and non-volatile storage 42 (bubble) highlighted in green. Petitioner’s arguments are supported by the testimony of Dr. Baker. See Ex. 1003 ¶¶ 182–184.

Patent Owner does not specifically contest Petitioner’s evidence and arguments with respect to the preamble. *See* Prelim. Resp. 10–20.

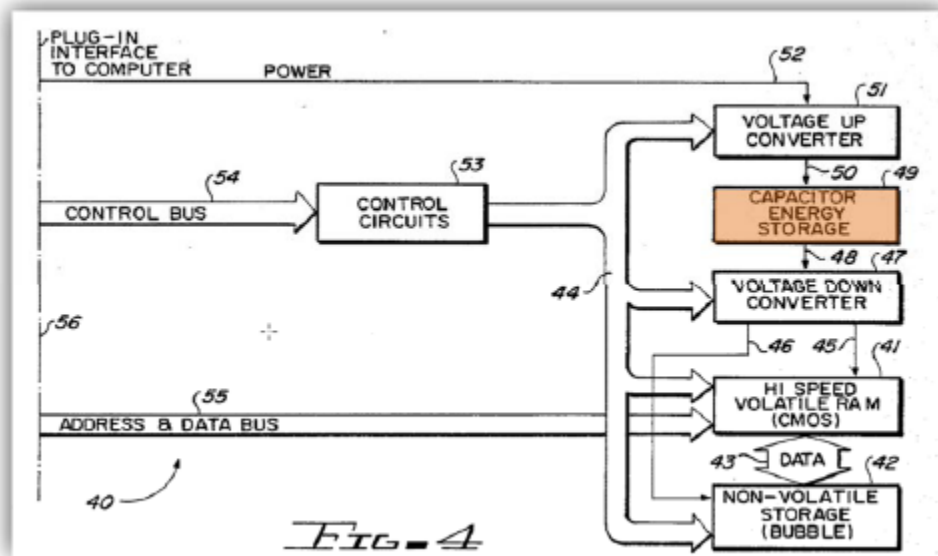
On this preliminary record, we determine that Petitioner has shown sufficiently for purposes of institution that Bruder's description of the operation of control circuits 53 that control data transfer between hi-speed volatile CMOS RAM 41 and non-volatile bubble memory storage 42 during a power interruption, meets the recited language "*method for controlling*

data in a computer system when the computer system loses power, the computer system comprising a computing engine” of the preamble.

a) [1a] activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;

Petitioner contends that “Bruder renders this claim element obvious in view of Stokes.” Pet. 40. According to Petitioner, “Bruder discloses a capacitor bank (i.e., a ‘plurality of capacitors’) that stores and ‘supplies enough energy to maintain the voltage supply lines’ to the memory and other circuitry when external power is interrupted.” *Id.* at 40–41 (citing Ex. 1005, 7:60–66, Abstract, 2:35–38, 8:2–7, Fig. 4; Ex. 1003 ¶ 185). Petitioner asserts that “Bruder also teaches activating the capacitors when external power is removed from the computer system.” Pet. 41. Petitioner notes that “Bruder states that, when external power to the computing system is interrupted, ‘low power control circuitry actuates a voltage down converter circuit that produces a regulated output voltage’ from the capacitor bank ‘to temporarily power the control circuitry.’” *Id.* (citing Ex. 1005, Abstract, 8:2–10, 2:35–38; Ex. 1003 ¶ 186).

Bruder’s capacitor bank is illustrated in Bruder’s Figure 4, shown below, annotated by Petitioner. *See* Pet. 41 (citing Ex. 1003 ¶ 187).



Bruder's Figure 4, shown above, annotated by Petitioner, shows capacitor energy storage 49 highlighted in orange.

Petitioner concedes that “Bruder does not refer to [its] capacitors as ‘super capacitors.’” Pet. 41. Petitioner points out, however, that

[t]he '939 patent does not define what a super-capacitor [is], nor does it differentiate a super-capacitor from a “capacitor.” Instead, the specification, simply states that “with the advent of low cost super-capacitors available in values of over 10 Farads, large amounts of energy can be affordably stored in a very small space.”

Pet. 33 n.7 (citing Ex. 1001, 3:7–10).

According to Petitioner, the “use of super-capacitors in Bruder's invention would have been obvious in view of Stokes.” Pet. 41–42 (citing Ex. 1003 ¶ 188). Petitioner argues that “super-capacitors would have been well-known to a POSITA at the time that [the] '939 patent was filed, and were also known to provide more capacitance in a smaller form factor.” Pet. 42 (citing *id.* at Pet. § IX.E.; Ex. 1003 ¶¶ 114–115, 188).

“Moreover,” Petitioner argues, a person of ordinary skill in the art “would have known that supercapacitors could be used [in] electronic systems and circuits.” Pet. 42. According to Petitioner,

using a “supercapacitor” in place of a “capacitor” would have been obvious to a POSITA based on the advantages taught by Stokes and also given Bruder’s disclosure that the capacitors need to have sufficient capacity to power the computing engine, and ensure the complete transfer of data to non-volatile memory, in the event of power loss.

Id. (citing Pet. § IX.E. (discussing characteristics of super capacitors); Ex. 1003 ¶¶ 114–115, 188).

Petitioner’s arguments are supported by the testimony of Dr. Baker. *See* Ex. 1003 ¶¶ 185–189.

Patent Owner does not specifically contest Petitioner’s evidence and arguments with respect to the preamble. *See* Prelim. Resp. 10–20.

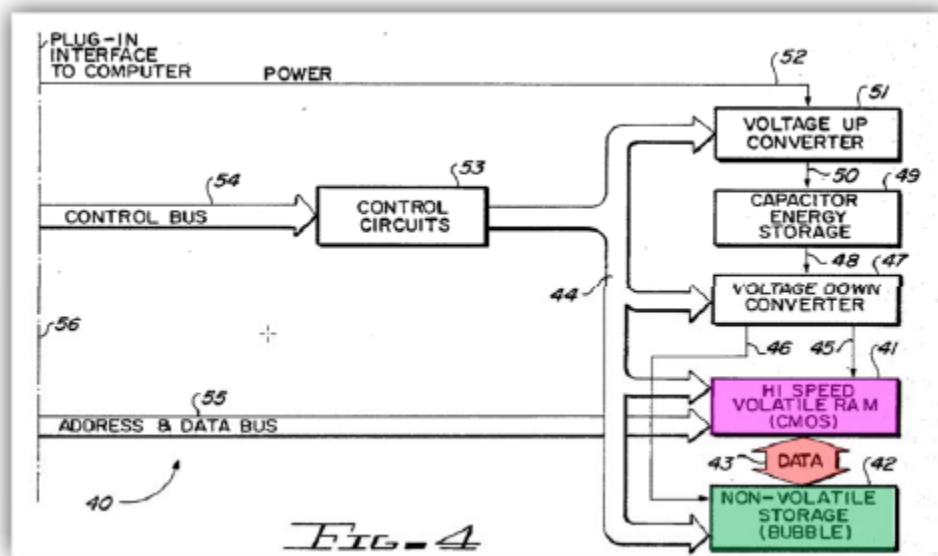
On this preliminary record, we determine that Petitioner has shown sufficiently for purposes of institution that Bruder’s description of control circuitry 53 generating the necessary signals to effectuate proper operation of voltage down converter 47 to achieve the desired data transfer between CMOS RAM 41 and bubble memory 42 during a power interruption in combination with Stokes description of super-capacitors to provide power and sustain operations during outages, meets the recited limitation “*activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system*” of claim 1.

b) [1b] *reconfiguring the data in the computing engine;*

Petitioner contends “Bruder discloses that, in the event of a power interruption, data is reconfigured in the computing engine by ‘transfer[ring]

the entire contents' of volatile CMOS RAM to non-volatile bubble memory.” Pet. 42 (citing Ex. 1005, 7:57–60, 8:2–10, 10:58–64; Ex. 1003 ¶ 194).

According to Petitioner, Bruder’s Figure 4, shown below annotated by Petitioner, “depicts the transfer—or reconfiguration—of data from volatile memory to non-volatile memory.” Pet. 42–43 (citing Ex. 1003 ¶ 191).



Bruder’s Figure 4, annotated by Petitioner, shows hi-speed volatile RAM (CMOS) 41 highlighted in purple, data bus 43 highlighted in red, and non-volatile storage (bubble) 42 highlighted in green.

Petitioner’s arguments are supported by the testimony of Dr. Baker. See Ex. 1003 ¶¶ 190–192.

Patent Owner does not specifically contest Petitioner’s evidence and arguments with respect to the preamble. See Prelim. Resp. 10–20.

On this preliminary record, we determine that Petitioner has shown sufficiently for purposes of institution that Bruder’s description of control

circuitry 53 generating the necessary signals to achieve the desired data transfer between CMOS RAM 41 and bubble memory 42 during a power interruption, meets the recited limitation “*reconfiguring the data in the computing engine*” of claim 1.

c) [1c] *deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.*

Petitioner contends that “Bruder renders this claim element obvious in view of Horning further in view of Stokes.” Pet. 43. According to Petitioner, “Bruder teaches that the capacitor bank supplies power to the down converter to ‘temporarily power the control circuitry’ while data is being transferred from volatile to non-volatile memory.” Pet. 43 (citing Ex. 1005, Abstract, 2:35–42, 7:64–66). Petitioner argues that “[b]y teaching that the capacitor bank is only activated ‘temporarily’—and only for ‘long enough’ to affect a complete data transfer from volatile to non-volatile memory—Bruder indicates that the capacitor bank is deactivated.” Pet. 43. Petitioner indicates that “Bruder also teaches the importance of regulating the power output from the reserve power supply, noting that the capacitors maintain voltage ‘long enough to allow this transfer of data [from volatile to non-volatile memory] to be accomplished.’” Pet. 43–44 (alterations in original) (citing Ex. 1005, 7:64–66, 3:40–44, 8:7–10, 10:58–64; Ex. 1003 ¶ 194).

Petitioner explains that “Horning discloses a system and method of data protection that includes discharging a reserve power supply to a predetermined level at which it can supply enough power to the computing engine so that it can transfer all the data from the volatile memory array to the non-volatile memory array.” Pet. 44 (citing *id.* at Pet. § IX.D; Ex. 1008,

8:13–17). Petitioner also explains that “Horning teaches that cutting off power from the reserve power supply at that level allows the user to obtain ‘optimum utilization of the reserve power supply regardless of the capacity of the reserve power supply.’” Pet. 44 (citing Ex. 1008, 8:6–8, 8:19–24).

According to Petitioner, “Horning also discloses that, after all data has been transferred from volatile to nonvolatile memory, power is cut off to the computing engine by a circuit that ‘removes power from the primary, secondary, and tertiary power conductors . . . thereby deactivating the entire data protection system 10.’” Pet. 44 (citing Ex. 1008, 9:20–27; Ex. 1003 ¶ 195).

Petitioner argues that “it would have been obvious to a POSITA to include the teachings of Horning, including Horning’s functionality for deactivating the reserve power system, in Bruder’s data protection system in order to achieve the stated optimum utilization of the reserve power capacitor.” Pet. 44–45 (citing *id.* at Pet. § X.C.1.b; Ex. 1003 ¶¶ 185–189). Petitioner also argues that “it would have been obvious to a POSITA to replace Bruder’s capacitors with a plurality of Stokes’ super capacitors in order to supply sufficient reserve power from a reduced physical volume.” Pet. 45 (citing *id.* at Pet. § X.C.1.b; Ex. 1003 ¶¶ 185–189).

Patent Owner contends that Horning fails to disclose the recited “predetermined level,” relying upon its arguments addressing this issue for claim 1, Ground 1. *See* Prelim. Resp. 18–19. There, Patent Owner argues that “Horning does not disclose any deactivation or disconnection upon the reserve power supply 34 reaching a predetermined level.” *Id.* at 13–14. “Instead,” Patent Owner argues, “Horning discloses ‘transferring data from the volatile memory 15 to the non-volatile memory array 18 while there is

still enough power in the reserve power supply 34 to accomplish this data transfer.” *Id.* (citing 1008, 7:10–23). Patent Owner argues that “Horning does not, however, disclose a power level of the reserve power supply when any deactivation or disconnection of the reserve power supply occurs.”

Prelim. Resp. 14.

Rather, Patent Owner argues,

Horning only discloses a disconnection after the data transfer process is complete, and without disclosing a power level corresponding to the disconnection: “After all the data have been transferred, the reserve power supply 34 is disconnected from all the power conductors and the system 10 will remain in this power off state until power is restored to the system.”

Id. (citing Ex. 1008, 7:23–27; *see also id.* at 9:23–27, 11:14–17). Patent Owner argues that according to Horning, “the level of the reserve power supply 34 can initiate the data transfer task, but *not* a deactivation of the reserve power supply 34.” Prelim. Resp. 14 (citing Ex. 1008, 8:13–19).

Patent Owner asserts that “Petitioners characterize Horning’s ‘level where there is only enough energy left for the data transfer’ as the claimed ‘predetermined level,’” but according to Patent Owner, “[t]his is wrong,” because “there is no deactivation occurring in Horning at this level or even based on this level.” Prelim. Resp. 15. Rather, Patent Owner argues, “[t]his level in Horning marks the level when the reserve power supply is used to begin the data transfer task.” *Id.* According to Patent Owner, “[u]pon Horning’s reserve power system discharging to a low level, Horning begins a data transfer process, [but] it does not deactivate the reserve power supply or cut off power to the computing engine.” *Id.* at 16.

“Simply put,” Patent Owner argues, “Horning’s reserve power level cited to and relied upon by Petitioners does not correspond to the

deactivation of Horning's reserve power supply 34.” *Id.* “Indeed,” Patent Owner argues, “Horning discloses nothing about the level of the reserve power supply 34 when any disconnection occurs.” *Id.*

Patent Owner further argues that “Petitioners also fail to address the requirement that the claimed ‘level’ at issue be ‘predetermined.’” *Id.* (citing Pet. 24–26). “Specifically,” Patent Owner argues, “Petitioners fail to point to any disclosure in Horning that would justify interpreting the level at which Horning begins the data transfer process as ‘predetermined.’” Prelim. Resp. 16. According to Patent Owner, “Horning discloses the level to begin the data transfer process as corresponding to a ‘low voltage condition’ where the ‘storage batteries in the reserve power supply 34 are almost exhausted,’” but “Petitioners provide no basis to conclude that such low voltage condition is ‘predetermined.’” *Id.* (citing Ex. 1008, 13:16–20).

Patent Owner argues that “Horning does not disclose any deactivation or disconnection upon the reserve power supply 34 reaching a predetermined level.” Prelim. Resp. 13–14. We disagree with Patent Owner.

Horning explains that in the event of a power disruption

data from volatile memory array 16 will be transferred into the non-volatile memory array 18 *while there is still enough power remaining in the reserve power supply 34 to accomplish the data transfer process* [T]he control subsystem 14 will now immediately begin transferring data from the volatile memory array 16 to the non-volatile memory array 18. *Then, after all the data have been transferred, the supervisor circuit 38 removes power from the primary, secondary, and tertiary power conductors 22, 24, and 26, respectively, thereby deactivating the entire data protection system 10.*

Ex. 1008, 9:8–27 (emphases added).

Patent Owner’s argument appears to assume that the recited claim language “*based upon*” somehow precludes any other steps between “*discharging to a predetermined level*” and “*deactivating the . . . capacitors to cut off power.*”

However, use of the transition word “comprising” in a method claim like this indicates that the claim is open-ended and allows for additional steps. *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 811 (Fed. Cir. 1999); *Moleculon Research Corp. v. CBS, Inc.*, 793 F.2d 1261, 1271 (Fed. Cir. 1986) (“comprising” opens a method claim to the inclusion of steps in addition to those stated in the claim). “In the patent claim context the term ‘comprising’ is well understood to mean ‘including but not limited to.’” *CIAS, Inc. v. Alliance Gaming Corp.*, 504 F.3d 1356, 1360 (Fed. Cir. 2007) (quoting *Vivid Techs., Inc.*, 200 F.3d at 811).

We agree with Petitioner, therefore, that Horning’s teaching of transferring volatile memory array 16 into non-volatile memory array 18 upon a power disruption while there is still enough power remaining in the reserve power supply to accomplish the data transfer process and then, after all the data have been transferred, supervisor circuit 38 removes power thereby deactivating the entire data protection system 10 meets the claim limitation for purposes of institution. Pet. 43–44; *see also* Ex. 1008, 9:5–27.

Patent Owner also appears to assume that the recited “*predetermined level*” must be somehow be quantitative rather than qualitative. *See, e.g.*, Prelim. Resp. 14 (“Horning does not, however, disclose *a power level* of the reserve power supply when any deactivation or disconnection of the reserve power supply occurs.” (emphasis added)). If that is the case, we disagree with Patent Owner. Patent Owner has not pointed us to any persuasive

evidence that would require such a construction. Indeed, Patent Owner takes the position that “the Board need not engage in any pre-institution claim construction.” Prelim. Resp. 9.

Here, Petitioner points to Horning’s teaching of a *qualitative predetermined level* of Horning’s reserve power supply sufficient to meet the recited limitation, e.g.,

[i]f, at any time during these power load sequences 74 and 76, *the reserve power supply 34 is discharged to the point where there is only enough energy to accomplish the data transfer task*, the data protection system 10 will automatically initiate the data transfer process to ensure complete data integrity even if the user mistakenly programmed too long a time period for power load sequences 74 and 76.

Ex. 1008, 8:12–19.³

On this preliminary record, we find that Petitioner has shown sufficiently for purposes of institution that the combined teachings of Bruder, Horning, and Stokes meet the recited limitation “*deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level*” of claim 1.

d) Conclusion as to Claim 1

We have considered Petitioner’s evidence and arguments that the limitations of claim 1 are met by the combined teachings of Bruder, Horning, and Stokes, as well as Patent Owner’s evidence and arguments to

³ We also note that Horning discusses a predetermined safe minimum voltage of the reserve power supply, albeit in the context of a battery in the reserve power supply. *See* Ex. 1008, 43–68.

the contrary. Based on the current record, and for the reasons given by Petitioner, and those summarized above, we are persuaded that Petitioner has demonstrated sufficiently for purposes of institution that the combined teachings of the asserted art meet the limitations of independent claim 1 and that a person of ordinary skill in the art would have had sufficient reason to combine the art in the manner proffered by Petitioner.

3. *Independent Claim 10*

Independent claim 10 is a system claim that is substantially similar to independent claim 1, except that claim 10 uses functional “means for” language to recite the activating [1a], reconfiguring [1b], and deactivating [1c] steps of claim 1. *See* Ex. 1001, 7:65–8:9. Petitioner has proposed constructions for these limitations that we have adopted for purposes of this Decision (*see supra* Section III.C.3–5). Patent Owner takes the position that “the Board need not engage in any pre-institution claim construction.”

Prelim. Resp. 9.

For the reasons explained above with respect to independent claim 1, we are persuaded that Petitioner has demonstrated sufficiently for purposes of institution that the combined teachings of the asserted art also meet the limitations of independent claim 10 and that a person of ordinary skill in the art would have had sufficient reason to combine the art in the manner proffered by Petitioner.

4. *Dependent Claims 2, 3, 6, 11, 12, 15*

Petitioner contends that dependent claims 2, 3, 6, 11, 12, and 15 are unpatentable under 35 U.S.C. § 103 as obvious over the combined teachings of Bruder, Horning, and Stokes. Pet. 45–48, 58–62. Petitioner provides a

claim-by-claim analysis that is supported by the testimony of Dr. Baker. *See* Ex. 1003 ¶¶ 197–209, 230–246.

Patent Owner does not respond specifically to Petitioner’s evidence and arguments with respect to dependent claims 2, 3, 6, 11, 12, and 15. *See* Prelim. Resp. 10–20.

We have considered the evidence and arguments with respect to dependent claims 2, 3, 6, 11, 12, and 15. Based upon the current record, we are persuaded that Petitioner has shown sufficiently for purposes of institution that the combined teachings of the cited art meet the recited limitations of these claims, and that a person of ordinary skill in the art at the time of the invention would have combined the references in the manner proffered and would have had a reasonable expectation of success in that endeavor.

F. Other Grounds

Petitioner also contends that claims 1–3 are unpatentable under 35 U.S.C. § 103 as obvious over the combined teachings of Horning and Stokes (Ground 1, Pet. 19–27); claims 1–3 over Horning, Stokes, and Germer (Ground 2, Pet. 27–37); and claims 1–3, and 6 over Horning, Stokes, and Weber (Ground 4, Pet. 62–73). Petitioner provides evidence and arguments as to how the art teaches or suggests each claim limitation. Dr. Baker provides supporting testimony for Petitioner’s contentions. *See* Ex. 1003, 55–83, 122–143.

Patent Owner disputes some of Petitioner’s contentions and provides evidence and arguments as to how Petitioner has failed to demonstrate that the challenged claims are obvious over the asserted art, principally for failing to establish that the asserted prior art teaches or suggests the recited

limitation “*deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level*” in claim 1 and similarly in claim 10. See Prelim. Resp. 10–19 .

We have considered the parties evidence and arguments with respect to these claims. However, because we determine that Petitioner demonstrates a reasonable likelihood of prevailing in its challenge to independent claims 1 and 10 under 35 U.S.C. § 103(a) as obvious over the combined teachings of Bruder, Horning, and Stokes, we must institute *inter partes* review as to all challenges in the Petition, including Petitioner’s challenges with respect to these grounds and claims. See *PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018).

IV. CONCLUSION

For the foregoing reasons, we have determined that there is a reasonable likelihood that Petitioner would prevail with respect to at least one of the claims challenged in the Petition. We therefore institute trial as to all challenged claims on all grounds stated in the Petition.

V. ORDER

Upon consideration of the record before us, it is

ORDERED that *inter partes* review of claims 1–3, 6, 10–12, and 15 of the ’939 patent is instituted on all grounds in the Petition;

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this decision.

IPR2023-00743
Patent 6,496,939 B2

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