

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. AND
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioners

v.

DAEDALUS PRIME LLC
Patent Owner.

Case No. IPR2023-00753
U.S. Patent No. 10,372,197

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 10,372,197**

I.	INTRODUCTION	1
II.	MANDATORY NOTICES, STANDING, AND FEES.....	1
A.	Mandatory Notices Under 37 C.F.R. §42.8	1
B.	Grounds for Standing	3
C.	Fee Authorization	3
III.	RELIEF REQUESTED	3
IV.	THE CHALLENGED PATENT	4
A.	The '197 Patent	4
B.	Level of Ordinary Skill in the Art	6
V.	BRIEF DESCRIPTION OF THE APPLIED PRIOR ART REFERENCES	6
A.	Naveh (Ex-1005)	6
B.	Saeed (Ex-1006)	7
C.	Titiano (Ex-1007)	8
D.	Hansquine (Ex-1008)	9
VI.	CLAIM CONSTRUCTION	10
VII.	DETAILED EXPLANATION OF THE UNPATENTABILITY GROUNDS	11
A.	Grounds 1 and 2: Claims 1–3 and 19–20 Are Obvious Over Naveh and Obvious Over Naveh in view of Saeed.....	11
1.	A POSITA would have been motivated to combine Naveh with Saeed.....	11
2.	Independent Claim 1	13
a.	Element 1[preamble]: A processor comprising:.....	13
b.	Element 1[a]: a plurality of cores;	13
c.	Element 1[b]: a cache memory;.....	14
d.	Element 1[c]: an interconnect to couple the plurality of cores to the cache memory;	15

TABLE OF CONTENTS

(continued)

	Page
e. Element 1[d]: a power controller to control a plurality of power management features of the processor;	16
f. Element 1[e]: wherein the power controller includes a tuning circuit to receive a workload configuration input regarding a workload, receive a plurality of energy performance bias (EPB) values and determine a global EPB value based thereon, and update at least one setting of at least one of the plurality of power management features based on the workload configuration input and the global EPB value	17
i. Element 1[e1]: a tuning circuit to receive a workload configuration input regarding a workload;	18
ii. Element 1[e2]: a tuning circuit to ... receive a plurality of energy performance bias (EPB) values and determine a global EPB value based thereon;	23
iii. Element 1[e3]: a tuning circuit to ... update at least one setting of at least one of the plurality of power management features based on the workload configuration input and the global EPB value.	28
3. Dependent Claims 2–3, 19–20	30
a. Claim 2: The processor of claim 1, wherein the power controller is to access a power-performance tuning table based on the workload configuration input and the global EPB value, and use information from the power-performance tuning table to update the at least one setting.	30

TABLE OF CONTENTS

(continued)

	Page
b. Claim 3: The processor of claim 2, wherein the tuning circuit is to update the at least one setting of the at least one power management feature responsive to the global EPB value.....	34
c. Claim 19: The processor of claim 1, wherein the power controller is to enable a first power management feature based on the updated at least one setting.....	34
d. Claim 20: The processor of claim 1, wherein the power controller is to send an update message to a destination agent of the processor to cause the destination agent to control a first power management feature based on the updated at least one setting.....	35
B. Ground 3: Claims 1–6, 11, 13, and 19–20 Are Obvious Over Titiano.....	37
1. Independent Claim 1	37
a. Element 1[preamble]: A processor comprising:.....	37
b. Element 1[a]: a plurality of cores;	38
c. Element 1[b]: a cache memory;.....	41
d. Element 1[c]: an interconnect to couple the plurality of cores and the cache memory;.....	42
e. Element 1[d]: a power controller to control a plurality of power management features of the processor;	43

TABLE OF CONTENTS

(continued)

Page

f.	Element 1[e]: wherein the power controller includes a tuning circuit to receive a workload configuration input regarding a workload, receive a plurality of energy performance bias (EPB) values and determine a global EPB value based thereon, and update at least one setting of at least one of the plurality of power management features based on the workload configuration input and the global EPB value.	46
i.	Element 1[e1]: a tuning circuit to receive a workload configuration input regarding a workload;.....	47
ii.	Element 1[e2]: a tuning circuit to ... receive a plurality of energy performance bias (EPB) values and determine a global EPB value based thereon;	53
iii.	Element 1[e3]: a tuning circuit to ... update at least one setting of at least one of the plurality of power management features based on the workload configuration input and the global EPB value.	62
2.	Dependent Claims 2–6 and 19–20	69
a.	Claim 2: The processor of claim 1, wherein the power controller is to access a power-performance tuning table based on the workload configuration input and the global EPB value, and use information from the power-performance tuning table to update the at least one setting.	69
b.	Claim 3: The processor of claim 2, wherein the tuning circuit is to update the at least one setting of the at least one power management feature responsive to the global EPB value.	72

TABLE OF CONTENTS

(continued)

	Page
c. Claim 4: The processor of claim 3, wherein the tuning circuit includes a sampler to receive the plurality of EPB values from at least some of the plurality of cores and a combiner to generate the global EPB value from the EPB value from the plurality of cores.....	72
d. Claim 5: The processor of claim 4, wherein the sampler is to receive the EPB value from a plurality of threads to execute on the at least some of the plurality of cores.....	73
e. Claim 6: The processor of claim 4, wherein the power controller is to generate a bin value from the global EPB value and to access the power-performance tuning table using the bin value.....	74
f. Claim 19: The processor of claim 1, wherein the power controller is to enable a first power management feature based on the updated at least one setting.....	75
g. Claim 20: The processor of claim 1, wherein the power controller is to send an update message to a destination agent of the processor to cause the destination agent to control a first power management feature based on the updated at least one setting.....	75
3. Independent Claim 11	79
a. Element 11[pre]: A non-transitory machine-readable medium having stored thereon instructions, which if performed by a machine cause the machine to perform a method comprising:	79

TABLE OF CONTENTS

(continued)

	Page
b. Element 11[a]: receiving an energy performance bias (EPB) value in a tuning circuit of a power control logic of a processor from a plurality of threads executing on the processor and determining a global EPB value based at least in part on the EPB value received from the plurality of threads, the EPB value to indicate a preference of a user for a tradeoff between power optimization and performance optimization;..... c. Elements 11[b]: accessing a table based on the global EPB value; and Element 11[c]: updating at least one setting of a power management feature controlled by the power control logic based on information obtained from the table. 4. Dependent Claim 13: The non-transitory machine-readable medium of claim 11, wherein the method further comprises providing an interface to enable a user, an operating system or a baseboard management controller to set the EPB value, and controlling a plurality of power management features via input of the EPB value. C. Ground 4: Claims 2, and 15–18 Are Obvious Over Titiano in View of Hansquine..... 1. A POSITA would have been motivated to combine Titiano and Hansquine 2. Dependent Claim 2..... 3. Independent Claim 15 a. Element 15[a]: a multicore processor including a plurality of cores, at least one cache memory and a memory controller;	79 80 81 82 82 83 85 85

TABLE OF CONTENTS

(continued)

Page

b.	Element 15[b]: wherein the tuning circuit is to access an entry of a tuning table based at least in part on the EPB value and a workload configuration value and update a setting for a power management feature responsive to a value stored in a field of the entry;.....	86
c.	Element 15[c]: wherein the workload configuration value is to indicate a predominant workload type to be executed on the system, the tuning table including a first set of entries associated with a first workload type and a second set of entries associated with a second workload type;	86
d.	Element 15[d]: a system memory coupled to the multicore processor via a memory interconnect.....	87
4.	Dependent Claim 16: The system of claim 15, wherein the tuning circuit is to update at least one setting of a first power management feature controlled by a power control logic of the multicore processor, the at least one setting obtained from a field of an entry of the tuning table associated with a bin in which the EPB value is included.....	88
5.	Dependent Claim 17: The system of claim 16, wherein multicore processor comprises the tuning circuit.	89
6.	Dependent Claim 18: The system of claim 15, wherein the multicore processor comprises a power control logic, the power control logic comprising the tuning circuit, wherein the tuning circuit is to generate a bin value from the EPB value and access the tuning table using the bin value.	89
VIII.	THE BOARD SHOULD NOT USE ITS DISCRETION TO DENY INSTITUTION UNDER <i>FINTIV</i>	90
IX.	CONCLUSION.....	94

LIST OF EXHIBITS¹

Ex-1001	U.S. Patent No. 10,372,197 (“the ’197 Patent”)
Ex-1002	Declaration of Dr. Stephen W. Melvin
Ex-1003	Curriculum Vitae of Dr. Stephen W. Melvin
Ex-1004	Prosecution History of U.S. Patent No. 10,372,197 (App. No. 15/367,330)
Ex-1005	U.S. Patent Application Publication No. 2006/0026447 (“Naveh”)
Ex-1006	U.S. Patent No. 6,711,447 (“Saeed”)
Ex-1007	U.S. Patent Application Publication No. 2008/0162770 (“Titiano”)
Ex-1008	U.S. Patent Application Publication No. 2011/0004774 (“Hansquine”)
Ex-1009	Bruce Jacob et al., <i>Memory Systems, Cache, DRAM, Disk</i> (2008) (“Jacob”)
Ex-1010	Ahmed Amine Jerraya and Wayne Wolf, <i>Multiprocessor Systems-on-Chips</i> (2005) (“Jerraya”)
Ex-1011	Brinkley Sprunt, <i>The Basics Of Performance-monitoring Hardware; Pentium 4 Performance-Monitoring Features</i> (2002) (“Sprunt”)
Ex-1012	Dmitrijs Zaparanuks et al., <i>Accuracy of Performance Counter Measurements</i> (2009) (“Zaparanuks”)
Ex-1013	Paul West, <i>Core Monitors: Monitoring Performance In Multicore Processors</i> (2008) (“West”)
Ex-1014	K. Sreejith, <i>Workload Based Lookup Table for Minimal Power Operation Under Supply and Body Bias Control</i> (2009) (“Sreejith”)

¹ Four-digit pin citations that begin with 0 are the page stamps added by Samsung in the bottom right corner of the exhibits. All other pin citations are to original page, column, paragraph, or line numbers.

Ex-1015	<i>Enhanced Intel® SpeedStep® Technology for the Intel® Pentium® M Processor</i> (2004) (“Intel SpeedStep”)
Ex-1016	INTENTIONALLY LEFT BLANK
Ex-1017	U.S. District Courts – Combined Civil and Criminal Federal Court Management Statistics (June 30, 2022), available at: https://www.uscourts.gov/statistics-reports/federal-court-management-statistics-june-2022
Ex-1018	INTENTIONALLY LEFT BLANK
Ex-1019	INTENTIONALLY LEFT BLANK

I. INTRODUCTION

Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively, “Petitioner”) request *inter partes* review (“IPR”) of Claims 1–6, 11, 13, and 15–20 of U.S. Patent No. 10,372,197 (“the ’197 Patent”) (Ex-1001), currently assigned to Daedalus Prime LLC (“PO”).

II. MANDATORY NOTICES, STANDING, AND FEES

A. Mandatory Notices Under 37 C.F.R. §42.8

Real Parties-in-Interest: Petitioner identifies the following real parties-in-interest: Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., Samsung Austin Semiconductor, LLC, and ARM Ltd.

Related Matters: PO has asserted the ’197 Patent against Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., and Samsung Austin Semiconductor, LLC in *Daedalus Prime LLC v. Samsung Elecs. Co., Ltd.*, No. 2:22-cv-00354 (E.D. Tex. Sept. 12, 2022).

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B. Grounds for Standing

Petitioner certifies that the '197 Patent is available for review, and Petitioner is not barred or estopped from requesting review.

C. Fee Authorization

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-0639.

III. RELIEF REQUESTED

For purposes of this proceeding only, Petitioner assumes, without conceding, that the '197 Patent is entitled to its earliest alleged priority date, December 15, 2011, and thus applies pre-AIA 35 U.S.C. § 102.

Petitioner requests cancellation of Claims 1–6, 11, 13, and 15–20 as unpatentable. This Petition presents new arguments based on prior art that was not before the PTO during prosecution. Petitioner presents the following grounds, supported by a declaration from Dr. Steve Melvin. Ex-1002 ¶¶25, 65–211.

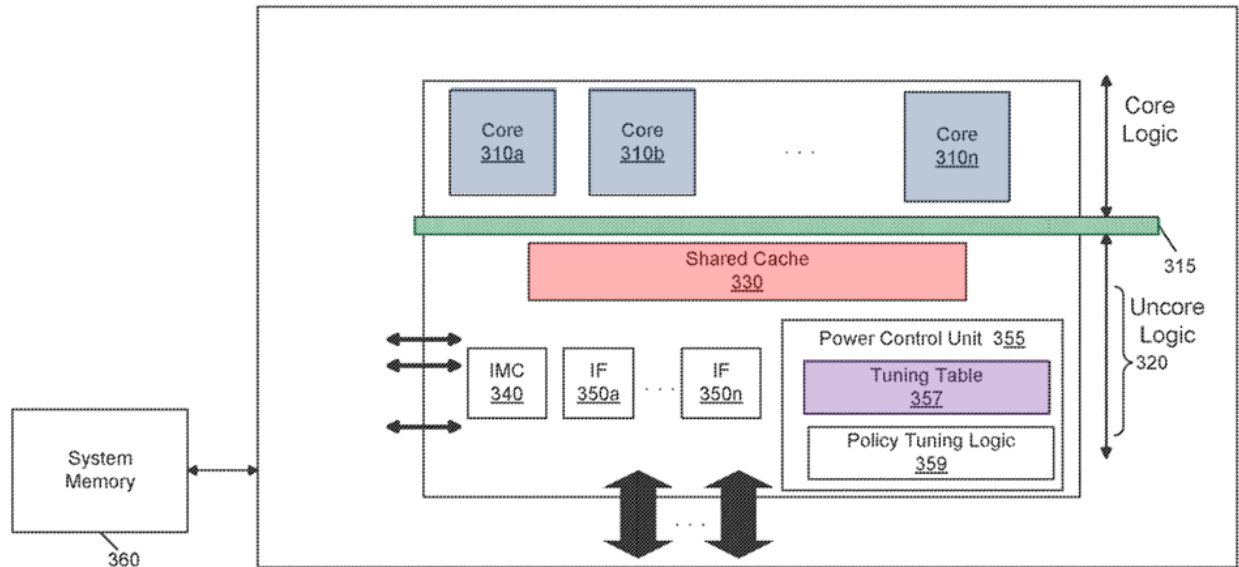
Ground	Summary
1	Claims 1–3 and 19–20 are obvious over Naveh (Ex-1005).
2	Claims 1–2 are obvious over Naveh in view of Saeed (Ex-1006).
3	Claims 1–6, 11, 13, and 19–20 are obvious over Titiano (Ex-1007).
4	Claims 2 and 15–18 are obvious over Titiano in view of Hansquine (Ex-1008).

IV. THE CHALLENGED PATENT

A. The '197 Patent

The alleged invention of the '197 Patent relates to power management. The claims recite a processor 300; a plurality of cores 310; a cache memory 330; and an interconnect 315 to couple the plurality of cores and the cache memory, as shown in annotated Figure 4. Ex-1001, 8:66–9:10. The '197 Patent does not suggest that this arrangement of components is inventive.

300



The '197 Patent purports to describe an allegedly inventive tuning circuit for controlling power management features. Specifically, processor 300 may include a tuning circuit to (1) receive a workload configuration input and a plurality of energy performance bias (EPB) values, (2) determine a global EPB value based on the plurality of EPB values, and (3) update a setting of a power management feature based on the workload configuration input and the global EPB value. *Id.*, 11:49–62. The system may also include a power-performance tuning table used to update the setting. *Id.*, 5:33–7:31.

B. Level of Ordinary Skill in the Art

A person of ordinary skill in the art at the relevant time (“POSITA”) would have had a bachelor’s degree in electrical engineering, computer engineering, or a related field, and three years of experience in the research, design, or development of processor systems, or the equivalent, with additional education substituting for experience and vice versa. *Id.* ¶35.

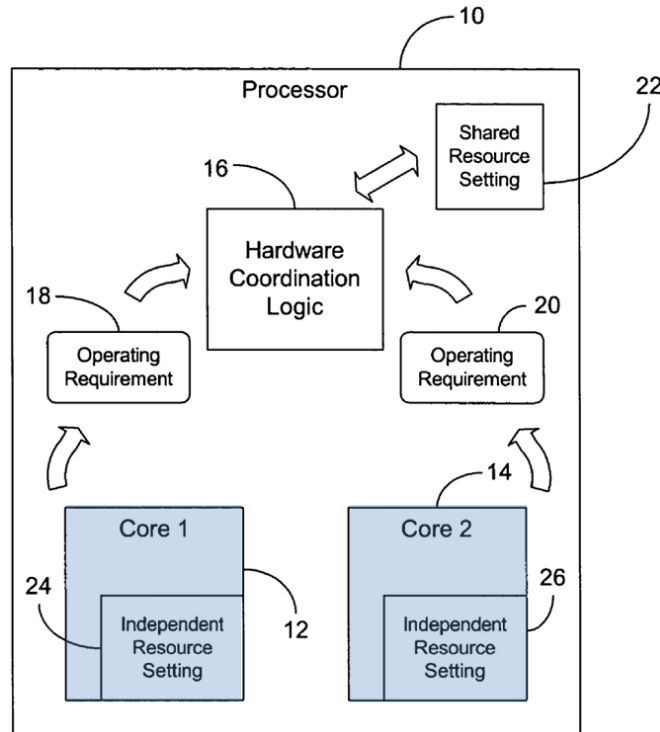
V. BRIEF DESCRIPTION OF THE APPLIED PRIOR ART REFERENCES

This Petition presents four references, none of which were of record during prosecution of the ’197 Patent. Ex-1004.

A. Naveh (Ex-1005)

Naveh was filed July 27, 2004, and published February 2, 2006. Ex-1005, cover. Naveh qualifies as prior art under at least pre-AIA 35 U.S.C. § 102(a), (b), and (e).

As shown in Figure 1, processor 10 include two cores 12, 14 and hardware coordination logic 16. Ex-1005 ¶17. Cores 12, 14 share a clock frequency and a power supply voltage represented by shared resource setting 22. *Id.* ¶20.



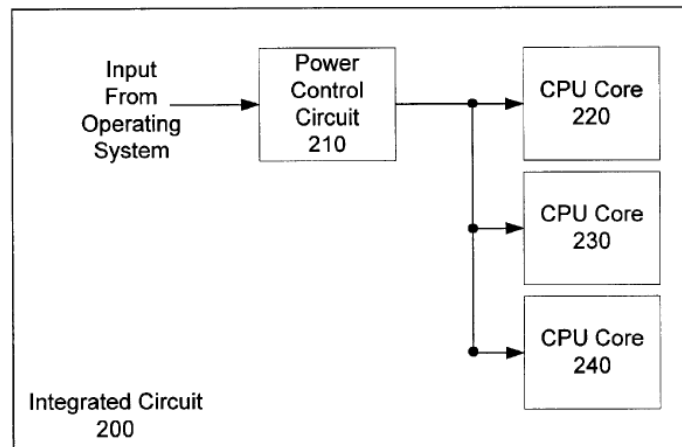
In Naveh, hardware coordination logic 16 receives operating requirements 18, 20 from cores 12, 14 and selects one of them to be shared resource setting 22. *Id.* ¶¶26–27. In a “max detect” mode, coordination logic 16 selects the higher of operating requirements, and in a “minimum-of-both-requests” mode, coordination logic 16 selects the lower of operating requirements. *Id.* ¶¶23, 26, 27, 33, 39.

B. Saeed (Ex-1006)

Saeed was filed January 22, 2003, and published March 23, 2004. Ex-1007, cover. Saeed qualifies as prior art under pre-AIA 35 U.S.C. § 102(a), (b), and (e).

Saeed teaches that the OS measures a workload based on the level of multi-threadedness. *Id.*, 2:9–11, 3:13–16. Power control circuit 210 receives and uses this workload configuration input to adjust the cores’ voltage and frequency. *Id.*, 3:8–

22, 4:35–37. Power control circuit 210 may also use this workload configuration input to select different power/performance modes. *Id.*, 4:24–35; Ex-1002 ¶40.



C. Titiano (Ex-1007)

Titiano was filed December 11, 2007, and published July 3, 2008. Ex-1006, cover. Titiano qualifies as prior art under at least pre-AIA 35 U.S.C. § 102(a), (b), and (e).

Titiano discloses a processor with multiple cores, a cache memory, and an interconnect coupling the cores to the cache. *Id.* ¶¶11, 63, 76. The cores “use a shared resource for operations.” Ex-1007 ¶13

Titiano describes using Dynamic Voltage and Frequency Scaling (DVFS) to dynamically adjust the voltage and frequency of the cores. *Id.* ¶¶107, 109. As illustrated in Figure 8, the SoC Voltage Controller receives voltage requests from the cores and selects the highest voltage request as the “voted resource level,” which it uses to update the voltage setting for the cores.

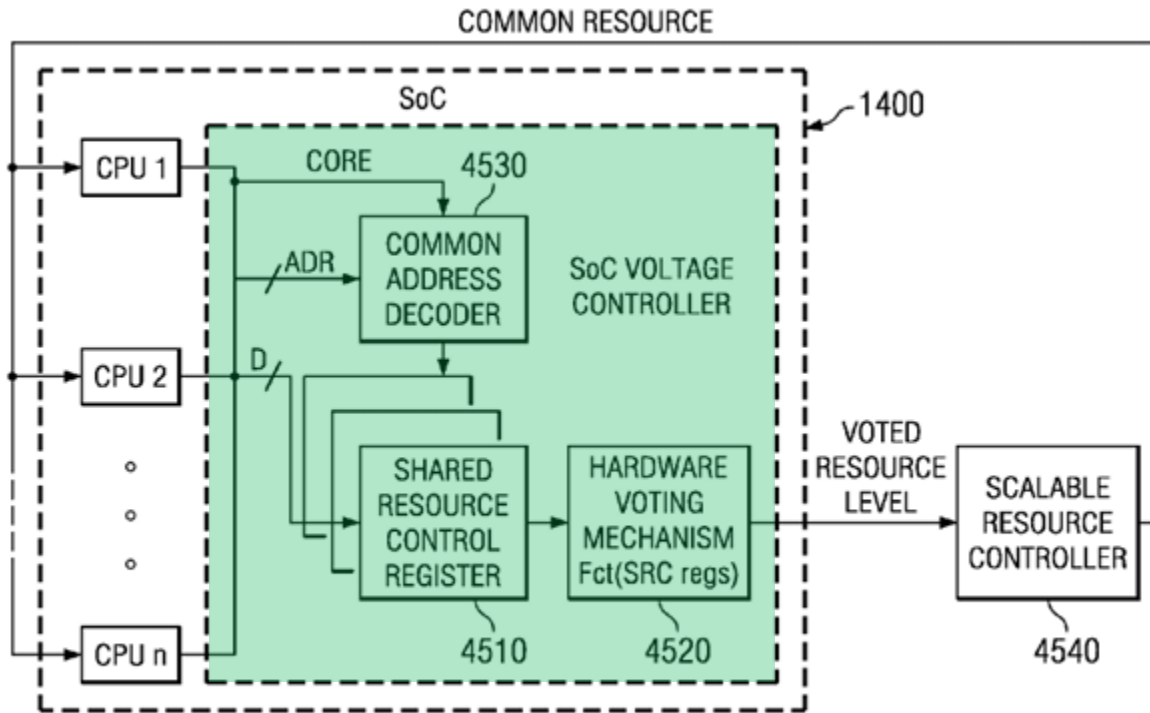


FIG. 8

Titiano also describes Dynamic Power Switching (DPS) and Adaptive Voltage Scaling (AVS) as additional features that may be combined with DVFS and used to manage power and performance of the multi-core processor. *Id.* ¶106. DPS is used to switch the cores to a sleep or low-power standby mode when they are not active. *Id.* ¶114. AVS is used to adjust the power supply voltage based, in part, on “the temperature induced current performance of the device.” *Id.* ¶174.

D. Hansquine (Ex-1008)

Hansquine was filed February 8, 2010, and published January 6, 2011. Ex-1008, Cover. Hansquine qualifies as prior art under pre-AIA 35 U.S.C. § 102(a) and (e).

Hansquine describes a particular implementation of AVS. Ex-1008 ¶8.

Figure 13 discloses a two-dimensional AVS table that can be used to implement AVS. *Id.* ¶9.

AVS Frequency/Voltage Level Table (140)

142

	T (°C)		f ₁	f ₂	...	f _N
B ₁ →	80	60	1.2V	1.18V	...	
B ₂ →	60	40	1.1V	1.08V	...	
B ₃ →	40	20	1.0V	.99V	...	
B ₄ →	20	0	⋮	⋮	...	⋮
B _N →	⋮	⋮	.95V	.94V	...	

144

$f_1 > f_2 > f_N$

FIG. 13

VI. CLAIM CONSTRUCTION

Petitioner interprets the '197 Patent's claims according to the *Phillips* claim construction standard. 37 C.F.R. § 42.100(b). To resolve the particular grounds presented in this Petition, Petitioner does not believe that any term requires explicit construction.² Ex-1002 ¶26.

² Petitioner reserves all rights to raise claim construction and other arguments in district court. Additionally, Petitioner will request leave to submit the district court's claim construction when available.

VII. DETAILED EXPLANATION OF THE UNPATENTABILITY GROUNDS

As explained below, the subject matter of the challenged claims is disclosed by the prior art.

A. Grounds 1 and 2: Claims 1–3 and 19–20 Are Obvious Over Naveh and Obvious Over Naveh in view of Saeed

1. A POSITA would have been motivated to combine Naveh with Saeed

In addition to the reasons set out below, a POSITA would have been motivated to combine Naveh and Saeed’s teachings, and would have had a reasonable expectation of success in doing so, because they are from the same field of endeavor and relate to the same well-known technologies. Ex-1002 ¶¶66. Naveh and Saeed provide complementary solutions for power management of multi-core processors. Ex-1005 ¶¶4–7, 19, 22–27, 29, 33, 41; Ex-1006, 2:47–3:7.

Naveh teaches a power controller (hardware coordination logic 16) that receives operating requirements 18, 20 from cores 12, 14 and selects the higher or lower of the requirements depending on the policy or mode of operation. *See infra* Section V.A.2.f.ii

Saeed teaches a power controller (power control circuit 210) that receives and use a workload configuration input to determine a policy or mode of operation. *See infra* Section V.A.2.f.i.

A POSITA would have been motivated to modify Naveh to select the policy or mode of operation (maximum or minimum policy in Naveh) based on a workload configuration input as taught in Saeed. Ex-1002 ¶¶66–69. Such modification would lead to a more adaptive processor and improve efficiency, which lowers operating costs and extends useful life of the products. *Id.* ¶68; *see* Ex-1005 ¶¶9, 70, 106, 110, 252–53; Ex-1006, 1:15–25, 3:3–5, 3:28–30; *Dystar Textilfarben GmbH v. C.H. Patrick Co.*, 464 F.3d 1356, 1368 (Fed. Cir. 2006) (explaining that the Federal Circuit has “repeatedly held that an implicit motivation to combine exists not only when a suggestion may be gleaned from the prior art as a whole, but when the ‘improvement’ is technology-independent and the combination of references results in a product or process that is more desirable...because it is stronger, cheaper, cleaner, faster, lighter, smaller, more durable, or more efficient”).

A POSITA would have had a reasonable expectation of success in combining Naveh and Saeed’s teachings because each purports to solve similar problems in similar and predictable ways. Ex-1002 ¶69; *Intel Corp. v. PACT XPP Schweiz AG*, No. 2022-1037, 2023 WL 2469631, at *4 (Fed. Cir. Mar. 13, 2023) (“[I]f there’s a known technique to address a known problem using ‘prior art elements according to their established functions,’ then there is a motivation to combine.”). Because both Naveh and Saeed focus on power management of cores

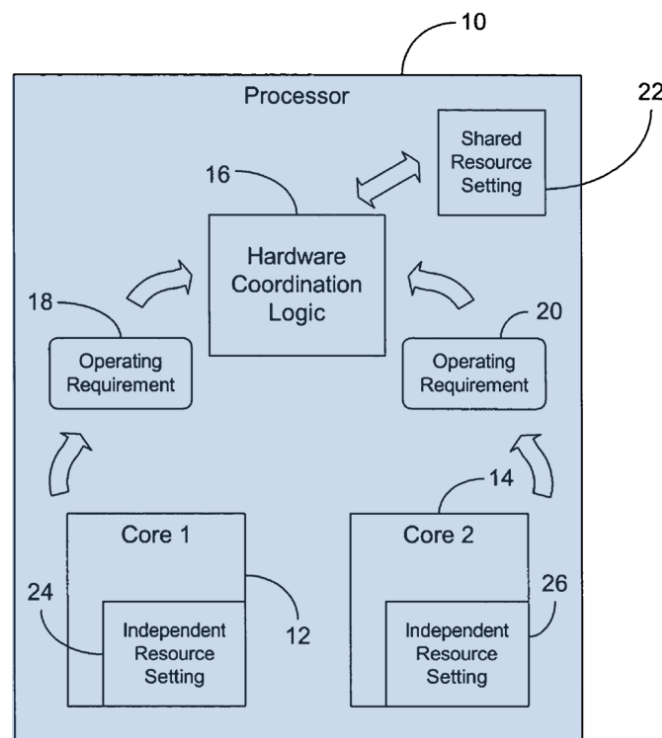
in a multi-core processor, a POSITA would have been motivated to combine the teachings of Naveh and Saeed. *Id.* ¶¶66.

2. Independent Claim 1

a. Element 1[preamble]: A processor comprising:

To the extent that the preamble of Claim 1 is limiting, Naveh discloses the preamble. Ex-1002 ¶¶70–72.

Naveh is directed to “coordinating power management activities in multi-core processors.” Ex-1005 ¶2. Figure 1 below shows processor 10. *Id.* ¶18.

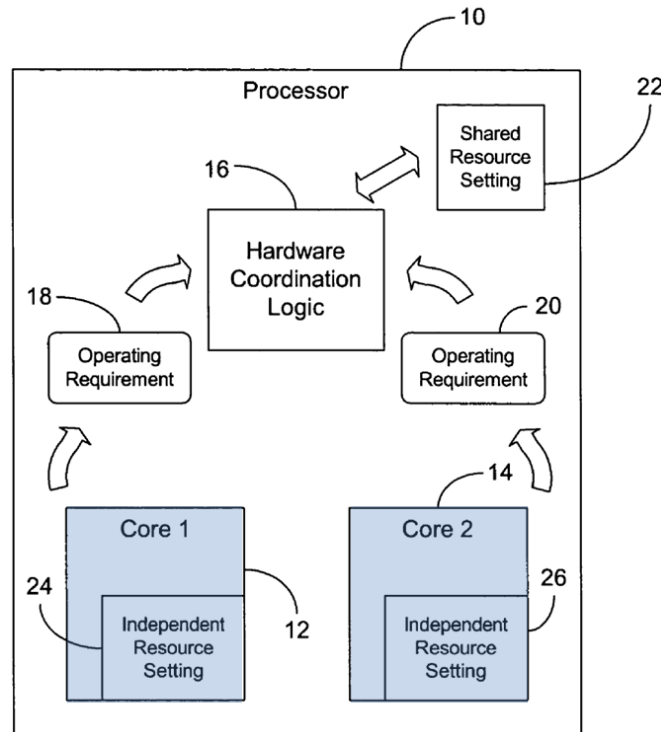


b. Element 1[a]: a plurality of cores;

Naveh discloses Element 1[a]. Ex-1002 ¶¶73–74.

Cores 12 and 14 in Figure 1 correspond to the claimed “plurality of cores.”

Id.; Ex-1005 ¶¶17, 22.



c. Element 1[b]: a cache memory;

Naveh discloses Element 1[b]. Ex-1002 ¶75.

Naveh describes that “scaling the frequency of the bus that the processor uses to communicate with other components such as chipsets, *memory subsystems*, input/output (I/O) devices, etc.” Ex-1005 ¶5 (emphasis added). A POSITA would have understood that a shared L2 cache is a well-known element in “memory subsystems” such as described in Naveh. Ex-1002 ¶¶51–55, 75. A shared L2 cache provides speed and other advantages for a memory subsystem *Id.* ¶¶51–55; *Intel*,

2023 WL 2469631, at *4 (“[I]f there’s a known technique to address a known problem using ‘prior art elements according to their established functions,’ then there is a motivation to combine.”). Thus, it would have been obvious to implement a shared L2 cache in the memory subsystem of Naveh’s processor. Ex-1002 ¶¶51–54, 75.

d. Element 1[c]: an interconnect to couple the plurality of cores to the cache memory;

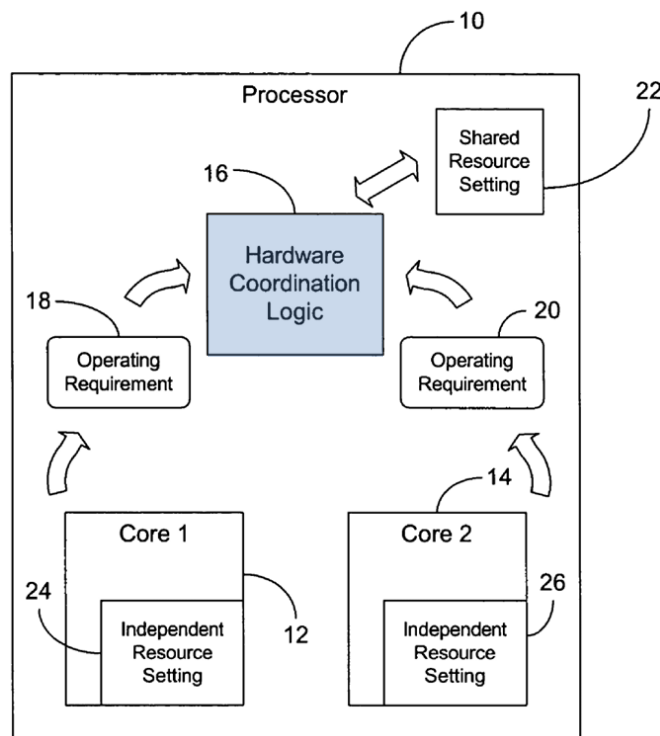
Naveh teaches Element 1[c]. Ex-1002 ¶¶76–77.

As discussed above with reference to Elements 1[preamble], 1[a], and 1[b], Naveh discloses a processor with a plurality of cores, and it would have been obvious to implement a shared L2 cache memory. *See supra* Section VII.A.2.a–c. The cores must be able to access the shared L2 cache memory, and thus, it would have been obvious to a POSITA to include in Naveh’s processor an interconnect to couple the plurality of cores to the cache memory. *Id.* ¶¶51–55, 76. For example, Naveh discloses that processor 10 of Figure 1 may include a bus (even though not illustrated in Figure 1). Ex-1005 ¶18; *see id.* ¶¶5, 17. A POSITA would have understood to use an interconnect, such as a bus, to couple the plurality of cores to the cache memory. Ex-1002 ¶¶51–55, 76–77. For at least these reasons, Naveh discloses or renders obvious an interconnect to couple the plurality of cores to the cache memory.

e. Element 1[d]: a power controller to control a plurality of power management features of the processor;

Naveh discloses Element 1[d]. Ex-1002 ¶¶78–80.

Hardware coordination logic 16 in Naveh corresponds to the claimed “power controller.” *Id.* As indicated by its name, *hardware* coordination logic 16 is implemented in hardware. *See, e.g., id.* ¶¶ 28, 37, 41; Ex-1002 ¶79.



Naveh teaches that coordination logic 16 controls power management settings shared by cores 12 and 14, which are called shared resource settings 22. Ex-1005 ¶¶20, 22; Ex-1002 ¶80. Naveh identifies clock frequency and power supply voltage as examples of shared resource settings 22. Ex-1005 ¶¶20, 31. By controlling shared resource settings 22 (such as clock frequency and power supply

voltage), coordination logic 16 “control[s] a plurality of power management features of the processor,” as recited in Element 1[d]. Ex-1002 ¶80.

- f. Element 1[e]: wherein the power controller includes a tuning circuit to receive a workload configuration input regarding a workload, receive a plurality of energy performance bias (EPB) values and determine a global EPB value based thereon, and update at least one setting of at least one of the plurality of power management features based on the workload configuration input and the global EPB value**

Naveh teaches Element 1[e]. Ex-1002 ¶¶81–102.

As explained above, the claimed “power controller” is hardware coordination logic 16 in Naveh. The claimed “tuning circuit” is the portion of hardware coordination logic 16 that implements the functions recited in Elements 1[e1], 1[e2] and 1[e3]. Ex-1002 ¶81.

As for Elements 1[e1], 1[e2] and 1[e3], this paragraph presents a brief overview of Naveh’s teachings and the following subsections provide more detailed analysis. According to Naveh, coordination logic 16 receives operating requirements 18, 20 from cores 12, 14 and selects one of them as shared resource setting 22. Ex-1005 ¶¶26, 39. Operating requirements 18, 20 received from cores 12, 14 are “a plurality of energy performance bias (EPB) values,” and the operating requirement selected as shared resource setting 22 is “a global EPB value.” *See infra* Section VII.A.2.f.ii. Naveh further teaches that coordination logic 16 may select shared resource setting 22 based on a performance/maximum policy or

power/minimum policy. Ex-1005 ¶23. The “workload configuration input” in Naveh corresponds to the information that coordination logic 16 receives and uses to determine whether to apply a performance/maximum policy or power/minimum policy. *See infra* Section VII.A.2.f.i.

i. Element 1[e1]: a tuning circuit to receive a workload configuration input regarding a workload;

Naveh teaches Element 1[e1]. Ex-1002 ¶¶83–90.

For “workload configuration input” in Elements 1[e1] and 1[e3], this Petition presents two alternative Grounds, which are addressed separately below.

Ground 1 (Naveh renders Element 1[e1] obvious):

As summarized above and described in additional detail below in Element 1[e2], coordination logic 16 receives operating requirements 18, 20 from cores 12 and 14. Ex-1005 ¶22. Coordination logic 16 compares operating requirements 18, 20 and selects one of them to be shared resource setting 22. *Id.* ¶¶26–27. In one mode, coordination logic 16 selects the higher of the two operating requirements. *Id.* ¶¶26, 39. Naveh refers to this mode as a performance/maximum policy. *Id.* ¶¶23, 27. In another mode, coordination logic 16 selects the lower of the two operating requirements. *Id.* ¶27. Naveh refers to this mode as a power/minimum policy. *Id.* ¶¶23, 27.

Naveh also states that the mode or policy may change over time depending on “what is currently the most important factor [i.e., performance or power] for software to control.” *Id.* ¶¶23, 41. Thus, coordination logic 16 receives, from software, information indicating whether to apply a performance/maximum or power/minimum policy. *Id.* This information is a workload configuration input. Ex-1002 ¶85. A performance/maximum policy indicates that the current workload is of a type that need to be processed quickly, and thus performance is more important than power for this workload. *Id.* On the other hand, a power/minimum policy indicates that the current workload is of a type that does not need to be processed quickly, and thus power is more important than performance for this workload. *Id.* Thus, the information determining the policy setting is a workload configuration input, and Naveh teaches that hardware coordination logic 16 receives this workload configuration input from the software. *Id.*

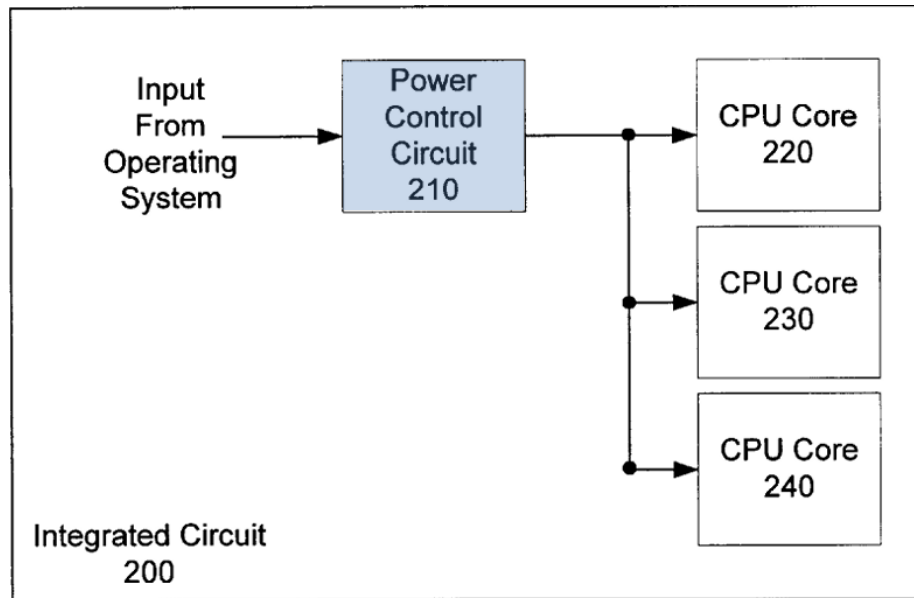
Alternatively, it would have been obvious to a POSITA to implement Navah’s hardware coordination logic 16 to receive a workload configuration input regarding a workload to determine whether to apply a performance/maximum policy or power/minimum policy. Ex-1005 ¶¶23, 41; Ex-1002 ¶¶56–58, 66–69, 86. Naveh teaches that the policy may change over time depending on “what is currently the most important factor [i.e., performance or power] for software to control” (Ex-1005 ¶¶23, 41) and that “processor 10 may have a feature that is able

to scale down the processor clock frequency to save power supply voltage (e.g., core voltage) when high performance is either not needed or not desired” (*id.* ¶18). Thus, it would have been obvious to a POSITA that the policy described in Naveh could be set based on a workload configuration input (such as performance requirements for a workload) received from a user, the operating system, or the cores. Ex-1002 ¶¶56–58, 66–69, 86. Thus, it would have been obvious that the tuning circuit of Naveh receives a “workload configuration input regarding a workload.” *Id.*

Ground 2 (Naveh in view of Saeed renders Element 1[e1] obvious):

The Naveh-Saeed combination also renders element 1[e1] obvious. Based on Saeed’s disclosure of using a workload configuration input to determine a mode of operation, it would have been obvious to a POSITA to modify Naveh to receive a workload configuration input to determine whether to apply a performance/maximum policy or power/minimum policy in Naveh. *Id.* ¶¶66–69, 90.

In Saeed, power control circuit 210 is a power controller including a tuning circuit. Ex-1002 ¶88. Power control circuit 210 controls the frequency and voltage of cores 220, 230, 240. Ex-1006, 3:8–13.



Like Naveh, Saeed recognizes a tradeoff between performance and power consumption (Ex-1006, 1:20–26, 2:1–4) and that the voltage and frequency applied to the cores affect performance and power consumption (*id.*, 2:63–3:5). Saeed teaches that power control circuit 210 receives as an input a measure of workload from the OS³ (*id.* 3:13–15) and uses this workload configuration input to adjust the cores' voltage and frequency (*id.*, 3:8–22, 4:35–37). Saeed also describes that power control circuit 210 may also use this workload configuration input to select different power/performance modes. *Id.*, 4:24–35; Ex-1002 ¶89.

³ As an example, Saeed teaches that the OS may determine workload by calculating the level of multi-threadedness. Ex 1006, 2:9–18 (describing use of a counter to determine the percentage of the workload that is multithreaded as opposed to single-threaded); 3:8–22.

It would have been obvious to a POSITA to apply the teachings of Saeed to hardware coordination logic 16 of Naveh. Ex-1002 ¶¶66–69, 90; *see also supra* Section VII.A.1. Specifically, it would have been obvious for coordination logic 16 of Naveh “to receive a workload configuration input regarding a workload” so that it could use the workload configuration input to determine the mode of operation, as taught by Saeed. Ex-1002 ¶¶56–58, 66–69, 90; *see also supra* Section VII.A.1. Hardware coordination logic 16 could use the workload configuration input to decide whether to apply a performance/maximum or power/minimum policy. Ex-1002 ¶90. For example, if the workload configuration input (e.g., level of multi-threadedness) was above a threshold, as Saeed teaches (Ex-1006, 2:27–32), coordination logic 16 could apply a performance/maximum policy and select the higher the two cores’ operating requirements to be shared resource setting 22, and if the workload configuration input was below the threshold, as Saeed teaches (*id.*), coordination logic 16 could apply a power/minimum policy and select the lower of the two cores’ operating requirements as shared resource setting 22. Ex-1002 ¶90. A POSITA would have been motivated to use of a workload configuration input to enable coordination logic 16 to apply a policy appropriate for the demands of applications running on the processor and to achieve a better balance of performance and power efficiency of the processor. *Id.* ¶¶56–58, 90.

ii. Element 1[e2]: a tuning circuit to ... receive a plurality of energy performance bias (EPB) values and determine a global EPB value based thereon;

Naveh discloses Element 1[e2]. Ex-1002 ¶91.

As stated above, the portion of coordination logic 16 that performs the functions recited in Elements 1[e1], 1[e2] and 1[e3] is the claimed “tuning circuit.” *See supra* Section VII.A.2.f. According to Naveh, coordination logic 16 receives operating requirements 18, 20 from cores 12, 14, compares operating requirements 18, 20, and selects one of them as shared resource setting 22. Ex-1005 ¶¶26, 27, 39. Operating requirements 18, 20 are “a plurality of energy performance bias (EPB) values,” and the one selected as shared resource setting 22 is “a global EPB value.” Ex-1002 ¶91. Thus, Naveh teaches “a tuning circuit ... to receive a plurality of energy performance bias (EPB) values and determine a global EPB value based thereon.” *Id.*

With reference to Figure 1, Naveh teaches that coordination logic 16 receives operating requirements 18, 20 from cores 12, 14, and coordination logic 16 determines shared resource setting 22 based on operating requirements 18, 20. Ex-1005 ¶22.

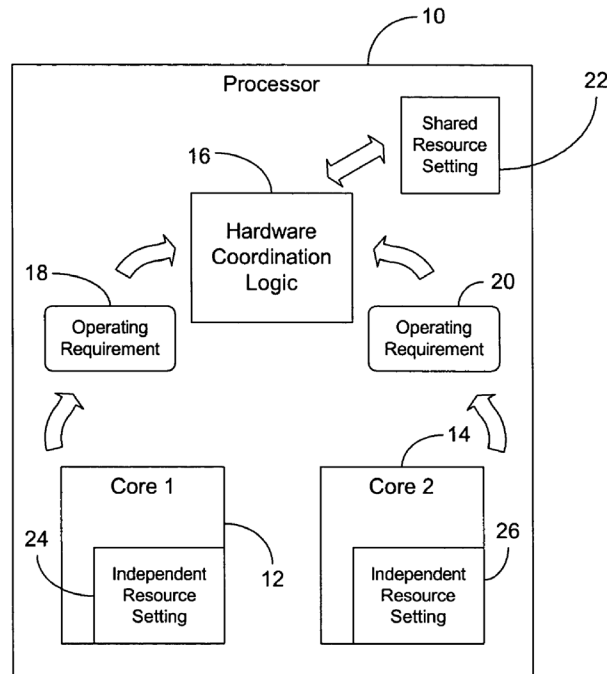


FIG. 1

Just as the ‘197 Patent states that the tuning circuit may “receive incoming EPB values from multiple cores of a multicore processor” (Ex-1001, 4:59-60), Naveh describes coordination logic 16 receiving operating requirements 18, 20 from cores 12, 14. Ex-1005 ¶22. Naveh states that after the operating requirements are “received by the coordination logic, they can be compared to one another for selection of an appropriate *global* setting.” *Id.* ¶31 (emphasis added). In one mode, coordination logic 16 selects the higher of the two operating requirements. *See id.* ¶26; Ex-1002 ¶92. Naveh refers to this mode as a “maximum” or “performance” policy. Ex-1005 ¶¶23, 27; Ex-1002 ¶92. In another mode, coordination logic 16 selects the lower of the two operating requirements. Ex-1005 ¶27; Ex-1002 ¶92.

Naveh refers to this mode as a “minimum” or “power” policy. Ex-1005 ¶¶23, 27; Ex-1002 ¶92.

Figure 7 provides an example of coordination logic 16 implementing the performance/maximum policy. Ex-1002 ¶93. Coordination logic 16 receives first operating requirements 18, 20 from core 12, 14 at blocks 96 and 98. *Id.* Coordination logic 16 compares the operating requirements at blocks 112 and 114 and selects the higher of the operating requirements as shared resource setting 22 at blocks 116 and 118. Ex-1005 ¶39; Ex-1002 ¶93.

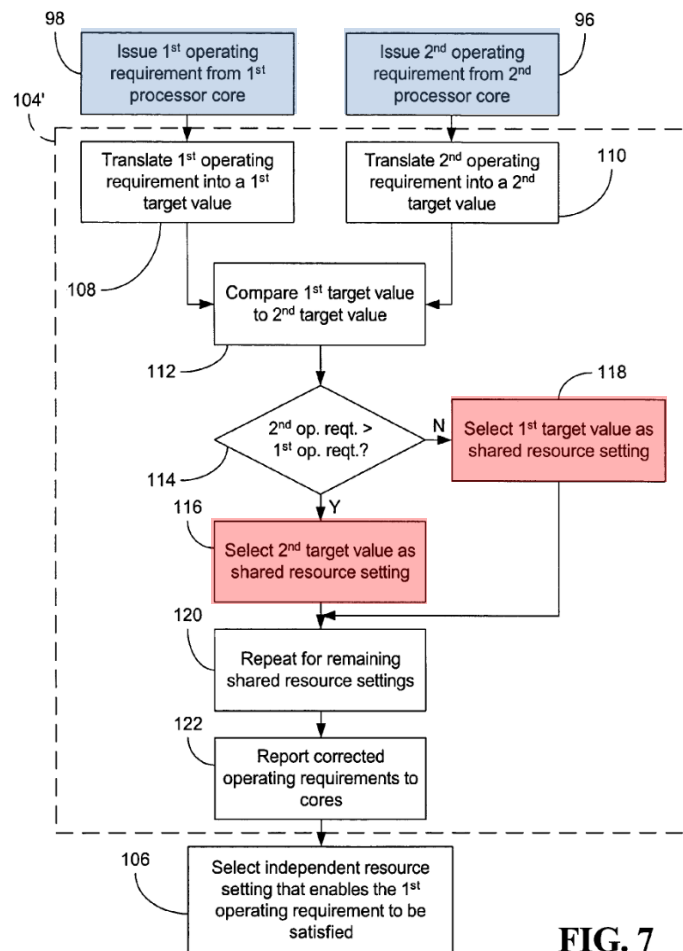


FIG. 7

Operating requirements 18, 20 and shared resource setting 22 represent tradeoffs between power and performance and, thus, are EPB values. Ex-1002 ¶94. According to the '197 Patent, energy performance bias (EPB) values represent a tradeoff between power and performance. Ex-1001, 2:34–38 (“a power/performance tradeoff preference”), *id.*, 3:49–51 (“Each EPB value can be mapped to a corresponding level of tradeoff between power and performance.”); *id.*, 4:58–64 (“power management tuning circuit 100 can ... use these [EPB] values to determine an appropriate tradeoff between power and performance policies”); Ex-1002 ¶94.

In Naveh, operating requirements 16, 18 and shared resource setting 22 represent the same tradeoff between power and performance. Ex-1002 ¶95. Specifically, Naveh describes saving power by scaling down the frequency and voltage of the cores when performance is not needed or desired: “For example, the processor 10 may have a feature that is able to scale down the processor clock frequency and power supply voltage (e.g., core voltage) when high performance is either not needed or not desired.” Ex-1005 ¶18; *see id.* ¶¶20 (identifying frequency and voltage as shared resource setting 22), 23, 36 (describing “a clock source 30 with a shared frequency setting 22”), 41; Ex-1002 ¶95.

Figure 3 of Naveh illustrates this power-performance tradeoff. Ex-1002 ¶96.

34

Combined Optimal State				Shared Feature				Independent Feature		
				SpeedStep® Control				TM1 Control		
Pindex	Perf	Abs-Pwr	Pwr%	Frequency	Vcc	Pwr%	Perf	Throttle%	Pwr%	Perf
0	1	100	100%	1700	1.233	100%	100%	0	1	100%
1	0.97	84	84%	1600	1.183	84%	97%	0	1	100%
2	0.94	68	68%	1500	1.133	68%	94%	0	1	100%
3	0.91	54	54%	1400	1.083	54%	91%	0	1	100%
4	0.88	41	41%	1300	1.008	41%	88%	0	1	100%
5	0.85	28	28%	1200	0.933	28%	85%	0	1	100%
6	0.82	16	16%	1100	0.85	16%	82%	0	1	100%
7	0.79	15	15%	1000	0.85	15%	79%	0	1	100%
8	0.76	13	13%	900	0.85	13%	76%	0	1	100%
9	0.73	12	12%	800	0.85	12%	73%	0	1	100%
10	0.7	10	10%	700	0.85	10%	70%	0	1	100%
11	0.67	9	9%	600	0.85	9%	67%	0	1	100%
12	0.58625	8	8%	600	0.85	9%	67%	0.125	0.9063	88%
13	0.5025	7	7%	600	0.85	9%	67%	0.25	0.8125	75%
14	0.41875	6	6%	600	0.85	9%	67%	0.375	0.7188	63%
15	0.335	6	6%	600	0.85	9%	67%	0.5	0.625	50%
16	0.1675	4	4%	600	0.85	9%	67%	0.75	0.4375	25%

50 52 42 44 36 38 40

FIG. 3

The higher frequencies and voltages in columns 36 and 38 correspond to higher performance levels (as shown in the columns labeled “Perf”) and correspond to less power optimization (as shown in the columns labeled “Abs-Pwr” and “Pwr%”). Ex-1002 ¶96. So, Naveh recognizes the same tradeoff between high performance and power optimization as the ’197 Patent. Ex-1002 ¶96. Operating requirements 18, 20 and shared resource setting 22 correspond to particular rows in Figure 3 and, thus, represent a tradeoff between power and performance. Ex-1005 ¶23, 36.

Shared resource setting 22 is a “global” EPB value because it indicates an energy performance bias for both cores 18 and 20 on processor 10. Ex-1002 ¶98. Naveh even describes selected resource setting 22 as a “global” setting. Ex-1005

¶31; *id.* ¶¶30 (“[S]hared resource settings may be integrated across various features and the actual operating requirements may be specified at a ‘*global*’ level.”(emphasis added)), 33 (describing the “appropriate global setting ... [as] 100% performance”), 36 (describing “a clock source 30 with a shared frequency setting 22”).

Accordingly, Naveh discloses Element 1[e2]. Ex-1002 ¶99.

iii. Element 1[e3]: a tuning circuit to ... update at least one setting of at least one of the plurality of power management features based on the workload configuration input and the global EPB value.

Naveh teaches Element 1[e3]. Ex-1002 ¶100.

As explained above, the “tuning circuit” in Naveh is the portion of coordination logic 16 that performs the functions recited in Elements 1[e1], 1[e2] and 1[e3]. Section VII.A.2.f. The “workload configuration input” in Naveh corresponds to the workload information (such as the measure of multi-threadedness described in Saeed) that coordination logic 16 receives and uses to determine whether to select the maximum or minimum of operating requirements 18, 20 as shared resource setting 22. *See supra* Section VII.A.2.f.i. The “global EPB value” is shared resource setting 22. *See supra* Section VII.A.2.f.ii.

Coordination logic 16 updates a power management feature based on shared resource setting 22 (the global EPB value). Ex-1002 ¶101. For example, as

discussed above for Element 1[e1], Naveh discloses that “clock frequency and power supply voltage settings could be viewed as a shared resource setting.” Ex-1005 ¶20; *see id.* ¶18. After coordination logic 16 selects the shared resource setting, it is “applied to the clock source and/or voltage source, instructing the shared resources to operate at the appropriate frequency and/or core voltage defined by the shared resource setting.” *Id.* ¶33. Thus, coordination logic 16 updates a power management feature (here, the frequency of the clock source and voltage of the voltage source) based on shared resource setting 22. *Id.*, Fig. 3; Ex-1002 ¶101.

Because the workload configuration input determines whether coordination logic 16 picks the maximum or minimum of operating requirements 18, 20 as shared resource setting 22 (*see supra* Section VII.A.2.f.i.), Naveh teaches that coordination logic 16 “update[s] at least one setting of at least one of the plurality of power management features based on the workload configuration input and the global EPB value.” Ex-1002 ¶102.

3. Dependent Claims 2–3, 19–20

- a. **Claim 2: The processor of claim 1, wherein the power controller is to access a power-performance tuning table based on the workload configuration input and the global EPB value, and use information from the power-performance tuning table to update the at least one setting.**

Naveh teaches dependent Claim 2. Ex-1002 ¶103. This Petition presents two grounds for Claim 2, as follows.

Ground 1 (Naveh renders Claim 2 obvious):

Under the first ground, the claimed “power-performance tuning table” is the performance state transition table in Figure 3 of Naveh. Ex-1005 ¶11; Ex-1002 ¶104.

34

Combined Optimal State				Shared Feature				Independent Feature		
				SpeedStep® Control				TM1 Control		
Pindex	Perf	Abs-Pwr	Pwr%	Frequency	Vcc	Pwr%	Perf	Throttle%	Pwr%	Perf
0	1	100	100%	1700	1.233	100%	100%	0	1	100%
1	0.97	84	84%	1600	1.183	84%	97%	0	1	100%
2	0.94	68	68%	1500	1.133	68%	94%	0	1	100%
3	0.91	54	54%	1400	1.083	54%	91%	0	1	100%
4	0.88	41	41%	1300	1.008	41%	88%	0	1	100%
5	0.85	28	28%	1200	0.933	28%	85%	0	1	100%
6	0.82	16	16%	1100	0.85	16%	82%	0	1	100%
7	0.79	15	15%	1000	0.85	15%	79%	0	1	100%
8	0.76	13	13%	900	0.85	13%	76%	0	1	100%
9	0.73	12	12%	800	0.85	12%	73%	0	1	100%
10	0.7	10	10%	700	0.85	10%	70%	0	1	100%
11	0.67	9	9%	600	0.85	9%	67%	0	1	100%
12	0.58625	8	8%	600	0.85	9%	67%	0.125	0.9063	88%
13	0.5025	7	7%	600	0.85	9%	67%	0.25	0.8125	75%
14	0.41875	6	6%	600	0.85	9%	67%	0.375	0.7188	63%
15	0.335	6	6%	600	0.85	9%	67%	0.5	0.625	50%
16	0.1675	4	4%	600	0.85	9%	67%	0.75	0.4375	25%

50 52 42 44 36 38 40

FIG. 3

As described above for Element 1[e2], coordination logic 16 receives operating requirements 18, 20 and selects one as shared resource setting 22. *See supra* Section VII.A.2.f.ii. Naveh teaches that coordination logic 16 uses operating

requirements 18, 20 (one of which is shared resource setting 22) to index into the table. Ex-1005 ¶23 (“[O]perating requirements 18, 20 could also identify a performance requirement such as a performance level or an index into a performance state transition table.”). The index into the table is shared resource setting 22, which is a global EPB value as explained above for Element 1[e2] (Section VII.A.2.f.ii). Ex-1002 ¶105. Because shared resource setting 22 is selected based, in part, on the workload configuration input (as explained above for Element 1[e1], *see supra* Section VII.A.2.f.i), coordination logic 16 accesses the table based on **both** the workload configuration input and the global EPB value as recited in Claim 2. Ex-1002 ¶108.

Naveh gives an example of using the 100% performance to index into the table and extract the target frequency/voltage value of 1700 Mhz/1.233V: “The coordination logic can therefore use the 100% performance to index into the combined optimal state portion of the table, extract the target frequency/voltage value of 1700 MHz/1.233V from the table, and place it on the control bus 66.” *Id.* ¶32. The 100% performance corresponds to “1” in the second column 52 of the annotated Figure 3 above. Ex-1002 ¶106. That entry corresponds to the 1700 MHz and 1.233V in columns 36 and 38. *Id.* Naveh further describes using the information from the table to update at least one setting, as recited in Claim 2. Ex-1005 ¶33 (“In the illustrated example, the shared resource setting 68 is applied to

the clock source and/or voltage source, instructing the shared resources to operate at the appropriate frequency and/or core voltage defined by the shared resource setting 68.”).

Ground 2 (Naveh in view of Saeed renders Claim 2 obvious):

The above Ground 1 argument also applies to Ground 2.

Moreover, the Naveh-Saeed combination provides further evidence of Claim 2’s obviousness because Saeed also teaches the use of a lookup table.

As described above, Saeed teaches that a workload configuration input (such as the level of multi-threadedness) may be used to control the performance state of a multicore processor. *See supra* Section VII.B.1.f.i; Ex 1006, 2:9–11;, 3:13–16; Ex-1002 ¶110. Saeed further teaches that power control circuit 210 may use this workload configuration input (the level of multi-threadedness) to index a “lookup table” to identify a “corresponding” frequency or voltage setting for the cores 220, 230, and 240:

The frequency setting may be a function of the level of multi-threadedness measured in operation 410. Depending on the level of multi-threadedness of the system, ***a lookup table*** or a logic circuit may be used to determine a corresponding frequency that is between the minimum frequency and the maximum frequency. Similarly, voltages of the CPU cores may be adjusted based on the level of multi-threadedness measured.

Ex-1006, 4:8–15 (emphasis added).

It would have been obvious to a POSITA to apply the teachings of Saeed to Naveh. *See supra* Section VII.A.1; Ex-1002 ¶¶66–69, 112. Both Saeed and Naveh describe using a look-up table to determine the frequency and voltage setting of the cores. Ex-1002 ¶¶104–108, 111–112; Ex-1005, Fig. 3, ¶¶23,32; Ex-1006, 4:8–15. Naveh teaches indexing the table using a global EPB value (shared resource setting 22). Ex-1005 ¶¶23, 32. Saeed teaches indexing the table using a workload configuration input (the level of multi-threadedness). Ex-1006, 4:8–15. Based on these teachings, it would have been obvious to use a two-dimensional table that can be indexed independently using both a global EPB value and a workload configuration input. Ex-1002 ¶112. A POSITA would have been motivated to do so to improve the power management of the cores. *Id.* ¶¶66–69, 104–108, 111–112. By indexing the table based on two variables, the table would include additional settings correlated more closely to the desired operating conditions of the cores, resulting in improved performance and power savings. *Id.* A POSITA would have recognized that Naveh and Saeed provide complimentary teachings and could be combined without substantial changes in their respective functions because they teach substantially similar systems. *Id.*

Thus, the Naveh-Saeed combination renders obvious dependent Claim 2.

- b. Claim 3: The processor of claim 2, wherein the tuning circuit is to update the at least one setting of the at least one power management feature responsive to the global EPB value.**

Naveh teaches dependent Claim 3 because Claim 3 is encompassed by the limitations of Claim 1. Ex-1002 ¶114; *see supra* Section VII.A.2.

- c. Claim 19: The processor of claim 1, wherein the power controller is to enable a first power management feature based on the updated at least one setting.**

Naveh teaches dependent Claim 19. Ex-1002 ¶115.

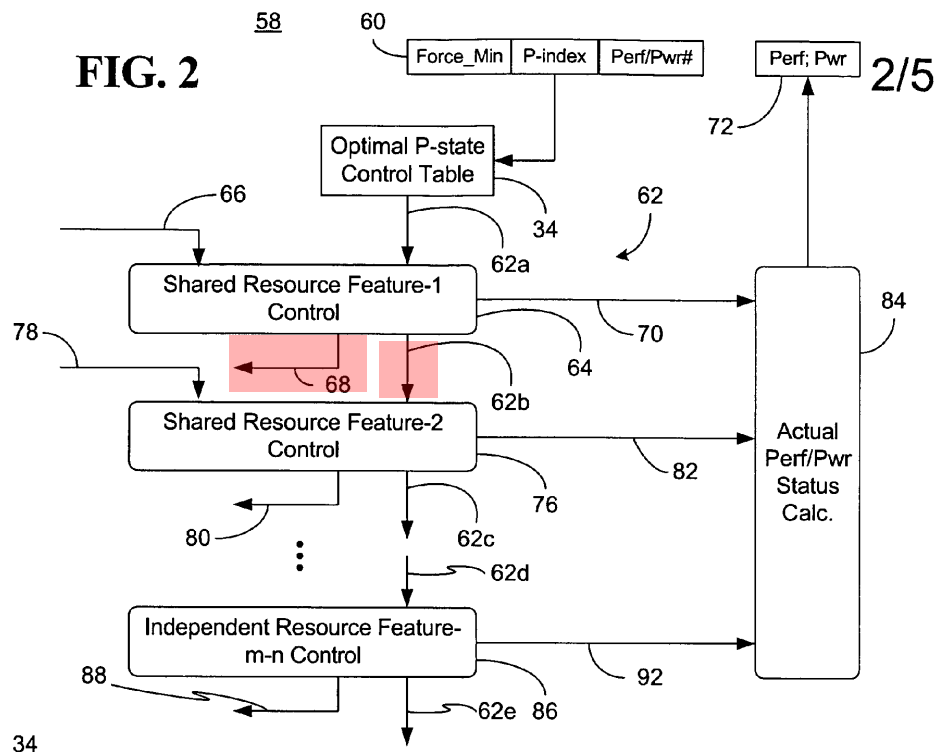
As described above with respect to Element 1[e3], Naveh teaches “updat[ing] at least one setting of at least one of the plurality of power management features.” *See supra* Section VII.A.2.f.iii. Naveh also discloses “enabl[ing] a first power management feature based on the updated at least one setting.” Ex-1002 ¶115. Naveh states that “the target values for the resource settings can be identified by *feature*.” Ex-1005 ¶31. For example, with reference to Figure 3, Naveh states, “the Speedstep® feature (‘Shared Feature’) may provide control over shared resource settings, which are illustrated as clock frequency settings (‘Frequency’) 36 and core voltage settings (‘Vcc’) 38.” Ex-1005 ¶31. Thus, Naveh teaches that coordination logic 16 enables a first power management

feature (the Speedstep® feature) based on the updated at least one setting (the frequency and voltage settings). Ex-1002 ¶115.

- d. **Claim 20: The processor of claim 1, wherein the power controller is to send an update message to a destination agent of the processor to cause the destination agent to control a first power management feature based on the updated at least one setting.**

Naveh teaches dependent Claim 20. Ex-1002 ¶116.

For example, Figure 2 shows “a power management architecture 58 that can be used to implement hardware coordination logic” 16. Ex-1005 ¶29.



Naveh states that “the shared resource setting 68 is applied to the clock source and/or voltage source, instructing the shared resources to operate at the appropriate frequency and/or core voltage defined by the shared resource setting 68.” *Id.* ¶33.

Based on this disclosure, Naveh teaches that a power controller (coordination logic 16) sends an update message to a destination agent (clock source and/or voltage source) of the processor to cause the destination agent (clock source and/or voltage source) to control a first power management feature (core frequency or voltage) based on the updated at least one setting (shared resource setting). Ex-1002 ¶116.

Alternatively, Naveh also states:

The first shared resource control block 64 can generate corrected operating requirements and/or target values based on the shared resource setting 68 and place the corrected target values on the control bus 62b, where the corrected target values enable a second shared resource control block 76 to determine a shared resource setting 80 for the next shared resource. ... In the illustrated example, the shared resource setting 80 could be a bus frequency setting.

Ex-1005 ¶34. Based on this disclosure, Naveh teaches that a power controller (coordination logic 16) sends an update message to a destination agent (second shared resource control block 76) of the processor to cause the destination agent (second shared resource control block 76) to control a first power management feature (bus frequency) based on the updated at least one setting (corrected target values based on the shared resource setting 68). Ex-1002 ¶¶116–17.

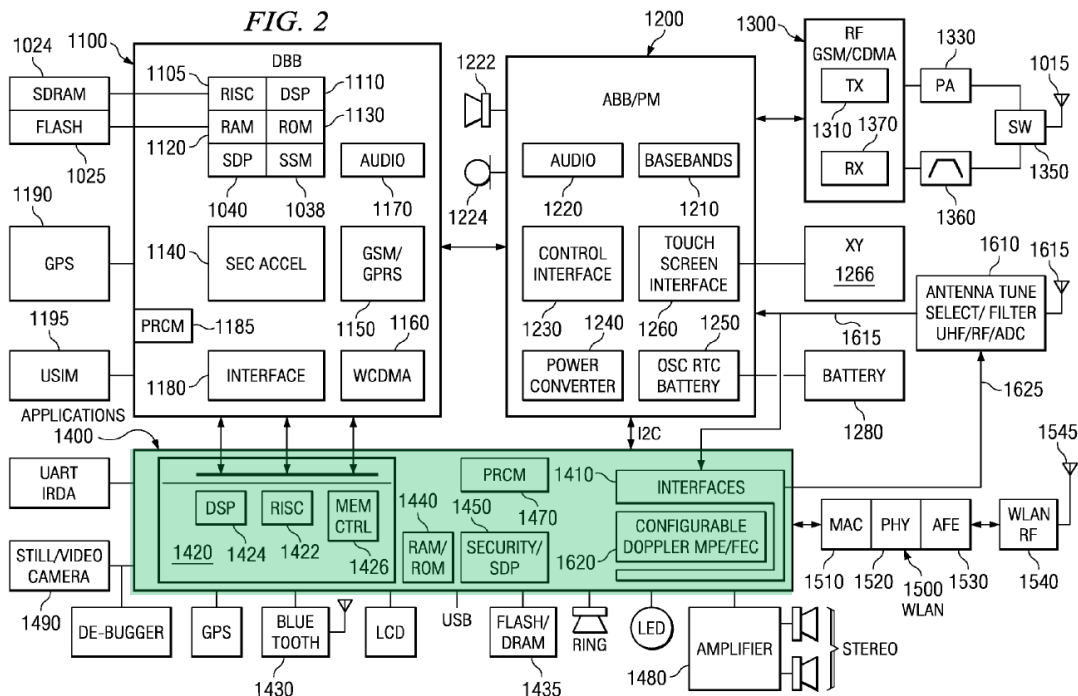
B. Ground 3: Claims 1–6, 11, 13, and 19–20 Are Obvious Over Titiano

1. Independent Claim 1

a. Element 1[preamble]: A processor comprising:

To the extent that the preamble of Claim 1 is limiting, Titiano discloses the preamble. Ex-1002 ¶118.

Titiano discloses a processor, which is typically identified as applications processor integrated circuit 1400 in the various figures. Ex-1007, Figs. 2, 3, 4, 5, 8, and 9; Ex-1002 ¶118. For example, annotated Figure 2 shows “an integrated circuit chip or core 1400 ... for applications processing and more off-chip peripherals.” Ex-1007 ¶63.



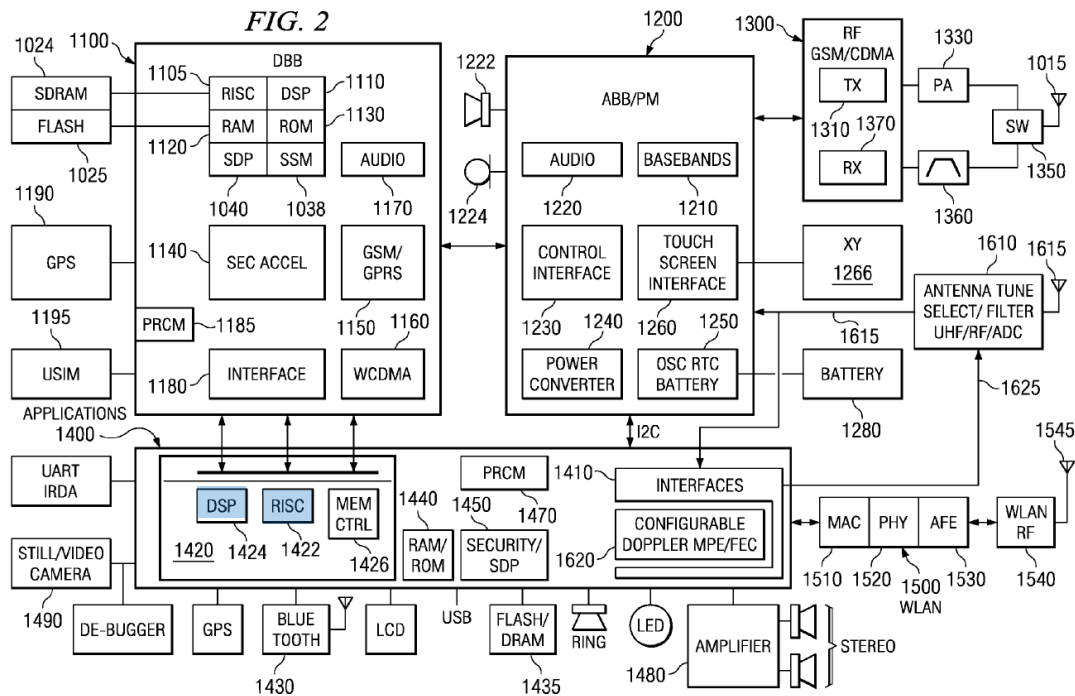
Titiano describes Figure 3 as illustrating the same processor. *Id.* ¶20 (“a block

diagram of an inventive applications processor integrated circuit in FIG. 2 with associated integrated circuits”).

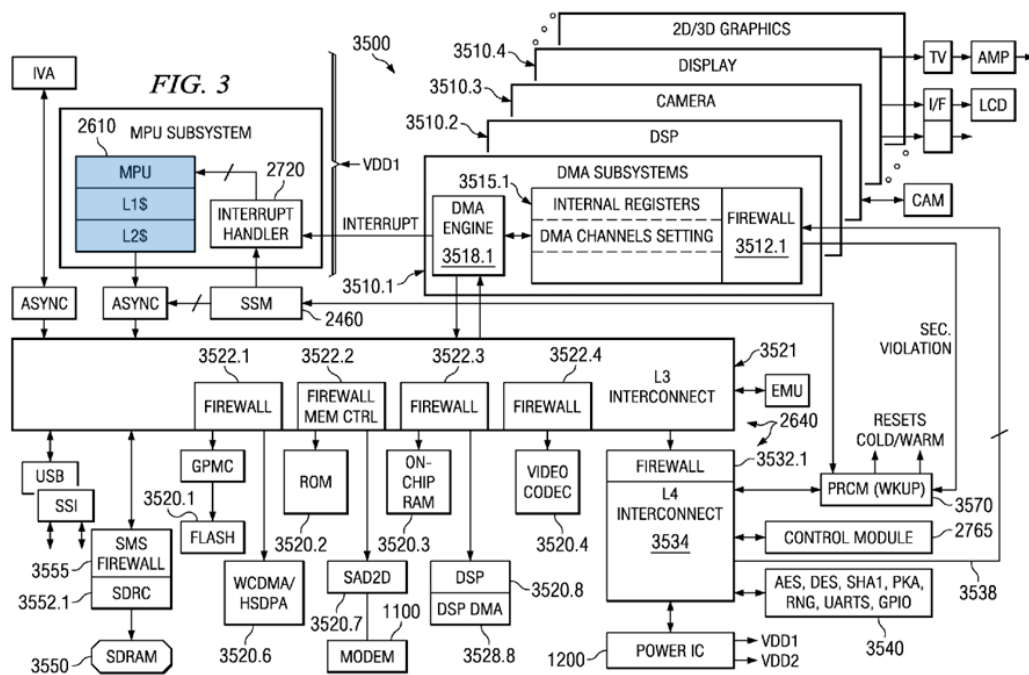
b. Element 1[a]: a plurality of cores;

Titiano discloses Element 1[a]. Ex-1002 ¶119–122.

The processor in Titiano includes a plurality of cores. *Id.* ¶119. For example, with respect to Figure 2, Titiano states that “provided on chip 1400 is an applications processing section 1420 which includes a RISC processor 1422 (such as MIPS core(s), ARM core(s), or other suitable processor), [and] a digital signal processor (DSP) 1424 such as from the TMS320C55x™ DSP generation and/or the TMS320C6x™ DSP generation from Texas Instruments Incorporated or other digital signal processor(s).” Ex-1007 ¶63.



Similarly, the processor IC in Figure 3 includes MPU subsystem, which “has one or more *processors with CPUs* such as RISC or CISC processors 2610, and having superscalar processor pipeline(s) with L1 and L2 caches.” *Id.* ¶76 (emphasis added). The CPUs in processors 2610 are a plurality of cores. Ex-1002 ¶119–120.



For the “power controller” claim elements addressed below, this Petition relies on the power management system in Figures 8–15 and 18–19, which Titiano states is “for use” in the systems of Figures 2 and 3. Ex-1007 ¶¶25–32, 35–36. Thus, the power management system in Figures 8–15 and 18–19 applies to the cores in Figures 2 and 3. Ex-1002 ¶121. Titiano illustrates those cores as boxes labeled “CPU” in Figures 8, 9, 10, 13 and 15 and as boxes labeled “CORE” in

Figures 18 and 19. *Id.* Annotated Figures 8, 10, and 13 below provide examples.

Id.

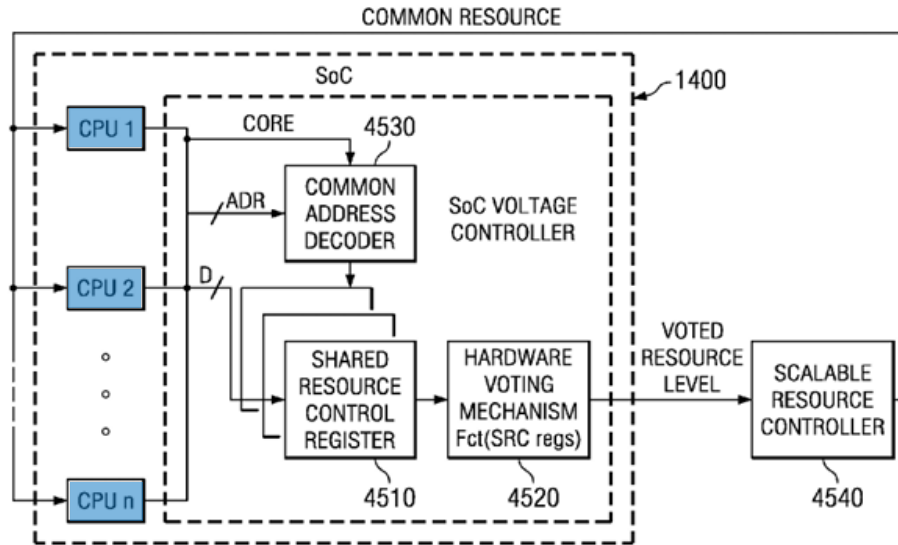


FIG. 8

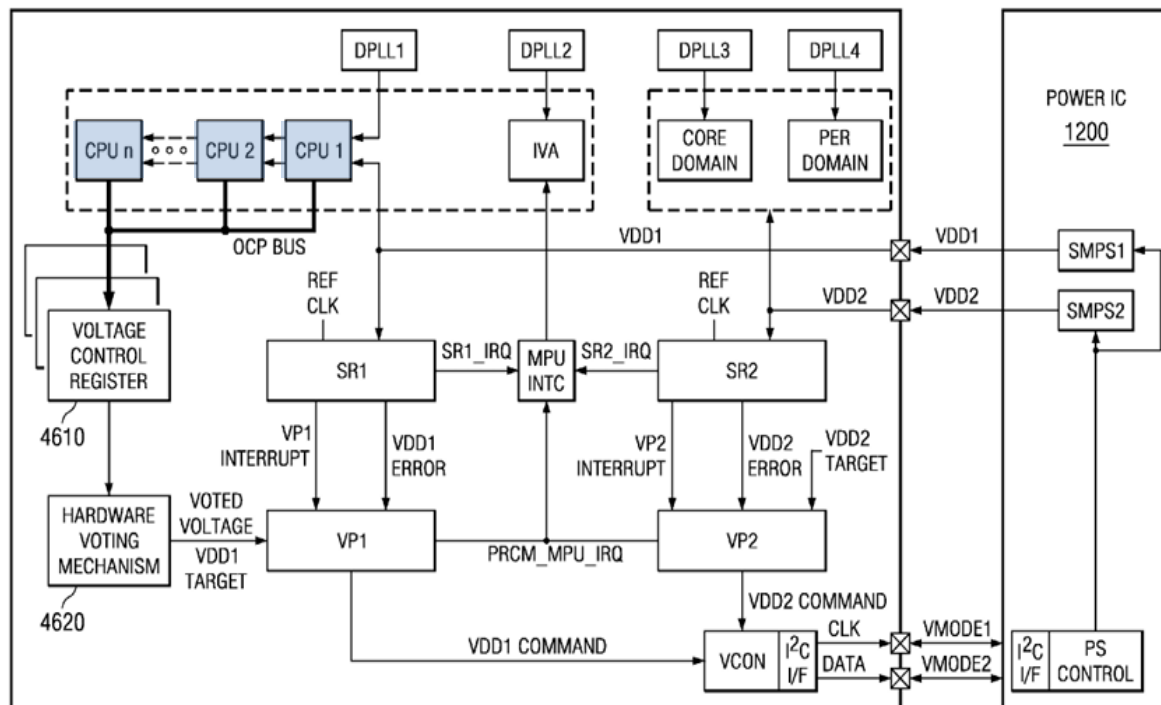


FIG. 10

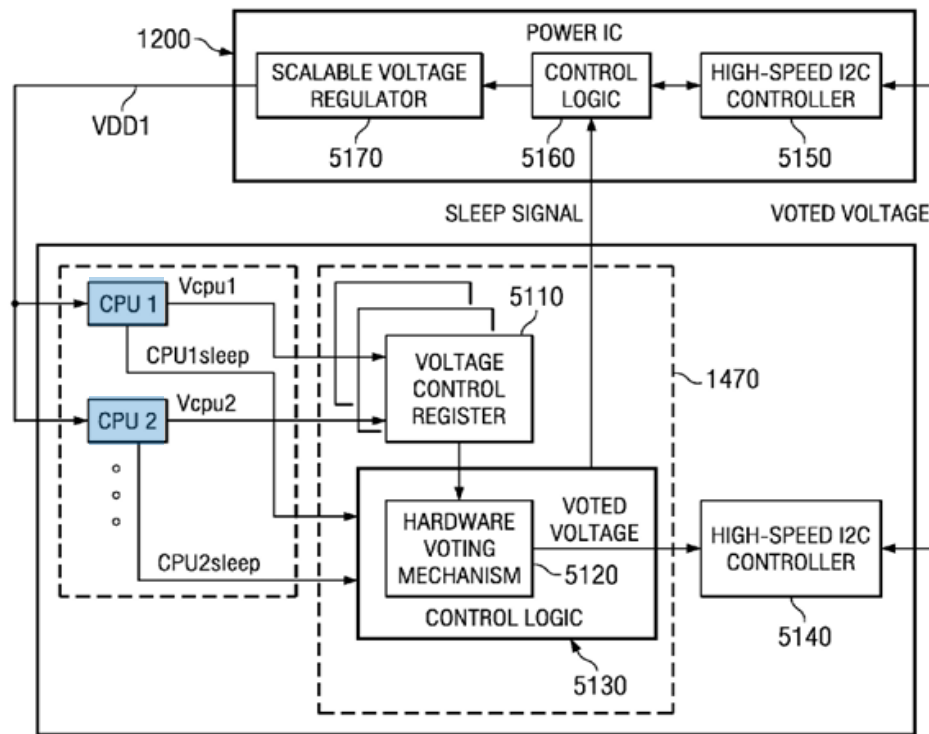


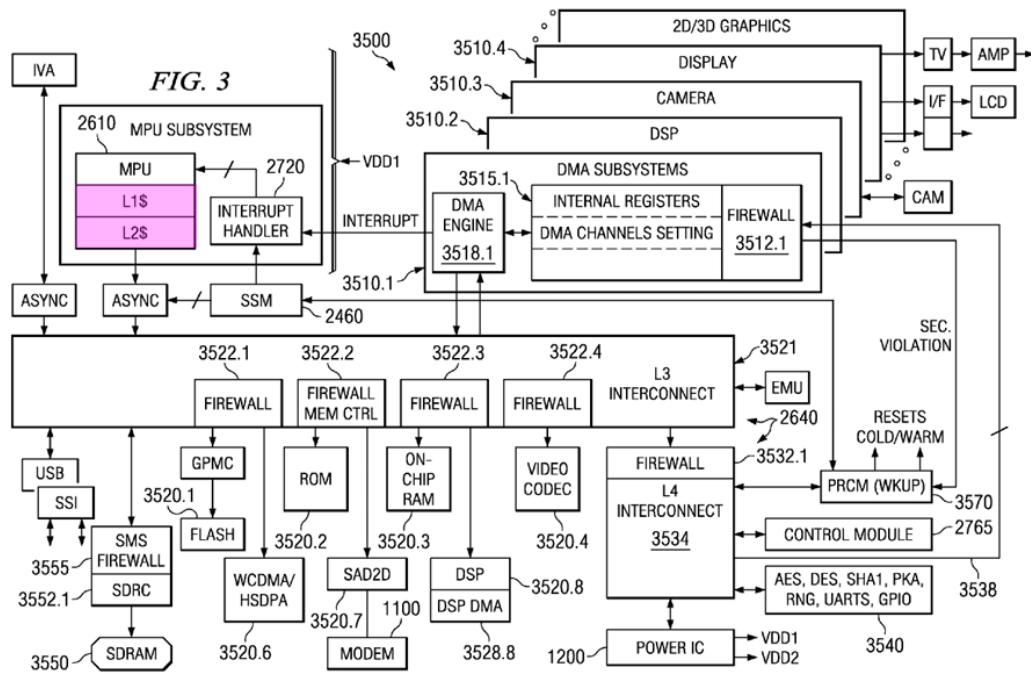
FIG. 13

Thus, Titiano discloses “a plurality of cores,” as recited in Element 1[a]. Ex-1002 ¶¶119–122.

c. Element 1[b]: a cache memory;

Titiano discloses Element 1[b]. Ex-1002 ¶¶123–24.

Titiano teaches that the RISC or CISC processors 2610 in Figure 3 have “superscalar processor pipeline(s) with *L1 and L2 caches*.” Ex-1007 ¶76 (emphasis added).



Thus, Titiano discloses “a cache memory,” as recited in Element 1[b]. Ex-1002 ¶¶122–24.

d. Element 1[c]: an interconnect to couple the plurality of cores and the cache memory;

Titiano teaches Element 1[c]. Ex-1002 ¶125.

As described above, Figure 3 of Titiano discloses a processor with a plurality of cores and L1 and L2 caches. Ex-1007 ¶76. The cores must be able to access the cache memory, which requires an interconnect. Ex-1002 ¶¶51–55, 125. A POSITA would understand that Titiano’s L2 cache is shared by the cores of the processor. *Id.* Thus, for the cores to properly access and use the L2 cache, there must be an interconnect coupling the cores to the L2 cache. *Id.* Accordingly, it is

inherent that the processor would also include an interconnect to couple the cores and cache memory. *Id.*

Alternatively, it would have been obvious to modify Titiano to include an interconnect to couple the plurality of cores to the L2 cache memory. *Id.* ¶¶51–55, 126. For example, Titiano discloses that the cores “are operable for inter-processor communication, such as by an OCP [Open Core Protocol] bus.” Ex-1007 ¶155. Therefore, a POSITA would have recognized that an OCP bus could be used as an interconnect to couple the cores together and to a cache memory. Ex-1002 ¶¶51–55, 126.

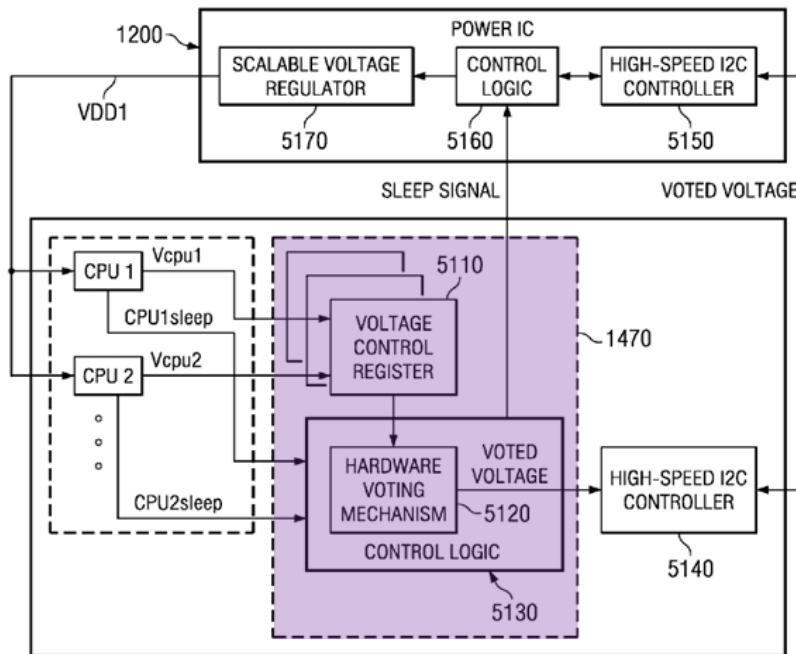
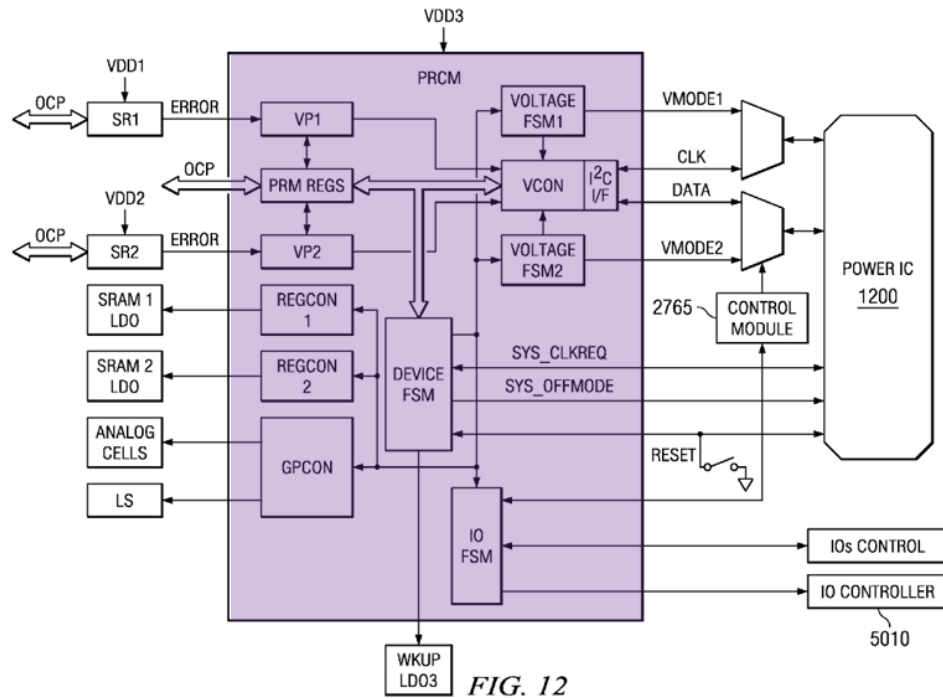
e. Element 1[d]: a power controller to control a plurality of power management features of the processor;

Titiano discloses Element 1[d]. Ex-1002 ¶127.

In Titiano, Figures 8–15 and 18–19 illustrate varying levels of detail and, thus, the claimed power controller corresponds to different blocks with different names in the figures. *Id.* ¶127. For example, Titiano describes the power controller as Power Reset and Clock Manager (PRCM) 1470 in Figures 5, 10,⁴ 12, 13,⁵ and 19, and Figures 8 and 9 illustrate the power controller as the SoC Voltage Controller. *Id.*

⁴ Titiano describes Figure 10 as including PRCM. Ex-1007 ¶¶163, 165

⁵ Titiano also calls PRCM 1470 in Figure 13 the “Power Management Control Module 1470.” Ex-1007 ¶¶185, 186.



Regardless of the nomenclature, the claimed “power controller” corresponds to the portion of the applications processor integrated circuit chip that controls the

power delivered to the processor. *See, e.g.*, Ex-1007 ¶¶119–120; Ex-1002 ¶128.

The power controller is used to control a plurality of power management features such as frequency and voltage, as described in further detail below with reference to Element 1[e]. *See infra* Section VII.B.1.f; Ex-1002 ¶128. That analysis focuses on PRCM 1470 in Figures 10, 12, 13, and 19.

- f. Element 1[e]: wherein the power controller includes a tuning circuit to receive a workload configuration input regarding a workload, receive a plurality of energy performance bias (EPB) values and determine a global EPB value based thereon, and update at least one setting of at least one of the plurality of power management features based on the workload configuration input and the global EPB value.**

Titiano teaches Element 1[e]. Ex-1002 ¶129.

In Figures 10, 12, 13, and 19 of Titiano, the power controller is PRCM 1470. The claimed “tuning circuit” is the portion of PRCM 1470 that performs the functions recited in Elements 1[e1], 1[e2] and 1[e3]. *Id.* ¶¶127–29.

- In Figure 10, the tuning circuit includes voltage control registers 4610, hardware voting mechanism 4620, and voltage processor VP1. *Id.*
- In Figures 12 and 19, the tuning circuit includes voltage control registers 4610 (which are included among the PRM registers), voltage processor VP1, and voltage controller VCON. *Id.*
- In Figure 13, the tuning circuit includes voltage control registers 5110 and control logic 5130 with hardware voting mechanism 5120. *Id.*

As described below, the tuning circuit in Titiano performs the functions recited in Elements 1[e1], 1[e2] and 1[e3].

i. Element 1[e1]: a tuning circuit to receive a workload configuration input regarding a workload;

Titiano teaches Element 1[e1]. Ex-1002 ¶130.

This Petition presents two alternative mappings for the “workload configuration input” in Elements 1[e1] and 1[e3]. One mapping is based on Titiano’s power management feature called Dynamic Power Switching (DPS); the other mapping is based on Titiano’s power management feature called Adaptive Voltage Scaling (AVS). Ex-1007 ¶106; Ex-1002 ¶130.

Dynamic Power Switching (DPS)

Titiano describes DPS as a power management feature that switches the cores to a sleep or low-power standby mode when they are not active. Ex-1007 ¶114; Ex-1002 ¶131. To implement DPS, the tuning circuit in Titiano receives a signal indicating whether the cores have an active workload (Ex-1007 ¶¶114, 211) and that signal is a “workload configuration input regarding a workload.” Ex-1002 ¶131.

Titiano states, “[b]ased on the hardware resources activity, as indicated by FIFO buffer status, for instance, DPS switches the device dynamically from any of several medium power modes to a lower power mode during application execution

or to a low power Standby mode.” Ex-1007 ¶114; *see also id.* (“DPS provides automatic hardware detection of conditions (e.g. FIFO fill status or IO hardware signals) for sleep and wakeup transition for clock and power.”). DPS also “predicts system load and switches the module clocks dynamically between On and Off modes.”⁶ *Id.*

As illustrated in annotated Figure 13, control logic 5130 receives from each CPU core a signal indicating whether the CPU has an active workload (CPU1sleep, CPU2sleep). Ex-1007 ¶188; Ex-1002 ¶133.

⁶ According to Titiano, DPS is used not only to assess the current workload of the CPU cores, but also to predict their future workload. Ex-1002 ¶132. The DPS software takes into account future workload such that it would be inefficient to place them into a sleep state, only to wake them up shortly thereafter. Ex-1007 ¶211 (“software predicts dynamically the performance requirement of the application(s) running on the processor”); Ex-1002 ¶132.

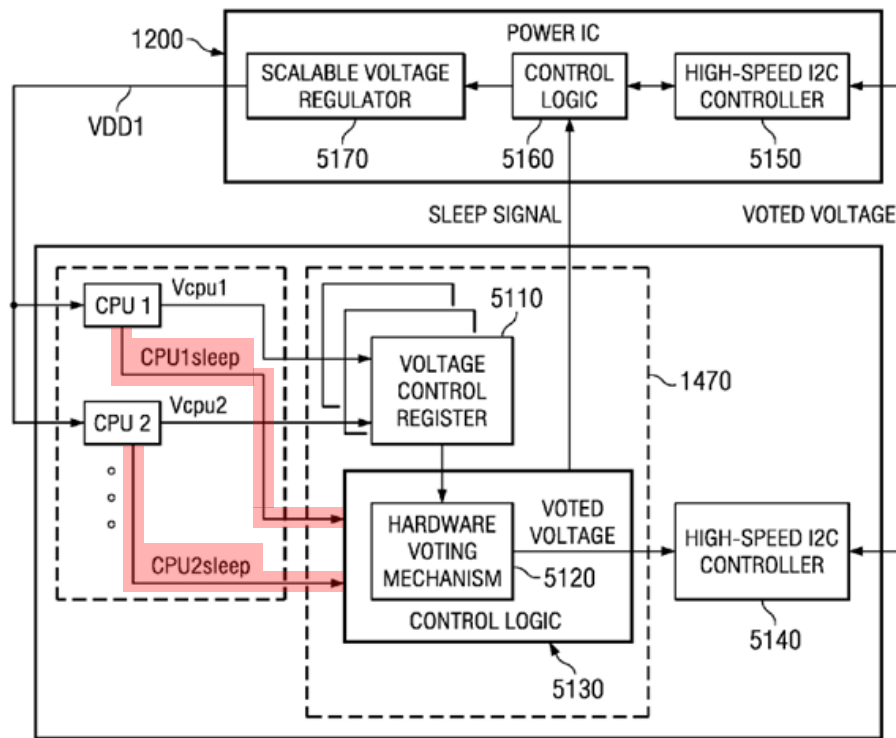


FIG. 13

For example, if the FIFO buffer status of CPU 1 is not empty, CPU1sleep signal indicates that CPU 1 has an active workload, and if the FIFO buffer status of CPU 1 is empty, CPU1sleep signal indicates that CPU 1 does not have an active workload. Ex-1007 ¶¶114, 208–209, 217; Ex-1002 ¶133. Thus, the tuning circuit of Titiano (control logic 5130) receives a workload configuration input (CPU1sleep or CPU2sleep signal) regarding a workload. Ex-1002 ¶133.

As described in further detail below with reference to Element 1[e3] (Section VII.B.1.f.iii), the tuning circuit of Titiano (control logic 5130) uses the workload configuration input to determine when all the cores are inactive so that the cores' power domain can be switched to the sleep voltage. Ex-1007 ¶¶185, 191.

Thus, Titiano's implementation of DPS teaches Element 1[e1]. Ex-1002

¶¶130–35.

Adaptive Voltage Scaling (AVS)

Titiano describes AVS as a power management feature that adjusts the power supply voltage based, in part, on “the temperature induced current performance of the device.” Ex-1007 ¶174. To implement AVS, the tuning circuit in Titiano receives a signal indicating “the temperature induced current performance of the device” and that signal is a “workload configuration input regarding a workload.” Ex-1002 ¶136.

Titiano states, “Adaptive power supply AVS reduces active power consumption. The power supply voltage is adapted to the silicon performance either statically (depending on the device manufacturing process), or dynamically (depending on the *temperature induced current performance of the device*).” Ex-1007 ¶134 (emphasis added).

The operation of AVS is illustrate below in annotated Figure 10.

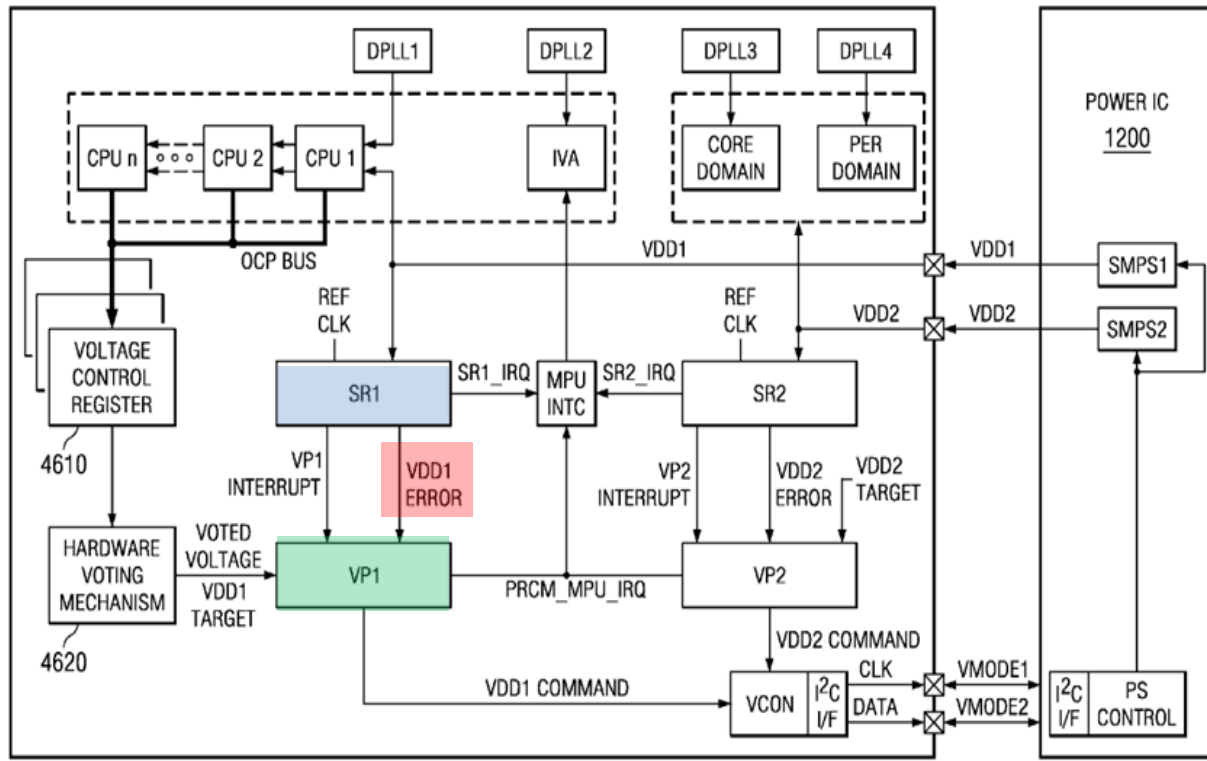


FIG. 10

As shown in Figure 10, CPU 1 and CPU 2 reside in a single voltage domain that both receive the same voltage VDD1. *Id.* ¶153, Fig. 10. Sensor Module SR1 generates a performance error signal VDD1 Error that it sends to the Voltage Processor VP1. *Id.* ¶¶177–78.

The VDD1 Error signal indicates “the temperature induced current performance of the device” (Ex-1007 ¶134), and thus is a “workload configuration input regarding a workload.”⁷ Ex-1002 ¶138. A POSITA would understand that

⁷ To the extent that the “workload configuration input” must come from a user input, it would have been obvious to modify Titiano to allow the user to set a

temperature is an indication of the load on and activity of the processor. *Id.* An increase in temperature means that more transistors are switching to process an increase in workload. *Id.* Lower temperatures correspond with less CPU-intensive workloads, such as processing emails, while higher temperatures correspond with more intensive workloads such as gaming. *Id.* The VDD1 Error signal is a direct representation of temperature (which indicates workload), allowing the processor to stay within its thermal limit. *Id.* Thus, the tuning circuit of Titiano (Voltage Processor VP1) receives a workload configuration input regarding a workload (VDD1 Error). *Id.* ¶¶136–38.

As described in further detail below with reference to Element 1[e3] (Section VII.B.1.f.iii), the tuning circuit of Titiano (Voltage Processor VP1) uses the workload configuration input to adjust the setting (VDD1 Command) provided to the voltage controller VCON. Ex-1007 ¶¶135, 156, 173, 178.

Thus, Titiano’s implementation of AVS teaches Element 1[e1]. Ex-1002

workload configuration input. Ex-1002 ¶139. For example, Titiano describes that “[w]hen performing DVFS, the user can program a new operating point in the sensor module by programming the new frequency target and caus[ing] the sensor module to re-calculate the error.” Ex-1007 ¶135. Then, “[t]he Voltage Processor takes the average frequency error from the AVS sub-chip and determines the appropriate voltage level to program into the power supply.” *Id.* Therefore, it would have been obvious to a POSITA that the user can input the AVS performance error by setting a new operating point, as described in Titiano. Ex-1002 ¶¶138–39.

¶¶136–141.

- ii. **Element 1[e2]: a tuning circuit to ... receive a plurality of energy performance bias (EPB) values and determine a global EPB value based thereon;**

Titiano teaches Element 1[e2]. Ex-1002 ¶142.

Titiano describes another power management feature, called Dynamic Voltage and Frequency Scaling (DVFS), which dynamically adjusts the shared voltage and frequency of the cores to reduce power consumption. Ex-1007 ¶¶107, 109; Ex-1002 ¶142. The tuning circuit in Titiano receives voltage requests from the cores and picks the highest of the voltage requests as the “voted voltage,” which it uses to update the voltage setting for the cores. Ex-1002 ¶142. The voltage requests received from the cores are “a plurality of energy performance bias (EPB) values” and the voted voltage is the “global EPB value.” *Id.*

Titiano states that the CPU cores submit requests for a voltage level sufficient to satisfy their operating requirements. Ex-1007 ¶12. The CPUs write their voltage requests in registers (which are called shared resource control registers 4510 in Figure 8 and voltage control registers 4610/5110 in Figures 9, 10, 12, 13, 15 and 19⁸). *Id.* ¶¶136, 137, 138, 146, 165, 196. These registers are shaded

⁸ Figures 12 and 19 illustrate PRM registers, which “include Voltage Control Registers 4610 ... and are used ... for DVFS.” Ex-1007 ¶¶165 (for Fig. 12), 220 (stating Fig. 19’s structures are analogous to Fig. 12).

red in the annotated figures below.

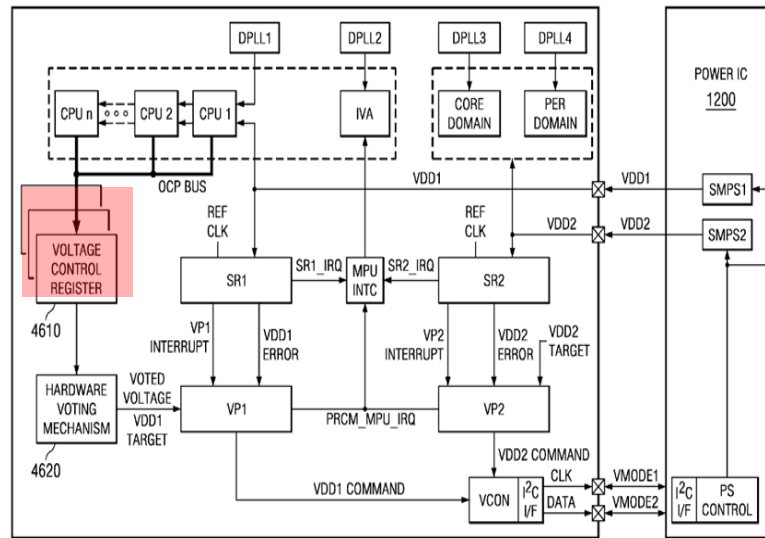


FIG. 10

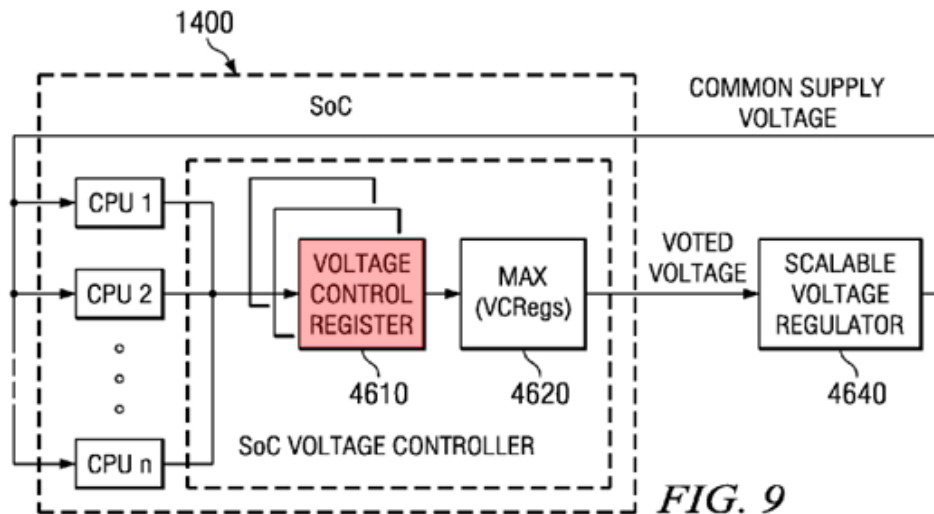


FIG. 9

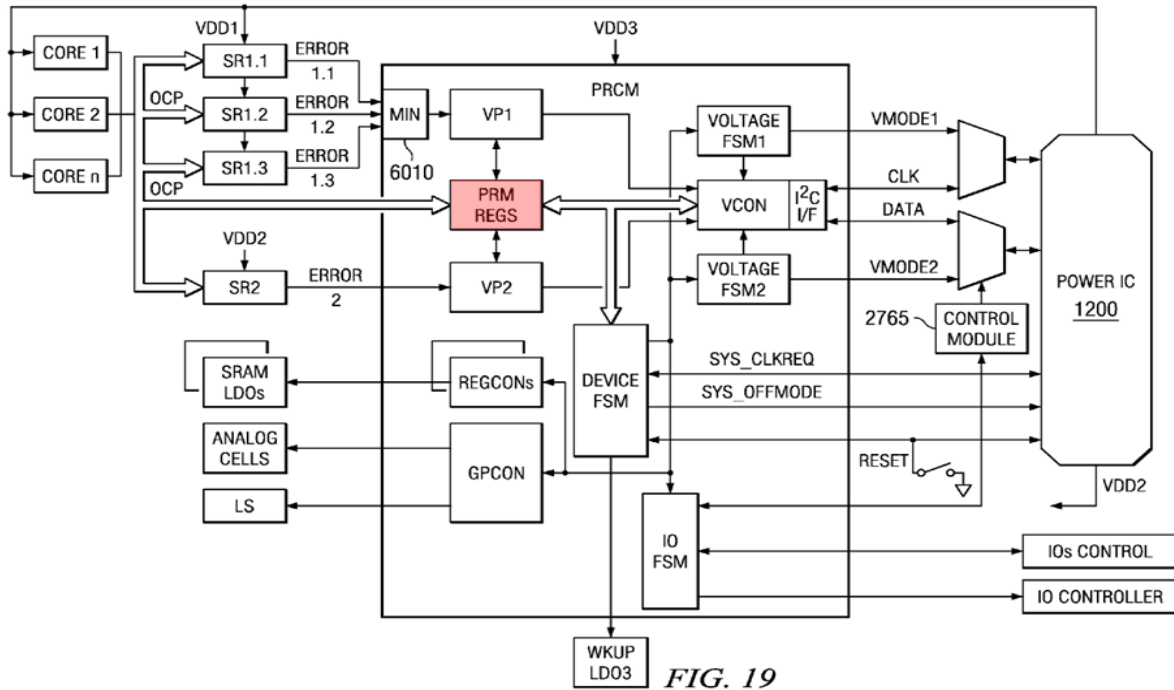


FIG. 19

These registers are part of the tuning circuit of Titiano. Ex-1002 ¶143. Thus, just as the '197 Patent states that tuning circuit 100 may “receive incoming EPB values from multiple cores of a multicore processor” (Ex-1005 4:59–60), the tuning circuit in Titiano receives a plurality of EPB values (requested voltages) from the cores. Ex-1002 ¶¶142–43.

In Titiano, arbitrating circuits select the maximum of the voltage requests as the voted voltage. Ex-1007 ¶136 (“The hardware voting mechanism 4520 selects the applicable one of the power management requirements or requests thus written[.]”); *id.* ¶¶137–38 (“the highest requested voltage”), *id.* ¶146 (“the highest requested voltage”); *id.* ¶150 (“the maximum of the values in the registers in the Voltage Control Registers block 4610”); *id.* ¶¶170, 199 (“voting circuit 5520

call[s] for the maximum or highest voltage requested by any processor in the voltage domain”). The arbitrating circuits⁹ are identified by green shading the figures below.

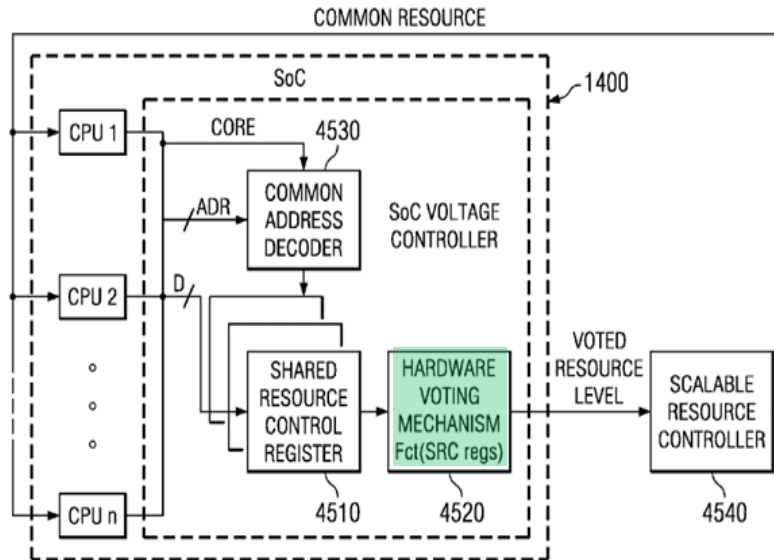


FIG. 8

⁹ The arbitrating circuit is hardware voting mechanism 4520 in Figure 8; hardware voting mechanism 4620 in Figures 9 and 10; hardware voting mechanism 5120 in Figure 13; and hardware voting circuit 5520 in Figure 15. Ex-1002 ¶144. In Figures 12 and 19, the arbitrating circuit for VDD1 is voltage FSM1. Ex-1007 ¶¶ 165, 175 (stating that Fig. 12 implements DVFS); *id.* ¶173 (stating that voltage FSM 1 manages VDD1); *id.* ¶220 (stating Fig. 19's structures are analogous to Fig. 12). Ex-1002 ¶144.

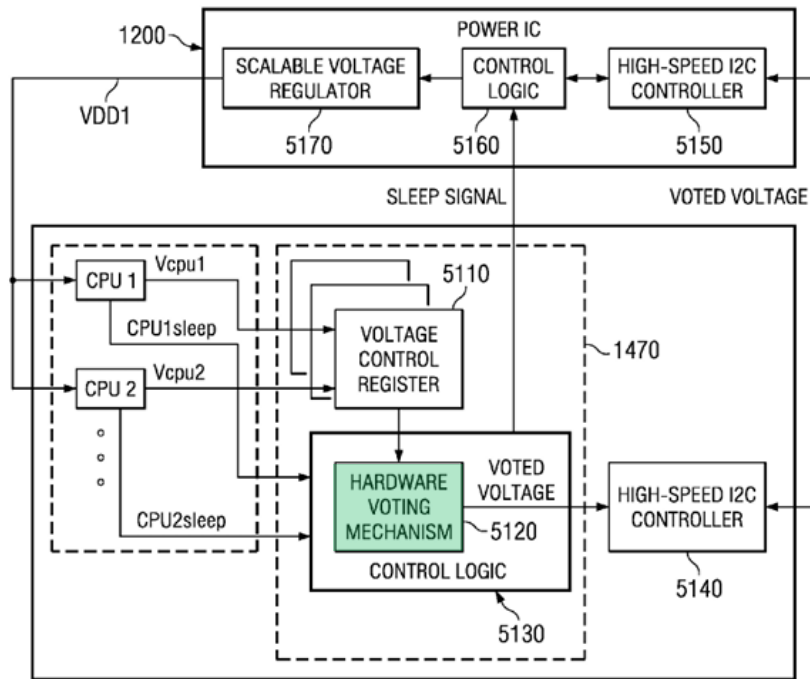
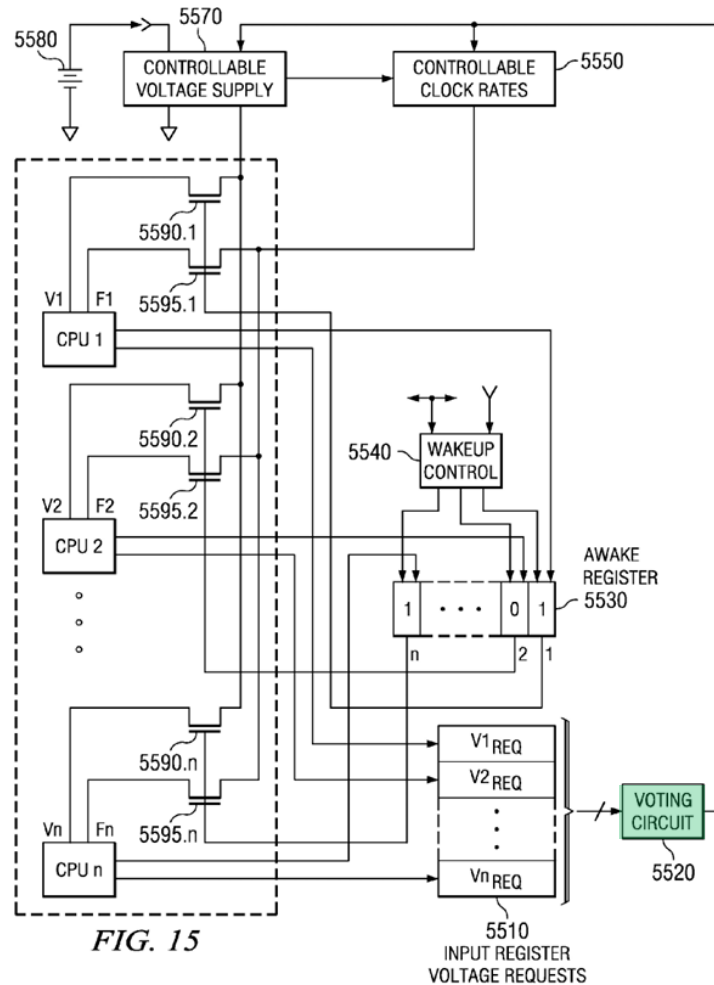


FIG. 13



These arbitrating circuits are part of the tuning circuit of Titiano. Ex-1002 ¶144.

Thus, the tuning circuit of Titiano determines a global EPB value (voted voltage) based on the plurality of EPB values (the voltage requests from the cores). *Id.*

According to the '197 Patent, energy performance bias (EPB) values represent a tradeoff between power and performance. Ex-1001, 2:34–38, 3:49–51, 4:58–64; Ex-1002 ¶145. In Titiano, the voltage requests and the highest voted voltage represent a tradeoff between power and performance and, thus, are EPB values. Ex-1007 ¶¶122; Ex-1002 ¶145.

The highest voted voltage selected by the arbitrating circuit is a “global” EPB value because, as described with reference to Element 1[e3], the tuning circuit of Titiano uses the voted voltage to update the global voltage setting for the shared domain of the cores. Ex-1005 ¶¶137, 146, 186; Ex-1002 ¶146.

Accordingly, Titiano discloses Element 1[e2]. Ex-1002 ¶¶142–47.

- iii. Element 1[e3]: a tuning circuit to ... update at least one setting of at least one of the plurality of power management features based on the workload configuration input and the global EPB value.**

Titiano teaches Element 1[e3]. Ex-1002 ¶148.

This Petition presents two alternative mappings based on the two alternative mappings (DPS and AVS) for workload configuration input (*see supra* Section VII.B.1.f.i), in combination with DVFS which discloses the global EPB value (*see supra* Section VII.B.1.f.ii). Titiano teaches that the power controllers may implement DVFS combined with either DPS or AVS. Ex-1007 ¶¶11, 106.

DPS and DVFS

Titiano teaches that DPS and DVFS may be combined to update a setting of a power management feature (VDD1 Common Supply Voltage) based on the workload configuration input (CPU1sleep or CPU2sleep signal) and the global EPB value (max voted voltage). Ex-1002 ¶149.

As shown in annotated Figure 13, control logic 5130 sends two control

signals—Sleep Signal and Voted Voltage—to the Power IC 1200.

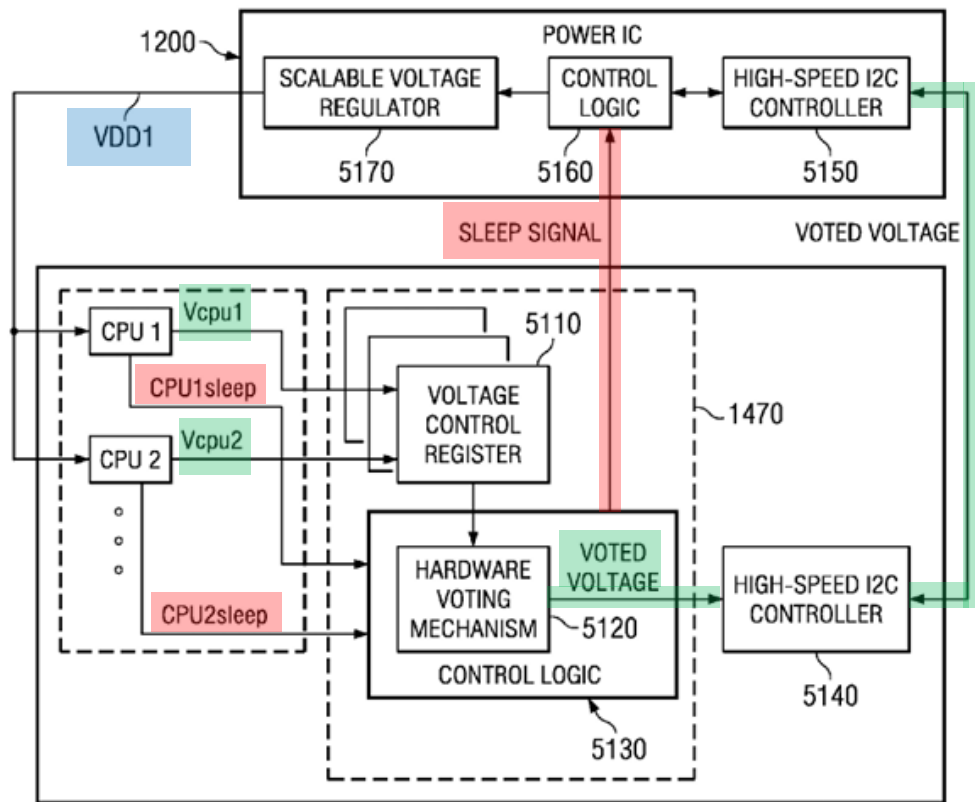


FIG. 13

Figure 14 illustrates the operation and timing of the signals in Figure 13. See *id.* ¶¶190–92.

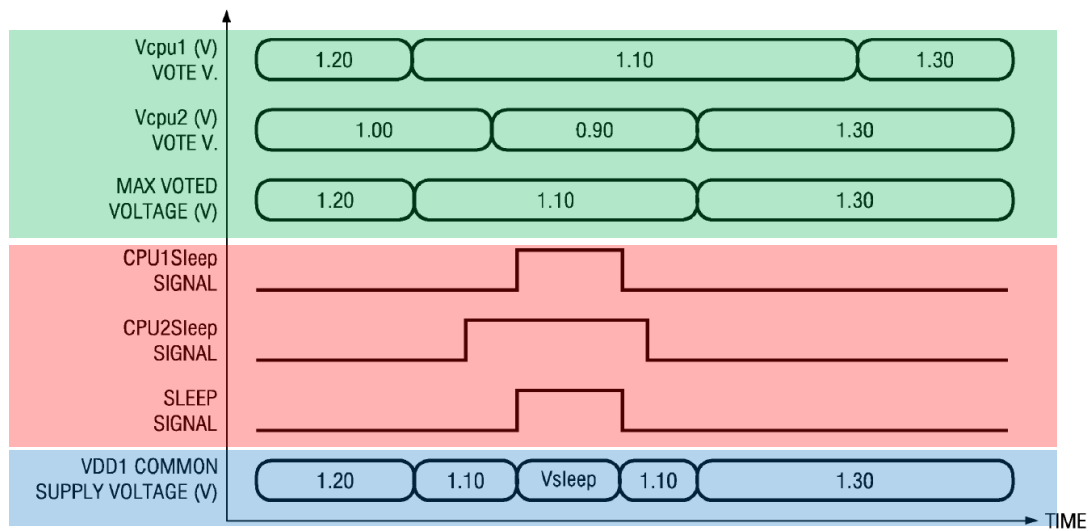


FIG. 14

As shown in the shaded green, the Max Voted Voltage is the maximum of the CPUs' voltage requests (Vcpu1 and Vcpu2). Ex-1007 ¶191; Ex-1002 ¶151. As shown in the shaded red, the Sleep Signal is the minimum function of the CPU1sleep and CPU2sleep signals (meaning that the Sleep Signal is high only when both individual sleep signals are high). Ex-1007 ¶¶190–191; Ex-1002 ¶151. As shown in the shaded blue, the VDD1 Common Supply Voltage is Vsleep when the Sleep Signal is high and otherwise is the Max Voted Voltage. Ex-1007 ¶192.

VDD1 is the claimed “at least one setting of at least one of the plurality of power management features,” as recited in Claim 1. Ex-1002 ¶152. VDD1 is based on CPU1sleep and CPU2sleep signals (the workload configuration input) and the Max Voted Voltage (the global EPB value). Ex-1002 ¶152. If CPU1sleep and CPU2sleep signals are both high (indicating the cores have no active workload), VDD1 is set to Vsleep. Ex-1007 ¶192; Ex-1002 ¶152. Otherwise, VDD1 is set to

the Max Voted Voltage. Ex-1007 ¶191; Ex-1002 ¶152. Thus, the tuning circuit of Titiano (which includes control logic 5130) updates at least one setting (VDD1) of at least one of the plurality of power management features based on the workload configuration input (CPU1sleep and CPU2sleep signals) and the global EPB value (Max Voted Voltage). Ex-1002 ¶152.

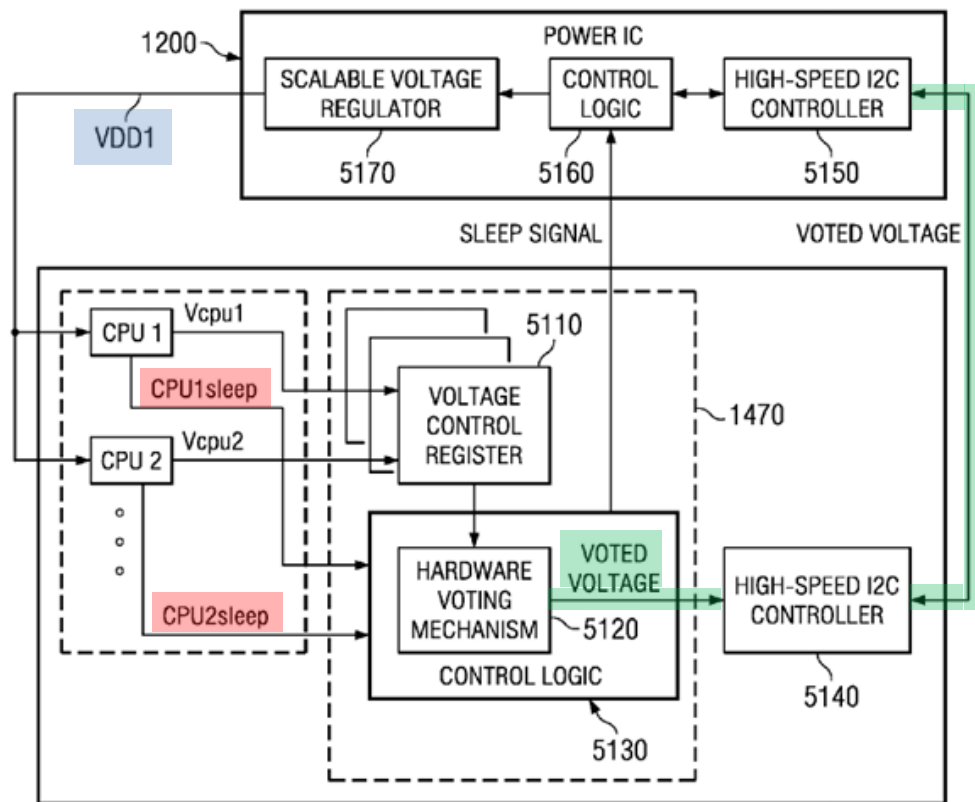
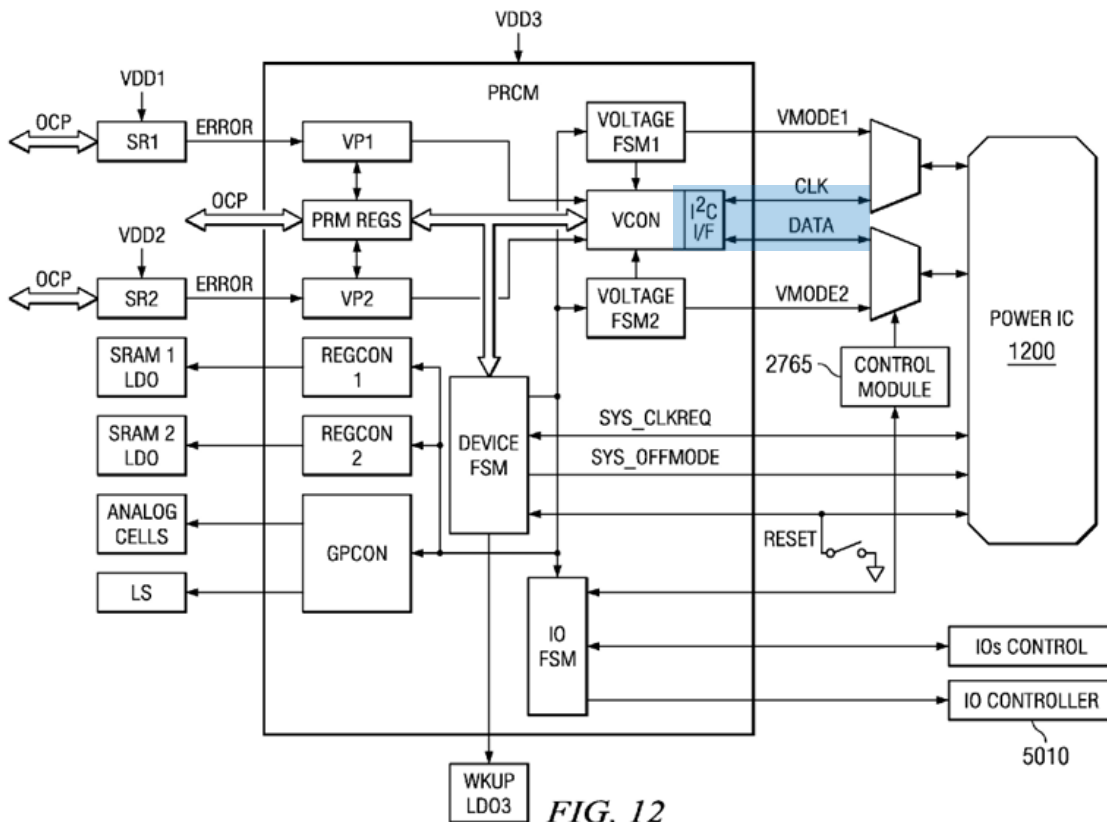


FIG. 13

Claim 1 does not preclude the tuning circuit from using another component (such as Power IC 1200) to effectuate the claimed update. *Id.* ¶153. As indicated by its name, **control** logic 5130 controls Power IC 1200 and thus is the component responsible for updating the setting VDD1. *Id.* Power IC 1200 does not exercise

any independent control over the value of VDD1; it merely responds to instructions from control logic 5130 to set the value of VDD1. *Id.*

To the extent that Claim 1 is read to require control logic 5130 to effectuate the claimed update, Figure 12 of Titiano implements the same functionality as described in Figure 13 but uses a single control interface (the “I2C interface”) to control Power IC 1200, as illustrated below. Ex-1007 ¶154; Ex-1002 ¶154.



In Figure 12, the tuning circuit includes PRM control registers, voltage processors VP1, voltage FSM 1, and voltage controller VCON. Ex-1007 ¶¶173, 178; Ex-1002 ¶154. This tuning circuit implements the same DPS and DVFS

functions described above: the voltage controller VCON sets the output voltage of Power IC 1200 based on whether the cores are active or inactive according to DPS and, if active, the voltage level according to DVFS (i.e., the voting mechanism).¹⁰ *Id.* ¶154. In I2C mode, the voltage controller VCON communicates the voltage setting to Power IC 1200 as Data over the I2C interface, and this communicated voltage setting is “at least one setting of at least one of the plurality of power management features based on the workload configuration input and the global EPB value,” as recited in Claim 1. *Id.* ¶154.

AVS and DVFS

Alternatively, Titiano’s combination of AVS and DVFS teach Element 1[e3]. Titiano teaches that AVS and DVFS may be combined to update a setting of a power management feature (e.g., VDD1 Command in Figure 10) based on the workload configuration input (e.g., VDD1 Error in Figure 10) and the global EPB value (e.g., Voted Voltage in Figure 10). Ex-1002 ¶155; Ex-1007 ¶11. In Figure 10, the tuning circuit corresponds to the voltage control register 4610, hardware

¹⁰ Titiano states that “[t]he VCON receives a voltage level from the voltage processor and also a command from the voltage state machine FSM of FIG. 12. In active mode, the VCON formats the voltage level and command and sends them over the I2C interface to control the external [Switch Mode Power Supply] SMPS.” Ex-1007 ¶154. Conversely, “[w]hen the device is in standby mode, the voltage controller VCON is then driven by the voltage state machines FSMs to allow the external supply to enter low power mode.” *Id.*

voting mechanism 4620, and voltage processor VP1. Ex-1002 ¶155.

Figure 10 illustrates the same voltage voting process described in connection with Figure 13. *Id.* ¶156. Figure 10 also illustrates sensor modules SR1 and SR2 used to implement AVS in the respective voltage domains of Voltage Processors VP1 and VP2. Ex-1007 ¶158.

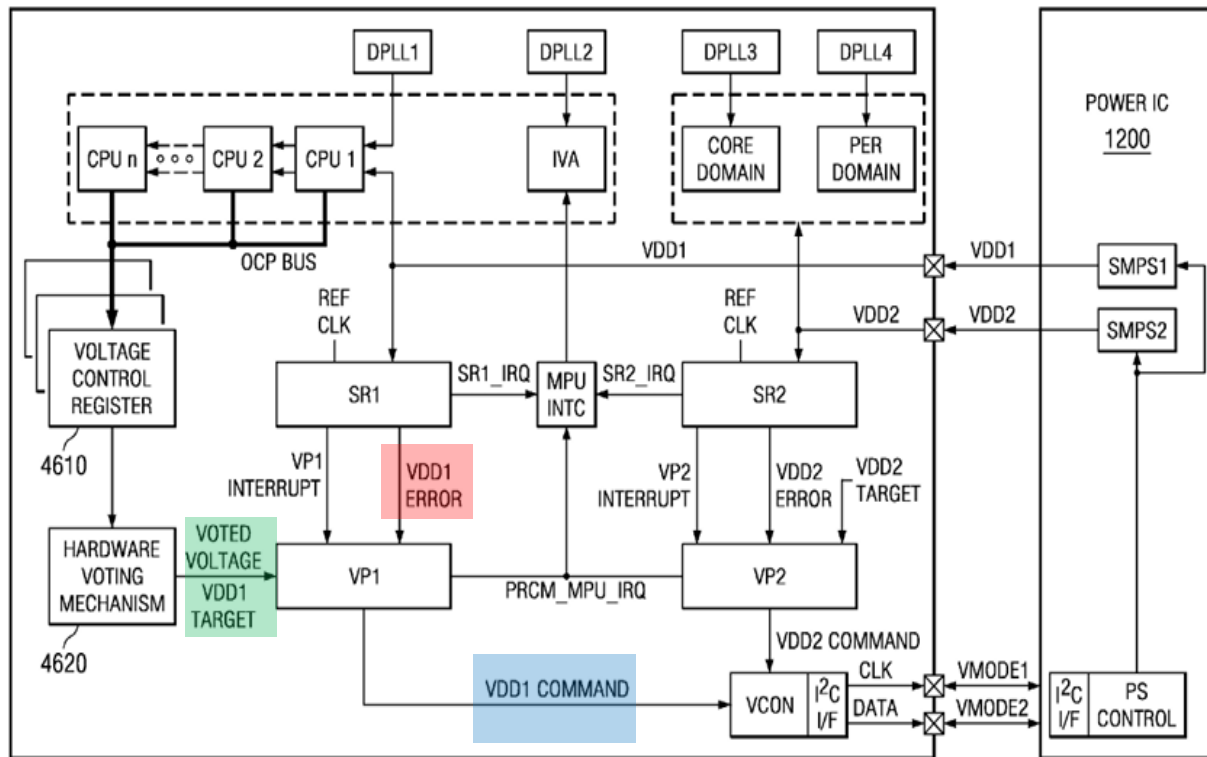


FIG. 10

SR1, for example, generates a VDD1 error and sends it to Voltage Processor VP1, which then uses the VDD1 error to “determine[] the appropriate voltage level to program into the power supply.” *Id.* ¶135; *see also id.* ¶155. Voltage Processor VP1 receives the “error value from the AVS sensor module SR, and automatically adjusts the power supply by sending a voltage command [VDD1 Command] to the

Voltage Controller.” *Id.* ¶135; Ex-1002 ¶156. Thus, Voltage Processor VP1 updates a setting (VDD1 Command) based on the workload configuration input (VDD1 Error) and the global EPB value (voted voltage). *Id.* ¶¶156–57.

2. Dependent Claims 2–6 and 19–20

- a. **Claim 2: The processor of claim 1, wherein the power controller is to access a power-performance tuning table based on the workload configuration input and the global EPB value, and use information from the power-performance tuning table to update the at least one setting.**

Titiano teaches dependent Claim 2. Ex-1002 ¶158.

As described above, this Petition presents two alternative mappings (DPS and AVS) for the “workload configuration input.” *See supra* Section VII.B.1.f. These mappings both render obvious Claim 2.

DPS and DVFS

Titiano discloses “a lookup table of OPP voltage-frequency pairs (V,F).” Ex-1007 ¶201. This lookup table corresponds to the “power-performance tuning table” of Claim 2. Ex-1002 ¶159.

Titiano teaches that the lookup table is indexed by a voltage to find a corresponding frequency. Ex-1007 ¶201; Ex-1002 ¶¶159–161. It would have been obvious to index the table by the voltage VDD1, which is based on the workload configuration input (CPU1sleep and CPU2sleep signals) and the global EPB value (the max voted voltage). *See supra* Section VIII.B.1.f.iii; Ex-1002 ¶¶160–61. Thus,

Titiano teaches accessing the lookup table based on the workload configuration input and the global EPB value. Ex-1002 ¶¶159–162.

It would have been obvious to use the information from the table to update a power management setting (the frequency associated with VDD1). Ex-1007 ¶109; Ex-1002 ¶¶161–62. Accordingly, Titiano’s implementation of DPS and DVFS teaches Claim 2. Ex-1002 ¶¶158–62.

AVS and DVFS

To implement AVS, Titiano describes that “[e]ach of the Voltage Processors contain Look-Up Tables and [are] correctly initialized and configured to optimize the voltage control.” Ex-1007 ¶159. This look-up table corresponds to the “power-performance tuning table” of Claim 2. Ex-1002 ¶163.

As explained above for Element 1[e3], Voltage Processor VP1 in Figure 10 generates VDD1 Command based on those two variables, VDD1 Error (workload configuration input) and the voted voltage (global EPB value). *See supra* Section VII.B.1.f.iii.

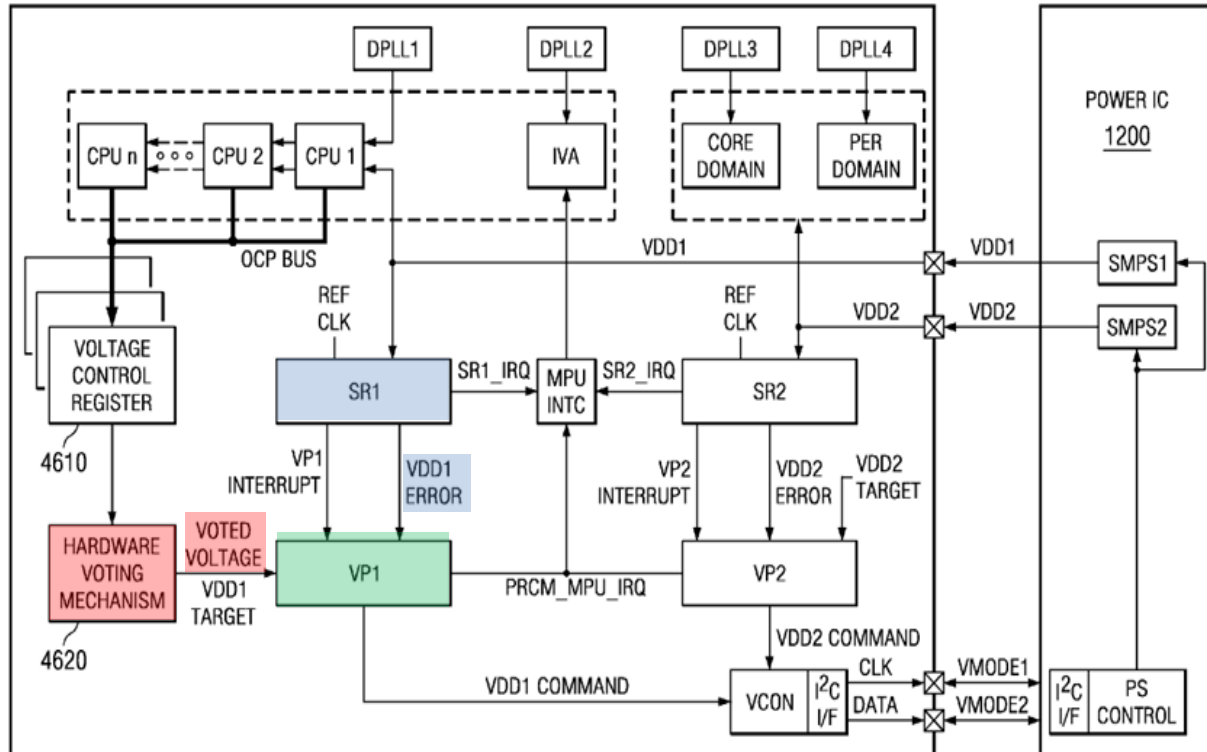


FIG. 10

It would have been obvious to a POSITA that Voltage Processor 1 indexes the lookup table in Titiano by those two variables to retrieve the VDD1 Command. Ex-1002 ¶¶163–65. A POSITA would have been motivated to implement the lookup table as such a two-dimensional table because a two-dimensional table is a well-known, fast, and efficient way to retrieve a result that is a function of two variables. *Id.* ¶¶59–64, 165. In such an implementation, the power controller

(which includes Voltage Processors VP1) would access the lookup table based on workload configuration input (VDD1 Error) and the global EPB (voted voltage) and use the information from the table to update at least one power management setting (VDD1 Command). *Id.*

Accordingly, Titiano's implementation of AVS and DVFS teaches Claim 2. *Id.* ¶¶163–66.

- b. Claim 3: The processor of claim 2, wherein the tuning circuit is to update the at least one setting of the at least one power management feature responsive to the global EPB value.**

Titiano teaches dependent Claim 3 because Claim 3 is encompassed by the limitations of Claims 1 and 2. Ex-1002 ¶167; *see supra* Section VII.B.1–2.

- c. Claim 4: The processor of claim 3, wherein the tuning circuit includes a sampler to receive the plurality of EPB values from at least some of the plurality of cores and a combiner to generate the global EPB value from the EPB value from the plurality of cores.**

Titiano teaches dependent Claim 4. Ex-1002 ¶¶168–171.

As explained above for Element 1[e2], the tuning circuit in Titiano includes registers which receive the plurality of EPB values from the plurality of cores. *See supra* Section VII.B.1.f.ii. These registers correspond to the claimed “sampler.” Ex-1002 ¶168.

Also, as explained above for Element 1[e2], the tuning circuit in Titiano includes an arbitrating circuit that generates the global EPB (maximum voted

voltage) from the EPB values from the cores. This arbitrating circuit is the claimed “combiner.” *See supra* Section VII.B.1.f.ii.

Thus, the tuning circuit in Titiano includes a sampler (registers) to receive the plurality of EPB values (voltage requests) from at least some of the plurality of cores and a combiner (arbitrating circuit) to generate the global EPB value (maximum voted voltage) from the EPB value from the plurality of cores. Ex-1002 ¶170. Accordingly, Titiano teaches dependent Claim 4. Ex-1002 ¶¶168–71.

d. Claim 5: The processor of claim 4, wherein the sampler is to receive the EPB value from a plurality of threads to execute on the at least some of the plurality of cores.

Titiano teaches dependent Claim 5. Ex-1002 ¶¶172–74.

As explained above for Claim 4, Titiano teaches a sampler (registers) that receives EPB values from the plurality of cores. *See supra* Section VII.B.2.c. Claim 5 adds only that the EPB values are “from a plurality of threads” on the cores. Ex-1002 ¶172. A POSITA would have understood that the term “thread” refers to the software thread running on the core. *Id.* This understanding is consistent with the specification of the ’197 Patent, which describes “logical threads.” *See* Ex-1001, 4:18–25. Titiano describes “symmetric multiprocessing (SMP) core(s) for use in the systems of FIGS. 1-19.” Ex-1007 ¶221. The plurality of SMP cores in Titiano would include multiple threads. Ex-1002 ¶172. Thus, the

sampler in Titiano receives the EPB values “from a plurality of threads to execute on the at least some of the plurality of cores.” *Id.* ¶172.

Alternatively, it would have been obvious to a POSITA that the SMP cores in Titiano could include a plurality of threads and thus that the sampler in Titiano receives the EPB values “from a plurality of threads to execute on the at least some of the plurality of cores.” *Id.* ¶173.

Accordingly, Titiano teaches dependent Claim 5. *Id.* ¶¶172–74.

- e. **Claim 6: The processor of claim 4, wherein the power controller is to generate a bin value from the global EPB value and to access the power-performance tuning table using the bin value.**

Titiano teaches dependent Claim 6. Ex-1002 ¶175.

According to Titiano, Operating Performance Points (OPPs) (Opp1, Opp2, etc.) are associated with different voltage and frequency pairs. Ex-1007 ¶109.

Thus, Titiano teaches generating a bin value (OPP number) from the global EPB value (max voted voltage). Ex-1002 ¶175. It would have been obvious to a POSITA that the power-performance tuning table could be accessed by the global EPB value (max voted voltage) or the bin value (OPP number). *Id.* ¶¶59–64, 175.

Accordingly, Titiano teaches dependent Claim 6. *Id.* ¶¶175–76.

- f. Claim 19: The processor of claim 1, wherein the power controller is to enable a first power management feature based on the updated at least one setting.**

Titiano discloses dependent Claim 19. Ex-1002 ¶177.

As described above with respect to Element 1[e3], the tuning circuit in Titiano “updat[es] at least one setting of at least one of the plurality of power management features.” *See supra* Section VII.B.1.f.iii. The updated setting relates to VDD1 supply voltage. *Id.* As explained above, by updating VDD1 supply voltage, the power controller in Titiano enables a power management feature called Dynamic Voltage Frequency Scaling (DVFS), which scales the supply voltage to the lowest voltage to deliver various operation modes and frequencies according to predicted needs. Ex-1007 ¶¶107, 109, 111, 112, 122, 126; Ex-1002 ¶177.

Accordingly, Titiano teaches dependent Claim 19. Ex-1002 ¶¶177–78.

- g. Claim 20: The processor of claim 1, wherein the power controller is to send an update message to a destination agent of the processor to cause the destination agent to control a first power management feature based on the updated at least one setting.**

Titiano teaches dependent Claim 20. Ex-1002 ¶¶179–183.

As explained above for Claim 19, the power controller in Titiano enables a first power management feature (DVFS) based on the updated at least one setting (VDD supply voltage). *See supra* Section VII.B.2.f. Claim 20 is similar to Claim

19 but further adds the use of a “destination agent.”

Titiano discloses the use of a destination agent, such as scalable resource controller 4540 in Figure 8, scalable voltage regulator 4640 in Figure 9, and Power IC 1200 in Figures 10, 12, 13, and 19. *Id.* ¶181.

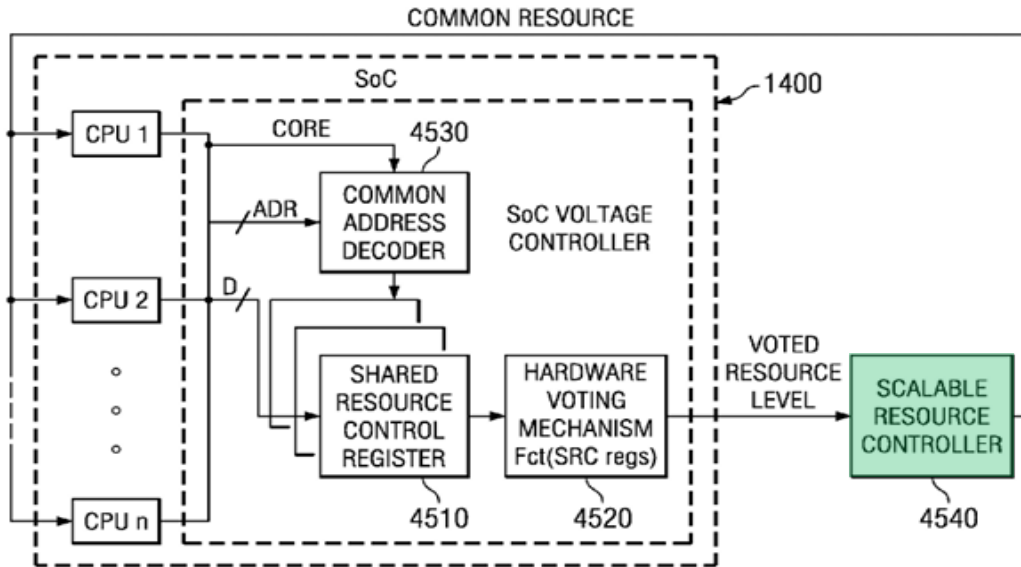


FIG. 8

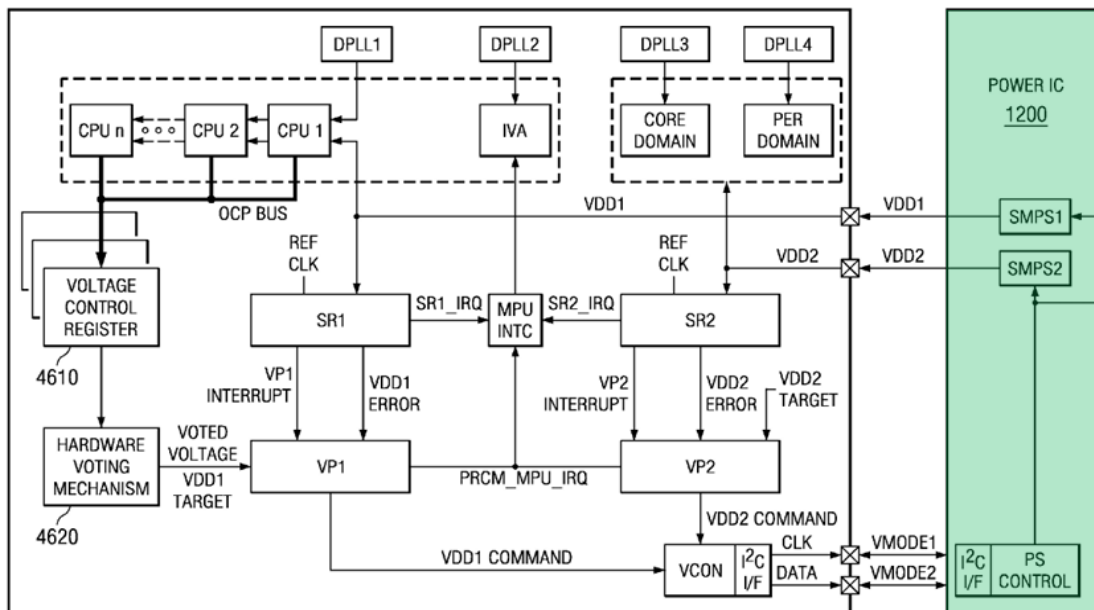


FIG. 10

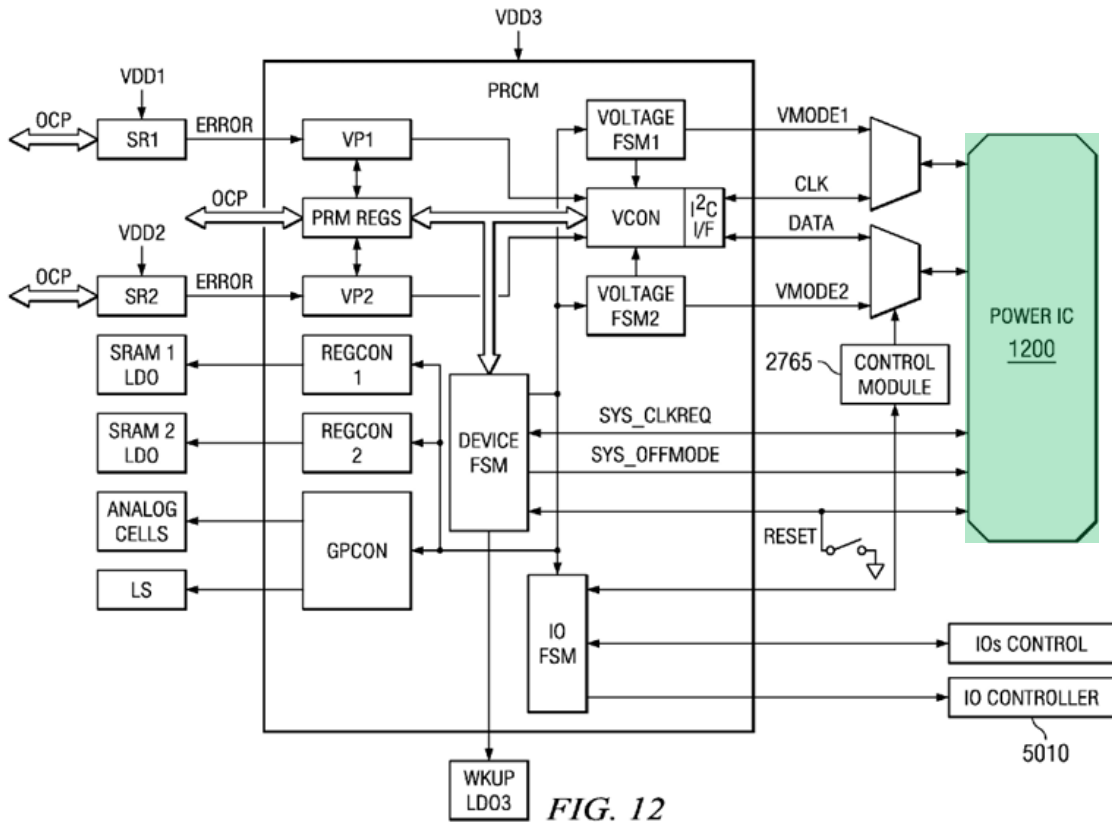


FIG. 12

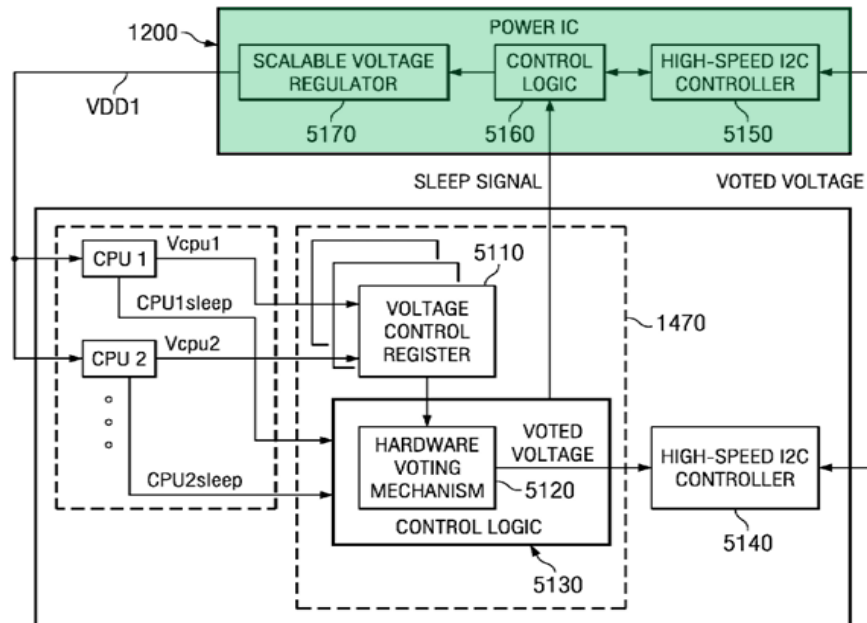
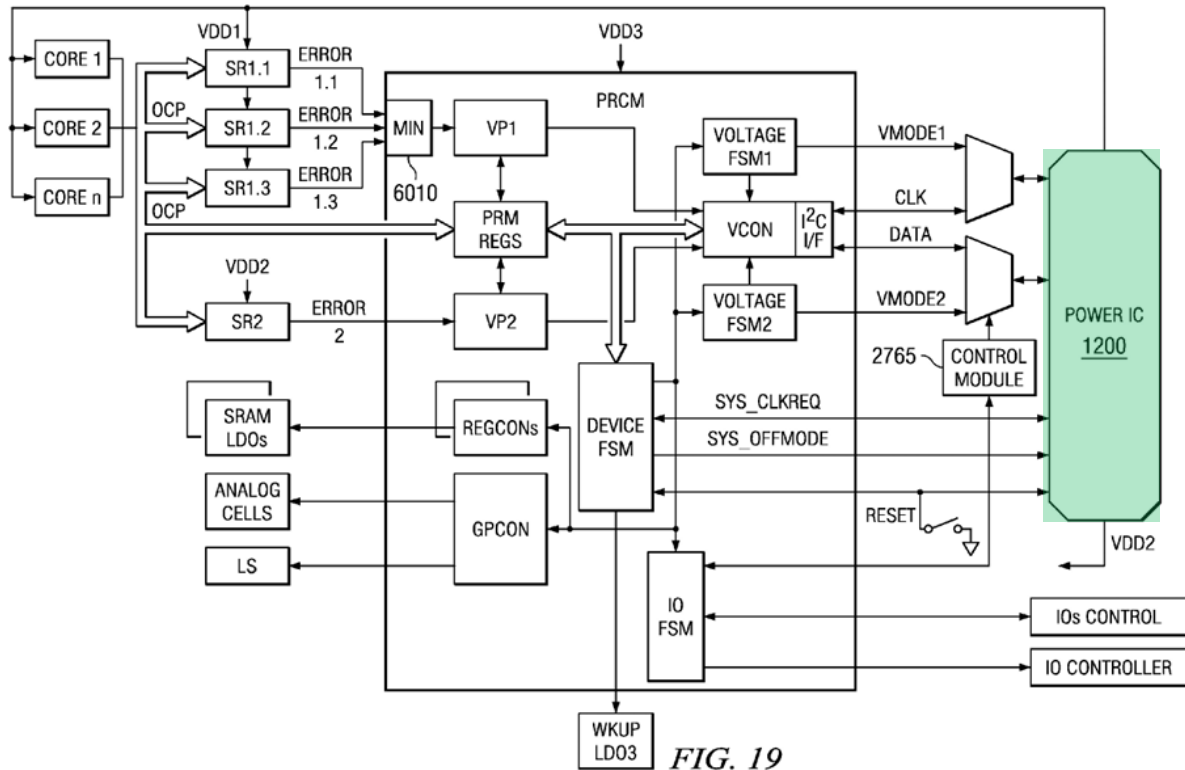


FIG. 13



The power controller in Titano sends an update message to these destination agents to control a power management feature (DVFS) based on the updated VDD voltage setting. Ex-1007 ¶¶136, 138, 155; Ex-1002 ¶182. As explained above for Element 1[e3], the power controller in Figures 10 and 12 of Titano communicates the voltage setting to Power IC 1200 as Data over the I2C interface. *See supra* Section VII.B.1.f.iii.

Accordingly, Titano teaches dependent Claim 20. Ex-1002 ¶¶179–183.

3. Independent Claim 11

- a. **Element 11[pre]: A non-transitory machine-readable medium having stored thereon instructions, which if performed by a machine cause the machine to perform a method comprising:**

To the extent that the preamble of Claim 11 is limiting, Titiano discloses the preamble. Ex-1002 ¶184. Titiano states that its power management process may be implemented by hardware, software, or firmware. Ex-1007 ¶258; *see also id.* ¶¶115 (“DVFS hardware and software”), 116 (“DVFS software”), 119 (“power management software”); 211.

- b. **Element 11[a]: receiving an energy performance bias (EPB) value in a tuning circuit of a power control logic of a processor from a plurality of threads executing on the processor and determining a global EPB value based at least in part on the EPB value received from the plurality of threads, the EPB value to indicate a preference of a user for a tradeoff between power optimization and performance optimization;**

Titiano teaches Element 11[a]. Ex-1002 ¶185.

As described above with reference to Element 1[e2], Titiano teaches a power controller (which is the same as “power control logic”) that receives EPB values and determines a global EPB based on the EPB values, and the EPB values indicate a tradeoff between power optimization and performance optimization. *See supra* Section VII.B.1.f.ii; Ex-1002 ¶185.

Element 11[a] adds only that the EPB value “indicate[s] a preference of a

user” for the power-performance tradeoff. Ex-1002 ¶186. Titiano also teaches this further limitation. *Id.* The voted voltages in Titiano are programmed into the voltage control registers via software operating on the CPU cores. *Id.*; Ex-1007 ¶119. Titiano suggests that a user may also control the software to effectuate the programming of the voted voltages in the voltage control registers. *See* Ex-1007 ¶135 (“When performing DVFS, the user can program a new operating point in the sensor module by programming the new frequency target and caus[ing] the sensor module to re-calculate the error.”); *see also* ¶¶105, 158, 175–76; Ex-1002 ¶186. Thus, it would have been obvious to enable a user to control the software in Titiano to determine an EPB value indicating the user’s preference for a tradeoff between power and performance optimization. *Id.* ¶186.

- c. Elements 11[b]: accessing a table based on the global EPB value; and
Element 11[c]: updating at least one setting of a power management feature controlled by the power control logic based on information obtained from the table.**

Elements 11[b] and 11[c] are the same subject matter as recited in Claim 2. Ex-1002 ¶187. Thus, Titiano teaches Elements 11[b] and 11[c] for the same reasons described above for Claim 2. *See supra* Section VII.B.2.a.

4. Dependent Claim 13: The non-transitory machine-readable medium of claim 11, wherein the method further comprises providing an interface to enable a user, an operating system or a baseboard management controller to set the EPB value, and controlling a plurality of power management features via input of the EPB value.

Titiano teaches Claim 13. Ex-1002 ¶188. Titiano describes that “[w]hen performing DVFS, the user can program a new operating point in the sensor module by programming the new frequency target and caus[ing] the sensor module to re-calculate the error.” Ex-1007 ¶135. Titiano also refers to the sensor module as an “interface.” *Id.* ¶153 (“The error is output on *SR interface* and is related to the actual voltage step that needs to be applied.”) (emphasis added). Thus, Titiano teaches “controlling a plurality of power management features via input of the EPB value.” Ex-1002 ¶188. As explained above for Claim 1, Titiano teaches “a power controller to control a plurality of power management features of the processor” using EPB values. *Supra* Sections VII.B.1.e and VII.B.1.f. Thus, Titiano teaches “providing an interface to enable a user, an operating system or a baseboard management controller to set the EPB value, and controlling a plurality of power management features via input of the EPB value.” Ex-1002 ¶¶188–189.

C. Ground 4: Claims 2, and 15–18 Are Obvious Over Titiano in View of Hansquine

1. A POSITA would have been motivated to combine Titiano and Hansquine

In addition to the reasons set out below, a POSITA would have been motivated to combine Titiano and Hansquine’s teachings and would have had a reasonable expectation of success in doing so, because they are from the same field of endeavor and relate to the same well-known technologies. Ex-1002 ¶190.

Titiano and Hansquine provide complementary solutions for power management of multi-core processors using a power management feature known as Adaptive Voltage Scaling (AVS). Ex-1007 ¶¶125, 134–35, 160; Ex-1008 ¶¶ 3, 11, 37; Ex-1002 ¶190.

Titiano teaches that AVS may be used to generate “an error output that indicates whether to raise or lower the voltage.” Ex-1007 ¶153. This error output indicates “the temperature induced current performance of the device.” *Id.* ¶134. Titiano further describes that “[e]ach of the Voltage Processors contain Look-Up Tables and [are] correctly initialized and configured to optimize the voltage control.” Ex-1007 ¶159.

Hansquine teaches to implement an AVS look-up table as a two-dimensional table. Ex-1008 ¶29.

It would have been obvious to a POSITA to implement the AVS look-up

table in Titiano as a two-dimensional table as taught in Hansquine. Ex-1002 ¶¶59–64, 190–92. A POSITA would have had a reasonable expectation of success in combining the teachings of Titiano and Hansquine because each purports to implement AVS in similar and predictable ways (using a lookup table). *Id.*

2. Dependent Claim 2

Titiano in view of Hansquine teaches dependent Claim 2. Ex-1002 ¶193.

As described above for Ground 3, it would have been obvious to implement the AVS lookup table in Titiano as a two-dimensional table. *See supra* Section VII.B.2.a. Hansquine provides further support for implementing an AVS lookup table as two-dimensional table, as shown in Figure 13.

AVS Frequency/Voltage Level Table (140)

142

	T (°C)		f ₁	f ₂	...	f _N
B ₁ →	80	60	1.2V	1.18V	...	
B ₂ →	60	40	1.1V	1.08V	...	
B ₃ →	40	20	1.0V	.99V	...	
B ₄ →	20	0	⋮	⋮	...	⋮
B _N →	⋮	⋮	.95V	.94V	...	

144

$f_1 > f_2 > f_N$

FIG. 13

Thus, based on the Titiano-Hansquine combination, it would have been obvious to implement the AVS lookup table in Titiano as a two-dimensional table. Ex-1002 ¶193.

A POSITA would have been motivated to combine the teachings of Titiano and Hansquine because Hansquine provides additional implementation details consistent with the teachings of Titiano. *Id.* ¶194. Both references use Adaptive Voltage Scaling techniques to optimize power consumption in a multi-core processor. Ex-1007 ¶111; Ex-1008 ¶3; Ex-1002 ¶¶190–92, 194. Both references also describe the use of a lookup table to implement AVS. Ex-1007 ¶159; Ex-1008 ¶74.

In view of Hansquine’s two-dimensional AVS lookup table, it would have been obvious to a POSITA to implement the AVS lookup table in Titiano as a two-dimensional table. *Id.* ¶¶190–92, 194. In such an implementation, the power controller (which includes Voltage Processors VP1) would access the lookup table based on workload configuration input (VDD1 Error) and the global EPB value (voted voltage) and use the information from the table to update at least one power management setting (VDD1 Command). *Id.* ¶¶190–92, 194–96.

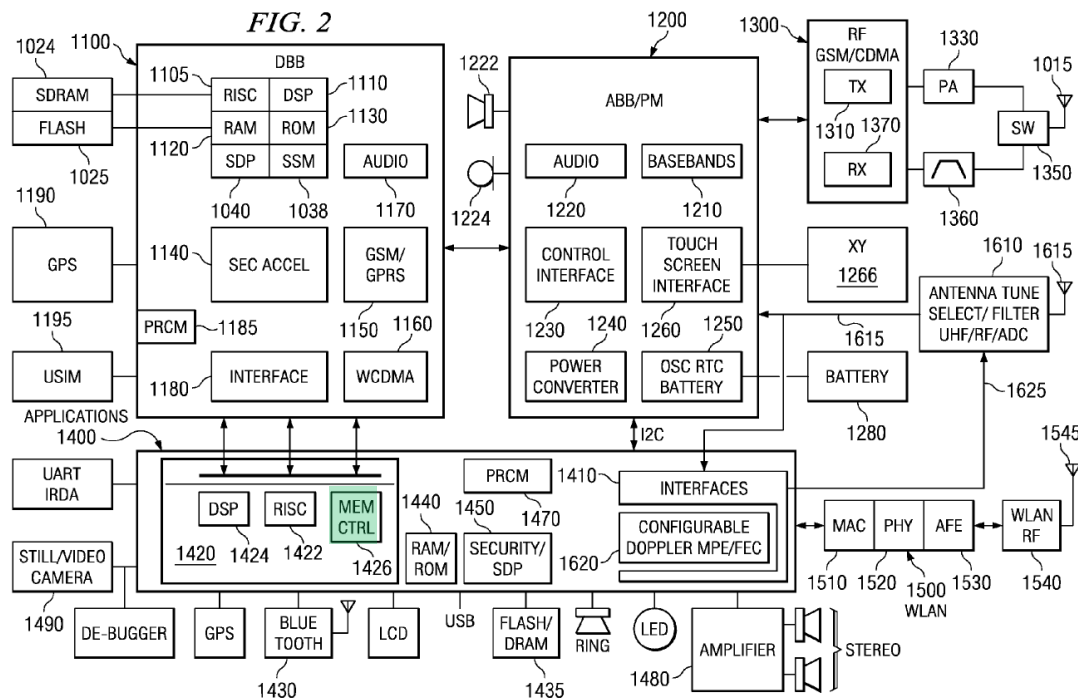
Accordingly, the Titiano-Hansquine combination renders obvious Claim 2. Ex-1002 ¶¶193–96.

3. Independent Claim 15

- a. Element 15[a]: a multicore processor including a plurality of cores, at least one cache memory and a memory controller;**

Titiano discloses Element 15[a]. Ex-1002 ¶197.

As explained above for Elements 1[pre], 1[a], and 1[b], Titiano discloses “a multicore processor including a plurality of cores” and “at least one cache memory.” *See supra* Section VII.B.1.a–c. Claim 15 adds only “a memory controller.” Ex-1002 ¶197. As shown below in Figure 2, the processor in Titiano includes a memory controller 1426. Ex-1007, ¶¶52, 64; Ex-1002 ¶197.



Accordingly, Titiano discloses Element 15[a]. *Id.* ¶¶197–98.

- b. Element 15[b]: wherein the tuning circuit is to access an entry of a tuning table based at least in part on the EPB value and a workload configuration value and update a setting for a power management feature responsive to a value stored in a field of the entry;**

Element 15[b] is the same as Claim 2, except Element 15[b] refers to “a value stored in a field of the entry” in contrast to Claim 2’s reference to “information” from the tuning table.¹¹ Ex-1002 ¶199. Because Titiano and Hansquine disclose a tuning table with values (i.e., voltage-frequency pairs,) the Titiano-Hansquine combination renders Element 15[b] obvious for the same reasons described above for Claim 2. *See supra* Section VII.C.2; Ex-1002 ¶199.

- c. Element 15[c]: wherein the workload configuration value is to indicate a predominant workload type to be executed on the system, the tuning table including a first set of entries associated with a first workload type and a second set of entries associated with a second workload type;**

The Titiano-Hansquine combination teaches Element 15[c]. Ex-1002 ¶200.

As explained above with reference to Element 1[e1], the VDD1 Error signal in Titiano indicates “the temperature induced current performance of the device” (Ex-1007 ¶134) and thus is a workload configuration input (or value). *See supra* Section VII.B.1.f.i; Ex-1002 ¶200. The workload configuration value indicates a

¹¹ Although Claim 15 refers to workload configuration “value” and Claim 2 refers workload configuration “input,” these terms do not appear to have different meanings. Ex-1002 ¶199. In any case, the workload configuration input in Titiano is a value. *See supra* Section VII.B.1.f.i.

predominant workload type. Ex-1002 ¶200. If the workload type is processor-intensive, a higher “temperature induced current performance of the device” results in a corresponding value for the VDD1 Error signal. *Id.* If the workload is less processor-intensive, a lower “temperature induced current performance of the device” results in a corresponding value for the VDD1 Error signal. *Id.* Thus, the workload configuration value indicates “a predominant workload type” (processor-intensive vs. less processor-intensive). *Id.*

As explained above for Claim 2, the Titiano-Hansquine combination teaches that the AVS table in Titiano could be implemented as a two-dimensional table, which is indexed by a workload configuration value (VDD1 Error signal). *See supra* Section VII.C.2. In such an embodiment, the table would include a first set of entries indexed by a high VDD1 Error signal, such that a different entries would be utilized depending on the value of the VDD1 Error signal. Thus, for at least two values of the VDD1 Error signal, a first set of entries would be associated with a first workload type (processor-intensive workloads), and a second set of entries which would be associated with a second workload type (less processor-intensive workloads). Ex-1002 ¶201.

d. Element 15[d]: a system memory coupled to the multicore processor via a memory interconnect.

Titiano discloses Element 15[d]. Ex-1002 ¶202.

Titiano states, “[o]n chip 1400, the shared memory controller 1426 in circuitry 1420 interfaces the RISC processor 1420 and the DSP 1424 via an on-chip bus to on-chip memory 1440 with RAM and ROM.” Ex-1007 ¶64. Thus, Titiano describes a system memory (chip memory 1440) coupled to the multicore processor (RISC processor 1420 and the DSP 1424) via a memory interconnect (the on-chip bus). Ex-1002 ¶202.

- 4. Dependent Claim 16: The system of claim 15, wherein the tuning circuit is to update at least one setting of a first power management feature controlled by a power control logic of the multicore processor, the at least one setting obtained from a field of an entry of the tuning table associated with a bin in which the EPB value is included.**

Titiano teaches dependent Claim 16. Ex-1002 ¶203.

As explained above with respect to Claim 1, Titiano teaches a “power controller includ[ing] a tuning circuit ... to update at least one setting of at least one of the plurality of power management features.” *See supra* Section VII.B.1.f. Titiano further teaches that the power controller (e.g., Power Management Control Module (PCRM)) includes Control Logic. *See, e.g.*, Ex-1007 ¶¶185–188, Fig. 13. Thus, a POSITA would have understood that the “at least one setting of a first power management feature” is “controlled by a power control logic of the multicore processor,” as recited in Claim 16. Ex-1002 ¶203.

In addition, as explained with respect to Claim 6, Titiano teaches that the “power controller is to generate a bin value from the global EPB value and to

access the power-performance tuning table using the bin value.” *See supra* Section VII.B.2.e. Thus, Titiano also teaches that “the at least one setting [is] obtained from a field of an entry of the tuning table associated with a bin in which the EPB value is included,” as recited in Claim 16. Ex-1002 ¶204.

5. Dependent Claim 17: The system of claim 16, wherein multicore processor comprises the tuning circuit.

Titiano teaches dependent Claim 17. Ex-1002 ¶205.

Titiano teaches that the CPU cores and the tuning circuit (e.g., the shared resource control register and hardware voting mechanism) are located on the same processor. *See, e.g.*, Ex-1007 ¶137; Figs. 8–9; *supra* Section VII.B.1. Thus, the multicore processor comprises the tuning circuit, as recited in Claim 17. Ex-1002 ¶205.

6. Dependent Claim 18: The system of claim 15, wherein the multicore processor comprises a power control logic, the power control logic comprising the tuning circuit, wherein the tuning circuit is to generate a bin value from the EPB value and access the tuning table using the bin value.

Titiano teaches dependent Claim 18. Ex-1002 ¶¶206–207.

The claimed “power control logic” corresponds to the tuning circuit, which is the portion of PRCM 1470 that performs the functions recited in Elements 1[e1], 1[e2] and 1[e3] (*see supra* Section VII.B.1.e). Ex-1002 ¶206.

The tuning circuit generates a bin value from the EPB value and accesses the tuning table using the bin value for the reasons explained above for Claim 6. *See supra* Section VII.B.2.e.

VIII. The Board should not use its discretion to deny institution under *Fintiv*

The Board should decline to exercise its discretion to deny institution under 35 U.S.C. § 314(a). While Director Vidal’s June 21, 2022, Guidance made clear that “*Fintiv* is limited to facts of that case,” for completeness, Petitioner addresses the factors set forth in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential). As explained below, the six factors set out in *Fintiv* do not justify denying institution.

The **first *Fintiv* factor** is neutral because Samsung has not yet moved to stay the district court proceedings pending IPR, and the PTAB will not infer how the district court would rule should a stay be requested. *See, e.g., Hulu, LLC v. SITO Mobile R&D IP, LLC*, IPR2021-00298, Paper 11 at 10–11 (PTAB May 19, 2021).

For the **second *Fintiv* factor**, the district court has set a trial date in the Daedalus matter for May 20, 2024. This timing does not tip in favor of denying the petition in this case. *See, e.g., Apple Inc. v. Koss Corp.*, IPR2021-00305, Paper 14 at 13 (PTA June 3, 2021). This Petition is filed in March 2023. An institution decision should be issued within six months of docketing, around September 2023. And a final written decision (FWD) should be issued in September 2024. Thus, the

trial date is likely less than four months before the Final Written Decision (“FWD”). Recent PTAB cases analyzing similar schedules have weighed the second factor as neutral or, at most, slightly in favor of denial. *See, e.g., Google LLC et al. v. Parus Holdings, Inc.*, IPR2020-00847, Paper 9 at 12 (PTAB Oct. 21, 2020) (trial scheduled for three months before FWD weighs “at best, neutral”); *Apple Inc. v. Koss Corp.*, IPR2021-00305, Paper 14 at 13-14 (PTAB June 3, 2021) (trial scheduled for two months before FWD weighs “at most, minimally in favor” of denial).

“The PTAB will also consider additional supporting factors such as the number of cases before the judge in the parallel litigation.” Director Vidal’s June 2022 Guidance. Here, the court has scheduled seven other trials (2:21-cv-00305-*JRG K.Mizra v. Hewlett Packard*; 2:22-cv-00118-*JRG Element Capital v. BOE Technology*; 2:22-cv-00172-*JRG NetSocket v. Cisco Systems*; 2:22-cv-00254-*JRG-RSP Distributed Media Solutions v. Deezer*; 2:22-cv-00312-*JRG-RSP, Fleet Connect Solutions v. Southern Tire Mart*; 2:22-cv-00322-*JRG-RSP, Lionra Technologies Limited v. Fortinet, Inc.*; and 2:22-cv-00361-*JRG-RSP S3G, Technology LLC v. Nordstrom Inc.*) in the same week as the trial for this case.

If the median time to trial for civil actions in the Eastern District of Texas is used to estimate the trial date (i.e., to account for potential delays, etc.), as advised by Director Vidal’s June 2022 Guidance, trial should not be expected to occur until

October 2024, after a FWD will issue. Ex-1017 at 35 (indicating a most-recent median time to trial for civil actions in the Eastern District of Texas of 24.5 months).

The **third *Fintiv* factor** weighs strongly against denial. In particular, Samsung has not yet answered Daedalus’s Complaint, and has instead moved to dismiss. No hearing has been set and no substantive activity has occurred in the case. Because the investment in the trial has been minimal and Petitioner acted diligently, this factor weighs strongly against discretionary denial. *See, e.g., Hulu*, Paper 11 at 13.

The **fourth *Fintiv* factor** also weighs against denial. As explained above, the median time to trial for civil actions in the Eastern District of Texas suggests that trial will not occur until after a FWD is issued. Thus, “there is a reasonable likelihood that the Board will address the overlapping validity issues prior to the district court reaching them at trial..., thereby providing the possibility of simplifying issues for trial.” *Juniper Networks, Inc. v. Packet Intelligence LLC*, IPR2020-0039, Paper 21 at 18 (PTAB Sept. 10, 2020); *see also MED-EL Elektromedizinische Geraete GmbH v. Sonova AG*, IPR2020-00176, Paper 13 at 15 (PTAB June 3, 2020) (“As to the fourth factor, the parties do not dispute that overlap exists between the invalidity issues in this case and in the district court. This overlap may inure to the district court’s benefit, however, by simplifying

issues for trial should we reach our determination on the challenges raised in the Petition before trial.”).

Moreover, Petitioner is challenging more claims than asserted in the district court litigation. Patent Owner’s infringement contentions assert only Claims 1–3. This Petition challenges Claims 1–6, 11, 13, and 15–20. This *inter partes* review proceeding is thus the only venue in which the invalidity challenges against several claims in the ’197 Patent will be adjudicated. Moreover, reviewing the challenged claims in this proceeding promotes efficiency in that many more claims will be addressed here, which will resolve disputes against future district court defendants. *See Fintiv*, Paper 11 at 4 (“the Board’s cases addressing earlier trial dates as a basis for denial under NHK have sought to balance considerations such as system efficiency, fairness, and patent quality.”). Accordingly, challenging additional claims further weighs against denial. *See, e.g., Vudu, Inc. v. Ideahub, Inc.*, IPR2020-01688, Paper 16 at 14–15 (PTAB April 19, 2021) (“differences in asserted claims” and claims challenged in the petition weighs against denial).

On the **fifth *Fintiv* factor**, the Board should give little weight to the fact that Petitioner and PO are the same parties as in district court. Although Samsung is both petitioner and litigation defendant, this factor does not outweigh the other factors that strongly weigh against discretionary denial. *See Weatherford U.S.*,

L.P., v. Enventure Global Tech., Inc., IPR2020-01684, Paper 16 at 11–13 (PTAB Apr. 14, 2021).

“Other circumstances” under the **sixth *Fintiv* factor** further weigh against discretionary denial. The Petition’s merits are strong with two primary references, Naveh and Titiano, alone or in combination with one or two secondary references, rendering each of independent Claims 1, 11, and 15 and dependent Claims 2–6, 13, and 16–20 obvious. *See Align Technology, Inc. v. 3Shape A/S*, IPR2020-01087, Paper 15 at 42–43 (PTAB Jan. 20, 2021); *see also supra* Section VII.

Taken together holistically, the *Fintiv* factors strongly weigh against exercising discretion to deny institution.

IX. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for Claims 1–6, 11, 13, and 15–20 of the ’197 Patent based on each of the grounds specified in this Petition.

Respectfully Submitted,

/s/ John Kappos

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CERTIFICATE OF WORD COUNT

Under 37 C.F.R. § 42.24(d), Petitioner certifies that this petition includes 13,990 words, as measured by Microsoft Word, exclusive of the table of contents, mandatory notices under § 42.8, certificates of service, word count, and exhibits.

CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e)(1))

The undersigned hereby certifies that the above document was served on March 24, 2023, by filing this document through the Patent Trial and Appeal Board P-TACTS System, as well as delivering a copy via express mail upon the following attorneys of record for the Patent Owner and Petitioner:

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Dated: March 24, 2023

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