

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.
Petitioner

v.

SHAMROCK INNOVATIONS, LLC
Patent Owner

Case No. IPR2023-00754
Patent No. 8,060,675

PETITION FOR *INTER PARTES* REVIEW

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1002	Prosecution History of the ’675 patent
1003	U.S. Patent No 5,991,304 to Abramson
1004	U.S. Patent No. 4,450,572 to Stewart et al. (“Stewart”)
1005	U.S. Patent No. 5,170,272 to Onno (“Onno”)
1006	U.S. Patent No. 4,979,185 to Bryans et al. (“Bryans”)
1007	Declaration of Michael Caloyannides, Ph.D.
1008	Curriculum Vitae of Michael Caloyannides, Ph.D.
1009	U.S. Patent No. 6,088,752 to Ahern et al.
1010	U.S. Patent No. 6,070,214 to Ahern et al.

I. INTRODUCTION

Western Digital Technologies, Inc. (“Petitioner” or “WD”) seeks an *inter partes* review (“IPR”) under 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42 to invalidate claim 7 of expired U.S. Patent No. 8,060,675 to Ahern et al. (“’675 patent”; EX. 1001), titled “COMPUTING MODULE WITH SERIAL DATA CONNECTIVITY” and currently owned by Shamrock Innovations, LLC, (“Shamrock” or “Patent Owner”).

As explained in this petition, claim 7 of the ’675 patent is unpatentable based on at least the prior art references presented herein, and there exists a reasonable likelihood that Petitioner will prevail based on at least one of the asserted invalidity grounds. Accordingly, Petitioner respectfully submits that the Board should institute an IPR and cancel claim 7 as unpatentable.

II. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104

A. Grounds for Standing Under 37 C.F.R. § 42.104(a)

Petitioner certifies that the ’675 patent is available for IPR. Petitioner is not barred or estopped from requesting review of claim 7 on the below-identified grounds.

B. Challenge/Relief Requested Under 37 C.F.R. § 42.22(a)(1) and 42.104(b)(1)-(2)

Petitioner requests *inter partes* review and invalidation of claim 7 of the '675 patent based on the grounds summarized in the table below. References to 35 U.S.C. § 102 are pre-AIA.

Ground	Basis for Unpatentability
1	Anticipated under 35 U.S.C. § 102(b) by U.S. Patent No. 4,450,572 to Stewart (“Stewart”)
2	Anticipated under 35 U.S.C. § 102(b) by U.S. Patent No. 4,979,185 to Bryans (“Bryans”)
3	Anticipated under 35 U.S.C. § 102(b) by U.S. Patent No. 5,170,272 to Onno (“Onno”)

III. OVERVIEW OF THE STATE OF THE ART AND THE '675 PATENT

A. Background and State of the Art

The following background is based on the accompanying Declaration of Michael Caloyannides, Ph.D. (EX 1007) and is supported by various prior art references (*see* EX. 1004, EX. 1005, and EX. 1006).

Serial communication has been known as far back as the invention of morse code, which transmitted data one bit at a time, in the form of a dot or dash. EX. 1007, at ¶ 19. As the proliferation of digital devices grew, and the speed at which

they operated continued to increase, devices were designed to operate using parallel data busses to increase the bandwidth of the respective devices. EX. 1007, at ¶ 16. This was known as far back as 1989. *Id.* For devices separated by more than a short distance, however, it was advantageous to use serial data communication, which reduces issues of cost, weight, interference, and electrical loading associated with parallel data communications. *Id.* at 17.

To send data between parallel devices using serial communications, parallel-to-serial and serial-to-parallel data converters were required to convert the parallel data to serial data, and vice versa. EX. 1007, at ¶ 21. This conversion, both from parallel data to serial data and from serial data to parallel data, requires conversion circuitry, which has been commonplace in the art, at least as far back as 1982. EX. 1007, ¶ 18.

Encoding of clock (or other control) data within the serialized data was used to provide sufficient information to a receiving device to be able to decode the received serialized data and convert back to parallel data as needed. EX. 1007, ¶¶ 19-21. Decoding circuitry on the receiving devices extracted the clock data for use in deserializing the received data using various known methods. EX. 1007, at ¶ 21.

B. The '675 Patent and Its Prosecution History

The '675 patent issued on November 15, 2011, from U.S. Patent Application No. 12/644,511 (“the '511 application”), filed on December 22, 2009. EX. 1001, cover. The '675 patent purports to claim priority to U.S. Application Serial No. 11/300,131, filed on December 13, 2005, now U.S. Patent No. 7,657,678 (“'678 patent”), which is a continuation of Application No. 09/559,678, filed on April 27, 2000, now U.S. Patent No. 7,734,852 (“'852 patent”), which is a continuation-in-part of Application No. 09/130,057, filed on August 6, 1998, now U.S. Patent No. 6,088,752 (“'752 patent”), which is a continuation-in-part of Application No. 09/130,058, filed on August 6, 1998, now U.S. Patent No. 6,070,214 (“'214 patent”). The '675 Patent also claims priority to provisional Application No. 60/198,317, filed on April 19, 2000. The earliest possible date to which the '675 patent can claim priority is August 6, 1998. EX1001, cover. Because the prior art references used in this Petition all published more than one year before August 6, 1998, Petitioner has not analyzed whether or not the '675 patent is entitled to an earlier filing date, but reserves the right to do so at a later date if it becomes relevant.

The '675 patent generally discloses providing a bridge device for facilitating communication between two parallel device such that the bridge device appears “transparent” to software on the communicating device. EX. 1001, at col. 3:61-65.

To ensure transparency, “all accesses to the configuration space were encoded, serialized, and ‘echoed’ across the serial link.” EX. 1001, at col. 1:65-67. This is stated as being accomplished via “Split-Bridge™” technology as disclosed in at least prior-filed application nos. 09/130,057 (now the ’752 patent) (EX. 1009) and 09/130,058 (now the ’214 patent) (EX. 1010), to which the ’675 patent claims priority.

The ’214 patent explains that the “Split-Bridge™” technology used by the noted bridge device (such as that described within the ’675 patent) includes two separate interface devices that are operable to “(a) send bus-related information serially through the link in a format different from that of the first bus and the second bus, (b) approve an initial exchange between the first bus and the second bus in response to a pending transaction having a characteristic signifying a destination across the bridge, and (c) allow the host processor, communicating through the first bus, to individually address different selectable ones of the bus compatible devices on the second bus. . . .” EX. 1010, at col. 3:45-54. Thus the “Split-Bridge™” technology requires specific steps to be performed to provide the desired “transparency” between devices, as outlined above. This process was described in detail throughout the ’214 patent specification, as well as in the claims. *See, e.g.*, EX. 1010 at col. 12:29 – col. 18:63. The ’752 Patent discloses similar subject matter to the ’214 patent.

In contrast to the Split-Bridge™ specific protocols and implementations described in detail not only throughout the '675 patent but also within the parent '214 and '752 patents (discussed above), claim 7 of the '675 patent diverges to claim the general concept of facilitating serial communication between parallel devices. Claim 7 abandons any connection or tie to the earlier-disclosed Split-Bridge™ technology and attempts to broadly claim: a) conversion of parallel data to serial data for transmission over a serial link; b) conversion of serial data received over the serial link to parallel data; and c) generation of a clock from the received data. As noted above in the discussion of the state of the art, these general concepts were already well known in the art at the time of the claimed invention. EX. 1007, at ¶¶ 16-22.

The '675 patent issued after a relatively brief prosecution. Claim 7 (originally-filed claim 13) was initially rejected as being anticipated in view of U.S. Patent No. 5,991,304 to Abramson (EX 1003), as well as under a non-statutory double patenting rejection in view of the applicant's U.S. Patent Application No. 11/300,131 (now the '678 patent). EX. 1002, at pp. 263-272 (non-final Office action, dated June 21, 2010). In response, the applicant amended originally-filed claim 13 to recite, *inter alia*, "generating a first clock signal, for use by the first module, using the second serial data" and cited the U.S. Application No. 09/130,058 (now the '214 patent (EX 1010)), cols. 6:33-46, 8:38-

53, as support for the amendment. EX. 1002, at pp. 238-252 (response to non-final Office action dated October 21, 2010). In a subsequent Office action, the examiner removed the anticipation rejection of claim 13 in view of the new amendments, and upon the filing of a terminal disclaimer, allowed claim 13 (issued claim 7). EX. 1002 at pp. 206-216 (final Office action dated November 19, 2010). It does not appear that the examiner performed any additional searching, nor did the examiner explain how the proposed amendment overcame the previously asserted art. *Id.* Rather, the examiner allowed overly-broad claim 7 with minimal prosecution and without identifying the allegedly patentable subject matter of claim 7.

IV. OVERVIEW OF THE PRIOR ART

As explained above, the earliest possible priority date of the '675 patent is August 6, 1998. As shown below in this brief introduction to the prior art, the applied references are prior art to the '675 patent under pre-AIA 35 U.S.C. § 102(b).

A. Stewart (EX 1004)

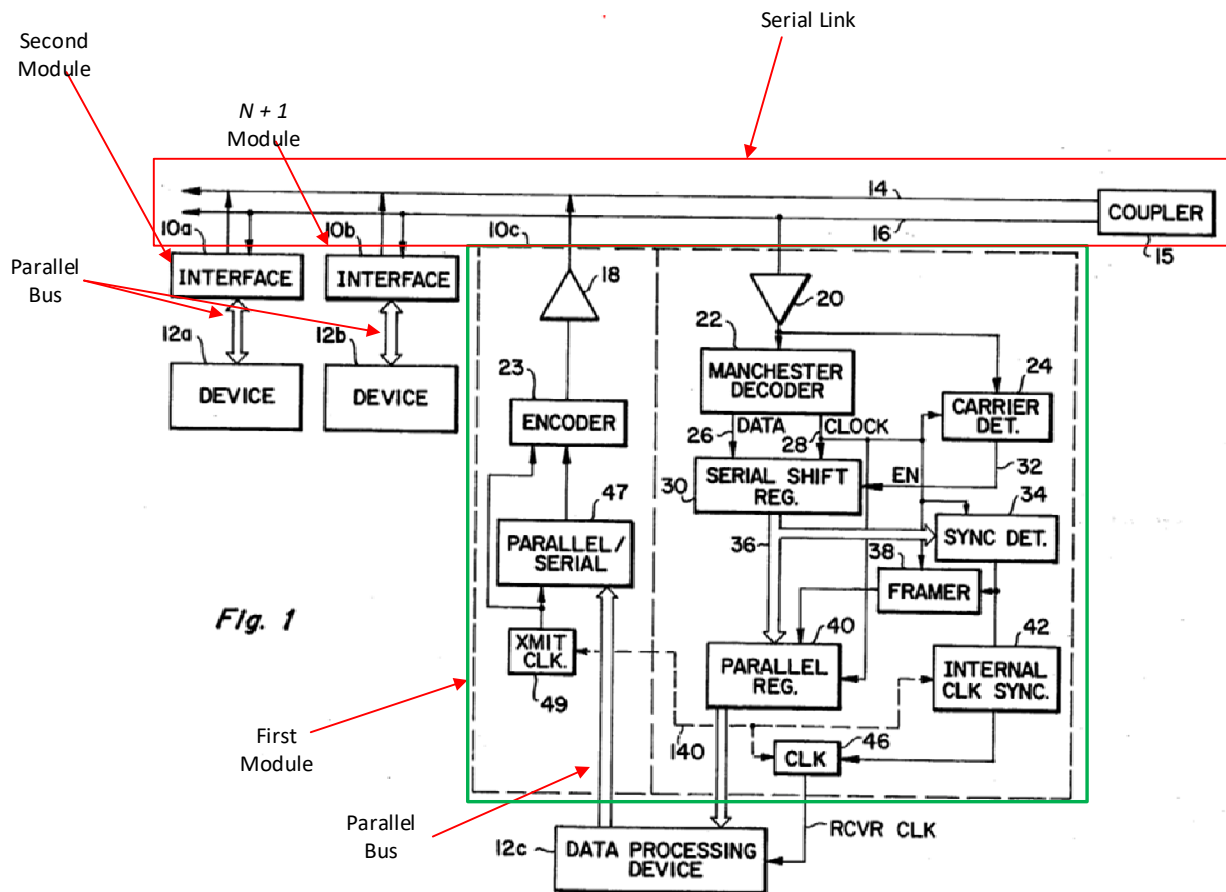
Stewart issued on May 22, 1984, more than one year before the '675 patent's earliest possible priority date. EX. 1004, at 1. Stewart is therefore prior art to the '675 patent under 35 U.S.C. § 102(b). Stewart was not before the examiner during

prosecution of the '675 patent, nor is Stewart duplicative of any art considered.

EX. 1001, at pp. 1-4.

Stewart discloses “an interface for coupling a computer with a data communications link that permits asynchronous bit-serial communications among devices transmitting and receiving Manchester-type codes over a serial information channel.” EX. 1004, col. 2:34-39. Parallel data is converted from the parallel format to a serial format and then transmitted to a target device over a serial communication link. *Id.*, col. 5:9-22. Stewart further discloses that encoded serial data is converted to parallel data and stored in a parallel register. *Id.*, col. 4:1-35. The received serial data is decoded to extract the data packets and an encoded clock signal. *Id.*, col. 4:11-16.

The following annotated Figure 1 from Stewart shows the serial links, modules, and interface devices as described by Stewart.

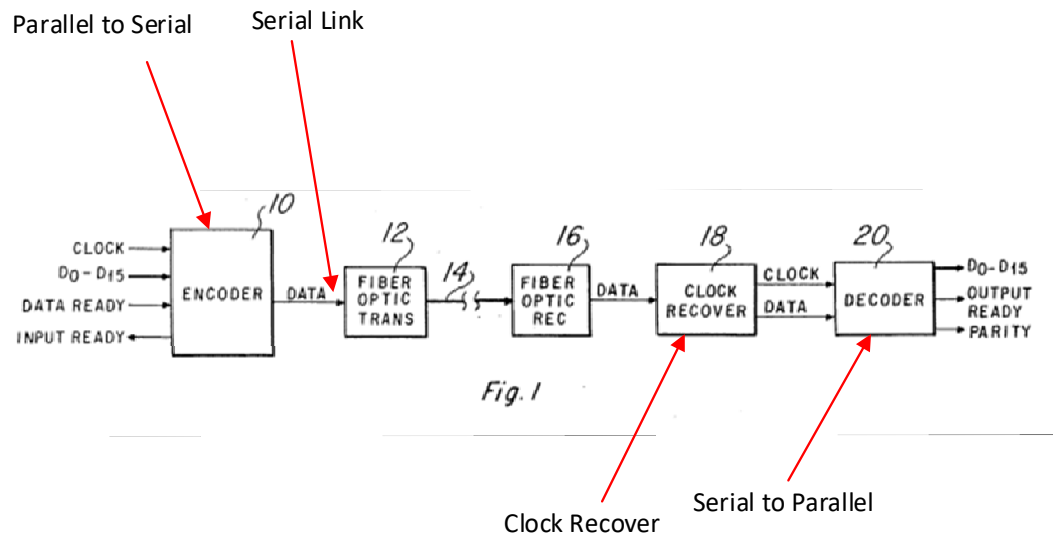


Stewart FIG. 1 (Annotated)

B. Bryans (EX. 1006)

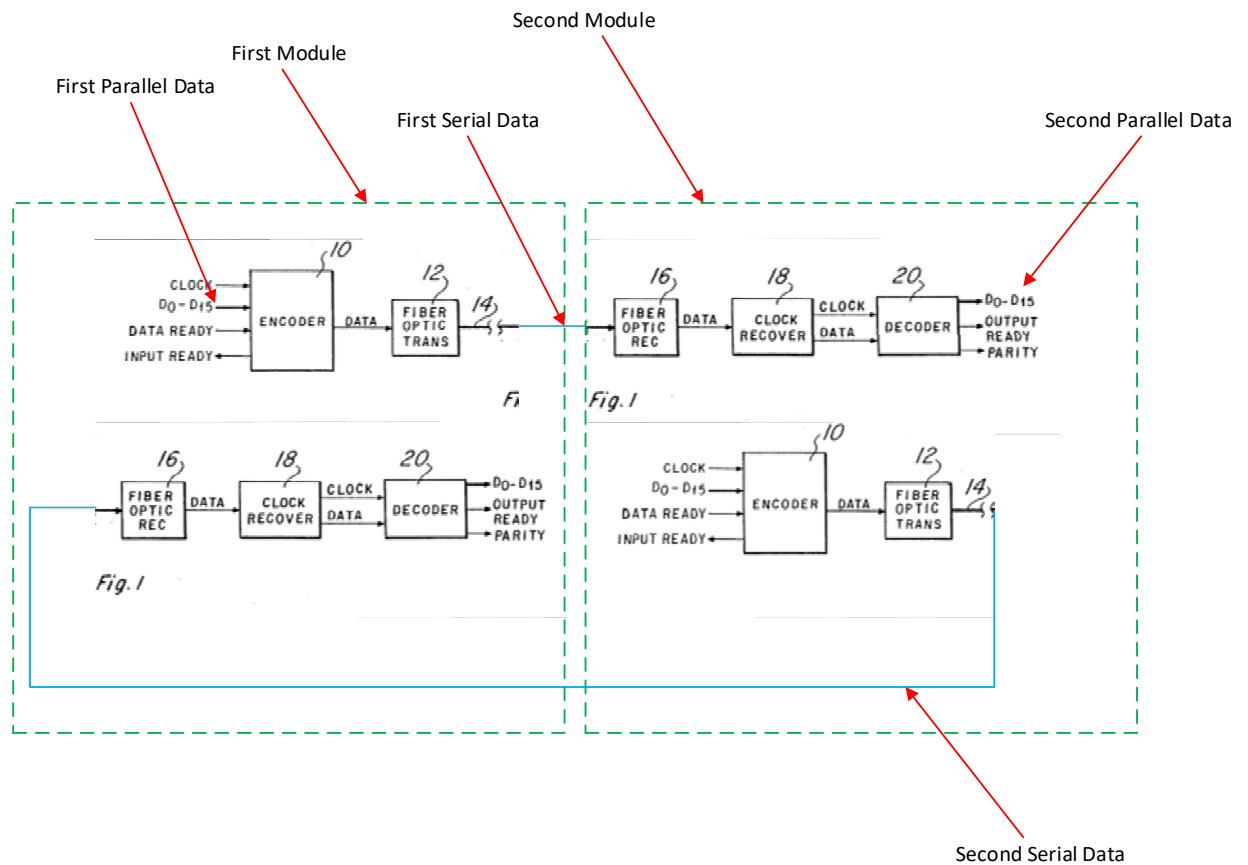
Bryans issued on December 18, 1990, more than one year before the '675 patent's earliest possible priority date. EX. 1006, at p. 1. Bryans is therefore prior art to the '675 patent under 35 U.S.C. § 102(b). Bryans was not before the examiner during prosecution of the '675 patent, nor is Bryans duplicative of any art considered. EX. 1001, at pps. 1-4.

Bryans discloses a high bit rate serial link for transmitting data asynchronously between two parallel devices. EX. 1006, at col. 2:4-5, 41-44. An encoder converts data from parallel to serial form for transmission, and a decoder converts received data back into parallel form. EX. 1006, at col. 2:11-22. A clock signal is further extracted from the received data by a clock recovery circuit. EX. 1006, at col. 2, lines 18-22. The following annotated Figure 1 from Bryans illustrates the general architecture of the serial communication link of Bryans as it would have been understood by a PHOSITA.



Bryans FIG. 1 (Annotated)

A modified version of Bryans FIG. 1 below shows the circuitry of the two parallel devices described in Bryans.

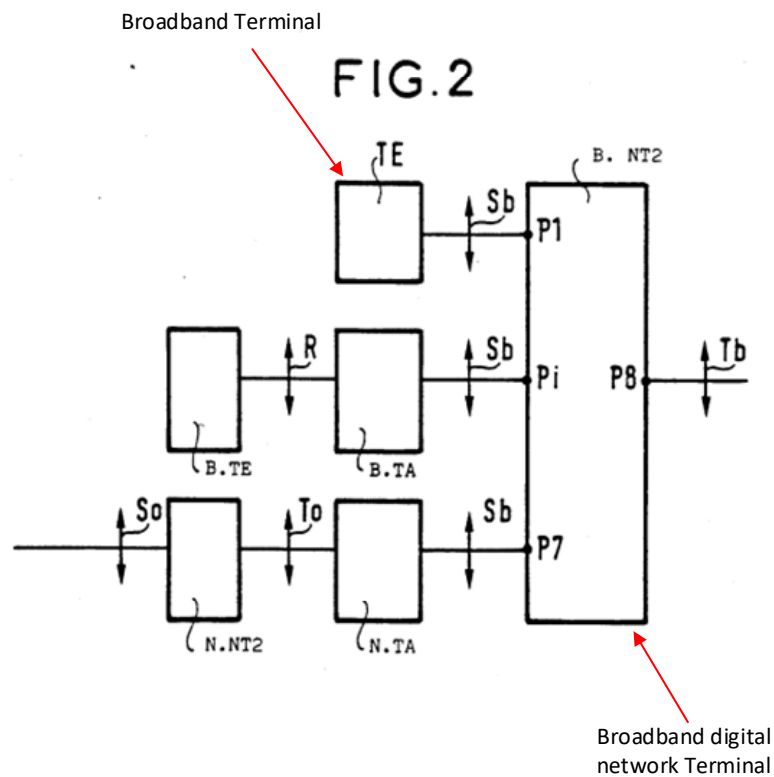


Bryans FIG. 1 (Annotated and Modified to Show Described Parallel Devices)

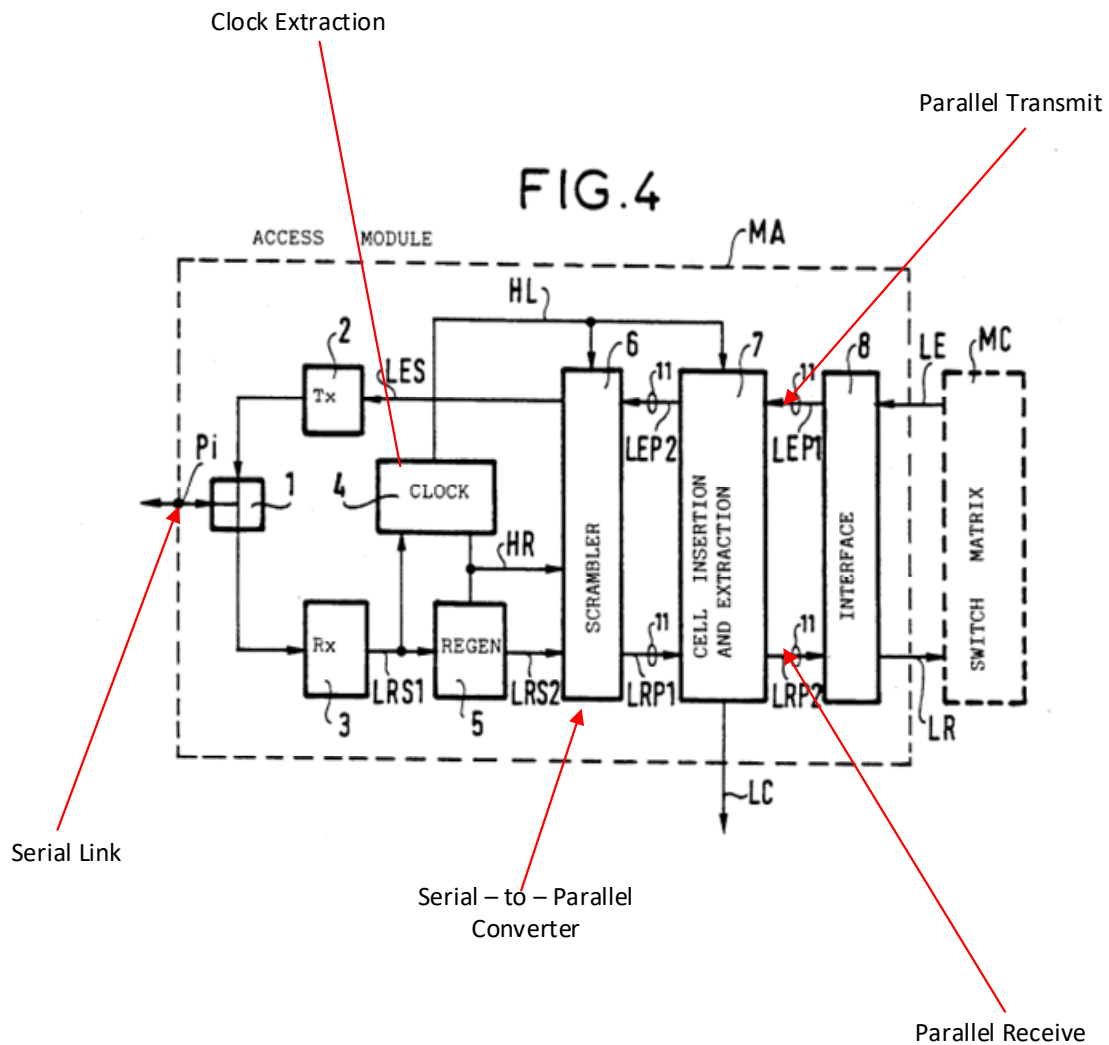
C. Onno (EX. 1005)

Onno issued on December 8, 1992, more than one year before the '675 patent's earliest possible priority date. EX. 1005, at p. 1. Onno is therefore prior art to the '675 patent under 35 U.S.C. § 102(b). Onno was not before the examiner during prosecution of the '675 patent, nor is Onno duplicative of any art considered. EX. 1001, at pps. 1-4.

Onno discloses broadband digital network terminals (B.NT2) for use with an asynchronous network using asynchronous serial communication between modules, such as a digital network terminal and one or more broadband terminals (TE). EX. 1005, at 2:51-66. The broadband digital network terminal performs serial to parallel conversion of data, and vice versa depending on whether it is transmitting or receiving. EX. 1005, at 4:20-31. A clock module of a receiving device recovers a clock signal from data received over a serial link. EX. 1005, at col. 4:11-16. The following annotated Figures 2 and 4 from Onno highlight the general architecture of the Onno system.



Onno FIG. 2 (Annotated)



Onno FIG. 4 (Annotated)

V. LEVEL OF ORDINARY SKILL IN THE ART

A person having ordinary skill in the art of the '675 patent at the time of the alleged invention would have had at least a bachelor's degree in electrical engineering, or equivalent, with about three years of professional work experience in serial and parallel data communication within or between computing devices or

systems. EX. 1007, ¶ 33. More education can supplement practical experience and vice versa. *Id.*

VI. CLAIM CONSTRUCTION UNDER 37 C.F.R. §§ 42.104(B)(3)

Claim terms should be construed according to the *Phillips* standard and given their ordinary and customary meaning as understood by one of ordinary skill in the art at the time of the invention, in light of the claim language, the specification, and the prosecution history. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (en banc); 37 C.F.R. § 42.100.

A. “Generating a first clock signal, for use by the first module, using the second serial data”

Claim 7 recites the method step of “***generating*** a first clock signal, for use by the first module, using the second serial data.” EX 1001, col. 10:4-5. This claim term does not appear anywhere in the specifications of the ’675 patent, the ’675 patent’s priority applications, or the patents or applications incorporated by reference in the ’675 patent. *See* EX 1001, EX 1009, EX 1010. During prosecution of the ’675 patent, the applicant added this limitation by amendment and cited portions of the related ’214 patent in support. EX. 1002, at pp. 238-252 (response to non-final Office action dated October 21, 2010) (citing U.S. Application No. 09/130,058 (now the ’214 patent (EX 1010)) at cols. 6:33-46, 8:38-53)). The cited portions of the ’214 patent, however, do not include “generating a first clock

signal . . .” and do not inform its intended meaning. See EX 1010 at cols. 6:33-46, 8:38-53; EX 1007, at ¶¶ 36-37.

Without any other helpful intrinsic evidence, the language and context of the claim itself would have informed a PHOSITA. In particular, this method step of claim 7 recites “generating a first clock signal,” not out of thin air or in a vacuum, but instead “**using the second serial data.**” EX. 1007, at ¶ 37. Thus, in the context of claim 7 and the art, a PHOSITA would have understood that “generating a clock signal . . . using second serial data” would include ways of producing a clock signal by **using** the second serial data, such as by extracting or recovering a clock signal **from** the second serial data. EX. 1007, at ¶ 37.¹

VII. CLAIM 7 OF THE '675 PATENT IS UNPATENTABLE

Each of the applied prior art references—Stewart, Bryans, and Onno—anticipates independent claim 7 of the '675 patent, as detailed below.

¹ Petitioner reserves all rights to raise claim construction and other arguments in district court as relevant and necessary to those proceedings. For example, a comparison of the claims to any accused product in litigation may raise claim construction controversies that are not present here, as well as challenges under 35 U.S.C. § 112 not applicable in IPR proceedings.

A. Ground 1: Stewart Anticipates Claim 7

As explained below, Stewart (EX 1004) anticipates claim 7.

7. A method comprising:

asynchronously, serially transferring first serial data, corresponding to first parallel bus data, from a first module to a second module using a serial link;

Stewart describes a method of performing asynchronous serial communication over a serial communication link, in general. EX. 1007, at ¶ 39. Specifically, Stewart discloses a “data communication link that permits asynchronous bit-serial communications among devices . . . over a serial information channel.” EX. 1004, at col. 2:35-39. Stewart further discloses that communication between “devices 12 coupled to the communications link [are allowed to] operate asynchronously and independently – i.e., under control of its own separate clocking circuit.” EX. 1004, at col. 2:13-15. Thus, Stewart unambiguously discloses asynchronous serial transmission of data from a first module (transmitting device) to a second module (receiving device). EX. 1007, at ¶ 40.

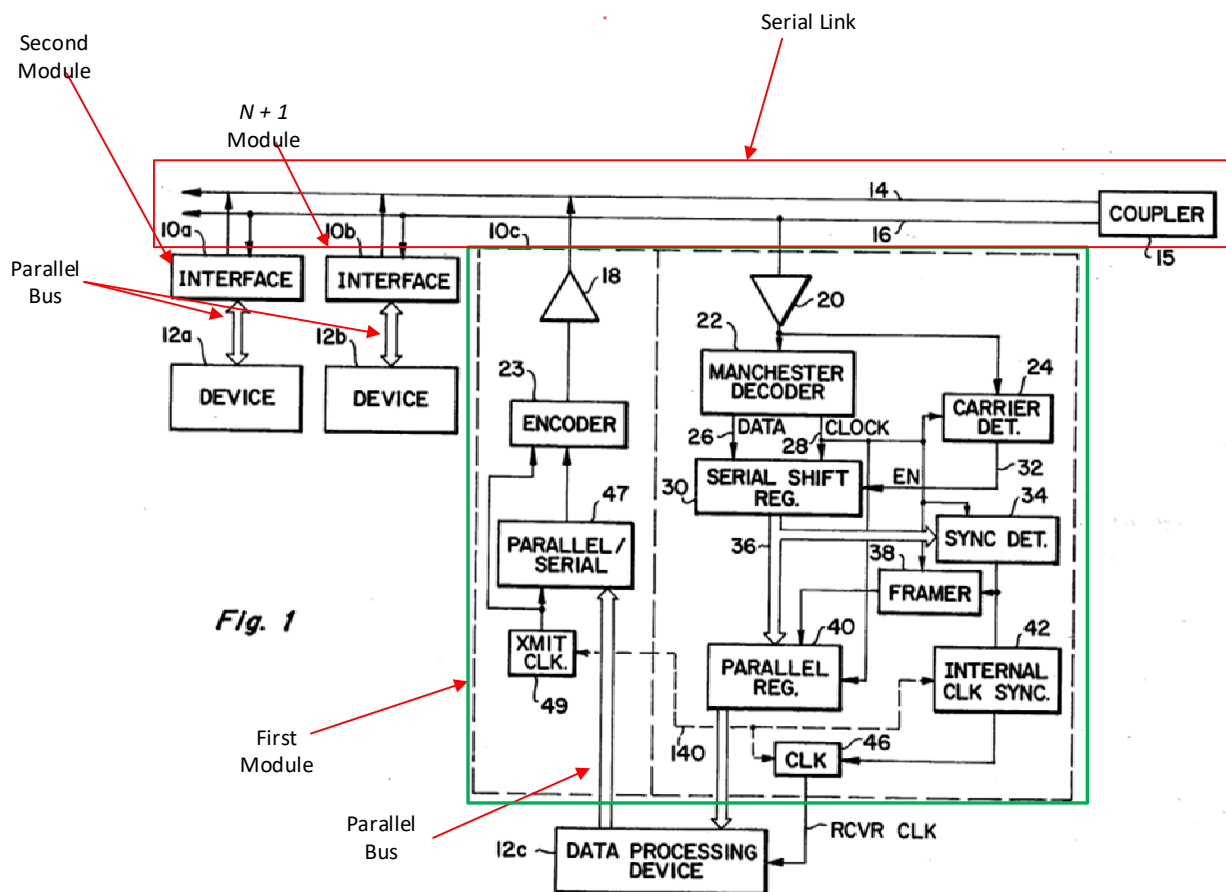
Stewart further discloses the claimed step of “serially transferring first serial data . . . from a first module to a second module using a serial link.” Stewart states,

with respect to interface 10c,² “a parallel-to-serial register 47 receives eight-bit bytes from the device 12c under control of a clock located therein, and when the signals representing the byte settle in the register 47, a clock 49 effects a shift on a serial basis of the data bits constituting the byte to the encoder. . . . These information signals are then applied to drive 18 which places the encoded information signals on the transmitting channel 14 where they are distributed by the passive coupler 15 to the other devices connected to the communicating link.” EX. 1004, at col. 5:9-22. This plainly discloses serial transmission (i.e., transferring) of serial data from a first module 10c to other devices on the link 14, such as 10a, 10b. EX. 1007, at ¶¶ 41-42.

Furthermore, Stewart discloses that the communications link includes “a transmitting channel 14 and a receiving channel 16 over which a plurality of devices 12a, 12b, and 12c connect via their respective interfaces 10a, 10b, and 10c. Information on the transmitting and receiving channels 14 and 16 are coupled by a

² Interface 10c is referenced throughout Stewart as it is described and shown as an “expanded block diagram of the interface circuitry” of the respective interfaces 10a, 10b, and 10c. EX. 1004, at col. 4:1-5, FIG. 1. A PHOSITA would have understood that the block diagram of 10c represents the circuitry and operation of interfaces 10a, and 10b as well. EX. 1007, ¶ 45.

coupler 15 which enables devices on the channel 16 to sense information signal transmitted on the channel 14.” EX. 1004, at col. 3:56-63. Thus, the serial channels 14 and 16, combined with the coupler 15, form a duplex serial link for two way “asynchronous bit-serial communications among devices.” EX. 1007, at ¶¶ 41, 45. This is further illustrated in annotated FIG. 1 of Stewart, below.



Stewart FIG. 1 (Annotated)

Stewart discloses that the serial data transmitted over the serial link 14 corresponds to first parallel data. EX. 1007, at ¶ 44. As discussed above, Stewart

discloses a “parallel-to-serial register 47 receives eight-bit bytes [parallel data] from the device 12c under controller control of a clock located therein, and when the signals representing the byte settle in the register 47, a clock 49 effects a shift on a serial basis of the data bits constituting the byte to the encoder. . . . These information signals are then applied to drive 18 which places the encoded information signals on the transmitting channel 14 where they are distributed by the passive coupler 15 to the other devices connected to the communicating link.”

EX. 1004, at col. 5:9-22. The parallel data is converted into serial data for transmission over transmitting channel 14, thereby disclosing that the first serial data corresponds to “first parallel bus data,” as claimed. EX. 1007, at ¶ 44.

Annotated FIG. 1 (above) explicitly shows the parallel bus (having parallel bus data) coupling the data processing device 12c to the parallel-to-serial register 47.

asynchronously, serially receiving second serial data, corresponding to second parallel bus data, from the second module using the serial link; and

Stewart recites that an objective of the invention is to provide a “data communication link that permits asynchronous bit-serial communications among devices transmitting and ***receiving*** . . . over a serial information channel.” EX. 1004, at col. 5:5-8 (emphasis added). This plainly discloses “asynchronously, serially receiving second serial data. . . . from the second module using the serial link.” EX. 1007, at ¶ 48.

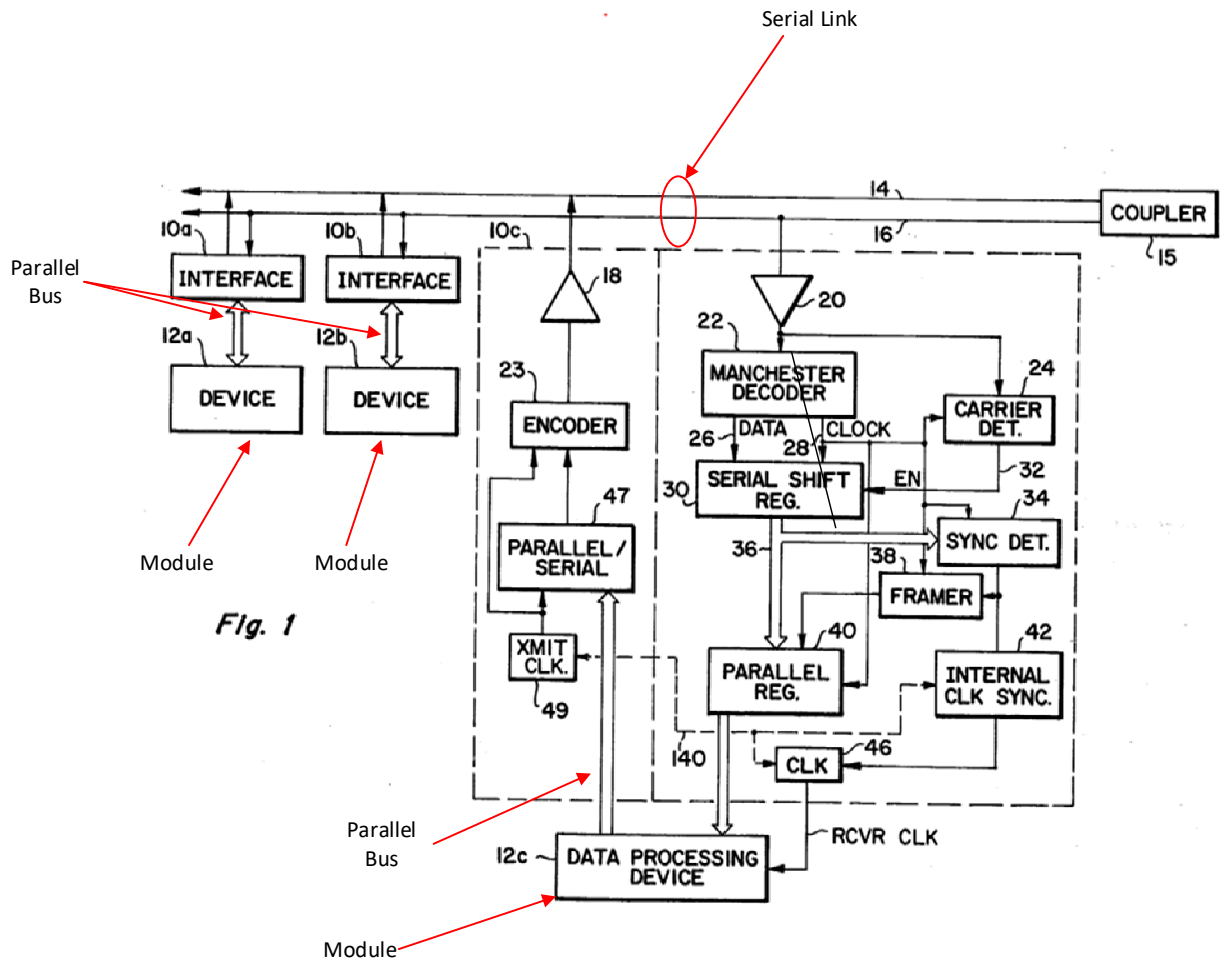
Furthermore, Stewart discloses that the interface 10c “receives from the receiving channel 16 signals representing serial data bits are [sic] clock transitions and supplies these signals to a Manchester decoder.”³ The data is received from a second module, such as interfaces 10a or 10b. EX. 1007, ¶ 53. Thus, Stewart discloses that the serially received data is received from a second module over the serial link (serial transmission line 14, receiving line 16, and coupler 15, as described above). EX. 1007, ¶¶ 49-50

Stewart explains that the “invention is concerned with a system for decoding Manchester-encoded serial data and transferring the decoded data to a parallel device.” EX. 1004, at col. 4:1-3. More specifically, Stewart discloses that data received at the driver 20 from the “the receiving channel 16 [are] signals representing serial data bits and supplies these signals to a Manchester decoder 22. . . . The decoder 22, being subsequently described, extracts the data signal (herein called data bits) and a clock (i.e., CLOCK) signal from the information signals on the channel 16 and supplies both the data bits and the CLOCK signal to

³ Manchester encoding is known in the art to encode data with representations of digital data bits and a clocking signal, which are combined “together for transmission as but one common information signal which [is] sent over a single serial data channel.” EX. 1004, at col. 1:54-58.

a serial shift register 30” EX. 1004, at col. 4:5-15. Stewart goes on to state that as “each set of eight data bits accumulates in the serial register 30, a byte is transferred under control of a framer 38, also subsequently described, which enables the loading of the parallel register 40 associated with the serial register 30.” EX. 1004, at col. 4:37-41. Therefore, the received data is converted to parallel data via the parallel register, disclosing that the received data corresponds to parallel data. EX. 1007, at 53.

Stewart further explains that within each of the interfaces 10a-10c, “a parallel-to-serial register 47 receives eight-bit bytes from the devices 12 under control of a clock located therein, and then signals representing the byte settle in the register 47, a clock 49 effects a shift on a serial basis of the data bits constituting the byte to the encoder 23.” EX. 1004, at col. 5:9-15. As interfaces 10a, 10b, 10c would all be understood to have the same functionality, it would also be understood that any data received at interface device 10c would have previously been converted from parallel data on a parallel bus, such as shown below in annotated FIG. 1 of Stewart, prior to being received at interface device 10c. EX. 1007, ¶¶ 51-53.



Stewart FIG. 1 (Annotated)

generating a first clock signal, for use by the first module, using the second serial data.

Stewart discloses that interface 10c “receives from the receiving channel 16 signals representing serial data bits [and] clock transitions and supplies these signals to a Manchester decoder 22. . . . The decoder 22, being subsequently described, extracts the data signals (herein called data bits) ***and a clock (i.e.,***

CLOCK) signal from the information signals.” EX. 1004, at col. 4:8-16 (emphasis added). Applying the construction of this claim limitation set forth above, Stewart’s decoder 22, as described above, **generates or produces** the clock signal by extracting it **from** (i.e., **using**) the received Manchester encoded data (i.e., second serial data). EX. 1007, at ¶ 56 (emphasis added). Accordingly, a device, such as interface device 10c, receiving the serial data over line 16, generates a clock signal using the received (second serial) data. EX. 1007, at ¶¶ 56-57.

In summary, as explained above, Stewart discloses each element of claim 7 and therefore anticipates claim 7.

B. Ground 2: Bryans Anticipates Claim 7

As explained below, Bryans (EX 1006) anticipates claim 7.

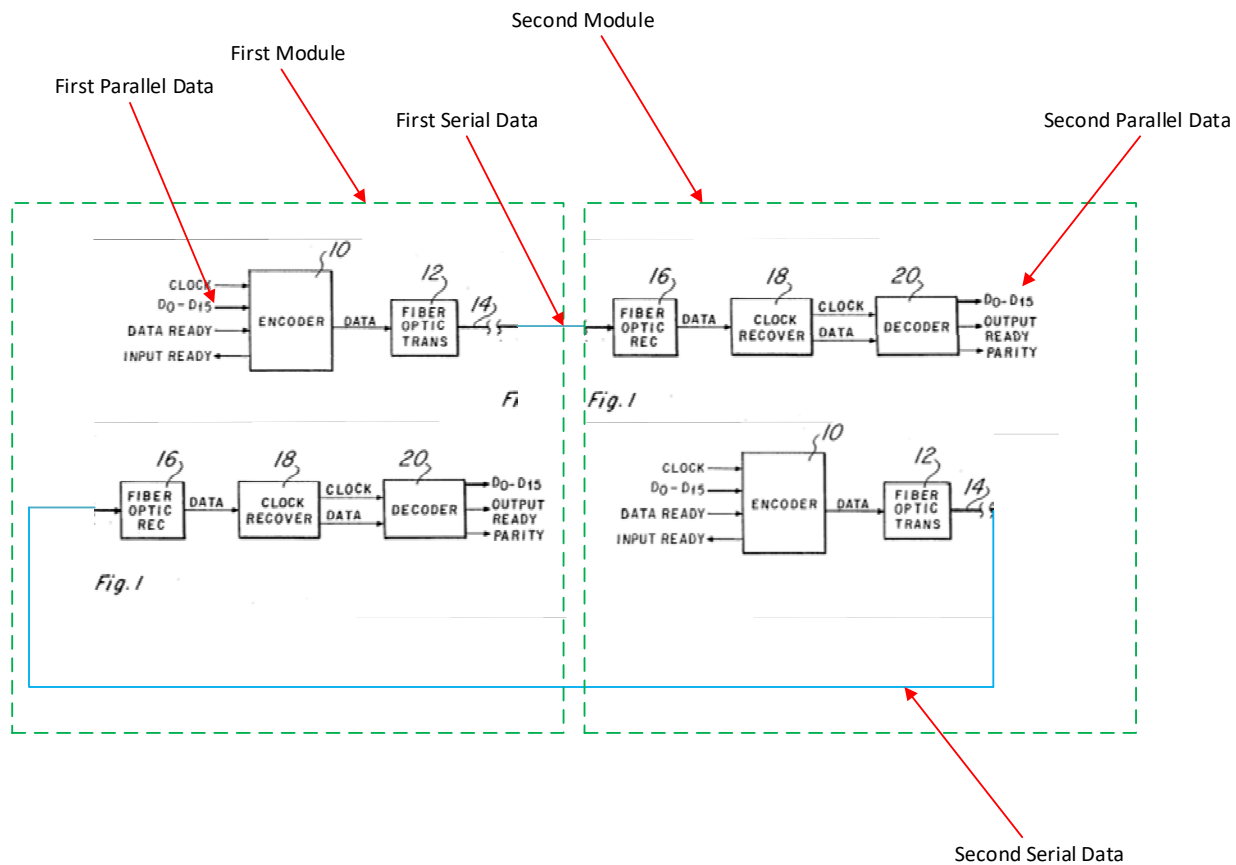
7. A method comprising:

asynchronously, serially transferring first serial data, corresponding to first parallel bus data, from a first module to a second module using a serial link;

Bryans discloses a “method and device for transmitting serial data at very high speeds.” EX. 1006, at col. 1:7-8. Bryans further discloses that the systems and methods are “preferably operated asynchronously, requiring that a sync pulse be transmitted along the serial link prior to transmission of each data word.” EX. 1006, col. 2:41-44. Thus, the transmission or “transferring” of data disclosed in Bryans is performed asynchronously. EX. 1007, at ¶ 60.

Bryans further discloses parallel data in the form of a “16 bit data word is presented to an encoder device 10 on lines $D_0 - D_{15}$. . . The encoder device 10 converts the data from parallel to serial form and sends it to a fiber optic transmitter 12. The data is transmitted along a fiber optic cable 14 to a fiber optic receiver 16.” EX. 1006, at col. 2:13-16. Thus, the data transmitted via the fiber optic transmitter 12 is serial data based on the parallel data provided to the encoder device 10. EX. 1007, at ¶ 57-58. As noted above, this data is transmitted “asynchronously” EX. 1006, at col. 2:13-15. This data is transmitted over a serial link in the form of fiber optic cable 14. EX. 1007, at ¶¶ 61-62. Annotated Bryans FIG. 1, below, illustrates that the first parallel data is converted to first serial data which is then transmitted over the serial link 14.

To further illustrate this disclosure, a modified version of FIG. 1 of Bryans below shows the circuitry of the two parallel devices described in Bryans. *Id.* at ¶ 65.



Bryans FIG. 1 (Annotated and modified to show described parallel devices)

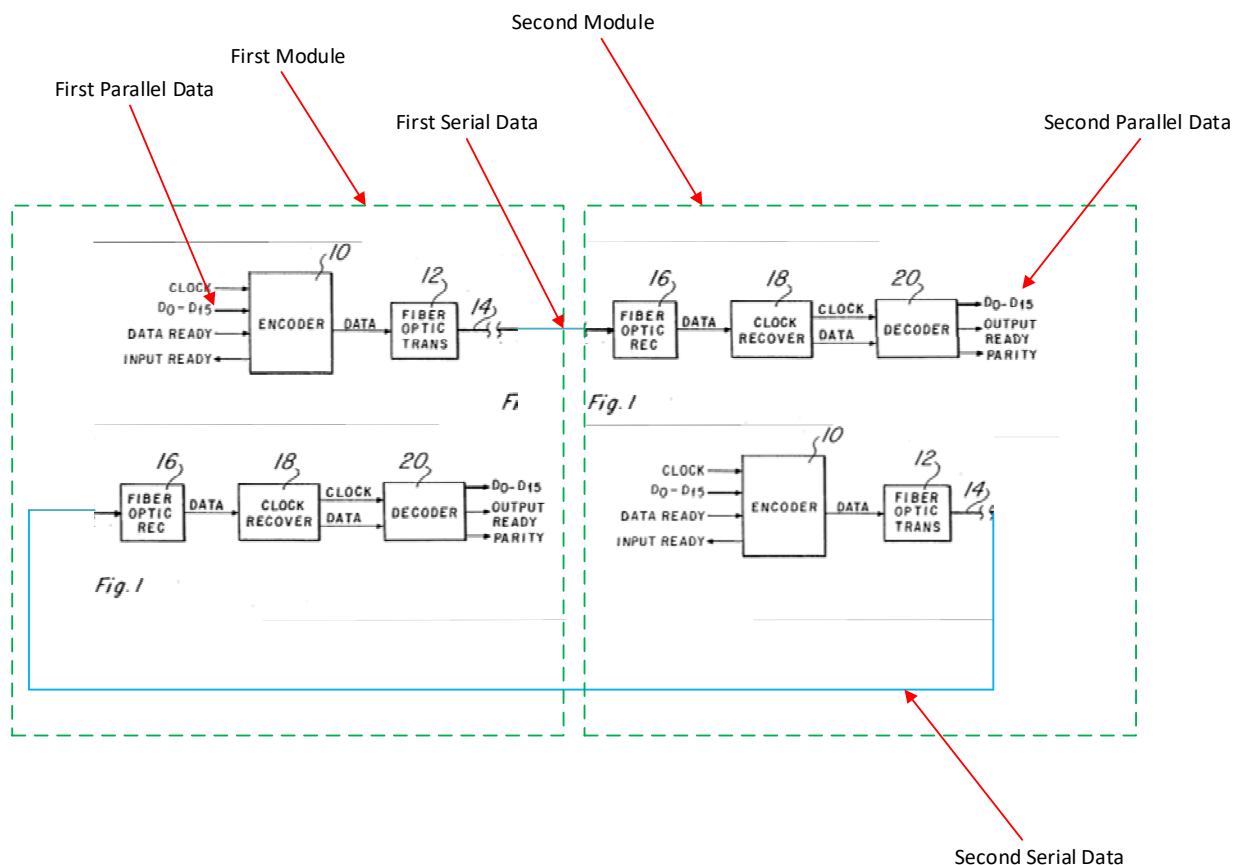
asynchronously, serially receiving second serial data, corresponding to second parallel bus data, from the second module using the serial link; and

Bryans discloses that “data is transmitted along a fiber optic cable 14 to a fiber optic receiver 16. EX. 1006, at col. 2:15-16. As noted above, this data reception is “preferably operated asynchronously” (EX. 1006, at col. 2:42) and thus the data received at the fiber optic receiver is received asynchronously. EX. 1007, at ¶ 68.

The received data is disclosed as corresponding to “second parallel bus data.” EX. 1007, at ¶ 69. Bryans discloses a decoder configured to convert the received “serial data into parallel form, and outputs it on data lines D₀ - D₁₅.” EX. 1006, at col. 2:20-22. The received data is therefore converted back into its original parallel form, and therefore corresponds to second parallel bus data. EX. 1007, at ¶ 69.

FIG. 1 of Bryans, on its face, describes the above elements of claim 1. FIG. 1, however, is drawn with the general concept of a transmitter portion of a device and a receiver portion of the device, with the break in line 14 separating the transmit portion of a device from the receive portion of the device. EX. 1007, at ¶ 63. A PHOSITA would have known that Bryans discloses multiple devices with the transmit and receive functionality shown in FIG. 1. EX. 1007, at ¶¶ 63-64. Specifically, to achieve the stated functionality of the serial communications link of FIG. 1 of facilitating “transmitting data between two parallel devices,” the parallel devices must each include transmission and reception circuits. *Id.*; see also, EX. 1006, at col. 2:4-5. In fact, Bryans explains that the “encoding and decoding functions can be easily implemented on a single integrated circuit for each function.” EX. 1006, at col. 1:43-45. The integration of encoding and decoding functions on the same integrated circuit discloses that parallel devices described in Bryans include all components of FIG. 1. EX. 1007, at ¶ 64.

To further illustrate this disclosure, a modified version of FIG. 1 of Bryans below shows the circuitry of the two parallel devices described in Bryans. *Id.* at ¶ 65.

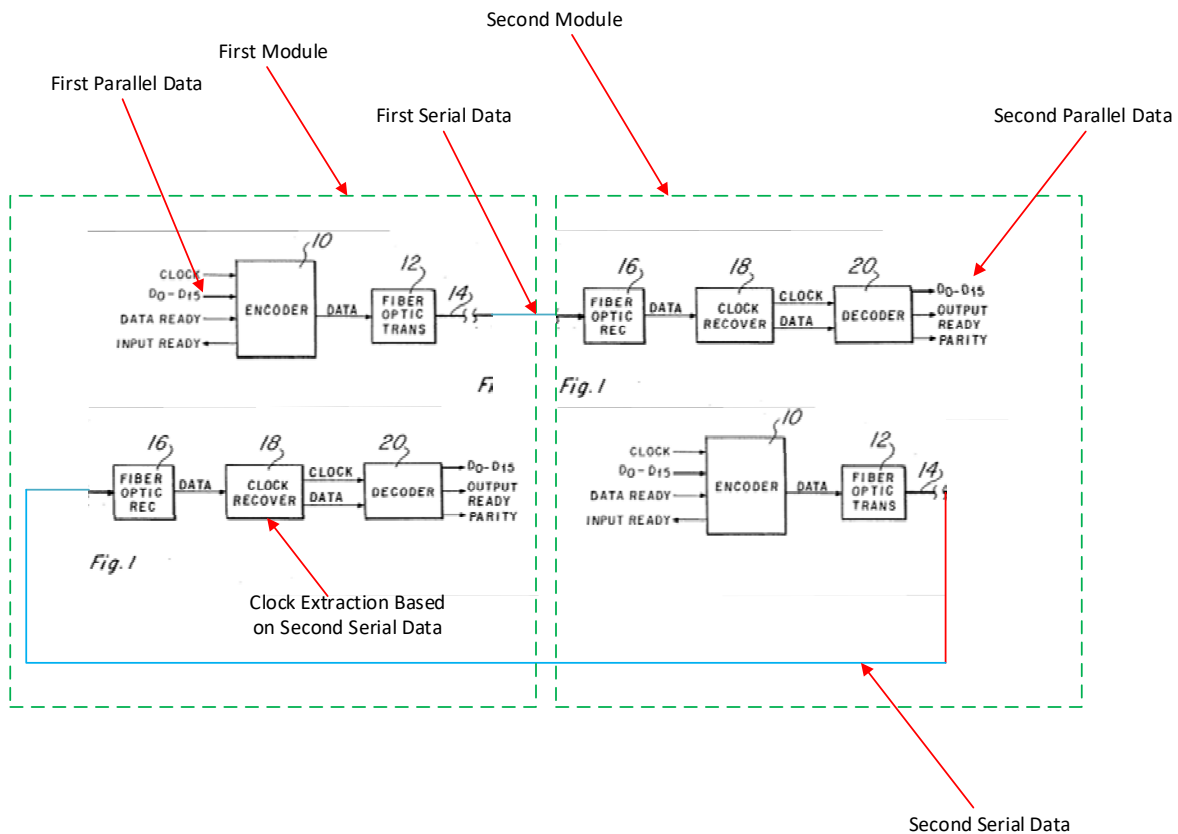


Bryans FIG. 1 (Annotated and modified to show described parallel devices)

generating a first clock signal, for use by the first module, using the second serial data.

Bryans discloses this element, stating that the fiber optic receiver 16 “presents digital data to a clock recover circuit 18. The clock recover circuit 18 extracts the clock from the data itself and presents both the CLOCK and the DATA

signals to a decoder circuit 20.” EX. 1006, at col. 2:17-20. Applying the construction of this claim limitation set forth above, Bryans’ clock receiver circuit 18, as described above, **generates** or **produces** the clock signal by extracting it *from* (i.e., *using*) the received serial data (i.e., second serial data). EX. 1007, at ¶ 72 (emphasis added). Bryans’ extraction of the clock from the received data and providing of the clock signal to the decoder of the receiving device (i.e., first module) discloses “generating a first clock signal, for use by the first module, using the second serial data.” EX. 1007, ¶¶ 72-75. Again, modified FIG. 1 of Bryans, below, illustrates the disclosure of this element of claim 7.



Bryans FIG. 1 (Annotated and modified to show described parallel devices)

In summary, as explained above, Bryans discloses each element of claim 7 and therefore anticipates claim 7.

C. Ground 3: Onno Anticipates Claim 7

As explained below, Onno (EX 1005) anticipates claim 7.

7. A method comprising:

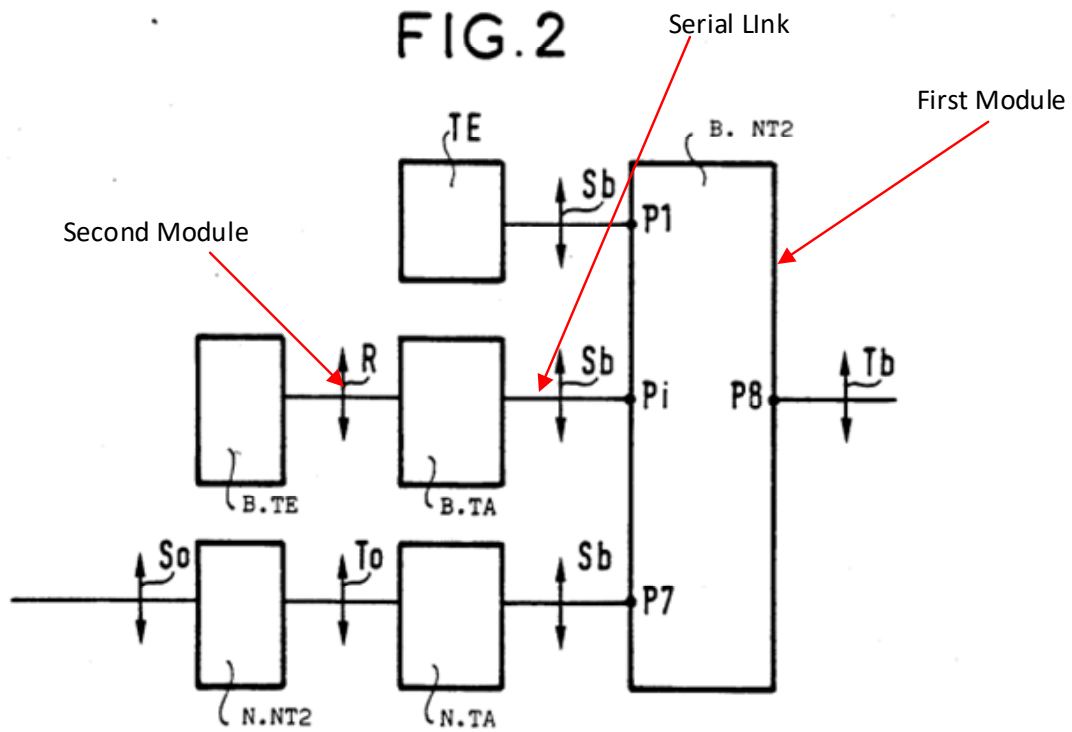
asynchronously, serially transferring first serial data, corresponding to first parallel bus data, from a first module to a second module using a serial link;

Onno discloses a method by describing a processor configured to perform actions and various operations. EX. 1007, at ¶ 77. Onno further discloses that “an

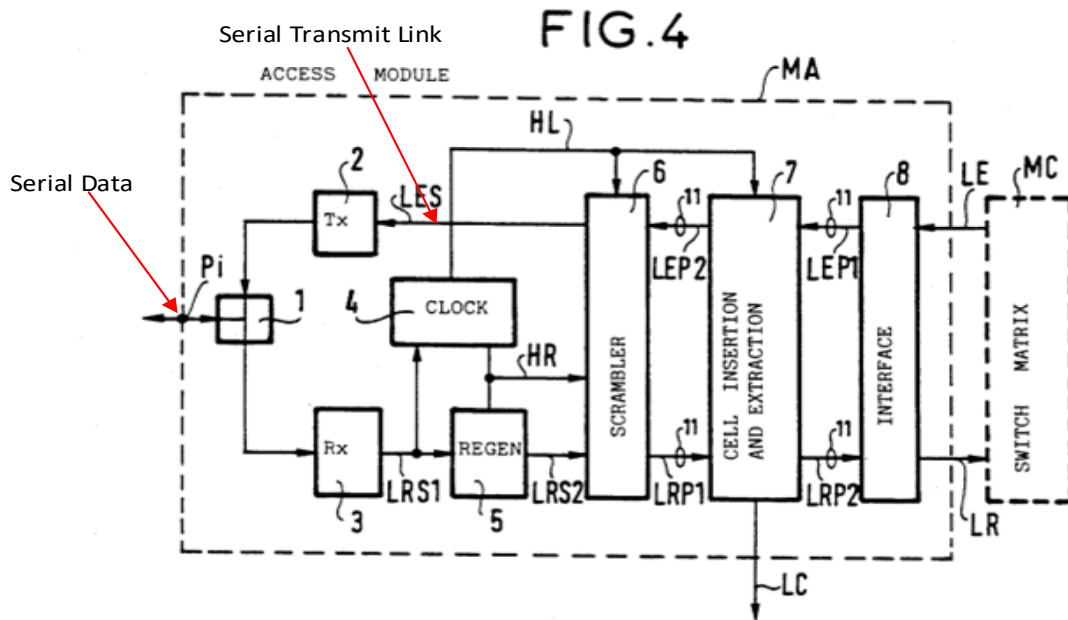
object of the invention is to provide a subscriber installation based on asynchronous transfer mode.” EX. 1005, at col. 1:42-43. Furthermore, in Onno’s description of FIG. 2 (annotated below) the multiple connections shown in FIG. 2 are “asynchronous optical interface Tb and Sb. . . .” EX. 1005, at col. 2:51-55. Onno, accordingly discloses transferring data “asynchronously.” EX. 1007, at ¶ 78.

Onno further discloses the claim step of “serially transferring first serial data.” EX. 1007 at ¶ 79. As disclosed in Onno, the input port “Pi is connected to an optical interface Sb or Tb. The optical interfaces Sb or Tb use a monomode optical fiber for transmission in both directions, . . .” EX. 1005, at col. 3:43-46. Onno further discloses that the “port Pi is connected to an optical duplexer 1, itself connected to an optical transmitter 2 and an optical receiver 3.” EX. 1005, at col. 4:7-9. The optical transmitter 2 is further disclosed as being coupled to “a serial transmit link LES.” EX. 1005, at col. 4:22, FIG. 2. Thus, a PHOSITA would have understood that the optical transmitter transmits first serial data provided over the serial transmit link LES. EX. 1007, at ¶ 79. Onno discloses “asynchronously, serially transferring first serial data, from a first module to a second module using a serial link.” EX. 1007, at ¶¶ 78-80.

Annotated Onno Figures. 2 and 4, below, further illustrate Onno’s disclosure of “serially transferring first serial data . . . from a first module to a second module using a serial link,” as described above.

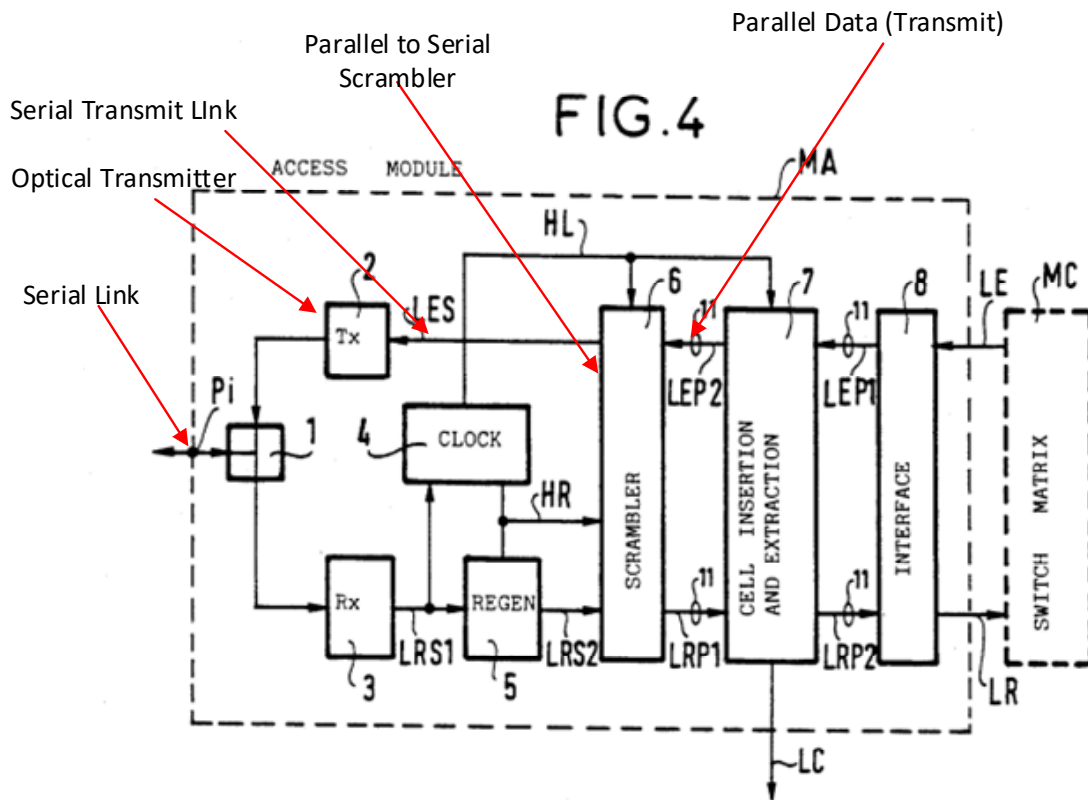


Onno FIG. 2 (Annotated)



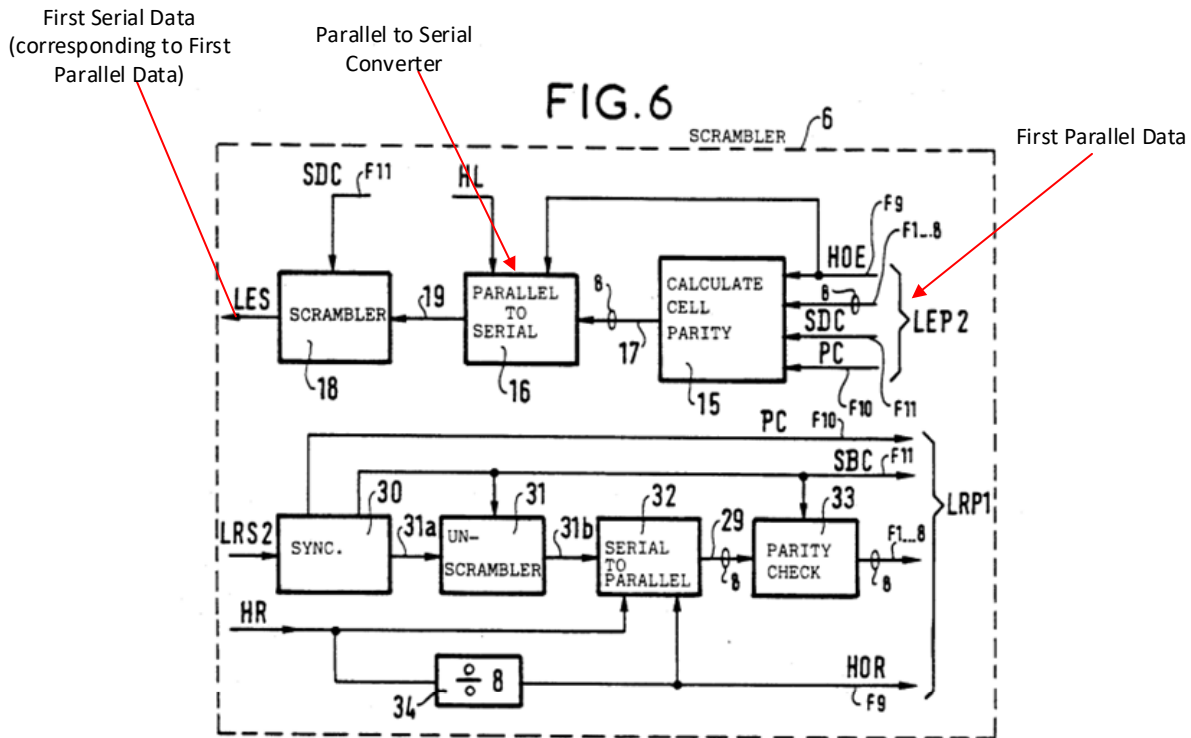
Onno FIG. 4 (Annotated)

Onno further discloses that the serially transferred first serial data corresponds “to first parallel bus data,” as claimed. Specifically, Onno discloses an “extract circuit 7 for inserting and extracting signaling cells [that] is connected to the parallel-series scrambler 6 by a parallel transmit link LEP2.” EX. 1005, at col. 4:26-31. The parallel-series scrambler discloses serializing parallel data to be output on the serial link Pi. EX. 1007, at ¶ 82. This is made clear in Onno, which states that the “parallel-series circuit 6 for scrambling is connected to the optical transmitter 2 via a serial transmit link LES. . . .” EX. 1005, at col. 4:20-23. This is readily apparent in view of annotated FIG. 4 (below), which illustrates that the parallel transmit link LEP2 provides parallel data to the parallel-series scrambler 6 which outputs data on the serial transmit link LES to the optical transmitter 2.



Onno FIG. 4 (Annotated)

FIG. 6 of Onno is further instructive, with the associated disclosure stating that the parallel-serial scrambler circuit 6 includes a “transmit path . . . constituted by a cell parity calculating circuit 15 having its input connected to the parallel transmit link LEP2, a parallel serial converter circuit 16 connected by a link 17 to the output from the circuit 15 . . . and a scrambler circuit 18 . . . whose output is connected to the serial transmit link LES. . . .” EX. 1005, at col. 5:6-15. Annotated FIG. 6, below, illustrates that the first serial data output to the serial transmit link LES corresponds to “first parallel bus data,” as claimed. *See* EX. 1007, at ¶¶ 83-84.



Onno FIG. 6 (Annotated)

Accordingly, Onno discloses “asynchronously, serially transferring first serial data corresponding to first parallel bus data, from a first module to a second module using a serial link.”

asynchronously, serially receiving second serial data, corresponding to second parallel bus data, from the second module using the serial link; and

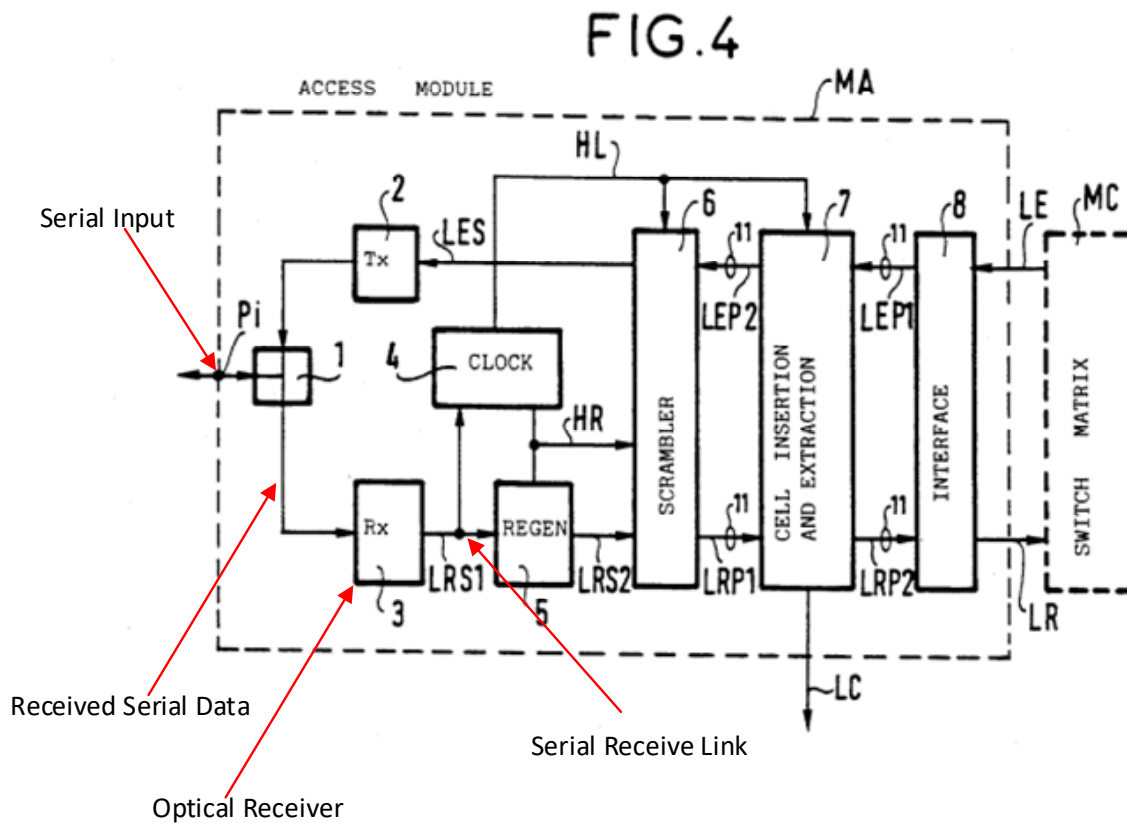
As noted above, Onno discloses that “an object of the invention is to provide a subscriber installation based on asynchronous transfer mode.” EX. 1005, at col. 1:42-43. Furthermore, Onno discloses that the broadband digital network terminal B.NT2 includes connection means which “are asynchronous optical interfaces Tb

and Sb. . . .” EX. 1005, at col. 2:51-55. A PHOSITA would have understood that data received over optical Tb and Sb would therefore be received “asynchronously.” EX. 1007, at ¶ 87.

Onno discloses “serially transferring first serial data.” Onno explains that the representative port Pi “is connected to an optical duplexer 1, itself connected to an optical transmitter 2 and an optical receiver 3 . . . [and] a clock signal from the data in the receive direction, with the clock module being connected to a serial receive link LRS1 at the output from the optical receiver 3.” EX. 1005, at col. 4:7-16 (emphasis added). A PHOSITA would have understood that the optical receiver 3 receives serial data (i.e., second serial data), which is then provided to the serial receive link LRS1. EX. 1007, at ¶ 88.

Annotated FIG. 4 of Onno, below, provides further evidence as to the disclosure of “serially receiving first serial data,” illustrating the path of the received serial data described above.

Parallel Data (Transmit)

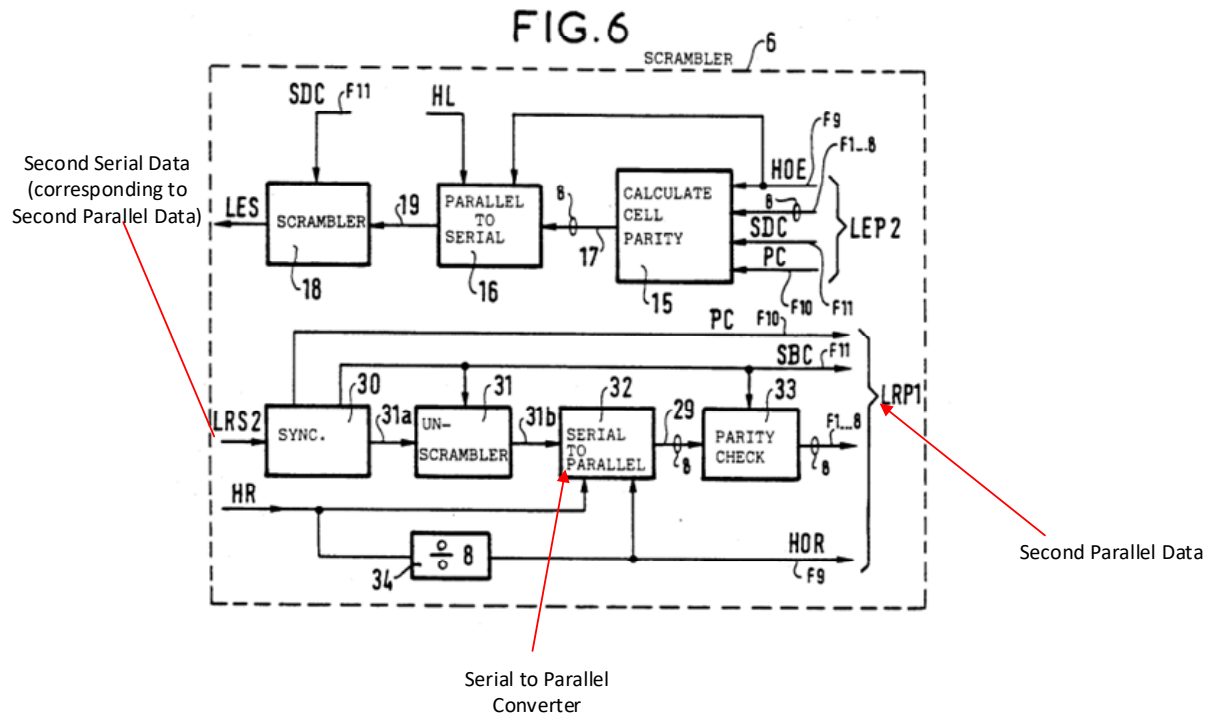


Onno FIG. 4 (Annotated)

Onno further discloses that the received serial data is “corresponding to second parallel bus data.” The broadband digital network terminal B.NT2 (first module) is described as including a serial-parallel converter circuit within scrambler circuit 6. See EX. 1005, at col. 4:26-31. The scrambler circuit is described as including a “transmit path and a receive path.” EX. 1005, at 5-7. The “receive path is constituted by a synchronization circuit 30 for searching for and verifying synchronization having its input connected to the serial receive link LRS2, an unscrambler circuit 31 connected via an input link 31a to the

synchronization circuit 30, a serial-parallel converter circuit 32 connected via a link 31b to the output from the unscrambler circuit 31, and a parity check circuit 33 connected to the output of the serial-parallel converter 32 via a parallel link 29 and having its output connected to the eight data wires F1 . . . 8 of the parallel receive link LRP1.” EX. 1005, at col. 5:19-29. This discloses that second parallel bus data is extracted from the received serial data using the serial-parallel converter 32. EX. 1007, at ¶ 92.

Annotated FIG. 6, below, further illustrates received serial data being provided on receive serial link LRS2, converted by serial to parallel circuit 32, and output as second parallel data on LRP1. As the received data is converted to parallel data, a PHOSITA would have understood that the received serial data was converted from parallel data to serial data by the transmitting device, thus needing to be reconstructed as parallel data by the digital network terminal B.NT2. EX. 1007, at ¶ 92.



Onno FIG. 6 (Annotated)

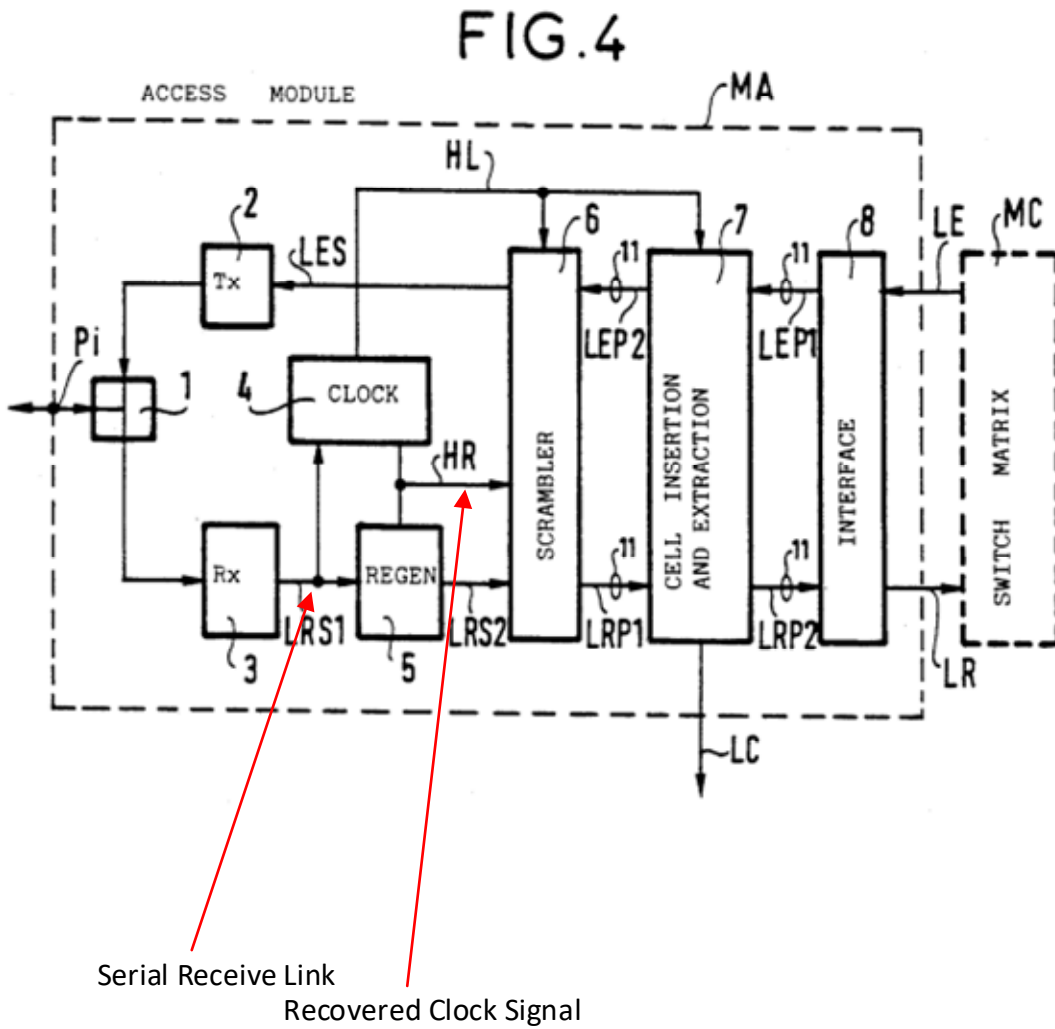
Onno therefore discloses “asynchronously, serially receiving second serial data, corresponding to second parallel bus data, from the second module using the serial link.”

generating a first clock signal, for use by the first module, using the second serial data.

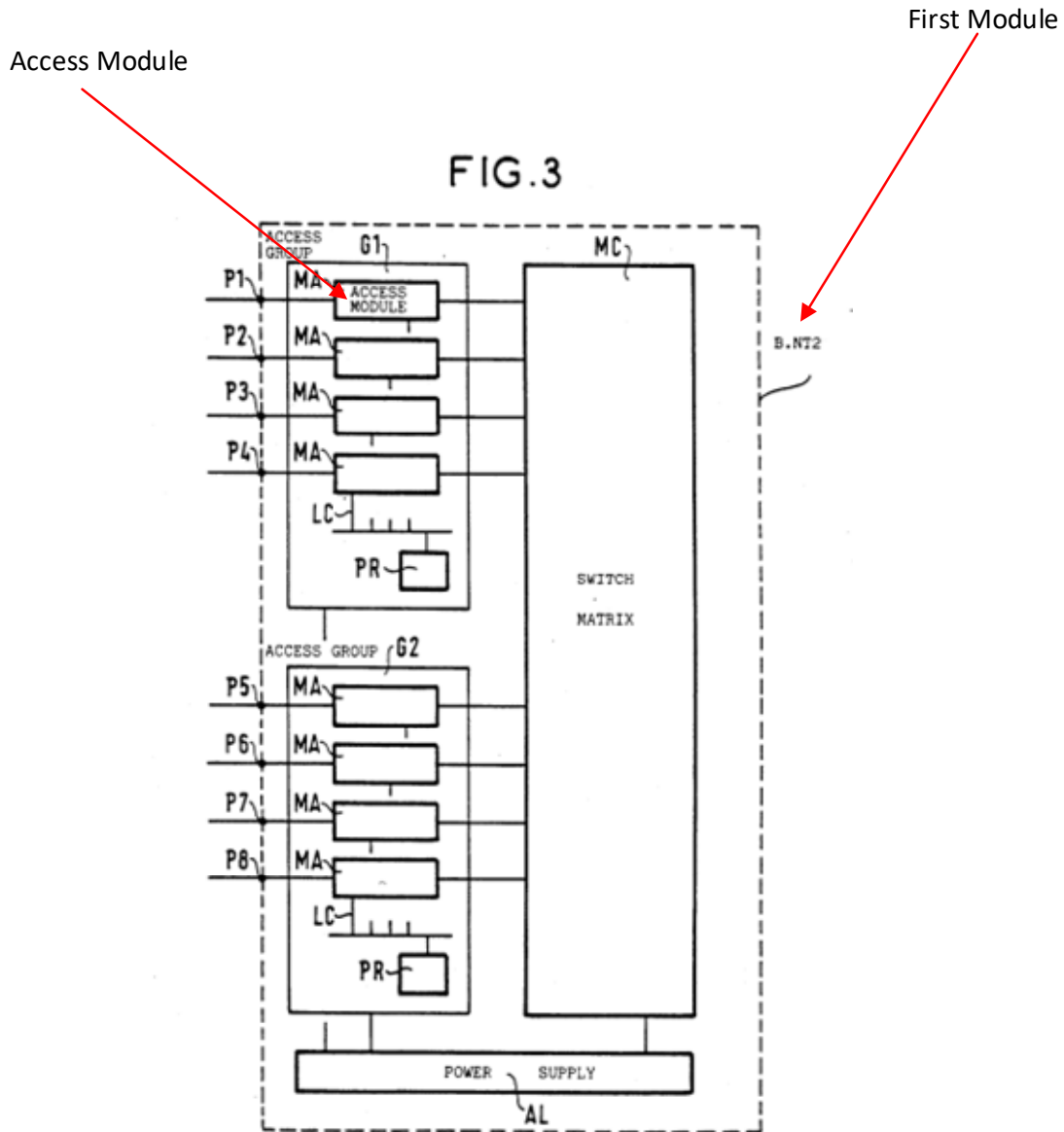
Onno discloses that a “clock module 4 generates a local clock signal HL at the data rate for the transmission direction (600 Mbit/s, 150 Mbit/s, or 10 Mbit/s) and it recovers a clock signal [HR] from the data in the receive direction.” EX. 1005, at col. 4:11-15 (emphasis added); *id.*, at col. 5:24-25. As noted above, the data in the receive direction discloses the claim second serial data. Applying the

construction of this claim limitation set forth above, Onno's clock module 4, as described above, **generates** or **produces** clock signal HR by recovering it *from* (i.e., *using*) data in the receive direction (i.e., second serial data), and therefore discloses "generating a first clock signal . . . using the second serial data," as claimed. EX 1007 at ¶ 96 (emphasis added)..

Further, the "serial-parallel converter 32 receives the recovered clock signal HR" as shown in annotated FIG. 4, below. The access module MA, shown in FIG. 4, below, is one of the components within B.NT2 (the first module), as shown in FIG. 3, below. Onno states that "B.NT2 comprises a switching matrix MC, two access groups G1 and G2, and a power supply AL. Each access group includes four access modules MA each connected via a control link LC to a processor PR which acts as a local controller," EX. 1005, at col. 3:23-27. This discloses that the recovered clock signal is used on the first module, B.NT2. EX 1007 at ¶ 97.



Onno FIG. 4 (Annotated)



Onno FIG. 3 (Annotated)

In summary, as explained above, Onno discloses each element of claim 7 and therefore anticipates claim 7.

VIII. TRIAL SHOULD BE INSTITUTED

The related district court litigation, *Shamrock Innovations, LLC v. Lenovo (United States), Inc.*, Case No. 5:22-cv-00102 (E.D. N.C.) (“Litigation”), does not warrant discretionary denial of institution under § 314(a). *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 5-6 (Pat. Tr. & App. Bd. Mar. 20, 2020) (precedential).

A. Factor 1: Either Party May Request a Stay

The first *Fintiv* factor weighs against discretionary denial of institution. Either party may request a stay of the Litigation pending the institution decision.

B. Factor 2: Proximity of Trial Date

The second *Fintiv* factor also weighs against discretionary denial of institution. The current median time from filing to trial (civil only) in the U.S. District Court for the Eastern District of North Carolina is 36.5 months. *See* U.S. District Courts – Federal Court Management Statistics, December 31, 2022, at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distprofile1231.2022.pdf, page 21. Although a stay of the Litigation deadlines pending Petitioner Western Digital’s motion to intervene was recently lifted, a final written decision would be issued before an estimated district court trial date in April 2025. Thus, the Board is the most efficient venue to make a binding determination on the invalidity of claim 7 of the ’675 patent.

C. Factor 3: Petitioner’s Diligence and Investment in IPR Outweighs the Parties’ Minimal Investment in Litigation

The third *Fintiv* factor also weighs against discretionary denial of institution. To date, the parties have not invested considerable resources in the Litigation, as the case is still at an early stage. Claim construction briefs have not yet been filed, a *Markman* hearing has not been held, only one named inventor has been deposed, minimal fact discovery has taken place, and expert discovery has not yet started. The court has not yet considered infringement or invalidity.

D. Factor 4: Overlap Will Be Avoided

The fourth *Fintiv* factor also weighs against discretionary denial of institution. If IPR is instituted, Petitioner will not pursue in the Litigation the same grounds as in the Petition, thus avoiding overlap.

E. Factor 5: Institution Would Promote Judicial Efficiency

Under the fifth *Fintiv* factor, all parties to this proceeding are included in the related proceedings. WD, Shamrock, and Lenovo (United States), Inc., are all parties to the Litigation, now that WD’s motion to intervene has been granted. These facts do not weigh against institution because the Board’s FWD would cancel the asserted claim or bind Petitioner with estoppel if Petitioner’s challenge is unsuccessful. As such “this factor does not weigh against exercising [the Board’s] discretion to deny.” *Cast Lighting, LLC v. Wangs Alliance Corp.*, PGR2021-00012, Paper 12 at 36 (Pat. Tr. & App. Bd. June 7, 2021).

F. Factor 6: The Merits Strongly Favor Institution

The sixth *Fintiv* factor weighs against discretionary denial of institution, as the merits of the case are strong enough to outweigh any inefficiencies borne of parallel litigation and institution would promote the AIA's objectives of providing an efficient alternative to litigation for claims that Shamrock has asserted.

Overall, all *Fintiv* factors either weigh against or do not warrant discretionary denial of institution here. Petitioner respectfully requests the Board institute this IPR.

IX. NON-INSTITUTION UNDER § 325(D) WOULD BE IMPROPER

This IPR should be instituted under the *Advanced Bionics* test for § 325(d) discretion because the evidence identified in this Petition was neither before the Office nor fully considered during prosecution. *See Advanced Bionics, LLC v. MEDEL Elektromedizinische Gerate GmbH*, IPR2019-01469, Paper 6, at 6–11 (Pat. Tr. & App. Bd. Feb. 13, 2020) (precedential).

None of the references relied on in this petition, or substantially the same prior art references, were before the USPTO during examination of the '675 patent. *See* EX1001, 1-2 (identifying art of record). Accordingly, each ground presented in this Petition alone is sufficient to find the first prong of the *Advanced Bionics* test not satisfied. *See Thorne Research, Inc. v. Tr. of Dartmouth Coll.*, IPR2021-00491, Paper 18, at 8–9 (Pat. Tr. & App. Bd. Aug. 12, 2021) (using a reference that

discloses new or additional subject matter may prevent the Board from finding the art to be substantially the same).

Moreover, the references relied up on in this Petition are not cumulative over the art cited during prosecution. In addition, the Examiner did not have the benefit of any expert declaration, like the declaration of Petitioner's expert Dr. Caloyannides (EX 1007), which explains the teachings of the prior art and what a PHOSITA would have understood from the asserted references as of Patent Owner's earliest possible priority date.

Accordingly, any argument for non-institution under § 325(d) should be rejected.

X. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(A)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Petitioner Western Digital Technologies, Inc. and Western Digital Corporation, both Delaware corporations, are real parties-in-interest. Lenovo (United States), Inc., a Delaware corporation, is also a real party-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any disclaimer or reexamination certificates for the '675 patent. As noted above, the '675 patent is currently the subject of the following pending lawsuit: *Shamrock Innovations, LLC v. Lenovo (United States), Inc.*, Case No. 5:22-cv-00102 (E.D. N.C.) ("Litigation"). Shamrock filed its

original complaint alleging infringement of the '675 Patent and related U.S. Patent No. 9,535,454 by Lenovo (United States), Inc. on March 21, 2022, and effectuated service on Lenovo on April 13, 2022. The Court recently granted WD's motion to intervene as a defendant in the Litigation. A decision on this Petition may impact the Litigation.

Additional lawsuits involving the '675 patent and related U.S. Patent No. 9,535,454 and different defendants include:

Shamrock Innovations, LLC v. HP Inc., Case No. 1:21-cv-00222 (W.D. Tex.), dismissed.

Shamrock Innovations, LLC v. Acer America Corporation et al., Case No. 6:20-cv-00696 (W.D. Tex.), dismissed.

C. Lead and Back-Up Counsel and Service Information Under 37 C.F.R. § 42.8(b)(3)-(4)

Petitioner provides the following designation of counsel.

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XI. PAYMENT OF FEES – 37 C.F.R. § 42.103

Petitioner authorizes the USPTO to charge Deposit Account No. 133080 for the fee set forth in 37 C.F.R. § 42.15 for this Petition and further authorizes payment for any additional fees to be charged to this Deposit Account.

XII. CONCLUSION

Claim 7 of the '675 patent is unpatentable over the prior art references set forth herein. Had any of these references been considered by the USPTO, claim 7 of the '675 patent would not have been allowed. Considering the art and argument presented above and underlying evidence, it is reasonably likely that the Board will

find claim 7 of the '675 patent unpatentable. Therefore, Petitioner respectfully requests that the Board grant this Petition and cancel claim 7.

Respectfully submitted,

Dated: March 21, 2023

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CERTIFICATE OF WORD COUNT UNDER 37 CFR §42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 7,292 words, according to the word-processing system used to prepare this Petition, excluding the words in the Table of Contents, Table of Authorities, Mandatory Notices, Certification Under 42.24(d), Certificate of Service, appendix of exhibits or claim listing, as set forth in 37 CFR § 42.24(a)(1).

Dated: March 21, 2023

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) et seq. and 42.105(a), the undersigned certifies that on March 22, 2023, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

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Dated: March 21, 2023

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