

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.
Petitioner

v.

SHAMROCK INNOVATIONS, LLC,
Patent Owner.

Case IPR2023-_____
Patent No. 8,060,675

DECLARATION OF MICHAEL CALOYANNIDES, PH.D.

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	QUALIFICATIONS	1
III.	SUMMARY OF OPINIONS	4
IV.	OVERVIEW OF THE TECHNOLOGY OF THE ‘675 PATENT AND THE STATE OF THE ART	4
V.	OVERVIEW OF THE PRIOR ART	7
	A. U.S. Patent No. 4,450,572 (“Stewart”) (Ex.1004)	8
	B. U.S. Patent No. 4,979,185 (“Bryans”) (Ex.1006)	9
	C. U.S. Patent No. 5,170,272 (“Onno”) (Ex.1005)	11
VI.	LEVEL OF ORDINARY SKILL IN THE ART	14
VII.	CLAIM CONSTRUCTION	15
	A. “Generating a first clock signal . . .”	15
VIII.	UNPATENTABILITY OF CLAIM 7 OF THE ‘675 PATENT	16
	A. Ground 1: Claim 7 in view of Stewart	17
	B. Ground 2: Claim 7 in view of Bryans	28
	C. Ground 3: Claim 7 in view of Onno.....	36
IX.	CONCLUSION.....	54

I, Michael Caloyannides, Ph.D., declare as follows:

I. INTRODUCTION

1. I have been retained by Western Digital Technologies, Inc., (“Petitioner” or “WD”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office regarding U.S. Patent No. 8,060,675 (“the ’675 patent”), which I understand is labeled as Ex. 1001. I have been asked to consider whether certain prior art references disclose the features recited in claim 7 of the ’675 patent. My opinions and the bases of my opinions are set forth below.

2. I am being compensated at my normal hourly consulting rate for the time I spend on this matter. No part of my compensation is dependent on the outcome of this proceeding. I have no other interest in this proceeding.

II. QUALIFICATIONS

3. I am an expert in the field of electrical engineering and digital communication and protocols. My entire professional life lasting over fifty years this far has concentrated on the overarching technologies underlying the ’675 patent, namely signal processing. The Thesis for my Ph.D. degree in Electrical Engineering, awarded to me by Caltech, was on a theoretical and experimental investigation of receiver noise and its effect on telecommunications. I was also awarded a Ph.D. “subject minor” by Caltech in Applied Mathematics. Even before

that, as a teenager, I had designed and built signal processing electronics for a high-power transceiver with which I communicated across the world.

4. Upon graduation I was employed for 14 years at top technical levels in Private Industry (e.g., Boeing Corp.) where I applied my education to advanced military telecommunications projects for the US Department of Defense and the Intelligence Community. During that time, I was also awarded a U.S. Patent in high-speed digital signal processing. I was subsequently hired by the CIA as senior scientist for its Office of Research and Development where, for 14 years, I led numerous classified projects in signal processing, both analog and digital; in that capacity I was awarded the highly competitive Scientist of the Year Award, as well as 5 separate Exceptional Accomplishment Awards and also the Meritorious Officer Award. One of my tasks was to design the architecture of a complete National Signals Interception (“SIGINT”) system for a nation that was then a U.S. ally.

5. When the Cold War ended, I returned to Private Industry in technical leadership positions in signal processing as Chief Scientist (at Ideal Innovations Inc.) and later as Senior Fellow (at Mitretek Systems, a spinoff from the MITRE Corp.), and I also accepted appointments as Adjunct Faculty, first at George Washington University and then at Johns Hopkins University where I taught digital signal processing to graduate school students studying for their advanced degrees.

In that capacity I was awarded the Excellence in Teaching Award by Johns Hopkins University. At the same time, I authored two textbooks in digital signal processing, as well as countless peer-reviewed technical papers; In addition, I was a monthly columnist for the IEEE's Security and Privacy Magazine for its entire first year of publication.

6. Upon retiring from private industry, I applied my experience in serving as an expert witness in well over a hundred intellectual property cases, the majority of which were on signal processing algorithms, techniques, processing, and applications; these included the reception and processing of GPS signals, point-to-point wireless links, and extraction of very weak signals from background noise, 3G, 4G, 5G cellular communications, Covert Communications, and other applications. Before any commercial cellular service became available in the US, I designed, fabricated and operated my own small-scale cellular telephone system which allowed me to place and received telephone calls over the Los Angeles Basin.

7. In light of all of the foregoing, I believe that I am well qualified to assess and opine authoritatively on the subject matter of the '675 patent, which deals with a subset of signal processing.

8. A true and correct copy of my curriculum vitae is provided, and I understand that it will be labeled as Exhibit 1008.

III. SUMMARY OF OPINIONS

9. The opinions in this Declaration are based on the documents I have reviewed and my knowledge and professional judgment. In forming my opinions, I reviewed each of the publications that I discuss.

10. My opinions are based upon how a person having ordinary skill in the art (“PHOSITA”) would have understood the claims of ’675 patent, the prior art, and the state of the art at the time of the alleged invention, which I understand to be on or around August 6, 1998.

11. I have been informed that a patent claim is invalid as anticipated if each and every element of a claim is disclosed in a single prior art reference.

12. In my opinion, and as explained in detail below, each of the prior art references I have been asked to review (Stewart, Bryans, and Onno) discloses all elements of claim 7 of the ’675 patent. Thus, as explained below, it is my opinion that each of Stewart, Bryans, and Onno anticipates claim 7 of the ’675 patent.

13. For reference, I attach to this declaration, claim charts that summarize my opinions regarding claim 7.

IV. OVERVIEW OF THE TECHNOLOGY OF THE ’675 PATENT AND THE STATE OF THE ART

14. The ’675 patent generally discloses bridging (i.e., interface or connection) devices for providing serial communication between two parallel data busses. *See, EX. 1001*, at col. 5:13-15.

15. The '675 patent includes 22 claims, including independent claims 1, 7, and 15. I was asked to analyze the patentability of only claim 7. For reference, I have reproduced below claim 7 of the '675 patent:

7. A method comprising:

asynchronously, serially transferring first serial data, corresponding to first parallel bus data, from a first module to a second module using a serial link;

asynchronously, serially receiving second serial data, corresponding to second parallel bus data, from the second module using the serial link; and

generating a first clock signal, for use by the first module, using the second serial data.

EX. 1001, claim 7.

16. Digital data processing equipment are useful primarily if they can communicate data to and from other digital data processing equipment. The oldest and most intuitive of such communication means was an outgrowth of the Morse Code of yesteryear and was serial in nature, i.e., one data bit at a time (dots and dashes). It, in turn, had evolved from ancient optical or audible signals, such as smoke signals or an assortment of sound signals.

17. As data processing equipment evolved to where it could handle a number of bits simultaneously, such as one data symbol at a time where each data symbol conveyed multiple bits of information, serial data buses gave way to parallel data buses handling 8, 16, 32, etc. bits at a time to maximize bandwidth of

the given device. *See e.g., EX. 1006*, at col. 1:9-22. This was known as far back as 1989. *EX. 1006*, at 1. While parallel data communication has higher bandwidth, it is not recommended for use over longer distances. For example, issues such as cost, weight, noise, and electrical loading all must be considered when designing a parallel bus communication link. *See e.g., EX. 1006*, at col. 1: 9-22. Serial communication provides simpler communication between parallel devices. *Id.*

18. To send and receive such data over serial communications channels, such as a pair of wires or a fiber optic cable, it became clear that parallel-to-serial and serial-to-parallel data converters had to be used, and such functional devices rapidly became commonplace during the last half-century. *See, e.g., EX. 1004*, at FIG. 1 (dating back to May 2, 1982); *EX. 1006*, at col. 2:11-22; *EX. 1005*, at col. 5:5-39, FIG. 6. Such devices are nothing more than elementary circuits that handle the conceptually simple tasks of book-keeping to convert, say, an 8-bit symbol (such as an alphanumeric character) to the string of bits (zeroes and ones) that it represents.

19. It is apparent from the foregoing that even in the simplest serial communications channel where only a single bit is communicated at a time, that the receiver needs to know when, during the duration of each bit, the received signal needs to be sampled. In other words, the receiver must be able to know when that received waveform that represents one data symbol should be sampled.

20. There are numerous ways whereby the above-needed metronome-like clock signal can be provided to the serial data receiver: it can be transmitted by the transmitter to the receiver (e.g. in a separate channel or mixed with the information-carrying signal), in some cases it can be inferred by the receiver by studying the incoming data signal, or both the transmitter and the receiver can be synchronized by the equivalent of both watching a conductor conduct the equivalent of an orchestra.

21. As noted above, a clock signal from a transmitting device may be encoded into the serial data string by the transmitting device. *See e.g., EX. 1006*, at col. 2:11-22. *See also, EX. 1004*, at col. 1:53-65; *EX. 1005*, at col. 4:7-40. A receiving parallel device would then include circuitry to extract the data and the encoded clock signal. *See e.g., EX. 1004*; at col. 4:8-16; *EX. 1006*, at col. 2:16-20; *EX. 1005*, at col. 4:11-16.

22. All of these conceptual methods have been described at length for decades in digital communications textbooks.

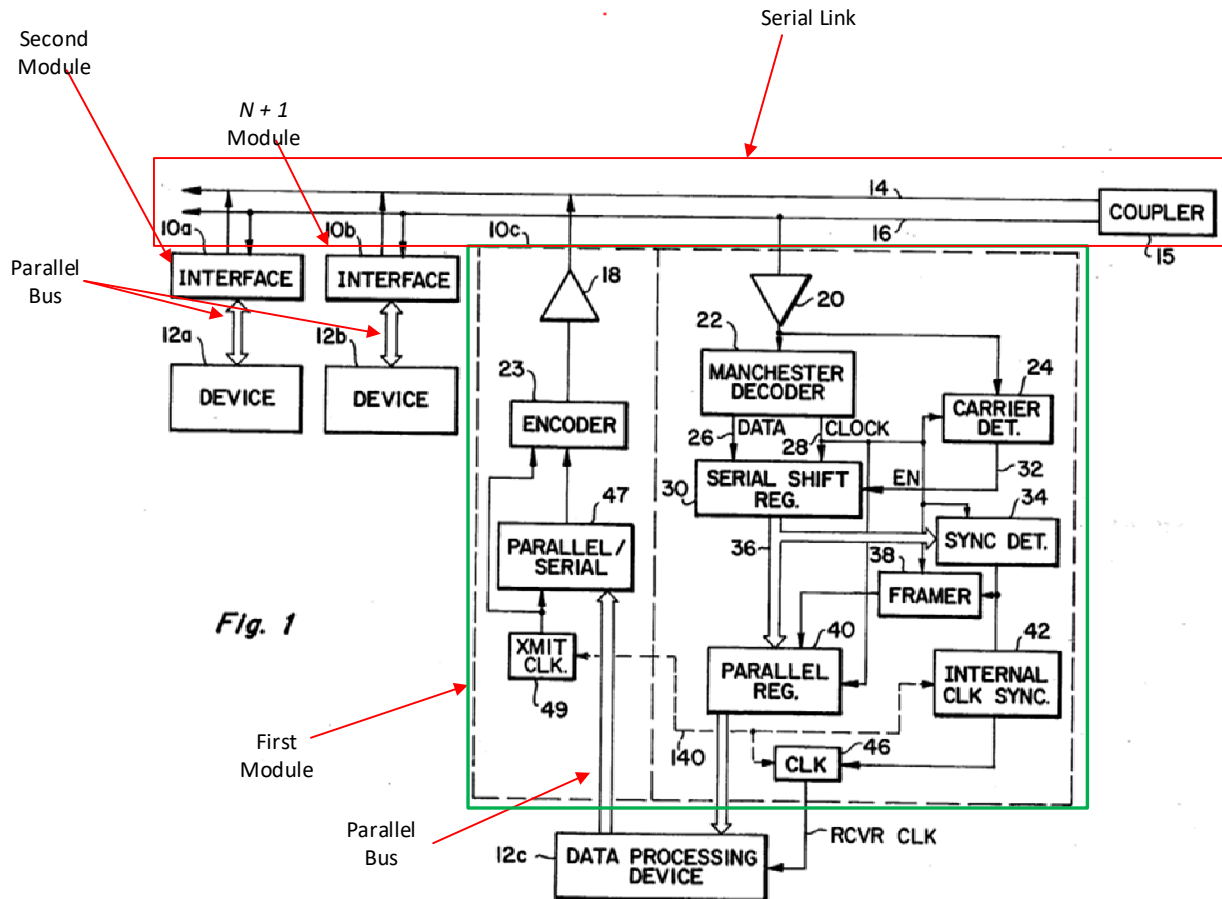
V. OVERVIEW OF THE PRIOR ART

23. I briefly summarize below the prior art patents I was asked to review: Stewart, Bryans, and Onno. All statements regarding a prior art reference's disclosures are made from the perspective of a PHOSITA at the time of the alleged invention.

A. U.S. Patent No. 4,450,572 (“Stewart”) (Ex.1004)

24. Stewart states that an “objective of this invention is to provide an interface for coupling a computer with a data communications link that permits asynchronous bit-serial communications among devices transmitting and receiving Manchester-type codes over a serial information channel.” *Ex. 1004*, col. 2:34-39. Data provided by a device, such as a computer, is converted from a parallel format to a serial format and then transmitted to a target device over a serial communication link. See *id.*, col. 5:9-22. Data provided by a connected device is converted from parallel data to serial data. *Id.* Stewart further states that an interface device receives encoded serial data, which is then converted to parallel data and stored in a parallel register. *Id.*, col. 4, lines 1-35. The received serial data is decoded to extract the data packets and encoded clock signal. *Id.*, col. 4:11-16.

25. The following is an annotated Figure 1 from Stewart that shows the serial links, modules, and interface (bridge) devices as they would have been understood by a PHOSITA.

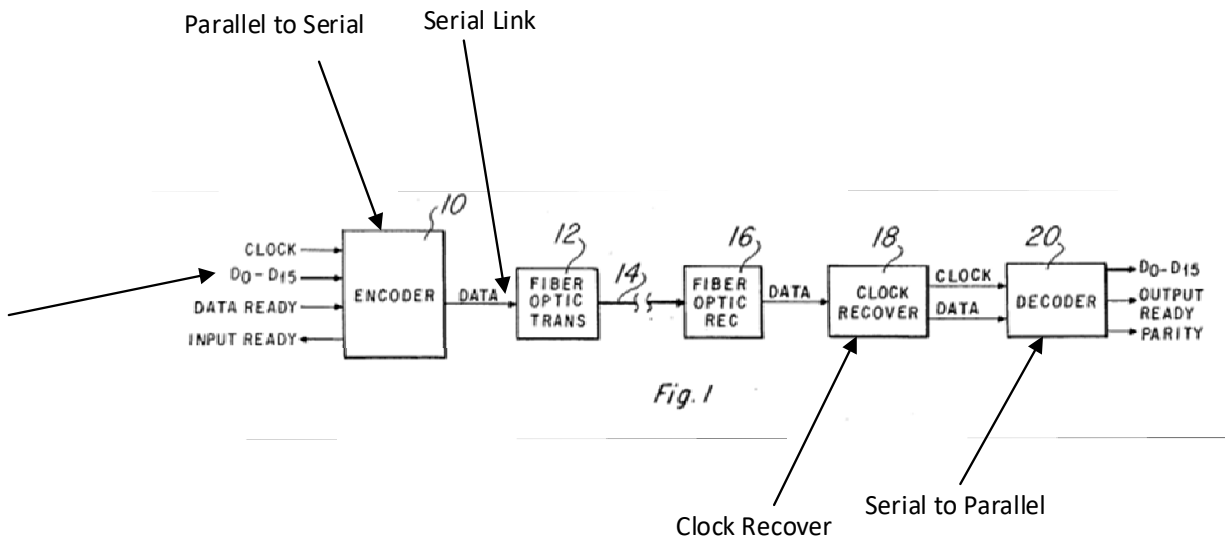


Stewart FIG. 1 (Annotated)

B. U.S. Patent No. 4,979,185 (“Bryans”) (Ex.1006)

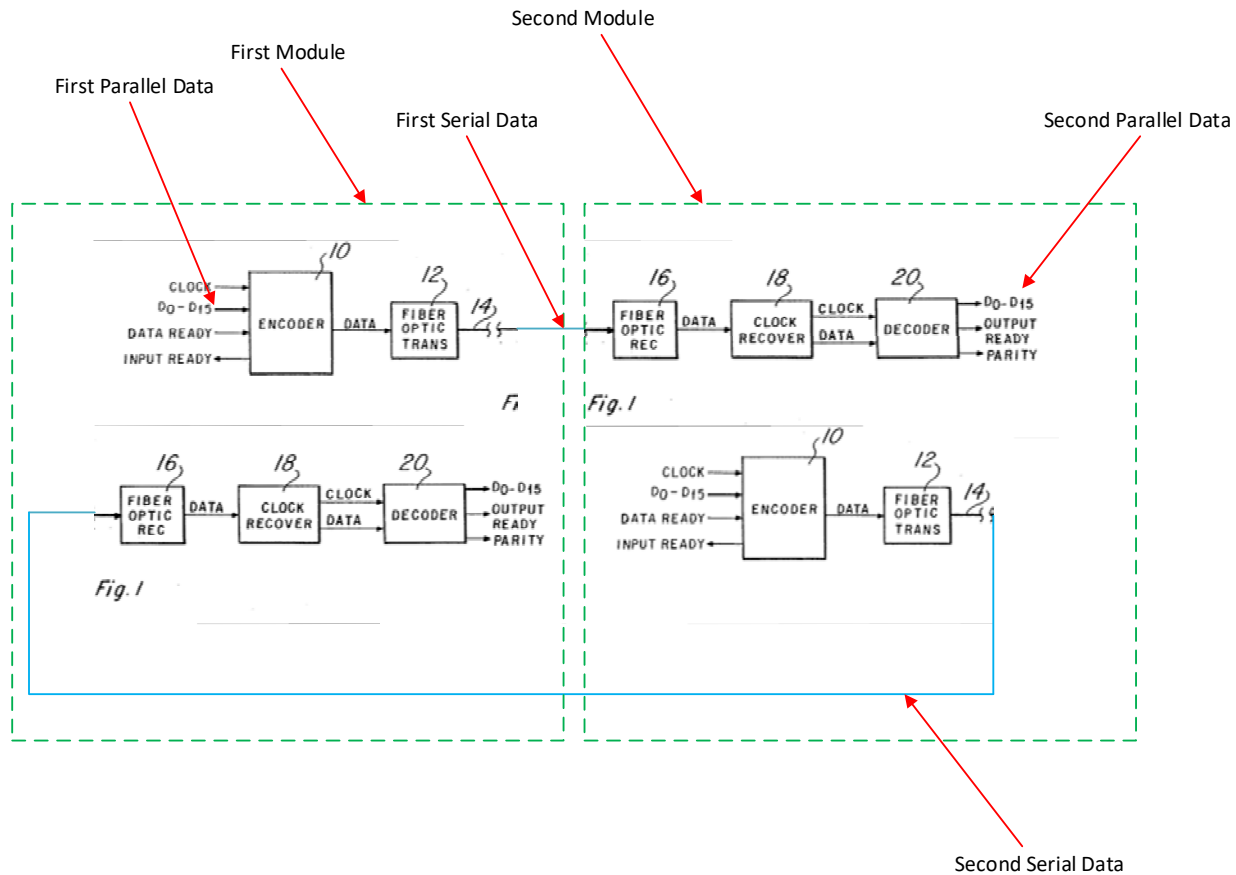
26. Bryans is a patent issued to Texas Instruments Incorporated. *EX. 1006*, at 1. Bryans generally discloses a high bit rate serial link for transmitting data asynchronously between two parallel devices. *EX. 1005*, at col. 2, lines 4-5, 41-44. An encoder converts data from parallel to serial form, and a decoder converts received data back into parallel form. *EX. 1006*, at col. 2:11-22. A clock signal is further extracted from received data by a clock recovery circuit. *EX. 1006*,

at col. 2, lines 18-22. Annotated Bryans Figure 1 illustrates the general architecture of the serial communication link of Bryans as it would have been understood by a PHOSITA.



Bryans FIG. 1 (Annotated)

27. A modified version of Bryans FIG, 1 is shown below to illustrate the parallel devices as they are described in Bryans.



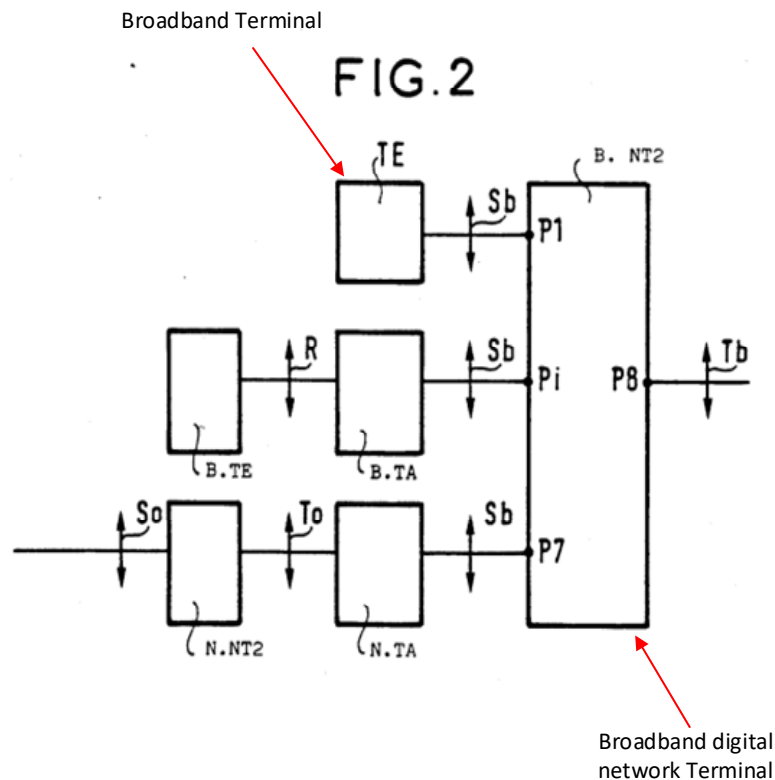
Bryans FIG. 1 (Annotated and modified to show described parallel devices)

28. The specifics of the asynchronous serial data channel (e.g. fiber optic, wire pair, wireless, etc.) are irrelevant to the observation that, as discussed below this prior art presents the same key elements as claim 7 of the '675 patent.

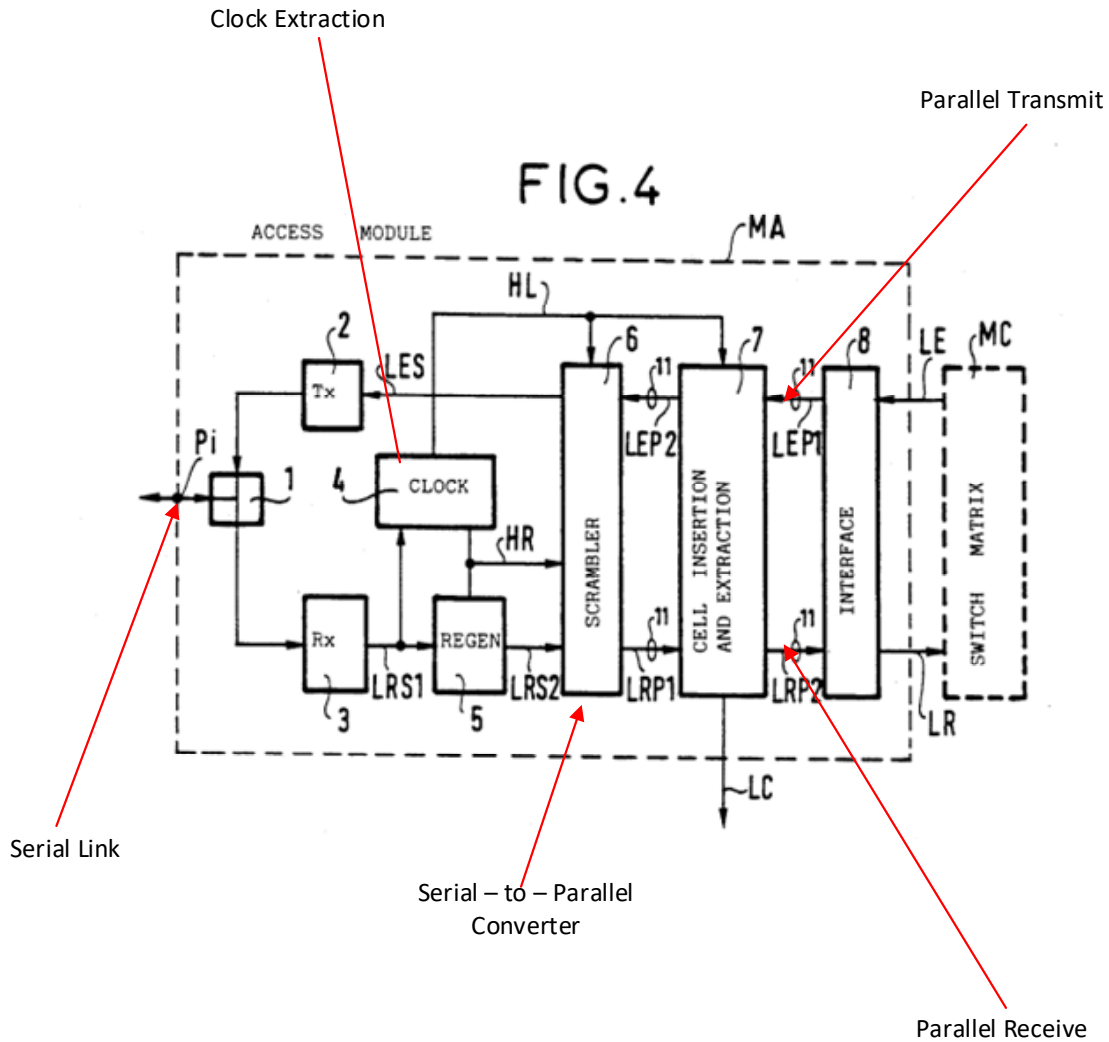
C. U.S. Patent No. 5,170,272 ("Onno") (Ex.1005)

29. Onno is a patent assigned to Alcatel Cit. Ex.1005 at 1. Onno discloses a subscriber terminal installation for an asynchronous network using asynchronous optical interfaces between a digital network terminal and one or more broadband terminals (TE) via broadband adapters (B.TA). EX. 1005 at col. 2:51-66. The

broadband digital network terminal performs serial to parallel conversion of data, and vice versa. *EX. 1005*, at col. 4:20-31. A clock module recovers a clock signal from data received over a serial link. *EX. 1005*, at col. 4:11-16. A PHOSITA would have understood that the serial communication between the broadband terminals and broadband digital network terminals is an asynchronous serial communication of parallel data. Annotated Figures 2 and 4 highlight the general architecture of the Onno system as it would have been understood by a PHOSITA.



Onno FIG. 1 (Annotated)



Onno FIG. 4 (Annotated)

30. As discussed below, this prior art, too, teaches all of the same key elements of claim 7 of the '675 patent, namely parallel-to-serial conversion, followed by asynchronous transmission over a serial link, extraction of clock information from the received data, and conversion back into a parallel bus.

VI. LEVEL OF ORDINARY SKILL IN THE ART

31. I have been asked to assume that the time of the alleged invention of the '675 patent is on or around August 6, 1998. I have applied that timeframe and understanding to my analysis and opinions in this declaration.

32. I have been asked to give my opinion regarding the level of ordinary skill in the art with respect to the '675 patent. To determine the level of ordinary skill in the art, I considered the '675 patent, the technology, the educational level, and experience of persons in the field, the types of problems encountered in the art, prior solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology in the field, observations of implementations in products for sale in the marketplace, and my own education and over half a century of experience in Industry, Government, and Academia summarized earlier in this declaration.

33. Based on these considerations, I believe a person of ordinary skill in the art at the time of the alleged invention of the '675 patent would have had at least a bachelor's degree in electrical engineering, or equivalent, with about three years of professional work experience in serial and parallel data communications within a computing device or system and between different computing devices, systems, or subsystems. More education can supplement practical experience and vice versa.

34. I understand this level of skill in the art and believe I am qualified to opine from the perspective of a person having ordinary skill in the art at the time of the claimed invention.

VII. CLAIM CONSTRUCTION

35. I have been informed that claim terms are typically given their ordinary and customary meaning, as would have been understood by a PHOSITA, at the time of the alleged invention, primarily taking into consideration the language of the patent claims, the specification and prosecution history. I also understand that references such as dictionaries or technical texts may be considered.

A. “Generating a first clock signal . . .”

36. In considering claim construction, I note that the claim term “generating a first clock signal . . .” is not present in the ’675 patent, and thus there is no disclosure to inform its meaning within the specification of the ’675 Patent. Nor is the term present in the ’675 patent’s related applications or patents. I also understand that the patent applicant identified certain portions of its related U.S. Patent Application No. 09/130,058 (now the U.S. Patent No. 6,070,214), at columns 6:33-46, 8:38-53, as support for the addition of this claim limitation during prosecution of the ’675 patent. I have reviewed these cited portions of the

‘214 patent, which does not include the claim limitation at issue, and I do not find it helpful to inform this claim limitation’s meaning.

37. In this particular analysis, however, the language of claim 7 would have provided a PHOSITA information to generally understand the plain meaning of the above term. Specifically, claim 7 recites “generating a first clock signal . . . ***using the second serial data.***” Thus, the generated clock signal is not created out of thin air or in the absence of additional information, but rather, “using the second serial data.” Thus, a PHOSITA would have understood that the creation of a clock signal using received serial data (i.e., second serial data) would include various ways of producing a clock signal, such as by extracting or recovering a clock signal ***from*** (i.e., using) the second serial data.

VIII. UNPATENTABILITY OF CLAIM 7 OF THE ‘675 PATENT

38. I have been asked to evaluate claim 7 of the ‘675 patent and give my opinion as to whether the above-referenced prior art references (Stewart, Bryans, and Onno) disclose the elements of claim 7 of the ‘675 patent. As explained in detail below, it is my opinion that each of the above-referenced prior art documents individually discloses each element of claim 7. I refer below to each prior art reference applied individually as a separate unpatentability “Ground.”

A. Ground 1: Claim 7 in view of Stewart

a. “A method comprising:”

39. Stewart describes a “method” in that it discloses various processes, including a process for asynchronous bit-serial communication. *EX. 1004*, at col. 2:34-39.

b. “asynchronously, serially transferring first serial data, corresponding to first parallel bus data, from a first module to a second module using a serial link;”

40. Stewart discloses this element of claim 7. Stewart discloses a “data communication link that permits asynchronous bit-serial communications among devices transmitting and receiving Manchester-type codes over a serial information channel.” *EX. 1004*, at col. 2:35-39. A PHOSITA would have known at the time of the ‘675 patent that Manchester encoding/decoding is a legacy asynchronous serial data communications protocol that, additionally, protects from the deleterious effect of a long string of zeros or ones. *See e.g., EX. 1004*, at col. 1:54-58. Stewart discloses that it is presumed that the transmitting device operates “asynchronously and independently from the receiving device,” disclosing asynchronous serial transmission. *EX. 1004*, at col. 2:13-15 and col. 5:5-8.

41. Stewart discloses that the asynchronously serially transferred data is first serial data. Specifically, Stewart states that “[t]he encoder 23 combines representations of the data bits with clocking signals from the clock 49 to produce

Manchester encoded information signals. These information signals are then applied to driver 18 which places the encoded information signals on the transmitting channel 14 where they are distributed by the passive coupler 15 to the other devices connecting to the communicating link.” EX. 1004, at col. 5:15-22. The coupler 15 is disclosed to enable “devices on the channel 16 to sense information signals transmitted on the channel 14.” EX. 1004, at col. 3:60-63. Thus, the coupler 15, together with serial channels 14 and 16 discloses a duplex (e.g., two way communication) serial link. EX. 1004, at col. 3: 56-63

42. The Manchester encoded information signals are transmitted and received over a serial communication link and, therefore, are serial data. EX. 1004, at col. 2:34-39. The serial transmission line 14 and receiving lines 16 are shown in annotated FIG. 1 of Stewart, below.

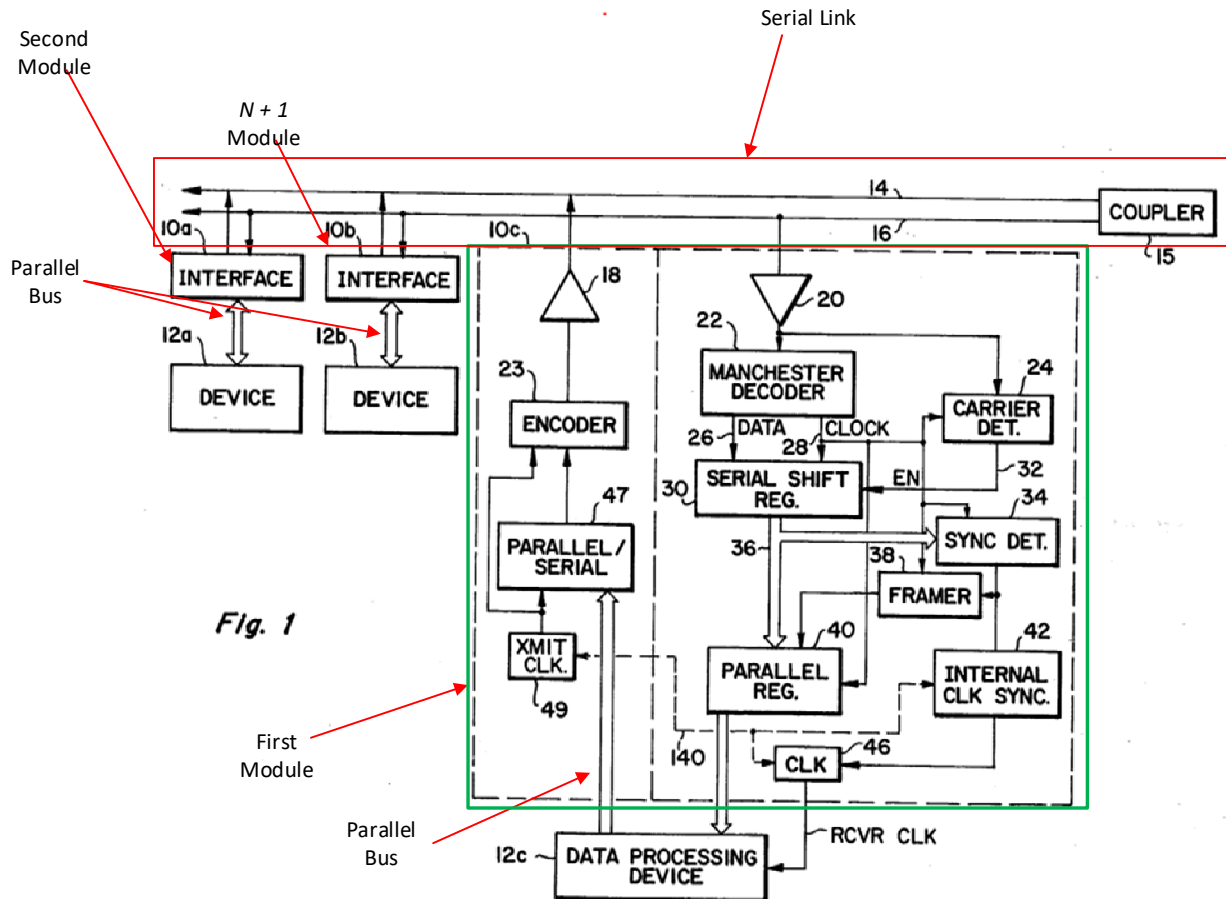


Fig. 1

Stewart FIG. 1 (Annotated)

43. The serial information channel represents a “serial link” and includes transmitting and receiving channels 14 and 16, which are individual serial channels, as well as the coupler 15, as described above. *EX. 1004*, at col. 3:56 – col. 4:19.

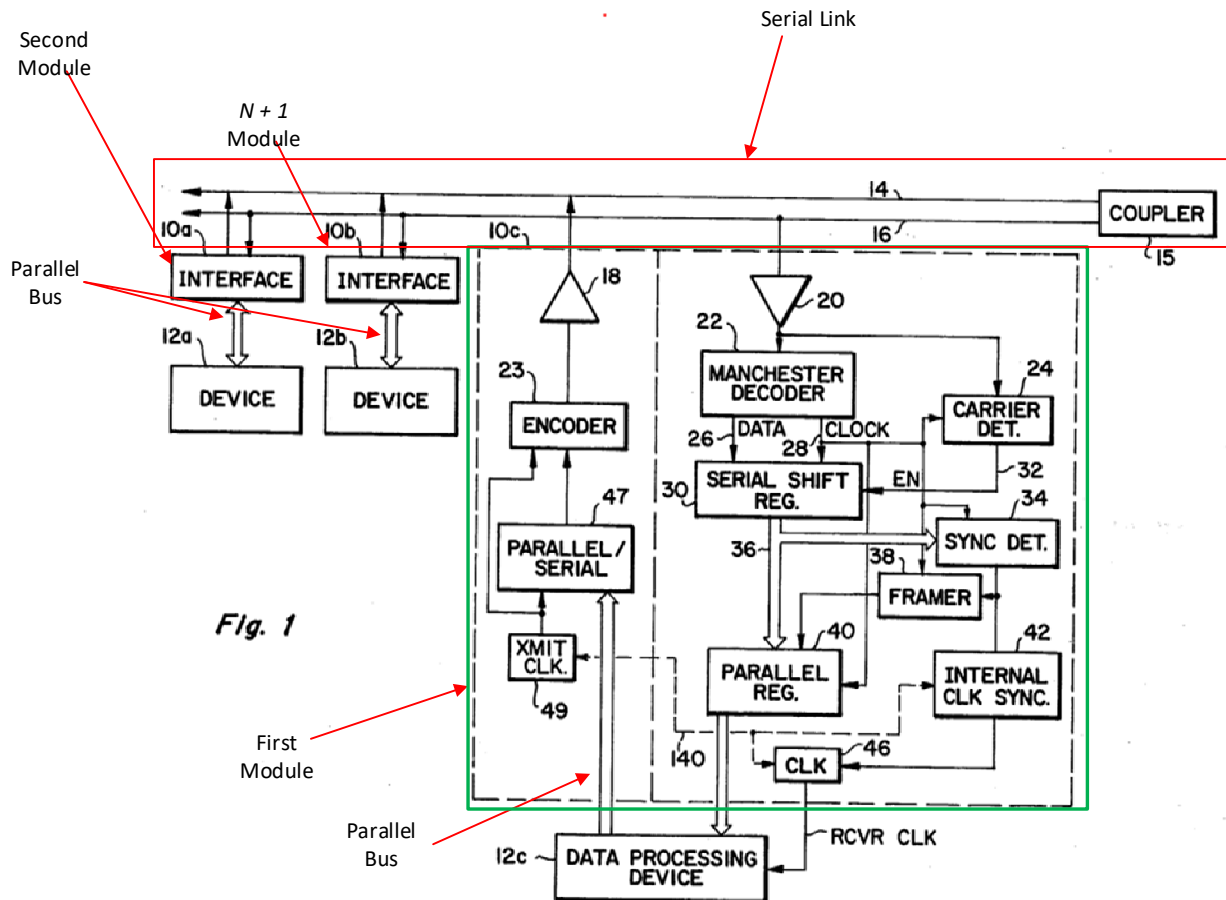
44. Stewart discloses that the claimed “first serial data[] correspond[s] to first parallel bus data.” Stewart explains that data received from a device, such as data processing device 12a-c, is parallel data, stating that a “this invention is

concerned with a system for decoding Manchester-encoded serial data and transferring the decoded data to a parallel device.” *EX. 1004*, col. 4:1-3. The parallel data is converted to serial data via a parallel-to-serial register. For example, Stewart states that a “parallel-to-serial register 47 receives eight-bit bytes from the device 12c under controller control of a clock located therein, and when the signals representing the byte settle in the register 47, a clock 49 effects a shift on a serial basis of the data bits constituting the byte to the encoder 23.” *EX. 1004*, at col. 5:9-15. This conversion of parallel data into serial data discloses that the asynchronous data described above is based on parallel data from devices, such as device 12c.

45. Stewart discloses that the asynchronous data is transmitted “from a first module to a second module using a serial link” as recited in claim 7. The basis of the technology of Stewart involves connecting various devices over a serial link. Stewart states that “FIG. 1 depicts a communications link [14, 16] and interface including a transmitting channel 14 and a receiving channel 16 over which a plurality of devices 12a, 12b, and 12c connect via their respective interfaces 10a, 10b and 10c.” *EX. 1004* at 3: 56-60. The interfaces 10a, 10b, 10c disclose the claimed first and second modules, as data is provided over a serial link (14, 16) between the devices. Interface 10c is disclosed as being an “expanded block diagram of the interface circuitry.” *EX. 1004*, at col. 4:4-5. In view of this, it is

understood that the expanded block diagram of 10c represents circuitry also contained within interface devices 10a, 10b, as would have been understood by a PHOSITA. Thus, interfaces 10a, 10b, and 10c are understood to have the same circuitry and functionality.

46. This is further illustrated in annotated FIG. 1 of Stewart, below.



Stewart FIG. 1 (Annotated)

47. Thus, Stewart discloses “asynchronously, serially transferring first serial data, corresponding to first parallel bus data, from a first module to a second module using a serial link.”

c. “asynchronously, serially receiving second serial data, corresponding to second parallel bus data, from the second module using the serial link; and”

48. Stewart discloses this element of claim 7. Stewart discloses a “data communication link that permits asynchronous bit-serial communications among devices transmitting and receiving Manchester-type codes over a serial information channel.” *EX. 1004*, at col. 2:35-39. Stewart discloses that it is presumed that the transmitting device operates “asynchronously and independently from the receiving device,” disclosing asynchronous serial transmission and reception. *EX. 1004*, at col. 2:13-15. *See also, EX. 1004*, at col. 5:5-8.

49. Stewart discloses that the asynchronously serially received data is a second serial data. For example, Stewart states that “[a]s this invention is concerned with a system for decoding Manchester-encoded serial data and transferring the decoded data to a parallel device, we show interface 10c, an expanded block diagram of the interface circuitry in which a driver 20 (e.g., amplifier) receives from the receiving channel 16 signals representing serial data bits are [sic] clock transitions and supplies these signals to a Manchester decoder 22.” *EX. 1004*, at col. 4:1-8. Thus, the data received by the interface 10c is serial

data. The Manchester encoded information signals are transmitted and received over a serial communication link (formed by transmission line 14, receiving line 16, and coupler 15, as described above) and therefore are serial data. *See, EX. 1004*, at col. 2:34-39. *See also, EX. 1004*, at col. 3: 56-63. The serial transmission line 14 and receiving lines 16 are shown in annotated FIG. 1, below.

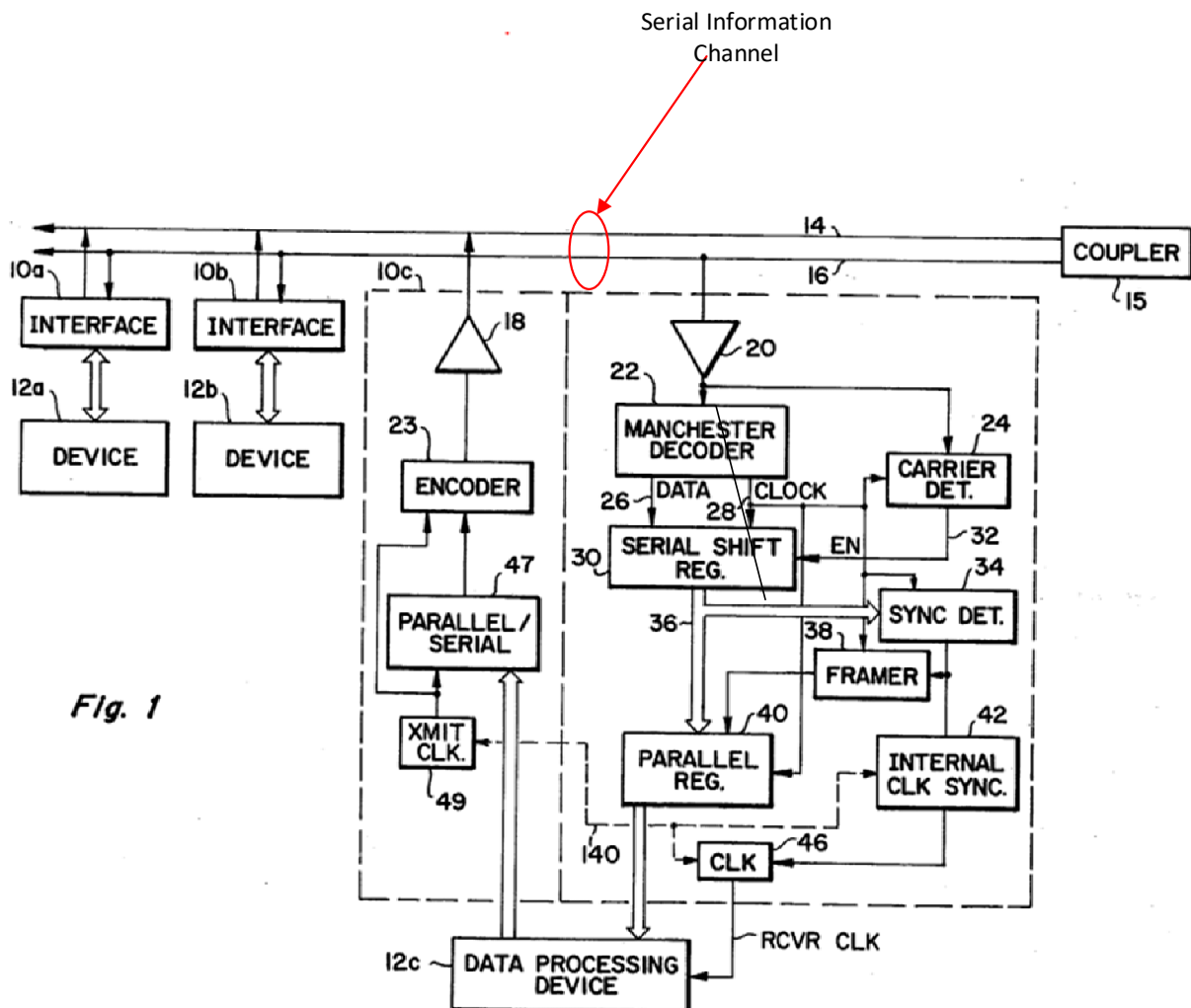


Fig. 1

Stewart FIG. 1 (Annotated)

50. The serial information channel represents a “serial link” and includes transmitting and receiving channels 14 and 16, which are individual serial channels, as well as coupler 15. *EX. 1004*, at col. 3:56 – col. 4:19.

51. Stewart discloses that the second serial data corresponds to “second parallel bus data.” Stewart explains that data received from a device, such as data processing device 12a-c, is parallel data, stating that “this invention is concerned with a system for decoding Manchester-encoded serial data and transferring the decoded data to a parallel device.” *EX. 1004*, col. 4:1-3. The parallel data is converted to serial data via a parallel-to-serial register. For example, Stewart states that a “parallel-to-serial register 47 receives eight-bit bytes from the device 12c under control of a clock located therein, and then the signals representing the byte settle in the register 47, a clock 49 effects a shift on a serial basis of the data bits constituting the byte to the encoder 23.” *EX. 1004*, at col. 5:9-15.

52. Stewart further explains that data received at the driver 20 from “the receiving channel 16 [are] signals representing serial data bits and supplies these signals to a Manchester decoder 22. . . . The decoder 22, being subsequently described, extracts the data signal (herein called data bits) and a clock (i.e., CLOCK) signal from the information signals on the channel 16 and supplies both the data bits and the CLOCK signal to a serial shift register.” *EX. 1004*, at col. 4:5-15. Stewart further explains that “each set of eight data bits accumulates in the

serial register 30, a byte is transferred under control of a framer 38, also subsequently described, which enables the loading of the parallel register 40 associated with the serial register 30.” *EX. 1004*, at col. 4:37-41. Thus, the data received at one of the interfaces 10a-10c is converted from serial data, as received via channel 16, to parallel data, which indicates that any serial data received on line 16 corresponds to parallel bus data.

53. The above-described conversion of parallel data into serial data discloses that the asynchronous data described above is based on parallel data from devices, such as device 12c. As interface 10c is described as being simply a detailed diagram of the interface circuitry which would be understood to be shared by interfaces 10a, 10b, and 10c, as all are concerned with “a system for decoding Manchester-encoded serial data and transferring the decoded data to a parallel device.” *EX. 1004*, at col. 4:1-3. Thus, any serial data received by the interface device 10c corresponds to parallel data that was previously encoded and serialized by interfaces 10a or 10b.

54. Stewart discloses that the asynchronous data is received from the second module using the serial link. The basis of the technology of Stewart involves connecting various devices over a serial link, as described above. Stewart states that “FIG. 1 depicts a communications link [14, 16] and interface including a transmitting channel 14 and a receiving channel 16 over which a plurality of

55. Thus, Stewart discloses “asynchronously, serially receiving second serial data, corresponding to second parallel bus data, from the second module using the serial link.”

d. “generating a first clock signal, for use by the first module, using the second serial data.”

56. Stewart discloses this element. As is known in the art, and acknowledged in Stewart, “Manchester-encoded data comprises data bits and clock transmissions combined in the same information signal. The decoder 22, being subsequently described, extracts the data signal (herein called data bits) and a clock (i.e., CLOCK) signal from the information signals on the channel 16 [the receive line] and supplies both the data bits and the CLOCK signal to a serial shift register 30 via conductors 26 and 28, respectively.” *EX. 1004* at 4:8-16. As noted above, a PHOSITA would have known that the terms “generate” and “extract” may be used interchangeably in the context of claim 7. Stewart’s decoder 22, as described above, ***generates*** or ***produces*** the clock signal by extracting it ***from*** (i.e., ***using***) the received Manchester encoded data (i.e., second serial data). Thus, a device, such as device 10c, receiving the Manchester-encoded data generates a clock signal using the received data [second serial data].

57. Thus, Stewart discloses “generating a first clock signal, for use by the first module, using the second serial data.”

58. Therefore, it is my opinion that Stewart discloses all elements of and anticipates claim 7.

B. Ground 2: Claim 7 in view of Bryans

a. “A method comprising:”

59. Bryans discloses that the invention is directed to a “method and device for transmitting serial data at very high speeds.” *EX. 1006*, at col. 1:7-8.

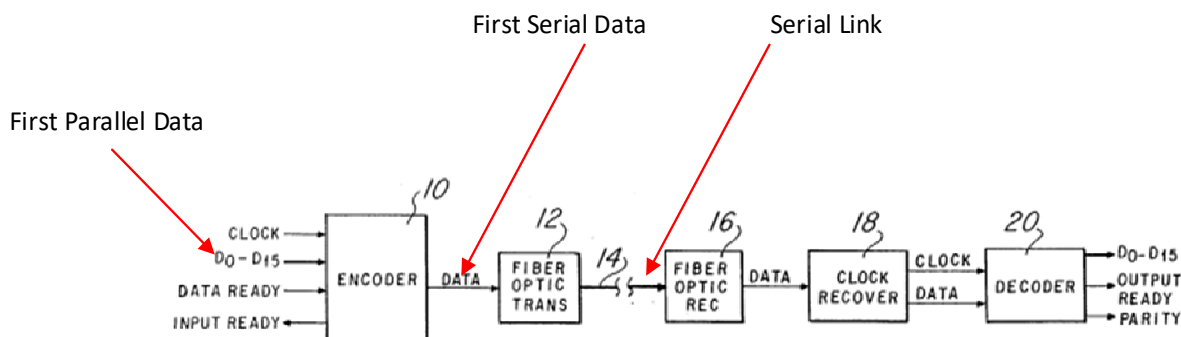
b. “asynchronously, serially transferring first serial data, corresponding to first parallel bus data, from a first module to a second module using a serial link”

60. Bryans discloses this element of claim 7. First, Bryans discloses asynchronously, serially transferring data. Specifically, Bryans states that the described systems are “preferably operated ***asynchronously***, requiring that a sync pulse be transmitted along the serial link prior to transmission of each data word.” *EX. 1006*, col. 2:41-44 (emphasis added).

61. Bryans also discloses transferring first serial data, corresponding to first parallel bus data. An encoder device 10 converts data from parallel to serial form, thus converting a first parallel bus data to a first serial data. “The encoder device 10 converts the data from parallel to serial form, and sends it to a fiber optic transmitter 12. The data is transmitted along a fiber optic cable 14 to a fiber optic receiver 16” *EX. 1006*, at col. 2:13-16. FIG. 1 of Bryans, as annotated below, illustrates the parallel data (represented as D0-D15) being encoded and

subsequently output as serial data. The particular physical implementation and architecture of the communications channel (wire pair, fiber optic line, ATM, or any other) is irrelevant to this discussion. However, the '675 patent does disclose that the “serial links 26 may also employ optical fiber and optical transceivers if desired.” *EX. 1001*, at col. 6:55-57. Thus, the '675 patent contemplated that the serial links could include fiber optic connections.

62. Bryans also discloses that the first serial data is serially transferred over a serial link. With respect to FIG. 1, Bryans explains that “FIG. 1 shows a serial communications link suitable for transmitting data between two parallel devices.” *EX. 1006*, at col. 2: 4-5. Specifically, the serial link is disclosed by the fiber optic cable 14 shown in FIG. 1, with Bryans stating that “[i]t would be desirable for a serial data link using fiber optic communications to utilize high bit rate data transmission.” *EX. 1006*, col. 1:35-38. Thus, the fiber optic cable 14 discloses a serial link.

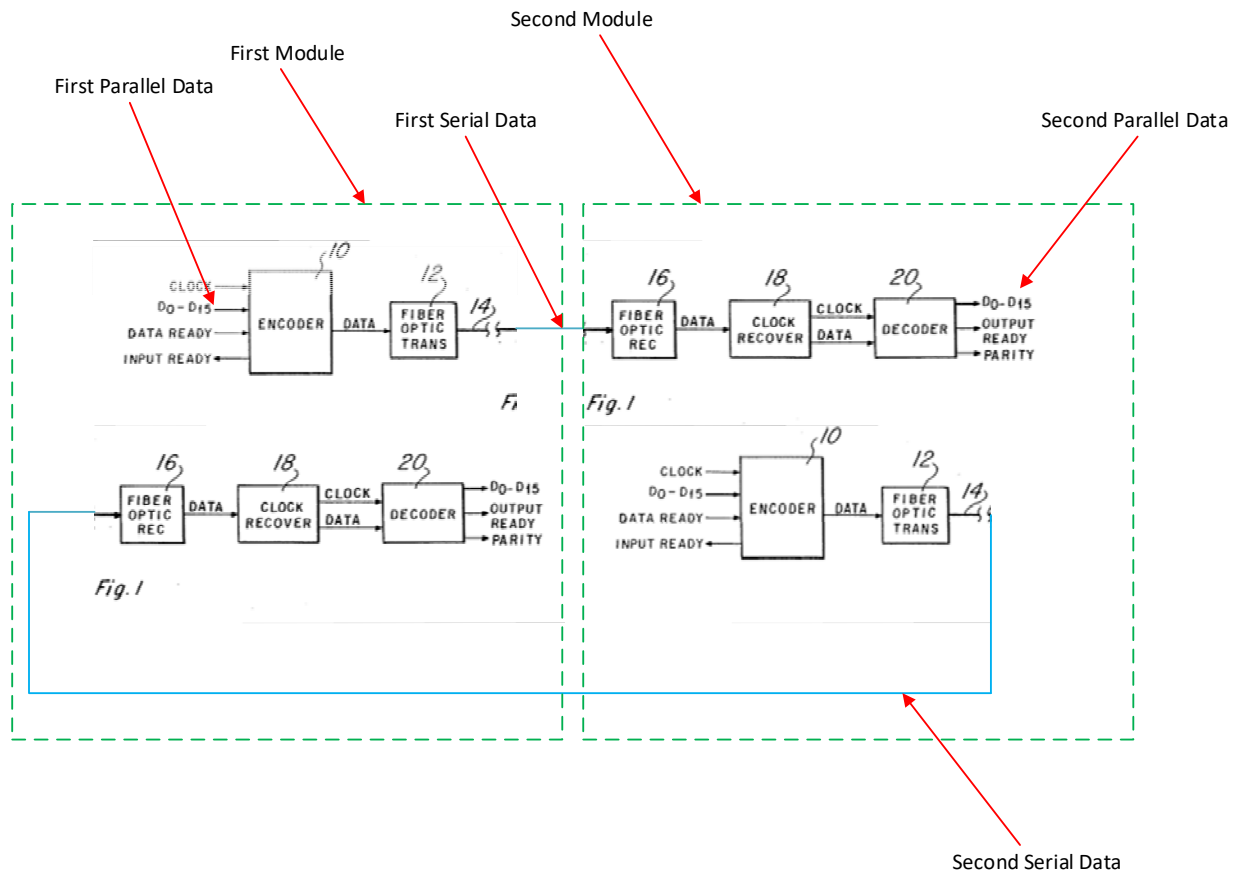


Bryans FIG. 1 (Annotated)

63. As noted above, Bryans is directed to a serial communications link suitable for “transmitting data between two parallel devices.” *EX. 1006*, at col. 2:4-5. The disclosed “two parallel devices” correspond to the first module and second module of claim 7, which transfer data between each other via the fiber optic link 14. The system shown in the above annotated FIG. 1 of Bryans shows a broken line on serial link 14, which indicates the transmission side of a first parallel device, as well as a receive side of the first parallel device. Thus, the parallel device is able to both transmit and receive, as would be necessary to transfer “high speed digital signals between various parts of a computer system, or between systems,” as presented by Bryans. *EX. 1006*, at col. 1:10-11.

64. Bryans further explains that the serial communications link of FIG. 1 is “suitable for transmitting data **between** two parallel devices.” *EX. 1006*, at col. 2:4-5 (emphasis added). Transmission of data between two device requires transmission *and* reception, and therefore, the described parallel devices of Bryans each include components of the serial communications link of FIG. 1. Bryans further states that “[t]he encoding and decoding functions can be easily implemented on a single integrated circuit for each function.” *EX. 1006*, at col. 1:43-45. As the encoding and decoding functions, which are part of the transmit and receive portions, respectively, are on the same chip, it is understood that each parallel device includes all of the components of FIG. 1.

65. Below is a further annotated version of FIG. 1, which duplicates the single parallel device shown in original FIG. 1 to illustrate the data transmission and reception between the two parallel devices described in Bryans.



Bryans FIG. 1 (Annotated and modified to show described parallel devices)

66. The above annotated version of FIG. 1, as modified according to the description of two parallel devices in Bryans, illustrates the first and second modules as would be understood by a PHOSITA.

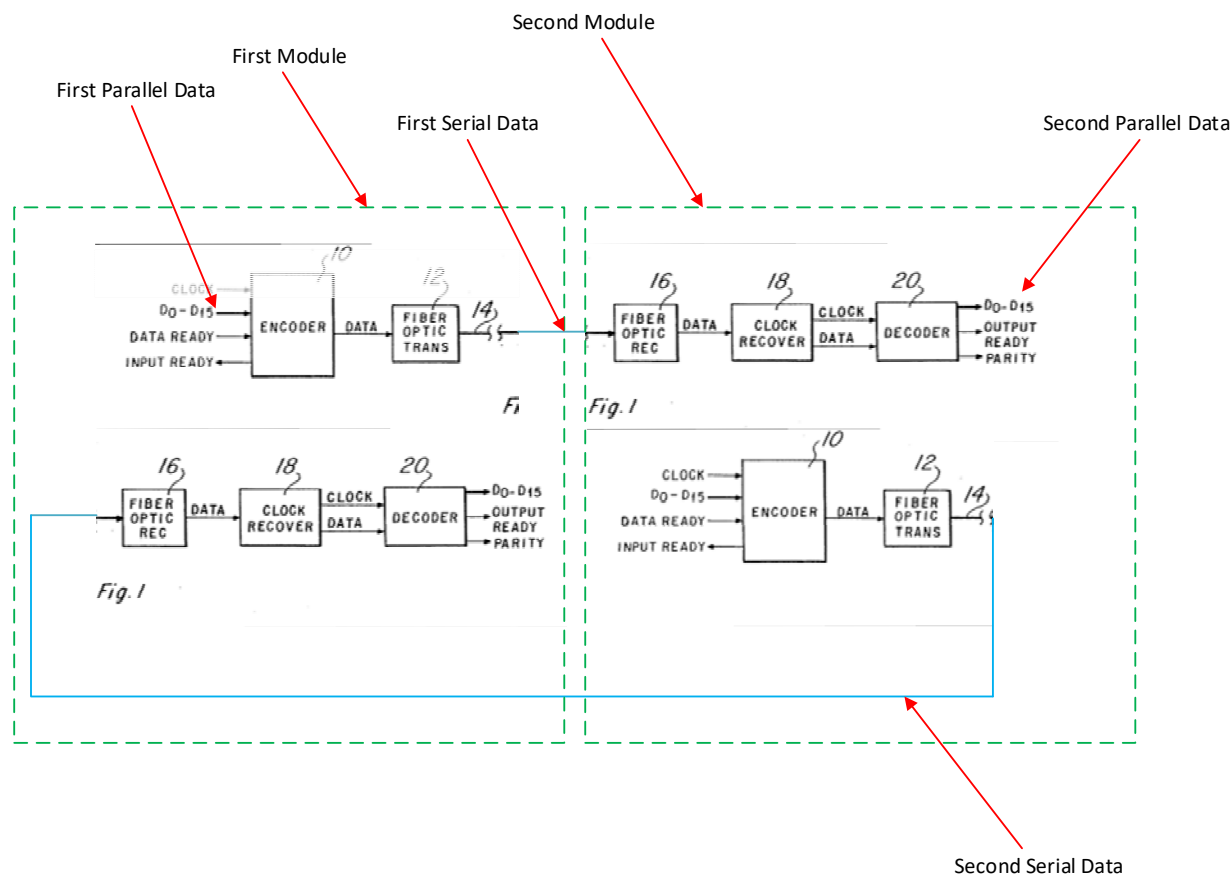
67. Thus, Bryans discloses “asynchronously, serially transferring first serial data, corresponding to first parallel bus data, from a first module to a second module using a serial link.”

c. “asynchronously, serially receiving second serial data, corresponding to second parallel bus data, from the second module using the serial link; and”

68. Bryans discloses this element of claim 7. As shown in annotated FIG. 1, below, a fiber optic receiver 16 is configured to receive serial data. Bryans states that the “data is transmitted along a fiber optic cable 14 [serial link] to a fiber optic receiver 16.” *EX. 1006*, at col. 2:15-16. This data transmission and reception is “preferably operated asynchronously.” *EX. 1006*, at col. 2:42-43. Bryans therefore teaches receiving second serial data, asynchronously.

69. Bryans further discloses that the received serial data corresponds to “second parallel bus data.” A decoder 20 is stated to convert “the [received] serial data into parallel form, and outputs it on data lines D0-D15.” *EX. 1006*, at col. 2:20-22. As the received second serial data is converted into parallel data it corresponds to “second parallel bus data,” as claimed. The below annotated FIG. 1 provides further illustration. The below annotated version of FIG. 1 duplicates the single parallel device shown in original FIG. 1 to illustrate the data transmission

and reception between the two parallel devices described in Bryans.



Bryans FIG. 1 (Annotated and modified to show described parallel devices)

70. As noted above, Bryans is directed to a serial communications link suitable for “transmitting data between two parallel devices.” *EX. 1006*, at col. 2:4-5. The two parallel devices disclose the first module and second module of claim 7, which transfer data between each other via the fiber optic link 14.

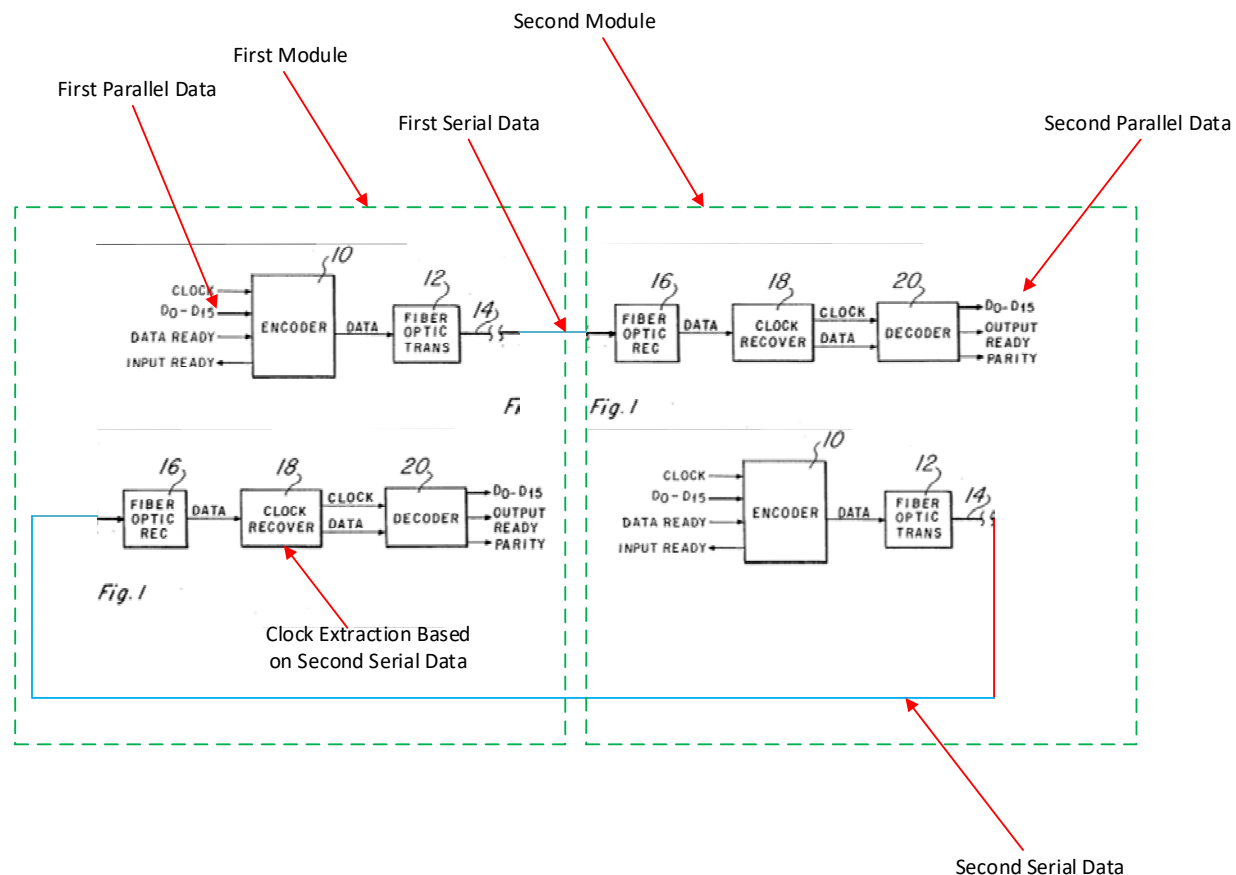
71. Thus, Bryans discloses “asynchronously, serially receiving second serial data, corresponding to second parallel bus data, from the second module using the serial link.”

d. “generating a first clock signal, for use by the first module, using the second serial data.”

72. Bryans discloses the above element of claim 7. Bryans discloses extracting [generating] a clock signal from received data using a clock receiver circuit 18, which “extracts the clock from the data itself, and presents both the CLOCK and the DATA signals to a decoder circuit 20. The decoder circuit 20 converts the serial data into parallel form, and outputs it on data lines D0-D15.” *EX. 1006*, at col. 2:18-22. The data in the above statement is received and converted to parallel data and therefore discloses the above noted “second serial data.” A PHOSITA would have known that the terms “generate” and “extract” may be used interchangeably in the context of claim 7. Bryans’ clock receiver circuit 18, as described above, **generates** or **produces** the clock signal by creating it **from** (i.e., **using**) the received serial data (i.e., second serial data), and therefore discloses “generating a first clock signal . . . using the second serial data,” as claimed. Thus, the receiving device, via the clock recover circuit 18 generates a clock signal by extracting clock data from the received data.

73. Further, as the recovered clock signal is provided to the decoder of the receiving device, the generated clock signal is “for use by the first module,” as recited in claim 7.

74. Annotated and modified FIG. 1 of Bryans, below, illustrates the disclosure of the above element of claim 7.



Bryans FIG. 1 (Annotated and modified to show described parallel devices)

75. Thus, Bryans discloses “generating a first clock signal, for use by the first module, using the second serial data.”

76. Therefore, it is my opinion that Bryans discloses all elements of and anticipates claim 7.

C. Ground 3: Claim 7 in view of Onno

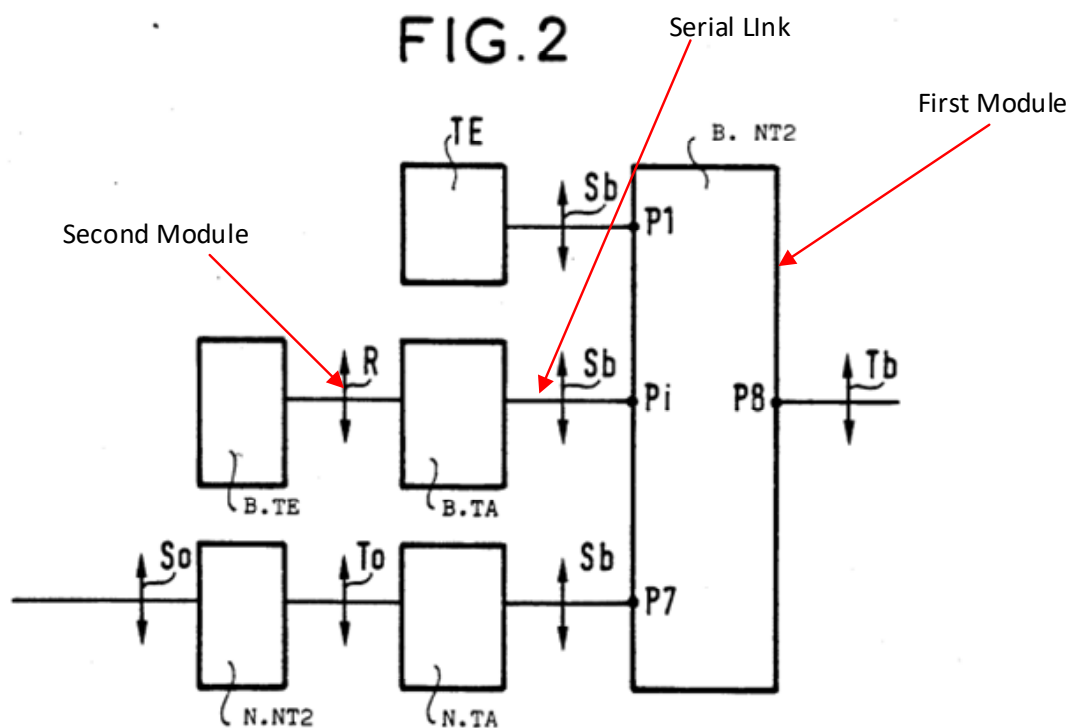
a. “A method comprising:”

77. Onno describes a “method” in that it discloses a processor for performing various operations, such as acting as a local controller and performing various operations such as signaling and supervisory processing functions. *See EX. 1005*, at col. 3:25-37.

b. “asynchronously, serially transferring first serial data, corresponding to first parallel bus data, from a first module to a second module using a serial link”

78. Onno discloses this element of claim 7. As outlined above, Onno is directed to a subscriber terminal installation to interconnect multiple terminals together, as well as to a public network. *See EX. 1005*, col. 1:5-9. Specifically, as stated by Onno, “[a]n object of the invention is to provide a subscriber installation based on asynchronous transfer mode.” *EX. 1005*, at col. 1:42-43. FIG. 2, as annotated below, “shows the general architecture of a subscriber terminal installation including a broadband digital network terminal B.NT2 and its connection means of the invention. These connection means are asynchronous optical interfaces Tb and Sb. . . .” *EX. 1005*, col. 2:51-55. A PHOSITA would have

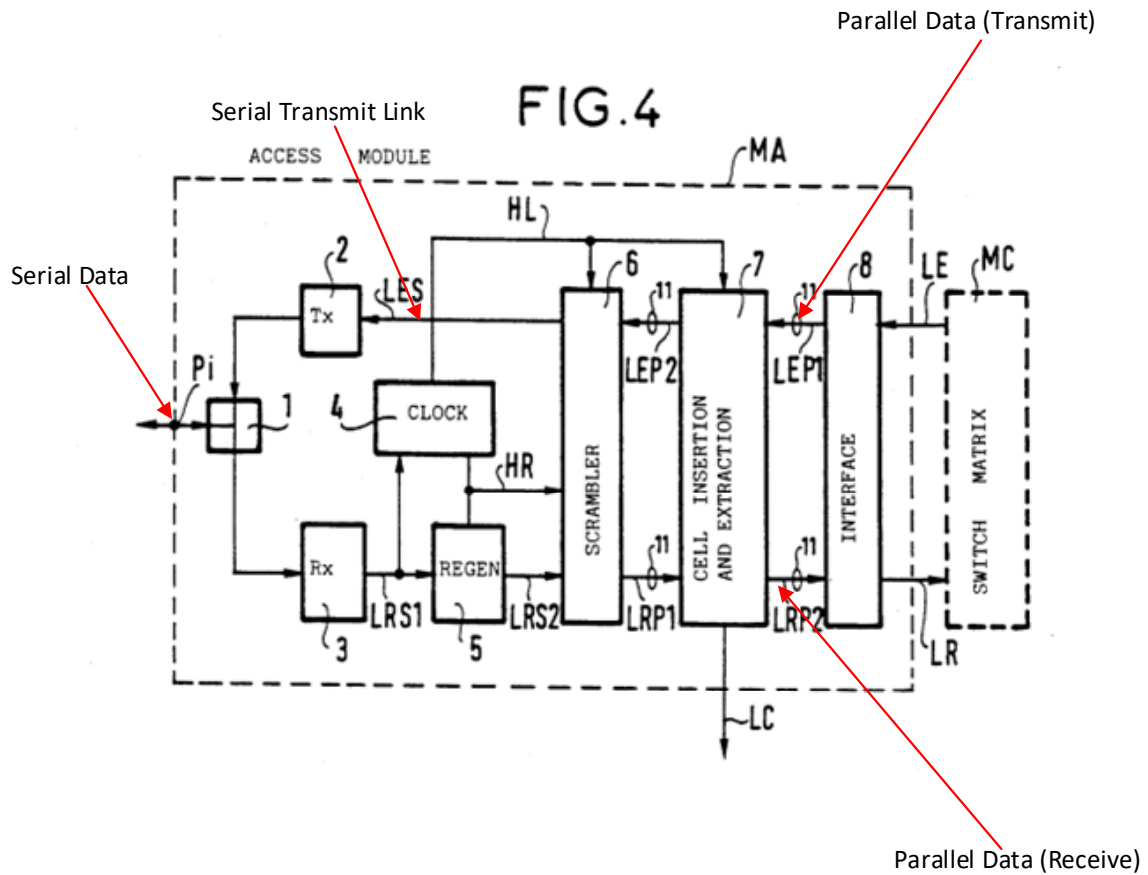
understood that serial data is transmitted and/or received asynchronously via the optical data lines Sb in Onno.



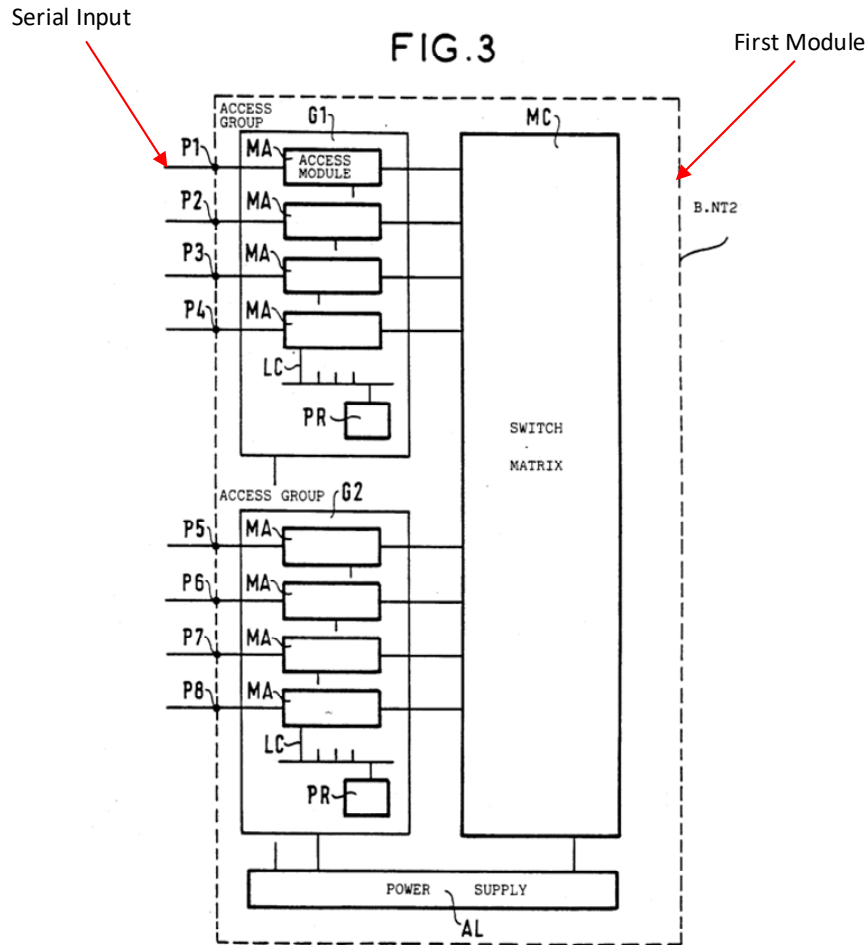
Onno FIG. 2 (Annotated)

79. Onno further explains that the “[p]ort Pi of the access module is connected to an optical interface Sb or Tb. The optical interfaces Sb or Tb use a monomode optical fiber for transmission in both directions, with the wavelengths used being 1300 nm for reception and 1500 nm for transmission. The data rate in each direction is no greater than 600 Mbit/s, with the signal being a multiplex of asynchronous cells. . . .” *EX. 1005*, col. 3:43-47. A PHOSITA would have understood the port Pi to be representative of ports P1-P8, as “[e]ach of ports P1 to

P7 is connected to an optical interface Sb, while the port P8 is connected to optical interface Tb, as shown in FIG. 2.” *EX. 1005*, col. 3:38-40. The port Pi “is connected to an optical duplexor 1, itself connected to an optical transmitter 2 and an optical receiver 3 . . . [and] a clock signal from the data in the receive direction, with the clock module being connected to a serial receive link LRS1 at the output from the optical receiver 3.” *EX. 1005*, col. 4:7-16. Onno goes on to disclose that the optical transmitter is coupled to “a serial transmit link LES.” *EX. 1005*, at col. 4: 22. A PHOSITA would have understood that the optical transmitter 2 and receiver 3 of the broadband digital network terminal B.NT2 facilitate serial transfer of first serial data, such as over optical transmitter 2, as the optical transmitter is coupled to a serial transmit link LES.



Onno FIG. 4 (Annotated)

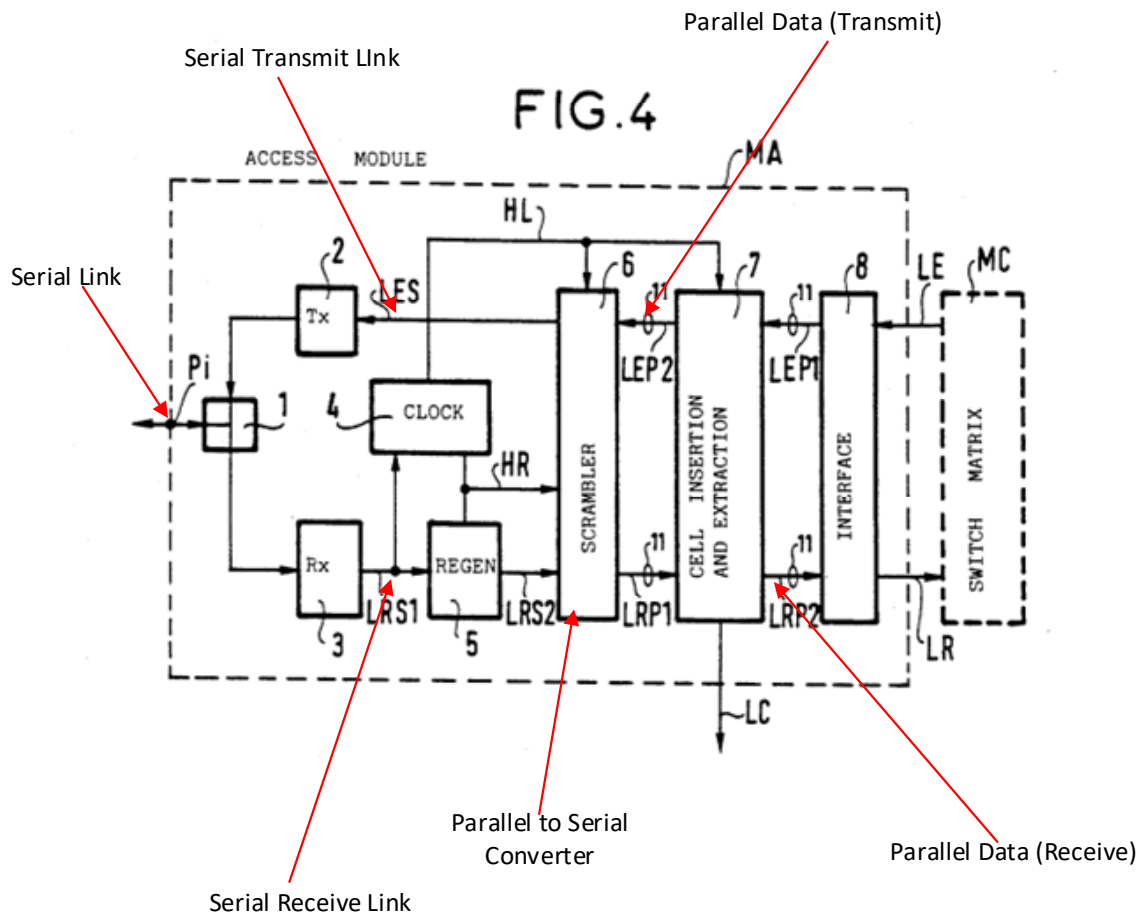


Onno FIG. 3 (Annotated)

80. A PHOSITA would have understood that Onno discloses asynchronous transferring of serial data between the broadband digital network terminal B.NT2 (first module) and other devices such as broadband terminals TE (second module).

81. Onno discloses that the first serial data is “corresponding to first parallel bus data.” As shown in annotated FIG. 4, below, the broadband digital network terminal B.NT2 includes a scrambler 6, which performs parallel to serial

operations. Specifically, the broadband digital network terminal B.NT2 includes an “extract circuit 7 for inserting and extracting signaling cells [that] is connected to the parallel-series scrambler 6 by a parallel transmit link LEP2 and a parallel receive link LRP1 to deliver data to the parallel-serial circuit in the transmit direction and to receive data therefrom in the receive direction.” *EX. 1005*, col. 4:26-31.

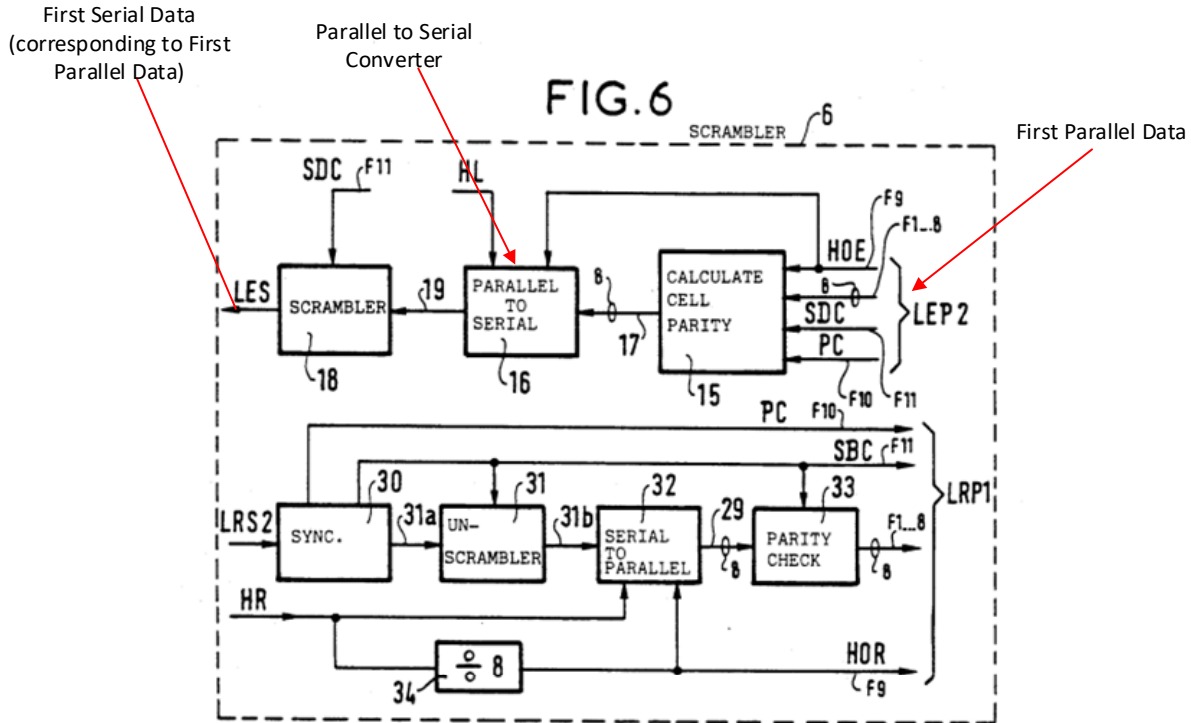


Onno FIG. 4 (Annotated)

82. The parallel-serial circuit serializes parallel data on parallel receive link LEP1 from the switch matrix MC, and then outputs on the serial link Pi. See *EX. 1005*, col. 4:25-31. The “transmit link LE and the receive line LR may be either of the parallel type having four data wires at 150 Mbit/s, a wire for a clock signal at 150 MHz, and a wire for a start of cell signal.” *EX. 1005*, at col. 4:44-48.

83. FIG. 6 and the associated portions of Onno are further instructive on this point. For example, Onno states that the parallel-serial scrambler (i.e., converter) circuit 6 of FIG. 4 “comprises a transmit path and a receive path. The transmit path is constituted by a cell parity calculating circuit 15 having its input connected to the parallel transmit link LEP2, a parallel serial converter circuit 16 connected by a link 17 to the output from the circuit 15 and receiving the local clock signal HL and a transmit byte signal HOE via the link LEP2, and a scrambler [converter] circuit 18 whose input is connected to the output from the circuit 126 via a serial link 19 and whose output is connected to the serial transmit link LES . . .” *EX. 1005*, at col. 5:6-15.

84. Onno therefore discloses that first parallel data is converted to serial data using parallel to serial converter 16, and then transmitted out over serial transmission line 3. This is highlighted in annotated FIG. 6, below.



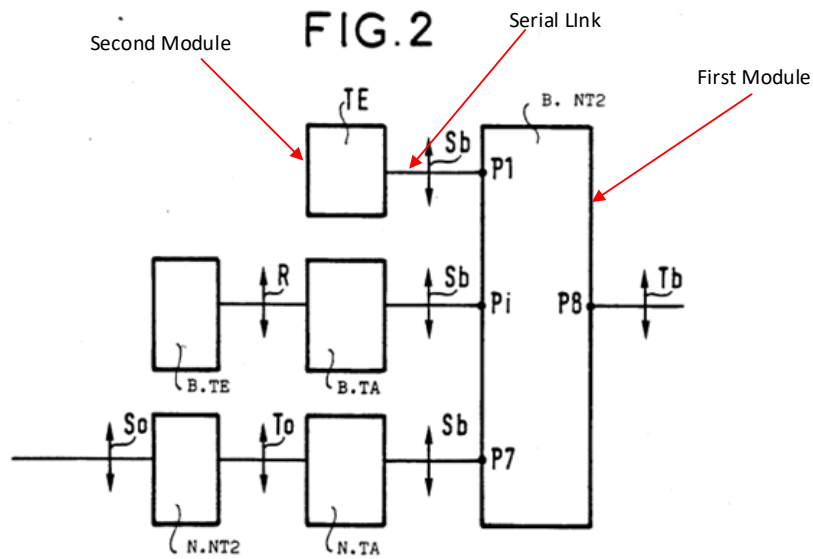
Onno FIG. 6 (Annotated)

85. Onno discloses that the asynchronous serial data is transferred from “a first module to a second module using a serial link.” Data is transferred from the broadband digital network terminal B.NT2 (first module) to various other devices, such as broadband terminals TE and/or broadband adapters B.TA via serial links Sb. For example, Onno states that “[b]roadband terminals TE in asynchronous transfer mode (only one of which is shown) are connected directly via an interface Sb to one of the ports of the termination B.NT2.” *EX. 1005*, at col. 3:1-4. Sb is an asynchronous optical interface, which conveys data at rates of up to 600Mbit/sec, *See, EX. 1005*, col. 2:67-68, and would therefore be understood by a PHOSITA to be a serial link.

86. Thus, Onno discloses “asynchronously, serially transferring first serial data, corresponding to first parallel bus data, from a first module to a second module using a serial link.”

c. “asynchronously, serially receiving second serial data, corresponding to second parallel bus data, from the second module using the serial link; and”

87. Onno discloses this element of claim 7. As stated by Onno, “[a]n object of the invention is to provide a subscriber installation based on asynchronous transfer mode. . . .” *EX. 1005*, at col. 1:42-43. Sb is an asynchronous optical interface, which convey data at rates of up to 600Mbit/sec, (*EX. 1005*, at col. 2:67-68), and would therefore be understood by a PHOSITA to be a serial link. FIG. 2, as annotated below, “shows the general architecture of a subscriber terminal installation including a broadband digital network terminal B.NT2 and its connection means of the invention. These connection means are asynchronous optical interfaces Tb and Sb. . . .” *EX. 1005*, col. 2:51-55. A PHOSITA would easily understand that serial data is transmitted and/or *received* asynchronously via the optical data lines Sb in Onno.

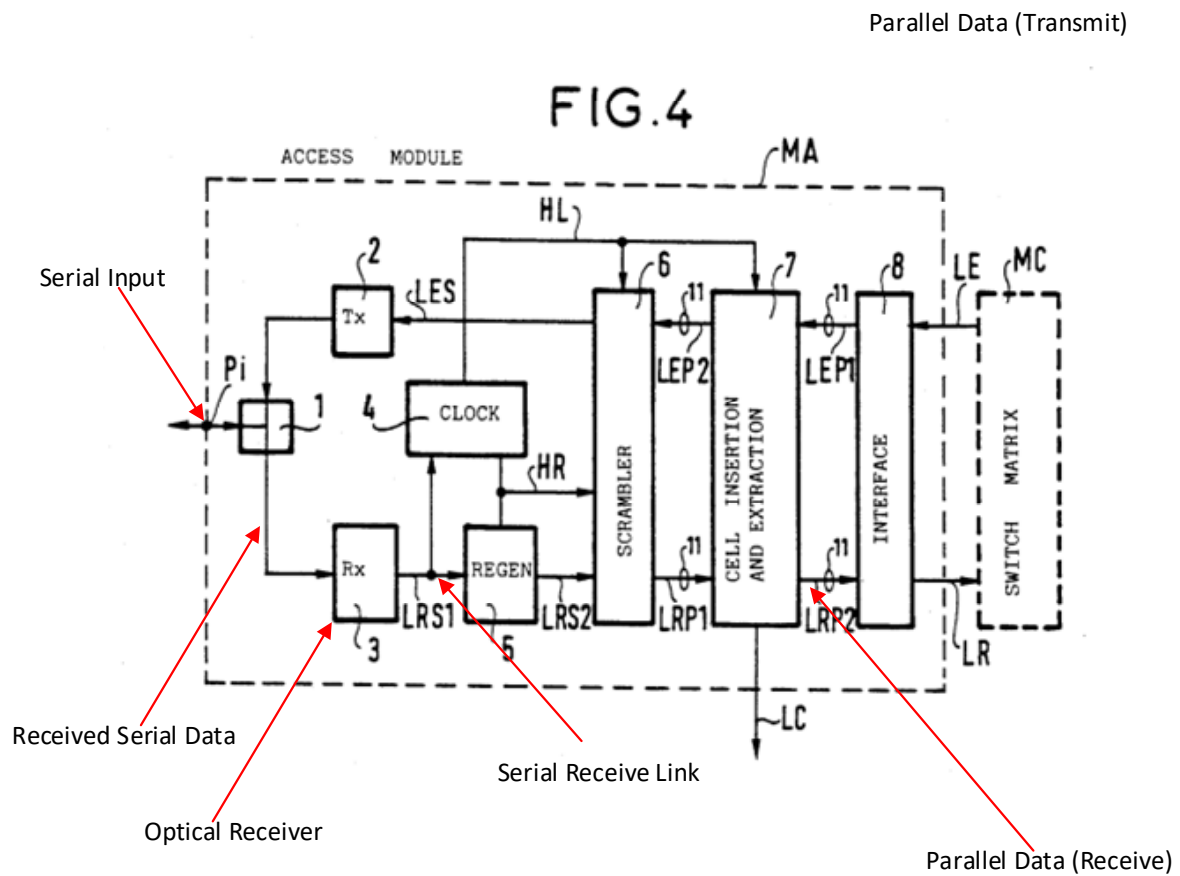


Onno FIG. 2 (Annotated)

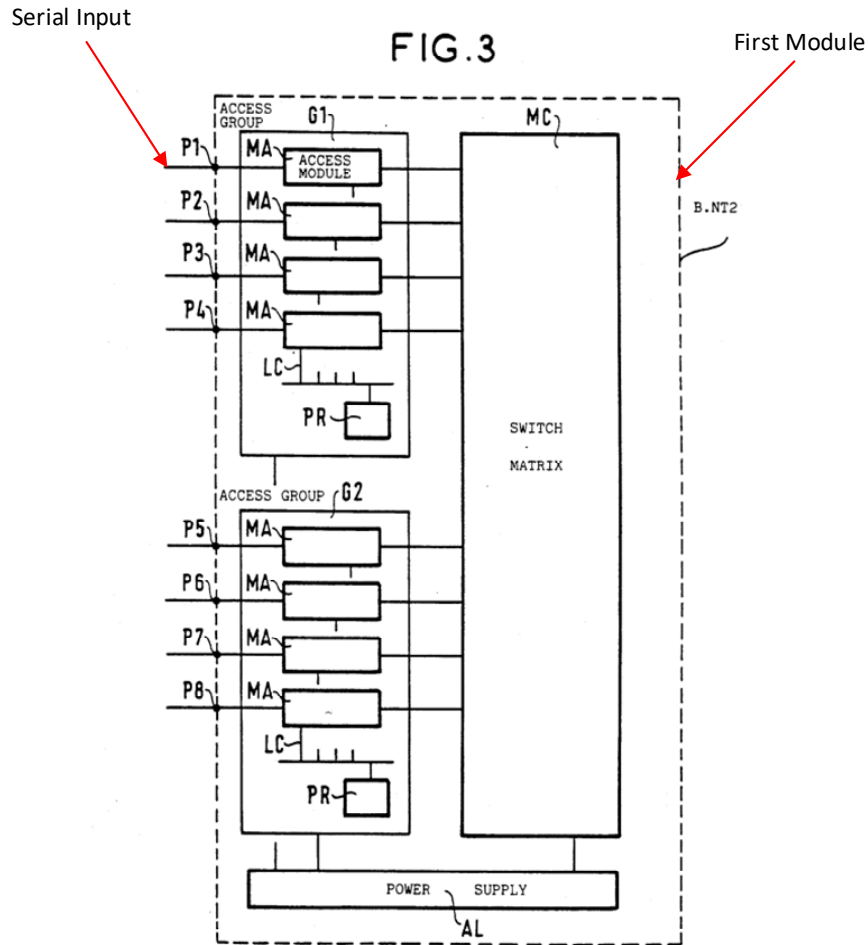
88. Onno further explains that the “[p]ort Pi of the access module is connected to an optical interface Sb or Tb. The optical interfaces Sb or Tb use a monomode optical fiber for transmission in both directions, with the wavelengths used being 1300 nm for reception and 1500 nm for transmission. The data rate in each direction is no greater than 600 Mbit/s, with the signal being a multiplex of asynchronous cells. . . .” *EX. 1005*, col. 3:43-49. The port Pi “is connected to an optical duplexor 1, itself connected to an optical transmitter 2 and an optical receiver 3 [and] a clock signal from the data in the receive direction, with the clock module being connected to a serial receive link LRS1 at the output from the optical receiver 3.” *EX. 1005*, at col. 4:7-16. A PHOSITA would understand that the optical transmitter 2 and receiver 3 of the broadband digital network terminal

B.NT2 facilitate serial reception of second serial data, such as over optical receiver

3.



Onno FIG. 4 (Annotated)

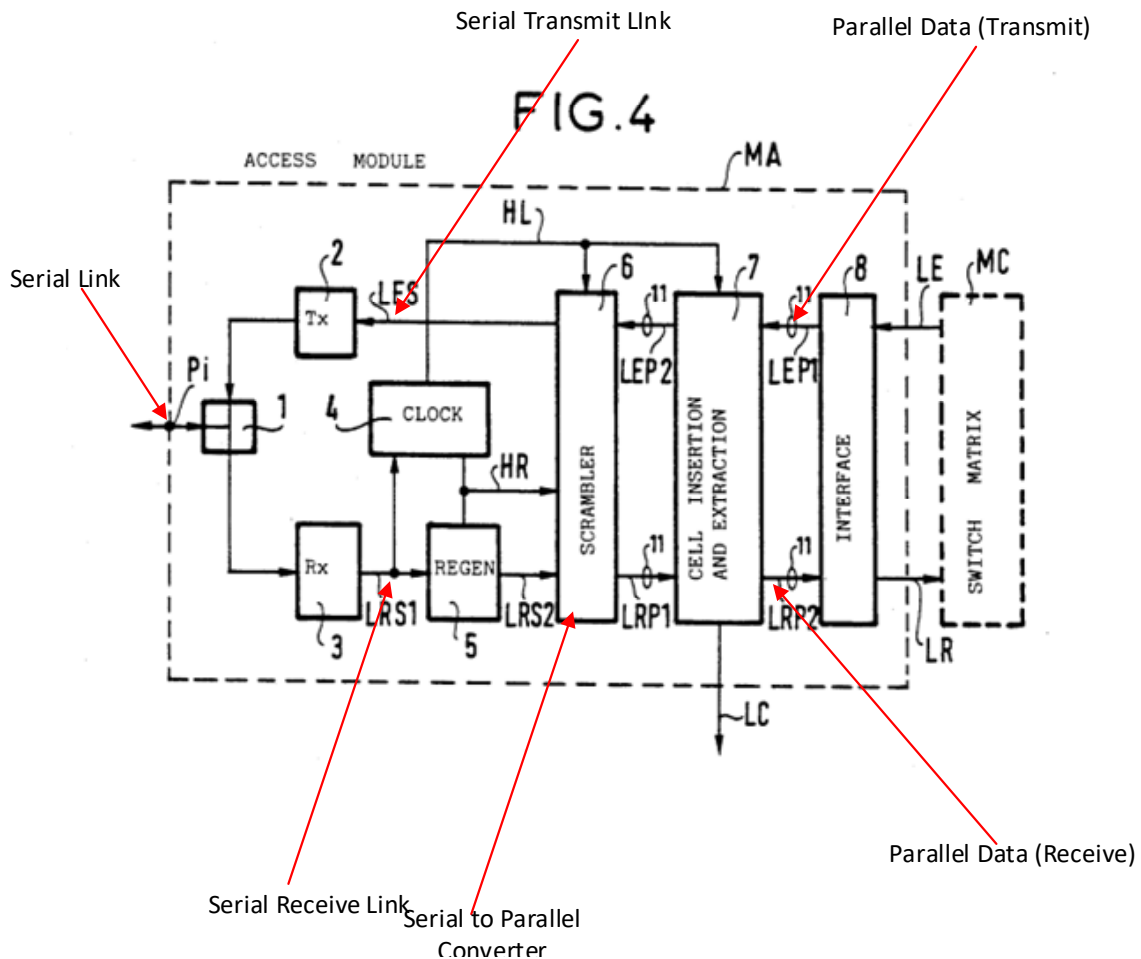


Onno FIG. 3 (Annotated)

89. A PHOSITA would have understood that Onno discloses asynchronous transferring of serial data between the broadband digital network terminal B.NT2 (first module) and other devices such as broadband terminals TE (second module).

90. Onno discloses that the received second serial data is “corresponding to second parallel bus data.” As shown in annotated FIG. 4, below, the broadband digital network terminal B.NT2 includes a scrambler 6, which performs parallel to

serial operations. Specifically, the broadband digital network terminal B.NT2 includes an “extract circuit 7 for inserting and extracting signaling cells [that] is connected to the parallel-series scrambler 6 by a parallel transmit link LEP2 and a parallel receive link LRP1 to deliver data to the parallel-serial circuit in the transmit direction and to receive data therefrom in the receive direction.” *EX. 1005*, col. 4:26-31 (emphasis added).

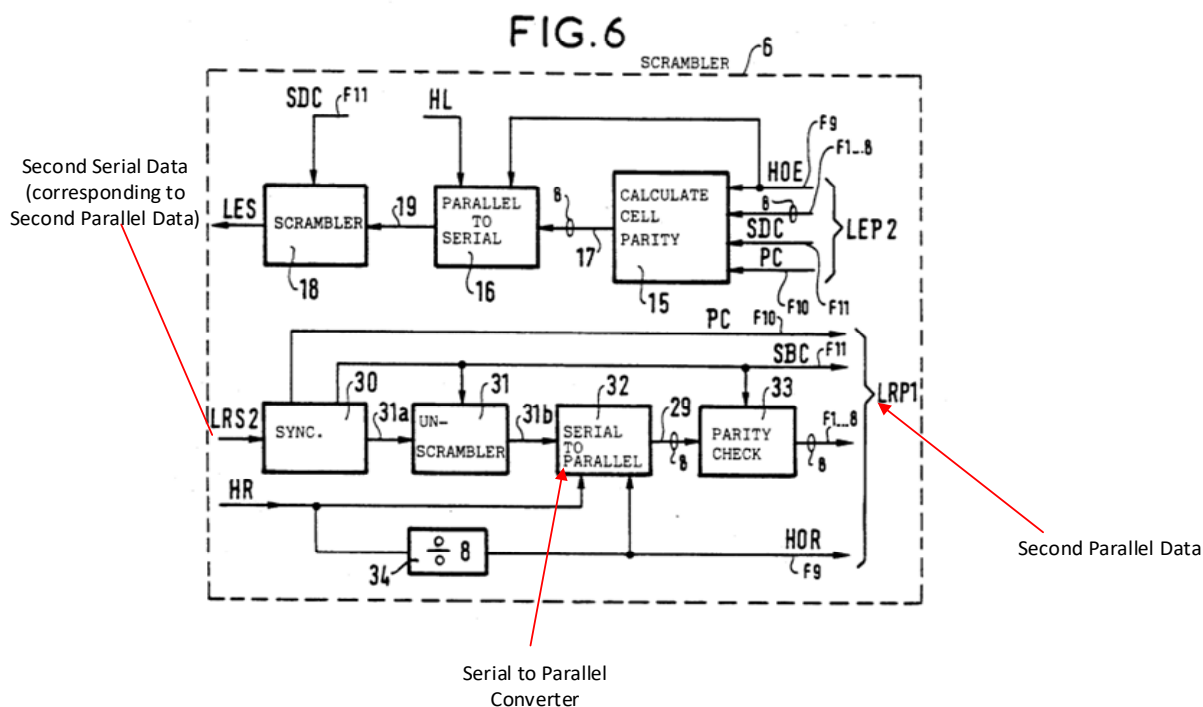


Onno FIG. 4 (Annotated)

91. Onno discloses that FIG. 6 “shows the parallel-serial scrambler circuit 6 of FIG. 4 which comprises a transmit path and a receive path.” *EX. 1005*, at col. 5:5-7. The receive path is described in Onno as including the “serial receive link LRS2, an unscrambler circuit 31 connected via an input link 31a to the synchronization circuit 30, a serial-parallel converter circuit 32 connected via a link 31b to the output from the unscrambler circuit 31, and a parity check circuit 33 connected to the output of the serial-parallel converter 32 via a parallel link 29 and having its output connected to the eight data wires F1 . . . 8 of the parallel receive link LRP1.” *EX. 1005*, at col. 5:19-29.

92. Onno therefore discloses that second parallel data is extracted from serial data using serial to parallel converter 32, and then transmitted out over the multiwire parallel receive link LRP1. As the received serial data is converted to parallel data by the serial to parallel converter 32, a PHOSITA would understand that the received data corresponds to second parallel bus data, as the received data is required to have originated in a parallel format in order to be reconstructed as parallel data by the serial to parallel converter 32. This is highlighted in annotated

FIG. 6, below.



Onno FIG. 6 (Annotated)

93. Onno discloses that the asynchronous serial data is received from “the second module using the serial link,” as recited in claim 7. Data is received by the broadband digital network terminal B.NT2 (first module) from various other devices, such as broadband terminals TE and/or broadband adapters B.TA (second module) via serial links Sb (serial link). For example, Onno states that “[b]roadband terminals TE in asynchronous transfer mode (only one of which is shown) are connected directly via an interface Sb to one of the ports of the termination B.NT2.” *EX. 1005*, at col. 3:1-4. Sb is an asynchronous optical

interface, which convey data at rates of up to 600Mbit/sec, (EX. 1005, col. 2:67-68), and would therefore be understood by a PHOSITA to be a serial link.

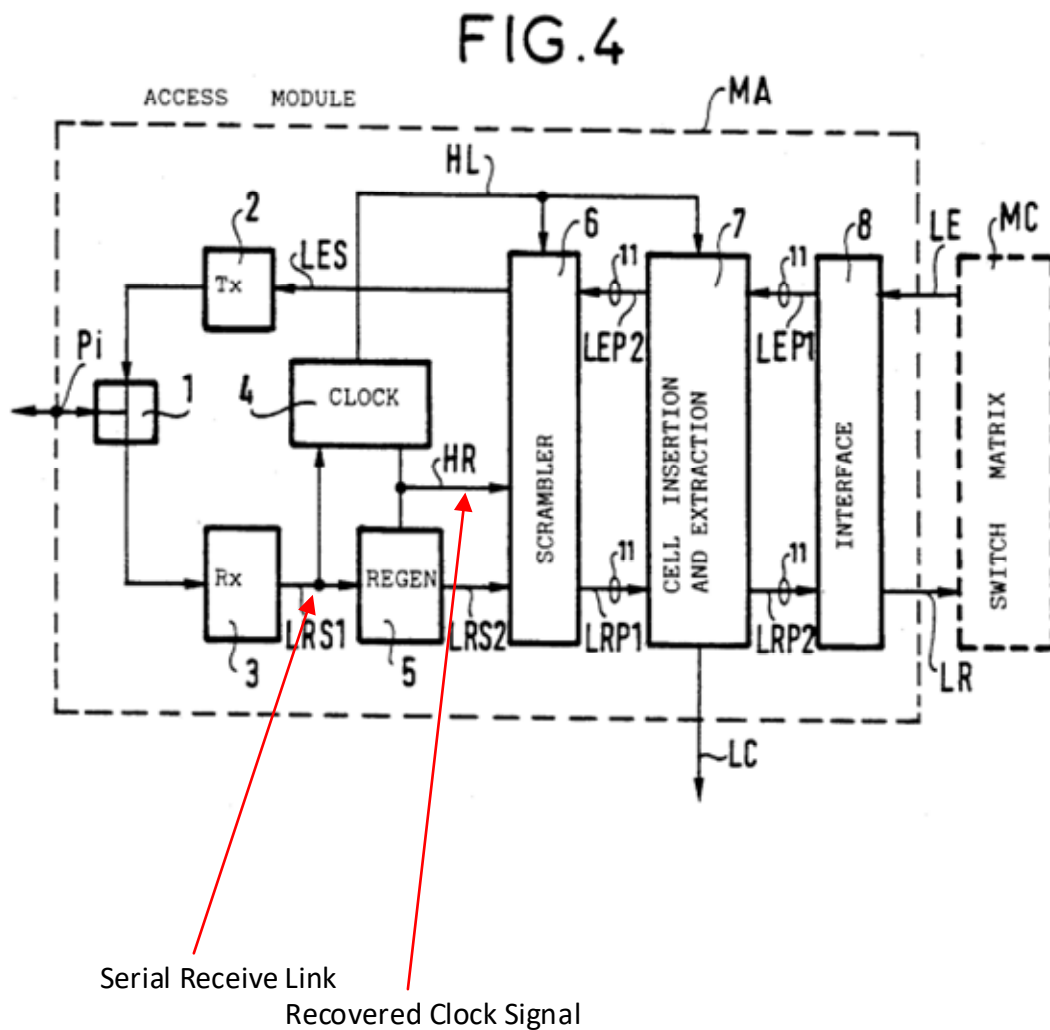
94. Thus, Onno discloses “asynchronously, serially receiving second serial data, corresponding to second parallel bus data, from the second module using the serial link.”

d. “generating a first clock signal, for use by the first module, using the second serial data.”

95. Onno discloses this element of claim 7. Onno states that a “clock module 4 generates a local clock signal HL at the data rate for the transmission direction (600 Mbit/s, 150 Mbit/s, or 10 Mbit/s) and it *recovers a clock signal* [HR] *from the data in the receive direction* [second serial data]. . . .” EX. 1005, col. 4:11-15. *See also, EX. 1005*, at col. 4:24-25 (emphasis added).

96. A PHOSITA would have known that the terms “generate” and “recovers” may be used interchangeably in the context of claim 7. Onno’s clock module 4, as described above, **generates** or **produces** clock signal HR by recovering it **from** (i.e., **using**) the data in the receive direction (i.e., second serial data), and therefore discloses “generating a first clock signal . . . using the second serial data,” as claimed.

97. The “serial-parallel converter 32 receives the recovered clock signal HR” as shown in annotated FIG. 4, below. This discloses that the recovered clock signal is used on the first module, B.NT2, as the clock module 4 is located within access module MA, which is one of multiple access modules of B.NT2. See, *EX. 1005*, at col. 3: 23-27 (“[t]he terminal B.NT2 comprises a switching matrix MC, two access groups G1 and G2, and a power supply AL. Each access group includes four access modules **MA** each connected via a control link LC to a processor PR which acts as a local controller.”) (emphasis added), and FIG. 3.



Onno FIG. 4 (Annotated)

98. Thus, Onno discloses “generating a first clock signal, *for use by the first module*, using the second serial data.” (Emphasis added).

99. Therefore, it is my opinion that Onno discloses all elements of and anticipates claim 7.

IX. CONCLUSION

100. As discussed above, it is my opinion that Stewart, Bryans, and Onno each discloses each element of claim 7 of the '675 patent. Thus, Stewart, Bryans, and Onno each anticipate claim 7.

I declare under penalty of perjury that the foregoing is true and correct to the best of my knowledge.

Executed on March 21, 2023


Michael Caloyannides, Ph.D.

Claim Charts Regarding US 8,060,675, Claim 7, in view of Prior Art
Stewart, Bryans, and Onno

A. Ground 1: Claim 7 in view of Stewart

US 8,060,675, Claim 7	US 4,450,572 Stewart (EX 1004)
7. A method, comprising:	Stewart describes a “method” in that it discloses various processes, including a process for asynchronous bit-serial communication. <i>Col. 2, lines 34-39.</i>
asynchronously, serially transferring first serial data,	“A further objective of this invention is to provide an interface for coupling a computer with a data communications link that permits <u>asynchronous bit-serial communications among devices transmitting and receiving</u> Manchester-type codes over a serial information channel.” [asynchronously, serially transferring first serial data].” <i>Col. 2, lines 34-39.</i> “The encoder 23 combines representations of the data bits with clocking signals from the clock 49 to produce Manchester encoded information signals [first serial data]. These information signals are then applied to driver 18 which places the encoded information signals on the transmitting channel 14 where they are distributed by the passive coupler 15 to the other devices connected to the communicating link.” <i>Col. 5, lines 15-17.</i>
corresponding to first parallel bus data,	“[A] parallel-to-serial register 47 receives eight-bit bytes from the device 12c under control of a clock located therein, and then the signals representing the byte settle in the register 47 [corresponding to first parallel bus data], a clock 49 effects a shift on a serial basis of the data bits constituting the byte to the encoder 23.” <i>Col. 5, lines 9-15. Fig. 1 (annotated below).</i>

US 8,060,675, Claim 7	US 4,450,572 Stewart (EX 1004)
Fig. 1	from a first module to a second module using a serial link
First Module = interface 10c Second Module = interfaces 10a, 10b Serial Link = communications link including transmitting channel 14, receiving channel 16, and coupler 15.	“FIG. 1 depicts a communications link and interface including a transmitting channel 14 and a receiving channel 16 over which a plurality of devices 12a, 12b and 12c connect via their respective interfaces 10a, 10b and 10c.” Col. 3, lines 56-60; Fig. 1 (annotated below)

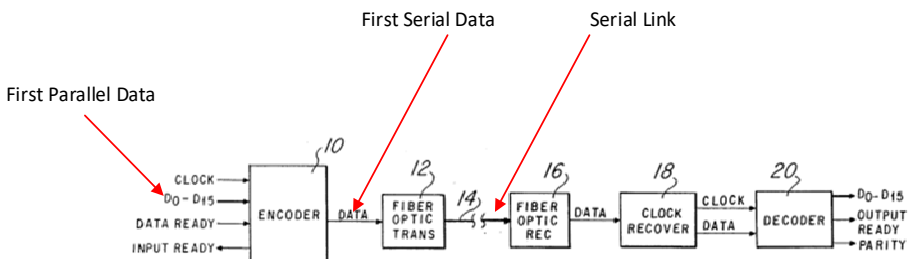
US 8,060,675, Claim 7	US 4,450,572 Stewart (EX 1004)
asynchronously, serially receiving second serial data,	“A further objective of this invention is to provide an interface for coupling a computer with a data communications link that permits <u>asynchronous bit-serial communications among devices transmitting and receiving Manchester-type codes over a serial information channel.</u>” [asynchronously, serially receiving second serial data]. <i>Col. 2, lines 34-39.</i> Stewart discloses that it is presumed that the transmitting device operates “asynchronously and independently from the receiving device,” disclosing asynchronous serial transmission and reception. <i>Col. 2, lines 13-15.</i> “As this invention is concerned with a system for decoding Manchester-encoded serial data and transferring the decoded data to a parallel device, we show interface 10c, an expanded block diagram of the interface circuitry in which a driver 20 (e.g., amplifier [of interface 10c] receives from the receiving channel signals representing serial data bits are [sic] clock transitions and supplies these signals to a Manchester decoder 22.” <i>Col. 4, lines 1-8.</i> Thus, the data received by the interface 10c is serial data. The Manchester encoded information signals are transmitted and received over a serial communication link (formed by transmission line 14, receiving line 16, and coupler 15, as described above) and therefore are serial data. <i>See col. 2:34-39; see also col. 3: 56-63.</i> The serial transmission line 14 and receiving lines 16 are shown in annotated FIG. 1, below.

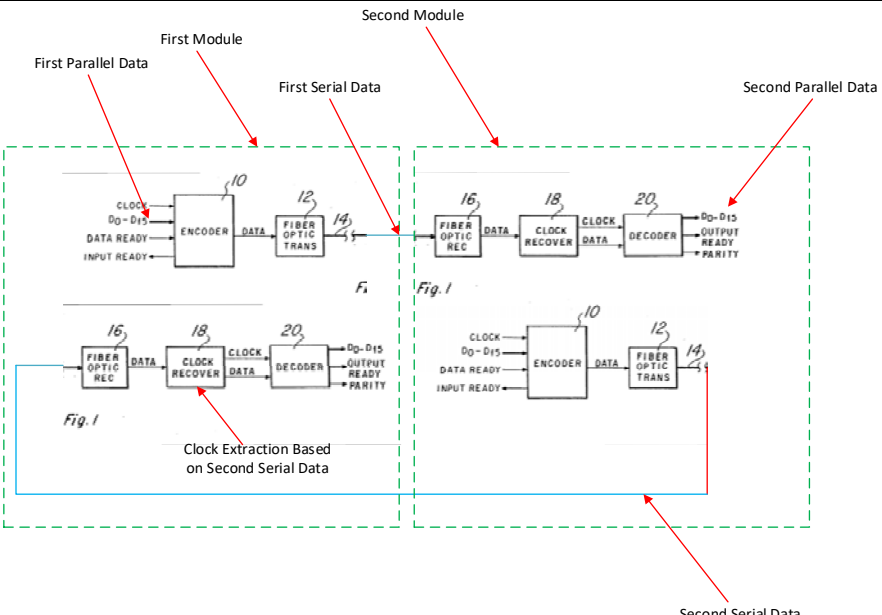
US 8,060,675, Claim 7	US 4,450,572 Stewart (EX 1004) Fig. 1
corresponding to second parallel bus data,	"As this invention is concerned with a system for decoding Manchester-encoded serial data and transferring the decoded data to a parallel device, we show interface 10c, an expanded block diagram of the interface circuitry in which a driver 20 (e.g., amplifier) receives from the receiving channel 16 signals representing serial data bits [corresponding to second parallel bus data] are [sic] clock transitions and supplies these signals to a Manchester decoder 22." Col. 4, lines 1-8.
from the second module using the serial link; and	"[P]arallel-to-serial register 47 receives eight-bit bytes from the device 12c under control of a clock located therein, and then the signals representing the byte settle in the register 47, a clock 49 effects a shift on a serial basis of the data bits constituting the byte to the encoder 23." Col. 5, lines 9-15. "A further objective of this invention is to provide an interface for coupling a computer with a data communications link that permits <u>asynchronous bit-serial communications among devices transmitting and receiving Manchester-type codes over a serial information channel.</u>" [asynchronously, serially receiving second serial data]." Col. 2, lines 34-39. "A driver 20 (e.g., amplifier [of interface 10c] receives from the receiving channel signals representing serial data bits are [sic] clock transitions and supplies these signals to a Manchester decoder 22." Col. 4, lines 5-8.

US 8,060,675, Claim 7	US 4,450,572 Stewart (EX 1004)
	“FIG. 1 depicts a communications link [14, 16] and interface including a transmitting channel 14 and a receiving channel 16 over which a plurality of devices 12a, 12b, and 12c connect via their respective interfaces 10a, 10b and 10c.” <i>Col. 3, lines 56-60; FIG. 1 (annotated below).</i> <i>Fig. 1</i>
generating a first clock signal, for use by the first module, using the second serial data.	“Manchester-encoded data comprises data bits and clock transmissions combined in the same information signal. The decoder 22, being subsequently described, extracts the data signal (herein called data bits) and a clock (i.e., CLOCK) signal from the information signals on the channel 16 [the receive line] and supplies both the data bits and the CLOCK signal to a serial shift register 30 via conductors 26 and 28, respectively.” [Channel 16 is the receive channel and would thus be where the second serial data is received.] <i>Col. 4, lines 8-16.</i> Stewart’s decoder 22 generates the clock signal by extracting it from (i.e., using) the received Manchester encoded data (i.e., second serial data).

B. Ground 2: Claim 7 in view of Bryans

US 8,060,675, Claim 7	US 4,979,185 Bryans (EX 1006)
7. A method, comprising:	Bryans discloses that the invention is directed to a “method and device for transmitting serial data at very high speeds.” <i>Col. 1, lines 7-8.</i>
asynchronously, serially transferring first serial data,	“The encoder device 10 converts the data from parallel to serial form [first serial data] , and sends a fiber optic transmitter 12. The data is transmitted along a fiber optic cable 14 to a fiber optic receiver 16.” <i>Col. 2, lines 13-16.</i>

US 8,060,675, Claim 7	US 4,979,185 Bryans (EX 1006)
	"In addition, the system is preferably operated <u>asynchronously</u>, requiring that a sync pulse be transmitted along the serial link prior to transmission of each data word." [asynchronously, serially transferring first serial data]" <i>Col. 2, lines 41-44.</i>
corresponding to first parallel bus data,	"The encoder device 10 converts the data from parallel [first parallel bus data] to serial form, and sends to a fiber optic transmitter 12. The data is transmitted along a fiber optic cable 14 to a fiber optic receiver 16." <i>Col. 2, lines 13-16.</i>
from a first module to a second module using a serial link	"FIG. 1 shows a <u>serial communications link</u> suitable for transmitting data <u>between two parallel devices</u>." <i>Col. 2, lines 4-5.</i> "It would be desirable for a serial data link using fiber optic communications to utilize high bit rate data transmission." <i>Col. 1, lines 35-38.</i> Thus, the fiber optic cable 14 discloses a serial link, shown below in FIG. 1 (annotated).  "The encoding and decoding functions can be easily implemented on a single integrated circuit for each function." <i>Col. 1:43-45.</i> As the encoding and decoding functions, which are part of the transmit and receive portions, respectively, are on the same chip, it is understood that each parallel device includes all of the components of FIG. 1. FIG. 1, as modified below, illustrates data flow from a first module to a second module, as described in Bryans.

US 8,060,675, Claim 7	US 4,979,185 Bryans (EX 1006)
	 The diagram illustrates a data transmission system between two modules. The First Module (left) contains an Encoder (10) and a Fiber Optic Trans (12). It receives First Parallel Data (D0-D15) and outputs First Serial Data (DATA) to a Fiber Optic Trans (14). The Second Module (right) contains a Fiber Optic Rec (16), a Clock Recover (18), and a Decoder (20). It receives Second Serial Data (DATA) from the Fiber Optic Trans (14) and outputs Second Parallel Data (D0-D15). A clock extraction circuit (18) extracts the clock from the serial data and provides it to the decoder (20). The diagram is labeled Fig. 1.
asynchronously, serially receiving second serial data,	"The data is transmitted along a fiber optic cable 14 [serial link] to a fiber optic receiver 16, which presents digital data to a clock recover circuit 18. The clock recover circuit 18 extracts the clock from the data itself and presents both the CLOCK and the DATA signals to a decoder circuit 20. The decoder circuit 20 converts the <u>serial data</u> into parallel form, and outputs it on data lines D0-D15." Col. 2, lines 15-22. "In addition, the system is preferably operated asynchronously, requiring that a sync pulse be transmitted along the serial link prior to transmission of each data word." Col. 2, lines 41-42. Modified FIG. 1, below, illustrates the second serial data being received from the second module by the first module, as described in Bryans.

US 8,060,675, Claim 7	US 4,979,185 Bryans (EX 1006)
	The diagram illustrates a two-module system for data transmission. The First Module (left) contains an Encoder (10) and a Fiber Optic Trans (12). It receives First Parallel Data (D0-D15) and outputs First Serial Data. The Second Module (right) contains a Fiber Optic Rec (16), a Clock Recover (18), and a Decoder (20). It receives Second Parallel Data and outputs Second Serial Data. A fiber optic cable (14) connects the First Serial Data output to the Second Serial Data input. A dashed green box labeled 'Fig. 1' encloses both modules. A blue box labeled 'Fig. 1' highlights the clock extraction process in the Second Module, where the Clock Recover (18) extracts a clock signal from the Second Serial Data and provides it to the Decoder (20).
corresponding to second parallel bus data,	"The decoder circuit 20 converts the serial data into <u>parallel form</u>, and outputs it on data lines D0-D15." <i>Col. 2, lines 18-22.</i> [the received serial data is originally parallel bus data that was originally encoded as described above] See, e.g., <i>Col. 2, lines 11-12.</i> "A 16 bit data word [second parallel bus data] is presented to an encoder device 10 on lines D0-D15." <i>Col. 2, lines 11-13.</i>
from the second module using the serial link; and	"The data is transmitted along a fiber optic cable 14 [serial link] to a fiber optic receiver 16 [from the second module], which presents digital data to a clock recover circuit 18. The clock recover circuit 18 extracts the clock from the data itself, and presents both the CLOCK and the DATA signals to a decoder circuit 20. The decoder circuit 20 converts the serial data into parallel form, and outputs it on data lines D0-D15." <i>Col. 2, lines 18-22.</i>
generating a first clock signal, for use by the first module, using the second serial data.	"The data is transmitted along a fiber optic cable 14 to a fiber optic receiver 16, which presents digital data [second serial data] to a clock recover circuit 18. The clock recover circuit 18 extracts the clock from the data itself [generating a first clock signal . . . using the second serial data], and presents both the CLOCK and the DATA signals to a decoder circuit 20. [for use by the first module]. The decoder circuit 20 converts the serial data into parallel form, and outputs it on data lines D0-D15" <i>Col. 2, lines 18-22.</i>

C. Ground 3: Claim 7 in view of Onno

US 8,060,675, Claim 7	US 5,170,272 Onno (EX 1005)
7. A method, comprising:	Onno describes a "method" in that it discloses a processor for performing various operations, such as acting as a local controller and performing various operations such as signaling and supervisory processing functions. <i>Col. 3:25-37.</i>
asynchronously, serially transferring first serial data,	"FIG. 2 shows the general architecture of a subscriber terminal installation including a broadband digital network terminal B.NT2 and its connection means of the invention. These connection means are asynchronous optical interfaces Tb and Sb." <i>Col. 2, lines 51-55.</i> "The broadband digital network termination B.NT2 performs a switching function in order to provide local calls between terminals connected to the ports P1 to P7 of said terminal via interfaces Sb, with there being seven such interfaces in this example." <i>Col. 2, lines 61-65.</i> The communication between B.NT2 and the associated terminals connected to ports P1-P7. As noted in Onno this communication is asynchronous and done via optical interfaces, which are serial in nature. First serial data = transferred data. "Port Pi of the access module is connected to an optical interface Sb or Tb. The optical interfaces Sb or Tb use a monomode optical fiber for transmission in both directions, with the wavelengths used being 1300 nm for reception and 1500 nm for transmission [serially transferring first data]. The data rate in each direction is no greater than 600 Mbit/s, with the signal being a multiplex of asynchronous cells." <i>Col.3, lines 43-49, FIG. 2. (annotated below).</i> "The port Pi is connected to an optical duplexer 1, itself connected to an optical transmitter 2 and an optical receiver 3. . . . [a] clock signal from the data in the receive direction, with the clock module being

US 8,060,675, Claim 7	US 5,170,272 Onno (EX 1005)
	connected to a serial receive link LRS1 [serial data] at the output from the optical receiver" Col. 4, lines 7-16., See also, FIG. 4 (annotated below). FIG. 4 The diagram illustrates the internal structure of an ACCESS MODULE (MA) and its connection to a SWITCH MATRIX (MC). The MA includes a Pi input, a Tx (2) and Rx (3) pair, a CLOCK (4) and REGEN (5) block, a SCRAMBLER (6), a CELL INSERTION AND EXTRACTION (7) block, and an INTERFACE (8). Serial links LRS1 and LRS2 connect the MA to the MC. A parallel link LEP2 connects the SCRAMBLER (6) to the CELL INSERTION AND EXTRACTION (7) block. The MC includes a SWITCH MATRIX and is connected to the MA via LE and LR lines. A red arrow points to the 'Serial Transmit Link' label.
corresponding to first parallel bus data,	"A cell insert and extract circuit 7 for inserting and extracting signaling cells is connected to the parallel-series scrambler 6 by a parallel transmit link LEP2 and by a parallel receive link LRP1 to deliver data to the parallel-series circuit 6 in the transmit direction and to receive data therefrom in the receive direction." Col. 4, lines 25-31, see also, FIG. 4. [Serial data is converted to parallel data, and vice versa. Thus, data provided over parallel transmit link LEP2 is the first parallel bus data.] "[T]he transmit linked LE and the receive line LR may either be of the parallel type having four data wires at 150 Mbit/s, a wire for a clock signal at 150 MHz, and a wire for a start-of-cell signal." Col. 4, lines 44-48. [LE and LR interface with the switch matrix and therefore correspond to parallel data. This data is then converted to serial by the scrambler 6. See, e.g., FIG. 6 (annotated below), showing detailed diagram of scrambler 6.]

US 8,060,675, Claim 7	US 5,170,272 Onno (EX 1005) The diagram illustrates a system for handling first serial data. It includes a Parallel to Serial Converter (16) which receives First Serial Data (F11) and outputs First Parallel Data (F1..8). This data passes through a SCRAMBLER (18), a CALCULATE CELL PARITY (15), and a SERIAL TO PARALLEL (32) converter. The system also features a SYNC. block (30), an UN-SCRAMBLER (31a), and a PARITY CHECK (33). Various control signals like LES, SDC, HL, PC, HOE, LRS2, HR, and HOR are shown, along with bus structures LEP2 and LRP1.
from a first module to a second module using a serial link	"Broadband terminals TE in asynchronous transfer mode (only one of which is shown) are connected directly via an interface Sb to one of the ports of the termination B.NT2." Col. 3, lines 1-4. First Module = B. NT2 (FIG. 2) Second Module = TE (FIG. 2) Serial link = Sb
asynchronously, serially receiving second serial data,	"FIG. 2 shows the general architecture of a subscriber terminal installation including a broadband digital network terminal B.NT2 and its connection means of the invention. These connection means are asynchronous optical interfaces TB and Sb." Col. 2, lines 51-55. "The broadband digital network termination B.NT2 performs a switching function in order to provide local calls between terminals connected to the ports P1 to P7 of said terminal via interfaces Sb, with there being seven such interfaces in this example." Col. 2, lines 61-65. The communication between B.NT2 and the associated terminals connected to ports P1-P7 is serial in nature due to the optical interface. As noted in the specification, this communication is asynchronous and done via optical interfaces, which are serial in nature. First serial data = transferred data. "Port Pi of the access module is connected to an optical interface Sb or Tb. The optical interfaces Sb or Tb use a monomode optical fiber for transmission in both directions, with the wavelengths used being 1300 nm for reception [serially receiving second data] and 1500 nm for transmission . The data rate in each direction is no greater than 600 Mbit/s. with the signal being a multiplex of asynchronous cells." Col.3,

US 8,060,675, Claim 7	US 5,170,272 Onno (EX 1005)
	lines 43-49. "The port Pi is connected to an optical duplexer 1, itself connected to an optical transmitter 2 and an optical receiver 3. . . [a] clock signal from the data in the receive direction, with the clock module being connected to a serial <u>receive</u> link LRS1 [serial data] at the output from the optical receiver." Col. 4, lines 7-16., see also, FIGs. 3, 4 (<i>annotated below</i>). FIG. 4 FIG. 3

US 8,060,675, Claim 7	US 5,170,272 Onno (EX 1005)
corresponding to second parallel bus data,	"A cell insert and extract circuit 7 for inserting and extracting signaling cells is connected to the parallel-series scrambler 6 by a parallel transmit link LEP2 and by a parallel receive link LRP1 to deliver data to the parallel-serial circuit 6 in the transmit direction and to receive data therefrom in the receive direction." <i>Col. 4, lines 25-31, see also, FIG. 4.</i> [Serial data is converted to parallel data, and vice versa. Thus, data provided over parallel transmit link LEP2 is the first parallel bus data.] The diagram illustrates the internal components of an Access Module (MA). A dashed box labeled 'ACCESS MODULE' contains blocks 1 through 9. Block 1 is a Pi network connected to a 'Serial Link'. Block 2 is a Tx (transmit) block, and block 3 is an Rx (receive) block. A 'CLOCK' block (4) and a 'REGEN' (regeneration) block (5) are also shown. A 'SCRAMBLER' block (6) is connected to a 'Serial Transmit Link' and a 'Serial Receive Link'. A 'CELL INSERTION AND EXTRACTION' block (7) is connected to the scrambler via parallel links LEP2 (transmit) and LRP1 (receive). An 'INTERFACE' block (8) is connected to the cell insertion/extraction block via parallel links LEP1 (transmit) and LRP2 (receive). The interface block is connected to a 'SWITCH MATRIX' (9) via lines LE and LR. A 'Serial to Parallel Converter' is shown between the interface and the switch matrix. External labels include 'Parallel Data (Transmit)' pointing to LEP2, 'Parallel Data (Receive)' pointing to LRP2, and 'LC' at the bottom. "[T]he transmit link LE and the receive line LR may either be of the parallel type having four data wires at 150 Mbit/s, a wire for a clock signal at 150 MHz, and a wire for a start-of-cell signal." <i>Col. 4, lines 44-48.</i> [LE and LR interface with the switch matrix and therefore correspond to parallel data. This data is then converted to serial by the scrambler 6. See, e.g., FIG. 6 (annotated below), showing detailed diagram of scrambler 6.]

US 8,060,675, Claim 7	US 5,170,272 Onno (EX 1005) First Serial Data (corresponding to First Parallel Data) Parallel to Serial Converter FIG. 6 SCRAMBLER 6 First Parallel Data
from the second module using the serial link; and	"Broadband terminals TE in asynchronous transfer mode (only one of which is shown) are connected directly via an interface Sb to one of the ports of the termination B.NT2." Col. 3, lines 1-4. First Module = B. NT2 (FIG. 2) Second Module = TE (FIG. 2) Serial link = Sb
generating a first clock signal, for use by the first module, using the second serial data.	"A clock module 4 generates a local clock signal HL at the data rate for the transmission direction (600 Mbit/s, 150 Mbit/s, or 10 Mbit/s) and it recovers a clock signal from the data in the receive direction, with the clock module being connected to a serial receive link LRS1 at the output from the optical receiver 3." Col. 4, lines 11-16, FIG. 4 (annotated below). [The recovered clock signal is a generated first clock signal, for use by B.NT2. As the clock signal is recovered from data in the receive direction, it is done using the second serial data.] The "serial-parallel converter 32 receives the recovered clock signal HR" as shown in annotated FIG. 4, below. This discloses that the recovered clock signal is used on the first module, B.NT2, as the clock module 4 is located within access module MA, which is one of multiple access modules of B.NT2. See col. 3: 23-27 ("The terminal B.NT2 comprises a switching matrix MC, two access groups G1 and G2, and a power supply AL. Each access group includes four access modules MA each connected via a control link LC to a processor PR which acts as a local controller.") (emphasis added); see also FIG. 3.

