

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner,

v.

SHAMROCK INNOVATIONS, INC.,
Patent Owner.

IPR2023-00754
Patent 8,060,675 B2

Before SHEILA F. McSHANE, GARTH D. BAER, and
IFTIKHAR AHMED, *Administrative Patent Judges*.

BAER, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Western Digital Technologies, Inc. (“Petitioner”) filed a Petition (Paper 2, “Pet.”), requesting an *inter partes* review of claim 7 of U.S. Patent No. 8,060,675 B2 (Ex. 1001, “the ’675 patent”). Shamrock Innovations, Inc. (“Patent Owner”) filed a Waiver of Preliminary Response under 37 C.F.R. § 42.107. Paper 7. We have authority under 35 U.S.C. § 314 to determine whether to institute *inter partes* review. For the reasons discussed below, we institute *inter partes* review of the challenged claim.

II. BACKGROUND

A. RELATED MATTERS

The ’675 patent is at issue in *Shamrock Innovations, LLC v. Lenovo (United States), Inc.*, Case No. 5:22-cv-00102 (E.D. N.C.). Pet. 45, Paper 4, 1.

B. THE ’675 PATENT

The ’675 patent is titled “Computing Module with Serial Data Connectivity.” Ex. 1001, code (54). The patent is directed to a module that “can asynchronously, serially transfer first parallel bus data to another module of the computer system, and can asynchronously, serially receive second parallel bus data from another module of the computer system.” *Id.* at code (57). Patent Owner states that the ’675 patent expired on August 6, 2018. Paper 7, 1; *see also* Ex. 1001, code (63).

C. THE CHALLENGED CLAIM

Claim 7 is the only challenged and is reproduced below:

7. A method comprising:

asynchronously, serially transferring first serial data,
corresponding to first parallel bus data, from a first module to a
second module using a serial link;

asynchronously, serially receiving second serial data, corresponding to second parallel bus data, from the second module using the serial link; and
generating a first clock signal, for use by the first module, using the second serial data.

Ex. 1001, 9:63–10:6.

D. ASSERTED GROUNDS OF UNPATENTABILITY

Petitioner asserts the following grounds of unpatentability. Pet. 2.

Reference/Basis	35 U.S.C §	Challenged Claim
Stewart ¹	102(b)	7
Bryans ²	102(b)	7
Onno ³	102(b)	7

Petitioner also relies on a declaration from Dr. Michael Caloyannides (Ex. 1007).

III. ANALYSIS

A. LEVEL OF SKILL IN THE ART

Petitioner contends a person of ordinary skill in the art “would have had at least a bachelor’s degree in electrical engineering, or equivalent, with about three years of professional work experience in serial and parallel data communication within or between computing devices or systems.” Pet. 13–14 (citing Ex. 1007 ¶ 33). Petitioner also explains that “[m]ore education can supplement practical experience and vice versa.” *Id.* At this stage, Patent Owner does not provide a description of the level of ordinary skill.

¹ U.S. Patent No. 4,450,572, issued May 22, 1984 (Ex. 1004).

² U.S. Patent No. 4,979,185, issued Dec. 18, 1990 (Ex. 1006).

³ U.S. Patent No. 5,170,272, issued Dec. 8, 1992 (Ex. 1005).

Petitioner’s description is supported by credible expert testimony. For the purpose of our decision, we adopt Petitioner’s description.

B. CLAIM CONSTRUCTION

For an *inter partes* review petition filed after November 13, 2018, we construe claim terms “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b) (2021). Citing the claim’s plain language as well as support from its expert, Petitioner asserts “‘generating a clock signal . . . using second serial data’ would include ways of producing a clock signal by *using* the second serial data, such as by extracting or recovering a clock signal *from* the second serial data.” Pet. 15 (citing Ex. 1007 ¶ 37). For purposes of this decision, we agree with and adopt Petitioner’s construction.

C. DESCRIPTION OF PRIOR ART REFERENCES

1. Stewart (Ex. 1004)

Stewart discloses “an interface for coupling a computer with a data communications link that permits asynchronous bit-serial communications among devices transmitting and receiving Manchester-type codes over a serial information channel.” Ex. 1004, 2:34–39. Stuart’s Figure 1 is reproduced below.



Figure 1 “depicts a communications channel to which several devices of a data processing system connect through the interface network of the present invention.” *Id.* at 3:32–36.

2. Bryans (Ex. 1006)

Bryans discloses “[a] high bit-rate serial communications link encodes data.” Ex. 1006, code (57). Bryans’ Figure 1 is reproduced below.

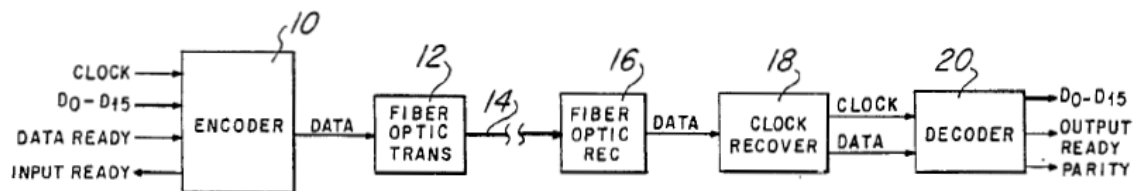


Figure 1 “shows a serial communications link suitable for transmitting data between two parallel devices.” *Id.* at 2:4–5.

3. Onno (Ex. 1005)

Onno “discloses digital network terminal[s]” that are “connected to [an] asynchronous network.” Ex. 1005, 2:56–60. Onno’s Figure 4 is reproduced below.

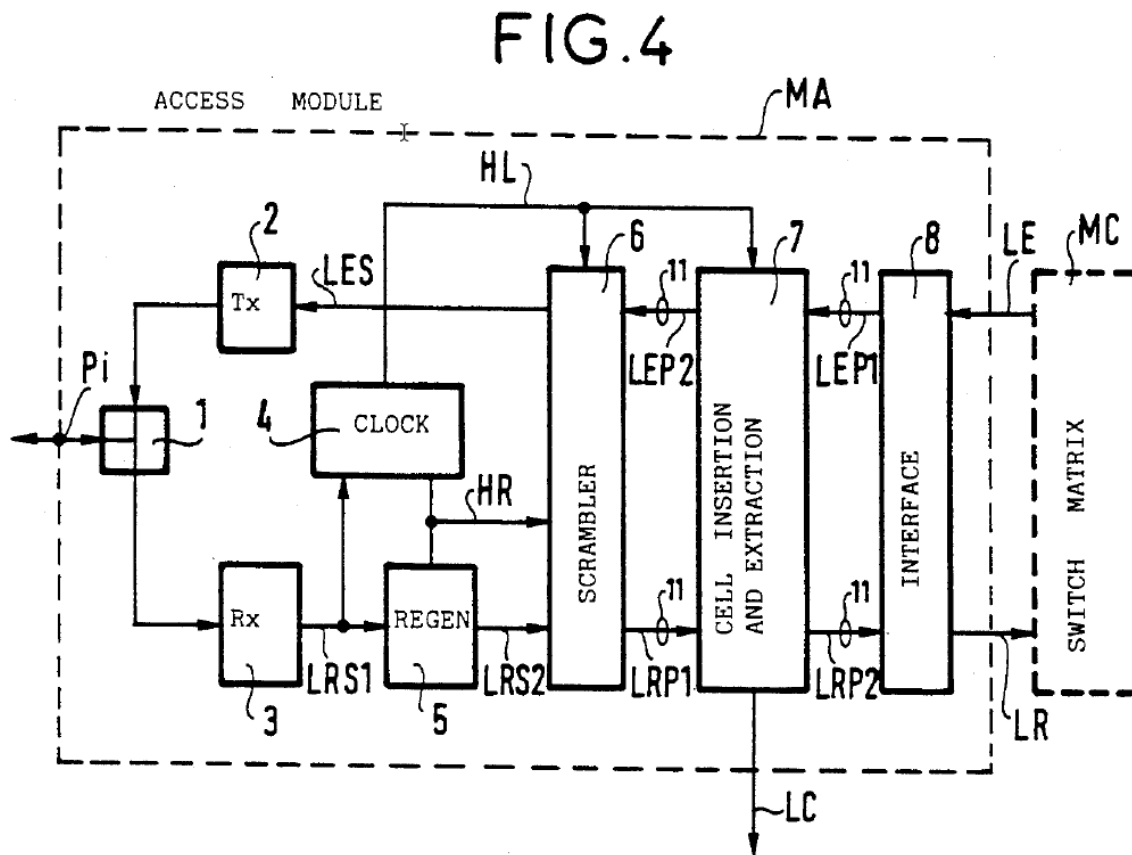


Figure 4 “shows an access module of the broadband digital network terminal.” *Id.* at 2:37–38. Figure 4 includes “parallel-series circuit 6 for scrambling” data. *Id.* at 4:20–21.

D. UNPATENTABILITY ANALYSIS

1. Anticipation of Claim 7 based on Stewart

Petitioner contends Stewart anticipates independent claim 7. Pet. 16–23. Specifically, Petitioner asserts Stewart teaches asynchronous, serial data transfer because Stewart discloses a “data communication link that permits asynchronous bit-serial communications among devices . . . over a serial

information channel.” *Id.* at 16 (quoting Ex. 1004, 2:35–39). According to Petitioner, Stewart teaches that the data corresponds to parallel bus data because Stewart also discloses a “parallel-to-serial register 47” that receives parallel data and “effects a shift on a serial basis of the data bits.” *Id.* at 18–19 (quoting Ex. 1004, 5:9–22). Petitioner presents evidence that Stewart also teaches claim 7’s corresponding receiving step because Stewart teaches that “interface 10c ‘receives from the receiving channel 16 signals representing serial data.’” *Id.* at 19–20 (quoting Ex. 1004, 4:5–7). Last, Petitioner presents evidence that Stewart teaches claim 7’s clock-signal generation step because Stewart describes that decoder 22 extracts a “***clock (i.e., CLOCK) signal*** from the information signals.” *Id.* at 22–23 (quoting Ex. 1004, 4:8–16).

We have reviewed Petitioner’s arguments and the underlying evidence cited in support and are persuaded that, at this stage, Petitioner sufficiently demonstrates a reasonable likelihood of succeeding in its anticipation challenge to claim 1 based on Stewart.

2. Anticipation of Claim 7 Based on Bryans

Petitioner contends Bryans anticipates independent claim 7. *Id.* at 23–29. Specifically, Petitioner asserts Bryans teaches asynchronous, serial data transfer because Bryans discloses a “method and device for transmitting serial data,” and that its “systems and methods are ‘preferably operated asynchronously.’” *Id.* at 23 (quoting Ex. 1006, 1:7–8, 2:41–44). According to Petitioner, Bryans teaches that the data corresponds to parallel bus data because Bryans also discloses an “encoder device 10 [that] converts the data from parallel to serial.” *Id.* at 24 (quoting Ex. 1006, 2:13–16). Petitioner presents evidence that Bryans also teaches claim 7’s corresponding receiving

step because Bryans teaches that “data is transmitted along a fiber optic cable 14 to a fiber optic receiver 16.” *Id.* at 25 (quoting Ex. 1004, 2:15–16). Last, Petitioner presents evidence that Bryans teaches claim 7’s clock-signal generation step because Bryans states that fiber optic receiver 16 “presents digital data to a clock recover circuit 18. The clock recover circuit 18 extracts the clock from the data itself and presents both the CLOCK and the DATA signals to a decoder circuit 20.” *Id.* at 27–28 (quoting Ex. 1006, 2:17–20).

We have reviewed Petitioner’s arguments and the underlying evidence cited in support and are persuaded that, at this stage, Petitioner sufficiently demonstrates a reasonable likelihood of succeeding in its anticipation challenge to claim 1 based on Bryans.

3. Anticipation of Claim 7 Based on Onno

Petitioner contends Onno anticipates independent claim 7. *Id.* at 29–41. Specifically, Petitioner asserts Onno teaches asynchronous, serial data transfer because Onno discloses “a subscriber installation based on asynchronous transfer mode,” and “a serial transmit link LES.” *Id.* at 29–30 (quoting Ex. 1005, 1:42–43, 4:22). According to Petitioner, Onno teaches that the data corresponds to parallel bus data because Onno also discloses a “parallel-series scrambler 6” that serializes parallel data. *Id.* at 32 (quoting Ex. 1005, 4:26–31). Petitioner presents evidence that Onno also teaches claim 7’s corresponding receiving step because Onno teaches “an optical **receiver** 3” that receives serial data. *Id.* at 35 (quoting Ex. 1005, 4:7–16). Last, Petitioner presents evidence that Onno teaches claim 7’s clock-signal generation step because Onno states that a “clock module 4 generates a local clock signal HL at the data rate for the transmission direction . . . and it

recovers a clock signal [HR] from the data in the receive direction.” *Id.* at 38 (quoting Ex. 1005, 4:11–15).

We have reviewed Petitioner’s arguments and the underlying evidence cited in support and are persuaded that, at this stage, Petitioner sufficiently demonstrates a reasonable likelihood of succeeding in its anticipation challenge to claim 1 based on Onno.

IV. CONCLUSION

For the foregoing reasons, we have determined that there is a reasonable likelihood that Petitioner would prevail with respect to the one challenged claim. We therefore institute trial on all grounds stated in the Petition.

V. ORDER

Accordingly, it is:

ORDERED that *inter partes* review of claim 7 of the ’675 patent is instituted on all grounds in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this decision.

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