

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG DISPLAY CO., LTD; SAMSUNG ELECTRONICS CO., LTD.; and
SAMSUNG ELECTRONICS AMERICA, INC.

Petitioners

v.

POLARIS POWERLED TECHNOLOGIES, LLC

Patent Owner

Case No. IPR2023-00771
U.S. Patent No. 7,259,521

**DECLARATION OF ALEX Z. KATTAMIS, PH.D., P.E. IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,259,521**

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I. INTRODUCTION

1. My name is Alex Kattamis. I make this declaration based upon my own personal knowledge and, if called upon to testify, would testify competently to the matters contained herein.

2. I am over the age of 21 and am competent to make this declaration.

3. I have been retained by counsel for Samsung Display Co., Ltd. (“Samsung”) to provide technical assistance in the inter partes review of U.S. Patent No. 7,259,521, (“the ’521 Patent”). This declaration is a statement of my opinions on issues related to the unpatentability of claims of the ’521 Patent.

4. I am a salaried employee of Exponent. Exponent charges \$525 per hour for my time plus expenses for work performed in connection with this project. I have received no additional compensation for work in this case, and my compensation does not depend upon the contents of this report, any testimony I may provide, or the ultimate outcome of the case.

II. EXPERIENCE AND QUALIFICATIONS

5. In formulating my opinions, I have relied upon my knowledge, training, and experience in the relevant art. My qualifications are stated more fully in my curriculum vitae, which has been provided as Ex. [1003]. My CV also lists publications on which I am a named author and identifies parties on behalf of whom

I have previously provided expert testimony within the past four years. Here, I provide a brief summary of my qualifications.

6. I am a Senior Managing Engineer in Exponent's Electrical Engineering and Computer Science practice. I received my B.A. in Electrical Engineering from the University of Connecticut in 2002 and an M.A. and Ph.D. in Electrical Engineering from Princeton University in 2004 and 2007 respectively.

7. During my time at the University of Connecticut and through a grant from the National Science Foundation I designed and implemented devices for people with disabilities. This included the design and manufacture of analog and digital control systems for devices including go-karts and electronic lifts.

8. Before joining Princeton University, I worked as a design engineering intern at General Electric Industrial Systems. There I designed and implemented analog circuits with included the implementation power supplies. The power supplies were comprised of operational amplifier circuits, filters, and transistors as well as controllers.

9. At Princeton University my research was focused on designing and fabricating pixel circuits on non-conventional substrates for driving liquid-crystal display (LCDs) and active-matrix organic light emitting diode displays

(AMOLEDs). This included the design of pixel circuits for producing stable luminance via controlled current flow.

10. Throughout my career at Exponent I have worked extensively on AMOLED and LCD displays including driver circuits, and thin-film transistor and pixel architectures.

11. I am a licensed Professional Engineer in the State of Connecticut, the State of Georgia, the Commonwealth of Massachusetts, the State of New Jersey, the State of New York, the Commonwealth of Pennsylvania, the State of Rhode Island, and in State of Texas. I am also designated a Model Law Engineer by the National Council of Examiners for Engineering.

12. I am a Senior Member of the Institute of Electrical and Electronics Engineers (IEEE), which is the world's largest technical professional organization dedicated to advancing technology for the benefit of humanity.

13. Therefore, based on my education, professional experience, scholarly books and publications, I am an expert in the relevant field of the Challenged Patent at issue here and have been an expert in this field since before the Challenged Patent was filed with the United States Patent and Trademark Office ("USPTO"). I am familiar with how a person having ordinary skill in the art would have understood and used the terminology found in the Challenged Patent at the time of its filing.

III. TASK SUMMARY AND MATERIALS REVIEWED

14. I have been asked to review the '521 Patent and its prosecution history, to provide an understanding of the technology relevant to the '521 Patent, to review certain prior-art references, and analyze whether or not those references disclose or teach limitations of claims from the '521 Patent. The opinions stated in this declaration are from the perspective of a person of ordinary skill in the art (POSA).

IV. LIST OF EXHIBITS

15. In forming my opinions, I have reviewed the '521 Patent, its prosecution history and references cited by the Examiner, the materials cited in the List of Exhibits, and the materials cited throughout my declaration.

Ex.	Description of Exhibits
1001	U.S. Patent No. 7,259,521 (“the '521 Patent”)
1003	CV of Dr. Alex Kattamis
1004	Prosecution File History of the '521 Patent
1006	U.S. Patent Publication No. 2005/0190128 (“Hayafuji”)
1007	U.S. Patent Publication No. 2005/0140600 (“Kim”)
1008	International Publication No. WO2004034365A1 (“Steer”)
1009	James W. Nilsson, et al., <i>Electric Circuits</i> (5th ed. 1996)
1010	Paul Horowitz, et al., <i>The Art of Electronics</i> (2nd ed. 1989)
1011	Willem Den Boer, <i>Active Matrix Liquid Crystal Displays – Fundamentals and Applications</i> (1st ed. 2005)
1012	Min-Koo Han, <i>AM backplane for AMOLED</i> , PROC. OF ASID (2006)

V. SUMMARY OF CONCLUSIONS AND GROUNDS FOR CHALLENGE OF '521 PATENT

16. After reviewing the materials identified in the List of Exhibits, I have concluded that each of Claims 1, 2, 3, 4, 5 and 7 of the '521 Patent would have been anticipated and/or obvious to a person of ordinary skill in the art, based on the following grounds.

Ground	Claims	Basis for Invalidity
1	1, 2 and 7	Anticipated by Kim
2	1, 2 and 7	Obvious in View of Kim and the Knowledge of a POSA
3	1 and 2	Anticipated by Hayafuji
4	1, 2, 3 and 5	Obvious in View of Hayafuji and the Knowledge of a POSA
5	1, 2, 3 and 4	Obvious in View of Steer and the Knowledge of a POSA

VI. UNDERSTANDING OF THE GOVERNING LAW

A. Level Of Ordinary Skill In The Art

17. When analyzing a patent, I understand that it is important to identify the relevant art pertaining to the patent as well as the level of ordinary skill in that art at the time of the claimed invention. The “art” is the field of technology to which the patent is related.

18. I have been instructed by counsel that the person of ordinary skill in the art (“POSA”) is a hypothetical person who is presumed to know the relevant prior art. I understand that the actual inventor’s skill is not determinative of the level of ordinary skill. I further understand that the factors that may be considered in

determining the level of skill include: the types of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field. I understand that not all such factors may be present in every case, and one or more of them may predominate.

B. Legal Standard For Claim Construction

19. I understand that the first step in determining whether a patent claim would have been anticipated or obvious is to ascertain how a POSA would have understood the claim terms.

20. I have been instructed by counsel on the law regarding claim construction and patent claims, and I understand that a patent may include two types of claims: independent claims and dependent claims. An independent claim stands alone and includes only the limitations it recites. A dependent claim can depend from an independent claim, or it can further depend from another dependent claim. I understand that a dependent claim includes all the limitations that it recites, in addition to all the limitations recited in the claim(s) from which it depends.

21. It is my understanding that in proceedings before the USPTO, the claims of a patent are to be construed under what is referred to as the “Phillips standard.” I understand that this means that claim terms of a patent are given the

meaning the terms would have to a POSA, in view of the description provided in the patent itself and the patent's file history.

22. I understand that to determine how a person of ordinary skill would understand a claim term, one should look to those sources available that show what a person of skill in the art would have understood the disputed claim language to mean. I understand that, in construing a claim term, one looks primarily to the intrinsic patent evidence, including the words of the claims themselves, the remainder of the patent, and the patent's prosecution history. I understand that extrinsic evidence, which is evidence external to the patent and the prosecution history, may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient.

23. I understand that words or terms should be given their ordinary and accepted meaning unless it appears that the inventors were using them to mean something else. In making this determination, the claims, the remainder of the patent, and the prosecution history are of paramount importance. Additionally, the patent and its prosecution history must be consulted to confirm whether the patentee has acted as its own lexicographer (i.e., provided its own special meaning to any disputed terms), or intentionally disclaimed, disavowed, or surrendered any claim scope.

24. In comparing the claims of the '521 Patent to the prior art, I have considered the '521 Patent and its file history in light of the understanding of a person of skill at the time of the alleged invention.

C. Anticipation

25. It is my understanding that the claims of a patent are anticipated by a prior art reference if each and every element of the claim is found either explicitly or inherently in a single prior art reference. I understand that inherency requires a showing that the missing descriptive matter in the claim is necessarily or implicitly present in the allegedly anticipating reference, and that it would have been so recognized by a POSA. In addition, I understand that an enabling disclosure is a disclosure that allows a POSA to make the invention without undue experimentation. Although anticipation typically involves the analysis of a single prior art reference, I understand that additional references may be used to show that the primary reference has enabling disclosure, to explain the meaning of a term used in the primary reference, and/or to show that a characteristic is inherent in the primary reference.

D. Obviousness

26. I understand that the prior art may render a patent claim "obvious." I understand that two or more prior art references (e.g., prior art articles, patents, or publications) that each disclose fewer than all elements of a patent claim may

nevertheless be combined to render a patent claim obvious if the combination of the prior art collectively discloses all elements of the claim and one of ordinary skill in the art at the time would have been motivated to combine the prior art in such a way. I understand that this motivation to combine need not be explicit in any of the prior art, but may be inferred from the knowledge of one of ordinary skill in the art at the time the patent was filed. I also understand that one of ordinary skill in the art is not an automaton, but is a person having ordinary creativity. I further understand that one or more prior art references, articles, patents or publications that disclose fewer than all of the elements of a patent claim may render a patent claim obvious if including the missing element would have been obvious to one of skill in the art (e.g., the missing element represents only an insubstantial difference over the prior art or a reconfiguration of a known system).

27. I understand that under the doctrine of obviousness, a claim may be invalid if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a POSA to which the subject matter pertains.

28. To assess obviousness, I understand that I am to consider the scope and content of the prior art, the differences between the prior art and the claim, the level of ordinary skill in the art, and any secondary considerations to the extent they exist.

29. I understand that any evidence of secondary indicia of non-obviousness should be considered when evaluating whether a claimed invention would have been obvious to one of ordinary skill at the time of invention. These secondary indicia of non-obviousness may include, for example:

- a long felt but unmet need in the prior art that was satisfied by the claimed invention;
- commercial success of processes claimed by the patent;
- unexpected results achieved by the invention;
- praise of the invention by others skilled in the art;
- the taking of licenses under the patent by others; and
- deliberate copying of the invention.

30. I understand that there must be a nexus between any such secondary indicia and the claimed invention.

31. It is also my understanding that there are additional considerations that may be used as further guidance as to when the above factors will result in a finding that a claim is obvious, including the following:

- the claimed subject matter is simply a combination of prior art elements according to known methods to yield predictable results;
- the claimed subject matter is a simple substitution of one known element for another to obtain predictable results;
- the claimed subject matter uses known techniques to improve similar devices or methods in the same way;

- the claimed subject matter applies a known technique to a known device or method that is ready for improvement to yield predictable results;
- the claimed subject matter would have been “obvious to try” choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- there is known work in one field of endeavor that may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to a POSA;
- there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent’s claims; and
- there is some teaching, suggestion, or motivation in the prior art that would have led a POSA to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed subject matter.

32. Finally, I understand that a claim may be deemed invalid for obviousness in light of a single prior art reference, without the need to combine references, if the elements of the claim that are not found in the reference can be supplied by the knowledge or common sense of one of ordinary skill in the relevant art.

VII. OVERVIEW OF THE ’521 PATENT

33. I have reviewed U.S. Patent No. 7,259,521 (“the ’521 Patent”), which is entitled “Video Driver Architecture for AMOLED Displays.” *See* Ex. [1001], the ’521 Patent.

A. Prosecution History

34. The '521 Patent had a short prosecution history with no official office action issued. *See* Ex. [1004], Prosecution File History of the '521 Patent. The application of the '521 Patent was filed on August 28, 2006. A Notice of Allowance was issued on April 13, 2007, allowing Claims 1-8, and the '521 Patent issued on August 21, 2007. *See* Ex. [1004], Prosecution File History of the '521 Patent at 1-13.

B. The Subject Matter of the '521 Patent

35. The '521 Patent relates to an AMOLED display system. This display system includes a panel which receives a video signal. Based on the video signal a video drive signal is generated which operates a current driver to supply current to an OLED.

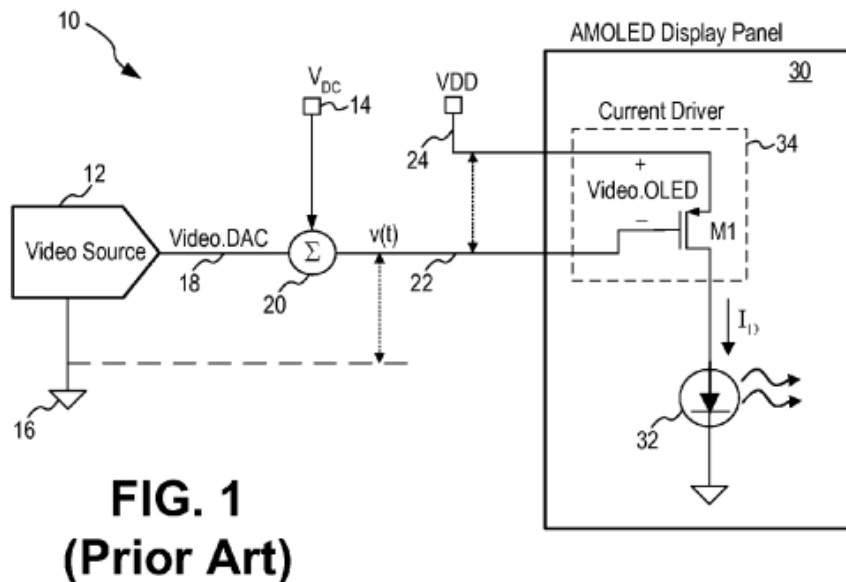
An AMOLED display system, including an AMOLED display panel receiving a video signal, includes a video driver receiving the video signal and generating a video drive signal indicative of the video signal and referenced to a positive power supply voltage of the display panel, and a current driver coupled to an OLED pixel element receiving the video drive signal and the positive power supply voltage and providing a drive current to the OLED pixel element.

See Ex. [1001], the '521 Patent at Abstract.

36. The '521 Patent further discloses that the drive current is proportional to the current drive voltage which is independent of the positive power supply voltage. *See* Ex. [1001], the '521 Patent at 3:58-57.

37. The '521 Patent's alleged invention relates to an AMOLED display system having a video driver and a pixel element. Ex. [1001], the '521 Patent at Abstract. The video driver may be either external or integrated with the display. *See* Ex. [1001], the '521 Patent at 7:52-8:2.

38. FIG. 1 depicts a diagram of a conventional AMOLED system. Ex. [1001] the '521 Patent at, 3:36-37, FIG. 1.



39. Video source 12 provides video signals (Video.DAC) to AMOLED display panel 30. Ex.[1001],1:57-59. “[V]ideo drive signal $v(t)$ is a signal that is referenced to the ground voltage (node 16).” *See* Ex. [1001], the '521 Patent at 2:2-3.

40. The purported invention references incoming video signals to the same positive power supply voltage as the display panel, instead of the ground voltage, to generate a video drive signal driving a current driver that provides current to the pixel element. *See* Ex. [1001], the '521 Patent at Abstract, FIG. 2.

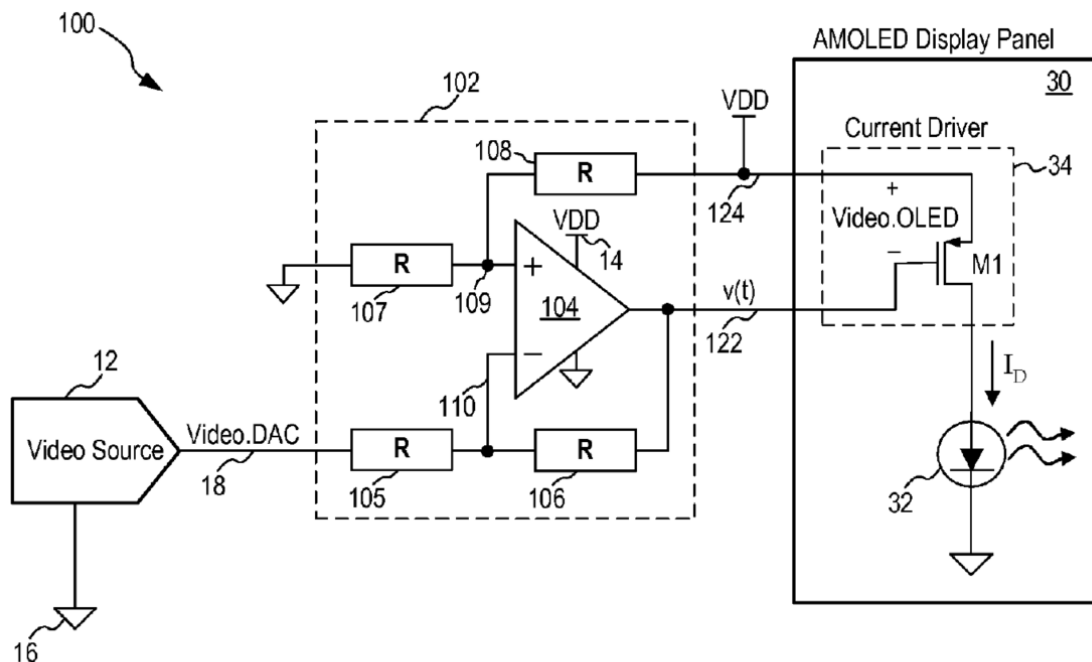
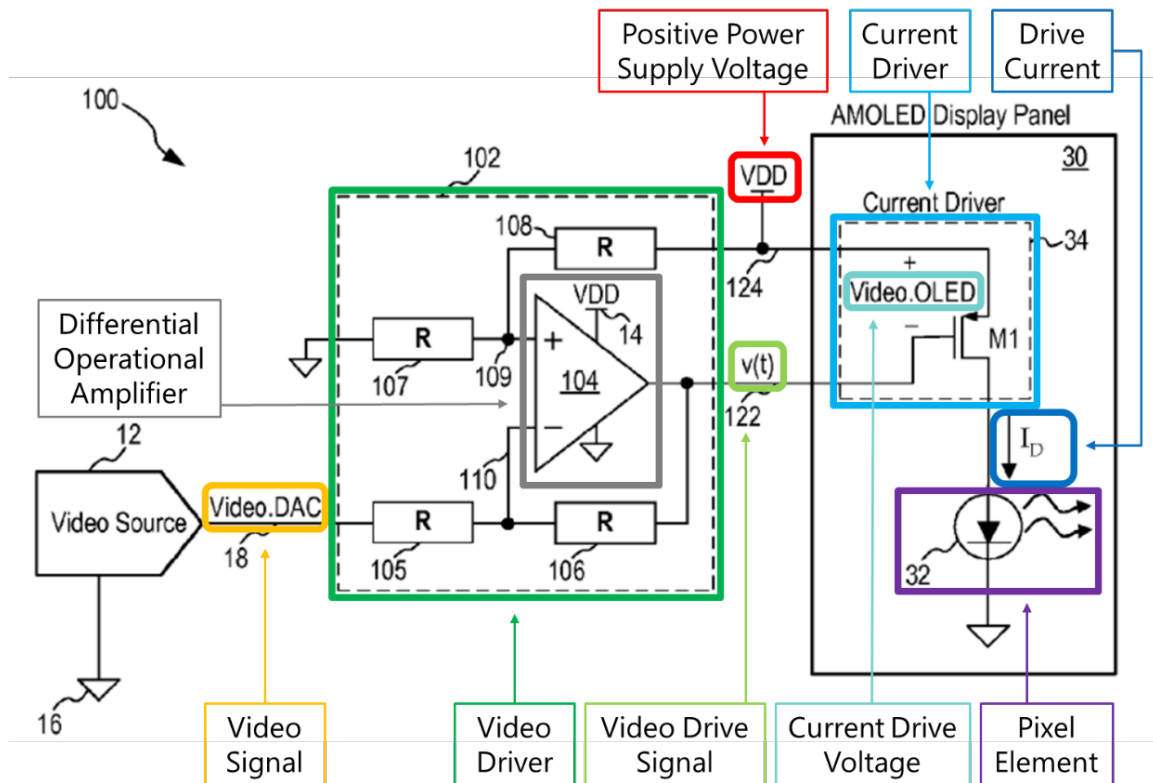


FIG. 2

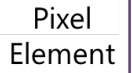
41. The '521 Patent purportedly provides a system “immune to power supply voltage variations and provides display images that are free from undesired flickers and brightness variations.” *See* Ex. [1001], the '521 Patent at 3:65-69.

42. However, video drivers referencing a video drive signal to the positive power supply voltage to eliminate or reduce effects of PPS voltage variation in display systems were well-known before the '521 Patent.

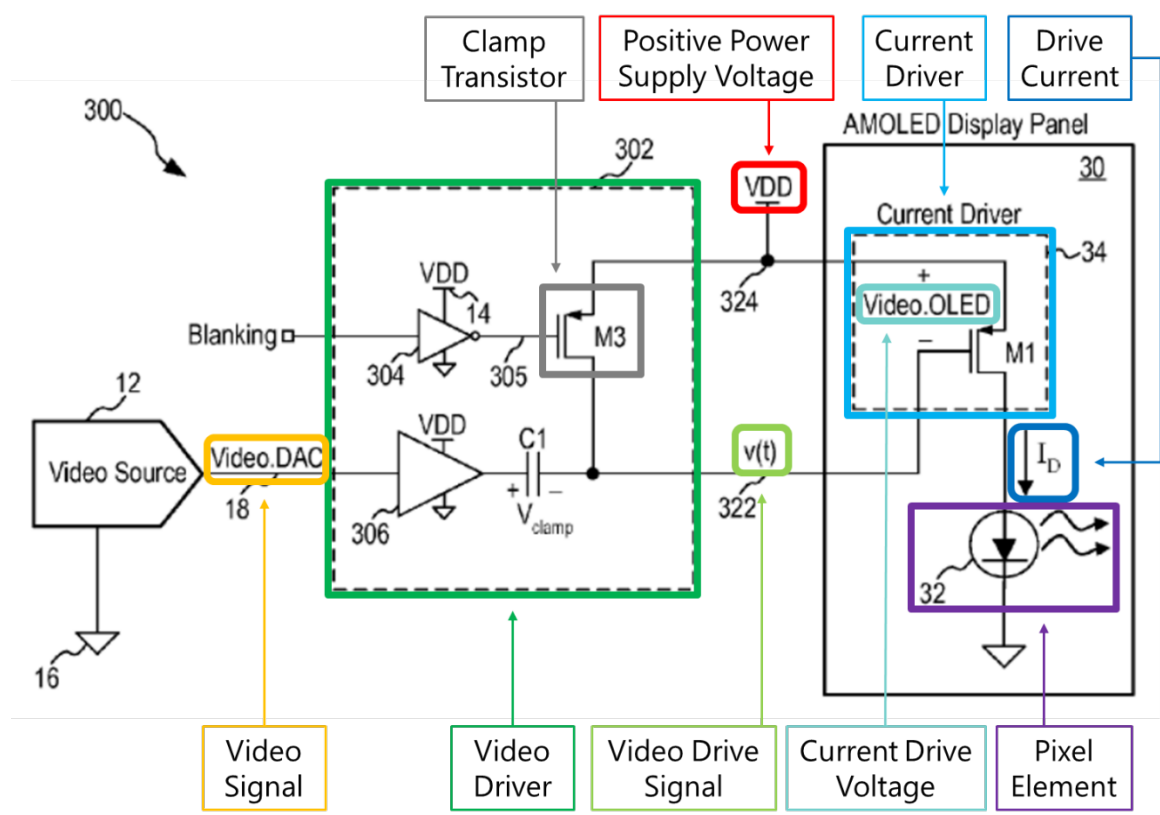
43. The '521 Patent describes three embodiments of the claimed invention.
Embodiments 1, 2 and 3 as shown below by FIG. 2 – 4 of the '521 Patent below.



See Ex. [1001], the '521 Patent at FIG. 2 (annotated).



See Ex. [1001], the '521 Patent at FIG. 3 (annotated).



See Ex. [1001], the '521 Patent at FIG. 4 (annotated).

C. The Challenged Claims of the '521 Patent

Limitation	Claim Language from '521 Patent
1-Pre	An active matrix organic light emitting diode (AMOLED) display system comprising an AMOLED display panel receiving a video signal to be displayed on the AMOLED display panel, the AMOLED display panel comprising a plurality of organic light emitting diode (OLED) pixel elements, the AMOLED display system comprising:
1-A	a video driver receiving the video signal and generating a video drive signal indicative of the video signal and referenced to a positive power supply voltage of the AMOLED display panel; and

Limitation	Claim Language from '521 Patent
1-B	a current driver coupled to at least one OLED pixel element, the current driver receiving the video drive signal and the positive power supply voltage and providing a drive current to the at least one OLED pixel element,
1-C	the drive current being proportional to a current drive voltage being indicative of the video signal and independent of the positive power supply voltage.
2	The AMOLED display system of claim 1, wherein the video drive signal is indicative of the sum of or the difference between the positive power supply voltage and the video signal and the current drive voltage is indicative of the difference between the positive power supply voltage and the video drive signal.
3	The AMOLED display system of claim 2, wherein the video driver comprises a differential instrumentation amplifier circuit for providing the video drive signal being the difference between the positive power supply voltage and the video signal.
4-Pre	The AMOLED display system of claim 3, wherein the video driver comprises:
4-A	an operational amplifier having a positive input terminal coupled to a first resistor, a negative input terminal coupled to a second resistor and an output terminal providing the video drive signal;
4-B	the first resistor being coupled between the positive input terminal of the operational amplifier and a ground voltage or a negative power supply voltage;
4-C	the second resistor being coupled between the video signal and the negative input terminal of the operational amplifier;
4-D	a third resistor being coupled between the positive input terminal of the operational amplifier and the positive power supply voltage; and
4-E	a fourth resistor being coupled between the negative input terminal and the output terminal of the operational amplifier.

Limitation	Claim Language from '521 Patent
5	The AMOLED display system of claim 2, wherein the video driver comprises a current mode isolator circuit for providing the video drive signal being the difference between the positive power supply voltage and the video signal.
7	The AMOLED display system of claim 2, wherein the video driver comprises a video clamp circuit for providing the video drive signal being the sum of the positive power supply voltage and the video signal.

VIII. LEVEL OF ORDINARY SKILL IN THE ART FOR THE '521 PATENT

44. As of August 28, 2006, a person of ordinary skill in the art (“POSA”) would have a B.S. in Electrical Engineering or equivalent field, with 3-5 years of academic or industry experience in OLED display engineering or comparable industry. Additional education could compensate for less practical experience and vice versa.

45. I believe that I would qualify as at least a person of ordinary skill in the art in the 2006 timeframe, and that I have a sufficient level of knowledge, experience, and education to provide an opinion in the field of the '521 Patent. I am familiar with what a person of ordinary skill in the art knew at that time because of my lengthy experience with engineering subjects of a similar nature to the concepts presented in the '521 Patent. Additionally, at that time, I was familiar with the general subject material in the cited prior art in this Declaration.

IX. CLAIM CONSTRUCTION

46. In my opinion, and for the purposes of this declaration, I apply the ordinary and customary meaning of the claim terms of the '521 Patent.

A. “referenced to”

47. The '521 Patent does not define “*referenced to*,” and describes many ways a signal can be “referenced to” a voltage. For example, specification describes at least the following relationships: a direct connection between a component and a voltage signal (e.g. at 2:20-23, 5:63-65); an indirect connection between multiple voltage signals (e.g. at 2:1-14, 3:55-58); a voltage differential’s minuend value (e.g. at 2:34-37); and a driver functionality (e.g. at 4:55-60). *See* Ex.[1001], the '521n Patent. A POSA would understand that claim terms should be understood based on the intrinsic record, and would therefore understand the claimed “*referenced to*” requirement to include these possibilities.

B. “independent of the...power supply voltage”

48. The claims require a current drive voltage that is independent of the positive power supply voltage. However, a POSA would understand that for any drive current to flow, there must a power supply voltage (e.g. with reference to Figure 2 of the '521 Patent, with no power supply voltage VDD, no current will flow through drive transistor M1). *See* Ex.[1001], the '521 Patent at FIG. 2.

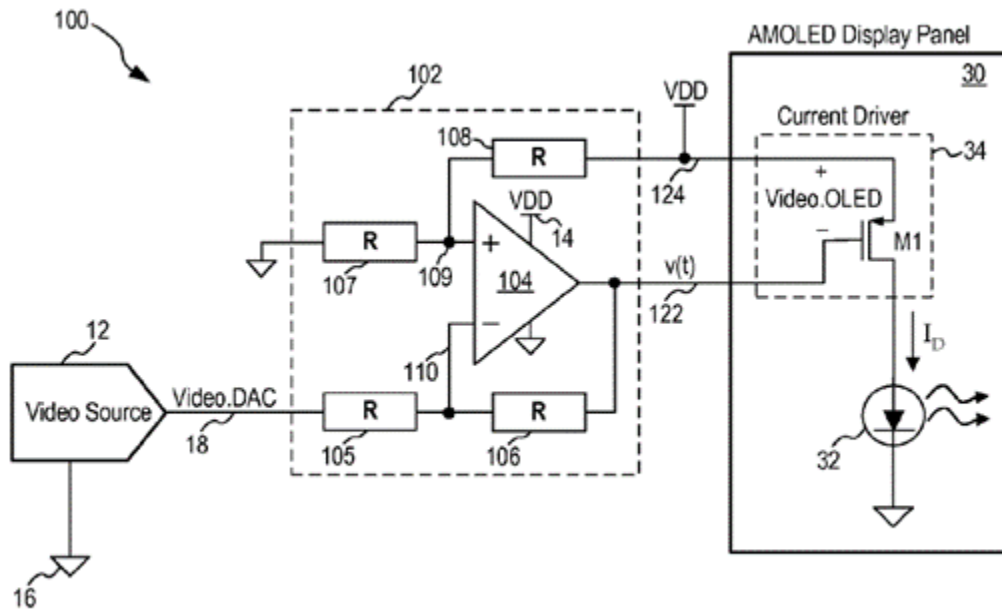


FIG. 2

See Ex.[1001], the '521 Patent at FIG. 2.

49. Instead, a POSA would understand this term to mean, consistent with the '521 Patent specification, that “noise or DC drifts in the power supply voltage...will not disturb the current drive signal...and will not affect the brightness” of the display; and, similarly, “[v]ariations in the power supply voltage V_{DD} will no longer adversely affect the” display. See Ex.[1001], the '521 Patent at 6:6-7, 5:18-23, 2:63-65.

X. TECHNOLOGY BACKGROUND AND STATE OF THE ART FOR THE '521 PATENT

50. In the subsections below, I describe some of the basic principles of electrical engineering that would have been well-known to a POSA in 2006 timeframe, and long before.

A. Exemplary References Corroborating The General Engineering Knowledge

a) Nilsson Text (Ex. [1009])

51. As an example of general electrical engineering knowledge regarding circuit design, Ex. [1009] is a textbook published in 1996 entitled “Electric Circuits,” and authored by James Nilsson et al. (“Nilsson Text”). This textbook is an introduction to electric circuits and is used a college textbook. I used this textbook during my sophomore year at the University of Connecticut. The course that relied on this text was a required for the B.S.E. program.

b) Horowitz Text (Ex. [1010])

52. As an example of general electrical engineering knowledge regarding circuit design, Ex. [1010] is a textbook published in 1989 entitled “The Art of Electronics,” and authored by Paul Horowitz et al. (“Horowitz Text”). This textbook covers electronics and is intended as a reference book and electronic circuit design textbook. I have relied on this textbook throughout my career as an electrical engineer as a reference when designing circuits.

c) den Boer Text (Ex. [1011])

53. As an example of engineering knowledge pertaining to flat-panel displays, Ex. [1011] is a textbook published in 2005, entitled “Active Matrix Liquid Crystal Displays: Fundamentals and Applications,” by Willem den Boer (“den Boer Text”). This book memorializes the state of the art of flat-panel displays as of 2005, including liquid crystal displays and organic electroluminescence displays, and provides a perspective of the knowledge of one of ordinary skill. In this book, thin-film-transistors, drive electronics, and drive methods, including compensation methods used for high-speed performance, are discussed in terms of their development, solutions to problems associated with increases in display size, and the rapid developments in these technologies.

d) Han Article (Ex. [1012])

54. As an example of specific pixel circuit design general engineering knowledge pertaining to flat-panel display, Exhibit [1012] is a paper published by the Asian Society for Information Display (“ASID”) in 2006, entitled “AM backplane for AMOLED,” by Min-Koo Han (“Han Article”). I am familiar with the Journal of the Society of Information Display and ASID is the Asian branch of the SID.

B. Transistors and Op-Amps

55. A transistor is a three-terminal device that allows for amplification or perform as electronic switch.

56. A transistor is a 3-terminal device available in 2 flavors (npn and pnp), with properties that meet the following rules for npn transistors (for pnp simply reverse all polarities):

Rule 1. The collector must be more positive than the emitter.

Rule 2. The base-emitter and base-collector circuits behave like diodes (Fig. 2.2). Normally the base-emitter diode is conducting and the base-collector diode is reverse-biased, i.e., the applied voltage is in the opposite direction to easy current flow.

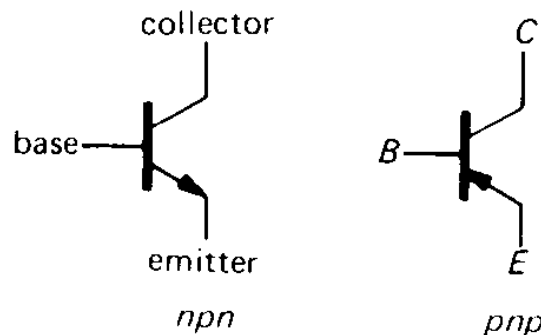


Figure 2.1. Transistor symbols, and small transistor packages.

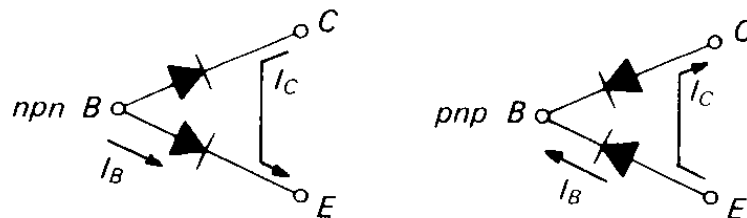


Figure 2.2. An ohmmeter's view of a transistor's terminals.

See Ex. [1010], Horowitz at p. 62.

Rule 3. Any given transistor has maximum values of I_C (collector current), I_B (base current), and V_{CE} that cannot be exceeded without costing the exceder the price of a new transistor.

Rule 4. I_C (collector current) is roughly proportional to I_B (base current) and can be written as

$$I_C = h_{FE} I_B = \beta I_B$$

where h_{FE} the current gain (also called betta), is typically about 100. Both I_C (collector current) and I_E (emitter current) flow to emitter.

See Ex. [1010], Horowitz Test at pp. 62.

57. One of the typical uses for a transistor is being a switch. A current flows across the collector- emitter path whenever voltage is applied to a transistor's base. If there's no voltage applied to the base, the switch is off, and if the voltage is applied to the base, the switch is on.

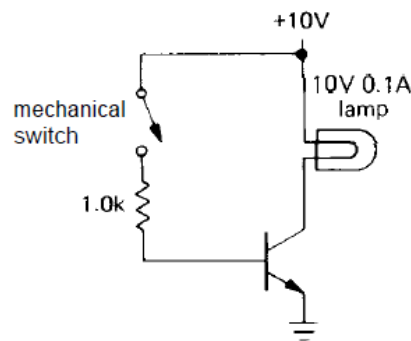


Figure 2.3. Transistor switch example.

Look at the circuit in Figure 2.3. This application, in which a small control current enables a much larger current to flow in another

circuit, is called a transistor switch. From the preceding rules it is easy to understand. When the mechanical switch is open, there is no base current. So, from rule 4, there is no collector current. The lamp is off.

See Ex. [1010], Horowitz Text at pp. 63.

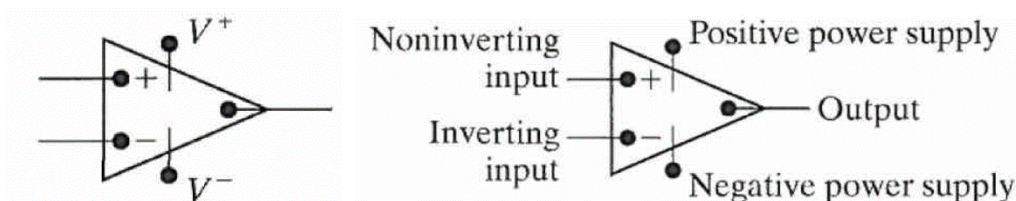
58. The operation and application of the transistor in the circuit would be customary to POSA. Respectively, it would have been well within routine activities of a POSA to design and implement specific transistor for common usage scenarios, including transistor performing as a switch.

59. The operational amplifier (“op-amp”) is an electrical component, and a well-known building block for analog circuits to any Electrical Engineering undergraduate.

The operational amplifier first came into existence as a basic building block in analog computers. It was referred to as *operational* because it was used to implement the mathematical operations of integration, differentiation, addition, sign changing, and scaling.

See Ex. [1009], Nilsson Text at pp. 177-178.

60. The circuit symbol for an op-amp below shows its five terminals as well as a simplified symbol indicating abbreviated terminal naming convention.



See Ex. [1009], Nilsson Text at p. 179.

61. Perhaps the most basic circuits that can be implemented with the op-amp are those of the inverting and non-inverting amplifiers. These amplifiers allow for signal gain as described below.

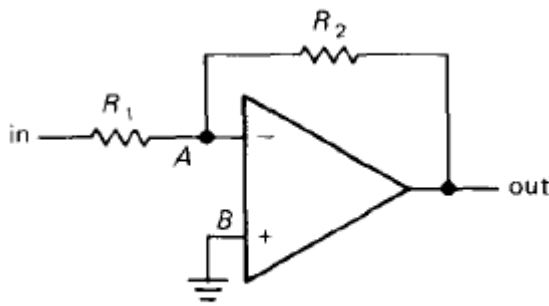


Figure 4.4. Inverting amplifier.

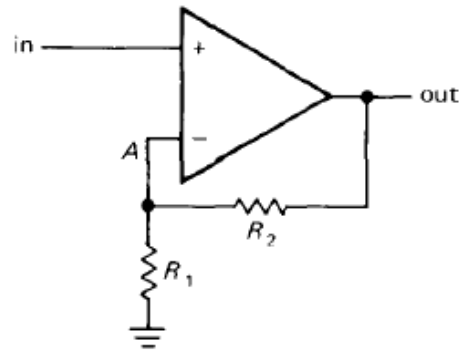


Figure 4.5. Noninverting amplifier.

See Ex. [1010], Horowitz Text at p. 178.

62. For the case of the inverting amplifier the voltage gain is given by:

$$\text{voltage gain} = \frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}$$

and for the case of the noninverting amplifier the voltage gain is given by:

$$\text{voltage gain} = \frac{V_{out}}{V_{in}} = 1 + \frac{R_2}{R_1}$$

63. As can be seen above for the inverting amplifier the amplified signal is of opposite sign from the input signal. Furthermore, the gain is set by the selection of R1 and R2.

64. Along with these amplifiers, and as explained above in the Nilsson Text op-amps are used for mathematical operations. Two important examples of such circuits are the differential amplifier and the summing amplifier.

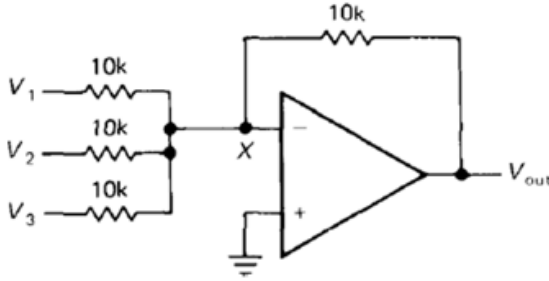


Figure 4.19. Summing amplifier.

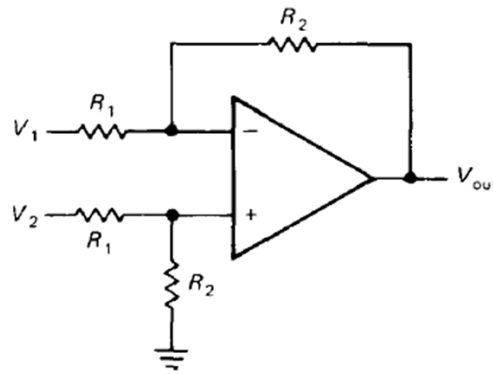


Figure 4.18. Classic differential amplifier.

See Ex. [1010], Horowitz at pg. 185.

65. For the case of the summing amplifier the voltage gain is given by:

$$V_{out} = -(V1 + V2 + V3)$$

and for the case of the differential amplifier the voltage gain is given by:

$$V_{out} = \frac{R2}{R1}(V2 - V1)$$

66. Thus, the use of such op-amp circuits and their implementation would be well known to POSA. More specifically, it would have been well within the routine activities of a POSA to design and implement application specific differential and/or summing amplifiers for a host of common usage scenarios including single processing and noise mitigation.

C. Active-Matrix Displays

67. In 2006, there were many flat panel display technologies, including liquid crystal displays (LCDs) and organic light-emitting diode (OLED) displays. To enable those displays, particularly active-matrix display technologies, switches in the form of electronic transistors were well known, including a subcategory of transistors called thin-film transistors (TFT). *See* Ex. [1011], den Boer Text at p. 29-39. It was known that an active-matrix display includes arrays of TFTs that worked with pixels, source (data) lines, and gate drivers. *See* Ex. [1011], den Boer Text at 39-43. As an example, it was known that an HDTV could have “1080x1920 pixels.” *See* Ex. [1011], den Boer Text at 176. Therefore, in such a known device, there would be 6,220,800 pixels ($1920 \times 1080 \times 3$) that are actively controlled to create an image.

68. It was also known to drive the pixels using a “TFT pixel array circuit (Fig. 2.17) [with] select buslines, data buslines, a TFT at each pixel, and a storage capacitor ... at each pixel.” *See* den Boer Text at 39-40. The storage capacitor “acts as a buffer,” helping control gray level of pixels. *See* Ex. [1011], den Boer Text at 27, 39. It was known that panels also include source drivers that use red-green-blue data to drive the columns of lines running vertically in the displays and provide the value of brightness required of each pixel. The gate or row drivers select the rows

of lines running horizontally within the displays, and they turn on the switches within pixels of each row in a row-by-row succession. *See* Ex. [1011], den Boer Text at p. 93-98.

D. OLED Pixel Circuits

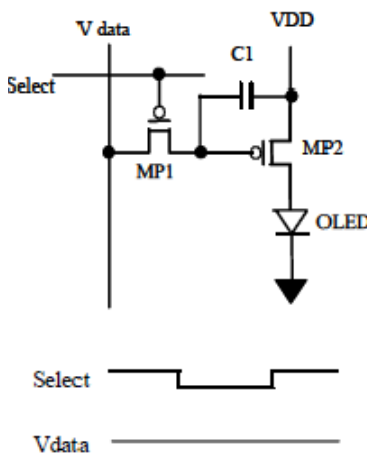
69. OLEDs are semiconducting devices comprised of organic materials that convert electrical energy to light, much like LEDs. In OLED displays, the individual pixels comprise OLEDs that are current-driven devices, which means that a given OLED's brightness is set by a fixed current. *See* Ex. [1012], Han at p. 53. It was known that a pixel's color and brightness are electronically adjusted by setting the current and therefore brightness of each pixel through the manipulation of TFT(s). For OLEDs to emit at a constant level the current must be kept constant.

70. It was known that if any pixels had non-uniform characteristics, that could lead to dark dots, bright dots, and other undesirable characteristics in the display. However, it was known that flat-panel displays are made with motherglass, in which microelectronics circuits (including the TFTs) are fabricated across several square meters of surface, and variations in electronic characteristics or properties are inevitable. *See* Ex. [1012], Han at p. 53 (Introduction). Because of known variations in the electronic characteristics across the motherglass and variations in the characteristics of TFTs, it was known to use compensation and calibration to adjust

for the variations. *See* Ex. [1012], Han at p. 53 at Abstract (“A number of TFT active matrix pixel circuits have been developed in order to compensate for TFT parameter variations”), Introduction (“Poly-Si TFT pixel circuit should compensate the non-uniform characteristics of the current, which originate from the inherent process variation of the crystal growth in polycrystalline film.”).

e) Voltage and Current Programming

71. The conventional OLED drivers relied on 2 TFTs as shown below.



See Ex. [1012], Han Article at Fig. 1(a).

72. In this configuration transistor MP2 drives the current for the OLED, and transistor MP1 is a switch that samples and holds the voltage on the storage capacitor C1. It was known that variations in TFT threshold voltage and series resistances change the current output to the OLED and therefore change the display brightness. For example, Figure 1(b) of Han reports “brightness non-uniformity (17%) of the conventional 2-TFT pixel.” *See* Ex. [1012], Han at p. 54. To

compensate for this non-uniformity, current programming schemes have been developed. It was known that to compensate for variation in TFT threshold voltage and mobility, current programming was used for driving OLEDs. *See* Ex. [1012], Han at p. 53 (“The current programming pixel circuits can compensate mobility variation as well as threshold voltage variation”). It was known that using current-programming, a current (as opposed to a voltage) is supplied to the pixel to charge a storage capacitor. A basic current-programming circuit (Fig. 5 of the Han) is shown below. In this circuit, the current I_{Data} charges capacitor C1 of the driving TFT until transistor MN2 can turn on. By using a current source I_{Data} to program the pixel, the current charging capacitor C1 remains constant even if there are variations in TFT threshold voltage or mobility.

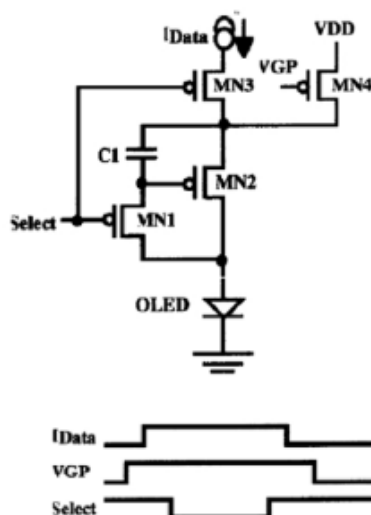


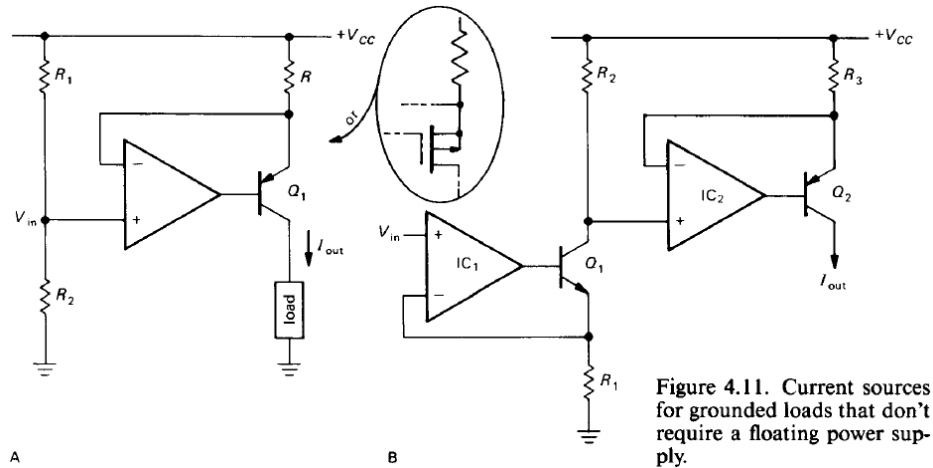
Figure 5. The reported current programming AMOLED pixel in which I_{DATA} is memorized and V_{GATE} of MN2 is determined to allow I_{DATA} [2].

See Ex. [1012], Han at Fig. 5.

E. Op-Amps as Current Supplies

73. It was well known that op-amp circuits could be used to build current sources for supplying loads such as OLEDs. The circuit shown in Figure 4.11A of the Horowitz Text is ordinary and well known and is often called a V-I (voltage-to-current) converter, or equivalently, a voltage-controlled current source. This circuit generates a current that easily adjustable by the user; the user chooses a value for resistor R , then sets the voltage V_{in} by some means, be it via a digitally-controlled DAC, a mechanically-adjustable potentiometer, or some other means. Thus, using this simple, well-known circuit, one can provide a well-defined, controllable current to a load, even if the impedance of that load is not known in advance or if it is likely to change over time. Controllable current delivery with load-insensitivity is the key feature of this circuit.

74. Furthermore, the concept of referencing the positive terminal input voltage of the op-amp via a resistive divider connected between V_{DD} and ground was known. The delivery of current to a load via a FET device, with gate of said FET driven by an op-amp, is also disclosed as shown in Figure 4.11A of Horowitz.



See Ex. [1010], Horowitz Text at pg. 181.

75. The Horowitz Text also teaches using an op-amp in feedback to control the gate voltage of a PFET, and thus control the current delivered to a load. In Figure 4.11 B, teaches a means of using a FET to deliver current to a load that does not depend on the supply level, and is thus insensitive to possible supply fluctuations.

XI. OVERVIEW OF THE PRIOR ART TO THE '521 PATENT

A. Hayafuji

76. U.S. Patent Publication No. 2005/0190128 ("Hayafuji") was filed on February 3, 2005 and published on September 1, 2005. As such, I understand that Hayafuji is prior art under §102(a).

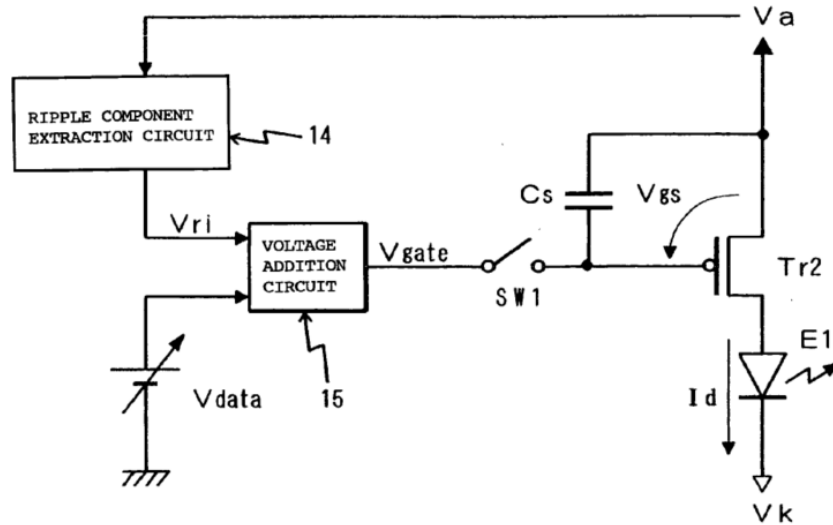
77. Hayafuji is directed to a drive device for a light emitting display panel. See Ex. [1006], Hayafuji at ¶ 0047, ("A drive device of a light emitting display panel

according to the present invention will be described below with reference to the embodiments shown in the drawings.”).

78. Hayafuji discloses that the drive device and method of a light emitting display panel in which deterioration of the display quality of an image caused by a ripple component generated in a power supply circuit represented by a DC-DC converter can be effectively reduced without increasing the circuit scale. *See* Ex. [1006], Hayafuji at ¶ 0047, (“a structure which is allowed to have ripple component supply means that the present invention is characterized, in a pixel structure of a conductance control method, similarly to the equivalent circuit shown in FIG. 2 already described.”).

79. Using a similar concept described in the '521 Patent, Hayafuji explains that a circuit (*see* Ex. [1006], Hayafuji at FIG. 6) can be used to extract the ripple component V_{ri} included in a drive voltage V_a and provided to an input terminal of a voltage additional circuit 15 such that the gate voltage V_{gate} includes the voltage variations, which compensates for the variations.

FIG. 6



See Ex. [1006], Hayafuji at FIG. 6.

In the embodiment shown in FIG. 6, a ripple component extraction circuit 14 and a voltage addition circuit 15 are provided and are constituting the ripple component supply means. The ripple component extraction circuit 14 extracts a ripple component included in a drive voltage V_a generated by the above-described DC-DC converter, and a ripple component V_{ri} extracted by this ripple component extraction circuit 14 is supplied to one input terminal of the voltage addition circuit 15. The data voltage V_{data} transmitted via the above-mentioned data line B1 is input to the other input terminal of the voltage addition circuit 15.

See Ex. [1006], Hayafuji at ¶ 0048.

B. Kim

80. U.S. Patent Publication No. 2005/0140600 (“*Kim*”) was filed on August 16, 2004 and published on June 3, 2005. As such, I understand that Kim is prior art under §102(a).

81. Kim is directed to a light emitting display that includes a plurality of data and select lines along with pixel circuits.

In an exemplary embodiment of the present invention, a light emitting display includes a plurality of data lines for transmitting data voltages corresponding to video signals, a plurality of scan lines for transmitting select signals, and a plurality of pixel circuits. each said pixel circuit is coupled to a corresponding said data line to receive a corresponding said data voltage and a corresponding said scan line to receive a corresponding said select signal.

See Ex. [1007], Kim at ¶ 0017.

82. Kim further discloses that a transistor coupled between the power supply voltage and an OLED controls the current flowing into the OLED. *See* Ex. [1007], Kim at ¶ 0008. *See also* Ex. [1007], Kim at ¶ 0009, (“Accordingly, the current I_{OLED} corresponding to a voltage V_{GS} charged by the capacitor C_{st} between the gate and the Source of the transistor M_a flows through the transistor M_a , and the OLED emits light corresponding to the current I_{OLED} .”).

83. Kim explains that the voltage drop along the power supply line can degrade image quality. *See* Ex. [1007], Kim at ¶ 0013, (“when a voltage drop (IR-

drop) is generated on a line for supplying the power supply voltage V_{DD} , and the power supply voltage V_{DD} applied to a plurality of pixel circuits is not uniform, a desired amount of current may not flow to the OLED, thereby degrading image qualities.”).

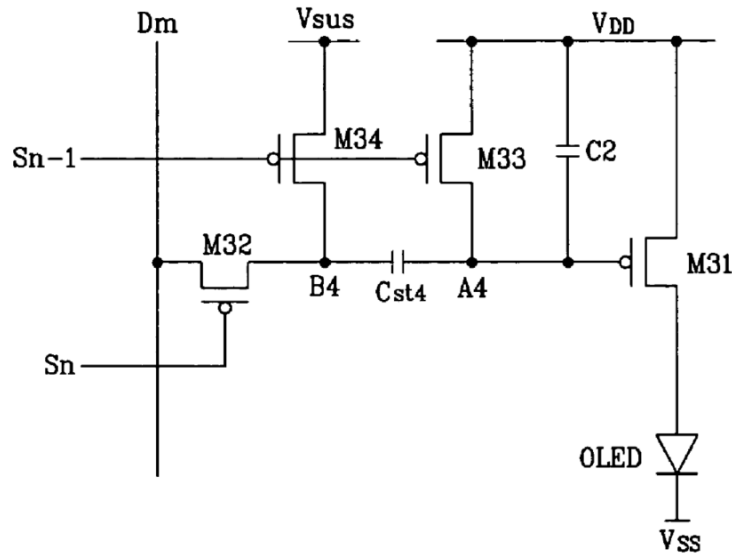
84. Kim further explains that the invention prevent the influence of power supply variations on display uniformity.

In exemplary embodiments of the present invention, a current that flows to the OLED of a pixel circuit in a light emitting display is substantially prevented from being influenced by a power supply voltage.

See Ex. [1007], Kim at ¶ 0014.

85. In one embodiment, shown below in FIG. 10, the video drive signal at A4 is referenced to the power supply voltage V_{DD} .

FIG.10



See Ex. [1007], Kim at FIG. 10.

C. Steer

86. PCT application number WO2004034365A1 (“Steer”) was filed on September 15, 2003 and first published on April 22, 2004. As such, I understand that Steer is prior art under §102(a).

87. *Steer* is directed to an active-matrix OLED display that may include OLEDs as the light emitting elements among others.

This invention relates to electroluminescent display devices, particularly active matrix display devices having thin film Switching transistors associated with each pixel.

Matrix display devices employing electroluminescent, light-emitting, display elements are well known. The display elements may comprise organic thin film electroluminescent elements, for example using polymer materials, or else light emitting diodes (LEDs) using traditional III-V semiconductor compounds.

See Ex. [1008], Steer at 1:6-14

88. Steer further discloses that a column driver provides voltage to the gate of a drive transistor to control the current through the OLED.

When the address transistor 16 is turned on, a Voltage on the column conductor 6 can pass to the remainder of the pixel. In particular, the address transistor 16 Supplies the column conductor Voltage to a current source 20, which comprises a drive transistor 22 and a storage capacitor 24. The column Voltage is provided to the gate of the drive transistor 22, and the gate is held at this Voltage by the storage capacitor 24 even after the row address pulse has ended. The drive transistor 22 draws a current from the power supply line 26.

See Ex. [1008], Steer 3:2-9.

89. Steer discloses that variations along the power supply lines negatively affect display brightness.

The significant row conductor resistance gives rise to Voltage drops is along the row conductors, and these Voltage variations along the power Supply line alter the gate-source voltage on the drive transistors, and thereby affect the bright ness of the display. Furthermore, as the currents drawn by the pixels in the row are image-dependent, it is difficult to correct the pixel drive levels by data correction techniques, and the distortion is essentially across talk between pixels in different columns.

See Ex. [1008], Steer at 4:14-20

90. Furthermore, Steer explains that in embodiments of the present invention “the control line voltage can be controlled in closed loop manner to achieve the desired current.” *See* Ex. [1008], Steer at 5:13-15.

91. In one embodiment, shown below in Figures 3 and 4, the power supply (V_{SUPPLY} and line 26) is used to generate the video drive signal and the current drive voltage therefore rendering current drive voltage independent of the positive power supply.

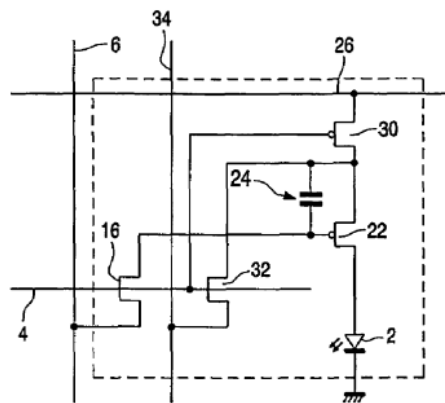


Fig.3

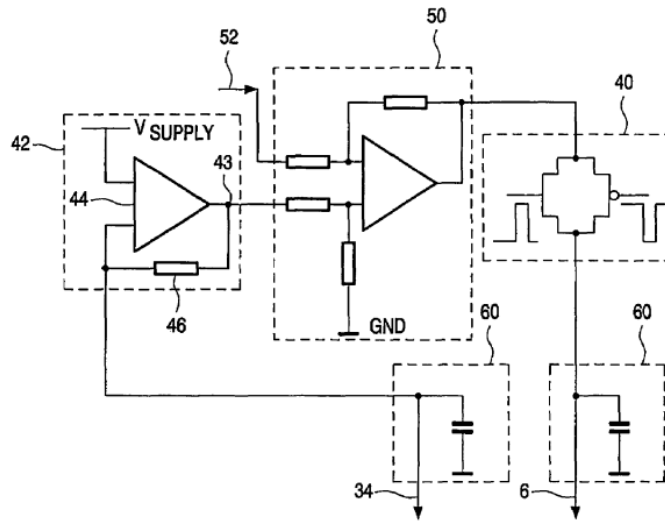


Fig.4

See Ex. [1008], Steer at FIGS. 3-4.

XII. ASSERTED GROUNDS OF INVALIDITY

A. Grounds 1 and 2: Claims 1, 2, and 7 of the '521 Patent are Anticipated or Rendered Obvious by Kim

92. The figure below is an annotated reproduction of FIG. 4 of the '521 Patent illustrating the third embodiment.



See Ex. [1001], the '521 Patent at FIG. 4 (annotated).

a) Claim 1

[1-Pre]: An active matrix organic light emitting diode (AMOLED) display system comprising an AMOLED display panel receiving a video signal to be displayed on the AMOLED display panel, the AMOLED display panel comprising a plurality of organic light emitting diode (OLED) pixel elements, the AMOLED display system comprising:

93. To the extent the preamble is limiting, Kim discloses an active-matrix organic light emitting diode (AMOLED) display system comprising an AMOLED display panel receiving a video signal to be displayed on the AMOLED display

panel, the AMOLED display panel comprising a plurality of organic light emitting diode (OLED) pixel elements.

94. Kim discusses a “conventional voltage programming-type pixel circuit for driving an organic EL element (OLED),” including the functionality and operation of the conventional implementations in the context of FIGs. 1-2. The concepts and functionality discussed in Kim and depicted in FIGs. 1-5 are applicable and relied upon for the detailed embodiments disclosed in the context of the subsequent figures. For example, Kim’s discussions of transistor Ma (corresponding to transistors M1/M11/M21/M31 in later embodiments), capacitor C_{st} (corresponding to capacitor C2 in later embodiments), voltage V_{GS} (across transistors M1/M11/M21/M31), data line D_m , data voltage V_{DATA} , and PPS voltage V_{DD} , are all relevant to the disclosures of the embodiments starting at FIG. 6A and beyond. *See* Ex. [1007], Kim at FIG. 2, FIG. 6A, FIG. 6B and FIG.

FIG.2

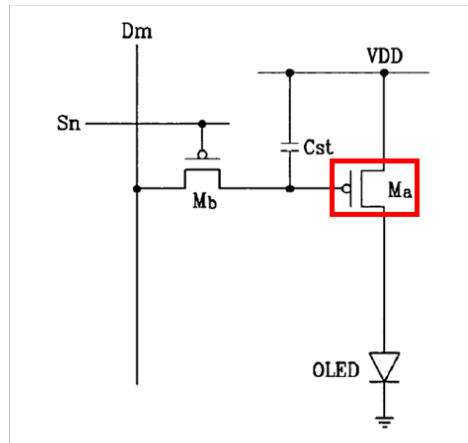


FIG.6A

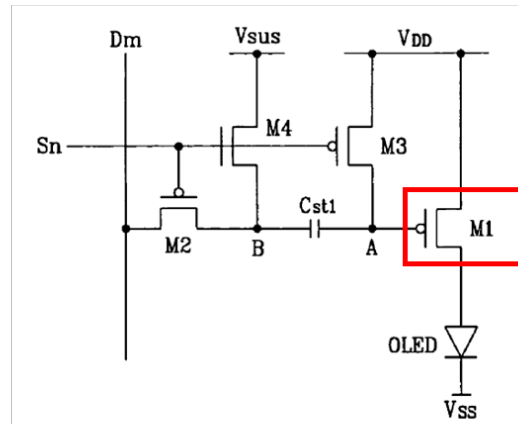


FIG.6B

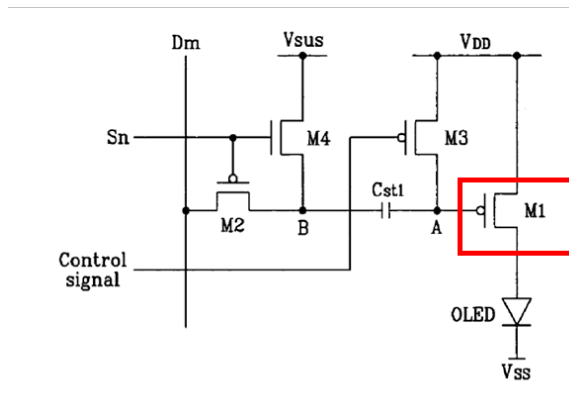
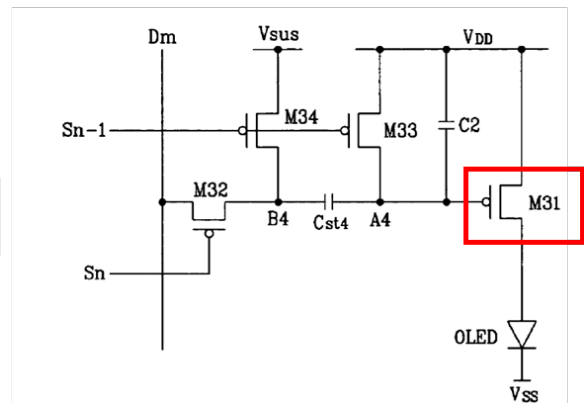


FIG.10



See Ex. [1007], Kim at FIG. 2, FIG. 6A, FIG. 6B and FIG. 10. (annotated).

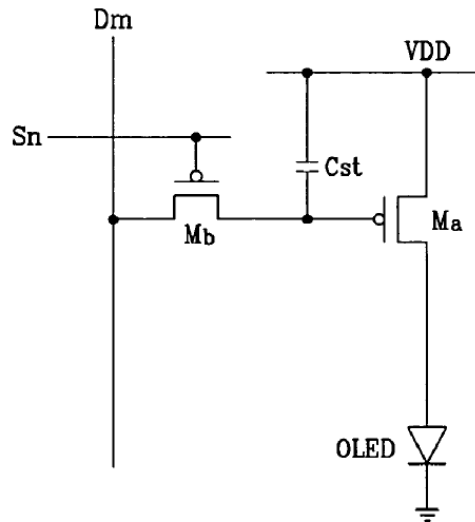
95. In all the above circuits the highlighted transistors have the same purpose, that of driving the OLED.

96. Furthermore, aspects of the first detailed embodiment discussed in the context of FIG.6A are also referred to and relied upon by subsequent embodiments. See Ex. [1007], Kim at ¶ 0105, (“In the pixel circuit of **FIG. 10**, transistors **M31**, **M32** and a capacitor C_{st4} are connected together in substantially the same

relationship as the transistors **M1**, **M2** and the capacitor C_{st1} of **FIG. 6A.**”). Therefore, although the analysis below is primarily directed to Kim’s “fourth exemplary embodiment” corresponding to FIG. 10, the concepts and discussions regarding FIGs. 1-6A are generally pertinent to the fourth embodiment in Kim as well.

97. Kim is directed to a light emitting display and driving method. *See* Ex. [1007], Kim at ¶ 0005, (“The present invention relates to a light emitting display and a driving method thereof. More specifically, the present invention relates to an organic EL (electroluminescent) display.”). *See also* Ex. [1007], Kim at ¶ 0006, (“Methods for driving the organic emitting cells include a passive matrix method, and an active matrix method using TFTs (thin film transistors) or MOSFETs.”).

98. Kim discloses among its embodiments a conventional voltage programmed pixel circuit for driving OLEDs. For example, FIG. 2 of Kim schematically describes a 2-transistor pixel circuit.



See Ex. [1007], Kim at FIG. 2

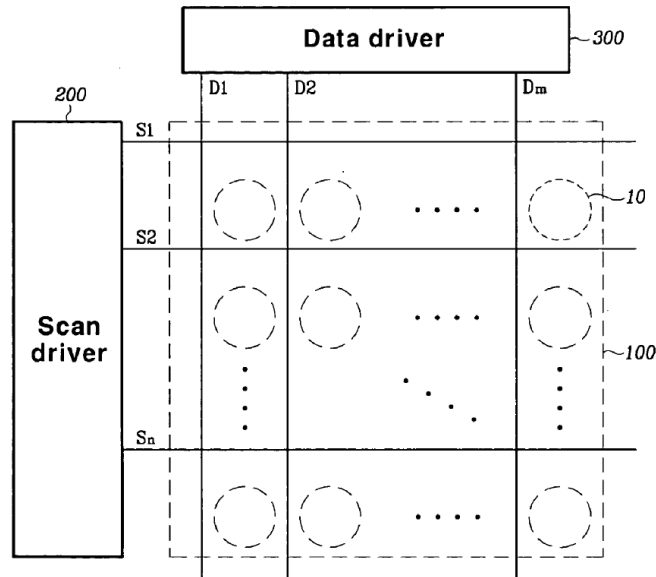
99. The operation of this circuit is well known in the art and is further described by Kim:

A transistor M_a coupled between the power supply voltage V_{DD} and an OLED controls the current flowing to the OLED. A transistor M_b transmits a data line voltage to a gate of the transistor M_a in response to a select signal applied from a scan line S_n . A capacitor C_{st} coupled between a source and the gate of the transistor M_a is charged with the data voltage and maintains the charged state for a predetermined time.

In detail, when the transistor M_b is turned on in response to a select signal applied to the gate of the switching transistor M_b , a data voltage from the data line D_m is applied to the gate of the transistor M_a . Accordingly, the current I_{OLED} corresponding to a voltage V_{GS} charged by the capacitor C_{st} between the gate and the source of the transistor M_a flows through the transistor M_a , and the OLED emits light corresponding to the current I_{OLED} .

See Ex. [1007], Kim at ¶¶ 0008-0009,

100. Kim further discloses that the display panel is comprised of a plurality of discrete pixels as shown in FIG. 3 of Kim.



See Ex. [1007], Kim at FIG. 3.

As shown, the organic EL display includes an organic EL display panel **100**, a scan driver **200**, and a data driver **300**.

The organic EL display panel **100** includes a plurality of data lines D₁ through D_m, each extending in a column direction, a plurality of scan lines S₁ through S_n, each extending in a row direction, and a plurality of pixel circuits **10**.

See Ex. [1007], Kim at ¶¶ 0045-46. See also FIG. 11.

101. Finally, Kim discloses data and scan lines that are used to bias the pixel circuits.

The data lines D_1 through D_m transmit data voltages that correspond to video signals to the pixel circuits **10**, and the scan lines S_1 through S_n transmit select signals for selecting the pixel circuits **10**.

See Ex. [1007], Kim at ¶ 46.

The scan driver **200** sequentially applies select signals to the scan lines S_1 through S_n , and the data driver **300** applies the data voltage that corresponds to video signals to the data lines D_1 through D_m .

See Ex. [1007], Kim at ¶ 0047.

102. A POSA would have recognized, consistent with FIG. 3 above, that because “data lines D_1 through D_m transmit data voltages that correspond to video signals to the pixel circuits **10**,” and also because, for example in FIG. 2 (which doesn’t include the additional video driver circuitry disclosed in Kim’s later embodiments), “data voltage from the data line D_m is applied to the gate of the transistor Ma,” and thus, “data voltage from the data line D_m ” corresponds to the claimed video signal to be displayed on the AMOLED display panel.¹

103. To the extent not anticipated, a POSA would have found it obvious that the Kim system could receive a video signal, and use that signal as the source for the

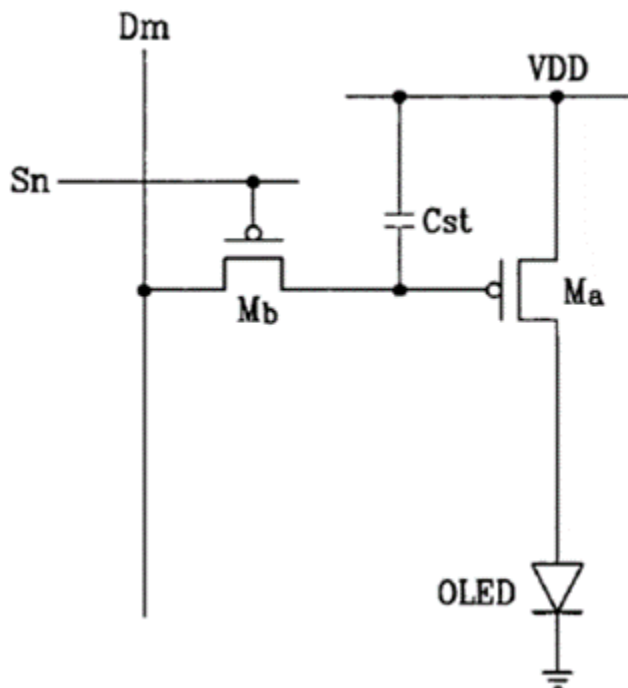
¹ Kim’s disclosure sometimes appears to use data line D_m and data voltage V_{DATA} interchangeably without clarifying that “data voltage V_{DATA} ” is the actual signal transmitted along “data line D_m ”. This is particularly apparent given that Kim’s figures always use “ D_m ” and not “ V_{DATA} ”, whereas Kim’s equations always use “ V_{DATA} ” and not “ D_m ”. A POSA would recognize, based on Kim’s disclosure, the “data voltage V_{DATA} ” which is transmitted along “data line D_m ” is what specifically corresponds to the claimed video signal.

“video signals” explicitly discussed in Kim, as a POSA would understand this is most-logical way of using the Kim system.

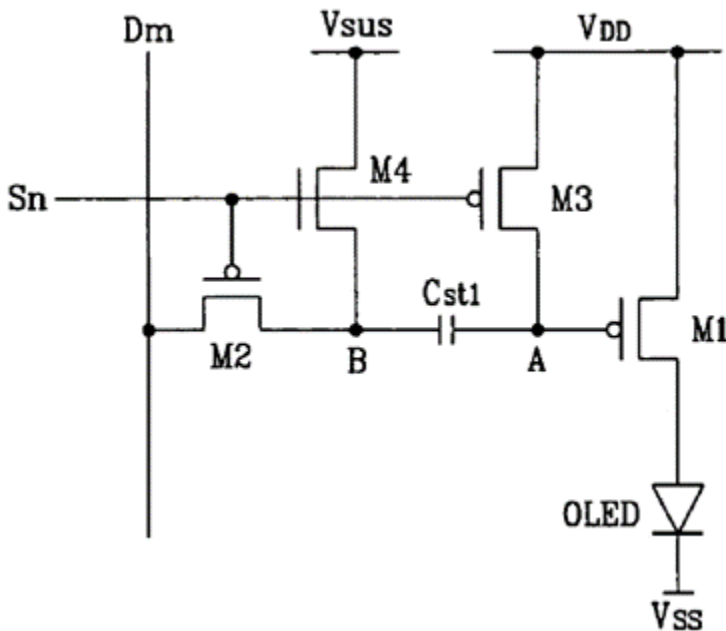
104. Therefore, Kim discloses an active matrix organic light emitting diode (AMOLED) display system comprising an AMOLED display panel receiving a video signal to be displayed on the AMOLED display panel, the AMOLED display panel comprising a plurality of organic light emitting diode (OLED) pixel elements, the AMOLED display and thus discloses limitation [1-Pre] of the '521 Patent.

105. Although the analysis below is primarily directed to Kim’s “fourth exemplary embodiment” corresponding to Figure 10, the concepts and discussions regarding Figures 1-6A are generally pertinent to the fourth embodiment in Kim. Kim specifically notes that aspects of the first detailed embodiment discussed in the context of Figure 6A are referred to and relied upon by the Figure 10 embodiment. *See* Ex. [1007], Kim at ¶ 0105 (“In the pixel circuit of FIG. 10, transistors M31, M32 and a capacitor Cst4 are connected together in substantially the same relationship as the transistors M1, M2 and the capacitor Cst1 of FIG. 6A. The capacitor Cst4 has electrodes A4 and B4 similar to the electrodes A and B of the capacitor Cst1.”). Thus, a POSA would recognize the correspondence between, for example, transistor Ma (corresponding to transistors M1/M11/M21/M31 in later embodiments), capacitor Cst (corresponding to capacitor C2 in later embodiments), voltage VGS

(across transistors M1/M11/M21/M31), data line Dm, data voltage VDATA, and PPS voltage VDD, and would further recognize that Kim's discussions of these related components are relevant to the components in other embodiments that they correspond to. Ex.[1007], ¶¶0073, 0105. The correspondence between these components, is also evident from their similar configurations in Figures 1, 6A, and 10 reproduced below. Ex.[1007], Figs. 1, 6A, 10. To the extent these disclosures are found to be distinct embodiments, it would be obvious to combine these disclosures in view of Kim's teachings and suggestions, which provide motivation to use the disclosures together in implementing variations of Kim's teachings.

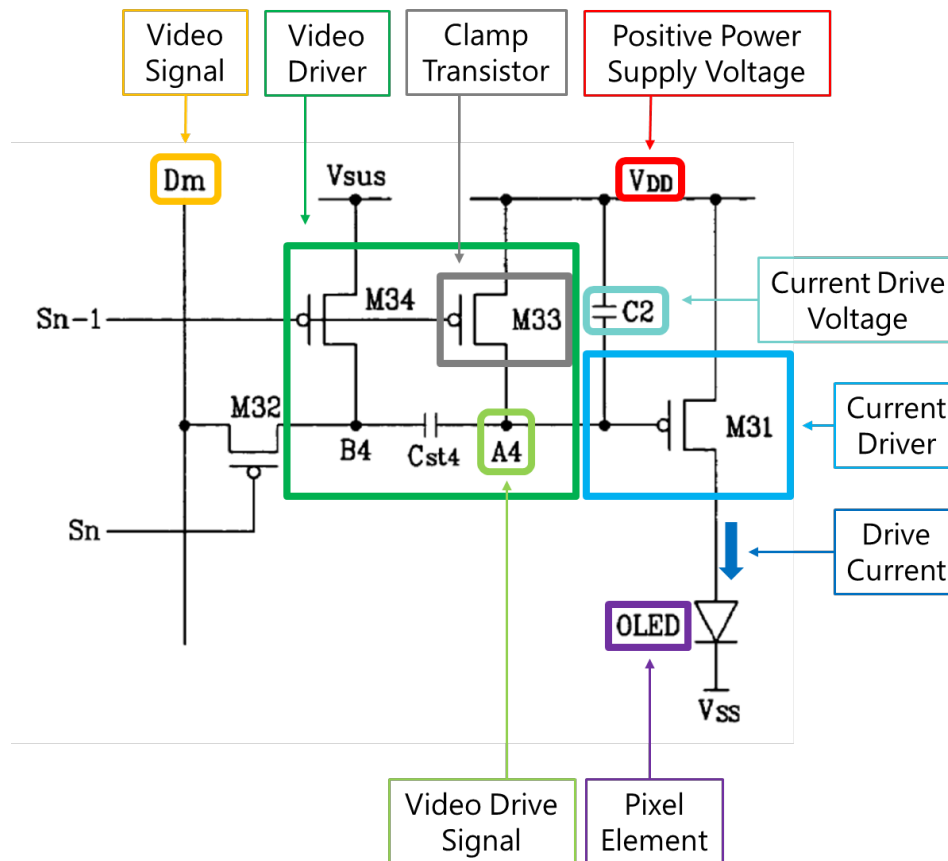


See Ex.[1007], Kim at FIG. 1.



See Ex.[1007], Kim at FIG. 6A.

106. As an example, A POSA would have recognized that Fig. 6A of Kim introduces the concept of using a series capacitor Cst to provide the video drive signal to the gate of the drive transistor in the manner described below. A POSA would have implement this technique in the manner disclosed by, for example, Fig. 10 by including capacitor C2 thus allowing for the OLED to emit for the entire frame period.



See Ex.[1007], See

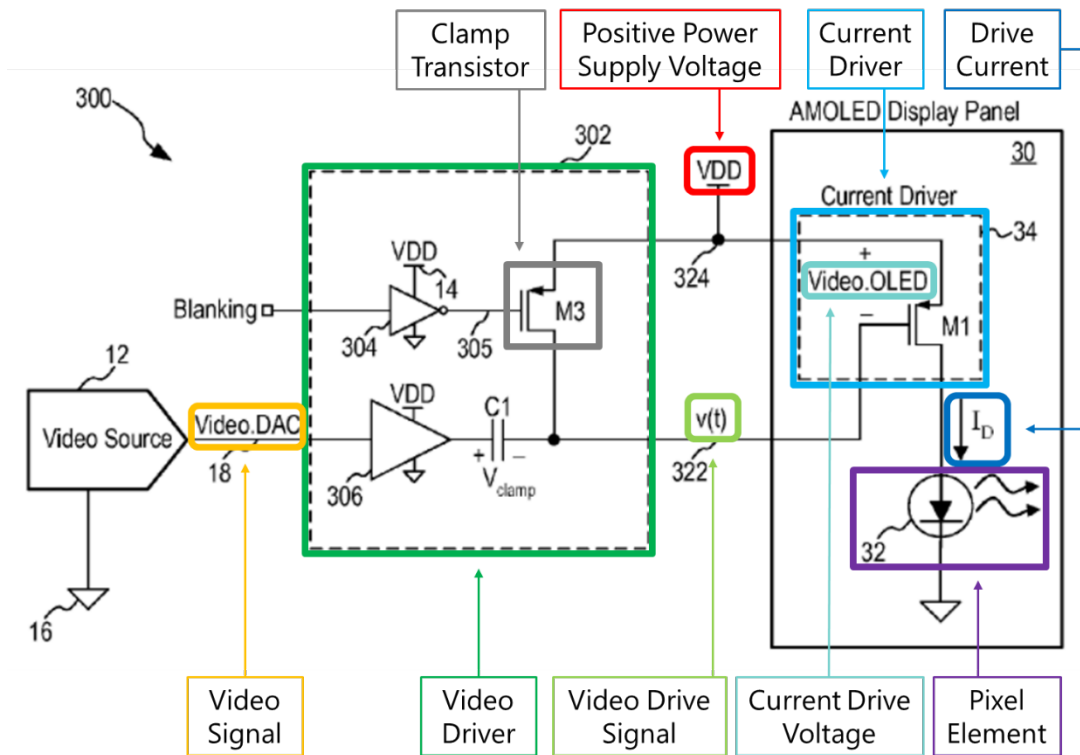
See Ex.[1007], Kim at FIG. 10.

[1-A]: a video driver receiving the video signal and generating a video drive signal indicative of the video signal and referenced to a positive power supply voltage of the AMOLED display panel; and

107. Kim discloses a video driver receiving the video signal and generating a video drive signal indicative of the video signal and referenced to a positive power supply voltage of the AMOLED display panel.

108. Regarding the claimed “video driver,” in the ’521 Patent’s third embodiment illustrated in FIG. 4 (annotated) reproduced below, the video driver

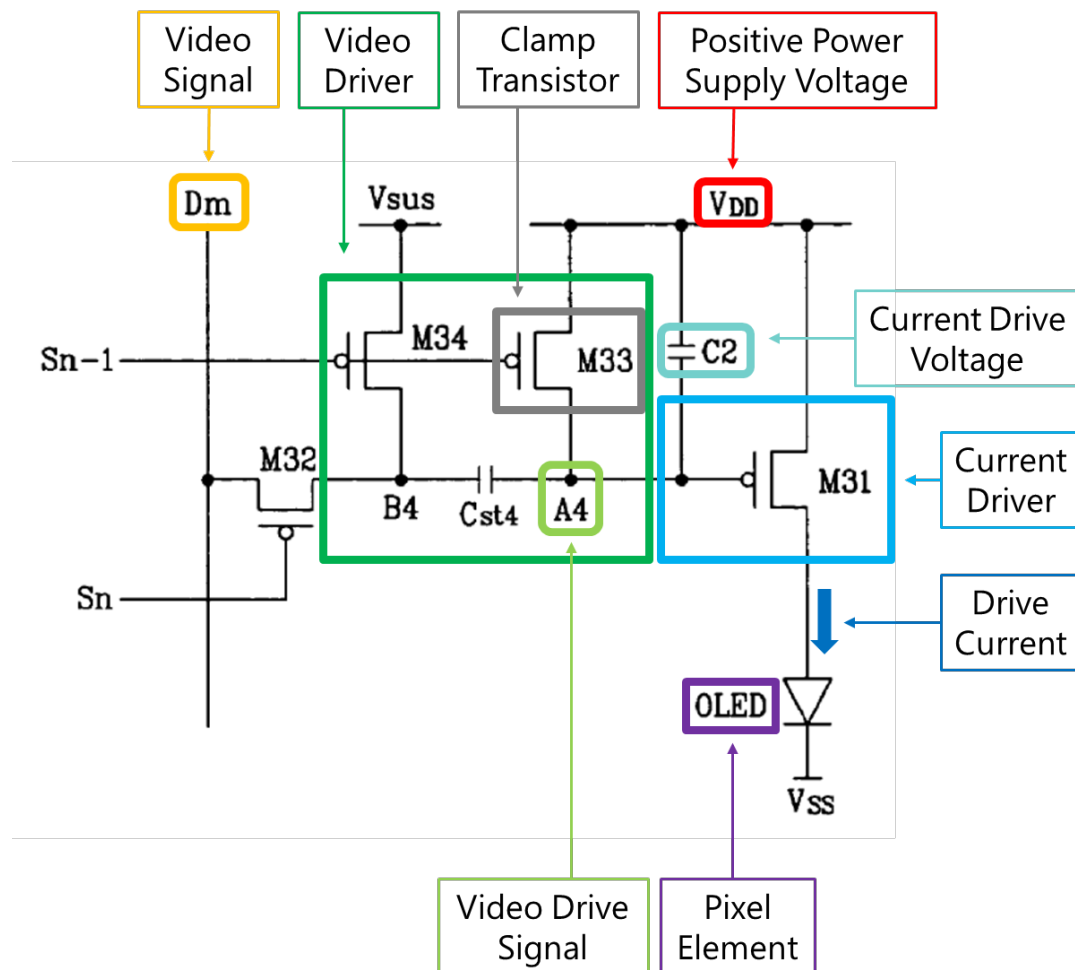
receives video signal Video.DAC and a clamp signal to turn off the OLED pixel, and outputs a V_{GS} to drive the OLED pixel when it's turned on. *See* Ex. [1001], the '521 Patent at 6:45-7:51. The video driver is implemented using a video clamp circuit comprising capacitor C1 having one plate driven by video signal Video.DAC and the other plate providing video drive signal $v(t)$. *See* Ex. [1001], the '521 Patent at 6:50-60. The video driver further comprises a clamp transistor M3 having a source terminal connected to PPS voltage VDD and a drain terminal connected to the capacitor C1 plate providing V_{GS} at node 322 such that, when activated, transistor M3 connects PPS voltage VDD with node 322, thereby preventing any current drive voltage ($VDD-v(t)=0$) and any drive current through transistor M1. *See* Ex. [1001], the '521 Patent at 6:50-60, FIG. 4 (annotated).



See Ex. [1001], the '521 Patent FIG. 4 (annotated).

109. A POSA would have recognized that Kim's fourth embodiment similarly discloses the claimed "video driver," including a video clamp circuit as in the '521 Patent's third embodiment. Specifically, Kim's fourth embodiment's video driver includes "capacitor C_{st4} [which] has electrodes **A4** and **B4** similar to the electrodes A and B of the capacitor C_{st1} [of FIG.6A]," and a "transistor **M33**." Consistent with Kim's FIG. 10 (annotated) and as discussed further below, a POSA would have understood that Kim's capacitor C_{st4} corresponds to the '521 Patent's capacitor C1, that Kim's transistor M33 corresponds to transistor M3 in the '521 Patent, and, based on the disclosed configuration and functionality of Kim's fourth

embodiment, Kim therefore discloses the claimed video driver (circuitry in green Video Driver annotation including Capacitor C_{st4} and clamp transistor M33) in the same manner as in the '521 Patent's third embodiment. Ex. [1007], Kim at FIG. 10 (annotated).



See Ex. [1007], Kim at FIG. 10 (annotated).

110. Regarding “receiving the video signal,” as discussed in Limitation [1-Pre], Kim discloses that “data voltage from the data line D_m is applied to the gate of

the transistor **Ma**,” (*see* Ex. [1007], Kim at ¶ 0009) and that a POSA would have recognized that “data voltage from the data line D_m ” corresponds to the claimed video signal.

111. Regarding “generating a video drive signal indicative of the video signal,” Kim discloses “**FIG. 10** shows a pixel circuit according to a fourth exemplary embodiment of the present invention.” *See* Ex. [1007], Kim at ¶0104, (“When the select signal from the previous scan line S_{n-1} becomes low level, the transistors **M33** and **M34** are turned on, the power supply voltage V_{DD} is applied to the first electrode **A4** of the capacitor C_{st4} .” *See also* Ex. [1007], Kim at ¶0107, (“Next, the select signal from the present scan line S_n becomes low level, and the transistor **M32** is turned on. Therefore, the voltage of the second electrode **B4** of the capacitor C_{st4} is changed to the data voltage, and the voltage of the first electrode **A4** of the capacitor C_{st4} is changed by a voltage variation of the second electrode **B4** of the capacitor C_{st4} . The voltage of the first electrode **A4** of the capacitor C_{st4} is given as Equation 11.”). *See* Ex. [1007], Kim at ¶¶ 0108, 0109 (“Equation 11”).

$$\begin{aligned} V_{A4} &= V_{DD} + \Delta V_{B4} \\ &= V_{DD} + V_{DATA} - V_{SUS} \end{aligned}$$

112. A POSA would have recognized that, as in the ’521 Patent’s third embodiment in which the claimed video drive signal is voltage $v(t)$ 322 supplied to

the gate of transistor M1 driving the OLED 32 by the video driver 302, Kim's fourth embodiment similarly discloses voltage at node A4 being supplied to the gate of transistor **M31** driving the organic light emitting diode OLED by the video driver circuitry including Capacitor C_{st4} and clamp transistor **M33**. A POSA would thus recognize that Kim's "voltage of the first electrode A4" corresponds to the claimed generated video drive signal.

113. A POSA also would have recognized in Kim that because the "the voltage of the second electrode B4 of the capacitor C_{st4} is changed to the data voltage $[V_{DATA}]$," which causes "the voltage of the first electrode **A4** of the capacitor C_{st4} to be changed by a voltage variation of the second electrode **B4** of the capacitor C_{st4} ," the resulting voltage of the first electrode **A4** is necessarily "indicative" of the data voltage (V_{DATA}). See Ex. [1007], Kim at ¶0108. This is also evident from Equation 11 above, in which voltage V_{A4} is explicitly a function of data voltage V_{DATA} . See Ex. [1007], Kim at ¶0109. Thus, a POSA would have recognized that Kim discloses a video drive signal (voltage of the first electrode V_{A4}) indicative of the video signal (voltage V_{DATA}).

114. Regarding the "video drive signal being referenced to a positive power supply voltage," the '521 Patent's third embodiment describes "video drive 302 is implemented using a video clamp circuit to reference the video drive signal to the

power supply voltage VDD. In video driver 302, the video clamp circuit is implemented using... PMOS transistor **M3** [which] has a source terminal connected to the power supply VDD voltage,” and “In this manner, the clamping voltage V_{clamp} [across capacitor C1] is added to the video signal Video.DAC for the rest of the video line and the video drive signal $v(t)$ is now referenced to the power supply voltage VDD.” *See* Ex. [1001], the ’521 Patent 6:48-7:8. Consistent with Kim’s FIG. 10 (annotated) and the discussion above, a POSA would have recognized that Kim’s fourth embodiment is similarly configured with voltage of the first electrode V_{A4} being “referenced to” PPS voltage VDD: “When... the transistors **M33** and **M34** are turned on, the power supply voltage V_{DD} is applied to the first electrode **A4** of the capacitor C_{st4} .” *See* Ex. [1007], Kim at FIG. 10 (annotated), ¶ 0107.

115. This is further illustrated below in a comparison between the ’521 Patent and Kim. The arrows indicate the application of VDD to C1 (*see* Ex. [1001], ’the 521 Patent at FIG. 4) and the application of V_{DD} to Cst4 (*see* Ex. [1007], Kim at FIG. 10) via clamp transistors M3 and M33 respectively.

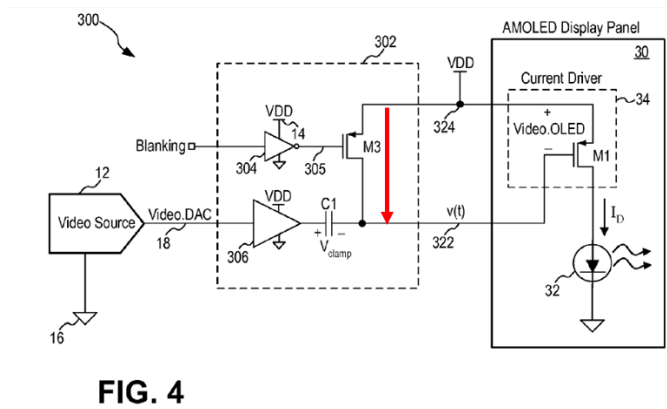


FIG. 4

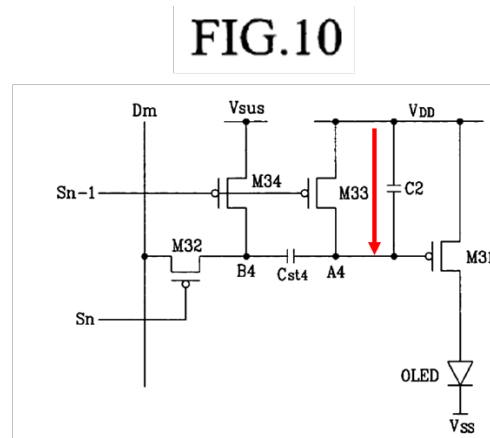
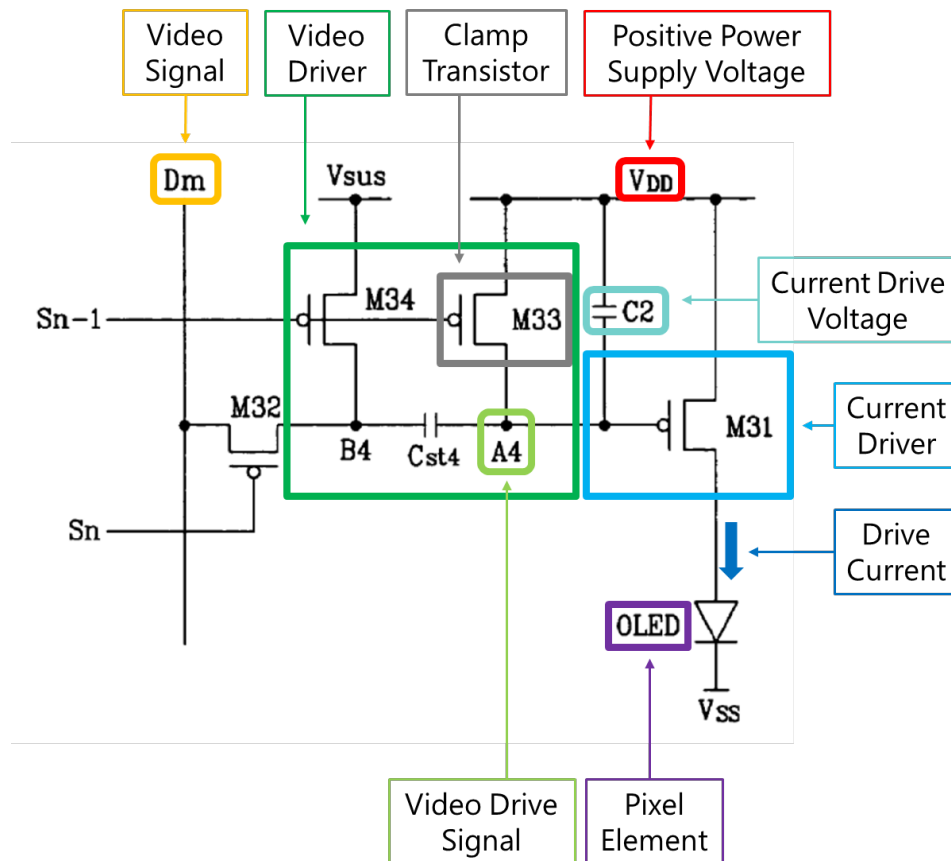


FIG. 10

116. This is also evident from Equation 11 above, in which voltage V_{A4} is explicitly a function of PPS voltage V_{DD} . *See* Ex. [1007], Kim at ¶ 0109. Thus, a POSA would have recognized that Kim discloses a video drive signal (voltage of the first electrode V_{A4})... referenced to a positive power supply voltage (PPS voltage V_{DD}).

117. Therefore, consistent with FIG. 10 (annotated) below, a POSA would have recognized that Kim discloses a video driver (circuitry in green Video Driver annotation including Capacitor C_{st4} and clamp transistor M33) receiving the video signal (voltage V_{DATA}) and generating a video drive signal (voltage of the first electrode V_{A4}) indicative of the video signal (voltage V_{DATA}) and referenced to a positive power supply voltage (PPS voltage V_{DD}) of the AMOLED display panel. *See* Ex. [1007], Kim at FIG. 10 (annotated).



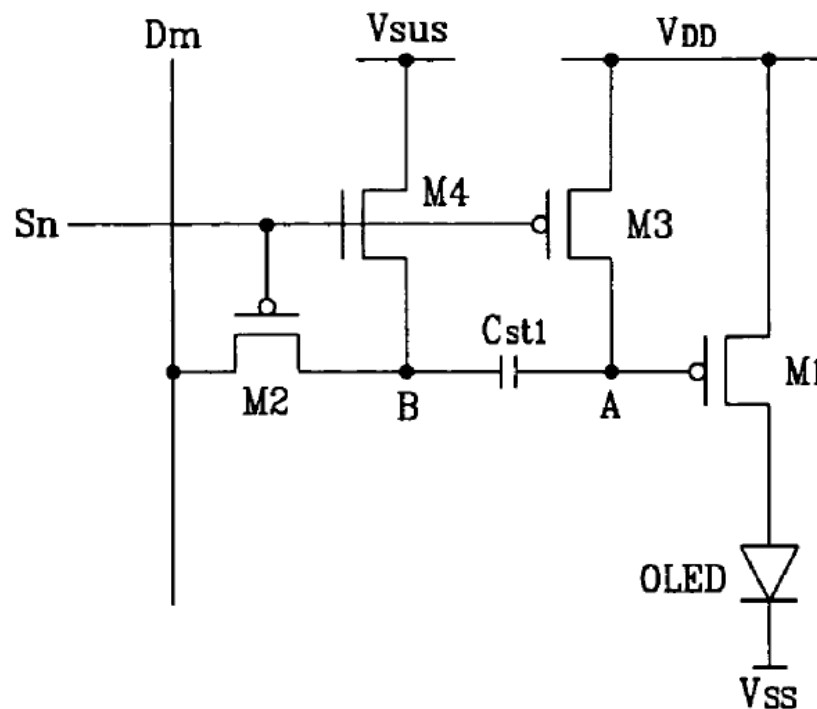
See Ex. [1007], Kim at FIG. 10 (annotated).

[1-B]: a current driver coupled to at least one OLED pixel element, the current driver receiving the video drive signal and the positive power supply voltage and providing a drive current to the at least one OLED pixel element,

118. Kim discloses a current driver coupled to at least one OLED pixel element, the current driver receiving the video drive signal and the positive power supply voltage and providing a drive current to the at least one OLED pixel element.

119. Regarding the claimed current driver coupled to at least one OLED pixel element, the current driver receiving the video drive signal and the positive power supply voltage, Kim explains that “In the pixel circuit of FIG. 10, transistors M31, M32 and a capacitor C_{st4} are connected together in substantially the same relationship as the transistors M1, M2 and the capacitor C_{st1} of FIG. 6A” which is reproduced below for reference. *See* Ex. [1007], Kim at ¶ 0105, FIG. 6A.

FIG.6A



120. *See* Ex. [1007], Kim at FIG. 6A.

121. Kim discloses that in FIG.6A, “The transistor **M1** is a driving transistor for controlling the current that flows to the **OLED**, and it has a source coupled to the power supply voltage V_{DD} , and a drain coupled to an anode of the **OLED**. A cathode of the **OLED** is coupled to a reference voltage V_{SS} and emits light that corresponds to the current applied from the transistor **M1**. The reference voltage V_{SS} is a voltage lower than the power supply voltage V_{DD} . By way of example, the ground voltage can be used as the reference voltage V_{SS} .” *See* Ex. [1007], Kim at ¶ 0052.

122. FIG. 10 of Kim discloses the pixel architecture of one embodiment of Kim.

Transistor M31 is a current driver that is coupled to an OLED. Therefore, the power supply voltage V_{DD} and the voltage of the first electrode A₄ of the capacitor C_{st4} are applied to both electrodes of the capacitor C₂, and the capacitor C₂ is charged.

In this instance, the voltage charged in the capacitor C₂ is given as Equation 12, and the corresponding current flows to the OLED.

See Ex. [1007], Kim at 0110-0111.

123. Thus, a POSA would recognize that Kim discloses a current driver (circuitry in blue Current Driver annotation below including transistor M31) coupled to at least one OLED pixel element (organic light emitting diode OLED), the current

driver receiving the video drive signal (voltage of the first electrode V_{A4}) and the positive power supply voltage (PPS voltage V_{DD}).

124. In the explanatory equations Kim describes the voltage at video drive signal A4 as a function of V_{DATA} or the data voltage applied to Dm:

$$V_{A4} = V_{DD} + \Delta V_{B4} = V_{DD} + V_{DATA} - V_{SUS}$$

See Ex. [1007], Kim at ¶ 0109.

125. The voltage applied to transistor M31 or V_{C2} is:

$$V_{A4} = V_{DD} + \Delta V_{B4} = V_{DD} + V_{DATA} - V_{SUS}$$

126. Regarding the current driver... providing a drive current to the at least one OLED pixel element, Kim continues “In this instance, the voltage charged in the capacitor C2 is given as Equation 12, and the corresponding current flows to the OLED.” *See* Ex. [1007], Kim at ¶¶ 0111, 0112(“Equation 12”).

$$V_{C2} = V_{DD} - (V_{DD} + V_{DATA} - V_{SUS}) = V_{DATA} - V_{SUS}$$

127. The current flowing through the OLED is set by the bias on transistor M31 by the gate-source voltage V_{GS} (equal to V_{C2}) and the transistor’s threshold voltage V_{TH} :

$$I_{OLED} = \frac{\beta}{2} (V_{GS31} - V_{TH31})^2$$

See Ex. [1007], Kim at ¶ 0113.

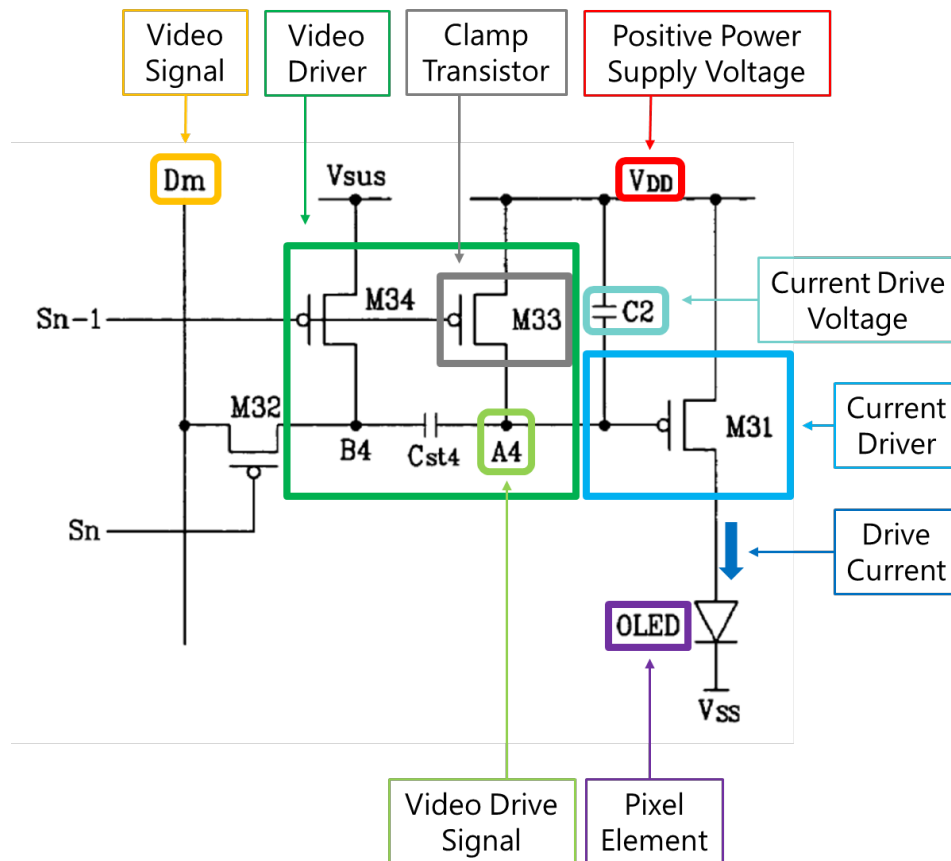
128. Therefore, according to FIG. 10 of Kim, the current flowing through the OLED is:

$$I_{OLED} = \frac{\beta}{2} (V_{C2} - V_{TH31})^2 = \frac{\beta}{2} ((V_{DATA} - V_{SUS}) - V_{TH31})^2$$

See Ex. [1007], Kim at ¶ 0113.

129. Thus, the current driver M31 receives a video drive signal V_{A4} which is applied to the gate and it receives V_{DD} which is applied to the source. This sets the current provide to the OLED pixel element.

130. Therefore, as explained above and consistent with the annotated version below of Figure 10, Kim discloses a current driver (circuitry including transistor M31 (annotated in light blue below)) coupled to at least one OLED pixel element (organic light emitting diode OLED), the current driver receiving the video drive signal (voltage of the first electrode V_{A4}) and the positive power supply voltage (power supply voltage V_{DD}) and providing a drive current (current flowing to the OLED, IOLED) to the at least one OLED pixel element and thus discloses limitation [1-B] of the '521 Patent.



See Ex. [1007], Kim at FIG. 10 (annotated).

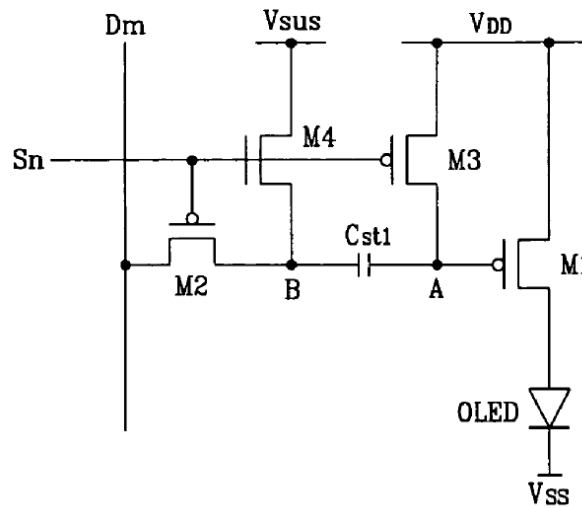
[1-C]: the drive current being proportional to a current drive voltage being indicative of the video signal and independent of the positive power supply voltage.

131. Kim discloses that the drive current being proportional to a current drive voltage being indicative of the video signal and independent of the positive power supply voltage.

132. Regarding the claimed drive current being proportional to a current drive voltage, as discussed for Limitations [1-Pre] and [1-B], Kim explains that “In

the pixel circuit of FIG. 10, transistors M31, M32 and a capacitor C_{st4} are connected together in substantially the same relationship as the transistors M1, M2 and the capacitor C_{st1} of FIG. 6A.” See Ex. [1007], Kim ¶ 0105, FIG.6A.

FIG.6A



See Ex. [1007], Kim FIG. 6A.

133. Kim discloses “a data voltage from the data line D_m is applied to the gate of the transistor Ma. Accordingly, the current I_{OLED} corresponding to a voltage V_{GS} charged by the capacitor C_{st} between the gate and the source of the transistor Ma flows through the transistor Ma, and the OLED emits light corresponding to the current I_{OLED} .” See Ex. [1007], Kim ¶ 0009. “By way of example, the current that flows to the OLED is given in Equation 1.” See Ex. [1007], Kim ¶ 0010. “As given in Equation 1, the current corresponding to the applied data voltage is supplied to

the OLED, and the OLED gives light corresponding to the supplied current.” See Ex. [1007], Kim ¶ 0012.

134. In this context, Kim explains for FIG. 10, “Therefore, the power supply voltage V_{DD} and the voltage of the first electrode A4 of the capacitor C_{st4} are applied to both electrodes of the capacitor C2, and the capacitor C2 is charged.” See Ex. [1007], Kim ¶ 0110. “In this instance, the voltage charged in the capacitor C2 is given as Equation 12, and the corresponding current flows to the OLED.” See Ex. [1007], Kim ¶¶ 0111,0112(“Equation 12”).

$$V_{C2} = V_{DD} - (V_{DD} + V_{DATA} - V_{SUS}) = V_{DATA} - V_{SUS}$$

See Ex. [1007], Kim at ¶ 0112.

135. The current flowing through the OLED is set by the bias on transistor M31 by the gate-source voltage V_{GS} (equal to V_{C2}) and the transistor’s threshold voltage V_{TH} :

$$I_{OLED} = \frac{\beta}{2} (V_{GS31} - V_{TH31})^2$$

See Ex. [1007], Kim at ¶ 0113.

136. In the ’521 Patent, the claimed current drive voltage is Video.OLED, which is the voltage across the gate and terminal of transistor M1 that drives OLED 32. As illustrated in Kim’s FIG. 10 (annotated) below, the voltage across the gate and source (V_{GS}) of transistor M31 that drives organic light emitting diode OLED is

also the same voltage across capacitor C2 (i.e., $V_{C2}=V_{GS31}$). Thus, consistent with FIG. 10 (annotated) below, a POSA would have understood the voltage across capacitor C2 ($V_{C2}=V_{GS31}$) as corresponding to the claimed current drive voltage.

137. A POSA would therefore have recognized that Kim's voltage across the gate and source (V_{GS}) of the transistor M31 corresponds to the claimed current drive voltage, and that Kim's current I_{OLED} corresponds to the claimed drive current. A POSA would also have recognized that because Kim's transistor M31 and the '521 Patent's transistor M1 are both P-channel MOSFETs, they would both operate in the same manner based on the well-known principles and functionalities of P-Channel MOSFETs. Therefore, in the context of the '521 Patent's drive current being "proportional" to the current drive voltage, because the P-channel MOSFETs would operate in the same manner, a POSA would have understood that Kim's current I_{OLED} is also "proportional" to the gate and source (V_{GS}), in the same manner as it is "proportional" in the '521 Patent.

138. Thus, a POSA would have recognized that Kim discloses the drive current (drain current I_d) being proportional to a current drive voltage (gate-to-source voltage V_{gs}).

139. Regarding the claimed current drive voltage being indicative of the video signal, as discussed for Limitation [1-A], Kim discloses the video drive signal

(voltage of the first electrode V_{A4}) being indicative of the video signal (voltage V_{DATA}). A POSA would have also understood that since voltage V_{GS31} is calculated based on voltage V_{A4} , because voltage V_{A4} is “indicative” of voltage V_{DATA} , voltage V_{GS31} must also be “indicative” of voltage V_{DATA} . This is also evident from Equation 12 above, in which the result of V_{A4} in Equation 11 is directly substituted into Equation 12.

140. Thus, a POSA would have recognized that Kim discloses the current drive voltage (voltage V_{C2} (=voltage V_{GS31})) being indicative of the video signal (V_{DATA}).

141. Regarding the claimed drive current being... independent of the positive power supply voltage, Kim discloses “a current that flows to the OLED of a pixel circuit in a light emitting display is substantially prevented from being influenced by a power supply voltage. Further, a current that flows to the OLED of a pixel circuit in a light emitting display may be substantially prevented from being influenced by deviations of a threshold voltage of a driving transistor.” *See* Ex. [1007], Kim at ¶¶ 0014-0015.

142. As discussed above, Kim explains for FIG. 10, “The current flowing to the OLED is given as Equation 13.” *See* Ex. [1007], Kim at ¶ 0113 (“Equation 13”).

$$I_{OLED} = \frac{\beta}{2} (V_{GS31} - V_{TH31})^2$$

$$I_{OLED} = \frac{\beta}{2} ((V_{DATA} - V_{SUS}) - V_{TH31})^2$$

143. “As can be seen from Equation 13, the current flowing to the OLED is substantially not influenced by the power supply voltage V_{DD} .” *See* Ex. [1007], Kim at ¶ 0114.

144. A POSA would have recognized that this is true because none of the parameters in this resulting equation are dependent on V_{DD} (β “is a constant,” V_{TH31} “is a threshold voltage at the transistor,” V_{DATA} is “a data voltage from the data line Dm,” and V_{SUS} is “a compensation voltage... differing from the power supply voltage V_{DD} ”). *See* Ex. [1007], Kim at ¶¶ 0009-0011, 0071. The purpose of the compensation voltage V_{SUS} is to modify the voltage that is applied to the drive transistor. The compensation voltage V_{SUS} disclosed by Kim must be different from the power supply V_{DD} otherwise no compensation can occur. *See also* Ex. [1007], Kim at ¶ 0018, (“A voltage compensator receives the corresponding said data Voltage transmitted by the first switch and applies a compensated data voltage based on the corresponding said data voltage and the first power supply voltage to the first electrode of the transistor.”).

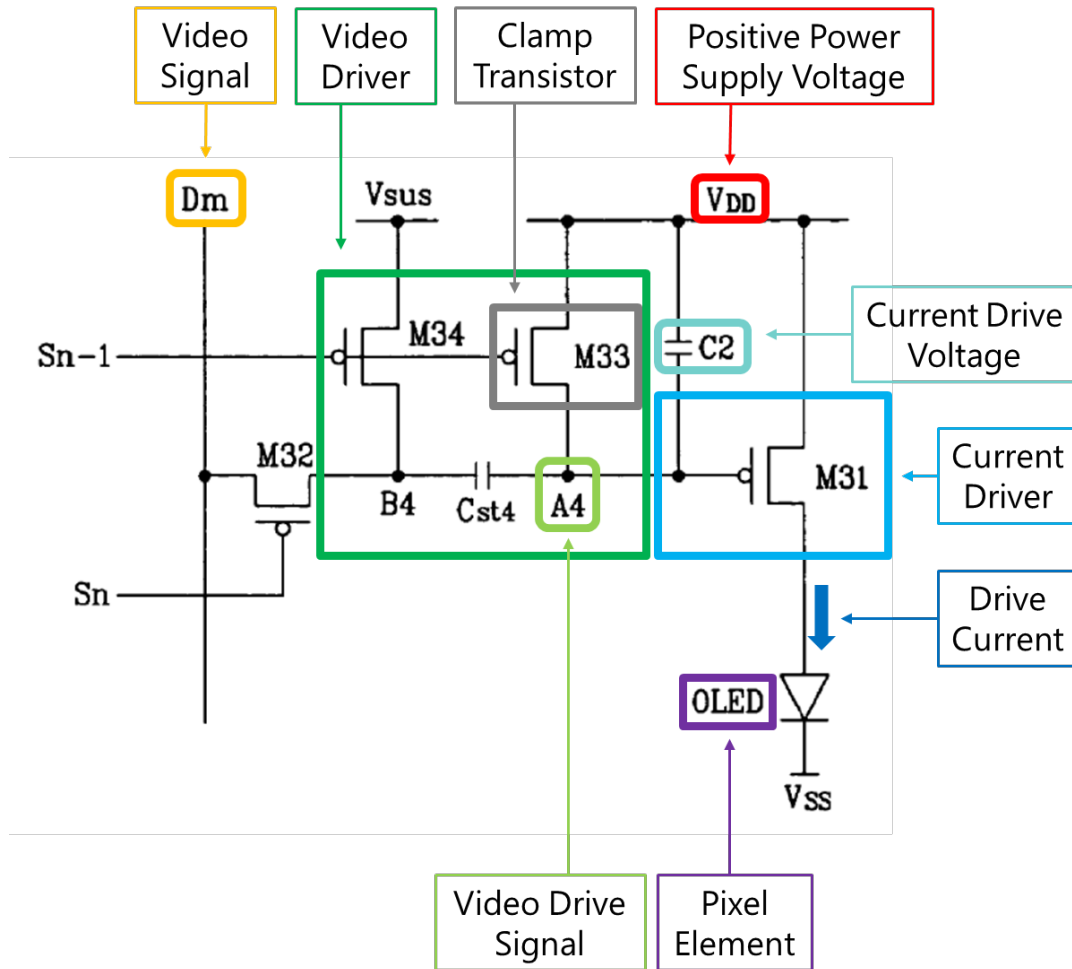
145. This is clearly shown in the equations 11 and 12 of Kim.

$$V_{C2} = V_{DD} - (V_{DD} + V_{DATA} - V_{SUS}) = V_{DATA} - V_{SUS}$$

$$I_{OLED} = \frac{\beta}{2} (V_{GS31} - V_{TH31})^2$$

146. A POSA would have understood that because Kim's drive current is "not influenced" by the PPS voltage V_{DD} it is therefore "independent of" the PPS voltage V_{DD} .

147. Therefore, as also consistent with FIG. 10 (annotated) below, a POSA would have recognized that Kim further discloses the drive current (I_{OLED}) being... independent of the positive power supply voltage (PPS voltage V_{DD}). *See* Ex. [1007], Kim FIG. 10 (annotated).



See Ex. [1007], Kim FIG. 10 (annotated).

b) Claim 2

[2]: The AMOLED display system of claim 1, wherein the video drive signal is indicative of the sum of or the difference between the positive power supply voltage and the video signal and the current drive voltage is indicative of the difference between the positive power supply voltage and the video drive signal.

148. Kim discloses that the video drive signal is indicative of the sum of or the difference between the positive power supply voltage and the video signal and the current drive voltage is indicative of the difference between the positive power supply voltage and the video drive signal.

149. As described above Kim discloses a pixel circuit where transistor M31 is biased by the V_{DD} and video drive signal, V_{A4} . This is also the voltage across capacitor C2.

150. In the explanatory equations Kim describes the voltage at A4 as a function of V_{DATA} , the data voltage on Dm:

$$V_{A4} = V_{DD} + V_{DATA} - V_{SUS}$$

151. Therefore, the power supply voltage V_{DD} and the voltage of the first electrode A4 of the capacitor Cst4 are applied to both electrodes of the capacitor C2, and the capacitor C2 is charged. As shown in the equation above the video drive signal V_{A4} is indicative of the difference between positive power supply voltage and the video signal.

152. Kim further discloses that the current drive voltage V_{C2} is:

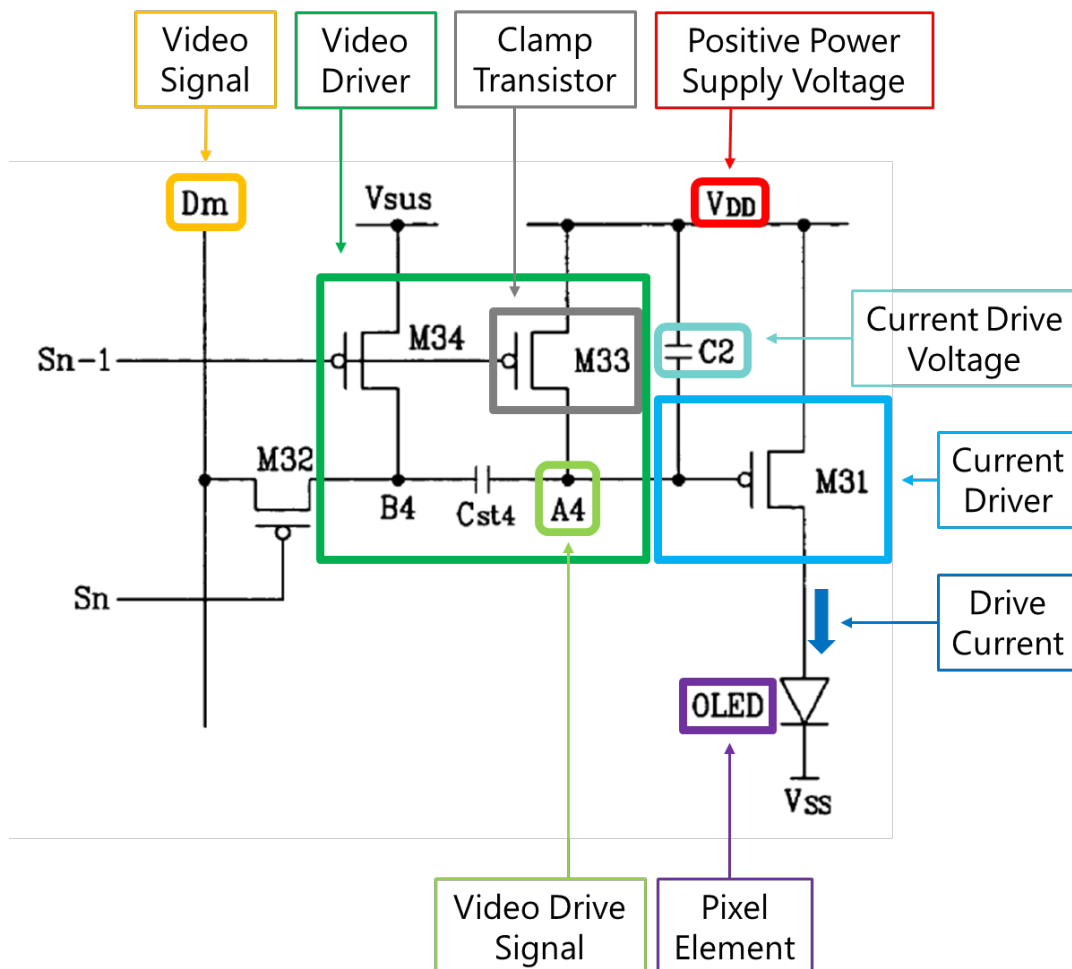
$$V_{C2} = V_{DD} - (V_{DD} + V_{DATA} - V_{SUS}) = V_{DATA} - V_{SUS}$$

or

$$V_{C2} = V_{DD} - V_{A4}$$

153. Thus, the current drive voltage V_{C2} is indicative of the difference between the positive power supply V_{DD} and the video drive signal V_{A4} .

154. Therefore, as described above and consistent with the annotated version below of Figure 10, Kim discloses that the current drive voltage (voltage V_{C2} (= voltage V_{GS31})) is indicative of the difference between ($V_{C2} = V_{DD} - V_{A4}$) the positive power supply voltage (power supply voltage V_{DD}) and the video drive signal (voltage of the first electrode V_{A4}) and thus discloses Claim 2 of the '521 Patent.

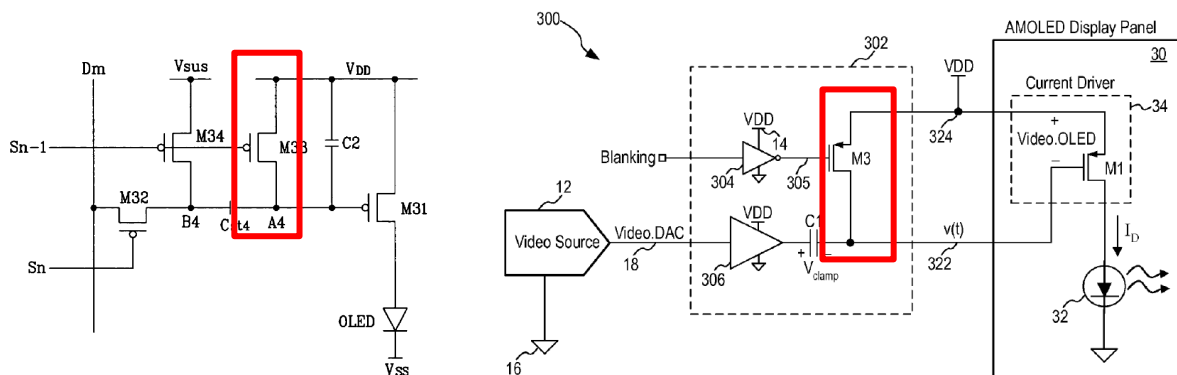


See Ex.[1001], the '521 Patent FIG. 4 (annotated).

157. As discussed for Claim [2], Kim discloses the video drive signal (voltage of the first electrode V_{A4}) being the sum of the positive power supply voltage (PPS voltage VDD) and the video signal (VDATA).

$$V_{A4} = V_{DD} + V_{DATA} - V_{SUS}$$

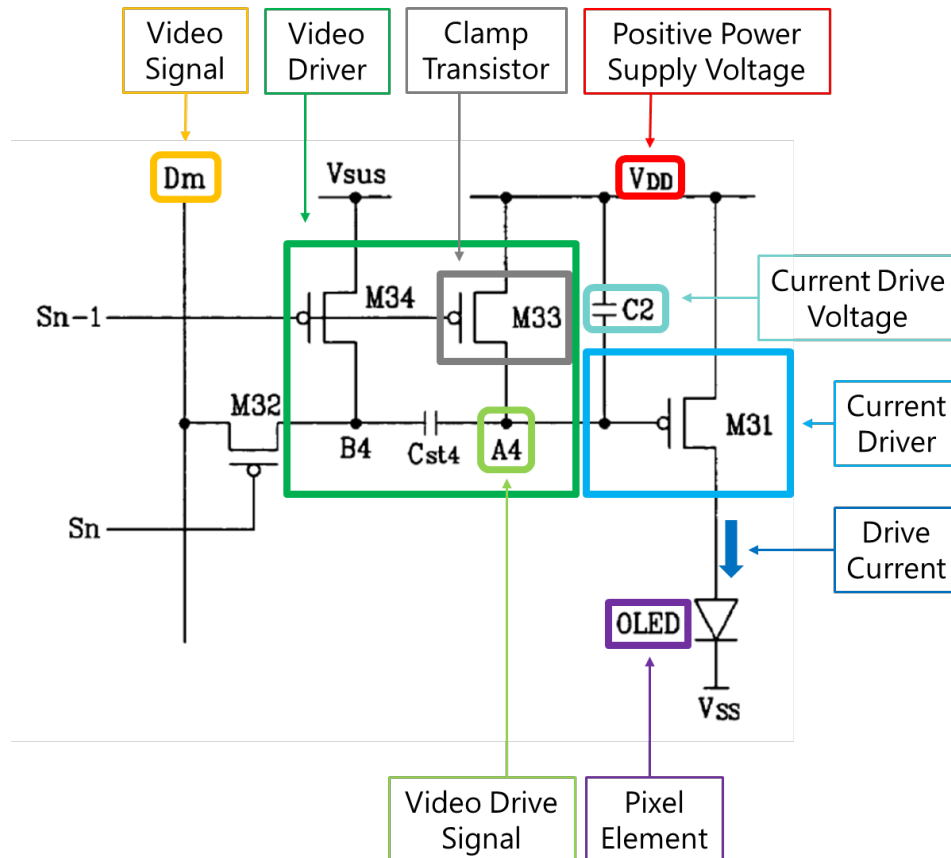
158. As shown in FIG. 10 of Kim, transistor **M33** acts as a clamp transistor placed across positive power supply voltage V_{DD} and the video drive signal V_{A4} . This is the same configuration as transistor **M33** in FIG. 4 of the '521 Patent.



See Ex. [1007], Kim at FIG. 10 and the '521 Patent at FIG. 4 (annotated).

159. A POSA would have understood that clamp circuits serve to ensure that “voltage drifts in the power supply voltage [] are removed from the current drive signal,” which is *Kim*’s transistor **M33**’s purpose. Ex.[1001],7:48-50. Thus, a POSA

would have recognized *Kim*'s circuitry including transistor **M33** is a *video clamp circuit*. See Ex. [1007], *Kim* at FIG. 10 (annotated).

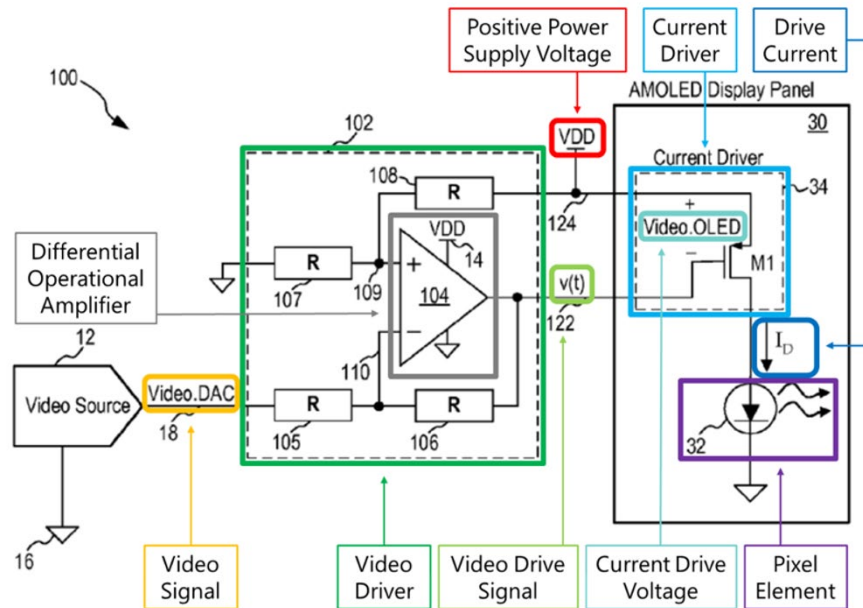


See Ex. [1007], *Kim* at FIG. 10 (annotated).

160. Therefore, as described above and consistent with the above annotated version of Figure 10, *Kim* discloses that the video driver comprises a video clamp circuit (circuitry including clamp transistor M33) for providing the video drive signal being the sum of the positive power supply voltage and the video signal and thus discloses Claim 7 of the '521 Patent.

B. Ground 3: Claims 1 and 2 of the '521 Patent are Anticipated by Hayafuji

161. The figure below is an annotated reproduction of FIG. 2 of the '521 Patent illustrating the first embodiment.



See Ex. [1001], the '521 Patent at FIG. 2 (annotated).

a) Claim 1

[1-Pre]: An active matrix organic light emitting diode (AMOLED) display system comprising an AMOLED display panel receiving a video signal to be displayed on the AMOLED display panel, the AMOLED display panel comprising a plurality of organic light emitting diode (OLED) pixel elements, the AMOLED display system comprising:

162. To the extent the preamble is limiting, Hayafuji discloses an active matrix organic light emitting diode (AMOLED) display system comprising an

AMOLED display panel receiving a video signal to be displayed on the AMOLED display panel, the AMOLED display panel comprising a plurality of organic light emitting diode (OLED) pixel elements, the AMOLED display system.

163. Hayafuji discloses a display panel using OLEDs (*see* Hayafuji at 0004) with an active-matrix driving scheme.

A display employing a display panel constructed by arranging light emitting elements in a matrix pattern has been developed widely, and as the light emitting element employed in such a display panel, for example, an organic EL (electroluminescent) element in which an organic material is employed...

See Hayafuji at ¶ 0004.

A drive device of a light emitting display panel according to the present invention which has been developed to solve the problems is a drive device of an active matrix type light emitting display panel in which a large number of light emitting display pixels at least provided with a light emitting element and a light emission drive transistor which is connected in series to the light emitting element in order to drive and allow the light emitting element to emit light are arranged...

See Hayafuji at ¶ 0029.

164. Hayafuji further discloses a video signal that is supplied to the display panel. *See* Hayafuji at ¶ 0013, (“[a] video signal displayed in the light emitting display panel **2** is supplied to a light emission control circuit **4** shown in **FIG. 1**. This

light emission control circuit **4** converts an input video signal to corresponding pixel data for each one pixel.”).

165. Hayafuji also discloses that a gate voltage, based on the video signal is applied to a drive transistor to supply current to an OLED. *See* Hayafuji at ¶ 0024, (“the gate voltage V_{gate} based on the video signal is supplied to the gate of the drive transistor **Tr2**.”).

166. Finally, Hayafuji explains “[a] drive device of a light emitting display panel... **FIG. 6** shows a first embodiment of a drive device according to the present invention.... In the equivalent circuit of a pixel shown in **FIG. 6**, parts which perform the same functions as those of the respective parts shown in **FIG. 2** are designated by the same reference characters, and detailed description thereof will be omitted.” *See* Ex. [1006], Hayafuji at ¶ 0047. *See also* Ex. [1006], Hayafuji at ¶ 0048, (“In the embodiment shown in **FIG. 6**,... data voltage V_{data} transmitted via the above-mentioned [FIG.1] data line B1 is input to the other input terminal of the voltage addition circuit 15.”).

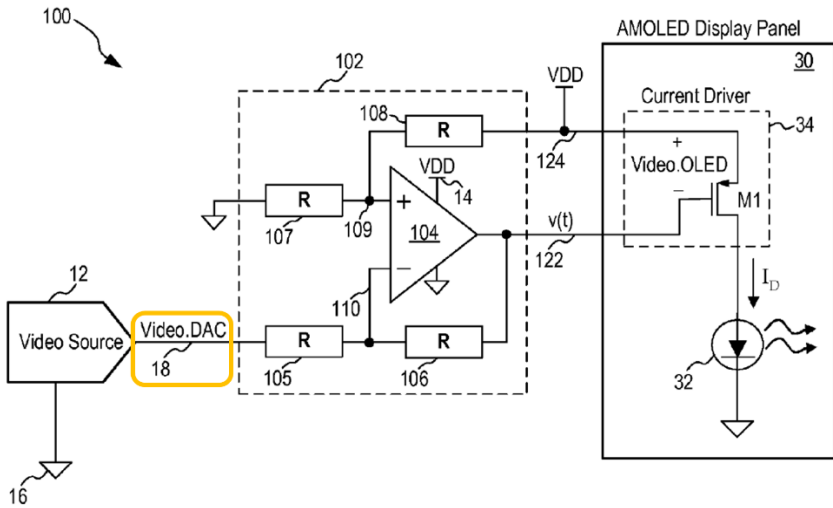
167. Though, FIG. 1 of Hayafuji shows a “video signal” going into light emission control circuit **4** there is also a video signal exiting data driver **5**, referred to by Hayafuji as V_{data} . Hayafuji further discloses that a gate voltage, based on the video signal is applied to a drive transistor to supply current to an OLED. *See*

Hayafuji at ¶ 0024, (“the gate voltage V_{gate} based on the video signal is supplied to the gate of the drive transistor **Tr2**.”).

168. Regarding the “data voltage V_{data} transmitted via the above-mentioned data line B1,” Hayafuji explains “data voltage V_{data} [] corresponds to a write data from the data line B1” and “data voltage V_{data} transmitted via the above-mentioned data line B1 is equivalently output from a D/A converter.” *See* Ex. [1006], Hayafuji at ¶¶ 0009, 0051.

169. When looking to the '521 Patent the claimed video signal, Video.DAC is an input to the driver circuit. *See* Ex. [1001], the '521 Patent at FIG. 1. A POSA would have recognized that the acronym DAC in the “Video.DAC” signal is also a digital to analog converted signal just as that of the D/A converter disclosed in Hayafuji.

170. Additionally, the video signal of the '521 Patent feeds one sole pixel just as the V_{data} signal of Hayafuji.



See Ex. [1001], the '521 Patent at FIG. 2 (annotated to show the video signal).

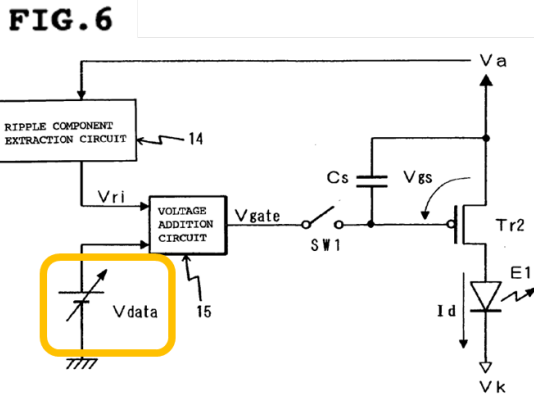


FIG. 7

The diagram shows a two-stage operational amplifier circuit. The first stage is an inverting buffer with input V_a , feedback resistor R_{21} , and output $OP3$. The second stage is another inverting buffer with feedback resistor R_{22} and output V_{gate} . A D/A converter (16) is connected to the input of the first stage. A dashed box 14 encloses the input network.

FIG. 1

The diagram illustrates a video signal processing system. A VIDEO SIGNAL input is connected to a LIGHT EMISSION CONTROL CIRCUIT (4). This circuit outputs to a DATA DRIVER (5), which contains a SHIFT REGISTER & DATA LATCH (5a) and a LEVEL SHIFTER (5b). The DATA DRIVER also receives a (V data) input (highlighted with a yellow box). The output of the DATA DRIVER is connected to a SCAN DRIVER (6), which includes a SHIFT REGISTER (6a) and a LEVEL SHIFTER (6b). The SCAN DRIVER outputs to a pixel circuit (B1), which is part of a larger block (1) containing a Select input, a capacitor Cs, and transistors Tr1 and Tr2. The pixel circuit is connected to a power supply (Va) and a ground. The system also includes a reference voltage Vref (10) and a video signal input (9) connected to an oscillator (OSC) and a pulse-width modulator (PWM) (11). The PWM output is connected to a transistor Q1, which is in series with a resistor R11 and a diode TH1. The output of the PWM is also connected to a resistor R12 and a ground. The system is powered by a battery Ba.

See Ex. [1006], Hayafuji at FIG. 1, FIG. 6 and FIG. 7 (annotated to show the video signal).

171. Finally, Vdata of Hayafuji is also an analog signal just as in the '521 Patent, and thus corresponds to the claimed video signal. *See* Ex. [1001], the '521 Patent at 1:61-65, (“In most systems, the video signals are digital in nature and the signal processing step of video source 12 is to convert the digital video signals to analog signals, thereby generating the analog signal Video.DAC on an output bus 18.”).

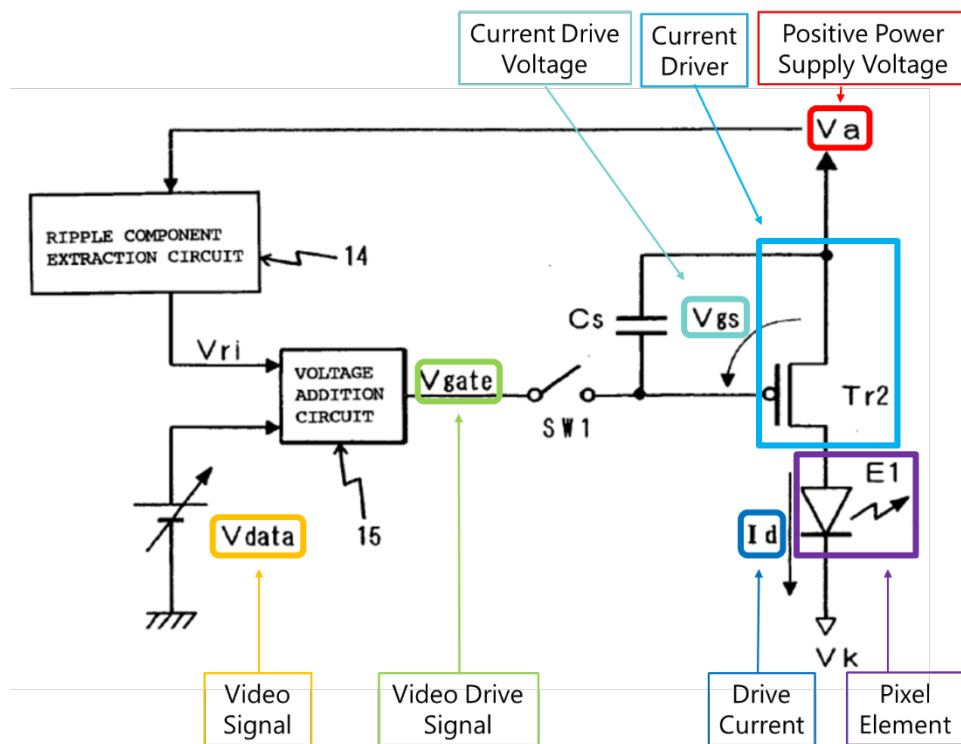
172. Therefore, Hayafuji discloses an active matrix organic light emitting diode (AMOLED) display system comprising an AMOLED display panel receiving a video signal to be displayed on the AMOLED display panel, the AMOLED display panel comprising a plurality of organic light emitting diode (OLED) pixel elements.

[1-A]: a video driver receiving the video signal and generating a video drive signal indicative of the video signal and referenced to a positive power supply voltage of the AMOLED display panel; and

173. Hayafuji discloses a video driver receiving the video signal and generating a video drive signal indicative of the video signal and referenced to a positive power supply voltage of the AMOLED display panel.

174. As illustrated below in FIG.6 (annotated), Hayafuji discloses a video driver (extraction circuit **14** and voltage addition circuit **15** in green annotation below) receiving the video signal (data voltage V_{data}) and generating a video drive

signal (gate voltage V_{gate}) indicative of the video signal (data voltage V_{data}) and referenced to a positive power supply voltage (drive voltage V_a) of the AMOLED display panel. *See* Ex. [1006], Hayafuji at FIG.6 (annotated); *see also* Ground 3, Claim [3] (further supporting this analysis in the context of FIG. 10).



See Ex. [1006], Hayafuji at FIG.6 (annotated).

175. As an initial matter, the '521 Patent does not define the term “referenced to.” Furthermore, throughout the specification the term appears to connote four possibilities.

- 1) A direct connection between a component and a voltage signal:

In most AMOLED display panels, the current driver is implemented so that the current driver 34 is referenced to the positive power supply voltage VDD (node 24) of the display system 10.

See Ex. [1001], the '521 Patent at 2:20-23

The current that passes through transistor M2 is put through resistor 206 which is referenced to the power supply voltage VDD.

Id. 5:63-65

2) An indirect connection between multiple voltage signals

In the conventional AMOLED display system, the video drive signal $v(t)$ is a signal that is referenced to the ground voltage (node 16)... Basically, the analog signal Video.DAC is referenced to ground and the VDC voltage level is added to offset the video signal to the power supply voltage VDD.

Id. 2:1-14

In accordance With the principles of the present invention, a video driver for an AMOLED display system generates a video drive signal that is referenced to the positive power supply voltage of the display panel.

Id. 3:55-58

3) A voltage difference:

Voltage Video.OLED is referenced to the power supply voltage VDD and is given as: $\text{Video.OLED} = \text{VDD} - v(t)$.

Id. 2:34-37

4) Driver functionality:

However, in accordance With the present invention, the positive input terminal 109 of opamp 104 is connected through resistor 108 to the power supply voltage VDD instead of the ground voltage so as to realize the re-referencing function of video driver 102.

Id. 4:55-60.

176. Based on these disparate uses a POSA would have understood that claim terms should be based on the intrinsic record, and would therefore approach the claimed “referenced to” requirement as having its plain and ordinary meaning in the context of the ’521 Patent and the manner in which it is used therein, including all of the examples described above.

177. Hayafuji discloses an invention to solve drive device problems by measuring and supplying the ripple current component to the drive transistor gate.

A drive device of a light emitting display panel according to the present invention which has been developed to solve the problems is a drive device of an active matrix type light emitting display panel in which a large number of light emitting display pixels at least provided with a light emitting element and a light emission drive transistor which is connected in series to the light emitting element in order to drive and allow the light emitting element to emit light are arranged, characterized by comprising ripple component supply means for supplying a ripple component having approximately the same phase and amplitude as those of a ripple component which is supplied to the source electrode of the light emission drive transistor to the gate electrode of the light emission drive transistor.

See Ex. [1006], ¶ 0029.

178. Hayafuji further teaches that “[t]he ripple component extraction circuit 14 extracts a ripple component $[V_{ri}]$ included in a drive voltage V_a generated by the above-described DC-DC converter, and a ripple component V_{ri} extracted by this ripple component extraction circuit 14 is supplied to one input terminal of the voltage addition circuit 15. The data voltage V_{data} transmitted via the above-mentioned data line B1 is input to the other input terminal of the voltage addition circuit 15.” *See* Ex. [1006], Hayafuji at ¶ 0048.

179. Hayafuji explains that “in the voltage addition circuit 15, treating the data voltage V_{data} as a base, the ripple component V_{ri} extracted by the ripple component extraction circuit 14 is added to the base. The output thereof as $V_{gate...}$ is supplied to the gate of a light emission drive transistor **Tr2**.” *See* Ex. [1006], Hayafuji at ¶ 0049.

180. According to Hayafuji “the data voltage V_{data} transmitted via the above-mentioned data line B1 is [] output from a D/A converter.” *See* Ex. [1006], Hayafuji at ¶ 0051. The “data voltage V_{data} ” is shown in FIG. 6 (annotated) above.

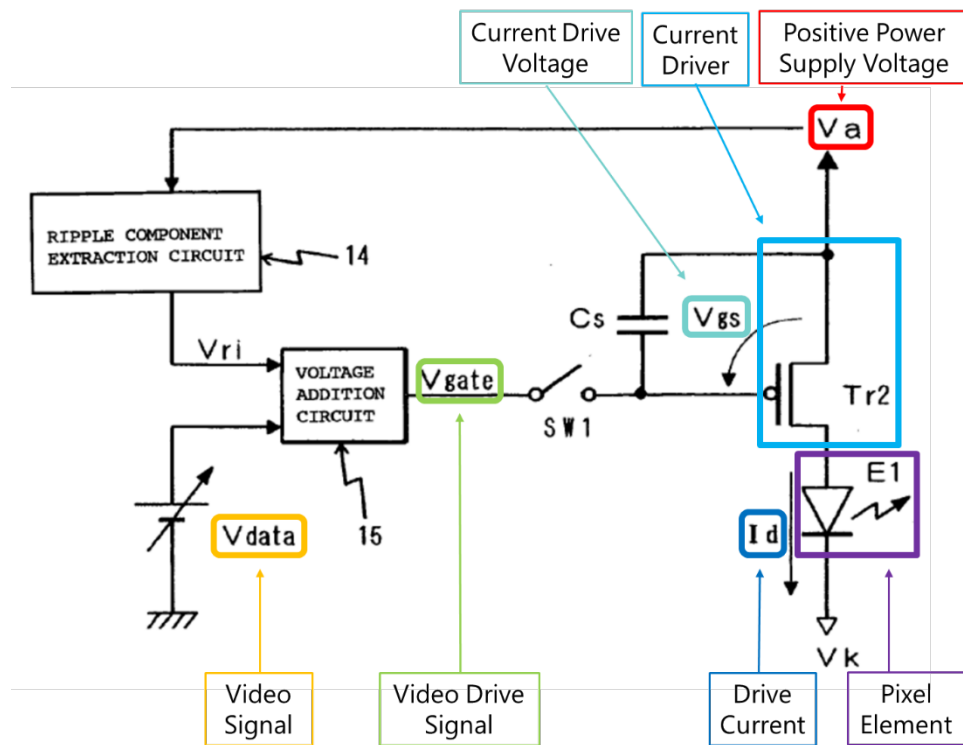
181. Thus, a POSA would have recognized that “data voltage V_{data} transmitted via the above-mentioned data line B1” corresponds to the claimed video signal.

182. Therefore, Hayafuji discloses a video driver receiving the video signal and generating a video drive signal indicative of the video signal and referenced to a positive power supply voltage of the AMOLED display panel.

[1-B]: a current driver coupled to at least one OLED pixel element, the current driver receiving the video drive signal and the positive power supply voltage and providing a drive current to the at least one OLED pixel element,

183. Hayafuji discloses a current driver coupled to at least one OLED pixel element, the current driver receiving the video drive signal and the positive power supply voltage and providing a drive current to the at least one OLED pixel element.

184. As illustrated in FIG.6 (annotated) below, Hayafuji discloses a current driver (circuitry including light emission drive transistor **Tr2** (see light blue annotation in FIG.6 below)) coupled to at least one OLED pixel element (organic EL element **E1**), the current driver receiving the video drive signal (gate voltage V_{gate}) and the positive power supply voltage (drive voltage V_a) and providing a drive current (drain current I_d) to the at least one OLED pixel element. *See* Ex. [1006], Hayafuji, at FIG.6 (annotated).



See Ex. [1006], Hayafuji at FIG. 6 (annotated).

185. Hayafuji discloses a that drive transistor $Tr2$ receives a drive power source Va , a gate voltage V_{gate} based on the video signal and is connected to the element $E1$.

In the embodiment shown in FIG. 6, a ripple component extraction circuit 14 and a voltage addition circuit 15 are provided and are constituting the ripple component supply means. The ripple component extraction circuit 14 extracts a ripple component included in a drive voltage Va generated by the above-described DC-DC converter, and a ripple component V_{ri} extracted by this ripple component extraction circuit 14 is supplied to one input terminal of the voltage addition circuit 15. The data voltage V_{data} transmitted via the above-mentioned data line $B1$ is input to the other input terminal of the voltage addition circuit 15.

Accordingly, in the voltage addition circuit 15, treating the data voltage V_{data} as a base, the ripple component V_{ri} extracted by the ripple component

extraction circuit 14 is added to the base. The output thereof as V_{gate} is supplied to a scan selection transistor Tr1 represented by reference character SW1, and the V_{gate} is supplied to the gate of a light emission drive transistor Tr2 by the turning on of the transistor Tr1 during the addressing time and is written in a capacitor Cs.

See Ex. [1006], Hayafuji at ¶ 48, 49.

186. Hayafuji also teaches that “drain current I_d which drives and allows the organic EL element E1 to emit light is determined by the error(gate-to-source voltage= V_{gs} of the transistor Tr2) between the drive voltage V_a supplied via the power line P1 and the gate voltage of the drive transistor **Tr2**.” *See* Ex. [1006], Hayafuji at ¶ 0021.

187. The term error is commonly used to connote a difference in analog circuits. For example a differential amplifier can be referred to as an error amplifier. *See* Ex. [1010], Horowitz at pg. 309, (“Q11 and Q12 form the differential amplifier (sometimes called the “error amplifier,” thinking of the whole thing as an exercise in negative feedback), a classic long-tailed pair with emitter current source Q13.”).

188. Therefore, a POSA would have understood that the term “error,” as used in Hayafuji, means the “difference” between drive voltage V_a and the gate voltage of drive transistor Tr2. This is consistent with the context it’s used in, as well as the use of “error” in mathematics to refer to a difference between measurements.

189. Therefore, Hayafuji discloses a current driver coupled to at least one OLED pixel element, the current driver receiving the video drive signal and the positive power supply voltage and providing a drive current to the at least one OLED pixel element.

[1-C]: the drive current being proportional to a current drive voltage being indicative of the video signal and independent of the positive power supply voltage.

190. Hayafuji discloses that the drive current being proportional to a current drive voltage being indicative of the video signal and independent of the positive power supply voltage.

191. Regarding the clause a “drive current being proportional to a current drive voltage,” the ’521 Patent describes that “current driver **34** includes a PMOS transistor **M1** having... its gate terminal connected to receive the video drive signal $v(t)$,” that “[c]urrent driver voltage Video.OLED is the voltage applied to the current driver 34 and determines the value of drive current I_D to be applied to the OLED pixel element of the display panel,” and that “Video.OLED = VDD – $v(t)$.” *See* Ex. [1001], the ’521 Patent 2:31-36. Hayafuji discloses a similar driver voltage across the terminals of “a P-channel type light emission drive transistor **Tr2**,” resulting in “current I_d which drives and allows the organic EL element **E1** to emit light...”. *See* Ex. [1006], Hayafuji at ¶¶ 7,21. Hayafuji explains the current is “determined by the

error (gate-to-source voltage= V_{gs} of the transistor **Tr2**) between the drive voltage V_a supplied via the power line P1 and the gate voltage of the drive transistor **Tr2**.” *Id.*

192. A POSA would have understood that Hayafuji’s gate-to-source voltage V_{gs} across drive transistor Tr2 corresponds to the claimed current drive voltage, and that Hayafuji’s drain current I_d corresponds to the claimed drive current. A POSA would also have recognized that because Hayafuji’s drive transistor **Tr2** and the ’521 Patent’s transistor M1 are both P-channel MOSFETs, they would both operate in the same manner based on the well-known principles and functionalities of P-Channel MOSFETs. Therefore, in the context of the ’521 Patent’s drive current being “proportional” to the current drive voltage, because the P-channel MOSFETs would operate in the same manner, a POSA would have understood that Hayafuji’s drain current I_d is also “proportional” to the gate-to-source voltage V_{gs} .

193. The ’521 Patent does not discuss or give any specific meaning to the term “proportional.” Furthermore, it does not provide any specifics related to the operation of PMOS transistor M1. For example it does not disclose the geometry, oxide capacitance or mobility. These values would set the current I_D based on the applied bias voltages (gate-to-source and drain-to-source). (*See* Ex. [1010], Horowitz Text at pg. 121.

194. Thus, a POSA would have understood the term “proportional” as having its plain and ordinary meaning in the context of the ’521 Patent based on the operation of a typical P-channel MOSFET.

195. Thus, a POSA would recognize that Hayafuji discloses the drive current (drain current I_d) being proportional to a current drive voltage (gate-to-source voltage V_{gs}).

196. Regarding the clause “current drive voltage being indicative of the video signal,” as discussed above for Ground 3, Limitation [1-A], Hayafuji discloses that the video drive signal (gate voltage V_{gate}) is indicative of the video signal (data voltage V_{data}). As such, a POSA would have recognized that because Hayafuji’s (1) drain current I_d is based on the gate-to-source voltage V_{gs} as discussed above, (2) gate-to-source voltage V_{gs} is necessarily based on gate voltage V_{gate} (“ $gate$ ” being the “ g ” in “ V_{gs} ”), and (3) gate voltage V_{gate} is indicative of the data voltage V_{data} , that therefore, Hayafuji’s drain current I_d is also necessarily based on gate voltage V_{gate} . Thus, a POSA would have recognized that Hayafuji discloses the current drive voltage (gate-to-source voltage V_{gs}) being indicative of the video signal (data voltage V_{data}).

197. Regarding the clause a “drive current being... independent of the positive power supply voltage,” as a preliminary matter, a POSA would have

understood that what the claimed drive current is “independent of” are the variations in the PPS voltage VDD, not from the PPS voltage VDD itself. This is necessarily true because the drive current can only exist where current flows through the ’521 Patent’s transistor M1, which only happens if the terminal of transistor M1 is powered by voltage VDD. Thus, being “independent of” cannot mean that the drive current is wholly unrelated to the PPS voltage. A POSA would have also recognized that the express purpose of the ’521 Patent is to prevent “the noise and drift components of the PPS voltage VDD [from] appear[ing] directly in the current driver voltage signal Video.OLED which determines the drive current I_D for the OLED pixel element.” *See* Ex. [1001], the ’521 Patent 2:63-65; A POSA would have therefore understood “independent of” as referring to the noise and drift components of the PPS voltage.

198. Hayafuji explains that “[t]he present invention has been developed... to provide a drive device and a drive method of a light emitting display panel in which deterioration of the display quality of an image caused by a ripple component generated in a power supply circuit... can be effectively reduced.” *See* Ex. [1006], Hayafuji, ¶ 0028.

199. Hayafuji teaches “in the voltage addition circuit **15**, treating the data voltage V_{data} as a base, the ripple component V_{ri} extracted by the ripple component

extraction circuit **14** is added to the base. The output thereof as $V_{gate}...$ is supplied to the gate of a light emission drive transistor **Tr2**” (*see* Ex. [1006], Hayafuji ¶ 0049) and that “it can be said that the ripple component V_{ri} obtained by the ripple component extraction circuit **14** is a ripple component having approximately the same phase and the same amplitude as those of the ripple component supplied to the source of the light emission drive transistor **Tr2**.” *See* Ex. [1006], Hayafuji ¶ 0053.

200. A POSA would have quickly recognized that because Hayafuji’s (1) drain current I_d is based on the gate-to-source voltage V_{gs} as discussed above, (2) gate-to-source voltage V_{gs} is the difference between gate voltage V_{gate} and drive voltage V_a , and (3) gate voltage V_{gate} and drive voltage V_a both include the ripple component V_{ri} which is thus cancelled out in gate-to-source voltage V_{gs} , that therefore, Hayafuji’s drain current I_d is “independent of” drive voltage V_a (i.e., drain current I_d is “independent of” ripple component V_{ri}). Thus, a POSA would have recognized that Hayafuji discloses the drive current (drain current I_d) being... independent of (unaffected by ripple component V_{ri}) the positive power supply voltage (drive voltage V_a).

201. Therefore, Hayafuji discloses that the drive current being proportional to a current drive voltage being indicative of the video signal and independent of the positive power supply voltage.

b) Claim 2

[2]: The AMOLED display system of claim 1, wherein the video drive signal is indicative of the sum of or the difference between the positive power supply voltage and the video signal and the current drive voltage is indicative of the difference between the positive power supply voltage and the video drive signal.

202. Hayafuji discloses that the video drive signal is indicative of the sum of or the difference between the positive power supply voltage and the video signal and the current drive voltage is indicative of the difference between the positive power supply voltage and the video drive signal.

203. According to Hayafuji the extracted ripple component is added to Vdata.

In the embodiment shown in FIG. 6, a ripple component extraction circuit **14** and a voltage addition circuit **15** are provided and are constituting the ripple component supply means. The ripple component extraction circuit **14** extracts a ripple component included in a drive voltage V_a generated by the above-described DC-DC converter, and a ripple component V_{ri} extracted by this ripple component extraction circuit **14** is supplied to one input terminal of the voltage addition circuit **15**. The data voltage V_{data} transmitted via the above-mentioned data line Bl is input to the other input terminal of the voltage addition circuit **15**.

See Ex. [1006], Hayafuji at ¶ 0048

204. According to Hayafuji the output signal V_{gate} is applied to the gate of Tr2.

Accordingly, in the voltage addition circuit **15**, treating the data voltage V_{data} as a base, the ripple component V_{ri} extracted by the ripple component extraction circuit **14** is added to the base. The output thereof as V_{gate} is supplied to a scan selection transistor **Tr1** represented by reference character **SW1**, and the V_{gate} is supplied to the gate of a light emission drive transistor **Tr2** by the turning on of the transistor **Tr1** during the addressing time and is written in a capacitor C_s .

See Ex. [1006], Hayafuji at ¶ 0049.

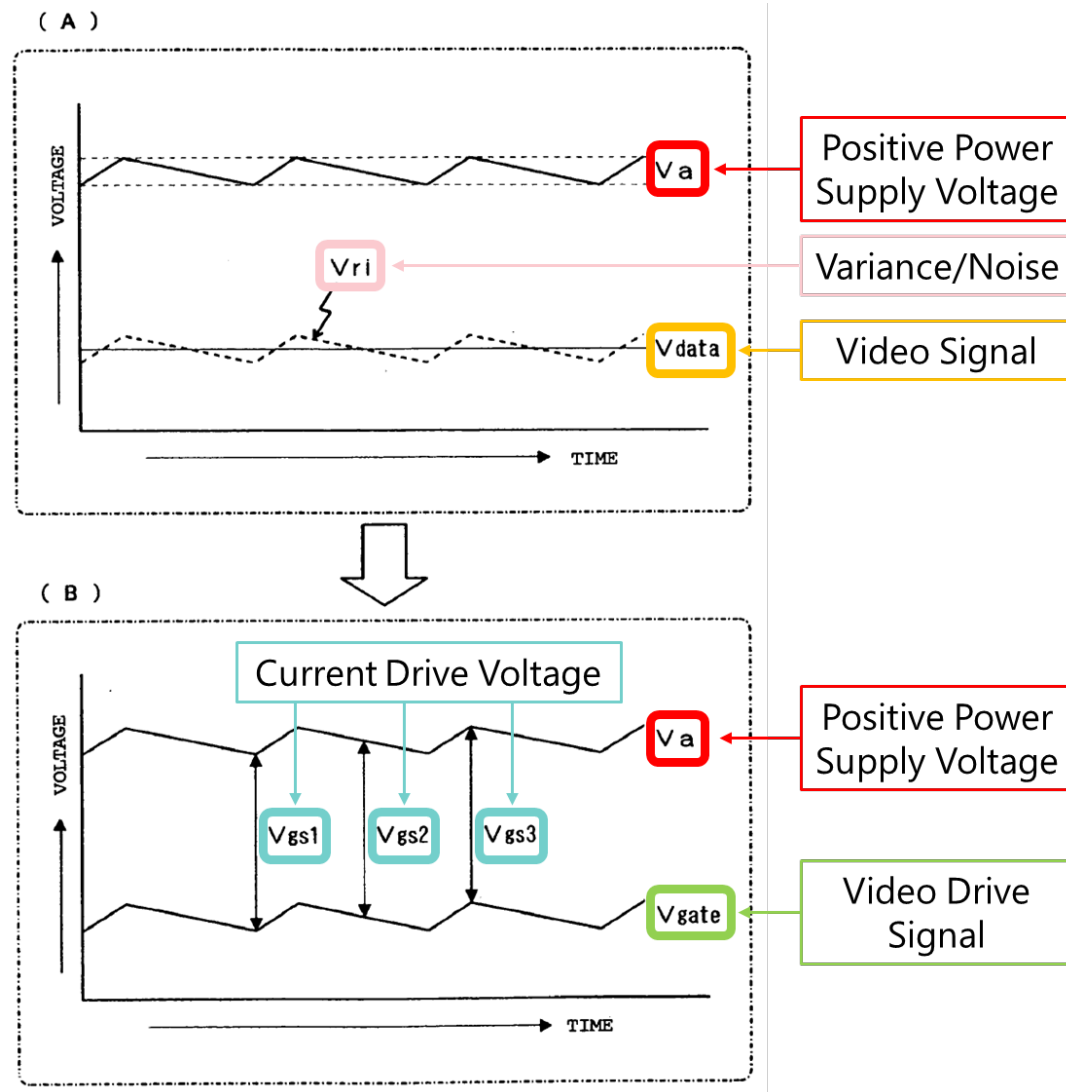
205. Thus Hayafuji discloses that that (1) the drive voltage V_a is the sum of a constant DC output voltage component (herein “ V_{dc} (constant)”)) of the drive voltage V_a and the extracted ripple component V_{ri} ; (2) that the gate voltage V_{gate} is the sum of the data voltage V_{data} and the extracted ripple component V_{ri} ; and consequently, (3) that the gate voltage V_{gate} is indicative of the sum of or the difference between the drive voltage V_a and the data voltage V_{data} :

$$V_a = V_{dc} + V_{ri} \quad (1)$$

$$V_{gate} = V_{data} + V_{ri} \quad (2)$$

$$V_{gate} = V_{data} + V_a - V_{dc} (constant) \quad (3)$$

206. Therefore, consistent with FIG.8 (annotated) below, a POSA would have recognized that Hayafuji discloses the video drive signal (gate voltage V_{gate}) is indicative of the sum of or the difference between the positive power supply voltage (drive voltage V_a) and the video signal (data voltage V_{data}). See Ex. [1006], Hayafuji at FIG.8 (annotated).



See Ex. [1006], Hayafuji at FIG.8 (annotated).

207. Hayafuji discloses that the potential difference between the drive voltage V_a supplied to the source of Tr_2 , and the voltage V_{gate} supplied to its gate is an approximately constant value.

Here, it can be said that the ripple component V_{ri} obtained by the ripple component extraction circuit **14** is a ripple component having approximately the same phase and the same amplitude as those of the

ripple component supplied to the source of the light emission drive transistor **Tr2**.

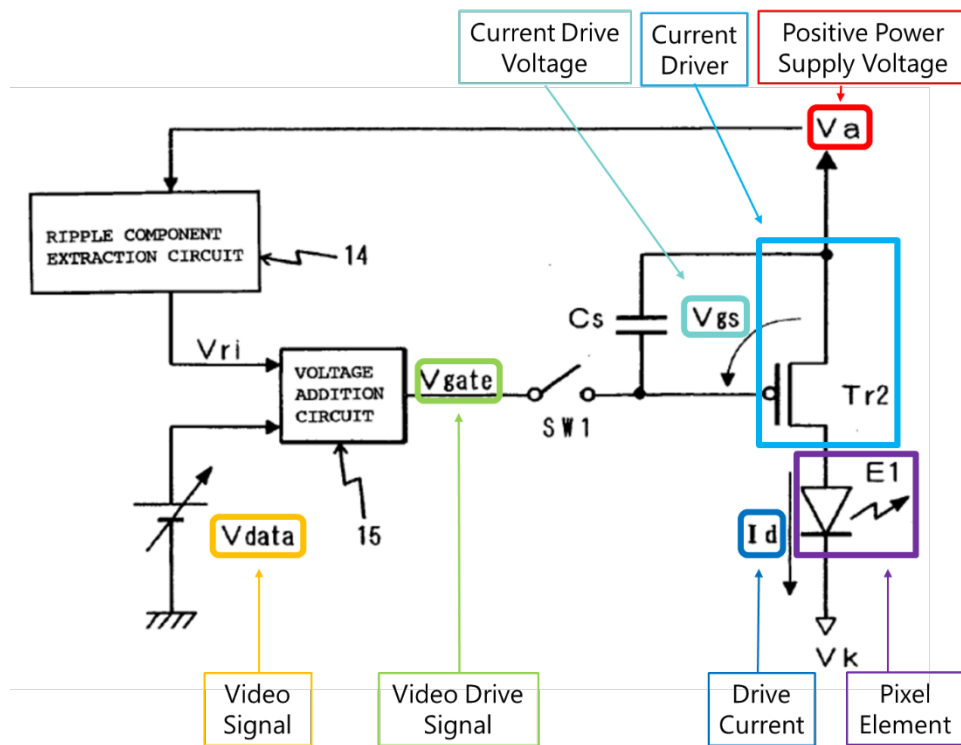
Therefore, although a slight delay is produced by the ripple component extraction circuit **14** and the voltage addition circuit **15**, the potential difference between the drive voltage V_a supplied to the source of the light emission drive transistor **Tr2** and the gate voltage V_{gate} supplied to the gate of the same transistor **Tr2**, that is, the gate-to-source voltage= V_{gs} , represents an approximately constant value all the time regardless of timing of addressing as shown in FIG. 8B. That is, as exemplified by V_{gs1} , V_{gs2} , V_{gs3} in FIG. 8B, the same level of V_{gs} is applied between the gate and the source at any of addressing timings.

See Hayafuji at ¶ 0053.

208. Therefore, Hayafuji discloses that the gate-to-source voltage V_{gs} is the difference between the drive voltage V_a and the gate voltage V_{gate} :

$$V_{gs} = V_a - V_{gate}$$

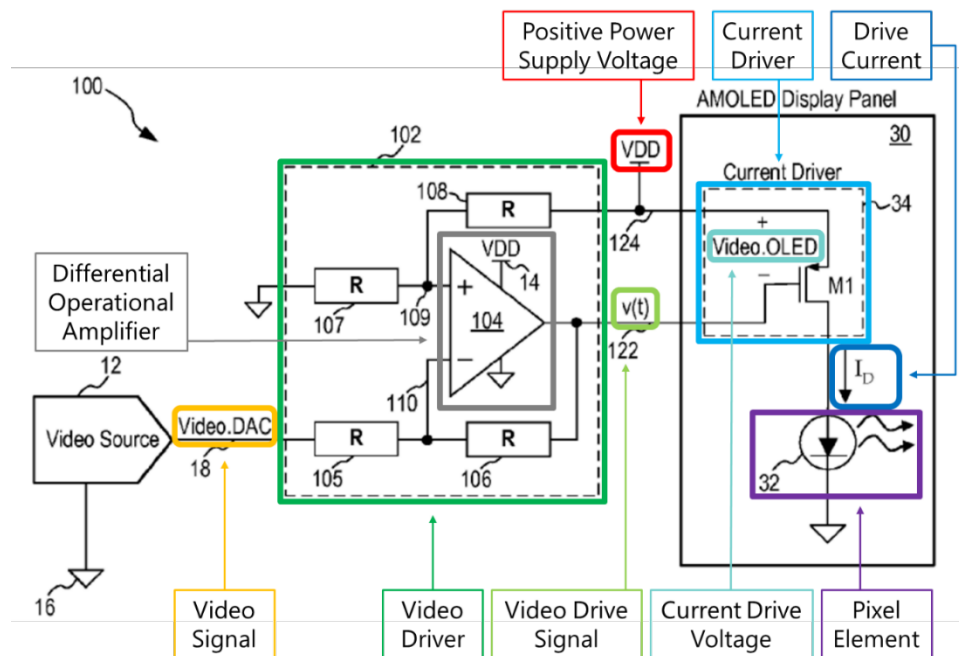
209. Therefore, consistent with FIG.6 (annotated) below, a POSA would have recognized that Hayafuji further discloses the current drive voltage (gate-to-source voltage= V_{gs}) is indicative of the difference between the positive power supply voltage (drive voltage V_a) and the video drive signal (gate voltage V_{gate}).



See Ex. [1006], Hayafuji at FIG.6 (annotated).

C. Ground 4: Claims 1, 2, 3 and 5 of the '521 Patent are Obvious in View of Hayafuji and the Knowledge of a POSA

210. The figure below is an annotated reproduction of FIG. 2 of the '521 Patent illustrating the first embodiment.



See Ex. [1001], the '521 Patent at FIG. 2 (annotated).

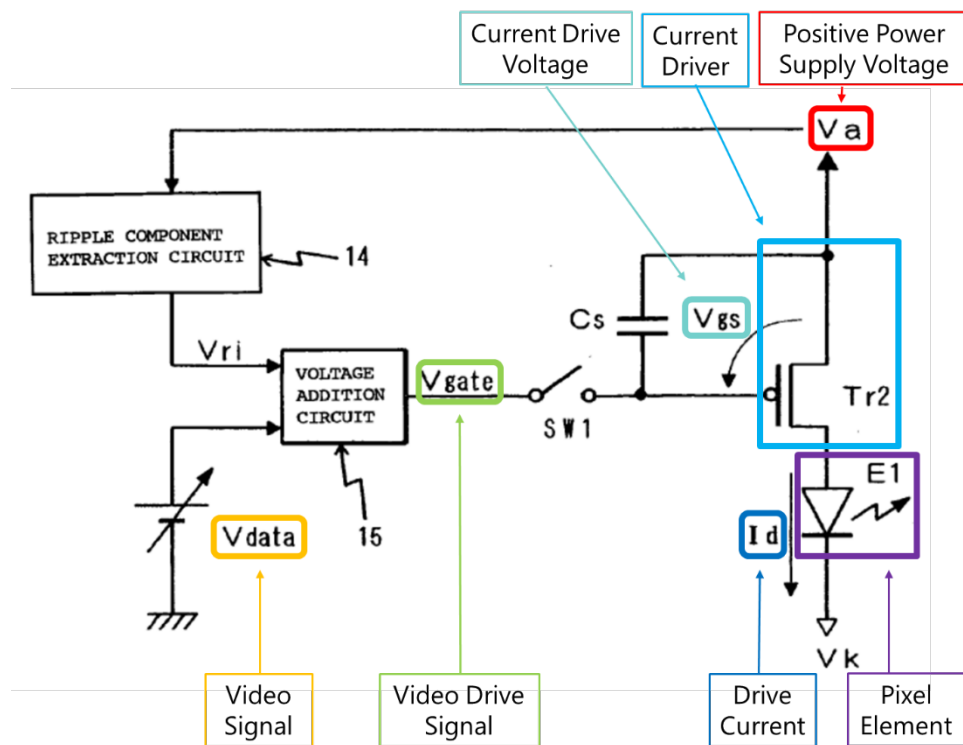
a) Claim 3

[3]: The AMOLED display system of claim 2, wherein the video driver comprises a differential instrumentation amplifier circuit for providing the video drive signal being the difference between the positive power supply voltage and the video signal.

211. The '521 Patent explains that whereas conventional video drivers would connect the positive input terminal of the op-amp through a resistor to ground voltage, the '521 Patent connects the positive input terminal of the op-amp through a resistor to the PPS voltage VDD, in order to reference the V_{GS} to VDD such that the output video drive signal $v(t)$ of the op-amp tracks any PPS voltage variations.

See Ex. [1001], the '521 Patent at 4:53-65. See also Ex. [1010], Horowitz Text at pg. 181.

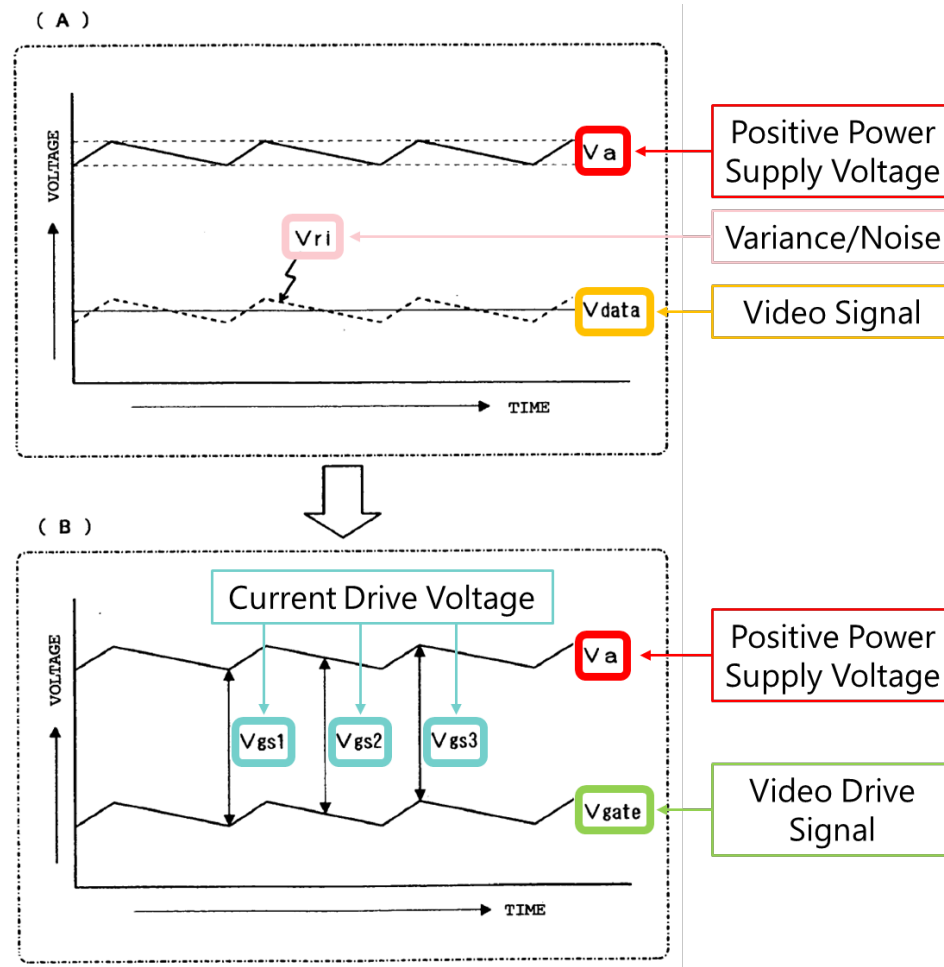
212. As detailed above with respect to Ground 3, Limitation [1-A], Hayafuji discloses a video driver (circuitry in green annotation below for Video Driver) receiving the video signal (data voltage V_{data}) and generating a video drive signal (gate voltage V_{gate}) indicative of the video signal and referenced to a positive power supply voltage (drive voltage V_a) of the AMOLED display panel.



See Ex. [1006], Hayafuji at FIG. 6 (annotated).

213. Furthermore, as detailed above with respect to Ground 3, Claim 2, Hayafuji discloses that the video drive signal (gate voltage V_{gate}) is indicative of the

sum of or the difference between the positive power supply voltage (drive voltage V_a) and the video signal (data voltage V_{data}).

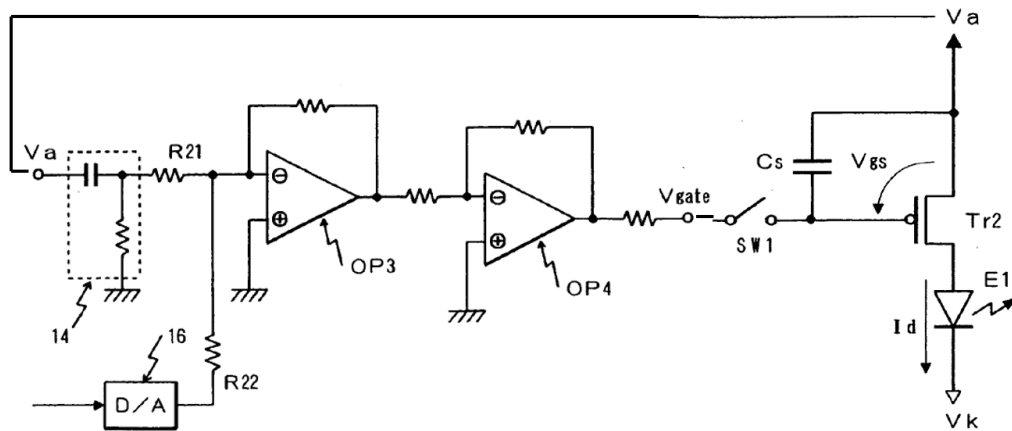


See Ex. [1006], Hayafuji at FIG. 8 (annotated).

214. A POSA would have found it obvious to modify the circuits of Hayafuji such that video drive signal (gate voltage V_{gate}) is not only 'indicative' of the sum of or the difference between the positive power supply voltage (drive voltage V_a) and the video signal (data voltage V_{data}), but also specifically configured such that the video drive signal (gate voltage V_{gate}) is output by the video driver as the

difference between the positive power supply voltage (drive voltage V_a) and the video signal (data voltage V_{data}).

215. Such a modification is detailed below with respect to FIG. 6 and FIG. 7 of Hayafuji. The figure below is the original design of Hayafuji.

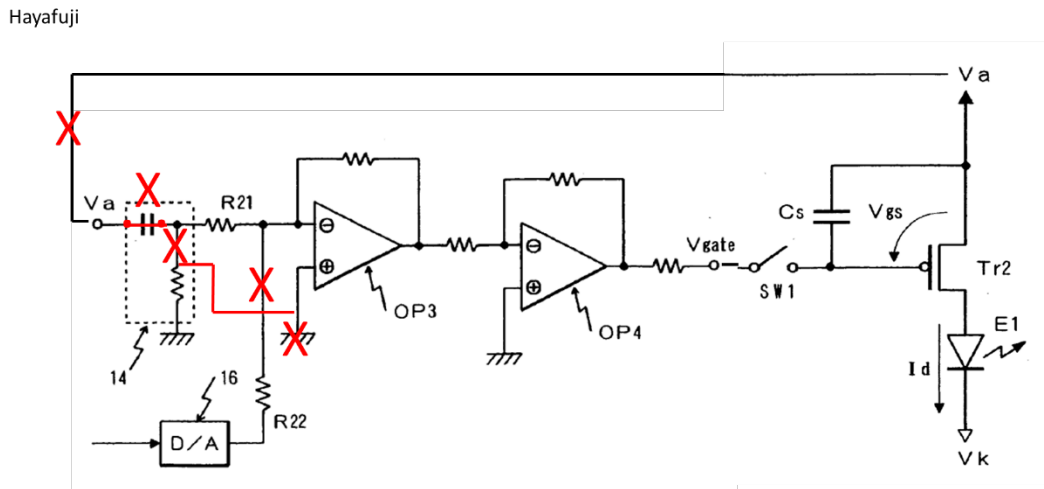


See Ex. [1006], Hayafuji at FIG. 6 and FIG. 7.

216. As shown above the original circuit of Hayafuji relies on a high-pass filter 14 comprised of a capacitor and resistor.² The input to the filter is V_a (positive power supply voltage). The output of the filter is added to the data signal from 16 with the result outputted from op-amp OP3. The output of block 16 D/A is equivalent to V_{DATA} or the video signal. See Ex. [1006], Hayafuji at ¶ 0051.

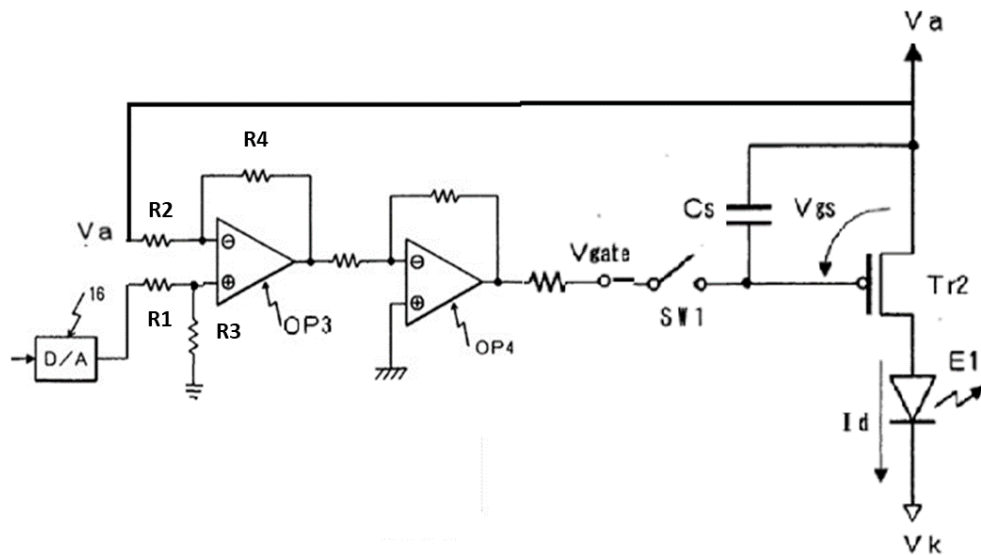
² Hayafuji at ¶ 0050 refers to block 14 of Fig. 6 as a “bypass filter.” Based on its configuration with a capacitor in series and a resistor connected to ground, a POSA would recognize this as a high pass filter.

217. Below is a modified configuration of FIG. 6 and FIG. 7 of Hayafuji. The modification includes the removal of filter 14, applying V_a to one terminal of OP3 and applying the data signal from 16 to the other terminal of OP3.



See Ex. [1006], Hayafuji at FIG. 6 and FIG. 7 (during modification).

218. The circuit following the modification is shown below.



See Ex. [1006], Hayafuji at FIG. 6 and FIG. 7 (modified).

219. A POSA would have been motivated to reconfigure Hayafuji in this manner for at least the following reasons.

220. First, Hayafuji discloses that there is a ripple component in the power source that drives the OLED element. This is due to the DC-DC converter.

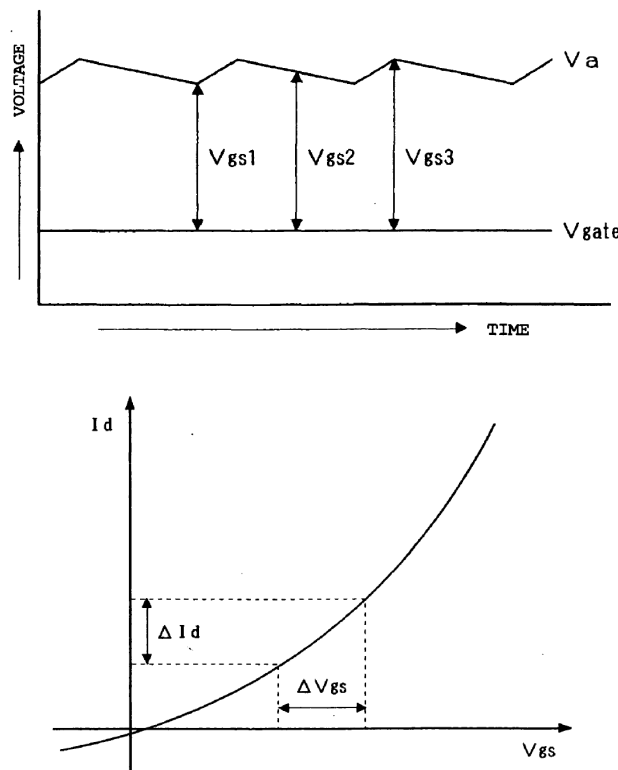
Here, for the drive voltage V_a supplied to the source of the transistor Tr2, the boosted voltage by the DC-DC converter is employed as already described, and in this type of DC-DC converter, it is unavoidable that ripple noise (ripple component) is superimposed on the voltage V_a to some degree since switching operation is accompanied as a matter of its operating principle. In the DC-DC converter, although the level of the ripple component can be decreased more when a large capacitance capacitor is used for the smoothing capacitor Cl, decrease effect for the ripple component cannot be expected so much compared to the ratio at which the capacitance thereof is increased.

See Ex. [1006], Hayafuji at ¶ 0022.

221. Hayafuji further states that the capacitor size is limited. *See* Ex. [1006], Hayafuji at ¶ 0023, (“the capacitance of the smoothing capacitor has to be restrained to some degree exists in an actual condition.”).

222. Second, Hayafuji teaches that this ripple causes deterioration of the light emitting elements. *See* Ex. [1006], Hayafuji at ¶ 0024, (“the drive voltage V_a on which the ripple component shown in FIG. 3 is superimposed is supplied to the source of the light emission drive transistor Tr2... Therefore, a gate-to-source voltage which changes corresponding to the ripple component is supplied between

the source and the gate of the transistor Tr2 shown in FIG. 2, in response to respective timings of addressing, as shown as V_{gs1} , V_{gs2} , V_{gs3} in FIG. 3.”) *See also* Ex. [1006], Hayafuji at ¶ 0025, (“ FIG. 4 shows a V_{gs}/I_d characteristic (a gate-to-source voltage versus drain current characteristic) of a TFT, represented by the transistor Tr2, and when the gate-to-source voltage changes within a range of ΔV_{gs} , accompanied by this, the drain current also changes within a range of ΔI_d .”).



See Ex. [1006], Hayafuji at FIG. 3 and FIG. 4.

Here, it has been known that the organic EL element exhibits a light emission intensity characteristic approximately proportional to the value of the current flowing in this element. Accordingly, as a result of the state in which V_{gs} changes influenced by the ripple component corresponding to timings of addressing as described above, a result in which the light emission intensity of each EL element in the light emitting display panel 1 differs for each scan line occurs. Thus, in the display panel, a problem that the display quality of an image is considerably deteriorated, that is, for example, a fine striped pattern or phenomenon of flicker occurs and the like, can occur.

See Ex. [1006], Hayafuji at ¶ 0025.

223. Third, to deal with the effect of the ripple on the OLED pixels Hayafuji teaches to extract the ripple component of the power source V_a and add this to the data signal. Then when this signal is placed on the gate of the drive transistor and references to V_a the ripple is in essence cancelled out across and does not appear as part of the gate-to-source voltage. *See* Hayafuji at ¶ 0030, (“by supplying a ripple component having approximately the same phase and amplitude as those of a ripple component superimposed on a drive power source which is supplied to the source electrode of the light emission drive transistor to the gate electrode of the light emission drive transistor at an addressing time.”). *See* Ex. [1006], Hayafuji at FIG. 8.

224. Based on the knowledge of a POSA specifically as it relates to traditional op-amp circuits, modifying the op-amp to generate the difference of the

power source signal and the data signal using a differential instrumentation³ amplifier would allow for an improved system that would be more immune to noise in the power source. The invention of Hayafuji is inherently limited by the design of the filter (the capacitor and resistor of 14 in Hayafuji FIG. 6). This design means there will be a range of noise of certain frequencies that will not be prevented from impacting the OLED brightness. For example low frequency noise such as drift would not be prevented from impacting OLED brightness. Thus, a POSA would have realized that the modified circuit allows for an OLED driver with improved immunity to power source noise not limited just to ripple but to other forms of noise such as drift.

225. Furthermore, the removal of the capacitor of the filter 14 disclosed would also potentially reduce the required real estate for the circuit something suggested by Hayafuji with respect to the capacitor of the DC-DC converter. *See* Ex. [1006], Hayafuji at ¶ 0023.

226. Furthermore a POSA would have been motivated to make this obvious modification because it is a trivial design change comprised of well-known

³ The term “instrumentation amplifier” is not defined in the ’521 Patent. A POSA would have understood that such an amplifier (e.g., FIG. 6 in Hayafuji) is simply a differential amplifier with a high common-mode rejection ratio. *See* Ex. [1010], Horowitz Text at pg. 421.

components (op amps and resistors) used in well known configurations that would better accomplish the stated goal of Hayafuji.

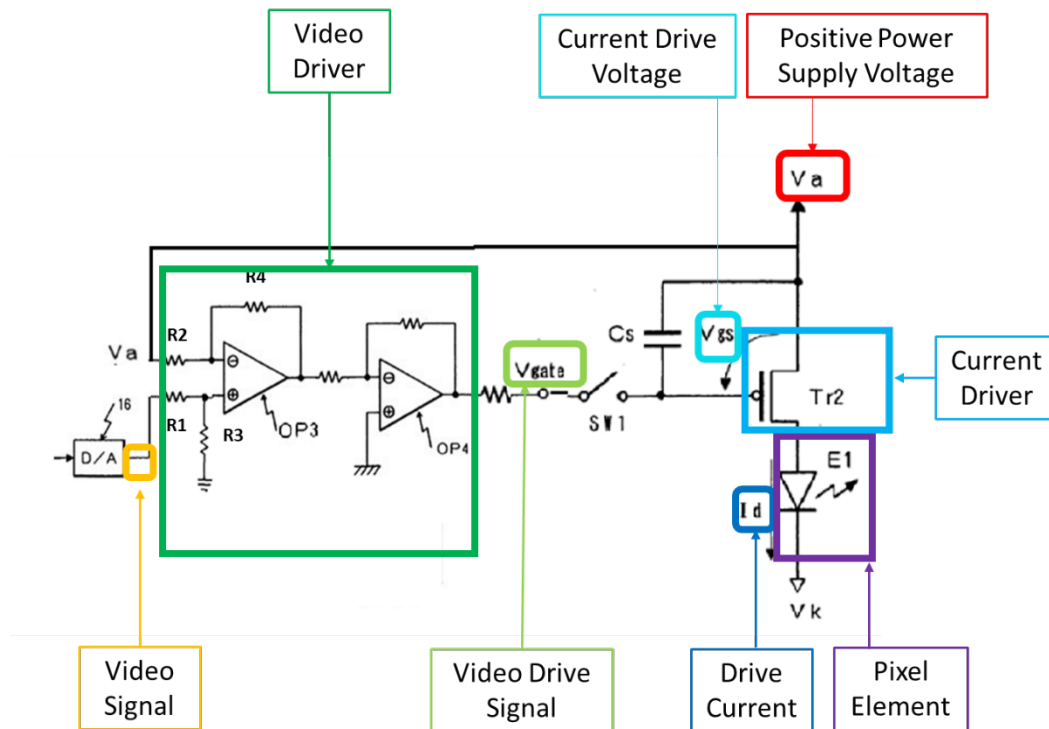
The present invention has been developed as attention to the above-described problems has been paid, and it is an object of the present invention to provide a drive device and a drive method of a light emitting display panel in which deterioration of the display quality of an image caused by a ripple component generated in a power supply circuit represented by a DC-DC converter can be effectively reduced without increasing the circuit scale so much.

See Ex. [1006], Hayafuji at ¶ 0028.

227. Finally, the modification of the Hayafuji circuit into a differential amplifier circuit is based on a well-known and fundamental op amp configuration, specifically where the non-inverting terminal is the reference voltage against which the inverting terminal voltage is compared to. A POSA would have had a reasonable expectation of success when making this modification because of this. *See* also Ex. [1010], Horowitz Text at pg. 181.

228. Therefore, as described above and consistent with the annotated and modified version of FIGs. 6 and 7 below, a POSA would have found it obvious, in view of Hayafuji, that the video driver (circuitry in green annotation below for Video Driver) comprises a differential instrumentation amplifier circuit (operational amplifier OP3) for providing the video drive signal (gate voltage V_{gate}) being the

difference between the positive power supply voltage (drive voltage V_a) and the video signal video signal (data voltage V_{data}).



See Ex. [1006], Hayafuji at FIGs. 6 and 7 (combined; modified; annotated).

229. Furthermore, the modified circuit still satisfies all the limitations of Claims 1 and 2 of the '521 Patent as set forth below.

230. The only modification made to Hayafuji was to its driver circuit, specifically modifying OP3 from a summing amplifier with filter to a differential amplifier. Thus the modified Hayafuji circuit is still used with an active matrix

organic light emitting diode (AMOLED) display system comprising an AMOLED display panel receiving a video signal to be displayed on the AMOLED display panel, the AMOLED display panel comprising a plurality of organic light emitting diode (OLED) pixel elements, the AMOLED display system as required by Limitation [1-Pre].

231. The modification made to the video driver does not change that fact that is it is still a video driver that receives a video signal generating a video drive signal (V_{gate}) indicative of the video signal (V_{data}) and referenced to a positive power supply voltage (V_a) of the AMOLED display panel as required by Limitation [1-A]. This is further shown by the below equation:

$$V_{gate} = V_a - V_{data}$$

232. After modification Hayafuji still includes a current driver **Tr2** coupled to at least one OLED pixel element, the current driver receiving the video drive signal and the positive power supply voltage and providing a drive current to the at least one OLED pixel element as required by Limitation [1-B]. This is further shown by the below equation:

$$V_{gs} = V_a - V_{gate} = V_a - V_a + V_{data} = V_{data}$$

233. Furthermore, the drive current is proportional to a current drive voltage being indicative of the video signal and independent of the positive power supply

voltage in the modified Hayafuji circuit as required by Limitation [1-C]. This is further shown by the below equation:

$$I_{OLED} = k(V_{gs} - V_t) = k(Vdata - Vt)$$

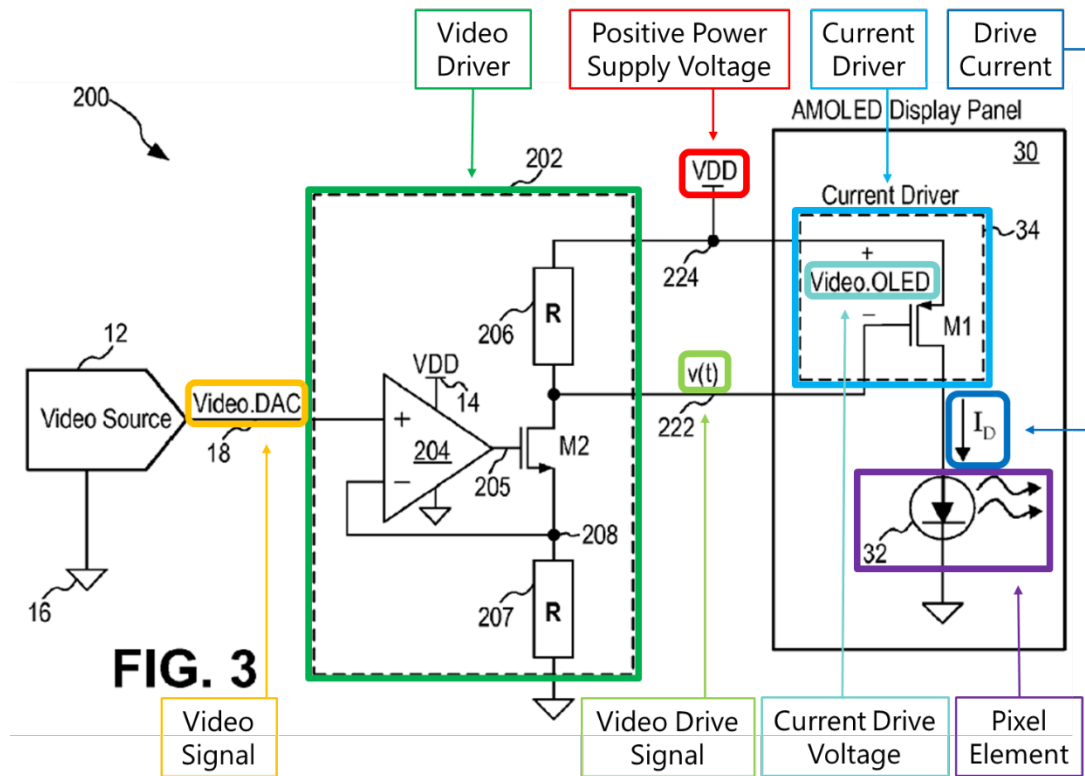
234. Finally, the video drive signal is indicative of the difference between the positive power supply voltage and the video signal and the current drive voltage is indicative of the difference between the positive power supply voltage and the video drive signal as required by Claim [2]. This is further shown by the below equation:

$$V_{gate} = Va - Vdata$$

b) Claim 5

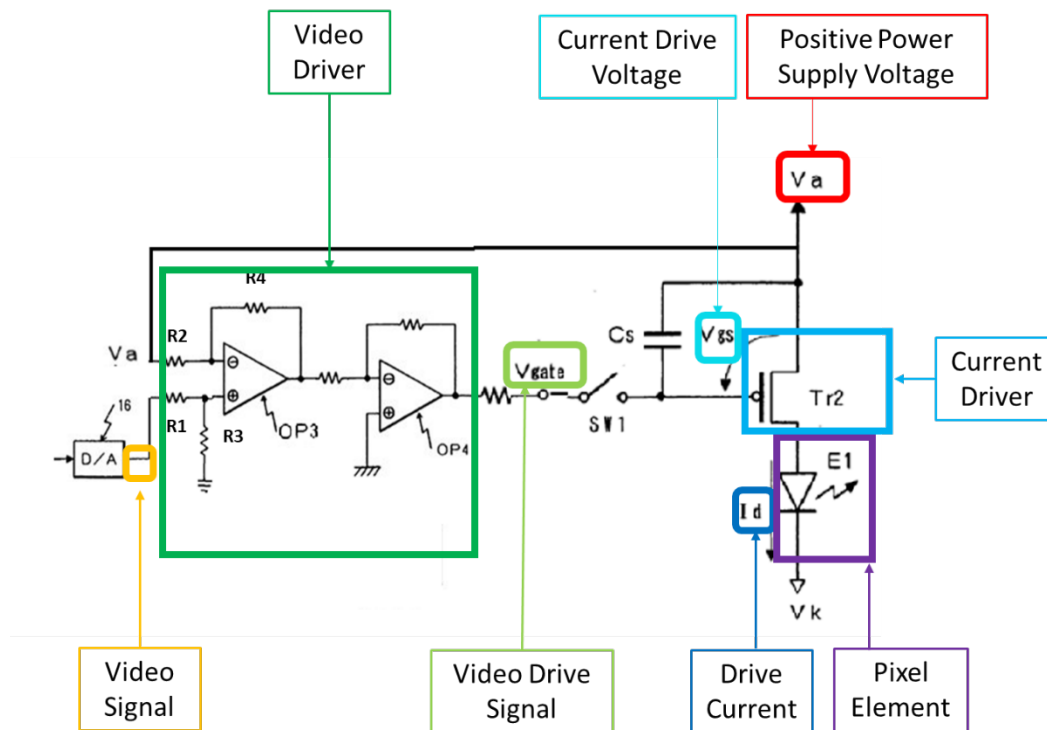
[5]: The AMOLED display system of claim 2, wherein the video driver comprises a current mode isolator circuit for providing the video drive signal being the difference between the positive power supply voltage and the video signal

235. The figure below is an annotated reproduction of FIG. 3 of the '521 Patent illustrating the second embodiment.



See Ex. [1001], the '521 Patent at FIG. 3 (annotated).

236. As discussed above, Hayafuji discloses the elements of Claims 1 and 2. Ex.[1006], Figs. 6, 8. Additionally, as explained with respect to Figure 3, a POSA would have been motivated to modify the Hayafuji circuit as shown below. See Ground 3, Limitations [1-C] and Claim [2]



See Ex.[1006],Hayafuji, Figs. 6, 7 (combined, modified, annotated).

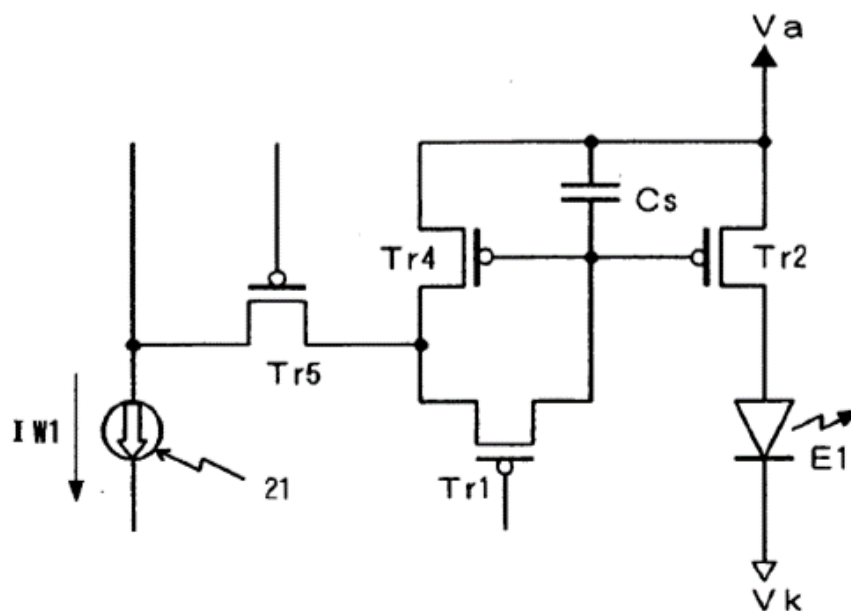
237. Hayafuji notes that “[t]he combination shown in **FIG. 10** of the ripple component extraction circuit **14**, the voltage addition circuit **15**, and V_{data} represented by the variable voltage source is the same as the structure shown in **FIG. 6** already described.” See Ex, [1006], Hayafuji at ¶ 0060.

238. Thus, a POSA would have understood that the Ground 4, Claim 3 analysis is similarly applicable here, in that it would be obvious for the video driver to be configured in the same manner as discussed for Ground 4, Claim 3 such that

the video driver provides the video drive signal being the difference between the positive power supply voltage and the video signal.

239. For the reasons discussed below, a POSA would also have recognized that Hayafuji discloses the video driver comprising a current mode isolator circuit.

240. Hayafuji discloses that “**FIG. 9** shows a pixel structure of a current mirror drive method, and in the example shown in this **FIG. 9**, a p-channel type light emission drive transistor **Tr2** and the same p-channel type mirror operation transistor **Tr4** are symmetrically provided wherein the gates thereof are commonly connected, the sources of the [sic] both transistors **Tr2**, **Tr4** are commonly connected, and a charge-holding capacitor C_s is connected between the sources and the gates thereof. The drive voltage V_a is supplied to the sources of the [sic] both transistors **Tr2**, **Tr4**.” See Ex. [1006], Hayafuji at ¶ 0056.



See Ex.[1006], Hayafuji FIG. 9.

241. Hayafuji explains the “[a] scan selection transistor **Tr1** constituted by the same p-channel type TFT is connected between the gate and the drain of the mirror operation transistor **Tr4**, and by an ON operation of this scan selection transistor **Tr1**, the transistors **Tr2**, **Tr4** function as a current mirror circuit. A write transistor **Tr5** constituted by a p-channel TFT is also turned on together with the scan selection transistor **Tr1** being turned on, and thus a write current source **21** is connected via the write transistor **Tr5**.” *See* Ex. [1006], Hayafuji at ¶ 0057.

242. Hayafuji further described that “a current path from the power source V_a to the write current source **21** via the transistors **Tr4**, **Tr5** is formed during an address period. By the operation of the current mirror, current corresponding to current **IW1** flowing in the power source **21** is supplied to the EL element **E1** via the light emission drive transistor **Tr2**. By this operation, the gate voltage of the transistor **Tr4** corresponding to the current **IW1** flowing in the write power source **21** is written in the capacitor **Cs**. After the gate voltage value is written in the capacitor **Cs**, the scan selection transistor **Tr1** is brought to an OFF state, and the light emission drive transistor **Tr2** operates to allow a predetermined current (**=IW1**) to be supplied to the EL element **E1** based on electrical charge accumulated in the

capacitor C_s , whereby the light emission drive for the EL element **E1** is continued.”

See Ex. [1006], Hayafuji at ¶ 0058.

243. Hayafuji further discloses “**FIG. 10** shows an example of the structure of the write current source **21** shown in **FIG. 9** and a structure controlling the current value of the write current source **21** by the ripple component included in the drive voltage V_a . The write current source **21** is constituted by a combination of a PNP type transistor **Q3** and a resistor **R25** which is connected between the emitter of this transistor **Q3** and the ground in the example shown in **FIG. 10**.” *See* Ex. [1006], Hayafuji at ¶0059.

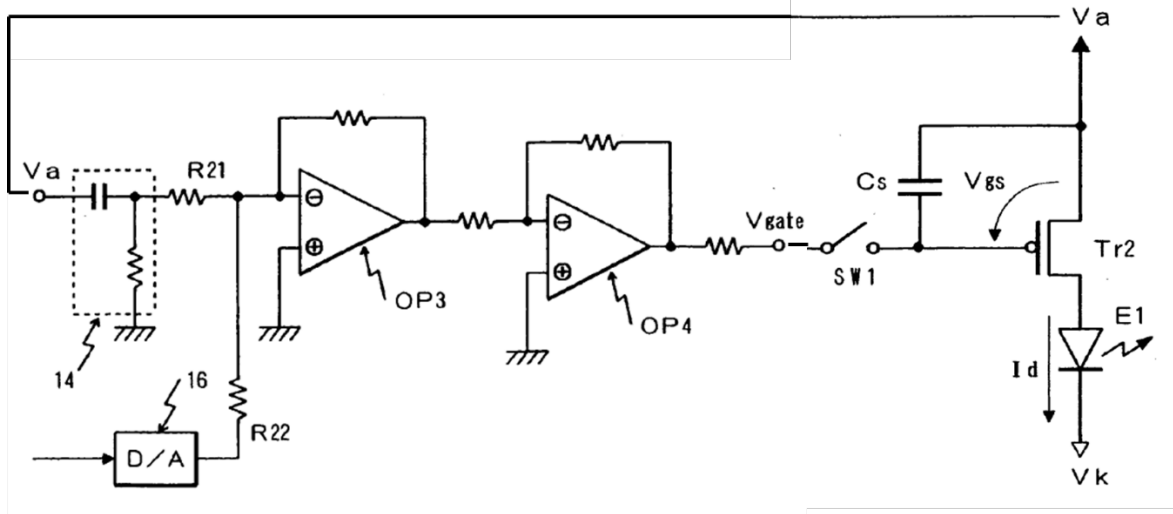
244. Hayafuji teaches “[t]he output of the voltage addition circuit **15** is supplied to the base of the transistor **Q3** via a voltage amplifier **18** constituted by an operational amplifier. Accordingly, absorption current **IW1** by the transistor **Q3** constituting the write current source **21** operates such that the current value of the ripple component changes every moment by the ripple component included in the drive voltage V_a .” *See* Ex. [1006], Hayafuji at ¶ 0060.

245. Hayafuji explains “[a]ccordingly, a voltage value corresponding to the data voltage V_{data} supplied from the data driver is written in the charge-holding capacitor C_s in the pixel structure of the current mirror drive method shown in **FIG. 9** without being influenced by the ripple component included in the drive voltage V_a .

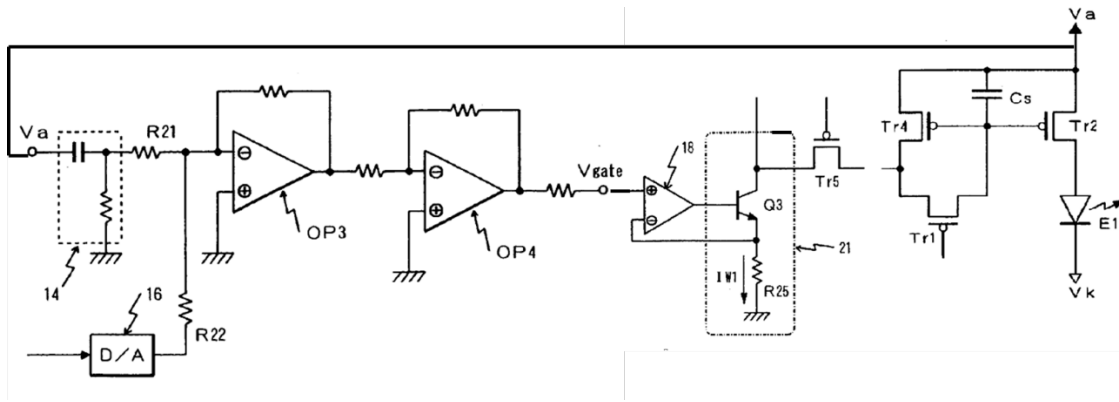
Therefore, in the pixel structure of the current mirror drive method shown in **FIG. 9**, by adopting the circuit structure shown in **FIG. 10**, a problem that a state is brought in which light emission intensity differs for each scan line in the display panel **1** influenced by the ripple component can be avoided.” See Ex. [1006], Hayafuji at ¶ 0061.

246. A POSA would have understood that *Hayafuji*’s video driver discussed above is a ‘current-mode’ circuit because the video driver (circuitry in green Video Driver annotation below) generates and provides a control current to the current driver (circuitry in blue Current Driver annotation below). Specifically, a POSA would have recognized this because transistor **Q3** generates control current **IW1**, which controls current through transistor **Tr4**, which is configured together with transistor **Tr2** as a current mirror, and thereby controls drive current **Id** through pixel element **32**.

247. The annotated figures below are the original circuits from Hayafuji showing the first embodiment and second embodiment.



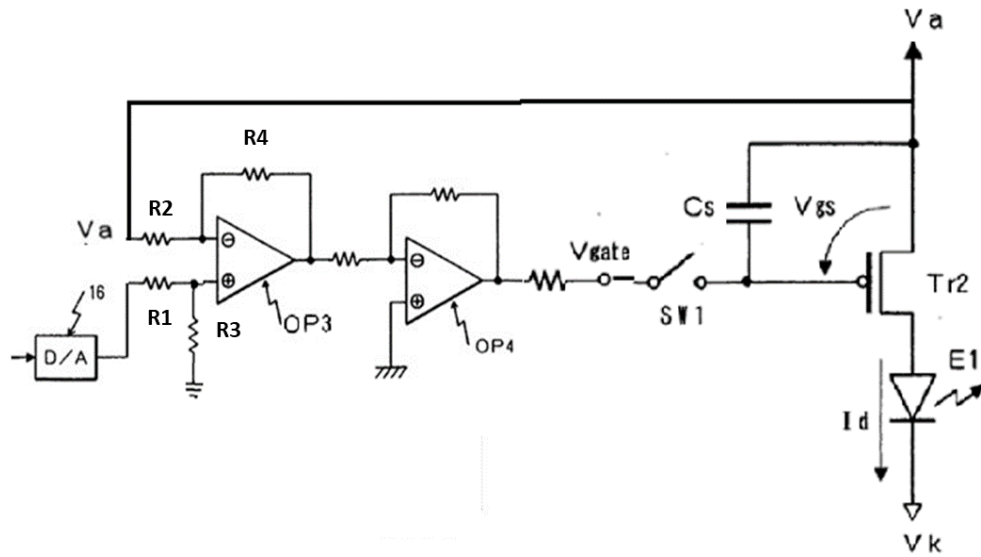
See Ex. [1006], Hayafuji at FIG. 1 and FIG. 7 (combined).



See Ex. [1006], Hayafuji at FIG. 7, FIG. 9 and FIG. 10(combined).

248. According to Hayafuji in both embodiments the current driver **Tr2** is not “influenced by the ripple component.” See Ex. [1006], Hayafuji at ¶¶ 54 and 61. Therefore the conversion from voltage to current by the current mirror does not change the fact that the rippled component is compensated for.

249. Following the modification of Hayafuji as detailed in Ground 4, Claim 3, the signal Vgate is the difference between the positive power supply Va and the video signal exiting D/A 16.



See Ex. [1006], Hayafuji at FIG. 6 and FIG. 7 (modified).

250. In this circuit the voltage applied to the drive transistor Tr2 is also not influenced by ripple in Va. The addition of the circuitry of FIG. 10 of Hayafuji simply converts this difference from a voltage into a current as it does in the second embodiment of Hayafuji.

251. A POSA would have understood that, in view of the intrinsic record, the plain and ordinary meaning of “current mode isolator circuit” is a circuit that is a “current-mode” circuit, i.e., a circuit in which the current driver for the OLED pixel

is provided with a control current by the video driver, and serves as an isolator for the control current signal.

252. Furthermore, a POSA would also have recognized that Hayafuji's video driver is an isolator for control current **IW1**. A POSA would have understood, based on the specification of the '521 Patent, that the claimed "isolator" functionality is describing isolating the control current from being influenced by variations in the PPS: "By using video driver 202 incorporating a current mode isolator, the video drive signal $v(t)$ is made referenced to the power supply voltage VDD so that the current drive voltage signal Video.OLED is made independent of the power supply voltage VDD. Variations in the power supply voltage VDD will no longer adversely affect the AMOLED display." *See* Ex. [1001], the '521 Patent at 6:1-7.

253. Furthermore, as described in Ground 3, Limitation [1-C] being "independent of" cannot mean that the drive current is wholly unrelated to the PPS voltage. A POSA would have also recognized that the express purpose of the '521 Patent is to prevent "the noise and drift components of the PPS voltage VDD [from] appear[ing] directly in the current driver voltage signal Video.OLED which determines the drive current I_D for the OLED pixel element." *See* Ex. [1001], the '521 Patent 2:63-65; A POSA would have therefore understood "independent of" as referring to the noise and drift components of the PPS voltage.

254. By connecting V_a to the non-inverting terminal of OP3 and V_{data} to the inverting terminal, V_{gate} becomes the difference between these two signals. As this modified V_{gate} includes the ripple component V_{ri} because V_{gate} is still the output at opamp OP3 and output of OP4 (buffer). This is illustrated in the equations below where $V_{a'}$ is the component of V_a

$$V_a = V_{a'} + V_{ri}$$

$$V_{gate} = V_{a'} + V_{ri} - V_{data}$$

255. As, Hayafuji's drain current I_d is based on the gate-to-source voltage V_{gs} , where gate-to-source voltage V_{gs} is the difference between gate voltage V_{gate} and drive voltage V_a , the gate voltage V_{gate} and drive voltage V_a both still include the ripple component V_{ri} which is thus cancelled out in gate-to-source voltage V_{gs} . Therefore, as modified, Hayafuji's drain current I_d is "independent of" drive voltage V_a (i.e., drain current I_d is "independent of" ripple component V_{ri}). Thus, a POSA would have recognized that Hayafuji discloses the drive current (drain current I_d) being... independent of (unaffected by ripple component V_{ri}) the positive power supply voltage (drive voltage V_a).

256. Thus, a POSA would have recognized that Hayafuji discloses the drive current (drain current I_d) being... independent of (unaffected by ripple component V_{ri}) the positive power supply voltage (drive voltage V_a).

257. A POSA would therefore have recognized that Hayafuji also expressly discloses isolating control current I_{W1} from variations in PPS voltage V_a : “Accordingly, a voltage value corresponding to the data voltage V_{data} supplied from the data driver is written in the charge-holding capacitor C_s in the pixel structure of the current mirror drive method shown in **FIG. 9** without being influenced by the ripple component included in the drive voltage V_a .” *See* Ex. [1006], Hayafuji at ¶ 0061.

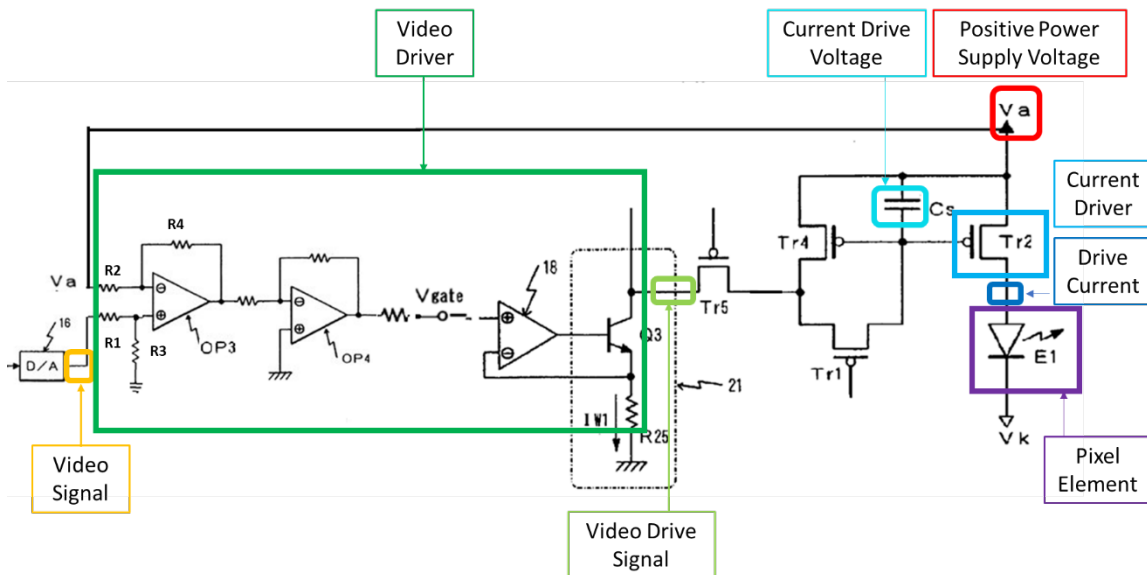
258. As such, a POSA would have recognized that Hayafuji’s circuitry including transistor Q3 is a current mode isolator circuit.

259. A POSA would have been motivated to use a current programming technique disclosed by Hayafuji as it allowed for improved compensation to transistor mobility and threshold variations and thus better display performance. *See* Ex. [1012], Han Article at pg. 53.

260. A POSA would be well versed in the design of both voltage programmed and current programmed pixel driver circuit. Therefore, as Hayafuji discloses that the method of adding the ripple current component to the video signal can be adapted from a voltage programmed pixel to a current programmed pixel while still reducing the effect of power supply ripple, a POSA would have had reasonable expectation of success when using the modified Hayafuji differential

amplifier arrangement in a current programmed implementation rather than a voltage programmed implementation.

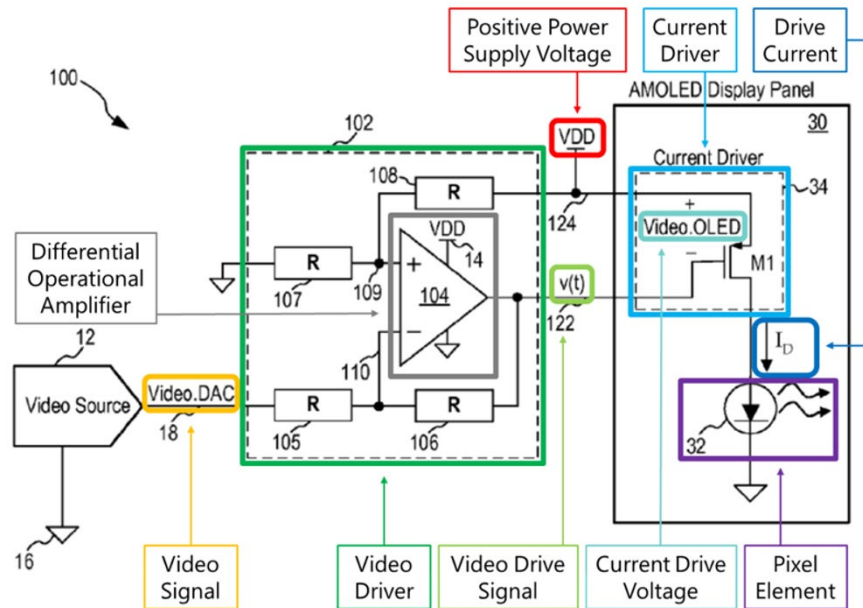
261. Therefore, consistent with the Ground 3, Claim 3 analysis, and FIGs.7, 9, 10 (combined / modified / annotated) below, a POSA would have found it obvious, in view of Hayafuji, the video driver comprises a current mode isolator circuit (circuitry including transistor Q3) for providing the video drive signal (gate voltage V_{gate} at transistors Tr2 and Tr4 driven by control current I_{w1}) being the difference between the positive power supply voltage (drive voltage V_a) and the video signal (data voltage V_{data}). *See* Ex. [1006], Hayafuji at FIGs.7, 9, 10 (combined / modified / annotated).



See Ex. [1006], Hayafuji at FIG. 6, FIG. 9 and FIG. 10 (annotated and modified).

D. Ground 5: Claims 1, 2, 3 and 4 of the '521 Patent are Obvious in View of Steer and the Knowledge of a POSA

262. The figure below is an annotated reproduction of FIG. 2 of the '521 Patent illustrating the first embodiment.



See Ex. [1001], the '521 Patent at FIG. 2 (annotated).

a) Claim 1

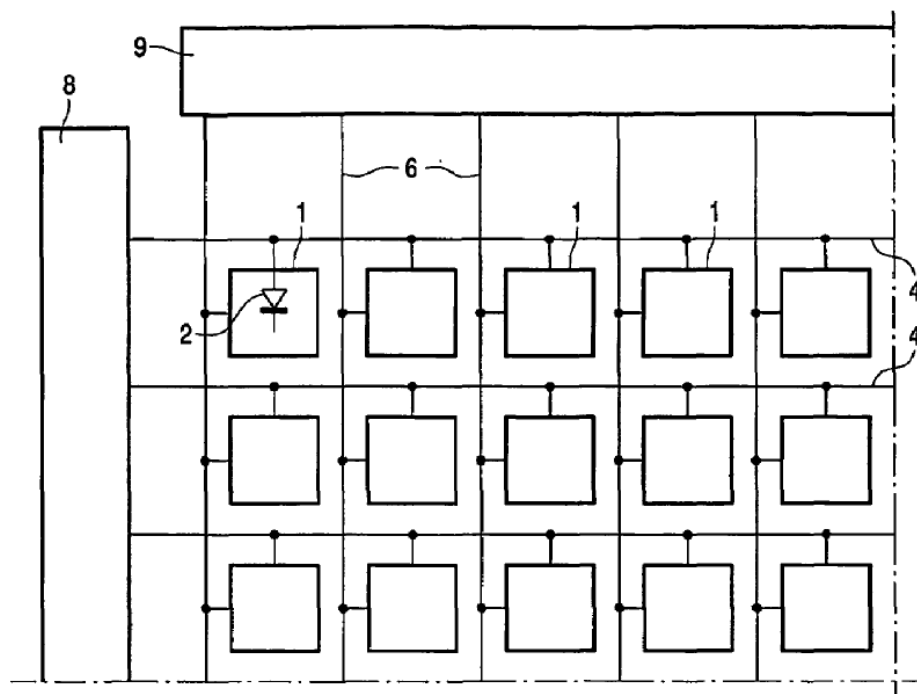
[1-Pre]: An active matrix organic light emitting diode (AMOLED) display system comprising an AMOLED display panel receiving a video signal to be displayed on the AMOLED display panel, the AMOLED display panel comprising a plurality of organic light emitting diode (OLED) pixel elements, the AMOLED display system comprising:

263. To the extent the preamble is limiting, Steer discloses an active matrix organic light emitting diode (AMOLED) display system comprising an AMOLED

display panel receiving a video signal to be displayed on the AMOLED display panel, the AMOLED display panel comprising a plurality of organic light emitting diode (OLED) pixel elements, the AMOLED display system.

264. Steer discloses an active matrix OLED display the includes an array of display pixels. *See* Ex. [1008], Steer at Abstract, (“[a]n active matrix electroluminescent display device compris[ing] an array of display pixels.”). *See also* Ex. [1008], Steer at 1:11-14, (“[t]he display elements may comprise organic thin film electroluminescent elements, for example using polymer materials, or else light emitting diodes (LEDs) using traditional III-V semiconductor compounds.”).

265. Steer further discloses a display panel consisting of rows, columns and pixel circuits.



See Ex. [1008], Steer at FIG. 1

FIG. 1 shows a known pixel circuit for an active matrix addressed electroluminescent display device. The display device comprises a panel having a row and column matrix array of regularly-spaced pixels, denoted by the blocks **1** and comprising electroluminescent display elements **2** together with associated Switching means, located at the intersections between crossing sets of row (selection) and column (data) address conductors **4** and **6**. Only a few pixels are shown in the Figure for simplicity. In practice, there may be several hundred rows and columns of pixels. The pixels **1** are addressed via the sets of row and column address conductors by a peripheral drive circuit comprising a row, Scanning, driver circuit **8** and a column, data, driver circuit **9** connected to the ends of the respective sets of conductors.

See Ex. [1008], Steer at 2:3-13.

266. Steer further explains that “a comparator section **50** compares the voltage at node **43** with an input voltage at input **52** representing the desired current.”

See Ex. [1008], Steer at 9:14-15.

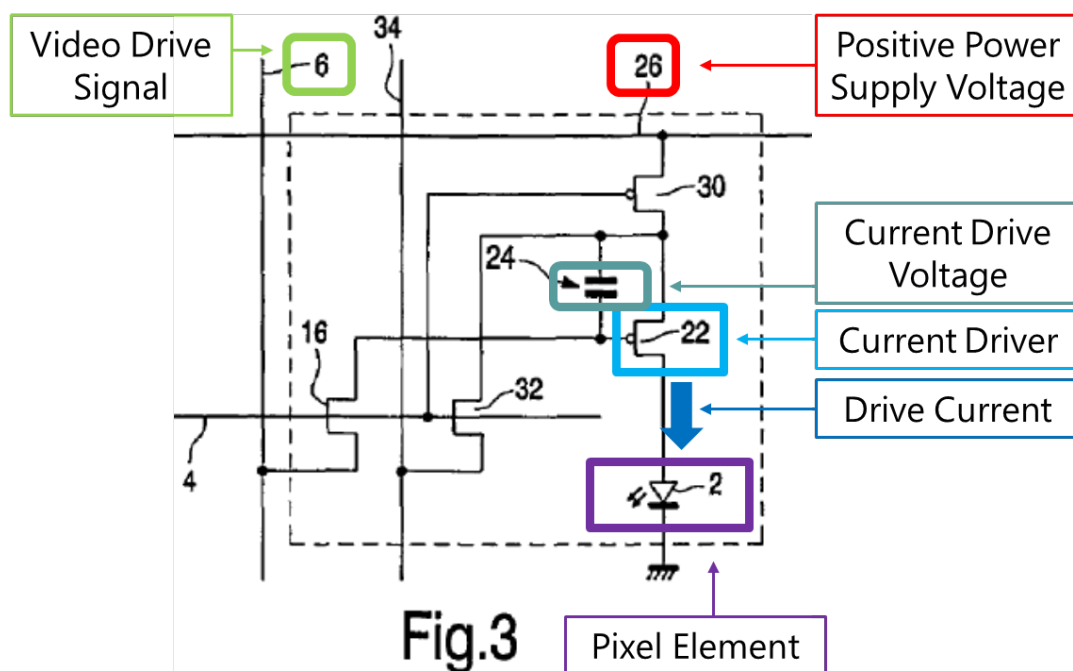
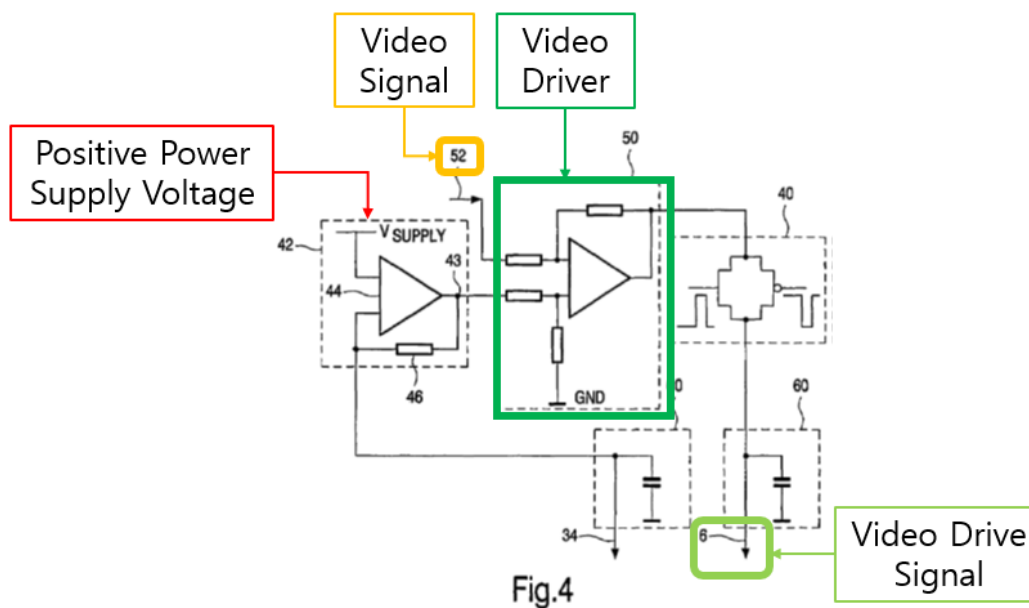
267. Though, Steer does not expressly disclose that input voltage **52** is a video signal, A POSA would have been motivated to make the obvious design choice of inputting a video signal at **52** at least because it's well-known in the art to use video signals as inputs to display panels and particularly for video drivers like in Steer.

268. As described in the '521 Patent the video signal that is used to set the drive voltage, biases the gate of the drive transistor and sets the brightness along

with the voltage V_{DD} . *See* Ex. [1001], the '521 Patent at 1:65:2:1, (“The analog video signal Video.DAC is summed With a DC voltage VDC (node 14) at a summer 20 to generate the video drive signal $v(t)$ for driving the AMOLED display panel.”). *See* Ex. [1001], the '521 Patent at 1:37-39, (“Thus, the brightness level of an AMOLED display Will tend to drift with power supply voltage [V_{DD}] variations.”). A POSA would realize that as input 52 represents the “desired current” flowing in the OLED that this also corresponds to the desired brightness of the OLED which according to Steer, is set in by the input voltage 52, the video signal and the power supply voltage as applied to the drive transistor.

269. Furthermore, Steer is directed to an “analogue implementation,” providing a POSA further motivation to use an (analogue) video signal. *See* Ex. [1008], Steer at 11:3-4. *Steer* also suggests that matrix display devices, such as in *Steer*, are commonly used for video because they have “demonstrated their ability to be used practically for video display devices.” *See* Ex. [1008], Steer at 1:15-16.

270. Steer further explains “FIG. 3 shows a first pixel arrangement in accordance with the invention,” and “FIG. 4 shows the column driver architecture for a display using the pixel of FIG. 3.” *See* Ex. [1008], Steer at 8:3-4, 7:26-27. Thus, a POSA would have understood that FIGs. 3 - 4 correspond to the same embodiment. *See* Ex. [1008], Steer at FIGs. 3 - 4 (annotated).



See Ex. [1008], Steer at FIGs. 3-4 (annotated).

271. Therefore, Steer discloses an active matrix organic light emitting diode (AMOLED) display system comprising an AMOLED display panel receiving a video signal to be displayed on the AMOLED display panel, the AMOLED display panel comprising a plurality of organic light emitting diode (OLED) pixel elements and thus discloses limitation [1-Pre] of the '521 Patent.

[1-A]: a video driver receiving the video signal and generating a video drive signal indicative of the video signal and referenced to a positive power supply voltage of the AMOLED display panel; and

272. Steer discloses a video driver receiving the video signal and generating a video drive signal indicative of the video signal and referenced to a positive power supply voltage of the AMOLED display panel.

273. Steer describes that transistor switching circuits are associated with each pixel. *See* Ex. [1008], Steer at 1:6-8, (“[t]his invention relates to electroluminescent display devices, particularly active matrix display devices having thin film switching transistors associated with each pixel.”).

274. Furthermore, Steer describes that each pixel is addressed by column and row driver circuits. *See* Ex. [1008], Steer at 2:10-13, (“[t]he pixels **1** are addressed via the sets of row and column address conductors by a peripheral drive

circuit comprising a row, scanning, driver circuit **8** and a column, data, driver circuit **9** connected to the ends of the respective sets of conductors.”).

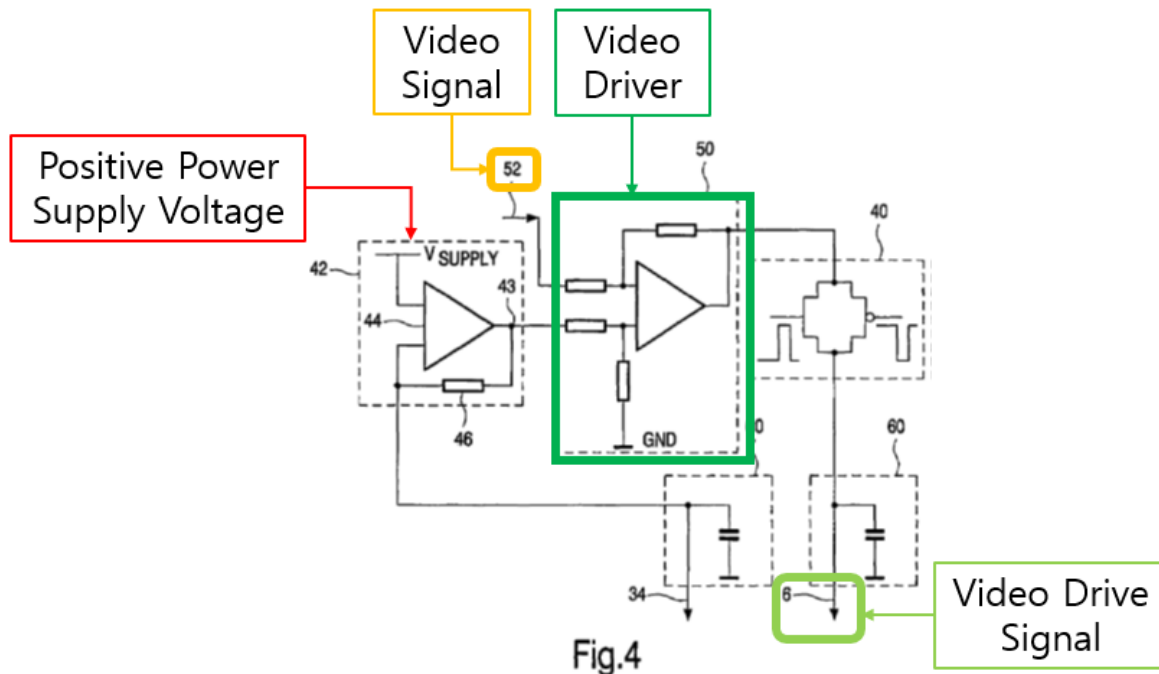
275. For the column driver Steer discloses that it may include a feedback circuit (*see* Steer at 8:18-20) including a current-to-voltage converter that includes an amplifier biased with V_{SUPPLY} .

A current-to-voltage converter section **42** provides a voltage at node **43** dependent on the current being provided down the current-measurement supply line **34**. The current-to-voltage converter section **42** has a high open loop gain amplifier **44** so that the current-measurement Supply line, connected to the virtual earth amplifier input, is held at the voltage V_s . on the other input of the amplifier **44**. This is the same supply voltage as for the power supply line **26**.

See Ex. [1008], Steer at 9:4-10.

276. Steer further explains that the voltage output of the amplifier may differ from the supply voltage by a value related to the resistance of, and current through, feedback resistor **46**. *See* Steer at 9:10-12, (“[t]he voltage at node **43** [i.e., the output of section **42**] differs from this supply voltage by a value RxI , where R is the resistance of the feedback resistor **46** and I is the current flowing.”).

277. Steer further discloses a comparator **50** that compares the node **43** an input voltage at **52** that represents the desired current. *See* Ex. [1008], Steer at 9-14-15, (“a comparator section **50** compares the voltage at node **43** with an input voltage at input **52** representing the desired current.”).



See Steer FIG. 4 (annotated).

278. Finally as shown above the signal on 6 is applied to the gate of transistor 22 through transistor 16. Thus, comparator section 50 corresponds to the claimed video driver.

279. Therefore, a POSA would have recognized that “comparator section 50” that “acts as a driver” corresponds to the claimed video driver. Moreover, as discussed above for Ground 5, Limitation [1-Pre], a POSA would have understood it was obvious that “input voltage at input 52” is the claimed video signal.

280. Additionally, a POSA would have recognized that the output of comparator section 50, which is a comparison between “the voltage at node 43 with

an input voltage at input **52** representing the desired current” corresponds to the claimed video drive signal indicative of the video signal and referenced to a positive power supply voltage of the AMOLED display panel. In particular, voltage on node **43** corresponds to V_{SUPPLY} added to R multiplied by I , where R is the resistance of resistor **46** and I is the current flowing. *See* Ex. [1008], Steer at 9:10-14; Steer’s Node **43** voltage is thus represented as:

$$\text{Steer (1): } V_{43} = V_{SUPPLY} + R * I$$

281. Therefore, a POSA would have recognized that voltage at node **43** is V_{SUPPLY} with a offset, and therefore, a comparison between voltage at node **43** (V_{43}) and input voltage at input **52** via the operational amplifier would result in a signal indicative of voltage at input **52** (V_{52} or $input(t)$) (i.e., the claimed video signal) and referenced to V_{SUPPLY} (i.e., the claimed positive power supply voltage of the AMOLED display panel). The resulting output on node **6** (V_6) (the claimed video drive signal) in Steer is shown below in equation (2), which shows that the VGS includes video signal ($input(t)$) subtracted from V_{SUPPLY} .

$$\text{Steer (2): } V_6 = V_{SUPPLY} + R * I - input(t)$$

282. The ’521 Patent similarly explains that vide drive signal $v(t)$ is “referenced to” V_{DD} in equation (5) reproduced below, which shows video signal

(Video.DAC) being subtracted from VDD. *See* Ex. [1008], Steer at 6:10-31 (“Equation 5”).

’521 Eq.(5):
$$v(t) = V_{DD} - Video.DAC$$

283. Therefore, as described above and consistent with the annotated image above in the annotated version of FIG. 3 and 4, Steer discloses a video driver (circuitry in green annotation below for Video Driver) receiving the video signal (signal on input **52** representing the desired current) and generating a video drive signal (output on line **6**) indicative of the video signal and referenced to a positive power supply voltage (drive voltage V_{SUPPLY}) of the AMOLED display panel.

[1-B]: a current driver coupled to at least one OLED pixel element, the current driver receiving the video drive signal and the positive power supply voltage and providing a drive current to the at least one OLED pixel element,

284. Steer discloses a current driver coupled to at least one OLED pixel element, the current driver receiving the video drive signal and the positive power supply voltage and providing a drive current to the at least one OLED pixel element.

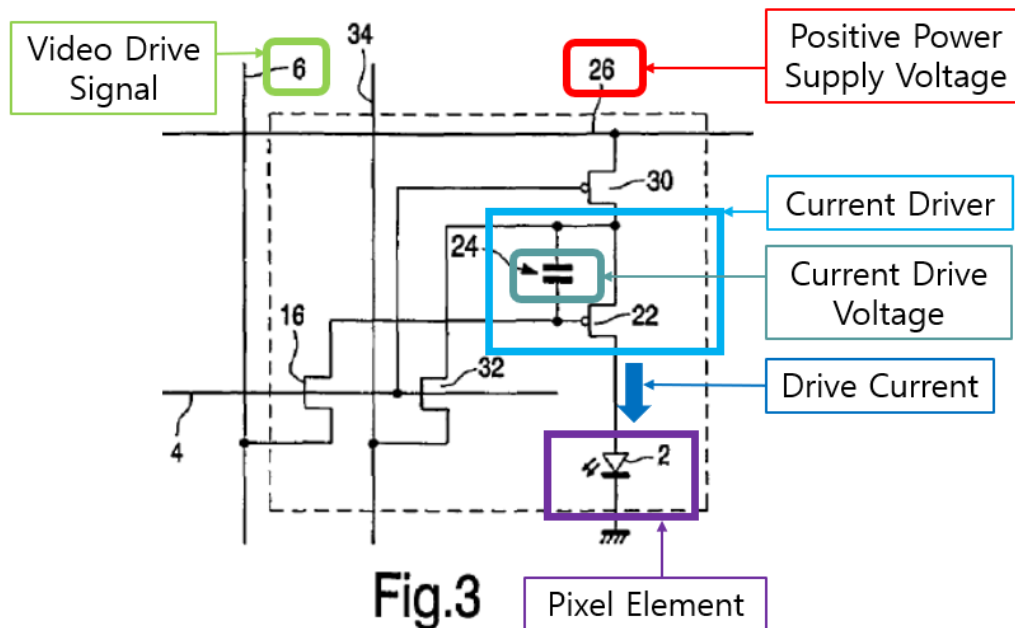
285. Steer discloses “Each pixel **1** comprises the EL display element **2** and associated driver circuitry.... the address transistor **16** supplies the column conductor voltage [e.g., line **6**] to a current source **20**, which comprises a drive transistor **22** and a storage capacitor **24**.” *See* Ex. [1008], Steer at 2:31-3:6. Steer

teaches that “row (selection) and column (data) address conductors [respectively correspond to] **4** and **6**.” *See* Ex. [1008], Steer at 2:8-9. Steer explains “the control line voltage on the column conductor **6** provides drive of the drive transistor **22** in the pixel.” *See* Ex. [1008], Steer at 9:25-26. Thus, a POSA would have understood that output of the comparator section **50** is column conductor 6, which is supplied to the gate of the drive transistor **22** when the transistor **16** and transmission gate **40** are turned on. *See* Ex. [1008], Steer at 8:32-9:3

286. *Steer* discloses that in FIG. 3, “the potential on the current-measurement supply line **34** is maintained at the power supply voltage V_{SUPPLY} , which corresponds to the voltage on the power supply line 26 during the pixel drive phase.” *See* Ex. [1008], Steer at,10:14-16. Moreover, during the pixel drive phase where current is supplied to the pixel, PPS line **26** corresponds to V_{SUPPLY} . *Steer* also explains that during the drive phase after the pixel programming mode, that transistor **30** is turned on such that PPS line **26** voltage would appear at the source terminal of the drive transistor **22**. *See* Ex. [1008], Steer at,10:5-10.

287. Therefore, consistent with FIG. 3 (annotated) above, a POSA would have recognized that Steer discloses a current driver (circuitry in light blue annotation including drive transistor **22** and capacitor **24**) coupled to at least one OLED pixel element (organic EL element **2**), the current driver receiving the video

drive signal (column conductor voltage 6 gate-connected via transistor 16 to drive transistor 22) and the positive power supply voltage (supply voltage 26) and providing a drive current (via drive transistor 22) to the at least one OLED pixel element. *See Ex. [1008], Steer at FIG. 3 (annotated).*



See Ex. [1008], Steer at FIG. 3 (annotated).

[1-C]: the drive current being proportional to a current drive voltage being indicative of the video signal and independent of the positive power supply voltage.

288. Steer discloses that the drive current being proportional to a current drive voltage being indicative of the video signal and independent of the positive power supply voltage.

289. Steer discloses that the column voltage at line **6** is provided to the gate of the drive transistor **22**. *See* Ex. [1008], Steer at 3-6-7, (“the column voltage [via line 6] is provided to the gate of the drive transistor **22**.”).

290. Steer further describes how drive transistor **22** is a PMOS TFT that is biased by the voltage across capacitor **24**.

The column voltage is provided to the gate of the drive transistor **22**, and the gate is held at this voltage by the storage capacitor **24** even after the row address pulse has ended. The drive transistor **22** draws a current from the power supply line **26**.

The drive transistor **22** in this circuit is implemented as a PMOS TFT, so that the storage capacitor **24** holds the gate source voltage fixed. This results in a fixed source-drain current through the transistor, which therefore provides the desired current source operation of the pixel.

See Ex. [1008], Steer at 3:6-13

291. The gate voltage supplied to the gate of the drive transistor **22** results in the gate source voltage being a value equal to the difference between the voltage at the source of the drive transistor **22** (coupled to the positive power supply **26**) and the voltage provided from the driver on line 6 on the gate of the drive transistor **22**. Thus “gate source voltage” is the claimed current drive voltage and the voltage is indicative of the video signal since the gate voltage, as explained with reference to Limitation [1-B], is generated using the video signal on line **52**.

292. As explained above with reference to Limitation [1-B], the current that flows through the drive transistor **22** and into the EL element **2** is the claimed drive current. Further, a POSA would have understood that the gate source voltage changes as the gate voltage changes. Accordingly, a POSA would have understood that the claimed drive current is proportional to the current drive voltage.

293. Moreover, as explained with reference to Limitation [1-A], the video drive signal applied to the gate of the drive transistor **22** is generated by the “comparator section **50**” (i.e., the claimed video driver) via a comparison between the voltage on the input **52** (i.e., the claimed video signal) and a voltage at node **43** that is dependent on V_{SUPPLY} (which is also the voltage on line **26**) (i.e., the claimed positive power supply voltage).

294. Accordingly, generating the video drive signal using the positive power supply voltage and then applying the video drive signal as a gate voltage to drive transistor **22** relative to the positive power supply voltage to generate the drive current renders the current drive voltage independent of the positive power supply voltage as claimed. This change in voltage of V_{SUPPLY} will be recognized both at node **43** and at line **26** and therefore the current drive voltage will be independent of the positive power supply.

295. A mathematical representation of the voltages at each node shows that the V_{SUPPLY} does not appear in the gate to source voltage over the drive transistor **22** and therefore is independent of V_{SUPPLY} for at least the same reasons as described in the '521 Patent. As discussed with reference to Limitation [1-A], V_{SUPPLY} is the same as the voltage on line **26**. The voltage on line **52** is represented by $input(t)$ in equation (1), the voltage on line **43** is represented by equation (2), the voltage on line **6** is represented by equation (3), and the gate-to-source voltage on the drive transistor is represented by equation (4).

$$V_{52} = video\ signal\ (t) \quad (1)$$

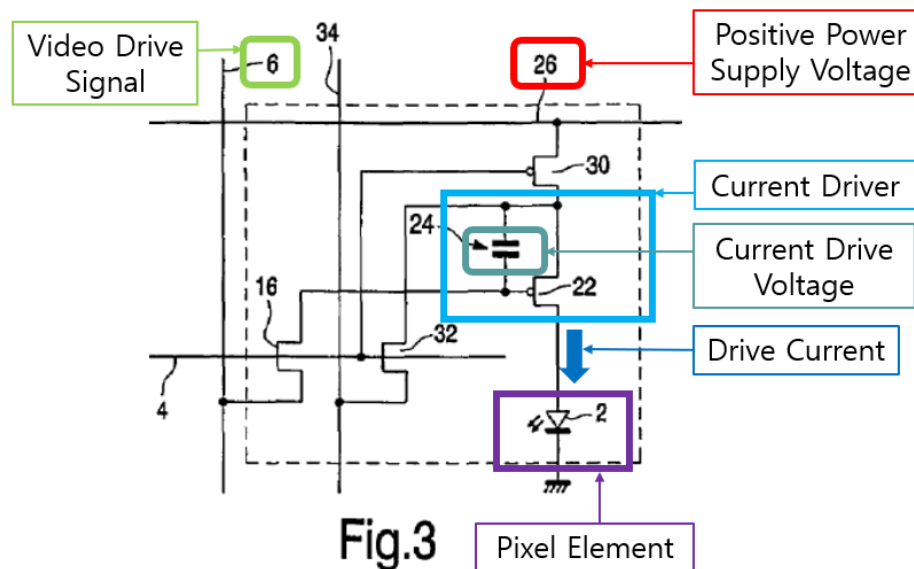
$$V_{43} = V_{SUPPLY} + R * I \quad (2)$$

$$V_6 = V_{43} - V_{52} \quad (3)$$

296. Substituting equations (1)-(3) into equation (4) yields the updated equation (4A).

$$V_{GS} = V_{SUPPLY} + R * I - video\ signal\ (t) - V_{SUPPLY} \quad (4A)$$

297. Since the first V_{SUPPLY} will be eliminated in equation (4A) via subtraction of the second V_{SUPPLY} , the gate-to-source voltage V_{GS} on the drive transistor **22** (i.e., the claimed current drive voltage) is independent of the positive power supply voltage.



See Ex. [1008], Steer FIG. 3 and FIG. 4 (annotated).

b) Claim 2

[2]: The AMOLED display system of claim 1, wherein the video drive signal is indicative of the sum of or the difference between the positive power supply voltage and the video signal and the current drive voltage is indicative of the difference between the positive power supply voltage and the video drive signal.

299. Steer discloses that the video drive signal is indicative of the sum of or the difference between the positive power supply voltage and the video signal and the current drive voltage is indicative of the difference between the positive power supply voltage and the video drive signal.

300. As described above with reference to Limitation [1-A], the video drive signal is generated by the “comparator section 50.”

301. Steer discloses that the comparator section compares the voltage at **43** with input **52**, the desired current and that the voltage at node **43** differs from the supply voltage based on the current though, and the value of resistor **26**. *See* Ex. [1008], Steer at 9:14-15, (“A comparator section **50** compares the voltage at node **43** with an input voltage at input **52** representing the desired current.”). *See also* Ex. [1008], Steer at 9:10-12, (“The voltage at node **43** differs from this supply voltage by a value $R \times I$, where R is the resistance of the feedback resistor **46** and I is the current flowing.”).

302. Steer further discloses that the output of comparator **50** is connected to the column conductor **6** and to the gate of the drive transistor. *See* Ex. [1008], Steer at 10:1-4, (“With reference to FIG. 3, the gate-source voltage for the drive transistor is stored on capacitor **24**. This voltage is derived from the voltage provided by the feedback system on the column conductor **6**.”).

303. Thus, Steer teaches that the drive voltage on line **6** (V_6) (i.e., the claimed video drive signal) is the difference between the voltage at node **43** (V_{43}) and the voltage on input line **52** (input(t)) (i.e., the claimed video signal). Further, a POSA would have understood that V_{43} as discussed with reference to Limitations [1-A] and [1-C] is equal to $V_{\text{SUPPLY}} + R * I$. Consequently, a (V_6) (i.e., the claimed

video drive signal) is indicative of the difference between positive power supply voltage and the video signal, as claimed.

$$V_6 = V_{43} - input(t)$$

$$V_{43} = V_{supply} + R * I$$

$$V_6 = V_{supply} + R * I - input(t)$$

304. Moreover, as discussed with reference the Limitation [1-C], the claimed current drive voltage is the gate-to-source voltage over the drive transistor **22** (V_{GS}). As also discussed, V_{GS} is equal to the difference between the gate voltage applied via line **6** (V_6) and the voltage on line **26** (V_{SUPPLY}). Consequentially, a POSA would have understood that the current drive voltage (V_{GS}) is indicative of the difference between the positive power supply voltage (V_{SUPPLY}) and the video drive signal (V_6)

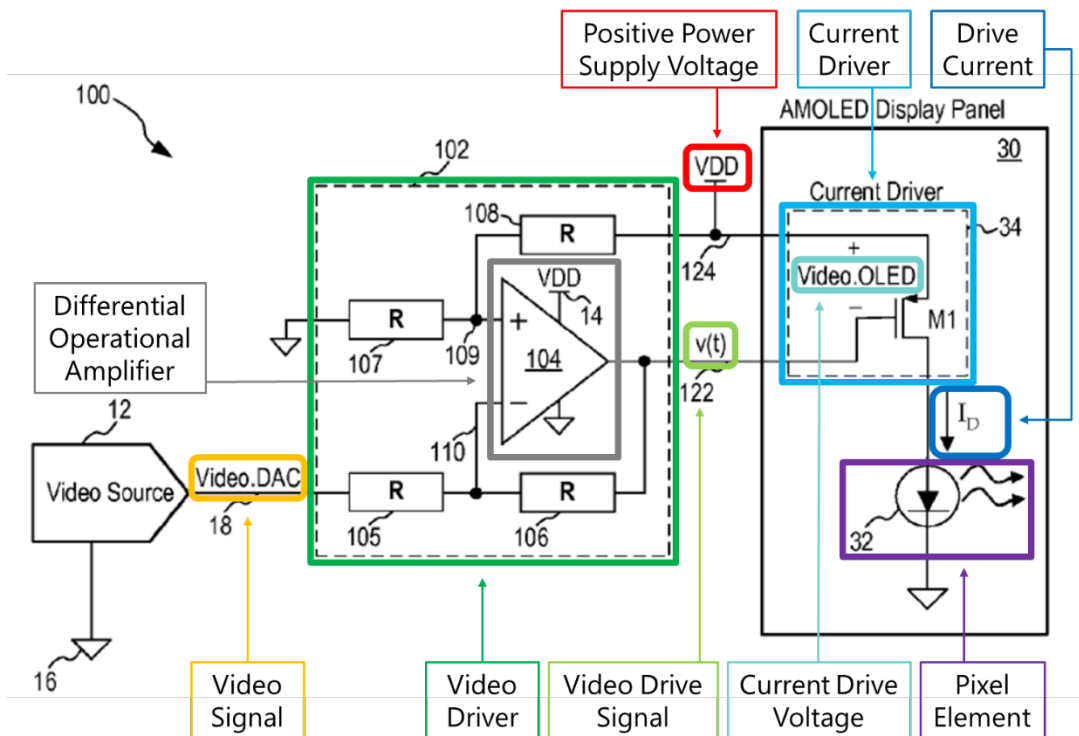
$$V_{GS} = V_6 - V_{SUPPLY}$$

305. Therefore Steer discloses that the video drive signal (gate voltage V_6) is indicative of the sum of or the difference between the positive power supply voltage (drive voltage V_{SUPPLY}) and the video signal (voltage on the input line **52** ($input(t)$)) and the current drive voltage (gate-to-source voltage= V_{GS}) is indicative of the difference between the positive power supply voltage (drive voltage V_{SUPPLY}) and the video drive signal (gate voltage supplied on line **6** V_6) .

c) Claim 3

[3]: The AMOLED display system of claim 2, wherein the video driver comprises a differential instrumentation amplifier circuit for providing the video drive signal being the difference between the positive power supply voltage and the video signal.

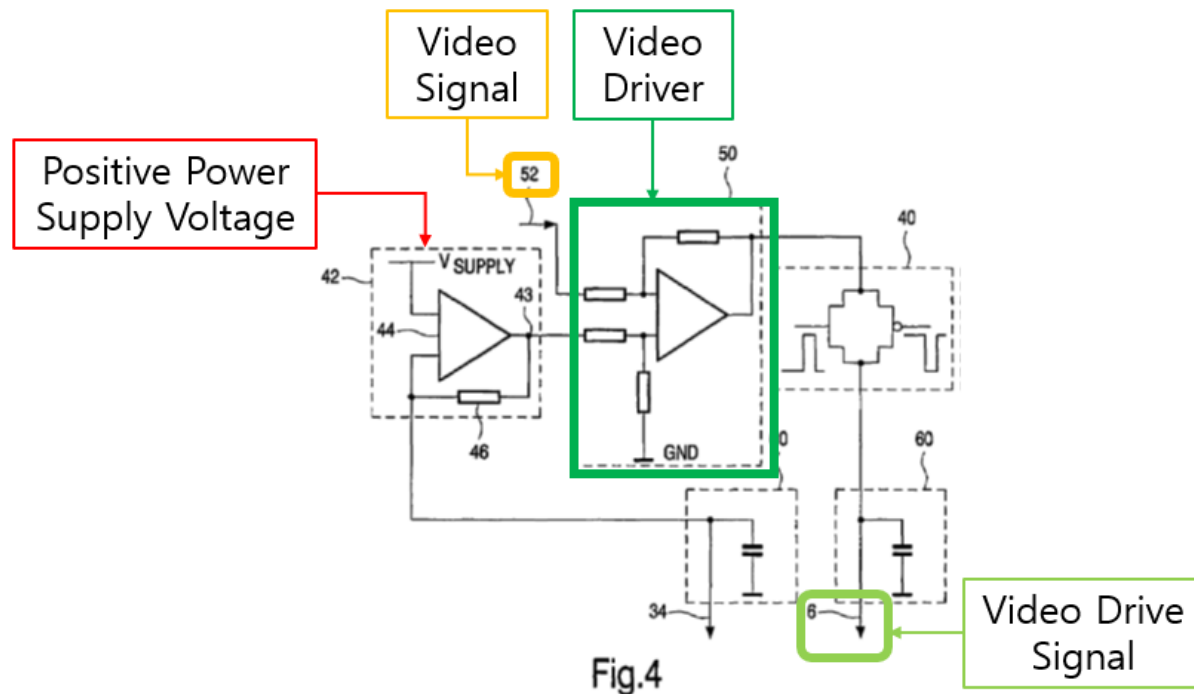
306. The figure below is an annotated reproduction of FIG. 2 of the '521 Patent illustrating the first embodiment.



See Ex. [1001], the '521 Patent at FIG. 2 (annotated).

307. As discussed above a POSA would have recognized that Steer discloses a video driver (circuitry in green annotation below for Video Driver) receiving the video signal (a voltage on input line **52**) and generating a video drive signal (gate

voltage V_6) indicative of the video signal and referenced to a positive power supply voltage (supply voltage V_{SUPPLY}) of the AMOLED display panel.



See Ex. [1008], the '521 Patent at FIG. 4 (annotated).

308. Steer discloses that the comparator section 50 compares the voltage at node 43 with input node 52 which represents the desired current. See Ex. [1008], Steer at 9:23-24. The placement of the resistors of comparator 50 are that of a differential amplifier (see Ex. [1010], Horowitz at pg. 185) and that the input line 52 is coupled to the negative terminal of the operational amplifier via a resistor and that node 43 that is a function of V_{SUPPLY} is coupled to a positive terminal of the

operational amplifier and therefore the output on line **6** (V_6) is the difference between the V_{SUPPLY} and the voltage on input line **52** ($\text{input}(t)$).

309. Steer teaches that the drive voltage on line **6** (V_6) (i.e., the claimed video drive signal) is the difference between the voltage at node **43** (V_{43}) and the voltage on input line **52** ($\text{input}(t)$) (i.e., the claimed video signal). Further, a POSA would have understood that V_{43} as discussed with reference to Limitations [1-A] and [1-C] is equal to $V_{\text{SUPPLY}} + R * I$. Consequently, a (V_6) (i.e., the claimed video drive signal) is indicative of the difference between positive power supply voltage and the video signal, as claimed.

$$V_6 = V_{43} - \text{input}(t)$$

$$V_{43} = V_{\text{supply}} + R * I$$

$$V_6 = V_{\text{supply}} + R * I - \text{input}(t)$$

310. Moreover, as discussed with reference the Limitation [1-C], the claimed current drive voltage is the gate-to-source voltage over the drive transistor **22** (V_{GS}). As also discussed, V_{GS} is equal to the difference between the gate voltage applied via line **6** (V_6) and the voltage on line **26** (V_{SUPPLY}). Consequentially, a POSA would have understood that the current drive voltage (V_{GS}) is indicative of the difference between the positive power supply voltage (V_{SUPPLY}) and the video drive signal (V_6)

$$V_{GS} = V_6 - V_{SUPPLY}$$

311. Therefore Steer discloses that the video drive signal (gate voltage V_6) is indicative of the sum of or the difference between the positive power supply voltage (drive voltage V_{SUPPLY}) and the video signal (voltage on the input line **52** (input(t)) and the current drive voltage (gate-to-source voltage= V_{GS}) is indicative of the difference between the positive power supply voltage (drive voltage V_{SUPPLY}) and the video drive signal (gate voltage supplied on line **6** V_6) .

312. Steer further discloses that “[a]fter the pixel programming mode, the transmission gate **40** is turned off, and the row conductor **4** is operated to turn off the address transistor **16** and the transistor **32** but to turn on the transistor **30**.” *See* Ex. [1008], Steer at 10:5-7.

313. Steer is silent on the value of the resistors in the differential circuit of the video driver. A POSA would have been motivated to make the obvious design choice of using the same value of resistors in the differential circuit making the amplifier unity-gain for the following reasons: (1) it is a conceptually simpler design less sensitive to resistor tolerances; (2) a unity-gain differential amplifier can be implemented in a single integrated-circuit with embedded resistor leading to a simpler implementation; and (3) this simple implementation can reduce costs.

314. A POSA would have been further motivated to make this obvious modification because it is a mere design choice that would also accomplish the stated purpose of *Steer*. Indeed, *Steer* does not disclose that a non-unity gain would be desired or necessary.

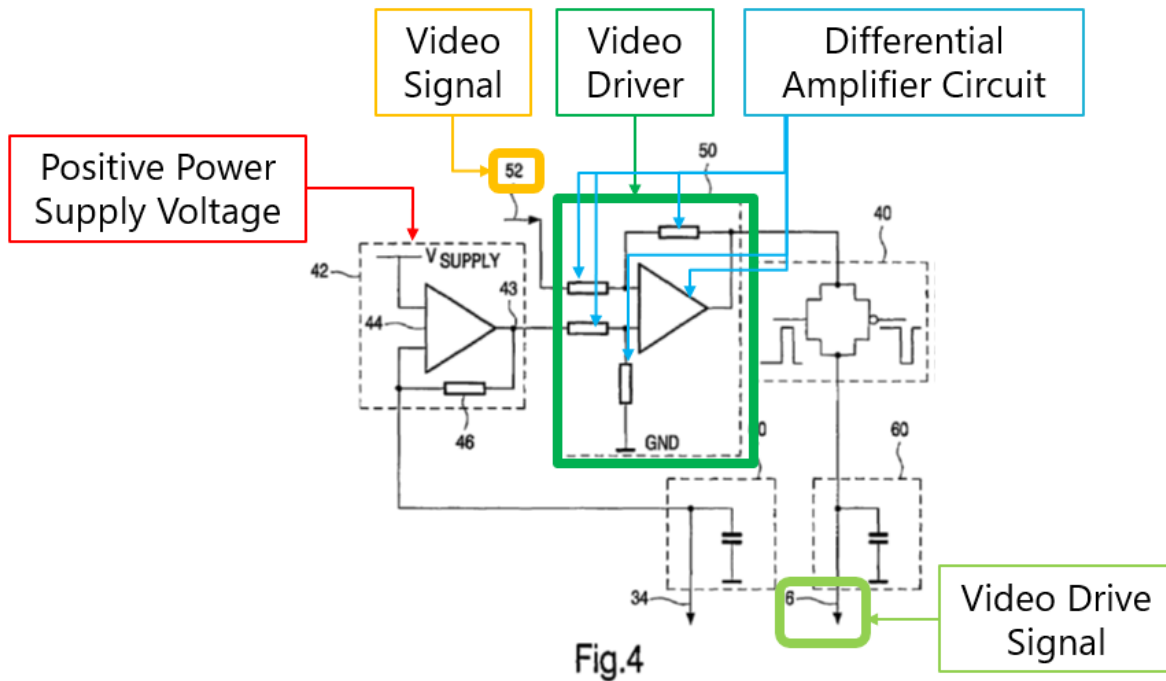
315. Accordingly, a POSA would have recognized that *Steer* discloses a condition of the video drive signal (V_6) being the difference between the positive power supply voltage and the video signal. In a first example, V_6 (the claimed video drive signal) will be exactly the difference between V_{SUPPLY} (the claimed positive power supply voltage) and the input(t) (the claimed video signal) when the current (I) through resistor **46** (R) is zero. This will initially occur when the programming phase of the pixel begins.

316. For example, at least at the moment at which the programming phase begins, the voltage at node **43** will be equal to V_{SUPPLY} because there is no current flowing through resistor **46** (R). There is no current flowing through resistor **46** (R) at this time because the current has not yet started to flow through the pixel element **2**.

317. Moreover, in some circumstances, a first programming phase will charge the capacitor **24** to a first voltage of V_{GS} for a particular first current (e.g., set by the voltage on the input line **52** input(t)). That is, the first current will correspond

to a first magnitude of V_{GS} . The programming phase ends and the top terminal of capacitor **24** is held at V_{SUPPLY} supplied via line **26** and the first magnitude of V_{GS} is held at a constant voltage. *See* Ex. [1008], Steer at 2:1-2 (“[a] storage capacitor **24** holds the voltage on the gate of the drive transistor **22** after the pixel addressing (programming) phase.”) When a second programming phase begins that requires a second magnitude of V_{GS} that is smaller than the first magnitude, the capacitor **24** will discharge from the first magnitude voltage to the second magnitude thereby supplying current to the pixel element **2** for some period of time. During the discharge, the current through resistor **46** (R) will be zero and the voltage at node **43** will be exactly V_{SUPPLY} . Accordingly, it will not be until the capacitor **24** sufficiently discharges that a current (I) will flow through **46** (R).

318. Therefore, as shown in annotated FIG. 4 below, a POSA would have recognized that Steer discloses wherein the video driver (comparator section **50**) comprises a differential instrumentation amplifier circuit (operation amplifier and resistors in differential arrangement annotated in light blue) for providing the video drive signal being the difference between the positive power supply voltage (node **43**) and the video signal (input voltage on input **52**).

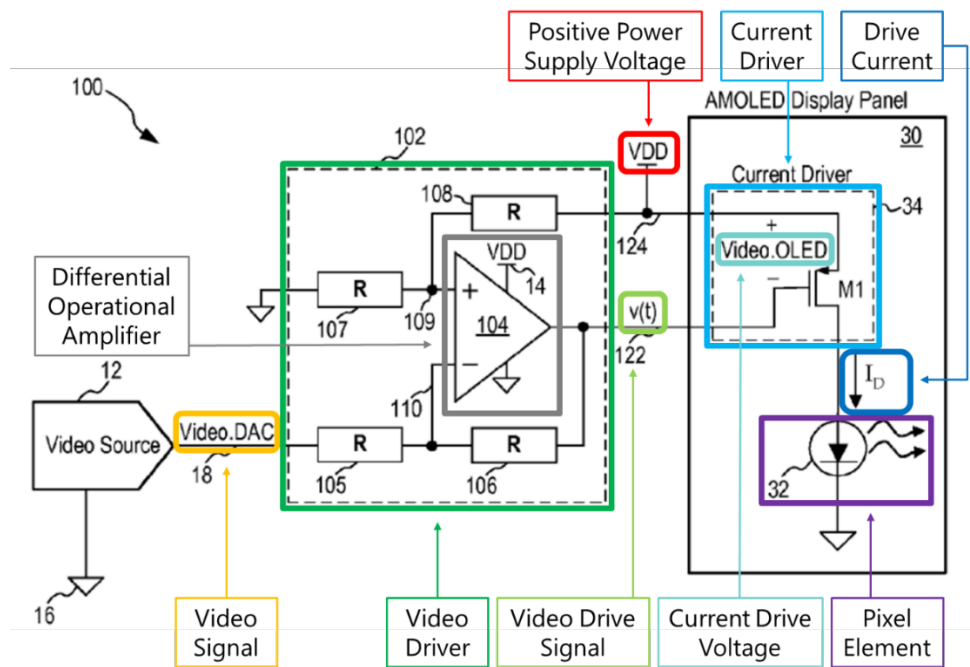


See Ex. [1008], Steer at FIG. 4(annotated).

d) Claim 4

[4-Pre]: The AMOLED display system of claim 3, wherein the video driver comprises:

319. The figure below is an annotated reproduction of FIG. 2 of the '521 Patent illustrating the first embodiment.



See Ex. [1001], the '521 Patent at FIG. 2 (annotated).

[4-A]: an operational amplifier having a positive input terminal coupled to a first resistor, a negative input terminal coupled to a second resistor and an output terminal providing the video drive signal;

320. In the '521 Patent, the operational amplifier corresponds to element 104 in FIG. 2.

321. As discussed above a POSA would have understood that amplifier and resistors of the comparator **50** are in a differential arrangement and be motivated to make the obvious design choice of having the input line **52** coupled to the negative terminal of the operational amplifier via a (second) resistor because it was well known that in conventional differential instrumentation amplifier circuits, the

positive input terminal is the reference voltage against which the negative terminal voltage is compared to. *See also* Ex. [1010], Horowitz Text at pg. 181.

322. Furthermore, according to Steer, the current-to-voltage converter 42 includes a high open loop gain amplifier 44 such that the current-measurement line 34 is connected to the virtual earth input with V_{SUPPLY} connected to the other input of amplifier 44. *See* Ex. [1008], Steer at 9:6-9, (“The current-to-voltage converter section 42 has a high open loop gain amplifier 44 so that the current-measurement supply line, connected to the virtual earth amplifier input, is held at the voltage V_{SUPPLY} on the other input of the amplifier 44.”).

323. The output of this amplifier 44 is connected to the input of the amplifier 50. *See* Ex. [1008], Steer at 5:57-59, (“A comparator section 50 compares the voltage at node 43 with an input Voltage at input 52 representing the desired current.”).

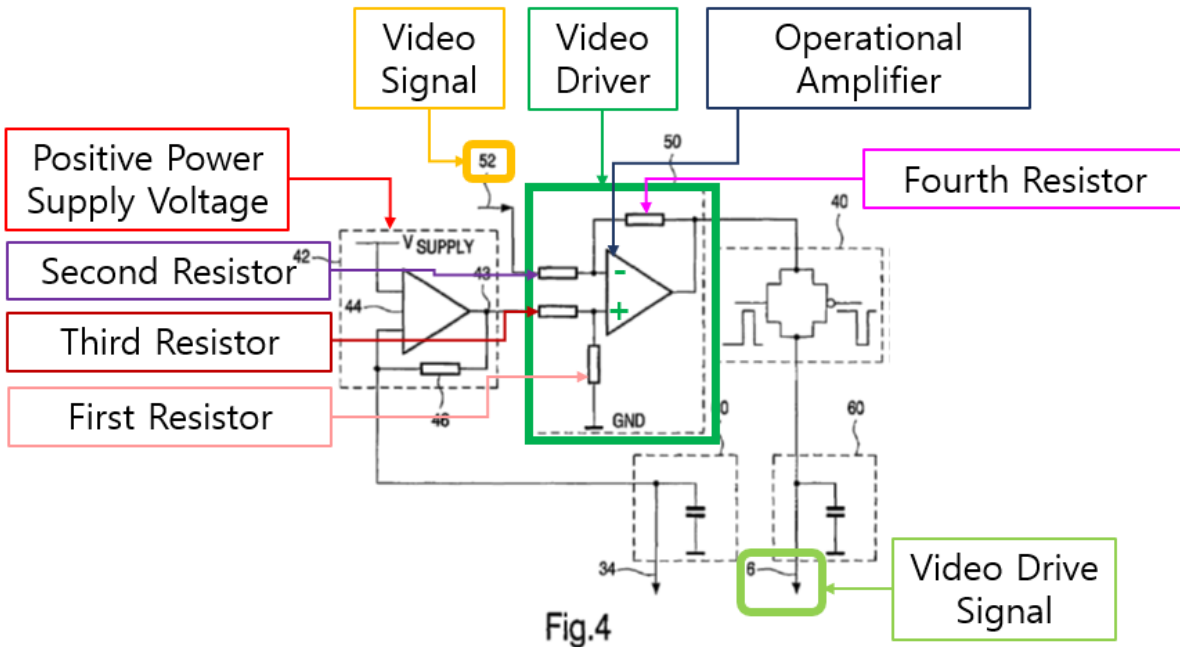
324. In order for the output of the amplifier 50 to output a correct polarity to bias the drive transistor via control line 6, virtual earth must be connected to the non-inverting terminal of the op amp.

325. Furthermore the conventional differential amplifier is typically configured with negative feedback meaning that the feedback resistor is connected to the inverting terminal of the op amp. *See* Ex. [1010], Horowitz at pg. 185.

326. Thus, a POSA would have understood that a first resistor would be connected to the positive terminal. Moreover, a POSA would understand that node **43** that is a function of V_{SUPPLY} is coupled to a positive terminal of the operational amplifier and therefore the output on line **6** (V_6) is the difference between the V_{SUPPLY} and the voltage on input line **52** (input(t)). Also, there are particular circumstances where node 43 is exactly V_{SUPPLY} .

327. Therefore, as shown in annotated FIG. 4 below, a POSA would have understood that Steer discloses or renders obvious an operational amplifier (annotated in dark blue) having a positive input terminal coupled to a first resistor (annotated in light pink), a negative input terminal coupled to a second resistor (annotated in purple) and an output terminal providing the video drive signal (annotated in lime green as the video drive signal on conductor line **6**).

positive input terminal of the operational amplifier (annotated in blue) and a ground voltage (“GND” in FIG. 4) or a negative power supply voltage.



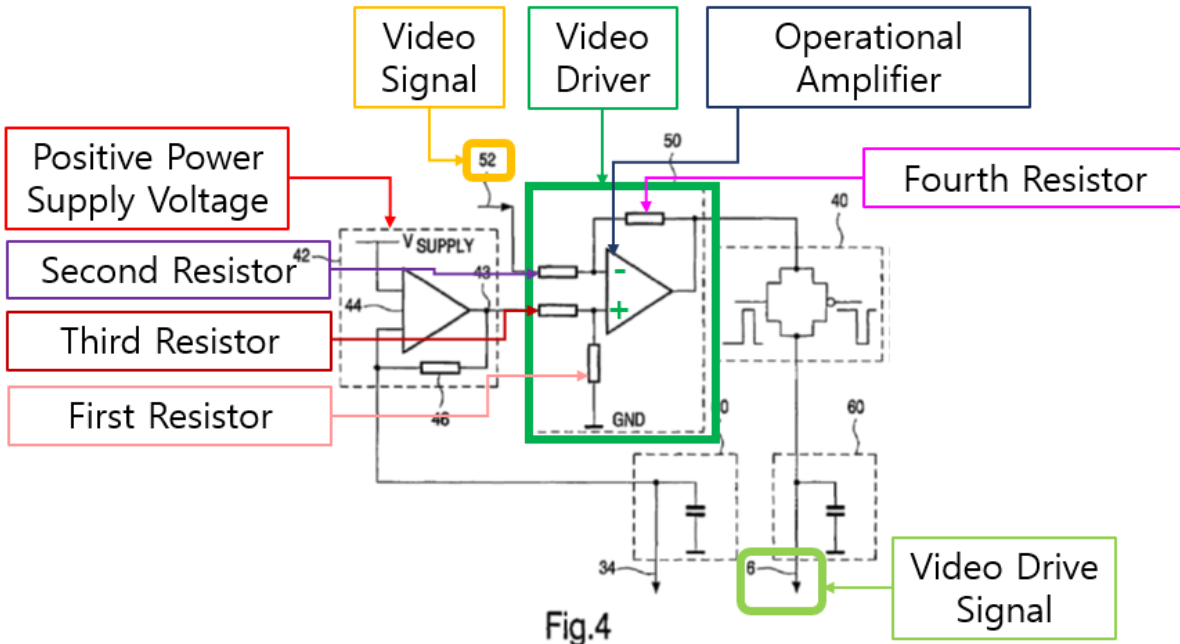
See Ex. [1008], Steer at FIG. 4(annotated).

[4-C]: the second resistor being coupled between the video signal and the negative input terminal of the operational amplifier;

330. In the '521 Patent, the second resistor corresponds to element 105 in FIG. 2.

331. For the same reasons as discussed at Claim 3 and as shown in annotated FIG. 4 below, a POSA would have understood that Steer discloses or renders

obvious the second resistor (annotated in purple) being coupled between the video signal (annotated in orange) and the negative input terminal of the operational amplifier (annotated in blue).



See Ex. [1008], Steer at FIG. 4 (annotated).

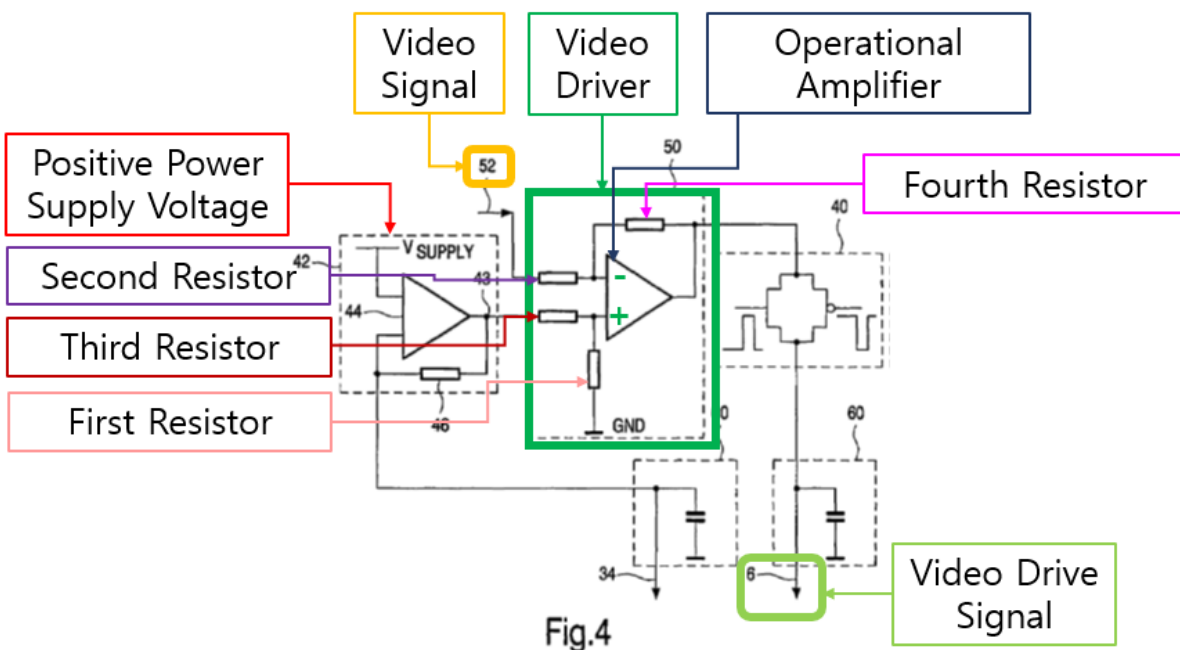
[4-D]: a third resistor being coupled between the positive input terminal of the operational amplifier and the positive power supply voltage; and

332. In the '521 Patent, the third resistor corresponds to element 108 in FIG.

2.

333. As discussed at Limitation [1-A], node **43** is the PPS voltage offset by a value of R multiplied by I . R is the resistor labeled 46. *See Ex.[1008]*, Steer at 5:51-**54**. Also as discussed at Claim 3 there are circumstances where node **43** is exactly V_{SUPPLY} . Thus, a POSA would have understood the voltage at node **43** to be the PPS voltage at least during the described conditions.

334. For the same reasons as discussed at Claim 3 and as shown in annotated FIG. 4 below, a POSA would have understood that Steer discloses a third resistor (annotated in dark red) being coupled between the positive input terminal of the operational amplifier (annotated in blue) and the positive power supply voltage (node **43** that is V_{SUPPLY} when the current through resistor **46** (R) is zero).

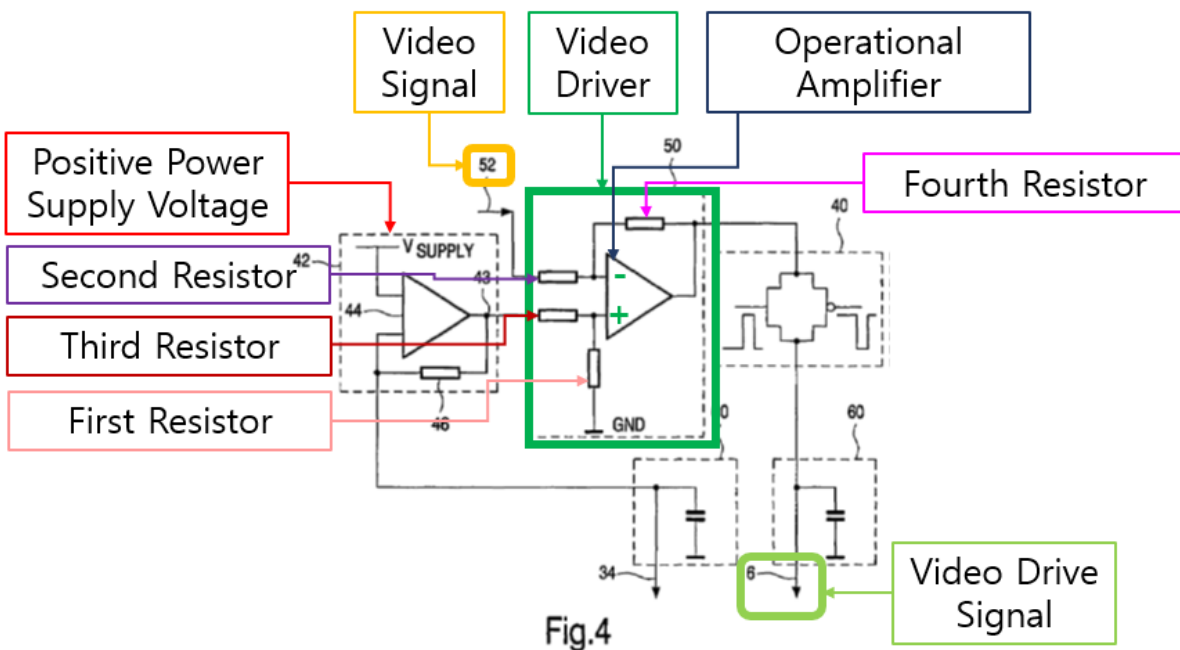


See Ex. [1008], Steer at FIG. 4 (annotated).

[4-E]: a fourth resistor being coupled between the negative input terminal and the output terminal of the operational amplifier.

335. In the '521 Patent, the fourth resistor corresponds to element 106 in FIG. 2.

336. For the same reasons as discussed at Claim 3 and as shown in annotated FIG. 4 below, a POSA would have understood that Steer discloses a fourth resistor (annotated in bright pink) being coupled between the negative input terminal and the output terminal of the operational amplifier (annotated in blue).



See Ex. [1008], Steer at FIG. 4 (annotated).

XIII. SECONDARY CONSIDERATIONS

337. During prosecution of the Challenged Patent, the applicants did not discuss any secondary considerations of non-obviousness, and I am not aware of any secondary considerations that would support non-obviousness. Should the Patent Owner put forth any alleged evidence of secondary considerations in connection with the Challenged Patent, I reserve the right to consider such evidence, to consider whether any such evidence has a nexus to any claims of the Challenged Patent, and to update my analysis.

XIV. CONCLUSION

338. All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. I further understand that willful false statements and the like are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code. I declare under penalty of perjury that the foregoing is true and correct.

Executed on March 24, 2023.



Alex Z. Kattamis, Ph.D., P.E.