IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG DISPLAY CO., LTD; SAMSUNG ELECTRONICS CO., LTD.; and SAMSUNG ELECTRONICS AMERICA, INC.
Petitioners
v.

POLARIS POWERLED TECHNOLOGIES, LLC
Patent Owner

_____

U.S. Patent No. 7,259,521

_____

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,259,521

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EXHIBIT LIST

Exhibit No.[1]	Description
1001	U.S. Patent No. 7,259,521 ("the '521 Patent")
1002	Expert Declaration of Dr. Alex Kattamis
1003	CV of Dr. Alex Kattamis
1004	Prosecution File History of the '521 Patent
1005	Complaint in *Polaris PowerLED Technologies, LLC v. Samsung Electronics America, Inc.*, Case No. 2:22-cv-00469 (E.D. Tex.)
1006	U.S. Patent Publication No. 2005/0190128 ("Hayafuji")
1007	U.S. Patent Publication No. 2005/0140600 ("Kim")
1008	International Publication No. WO2004034365A1 ("Steer")
1009	James W. Nilsson, et al., *Electric Circuits* (5th ed. 1996)
1010	Paul Horowitz, et al., *The Art of Electronics* (2nd ed. 1989)
1011	Willem Den Boer, *Active Matrix Liquid Crystal Displays – Fundamentals and Applications* (1st ed. 2005)
1012	Min-Koo Han, *AM backplane for AMOLED*, PROC. OF ASID (2006)

[1] Citations to patents are made by column and line cite; citations to U.S. patent publications are made by paragraph number; citations to International patent applications are made by page number; citations to other exhibits are made with reference to the Bates-stamped pagination.

I. 37 C.F.R. §42.8–MANDATORY NOTICES

A. 37 C.F.R. §42.8(b)(1)–Real Party-in-Interest

Samsung Display Co., Ltd.; Samsung Electronics Co., Ltd.; and Samsung Electronics America, Inc. are the Petitioners. No other parties exercised or could have exercised control over this Petition and no other parties funded or directed this Petition.

B. 37 C.F.R. §42.8(b)(2)–Related Matters

Polaris PowerLED Technologies, LLC has asserted the '512 Patent in the following civil action:

- *Polaris PowerLED Technologies, LLC v. Samsung Electronics America, Inc.*, Case No. 2:22-cv-00469 (E.D. Tex.), filed December 12, 2022 (the "District Court Litigation"). *See* Ex.[1005], (Complaint).

C. 37 C.F.R. §42.8(b)(3)–Lead and Back-Up Counsel

Petitioners provide the following designation of counsel.

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D. 37 C.F.R. §42.8(b)(4)–Service Information

A copy of this entire Petition, including all Exhibits and a Power of Attorney, is being served by FEDERAL EXPRESS, costs prepaid, to the address of the attorney or agent of record for Patent Owner at the USPTO for the '521 Patent:

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A Power of Attorney is filed concurrently herewith under 37 C.F.R. §42.10(b).

II. CLAIM LISTING

Claim 1

[1-Pre]	An active matrix organic light emitting diode (AMOLED) display system comprising an AMOLED display panel receiving a video signal to be displayed on the AMOLED display panel, the AMOLED display panel comprising a plurality of organic light emitting diode (OLED) pixel elements, the AMOLED display system comprising:
[1-A]	a video driver receiving the video signal and generating a video drive signal indicative of the video signal and referenced to a positive power supply voltage of the AMOLED display panel; and
[1-B]	a current driver coupled to at least one OLED pixel element, the current driver receiving the video drive signal and the positive power supply voltage and providing a drive current to the at least one OLED pixel element,
[1-C]	the drive current being proportional to a current drive voltage being indicative of the video signal and independent of the positive power supply voltage.

Claim 2

[2]	The AMOLED display system of claim 1, wherein the video drive signal is indicative of the sum of or the difference between the positive power supply voltage and the video signal and the current drive voltage is indicative of the difference between the positive power supply voltage and the video drive signal.

Claim 3

[3]	The AMOLED display system of claim 2, wherein the video driver comprises a differential instrumentation amplifier circuit for providing the video drive signal being the difference between the positive power supply voltage and the video signal.

Claim 4

[4-pre]	4. The AMOLED display system of claim 3, wherein the video driver comprises:
[4-A]	an operational amplifier having a positive input terminal coupled to a first resistor, a negative input terminal coupled to a second resistor and an output terminal providing the video drive signal;
[4-B]	the first resistor being coupled between the positive input terminal of the operational amplifier and a ground voltage or a negative power supply voltage;
[4-C]	the second resistor being coupled between the video signal and the negative input terminal of the operational amplifier;
[4-D]	a third resistor being coupled between the positive input terminal of the operational amplifier and the positive power supply voltage; and
[4-E]	a fourth resistor being coupled between the negative input terminal and the output terminal of the operational amplifier.

Claim 5

[5]	The AMOLED display system of claim 2, wherein the video driver comprises a current mode isolator circuit for providing the video drive signal being the difference between the positive power supply voltage and the video signal.

Claim 7

[7]	The AMOLED display system of claim 2, wherein the video driver comprises a video clamp circuit for providing the video drive signal being the sum of the positive power supply voltage and the video signal.

III. PETITION CONTENT

A. Standing

Petitioners certify that the '521 Patent is eligible for *inter partes* review and that Petitioners meet the eligibility requirements of 37 C.F.R. § 42.104.

B. Relief Requested

Petitioners request invalidation of Claims 1-5 and 7 (collectively, "Challenged Claims") of U.S. Patent No. 7,259,521 ("the '521 Patent"), assigned to Polaris PowerLED Technologies, LLC. ("Patent Owner" or "PO").

C. Priority Date

The '512 Patent was filed on August 28, 2006. Ex.[1001], Cover. The '512 Patent does not claim any earlier priority date.

D. Invalidity Grounds[2]

Ground	Claims	Basis for Challenge
1, 2	1, 2, 7	§102–Anticipated or obvious in view of by *Kim* and the knowledge of a POSA
3	1, 2	§102–Anticipated by *Hayafuji*
4	1-3, 5	§103–Obvious in view of *Hayafuji* and the knowledge of a POSA
5	1-4	§103–Obvious in view of *Steer* and the knowledge of a POSA

[2] *See* §VIII.

IV. DISCRETIONARY DENIAL IS NOT APPROPRIATE

The factors identified in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (March 20, 2020), do not provide a basis for denying institution.

The **first *Fintiv* factor** is neutral here. Samsung has not yet moved to stay the district court proceedings pending IPR, and the PTAB will not infer how the district court would rule should a stay be requested. *Hulu LLC v. SITO Mobile R&D IP, LLC et al*., IPR2021-00298, Paper 11 at 10-11 (PTAB May 19, 2021).

For the **second *Fintiv* factor**, the district court has not set a trial date in the litigation. Speculating based on prior practice in Judge Gilstrap's Court, the earliest estimated trial date is approximately October 2024. Even if trial proceeds in October 2024, the above timing does not tip in favor of denying the petition in this case. *Apple Inc. v. Koss Corp*., IPR2021-00305, Paper 14 at 13 (PTAB June 3, 2021). This Petition is filed in March 2023. An institution decision should be issued in September 2023, with a final written decision (FWD) in September 2024. Thus, the ***earliest*** estimated trial date would be after the FWD. PTAB cases analyzing similar schedules have weighed the second factor as neutral or only slightly in favor of denial. *Google LLC et al. v. Parus Holdings, Inc*., IPR2020-00847, Paper 9 at 12 (PTAB Oct. 21, 2020) (trial scheduled three months before FWD weighs "at best, neutral").

Using the median time to trial for civil actions in E.D. Tex. (~24.5 months) to estimate the trial date, (*See* USPTO Memorandum RE Discretionary Denials, June 21, 2022), trial is not expected to occur until December 2024, several months *after* a FWD will issue.

The **third *Fintiv* factor** weighs strongly against denial. Samsung has not yet answered Polaris's Complaint. No hearing has been set and no substantive activity has occurred in the case. The Case Management Conference is expected to be set no earlier than April 2024. Because the investment in the parallel proceeding by the court has been minimal and Petitioners acted diligently, this factor weighs strongly against discretionary denial. *Hulu*, Paper 11 at 13.

The **fourth *Fintiv* factor** also weighs against denial. Because the median time to trial for civil actions in E.D. Tex. suggests that trial will not occur until at least a month after a FWD is issued, "there is a reasonable likelihood that the Board will address the overlapping validity issues prior to the district court reaching them at trial..., thereby providing the possibility of simplifying issues for trial." *Juniper Networks, Inc. v. Packet Intelligence LLC*, IPR2020-0039, Paper 21 at 18 (PTAB Sept. 10, 2020); *MED-EL Elektromedizinische Geraete GmbH v. Sonova* AG, IPR2020-00176, Paper 13 at 15 (PTAB June 3, 2020).

Moreover, Petitioners are challenging more claims than what is likely to be asserted in the district court litigation. PO's Complaint identifies only independent

Claim 1. Ex.[1005], ¶39. In the district court, PO will likely assert a subset of claims, while this Petition challenges Claims 1-5 and 7. This IPR proceeding is thus likely the only venue in which these invalidity challenges will be adjudicated against several claims in the '521 Patent, which promotes system efficiency and benefits the public in that more claims will be addressed here and will resolve disputes against future district court defendants. *Vudu, Inc. v. Ideahub, Inc.,* IPR2020-01688, Paper 16 at 14-15 (PTAB Apr. 19, 2021) ("differences in asserted claims" and claims challenged in the petition weighs against denial).

On the **fifth *Fintiv* factor**, the Board should give little weight to the fact that Petitioners and PO are the same parties as in district court. *Weatherford U.S., L.P., v. Enventure Global Tech., Inc*., Paper 16 at 11-13 (Apr. 14, 2021).

"Other circumstances" under the **sixth *Fintiv* factor** further weigh against discretionary denial. The merits of the Petition are compelling. Here, there are three references that anticipate or render obvious independent Claim 1 and the three references (each directed toward one of the three embodiments of the '521 Patent) render obvious nearly all of the '521 Patent claims. All elements recite nothing more than predictable approaches applying a drive current to a pixel that is immune from supply voltage variations as explained by the prior art and are well within a POSITA's skill and knowledge. *Align Tech., Inc. v. 3Shape A/S*, IPR2020-01087, Paper 15 at 42-43 (PTAB Jan 20, 2021).

Taken together, the *Fintiv* factors strongly weigh against denial.

V. '521 PATENT OVERVIEW

A. Prosecution History

The '521 Patent was filed August 28, 2006, issued August 21, 2007, and had a short prosecution history with no rejections. Ex.[1002], ¶34. Ex.[1004]. None of the references relied upon herein were raised during prosecution.

B. Specification

The '521 Patent's alleged invention relates to an AMOLED display system having a video driver and a pixel element. Ex.[1001], Abstract. The video driver may be either external or integrated with the display. Ex.[1001], 7:52-8:2. Figure 1 depicts a diagram of a conventional AMOLED system. Ex.[1001], 3:36-37, Fig. 1.

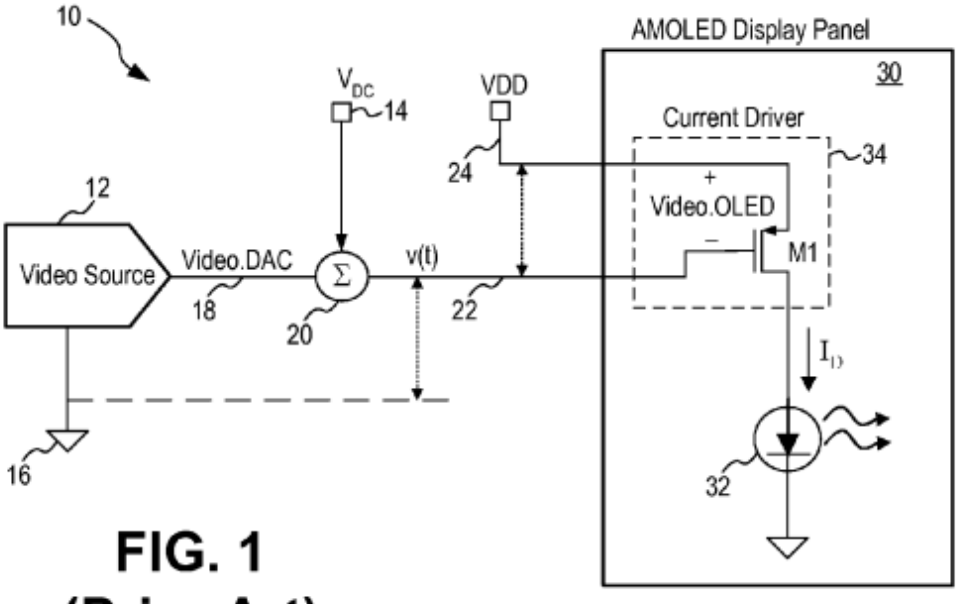


FIG. 1
(Prior Art)

Ex.[1001], Fig. 1.

Video source 12 provides video signals (Video.DAC) to AMOLED display panel 30. Ex.[1001], 1:57-59. "[V]ideo drive signal v(t) is a signal that is referenced to the ground voltage (node 16)." Ex.[1001], 2:2-3.

The purported invention references incoming video signals to the same positive power supply ("PPS") voltage as the display panel, instead of the ground voltage, to generate a video drive signal ("VDS") driving a current driver that provides current to the pixel element. Ex.[1001], Abstract, Fig. 2.

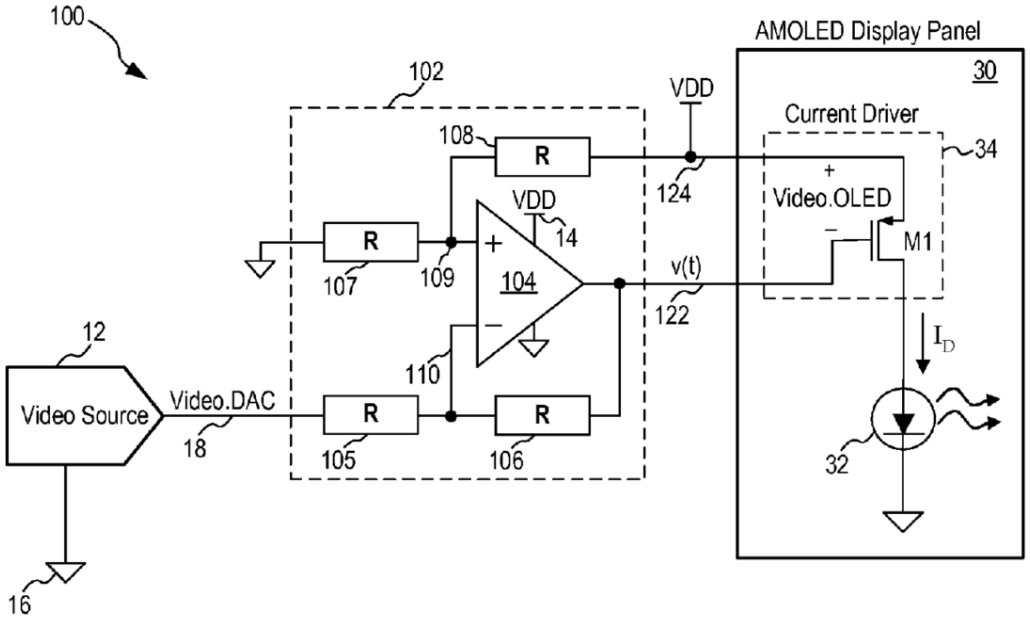


FIG. 2

Ex.[1001], Fig. 2.

The '521 Patent purportedly provides a system "immune to power supply voltage variations and provides display images that are free from undesired flickers and brightness variations." Ex.[1001], 3:65-69.

However, video drivers referencing VDS to PPS voltage to eliminate or reduce effects of PPS voltage variation in display systems were well-known before the '521 Patent. *See also* Ex.[1002], ¶¶35-43, 50-75 (discussing the '521 Patent's purported invention and explaining related background concepts).

C. Level of Ordinary Skill in the Art

As of August 28, 2006, a person of ordinary skill in the art ("POSA") would have a B.S. in Electrical Engineering or equivalent field, with 3-5 years of academic or industry experience in OLED display engineering or comparable industry. Ex.[1002], ¶¶0044-0045. Additional education could compensate for less practical experience and vice versa. Ex.[1002], ¶¶44-45.

VI. CLAIM CONSTRUCTION

For terms not explicitly construed below, Petitioners interpret them for this proceeding in accordance with their plain and ordinary meaning.[3]

A. "referenced to"

The '521 Patent does not define "***referenced to***," and describes many ways a signal can be "referenced to" a voltage. For example, specification describes at least the following relationships: a direct connection between a component and a voltage

[3] Petitioners do not concede that the terms of the challenged claims are definite under 35 U.S.C. §112.

signal (e.g., 2:20-23, 5:63-65); an indirect connection between multiple voltage signals (e.g., 2:1-14, 3:55-58); a voltage differential's minuend value (e.g., 2:34-37); and a driver functionality (e.g., 4:55-60). Ex.[1001]. A POSA would understand that claim terms should be understood based on the intrinsic record, and would therefore understand the claimed "***referenced to***" requirement to include these possibilities. Ex.[1002], ¶47.

B. "independent of the…power supply voltage"

The claims require a current drive voltage that is independent of the positive power supply voltage. However, a POSA would understand that for any drive current to flow, there must a power supply voltage (e.g. with reference to Figure 2 of the '521 Patent, with no power supply voltage VDD, no current will flow through drive transistor M1). Ex.[1001], Fig. 2; Ex.[1002], ¶48.

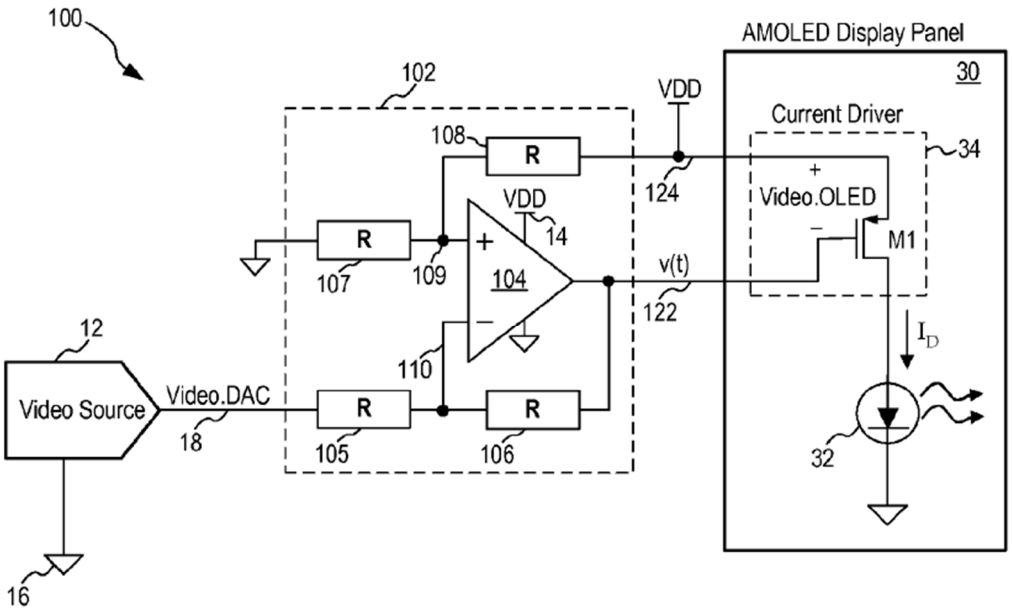


FIG. 2

Ex.[1001], Fig. 2.

Instead, a POSA would understand this term to mean, consistent with the '521 Patent specification, that "noise or DC drifts in the power supply voltage…will not disturb the current drive signal…and will not affect the brightness" of the display; and, similarly, "[v]ariations in the power supply voltage VDD will no longer adversely affect the" display. Ex.[1001], 6:6-7, 5:18-23, 2:63-65; Ex.[1002], ¶49.

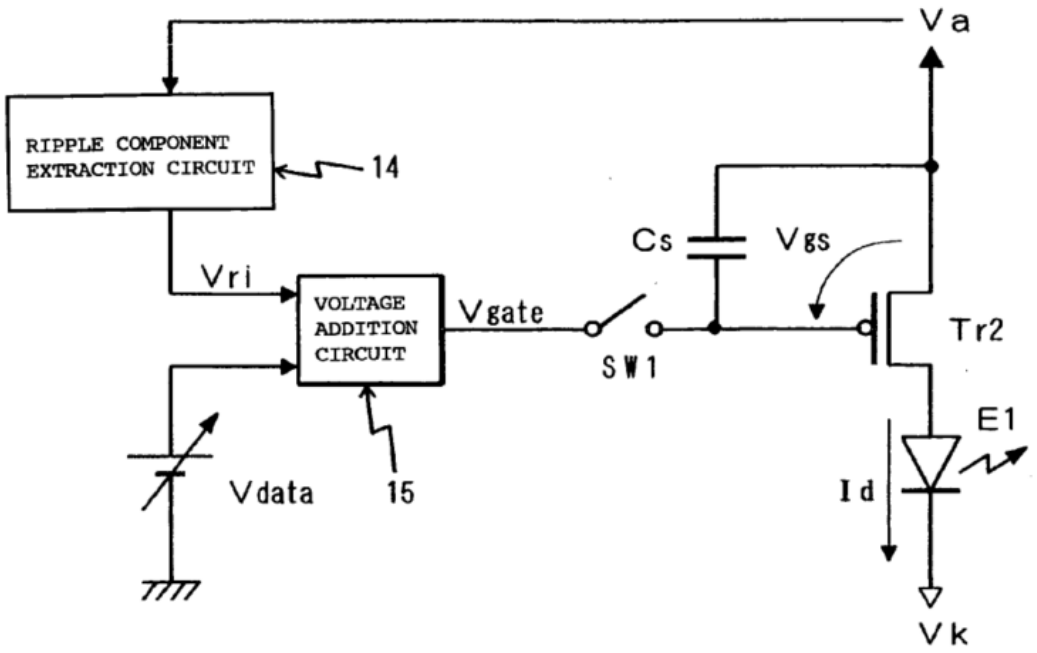
VII. PRIOR ART

The '521 Patent was filed August 28, 2006, without a priority claim, and is subject to the pre-AIA provisions of 35 U.S.C §§102/103.

A. *Hayafuji*–Ex.[1006]

U.S. Patent Publication No. 2005/0190128 ("*Hayafuji*," Ex.[1006]) was filed February 3, 2005, and published September 1, 2005. *Hayafuji* is prior art under at least 35 U.S.C §§102(a) and (e).

Hayafuji is directed to "a drive device of a light emitting display panel." Ex.[1006], ¶0047. *Hayafuji* explains that in conventional implementations, "deterioration of the display quality of an image [is] caused by a ripple component generated in a power supply circuit." Ex.[1006], ¶¶0025-0028. Achieving the same objective as the '521 Patent, *Hayafuji* corrects for this by applying the ripple component $\mathbf{V_{ri}}$ extracted from the supply voltage $\mathbf{V_a}$ to the gate voltage $\mathbf{V_{gate}}$ of light emission drive transistor **Tr2.** The ripple component supplied via $\mathbf{V_{gate}}$ has "approximately the same phase and the same amplitude as those of the ripple component supplied to the source of the light emission drive transistor **Tr2**." Ex.[1006], ¶¶0053-0054, Fig. 6. Ex. [1002], ¶¶77-79.



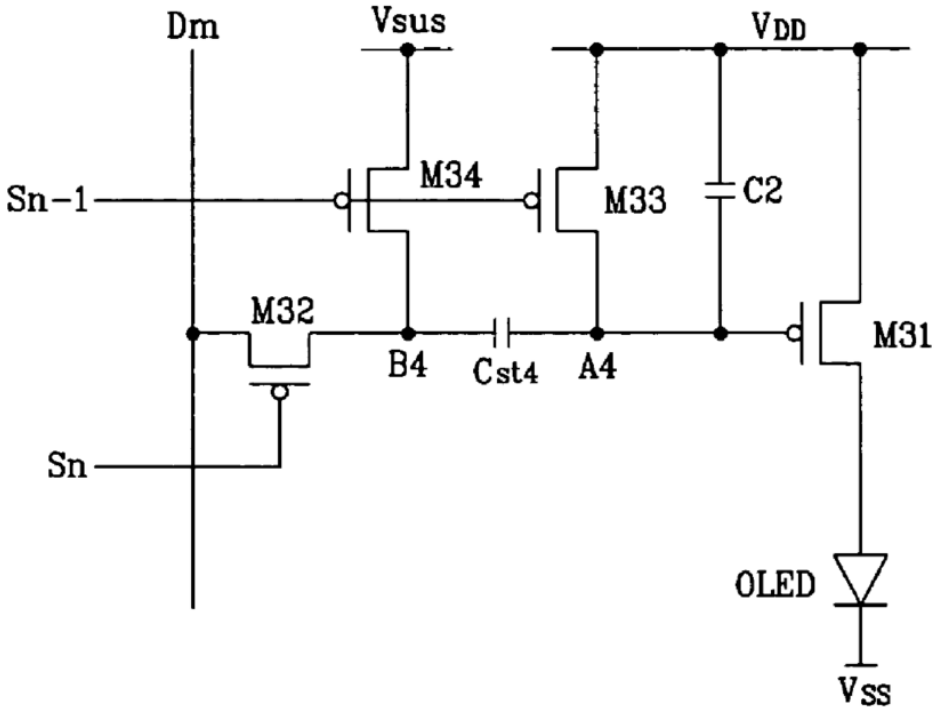
Ex.[1006], Fig. 6.

B. *Kim*–Ex.[1007]

U.S. Patent Publication No. 2005/0140600 ("*Kim*," Ex.[1007]) was filed August 16, 2004, and published June 30, 2005. *Kim* is prior art under at least 35 U.S.C. §102(b).

Kim is directed to a "light emitting display including data lines for transmitting data voltages, scan lines for selecting signals, and pixel circuits." Ex.[1007], Abstract. *Kim* explains that a problem with conventional devices is that "when a voltage drop (IR-drop) is generated on a line for supplying the power supply voltage $\mathbf{V_{DD}}$, and the power supply voltage $\mathbf{V_{DD}}$ applied to a plurality of pixel circuits is not uniform, a desired amount of current may not flow to the OLED, thereby degrading

image qualities." Ex.[1007], ¶0012. *Kim*'s solution is to reference the gate voltage (**A4**) of OLED drive transistor **M31** to power supply voltage $\mathbf{V_{DD}}$. By doing so, *Kim* explains "a current that flows into the OLED of a pixel circuit in a light emitting display is substantially prevented from being influenced by a power supply voltage." Ex.[1007], ¶0014, Fig. 10. Ex.[1002], ¶¶81-85.

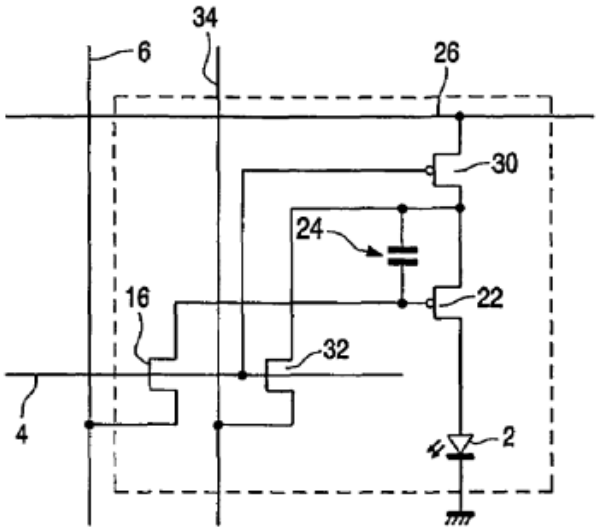


Ex.[1007], Fig. 10.

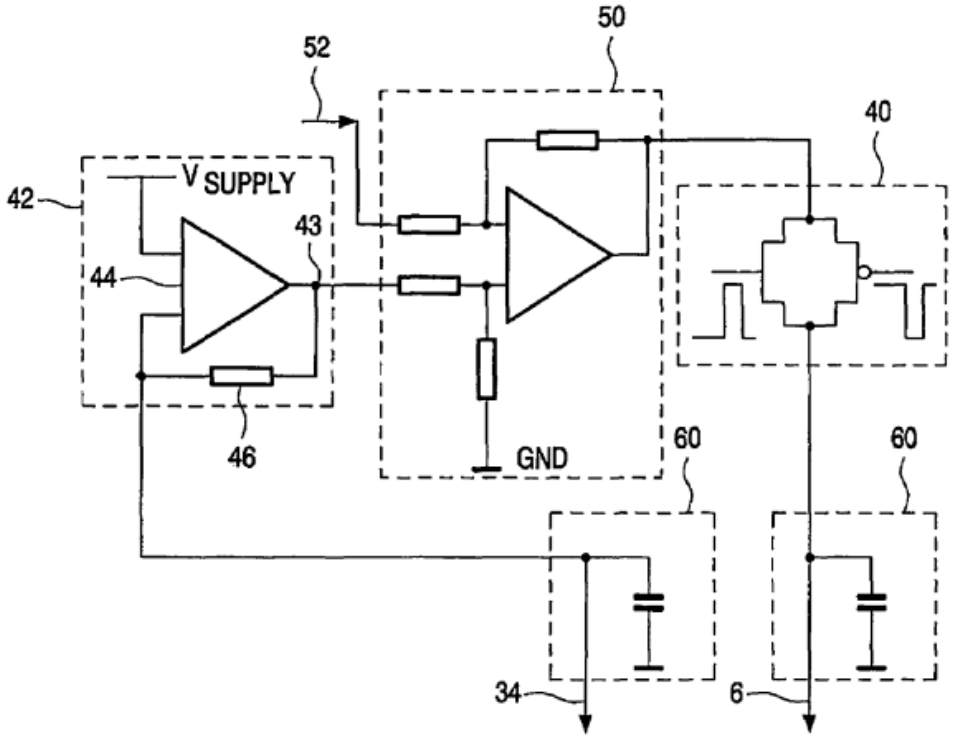
C. *Steer*–Ex.[1008]

PCT application number WO2004034365A1 ("Steer," Ex.[1008]) was filed September 15, 2003, and published April 22, 2004. *Steer* is prior art under at least 35 U.S.C §102(b).

Steer is directed to "[a]n active matrix electroluminescent display device compris[ing] an array of display pixels." Ex.[1008], Abstract, 1:11-12. Like the '521 Patent, *Steer* also identifies the problem that "voltage variations along the power supply line alter the gate-source voltage on the drive transistors, and thereby affect the brightness of the display." Ex.[1008], 4:15-17. *Steer* describes a solution shown below in Figures 3 and 4, where the power supply (**V_{SUPPLY}** and line **26**) is used to generate the current drive voltage, thereby rendering current drive voltage independent of the power supply variation. Ex.[1008], Figs. 3, 4. Ex.[1002], ¶¶87-91.



Ex.[1008], Fig. 3.



Ex.[1008], Fig. 4.

VIII. ASSERTED INVALIDITY GROUNDS

A. Grounds 1 and 2: Claims 1, 2, and 7 are Anticipated or Obvious in View of *Kim*

1. *Claim 1*

Claim[1-Pre]

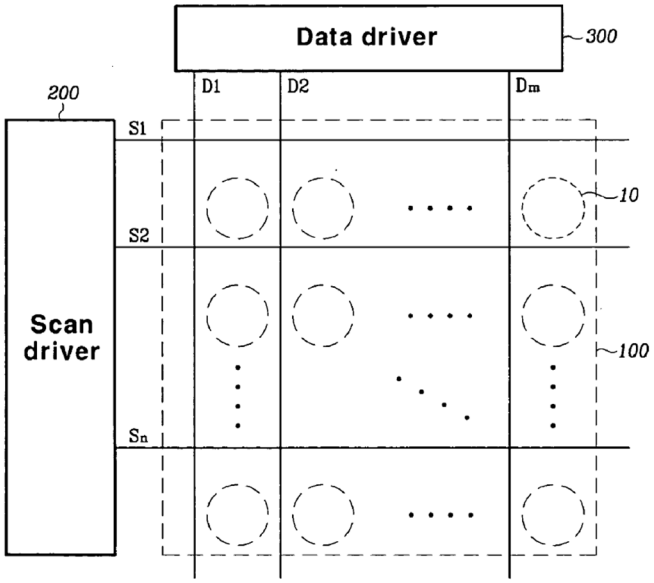
To the extent the preamble is limiting, *Kim* discloses it. Ex.[1002], ¶¶93-106.

Active Matrix Organic Light Emitting Diode Display Panel…Comprising a Plurality of [OLED] pixel elements

Kim discloses "a light emitting **display** and a driving method" for "an organic EL (electroluminescent) display" consisting of multiple pixel circuits "for driving

an organic EL element (**OLED**)" and which can use an "**active matrix**" method. Ex.[1007], ¶¶0005-0007.

Kim teaches "FIG. 3 shows an organic EL display… As shown, the organic EL display includes an organic EL **display panel 100**, a scan driver **200**, and a data driver **300**. The organic EL display panel **100** includes a plurality of data lines $\mathbf{D_1}$ through $\mathbf{D_m}$, each extending in a column direction, a plurality of scan lines $\mathbf{S_1}$ through $\mathbf{S_n}$, each extending in a row direction, and a plurality of pixel circuits **10**." Ex.[1007], ¶¶0044-46, Fig. 3. "The data lines $\mathbf{D_1}$ through $\mathbf{D_m}$ transmit data ***voltages that correspond to video signals*** to the pixel circuits **10**." Ex.[1007], ¶¶0017, 0045-0046.



Ex.[1007], Fig. 3.

Receiving a Video Signal To Be Displayed

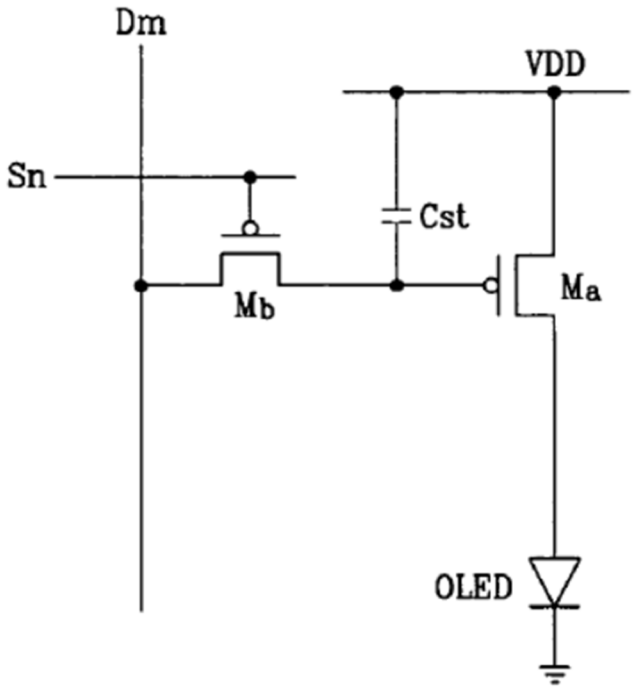
A POSA would recognize, consistent with Figure 3 above, that because "data lines **D_1** through **D_m** transmit data voltages that correspond to video signals to the pixel circuits **10**," and also because, for example in Figure 2 (which doesn't include the additional video driver circuitry disclosed in *Kim*'s later embodiments), "data voltage from the data line **D_m** is applied to the gate of the transistor **Ma**," and thus, "data voltage from the data line **D_m**" corresponds to the relevant portion of the claimed ***video signal to be displayed on the AMOLED display panel***.[4] To the extent not anticipated, a POSA would find it obvious that the Kim system could receive a video signal, and use that signal as the source for the "video signals" explicitly discussed in Kim, as a POSA would understand this is most-logical way of using the Kim system. Ex.[1002], ¶¶93-104.

[4] *Kim's* disclosure sometimes appears to use data line **D_m** and data voltage **V_{DATA}** interchangeably without clarifying that "data voltage **V_{DATA}**" is the signal transmitted along "data line **D_m**". This is particularly apparent given that *Kim*'s figures always use "**D_m**" and not "**V_{DATA}**", whereas *Kim*'s equations always use "**V_{DATA}**" and not "**D_m**". A POSA would recognize, based on *Kim's* disclosure, the "data voltage **V_{DATA}**" transmitted along "data line **D_m**" is the relevant portion of the claimed ***video signal*** destined for the addressed pixel. Ex.[1002], Fn.1.

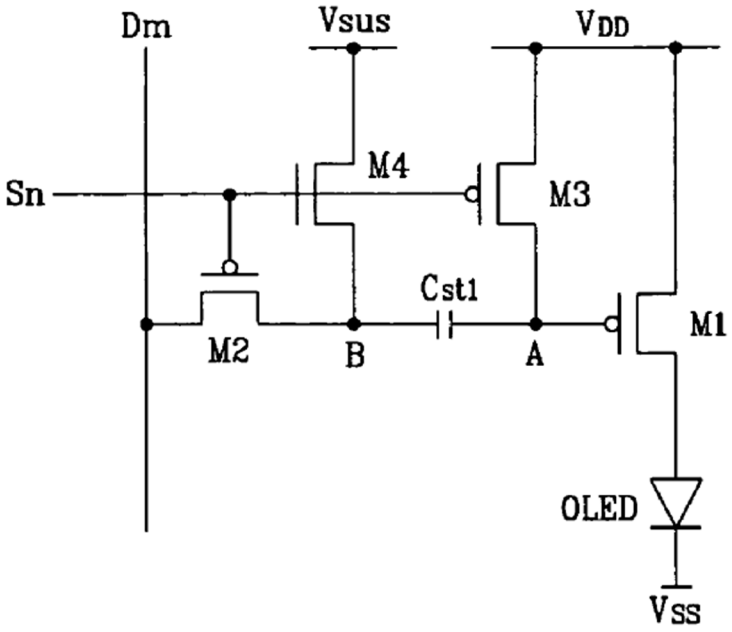
Therefore, a POSA would recognize that *Kim* discloses an ***active matrix organic light emitting diode (AMOLED) display system comprising an AMOLED display panel receiving a video signal to be displayed on the AMOLED display panel, the AMOLED display panel comprising a plurality of organic light emitting diode (OLED) pixel elements, the AMOLED display system comprising***. Ex.[1002], ¶¶93-104.

Although the analysis below is primarily directed to *Kim's* "fourth exemplary embodiment" corresponding to Figure 10, the concepts and discussions regarding Figures 1-6A are generally pertinent to the fourth embodiment in *Kim*. Ex.[1002], ¶¶105-106. *Kim* specifically notes that aspects of the first detailed embodiment discussed in the context of Figure 6A are referred to and relied upon by the Figure 10 embodiment. Ex.[1007], ¶0105 ("In the pixel circuit of FIG. 10, transistors **M31**, **M32** and a capacitor $\mathbf{C_{st4}}$ are connected together in substantially the same relationship as the transistors **M1**, **M2** and the capacitor $\mathbf{C_{st1}}$ of FIG. 6A. The capacitor $\mathbf{C_{st4}}$ has electrodes **A4** and **B4** similar to the electrodes **A** and **B** of the capacitor $\mathbf{C_{st1}}$."). Thus, a POSA would recognize the correspondence between, for example, transistor **Ma** (corresponding to transistors **M1**/**M11**/**M21**/**M31** in later embodiments), capacitor $\mathbf{C_{st}}$ (corresponding to capacitor **C2** in later embodiments), voltage $\mathbf{V_{GS}}$ (across transistors **M1**/**M11**/**M21**/**M31**), data line $\mathbf{D_m}$, data voltage $\mathbf{V_{DATA}}$, and PPS voltage $\mathbf{V_{DD}}$, and would further recognize that *Kim's* discussions of

these related components are relevant to the components in other embodiments that they correspond to. Ex.[1006], ¶¶0073, 0105; Ex.[1002], ¶¶105-106. The correspondence between these components, is also evident from their similar configurations in Figures 1, 6A, and 10 reproduced below. Ex.[1006], Figs. 1, 6A, 10; Ex.[1002], ¶¶105-106. To the extent these disclosures are found to be distinct embodiments, it would be obvious to combine these disclosures in view of *Kim's* teachings and suggestions, which provide motivation to use the disclosures together in implementing variations of *Kim*'s teachings. Ex.[1002], ¶¶105-106.

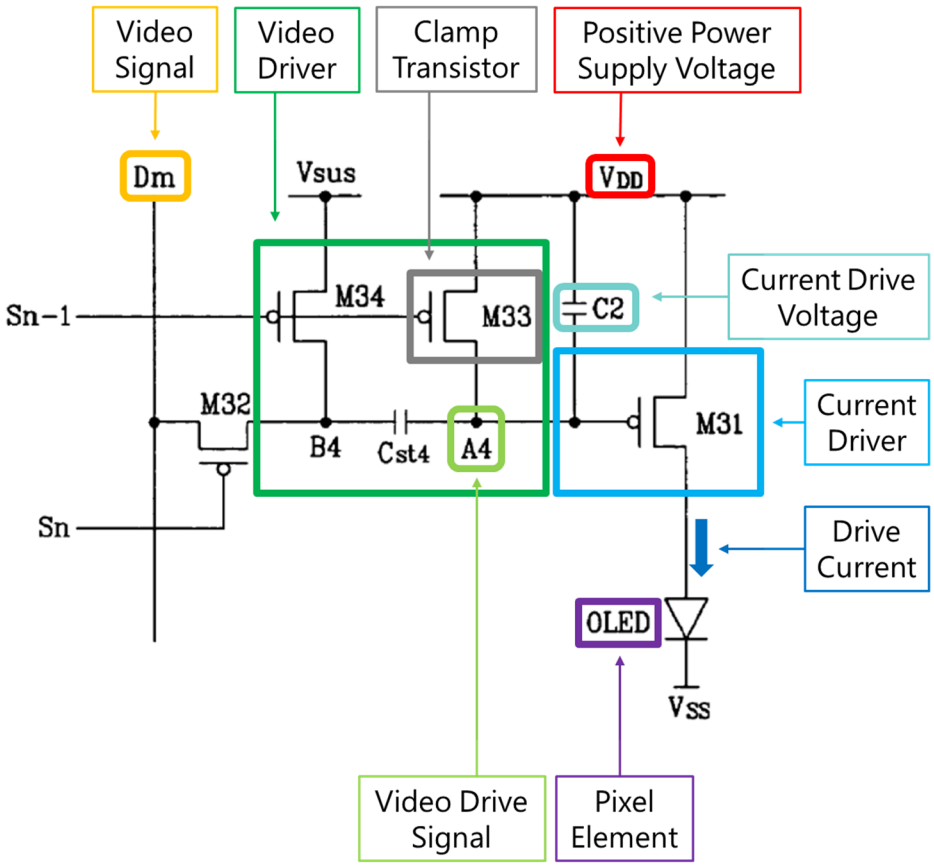


Ex.[1007], Fig. 1.



Ex.[1007], Fig. 6A.

As an example, A POSA would have recognized that Fig. 6A of Kim introduces the concept of using a series capacitor $\mathbf{C_{st1}/C_{st4}}$ to provide the video drive signal to the gate of the drive transistor in the manner described below. A POSA would have implemented this technique, for example, in the manner disclosed by Fig. 10 by including capacitor **C2** to allow the OLED to emit for the entire frame period. Ex.[1002], ¶106.



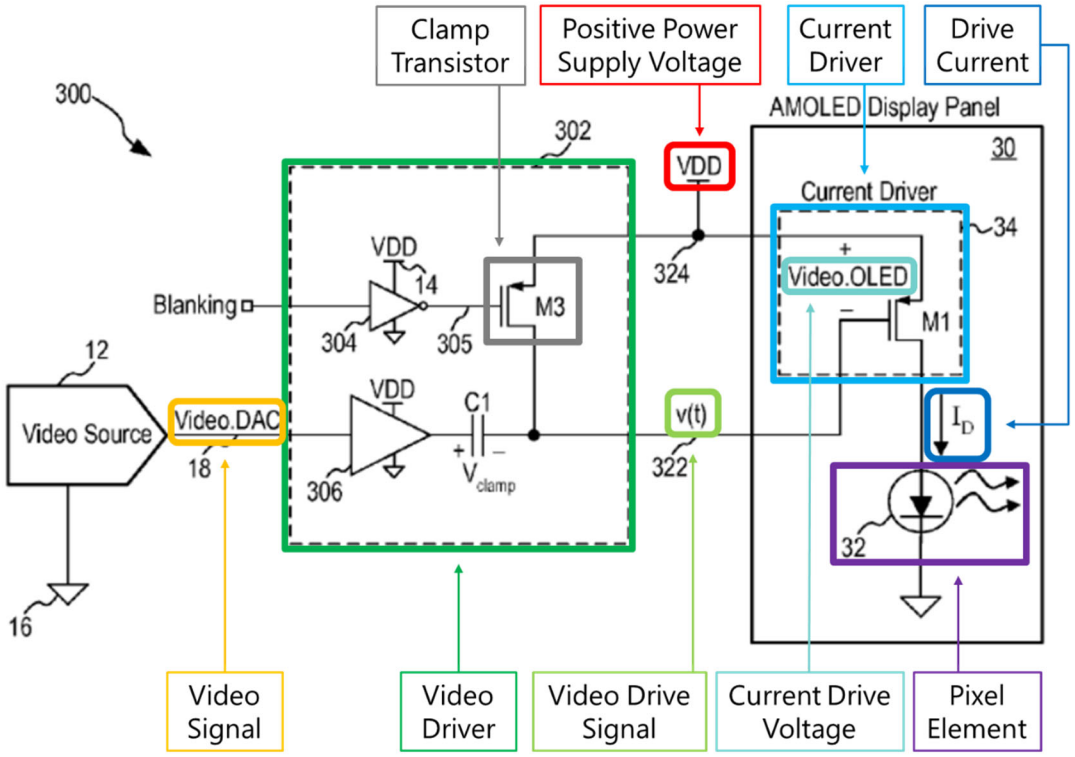
Ex.[1007], Fig. 10.

Claim[1-A]

Video Driver Receiving The Video Signal

Regarding the claimed ***video driver***, in the '521 Patent's third embodiment illustrated in Figure 4 (annotated) reproduced below, the video driver receives video signal Video.DAC and a clamp signal to turn off the OLED pixel, and outputs a VDS v(t) to drive the OLED pixel when it's turned on. Ex.[1001], 6:45-7:51, Fig. 4. The video driver is implemented using a video clamp circuit comprising capacitor C1 having one plate driven by video signal Video.DAC and the other plate providing

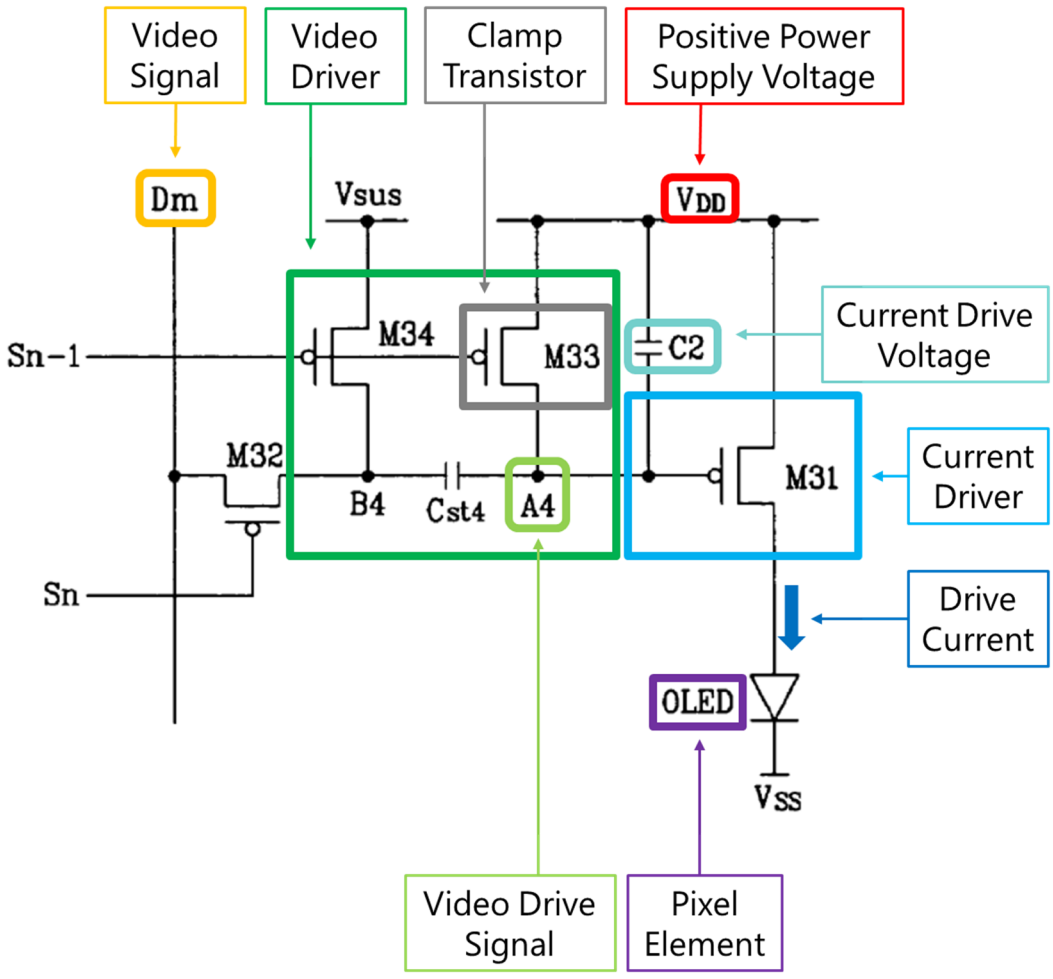
VDS v(t). Ex.[1001], 6:50-60, Fig. 4. The video driver further comprises a clamp transistor M3 having a source terminal connected to PPS voltage VDD and a drain terminal connected to the capacitor C1 plate providing VDS v(t) at node 322 such that, when activated, transistor M3 connects PPS voltage VDD with node 322, thereby preventing any current drive voltage (VDD-v(t)=0) and any drive current through transistor M1. Ex.[1001], 6:50-60, Fig. 4.



Ex.[1001], Fig. 4 (annotated)

Kim's fourth embodiment similarly discloses the claimed ***video driver***, including a video clamp circuit as in the '521 Patent's third embodiment. Specifically, *Kim's* fourth embodiment's video driver includes "capacitor $\mathbf{C_{st4}}$

[which] has electrodes **A4** and **B4** similar to the electrodes **A** and **B** of the capacitor $\mathbf{C_{st1}}$ [of Figure 6A]," and a "transistor **M33**." Ex.[1007], ¶0105. Consistent with *Kim's* Figure 10 (annotated) and as discussed further below, a POSA would understand that *Kim's* capacitor $\mathbf{C_{st4}}$ corresponds to the '521 Patent's capacitor C1, that *Kim's* transistor **M33** corresponds to transistor M3 in the '521 Patent, and, based on the disclosed configuration and functionality of *Kim's* fourth embodiment, *Kim* therefore discloses the claimed ***video driver*** (circuitry in green Video Driver annotation including Capacitor $\mathbf{C_{st4}}$ and clamp transistor **M33**) in the same manner as in the '521 Patent's third embodiment. Ex.[1002], ¶¶107-109; Ex.[1007], Fig. 10.



Ex.[1007], Fig. 10 (annotated).

Regarding ***receiving the video signal***, as discussed in Gr.1-2,Cl.[1-Pre], *Kim* discloses that "data voltage from the data line $\mathbf{D_m}$ is applied to the gate of the transistor **Ma**," and as explained above, a POSA would recognize or find obvious that "data voltage from the data line $\mathbf{D_m}$" corresponds to the relevant portion of the claimed ***video signal***. Ex.[1007], ¶¶0009, 0062; Ex.[1002], ¶110.

Generating Drive Signal Indicative of Video Signal and Referenced To Supply Voltage

Regarding ***generating a video drive signal indicative of the video signal***, as shown above, *Kim's* Figure 10 shows video drive signal (node **A4**) generated by the video driver (green box). "The voltage of the first electrode **A4** of the capacitor $\mathbf{C_{st4}}$ is given as Equation 11." Ex.[1007], ¶¶0108-0109 ("Equation 11").

$$\mathbf{V_{A4}=V_{DD}+\Delta V_{B4}}$$

$$\mathbf{=V_{DD}+V_{DATA}-V_{SUS}}$$

A POSA would recognize that, as in the '521 Patent's third embodiment in which the claimed ***video drive signal*** is voltage v(t) **322** supplied to the gate of transistor **M1** driving the OLED **32** by the video driver **302**, *Kim*'s fourth embodiment similarly discloses voltage at node **A4** being supplied to the gate of transistor **M31** driving the organic light emitting diode **OLED** by the video driver circuitry including Capacitor $\mathbf{C_{st4}}$ and clamp transistor **M33**. A POSA would thus recognize that *Kim*'s "voltage of the first electrode **A4**" corresponds to the claimed ***generated video drive signal***. Ex.[1002], ¶¶111-113.

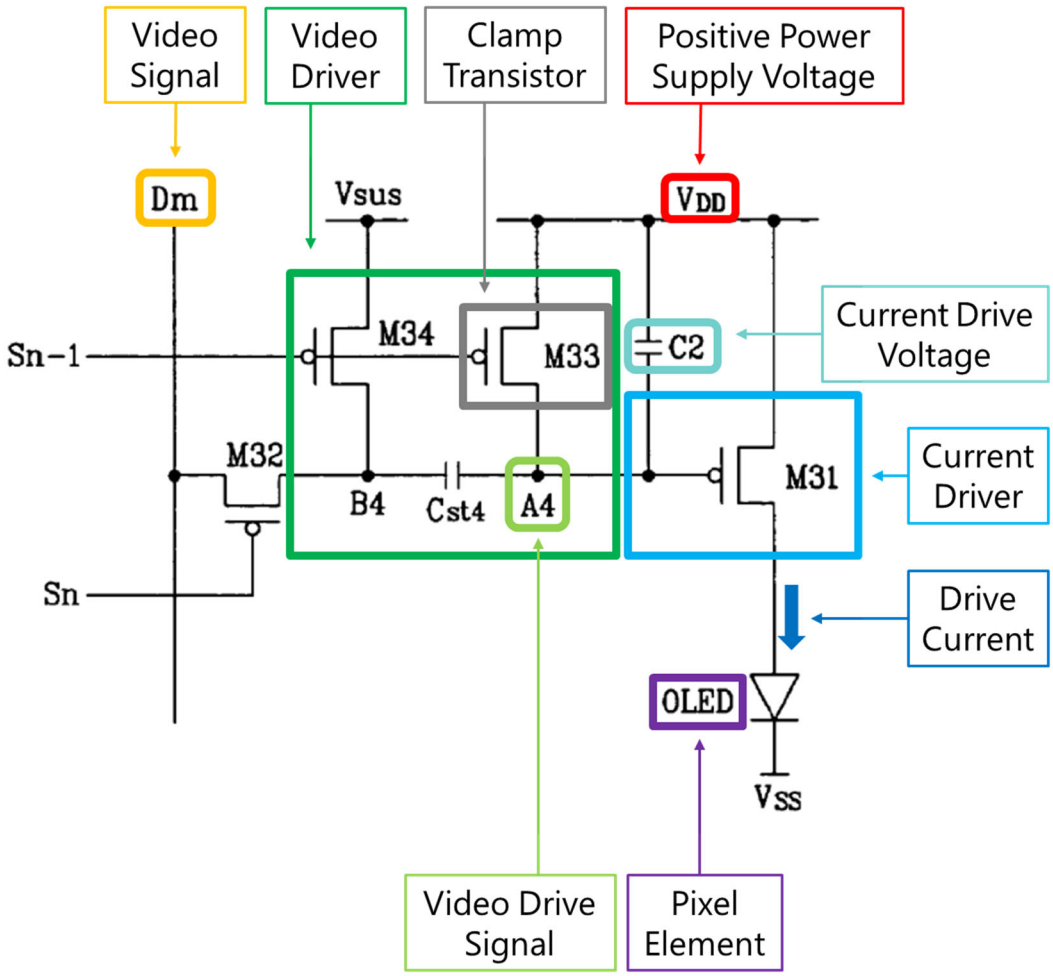
A POSA also would recognize from Equation 11 above that *Kim* discloses ***a video drive signal*** (voltage of the first electrode $\mathbf{V_{A4}}$) ***indicative of the video signal*** (voltage $\mathbf{V_{DATA}}$) because voltage $\mathbf{V_{A4}}$ explicitly depends on data voltage $\mathbf{V_{DATA}}$. Ex.[1007], ¶¶0108-0109 (discussing relationship between nodes A4, B4 and $\mathbf{V_{DATA}}$ via operation of capacitor $\mathbf{C_{st4}}$); Ex.[1002], ¶¶111-113.

Regarding the ***video drive signal*** being ***referenced to a positive power supply voltage***, the '521 Patent's third embodiment describes "video drive 302 is implemented using a video clamp circuit to reference the video drive signal to the power supply voltage VDD. In video driver 302, the video clamp circuit is implemented using… PMOS transistor M3 [which] has a source terminal connected to the power supply VDD voltage," and "In this manner, the clamping voltage V_{clamp} [across capacitor C1] is added to the video signal Video.DAC for the rest of the video line and the video drive signal v(t) is now referenced to the power supply voltage VDD." Ex.[1001], 6:48-7:8.

Consistent with *Kim*'s Figure 10 (annotated) and the discussion above, a POSA would recognize that *Kim*'s fourth embodiment is similarly configured with voltage of the first electrode $\mathbf{V_{A4}}$ being "***referenced to***" PPS voltage $\mathbf{V_{DD}}$: "When… the transistors **M33** and **M34** are turned on, the power supply voltage $\mathbf{V_{DD}}$ is applied to the first electrode **A4** of the capacitor $\mathbf{C_{st4}}$." Ex.[1007], Fig. 10 (annotated), ¶0107. This is also evident from Equation 11 above, in which voltage $\mathbf{V_{A4}}$ is explicitly a function of power supply voltage $\mathbf{V_{DD}}$. Ex.[1007], ¶0109; Ex.[1002], ¶¶114-117.

Therefore, consistent with Figure 10 (annotated) below, a POSA would recognize that *Kim* discloses ***a video driver*** (circuitry in green Video Driver annotation including Capacitor $\mathbf{C_{st4}}$ and clamp transistor **M33**) ***receiving the video signal*** (voltage $\mathbf{V_{DATA}}$) ***and generating a video drive signal*** (voltage of the first

electrode $\mathbf{V_{A4}}$) ***indicative of the video signal*** (voltage $\mathbf{V_{DATA}}$) ***and referenced[5] to a positive power supply voltage*** (PPS voltage $\mathbf{V_{DD}}$) ***of the AMOLED display panel***. Ex.[1007], Fig. 10; Ex.[1002], ¶¶107-117.



Ex.[1007], Fig. 10 (annotated).

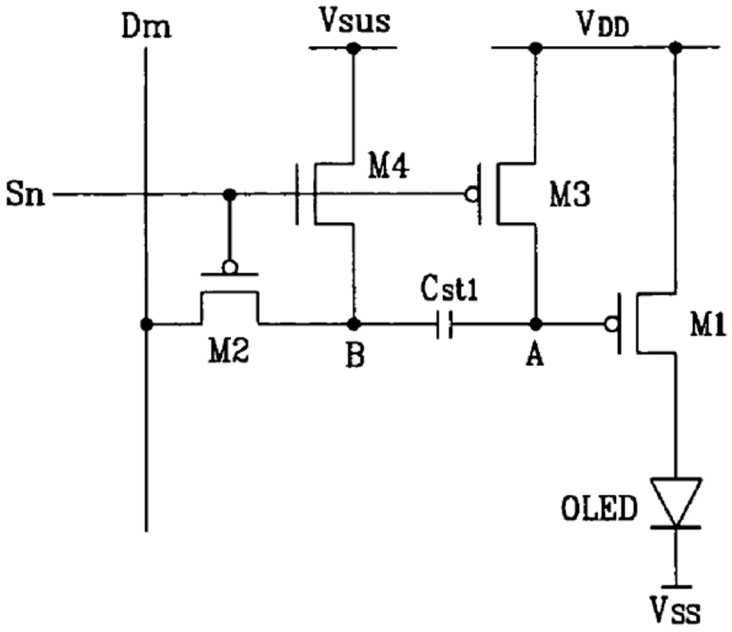
Claim[1-B]

Current Driver Coupled to the OLED Pixel Element Receiving the Video Drive Signal and the Positive Power Supply

[5] *See supra,* §VI.

Regarding the ***current driver coupled to at least one OLED pixel element***, ***the current driver receiving the video drive signal and the positive power supply voltage***, as shown above, *Kim* has a current driver (e.g. **M31**) receiving the video drive signal generated at node **A4**, and the driver is coupled to a pixel element (OLED) and power supply ($\mathbf{V_{DD}}$). In this context, *Kim* explains for Figure 10, "Therefore, the power supply voltage $\mathbf{V_{DD}}$ and the voltage of the first electrode **A4** of the capacitor $\mathbf{C_{st4}}$ are applied to both electrodes of the capacitor **C2**, and the capacitor **C2** is charged," creating a current drive voltage. Ex.[1007], ¶0110.

As discussed in Gr.1-2,Cl.[1-Pre], *Kim* also shows a circuit in Figure 6A which it explains has components connected in "substantially the same relationship as" shown in Figure 10, although without line **Sn-1** present. Ex.[1007], ¶0105, Fig. 6A.



Ex.[1007], Fig. 6A.

Kim discloses that in Figure 6A, "transistor **M1** is a driving transistor for controlling the current that flows to the **OLED**, and it has a source coupled to the power supply voltage $\mathbf{V_{DD}}$, and a drain coupled to an anode of the **OLED**. A cathode of the **OLED** is coupled to a reference voltage $\mathbf{V_{SS}}$ and emits light that corresponds to the current applied from the transistor **M1**" where $\mathbf{V_{SS}}$ may be ground. Ex.[1007], ¶0052.

Thus, a POSA would recognize that *Kim* discloses ***a current driver*** (circuitry in blue Current Driver annotation including transistor **M31/M1**) ***coupled to at least one OLED pixel element*** (organic light emitting diode **OLED**)***, the current driver***

receiving the video drive signal (voltage of the first electrode $\mathbf{V_{A4}}$ or node **A**) ***and the positive power supply voltage*** ($\mathbf{V_{DD}}$). Ex.[1002], ¶¶118-125.

Providing a Drive Current to the OLED Pixel Element

Regarding ***providing a drive current to the at least one OLED pixel element***, *Kim* explains "the voltage charged in the capacitor **C2** is given as Equation 12, and the corresponding current flows to the **OLED**." Ex.[1007], ¶¶0111.

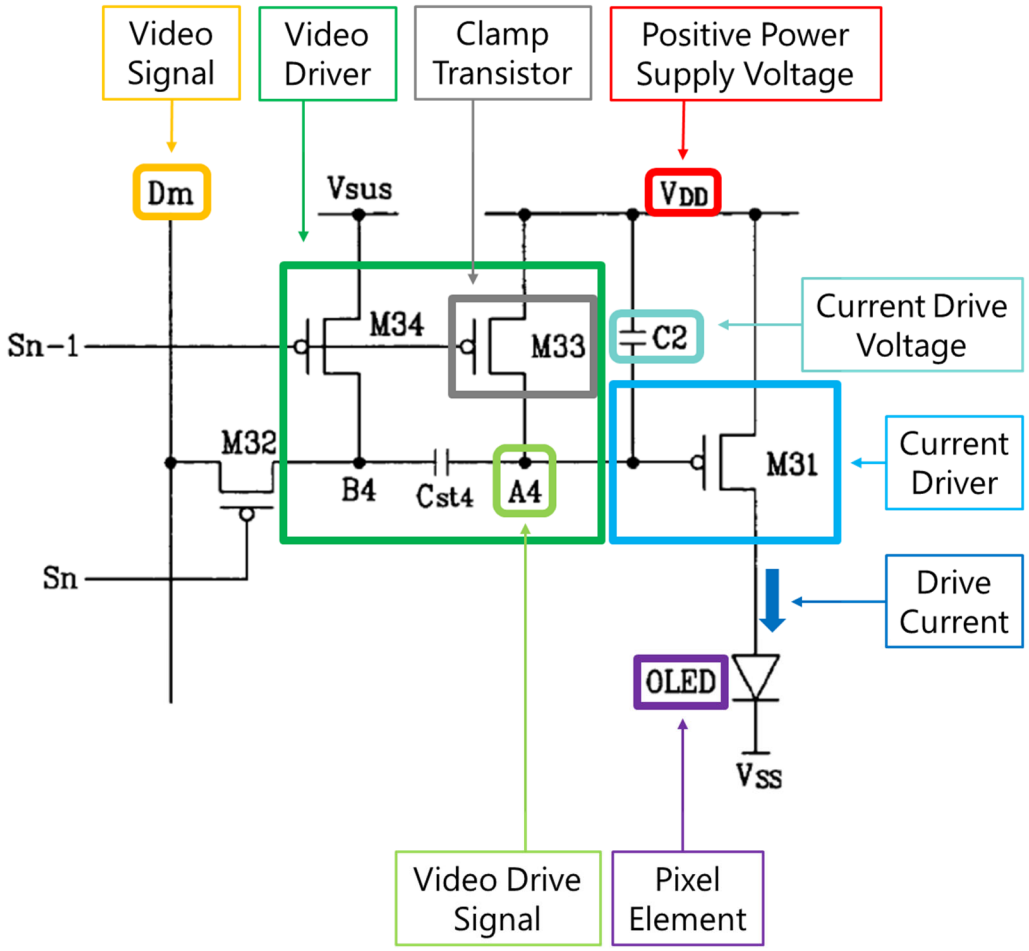
$$\mathbf{V_{C2}=V_{DD}-(V_{DD}+V_{DATA}-V_{sus})=V_{DATA}-V_{SUS}}$$[6]

Ex.[1007], ¶0112 ("Equation 12").

"The current flowing to the **OLED** is given as Equation 13," which *Kim* labels as "$\mathbf{I_{OLED}}$," which is discussed further in Gr.1-2,Cl.[1-C] below. Ex.[1007], ¶0113. Similarly in Figure 6A, *Kim* identifies the drive current as "$\mathbf{I_{OLED}}$," which is "the current flows to the OLED through the transistor **M1**," and is based on "$\mathbf{V_{GS1}}$ [which] is [the] voltage between the gate and the source of the transistor **M1**." Ex.[1007], ¶¶0069-0070. A POSA would therefore recognize that *Kim* discloses ***providing a drive current*** (transistor current $\mathbf{I_{OLED}}$) ***to the at least one OLED pixel element***. Ex.[1002], ¶¶126-130.

[6] Petitioner notes that although Equation 12 should properly result in $\mathbf{V_{C2}=V_{SUS}-V_{DATA}}$ instead of $\mathbf{V_{C2}=V_{DATA}-V_{SUS}}$, this error in *Kim* does not affect the mapping to the '521 claims as set forth in the analysis in Grounds 1 and 2.

Claim[1-C]



Ex.[1007], Fig. 10 (annotated).

The Drive Current being Proportional to a Current Drive Voltage

Regarding the claimed ***drive current being proportional to a current drive voltage***, *Kim* explains for Figure 10, "the voltage charged in the capacitor **C2** is given as Equation 12, and the corresponding current flows to the **OLED**." Ex.[1007], ¶¶0111-0112 ("Equation 12").

$$V_{C2}=V_{DD}-(V_{DD}+V_{DATA}-V_{SUS})$$

$$=V_{DATA}-V_{SUS}$$

"The current flowing to the **OLED** is given as Equation 13." Ex.[1007], ¶0113 ("Equation 13").

$$I_{OLED}=\beta/2(V_{GS31}-V_{TH31})^2$$

$$=\beta/2((V_{DATA}-V_{SUS})-V_{TH31})^2$$

In the '521 Patent, the claimed ***current drive voltage*** is Video.OLED, which is the voltage across the gate and terminal of transistor M1 that drives OLED 32. As illustrated in *Kim's* Figure 10 (annotated), the voltage across the gate and source (V_{GS}) of transistor **M31** that drives organic light emitting diode **OLED** is also the same voltage across capacitor **C2** (i.e., $V_{C2}=V_{GS31}$). Thus, the voltage across capacitor **C2** ($V_{C2}=V_{GS31}$) corresponds to the claimed ***current drive voltage***. Ex.[1002], ¶¶131-138.

A POSA would therefore recognize that *Kim's* voltage across the gate and source (V_{GS}) of the transistor **M31** corresponds to the claimed ***current drive voltage***, and that *Kim's* current I_{OLED} corresponds to the claimed ***drive current***. Ex.[1002], ¶¶131-138. A POSA would also recognize that because *Kim's* transistor **M31** and the '521 Patent's transistor M1 are both P-channel MOSFETs, they would both operate in the same manner based on the well-known principles and functionalities of P-Channel MOSFETs. Ex.[1002], ¶¶131-138. Therefore, in the context of the '521 Patent's drive current being "proportional" to the current drive voltage, because

the P-channel MOSFETs would operate in the same manner, a POSA would understand that *Kim's* current $\mathbf{I_{OLED}}$ is also "***proportional***" to the gate and source ($\mathbf{V_{GS}}$), in the same manner as it is "***proportional***" in the '521 Patent.[7] Ex.[1002], ¶¶131-138. Thus, a POSA would recognize that *Kim* discloses the ***drive current*** (drain current $\mathbf{I_d}$) ***being proportional to a current drive voltage*** (gate-to-source voltage $\mathbf{V_{gs}}$).

The Current Drive Voltage being Indicative of the Video Signal

Regarding the claimed ***current drive voltage being indicative of the video signal***, as discussed for Gr.1-2,Cl.[1-A], *Kim* discloses ***the video drive signal*** (voltage of the first electrode $\mathbf{V_{A4}}$) being ***indicative of the video signal*** (voltage $\mathbf{V_{DATA}}$). Ex.[1002], ¶¶139-140. A POSA would also understand that since voltage $\mathbf{V_{GS31}}$ is calculated based on voltage $\mathbf{V_{A4}}$, because voltage $\mathbf{V_{A4}}$ is "***indicative***" of voltage $\mathbf{V_{DATA}}$, voltage $\mathbf{V_{GS31}}$ must also be "***indicative***" of voltage $\mathbf{V_{DATA}}$. This is also evident from Equation 12 above, in which the result of $\mathbf{V_{A4}}$ in Equation 11 is directly substituted into Equation 12.

[7] A POSA would thus understand "proportional" as having its plain and ordinary meaning in the context of the '521 Patent based on the operation of a typical P-channel MOSFET disclosed therein. Ex.[1002], ¶¶137.

Thus, a POSA would recognize that *Kim* discloses the ***current drive voltage*** (voltage $\mathbf{V_{C2}}$ (=voltage $\mathbf{V_{GS31}}$)) ***being indicative of the video signal*** ($\mathbf{V_{DATA}}$). Ex.[1002], ¶¶139-140.

Independent of the Positive Power Supply Voltage

Regarding the claimed ***independent of the positive power supply voltage***, *Kim* discloses "a current that flows to the **OLED** of a pixel circuit in a light emitting display is substantially prevented from being influenced by a power supply voltage. Further, a current that flows to the **OLED** of a pixel circuit in a light emitting display may be substantially prevented from being influenced by deviations of a threshold voltage of a driving transistor." Ex.[1007], ¶¶0014-0015.

As discussed above, *Kim* explains for Figure 10, "The current flowing to the **OLED** is given as Equation 13." Ex.[1007], ¶0113("Equation 13").

$$\mathbf{I_{OLED}}=\beta/2(\mathbf{V_{GS31}}-\mathbf{V_{TH31}})^2$$

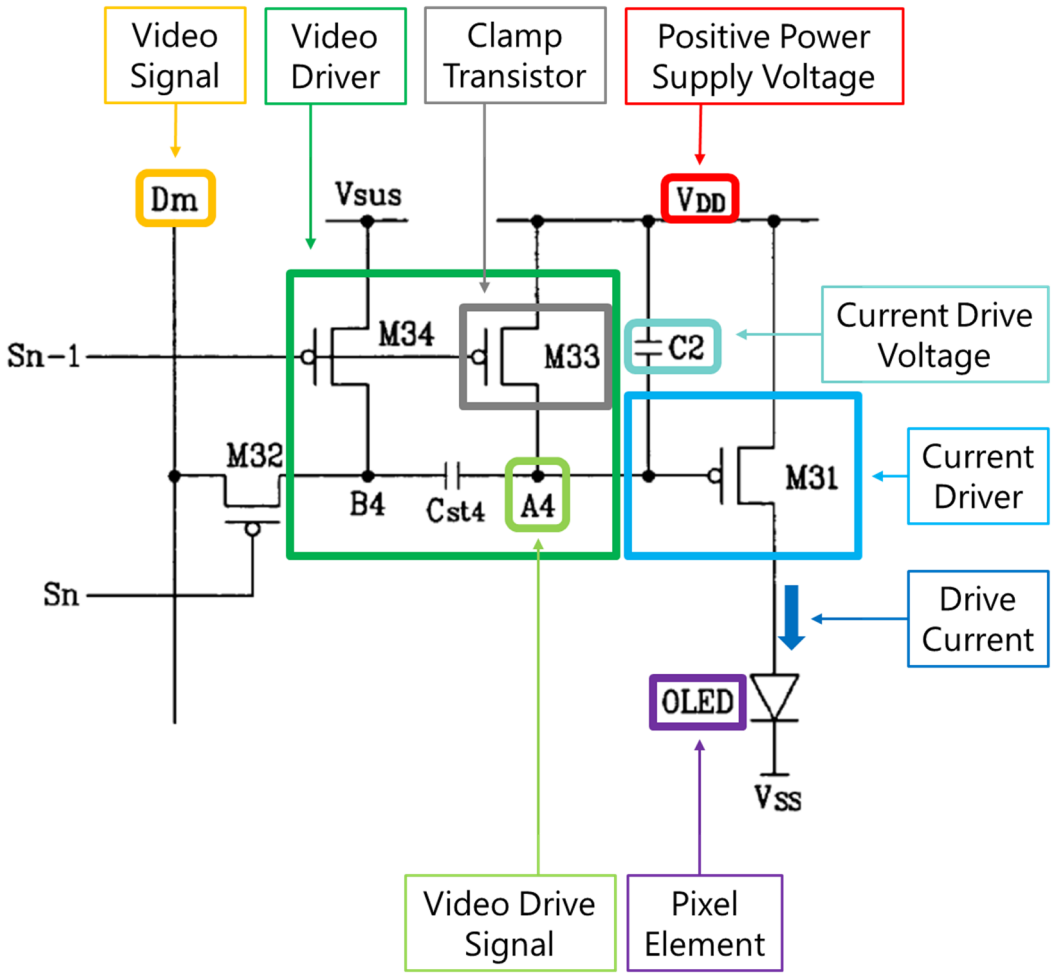
$$=\beta/2((\mathbf{V_{DATA}}-\mathbf{V_{sus}})-\mathbf{V_{TH31}})^2$$

"As can be seen from Equation 13, the current flowing to the **OLED** is substantially **not influenced** by the power supply voltage $\mathbf{V_{DD}}$." Ex.[1007], ¶0114. A POSA would recognize that this is true because none of the parameters in this resulting equation are dependent on $\mathbf{V_{DD}}$ (β "is a constant," $\mathbf{V_{TH31}}$ "is a threshold voltage at the transistor," $\mathbf{V_{DATA}}$ is "a data voltage from the data line Dm," and $\mathbf{V_{sus}}$

is "a compensation voltage… differing from the power supply voltage $\mathbf{V_{DD}}$"). Ex.[1007], ¶¶0009-0011, 0071; Ex.[1002], ¶¶141-147.

A POSA would understand that because *Kim's* drive current is "**not influenced**" by the PPS voltage $\mathbf{V_{DD}}$, it is therefore "***independent of***" the PPS voltage $\mathbf{V_{DD}}$. Ex.[1002], ¶¶141-147.

Therefore, as also consistent with Figure 10 (annotated) below, a POSA would recognize that *Kim* further discloses ***the drive current*** ($\mathbf{I_{OLED}}$) ***being… independent of the positive power supply voltage*** (PPS voltage $\mathbf{V_{DD}}$). Ex.[1007], Fig. 10; Ex.[1002], ¶¶141-147.



Ex.[1007], Fig. 10 (annotated).

2. *Claim 2*

Video Drive Signal is Indicative of the Sum…Between The Positive Power Supply Voltage and the Video Signal

Equation 11 below shows that voltage $\mathbf{V_{A4}}$ is explicitly a function of the sum of PPS voltage $\mathbf{V_{DD}}$ and voltage $\mathbf{V_{DATA}}$. Ex.[1002], ¶¶148-154; Ex.[1007], ¶0109 ("Equation 11").

$$\mathbf{V_{A4}=V_{DD}+\Delta V_{B4}}$$

$$\mathbf{=V_{DD}+V_{DATA}-V_{sus}}$$

Thus, consistent with Figure 10 (annotated) below, a POSA would recognize that *Kim* discloses ***the video drive signal*** (voltage of the first electrode $\mathbf{V_{A4}}$) ***is indicative of the sum of*** ($\mathbf{V_{A4}=V_{DD}+V_{DATA}-V_{sus}}$) ***the positive power supply voltage*** (PPS voltage $\mathbf{V_{DD}}$) ***and the video signal*** ($\mathbf{V_{DATA}}$). Ex.[1007], Fig. 10 (annotated); Ex.[1002], ¶¶148-154.

Current drive voltage…indicative of the difference between the positive power supply voltage and the video drive signal

Regarding the claimed ***current drive voltage*** being ***indicative of the difference between the positive power supply voltage*** (drive voltage $\mathbf{V_a}$) ***and the video drive signal***, a POSA would recognize that voltage $\mathbf{V_{C2}}$ is equivalent to the gate-source voltage $\mathbf{V_{GS31}}$, which is the difference between power supply voltage $\mathbf{V_{DD}}$ and voltage of the first electrode $\mathbf{V_{A4}}$. Ex.[1002], ¶¶148-154; *see also* Ex.[1007], ¶0110 ("the power supply voltage $\mathbf{V_{DD}}$ and the voltage of the first electrode **A4** of the capacitor $\mathbf{C_{st4}}$ are applied to both electrodes of the capacitor **C2**").

This is also evident from *Kim*'s Equation 12, which is simply the result of substituting Equation 11 for the voltage of the first electrode $\mathbf{V_{A4}}$. Ex.[1002], ¶¶148-154; Ex.[1007], ¶¶0111, 0112 ("Equation 12").

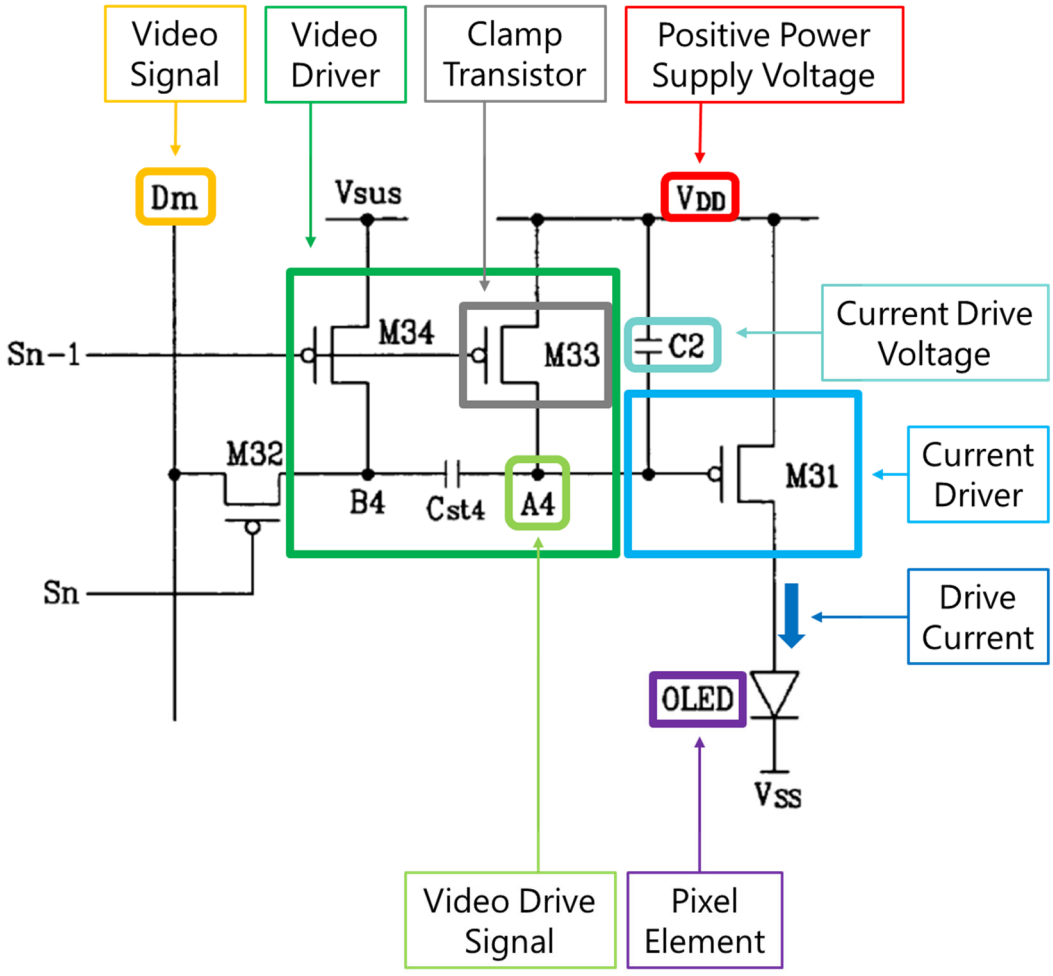
$$\mathbf{V_{C2}=V_{DD}-(V_{DD}+V_{DATA}-V_{sus})}$$

$$\mathbf{=V_{DATA}-V_{sus}}$$

Reversing said substitution results in the following equation. Ex.[1002], ¶¶148-154.

$$V_{C2}=V_{DD}-V_{A4}$$

Therefore, as also consistent with Figure 10 (annotated) below, a POSA would recognize that *Kim* further discloses ***the current drive voltage*** (voltage V_{C2} (=voltage V_{GS31})) ***is indicative of the difference between the positive power supply voltage*** (PPS voltage V_{DD}) ***and the video drive signal*** (voltage of the first electrode V_{A4}). Ex.[1007], Fig. 10; Ex.[1002], ¶¶148-154.

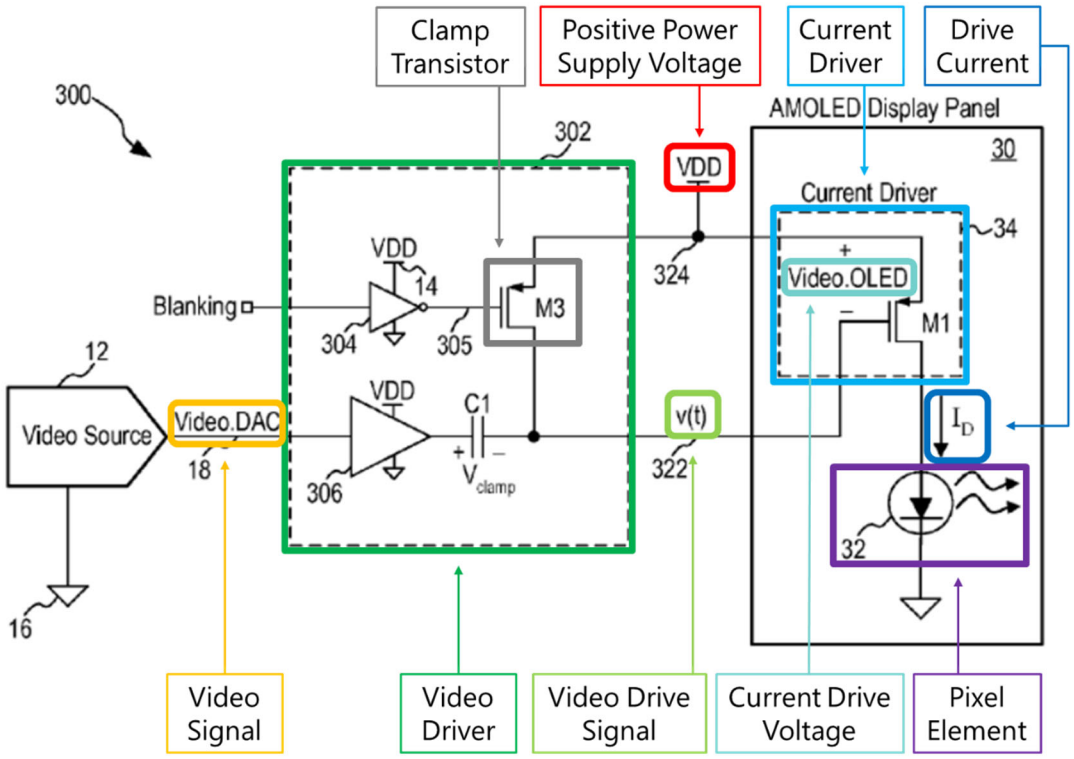


Ex.[1007], Fig. 10 (annotated).

3. *Claim 7*

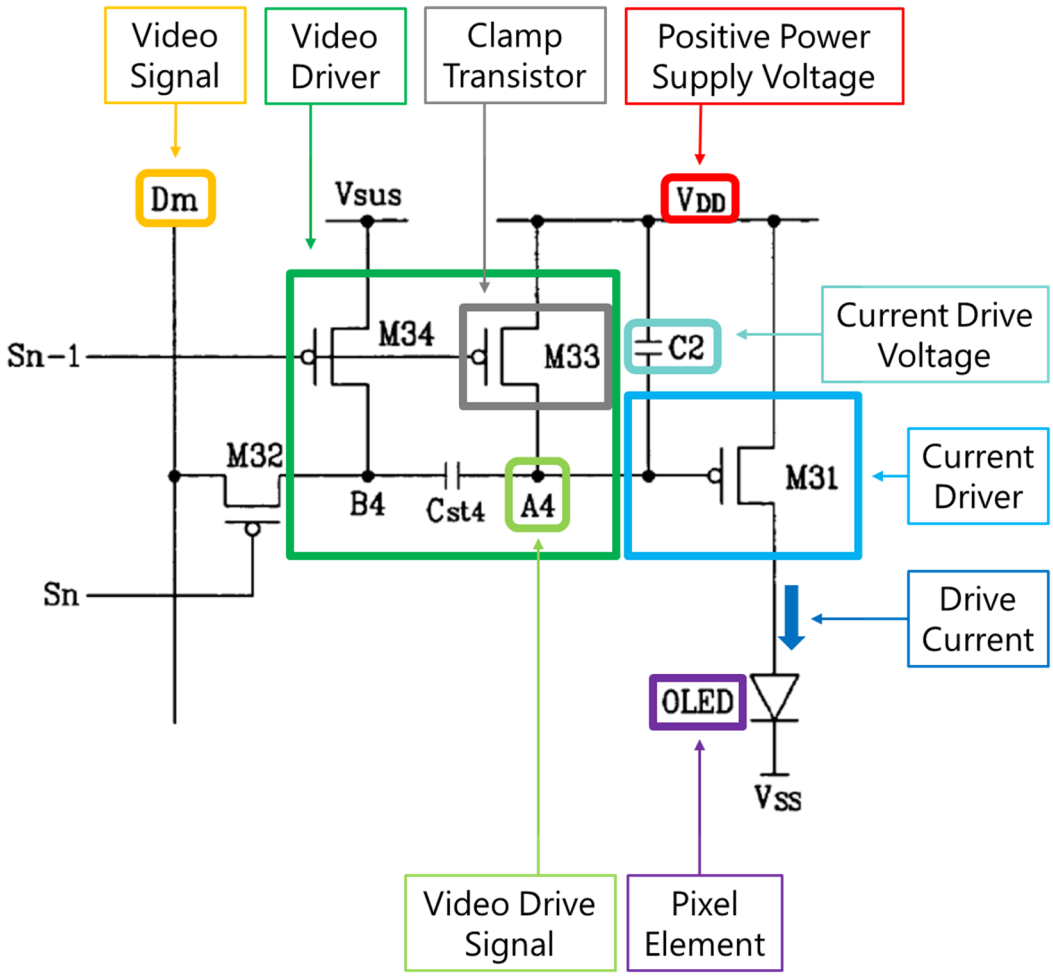
Video Driver includes a Video Clamp Circuit for Providing the Video Drive Signal being the Sum of the Positive Power Supply Voltage and the Video Signal

Claim 7 corresponds to the '521 Patent's third embodiment shown in Figure 4 (annotated) below. Ex.[1001], 6:45-8:2, Fig. 4.



Ex.[1001], Fig. 4 (annotated).

Kim discloses in Figure 10 (annotated) below, transistor **M33** is (similar to transistor M3 in the '521 Patent) coupled between power supply voltage $\mathbf{V_{DD}}$ and the gate of OLED drive transistor **M31** (M1 in the '521 Patent). Ex.[1007], Fig. 10.



Ex.[1007], Fig. 10 (annotated).

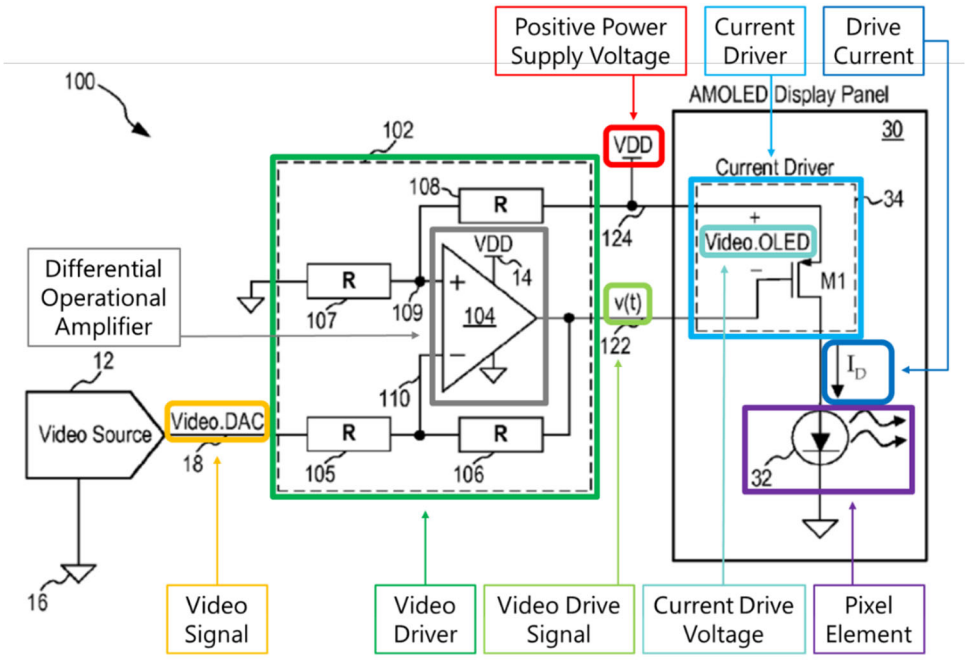
Kim explains for Figure 10, "[when] the transistors **M33** and **M34** are turned on, the power supply voltage $\mathbf{V_{DD}}$ is applied to the first electrode **A4** of the capacitor $\mathbf{C_{st4}}$. Ex.[1007], ¶0107. A POSA would understand that clamp circuits serve to ensure that "voltage drifts in the power supply voltage [] are removed from the current drive signal," which is *Kim*'s transistor **M33**'s purpose. Ex.[1001], 7:48-50; Ex.[1002], ¶¶155-160. Thus, a POSA would recognize *Kim*'s circuitry including

transistor **M33** is a ***video clamp circuit***. Ex.[1002], ¶¶155-160; Ex.[1007], Fig. 10 (annotated).

Therefore, consistent with Figure 10 (annotated) above, a POSA would recognize that *Kim* discloses ***the video driver comprises a video clamp circuit*** (circuitry including clamp transistor **M33**) ***for providing the video drive signal being the sum of the positive power supply voltage and the video signal***. Ex.[1002], ¶¶155-160.

B. Ground 3: Claims 1 and 2 are Anticipated by *Hayafuji*

Figure 2 of the '521 Patent illustrating the first embodiment is provided for reference in this invalidity analysis.



Ex.[1001], Fig. 2 (annotated).

1. *Claim 1*

Claim[1-Pre]

To the extent the preamble is limiting, *Hayafuji* discloses it. Ex.[1002], ¶¶162-172.

Active Matrix Organic Light Emitting Diode Display Panel…Comprising a Plurality of [OLED] pixel elements

Hayafuji discloses "a display panel constructed by arranging light emitting elements in a matrix pattern," including "an organic EL (electroluminescent) element in which an organic material is employed in a light emitting layer." Ex.[1006], ¶0004. The "organic EL elements are employed as light emitting elements" and "constitute[e] pixels." The organic emitting elements (**E1**) are depicted in both Figures 2 and 6 of *Hayafuji* (which show similar drive circuits with identical reference labels) using a circuit symbol that a POSA would understand is a diode emitting light. Ex.[1006], ¶¶0002, 0006, 0010, 0029-0030, 0047; Ex.[1002], ¶¶162-172. Thus, a POSA would understand that *Hayafuji's* organic EL elements are OLEDs. Ex.[1002], ¶¶162-172.

FIG.2
(Prior Art)

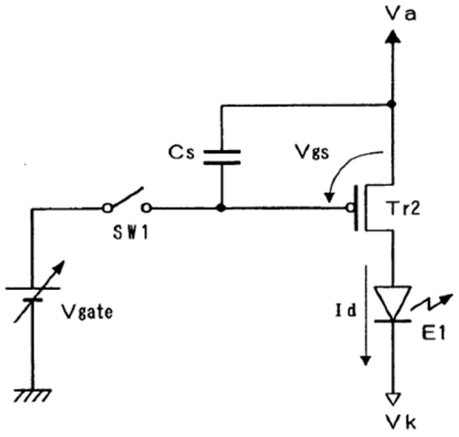
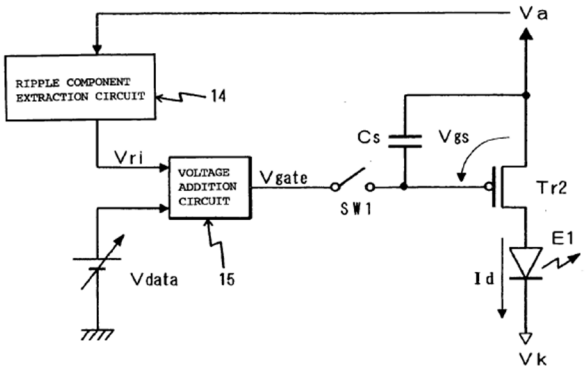


FIG.6

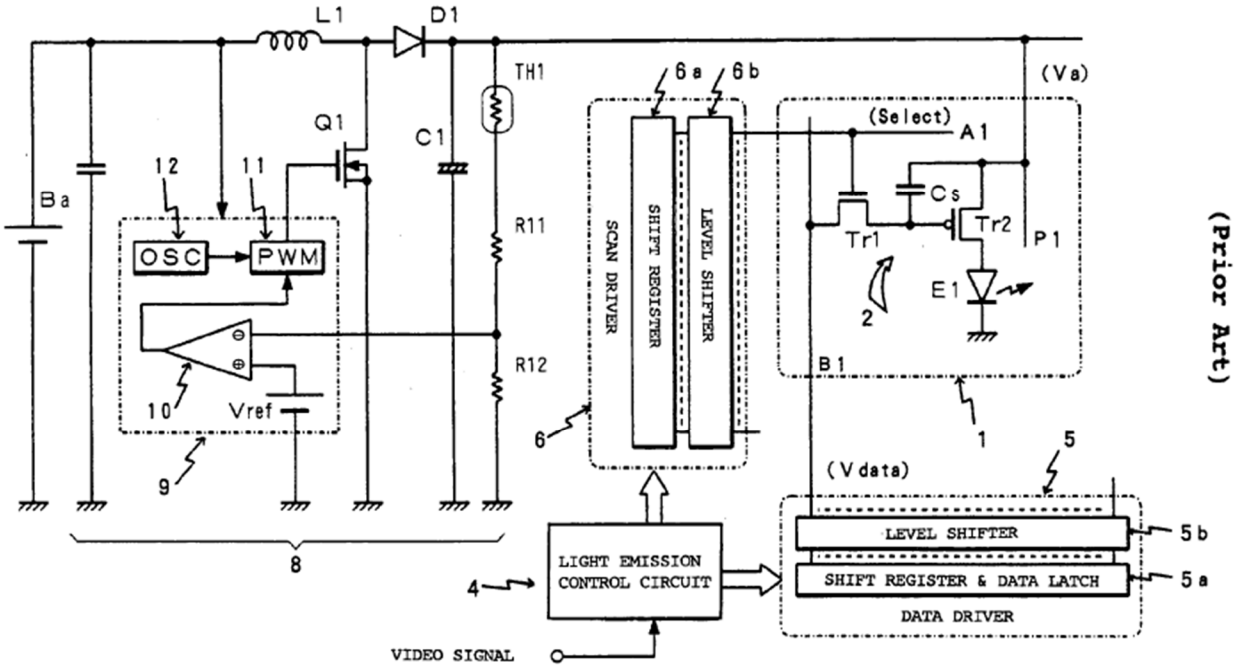


Ex.[1006], Figs. 2, 6.

Receiving a Video Signal To Be Displayed

In each of the '521 Patent's embodiments (e.g., as illustrated in Figure 2 (annotated) reproduced below), a video source provides, for a single pixel, a video signal Video.DAC to the video driver. A POSA would have recognized that the acronym DAC in the "Video.DAC" signal is a digital-to-analog converted (DAC) signal.

Hayafuji describes techniques useful in a display panel as shown in Figure 1 (which *Hayafuji* states depicts an "equivalent circuit diagram of a pixel structure" shown in Figure 2 (above)). Ex.[1006], ¶¶0031-0032, Fig. 1; Ex.[1002], ¶¶162-172.

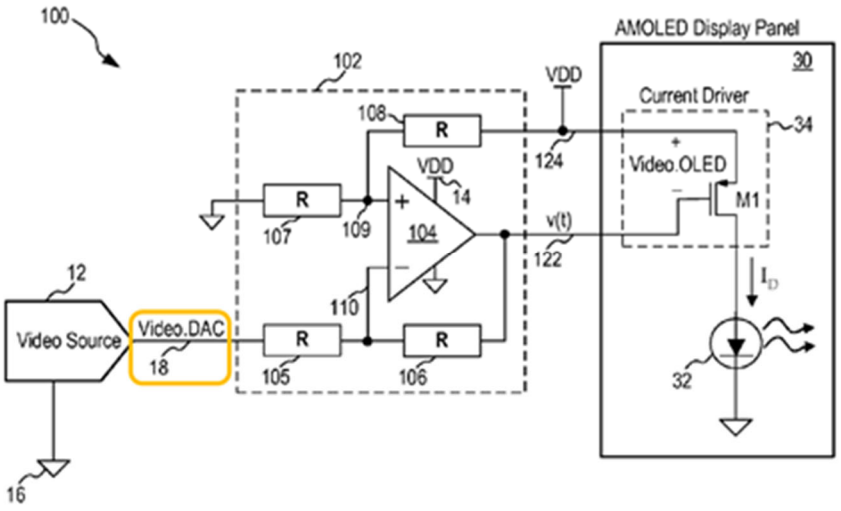


Ex.[1006], Fig. 1.

As illustrated in Figure 1, *Hayafuji* discloses an "input video signal" (bottom of Figure 1) is provided to "light emission control circuit 4 [which] converts [the] input video signal to corresponding pixel data for each one pixel." Ex.[1006], ¶0013. "During the address period… the serial pixel data… [is] sequentially supplied to a shift register and data latch circuit," which in turn outputs, "data voltage $\mathbf{V_{data}}$ corresponding to the pixel data [which] is respectively supplied [via data line **B1**] to the source of the scan selection transistor **Tr1**," which connects to the gate of "light emission drive transistor **Tr2**." More succinctly, *Hayafuji* explains that "data voltage $\mathbf{V_{data}}$ [] corresponds to a write data from the data line **B1**" and "data voltage $\mathbf{V_{data}}$

transmitted via the above-mentioned data line **B1** is equivalently output from a D/A converter." Ex.[1006], ¶¶0009, 0051, Fig. 1; Ex.[1002], ¶¶162-172.

Thus, despite the use of the term "video signal" in *Hayafuji* Figure 1, a POSA would understand that the analog signal ($\mathbf{V_{data}}$) output from the D/A converter in *Hayafuji* corresponds to the '521 Patent's claimed video signal (Video.DAC) that is similarly output by the digital-to-analog converter at video source 12. Ex.[1002], ¶¶162-172; *see also* Ex.[1001], 1:61-65 ("In most systems, the video signals are digital in nature and the signal processing step of video source 12 is to convert the digital video signals to analog signals, thereby generating the analog signal Video.DAC on an output bus 18."). The corresponding video signals (i.e., "Video.DAC" and "$\mathbf{V_{data}}$") are illustrated in the annotated figures below.



Ex.[1001], Fig. 2 (annotated).

FIG.6

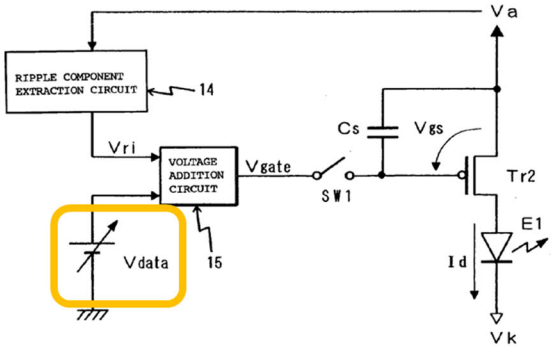


FIG.7

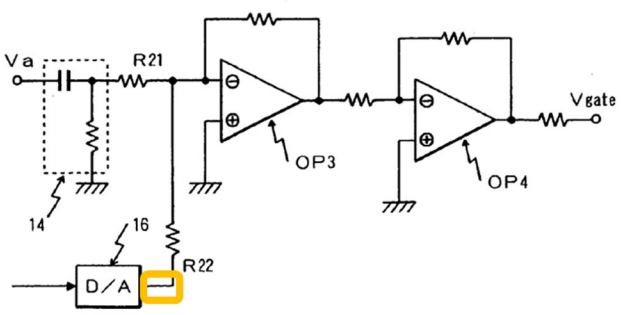
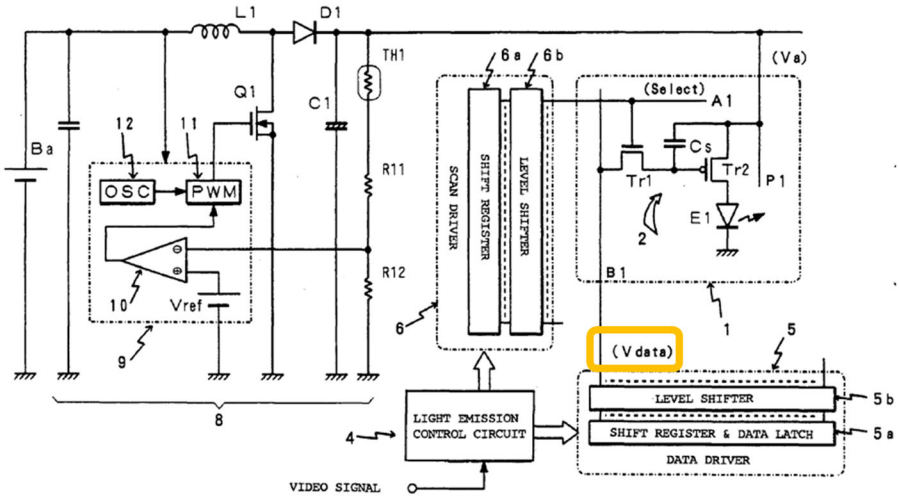


FIG.1



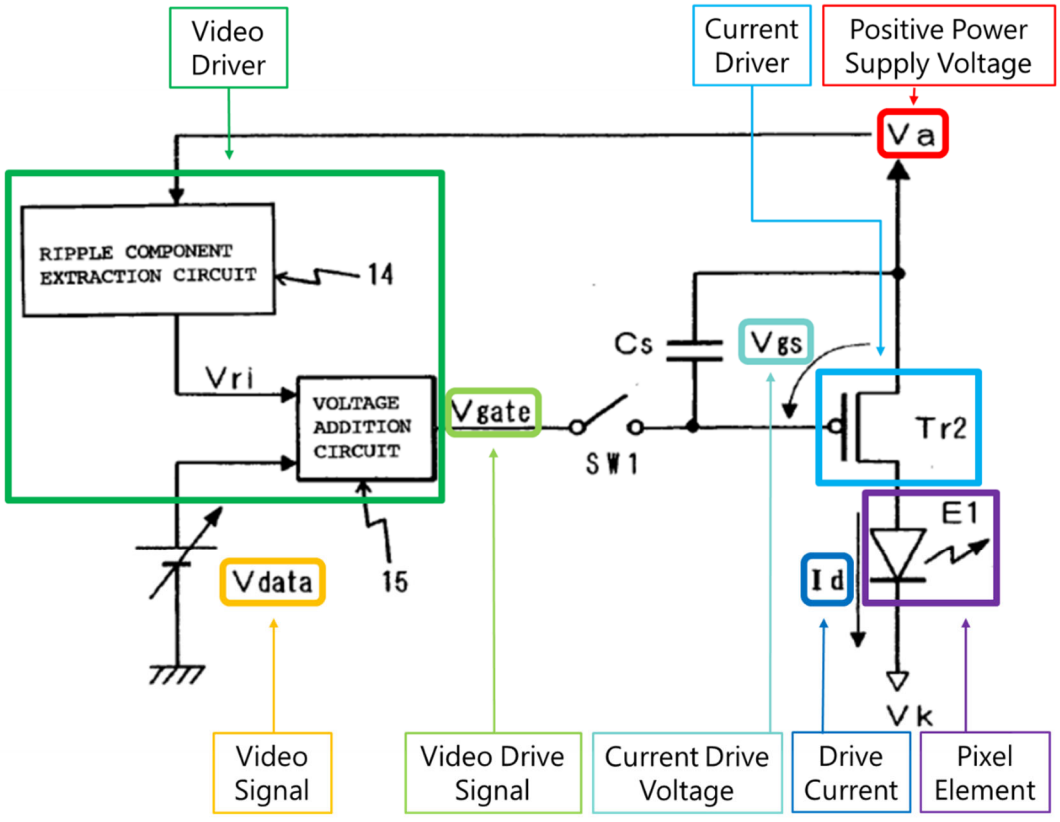
Ex.[1006], Figs. 1, 6, 7 (annotated).

Claim[1-A]

Video Driver Receiving The Video Signal

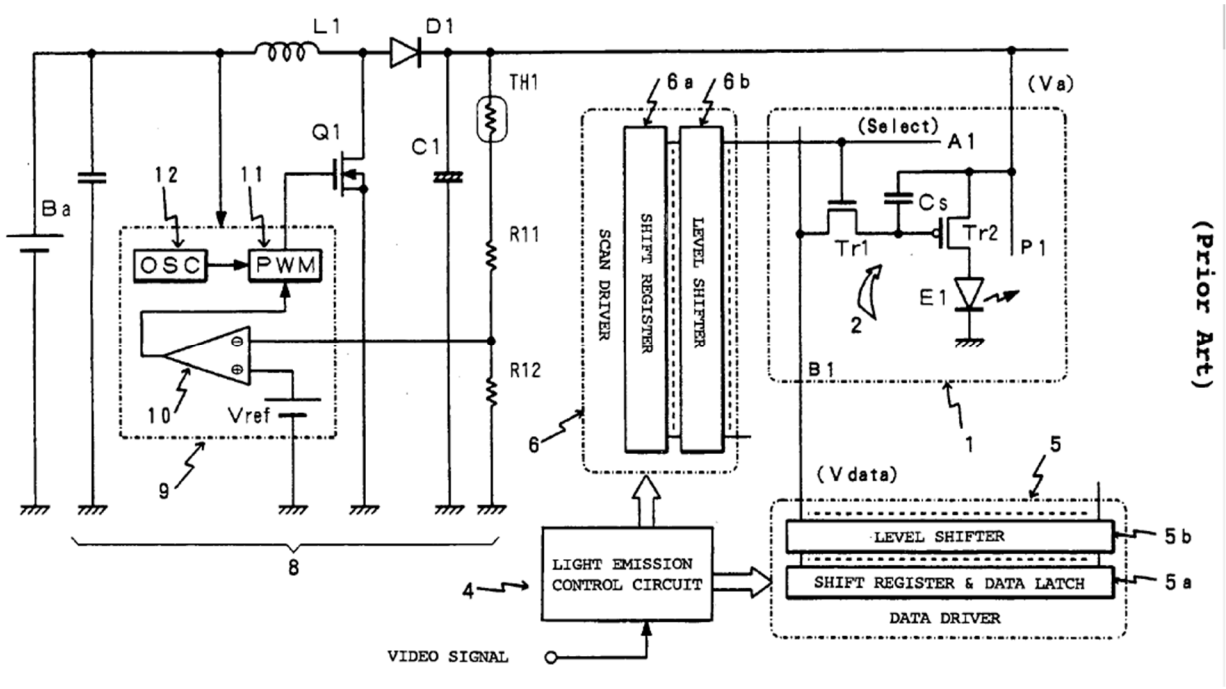
As illustrated below in Figures 1 and 6 (annotated), *Hayafuji* discloses ***a video driver*** (including extraction circuit **14** and voltage addition circuit **15** in green annotation below) ***receiving the video signal*** (video signal is received and processed into data voltage $\mathbf{V_{data}}$ on line **B1** corresponding to the portion of the video signal destined for a target pixel) ***and generating a video drive signal*** (gate voltage $\mathbf{V_{gate}}$) ***indicative of the video signal*** (e.g., indicative of data voltage $\mathbf{V_{data}}$) ***and referenced***

to a positive power supply voltage (drive voltage $\mathbf{V_a}$, as explained below) ***of the AMOLED display panel***.[8] Ex.[1006], Fig. 6; Ex.[1002], ¶¶173-182; *see also* Gr.4,Cl.[3] (further supporting this analysis in the context of Fig. 10).



Ex.[1006], Fig. 6 (annotated).

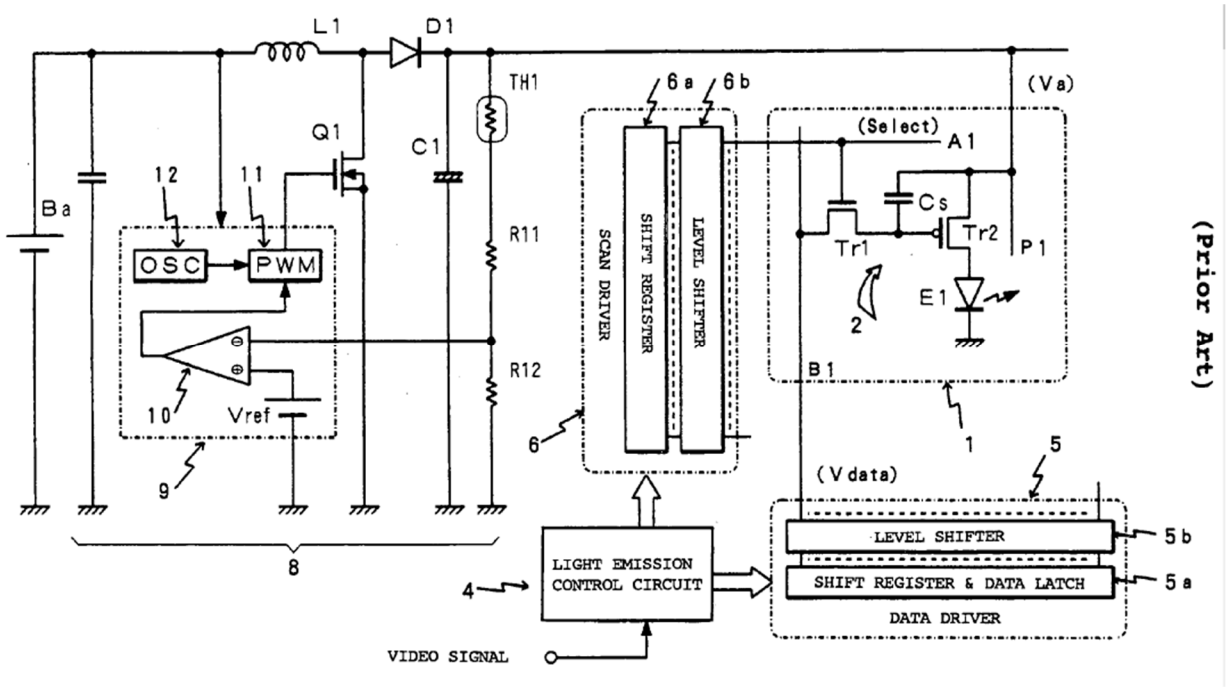
[8] Emphasis supplied throughout, unless noted.



Ex.[1006], Fig. 1.

Supply Voltage

Hayafui explains, with refence to Figure 1 (below), that DC-DC converter power supply 8 generates "drive voltage $\mathbf{V_a}$" supplied to "pixels **2** arranged in the display panel **1** via power lines **P1**". Ex.[1006], ¶¶0017-0018, 0021. Because $\mathbf{V_a}$ is depicted as the voltage output by the power supply and present on power line **P1**, a POSA would understand that $\mathbf{V_a}$ represents the positive power supply voltage. Ex.[1006], Fig. 1; Ex.[1002], ¶¶173-182.

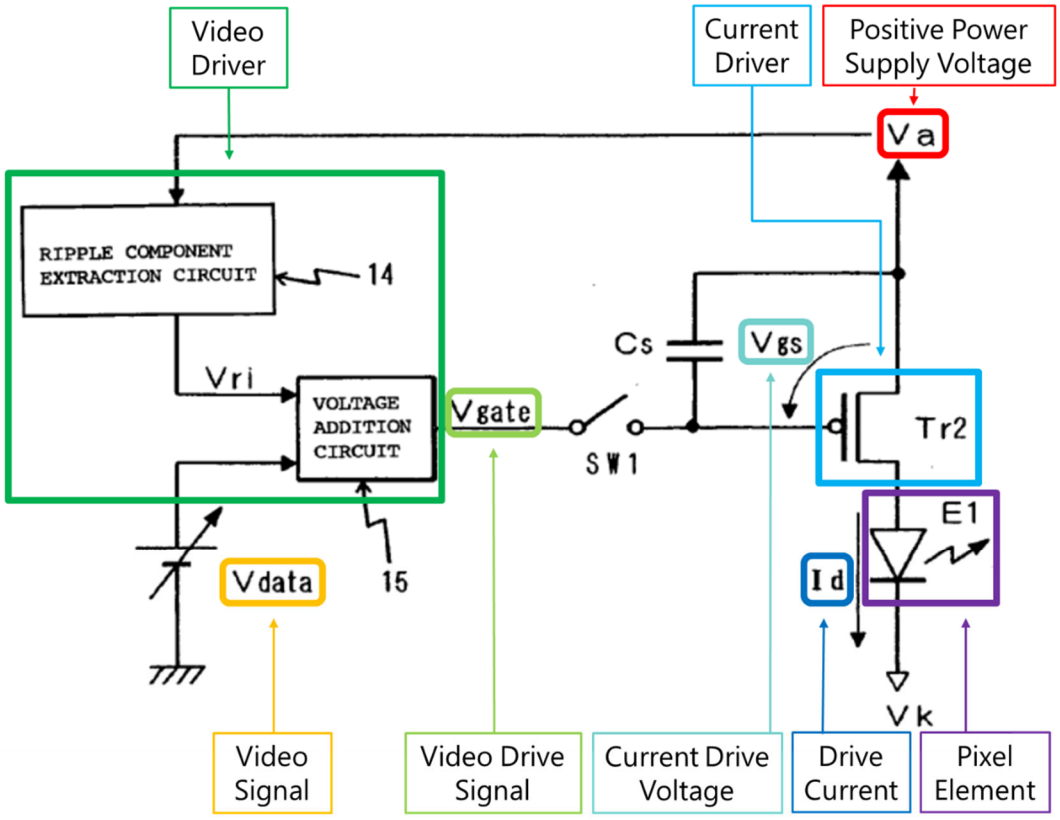


Ex.[1006], Fig. 1.

Generating Drive Signal Indicative of Video Signal and Referenced To Supply Voltage

Hayafuji generates a drive signal ($\mathbf{V_{gate}}$) meeting this requirement. *Hayafuji's* technique includes "ripple component supply means for supplying a ripple component having approximately the same phase and amplitude as those of a ripple component" supplied to the light emission drive transistor." Ex.[1006], ¶0029. In particular, " ripple component extraction circuit **14** extracts a ripple component [$\mathbf{V_{ri}}$] included in a drive voltage $\mathbf{V_a}$ generated by the above-described DC-DC converter, and a ripple component $\mathbf{V_{ri}}$ extracted by this ripple component extraction circuit **14** is supplied to one input terminal of the voltage addition circuit **15**. The data voltage $\mathbf{V_{data}}$ transmitted via the above-mentioned data line **B1** is input to the other input

terminal of the voltage addition circuit **15**." Ex.[1006], ¶0048. As explained previously, a POSA would recognize that "data voltage $\mathbf{V_{data}}$ transmitted via the above-mentioned data line **B1**" corresponds to the relevant portion of the claimed ***video signal*** destined for the pixel depicted in Figures 1, 2, and/or 6. Ex.[1002], ¶¶173-182.



Ex.[1006], Fig. 6 (annotated).

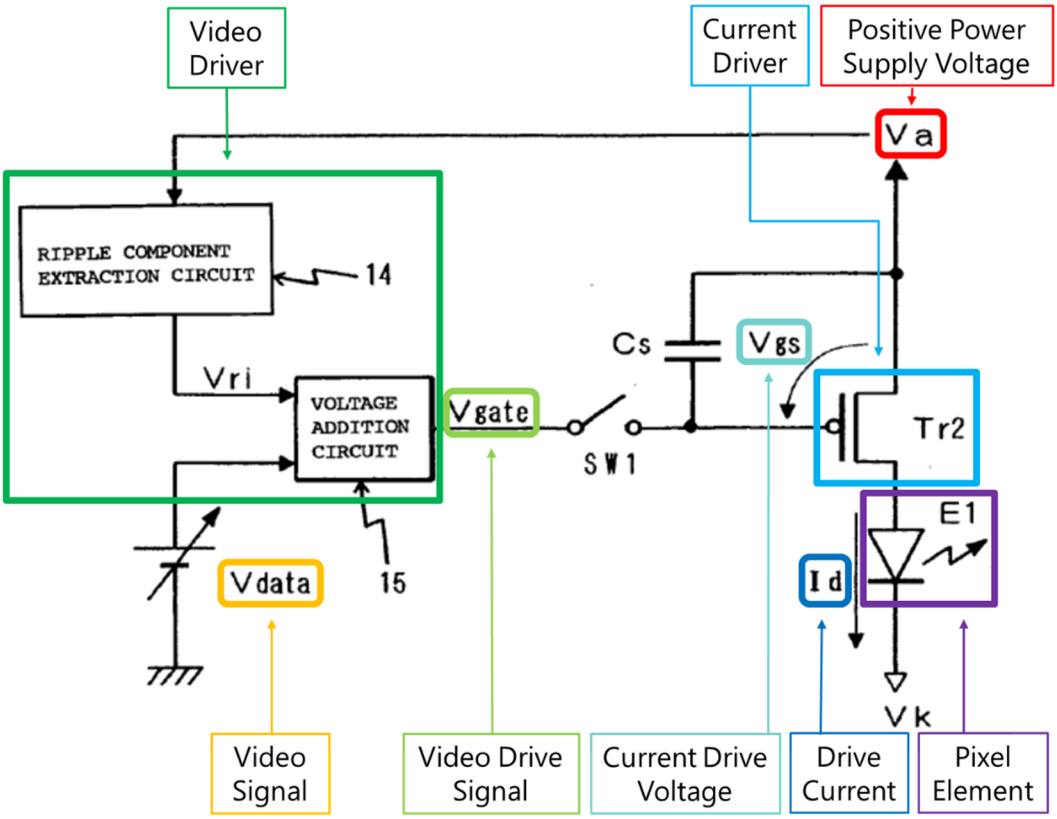
Hayafuji explains "in the voltage addition circuit **15**, treating the data voltage $\mathbf{V_{data}}$ as a base, the ripple component $\mathbf{V_{ri}}$ extracted by the ripple component extraction circuit **14** is added to the base. The output thereof as $\mathbf{V_{gate}}$… is supplied to the gate of a light emission drive transistor **Tr2**." Ex.[1006], ¶0049. Thus, because

the output of circuit 15 ($\mathbf{V_{gate}}$) is the sum of (1) the relevant portion of the video signal and (2) the ripple component of the supply voltage, $\mathbf{V_{gate}}$ is both indicative of the video signal and referenced to the supply voltage. Ex.[1002], ¶¶173-182.

Claim[1-B]

Current Driver Coupled to the OLED Pixel Element Receiving the Video Drive Signal and the Positive Power Supply and Providing a Drive Current to the OLED Pixel Element

As illustrated in Figure 6 (annotated) below, *Hayafuji* discloses ***a current driver*** (circuitry including light emission drive transistor **Tr2** (see light blue annotation in Figure 6 below)) ***coupled to at least one OLED pixel element*** (organic EL element **E1**)***, the current driver receiving the video drive signal*** (gate voltage $\mathbf{V_{gate}}$) ***and the positive power supply voltage*** (drive voltage $\mathbf{V_a}$) ***and providing a drive current*** (drain current $\mathbf{I_d}$) ***to the at least one OLED pixel element***. Ex.[1006], Fig. 6; Ex.[1002], ¶¶183-189.



Ex.[1006], Fig. 6 (annotated).

Hayafuji's text comports with Figure 6. In particular, it discusses a "light emission drive transistor **Tr2**" connected to the anode terminal of "organic EL element **E1**." Ex.[1006], ¶0008. "The source of the light emission drive transistor **Tr2**… receives supply of a drive power source $\mathbf{V_a}$." Ex.[1006], ¶0008. Moreover, "the gate voltage $\mathbf{V_{gate}}$ based on the video signal is supplied to the gate of the drive transistor **Tr2**." Ex.[1006], ¶¶0024, 0049. The text also discusses the "drain current $\mathbf{I_d}$ which drives and allows the organic EL element **E1** to emit light" and notes that the current is determined by the (gate-to-source voltage=$\mathbf{V_{gs}}$ of the transistor **Tr2**) between the drive voltage $\mathbf{V_a}$ supplied via the power line **P1** and the gate voltage of

the drive transistor **Tr2**."[9] Ex.[1006], ¶0021. The drive current $\mathbf{I_d}$ is discussed further below.

Claim[1-C]

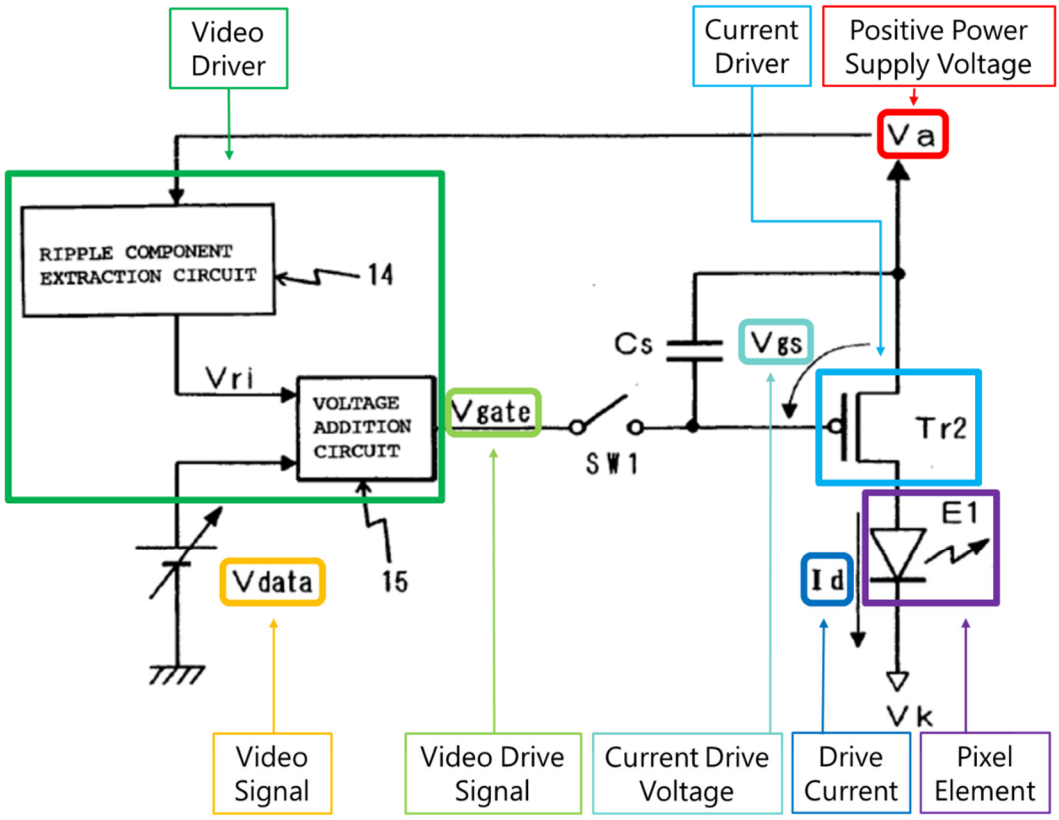
Current Drive Voltage being Indicative of the Video Signal

As explained above in Gr.3,Cl.[1-B], *Hayafuji's* drain ***current*** $\mathbf{I_d}$ is determined by the gate-to-source voltage $\mathbf{V_{gs}}$ of the transistor **Tr2**. Ex.[1006], ¶0021. $\mathbf{V_{gs}}$ therefore corresponds to the claimed "current drive voltage." Ex.[1002], ¶¶190-201.

As shown in Figure 6, gate-to-source voltage $\mathbf{V_{gs}}$ is the difference between supply voltage $\mathbf{V_a}$ and gate voltage $\mathbf{V_{gate}}$ ("$\mathbf{_{gate}}$" being the "$\mathbf{_g}$" in "$\mathbf{V_{gs}}$"). *Hayafuji* explains that "the gate voltage $\mathbf{V_{gate}}$ [is] based on the video signal." Ex.[1006], ¶¶0024, 0049. In particular, as previously explained in Gr.3,Cl.[1-B], $\mathbf{V_{gate}}$ is the sum of the relevant portion of the video signal ($\mathbf{V_{data}}$) and the ripple component of the power supply voltage. Ex.[1006], ¶0049. Thus, *Hayafuji's* current drive voltage

[9] *Hayafuji* calls this an "error" signal, which a POSA would understand means the "difference" between drive voltage $\mathbf{V_a}$ and the gate voltage of drive transistor **Tr2**. This is apparent from the context, as well as the use of "error" in mathematics to refer to a difference between measurements. Ex. [1002], ¶¶187-188.

$\mathbf{V_{gs}}$ is indicative of the video signal ($\mathbf{V_{data}}$) and is supplied to transistor **Tr2** to create a corresponding drive current. Ex.[1006], Fig. 6; Ex.[1002], ¶¶190-201.



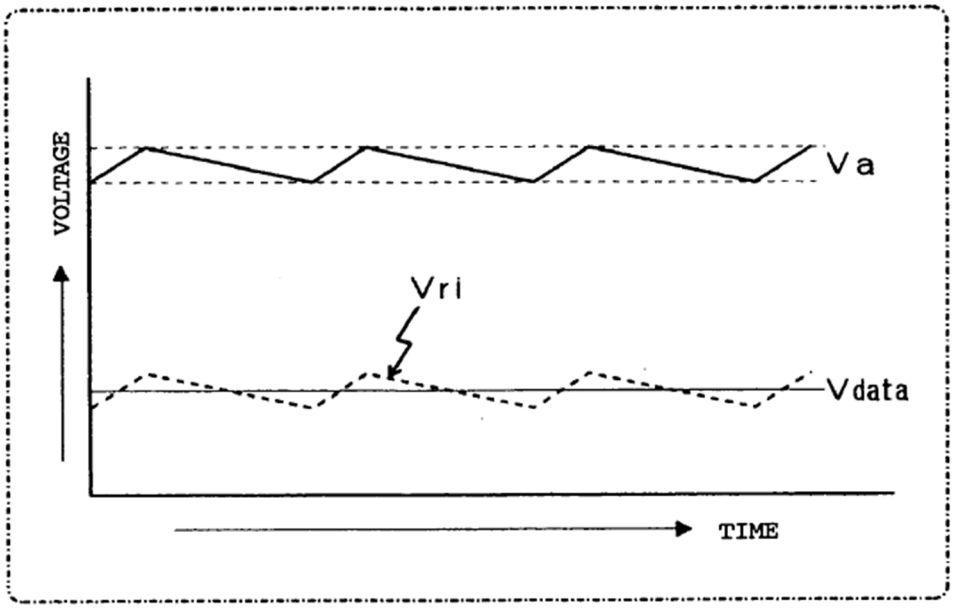
Ex.[1006], Fig. 6 (annotated).

Current Drive Voltage…Independent of the…Power Supply Voltage

As explained above, this limitation means that the drive voltage is independent of variations in the power supply voltage, so that such noise or DC drifts do not propagate to the LED drive current. *See* §VI. *Hayafuji* achieves this. *Hayafuji* discloses a "drive device and a drive method of a light emitting display panel in which ***deterioration of the display quality of an image caused by a ripple***

component generated in a power supply circuit… can be effectively reduced." Ex.[1006], ¶0028.

In particular, *Hayafuji* explains that power supply voltage $\mathbf{V_a}$ may have a variable "ripple" component, shown as a dotted line envelope in Figure 8A. Ex.[1006], Fig. 8A, ¶¶0052-0055.



Ex.[1006], Fig. 8A.

Thus, a POSA would understand $\mathbf{V_a}$ is composed of DC power $\mathbf{V_{dc}}$+$\mathbf{V_{ri}}$. Ex.[1002], ¶¶190-201. The impact of *Hayafui's* voltage addition circuit therefore is to generate output voltage $\mathbf{V_{gate}}$=$\mathbf{V_{data}}$+$\mathbf{V_{ri}}$. The resulting current drive voltage is therefore: $\mathbf{V_{gs}}$=$\mathbf{V_{dc}}$+$\mathbf{V_{ri}}$–$\mathbf{V_{data}}$–$\mathbf{V_{ri}}$, which simplifies to $\mathbf{V_{gs}}$=$\mathbf{V_{dc}}$–$\mathbf{V_{data}}$, removing the variations ($\mathbf{V_{ri}}$) in power supply voltage from the current drive voltage. Ex.[1002],

¶¶190-201; Ex.[1006], ¶¶0053-0054. Thus, *Hayafuji*'s current drive voltage satisfies this limitation. Ex.[1002], ¶¶190-201.

Drive Current being Proportional to a Current Drive Voltage

Hayafuji discloses a driver voltage across the terminals of "a P-channel type light emission drive transistor **Tr2**," resulting in "current $\mathbf{I_d}$ which drives and allows the organic EL element **E1** to emit light…". Ex.[1006], ¶¶0007, 0021. *Hayafui* explains the current is "determined by the error (gate-to-source voltage=$\mathbf{V_{gs}}$ of the transistor **Tr2**) between the drive voltage $\mathbf{V_a}$ supplied via the power line **P1** and the gate voltage of the drive transistor **Tr2**." *Id.* Because the drive current is "determined by" the current drive voltage (gate to source voltage $\mathbf{V_{gs}}$), that current is proportional to the current drive voltage. Ex.[1002], ¶¶190-201.

Moreover, *Hayafuji's* drive transistor **Tr2** and the '521 Patent's transistor M1 are both P-channel MOSFETs, are would both operate in the same manner based on the well-known principles of P-Channel MOSFETs. Ex.[1001], 2:31-36, Ex.[1002], ¶¶190-201. Therefore, to the same extent that the'521 Patent's drive current is "proportional" to the current drive voltage across M1, *Hayafuji's* drain current $\mathbf{I_d}$ is also through P-channel MOSFET **Tr2** would similarly be "***proportional***" to *Hayafuji's* gate-to-source voltage $\mathbf{V_{gs}}$.[10] Ex.[1002], ¶¶190-201.

[10] *See supra*, Fn.7 regarding "proportional."

2. *Claim 2*

Video Drive Signal is Indicative of the Sum…Between The Positive Power Supply Voltage and the Video Signal

Hayafuji discloses ***the video drive signal*** (gate voltage $\mathbf{V_{gate}}$) is indicative of ***"the sum …between the positive power supply voltage*** [drive voltage $\mathbf{V_a}$] ***and the video signal*** [data voltage $\mathbf{V_{data}}$]". Ex.[1006], Fig. 8 (annotated); Ex.[1002], ¶¶202-209.

In particular, *Hayafuji* discloses "The ripple component extraction circuit **14** extracts a ripple component [labelled $\mathbf{V_{ri}}$ in the Figures] included in a drive voltage $\mathbf{V_a}$ generated by the above-described DC-DC converter, and a ripple component $\mathbf{V_{ri}}$ extracted by this ripple component extraction circuit **14** is supplied to one input terminal of the voltage addition circuit **15**. The data voltage $\mathbf{V_{data}}$ transmitted via the above-mentioned data line **B1** is input to the other input terminal of the voltage addition circuit **15**." Ex.[1006], ¶0048.

Hayafuji continues "Accordingly, in the voltage addition circuit **15**, treating the data voltage $\mathbf{V_{data}}$ as a base, the ripple component $\mathbf{V_{ri}}$ extracted by the ripple component extraction circuit **14** is added to the base. The output thereof as $\mathbf{V_{gate}}$… is supplied to the gate of a light emission drive transistor **Tr2**." Ex.[1006], ¶0049.

Thus, a POSA would recognize that *Hayafuji* teaches: (1) that the drive voltage $\mathbf{V_a}$ is the sum of a constant DC output voltage component (herein "$\mathbf{V_{dc}}$

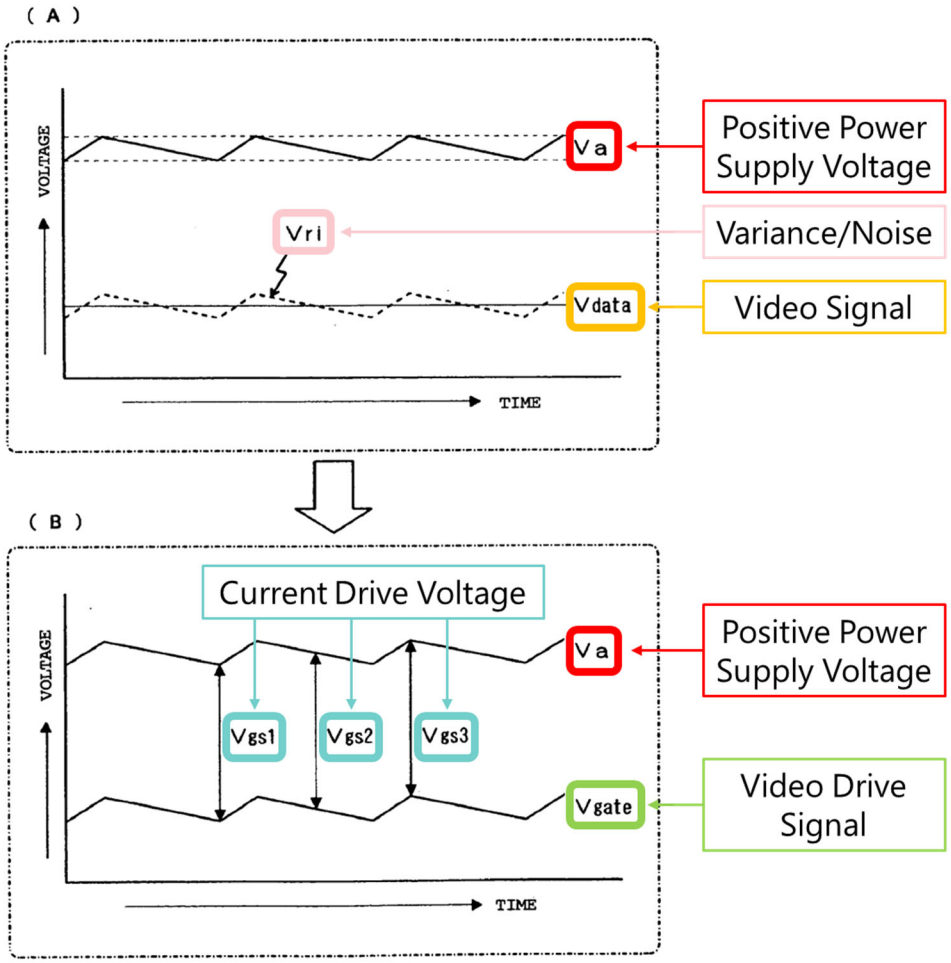
(constant)") of the drive voltage $\mathbf{V_a}$ and the extracted ripple component $\mathbf{V_{ri}}$; (2) that the gate voltage $\mathbf{V_{gate}}$ is the sum of the data voltage $\mathbf{V_{data}}$ and the extracted ripple component $\mathbf{V_{ri}}$; and consequently, (3) that the gate voltage $\mathbf{V_{gate}}$ is indicative of the sum of or the difference between the drive voltage $\mathbf{V_a}$ and the data voltage $\mathbf{V_{data}}$:

(1) $\mathbf{V_a}=\mathbf{V_{dc}}+\mathbf{V_{ri}}$

(2) $\mathbf{V_{gate}}=\mathbf{V_{data}}+\mathbf{V_{ri}}$

(3) $\mathbf{V_{gate}}=\mathbf{V_{data}}+\mathbf{V_a}-\mathbf{V_{dc}}$ (constant)

Ex.[1002], ¶¶202-209.



Ex.[1006], Fig. 8 (annotated).

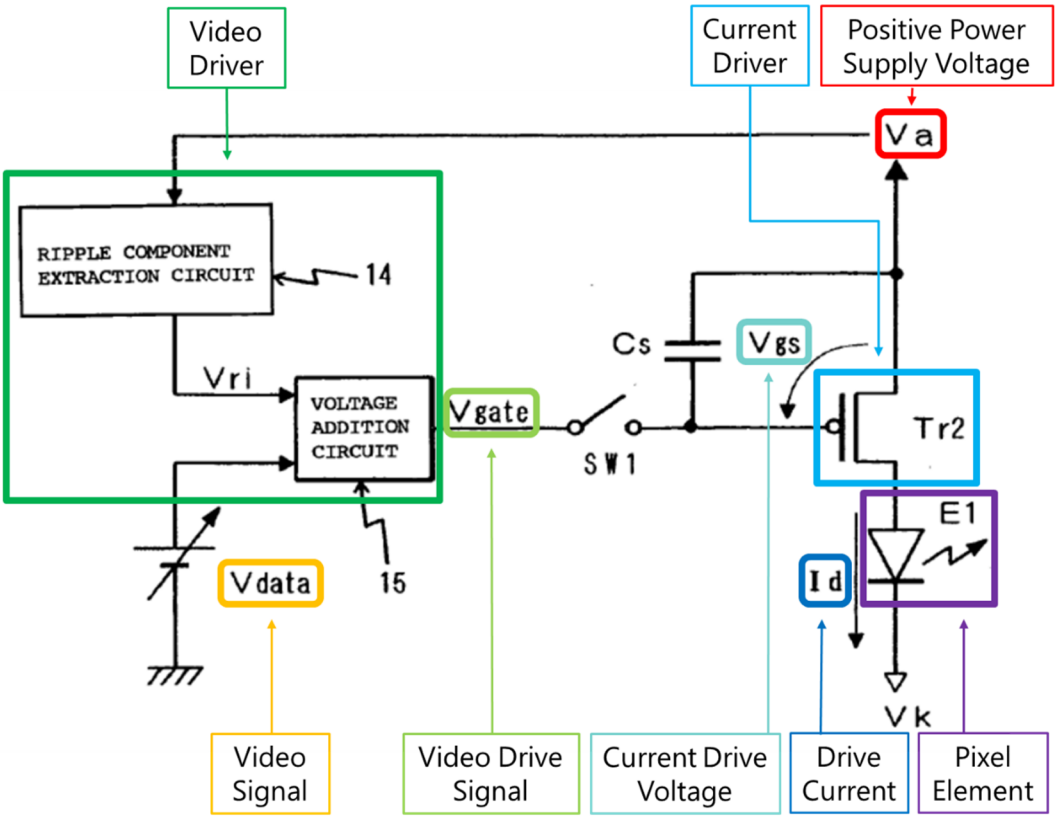
As equation (3) above shows, the drive voltage contains a DC voltage offset, but varies directly with the term ($\mathbf{V_{data}}$+$\mathbf{V_a}$) and is therefore "indicative" of that term, as the claim recites. Ex.[1002], ¶¶202-209.

Current Drive Voltage**…**Indicative of the Difference between the Positive Power Supply Voltage and the Video Drive Signal,

As discussed in Gr.3, Cl.[1-C], a POSA would recognize that *Hayafuji* teaches that the current drive voltage (gate-to-source voltage=$\mathbf{V_{gs}}$) is the difference between the power supply (drive voltage $\mathbf{V_a}$ (corresponding to the '521 Patent's VDD)) and the video drive signal (gate voltage $\mathbf{V_{gate}}$ (corresponding to the '521 Patent's gate voltage v(t)):

(4) $\mathbf{V_{gs}}=\mathbf{V_a}-\mathbf{V_{gate}}$

Ex.[1002], ¶¶202-209.



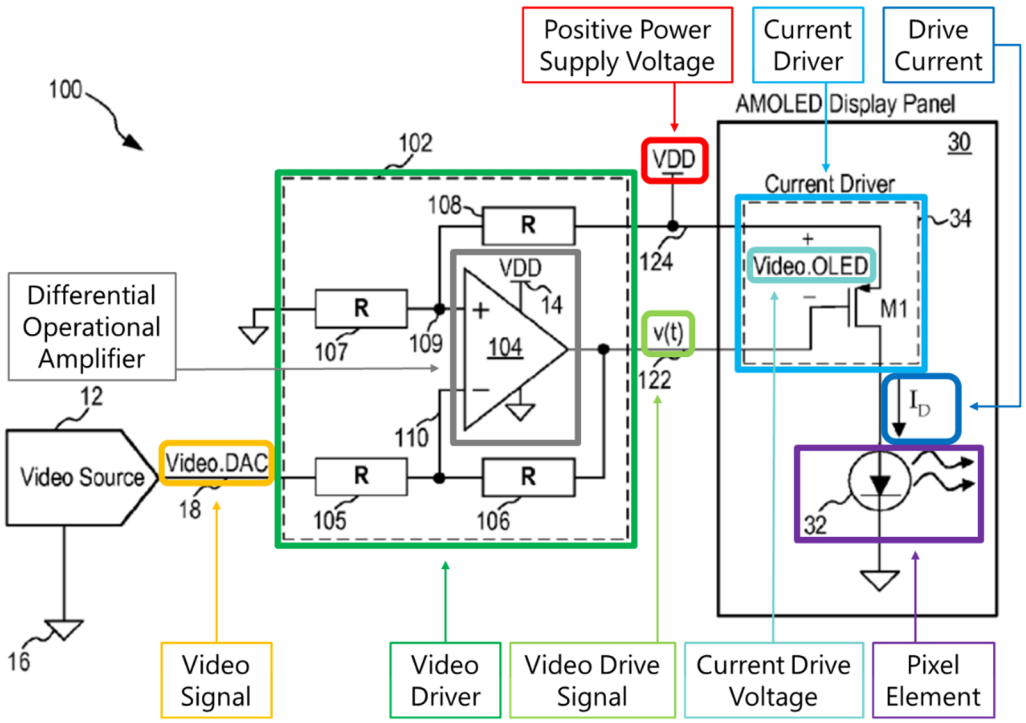
Ex.[1006], Fig. 6 (annotated).

C. Ground 4: Claims 1-3 and 5 are Obvious in View of *Hayafuji* and the knowledge of a POSA

1. *Claims 1-3*

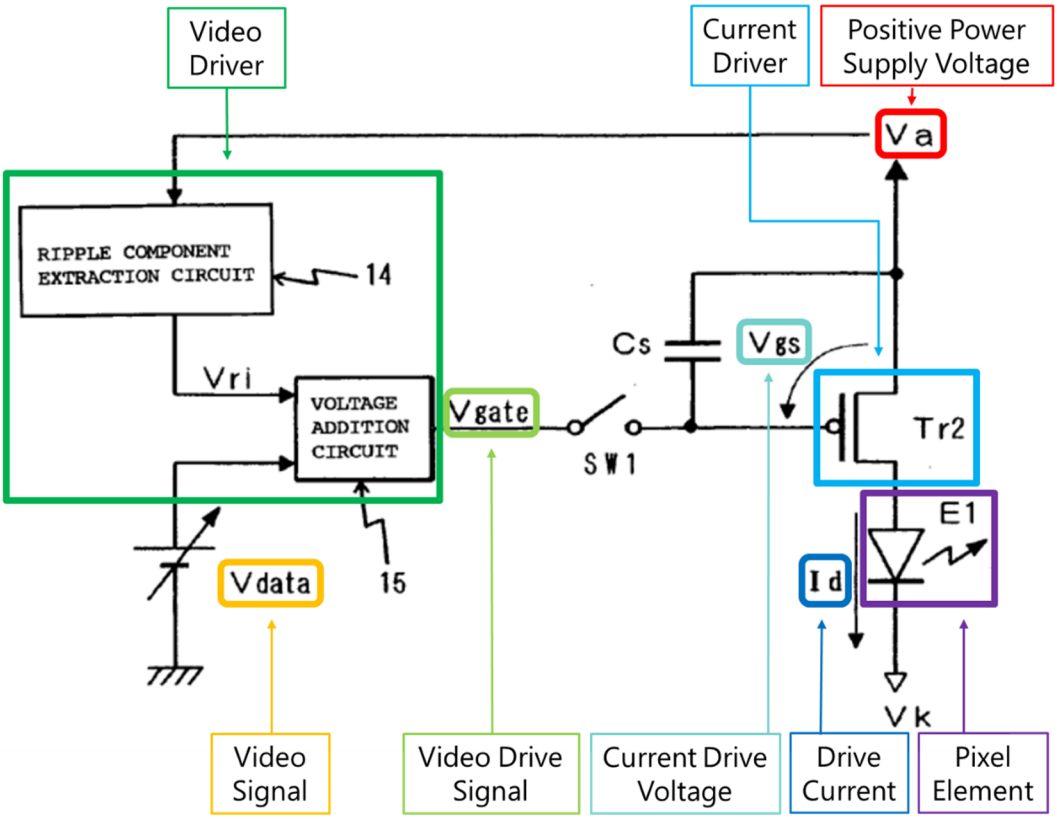
Video Drive Signal being the Difference between the Positive Power Supply Voltage and the Video Drive Signal

Claim 3 corresponds to the '521 Patent's first embodiment shown in Figure 2: "video driver 102 is implemented using a differential instrumentation amplifier circuit to re-reference the video drive signal v(t) to the positive power supply voltage VDD." *See* Ex.[1001], 4:7-37, 4:53-65, Fig. 2; Ex.[1002], ¶210.

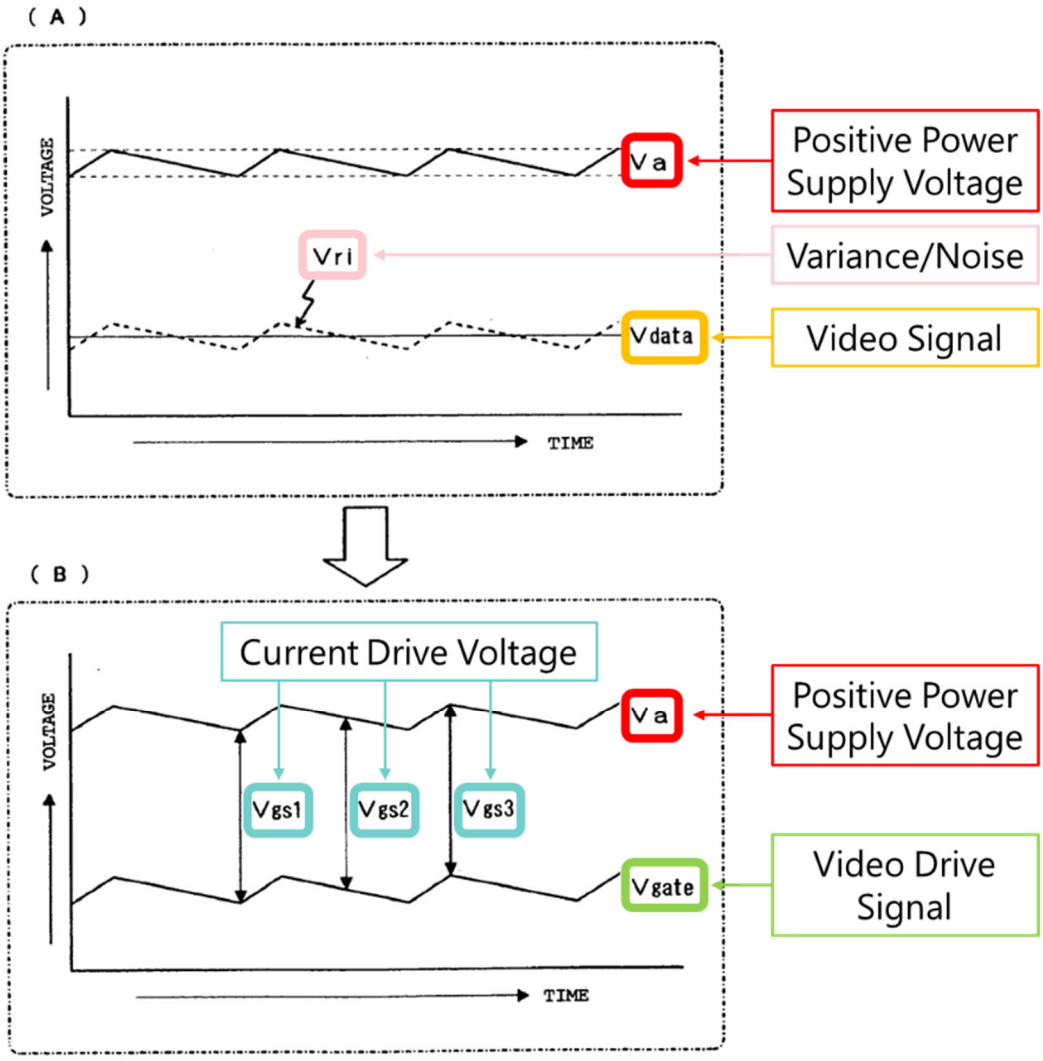


Ex.[1001], Fig. 2 (annotated).

As discussed above, *Hayafuji* discloses the elements of Claims 1 and 2. Ex.[1006], Figs. 6, 8; Ex.[1002], ¶¶211-212. As discussed below, the elements of Claims 1 and 2 are also satisfied by the following modification. Ex.[1002], ¶¶213-234.



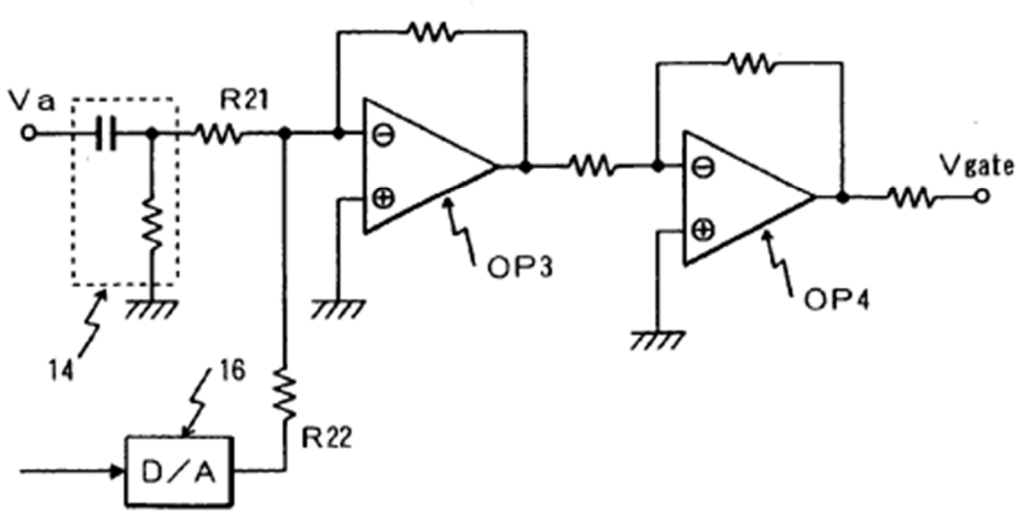
Ex.[1006], Fig. 6 (annotated).



Ex.[1006], Fig. 8 (annotated).

Hayafuji provides, in the Figure 7 exemplary implementation, details of "circuits employed in the structure shown in Fig. 6" that generate the $\mathbf{V_{gate}}$ signal. Ex.[1006], ¶¶0037, 0050-0051, Fig. 7.

FIG.7

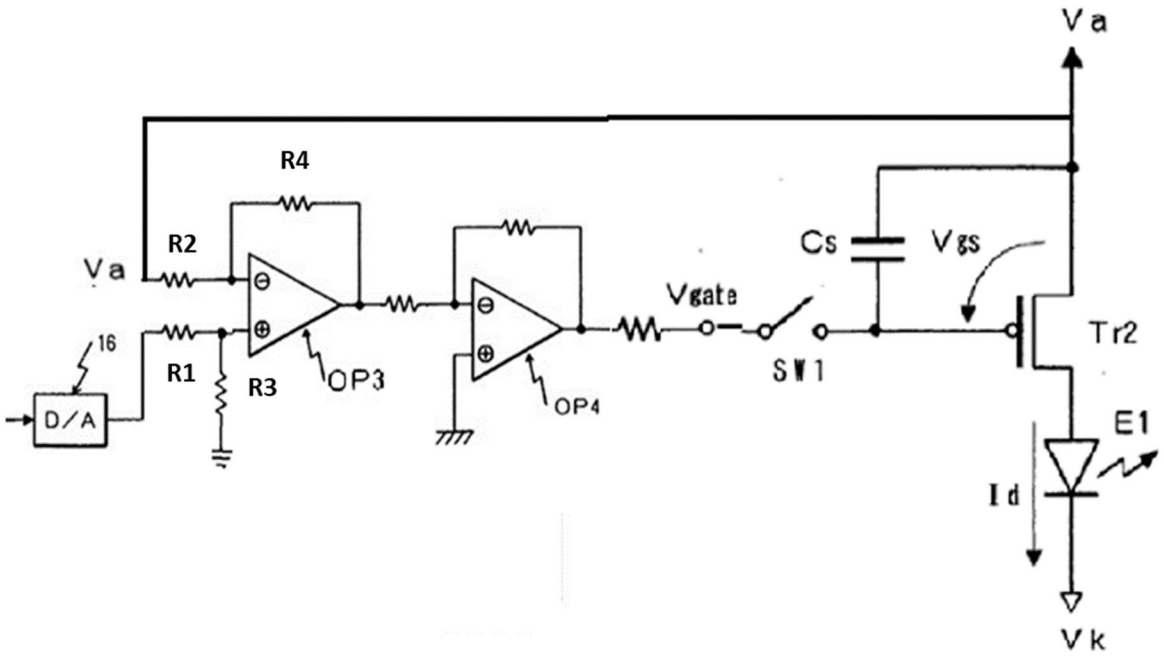


Ex.[1006], Fig. 7.

A POSA also would find it obvious to modify the system disclosed in *Hayafuji* such that ***video drive signal*** (gate voltage $\mathbf{V_{gate}}$) is configured such that ***video drive signal*** (gate voltage $\mathbf{V_{gate}}$) is output as ***the difference between the positive power supply voltage*** (drive voltage $\mathbf{V_a}$) ***and the video signal*** (data voltage $\mathbf{V_{data}}$). Ex.[1002], ¶¶213-234. Specifically, a POSA would modify the Figure 7 configuration by connecting the ***positive power supply voltage*** (drive voltage $\mathbf{V_a}$) to the inverting input of operational amplifier **OP3** rather than the non-inverting input. Ex.[1002], ¶¶213-234. This would be an obvious design choice and would simplify material needs and cost because as modified, the capacitor of the high pass filter of

the disclosed ripple component extraction circuit **14** would be unnecessary. Ex.[1002], ¶¶213-234.

This modification is illustrated in Figures 6-7 (combined/modified) below. Ex.[1006], Figs. 6, 7. Ex.[1002], ¶¶213-234.



Ex.[1006], Figs. 6, 7 (combined, modified).

As modified, drive voltage $\mathbf{V_a}$ (and accompanying voltage dividing resistors) are coupled to the negative terminal such that the output of the operational amplifier **OP3** would be the desired result of a control signal based on the data voltage $\mathbf{V_{data}}$ entering via **R1**, referenced against the drive voltage $\mathbf{V_a}$. Ex.[1002], ¶¶213-234.

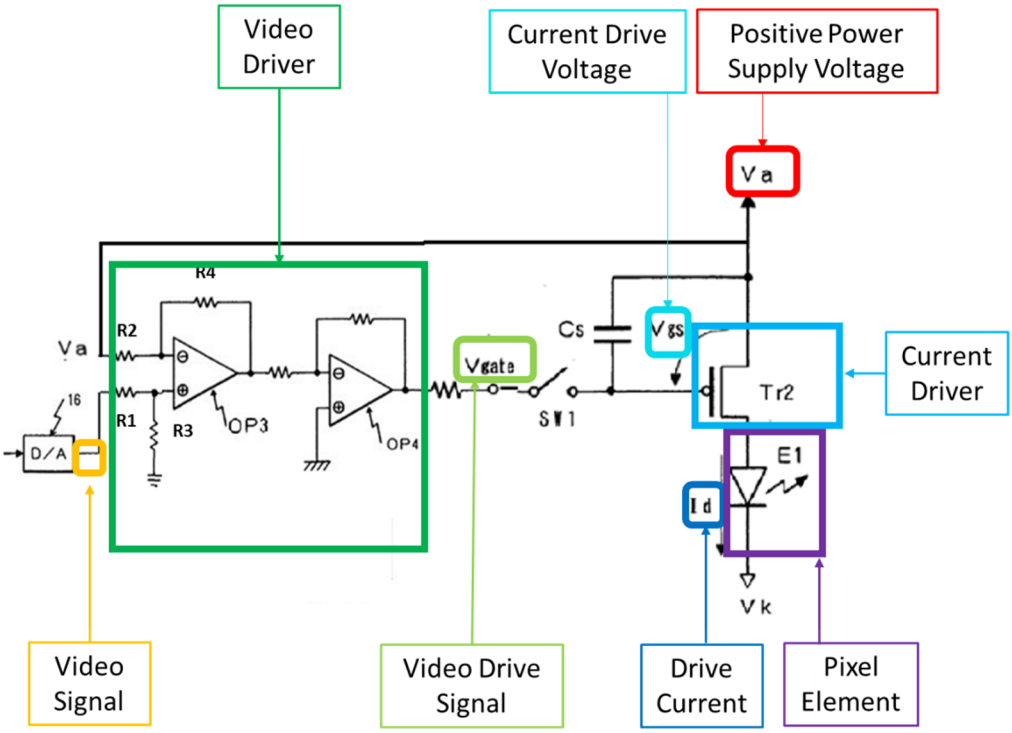
As noted, a POSA would be motivated to make this modification at least because it is a simpler design that eliminates the need for and the cost to include the

additional ripple component extraction circuit **14** module. Ex.[1002], ¶¶213-234. A POSA would also be motivated to make this modification because it was well-known that in conventional differential instrumentation amplifier circuits, the positive input terminal is the reference voltage (often ground) to which the negative terminal voltage is compared. Ex.[1002], ¶¶213-234. A POSA would further be motivated to make this obvious modification because it is merely a trivial design change that would also accomplish the stated purpose of *Hayafuji*: "it is an object of the present invention to provide a drive device and a drive method of a light emitting display panel in which deterioration of the display quality of an image caused by a ripple component generated in a power supply circuit." Ex.[1006], ¶0028; Ex.[1002], ¶¶213-234. Moreover, a POSA would have been motivated to make this modification because it would provide improved immunity to power source noise. In particular, the filter-design approach in Figure 6 of Hayafuji can only eliminate power supply noise in a range of frequencies determined by the frequency response of Hayafuji's filter. The modified design removes this limitation and would allow rejection of other power supply noise, such as drift. Ex.[1002], ¶ 224-226.

Further, a POSA would have had a reasonable expectation of success when making this modification because implementing a differential amplifier circuit in this manner is a well-known and fundamental op amp configuration. Ex.[1002], ¶¶213-234; *see also*, Ex. [1010], pg. 181.

Differential Instrumentation Amplifier Circuit

A POSA would also recognize (especially in this configuration) that the operational amplifier **OP3** as disclosed in *Hayafuji* corresponds to the claimed ***differential instrumentation amplifier circuit***. Ex.[1002], ¶¶213-234; Ex.[1001], 4:34-41. Ex.[1002], ¶¶213-234. Therefore, consistent with the above discussion, in the modified/annotated circuit below, ***the video driver*** (circuitry in green Video Driver annotation below) ***comprises a differential instrumentation amplifier circuit*** (operational amplifier **OP3**) ***for providing the video drive signal*** (gate voltage $\mathbf{V_{gate}}$, prior to any amplification by **OP4**) ***being the difference between the positive power supply voltage*** (drive voltage $\mathbf{V_a}$) ***and the video signal video signal*** (data voltage $\mathbf{V_{data}}$). Ex.[1006], Figs. 6, 7. Ex.[1002], ¶¶213-234.



Ex.[1006], Figs. 6, 7 (combined, modified, annotated).

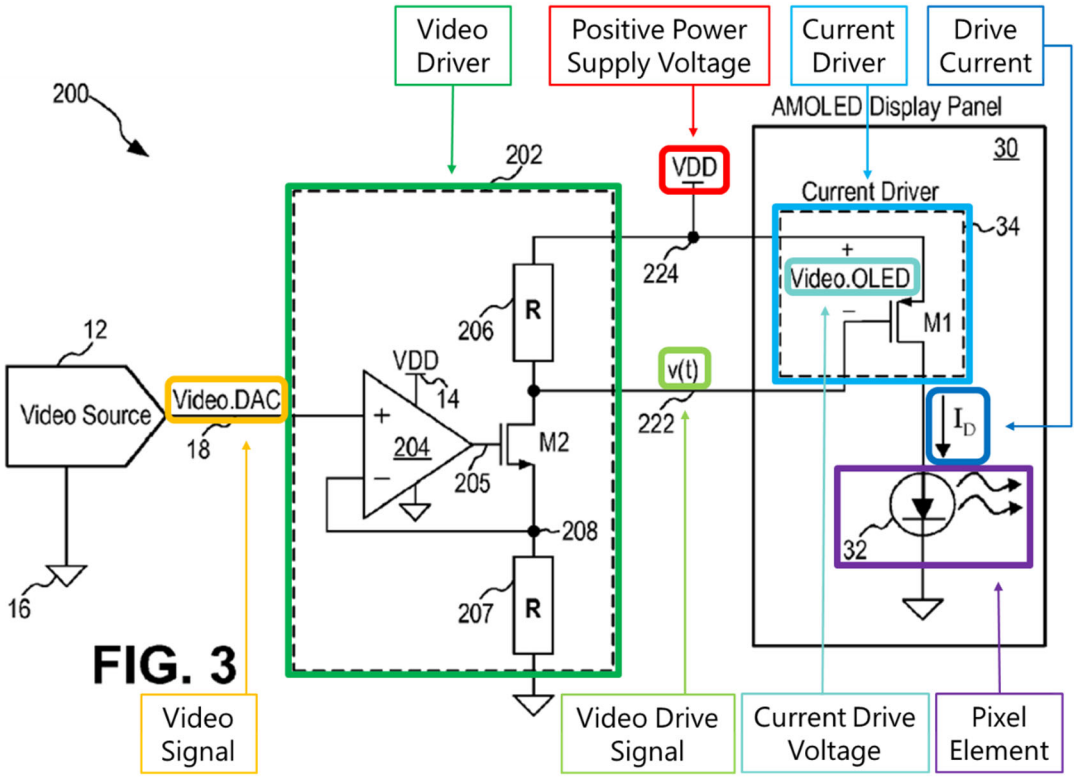
Moreover, the elements of Claim 1 would still be met by the modified circuit. As discussed in greater detail in Ex.[1002], Gr.4,Cl.[3], a POSA would recognize that this modification to *Hayafuji*'s circuitry merely changes op amp OP3 from a summing amplifier with a frequency filter to a differential amplifier. The video drive signal $\mathbf{V_{gate}}$ as modified would be the difference between positive power supply $\mathbf{V_a}$ and video signal $\mathbf{V_{data}}$, ($\mathbf{V_{gate}} = \mathbf{V_a} - \mathbf{V_{data}}$) and therefore, $\mathbf{V_{gate}}$ is still "referenced to" the Positive Power Supply $\mathbf{V_a}$, remains indicative of the relevant portion of the video signal, and independence of any variation in the power supply voltage is maintained because the drive voltage is equal to the data voltage, without dependence on the power supply voltage (i.e. $\mathbf{V_{gs}} = \mathbf{V_{data}}$) Ex.[1002], ¶¶213-234. Accordingly, the modified circuit still satisfies the claim limitations of Claims 1 and 2 of the '521 Patent as well as Claim 3. *Id.* A POSA would further recognize that, because the portion of *Hayafuji* corresponding to the current driver remains unchanged, that the drive current $\mathbf{I_d}$ is still proportional to the video drive signal $\mathbf{V_{gate}}$. Ex.[1002], ¶¶213-234.

2. *Claim 5*

Video Driver Comprising a Current Mode Isolator Circuit

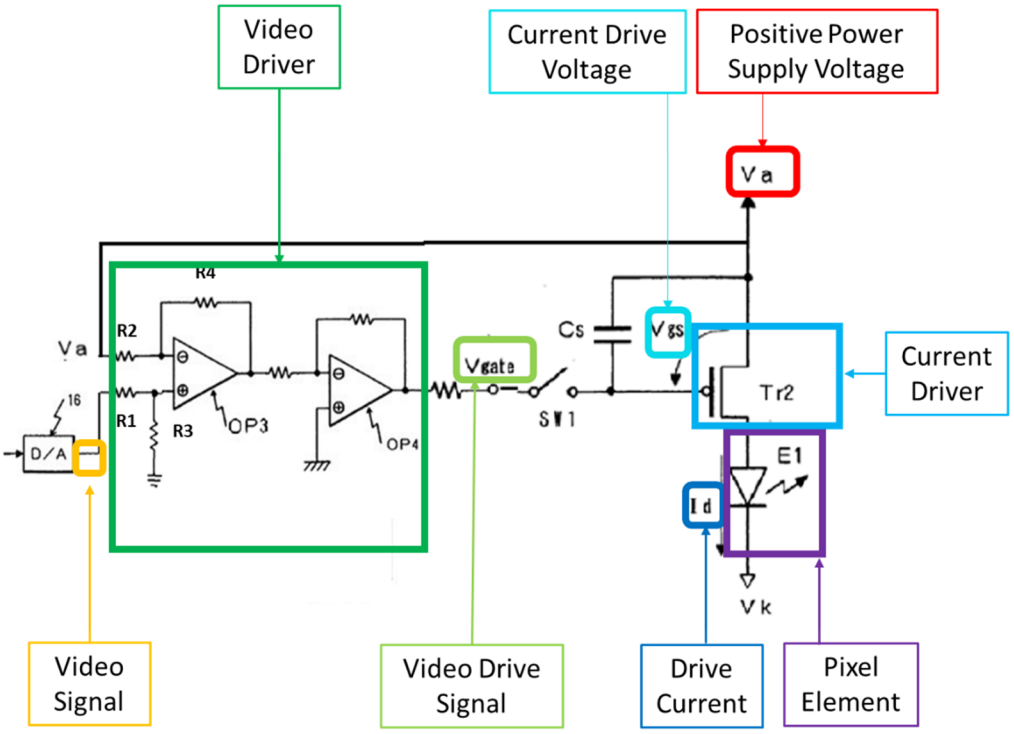
In the '521 Patent, Claim 5 corresponds to the '521 Patent's second embodiment: "FIG. 3 is a schematic diagram of a video driver for an AMOLED

display system according to a second embodiment of the present invention.… In the present embodiment, video driver 202 is implemented as a current mode isolator circuit." Ex.[1001], 5:38-47, Fig. 3 (annotated); Ex.[1002], ¶235.



Ex.[1001], Fig. 3 (annotated).

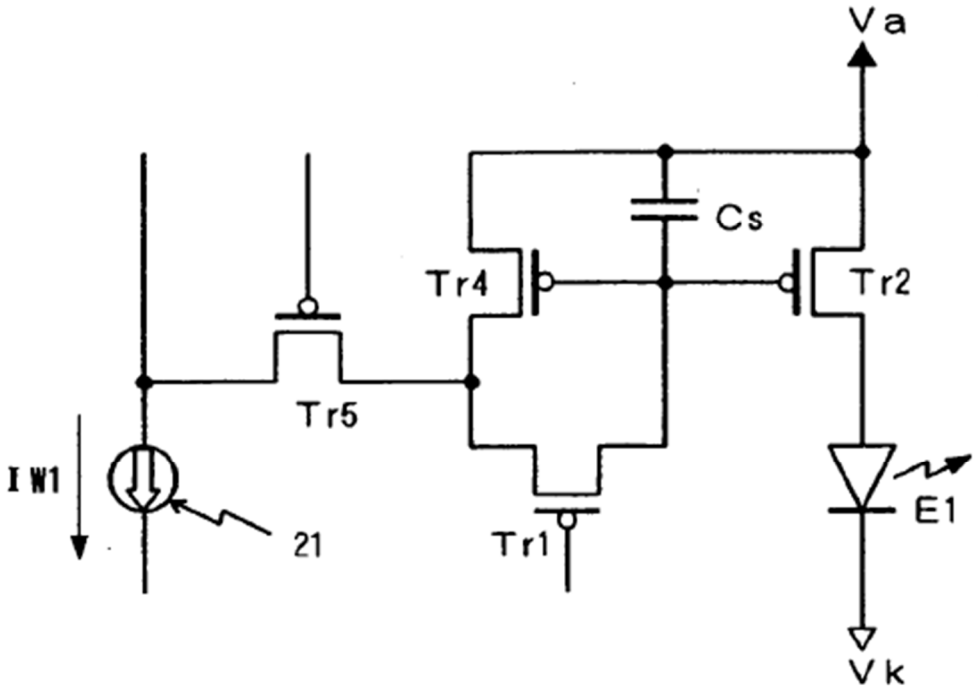
As discussed above, *Hayafuji* discloses the elements of Claims 1 and 2. Ex.[1006], Figs. 6, 8; Ex.[1002], ¶236. Additionally, as explained with respect to Figure 3, a POSA would have been motivated to modify the *Hayafuji* circuit as shown below. Ex.[1006], Figs. 6, 7; Ex.[1002], ¶236; *see* Gr.3,Cls.[1-C],[2]



Ex.[1006], Figs. 6, 7 (combined, modified, annotated).

For the reasons discussed below, a POSA would also recognize that *Hayafuji* discloses ***the video driver comprising a current mode isolator circuit***.

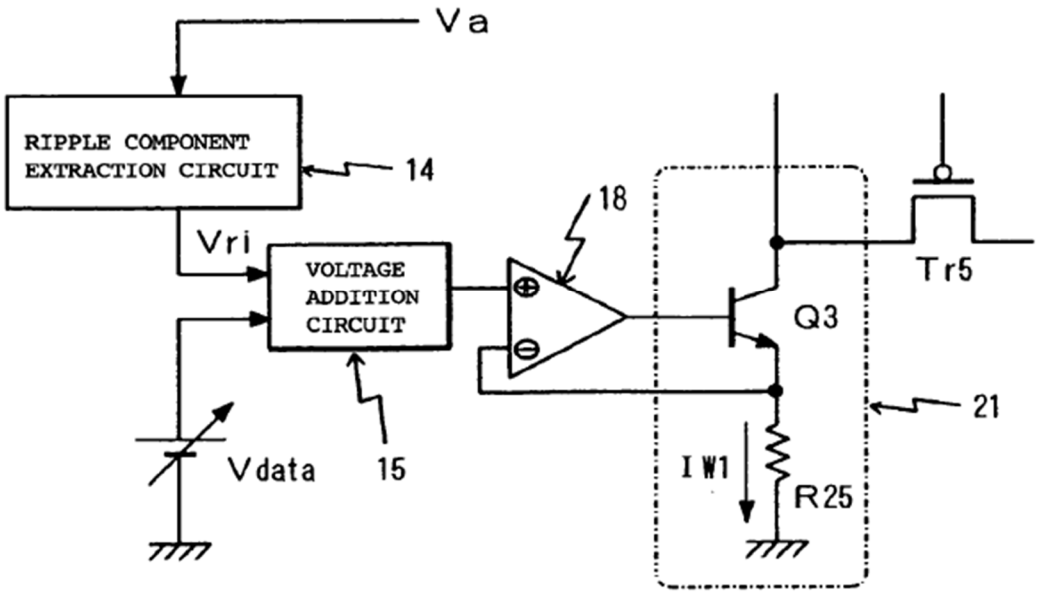
Hayafuji's Figure 9 shows "a current mirror drive method" including p-channel transistor **Tr2** and "mirror operation transistor **Tr4"** arranged symmetrically with common gate connection, and a charge-holding capacitor **Cs** is connected between the sources and the gates thereof. "The drive voltage $\mathbf{V_a}$ is supplied to the sources of the [sic] both transistors **Tr2**, **Tr4**." Ex.[1006], ¶0056, Fig. 9.



Ex.[1006], Fig. 9.

Hayafuji explains that operation of "scan selection transistor **Tr1**" causes transistors **Tr2**, **Tr4** to "function as a current mirror circuit". Ex.[1006], ¶0057. Thus, a path between "write current source **21"** is created via transistors **Tr4**, **Tr5** allowing current corresponding to current **IW1** flowing in the power source **21** to be supplied to the EL LED element **E1**. Ex.[1006], ¶0058. In particular, a predetermined current (=**IW1**) creates an electrical charge accumulation in capacitor **Cs**, which results in drive current through the EL LED element **E1**. Ex.[1006], ¶0058, Ex.[1002], ¶¶237-261.

Details of write current source **21** in Figure 9 above are shown surrounded by dotted lines in *Hayafuji's* Figure 10. Ex.[1006], ¶0059, Fig. 10.



Ex.[1006], Fig. 10.

Hayafuji explains that "write current source **21** operates such that the current value of the ripple component changes every moment by the ripple component included in the drive voltage $\mathbf{V_a}$." Ex.[1006], ¶0060.

The result of this is, as explained by *Hayafuji* is "a voltage value corresponding to the data voltage $\mathbf{V_{data}}$ …is written in the charge-holding capacitor **Cs** in the…current mirror drive method shown in FIG. 9 without being influenced by the ripple component included in the drive voltage $\mathbf{V_a}$" creating a LED drive signal independent from variations in the power supply. Ex.[1006], ¶0061.

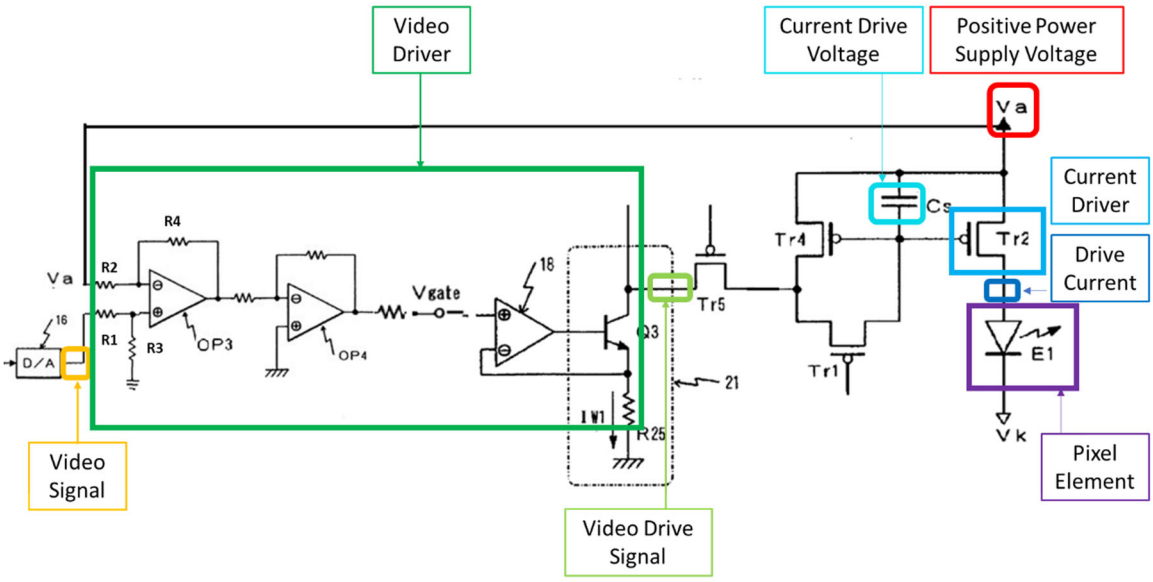
A POSA would understand that *Hayafuji*'s video driver discussed above is a 'current-mode' circuit because the video driver (circuitry in green Video Driver annotation below) generates and provides a control current to the current driver

(circuitry in blue Current Driver annotation below). Ex.[1002], ¶¶237-261. Specifically, a POSA would recognize this because transistor **Q3** generates control current **IW1**, which controls current through transistor **Tr4**, which is configured together with transistor **Tr2** as a current mirror, and thereby controls drive current **Id** through pixel element **32**. Ex.[1002], ¶¶237-261.

Moreover, a POSA would also recognize that *Hayafuji*'s video driver is an isolator for control current **IW1**. Ex.[1002], ¶¶237-261. A POSA would understand, based on the specification of the '521 Patent, that the claimed "***isolator***" functionality is describing isolating the control current from being influenced by variations in the power supply: "**By using video driver 202 incorporating a current mode isolator**, the video drive signal v(t) is made referenced to the power supply voltage VDD so that the current drive voltage signal **Video.OLED is made independent of the power supply voltage VDD**. Ex.[1002], ¶¶237-261. Variations in the power supply voltage VDD will no longer adversely affect the AMOLED display." Ex.[1001], 6:1-7. As noted above, *Hayafuji*'s current mode technique expressly discusses providing a drive signal to the LED "without being influenced by the ripple component included in the drive voltage $\mathbf{V_a}$." Ex.[1006], ¶0061. As such, a POSA would recognize that *Hayafuji*'s circuitry including transistor **Q3** is a ***current mode isolator circuit***. Ex.[1002], ¶¶237-261.

As discussed in greater detail in Ex.[1002], Gr.4,Cl.[3], a POSA would be motivated to use this current drive technique in conjunction with the configuration discussed in Gr.4,Cl.[3] at least because it allows for improved compensation to transistor mobility and threshold variations, and therefore results in better display performance. Ex.[1002], ¶¶237-261. Further, a POSA would have a reasonable expectation of success because *Hayafuji* discloses adapting from a voltage programmed pixel to a current programmed pixel while still reducing the effect of power supply ripple. Ex.[1002], ¶¶237-261.

Therefore, consistent with the Gr.4,Cl.[3] analysis, and Figures 6, 9, and 10 (combined/modified/annotated) below, a POSA would find obvious, in view of *Hayafuji*, ***the video driver comprises a current mode isolator circuit*** (circuitry including transistor **Q3**) ***for providing the video drive signal*** (gate voltage $\mathbf{V_{gate}}$ at transistors **Tr2** and **Tr4** driven by control current **Iw1**) ***being the difference between the positive power supply voltage*** (drive voltage $\mathbf{V_a}$) ***and the video signal*** (data voltage $\mathbf{V_{data}}$). Ex.[1006], FIGs. 6, 9, 10; Ex.[1002], ¶¶237-261.

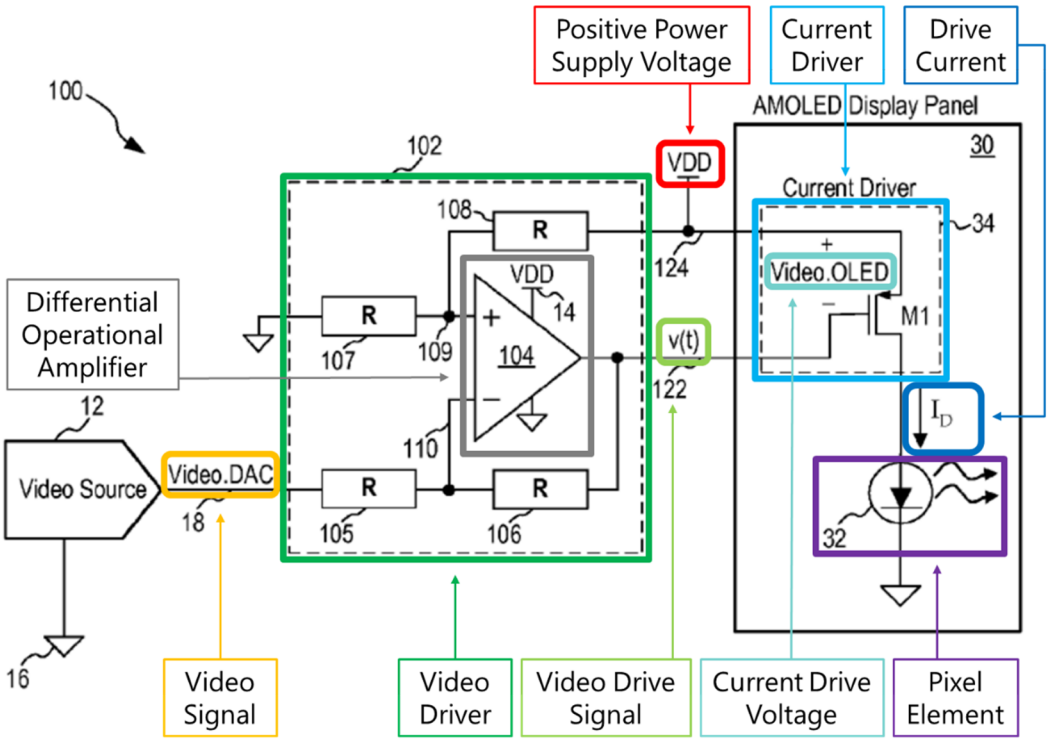


Ex.[1006], Figs. 6, 9, 10 (combined, modified, annotated).

D. Ground 5: Claims 1-4 are Obvious in View of *Steer* and the knowledge of a POSA

1. *Claim 1*

Figure 2 illustrating the first embodiment of the ’521 Patent is shown below. As discussed below, *Steer* discloses a substantially similar structure. Ex.[1001], Fig. 2.



Ex.[1001], Fig. 2 (annotated).

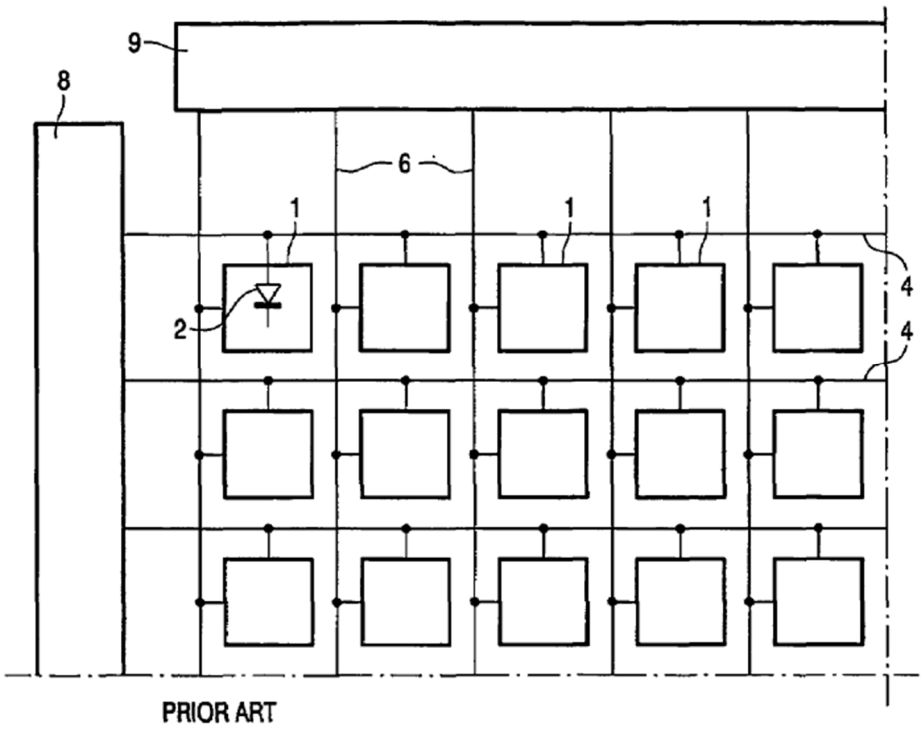
Claim[1-Pre]

To the extent the preamble is limiting, *Steer* renders it obvious as shown in annotated Figures 1, 2, 3, and 4. Ex.[1002], ¶¶263-271.

Active Matrix Organic Light Emitting Diode Display Panel…Comprising a Plurality of [OLED] pixel elements

Steer discloses "[a]n ***active matrix electroluminescent display device*** compris[ing] an array of display pixels" comprising a "panel." Ex.[1008], Abstract, 2:4-14. "The display elements may comprise ***organic thin film electroluminescent elements***, for example using polymer materials, or else light emitting diodes (LEDs)…," which a POSA would understand includes organic light emitting diodes

(OLED). Ex.[1008], 1:11-12, Ex.[1002], ¶¶263. The elements are "***active matrix addressed***" Ex.[1008], 2:3-4, Fig. 1.



Ex.[1008], Fig. 1.

Receiving a Video Signal To Be Displayed

Steer entails "***an input voltage at input 52 representing the desired current***." Ex.[1008], 9:14-15. A POSA would recognize that "the input voltage at input 52 representing the desired current" corresponds to the claimed ***video signal***. For instance, *Steer* explains that the OLED materials discussed therein are "used practically ***for video display devices***" Ex.[1008], 1:15-16. Moreover, a POSA would understand that the desired amount of current through the pixel element corresponds to the brightness of the pixel thus a voltage that represents the desired current at

input **52** would be understood as a ***video signal***. In the alternative, it would be obvious that the "input voltage at input **52**" would correspond to a ***video signal***. A POSA would be motivated to make the obvious design choice of inputting a video signal at **52** at least because it's well-known in the art to use video signals as inputs to display panels and particularly for video drivers like in *Steer,* and as noted above, *Steer* itself notes the display is useful to display video, which a POSA would understand means the display would need to be connected to an input video signal to display. Ex.[1002], ¶¶267-269. Moreover, *Steer* is directed to an "analogue implementation," providing a POSA further motivation to use an (analogue) video signal. Ex.[1008], 11:3-4.

Steer explains "FIG. 3 shows a first pixel arrangement in accordance with the invention," and "FIG. 4 shows the column driver architecture for a display using the pixel of FIG. 3." Ex.[1008], 8:3-4, 7:26-27. Thus, a POSA would understand that Figures 3-4 correspond to the same embodiment. Ex.[1002], ¶270; Ex.[1008], Figs. 3, 4.

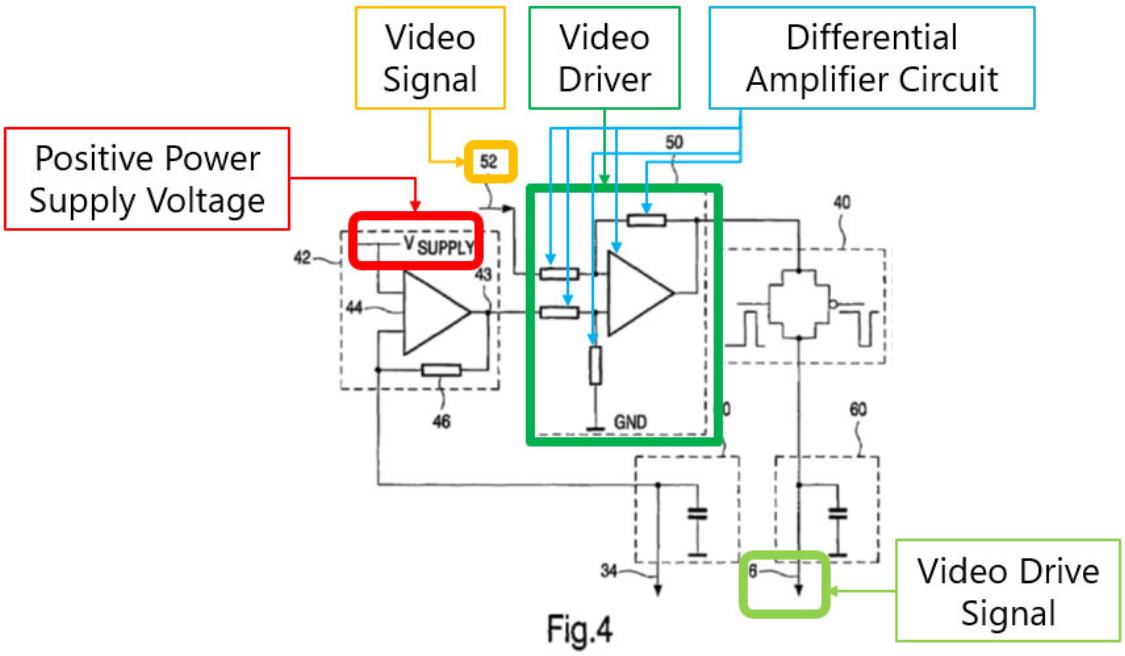


Fig.4

Ex.[1008], Fig. 4 (annotated).

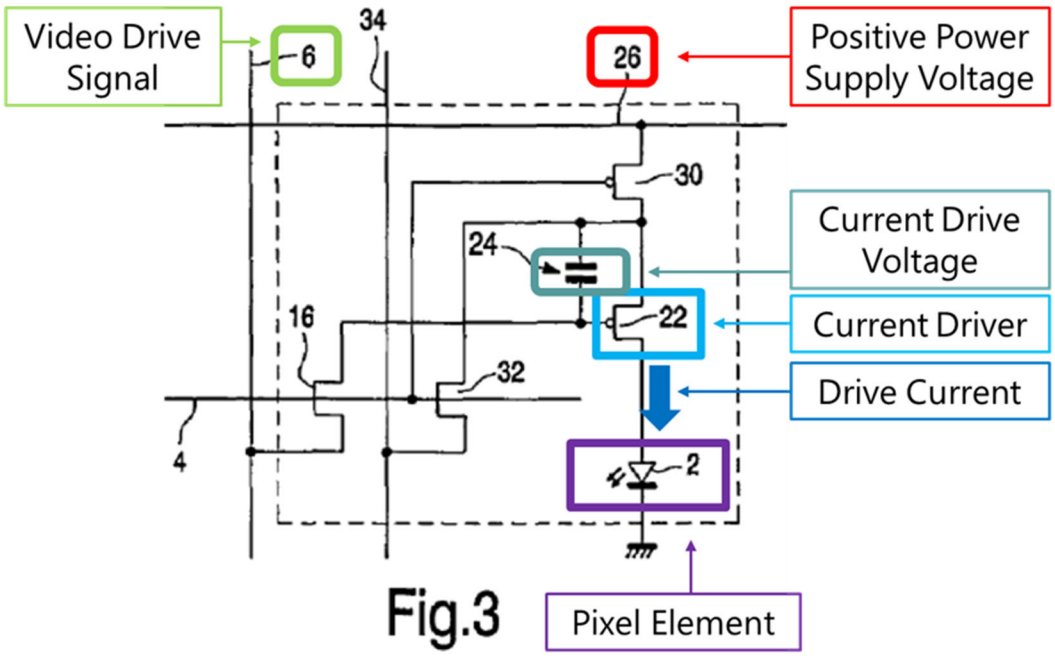


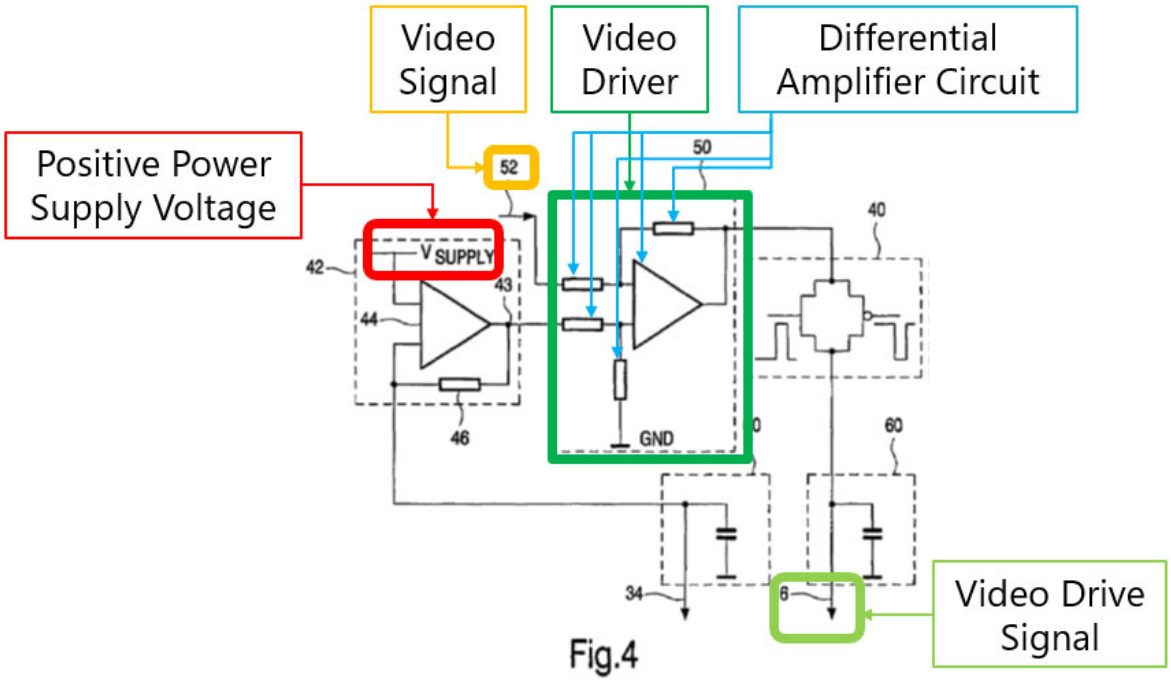
Fig.3

Ex.[1008], Fig. 3 (annotated).

Claim[1-A]

Video Driver Receiving The Video Signal

As annotated in Figure 4, *Steer* discloses a ***video driver*** ("comparator section **50**" shown in green) receiving the input ***video signal* 52** ("representing the desired current") Ex.[1008], 9:14-19, 8:28-29, Fig. 4.



Ex.[1008], Fig. 4 (annotated).

Supply Voltage

Steer's video driver also receives an input from "high open loop gain amplifier **44**" which itself is connected to "$\mathbf{V_{SUPPLY}}$" which is "the same supply voltage as for the power supply line **26**." Ex.[1008], 9:4-12. That amplifier **44** outputs at node **43**

a value that differs from $\mathbf{V_{SUPPLY}}$ "by a value **R**x**I**, where **R** is the resistance of the feedback resistor **46** and **I** is the current flowing." Ex.[1008], 9:4-12.

Generating Drive Signal Indicative of Video Signal and Referenced To Supply Voltage

The "output of the comparator section **50** [Video Driver] is provided to the column conductor through the gate **40**. The comparator section **50** thus also acts as the driver for providing the column conductor voltage." Ex.[1008], 9:14-19.

Additionally, a POSA would recognize that the output of comparator section **50**, which is a comparison between "the voltage at node **43** with an input voltage at input **52** representing the desired current" corresponds to the claimed ***video drive signal indicative of the video signal and referenced to a positive power supply voltage of the AMOLED display panel***. In particular, voltage on node **43** corresponds to $\mathbf{V_{SUPPLY}}$ added to **R*I**, where **R** is the resistance of resistor **46** and **I** is the current flowing. Ex.[1008], 9:10-14; Ex.[1002], ¶¶276-280. *Steer*'s Node 43 voltage is thus represented as:

Steer (1): $\mathbf{V_{43}=V_{SUPPLY}+R*I}$

A POSA would thus recognize that voltage at node **43** is $\mathbf{V_{SUPPLY}}$ with an offset, and a comparison between voltage at node **43** ($\mathbf{V_{43}}$) and input voltage at input **52** would result in an output signal indicative of voltage at input **52** ($\mathbf{V_{52}}$ or *input(t)*) (*i.e.*, the claimed ***video signal***) and referenced to $\mathbf{V_{SUPPLY}}$ (*i.e.*, the claimed ***positive***

power supply voltage of the AMOLED display panel). The output of the comparator **50** is column conductor **6** (or node **6)** which has a transmission gate **40** connected in series with the conductor line **6**. Ex.[1008], 9:1-2. The resulting output on node **6** ($\mathbf{V_6}$) (the claimed ***video drive signal***) in *Steer* is shown below in equation (2), which shows the output of the comparison between $\mathbf{V_{43}}$ and $\mathbf{V_{52}}$ that the video drive signal includes video signal (*input(t)*) subtracted from $\mathbf{V_{SUPPLY}}$.

Steer (2): $\mathbf{V_6}=\mathbf{V_{SUPPLY}}+\mathbf{R*I}-$*input(t)*

Ex.[1002], ¶281.

This is substantially identical to operation of the embodiments of the'521 Patent, where the video drive signal *v(t)* is "referenced to" VDD as shown in equation (7), where video signal (Video.DAC) is similarly subtracted from supply voltage V_{DD}. Ex.[1001], 6:10-31 ("Equation 5").

'521 Eq.(5): ***v(t)***=**VDD-Video.DAC**

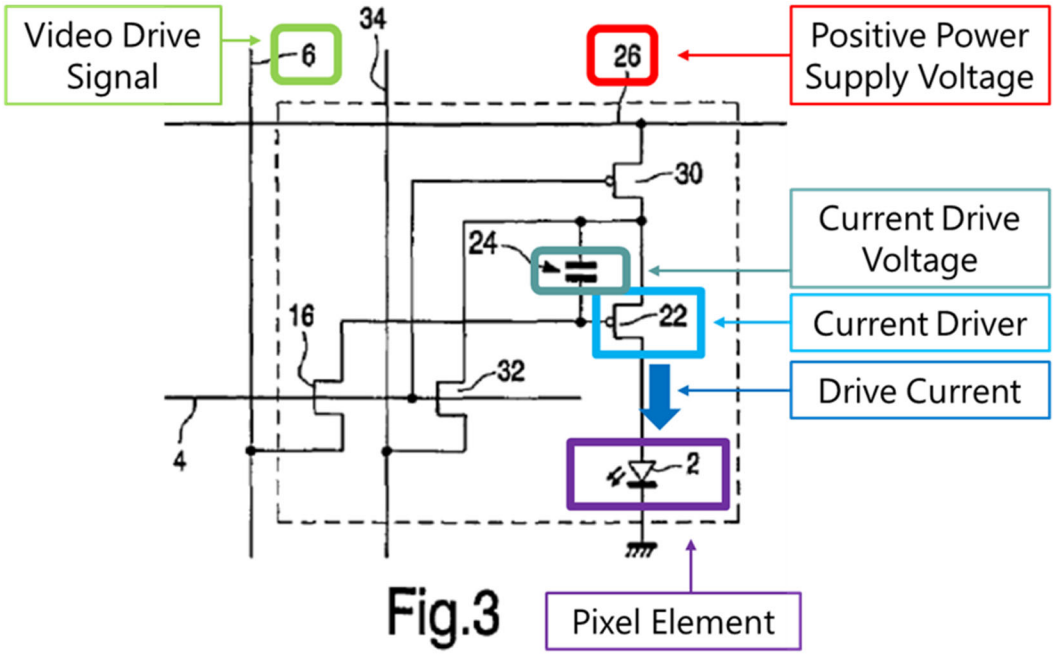
Ex.[1002], ¶282.

Therefore, as illustrated in Figure 4 (annotated) above, a POSA would recognize that *Steer* discloses Claim [1-A]. Ex.[1008], Fig. 4; Ex.[1002], ¶283.

Claim[1-B]

Current Driver Coupled to the OLED Pixel Element Receiving the Video Drive Signal and the Positive Power Supply and Providing a Drive Current to the OLED Pixel Element

Steer explains "FIG. 3 shows a first pixel arrangement in accordance with the invention." Ex.[1008], 8:3-4, Fig. 3.



Ex.[1008], Fig. 3 (annotated).

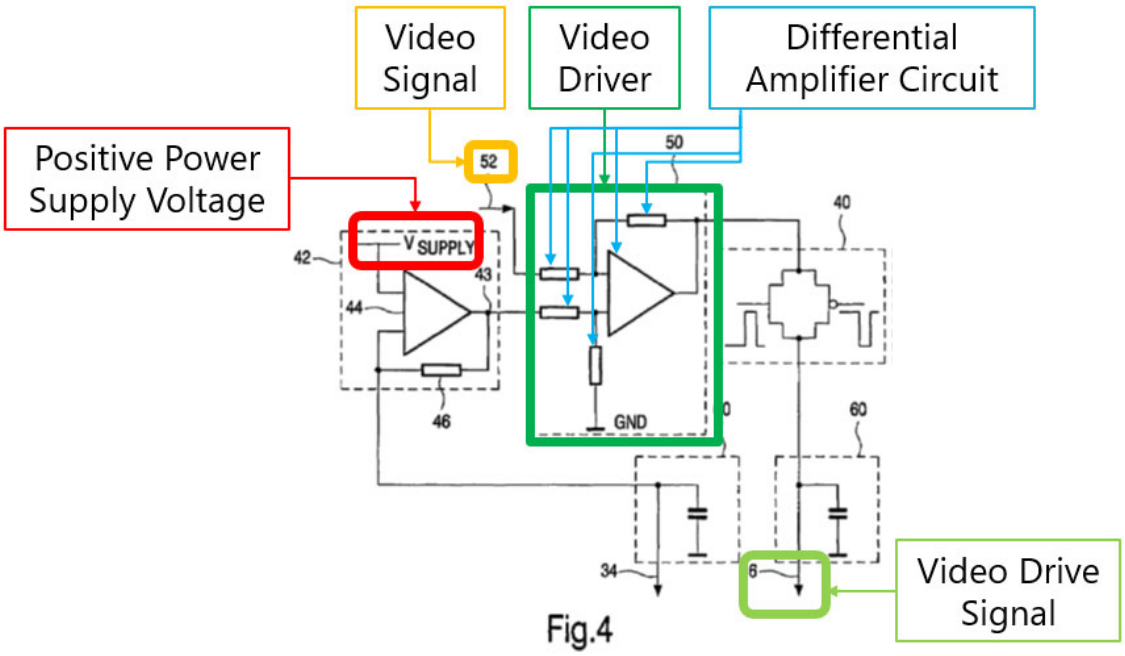
As shown, *Steer* includes current driver ("drive transistor **22**") coupled to OLED pixel element ("EL display element **2**"). Ex.[1008], 2:30-3:9. The current driver (**22**) receives the drive signal (**6**) at its gate via "address transistor **16**" and power supply voltage from "power supply line **26**" via transistor 30. *Id.* Ex.[1008], 8:32-9:3, 9:25-26, 10:5-10. During the pixel drive phase, line **26** corresponds to $\mathbf{V_{SUPPLY}}$. Ex.[1008], 10:5-10. Additionally, current driver "drive transistor 22" operates to "give[] rise to the desired [drive] current" through OLED 2. Ex.[1008], 9:25-29.

Therefore, consistent with Figure 3 (annotated) above, a POSA would recognize that *Steer* discloses Claim [1-B]. Ex.[1002], ¶¶285-287.

Claim[1-C]

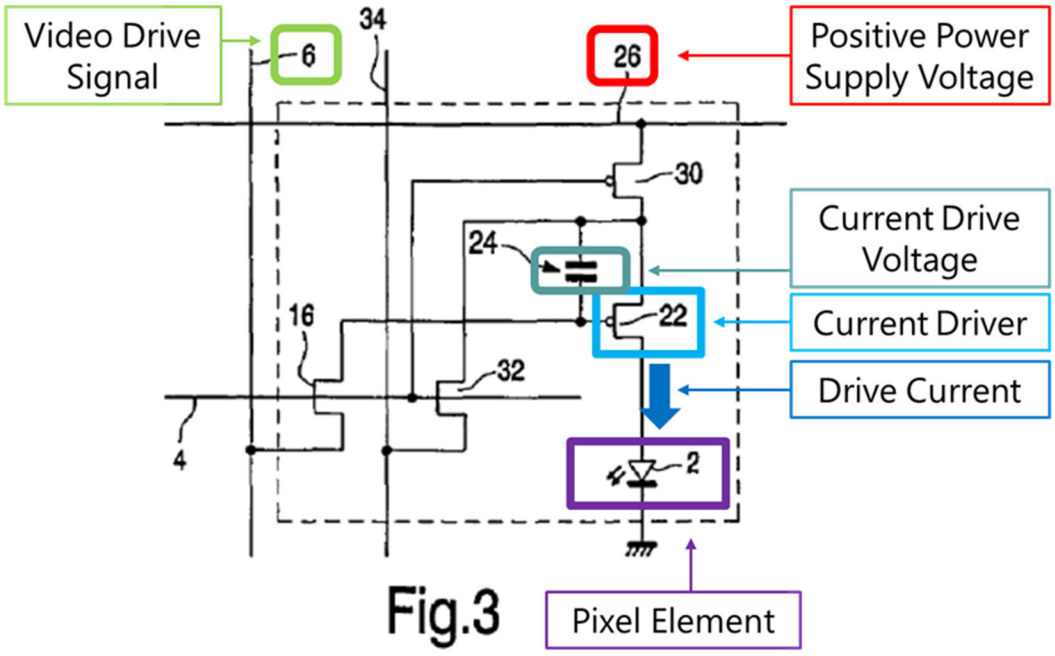
Current Drive Voltage being Indicative of the Video Signal

Steer explains its current driver (drive transistor **22)** "is implemented as a PMOS TFT…which therefore provides the desired current source operation of the pixel." Ex.[1008], 3:6-13. Current driver (**22**) receives a "***current drive voltage***" comprising the gate-source voltage—the difference between the voltage at the source of drive transistor **22** (coupled to the positive power supply line **26** through transistor **30**) and the voltage provided from the driver on line **6** on the gate of drive transistor **22**. As previously noted, the voltage on line **6**, in turn, is ***indicative of the video signal*** because voltage is generated on line **6** varies directly with the video signal input on line **52**. Ex.[1002], ¶¶293-297; Ex.[1008], Fig. 4.



Ex.[1008], Fig. 4 (annotated).

Accordingly, a POSA would understand that the gate-source voltage for drive transistor **22** is the claimed ***current drive voltage***, and would further understand that the current flowing through drive transistor **22** and into EL element **2** is the claimed ***drive current***. Ex.[1002], ¶¶289-290, 292; Ex.[1008], Fig. 3.



Ex.[1008], Fig. 3 (annotated).

The Drive Current being Proportional to a Current Drive Voltage

A POSA would also recognize that because *Steer's* drive transistor **22** and the '521 Patent's transistor M1 are both P-channel MOSFETs, they would both operate in the same manner based on the well-known principles and functionalities of P-Channel MOSFETs. Ex.[1002], ¶¶290. Therefore, to the same extent that the '521 Patent's drive current is "proportional" to its gate-source current drive voltage, a POSA would understand that *Steer's* current flowing through drive transistor **22** and into the EL element **2** is also "***proportional***" to *Steer's* gate-source voltage.[11] Ex.[1008], Fig. 3 (annotated); Ex.[1002], ¶¶291-292.

[11] *See supra*, Fn.7 regarding "proportional."

Current Drive Voltage…Independent of the…Power Supply Voltage

Moreover, as explained for Gr.5,Cl.[1-A], the video drive signal applied to the gate of drive transistor **22** is generated by "comparator section **50**" (*i.e.*, the claimed ***video driver***) via a comparison between the voltage on input **52** (*i.e.*, the claimed ***video signal***) and a voltage at node **43** that's dependent on $\mathbf{V_{SUPPLY}}$ (which is also the voltage on line **26**) (*i.e.*, the claimed ***positive power supply voltage***). Accordingly, a POSA would understand that generating the ***video drive signal*** using the ***positive power supply voltage*** and then applying the ***video drive signal*** as a gate voltage to drive transistor **22** relative to the ***positive power supply voltage*** to generate the drive current renders the current drive voltage ***independent of the positive power supply voltage*** as claimed. Ex.[1002], ¶¶293-297. That is, a change in voltage of $\mathbf{V_{SUPPLY}}$ will be recognized both at node **43** and at line **26**, and therefore, the current drive voltage will be independent of the PPS.

A mathematical representation of the voltages at each node shows that $\mathbf{V_{SUPPLY}}$ does not appear in the gate-to-source voltage over drive transistor **22**, and therefore, is independent of $\mathbf{V_{SUPPLY}}$ for at least the same reasons as described in the '521 Patent. As discussed for Gr.5,Cl.[1-A], $\mathbf{V_{SUPPLY}}$ is the same as the voltage on line **26**. The voltage on line **52** is represented by *input(t)* in equation (1), the voltage at node **43** is represented by equation (2), the voltage on line **6** is represented

by equation (3), and the gate-to-source voltage on the drive transistor is represented by equation (4).

$$V_{52} = input(t) \qquad (1)$$

$$V_{43} = V_{SUPPLY} + R * I \qquad (2)$$

$$V_6 = V_{43} - V_{52} \qquad (3)$$

$$V_{GS} = V_6 - V_{SUPPLY} \qquad (4)$$

Substituting equations (1)-(3) into equation (4) yields the updated equation (4A).

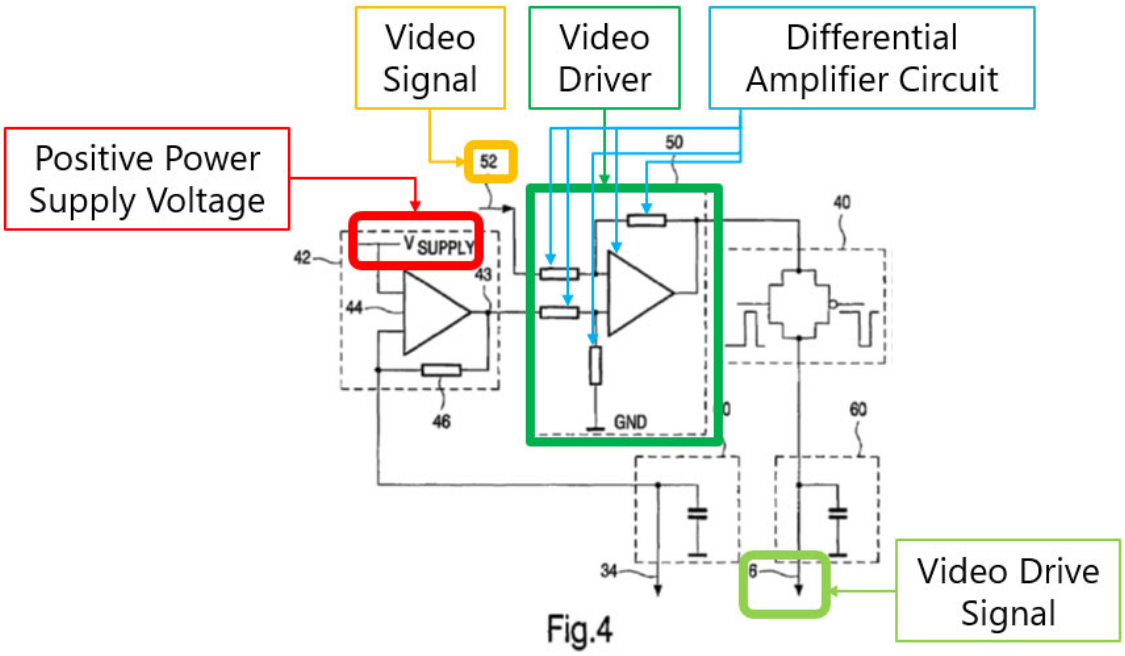
$$V_{GS} = V_{SUPPLY} + R * I - input(t) - V_{SUPPLY} \qquad (4A)$$

$$V_{GS} = R * I - input(t) \qquad 4(B)$$

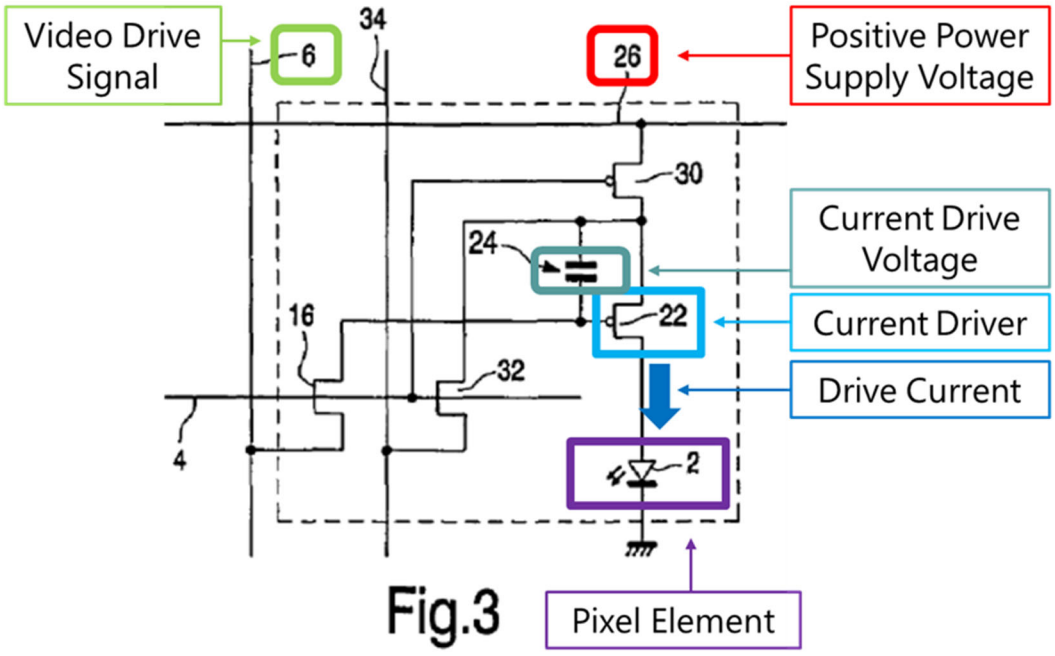
Since the first $\mathbf{V_{SUPPLY}}$ will be eliminated in equation (4A) via subtraction of the second $\mathbf{V_{SUPPLY}}$, the gate-to-source voltage $\mathbf{V_{GS}}$ on drive transistor **22** (i.e., the claimed ***current drive voltage***) is ***independent of the positive power supply voltage*** as shown in equation (4B). Ex.[1002], ¶¶295-297.

Therefore, consistent with Figures 3-4 (annotated) below, a POSA would recognize that *Steer* discloses ***the drive current*** (drain current of drive transistor **22**) ***being proportional to a current drive voltage*** (gate-to-source voltage of drive transistor **22**) ***being indicative of the video signal*** (voltage on input **52**) ***and***

independent of the positive power supply voltage (supply voltage **V_{SUPPLY}** on line **26** and within **42**). Ex.[1008], Figs. 3, 4; Ex.[1002], ¶298.



Ex.[1008], Fig. 4 (annotated).



Ex.[1008], Fig. 3 (annotated).

2. *Claim 2*

Video Drive Signal is Indicative of the Difference…Between The Positive Power Supply Voltage and the Video Signal

As described above for Gr.5,Cl.[1-A], "comparator section **50**" generates the claimed ***video drive signal***.

Steer discloses "comparator section **50** compares the voltage at node 43 with an input voltage at input **52** representing the desired current." Ex.[1008], 9:14-15. *Steer* explains "the voltage at node 43 differs from this supply voltage by a value **R**x**I**, where **R** is the resistance of the feedback resistor **46** and **I** is the current flowing." Ex.[1008], 9:10-12. Steer continues "output of the comparator section **50** is provided to the column conductor through the gate **40**." Ex.[1008], 9:17-18.

Thus, a POSA would recognize that *Steer* teaches that drive voltage on line 6 ($\mathbf{V_6}$) (i.e., the claimed ***video drive signal***) is the difference between the voltage at node **43** ($\mathbf{V_{43}}$) and the voltage on input line **52** (*input(t)*) (i.e., the claimed ***video signal***). Further, as discussed for Gr.5,Cls.[1-A, 1-C], a POSA would understand that $\mathbf{V_{43}}$ is equal to $\mathbf{V_{SUPPLY}+R*I}$. Consequently, a POSA would recognize that ($\mathbf{V_6}$) (i.e., the claimed ***video drive signal***) is ***indicative*** of the difference between power supply voltage and the video signal ($\mathbf{V_{SUPPLY}}$-*input(t)*), as claimed. Ex.[1002], ¶299-303.

(1) $\mathbf{V_6}=\mathbf{V_{43}}$–*input(t)*

(2) $\mathbf{V_{43}}$=R*I+$\mathbf{V_{SUPPLY}}$

(3) $\mathbf{V_6}$= **R*I+** $\mathbf{V_{SUPPLY}}$-*input(t)*

Moreover, as discussed for Gr.5,Cl.[1-C], the claimed ***current drive voltage*** is the gate-to-source voltage over drive transistor **22** ($\mathbf{V_{GS}}$). As also discussed, $\mathbf{V_{GS}}$ is equal to the difference between the gate voltage applied via line **6** ($\mathbf{V_6}$) and the voltage on line **26** ($\mathbf{V_{SUPPLY}}$). Consequentially, a POSA would understand that the ***current drive voltage*** ($\mathbf{V_{GS}}$) is ***indicative*** of the ***difference*** between the ***positive power supply voltage*** ($\mathbf{V_{SUPPLY}}$) and the ***video drive signal*** ($\mathbf{V_6}$). Ex.[1002], ¶304

(4) $\mathbf{V_{GS}}=\mathbf{V_6}$-$\mathbf{V_{SUPPLY}}$

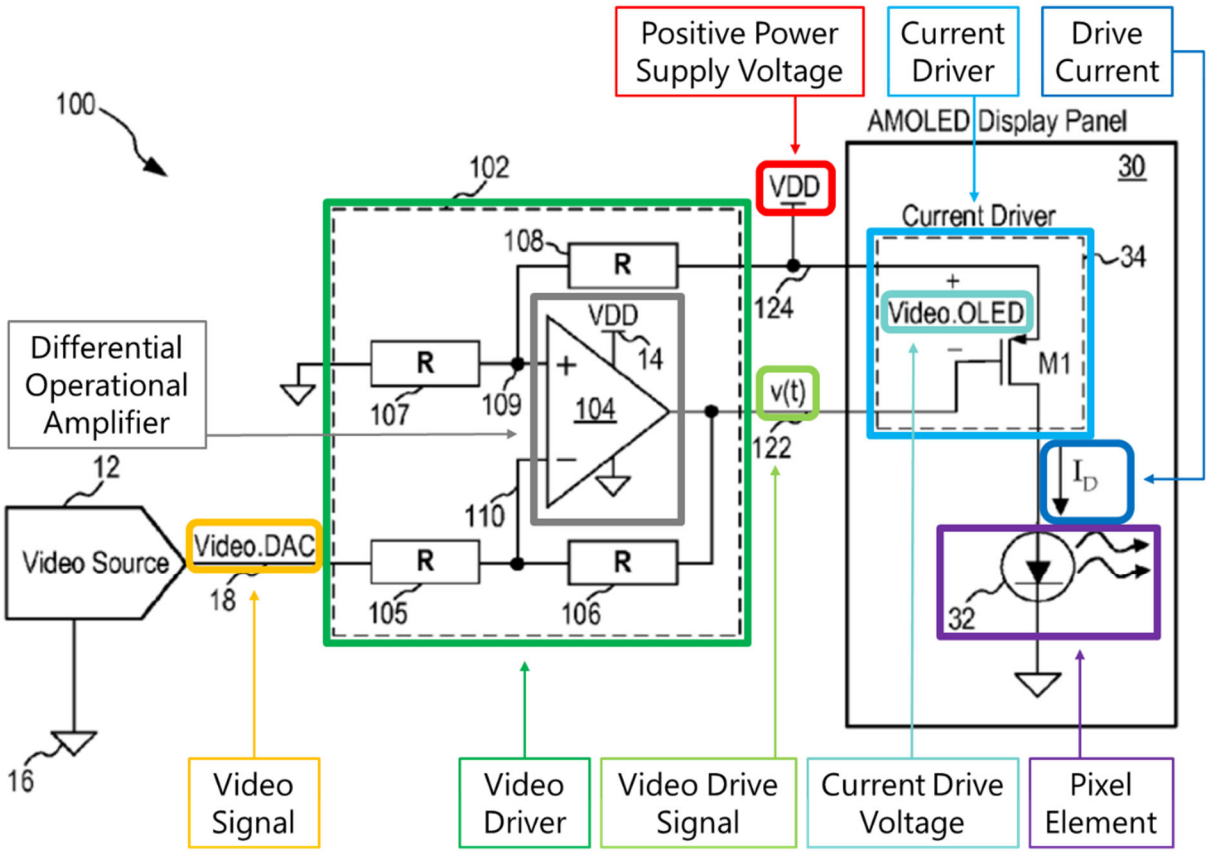
Therefore, a POSA would recognize that *Steer* discloses ***the video drive signal*** (gate voltage $\mathbf{V_6}$) ***is indicative of the sum of or the difference between the positive***

power supply voltage (drive voltage $\mathbf{V_{SUPPLY}}$) ***and the video signal*** (voltage on the input line **52** (*input(t)*) ***and the current drive voltage*** (gate-to-source voltage=$\mathbf{V_{GS}}$) ***is indicative of the difference between the positive power supply voltage*** (drive voltage $\mathbf{V_{SUPPLY}}$) ***and the video drive signal*** (gate voltage supplied on line **6** ($\mathbf{V_6}$)). Ex.[1002], ¶305.

3. *Claim 3*

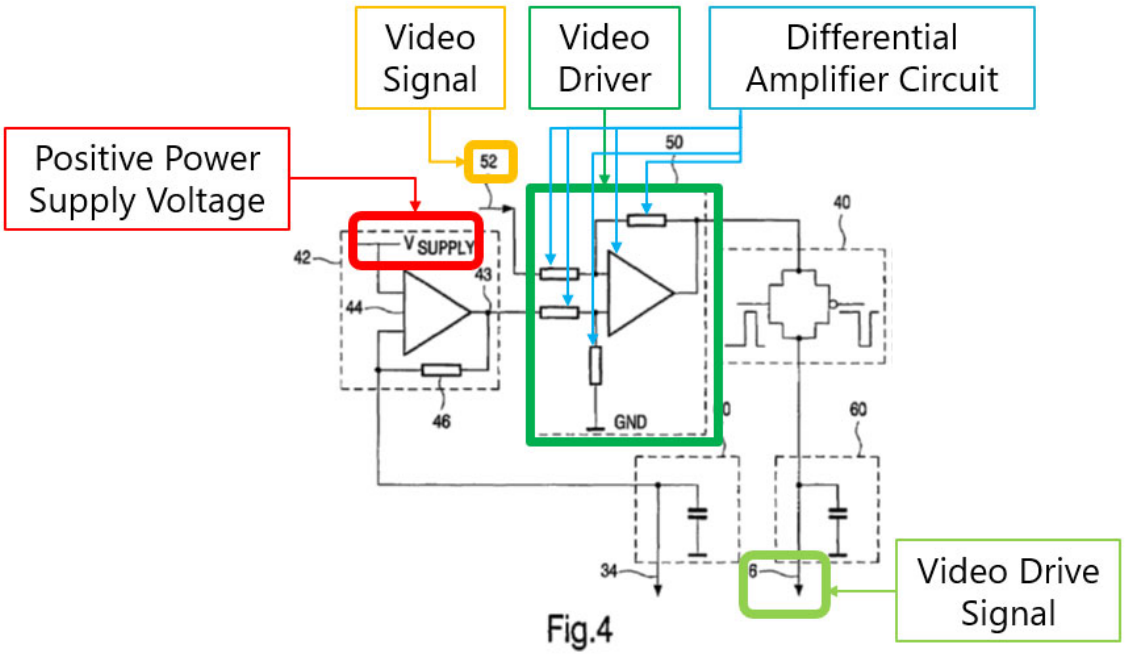
Differential Instrumentation Amplifier Circuit … Video Drive Signal being the Difference between the Positive Power Supply Voltage and the Video Drive Signal

Claim 3 corresponds to the '521 Patent's first embodiment shown in Figure 2 (annotated) below, where: "video driver 102 is implemented using a differential instrumentation amplifier circuit to re-reference the video drive signal v(t) to the positive power supply voltage VDD." Ex.[1001], 4:7-37, Fig. 2.



Ex.[1001], Fig. 2 (annotated).

As discussed above for Gr.5,Cl.[1-A], a POSA would recognize that *Steer* discloses ***a video driver*** (circuitry in green Video Driver annotation above) ***receiving the video signal*** (a voltage on input line **52**) ***and generating a video drive signal*** (gate voltage $\mathbf{V_6}$) ***indicative of the video signal and referenced to a positive power supply voltage*** (supply voltage $\mathbf{V_{SUPPLY}}$) ***of the AMOLED display panel***. Ex.[1008], Fig. 4; Ex.[1002], ¶309.



Ex.[1008], Fig. 4 (annotated).

Steer discloses that there is an "amplifier of the comparator." Ex.[1008], 6:1. *Steer* explains that "a comparator section **50** compares the voltage at node **43** with an input voltage at input **52** representing the desired current." Ex.[1008], 9:23-24.

A POSA would understand that the amplifier and resistors of comparator **50** are in a differential arrangement and that input line **52** is coupled to the negative terminal of the operational amplifier via a resistor and that node **43** (a function of $\mathbf{V_{SUPPLY}}$) is coupled to a positive terminal of the operational amplifier, and therefore, the output on line **6** ($\mathbf{V_6}$) is the difference between $\mathbf{V_{SUPPLY}}$ and the voltage on input line **52** (*input(t)*). Ex.[1002], ¶¶307-309. That is, as discussed for Gr.5,Cl.[2], node

43 has a voltage corresponding to $\mathbf{V_{SUPPLY}}$ added to the feedback voltage denoted by the resistor value of resistor **46** multiplied by the current passing through resistor **46**. Mathematically, the voltage at node **43** ($\mathbf{V_{43}}$) is represented by equation (1) below, which yields the voltage of conductor **6** ($\mathbf{V_6}$) ***video drive signal*** represented by equation (2) below. Also, as explained in Gr.5,Cl.[1-C] the gate-to-source voltage ($\mathbf{V_{GS}}$), which is the current drive voltage, is represented by equation (3) below.

(1) $\mathbf{V_{43}=V_{SUPPLY}+R*I}$

(2) $\mathbf{V_6=R*I+V_{SUPPLY}}-input(t)$

(3) $\mathbf{V_{GS}=V_6-V_{SUPPLY}=R*I}-input(t)$

Ex.[1008], 309.

Steer does not disclose the value of the resistors in the differential circuit of the video driver. A POSA would be motivated to make the obvious design choice of using the same resistance values in the differential circuit at least because the POSA would recognize that a gain of unity would make the circuit easier to analyze, and make manufacturing more efficient by only needing to buy and maintain one resistor type to implement the circuit. Ex.[1002], ¶¶313-314. A POSA would further be motivated to make this obvious modification because it is a mere design choice that would also accomplish the stated purpose of *Steer*. Indeed, Steer does not disclose that a non-unity gain would be desired or necessary. Ex.[1008], ¶0028; Ex.[1002], ¶314. The result of the design choice of unity gain is that the output (on column

conductor **6**) of comparator **50** is the difference between the signals on input node **43** and **52**.

Accordingly, a POSA would recognize that *Steer* discloses at least one condition of ***the video drive signal*** (**V_6**) ***being the difference between the positive power supply voltage and the video signal***. Ex.[1002], ¶¶315-318. In a first example, **V_6** (the claimed ***video drive signal***) will be exactly the difference between **V_{SUPPLY}** (the claimed ***positive power supply voltage***) and the *input(t)* (the claimed ***video signal***) when the current (**I**) through resistor **46** (**R**) is zero. This will initially occur when the programming phase of the pixel begins. For example, at least at the moment at which the programming phase begins, the voltage at node **43** will be equal to **V_{SUPPLY}** because there is no current flowing through resistor **46** (**R**). There is no current flowing through resistor **46** (**R**) at this time because the current has not yet started to flow through the pixel element **2**. Moreover, in some circumstances, a first programming phase will charge capacitor **24** to a first voltage of **V_{GS}** for a particular first current (e.g., set by the voltage on the input line **52** *input(t)*). That is, the first current will correspond to a first magnitude of **V_{GS}.** The programming phase ends and the top terminal of capacitor **24** is held at **V_{SUPPLY}** supplied via line **26** and the first magnitude of **V_{GS}** is held at a constant voltage. Ex.[1008], 2:1-2 ("a storage capacitor **24** holds the voltage on the gate of the drive transistor **22** after the pixel addressing (programming) phase.") When a second programming phase begins that

requires a second magnitude of $\mathbf{V_{GS}}$ that is smaller than the first magnitude, the capacitor **24** will discharge from the first magnitude voltage to the second magnitude thereby supplying current to the pixel element **2** for some period of time. During the discharge, the current through resistor **46** (**R**) will be zero and the voltage at node 43 will be exactly $\mathbf{V_{SUPPLY}}$. Accordingly, it will not be until the capacitor **24** sufficiently discharges that a current (**I**) will flow through **46** (**R**). In this way, the voltage at node **43** will be equal to $\mathbf{V_{SUPPLY}}$ because there is no current flowing through resistor **46** (**R**) and therefore the R*I value in equation shown for $\mathbf{V_6}$ be zero, and the output of the comparator **50** will be the difference between $\mathbf{V_{SUPPLY}}$ and the input voltage on line **52**. Ex.[1002], ¶¶316-317.

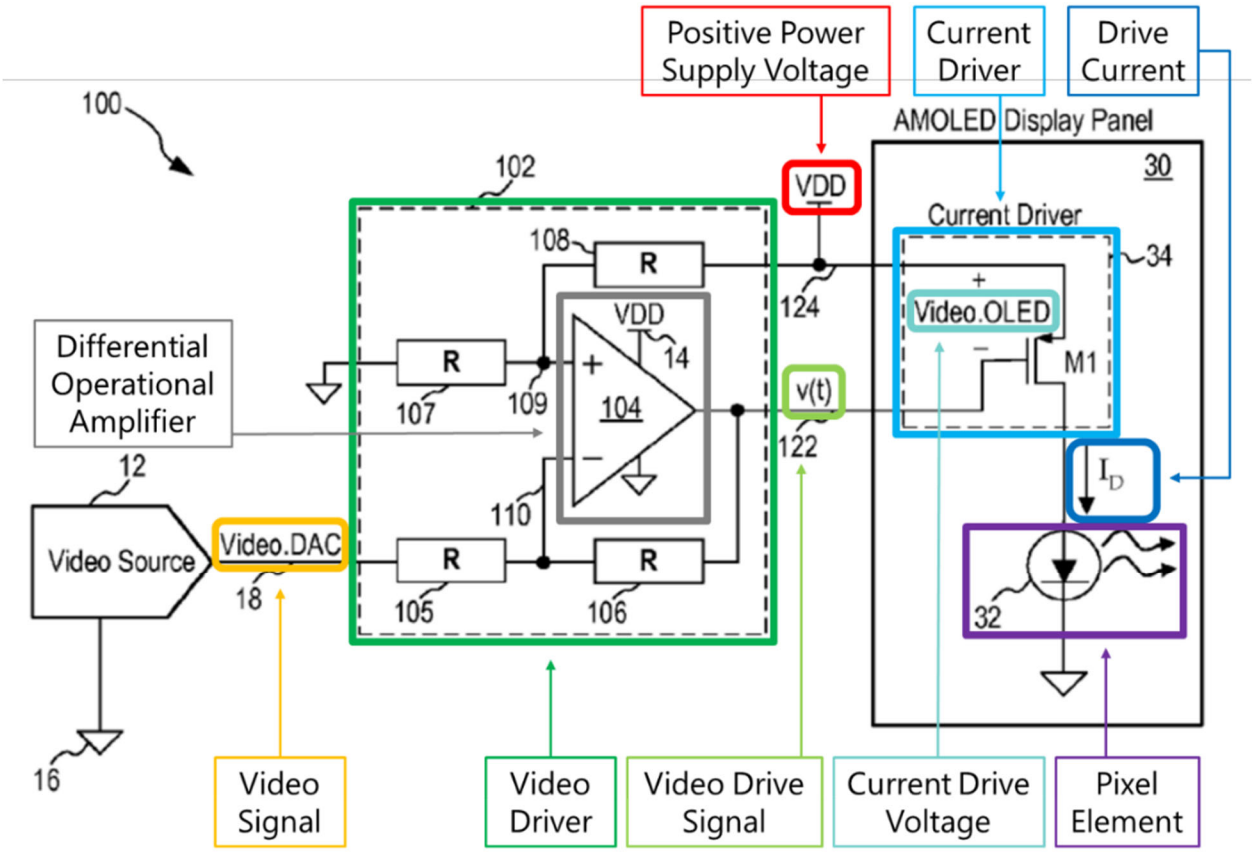
Therefore, as shown in Figure 4 (annotated) above, a POSA would recognize that *Steer* discloses ***wherein the video driver*** (comparator section **50**) ***comprises a differential instrumentation amplifier circuit*** (operation amplifier and resistors in differential arrangement annotated in light blue) ***for providing the video drive signal being the difference between the positive power supply voltage*** (node **43**) ***and the video signal*** (input voltage on input **52**). Ex.[1002], ¶318.

4. *Claim 4*

Claim[4-Pre]

Claim 4 corresponds to the ’521 Patent’s first embodiment shown in Figure 2 (annotated) below: “FIG. 2 is a schematic diagram of a video driver for an AMOLED

display system according to a first embodiment of the present invention." Ex.[1001], 4:7-9, Fig. 2.



Ex.[1001], Fig. 2 (annotated).

Claim[4-A]

In the '521 Patent, the operational amplifier corresponds to element 104 in Figure 2.

> ***An Operational Amplifier … a First Resistor Coupled to a Positive Input Terminal … A Second Resistor Coupled to a Negative Input Terminal… and an Output Terminal Providing the Video Drive Signal***

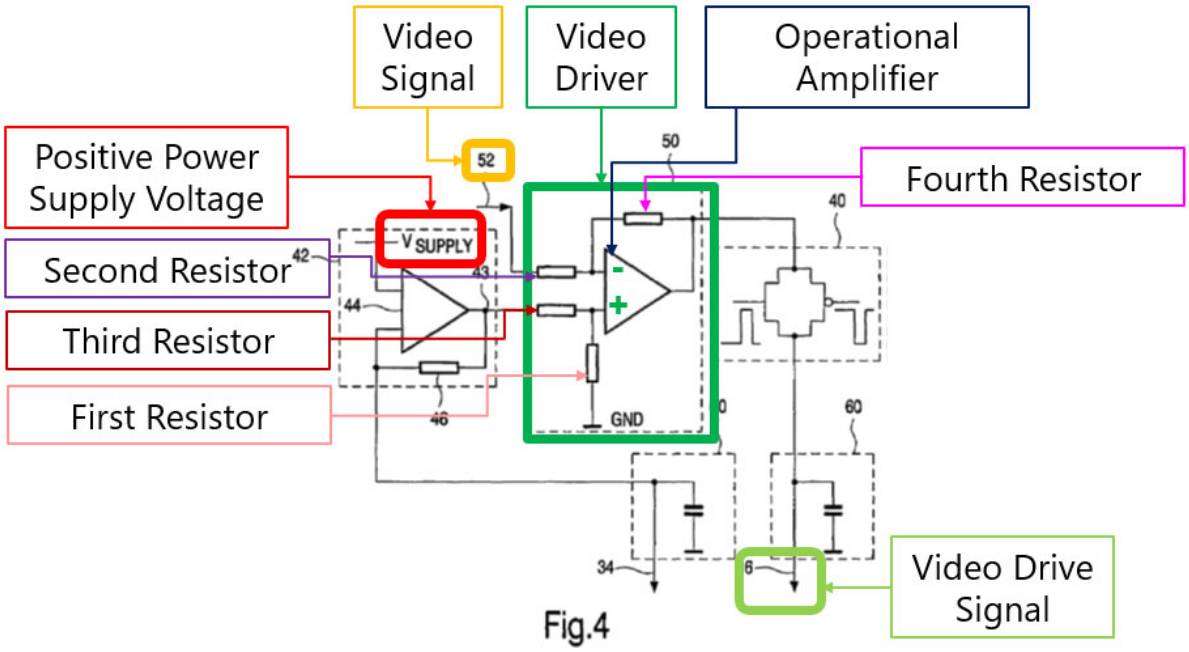
Steer discloses that there is an "amplifier of the comparator." Ex.[1008], 9:22-23. *Steer* explains that "a comparator section **50** compares the voltage at node **43**

with an input voltage at input 52 representing the desired current." Ex.[1008], 9:14-15.

As discussed in Gr.5,Cl.[3], a POSA would understand that amplifier and resistors of the comparator **50** are in a differential arrangement and be motivated to make the obvious design choice of having the input line **52** coupled to the negative terminal of the operational amplifier via a (second) resistor because it was well known that in conventional differential instrumentation amplifier circuits, the positive input terminal is the reference voltage (often ground) against which the negative terminal voltage is compared to. Ex.[1002], ¶321. Thus, a POSA would understand that a first resistor would be connected to the positive terminal. Furthermore, the current-to-voltage converter 42 includes a high open loop gain amplifier 44 such that the current-measurement line 34 is connected to the virtual earth input with the power supply connected to the other input of amplifier 44. Ex.[1008],9:6-9. The output of this amplifier is connected to the input of the amplifier 50. A POSA would understand that in order for the output of the amplifier 50 to output a correct polarity to bias the drive transistor via control line 6, virtual earth must be connected to the non-inverting terminal of the op amp. Ex.[1002], ¶324. Thus, a POSA would understand that node **43** that is a function of $\mathbf{V_{SUPPLY}}$ is coupled to a positive terminal of the operational amplifier and therefore the output on line 6 ($\mathbf{V_6}$) is the difference between the $\mathbf{V_{SUPPLY}}$ and the voltage on input line **52** (*input(t)*).

Ex.[1002], ¶¶321-327. Also as discussed for Gr.5,Cl.[3], there are particular circumstances where node **43** is exactly **V_{SUPPLY}**. Ex.[1002], ¶¶315-317.

Therefore, as shown in Figure 4 (annotated) below, a POSA would understand that *Steer* discloses or renders obvious ***an operational amplifier*** (annotated in dark blue) ***having a positive input terminal coupled to a first resistor*** (annotated in light pink)***, a negative input terminal coupled to a second resistor*** (annotated in purple) ***and an output terminal providing the video drive signal*** (light green annotation of VDS on line **6**). Ex.[1008], Fig. 4.



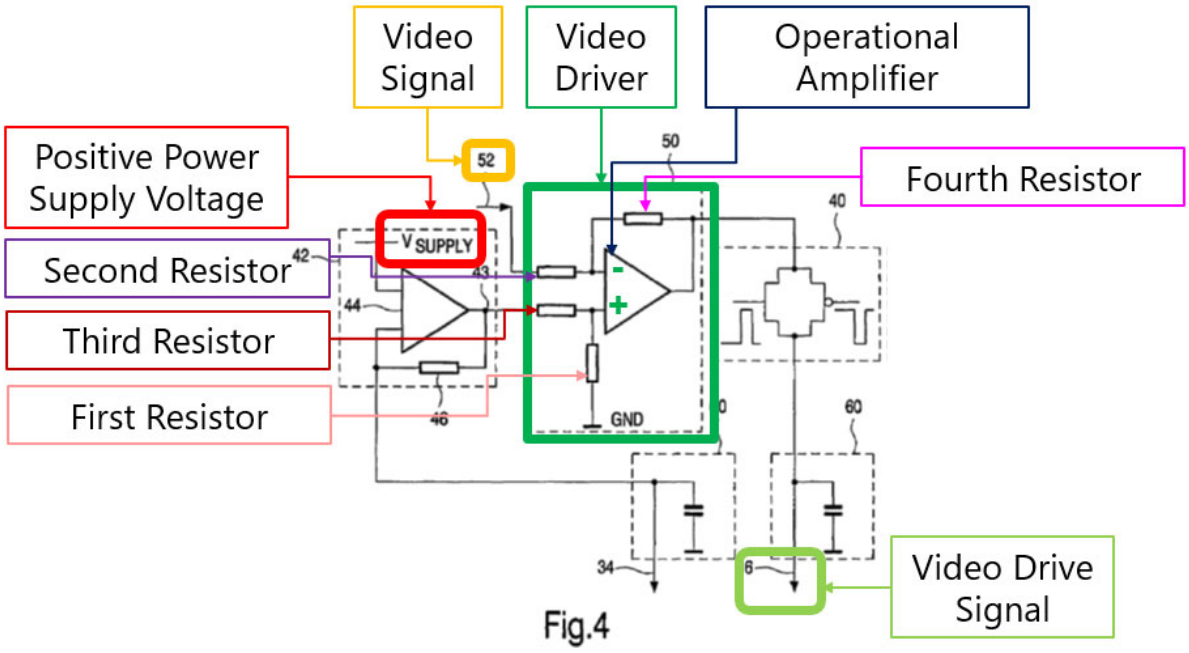
Ex.[1008], Fig. 4 (annotated).

Claim[4-B]

First Resistor Coupled between the Positive Input Terminal and a Ground Voltage

In the '521 Patent, the first resistor corresponds to element 107 in Figure 2.

For the same reasons discussed for Gr.5,Cl.[3], and as shown in Figure 4 (annotated) below, a POSA would understand that *Steer* discloses or renders obvious ***the first resistor*** (annotated in light pink) ***being coupled between the positive input terminal of the operational amplifier*** (annotated in blue) ***and a ground voltage*** ("GND" in Figure 4) ***or a negative power supply voltage***. Ex.[1008], Fig. 4; Ex.[1002], ¶¶328-329.



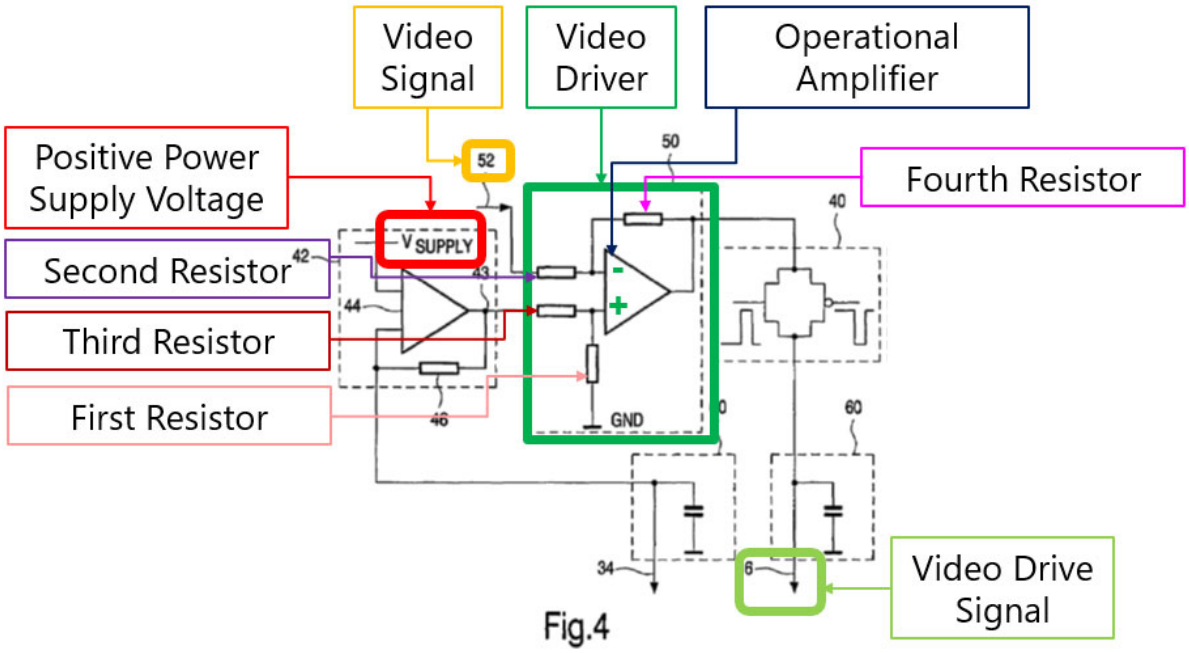
Ex.[1008], Fig. 4 (annotated).

Claim[4-C]

Second Resistor Coupled between the Negative Input Terminal and the Video Signal

In the ’521 Patent, the second resistor corresponds to element 105 in Figure 2.

For the same reasons as discussed in Gr.5,Cl.[3], and as shown in annotated Figure 4 below, a POSA would understand that *Steer* discloses or renders obvious ***the second resistor*** (annotated in purple) ***being coupled between the video signal*** (annotated in orange) ***and the negative input terminal of the operational amplifier*** (annotated in blue). Ex.[1008], Fig. 4; Ex.[1002], ¶¶330-331.



Ex.[1008], Fig. 4 (annotated).

Claim[4-D]

Third Resistor Coupled between the Positive Input Terminal and the Positive Power Supply

In the ’521 Patent, the third resistor corresponds to element 108 in Figure 2.

As discussed in Gr.5,Cl.[1-A], node **43** is the PPS voltage offset by a value of **R*I**. **R** is the resistor labeled **46**. Ex.[1008], 5:51-54. Also as discussed in Gr.5,Cl.[3], there are particular circumstances where node **43** is exactly **V_{SUPPLY}**. Thus, a POSA would understand the voltage at node **43** to be the PPS voltage at least during the described conditions. Ex.[1002], ¶333.

For the same reasons as discussed in Gr.5,Cl.[3], and as shown in annotated Figure 4 (annotated) below, a POSA would understand that *Steer* discloses ***a third resistor*** (annotated in dark red) ***being coupled between the positive input terminal of the operational amplifier*** (annotated in blue) ***and the positive power supply voltage*** (node **43** that is **V_{SUPPLY}** when the current through resistor **46** (**R**) is zero). Ex.[1008], Fig. 4; Ex.[1002], ¶334.

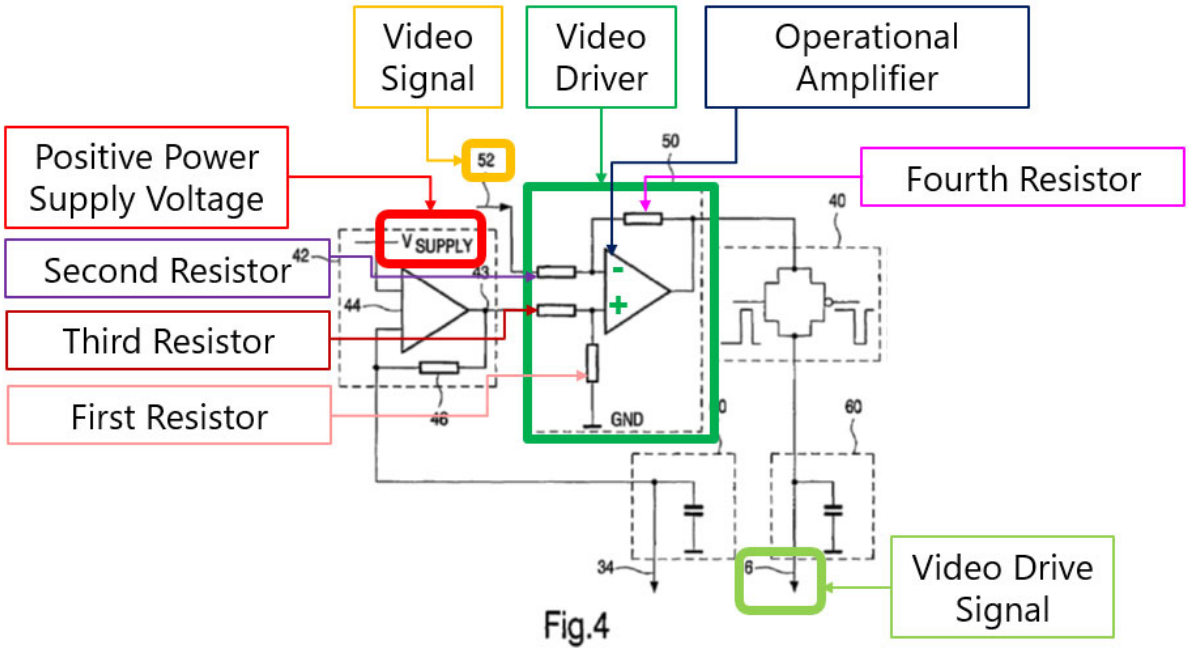


Fig.4

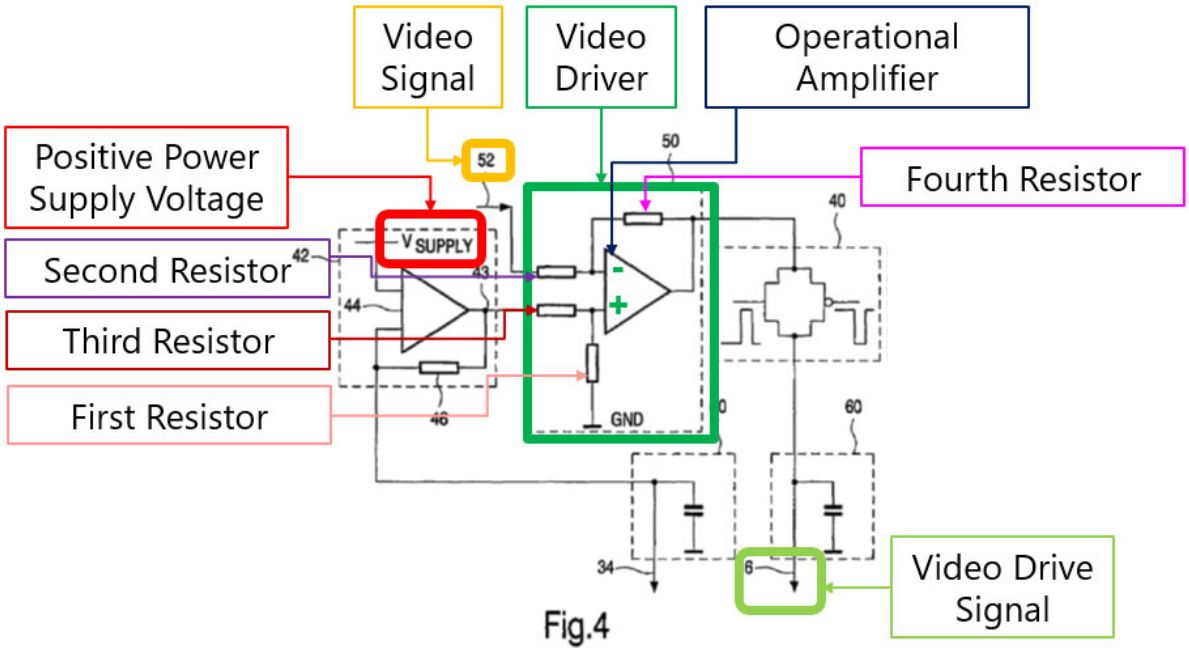
Ex.[1008], Fig. 4 (annotated).

Claim[4-E]

Fourth Resistor Coupled between the Negative Input Terminal and the Output Terminal of the Operational Amplifier

In the '521 Patent, the fourth resistor corresponds to element 106 in Figure 2.

For the same reasons as discussed in Gr.5,Cl.[3], and as shown in annotated Figure 4 (annotated) below, a POSA would understand that *Steer* discloses ***a fourth resistor*** (annotated in bright pink) ***being coupled between the negative input terminal and the output terminal of the operational amplifier*** (annotated in blue). Ex.[1008], Fig. 4; Ex.[1002], ¶¶335-336.



Ex.[1008], Fig. 4 (annotated).

IX. SECONDARY CONSIDERATIONS

To Petitioners' knowledge, there is no evidence of secondary considerations of non-obviousness tied to the claimed invention of the '521 Patent.[12] Accordingly, there is no objective evidence of non-obviousness that might warrant a finding that Claims 1-5 and 7 are patentable. Ex.[1002], ¶337. Furthermore, even if PO were able to establish any secondary considerations and a proper nexus, any such secondary considerations would be insufficient to overcome the strong case of obviousness presented in Grounds 1-5. *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007).

X. CONCLUSION

Petitioners respectfully request institution of *inter partes* review and cancelation of Claims 1-5 and 7 of the '521 Patent as unpatentable.

March 24, 2023

Respectfully submitted,

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[12] Petitioners reserve the right to rebut any purported evidence of secondary considerations of non-obviousness identified by PO.

CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATION, TYPEFACE REQUIREMENTS, AND TYPE STYLE REQUIREMENTS

This Petition complies with the type-volume limitations as mandated in 37 C.F.R. §42.24, totaling less than 14,000 words. Counsel has relied upon the word count feature provided by Microsoft Word.

Respectfully submitted,

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Date: March 24, 2023

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CERTIFICATE OF SERVICE

The undersigned hereby certifies on this March 24, 2023, a true and correct copy of the foregoing **Petition for *Inter Partes* Review of U.S. Patent No. 7,259,521**, Exhibits 1001-1012, and Powers of Attorney were served to the following parties via electronic mail and Federal Express:

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