

A 10-bit Linear R-string DAC Architecture for Mobile Full-HD AMOLED Driver ICs

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Abstract

A display driver IC prototype for mobile full-HD AMOLED display is presented. Since full-HD AMOLED display has too short driving time, conventional R-string DAC column driver cannot obtain enough internal settling time. To solve the problem, therefore, a new R-string DAC column driver architecture is proposed, which has much faster settling time with high accuracy. Also, with the architecture, one 8-bit PTL in conventional R-string DAC is replaced with much smaller two sub-PTLs, decreasing the overall driver area. The measured INL and DNL are 0.49 LSB and 0.38 LSB, respectively. The mean and maximum value of inter-channel DVO is 4.6mV and 7mV, respectively. The proposed linear 10-bit DAC fabricated on 90-nm CMOS process occupies 81% of conventional nonlinear 8-bit R-string DAC area in the same technology.

1. Introduction

AMOLED display, in the spotlight as one of the most promising next generation displays, has been successfully adopted in mobile smartphone application, based on simple voltage driving scheme like AMLCD scheme. In these days, to obtain higher image quality for high-end smartphones, AMOLED display resolution has been being increased, so even 1920 x 1080 of full-HD resolution has been introduced. However, full-HD AMOLED has very short driving time, so some technical huddles issued for conventional R-string DAC column driver architecture. In this paper, therefore, we present the detailed technical huddles, and to overcome the issue, a new R-string column driver architecture is proposed, including a new buffer amplifier with special function for the architecture.

2. Technical Huddles for full-HD AMOLED display driver

Fig.1 shows timing diagram for full-HD AMOLED display driver. For gate driver, 1920 of gate timings and vertical porch period are defined. For source driver with 2:1 channel-MUX (our target), driving periods for even and odd lines are defined with 4- μ s required time for AMOLED display. Consequently, we obtain about 2 μ s of short driving time per a horizontal line time. Note that negligible timings are not shown in the figure.

Fig.2 shows a layout of conventional R-string DAC column driver for full-HD AMOLED display. Nonlinear R-string globally provides 256 x 3 of RGB gamma references so that local 2-channel PTL (Pass Transistor Logic) selects two references from each RGB gamma according to 8-bit input data, one of which, selected by MUX, is input to a buffer to drives massive panel load. In the figure, unexpectedly, the dominant area is not the

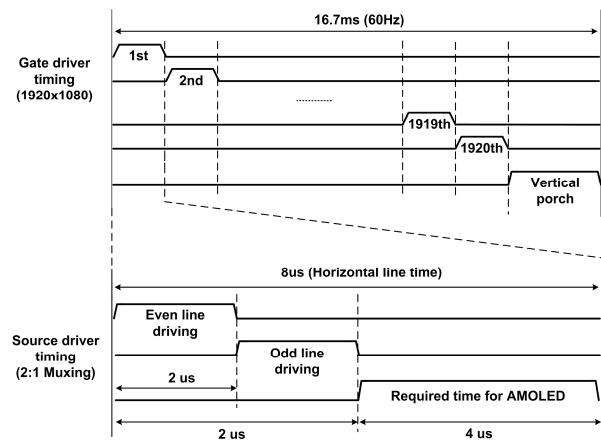


Figure.1 Timing diagram for full-HD AMOLED display driver

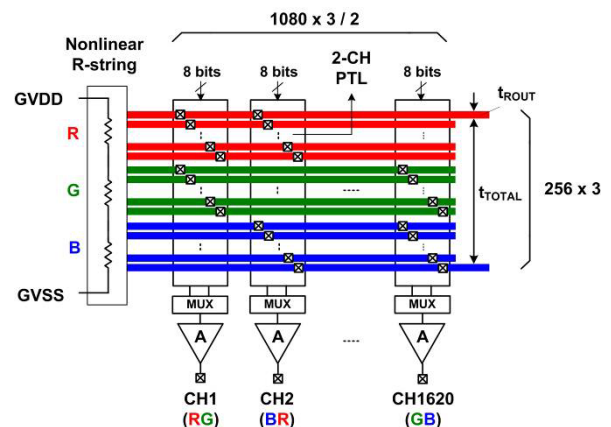


Figure.2 A layout of conventional 8-bit R-string DAC column driver for full-HD AMOLED displays

PTL-area but the routing area caused by 256 x 3 reference lines – called “routing limit”, thus to avoid serious area increase (i.e. to decrease t_{TOTAL}), the single line routing width t_{ROUT} should be designed to minimum metal width defined by design rule of process technology. However, understandably, the minimal metal width results in large routing resistance of reference lines and it causes non-small settling time with large RC time constant τ .

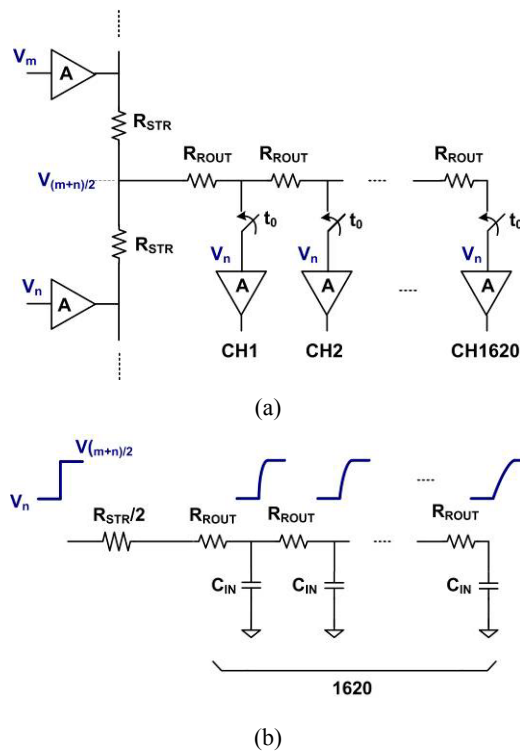


Figure.3 (a) Circuit model for the largest time constant case (b) Equivalent RC model for the case in (a)

To calculate the time constant τ of the architecture in Fig. 2, circuit model is presented in Fig.3 (a), which is the largest time constant case that all channels simultaneously select the center reference ($V_{(m+n)/2}$) between two gamma buffers with the reference V_m and V_n , while they have the voltage value V_n as their initial value for $t < t_0$. R_{STR} and R_{ROUT} are R-string resistance and routing resistance, respectively. For more simple approach, we can have simplified RC model for the case as shown in Fig.3 (b), where C_{IN} is the input parasitic capacitance of channel buffer ('A' in Fig.3 (a)). Note that non-dominant routing capacitance is included in C_{IN} . In the figure, the time constant τ of the RC network simply can be calculated as $(1620 \times C_{IN}) \times (R_{STR}/2 + 1620 \times R_{ROUT}) / 2.2$. Note that 2.2 is compensation factor for distributed models from

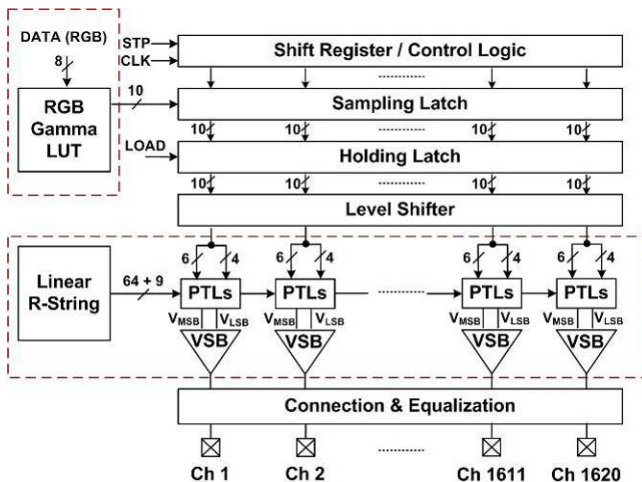


Figure.4 Proposed Column Driver Architecture

lumped calculation. Under reasonable assumption that C_{IN} , R_{STR} and R_{ROUT} typically have 50fF, 4k Ω and 10 Ω , respectively, we can finally have 0.7 μ s of time constant τ in the architecture.

Assuming that 8 gamma buffers are used (3 bits), so $V_m - V_n$ is 'full gamma range'/8, the reasonable settling percentage is 98.5% (5-bit accuracy), thus 6τ ($\approx 4.2\mu$ s) is required for that. As shown before, our driving time is only 2 μ s, so the 4.2- μ s internal settling time of conventional R-string DAC is too long to meet the time spec. To solve the settling time problem, essentially, we have to decrease the values of C_{IN} , R_{STR} and R_{ROUT} . However, it is limited to decrease each value because the size of input transistor of channel buffer (i.e. C_{IN}) should be large enough to reduce the offset voltage of channel buffer, and the resistance R_{STR} might be large enough to decrease redundant static power consumption of R-string, and the resistance R_{ROUT} might be large to minimize routing area of reference lines as mentioned previously, respectively.

3. Proposed Column Driver Architecture

To inherently overcome the settling time problem of conventional R-string DAC architecture, we propose a new R-string DAC column driver architecture as shown in Fig. 4. First of all, 8-bit RGB input data is mapped to 10-bit common code by AMOLED RGB gamma LUT – called "digital gamma control". Note that the gamma digital LUT is very small-sized so the area overhead is not too much. Furthermore, it can be much more shrunk according to process migration to smaller process technology. The converted common code is buffered and level-shifted to analog level, and the resultant 10-bit code is split to upper 6-bits and lower 4-bits used for selecting coarse voltage V_{MSB} and fine voltage V_{LSB} in PTLs, respectively. V_{MSB} is selected to one of whole range of 64 reference voltages in 6-bit resolution and V_{LSB} is selected to narrow differential voltage from 9 references in 10-bit resolution [1]. Finally, specially designed buffer amp voltage-summing buffer (VSB) accurately sums these two voltages V_{MSB} and V_{LSB} , and, at the same time, drives the desired analog voltage to massive panel load with the scheme specified by the designed connection and equalization block. Since the proposed architecture requires only 64 + 9 common reference lines for all channels, the reference routing area is very small ($t_{TOTAL} = t_{ROUT} \times 73$ in Fig. 2), so the routing metal width t_{ROUT} can be increased maximally about ten times in the same area, resulting in ten times smaller routing resistance R_{ROUT} in Fig. 3(b). Therefore, in the same calculation as previous, we can obtain about 5x faster internal settling time ($6\tau = 0.84\mu$ s), which meets the reasonable target spec 1 μ s.

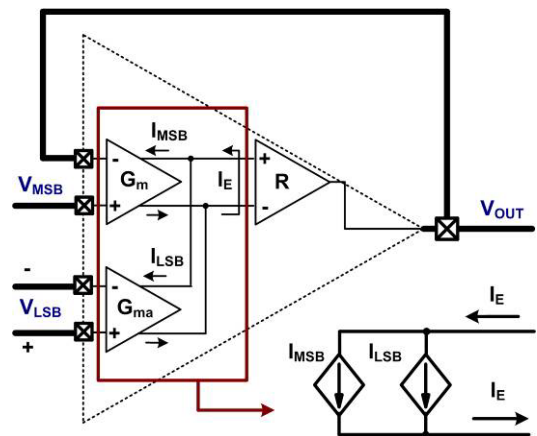


Figure.5 Conceptual schematic of proposed voltage-summing buffer

4. Voltage-Summing Buffer

Fig.5 shows conceptual schematic of proposed voltage-summing buffer (VSB), which consists of normal op-amp G_m -R with unit gain feedback and additional G_{ma} , where G_m and G_{ma} are trans-conductance (V to I) and R is trans-impedance (I to V). In the figure, each output of G_m and G_{ma} is tied in the same direction, thus the output currents I_{MSB} and I_{LSB} flow from positive input node of R and these currents comes to be equal to the error current I_E of negative feedback as simply modeled in the bottom of the figure. For input voltages V_{MSB} and V_{LSB} , the output currents I_{MSB} and I_{LSB} are $(V_{MSB}-V_{OUT}) \cdot G_m$, $V_{LSB} \cdot G_{ma}$, respectively, and the error current I_E is $-V_{OUT}/R$, therefore we can have the following equation applying these to the model.

$$V_{OUT} \cdot \left(1 - \frac{1}{T}\right) = V_{MSB} + \frac{G_{ma}}{G_m} \cdot V_{LSB}$$

,where T is op-amp loop gain $G_m \cdot R$. Since $1/T$ is negligible due to large loop gain of op-amp, following the equation, the function of voltage summation for V_{MSB} and V_{LSB} is obtained under the well-matched condition for G_m and G_{ma} ($G_m = G_{ma}$). Consequently, only with additional identical transconductance, we can simply implement buffer amp with accurate voltage-adding function. Moreover, in the proposed configuration, since the nonlinear distortions of two identical transconductances cancels out each other and their matching is very robust to temperature and process variation, very highly accurate voltage-adding function might be expected without any systematic error like the buffer in [1].

Fig.6 shows full schematic of proposed VSB DAC with rail-to-rail input/output voltage-summing buffer based on [2], generally used to cover full range of rail-to-rail DAC output in mobile display driver. Since the op-amp in [2] has both N-type and P-type trans-conductance for rail-to-rail input, both type of

additional trans-conductance $MP_{1a} \sim MP_{4a}$ and $MN_{1a} \sim MN_{4a}$ are included as shown. Therefore, P-type input pairs and N-type input pairs are in charge of low-rail to middle and middle to high-rail of DAC range, respectively. The separate range control is performed by tail switches (SW_P , SW_{Pa} , SW_N and SW_{Na}) which disable non-relevant input pairs according to MSB (D_9). Since the voltage level of V_{MSB} is widely changed while common mode voltage level of differential V_{LSB} is not, the mismatches of body effect for the two differential input pairs and channel length modulation for two tail currents might occur, resulting in the serious mismatch for G_m and G_{ma} . Therefore, the body terminals of each input pair (MP_1 and MP_2 , MP_{1a} and MP_{2a} , MN_1 and MN_2 , MN_{1a} and MN_{2a}) are connected to its common source terminal and each tail current source is cascoded (MP_3 and MP_4 , MP_{3a} and MP_{4a} , MN_3 and MN_4 , MN_{3a} and MN_{4a}) to eliminate body effect and to prevent channel length modulation, respectively.

In Fig. 6, 64-to-1 PTL with 6 MSBs ($D_9 \sim D_4$) selects V_{MSB} from 64 reference voltages equally-divided from the whole range of global R-string. 8-to-1 PTL and MUX with 4 LSBs ($D_3 \sim D_0$) select differential voltage V_{LSB} from 9 reference voltages in sub-range of global R-string divided into 1 LSB step in 10-bit resolution. When D_3 is '0', the MUX selects the highest voltage of 9 references for its output V_{LSB-} , thus the V_{LSB} has the negative voltage from -8 to -1 LSB according to the value of the following 3 LSB ($D_2 \sim D_0$) from '000' to '111', respectively. When D_3 is '1', the MUX selects the lowest voltage, thus the V_{LSB} has the voltage from 0 to 7 LSB according to the value of the 3 LSB from '000' to '111', respectively. Therefore, $GVREF_H$ and $GVREF_L$ of global R-string are $GVDD+8LSB$ and $GVSS+8LSB$, respectively, for VSB DAC to output the whole range of voltages from $GVSS$ to $GVDD$. Note that, in VSB DAC architecture, since one 8-bit PTL in conventional R-string DAC is replaced with 6-bit and 3-bit PTLs, the PTL-area is highly reduced.

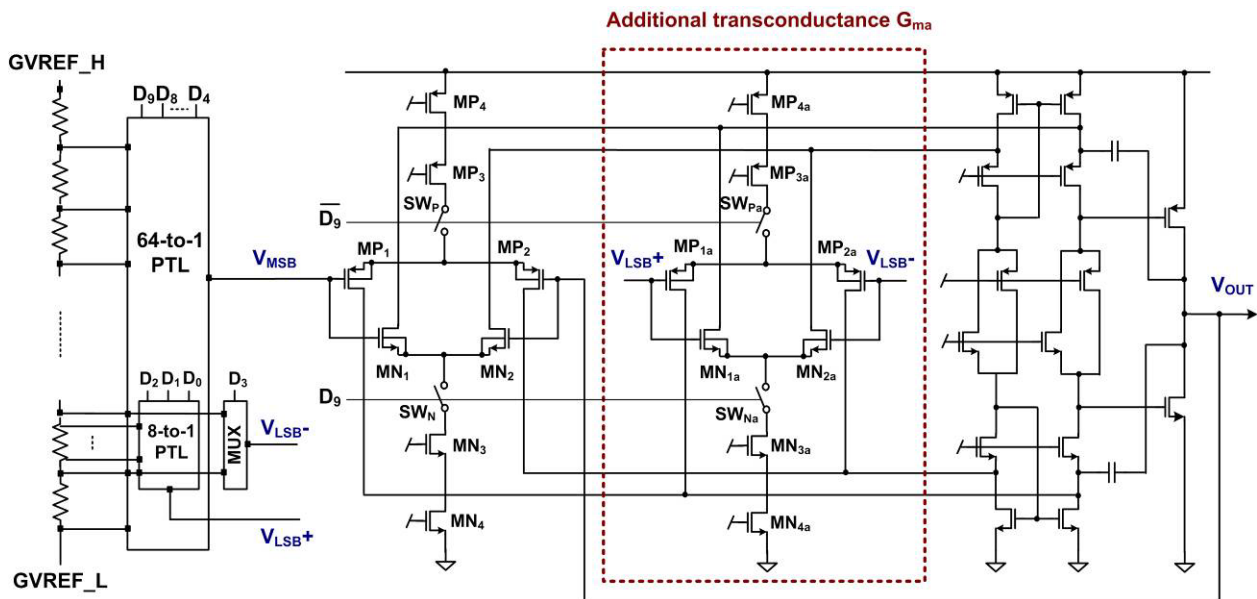


Figure.6 Full schematic of proposed VSB DAC with rail-to-rail input/output voltage-summing buffer

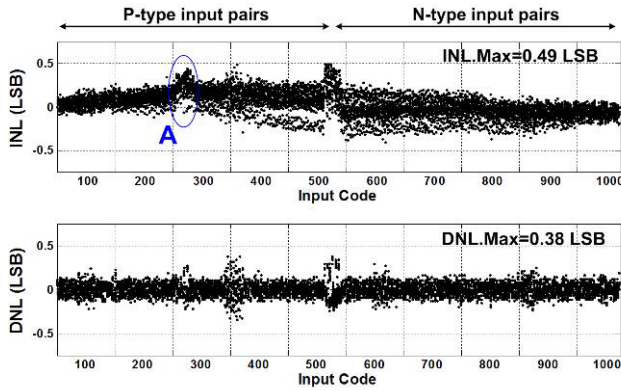


Figure.7 Measured INL and DNL for 8 channels

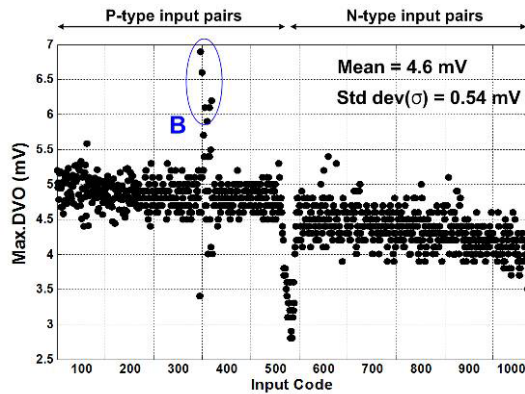


Figure.8 The measured maximum DVO for 24 channels

5. Measurement Results

Fig.7 shows measured INL and DNL for 8 channels of proposed column driver. The maximum INL and DNL are 0.49 LSB and 0.38 LSB, respectively. At the half code for range-switching by MSB from P-type to N-type input pairs, discrete profile is observed due to their different input offsets, but the continuous INL and low DNL in each range shows VSB accurately sums two voltages V_{MSB} and V_{LSB} without unexpected error. Note that the common distortion is observed in region 'A', which is caused by process defect of global R-string. Fig.8 shows the maximum inter-channel deviation of voltage output (DVO) of each code for 24 channels, without offset averaging such as chopper stabilization, etc. All those DVOs are smaller than 7mV caused by process defect in region 'B', and are uniformly distributed since the size of input pairs can be designed to meet the specified DVO and to have the same offset for both type of input pairs. The mean and standard deviation of the maximum DVOs are 4.6mV and 0.54mV, respectively.

6. Performance Summary

Table I summarizes the performance of proposed column driver. The triple-well in the CMOS process makes it possible that body terminal of N-type differential input pair is tied to its source terminal to eliminate body effect. Fig.9 shows area comparison for conventional 8-bit nonlinear R-string DAC and proposed 10-bit linear VSB DAC in the same 90-nm CMOS technology. With the same 14- μ m pitch, the heights are 330 μ m and 270 μ m for the

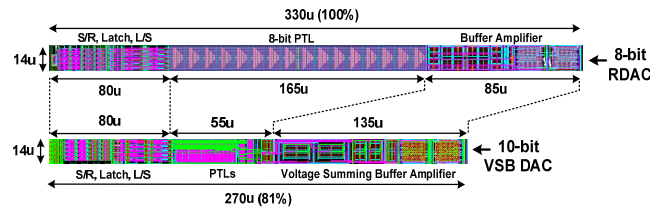


Figure.9 A layout for 8-bit R-DAC and 10-bit VSB DAC

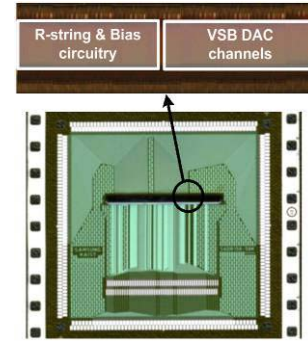


Figure.10 Die photograph and chip-on-film (COF) packaging

R-string DAC and the VSB DAC, respectively. Although the area overhead of VSB caused by additional trans-conductance is 50 μ m in height, the total area of the proposed DAC is as small as 81% area of R-DAC since the PTL-area is highly reduced to 55 μ m by applying VSB as mentioned before. Fig.10 shows die photograph and chip-on-film (COF) packaging of proposed driver IC.

TABLE I. Performance summary

Process	1.5V/5V 90-nm triple-well CMOS Process (1-poly, 5-metal, MIM-CAP)
Application	AMOLED Mobile Display
Display resolution	Full-HD (1920 x 1080)
Color depth	16.7M colors
Internal settling time	<1 μ s
Gamma voltage range	2~5V
INL/DNL	0.49LSB / 0.38LSB
DVO	4.6mV / 7mV (Mean / Maximum)
Power Consumption	1~3 μ A / Channel (Static)
Channel pitch/height	14 μ m / 270 μ m
Chip Size	20 x 4 mm ²

7. References

- [1] Changbyung Park et al., "A 10b Linear Interpolation DAC using Body-Transconductance Control for AMLCD Column Driver", *ASSCC Dig. Tech. Papers*, 6-2, Nov.2010.
- [2] Ron Hogervorst et al., "A Compact Power-Efficient 3 V CMOS Rail-to-Rail Input/Output Operational Amplifier for VLSI Cell Libraries", *IEEE J.Solid-State Circuits*, vol. 29, no.12, pp.1505-1513, DEC.1994.