

Liquid Crystal Display Drivers

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Techniques and Circuits

by

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The amateur photo in the cover was taken by S. Pennisi during a summer thunderstorm in front of Taormina, Sicily, where he lives. The idea of the cover was suggested by his friend Eng. Giuseppe Cavallaro.

Chapter 6

Drivers for Active-Matrix LCDs

AMLCDs were originally conceived for *large*-screen full-motion applications, but the demand for multimedia handheld equipments with embedded high-quality (*small*-screen) displays has recently pushed their utilization also in this market segment.¹ Nevertheless, the driver circuits for these two LCD panel categories are subject to different trade-offs:

(1) Small-area LCDs are typically battery operated and are cost driven and area driven. Thus, the evolution of the driver architecture has been aimed to the reduction of the number of IC components ultimately converging to a monolithic IC (single chip, or *combo* chip), conceptually similar to that studied in Chapter 4 for PMLCDs.

(2) Owing to the greater number of rows and columns, large-area high-resolution panels cannot be driven by a single chip, which would require an unfeasible number of pins. Besides, large-area LCDs are not strictly focused on reducing power consumption and dimensions. Their main concern is on performance. Their driver design is hence characterized by a multichip architecture where the main functionalities are implemented by separate specialized ICs.

(3) As already discussed in the previous chapter, small-area AMLCDs can be realized either in a-Si and LTPS technologies, whereas large-area AMLCDs exploit only a-Si because of the inherent wide process variations of LTPS over the substrate area. Research is however performed to overcome this limitation.

(4) Column voltages of small-area AMLCDs must have a reduced voltage swing (of about 5 V and V_{COM} -switching is adopted) to employ thin-gate-oxide transistors in the implementation of the Source Drivers, choice driven by size and cost reduction. In contrast, Source Drivers for large-size AMLCDs require a higher voltage swing in the range of 16 V, because this supports the increasing number of gray levels required (10 bit per RGB color, at least). Therefore, 20-V thick-gate transistors are adopted. In this case V_{COM} is held constant to $V_{LCD}/2$ (≈ 8 V) and V_{COM} -switching is not exploited. Dot Inversion or column and n-Line inversion is generally used in large-area AMLCDs for its better performance.

¹The demarcation between small-area and large-area AMLCDs can be roughly set to 5 in., despite this value is dependent on the application (e.g., mobile phones, smart phones, MP3/MP4 players, PDAs, etc.). This differentiation is becoming less and less evident with the increasing of the resolution.

(5) High voltage boosters must be integrated on silicon in small-size AMLCD drivers and are consequently implemented through charge pumps. In contrast, large-size panel can adopt more standard DC-DC converters which are realized in a centralized fashion and are not implemented within each source driver and gate driver IC because of the unavoidable mismatches.

Other differences between large-size and small-size AMLCD drivers will emerge in the remaining of the chapter.

Due to the strategic commercial significance of AMLCDs, their driving circuits have been the subject of intensive study and prototyping from the most important manufacturers. In this chapter we shall consider some of the main accomplishments. Section 6.1 deals with the driver architectures suitable for small-area AMLCDs (either for a-Si or LTPS technologies) and for large-area AMLCDs. Video interfaces are discussed in Section 6.2. The implementation issues of Source Drivers for small- and large-size AMLCDs, sharing many common characteristics, will be studied in Section 6.3, whereas Gate Drivers will be treated in Section 6.4.

6.1 Amlcd Driver Architectures

We shall start our discussion with small-area LCDs which are typically used in mobile equipments. The basic requirement is here low power consumption but, in addition, continuous efforts are also on enhancing image quality to provide entertainment. In this context driver ICs are key components because they greatly affect the display performance from the point of view of power consumption, image quality, and module cost.

6.1.1 Driver Architecture for Small-area a-Si Panels

The first driver architecture for small-area a-Si AMLCDs was based on several specialized ICs (see Fig. 6.1a where IC interconnections are not shown for simplicity). In order to reduce power consumption, area, and costs, the functions were progressively integrated into only two main chips (Fig. 6.1b). The first is a high-speed and low-voltage IC, which includes Timing Control logic, and DC/DC converters (a RAM block may or not be included as we will shortly see), and that drives all the source lines on the panel using an output buffer/DAC per channel. The second is a high-voltage IC that implements the gate drivers.

Presently, the monolithic IC solution, supporting both high-voltage and low-voltage transistors, is adopted (Fig. 6.1c). It implements all functions in a similar way seen for PMLCDs;

An alternative architecture under feasibility study, which integrates the gate drivers directly on the a-Si TFT backplane is shown in Fig. 6.1d, [JCL2004, KSS2004, EWK2006]. In this case the single monolithic IC supports only low-voltage transistors.

The latter design approach reduces the number of interconnect lines to the display compared to that with external gate drivers, minimizing costs and improving reliability. Unfortunately, the limited a-Si carrier mobility makes difficult the realization of more complex digital and analog circuits directly on glass.

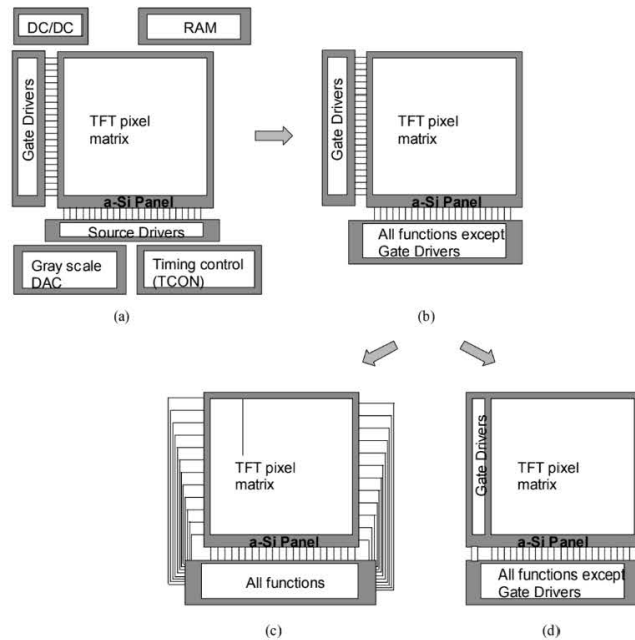


Fig. 6.1 Chipset evolution for a-Si small-size AMLCD drivers: multichip architecture (a), two-chip architecture (b), single-chip architecture (c), single-chip architecture with gate drivers integrated on the TFT backplane (d)

Since the driver IC in Fig. 6.1c is the most complete one, it will be used as a reference for the following discussion. Figure 6.2 depicts the block diagram of a possible driver IC for small a-Si AMLCDs. The architecture closely resembles that of a PMLCD already depicted in Fig. 4.1 and deserves no further explanation. The main difference is in the video interfaces (see Section 6.2), the presence of the VCOM driver and a larger non-volatile memory. In most of the cases, when a memory larger than 1-kbit is required, an E²PROM is used instead of the OTP. When the E²PROM is external, an E²PROM interface must be included.

The above architecture includes a video RAM block. More frequently, a RAM-less type driver IC is adopted. The presence or the absence of the RAM is related to the intended application. A video RAM is useful when displaying fixed pictures or low-rate-refresh images. In this case the data frame are stored into the RAM and not transmitted at the frame rate by the baseband processor to the driver, thereby reducing power consumption. In contrast, if the LCD must primarily display full motion video, storing each frame into the RAM and then retransmitting it to the source driver not only is useless, but it even increases power dissipation (without mentioning the other drawback of the augmented silicon area overhead). As a rule, drivers for panels up to QVGA resolution include a full video RAM. For higher

resolutions the driver IC does not include the RAM. Some implementation may have a partial RAM which stores some low-color-depth low-rate-refresh data. For instance, in a mobile videophone, these data may be either the clock information (which refreshes once a second or even once a minute) or the name of the calling person. They are usually written in a small portion of the display using 1 bit per RGB color.

The alternative RAM-less architecture differs from that shown in Fig. 6.2 for the absence, of course, of the RAM, as well as of the LUT/Dithering and the Oscillator. Video data presented to the driver interface are indeed in the RGB format that includes a clock signal. Therefore the internal oscillator is avoided.

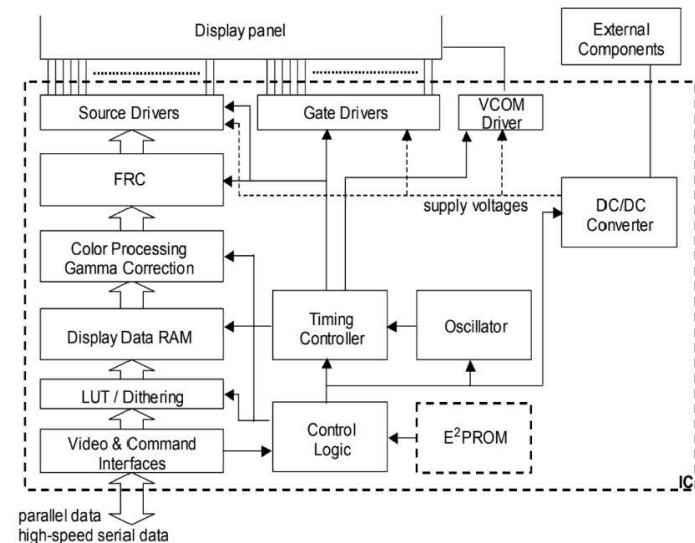


Fig. 6.2 Internal architecture of a-Si small-size AMLCD drivers. RAM-less types are for display resolutions higher than QVGA

6.1.2 Driver Architecture for LTPS Panels

With the increase of display resolution in smaller areas, the interconnections between the driver IC and the panel become more critical and the probability of electrical breaks increases, reducing in turn the yield. In addition, the cost of a flexible PCB increases with the number of I/O pins. To minimize the number of bonding connections to the panel, LTPS technologies offer a substantial advantage because they allow integration of digital and analog electronics directly on glass (approach denoted alternatively as System on Glass, SOG, or System on Panel, SOP, [NKM2004]).

For instance, if M is the number of columns, LTPS can be exploited to multiplex a number (say m) of the source lines (by implementing the demultiplexers on glass,

as shown in Fig. 6.3, showing a driver IC for an LTPS panel), thereby decreasing the number of external source lines as well as the required number of DACs plus Buffers from $3M$ to $3M/m$. This relaxes the area requirements, but mandates for circuits with faster settling, because now only the fraction $1/m$ of the row scanning time is dedicated to each pixel.

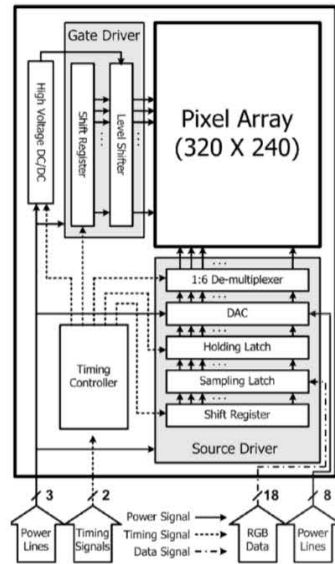


Fig. 6.3 Architecture of a 2.2-in. QVGA AMLCD LTPS panel [SCK2007]. Note the absence of a RAM and Oscillator and Interface since the incoming data are in the RGB format

LTPS TFT technology was initially adopted in high-end video projectors and digital cameras [SMH2000, K2001] in which the reduction of peripheral bonding was of outmost importance. Prototypes have been also recently developed for the consumer market of mobile devices, in the attempt to reduce costs and complexity required by the flexible PCB and to improve reliability. For instance, source/gate drivers, timing controller, DC-DC converters, interface circuits, and V_{COM} driver have been fully integrated in 2.2-in. QVGA displays [TSL2005, SCK2007].

The RAM-less architecture reported in the last referenced paper is illustrated in Fig. 6.3. Prototypes of 10.4-in. XGA and 10.2-in. VGA displays with integration of gate driver and demultiplexers for source driver have been also presented [PLY2005, YCL2007]. The recent trend is to use pMOS LTPS TFT circuits especially for medium panel sizes due to the less number of masks (four) compared to those of CMOS (six) [PLY2005]. Indeed, for small-area panels the CMOS LTPS retains its advantages even if the number of masks is higher than a-Si. However, the

benefits will be lost with increasing panel sizes due to higher manufacturing costs and lower yield, unless the integration of the whole system is possible. Therefore, to overcome these disadvantages, the approach of photomask reduction has been followed.

The main shortcoming of LTPS technologies is the high variability of process parameters, mainly threshold voltage and mobility, presenting no spatial uniformity [KDH2006]. This problem impacts especially analog circuits. For instance, if analog buffers are sensitive to threshold voltage variations, the source voltage level will be affected by a (random) offset error, and the LCD will exhibit nonuniform brightness and grey levels. Techniques to combat the effect of process tolerances are well known [ET1996] and many of these can be exploited to the design of LTPS drivers [CLH2001, JPH2004, YCS2004, LLY2005, YKL2005, KDH2006, SCK2007]. An example is shown in Fig. 6.4 representing a voltage buffer compensated to the offset (which is modelled as a concentrate voltage at the input of the ideal amplifier).

The circuit adopts a well-known autozero technique that uses three switches driven by two nonoverlapping phases ϕ_1 and ϕ_2 . The hold capacitor, C_H , samples the offset voltage during phase ϕ_1 high (T2 and T1 act as closed switches and the amplifier is in unity gain configuration). The resulting circuit is shown in Fig. 6.4b and the voltage across the capacitor is V_{OS} (also V_{out} equals V_{OS} , but this voltage is not applied to the columns). When ϕ_2 is high, the circuit becomes that shown in Fig. 6.4c, the voltage on C_H subtracts to the amplifier offset and the output voltage is V_{in} which is applied to the columns.

The main sources of error are now due to the finite gain of the amplifier causing the voltage stored on C_H to be $V_{OS} A/(1+A)$ and clock-feedthrough and charge injection effects of the switches. They can be limited by adopting large C_H values (larger than the parasitic C_{gd} of the transistors implementing the switches), and complementary switches (transmission gates in place of simple pass transistors) or even more complex structures including dummy transistors.

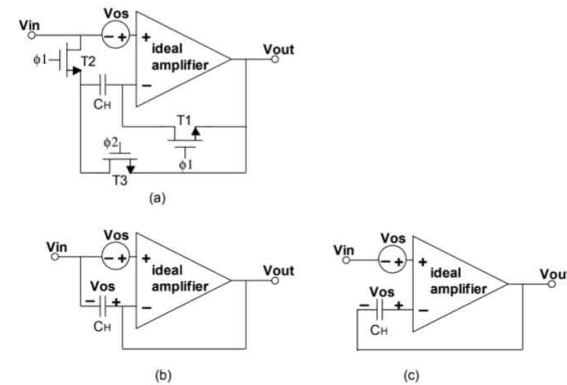


Fig. 6.4 Example of buffer amplifier with offset compensation [TSL2005]

6.1.3 Driver Architecture for Large-Area Panels

The development of improved multi domain IPS and VA pixel structures (discussed in Section 2.4.4) has been the key point to obtain wide viewing angles for large-area LCDs. However, every new mode of operation must provide its improvements while maintaining the same simple pixel driving scheme, with one gate line, one source line and one common line, as well as a standard timing controller.

We already mentioned in Chapter 5 that large-size high-resolution displays cannot take advantage of the LTPS technology, because of the large spread in the electrical characteristics of individual LTPS TFTs over the substrate area and kink effect. In contrast, the same advantages deriving from the integration of a-Si gate drivers could be in principle obtained also on large-area AMLCDs, but two main technological issues must be solved. One is the instability of a-Si TFTs, due to bias stress from an applied-voltage bias during circuit operation, causing a change in the TFT characteristics. The other is the required large width of the a-Si TFTs, extended to thousands of micrometers due to the low electrical mobility and high capacitive load of large-area panels.

As already anticipated, large-area AMLCDs adopt typically a multi-IC driver architecture. Figure 6.5 shows a block diagram where a Controller Board, including I/O Interfaces, Timing Controller (TCON), DC/DC converter, and Parallel-to-Serial decoders, is connected via a parallel bus to the Gate Driver and Source Driver sections without the need, as early observed, of a video RAM. The TCON PCB, Gate Driver PCB, and Source Driver PCB are connected together through a Flexible Printed Circuit (FPC).

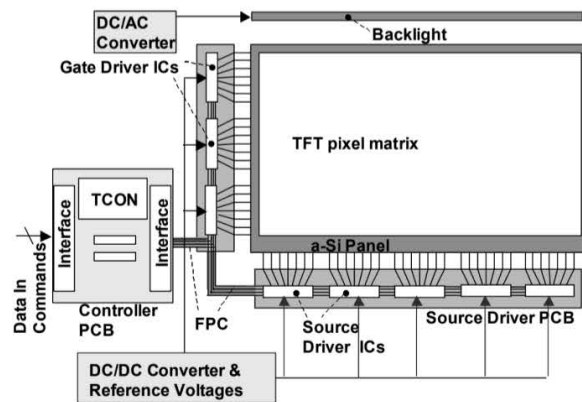


Fig. 6.5 Typical multichip driver architecture for large-area AMLCDs

The TCON of an AMLCD is conceptually simpler than that of a PMLCD. It is fully digital and operating at low voltages. The LCD gamma correction curve is stored in look-up tables within the timing controller. There may be three separate

LUTs, one for each color. The LUTs are loaded from an external E²PROM. LUT data can be digitally manipulated to compensate for temperature, ambient light, and LCD response.

In the past TCON ICs have been implemented as full custom ASIC (Application Specific Integrated Circuit) devices, with limited possibility of reuse in different LCD panel systems e.g., characterized by different resolutions, color depths, etc. (see Fig. 6.6). Recently, highly functional TCON ICs (programmable through high-level description languages such as VHDL and Verilog) have been developed supporting even non-standard resolutions and different LCD panel configurations from different manufacturers. These TCON ICs result in smaller PCBs and lower power consumption by integrating also on chip I/O data Interfaces (see also Section 6.2).

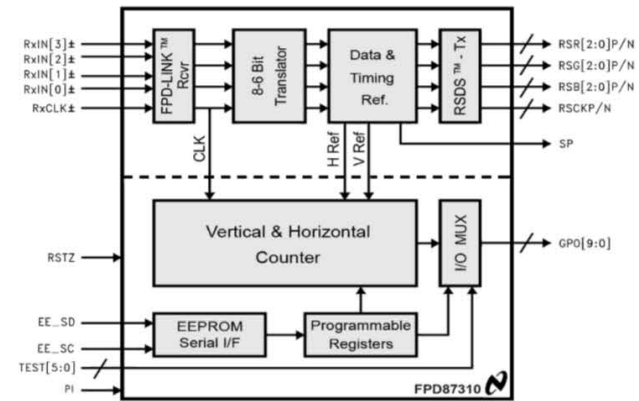


Fig. 6.6 Example of fully integrated TCON IC from National Semiconductor Corp [LL2000]

One of the main problems associated with the multi IC architecture is due to the length of the wiring between the TCON IC and the Source Driver ICs (for a 45-in. display it commonly exceeds 50 cm, being the manufacturing limit equal to 60 cm [K2005]) thus making communication difficult via a conventional bus interface. One practical solution is to use 2–4 timing controller ICs (Fig. 6.7) but it requires more components (including peripheral FPCs and connectors) and results in higher cost.

In a conventional bus interface (Fig. 6.8a) the number of wires remains the same even if we reduce the number of Source Driver ICs. Point-to-point connection (Fig. 6.8b) minimizes the length of wires and reduces their number for a lesser number of source drivers used. Besides, thanks to the decreased loading, higher speeds can be achieved. As detailed in Section 6.2, the point-to-point connection supports high-speed serial data transfer.

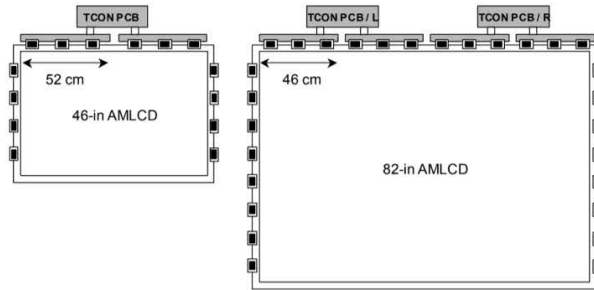


Fig. 6.7 82-in. AMLCD with two TCON PCBs

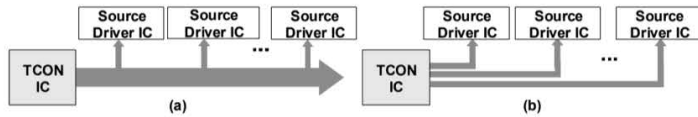


Fig. 6.8 Connection between TCON IC Source Driver ICs: (a) Parallel style (a) and (b) point-to-point style

While LCD drivers for TV application have substantially maintained the multi-IC architecture,² notebook computers (where reduction of size, weight, cost, and driving efficiency are more important objectives) have changed somewhat radically their LCD driver architecture to follow almost the same evolution of small a-Si LCDs described in Fig. 6.1, in order to reduce the chip count and flexible PCBs. Figure 6.9 shows the photograph of a conventional 15-in. AMLCD for notebook PCs. The constituting elements are clearly evidenced.

² LCD TVs main accomplishments are oriented towards improvements in color and image quality. For instance, the gray level distribution is expanded to make the level utilization more efficient and improve *contrast*. At this purpose, histogram equalization is usually adopted by adjusting the entire image frame according to a global statistics regardless of the spatial information. Such an approach may cause artefacts such as unnatural color levels. Improved schemes take also the pixel locality (edge information) into account. However, contrast enhancement typically leads to some reduction of color *saturation*. Improved solutions keep saturation, hue, and intensity of every pixel constant to ensure color accuracy. AMLCD TVs generally have 16:9 aspect ratios. Older video sources that provide the 4:3 formats will be expanded to fill the display area and, as a result, the video edge may become blurred. To avoid such defects, sharpness enhancement is performed by enlarging the intensity between vicinal edge pixels. Improved solutions avoid overshoot effects at the strong edges by dynamically varying the *sharpness* enhancement, enlarging (reducing) the enhancement for low-swinging (high-swinging) regions. Simple Frame Rate Control (FRC) schemes used to increase the color depth adopt fixed pattern to vary the intensity of pixels in temporally consecutive frames. Occasionally the fixed pattern may result in unwanted textures when the upstream video board adopts another fixed FRC pattern. DFRC (*Dynamic FRC*), reduces the risk of conflict of cascaded FRCs [LWH2005].

In this framework, since 1999 Samsung began upgrading its LCD driving architecture in a series of steps code-named Mont Blanc (MB) [BMK2005]. Table 6.1 summarizes these steps. The 12.1-in. WXGA module resulting from step MB5 is illustrated in Fig. 6.9b, a single flexible printed circuit connects the TCON board to the panel, carrying all data, power, and gamma information.

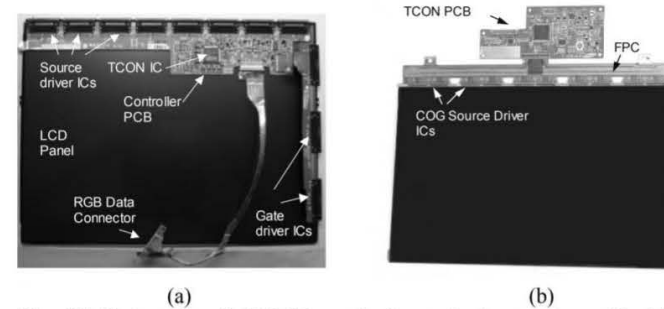


Fig. 6.9 Photographs of AMLCD panels for notebook computers with driving circuitry: (a) 14-in. conventional style; (b) 12.1-in. with integrated a-Si Gate Drivers and COG PAD ring of Source Drivers by Samsung [BMK2005]

Table 6.1 Samsung developments for notebook computers LCD drivers.

Mont Blanc Step (year)	Improvement
MB1 (1999)	The FPC connecting the source and gate PCBs was removed by routing the gate signals on the glass panel itself.
MB2 (2000)	The gate driver PCB was eliminated by routing the gate signals into and out of film-based row drivers mounted directly to the LCD glass using adhesive coated film (ACF).
MB3 (2000)	Reduced Swing Differential Signalling (RSDS) was adopted as a second-generation interface between the timing controller and column driver ICs.
MB4 (2004)	Gate drivers were integrated onto the glass itself in a-Si.
MB5 (2004)	The source driver PCB was eliminated by realizing Chip on Glass (COG) source driver ICs mounted directly onto the glass, held in place by ACF.

6.2 Video Interfaces

We have already dealt with serial and parallel interfaces adopted by PMLCD drivers in Section 4.2. The data transfer rate required by high-resolution AMLCDs cannot be supported by low speed serial interfaces which, as a rule, are employed up to the QCIF resolution. 8-bit parallel interfaces are employed from 96×128 to WQVGA, while 16-bit parallel from QCIF to WQVGA. RAM-less drivers adopt RGB or YUV

(see Appendix D) parallel interfaces employing CMOS signal levels and typically for resolutions higher than QVGA. The data bus, depending on the display architecture and color depth (6 or 8 bit/color) can be a single or dual bus of 18 or 24 conductors each. However, CMOS signalling and the increased frequency of commutations cause and unacceptable increase in power consumption and in electromagnetic interferences (EMI).

To avoid the above drawbacks while achieving higher transfer rates required by video streaming and high color depths, **high-speed serial interfaces** (HSSI) based on **low voltage differential signalling** (LVDS) techniques have been developed (always for RAM-less drivers) [IEEE1996, HG1998, K2000, M2002].

LVDS is adopted in two contexts: (1) as input interface from baseband processor to display driver and (2) as output interface from TCON (either PCB or IC) to the Source Driver ICs (see Figs. 6.5, 6.6, 6.7).

6.2.1 Low Voltage Differential Signalling

LVDS was introduced by National Semiconductor in the early 1990s and was adopted as a standard by Electronic Industries Association, later the Electronic Industries Alliance, as EIA-644. It was developed in order to provide a low-power and low-voltage alternative to other high-speed I/O interfaces for point-to-point transmission, such as emitter-coupled logic (ECL).

In an LVDS communication system, input data are first serialized, distributed to a limited number of wire pairs and then transmitted at a clock rate 7-times higher than the original. The pixel clock is also transmitted via a dedicated differential pair. A single LVDS pair with the associated transmitter, receiver, and transmission line with resistive termination (R_{TR}) is illustrated in Fig. 6.10.

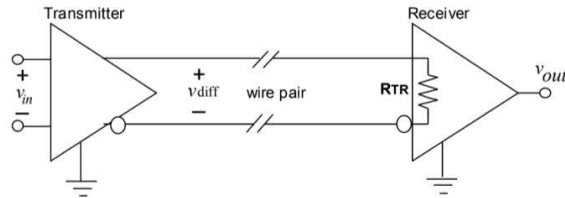


Fig. 6.10 Single transmission line of an LVDS system

The wire pair operates in a differential voltage mode, with a differential swing of ± 350 mV. This limited signal excursion (compared to the full swing of, say, 1.8 V of CMOS) improves settling time, thereby reducing propagation delay at the transmission line end. The value of the termination resistance is set to 100 Ω . This value keeps low the RC time constant of the transmission line. The differential-mode signalling causes two equal amplitude currents ($150 \text{ mV}/100 \Omega = 3.5 \text{ mA}$), but with opposite signs, to flow into the two wires. As a result, the associated electromagnetic fields are nearly cancelled out if the wires are in close proximity (EMI are strongly reduced up to 90%). Another advantage, useful in handset equipments, is that

reducing the number of wires facilitates design of narrow rotating part of rotating or sliding displays, such as those in cellular phones.

As an example, consider the input interfacing between the baseband processor and the LCD driver adopting an 18-bit data format. A parallel data bus would hence require 18 wires. LVDS reduces the number of wires to only 8 through a 7:1 multiplexing scheme. In other words, 3 couples of wires are exploited for RGB data transmission at a clock rate 7 times the original, as illustrated in Fig. 6.11. The remaining additional 3 bit per clock are exploited to convey the horizontal and vertical sync signals (HSYNC and VSYNC) and the display enable (DE). A Phase Locked Loop circuit (PLL) is also used to match the clock frequency to the transmission data rate, while a frequency divider is used in the receiver. A similar solution holds for a 24-bit data format. In this case we have 4 couples of wires for serial transmission of 24-bit RGB data and 4 bit for commands (one is a custom bit).

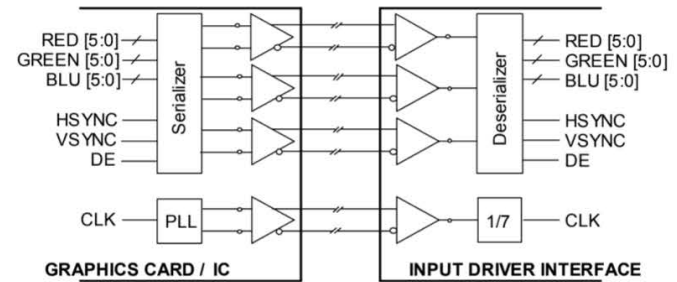


Fig. 6.11 Example of 18-bit LVDS interface

A simplified transistor-level implementation of LVDS transmitter and receiver is depicted in Fig. 6.12a, b. The current-mode transmitter is made up of four MOS switches, M_1 - M_4 , in bridge configuration. As said, I_{B1} is equal to 3.5 mA. Depending on the sign of the input voltage, $v_{in}^+ - v_{in}^-$, current I_{B1} can be switched in both positive and negative polarity over the transmission line, thereby generating the differential signal voltage, v_{diff} , across R_{TR} . If $v_{in}^+ - v_{in}^- > 0$, then M_2 and M_3 are OFF whereas M_1 and M_4 are ON. Therefore, a negative differential voltage nominally equal to 355 mV is produced. Conversely, a positive differential voltage is set across R_{TR} for $v_{in}^+ - v_{in}^- < 0$.

The receiver (Fig. 6.12b) is a simple differential amplifier acting as a comparator converting the differential-mode input voltage into a single-ended output voltage.

The LVDS standard prescribes the following admissible ranges for the *differential* and *common-mode* levels over the full range of process, supply voltage, and temperature variations:

$$250\text{mV} \leq |v_{diff}| \leq 450\text{mV} \quad \text{and} \quad 1.125\text{mV} \leq |v_{cm}| \leq 1.375\text{V}.$$

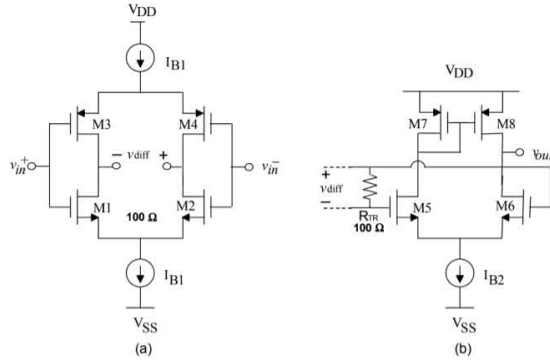


Fig. 6.12 Simplified LVDS transmitter (a) and receiver (b)

Because of the above wide limitations, the circuits in Fig. 6.12 are oversimplified and not practical. Besides, we have to set properly the output common-mode voltage of the transmitter that otherwise would be free to drift. Finally, the receiver cannot be a simple comparator, but should provide an appropriate hysteresis to avoid comparator multiple commutations for zero crossing input levels due to superimposed disturbances.

The schematic diagram of a practical and simple LVDS transmitter offering transmission speeds in the range of Gbit/s and common-mode control is depicted in Fig. 6.13 [BPV2001]. For maximum speed transfer, a termination resistor at the transmitter end, R_{TT} , is also adopted to provide impedance adaptation ($R_{TT} = 100 \Omega$). As a drawback, this doubles the current required to generate a 350-mV differential swing ($I_B = 7 \text{ mA}$ is now required for driving the $50\text{-}\Omega$ equivalent system resistance). The common-mode output voltage is sensed at the center tap of R_{TT} and compared with a 1.25-V reference via the auxiliary error amplifier implemented by M_5 - M_8 and M_{B1a} - M_{B1} . Current mirrors M_{B1a} - M_{B1} and M_{B2a} - M_{B2} have current gain equal to k ($k \gg 1$) in order to keep low the current consumption of the error amplifier and increase its loop gain. Of course, the tail current of the error amplifier must be $2 I_B / k$.

The schematic diagram of a practical and simple LVDS receiver is shown in Fig. 6.14. It implements a conventional CMOS Schmitt trigger which ensures a 25 mV–50 mV hysteresis. Full output swing is by the inverter M_7 - M_8 [USS1996]. An improved implementation that better supports the full variation of the common-mode voltage as prescribed by the standard is reported in [BPV2001].

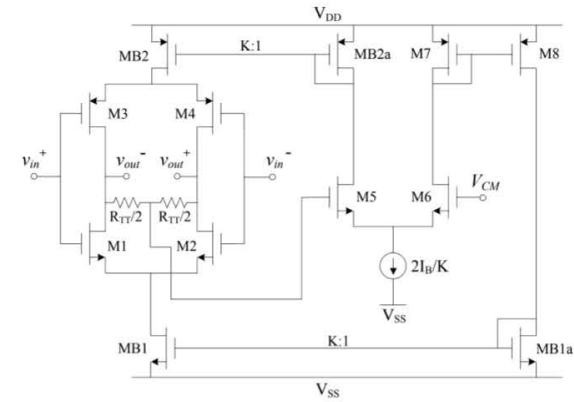


Fig. 6.13 Schematic diagram of LVDS Transmitter with common-mode control [BPV2001]

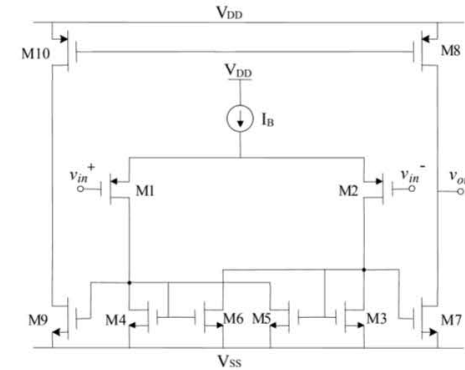


Fig. 6.14 Schematic diagram of LVDS receiver based on a Schmitt trigger (termination resistor R_{TR} is not shown) [USS1996]

LVDS is now adopted as physical layer in different communication protocols developed for usage in LCD drivers.

For example, the Mobile Industry Processor Interface (MIPI) Alliance, which deals with the definition of open standards employed in processors for mobile applications, has defined a high-speed ($>100 \text{ Mbit/s}$) communication protocol called MIPI-DSI (Display Serial Interface). It is organized in different layers with a version of LVDS as physical layer. Here, the differential voltage is $\pm 100 \text{ mV}$ and the multiplexing ratio can be higher than 7:1 (usually, from 10:1 to 30:1). In order to

optimize the power consumption, the high-speed interface is enabled only for video data transmission. The same bus is also used for low-power low-speed communication to transmit the data commands to the display. The transition from high-speed to low-power communication is done by pulling up the common-mode voltage of the differential transmission lines. Vice versa, the interface enters high-speed mode via a proper command sent when the interface is set in low-power mode.

Other proprietary high-speed LVDS-based serial interfaces are the Compact Display Port (CDP) by Nokia, the mini-RGB serial interface by Solomon Systech, Mobile CMADS (Current Mode Advanced Differential Signalling) by NEC Electronics, and the Mobile Display Digital Interface (MDDI) originated by Qualcomm and accepted by the VESA (Video Display Digital Interface) in 2002. All these approaches provide the benefits inherent to LVDS and expedite time-to-market, as the complexity of handset integration is reduced.

As already said, LVDS and its derivations are also adopted in point-to-point communication between TCON and the Source Driver ICs in large-size AMLCDs. Here, the high data rates required for video streaming cannot be supported by the traditional data transmission methods. For instance, NEC adopts the Mini-LVDS technique, while National adopts the Reduced Swing Differential Signalling (RSDS) technique only for RGB data (not commands) in which the differential swing is further lowered to ± 200 mV and multiplexing is 2:1 to relax speed requirements [LL2000].

6.3 Source Drivers

Basically, Source Drivers receive the RGB data as inputs, convert them into analog voltages and drive the columns through analog buffers.

The internal architecture of Source Drivers for small- and large-size AMLCDs does not differ substantially. The main differences are in the voltages managed (5 V or below for the former and 16 V for the latter) and in the preemphasis which is absent in small-size AMLCD drivers. Besides, the analog reference voltages of large-size AMLCDs (e.g., 0 V, 8 V and 16 V) are externally distributed (i.e., they are common to all the Source Driver ICs). These voltages cannot be generated within each different IC because they would be subject to unacceptable spreads causing in turn differences in the grey levels of each Source Driver IC.

The block diagram of a Source Driver for large-size AMLCDs is shown in Fig. 6.15. Digital RGB data are stored sequentially into the input registers and latched. These operations are usually performed with high-speed low-voltage CMOS circuits. Level shifters must be then used to boost the digital signals to higher levels compatible with the Digital-to-Analog Converters (DACs). Pre-emphasis can be used to contrast the RC delay of the columns (already described in Section 5.3.1). When required by the highly capacitive data lines of the LCD panel, output analog buffers provide both low driving impedance and high current drive capability. Charge recycler is the final block attached for power saving purposes.

The digital section is quite conventional and level shifters will be discussed in Section 6.4. Therefore, we will focus our attention on the last four blocks. Another function managed by the Source Driver is the inversion method, that will be discussed in Section 6.3.2.

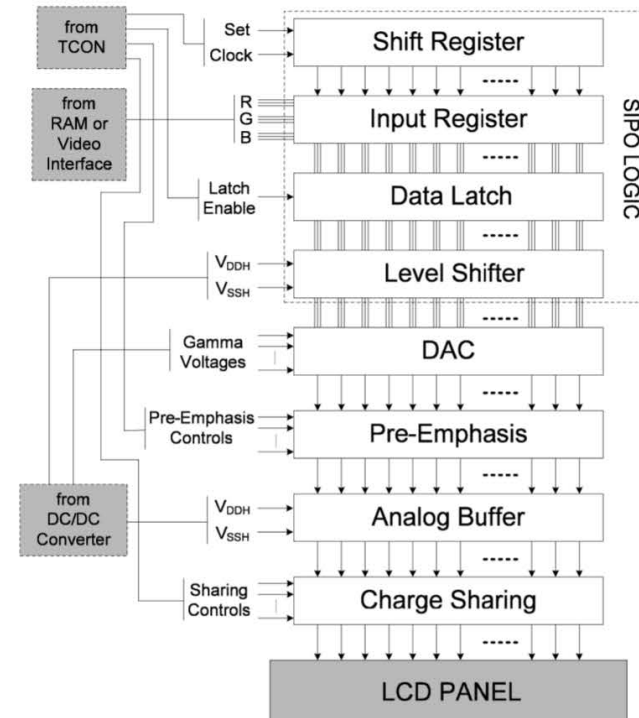


Fig. 6.15 Source Driver architecture of large size AMLCDs

6.3.1 DACs

The overall Source Driver resolution and accuracy mostly relies on the DAC section.

Up to 8-bit resolution, AMLCD drivers adopt **resistor-string DACs (R-DACs)**.

In principle, an R-DAC is made up of one resistor string providing 2^b voltage levels (b is the number of bits) and one multiplexer for each column conveying the analog column voltage associated to the input data word. Actually, this simple scheme must be modified to allow gamma voltages programmability.

As illustrated in Fig. 6.16 (which shows a 6-bit R-DAC plus buffering section), 12 **primary** gamma voltages are generated by a first-level resistor string (10 of these

primary voltages can be programmed by the control word associated to the first group of multiplexers) and buffered. A second-level string is then exploited to fit the nonlinear gamma curve by generating the remaining 52 voltage levels. Also these voltages are buffered by a second level of Buffers. Output multiplexers drive the columns. Video data appropriately select the multiplexer output voltage providing digital-to-analog conversion. The 12 primary voltages as well as their allowed programmable range are qualitatively shown in Fig. 6.18.

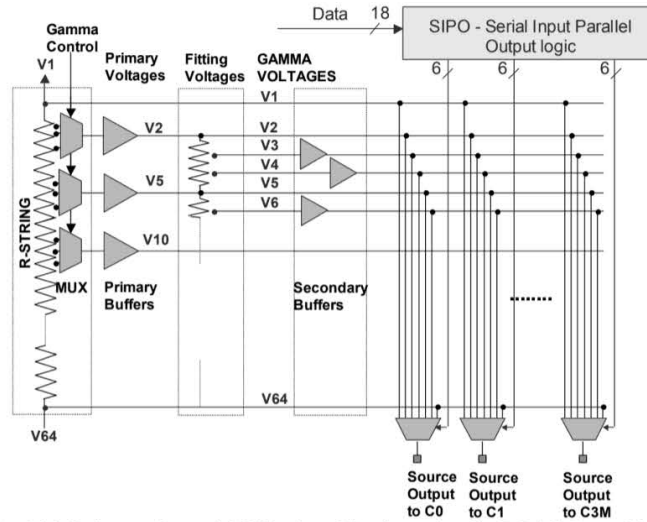


Fig. 6.16 Resistor string and MUX adopted implementing the R-DAC for positive voltages

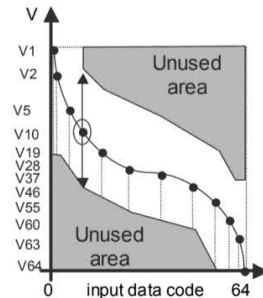


Fig. 6.17 Primary Gamma Voltages distribution, unused and allowed programmable areas

As a result, Fig. 6.16 implements a (nonlinear) R-DAC for the positive gamma voltages. A complementary R-DAC is also needed for the generation of negative polarity gamma voltages.

The MUXs in Fig. 6.17 are easily implemented through switches. A binary tree solution, depicted in Fig. 6.18a is usually adopted for its simplicity. For n bit the MUX requires a number of switches equal to $\sum_{i=0}^{n-1} 2^{n-i} = 2^n - 1$. The main drawback of this solution is that the output resistance is given by the series of each resistance switch. An alternative scheme requires an n -to- 2^n decoder and employs a number of 2^n switches [AH2002], as illustrated in Fig. 6.18b. The output resistance is now that of a single switch.

An intermediate solution employs decoded couple of bits to halve the number of switches in series with respect to the solution in Fig. 6.18a.

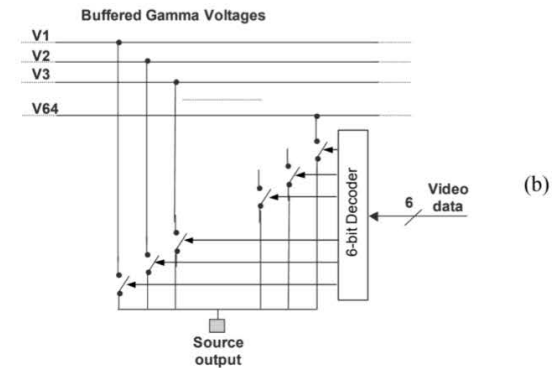
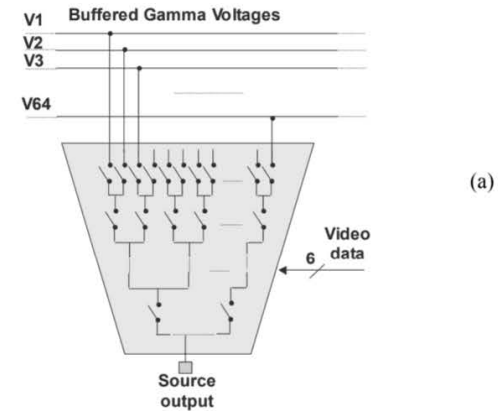


Fig. 6.18 Implementation of the multiplexers with: (a) binary tree switches, (b) with decoder

Returning to Fig. 6.16, we see also the inclusion of voltage buffers to provide the gamma voltages with current driving capability. Buffers can be placed using two different approaches. The former is in a *centralized* architecture as already described in Section 4.3.3 and illustrated in Fig. 6.17. This approach is convenient when the number of columns times three, $3M$, is much higher than the gamma levels. The alternative *distributed* buffering approach is illustrated in Fig. 6.19. Due to the large number of buffers (equal to $3M$) both area and current consumption is considerable. Therefore, attention must be paid in optimizing such performance parameters. The advantage of this solution is in the low driving point output resistance that reduces the series resistance added to that of the source line (in contrast, the output resistance offered by the MUX is dominated by the series of the n switches). The buffer performance and implementation strategies will be discussed in Section 6.3.4.

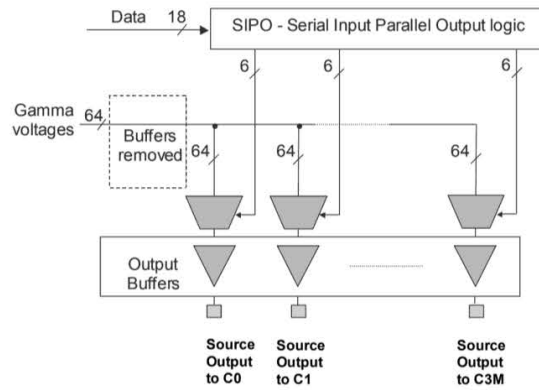


Fig. 6.19 Distributed buffer architecture

In general, the advantages of R-DACs are their monotonicity and immunity against process variations. The main drawback is the area occupation. In a 6-bit/color Source Driver, the R-DAC section occupies 30% of whole driver area, mainly because of the switches and metal routing. It can be shown that each increase in number of bits doubles the area of the R-DAC. Consequently, the area of a 10-bit DAC is 16 times as large as that of a 6-bit counterpart and the area occupation of the simple R-DAC becomes prohibitively large. To increase the color depth, many drivers for mainstream LCD TVs adopt 8-bit R-DACs expanded to 10 bit by Frame Rate Control or Spatial Dithering [HIK1992, MFT1991]. As explained in Section 3.4, these approaches work at the expense of higher frame frequency or reduction in pixel resolution.

To implement true 10-bit DACs while contrasting the area increase, various two-stage DAC architectures for TFT-LCD drivers have been proposed. One (Fig. 6.20a) cascades an 8-bit R-DAC and a 2-bit R-DAC directly [SSK2005]. According to the

authors the area increment of this DAC may be only 30% compared to the 8-bit R-DAC, but its performance is impaired by the loading effect of the second resistor string to the first one. To avoid this drawback the two strings are interfaced by two intermediate buffers [G1999] (Fig. 6.20b).

Another 10-bit DAC scheme employs an 8-bit resistor-string DAC and a 2-bit binary weighted capacitor DAC (Fig. 6.20c) [KCK2005]. This RC-DAC has a very simple structure and is area-efficient, as the area increase is only 30% compared to the area of an 8-bit R-DAC, but it is exposed to the disadvantages of a switched-capacitor circuit such as capacitor mismatch, charge injection, and clock feedthrough. Remedies to these problems will be briefly discussed in the following.

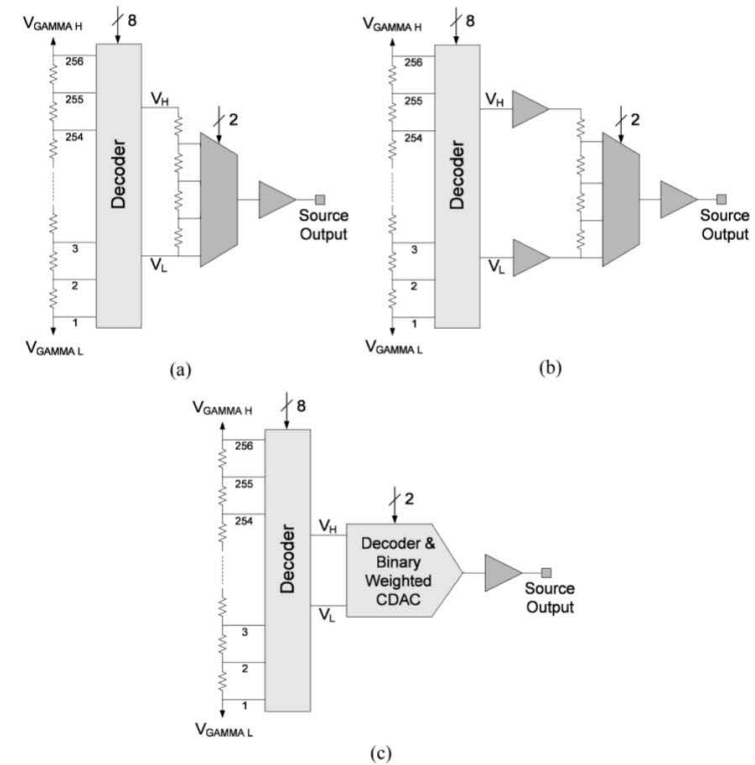


Fig. 6.20 Two-stage DACs: (a) 8-bit R-DAC followed by a 2-bit R-DAC; (b) 8-bit R-DAC followed by a 2-bit R-DAC with intermediate buffers; (c) 8-bit R-DAC followed by a 2-bit binary weighted capacitor DAC

In order to drastically reduce the die area of the source driver for high-resolution displays, the best solution is the serial charge-redistribution (or cyclic) switched-capacitor digital-to-analog converter SC-DAC, first described in [SGH1975] and applied to AMLCDs in [B2005]. Figure 6.21a shows the simplified schematic of the charge-redistribution DAC. It consists of four switches, two equal-valued capacitors, a reference voltage, and an output unity-gain amplifier. The function of the switches is as follows: S_1 is used to precharge capacitor C_S to V_{REF} (if the i -th bit, D_i , is a logical 1), while S_2 is used to discharge C_S to 0 V (if the i -th bit is a 0). Switch S_3 enables the charge redistribution between C_S and C_1 . Switch S_4 is used at the beginning of the conversion cycle to discharge C_1 to 0 V. The conversion always begins with the LSB and ends with the MSB. A conversion example for the six-bit code 110100 is also illustrated in Fig. 6.21b.

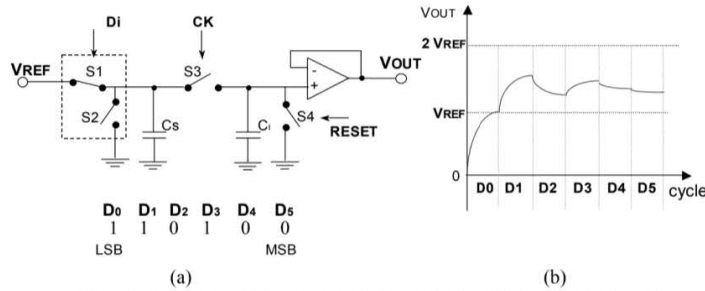


Fig. 6.21 Charge redistribution DAC (and example with 6-bit conversion)

The output voltage, after 6 clock cycles, is given by

$$V_{OUT} = V_{REF} \left(\frac{D_0}{2^6} + \frac{D_1}{2^5} + \frac{D_2}{2^4} + \frac{D_3}{2^3} + \frac{D_4}{2^2} + \frac{D_5}{2^1} \right) \quad (6.1)$$

In general for an N -bit converter we get

$$V_{OUT} = V_{REF} \sum_{n=0}^{N-1} \frac{D_n}{2^{N-n}} \quad (6.2)$$

It is apparent that the circuit requires auxiliary digital circuitry to generate the phase signals for the switches.

The amplifier offset and parasitic capacitances of the two capacitors may be the primary causes limiting resolution. An offset-compensated solution insensible to parasitic capacitances should sample the offset in both capacitors thereby compensating it when charge redistribution occurs. Besides, the two capacitors must be placed in such a manner that the charge on parasitic capacitors should not

contribute to the output voltage. Figure 6.22 shows the conversion steps of such an offset-compensated charge redistribution DAC. Furthermore, the amplifier is operated in inverting configuration (i.e., in which both the input terminals are grounded as the inverting input terminal is at virtual ground), thus minimizing the required common-mode input range of the amplifier. The last conversion step produces the ideal analog voltage unaffected by offset. In practice, offset specification is relaxed well below $\frac{1}{2}$ LSB.

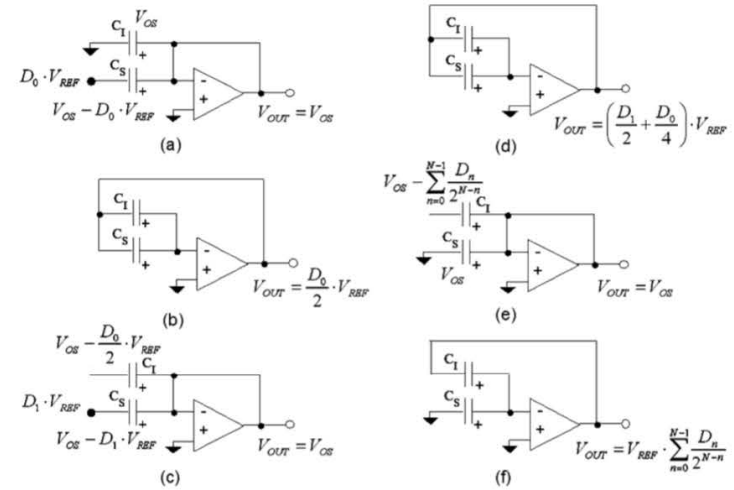


Fig. 6.22 Conversion steps of the offset-compensated charge redistribution DAC. Output and capacitor voltages are indicated

The remaining source of errors, limiting the DAC performance, are due to the capacitor mismatches and switch nonidealities (clock feedthrough and charge injection). The latter are contrasted by adopting improved switch structures (that use complementary and/or dummy transistors). Capacitor mismatches, as known, are minimized by adopting large geometries and careful layout. Two 0.25-pF capacitors were used for a 10/12-bit DAC in [B2005]. A technique to further reduce mismatches and improve linearity is obtained by exchanging the role of C_1 and C_S at each clock cycle. In this manner, any mismatch is time averaged [RW1996, RWR1998].

The SC-DAC provides an 80% reduction in area occupation over a 10-bit R-DAC. Actually, the DAC circuit is the same for any number of bits. What changes is the number of charge redistributions, i.e., the number of cycles. Since the row time is constant, this means that the clock frequency must increase for higher resolutions.

Gamma correction is in this case performed digitally by increasing the converter resolution and exploiting only a reduced set of output voltages. For instance a 12-bit SC-DAC is necessary for 10-bit color depth. This is also an advantage of the SC-DAC

in order to support three independent gamma curves for each RGB color without severely increasing the die size.

To understand frequency and settling time requirements of an amplifier used in an SC-DAC, we have to consider that the cyclic conversion of an n -bit DAC requires n charge redistribution steps. The conversion occurs with the DAC not connected to the column (and hence to the heavy capacitive load). Therefore, during conversion, the amplifier is loaded only by the DAC capacitance. The minimum value of these capacitances is dictated by the required matching properties which in turn impact resolution. Unless using the above mentioned capacitor swapping techniques, that average capacitor mismatch, the minimum capacitance allowed is in the range of 200–500 fF. If T_{CK} is the DAC clock period, the amplifier must settle in $T_{CK}/2$ under this (light) load. The above performance must be achieved under a very small standby current budget. Besides, to optimize the area occupation, the same amplifier should be used to drive the column. Therefore, the converted analog voltage must be applied to the “heavy” capacitive load (in the range of tens of picofarads for small-size panels). Fortunately, in this case the amplifier is allowed to settle in a larger time interval.

For example assuming T_{CK} equal to 2 μ s, a 10-bit SC-DAC needs 20 μ s to perform the conversion. During this phase the amplifier is loaded with a 200–500 fF load and for each charge redistribution the settling requirement is below 1 μ s. Assuming also a 60-Hz frame frequency and 320 display rows, the time left for settling, when the amplifier is loaded by the column, is 32 μ s ($=16.6$ ms/320–20 μ s) which is a sufficiently large time.

Design aspects of the analog Buffers will be discussed in Section 6.3.4.

6.3.2 Polarity Inversion

Another function managed by the Source Driver is the inversion method. Either Frame Inversion or n-Line inversion techniques are adopted in small-size LCDs for their good trade-offs between power consumption and crosstalk compensation, whereas the better Dot Inversion is prevalently adopted in large-size LCDs. For large-area panels, inversion techniques require Source Drivers with both positive and negative output polarity capability for the same digital input code.

The additional bit required by the inversion can be implemented through reverse-polarity switches that can follow two approaches. Switching polarity can be accomplished either before or after the Analog Buffers as depicted in Fig. 6.21a, b [SCK2007, MB2004, LH2004]. Switches S_I connect the positive output voltages to the column lines, while S_{IB} provide polarity reversal. This means that each buffer in Fig. 6.23a should have a rail-to-rail swing both at the input and output because the amplifier should cover all data voltages in the positive and negative reference voltage/gamma ranges [HT1994, KS2006, L2004, CM2007]. In contrast, the solution in Fig. 6.23b does not require rail-to-rail amplifiers because two types of buffers are adopted: B_H dedicated to the positive voltage range and B_L dedicated to the negative voltage range.

The second solution is preferable in terms of design simplicity and current consumption leaving performance unchanged. In fact, current consumption can be

halved by staking buffers B_H and B_L buffers that now share the same biasing current. However, the mismatch of different buffers B_H and B_L , especially in their offset voltages, can be an issue that must be taken into account through suitable offset-compensating schemes.

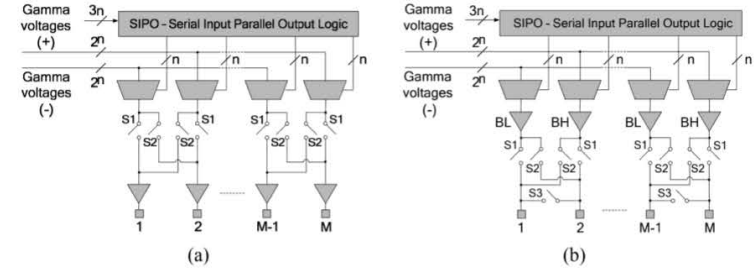


Fig. 6.23 Polarity inversion implementation with polarity reversal switches: (a) at the input and (b) at the output of the buffer amplifiers

6.3.3 Pre-emphasis

Pre emphasis (also referred to as overdrive) can be easily accomplished in the digital domain [KFT2001, SN2001, M2003, SOY2003, KPP2004] but it requires additional frame memories or look-up tables for data processing. To preserve system simplicity, analog implementations directly within the source driver are preferable [SK2007].

As discussed in (5.3.1), the pre-emphasis technique requires the generation of an adaptive pre-emphasis voltage proportional to the voltage swing of the analog video signal. For example, this can be achieved without using additional reference gamma voltages thanks to a pre-emphasis driving circuit, inserted between the DAC output and the Buffer input. It can be implemented by adding six switches and two capacitors to the conventional unity-gain amplifier as shown in Fig. 6.24, [SK2007]. The switches phases, and near/end voltage waveforms as well as the voltages stored on both capacitors, C_1 and C_2 , are shown in Fig. 6.25.

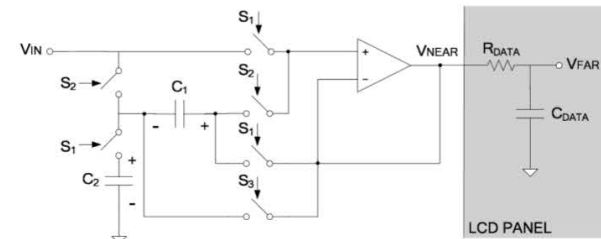


Fig. 6.24 Circuit diagram for the pre-emphasis driving method

The circuit requires three steps at the beginning of each row-line time. The synchronization phases are extracted from the master clock of the source driver.

In the first step, V_{OUT} (that is equal to V_{NEAR}) slews up to the incoming video signal voltage from the digital to analog converter (DAC). As defined in Section 5.3.1, V_{SWING} is the difference between the actual pixel voltage $V_{IN}(i)$ and the previous $V_{IN}(i-1)$ that is stored onto capacitor C_2 at the end of each row time (as shown in Fig. 6.26c). The precharge voltage V_{PRE} is proportional to V_{SWING} as described in (5.18) and reported below for the sake of clarity.

$$V_{PRE}(i) = \frac{e^{-\frac{T_{PRE}}{R_{DATA}C_{DATA}}}}{1 - e^{-\frac{T_{PRE}}{R_{DATA}C_{DATA}}}} V_{SWING}(i) \quad (6.3)$$

V_{PRE} is obtained in step 1 (Fig. 6.26a) since C_1 and C_2 are connected in series and the voltage on C_1 is

$$V_{C1}(i) = \frac{C_2}{C_1 + C_2} V_{SWING}(i) \quad (6.4)$$

Then, the voltage stored on C_1 equals $V_{PRE}(i)$ provided that

$$\frac{C_2}{C_1 + C_2} = \frac{e^{-\frac{T_{PRE}}{R_{DATA}C_{DATA}}}}{1 - e^{-\frac{T_{PRE}}{R_{DATA}C_{DATA}}}} \quad (6.5)$$

After the detection step, the pre-emphasis voltage stored in capacitor C_1 is added to the original incoming pixel voltage and applied to the unity gain buffer during the preemphasis time (Fig. 6.26b). Therefore, the positive buffer output voltage is

$$V_{OUT}(i) = V_{IN}(i) + V_{C1}(i) \quad (6.6)$$

In step 2, the far-end voltage of the data line rises up to about the original incoming analog video signal voltage from DAC.

Finally, in step 3 (Fig. 6.26c), the current video signal voltage is applied directly to the unity gain OP-AMP, and capacitor C_1 is shorted and reset and $V_{IN}(i)$ is stored onto C_2 . The near-end voltage of the data line is driven to the target video signal voltage. The three steps of driving sequences are repeated at every row-line-time.

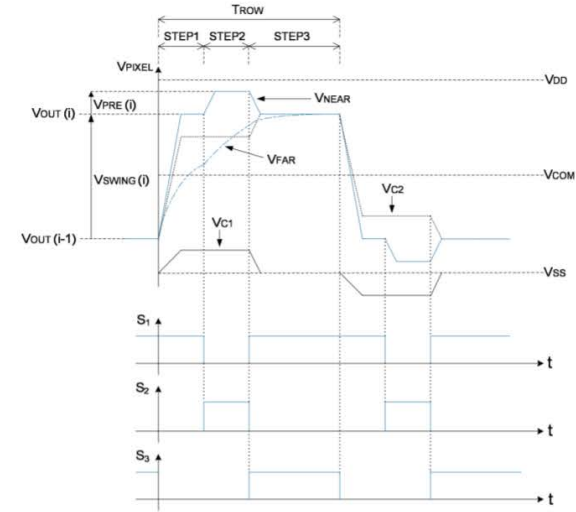


Fig. 6.25 The timing diagram and conceptual waveforms of proposed circuit for pre-emphasis driving method

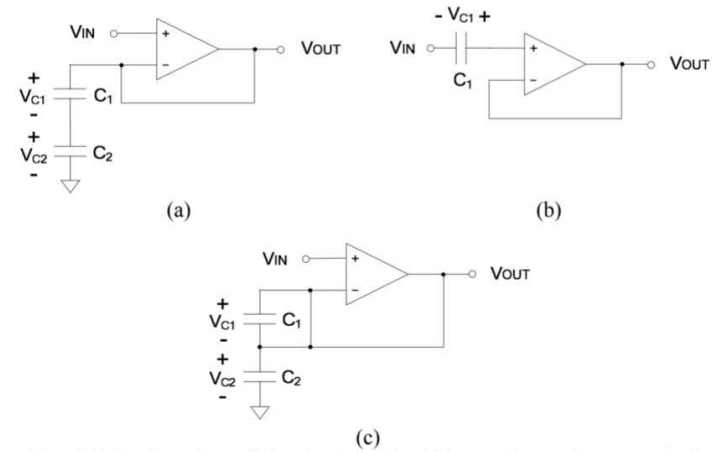


Fig. 6.26 Configurations of the circuit in Fig. 6.24 according to the pre-emphasis steps: (a) first step; (b) second step; (c) third step

6.3.4 Analog Buffers

The voltages coming from the DAC section must be properly buffered to provide low impedance driving point and current drive capability for the relatively high capacitive source load.

R-DACs usually adopt a two-stage operational amplifier in unity gain as voltage buffer. At this purpose, class AB or even B configurations have been exploited to provide sufficient slew rate values with reduced standby currents [IMS2003, L2004, KCK2005]. Describing the detailed design of a feedback amplifier is outside the scopes of this book. Good references, especially for two-stage CMOS amplifiers are found in [PP2002, GT1986, AH1987, LS1994, PPP2001].

A simplified scheme of a possible class-AB two-stage amplifier is shown in Fig. 6.27. Except for transistors M_7 – M_8 and M_{11} – M_{14} , the amplifier is a conventional two-stage class A topology. By suitably choosing the aspect ratios of M_{11} and M_7 (M_{12} and M_8) with respect to M_5 and M_3 so that

$$\frac{(W/L)_7}{(W/L)_3} > 2 \frac{(W/L)_{11}}{(W/L)_5} \quad \text{and} \quad 2 \frac{(W/L)_{12}}{(W/L)_5} > \frac{(W/L)_8}{(W/L)_3}$$

transistors M7 and M12 are biased in triode, so that M13 and M14 are normally OFF. They are however able to draw a large amount of current in a push-pull fashion under large-signal operation. It is worth noting that the limited positive common-mode range of the differential input stage requires a higher positive supply voltage. Otherwise, a rail-to-rail input stage, made up of two complementary p -channel and n -channel differential stages, must be adopted. Though two-stage amplifiers usually adopt Miller frequency compensation, the large capacitive load can be profitable exploited to provide dominant pole compensation and avoid the use the Miller capacitor.

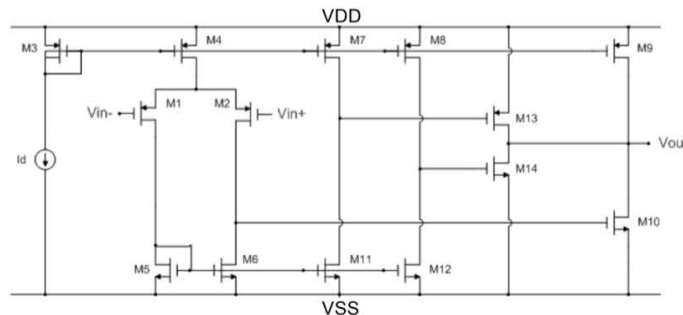


Fig. 6.27 Class-AB two-stage amplifier

The schematic diagram in Fig. 6.28 represents the amplifier adopted in the switched-capacitor DAC in [B2005]. It is made up of a folded cascode first gain stage, M_1 - M_9 , followed by a rail-to-rail class AB output stage, M_{OP} , M_{ON} . A

somewhat complex quiescent current control section is implemented by M_A - M_B (which also causes an undesirable positive feedback path, for small-signal operations). Frequency compensation is obtained through C_{C1} and C_{C2} . Note that the positive zero due to the feedforward path is avoided through the current buffer action of M_{8P} and M_{6N} (thus preventing the use of nulling resistors). All the transistors (except transistors M_{DEG}) work in their *subthreshold* region with a total DC current of about 20 μA . The application was for LCD-TV. The main advantage of the amplifier is its high gain (equivalent to three stages) and rail-to-rail output capability (due to the presence of only two transistors M_{ON} M_{OP} at the output). Disadvantages are due to the class A function of the input stage and to the Miller compensation, causing limited slew rate and gain-bandwidth product values and an increase of the area occupation.

To fit the requirements of battery-operated LCD applications, the standby current of the above circuit must be reduced more than one order of magnitude. Besides, since area occupation is more critical in hand-held devices, degeneration resistors of the differential pair M_1 - M_2 included in the original scheme should be replaced by triode-biased MOS transistors (M_{DEG} in Fig. 6.28). However, the class A input stage seems a hard obstacle for substantial current reduction without compromising the slew rate.

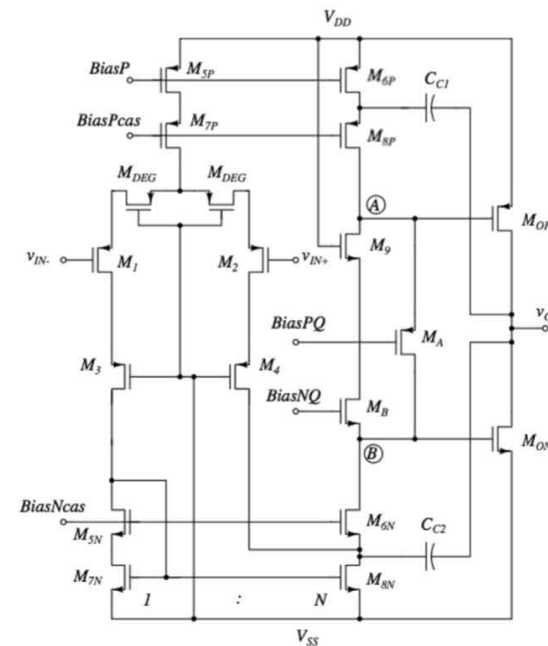


Fig. 6.28 Schematic of the transconductance amplifier in [B2005]

The amplifier, whose schematic is shown in Fig. 6.29, avoids the mentioned drawback. This topology was proposed in [LCG1984] and redesigned to meet the requirements of an SC-DAC for AMLCD drivers in [DPS2007]. It exploits a single-stage cascode topology featuring class-AB operation. Quiescent current is set by M_{B1} and M_{B2} , but under large signal condition M_1 (M_3) and M_2 (M_4) can deliver a large current, solely limited by the overdrive voltage and transistor dimensions. This current is mirrored to the output multiplied by N . The main advantage of this solution is its high achievable slew rate (owing to the full class AB operation), superior unity gain bandwidth and the absence of an explicit compensation capacitor. This reduces the area of the circuit notwithstanding separate wells for M_1 - M_8 are required to avoid the increase in threshold voltages caused by the body effect. The main drawbacks are the lower gain (it is equivalent to two gain stages, if required this value could be increased by adopting well-known gain-boosting techniques [SG1990, BG1990, A2006]) and reduced output swing, due to cascoding.

It should be also observed that the limited common-mode input range is not a real limitation as the amplifier will operate in inverting configuration (i.e., with both inputs grounded). Finally, the transfer accuracy of current mirrors that may be impaired by the subthreshold operation results to be adequate thanks to the adopted cascoded topologies that strongly reduce the channel-length modulation effect.

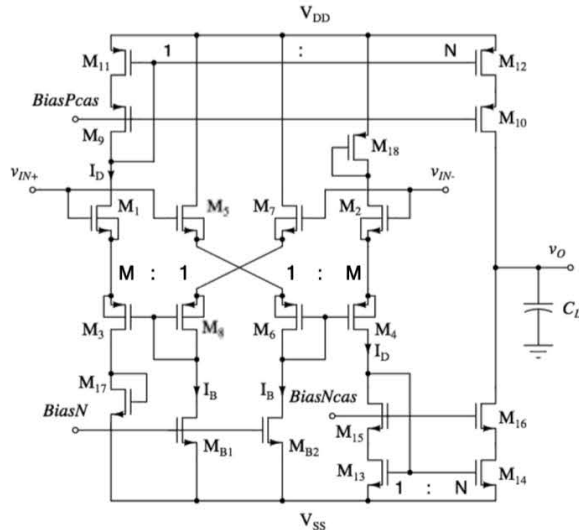


Fig. 6.29 Schematic of the transconductance amplifier in [DPS2007]

As reported in [DPS2007], the amplifier was implemented in the STMicroelectronics HVG8 process with 0.18- μm CMOS technology. Using a total standby current as low as 670 nA, it exhibits a DC open-loop gain of about 80 dB,

and a gain-bandwidth product and phase margin around 2 MHz and 70° , with a load capacitance of 500 fF (the one used in the SC-DAC). Besides, the solution provides a slew rate equal to 27 V/ μs and a settling time at 0.01% of the final value equal to 800 ns. Area was smaller compared to alternative solutions and was $17.6 \mu\text{m} \times 40 \mu\text{m}$.

The amplifier can be used in unity gain also to drive the column load. Assuming a 10-pF load, the settling time at 0.01% of the final value was about 9.4 μs .

6.3.5 Charge Sharing

Power dissipation in a conventional source driver has three contributions:

- *Digital part.* It represents usually less than 1/10 of the total power dissipation. It is hence negligible.
- *Static power.* It is due to DC bias currents in resistor strings and buffer amplifiers.
- *Dynamic power.* It is consumed in charging capacitive outputs. It is the relevant part.

Charge sharing is a technique for recovering some of the energy that is stored into the display, reducing the dynamic power consumption of source drivers. In a dot-inversion driving method, half of the pixels in a column is driven positively and the other half is driven negatively. Charge sharing is performed by shorting the column terminals together at the beginning of each row addressing before the source buffers are connected to the columns. In such a way, the source lines voltage is averaged so that when the buffers are let to drive the columns they do not start from the most extreme voltage, but from an intermediate value, saving power. If properly designed, this technique may even fasten the rise and fall times because the short provides a very low impedance high-speed path. Figure 6.30 shows a possible implementation of the charge sharing technique. Two series of switches controlled by signal CR are used to connect the columns either to the buffers or together. The associated main voltage waveforms are exemplified in Fig. 6.31. The positively (negatively) driven pixel voltage is assumed equal to V_H (V_L). During the small time interval in which CR is high the charge sharing process occurs and the pixel voltages are averaged to V_{COM} .

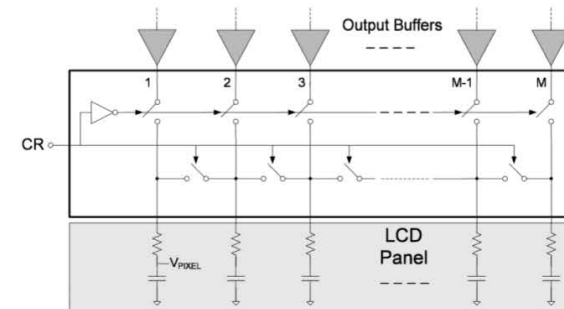


Fig. 6.30 Simple charge sharing circuit

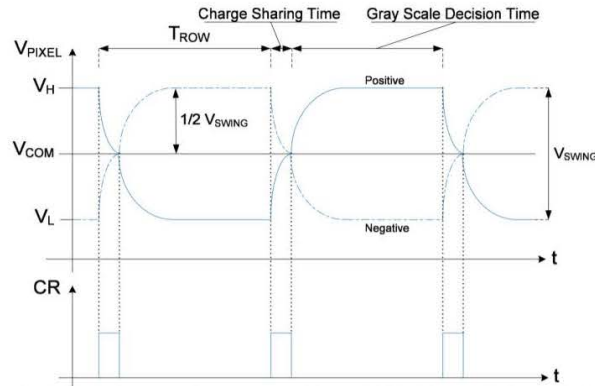


Fig. 6.31 Timing diagram and output waveforms of the charge sharing solution in Fig. 6.30

The simple charge-sharing technique has a power efficiency limited to only 50%. An efficiency of 66.6% is obtainable by the so called *triple charge-sharing method* [SCK1999]. Here, about two-thirds of the total voltage swing of data line is provided by charge sharing between source line and an additional large external capacitor, C_{EXT} , with a negligible area penalty and without increase in the circuit complexity.

C_{EXT} acts as an additional power supply provided that $C_{EXT} \gg M C_L$, where M is the number of the outputs and C_L is the capacitance of a single source line.

The source driver architecture that uses triple charge sharing is shown in Fig. 6.32. Compared to the simple approach, other than C_{EXT} , it requires four control signals, AMP, SEL₁, SEL₂, SEL₃, and another set of M switches.

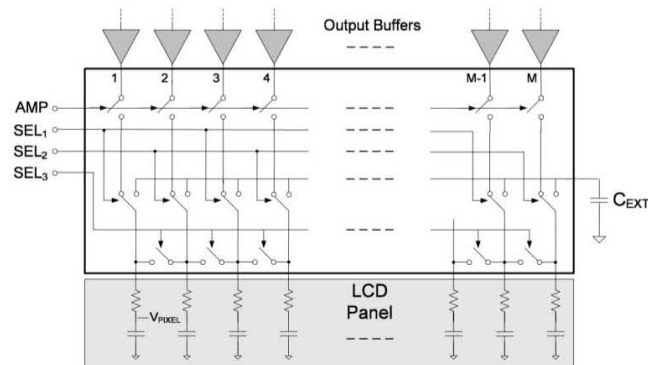


Fig. 6.32 Triple charge sharing circuit

The operation of the triple charge sharing can be understood through the aid of Fig. 6.33. Here it should be noted that the swing of the output buffers to charge the source line capacitance is reduced to a third compared to that of the conventional source driver. The remaining two-thirds of the swing are accomplished through triple charge sharing: (1) among odd lines, (2) among all lines, and (3) among even lines and the external capacitor.

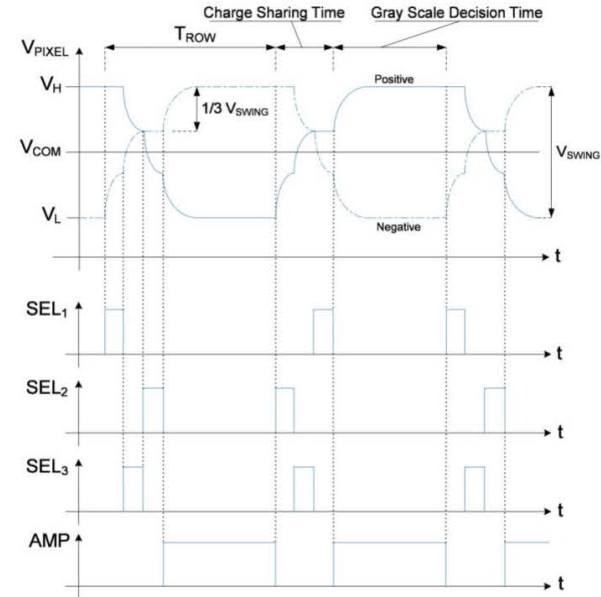


Fig. 6.33 Timing diagram and output waveforms of the triple charge sharing solution in Fig. 6.32

Up to 75% saving efficiency in AC power consumption of the TFT-LCD column driver can be obtained by multi-phase charge-recycling technique (75% is theoretically obtainable with infinite phases) [YGC2003]. This technique is easy to be implemented because it does not require any external capacitor in dot inversion driving. Figure 6.34 exemplifies the approach in which four columns are grouped into one set with switches controlled by signals S_1 - S_3 . Related waveforms are illustrated in Fig. 6.35, where column voltages for the four columns O_1 , O_2 , O_3 , and O_4 are shown in particular. AC power is dissipated in the last step with the worst case voltage swing of $(V_H - V_L)/2$ for half columns and $(V_H - V_L)/4$ for the remaining half. The power saving is up to 62.5% with respect to a source driver without charge sharing. Expanding this concept, more column lines can be grouped as one set to further reduce power consumption.

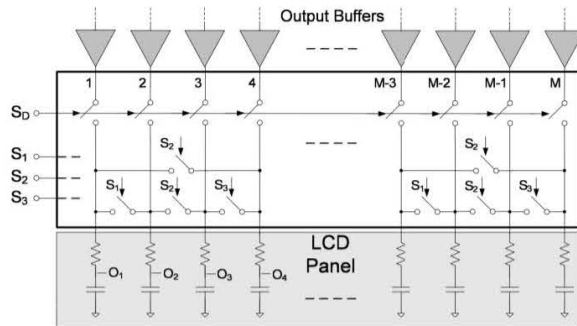


Fig. 6.34 Multiphase charge sharing circuit

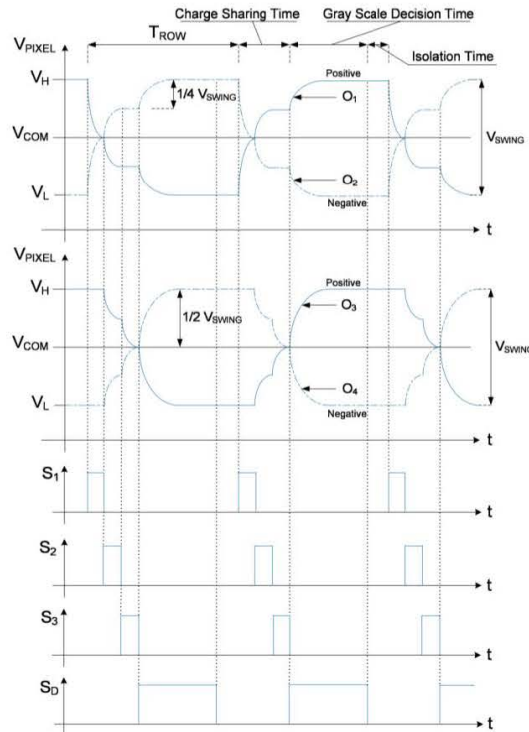


Fig. 6.35 Timing diagram and output waveform of the multiphase charge sharing solution in Fig. 6.34

6.4 Gate Drivers

The Gate Driver has to turn on the TFT switches of each row in a row-by-row succession. A gate driver generally includes a shift register, a level shifter and output buffers, as shown by the block diagram in Fig. 6.36. The scan impulse voltage is provided by a shift register operating at low supply voltage to contain power consumption. However, as discussed in Section 5.1, TFTs must be driven by large gate-source voltages (from 15 V to 20 V in the ON state and from -5 V to -8 V in the OFF state), a dual level shifter is therefore necessary. The output digital buffers, required in large-area and/or high-resolution displays, are used to enhance the driving capability for adequate switching speed.

The level shifter *must precede* the shift register if the gate driver is integrated in the panel.

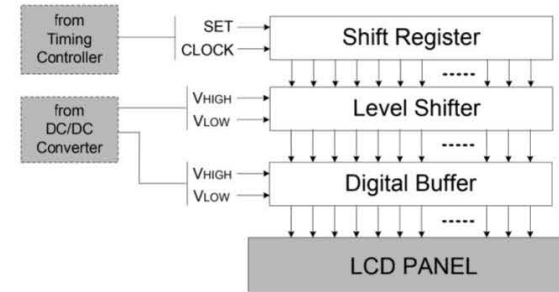


Fig. 6.36 Block diagram of the gate driver

6.4.1 Shift Registers

The simplest gate driver includes a shift register with a walking '1' data running at the row scan rate. The well-known diagram of a shift register is illustrated in Fig. 6.37a. It consists of a chain of flip flops (or latches). A set pulse is presented at the input and is shifted right one stage for each high-to-low (or low-to-high) transition of the clock signal as shown in Fig. 6.37b. If the shift register is formed by latches the input is transferred in correspondence of the clock high (or low) level.

Driver ICs fabricated in monocrystalline silicon typically adopt the solution in Fig. 6.37a, implemented with standard CMOS logic which minimizes the static consumption.