

1 UNITED STATES PATENT AND TRADEMARK OFFICE

2
3 BEFORE THE PATENT TRIAL AND APPEAL BOARD

4
5 SAMSUNG DISPLAY CO., LTD; SAMSUNG ELECTRONICS CO.,
6 LTD.; and SAMSUNG ELECTRONICS AMERICA, INC.,
7 Petitioners

8 v.

9 POLARIS POWERLED TECHNOLOGIES, LLC,
10 Patent Owner

11
12 Case No. IPR2023-00771

13 U.S. Patent No. 7,259,521

14
15 Deposition of ALEX Z. KATTAMIS, PH.D., P.E.

16 Conducted Virtually

17 Tuesday, June, 4, 2024

18 12:03 p.m. EDT

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21 Stenographically reported by: Judith E. Bellinger,
22 RPR, CRR, CSR-TX CCR-WA, CCR-NM

1 Deposition of ALEX Z. KATTAMIS, PH.D., P.E.,
2 conducted virtually.

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11 Pursuant to notice, before Judith E.
12 Bellinger, Registered Professional Reporter,
13 Certified Realtime Reporter, and Notary Public in
14 and for the State of Maryland.

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A P P E A R A N C E S

ON BEHALF OF THE PETITIONER:

MARK ODA, ESQUIRE

ELIOT D. WILLIAMS, ESQUIRE (DC office)

NEIL SIROTA, ESQUIRE (New York office)

BAKER BOTTS, L.L.P.

101 California Street

Suite 3200

San Francisco, CA 94111-5802

415.291.6234

ON BEHALF OF THE PATENT OWNER:

ANDREW G. HAMILL, ESQUIRE

KRAMER ALBERTI LIM & TONKOVICH LLP

577 Airport Boulevard

Suite 250

Burlingame, CA 94010

650.825.4300

- and -

1 A P P E A R A N C E S C O N T I N U E D

2

3 JASON A. FITZSIMMONS, ESQUIRE

4 RICHARD M. BEMBEN, ESQUIRE

5 STERNE, KESSLER, GOLDSTEIN & FOX

6 P.L.L.C.

7 1101 K Street NW

8 Washington, DC 20005

9 202.371.2600

10

11

12 ALSO PRESENT:

13 Jesse Castro, Planet Depos Technician

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C O N T E N T S

EXAMINATION OF ALEX Z. KATTAMIS, PH.D., P.E.	PAGE
By Mr. Hamill	6

E X H I B I T S

(Attached to the transcript)

Kattamis Exhibits:	PAGE
Exhibit 1 Patent Owner's Notice of Remote Deposition of Alex Z. Kattamis, Ph.D., P.E.	7
Previously Marked: Exhibit:	
Exhibit 1001 United States Patent Number 7,259,521 B1	9
Exhibit 1006 Unites States Patent Application Publication Number US 2005/0190128. A1	20
Exhibit 1015 Supplemental Declaration of Alex Z. Kattamis, Ph.D., P.E., For Inter. Partes Review of U.S. Patent. No. 7,259,521	16

1 P R O C E E D I N G S

2

3 ALEX Z. KATTAMIS, PH.D., P.E.,

4 being first duly sworn, was examined
5 and testified as follows:

6 EXAMINATION BY COUNSEL FOR THE PATENT OWNER

7 BY MR. HAMILL:

8 Q Please state your name for the record.

9 A Alex Z. Kattamis.

10 Q And where are you located today?

11 A In Baker Botts' offices in Midtown
12 Manhattan.

13 Q And who's in the room with you today?

14 A Mark Oda of Baker Botts.

15 Q Anyone else?

16 A No.

17 Q And before we got started you mentioned
18 that you had some documents with you.

19 Can you let me know what those
20 documents are again, please?

21 A Sure. I can list them off, if you'd
22 like.

1 I have my declaration, the original
2 one, a CV, the supplemental declaration, my
3 supplemental declaration, the deposition notice,
4 that's in the -- this smaller binder. And then in
5 the left binder, I have --

6 MR. ODA: By exhibit number.

7 A I have Exhibit Number 1001, 1004, 6, 7,
8 8, 9, 1010, 12, 1014, 1016, 1017, and 1018, and
9 the institution decision.

10 Q And, Dr. Kattamis, did you do anything
11 to prepare for this deposition?

12 A Yes, in preparing for the deposition, I
13 reviewed many of the documents I just listed and
14 spent time reviewing my declaration, as well as
15 the declaration of Mr. Credelle, and then had
16 discussions with Mark Oda.

17 Q Okay. Let's introduce the deposition
18 notice as Exhibit 1. That's the only -- I think
19 that's the only exhibit that's not already marked.

20 (Kattamis Exhibit 1 marked for
21 identification and attached to the transcript.)

22 Q Okay. Dr. Kattamis, do you understand

1 that the testimony you're providing today will be
2 used in inter partes IPR2023-00771?

3 A Yes.

4 Q And this matter pertains to U.S. Patent
5 7,259,521.

6 Are you comfortable if we refer to it
7 by the last three digits, so, '521?

8 A Yes, that works.

9 Q And if I use the acronym "POSA" or
10 "POSITA," do you understand that to be a person of
11 ordinary skill in the art?

12 A Yes, I do.

13 Q And, Dr. Kattamis, are all -- have you
14 provided opinions in this matter?

15 A Yes, I have.

16 Q And are all of your opinions set forth
17 in your declarations?

18 A Yes.

19 Q And are the bases for your opinions in
20 your declarations?

21 A Yes.

22 Q And your supplemental declaration, did

1 you review it before submitting it?

2 A Yes.

3 Q Are there any errors that you've
4 noticed in that declaration?

5 A No technical errors that I've noticed.
6 A typo at one point, but not substantive.

7 Q Okay. Do you know what typo that is?

8 A There is one point where I think I
9 refer to it as the '512 instead of '521.

10 (Exhibit 1001 previously marked for
11 identification and attached to the transcript.)

12 Q Okay. Let's turn to Exhibit 1001.
13 That would be the '521 patent.

14 A I'm there.

15 Q And can you, please, turn to page 3 of
16 Exhibit 1001. It has Figures 3 and 4.

17 A Yes, I see it.

18 Q I'd like to ask you some questions
19 about the embodiment described in Figure 4.

20 Are you familiar with this embodiment?

21 A Yes, I am.

22 Q And this is the embodiment that has a

1 clamp circuit, right?

2 A Yes.

3 Q Okay. Please turn to page 7 in
4 Exhibit 1001.

5 Do you see toward the bottom of column
6 6 is where the specification discusses this
7 embodiment?

8 A Yes, at line 45.

9 Q Right. That's where it starts. That's
10 right.

11 And in this embodiment, VDD refers to
12 the positive power supply voltage of the display,
13 right?

14 A Yes.

15 Q Okay. If you can look down, there's a
16 passage starting at line 61, the paragraph there,
17 it says "As thus configured, when the Blanking
18 signal is asserted at the beginning of each video
19 line to re-establish the black reference of the
20 video display, transistor M3 is turned on and the
21 right plate of capacitor C1 is charged up to the
22 power supply voltage VDD."

1 What does it mean for the right plate
2 capacitor C1 to be charged up to the power supply
3 voltage VDD?

4 MR. ODA: Objection. Form.

5 A Well, as it states when transistor M3
6 is turned on, the right plate, I believe, is just
7 what they're referring to as the negative terminal
8 C1, is charged up to VDD.

9 Q Okay. Then the next sentence, starting
10 on line 65 reads "In this manner, the power supply
11 voltage, VDD, including any voltage drifts, is
12 stored on capacitor C1 as the clamping voltage
13 Vclamp."

14 And so, is the voltage VDD stored on
15 that capacitor C1?

16 A Yeah, as it says, yep, VDD is stored on
17 the right plate of C1.

18 Q Okay. Then continuing onto the next
19 sentence. So that starts on line 67 of column 6
20 and then goes on to column 7 "When the Blanking
21 signal is deasserted, transistor M3 is turned off
22 and no longer drives node 322."

1 And it continues -- continue to the
2 next sentence as well. "Instead, the video signal
3 Video.DAC is applied through amplifier 306 and is
4 added to the clamping voltage Vclamp stored on
5 capacitor C1."

6 And so, here, it mentions the
7 transistor M3 being turned off. So does this mean
8 that the voltage VDD, stored on the right side of
9 capacitor C1, is the value of VDD at that moment,
10 when the transistor M3 is turned off?

11 MR. ODA: Objection. Form.

12 A Yeah, that's what it says here, yes.

13 Q Okay. Then let's skip down to line 9
14 in column 7.

15 It says "More specifically, the video
16 driver 302 is effective in removing voltage drifts
17 in the power supply voltage but" not necessarily
18 -- "but does not necessarily remove noise or
19 glitches in the power supply voltage from
20 impacting the video drive signal. This is because
21 the clamping voltage Vclamp is recharged only once
22 for each video line and thus any noise or voltage

1 glitches that may appear on the power supply
2 voltage VDD will not get charged to capacitor C1
3 until the next Blanking period."

4 So, my first question here is, what
5 does it mean that noise or voltage glitches, that
6 may appear on the power supply voltage VDD, will
7 not get charged to the capacitor C1 until the next
8 Blanking period?

9 MR. ODA: Objection to form.

10 A The way I'm reading it, it means that
11 VDD, or that signal that's applied to the right
12 terminal of C1, would remain.

13 Q Sorry, what do you mean by "will
14 remain"?

15 Or "would remain"?

16 MR. ODA: Objection to form.

17 A The signal that's applied during that
18 Blanking period. So the signal that's applied to
19 the right temp -- right plate, excuse me, of C1
20 would remain until the Blanking signal's
21 reasserted.

22 Q So the value of VDD, essentially, at

1 the moment M3 is turned off, that value would be
2 stored on the right side of capacitor C1 until
3 it's reprogrammed?

4 MR. ODA: Objection. Form.

5 A Yeah, I think that's accurate.

6 Q And so, in this statement, is it --
7 would you agree that any voltage glitches that are
8 part of VDD, when M3 is turned off, would be
9 stored on capacitor C1?

10 MR. ODA: Objection. Form.

11 A Yeah, that is -- that's what it states.

12 Q And that's your understanding of this
13 embodiment, right?

14 MR. ODA: Objection. Form.

15 A Yes.

16 Q Okay. So there are no types of voltage
17 glitches that are part of VDD that are not stored
18 on capacitor C1, at that moment when the
19 transistor M3 is turned off, right?

20 MR. ODA: Objection. Form.

21 A No. I think it's more -- I mean, as it
22 states, voltage, right, power supply voltage does

1 not necessarily remove noise or glitches. It
2 doesn't mean it can't.

3 Q Right. But that's a statement about
4 removing -- that's about preventing noise or
5 glitches from impacting the video drive signal,
6 right?

7 MR. ODA: Objection. Form.

8 A Could you restate your initial question
9 or read it back?

10 Q Yeah. So my question was, when VDD is
11 stored to capacitor C1, at that moment that
12 transistor M3 is turned off, any fluctuations,
13 including noise or drift, that are a part of VDD,
14 at that moment, would be stored to capacitor C1,
15 right?

16 MR. ODA: Objection. Form.

17 A Yeah, when blanking is asserted and M3
18 is turned on, the whole VDD would be placed on C1.

19 MR. HAMILL: Okay. Let's introduce the
20 next exhibit. That'll be Exhibit 1015, the
21 supplemental declaration.

22 (Exhibit 1015 previously marked for

1 identification and attached to the transcript.)

2 A 1015, correct?

3 Q Correct.

4 A I have it.

5 Q Okay. In this exhibit, in your
6 supplemental declaration there are sections, in
7 your discussion of the various grounds, that begin
8 with a heading, like, responses to specific issues
9 raised by Mr. Credelle.

10 Are you familiar with those sections?

11 A Of course.

12 Q Other than those sections, it appears
13 that the full content of your original declaration
14 is included in this supplemental declaration.

15 Is that correct? Is this declaration
16 the original declaration, plus these new sections?

17 A There must be some paragraphs that are
18 slightly modified, but, yeah, that's the intent,
19 is that it contained all the original opinions,
20 plus addressing new opinions of Credelle.

21 Q And other than those new sections, what
22 modifications did you make to the original

1 declaration?

2 A I mean, there are little changes,
3 right, the list of exhibits is different. I
4 believe the legal standards are all the same, or
5 the obviousness and anticipation introductions.

6 I could go through it, but they should
7 be -- should basically be the same. Yeah, it's
8 the same technology background.

9 Q Okay. How about in the asserted
10 grounds of invalidity? Did you make any changes
11 to the paragraphs -- to the content in those
12 sections, other than add these new sections
13 addressing Mr. Credelle's declaration?

14 A I don't expect anything substantive to
15 be different.

16 Q Were there any non-substantive changes
17 to the content in the asserted grounds of
18 invalidity section?

19 A I don't expect any. We -- basically, I
20 was adding to the original declaration.

21 Q You're not aware of any substantive
22 changes?

1 A No.

2 Q Okay. Please turn to page 126 of --
3 well, I guess it's page 129 of Exhibit 1015.

4 A Just for consistency, are we referring
5 to the number in the center of the page or to the
6 right of -- in the bottom?

7 Q On the right. I'm referring to the
8 number on the right.

9 A Okay. Yes, this is 129, in reference
10 to Hayafuji.

11 Q Actually. I meant to say 165, excuse
12 me, page 165.

13 A Yeah, 165, sorry.

14 Q And at the top of the page, there's a
15 heading "c) Responses to Specific Issues Raised by
16 Mr. Credelle," and this is in the context of your
17 discussion of ground 4. Ground 4 starts on
18 page 139.

19 Do you see that?

20 A Yes, I do.

21 Q Okay. And then if we can skip ahead
22 from there to page 170, you've got paragraph 328

1 there.

2 A Yes.

3 Q Here, you, in this paragraph you have a
4 discussion of algebraic manipulations. The first
5 sentence reads "With this mathematical framework
6 in place, a POSA would readily see potential
7 algebraic manipulations of Hayafuji's equations."

8 Do you see that?

9 A Yes, I do.

10 Q And then you have a discussion of
11 Figure 6 and 7. You state "For instance, a POSA
12 would understand that the conceptual block diagram
13 of Hayafuji's Figure 6 equation appears to
14 prescribe that the system implement the function
15 $V_{gate} = V_{data} + V_{ri}$."

16 Do you see that?

17 A Yes.

18 Q And it continues, "however, a POSA
19 would recognize that the corresponding op amp
20 circuit implementation in Figure 7 clearly
21 implements the equation $V_{gate} = -(V_{data} - V_{ri})$,
22 under the reasonable assumption of matched

1 resistors."

2 Do you see that?

3 A Yes, I do.

4 Q And then you conclude with the
5 statement "A POSA would understand that these
6 equations are equivalent and would understand the
7 motivation to manipulate intended circuit behavior
8 algebraically in order to arrive at expressions
9 that utilize mathematical operations that can be
10 implemented by standard op amp circuits."

11 Do you see that?

12 A I do.

13 Q Can you explain what you mean by "the
14 motivation to manipulate intended circuit behavior
15 algebraically"?

16 A Sure. Would you be okay if I open
17 Hayafuji to look at those two figures?

18 (Exhibit 1006 previously marked for
19 identification and attached to the transcript.)

20 Q Sure. And Hayafuji is Exhibit 1006.

21 A Sure. Pulling up Figure 6 and 7.

22 So, what I'm trying to explain is that

1 Figure 6 it's showing you block diagrams. It's
2 not showing you actual hardware or how you would
3 use op amps, for example, to get that desired
4 output. And what Figure 7 is showing you is how
5 you would take the -- a standard -- you're making,
6 in this case, Figure 7 the voltage-addition
7 circuit, right? And to make a voltage-addition
8 circuit, you deal with inversions that occur in
9 the op amps when they're in a feedback -- or when
10 they're in an inverting setup.

11 And so, it's just explaining that, you
12 know, in order to get the functionality that's
13 defined at Figure 6, box 15, you would implement
14 Figure 7.

15 Q What did you mean with the statement
16 "the motivation to manipulate intended circuit
17 behavior algebraically"?

18 A So when you're trying to get the
19 functionality encompassed in box 15 of Figure 6,
20 you have certain ways you can do that, and one is
21 with op amps that allow you to, you know, easily
22 do sums, differences. But then you also have to

1 consider whether the signals are inverted. And
2 so, you have to, then, invert them back. And
3 that's -- that's why the equation is written here
4 as, instead of $V_{gate} = V_{data} + V_{ri}$, it's,
5 basically, an inverted negative of it, which gives
6 you that same result, and that occurs because of
7 op amp 3 and 4.

8 Q And what is the relevance of that to
9 your analysis in this section?

10 MR. ODA: Objection. Form.

11 A Simply stating that a POSA would know,
12 from the disclosure of Hayafuji, that you can
13 manipulate these op amps to do algebraic -- to
14 perform algebra on signals.

15 Q And is this a discussion that is new to
16 the supplemental declaration?

17 A Yes. I believe so.

18 Q This is not an argument that was in
19 your original declaration, right?

20 A I don't think so, no.

21 Q Please turn to the next paragraph.
22 Here, there's some additional

1 discussion of inversions here. Let's go through
2 it.

3 It starts "Further, a POSA would note
4 that drive transistor Tr2 is a PFET and would
5 recognize an opportunity to use the algebraic
6 manipulation and corresponding op amp circuit
7 implementations taught by Hayafuji to realize the
8 simple improvement to the design of Hayafuji." It
9 goes on. "The design Hayafuji presents in
10 Figure 7 results in the Vdata signal arriving at
11 PFET Tr2 having undergone two inversions, thus
12 presenting as a signal with no net inversion."

13 Can you please explain to me the two
14 inversions?

15 A I think the easiest way is probably --
16 so what I'm describing here is the modification.
17 So I'd like to just pull up the modified circuit
18 in this supplemental declaration, and I can give
19 you the page number when I find it.

20 Q Sure.

21 A Yeah. So, for example, the figure at
22 page 155.

1 Q Is that 155 in the middle of the page?

2 A Yeah.

3 Q That's in paragraph 302?

4 A Correct.

5 Q Okay. I'm there.

6 A All right. So in this case, there are
7 two inversions at OP3 and OP4. And then, in the
8 modification, at 157, there's only a single
9 inversion at OP4.

10 Q Okay. So then, continuing in paragraph
11 329, you state "Since Tr2 is a PFET, this will
12 result in the pixel current Id being in anti-phase
13 with data-encoded signal Vdata."

14 What does it mean for the pixel current
15 to be in anti-phase with the Vdata?

16 A What I'm basically saying is inverted.

17 Q Okay. And then you can conclude this
18 paragraph "As such, Hayafuji's implementation will
19 require additional accommodation for this."

20 A Yeah. For example, it's kind of
21 dependent on what comes out of the D-to-A
22 converter.

1 Q And what do you mean by that?

2 MR. ODA: Objection. Form.

3 A Well, I discuss, in 330, that there's
4 preprocessing that happens at the D to A. And so,
5 the number of inversions you perform or the
6 algebra you perform, you know, it's all dependent
7 on that.

8 Q Sorry about that.

9 A Sure.

10 Q Okay. And this discussion, at
11 paragraph 329, how does this fit in with your
12 argument?

13 MR. ODA: Objection. Form.

14 A It's a way to reduce the amount of
15 times you have to invert the signal.

16 Q You mean the modification discussed in
17 paragraph 330 is a way of reducing the amount of
18 times you have to invert the signal?

19 A That's part of it, yeah.

20 Q Okay. This discussion of multiple
21 inversions and the current at the pixel being
22 anti-phased with Vdata, is that also a new

1 argument in your supplemental declaration?

2 A Yes. Yeah.

3 Q Okay. So in paragraph 330, as you
4 mentioned, that's where you refer to potential
5 preprocessing.

6 You mentioned that would take place in
7 the DAC; is that right?

8 MR. ODA: Objection. Form.

9 A Yeah, it would be the DAC, yeah.

10 Q And what does preprocessing mean, in
11 this context?

12 A It really means, what is the voltage
13 level that comes out of there for Vgate to be
14 applied properly? And those depend on, you know,
15 whether you're using a PFET there, to drive to
16 OLED, or a regular N channel.

17 Q So the preprocessing, specifically,
18 what type of modifications to the voltage level
19 will that do, the type of preprocessing you're
20 referring to?

21 MR. ODA: Objection. Form.

22 A The way I see it, it would be whether

1 it's an inverted signal or not.

2 Q Okay. So this refers to whether the
3 signal coming from the DAC is inverted or not, and
4 that would tie into -- it would take into account
5 any subsequent inversions so that it arrives at
6 the pixel circuit in the correct phase?

7 MR. ODA: Objection. Form.

8 A That's fair, yes.

9 Q And this discussion of preprocessing,
10 to make sure the Vdata's in the correct phase,
11 that's also new in the supplemental declaration,
12 right?

13 A Yeah. I don't believe I went into
14 detail in the first declaration.

15 MR. HAMILL: Why don't we go ahead and
16 take a ten-minute break here.

17 MR. ODA: Sure.

18 (Recess taken from 12:48 p.m. to
19 12:59 p.m.)

20 MR. HAMILL: Okay. I have no further
21 questions at this time.

22 MR. ODA: Okay. Let's take a short

1 break. Maybe ten minutes.

2 (Recess taken from 12:59 p.m. to
3 1:11 p.m.)

4 MR. ODA: Thank you. Petitioner has no
5 redirect, so we can go off the record.

6 MR. HAMILL: I'm not sure. I certainly
7 want a copy, expedited.

8 THE STENOGRAPHER: Does anyone else
9 need a copy?

10 MR. ODA: Yes, you can send Petitioner
11 a copy as well. You can make it standard delivery
12 for us.

13 (Off the record at 1:12 p.m.)

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1 CERTIFICATE OF SHORTHAND REPORTER - NOTARY PUBLIC

2
3 I, Judith E. Bellinger, Certified Reporter and
4 Notary Public within and for the State of Maryland
5 do hereby certify:

6 That ALEX Z. KATTAMIS, PH.D., P.E., the
7 witness whose deposition is hereinbefore set
8 forth, was duly sworn by me before the
9 commencement of such deposition and that such
10 deposition was taken before me and is a true
11 record of the testimony given by such witness.

12 I further certify that the adverse
13 party, Samsung, was represented by counsel at the
14 deposition.

15 I further certify that the deposition
16 of ALEX Z. KATTAMIS, PH.D., P.E., occurred
17 remotely via Zoom on Tuesday, June 4, 2024,
18 commencing at 12:03 p.m. to 1:12 p.m.

19 I further certify the inspection,
20 reading and signing of said deposition was not
21 discussed on the record.

22 I further certify that I am not related

1 to any of the parties to this action by blood or
2 marriage, I am not employed by or an attorney to
3 any of the parties to this action, and that I am
4 in no way interested, financially or otherwise, in
5 the outcome of this matter.

6 IN WITNESS WHEREOF, I have hereunto set
7 my hand this 5th day of June, 2024.

8

9 My commission expires:

10 November 3rd, 2024

11

Judith E. Bellinger

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13 NOTARY PUBLIC IN AND FOR THE

14 STATE OF MARYLAND

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a1	algebraic	anything	bases
5:17	19:4, 19:7,	7:10, 17:14	8:19
about	22:13, 23:5	appeal	basically
9:19, 15:3,	algebraically	1:3	17:7, 17:19,
15:4, 17:9, 25:8	20:8, 20:15,	appear	22:5, 24:16
accommodation	21:17	13:1, 13:6	because
24:19	all	appears	12:20, 22:6
account	8:13, 8:16,	16:12, 19:13	before
27:4	16:19, 17:4,	application	1:3, 2:11,
accurate	24:6, 25:6	5:15	6:17, 9:1, 29:8,
14:5	allow	applied	29:10
acronym	21:21	12:3, 13:11,	begin
8:9	already	13:17, 13:18,	16:7
action	7:19	26:14	beginning
30:1, 30:3	also	argument	10:18
actual	4:12, 21:22,	22:18, 25:12,	behalf
21:2	25:22, 27:11	26:1	3:3, 3:13
actually	america	arrive	behavior
18:11	1:6	20:8	20:7, 20:14,
add	amount	arrives	21:17
17:12	25:14, 25:17	27:5	being
added	amp	arriving	6:4, 12:7,
12:4	19:19, 20:10,	23:10	24:12, 25:21
adding	22:7, 23:6	art	believe
17:20	amplifier	8:11	11:6, 17:4,
additional	12:3	asserted	22:17, 27:13
22:22, 24:19	amps	10:18, 15:17,	bellinger
addressing	21:3, 21:9,	17:9, 17:17	1:21, 2:12,
16:20, 17:13	21:21, 22:13	assumption	29:3
adverse	analysis	19:22	bemben
29:12	22:9	attached	4:4
again	andrew	5:5, 7:21,	binder
6:20	3:14	9:11, 16:1,	7:4, 7:5
agree	anti-phase	20:19	black
14:7	24:12, 24:15	attorney	10:19
ahead	anti-phased	30:2	blanking
18:21, 27:15	25:22	aware	10:17, 11:20,
airport	anticipation	17:21	13:3, 13:8,
3:16	17:5	B	13:18, 13:20,
alberti	any	b1	15:17
3:15	9:3, 11:11,	5:14	block
alex	12:22, 14:7,	back	19:12, 21:1
1:15, 2:1, 5:2,	15:12, 17:10,	15:9, 22:2	blood
5:8, 5:18, 6:3,	17:16, 17:19,	background	30:1
6:9, 29:6, 29:16	17:21, 27:5,	17:8	board
algebra	30:1, 30:3	baker	1:3
22:14, 25:6	anyone	3:7, 6:11, 6:14	bottom
	6:15, 28:8		10:5, 18:6

botts 3:7, 6:11, 6:14 boulevard 3:16 box 21:13, 21:19 break 27:16, 28:1 burlingame 3:18 C c 18:15 cl 10:21, 11:2, 11:8, 11:12, 11:15, 11:17, 12:5, 12:9, 13:2, 13:7, 13:12, 13:19, 14:2, 14:9, 14:18, 15:11, 15:14, 15:18 ca 3:10, 3:18 california 3:8 can't 15:2 capacitor 10:21, 11:2, 11:12, 11:15, 12:5, 12:9, 13:2, 13:7, 14:2, 14:9, 14:18, 15:11, 15:14 case 1:12, 21:6, 24:6 castro 4:13 ccr-nm 1:22 ccr-wa 1:22 center 18:5	certain 21:20 certainly 28:6 certificate 29:1 certified 2:13, 29:3 certify 29:5, 29:12, 29:15, 29:19, 29:22 changes 17:2, 17:10, 17:16, 17:22 channel 26:16 charged 10:21, 11:2, 11:8, 13:2, 13:7 circuit 10:1, 19:20, 20:7, 20:14, 21:7, 21:8, 21:16, 23:6, 23:17, 27:6 circuits 20:10 clamp 10:1 clamping 11:12, 12:4, 12:21 clearly 19:20 column 10:5, 11:19, 11:20, 12:14 comes 24:21, 26:13 comfortable 8:6 coming 27:3 commencement 29:9 commencing 29:18	commission 30:9 conceptual 19:12 conclude 20:4, 24:17 conducted 1:16, 2:2 configured 10:17 consider 22:1 consistency 18:4 contained 16:19 content 16:13, 17:11, 17:17 context 18:16, 26:11 continue 12:1 continues 12:1, 19:18 continuing 11:18, 24:10 converter 24:22 copy 28:7, 28:9, 28:11 correct 16:2, 16:3, 16:15, 24:4, 27:6, 27:10 corresponding 19:19, 23:6 could 15:8, 17:6 counsel 6:6, 29:13 course 16:11 credelle 7:15, 16:9, 16:20, 18:16 credelle's 17:13	crr 1:22 csr-tx 1:22 current 24:12, 24:14, 25:21 cv 7:2 D d-to-a 24:21 dac 12:3, 26:7, 26:9, 27:3 data-encoded 24:13 day 30:7 dc 3:5, 4:8 deal 21:8 deasserted 11:21 decision 7:9 declaration 5:18, 7:1, 7:2, 7:3, 7:14, 7:15, 8:22, 9:4, 15:21, 16:6, 16:13, 16:14, 16:15, 16:16, 17:1, 17:13, 17:20, 22:16, 22:19, 23:18, 26:1, 27:11, 27:14 declarations 8:17, 8:20 defined 21:13 delivery 28:11 depend 26:14
--	---	--	--

dependent 24:21, 25:6	10:20	encompassed 21:19	expressions 20:8
depos 4:13	documents 6:18, 6:20, 7:13	equation 19:13, 19:21, 22:3	F
deposition 1:15, 2:1, 5:8, 7:3, 7:11, 7:12, 7:17, 29:7, 29:9, 29:10, 29:14, 29:15, 29:20	down 10:15, 12:13	equations 19:7, 20:6	fair 27:8
described 9:19	dr 7:10, 7:22, 8:13	equivalent 20:6	familiar 9:20, 16:10
describing 23:16	drift 15:13	errors 9:3, 9:5	feedback 21:9
design 23:8, 23:9	drifts 11:11, 12:16	esquire 3:4, 3:5, 3:6, 3:14, 4:3, 4:4	figure 9:19, 19:11, 19:13, 19:20, 20:21, 21:1, 21:4, 21:6, 21:13, 21:14, 21:19, 23:10, 23:21
desired 21:3	drive 12:20, 15:5, 23:4, 26:15	essentially 13:22	figures 9:16, 20:17
detail 27:14	driver 12:16	examination 5:2, 6:6	financially 30:4
diagram 19:12	drives 11:22	examined 6:4	find 23:19
diagrams 21:1	duly 6:4, 29:8	example 21:3, 23:21, 24:20	first 6:4, 13:4, 19:4, 27:14
differences 21:22	during 13:17	excuse 13:19, 18:11	fit 25:11
different 17:3, 17:15	each 10:18, 12:22	exhibit 5:7, 5:12, 5:13, 5:15, 5:18, 7:6, 7:7, 7:18, 7:19, 7:20, 9:10, 9:12, 9:16, 10:4, 15:20, 15:22, 16:5, 18:3, 20:18, 20:20	fitsimmons 4:3
digits 8:7	easiest 23:15	exhibits 5:6, 17:3	fluctuations 15:12
disclosure 22:12	easily 21:21	expect 17:14, 17:19	follows 6:5
discuss 25:3	edt 1:18	expedited 28:7	form 11:4, 12:11, 13:9, 13:16, 14:4, 14:10, 14:14, 14:20, 15:7, 15:16, 22:10, 25:2, 25:13, 26:8, 26:21, 27:7
discussed 25:16, 29:21	effective 12:16	expires 30:9	forth 8:16, 29:8
discusses 10:6	electronics 1:5, 1:6	explain 20:13, 20:22, 23:13	fox 4:5
discussion 16:7, 18:17, 19:4, 19:10, 22:15, 23:1, 25:10, 25:20, 27:9	eliot 3:5	explaining 21:11	
discussions 7:16	else 6:15, 28:8		
display 1:5, 10:12,	embodiment 9:19, 9:20, 9:22, 10:7, 10:11, 14:13		
	employed 30:2		
	E		

framework 19:5 francisco 3:10 full 16:13 function 19:14 functionality 21:12, 21:19 further 23:3, 27:20, 29:12, 29:15, 29:19, 29:22 G give 23:18 given 29:11 gives 22:5 glitches 12:19, 13:1, 13:5, 14:7, 14:17, 15:1, 15:5 go 17:6, 23:1, 27:15, 28:5 goes 11:20, 23:9 goldstein 4:5 ground 18:17 grounds 16:7, 17:10, 17:17 guess 18:3 H hamill 3:14, 5:3, 6:7, 15:19, 27:15, 27:20, 28:6 hand 30:7	happens 25:4 hardware 21:2 hayafuji 18:10, 20:17, 20:20, 22:12, 23:7, 23:8, 23:9 hayafuji's 19:7, 19:13, 24:18 heading 16:8, 18:15 here 12:6, 12:12, 13:4, 19:3, 22:3, 22:22, 23:1, 23:16, 27:16 hereby 29:5 hereinbefore 29:7 hereunto 30:6 however 19:18 I id 24:12 identification 7:21, 9:11, 16:1, 20:19 impacting 12:20, 15:5 implement 19:14, 21:13 implementation 19:20, 24:18 implementations 23:7 implemented 20:10 implements 19:21 improvement 23:8	inc 1:6 included 16:14 including 11:11, 15:13 initial 15:8 inspection 29:19 instance 19:11 instead 9:9, 12:2, 22:4 institution 7:9 intended 20:7, 20:14, 21:16 intent 16:18 inter 5:19, 8:2 interested 30:4 introduce 7:17, 15:19 introductions 17:5 invalidity 17:10, 17:18 inversion 23:12, 24:9 inversions 21:8, 23:1, 23:11, 23:14, 24:7, 25:5, 25:21, 27:5 invert 22:2, 25:15, 25:18 inverted 22:1, 22:5, 24:16, 27:1, 27:3 inverting 21:10 ipr 1:12, 8:2	issues 16:8, 18:15 J jason 4:3 jesse 4:13 job 1:19 judith 1:21, 2:11, 29:3 june 1:17, 29:17, 30:7 K kattamis 1:15, 2:1, 5:2, 5:6, 5:8, 5:19, 6:3, 6:9, 7:10, 7:20, 7:22, 8:13, 29:6, 29:16 kessler 4:5 kind 24:20 know 6:19, 9:7, 21:12, 21:21, 22:11, 25:6, 26:14 kramer 3:15 L last 8:7 left 7:5 legal 17:4 let's 7:17, 9:12, 12:13, 15:19, 23:1, 27:22
--	--	---	---

level 26:13, 26:18 lim 3:15 line 10:8, 10:16, 10:19, 11:10, 11:19, 12:13, 12:22 list 6:21, 17:3 listed 7:13 little 17:2 llc 1:9 llp 3:15 located 6:10 longer 11:22 look 10:15, 20:17 M m3 10:20, 11:5, 11:21, 12:7, 12:10, 14:1, 14:8, 14:19, 15:12, 15:17 make 16:22, 17:10, 21:7, 27:10, 28:11 making 21:5 manhattan 6:12 manipulate 20:7, 20:14, 21:16, 22:13 manipulation 23:6 manipulations 19:4, 19:7	manner 11:10 many 7:13 mark 3:4, 6:14, 7:16 marked 5:11, 7:19, 7:20, 9:10, 15:22, 20:18 marriage 30:2 maryland 2:14, 29:4, 30:14 matched 19:22 mathematical 19:5, 20:9 matter 8:4, 8:14, 30:5 maybe 28:1 mean 11:1, 12:7, 13:5, 13:13, 14:21, 15:2, 17:2, 20:13, 21:15, 24:14, 25:1, 25:16, 26:10 means 13:10, 26:12 meant 18:11 mentioned 6:17, 26:4, 26:6 mentions 12:6 middle 24:1 midtown 6:11 minutes 28:1 modification 23:16, 24:8,	25:16 modifications 16:22, 26:18 modified 16:18, 23:17 moment 12:9, 14:1, 14:18, 15:11, 15:14 more 12:15, 14:21 motivation 20:7, 20:14, 21:16 multiple 25:20 must 16:17 N name 6:8 necessarily 12:17, 12:18, 15:1 need 28:9 negative 11:7, 22:5 neil 3:6 net 23:12 new 3:6, 16:16, 16:20, 16:21, 17:12, 22:15, 25:22, 27:11 next 11:9, 11:18, 12:2, 13:3, 13:7, 15:20, 22:21 node 11:22 noise 12:18, 12:22, 13:5, 15:1,	15:4, 15:13 non-substantive 17:16 notary 2:13, 29:1, 29:4, 30:13 note 23:3 notice 2:11, 5:7, 7:3, 7:18 noticed 9:4, 9:5 november 30:10 number 5:13, 5:16, 7:6, 7:7, 18:5, 18:8, 23:19, 25:5 nw 4:7 O objection 11:4, 12:11, 13:9, 13:16, 14:4, 14:10, 14:14, 14:20, 15:7, 15:16, 22:10, 25:2, 25:13, 26:8, 26:21, 27:7 obviousness 17:5 occur 21:8 occurred 29:16 occurs 22:6 oda 3:4, 6:14, 7:6, 7:16, 11:4, 12:11, 13:9, 13:16, 14:4, 14:10, 14:14, 14:20, 15:7,
--	---	---	---

15:16, 22:10, 25:2, 25:13, 26:8, 26:21, 27:7, 27:17, 27:22, 28:4, 28:10 office 1:1, 3:5, 3:6 offices 6:11 okay 7:17, 7:22, 9:7, 9:12, 10:3, 10:15, 11:9, 11:18, 12:13, 14:16, 15:19, 16:5, 17:9, 18:2, 18:9, 18:21, 20:16, 24:5, 24:10, 24:17, 25:10, 25:20, 26:3, 27:2, 27:20, 27:22 oled 26:16 once 12:21 one 7:2, 9:6, 9:8, 21:20 only 7:18, 7:19, 12:21, 24:8 op 19:19, 20:10, 21:3, 21:9, 21:21, 22:7, 22:13, 23:6 op3 24:7 op4 24:7, 24:9 open 20:16 operations 20:9 opinions 8:14, 8:16,	8:19, 16:19, 16:20 opportunity 23:5 order 20:8, 21:12 ordinary 8:11 original 7:1, 16:13, 16:16, 16:19, 16:22, 17:20, 22:19 other 16:12, 16:21, 17:12 otherwise 30:4 out 24:21, 26:13 outcome 30:5 output 21:4 owner 1:10, 3:13, 6:6 owner's 5:7 P page 5:2, 5:6, 9:15, 10:3, 18:2, 18:3, 18:5, 18:12, 18:14, 18:18, 18:22, 23:19, 23:22, 24:1 pages 1:20 paragraph 10:16, 18:22, 19:3, 22:21, 24:3, 24:10, 24:18, 25:11, 25:17, 26:3 paragraphs 16:17, 17:11	part 14:8, 14:17, 15:13, 25:19 partes 5:20, 8:2 parties 30:1, 30:3 party 29:13 passage 10:16 patent 1:1, 1:3, 1:10, 1:13, 3:13, 5:7, 5:13, 5:15, 5:20, 6:6, 8:4, 9:13 perform 22:14, 25:5, 25:6 period 13:3, 13:8, 13:18 person 8:10 pertains 8:4 petitioner 3:3, 28:4, 28:10 petitioners 1:7 pfet 23:4, 23:11, 24:11, 26:15 ph 1:15, 2:1, 5:2, 5:9, 5:19, 6:3, 29:6, 29:16 phase 27:6, 27:10 pixel 24:12, 24:14, 25:21, 27:6 place 19:6, 26:6 placed 15:18	planet 4:13 plate 10:21, 11:1, 11:6, 11:17, 13:19 please 6:8, 6:20, 9:15, 10:3, 18:2, 22:21, 23:13 plus 16:16, 16:20, 19:15 point 9:6, 9:8 polaris 1:9 posa 8:9, 19:6, 19:11, 19:18, 20:5, 22:11, 23:3 posita 8:10 positive 10:12 potential 19:6, 26:4 power 10:12, 10:22, 11:2, 11:10, 12:17, 12:19, 13:1, 13:6, 14:22 powered 1:9 prepare 7:11 preparing 7:12 preprocessing 25:4, 26:5, 26:10, 26:17, 26:19, 27:9 prescribe 19:14 present 4:12
--	--	--	---

presenting 23:12	reads 11:10, 19:5	remote 5:7	18:7, 18:8, 21:7, 22:19,
presents 23:9	realize 23:7	remotely 29:17	24:6, 26:7, 27:12
preventing 15:4	really 26:12	remove 12:18, 15:1	room 6:13
previously 5:11, 9:10, 15:22, 20:18	realtime 2:13	removing 12:16, 15:4	rpr 1:22
probably 23:15	reasonable 19:22	reported 1:21	S
professional 2:12	reasserted 13:21	reporter 2:12, 2:13, 29:1, 29:3	said 29:20
properly 26:14	recess 27:18, 28:2	represented 29:13	same 17:4, 17:7, 17:8, 22:6
provided 8:14	recharged 12:21	reprogrammed 14:3	samsung 1:5, 1:6, 29:13
providing 8:1	recognize 19:19, 23:5	require 24:19	san 3:10
public 2:13, 29:1, 29:4, 30:13	record 6:8, 28:5, 28:13, 29:11, 29:21	resistors 20:1	say 18:11
publication 5:16	redirect 28:5	responses 16:8, 18:15	saying 24:16
pull 23:17	reduce 25:14	restate 15:8	says 10:17, 11:16, 12:12, 12:15
pulling 20:21	reducing 25:17	result 22:6, 24:12	section 17:18, 22:9
pursuant 2:11	refer 8:6, 9:9, 26:4	results 23:10	sections 16:6, 16:10, 16:12, 16:16, 16:21, 17:12
Q	reference 10:19, 18:9	review 5:20, 9:1	see 9:17, 10:5, 18:19, 19:6, 19:8, 19:16, 20:2, 20:11, 26:22
question 13:4, 15:8, 15:10	referring 11:7, 18:4, 18:7, 26:20	reviewed 7:13	send 28:10
questions 9:18, 27:21	refers 10:11, 27:2	reviewing 7:14	sentence 11:9, 11:19, 12:2, 19:5
R	registered 2:12	richard 4:4	set 8:16, 29:7, 30:6
raised 16:9, 18:15	regular 26:16	right 10:1, 10:9, 10:10, 10:13, 10:21, 11:1, 11:6, 11:17, 12:8, 13:11, 13:19, 14:2, 14:13, 14:19, 14:22, 15:3, 15:6, 15:15, 17:3, 18:6,	setup 21:10
re-establish 10:19	related 29:22		
read 15:9	relevance 22:8		
readily 19:6	remain 13:12, 13:14, 13:15, 13:20		
reading 13:10, 29:20			

short 27:22 shorthand 29:1 should 17:6, 17:7 showing 21:1, 21:2, 21:4 side 12:8, 14:2 signal 10:18, 11:21, 12:2, 12:20, 13:11, 13:17, 13:18, 15:5, 23:10, 23:12, 24:13, 25:15, 25:18, 27:1, 27:3 signal's 13:20 signals 22:1, 22:14 signature-plkal 30:11 signing 29:20 simple 23:8 simply 22:11 since 24:11 single 24:8 sirota 3:6 skill 8:11 skip 12:13, 18:21 slightly 16:18 smaller 7:4 some 6:18, 9:18,	16:17, 22:22 sorry 13:13, 18:13, 25:8 specific 16:8, 18:15 specifically 12:15, 26:17 specification 10:6 spent 7:14 standard 20:10, 21:5, 28:11 standards 17:4 started 6:17 starting 10:16, 11:9 starts 10:9, 11:19, 18:17, 23:3 state 2:14, 6:8, 19:11, 24:11, 29:4, 30:14 statement 14:6, 15:3, 20:5, 21:15 states 1:1, 5:13, 5:15, 11:5, 14:11, 14:22 stating 22:11 stenographer 28:8 stenographically 1:21 sterne 4:5 stored 11:12, 11:14, 11:16, 12:4, 12:8, 14:2, 14:9, 14:17,	15:11, 15:14 street 3:8, 4:7 submitting 9:1 subsequent 27:5 substantive 9:6, 17:14, 17:21 suite 3:9, 3:17 sums 21:22 supplemental 5:18, 7:2, 7:3, 8:22, 15:21, 16:6, 16:14, 22:16, 23:18, 26:1, 27:11 supply 10:12, 10:22, 11:2, 11:10, 12:17, 12:19, 13:1, 13:6, 14:22 sure 6:21, 20:16, 20:20, 20:21, 23:20, 25:9, 27:10, 27:17, 28:6 sworn 6:4, 29:8 system 19:14	technician 4:13 technologies 1:9 technology 17:8 temp 13:19 ten 28:1 ten-minute 27:16 terminal 11:7, 13:12 testified 6:5 testimony 8:1, 29:11 thank 28:4 think 7:18, 9:8, 14:5, 14:21, 22:20, 23:15 three 8:7 through 12:3, 17:6, 23:1 tie 27:4 time 7:14, 27:21 times 25:15, 25:18 today 6:10, 6:13, 8:1 tonkovich 3:15 top 18:14 toward 10:5 tr2 23:4, 23:11, 24:11 trademark 1:1
---	--	--	--

transcript 5:5, 7:21, 9:11, 16:1, 20:19 transistor 10:20, 11:5, 11:21, 12:7, 12:10, 14:19, 15:12, 23:4 trial 1:3 true 29:10 trying 20:22, 21:18 tuesday 1:17, 29:17 turn 9:12, 9:15, 10:3, 18:2, 22:21 turned 10:20, 11:6, 11:21, 12:7, 12:10, 14:1, 14:8, 14:19, 15:12, 15:18 two 20:17, 23:11, 23:13, 24:7 type 26:18, 26:19 types 14:16 typo 9:6, 9:7 U under 19:22 undergone 23:11 understand 7:22, 8:10, 19:12, 20:5, 20:6 understanding 14:12	united 1:1, 5:13 unites 5:15 until 13:3, 13:7, 13:20, 14:2 use 8:9, 21:3, 23:5 using 26:15 utilize 20:9 V value 12:9, 13:22, 14:1 various 16:7 vclamp 11:13, 12:4, 12:21 vdata 19:15, 19:21, 22:4, 23:10, 24:13, 24:15, 25:22 vdata's 27:10 vdd 10:11, 10:22, 11:3, 11:8, 11:11, 11:14, 11:16, 12:8, 12:9, 13:2, 13:6, 13:11, 13:22, 14:8, 14:17, 15:10, 15:13, 15:18 vgate 26:13 vgate= 19:15, 19:21, 22:4 via 29:17 video 10:18, 10:20, 12:2, 12:3, 12:15, 12:20, 12:22, 15:5 virtually 1:16, 2:2 voltage 10:12, 10:22, 11:3, 11:11, 11:12, 11:14, 12:4, 12:8, 12:16, 12:17, 12:19, 12:21, 12:22, 13:2, 13:5, 13:6, 14:7, 14:16, 14:22, 26:12, 26:18 voltage-addition 21:6, 21:7 vri 19:15, 19:21, 22:4 W want 28:7 washington 4:8 way 13:10, 23:15, 25:14, 25:17, 26:22, 30:4 ways 21:20 went 27:13 whereof 30:6 whether 22:1, 26:15, 26:22, 27:2 whole 15:18 williams 3:5 within 29:4 witness 29:7, 29:11, 30:6 works 8:8 written 22:3 Y yeah 11:16, 12:12, 14:5, 14:11, 15:10, 15:17, 16:18, 17:7, 18:13, 23:21, 24:2, 24:20, 25:19, 26:2, 26:9, 27:13 yep 11:16 york 3:6 Z zoom 29:17 , ,4 1:17 . .2600 4:9 .4300 3:19 .6234 3:11 0 00771 1:12, 8:2 0190128 5:16 03 1:18, 29:18 1 28:3, 28:13,
--	--

29:18 1001 5:13, 7:7, 9:10, 9:12, 9:16, 10:4 1004 7:7 1006 5:15, 20:18, 20:20 101 3:8 1010 7:8 1014 7:8 1015 5:18, 15:20, 15:22, 16:2, 18:3 1016 7:8 1017 7:8 1018 7:8 11 28:3 1101 4:7 12 1:18, 7:8, 27:18, 27:19, 28:2, 28:13, 29:18 126 18:2 129 18:3, 18:9 139 18:18 15 21:13, 21:19 155 23:22, 24:1 157 24:8 16 5:18	165 18:11, 18:12, 18:13 170 18:22 2 20 5:15 20005 4:8 2005 5:16 202.371 4:9 2023 1:12, 8:2 2024 1:17, 29:17, 30:7, 30:10 250 3:17 3 30 1:20 302 12:16, 24:3 306 12:3 3200 3:9 322 11:22 328 18:22 329 24:11, 25:11 330 25:3, 25:17, 26:3 3rd 30:10 4 415.291 3:11 45 10:8	48 27:18 5 512 9:9 521 8:7, 9:9, 9:13 539563 1:19 577 3:16 5802 3:10 59 27:19, 28:2 5th 30:7 6 61 10:16 65 11:10 650.825 3:19 67 11:19 7 7,259,521 1:13, 5:14, 5:21, 8:5 9 94010 3:18 94111 3:10	
---	---	---	--