# PAUL D. FRANZON

Cirrus Logic Distinguished Professor
Director of Graduate Programs
Department of Electrical and Computer Engineering

# I. INTRODUCTION

## B. BRIEF RESUME

### 1. Education

- Doctor of Philosophy, Electrical and Electronic Engineering 1989, University of Adelaide, Australia . Advisor: Kamran Eshraghian.
- Bachelor of Engineering with First Class Honours, Electrical and Electronic Engineering: 1984, University of Adelaide, Australia
- Bachelor of Science, Physics and Mathematics: 1983, University of Adelaide, Australia.

### 2. Professional Experience

- Assistant Professor, Associate Professor, Professor, and Distinguished Professor North Carolina State University, Department of Electrical and Computer Engineering, Raleigh, North Carolina, January 1989 – present
- Technical Director, Rambus (part time/consulting), 2009-11, Chapel Hill, NC.
- Cofounder, LightSpin Technologies Inc., 2001-. Vice-President of Engineering, 2001-2002, Raleigh NC.
- PhD Candidate, University of Adelaide, Department of Electrical and Electronic Engineering, Adelaide, South Australia, Australia, April 1987 - December 1988.
- Director and Co-Founder, Network Communications Pty. Ltd., Adelaide, South Australia, Australia, April 1987 - April 1989.
- Consultant, AT&T Bell Laboratories, Holmdel NJ, January 1986 - April 1987.
- PhD Candidate, University of Adelaide, Department of Electrical and Electronic Engineering, Adelaide, South Australia, Australia, August 1984-December 1985.
- Engineer, Defence Science and Technology Organization, Salisbury, South Australia, Australia, January 1984--July 1984
- Intern, Defense Science and Technology Organization, Salisbury, South Australia, Australia, December 1982--March 1983.
- Intern, Telecom Australia, Adelaide, South Australia, Australia, December 1981-March 1982.
- Infantry Soldier and Officer, (Ranks held: Private - Captain), Royal Australian Infantry Corps, Australian Army Reserve, December 1979 - December 1991.

### 3. Scholarly and Creative activities



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| *Type* | *Number* |
|---|---|
| Books | 4 |
| Solution Manuals | 1 |
| Edited Book Chapter | 19 |
| Refereed Journal article | 99 |
| Conference Paper (refereed) | 237 |
| Patents granted | 10 |

**4. Membership in professional organizations**

Fellow, Institute of Electrical and Electronic Engineers
Member, IMAPS
Member, SPIE
Member, Association of Computing Machinery

**5. Scholarly and professional honors**

- Alumni Distinguished Graduate Professor Award, 2021
- NCSU Innovator of the Year Award, 2015
- College of Engineering Board of Governor's Award, 2014
- NRL Alan Berman Research Publication Award, 2008
- Babbage Award, Synopsys, 2008
- Fellow of the IEEE, 2006
- Alcoa Research Award, 2005
- ECE Graduate Teacher of the year award, 2007
- ECE Most Helpful Teacher of the year award, 2007
- ECE Teacher of the year award, 2006
- ECE Graduate Advisor of the year award, 2006
- Alumni Undergraduate Distinguished Professor, 2003-2005.
- Graduate teacher of the year, ECE department, 2005
- NSW Australia Expatriate Scientist Award, 2003
- Selected to the NCSU Academy of Outstanding Teachers, 2001
- First round prize winner, SRC copper challenge, 2000.
- Teacher of the Year Award, presented by the IEEE Student Branch, 1997
- National Science Foundation Young Investigator's Award, 1993.
- 13 prizes while a student at the University of Adelaide
- Australia Defense Medal, 2006

**6. Professional service on campus**

- Member, STRAG 2003-2005
- Instructor, PE preparation course 1995-2000

**7. Professional service off campus**



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- Consultant to Perkins Cole, 2022, patent issues
- Consultant to Micross, 2022, 3DIC processes
- Consultant to DLA Piper, 2022, patent issues
- Consultant to Wolf Greenfield, 2022, patent issues
- Consultant to Lee Hayes, 2020-, patent issues
- Consultant to Fish and Richardson, 2020-22, patent issues
- Consultant to Sofwerx, 2018, Machine learning for UAVs.
- Consultant to Kirkland, 2019- patent issues
- Consultant to Finnigan, 2016-, patent issues
- Consultant to Wilmar, 2017-, patent issues
- Consultant to Unified Patents, 2017- , patent issues
- Consultant to DARPA, Thermal issues, 2012-2016
- Consultant to Paul Hastings, OMM, KL Gates, Samsung, Micron and SK Hynix, 2015-,2017 Patent issues
- Consultant to LDKM and AVT, Patent issues, 2013-2015
- Consultant to Skiermont Puckett and Spherix, Patent issues, 2014-2016
- Consultant to Haliburton, 2014
- Consultant to DARPA, Exascale Computing Study, 2007-9.
- Consultant to Rambus, Semiconductors, 2009-12
- Consultant to Techsearch, 2008.
- Consultant, NTU, 2004-9. ASIC Design.
- Consultant to Tessera, 2009. 3DIC advising.
- Consultant, Irvine Sensors, 2006. Secure chip design.
- Consultant, Cisco Systems, 2006, Signal Integrity.
- Consultant, Talon Logic, 2005. Secure system Design.
- Consultant to O'Malveny and Meyers, 2000-2002, Patent issues.
- Consultant to Venture 2000, 2000, Due Diligance.
- Consultant to CAPPS, 1999-2000, IP Development.
- Consultant to Sofrent, 1999-2000, IP Development.
- Consultant to Ericsson, 1997, Synthesis Methodology.
- Consultant to Cadence, 1996. Evaluated possible company acquisition.
- Consultant to Polychip, 1994 - 2000. Circuit Design.
- Consultant to Square-D, 1996. Interconnect Design.
- Consultant to Mentor Graphics, 1995, 1996. Technical advisory board.
- Consultant to Cadence Design Systems, 1992, 1996. Technical advisory board.
- Consultant to DCT, 1995-1996. ASIC Design.
- Consultant to Techsearch International, 1989-1991. Report Preparation.
- Consultant to BNR, HP, Sun. 1992-4. Interconnect Design.
- Consultant to MCNC, 1989. CAD

## C. CANDIDATES STATEMENT

As **Director of Graduate Programs in ECE** (starting in 2016), I have introduced the following innovations:



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1. I led the faculty in agreeing to a reduced course load for our PhD students (from 42 CH to 30 and simplified rules). This has been very popular with PhD students. (2016)
2. I introduced a PhD Visit Day and held one every year. The ones held in 2017 and 2018 each involved over 40 visitors and about the same number of alumni, faculty and current students. Over 90% of students surveyed stated they are more likely to come as a result of the visit day.
3. I reorganized an office into 3 staff and 1 EPA position. The 3 staff consist of two GSSCs (one for admissions and one for current students), and one assistant for both. The EPA position is our new Director of Graduate Employment Services. Her role is to help students get jobs and internships.
4. I introduced a series of panels aimed at PhD students. Panels held so far include the following
    a. Becoming faculty (2017);
    b. Becoming an industry researcher (2018);
    c. Writing proposals (2019).
5. I held two classes on advanced study skills aimed at MS students (2018).
6. I took over leadership of the Graduate Admissions Committee. We reorganized the PhD recruiting flow, starting from information disseminated by the Admissions GSSC through to TA allocations. I reorganized the MS admissions flow, starting from data prep by the Admissions GSSC to using statistical models to assist (not make) the decision making process.
7. I changed the PhD application process to encourage students to answer questions specifical to what they can draw upon to make good PhD students.
8. I redid our marketing materials and started marketing at other campuses in the UNC system.
9. I conducted surveys of current students, and alumni to determine gaps in our program. As a result, I introduced additional courses in verification with UVM, operating systems and hardware security. In addition the Neural Networks course was refocused and a concentration on Machine Learning introduced.
10. Introduced Graduate Certificates in 5G, ASIC Design and Verification, CPE and EE.

As **Site Director for the Center for Advanced Electronics through Machine Learning** (CAEML) I lead this Center for NCSU. I am one of the founding directors for this Center, which is run jointly with UIUC and Ga Tech. I am responsible for member company recruiting, faculty recruiting and running the biannual meetings as held every 18 months on campus here. I have particularly focused on drawing in other NCSU faculty to the Center. Two new faculty have joined since the center started.



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# II. TEACHING AND MENTORING OF UNDERGRADUATE AND GRADUATE STUDENTS

## A. TEACHING EFFECTIVENESS

1. Courses Taught

Since becoming DGP, I am not required to teach, though I did teach ECE 464/564 in 2016, 17 and 19. I continue to remain involved in ECE 464/564 and ECE 733 though by giving guest and substitute lectures, advising on course policies, content and suggesting suitable class projects.

| Course | When | Enrollment | Instructor effectiveness | Course excellence |
|---|---|---|---|---|
| ECE 464 ASIC Design | F 21 | 41 | na | na |
| ECE 564 ASIC Design | F 21 | 157 | na | na |
| ECE 564-601 | F 21 | 7 | 5.0/4.3 | 4.7/4.1 |
| ECE 564-640 | F 21 | 11 | 4.8 | 4.3 |
| ECE 564-651 | Sum 21 | 9 | 4.3/3.8 | 4.2/3.8 |
| ECE 464 ASIC Design | F 20 | 39 | | |
| ECE 564 ASIC Design | F 20 | 54 | | |
| ECE 564-601 | F 20 | 10 | 4.2 | 4.6 |
| ECE 564-651 | Sum 20 | 16 | 4.3 | 4.0 |
| ECE 464-001 | F 19 | 39 | 4.7 | 4.5 |
| ECE 564-001 | F 19 | 139 | 4.7 | 4.5 |
| ECE 564-601 | F 19 | 6 | 5.0 | 5.0 |
| ECE 464-001 | F 17 | 36 | 4.4 | 4.4 |
| ECE 564-001 | F 17 | 148 | 4.4 | 4.4 |
| ECE 564-601 | F 17 | 7 | | |
| ECE 464-001 | F 16 | 29 | 4.8 | 4.6 |
| ECE 520-001 | F 16 | 121 | 4.8 | 4.8 |
| ECE 520-601 | F 16 | 9 | 4.4 | 4.2 |
| ECE 520-651 | Su 16 | 16 | 4.6 | 4.6 |
| ECE 464-001 | S 15 | 19 | 4.3 | 4.3 |
| ECE 520-001 | S 15 | 119 | 4.3 | 4.3 |
| ECE 520-601 | S 15 | 11 | 4.8 | 5.0 |
| ECE 520-603 | S 15 | 3 | | |
| ECE 520-651 | SuI 15 | 16 | 4.6 | 4.6 |
| ECE 733-001 | S 15 | 50 | 4.5 | 4.3 |
| ECE 464-002 | F 15 | 21 | 4.6 | 4.5 |
| ECE 520-002 | F 15 | 129 | 4.6 | 4.5 |
| ECE 520-601 | F 15 | 7 | 5.0 | 5.0 |
| ECE 634-602 ASIC Design | F 2014 | 6 | | |
| ECE 634-602 ASIC Design | F 2014 | 2 | | |
| ECE 520-601 | S1 2014 | 9 | | |



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| | | | | |
|---|---|---|---|---|
| ECE 464-001 | S 2014 | 10 | 4.5 | 4.5 |
| ECE 520-001 | S 2014 | 111 | 4.5 | 4.5 |
| ECE 520-601 | S 2014 | 9 | 4.5 | 4.5 |
| ECE 733-001 | S 2014 | 49 | 4.7 | 4.4 |
| ECE 520-601 | F 2013 | 2 | | |
| ECE 520-651 ASIC Design | SII '13 | 7 | 4.3 | 4.3 |
| ECE 464-051 ASIC Design | SII '13 | 6 | 4.5 | 4.5 |
| ASIC Design OOC | SII '13 | 635 | | |
| ECE 733 Digital Electronics | S 2013 | 62 | 4.5 | 4.3 |
| ECE 520-001 ASIC Design | S 2013 | 136 | 4.6 | 4.5 |
| ECE 464 ASIC Design | S 2013 | (with above) | 4.3 | 4.3 |
| ECE 520-651 ASIC Design | Sum '12 | 18 | | |
| ECE 733 Digital Electronics | S 2012 | 52 | 4.2 | 4.2 |
| ECE 520-601 | S 2012 | 12 | 4.3 | 4.2 |
| ECE 520-001 ASIC Design | S 2012 | 116 | 4.3 | 4.3 |
| ECE 464 ASIC Design | S 2012 | 14 | 4.3 | 4.3 |
| ECE 406 Des. Complex Systems | F 2011 | 58 | 4.6 | 4.6 |
| ECE 520-651 ASIC Design | Sum '11 | 13 | 4.2 | 4.2 |
| ECE 733 Digital Electronics | S 2011 | 18 | 4.5 | 4.5 |
| ECE 520-601 | S 2011 | 12 | 4.3 | 4.2 |
| ECE 520-001 ASIC Design | S 2011 | 75 | 4.5 | 4.5 |
| ECE 464 ASIC Design | S 2011 | 25 | 4.5 | 4.5 |
| ECE 406 Des Complex Systems | F 2010 | 75 | 4.6 | 4.6 |
| ECE 733 Digital Circuits 001 | S 2010 | 36 | 4.3 | 4.2 |
| ECE 733 Digital Circuits 601 | S 2010 | 3 | 5.0 | 5.0 |
| ECE 520 ASIC Design 001 | S 2010 | 57 | 4.3 | 4.4 |
| ECE 520 ASIC Design 601 | S 2010 | 17 | 4.2 | 4.4 |
| ECE 464 ASIC Design | S 2010 | 9 | 4.3 | 4.4 |
| ECE 733 Digital Circuits 001 | S 2009 | 57 | 4.6 | 4.5 |
| ECE 733 Digital Circuits 601 | S 2009 | 7 | 4.4 | 4.2 |
| ECE 520 ASIC Design 001 | S 2009 | 128 | 4.6 | 4.4 |
| ECE 520 ASIC Design 601 | S 2009 | 17 | 4.5 | 4.20 |
| ECE 520 ASIC Design 620 | S 2009 | 1 | | |
| ECE 464 ASIC Design | S 2009 | 16 | 4.6 | 4.4 |
| ECE 733 Digital Circuits 001 | S 2008 | 67 | 4.64 | 4.64 |
| ECE 733 Digital Circuits 601 | S 2008 | 2 | | |
| ECE 520 ASIC Design 001 | S 2008 | 101 | 4.76 | 4.59 |
| ECE 520 ASIC Design 601 | S 2008 | 15 | 4.5 | 4.20 |
| ECE 464 ASIC Design | S 2008 | 27 | 4.76 | 4.59 |
| ECE 733 | S 2007 | 58 | 4.64 | 4.46 |



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| | | | | |
|---|---|---|---|---|
| ECE 520 ASIC Design 001 | S 2007 | 129 | 4.75 | 4.68 |
| ECE 520 ASIC Design 601 | S 2007 | 6 | | |
| ECE 464 ASIC Design | S 2007 | 17 | 4.75 | 4.68 |
| ECE 745 ASIC Verification | F 2006 | 20 | | 4.6 |
| ECE 733 Digital Circuits 001 | S 2006 | 43 | 4.5 | 4.6 |
| ECE 520 ASIC Design 001 | S 2006 | 65 | | |
| ECE 520 ASIC Design 601 | S 2006 | 8 | | |
| ECE 464 ASIC Design 001 | S 2006 | 17 | 4.4 | 4.1 |
| ECE 733 Digital Circuits 001 | S 2005 | 30 | 4.5 | 4.6 |
| ECE 733 Digital Circuits 601 | S 2005 | 5 | | |
| ECE 520 ASIC Design 001 | S 2005 | 44 | 4.6 | 4.3 |
| ECE 520 ASIC Design 002 | S 2005 | 34 | 4.6 | 4.5 |
| ECE 520 ASIC Design 601 | S 2005 | 2 | | |
| ECE 464 ASIC Design 001 | S 2005 | 15 | 4.9 | 4.1 |
| ECE 464 ASIC Design 002 | S 2005 | 13 | 4.9 | 4.1 |
| ECE 733 Digital circuits | S 2004 | 45 | 4.2 (4.1) | 4.2 (3.9) |
| ECE 520 ASIC Design | S 2004 | 76 | 4.4 (4.1) | 4.3 (3.9) |
| ECE 520 ASIC Design 601 | S 2004 | 17 | | |
| ECE 464 ASIC Design | S 2004 | 69 | 4.5 (4.1) | 4.0 (3.9) |
| ECE 733 Digital Circuits | S 2003 | 84 | 4.3 (4.0) | 4.2 (3.8) |
| ECE 520 ASIC Design | S 2003 | 81 | 4.2 (4.0) | 3.9 (3.8) |
| ECE 520 ASIC Design 601 | S 2003 | 30 | | |
| ECE 464 ASIC Design | S 2003 | 63 | 3.9 (4.0) | 3.5 (3.8) |
| ECE 406 Design Complex DS | F 2002 | 167 | 4.2 (4.1) | 3.8 (3.9) |
| ECE 520 ASIC Design | S 2002 | 239 | 4.4 (4.1) | 4.2 (3.9) |
| ECE 520 ASIC Design 601 | S 2002 | | | |
| ECE 464 ASIC Design | S 2002 | 39 | 4.1 (4.1) | 3.6 (3.9) |
| ECE 406 Des. Complex Dig Sys | F 2000 | | 4.7 (4.0) | 4.5 (3.7) |
| ECE 704 Design For Test | F 2000 | | 4.6 (4.0) | 4 (3.8) |
| ECE 520 ASIC Design 001 | S 2000 | | 4.5 (4.1) | 4.4 (3.9) |
| ECE 520 ASIC Design 002 | S 2000 | | 4.6 (4.1) | 4.3 (3.9) |
| ECE 520 ASIC Design 601 | S 2000 | | | |
| ECE 492B ASIC Design | S 2000 | | 4.5 (4.1) | 4.3 (3.9) |
| ECE 342 Des. Complex Dig Sys | F 1999 | | 4.4 (4.1) | 4 (3.9) |
| ECE 520 ASIC Design 005 | S 1999 | | 4.6 (4.2) | 4.5 (4.0) |
| ECE 520 ASIC Design 006 | S 1999 | | 4.5 (4.2) | 4.3 (4.0) |
| ECE 342 Des. Complex Dig Sys | F 1998 | | 4.3 (4.1) | 4.1 (3.9) |
| ECE 520 ASIC Design | S 1998 | | 4.6 (4.1) | 4.4 (3.9) |
| ECE 492B ASIC Design | S 1998 | | 4.7 (4.1) | 4.8 (4.1) |
| ECE 342 Des. Complex Dig Sys | F 1997 | | 4.6 (4.0) | 4.4 (4.0) |
| ECE 520 ASIC Design | S 1997 | | 4.7 (4.1) | 4.7 (3.9) |



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| | | | | |
|---|---|---|---|---|
| ECE 492B ASIC Design | S 1997 | | 4.7 (4.1) | 4.4 (3.9) |
| **AVERAGE** | | | | |

- ECE 342 Design of Complex Digital Systems, Fall 1996, Overall Rating: 4.6/5.0.
- ECE 592B ASIC Design, Spring 1996, Overall Rating: 4.75/5.0. (With Dr. Liu.)
- ECE 492B ASIC Design, Spring 1996, Overall Rating: 4.00/5.0. (With Dr. Liu.)
- ECE 544, Design of Electronic Packaging and Interconnects, Spring 1999, Overall Rating : 4.60/5.0.
- ECE 520, Fundamentals of Logic Systems, Fall 1995, Overall Rating: 4.50/5.0.
- ECE 218, Computer Organization and Microprocessors, Both Sections, Spring, 1995: Section 001: 4.45/5.0; Section 002: 4.62/5.0.
- ECE 592V, VLSI Microprocessor Project, Spring 1995. (13 students but not rated).
- ECE 681/693A, Computer Engineering Seminar. Spring 1996 and Fall 1996.
- ECE 521 Computer Design and Technology, Fall 1994, Overall Rating: 4.24/5.0.
- ECE 691F, High Speed VLSI, Fall 1994, Overall Rating: 4.45/5.0.
- ECE 691P, Superscalar Processor Design, Spring 1994, Overall Rating: 4.67/5.0.
- ECE 591F, Design of Electronic Packaging and Interconnects, Spring 1994, Overall Rating: 4.60/5.0.

## B. INSTRUCTIONAL DEVELOPMENT

1. NSF-funded CISE Infrastructure effort, “Experimental High Performance Computing and Communications Systems". (Total: $1,338,283 including $503,046 in matching.) Approximately $283,000 of this funding went towards outfitting the ECE Design Center.

2. CAD Tools. Modern design is done with sosphisticated Computer – Aided Design Tools, not with pencil and paper. I have spent considerable effort bringing such tools into the Unity environment, gaining the `corporate knowledge' about how to use these tools effectively and obtaining additional computers for use with these tools. *Students tell me that knowledge of these tools is highly regarded by potential employers. In fact one student stated that `Dr. Franzon teaches courses that gets jobs'. In addition , in 1999, we won the Cadence University Alliance Best Web site Awards.* Through my funded research efforts and Corporate Donations introduced the following Computer Aided Design Tools into the curricula:

- Cadence Design Systems. A complete suite of over 4 GB of executables that facilitate chip, board and system design, with a retail value of over $100,000,000. Cadence donates these tools because of the widespread recognition of our contributions to CAD. (i.e. It waives the $5,000 fee.)
- Synopsys. The industry leading chip (ASIC) synthesis tool,with a retail value of over $7,000,000.
- In 2008, NCSU won the “Babbage Award” from Sun and Synopsys, in recognition of our contributions towards lab infrastructure. The award comes in the form of $15,000 of computers.



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- Mentor. We integrate some mentor graphics tools with the other tools above. The tools have a retail value of over $5,000,000. Mentor donates these tools because of the widespread recognition of our contributions to CAD.
- Mentor donates $30,000 annually to the University to assist in CAD infrastructure development.

As well as obtaining these tools, my group has spent considerable effort making these tools useful to us by writing integration scripts and generating `know-how'. Much of this `know-how' has been published on the Web and in our own lockers. Most of this learning was conducted driven by research needs and serves as an excellent example of the integration of research and teaching. This work is ongoing. For example, over 2000 organizations world-wide, use our "Physical Design Kit"..

3. ECE 745. ASIC Verification. I introduced this course in 2007, though it was taught by Meeta Yadav.

4. ECE 342, Design of Complex Digital System, Fall 1996:
   - Completely redesigned and updated course to reflect modern design practices, and use of modern Hardware Description Languages and Design Tools.
   - Completed a new laboratory course ECE 342L for use with this course.

5. ECE 520 ASIC Design (formerly `Fundamentals of Logic Systems'), Spring 1997:
   - Based on my teaching of ECE592B in Spring 1995, this course has been completely updated to reflect modern design practices, modern tools, and emphasize an understanding of algorithms used in modern tools. (`ASIC' stands for `Application Specific Integrated Circuit'. For example the chips in a satellite dish receiver are ASICs. ASIC engineering is the fastest growing area of ECE today.)
   - Once the course action forms are approved, this course will be taught concurrently with ECE 420 ASIC Design.

6. ECE 544, Design of Electronic Packaging and Interconnects, Spring 1995. New course emphasizing `transmission line effects' in electronic packages and how to design `deep sub-micron interconnect'. I receive tremendous demand from industry for graduates from this course.

7. ECE 691/693A, Computer Engineering Graduate Seminar
   - Created new seminar course (with Dr. Tom Conte) for computer engineering students.
   - Recruited and scheduled weekly speakers.

8. ECE CAD Lab. $75,000. Provost Office, 1995.

## C. MENTORING ACTIVITIES

UNDERGRADUATE STUDENT SUPERVISIOR

1. 2012. Spring advisor to two undergraduates.



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2. 2010. Summer REU supervisor to three Undergraduates
3. 2009. Summer REU supervisor to one Undergraduate.
4. 2009. Supervised Senior Design Team
5. 2008. Summer REU supervisor to two Undergraduates.
6. 2005 Andrew Pita, SRC Undergraduate Research Fellowship
7. 1999 Ecoh Oh, NSF Undergraduate Research Award
8. 1999 Ben Hughes, NSF Undergraduate Research Award
9. 1993- Numerous Senior Design projects

GRADUATE STUDENT SUPERVISION

GRADUATE COMMITTEES

Currently member of several PhD and MS committees.

GRADUATE COMMITTEES

For a list of graduate committees I chair, see below. I am on numerous committees as a member, but I do not track the numbers.

## D. MASTER'S AND DOCTORAL THESES DIRECTED AND BEING DIRECTED

**Masters and Doctoral Theses under direction**

| Student's Name | Ph.D. MS | Chair/ Co-chair |
|---|---|---|
| Han Pan | PhD | x |
| Ahmad Benaki | PhD | x |
| George Li | PhD | X |
| Wen Yuejing | PhD | X |
| Josh Stevens | PhD | X |
| Archit Gaijar | PhD | X |
| Priyank Kashyap | PhD | X |
| Batool Khader | PhD | X |

I do not track memberhips.

Doctoral Theses Directed

1. Luis Francisco, "Machine Learning for Design Rule Checking, Multilayer CMP Hotspot Detection, using Transfer Learning and Synthetic Training", May 202, co-Chair..
2. Billy Huggins, "An Evolutionary Approach to Producing Optimal Electronic Design Automation Tool Settings", May 2021, co-chair.



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3. Theodros Nigussie, "Design obfuscation throught smart partitioning and 3D integration,", Mar. 2020, chair.
4. Kirti Bhanashuli, "On implementing power-efficient and scalable short-range RF-power radios using RF-only architectures," Jan., 2020, chair.
5. Yi Wang, "Solving Inverse Problem through optimization and its application to Analog/RF Design," March 2020, chair.
6. Bowen Li, "High-speed receiver behavioral modeling using machine learning,", Jan. 2020, chair.
7. Sumon Dey, "Design of a scalable, confirugate and cluster-based hierarchical hardware accelerator for a cortically inspired algorithm and recurrent neural networks," August, 2019, chair.
8. Weifu Li. Design of Hardware Accelerators for Hierarchical Temporal Memory and Convolutional Neural Networks", August 2019, chair.
9. Nazia Zannat, "Design of contactless connectors for simultaneous power and data transfer," May, 2019, chair.
10. Zhao Wang, "Efficient linear matrix solver and its hardware implementations dedicated to faster than real time dynamic simulation of large scale power systems," September, 2018, chair.
11. Lee Baker, "Design of a 3DIC system to aid in the acceleration of embedded system that employ multiple instances of disparate artificial neural networks," March 2018, chair.
12. Jong Beom Park, "A circuit level three-dimensional DRAM area timing and energy model," March 2018, co-chair.
13. Josh Schabel, "Design of an application specific instruction set processor for sparse neural networks,", October 2017, chair.
14. Weiyi Qi, "IC Design Analysis, Optimization and Reuse via Machine Learning, August, 2017, Chair.
15. Wenxu Zhao, "RF-only Logic Enbabled RFID Transponder Size Reduction,", December 2016. Chair.
16. Marcus Tshibangu, "Study and analysis of Energy Efficient DRAM Cache with unconventional row buffer size," August 2016. Chair.
17. Randy Widialaksono, "Three Dimensional Integration of Hterogeneous Multi-Core Processors," June, 2016. Co-chair.
18. Zhenquian Zhang, "Design of On-chip bus of Heterogeneous 3DIC Micro-processors," May 2016, Chair.
19. Sarkar, Biplap, "Atomic Layer Deposition Techniques for Novel Memory Applications," August 2015. Cochair
20. Winick, David, "Electroactive Polymer Refreshable Braille Display, December 2015 (Posthumous).
21. Gary Charles, "Design, Model and Analysis of TSV-based On-Chip PDN Interconnects for 3-D Integrated Circuits. ", March 2015.
22. Zhao Yan, "S-Parameter Based Binary Multimode Interconnect Design Methodology and Implementation," December, 2014 .
23. W.S. Pitts, "High quality CMOS Integratable Varactors," March 2014.
24. Peter Gadfort, "Packaging and Integration of Three Dimensional Microsensors," December, 2013.
25. Evan Erickson, "Multi-Gbps Inductively Coupled Connectors," December, 2013.



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26. Akalu Lentiro, "Low-Density, Ultra-Low Power and Smart Radio Frequency Telemetry Sensor," October, 2013.
27. Shivam Priyadarshi, "System and Gate Level Dynamic Electrothermal Simulation of Three Dimensional Integrated Circuits," June, 2013.
28. Eric Wyers, "Direct Search Calibration Algorithms for Digitally Reconfigurable Radio Frequency Integrated Circuits," March 2013.
29. Ojas Ashok BOpat, "A Generic Scalable Architecture For a Large Acoustic Model and Large Vocabularly Speech Recognition Accelerator," October, 2012.
30. Won Hao Choi, "System Level Power Prediction Methodology for Mobile 3-D Graphic Engines," May 2012.
31. Hsuan-Jung Su, "Continuous-Time Fractionally Spaced Equalization and Its Application in Capacitively Coupled Chip-To-Chip Interconnect," May, 2012.
32. Matthew Hamlett, "A Novel Approach to IP Protection Using Automated Hardware Techniques to Secure a Design," March 2012.
33. Mustafa Berke Yelten, "Variability and Reliability in Nanoscale Circuits: Simulation, Desgin, Monitoring and Characterization," January, 2012.
34. Hoon Seok Kim, "Advanced Multi Mode Interconnect," December, 2011.
35. Xiangzhong Xue, "Electronic System Optimization Via Convex Programming," December, 2011.
36. Tsing Zhu, A Surrogae Model-based Framework for Design and Macromodeling of Self-calibrated Analog Circuits," October, 2011.
37. Chanyoun Won, "Multimode Interconnect for High-Density Links: Implementation, Design Methodology and New Crosstalk Cencallation Scheme," July 2011
38. Thor Thorolfsson, "Three Dimensional Integration of Synthetic Aperture Radar Processors," April 2011
39. Daniel Schinke, "Computing with Novel Floating Gate Devices," April 2011
40. Yongjin Choi, "Design of Multimodel Signaling Transceiver for High-Density and High-Speed Links," May 2010.
41. Eun Chu Julie Oh, Ph.D. Dissertation, "Design and Applications of Three-Dimensional Circuits", December, 2009.
42. Karthik Chandrashekhar, Ph.D. Dissertation, "Inductively Coupled Connectors," December, 2008
43. Dhruba Chandra, Ph.D. Dissertation, Speech Recognition CoProccessor, December, 2007.
44. Meeta Yadav, "Hardware Architecture of behavior Modeling Coprocessor for Network Intrusion Detection," Ph.D. Dissertation, March, 2007.
45. Ullas Pazhayaveetil, "Hardware Implementation of a Low Power Speech Recognition System," Ph.D. Dissertation, February, 2007.
46. Jian Xu, "AC Coupled Interconnect for Inter-Chip Communications," Ph.D. Dissertation, December, 2006.
47. Ambrish Varma, "Improved behavioral modeling based on Input Output Buffer Information Specification," Ph.D. Dissertation, NCSU, October, 2006.
48. Sachin Sonkusale, "Planar edge defined alternate layer process (PEDAL) – an unconventional technique for the fabrication of wafer scale sub-25 nm nanowires and nanowire template," PhD, October, 2006.



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49. Liang Zhang, "Driver Pre-emphasis Signaling for on-chip global interconnects," Ph.D. Dissertation, September, 2006.
50. Monther Al Dwairi, "Hardware Efficient Pattern Matching Algorithms and Architectures for Fast Intrusion Detection," Ph.D., November, 2006.
51. John Damiano, "Active body bias for low-power silicon-on-insulator design," Ph.D., March 2006.
52. Neil DiSpigna, "Electronic Devices and Interface Strategies for Nanotechnology," Ph.D., April 2006.
53. Christian Amsinck, "Molecular Electronic Memories," Ph.D., March 2006.
54. Lei Luo, "Capacitively Coupled Chip to Chip Interconnect Design, Ph.D., December, 2005.
55. Leon Zhang, "Driver pre-emphasis signaling for on-chip global interconnects," Ph.D., December, 2005.
56. Steve Lipa, "Phase Noise Analysis of Rotary Oscillators," Ph.D. May 24, 2005
57. David Nackashi, Circuit and Integration Technologies for Molecular Electronics, Ph.D. 2004
58. Stephen Mick, AC Coupled Interconnect, Ph.D. 200
59. John Wilson, Linearly Tunable RF MEMS Capacitors Implemented Using an Integrated Removable Self-Masking Technique, Ph.D. 2004
60. Andrew Stanaski, Sensor Circuits for Flip Chip Debug, Ph.D. 2004
61. Pronita Mehrotra, High Performance Hardware Memory Algorithms, Ph.D. 2003
62. Bruce Duewer, MEMS Switch Fabric, Ph.D.
63. Toby Schaffer, Chip-package Codesign, Ph.D.
64. Mouna Nakkar, Dynamically Programmable Cache, Ph.D.
65. Mir Azam, Custom CMOS Design and Architecture for Low-Power High-Performance Circuits, PhD.
66. Debu Ghosh (co-chair), Synthesis of Benchmarking Expiriments, Ph.D.
67. Chris Harvatis, Performance Driven Partitioning for MCMs, PhD.
68. Slobodan Simovich, Computer-Aided Analysis of Interconnect,PhD.
69. Scott Washabaugh, Low energy FSM Design, PhD.
70. Sharad Mehrotra, Automated Synthesis of High Speed Digital Circuits and Package-Level Interconnect, PhD.
71. Todd Cook, Instruction Set Architecture Specification, PhD.
72. Robert Evans, Energy Consumption for Modeling and Optimization of SRAMs, PhD.

<u>Masters Theses directed</u>

1. Abhishek Bhattacharya, "Design and Power Optimization of a16 nm Dual Floating Gate FET Memory Array and Peripheral Circuits," October, 2013.
2. Joshua Schabel, "An Analysis of Subthreshold SRAM Bitcells for Operation in Low Power RF only Technologies," July 2013.
3. Vinod Kotipllai, "Impact of Process Variations on 16-nm Dual Floating Gate FET using TCAD simulations," December 2012.
4. Wenxu Zhao, "Headphone Deiver Design with Inductive Coupled Interconnection," November, 2012.



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5. Shiney Gupta, "Multi-Storey Stacked Driver Topolo9gy for Reduced Swing and Low Power Bus Operation,", May 2012.
6. Pattabhiraman Ravindran, "Harvesting Thermal Energy to Power Agricultural Sensors," October, 2011.
7. Alex Leaonard, "Implementation of a System-on-Chip for self-healing of analog receiver components in a 65 nm CMOS process", May 2011
8. Seema Kumar, "Memory Diesgn for Sensor IC," May 2010.
9. Mihir Shiveshwarkar, "A Nanocrystal Floating Gate Flash Analog to Digital Converter," December, 2009.
10. Ojas Bapat. "Design of DDR2 Interface for Tezzaron TSC8200A Octupus Memory intended for Chip Stacking Applications," April 2009.
11. Peter Gadfort, "Low power driver for silicon carrier interconnects," April 2009.
12. Chintan Shah, "Inductively Coupled Interconnect for Chip to Chip Commmunication over Transmission Line," Feb 2009.
13. Kiran Gonsalves, "Memory Design for FFT Processor in 3DIC Technology," March, 2009.
14. Vinay Honnavara, "Cost optimization by method of allocating software component units to electronic control units for model-driven designs," October, 2008.
15. Wei Cao, "Design of temperature sensors for validation of aseptic food processing," Sept. 2008.
16. Akalu Lentiro, "Implemention of AC Coupled Interconnect Test Vehicle," May, 2008.
17. Vinayak Devasthali, "Application of body biasing and supply voltage scaling techniques for leakage reduction and performance improvement of CMOS Circuits," December 2007.
18. Paul Fernando, "Adding scalability to IBIS using AMS Languages," September 2007.
19. Vivek Jayadav, "Hardware-Software Codesign of a Large Vocabularly Speech Recognition System," February, 2007.
20. Srivatsan Parthasarathy, "Interfacing AC Coupled Interconnect Design with Rocket I/O compatible FPGA Systems," December 2006.
21. Janani Mukundan, "Instruction Cache Checkpoints Using Phase Tracking and Prediction," June 2006.
22. Yasaswini Sudarsanam, "Implementatin of Double Precision Floating Point Arithmetic for Matrix Multiplication," October 2006
23. Itisha Tyagi, "Design of array based row decoders and self-referencing sense amplifier for large scale resistance change style molecular memories," June 2006.
24. Indraneel Kelkar, "Tradeoffs involved in the design of SRAMs," December 2005.
25. Wallace Pitts, "Partially depleted silicon on insulator phase lock loop design," January, 2006.
26. Janani Mukundan, "Instruction cache checkpoints using phase tracking and prediction," December 2006.
27. Deepak Kumar, "Design of fully integrated wireless CMOS MEMS device for intraocular pressure measurement," March 2006.
28. Manav Shah, "Design of a self-test vehicle for AC Coupled Interconnect Technology," May 2006.



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29. Andrew Morgan, Design Flow based on Sensitivity Analysis for High Speed Digital Circuits, MS, 2004
30. Brian Phelp, Hardware Realization and Implementation Issues for the Sliding Window Packet Switch, MS, 2004
31. Ishdeep Sawhney, Hardware Forwarding for IPV6, MS, 2003
32. Kaustabh Bhate, MEMS Design for textiles sensor, MS
33. Praveen Prasad, Reconfigurable Computing for Network Security, MS
34. Patrick Lall, Verification of a Network Processor, MS
35. Ambrish Varma, SHOCC Design Tools, MS
36. Karthik Chandrasekhar, Hardware to support multicast in all-optical networks, M
37. V. Parameshawara (co-chair), Enhancement of NC Agricultural Automated Weather Network and Development of Advanced Communication, Data Acquisitions amd Dissemation System, MS.
38. Jeremy Palmer, Design and Analysis of a VLSI-MEMS-Based Diffractive Optical Beam Steering System, MS.
39. Som Chaudry, MEMS devices for laser radar, MS.
40. Srisai Rao, Design, place and route of an IDEA processor, MS.
41. Kevin Mock, IDEA Implementation, MS.
42. Sibi Kuruvilli, Synthesized SAND Issue Unit, MS
43. Tom Mills, Macromodelling of high speed digital drivers and receivers, MS.
44. Matreiya Sengupta, Managing Crosstalk in Interconnect Design, MS.
45. Andrew Stanaski, Optimizing Memory Design for Packagability, MS.
46. Jonathon Schaeffer, A 400 MHz CMOS Multiplier, MS.
47. Harsh Deshmane, MCM Extractor in Magic, MS.
48. Sha Ma, Circuits for Low Energy Computing, MS.
49. Shauki Elassaad, Placement tools for multi-chip modules, MS.
50. Alex Dalal, CAD tools for yield estimation, MS.

Committee Memberships: Do not track

## D. HONORS AND AWARDS RELATED TO TEACHING AND MENTORING

- Board of Governers Teaching Award for Excellence in Teaching, 2014
- Babbage Award, Synopsys, 2008
- ECE Graduate Teacher of the year award, 2007
- ECE Most Helpful Teacher of the year award, 2007
- ECE Teacher of the year award, 2006
- ECE Graduate Advisor of the year award, 2006
- Alumni Undergraduate Distinguished Professor, 2003-2005.
- Graduate teacher of the year, ECE department, 2005
- Selected to the NCSU Academy of Outstanding Teachers, 2001
- First round prize winner, SRC copper challenge, 2000.
- Teacher of the Year Award, presented by the IEEE Student Branch, 1997



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# III. SCHOLARSHIP IN THE REALMS OF FACULTY RESPONSIBILITY

## A. PUBLICATIONS AND AWARDS

BOOKS

1. P. Franzon, E. Martissen, M. Bakir (eds), "3DIC Handbook Design and Test" (Wiley), 2019.

2. Smith and P. Franzon*: Verilog Styles for Synthesis of Digital Systems*, 2000, by Prentice Hall.

3. D. Doane and P. Franzon: *Multichip Modules: Basics and Alternatives*, 1993, by Van Nostrand Rheinhold.

4. J-D Cho and P.D. Franzon, *High Performance Design Automation for Multi-Chip Modules and Packages*, 1996, World Scientific.

BOOK CHAPTERS

1. Yi Wang, P. Franzon, "Solving the inverse problem through optimization – Applications to Analog/RF IC Design," to appear in "Surrogate Modeling for High-Frequency Design - Recent Advances", S. Koziel (ed). 2021. (World Scientific)

2. P. Franzon, "3D Integration: Technology and Design," in "3D Integration in VLSI Circuits," in K. Sakuma (ed), 2018.

3. P. Franzon, "Electronic Design Automation for 3D", in "3D Handbook Design and Test,", P. Franzon, E. Martissen, M. Bakir (eds), (Wiley), 2019.

4. P. Franzon, "3D Design Styles", in "3D Handbook Design and Test,", P. Franzon, E. Martissen, M. Bakir (eds), (Wiley), 2019.

5. G. Burr, P. Franzon, "Storage Class Memories", in "Emerging Nanoelectronic Devices," An Chen, J. Hutchby, V. Zhrinov, G. Bourianoff, (Wiley), 2014.

6. P. Franzon, M. Swaminathan, "Chip Package Codesign," in The Handbook for EDA of Electronic Circuits, Lou Scheffer, Luciano Lavagno and Grant Martin (editors), CRC Press, 2015. (Second Edition.)

7. Eric Wyers, Tim Kelley, and Paul Franzon, "Optimization for Self-Calibrating Circuits," in Semiconductor Devices in Harsh Conditions, (CRC), 2015.



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**8.** Ting Zhu, Mustafa Berke Yelten, Michael B. Steer, and Paul D. Franzon**, "**Model-based Variation Aware Integrated Circuit Design", (Springer)

9. P. Franzon, "Use of AC Coupled Interconnect in Contactless Packaging," in "Coupled Data Communications," Ron Ho and Ivan Sutherland (ed), Springer-Verlag, Fall 2010

10. P. Franzon, *Design for 3-D Integration,* 3-D IC Integration: Technology and Applications, P. Garrou, P. Ramm, C. Bower, (editors), Wiley VCH, May 2008.

11. P. D. Franzon, D. Nackashi, C. Amsinck, N. DiSpigna, S. Sonkulale, "Molecular Electronics – Devices and Circuits Technology", in Vlsi-Soc: From Systems To Silicon, (Springer Boston), Oct. 2007.

12. P. Franzon, *Chip-Package Codesign,* in The Handbook for EDA of Electronic Circuits, Lou Scheffer, Luciano Lavagno and Grant Martin (editors), CRC Press, 2005.

13. P. Franzon, *Multichip Module Technology*, to appear in the The Electronic Handbook, J. Whitaker (editor), (CRC Press), 1996.

*14.* S. Mehrotra and P. Franzon, *Performance Driven Global Routing and Wiring Rule Generation for High Speed PCBs and MCMs* , in Advanced Routing of Electronic Modules, M. Pecht (editor), (Kluwer), 1995.

*15.* P. Franzon and Michael Steer: *Tools and Techniques for the Design of High Speed Multichip Modules*}, Chapter 7 in Electronics Packaging Forum,Volume 3, J. Morris (ed), 1993 by IEEE Press.

16. P. Franzon, *Comparison of Reconfiguration Schemes for Defect Tolerant Mesh Arrays* , in Defect and Fault Tolerance in VLSI Systems, Volume 2, V.K. Jain (editor), (Plenum), 1989.

17. M. Hatamian, L.A. Hornak, T. Little, S.K. Tewksbury and P. Franzon: *Fundamental interconnection issues* in, Electronic Materials Handbook,Volume 1:Packaging, Article 1BA (ASM International), 1989, pages 1-11.

18. P. Franzon and S.K. Tewksbury: *'Chip Frame'* scheme for reconfigurable mesh-connected arrays, in Wafer Scale Integration II, R.M. Lea (editor), (North Holland), 1988.

19. P.D. Franzon: *Yield Modeling for Fault Tolerant VLSI* ,in Systolic Arrays, W. Moore, A. McCabe and R. Urquhart (editors), (Adam Hilger), 1987.

<u>JOURNAL PUBLICATIONS</u>



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1. L. Francisco, W. Rhett Davis and P. Franzon, "A Deep Transfer Learning Design Rule Checker with Synthetic Training," in *IEEE Design & Test*. 2022. doi: 10.1109/MDAT.2022.3162786

2. K. Bhanushali, W. Zhao, W. S. Pitts and P. D. Franzon, "A 125 μm × 245 μm Mainly Digital UHF EPC Gen2 Compatible RFID Tag in 55 nm CMOS Process," in *IEEE Journal of Radio Frequency Identification*, vol. 5, no. 3, pp. 317-323, Sept. 2021.

3. P. Kashyap, F. Aydin, S. Potluri, P. D. Franzon and A. Aysu, "2Deep: Enhancing Side-Channel Attacks on Lattice-Based Key-Exchange via 2-D Deep Learning," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 40, no. 6, pp. 1217-1229, June 2021.

4. N. Zannat and P. D. Franzon, "Asymmetric Transformer Design With Multiband Frequency Response for Simultaneous Power and Data Transfer," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 10, no. 4, pp. 644-653, April 2020.

5. P. Kashyap, F. Aydin, S. Potluri, P. Franzon and A. Aysu, "2Deep: Enhancing Side-Channel Attacks on Lattice-Based Key-Exchange via 2D Deep Learning," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020.*

6. B. Li, B. Jiao, C. Chou, R. Mayder and P. Franzon, "Self-Evolution Cascade Deep Learning Model for High-Speed Receiver Adaptation," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 10, no. 6, pp. 1043-1053, June 2020.

7. Yi Wang, P. Franzon, D. Smart, B. Swahn, “Multi-fidelity surrogate-based optimization for electromagnetic simulation acceleration”, ACM Trans. Design Automation of Electronic Systems, Aug. 2020, No. 45

8. J. B. Park, W. R. Davis and P. D. Franzon, "3-D-DATE: A Circuit-Level Three-Dimensional DRAM Area, Timing, and Energy Model," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 2, pp. 756-768, Feb. 2019.

9. S. W. Park, L. B. Baker and P. D. Franzon, "Appliance Identification Algorithm for a Non-Intrusive Home Energy Monitor Using Cogent Confabulation," in *IEEE Transactions on Smart Grid*, vol. 10, no. 1, pp. 714-721, Jan. 2019.

10. J. C. Schabel and P. D. Franzon, "Exploring the Tradeoffs of Application-Specific Processing," in *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 8, no. 3, pp. 531-542, Sept. 2018.

11. W. Zhao, P. Gadfort, K. Bhanushali and P. D. Franzon, "RF-Only Logic: an Area Efficient Logic Family for RF-Power Harvesting Applications," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 1, pp. 406-418, Jan. 2018.



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12. B. Sarkar, S. Mills, B. Lee, W. Pitts, V. Misra, P. Franzon, “On Using the Volatile Mem-Capacitive Effect of TiO2 Resistive Random Access Memory to Mimic the Synaptic Forgetting Process,” in Journal of Electronic Materials, v 47, n 2, p 994-997, February 1, 2018

13. Kim, C. Won and P. D. Franzon, "Corrections to “Crosstalk-Canceling Multimode Interconnect Using Transmitter Encoding”[ Aug 13 1562-1567]," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 5, pp. 1792-1792, May 2017.

14. E. J. Wyers, M. A. Morton, T. C. L. G. Sollner, C. T. Kelley and P. D. Franzon, "A Generally Applicable Calibration Algorithm for Digitally Reconfigurable Self-Healing RFICs," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 3, pp. 1151-1164, March 2016.

15. Z. Yan, K. Aygün, H. Braunisch and P. D. Franzon, "Multimode High-Density Link Design Methodology and Implementation," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 6, no. 8, pp. 1251-1260, Aug. 2016.

16. G. Charles and P. D. Franzon, "A Multitier Study on Various Stacking Topologies of TSV-Based PDN Systems Using On-Chip Decoupling Capacitor Models," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 5, no. 4, pp. 541-550, April 2015

17. Bapat, O.A.; Franzon, P.D.; Fastow, R.M., "A Generic and Scalable Architecture for a Large Acoustic Model and Large Vocabulary Speech Recognition Accelerator Using Logic on Memory," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on* , vol.PP, no.99, pp.1,1, 2014.

18. Xi Chen; Ting Zhu; Davis, W.R.; Franzon, P.D., "Adaptive and Reliable Clock Distribution Design for 3-D Integrated Circuits," Components, Packaging and Manufacturing Technology, IEEE Transactions on , vol.4, no.11, pp.1862,1870, Nov. 2014

19. Gadfort, P.; Franzon, P.D., "Millimeter-Scale True 3-D Antenna-in-Package Structures for Near-Field Power Transfer," Components, Packaging and Manufacturing Technology, IEEE Transactions on , vol.4, no.10, pp.1574,1581, Oct. 2014

20. Priyadarshi, S.; Davis, W.R.; Steer, M.B.; Franzon, P.D., "Thermal Pathfinding for 3-D ICs," Components, Packaging and Manufacturing Technology, IEEE Transactions on , vol.4, no.7, pp.1159,1168, July 2014

21. Sarkar, B.; Ramanan, N.; Jayanti, S.; Di Spigna, N.; Bongmook Lee; Franzon, P.; Misra, V., "Dual Floating Gate Unified Memory MOSFET With Simultaneous Dynamic and



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Non-Volatile Operation," *Electron Device Letters, IEEE* , vol.35, no.1, pp.48,50, Jan. 2014

22. Wyers, E.J.; Steer, M.B.; Kelley, C.T.; Franzon, P.D., "A Bounded and Discretized Nelder-Mead Algorithm Suitable for RFIC Calibration," *Circuits and Systems I: Regular Papers, IEEE Transactions on* , vol.60, no.7, pp.1787,1799, July 2013

23. HoonSeok Kim; Chanyoun Won; Franzon, P.D., "Crosstalk-Canceling Multimode Interconnect Using Transmitter Encoding," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on* , vol.21, no.8, pp.1562,1567, Aug. 2013

24. T. Zhu, M. Steer, P. Franzon, "Surrogate model-based self-calibrated design for process and temperature compensation in Analog/RF circuits," in IEEE Design and Test, Vol. PP, No. 99, 2013.

25. M.B. Yelten, P.D. Franzon, M.B. Steer, "Analog Negative Bias Temperature Instability Monitoring Circuit," in IEEE Trans. Device and Materials Reliability, Vol. 12., No. 1, 2012, pp. 177-179.

26. R.T. Harris. S. Priyadarshi, S. Melamed, C. Ortega, M. Rajit, S. Doorly, N. Kriplani, W. Davis, P. Franzon, M. Steer, "A transient electrothermal analysis of three-dimensional integrated circuits," in IEEE Trans. CPMT, Vol. 2, No. 4, 2012, pp. 660-667.

27. S. Priyadarshi, C. Saundrs, N Kriplani, H. Demiricoglu, W. Davis, P. Franzon, M.B. Steer, "Parallel transient simulation of multiphysics circuits using delay-based partitioning," in IEEE Tran. CAD, Vol. 31, No. 10, 2012, pp. 1522-1535.

28. S. Melamed, T. Thorolfsson, R.T. Harris, S. Priyadarshi, P.D. Franzon, M.B. Steer, W.R. Davis, "Junction level thermal analysis of 3-D integrated circuits using high definition power blurring," in IEEE Trans CAD, Vol. 31, No. 5, 2012, pp. 676-689.

29. M.B. Yelten, T. Zhu, S. Koziel, P.D. Franzon, M.B. Steer, "Demystifying Surrogate Modeling for Circuits and Systems," in IEEE Circuits and Systems Magazine, VOl. 12, No. 1, 2012, pp. 45-63.

30. S. Priyadarshi, T.R. Harris, S. Melamed, C. Otero, N.M. Kriplani, C.E. Christoffersen, R. Manohar, S.R. Dooley, W.R.Davis, P.D. Franzon, M.B. Steer, "Dynamic Electrothermal Simulation of Three-Dimensional Circuits Using Standard Cell Macromodels," in IET Circuits, Devices, and Systems, Vol. 6., No. 1., 2012, pp. 35-44.

31. M.B. Yelten, P.D. Franzon, M.B. Steer, "Analog Negative Bias Temperature Instability Monitoring Circuit," in IEEE Trans. Devices and Materials Reliability, Vol. 12, No. 1, 2012, pp. 177-179.



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32. P. Chakraborti, H. Topraki, P. Yand, N. DiSpigna, P. Franzon, T. Ghosh, "A compact dielectric elastomer tubular actuator for refereshable Braille displays," in Sensors and Actuators A:Physical, V> 179, p. 151-157, June 2012.

33. T.R. Harris, S. Priyadarshi, S. Melamed, C. Ortega, R. Manohar, S.R. Dooley, N.M. Kriplani, W.R. Davis, P.D. Franzon, M.B. Steer, "A Transient Electrothermal Analysis of Three-Dimensional Integrated Circuits," in IEEE Trans CPMT, Vol. P, Issue 99, 2012, pp. 1.

34. T. Zhu, M.B. Steer, and P.D. Franzon, "Accurate and Scalable IO Buffer Macromodel Based on Surrogate Modeling," in IEEE Transactions CPMT, VOl. 1, Issue 8, 2011, pp. 1240-1249.

35. M.B. Yelten, P.D. Franzon and M.B. Steer, "Surrogate Model-Based Analysis of Analog Circuits – Part I. Variability Analysis," in IEEE Trans. Device and Materials Reliability, Vol. PP, Issue 99, 2011.

36. M.B. Yelten, P.D. Franzon and M.B. Steer, "Surrogate Model-Based Analysis of Analog Circuits – Part II. Reliability Analysis," in IEEE Trans. Device and Materials Reliability, Vol. PP, Issue 99, 2011.

37. D. Schinke, N. DiSpigna, M. Shiveshwarkar, and P. Franzon, "Computing With Novel Floating Gate Devices", in IEEE Computer, Vol. 44, No. 2, 2011, pp. 29-36.

38. D. Schinke, S. Priyadarshi, W.S. Pitts, N.H. DiSpigna, P.D. Franzon, "SPICE-compatible Physical Model of Nanocrystal Floating Gate Devices for Circuit Simulation," in IET Circuits, Devices and Systems, Vol. 5, No. 6, 2011, pp. 477-483.

39. T. Thorolffson, N. Moezzi-Madani, P.D. Franzon, "Reconfigurable five-layer three-dimensional integrated memory on logic synthetic aperture radar processor, in IET Computers and Digital Techniques, Vol. 5, Issue 3, 2011, pp. 198-204.

40. L. Zhang, J.M. Wilson, R. Bashirullah, L. Luo, J. Xu, P. Franzon, "A 32-Gb/s on-chip Bus with Driver Pre-Emphasis Signaling," in Trans. VLSI, Vol. 17, No. 9, Sept. 2010, pp. 1267-74.

41. H. Tao, D. Corley, M. Lu, N. DiSpigna, D. Nackashi, P. Franzon, J. Tour, "Controllable Molecular Modulation of Conductivity in Silicon Based Devices," in Journal of the American Chemical Society, 131(29), 2009, pp. 10023-30.

42. W. Davis, E. Oh, A. Sule, T. Thorolfsson, and P.D. Franzon, "Application Exploration for 3-D Integrated Circuis: TCAM, FIFO and FFT Case Studies," in IEEE Trans. On VLSI, Vol. 17, No. 4, April 2009, pp. 496-506.

43. A. Varma, M.B. Steer, and P.D. Franzon, "Improving Behavioral IO Buffer Modeling Based on IBIS," in IEEE Trans. Adv. Pack., VOl. 31, No. 4, Nov. 2008, pp. 711-721.



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44. K. Chadrashekar, J. Wilson, E. Erickson, Z. Feng, S. Mick, J Xu, and P.D. Franzon, "Inductively Coupled Connectors and Sockets for Multi-Gbps Pulse Signaling," in IEEE. Trans. Adv. Pack., Vol. 31, No. 4, Nov. 2008, pp. 749-758.

45. A.S. Blum, C.M. Soto, C.D. Wilson, C. Amsinck, P. Franzon, B.R. Ratna, "Electronic Properties of Molecular Memory Circuits on a Nanoscale Scaffold," in IEEE Trans NanoBioscience, 6(4), Dec. 2007, pp. 270-274.

46. S.R. Sonkusale, N.H. DiSpigna, P.D. Franzon, "Uniformity analysis of wafer scale sub-25 nm wide nanowire array nanoimprint mold fabricated by PEDAL process," in Microelectronic Engineering, 84(5-8), May-Aug 2007, pp. 1523-7.

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48. L. Zhang, J.M. Wilson, R. Bashirullah, L. Luo, J. Xu, P.D. Franzon, "Voltage-Mode Driver Pre-emphasis technique for on-chip global buses," in IEEE Trans. VLSI, Vol. 15, No. 2, Feb. 2007, pp. 231-236.

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192. Baribrata Biswas, Allen Glasser, Steven Lipa, Michael Steer, Paul Franzon, Dieter Griffis, Phillip Russell, "Experimental Electrical Characterization of On-Chip Interconnects", *IEEE Topical Meeting on Electrical Performance of Electronic Packaging* , Oct. 1997, pp. 57-59.

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202. P. Franzon, Computer Design Strategy for MCM-D/Flip-Chip Technology, Invited paper, in *Proceedings 1996 ASIC Conference*, Oct. 1996, pp35-39.

203. P. Franzon, System Design Optimization With Multichip Module Technology, Invited Paper, *in Proceedings 1996 Conference of the Brazilian Microelectronics Society*, July 1996.

204. Christoforos Harvatis, Yusuf C. Tekmen, Grif L. Bilbro, Paul D. Franzon, Pin Assignment for High-Performance MCM Systems, in *Proceedings 1996 IEEE ISCAS Conference*. pp. 771-774.

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208. Winick, M. Teague, and P. Franzon, A Micro-machined Approach to Optical Interconnect, *in Proc. 1995 Electronic Components and Technology Conference. pp. 620-627.* Won best student paper award.

209. Sharad Mehrotra, Paul Franzon, Michael Steer, Performance Driven Global Routing and Wiring Rule Generation for High Speed PCBs and MCMs, in *Proceedings 1995 Design Automation Confere*nce, pp. 36-40.

210. Paul Franzon, Andrew Stanaski, Yusuf Tekmen, Sanjeev Banerjia, "System Design Optimization for MCM", in *Proc. 1995 IEEE MultiChip Module Conference*.

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213. S. Mehrotra, P. Franzon and W. Liu, Skew and Delay Minimization of High Speed CMOS Circuits using Stochastic Optimization,*Proc. 1994 Custom Integrated Circuits Conference*, pp. 45-48.

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216. M.S. Basel, M.B. Steer, and P.D. Franzon, "Hierarchical simulation of high speed digital interconnects using a packaging simulator," *Proceedings 44th Electronic Components and Technology Conference*, May 1994.

217. Slobodan Simovich, Sharad Mehrotra, Paul Franzon, Michael Steer, Zaki Rakib and Garrett Simpson, A Signal Integrity Advisor for Automated Packaging Design, in *Proc. 1993 IEEE Topical Meeting on Electrical Performance of Electronic Packaging*, Monterey CA, October 20--22.

218. Todd A. Cook, P.D. Franzon, and Thomas K. Miller III: "LISAS: A Language for Instruction Set Architecture Specification", *Proc. 1993 ICCD Conference*, pp. 552-557.

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220. Paul Franzon, Slobodan Simovich, Sharad Mehrotra, Michael Steer, Macromodels for Generating Signal Integrity and Timing Management Advice for Package Design, in *Proc. IEEE 1993 ECTC Conference*. pp. 523-529.

*221.* Paul Franzon, Slobodan Simovich, Sharad Mehrotra and Michael Steer, Automatic A-Priori Generation of Delay and Noise Macromodels and Wiring Rules for MCMs, *IEEE 1993 MCM Conference.*

222. Slobodan Simovich and Paul Franzon, A simple method for noise tolerance characterization of digital circuits , *Proc. 1993 Great Lakes VLSI Conference*.

223. Todd A. Cook, Ed Harcourt, Thomas K. Miller III, and Paul D. Franzon: Beharvioral modeling of processors from instruction set specifications, to appear in the *Open Verilog International 1993 Conference*.

224. J. Bowen, D. Bahler, and P. Franzon, Design advice systems for concurrent engineering: A constraint-based approach, *NSF Grantees Conference*, Charlotte NC, Jan 93.

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228. Dholakia, T.M. Lee, D.L. Bitzer, M.A. Vouk, L. Wang, and P.D. Franzon, An efficient table-driven decoder for one-half rate convolutional codes, *Proc. 30th ACM SouthEastCon,* pp.116-123.

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230. Paul Franzon, Sharad Mehrotra, Slobodan Simovich, Michael Steer, "Automating Design for Signal Integrity", *Topical Meeting on Electrical Performance of Electronic Packaging*,Tucson, Arizona, April 23, 1991.

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characteristic impedance," *Topical Meeting on Electrical Performance of Electronic Packaging*, Tucson, Arizona, April 23, 1991.

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233. Paul Franzon, Michael Steer, Ronald Gyurcsik, Tools and echniques for the Design of High Speed Multichip Modules *Proc. Japan IEMT*, July, 1991.

234. D. Van den Bout, T. Nagle, T. Miller and P. Franzon, The NCSU Design Center, in *Proc 1991 Microsystems Educators Conference,* July 1991, San Jose CA.

235. P.D Franzon and M.B. Steer, Interconnect Modeling and Simulation for High Speed MCM, in *Proc. Multichip Module Workshop*, March 28th-29th, 1991, pp. 122--129.

236. P. Franzon and Michael Steer: Tools and Techniques for the Design of High Speed Multichip Modules , in *Proc. Third Annual Electronics Packaging Symposium*,May 13 -14, 1991, Binghamton NY.

237. M.S. Basel, M.B. Steer, P.D. Franzon and D. Winkelstein, High Speed Digital System Simulation using Frequency Dependent Transmission Line Network Modeling, *1991 IEEE MTT-S International Microwave Symposium Digest*, June 1991.

238. S.B. Goldberg, M.B. Steer, and P.D. Franzon, Accurate experimental characterization of three-ports , *1991 IEEE MTT-S International Microwave Symposium Digest*, June 1991.

239. S.B. Goldberg, M.B. Steer, and P.D. Franzon, Experimental electrical characterization of high speed interconnects, *41st Electronic Components and Technology Conference*, May 1991.

240. M.B. Steer and P.D. Franzon: Circuit Simulation with Distributed Elements,Workshop on Circuit and Process Simulation, *Microelectronics Center of North Carolina*, Research Triangle Park, Nov. 6, 1990.

241. P. Franzon, et al: CAD Tools for the Automated Design of High Speed Multichip Modules, *Proceedings of the 1990 International Packaging Symposium.*

*242.* M. Lorenzetti, A. Dalal, and P. Franzon: McYield: A CAD Tool for Functional Yield Projections for VLSI, *1990 International Workshop on Defect and Fault Tolerance in VLSI Systems.*

243. P. Franzon, D. VanDenBout J. Paulos, T. Miller III, W. Snyder, T. Nagle, and W. Liu: Defect tolerant implementations for feed-forward and recurrent neural networks,



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*Proceedings of 1990 International Conference on Wafer-Scale Integration,* January 1990, pages 160-166.

244. P. Franzon: Comparison of Reconfiguration Schemes for Defect Tolerant Mesh Arrays, in *Proceedings of the 1989 Workshop on Defect Tolerance*, Tampa Florida, 22 - 24 October, 1989.

245. P.D. Franzon: Yield Modeling for Fault Tolerant VLSI, in the *Proceedings of the International Workshop on Systolic Arrays*, University of Oxford, England, July 1986.

246. P. Franzon and S.K. Tewksbury: `Chip Frame' scheme for reconfigurable mesh-connected arrays , in the *Proceedings of the 1987 International workshop on Wafer Scale Integration*, Uxbridge England, Sept., 1987.

247. L.A. Hornak, S.K. Tewksbury, M. Hatamian, A. Ligtenberg, B. Sugla and P. Franzon: Through-Wafer Optical Interconnects for Multi-Wafer Wafer-Scale Integrated architectures, in the *Proceedings of SPIE 86*, San Diego California, August 1986.

248. P.D. Franzon: Interconnect Strategies for Fault Tolerant 2D VLSI Arrays , in the *Proceedings of the International Conference on Computer Design*, ICCD-86, Rye Town NY, October 1986, pp. 230-234.

249. K.Eshraghian. R.C.Bryant, A.Dickinson, D.S.Fensom, P.D.Franzon,M.T.Pope, J.E.Rockliff, G.Zyner: The Transform and Filter Brick: A new architecture for signal processing, *VLSI 85*, Tokyo Japan, 25-28 August, 1985.

Invited Research Presentations, Conferences

1. Quantum Computing Panel, DesignCon, 2020.
2. Future of 3DIC. Plenary Session, ECTC, 2020.
3. Quantum Computing Panel, ECTC, 2020.
4. Machine Learning Panel, DAC, 2020.
5. P. Franzon, “Candidate Algorithms,” tutorial, EDAPS, Dec. 2019.
6. P. Franzon, “Stress management in heterogeneous integration,” invited talk, IRSP, Nov. 2019.
7. P. Franzon, “Future of 3DIC”, invited talk, 3DIC 2019, October 2019.
8. P. Franzon, “Machine Learning for EDA,” invited talk, ML CAD Workshop, Sept., 2019.
9. P. Franzon, “Securing Machine Learning,” invited talk, IVSW, July 2019.
10. P. Franzon, “Securing Chips with RFID,” invited talk, IVSW, July 2019.
11. P. Franzon, “Circuit Design with Robots,” panel, RFIC 2019, June 2019.
12. P. Franzon, “Securing Machine Learning,” panel, FAME, May 2019.
13. P. Franzon, “Machine Learning for EDA,” panel, DAC ML CAD Workshop, June, 2019.



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14. P. Franzon, “Machine Learning for EDA,” invited presentation, DATE ML CAD Workshop, March, 2019.
15. P. Franzon, “Design Rule Checking with CNNs”, invited presentation, SPIE Litho, Feb. 2019.
16. P. Franzon, “Machine Learning and EDA”, panel, DesignCon, Jan. 2019.
17. P. Franzon, “Surrogate Modeling”, tutorial, DesignCon, Jan. 2019.
18. P. Franzon, “Recurrent Neural Networks”, tutorial, Design Con, Jan. 2019.
19. P. Franzon, “Jitter Management in High Speed SerDes”, tutorial in EDAPS 2018, Dec. 2018.
20. P. Franzon, “2.5D and 3D for Machine Learning,” invited presentation in S3S 2018, Nov. 2018.
21. P. Franzon, “3D Memories”, invited presentation at DATE Memory workshop,March 2018.
22. P. Franzon, “Power Efficient Computing Using 3DIC Technologies,” in International Green Semiconductor Symposium,” Oct. 2017.
23. P. Franzon, “Machine Learning in EDA” in EDAPS 2017, Dec. 2017 (invited)
24. P. Franzon, “Cortical Memories,” in DATE Memory Workshop, March 2017 (invited).
25. P. Franzon, “Machine Learning for next generation EDA,” in EDPS 2017, Sept. 2017 (invited).
26. P. Franzon, “Computing in 3D”, in NASA Workshop on Space Electronics, June 2017.
27. P. Franzon, “Computing in 3D,” in EDTM 2017, March 2017.
28. P. Franzon, et.al. “Machine Learning and Electronic Design,” in 2016 EPEPS, October, 2016. (invited).
29. P. Franzon, “Interconnect Solutions Through Codesign,” in Semicon West, July 2016. (invited)
30. P. Franzon, “Interconnect Solutions Through Codesign,” in ASME, June 2016. (invited)
31. P. Franzon, “Cortical Memories,” in DATE Memory Workshop, March 2016 (invited).
32. P. D. Franzon *et al.*, "Computing in 3D," *3D Systems Integration Conference (3DIC), 2015 International*, Sendai, 2015, pp. TS6.1.1-TS6.1.2 (invited)
33. P. Franzon *et al.*, "Computing in 3D," *Custom Integrated Circuits Conference (CICC), 2015 IEEE*, San Jose, CA, 2015, pp. 1-6. (invited)
34. P. Franzon, et.al. “Computing in 3D”, EDSSC, Singapore, June 2015 (invited)
35. Franzon, P.D.; Rotenberg, E.; Tuck, J.; Davis, W.R.; Huiyang Zhou; Schabel, J.; Zhang, Z.; Park, J.; Dwiel, B.; Forbes, E.; Joonmoo Huh; Priyadarshi, S.; Lipa, S.; Thorolfsson, T., “Computing in 3D”, EDAPS 2014, Bangalore, India, Dec. 2014. (Invited presentation).
36. Franzon, P.D.; Rotenberg, E.; Tuck, J.; Davis, W.R.; Huiyang Zhou; Schabel, J.; Zhang, Z.; Park, J.; Dwiel, B.; Forbes, E.; Joonmoo Huh; Priyadarshi, S.; Lipa, S.; Thorolfsson, T., “Computing in 3D”, ICSJ 2014, Kyoto, Japan, Nov. 2014. (Invited presentation).



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37. Franzon, P.D.; Rotenberg, E.; Tuck, J.; Davis, W.R.; Huiyang Zhou; Schabel, J.; Zhang, Z.; Park, J.; Dwiel, B.; Forbes, E.; Joonmoo Huh; Priyadarshi, S.; Lipa, S.; Thorolfsson, T., "Computing in 3D", IME Workship 2014, Singapore, Aug. 2014. (Invited presentation).
38. Franzon, P.D.; Rotenberg, E.; Tuck, J.; Davis, W.R.; Huiyang Zhou; Schabel, J.; Zhang, Z.; Park, J.; Dwiel, B.; Forbes, E.; Joonmoo Huh; Priyadarshi, S.; Lipa, S.; Thorolfsson, T., "Computing in 3D", SLIP 2014, San Francisco, CA< June. 2014. (Invited presentation).
39. Franzon, P.D.; Rotenberg, E.; Tuck, J.; Davis, W.R.; Huiyang Zhou; Schabel, J.; Zhang, Z.; Park, J.; Dwiel, B.; Forbes, E.; Joonmoo Huh; Priyadarshi, S.; Lipa, S.; Thorolfsson, T., "Computing in 3D", SPI 2014, Ghent, Belgium, May 2014. (Invited presentation).
40. Franzon, P.D "3D Design, Test and CAD", SPI 2014, DesignCon, Santa Clara, CA, Jan. 2014. (Invited presentation).
41. P. Franzon, P. Gadfort, W. Zhao, "AC powered circuits," S3S, San Francisco, California, Oct. 2014. (Invited presentation).
42. Franzon, P.D.; Rotenberg, E.; Tuck, J.; Davis, W.R.; Huiyang Zhou; Schabel, J.; Zhang, Z.; Park, J.; Dwiel, B.; Forbes, E.; Joonmoo Huh; Priyadarshi, S.; Lipa, S.; Thorolfsson, T., "Applications and design styles for 3DIC," *Electron Devices Meeting (IEDM), 2013 IEEE International* , vol., no., pp.29.4.1,29.4.4, 9-11 Dec. 2013 (invited paper)
43. Franzon, P.; Bar-Cohen, A., "Thermal requirements in future 3D processors," *3D Systems Integration Conference (3DIC), 2013 IEEE International* , vol., no., pp.1,6, 2-4 Oct. 2013 (Invited Paper)
44. Franzon, P.D., "MOOCs, OOCs, flips and hybrids: The new world of higher education," *Microelectronic Systems Education (MSE), 2013 IEEE International Conference on* , vol., no., pp.13,13, 2-3 June 2013 (Invited Paper)
45. Franzon, P.D.; Priyadarshi, S.; Lipa, S.; Davis, W.R.; Thorolfsson, T., "Exploring early design tradeoffs in 3DIC," *Circuits and Systems (ISCAS), 2013 IEEE International Symposium on* , vol., no., pp.545,549, 19-23 May 2013 (invited paper)
46. Keynote, "3D System Design: Present and Future," IEEE 3DIC Test Workshop, Anaheim CA, Dec. 2012
47. Invited Paper, "3D Specific Systems", NY packaging society, GE, Albany, NY, Oct. 2012.
48. Invited Paper, "Design of 3D Specific Systems," D43D, Lausanne, Switzerland, July 2012.
49. Keynote, "Design of 3D Specific Systems: Prospectives and Interface Requirements," IEEE NOC Conference, Copenhagen, Denmark, May 2012.
50. Keynote, "Design of 3D Specific Systems: Prospectives and Interface Requirements," IEEE NOC Conference, Chipex, Tel Aviv, Isreal, May 2012.
51. Keynote, "Design of 3D Specific Systems," DATE 3DIC Workshop, Dresden, Germany, March 2012.
52. Invited Paper, "Coordinating 3D Designs," IEEE 3DIC Conference, Osaka Japan, January 2011.
53. Invited Paper, "3D Specific Design and Test" ATS 2011, New Delhi, India, Nov. 2011.



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54. Invited Paper, "3D Specific Design," IEEE SAMOS Conference, Samos, Greece, August 2011.
55. Keynote, "3D TSV Processes and Design Challenges," ICMAT, Singapore, June 2011
56. "Computing with Novel Floating Gate Devices," CMOS-ET, Whistler Canada, June 2011
57. Keynote "3DIC, Which Flavor for You?", TIPPS, Chicago IL, June 2011
58. "Design of 3D Specific Systems," NYU-AD 3DIC Workshop, April, 2011
59. "Design of 3D Specific Systems", IMAPS 2010, Raleigh, NC, November, 2010
60. "Creating 3D Specific Systems," DATE 2010, Dresden Germany, March, 2010.
61. "3D Design and Applications," IEEE Litho 2009, June 2009.
62. "Creating 3D Specific Systems," D43D, Grenoble France, June 2009.
63. "3DIC Design and CAD," Austin Chapter Meeting on 3DIC, April 2009.
64. "Application and Design Exploration for 3D Integrated Circuits," VLSI Multi-level Interconnect Conference, September 2008.
65. "Memory rich applicatons for 3D integration," in Proc SPIE 7268, Smart Structures, Devices and Systems IV, Dec. 2008.
66. "Green Electronics, Fact or Myth", panel member, IEEE SOC Conference, September 2008.
67. "Application and Design Exploration for 3D Integrated Circuits," VLSI Multi-level Interconnect Conference, September 2008.
68. "Design and CAD for 3D Integrated Circuits", IEEE/ACM Design Automation Conference, June 2008.
69. "Keeping Chips Hot, Are IC Thermal Problems Hot Air", panel member, IEEE/ACM Design Automation Conference, June 2008.
70. "Application and Design Exploration for 3D Integrated Circuits," VLSI Multi-level Interconnect Conference, September 2007
71. "3DIC", Materials Research Conference, Dec. 2007
72. **"**Molecular Computing," 2nd IEEE International Workshop on advances in sensors and interfaces, June 2007.
73. "TCAM core design in 3D IC for low matchline capacitance and low power," Proc. SPIE Smart Structures, Devices and Systems III, December, 2007.
74. "3-D Design," Fall MRS Conference, December 2007.
75. "3-D Design," RTI 3D Technologies Conference, November, 2007.
76. "Controlled nanowire fabrication by PEDAL process," IEEE NanoNet '06, Sept. 2006,
77. "An integrated self-masking technique for providing low-loss metallized RF MEMS devices in a polysilicon only MEMS process," SPIE Euro Micro Conference, May 2005
78. "Simultaneous switching noise in IBIS models," IEEE EMC, August 2004
79. "Nanoscale Circuits and Computing Systems," ISCAS, May 2004
80. "Integration for Molecular Electronics," FNANO, April 2004
81. "High Frequency, High Density Interconnect Using AC Coupling," MRS Fall Meeting, December 2003
82. AC Coupled Interconnect for High-Density High-Bandwidth Packaging," SPIE Australia Micro Conference, December 2003



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83. "High Frequency, High Density Interconnect Using AC Coupling," SSDM Japan, September, 2003
84. "Scalable Molecular Circuit Architectures," Molecular Electronics Conference, Decemeber 2002
85. "4 Gbps AC Coupled Interconnection," IEEE CICC, May 2002
86. "Design Automation and Design Challenges for Package/Systems,"Asia DAC, January 1999
87. "Integrated Package Design of a DES Processor," IMAPS MCM Conference, Oquinqit Maine, August 1997.
88. "Computer Design Strategy for MCM-D/Flip-Chip Technology," IEEE ASIC, Sept. 1996.
89. "System Design Optimization With Multichip Module Technology," Brazil Microelectronics Conference, Aug. 1996.
90. "Optimal System Design with MultiChip Module Technology," Microelectronics 1995, June 1995.

Invited Research Presentations, Universities and Industry

1. "3DIC Design and Floorplanning", Qualcomm, Dec. 2020.
2. "Chips for AI," Rambus, June 2020.
3. "Intersecting Machine Learning and EDA," Apple, Sept. 2019.
4. "Intersecting Machine Learning and EDA," Cisco, Sept. 2019.
5. "Intersecting Machine Learning and EDA," BAE, August 2019.
6. "Intersecting Machine Learning and EDA," Cadence, Jan. 2019.
7. "Machine Learning and EDA," Global Foundires July 2018.
8. "3D Processors", Cirrus Logic, June 2018.
9. "H3: A heterogeneous 3DIC Multiporcessor," Intel, December, 2017
10. "Machine Learning and EDA," Draper Labs, Sept. 2017.
11. "Cortical Processors," IBM, Sept. 2017.
12. "Machine Learning in EDA", Cadence Users Group Meeting, April 2017.
13. "Machine Learning and EDA," Cadence, June 2017.
14. "Machine Learning and EDA", Cirrus, May 2017,
15. "Cortical Processors," Northrop Grumman, Jan 2016.
16. "Computing in 3D", IMEC, May 2016.
17. "Cortical Processors," Cirrus, June 2016.
18. "Machine Learning and EDA,", Synopsys, Nov. 2016.
19. "Mcahine Learning and EDA," Xilinx, Nov. 2016.
20. "Computing in 3D", Google, Oct. 2014.
21. "Computing in 3D", Cirrus Logic, Aug. 2014.
22. "Computing in 3D", Sandia Labs, May 2014.
23. "3D Specific Design", Rambus, Sept. 2013
24. "3D Specific Design," University of Maryland, Dec. 2013
25. "3D Specific Design," Georgia Tech, May 2013.
26. "3D Specific Design", IBM, Jan. 2013.
27. "Connectivity in Future Systems," HP, October, 2012.
28. "3D Specific Design and CAD," IEEE CPMT Chapter, Portland OR, April 2012.
29. "Connectivity in Future Systems," IBM, March 2012.
30. "Sensors and System," IBM, April 2012.



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31. "3D Specific Systems," Technicon, April 2012.
32. **"**3D Speicifc Design," Mentor Graphics, Nov. 2011.
33. "3D Specific Design", Ga. Tech, June 2011.
34. "3D Specific Desgn and CAD," IBM, January 2011.
35. "Creating 3D Specific Systems," CMOS ET Conference, May 2010.
36. "3DIC CAD," Synopsys, April 2010.
37. "Designing 3D Specific Systems," LSI Logic, March 2010.
38. "3DIC Design and CAD," IMEC, March 2010.
39. "Creating 3D Specific Systems", IBM, March 2010.
40. "Creating 3D Specific Systems," RTI 3D, December, 2009.
41. "3D Memory Systems," SRC Signapore, October 2009.
42. "3DIC Design and Applications," IMEC, June 2009.
43. "3DIC Technology Design and Applications," Tessera, April 2009.
44. "3DIC Technology Design and Applications," Ultratech, January 2009.
45. "3DIC Design and CAD," University of Adelaide, December, 2009.
46. "3DIC Design", Qualcomm, September 2008.
47. "AC Coupled Interconncect", DARPA Exascale Committee, August 2007.
48. "3DIC Design and CAD", TI, March 2008
49. "3DIC Design and CAD," IBM, April 2008
50. "AC Coupled Channels", IBM, April 2008
51. "AC Coupled Interconnect", HP, Sept. 2007
52. "3DIC", CEA-LETI, June, 2008
53. "Interconnect", McGill University, Canada, July 2007.
54. "AC Coupled Interconnect," Intel, AZ, March 2006.
55. "AC Coupled Interconnect", Rambus CA, December 2005
56. "AC Coupled Interconnect," IBM, NY, December 2005
57. "Equalization for on-chip interconnect," IBM, NY, December 2005.
58. "AC Coupled Interconnect," University of Adelaide, October, 2005.
59. "Molecular Electronics," University of Sydney, October, 2005.
60. "AC Coupled Ineterconnect," UFL, April 2005
61. "Molecular Computing," UNCC, March 2005
62. "Nanoscale structures for Molecular Electronics," HP Labs, December 2004
63. "AC Coupled Interconnect," SRC Econfernce, Dec, 2004
64. "AC Coupled Interconnect," Rambus CA, December 2004
65. "AC Coupled Interconnect," Sun, CA, December 2004
66. "AC Coupled Interconnect," IBM RTP, February 2005
67. "AC Coupled Interconenct," Rambus NC, August 2004
68. "Emerging Memory Devices," ITRS, Stresa Italy, April 2004
69. "Optical Networking," ECU, Perth Australia, August 2003
70. "Molecular Electronics," University of Adelaide, August 2003
71. "Molecular Electronics," University of Sydney, August 2003
72. "AC Coupled Interconnect," IBM TX, May 2003
73. "Scalable Molecular Circuit Architectures," USC, April 2003
74. "Molecular Electronic Circuits," KAIST, Korea, July 2002
75. "AC Coupled Interconnect," IBM Research NY, April 2002
76. "AC Coupled Interconnect," Intel AZ, Feb. 2002



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77. "AC Coupled Interconnect," Intel OR, Feb. Nov 2001
78. "Structures and CAD for Chip-Package Codesign," TI TX, May 2000
79. "High Bandwidth On-Chip Interconnect," TI Dallas TX, May 2000
80. "Heteregenous System Integration," TI, Dallas TX, May 2000
81. "MEMS Application and Fabrication," Ford Microlectronics, CO, Dec. 1998
82. "Chip Package Codesign," Ga Tech, Oct, 1998
83. "Chip-Package Codesign," SRC, NC, April 1997
84. "Chip-Package Codesign," Intel, CA, Oct 1997
85. "Chip-Package Codesign," DEC, MA, Dec 1997
86. "Optimal Computer Design with MCM-D/Flip Chip Technology," Sun, CA, May 1996
87. "Signal Integrity Tools," Sun, CA, May 1996

I have aslso given invited presentations at the following organizations: Stanford University, University of Adelaide, Silicon Graphics, Intel, Ross Technology, Cadence, Mentor Graphics, LSI Technology, Tandem Computer, IBM,Bell Northern Research, MCNC. Dates and exact titles unrecorded.

Appointments or election to study sections and editorial boards.

- Associate Editor, IEEE Transactions on Advanced Pcakaging 1997-
- Associate Editor, ACM Journal on Emerging Computing Technologies, 2004-2011
- Editorial Board, Journal of Microelectronics System Integration.
- Associate Editor, IEEE Transactions on VLSI Systems. 1997 – 2001

## B. GRANTS AND CONTRACTS

**Total Funding Summary.**

80 Research grants and contracts, 1 equipment grant, 1 educational grant, more than 10 cash gifts, over $80 Million in research grants, and $500,000 in educational grants, and over $700,000 in gifts

EXTERNAL GRANT

1. P. Franzon, "Generative Adversarial Network generated models for Signal Integrity, Thermal Modeling, Etc., Center for Advanced Electronics through Machine Learning (CAEML) Core Project 5A3", CAEML IUCRC (UIUC), $59, 876, 8/1/21 – 07/31/22

2. P. Franzon, "Cirrus Logic Mixed Signal IC Design Fellowship," $80,00, 08/15/20 – 8/14/22.

3. P. Franzon, "Field Programmable Gate Arrays Hardware Accelerator for Real Time Security, Center for Advanced Electronics Machine Learning Core Project", $113,594, 1/1/20 – 7/31/22



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4. P. Franzon, "Three Dimensional Study of the Benefits of Hybrid Bonding," Xper, $163,392, 08/16/19 – 05/15/20 (PI).

Investigate 3DIC design styles.

5. A. Aysu and P. Franzon, "Differential Power Analysis of Deep Neural Networks with Mitigation at the Architecutre Level, SRC, 10/1/19 – 09/30/20, $58,000 (co-PI).

6. P. Franzon, A. Aysu, "FPGA Accelerator Hardware for Real Time Security," CAEML, 1/1/20 – 12/31/21, $100,000. (PI)

Detecting ransomware attacks suing FPGAs.

7. D. Baron, P. Franzon, "High dimensional structural inference for non-linear, deep markov of state base models, CAEML, 1/1/19 – 12/31/19, $54,000. (co-PI).

Investigate deep space ML techniques.

8. P. Franzon, "Agile 3D Memory Interfaces," AFRL, $15,0575, 08/27/15 – 08/26/18, PI

Design interfaces for 3D memories.

9. W. Davis, P. Franzon, "Fast Accurate Power Performance Area Model-Extraction," CAEML, 01/01/19 – 12/31/20, $108,000 (co-PI)

Build models for power/performance tradeoff evaluation.

10. P. Franzon, "Radition Effect in 3D Structures", DTRA via Venderbilt, 10/11/17 – 10/10/22, $705,469 (PI)

Investigate effects of space radiation on 3D elecrtonics.

11. P. Franzon, J. Tuck, "2.5D Extendible Processor,", DARPA/ONR, $3,206,856, 09/30/2017 – 09/30/2021

Build and demosntrated an extendible processor with machine learning chiplets.

12. P. Franzon, "Trusted Fabrication through 3D Integration Demonstration," DARPA/ONR, 09/30/2017 – 04/28/2021, $1,999,504. (PI)

Demonstrate trusted fabrication through a design experiment.

13. W. Davis, P. Franzon, "Applying Machine Learning to Back End IC Design," CAEML, $108,000 1/1/17 – 12/31/20. (co-PI)



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Develop automated back end flows using machine learning.

14. P. Franzon, "Research Site for I/UCRC Center for Advanced Electronics Through Machine Learning (CAEML)", NSF, 08/01/2016 – 07/31/2021, $300,000, (PI).

The mission of CAEML is to achieve better electronic design through machine learning.

15. P. Franzon, "Behaviroal Modeling for High Speed Links," CAEML I/UCRC, 01/01/2017 – 08/15/2019, $82,000, (PI).

Using machine learning to build better models for high speed links.

16. W. Davis, P. Franzon, "Design Rule Checking with Deep Networks," CAEML I/UCRC, 01/01/2017 – 12/31/2017, $60,000, (co-PI).

Applying machine learning to physical design.

17. B.A. Floyd, P. Franzon, "Intellectual Property Reused through Machine Learning," $100,000, 01/01/2017 – 08/15/2019. (co-PI).

Applying machine learning to custom circuit IP reuse.

18. P. Franzon, "Planning Grant for I/UCRC for Advanced Electronics Through Machine Learning," NSF, 04/15/15 – 03/31/16, $11,499

Planning grant for potential I/UCRC.

19. P. Franzon, "Trusted Fabrication through 3D Integration," DARPA/ONR, 08/01/2015 – 05/15/2017

Study on new techniques to effect trusted ICs.

20. P. Franzon, "Cognitive Computing," Google, $41,000, 3/1/2015 – 2/28/2016.

Investigate speedup potential of cognitively inspired algorithms.

21. P. Franzon, "Hardware acceleration of sparse cognitive algorithms," DARPA/AFRL, $320,372, 12/01/14 – 6/30/16.

Investigate speedup potential of new classes of cognitively inspried algorithms.

22. P. Franzon, "SHF:Small AC Powered Digital Circuits," NSF, 08/01/14 – 07/31/20, $445,713, (PI).

Design a new class of efficient RFID and backscatter BTLE chips.



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23. P. Franzon, A. Chakrabortty, "Faster than Real Time Simulation of Electromechanical Process of Large Scale Electrical Power Grid", $80,000, ABB, 12/15/14 – 8/15/16. (PI)

Architect an accelerator to simulate power grids.

24. P. Franzon, W. Davis, "Leveraging Commercial Flows for Heterogeneous Integration,", $1,505,643, DARPA, 5/16/2013 – 2/28/2017. (PI)

Produce CAD flows for managing temperature and stress in Heterogeneous 3DIC chip stacks.

25. P.Franzon, E. Rotenberg, W. Davis, H. Zhou, J. Tuck, "3D-Enabled Customized Embedded Computer," $1.1M, DARPA, 9/14/2011 – 9/14/2016. (PI)

Architectect, design and implement a 3D CPU capable of low power computing.

26. P. Franzon W. Davis, E. Rotenberg, "Modular, Testable, Tightly Coupled 3D Implementation of a Heterogeneous Processor", $1,200,000, Intel, 10/1/2011 – 12/10/2017. (PI)

Build novel architectural approaches to implementing 3D specific processors.

27. P. Franzon, Eric Rotenberg, "3D X86 Heterogeneous Core Stack," $55,000, Intel 11/12/2012 – 12/31/2013.

Investigate an X86 based CPU stack.

28. P. Franzon, NSF ASSIST ERC – portion to my projects, NSF, $150,000, 07/01/2011 – 12/31/2013.

System Thrust Leader for ASSIST ERC.

29. P. Franzon, V. Misra, and N.H. DiSpigna, "Computing via Monotlithic Three Dimensional Assemnbly of Novel Floating Gate Transistors," $839,740, NSF, 7/1/2011 – 6/30/2016 (PI)

We have developed the design for a new type of "unified" memory device, a Double Floating Gate FET (DGF FET). It can store two bits in each transistor, one in a volatile state, another in a non-volatile state. The purpose of this grant is to build sample devices and address practical issues related to implementation as a memory device.

30. P. Franzon, "Binary Multimode Interconnect for High Density Chip to Chip Communications," Intel, $300,000 7/1/2011 – 12/31/2014 (PI)



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A new implementaiton method has been identified for a high-density, low-power, crostalk cancelling chip to chip communications scheme. This paper addresses demonstration of this method.

31. P. Franzon, W.Davis, "Thermal-System Codesign of a Mobile Application," Qualcomm, $150,000, 07/01/2011 – 12/31/2014. (PI)

Investigate pathfinding for 3D systems.

32. P. Franzon, "EAP actuators for a Braille Display," PBI Inc., $30,000, 8/16/2012 – 12/31/2012.

Prototype a Braille cell based on EAPs.

33. **P**.Franzon, "Integrated 3D Packaging for Microscopic Systems," MARCO, $321,000, 11/01/2009 – 1/31/2013. (PI)

Develop integrated packaging concepts and antenna for 1 mm and 1 cm scale systems.

34. P. Franzon, "Speech Recognition Acceleration," Spansion, $123,761, 07/12/2010 – 05/15/2012.

Investigate hardware/software codesign for speech acceleration.

35. P. Franzon, N. DiSpigna, "Nanocrystal Computing," NSF (CCF-0811582), $400,000 07/01/2008 – 06/30/2012. (PI)

Develop new devices, based on nanocrystal films, suited for digital applications. Explore those applications.

36. P. Franzon, "Algorithms and Structures for Self Healing Circuits," $170,000, DARPA, 01/03/2012 – 12/31/2013. (PI)

Investigate CAD techniques for self-calibration of RF circuits

37. P. Franzon, "CAD Support for Tezzaron MPW," DARPA as a subcontract through Tezzaron, $50,000, 7/1/2009 – 6/30/2010.

Support commercial tools as used in Tezzaron MPW run.

38. P. Franzon, M. Steer, T. Kelley, M. Chow, F. Wu, "Self Healing Circuits," DARPA as a subcontract through Raytheon, $1,073,341, 4/1/2009 – 06/30/2013. (PI)

Investigate CAD techniques for self-calibration of RF circuits.



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39. P. Franzon, M. Ozturk, "Reconfigurable RF Electronics," AFRL, as a subcontract through Raytheon, $60,000, 5/1/2009 – 5/30/2010. (PI)

Design and model a new high-performance Varactor.

40. W.R. Davis, Paul D. Franzon, "Architectural Evaluator for Three Dimensional Integrated Circuits," Semiconductor Research Corporation, $240,000, 7/1/2008 – 6/30/2012. (Co-PI).

Establish CAD tools to help architect 3D Circuits.

41. Paul D. Franzon, W.R. Davis, "CAD Support For the Third MIT-LL 3D-Integrated Circuit Run", $53,375, DARPA, 5/1/2008 – 12/31/2008. NCSU PI. Subcontract through MIT-LL. (PI)

Develop 3D PDK to support third fabrication run.

42. W.R. Davis, P.D. Franzon, "FreePDK: An Open-Source, Variation-Aware Design Kit", CMU as a subcontract to MARCO, $42,338, 9/1/2007 – 8/31/2009. CoPI.

This work will create an open-source, variation-aware 45nm PDK (Process Design Kit) for use in VLSI education and small-businesses. This kit will include the necessary layout design-rules and extraction command-decks to capture layout-dependent systematic variation and perform statistical circuit analysis. The kit will also include a standard-cell library and I/O-pad library with the necessary support files to enable full-chip place & route and verification for System on Chip designs. Test-chips designed with this PDK will be fabricated by an SRC member company, allowing validation of the design-rules so that the rules may be used in future multi-project runs and design contests

43. Paul D. Franzon, "Micromachined Braille Reader", US Department of Education, 11/01/2007 – 10/31/2010, $600,000. PI.

Investigate and build a "full screen" programmable Braille display using ElectroActive Polymers (EAPs).

44. Paul D. Franzon, "Computer Aided Design for Digital Trust", $110,000, DARPA, 1/1/2007 – 06/30/2009. NCSU PI, subcontract to Irvine Sensors Corporation.

Investigate methods to identify theft and modification of chip intellectual property.

45. Paul D. Franzon, "Multimode Interconnect," Semiconductor Research Corporation, 11/01/06 – 12/31/10, $300,000. PI.

With higher core clock speeds, and the trend to multi-core, the demands on chip I/O are increasing rapidly. The key question is how to increase both the density and speed of chip I/O without increasing packaging costs. At high speeds, crosstalk issues typically dictate



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inter-pair spacings of four times the wire width in PCBs, and rich use of power and ground shields in connectors. In this research, we will investigate coding and circuit techniques that enable a group of signals to travel down a wire bundle, and potentially connectors and cable assemblies, without crosstalk

**46.** Franzon, Kingon, Wilson, "System Technologies for Space Electronics," AFRL, 09/25/2006 – 6/30/2011, $1,287,807. PI.

Build interconnect technologies for Space Applications. Deploy a demonstrator in a satellite.

47. K.P. Sandeep, Paul D. Franzon, J. Simunovic, "Use of RFID Tags in Determining the Time-Temperature History Within a Product During Processing, Transportation, and Storage," CAPPS, $60,000, 11/01/06 – 12/31/07. and 5/1/06-4/30/10 Co-PI.

Improving food quality, enhancing food safety, and aiding process filing with the FDA are three important areas of interest to the food industry. Accurate determination of the time-temperature history at the critical point in a system (slowest heating point) is necessary to accomplish this. We would like to make use of the RFID technology to capture and transmit internal temperatures of food particulates while they are being pumped through the heating, holding, and cooling sections of a continuous flow food processing system.

48. K.P Sandeep, Paul D. Franzon, Josip Simunovic, "Development and Use of Sensors in Validating Aseptic Processing of Multiphase Foods," US. Dept. of Agriculture, 09/01/06 – 08/31/10. $278,936. Co-PI.

The overall objective of the current study is to develop a sensor that can be used to determine the location and internal temperature of food particles as they flow through the heating, holding, and cooling sections of an aseptic processing system.

49. Franzon, "System Technologies for Low-Power Spaceborne Electronics," AFRL, $1,287,807, 9/25/06 – 9/24/07, NCSU PI.

Demonstrate a complete AC Coupled first level packaging solution in both Bulk CMOS and SOI. Launch a space demonstration vehicle.

50. K.P. Sandeep, Paul Franzon, Josip Simunovic, "Development of a Micro-Electro-Mechanical-System-based (MEMS) temperature sensor to determine internal temperatures within multiphase food products", CAPPS, $54,422, 7/1/06-12/31/11.

In collaboration with Food Science, develop miniaturized sensors for monitoring internal conditions in Food Processing Equipment.

51. Franzon, "MoleFET Design and Fabrication," DARPA, $150,000, 5/11/06 – 11/10/08. (PI at NCSU, subcontract to UVA.)



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Investigate molecular integration into FET structures for nanoflash and transistor applications.

52. Steer, Franzon, Davis, "Electromagnetic Modeling for 3D ICs," DARPA, $1,870,000, 7/5/04 – 3/31/10, (co-PI, subcontract through PTC).

Tools and Application Exploration for 3D ICs.

53. Franzon, "DNA Directed Circuit Assembly," NSF, $135,000 7/1/03 – 6/30/07. (PI at NCSU)

    In collaboration with Duke University, determine circuit interconnect strategies using DNA scaffolds.

54. Franzon, "High Performance Computer Interconnect," NSF, $350,000, 9/01/2002 – 8/31/2008, (PI).

    We are determining new approaches to interconnect large systems at the system level. These approaches promise high density, low power and low cost.

55. Franzon, "AC Coupled Interconnect for Low-Power Space-Borne Electronics," Mission Research Corporation, $3,116,813, 05/16/03 – 09/30/06. (PI).

    Demonstrate a complete AC Coupled first level packaging solution in both Bulk CMOS and SOI. MCNC is a sub-contractor performing the solder bump and package fabrication investigation.

56. Steer, Franzon, Kingon, "Mixed Signal Interposer," $475,000, DARPA, 6/19/02 – 6/18/06. (co-PI, subcontract from Purdue University).

57. Franzon, "Hybrid Defense Mechanisms for Network Security," MDA, $30,000, 8/22/05 – 2/22/06 (PI at NCSU, subcontract from Irvine Sensors).

In collaboration with Irvine Sensors, implement new hardware algorithms for Intrusion Detection for high performance networks.

58. Franzon, "System Packaging for AC Coupled Interconnect," DARPA, $501,550, 7/1/04 – 9/30/09. (PI at NCSU, Subcontract from Irvine Sensors Corporation).

In collaboration with Irvine Sensors, design and build a 3D Module incorporating multiple FPGAs and memories, capable of high performance DSP.

59. Franzon, "Molecular Computing Technology," DARPA,$62,293, 8/1/04 – 7/31/05,(PI at NCSU, subctrontract from Rice University).



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In collaboration with Rice University, build and demonstrate new technologies for Molecular Computing.

60. Franzon, "AC Coupled Interconnect Demonstration," SRC, 07/01/03 – 06/30/06, $300,000. (PI)

    Determine design rules for AC Coupled Interconnect Systems.

61. Franzon and Conte, "TRIPS SystemC/En-morph mode specification and Implementation", DARPA, 05/16/03-03/15/05, $275,000 (PI).

    Investigate the implementation of programmable network processors using reconfigurable computing concepts. Aim at achieving configurable line rate (10 Gbps) solutions for network security, routing, and difserv.

62. Steer and Franzon, "Advanced Modeling of Mixed-Signal Systems" Agency: DARPA 08/01/01 to 07/31/04, $1,665,235. (co-PI). (See Steer's PA2 for description).

63. Steer, Kingon, and Franzon, Mixed-Signal Interposer Design and Fabrication (as subcontract to Purdue University), $1,070,000, 1 May 2002–30 April 2005., (co-PI). (See Steer's PA2 for description).

64. Franzon, "Molecular Interconnect Studies" Mission Research Corp. to DARPA 07/11/2001 to 07/10/05, $533,123 (PI).

    Work within a Naval Research Labs-lead team to develop solutions for build nanoscale molecular memories using viruses as an interconnect scaffold. Perform circuit studies, and characterization experiments.

65. Franzon, "Molecular Circuits II" DARPA, 03/21/01 - 03/31/05 $500,000 (PI).

    Work within the Rice-lead team to determine circuit architectures suited for molecular memories.

66. Franzon and Cangelleris, "Inductance Control for On-Chip Signal Integrity" NSF 08/01/00 to 07/31/05, $420,000 (PI).

    Determine practical techniques to reduce the impact of on-chip inductance on circuit performance and design time.

67. Franzon, Liu and Hughes, "SOI Deep Space Radio" NASA (sub thru A&T), 03/12/01 to 05/30/05, $771,080 (PI).

    Investigate novel circuit structures for use in an ultra-low power deep space VHF radio communications system.



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68. Franzon and Liu, "AC Coupled Interconnect", SRC, 09/01/99 to 08/16/03 $321,166 (PI).

    Determine design rules and approaches for using capacitively and inductively coupled interconnect structures for between-chip communications.

69. Franzon, "Network Processor Design for Just in Time Optical Networking Protocols," ARDA, 10/01/01 to 03/28/03, $189,034 (PI).

    Implement a network processor for a future optical backbone protocols using Just-In-Time (JIT) Optical Burst Switching concepts. Work with MCNC to get a small JIT network up and running. Develop new hardware algorithms for critical bottlenecks, particularly the Forwarding Engine.

70. P.D. Franzon, A. Kingon, E. Grant, “Planar Processed Robots", DARPA, 6/28/98 - 6/2/02, $1,274,527.

71. R. Hodges, et.al. and P. Franzon, “Applications of MEMS to textiles" National Textiles Foundation, 4/15/00 - 4/14/01, ECE share: $35,000.

72. P. Franzon, and W. Lui, “AC Coupled Interconnect,"10/1/99 - 9/30/02, Semiconductor Research Corporation, $321,166.

73. P. Franzon, “VLSI Approaches to Chip-Package Codesign," 1/1/00 - 6/30/00, Semiconductor Research Corporation Exploratory Grant, $25,000.

74. P. Franzon, “Molecular Circuits," 2/1/00 - 1/31/01, DARPA, $53,015.

75. P.D. Franzon, T. Conte, “SHOCC Demonstrator Study," 7/1/99 - 5/26/00, Northrop Grumman, $128,857.

76. P.D. Franzon, MEMS-based Diffractive Beam Steerer, STTR Phase 2 under sub-contract to NIPT from the USAF, Jan 1, 1998 -- June 30, 2000, ($170,000).

77. P. Franzon, W. Liu, M. Steer, Low-Power, High-Performance MEMS-based Switch Fabric, Oct. 1, 1996--Sept. 30, 1999, DARPA, ($1,047,658).

78. P. Franzon, T. Conte, W. Liu, Three Dimensional High Density Electronic Module Design and Manufacturing, Jan. 1, 1997--Dec 31., 1998, From MCMC under sub-contract from DARPA, ($257,285).

79. P. Franzon, MEMS-based Diffractive Beam Steerer, STTR under sub-contract to NIPT from the USAF, Sept. 14, 1996-- Sept. 13, 1997, ($35,000).



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80. M. Steer, P. Russel, P. Franzon, “Experimental Determination of On-Chip nterconnect Capacitances", January 1, 1995 to October 31, 1995, warded by Sematech ($127,341).

81. G. Bilbro, P. Franzon, “Performance Driven System Design", awarded by Intel Corporation ($35,000 per year).

82. P. Franzon, G. Bilbro, M. Steer, “Methodology, Tools and Demonstration of MCM System Optimzition", November 1, 1993 to April 30, 1997,awarded by ARPA ($675,440).

83. P. Franzon, NSF Young Investigators Award, October 1993--March, 2000, ($285,000).

84. J. Bahler, J. Bowen, P. Franzon, “A Generic Architecture for Intelligent Networked Colocation in Concurrent Engineering" (with specific application to early system decision making vis electonic packaging), October 1, 1992 to March 31, 1996, awarded by NSF ($599,986).

85. P. Franzon, “P2E Transformation Engine for the Generation of Wiring Rules for Signal Integrity and Timing Management", May 1, 1992 to April 30, 1993, Cadence Design Systems ($35,009).

86. W. Alexander, P. Franzon, W. Liu, M. Steer, “Equipment for building and testing very high speed digital systems", awarded by NSF ($250,000).

87. P. Franzon, M. Steer, “Interconnect models for computer aided design of high speed, multichip modules and integrated circuits", 15 February, 1991 to 30 June, 1993, awarded by NSF ($273,466).

88. P. Franzon, A. Kelley, “New Approaches to Low Energy Computing", 28 February to 31 December, 1991, awarded by IBM ($29,994).

89. J. Bowen, J. Bahler, P. Franzon, “Design for Testability, Part II", 1 January, 1991 to 31 December, 1991, awarded by Integrated Manufacturing Systems Engineering Institute ($19,000).

90. H.T. Nagle, D. Van Den Bout, T. Miller, P. Franzon, “Design Center for Teaching Digital Design", 1 September, 1990 -- 31 August, 1993, awarded by NSF ($500,000).

91. P. Franzon, “Evaluation of CAD tools for teaching", MCNC, 1 January, 1991 -- 15 May, 1991, $4,500.

92. P. Franzon, “CAD Tools for MCMs", MCNC. ($24,008), 16 May 1989 -- 15 September 1990.

93. Principal Investigator, “CAD tools for yield modeling", MCNC. (\$8,694), 16 August 1989 -- 15 May 1990.



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GIFTS IN CASH

1. P. Franzon, Qualcom, Faculty Award, $70,000, 2019, 2021
2. P. Franzon, Mentor Graphics, Verification Tool flow, $240,000, 2010 - 2020
3. P. Franzon, Google, $42,000
4. P. Franzon, IBM, $95,000
5. P. Franzon, W. Davis, Cadence, Tool Flows, $25,000
6. P. Franzon, W. Liu, Analog Alliance, $142,263
7. P. Franzon, M. Steer, Cadence, Interconnect, $350,000
8. P. Franzon, W. Liu, Unrestricted Gift, Mitsubishi, VLSI Research, $93,899
9. P. Franzon, Unrestricted Gift, Motorola, $21,100
10. P. Franzon, SRC, Chip-package codesign, $25,000
11. P. Franzon, IEEE, $20,000

EDUCATIONAL GRANTS

1. H.T. Nagle, D. Van Den Bout, T. Miller, P. Franzon, "Design Center for Teaching Digital Design", 1 September, 1990 -- 31 August, 1993, awarded by NSF ($500,000).

UNSPONSORED REASEARCH

PENDING PROPOSALS

EXTERNAL EQUIPMENT

1. P. Franzon, T. Conte, W. Liu, C. Gloster, "Experimental High Performance Computing and Communications Systems", NSF CISE Infrastructure Award, July 1, 1997 -- June 30, 2003, ($1,338,283 including $503,046 in NCSU matching).

Provide the research infrastructure for a variety of activities in the Computer Engineering group at NCSU-ECE.

INTERNAL GRANTS

1. Chancellors Innovation Fund Award, $50,000, 2013-14.
2. NCSU ECE CAD Lab, Provost Office, $75,000, 1995.

## C. ORGANIZATION PARTICIPATION

- Center for Advanced Electronics through Machine Learning, Site Director
- Electronics Research Laboratory, Co-Director
- Microelectronic Systems Laboratory, Director

## D. HONORS AND AWARDS RELATED TO SCHOLARLY EFFORTS



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- NCSU Innovator of the Year Award, 2015
- NRL Alan Berman Research Publication Award, 2008
- Babbage Award, Synopsys, 2008
- Fellow of the IEEE, 2006
- Alcoa Research Award, 2005
- NSW Australia Expatriate Scientist Award, 2003
- First round prize winner, SRC copper challenge, 2000.
- National Science Foundation Young Investigator's Award, 1993.
- 13 prizes while a student at the University of Adelaide



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# IV. EXTENSION AND ENGATEMENT WITH CONSTITUENCIES OUTSIDE THE UNIVERSITY

## A. ACCOMPLISHMENTS

- **NCSU Education and Research Design Kit. This is a CAD tool (software) kit that enables researchers to design silicon chips using the MOSIS brokered foundries, and the popular Cadence And Mentor Design Tools. Originally introduced in 1994, we maintain this kit actively. Right now, there are over 2,000 active users, dominated by Universities, but also used by Industry.. I started and lead this activity. It has won several prizes from Cadence and the Cadence Users Group. With Rhett Davis, it recently expanded in a 45 nm and 14 nm PDKs. Several tool tutorial were also recently added. More information can be found at www.ece.ncsu.edu/cadence**

- NCSU Spice2Ibis Converter. This is a freeware software utility that allows the automatic macromodeling of chip input/output in the EIA IBIS standard. We have supported this converter since 1997. Version 3 was written last year. There are over 3,000 active users, mainly Industry. Together Michael Steer and I started and maintain this activity. More information can be found at www.ece.ncsu.edu/s2ibis

## B. PROGRAM IMPACTS



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# V. TECHNOLOGICAL AND MANAGERIAL INNOVATION

## A. KNOWLEDGE/TECHNOLOGY TRANSFER

PATENTS FILED

U.S. Provisional Patent Application
Title: DESIGN OF CONTACTLESS CONNECTOR FOR SIMULTANEOUS POWER AND DATA TRANSFER
Serial No.: 62/700,975; Filing Date: July 20, 2018
Inventor(s): Nazia Zannat and Paul D. Franzon
NCSU Ref.: 18107 T|H Ref.: 221404-8570

Granted:

| | |
|---|---|
| US-6934252-B2 | Methods and systems for fast binary network address lookups using parent node informa |
| US-6985483-B2 | Methods and systems for fast packet forwarding |
| US-2011169589-A1 | reconfigurable filter apparatus |
| US-2003100200-A1 | Buried solder bumps for AC-coupled microelectronic interconnects |
| US-2013176763-A1 | Stacked memory with redundancy |
| US-2007128744-A1 | Self-assembly of molecules and nanotubes and/or nanowires in nanocell computing devi |
| US-2007297216-A1 | Self-assembly of molecular devices |
| US-2013279280-A1 | Stacked memory device with redundant resources to correct defects |
| US-2012175696-A1 | Multilayer floating gate field-effect transistor (fet) devices and related methods |
| US-2014376364-A1 | Temporal redundancy |
| US-2015340872-A1 | Electrical connector parts for combining power delivery and signaling in inductively coup |
| US-2013168674-A1 | Methods and Systems for Repairing Interior Device Layers in Three-Dimensional Integrat |
| US-8208578-B2 | Systems, methods, and computer readable media for fractional pre-emphasis of multi-m |
| WO-2012058074-A2 | Thermal isolation in 3d chip stacks using gap structures and contactless communications |
| US-2013314291-A1 | Millimeter scale three-dimensional antenna structures and methods for fabricating same |
| US-2013300498-A1 | Methods, systems, and computer program products for low power multimode interconn |
| US-2013069709-A1 | Ac powered logic circuits and systems including same |
| US-2014003549-A1 | Methods, systems, and computer program products for asymmetric multimode intercon |
| US-9613544-B2 | Electroactive, actuated dot structures and associated methods |
| US-9568546-B2 | Delay fault testing for chip I/O |
| WO-2004068497-A2 | Self-assembly of molecules and nanotubes and/or nanowires in nanocell computing devi |

Applications not (yet) granted:

TECHNOLOGY TRANSFER

- **<Numerous submission – no longer tracked>**



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- T. Conte and P. Franzon, "Networking Benchmark Kit", released 2004.
- P. Franzon. DLX RTL Design. This copyrighted microprocessor design has been released to several companies to help them evalaute their Computer Aided Design tools.
- P. Franzon. DES RTL Design. This copyright encryption design has been released to several companies to help them evalaute their Computer Aided Design tools.
- S. Lipa, A. Glaser, M. Steer, P. Franzon, Spice2Ibis software, available on the ERL Web Site.
- Y. Tekmen, S. Mehotra, P. Franzon, Signal Integrity Advisor software, available on the ERL Web Site.

**B. DESCRIBE PROGRAM IMPACTS**



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# VI. SERVICE TO UNIVERSITY AND PROFESSIONAL SOCIETIES

DEPARTMENT SERVICE

- **Director of Graduate Programs, 2016-**
- **Chair, Graduate Studies Committee, 2016-**
- **Chair, Graduate Admissions Committee, 2016-**
- Graduate Studies Committee, 1992-3, 2003-12
- ECE Mission Committee, 2010-
- ECE Awards Committee, 2010-
- Circuits Search Committee, 2001, 2002, 2003, 2004, 2005
- CPE Search Committee, 1995, 1996
- ECE Department Head Search Committee, 1995, 2002
- Obtained funding for and recruited, and directed NCSU IT infrastructure personnel, 1996-2001.

UNIVERSITY SERVICE

- **DELTA Advisory Committee, 2013-**
- **Intellectual Property Committee, 2009-12, 2015-**
- **COE Faculty Advancement Round Table, 2016-**
- STRAG committee member, 2003-2005
- COE Computing Committeee, 1994-1995

INTERNATIONAL PROFESSIONAL ACTIVITIES

- Member, Board of Governors, IEEE CPMT, 2007-2009, 2010-2013.
- **Chair, IEEE 3DIC Conference, 2009, 2013, 2016, 2019**
- General Chair, IEEE CPCW, 2011.
- Technical Program CoChair, NanoArch, 2009
- **Chair, IEEE EPEP, 2007, 2017**
- Co-chair, IEEE EPEP, 2006.
- **Associate Editor, IEEE Transactions on Advanced Packaging.**
- Associate Editor, ACM Journal on Emerging Computing Technologies**.**
- Program Committee Member, ChinaCOM, 2007-2008
- Program Committee Member, NanoArch, 2008-
- Program Committee Member, DesignCon, 2007-
- Program Committee Member, NanoNet, 2006-
- Program Committee Member, SPIE Microelectronics, MEMS, and Nanotechnology 2008
- **Program Committer Member, IEEE EPEP Workshop, ongoing**
- Program Committee Member, IEEE FDDP Workshop, ongoing
- Member, DARPA ISAT advisory committee on 3D ICs, 2003
- **Reviewer, Hong Kong Engineering Research Council.**
- **Reviewer, Australia Research Council**
- **Reviewer, Innovate Canada**
- **Reviewer, Singapore Science Foundation**



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- **Reviewer, National Science Foundation**
- **Reviewer, Army Research Office**
- **Reviewer, US Department of Agriculture**
- **Reviewer for the journals: IEEE Transactions on Computer Aided Design, IEEE Transactions on Computers, IEEE Trans CPMT, IEEE Trans VLSI Systems, IEEE Journal of Solid State Circuits, IEEE Trans. Semiconductor Manfuacturing, Nature Materials, IEEE MTT, amongst others**
- Co-organizer, NSF Workshop on Molecular Computing, 2002
- Member, DARPA ISAT advisory committee on Molecular Computing, 2002.
- Co-Technical Chair, IEEE/IMAPS System Packaging Workshop, RTP, NC May 14-16, 2002.
- Chair, Design, Characterization, and Packaging for MEMS and Microelectronics II, SPIE Conference, Adelaide, Australia, Dec. 2001.
- General Chair, 1997 IEEE MultiChip Module Conference.
- Technical Program Chair, 1996 IEEE MultiChip Module Conference.
- Program Committee, 1996/1997 IEEE Innovative Systems In Silicon Conference.
- General Chair, 1997 IEEE MultiChip Module Conference.
- Technical Program Chair, 1996 IEEE MultiChip Module Conference.
- Co-Chair, 1993 SouthEastern Universities Undergraduate Design Conference.
- Co-Chair, 1997 IEEE Workshop on Clock Design.
- Program Committee, 1997, 1998 IEEE Int. Conference on Computer Design.
- Program Committee, 1997, 1998 ISIS.
- Tutorial Chair, 1994, 1995 IEEE MultiChip Module Conference.
- Education Committee Chair, IEEE CPMT Society, 1992-1995.
- Program Committee and Tutorial Chair, 1993-2000 IEEE Topical Meeting on
- Electrical Performance of Electronic Packaging.
- Program Committee, MICRO/MEMS'99.
- Program Committee, MICRO/MEMS'00.
- Program Committee, CPD-99, CPD-00.
- Program Committee, 1998 IPID.
- Program Committee, 1998 IMAPS MCM Conference.
- Reviewer, Design Automation Conference..
- Reviewer, Swiss National Science Foundation.

As Director of Graduate Programs (May 2016-), I have achieved the following:

- In consultation with the faculty reduced the coursework requirements for PhD students
- In consultation with the faculty simplified the coursework requirements for MS students
- Refocused the graduate office with an emphasis on student service
- Took direct responsibility for MS recruiting and headed the GAC committee, which focused on PhD recruiting
- Made the recruiting season earlier with a focus on getting offers to top students out earlier
- Made recruiting “friendlier” with a letter to all admitted students



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- Started a “big data” program to guide future recruiting efforts
- Started regular review of PhD students and progress towards degrees
- Provided closer management of TAs
- Encouraged faculty to develop new courses in areas of high demand, leading to the introduction of an Advanced Verification course, a OS course, and a better focus on machine learning
- Started the process to allow semester CPT for International MS students
- Established Graduate Certificates in 5G, ASIC, CPE and EE
- Introduced an effective PhD Visit Day



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