

lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations.

And performing at least one write operation on said second memory device by at least using a transfer size at least equal to a [...] page size attribute value from said second set of attributes. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations. Column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

And said attribute difference includes different attribute values of said first and second [...] page size attributes. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Although Falik teaches storing a page size attribute, it does not expressly teach storing a partial page size attribute.

With respect to claim 24, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 24**.

Claim 93 is taught by Falik as shown supra with respect to claim 80, and further as:

The electronic storage device of claim 80, wherein said memory controller is further adapted to: use a first partial page size attribute by performing a write operation on said first memory device and using a transfer size at least equal to said partial page size attribute. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations.

And use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations. Column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

Although Falik teaches storing a page size attribute, it does not expressly teach storing a partial page size attribute.

With respect to claim 93, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 93**.

10. **Claims 26-28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Lakhani et al. (US 6,961,805).

Claim 26 is taught by Falik as shown supra with respect to claim 1.

Falik further teaches, at column 20 lines 60-65, that Page Size Block1 stores the size of the minimal segment of a flash array erasable upon a single erase command. Additionally, column 16 line 53 through column 17 line 24 shows that data can be written to a block of addresses by designating the starting address and performing a series of program continue operations.

Falik does not expressly teach using the block size attribute in performing a write operation that uses a transfer size that corresponds to the block size.

With respect to claim 26, Lakhani teaches, at column 18 lines 19-46, that predecoder 50 asserts sets of multiblock selection bits in response to control bits from the controller, which allows a designated number of blocks to be selected for writing at the same time.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to perform a write operation that uses a transfer size equal to the a block size attribute value that corresponds to a block size attribute of the first memory device.

The motivation for doing so would have been to reduce the time used to test the memory cells of the block, Lakhani column 8 lines 21-32.

Therefore, it would have been obvious to combine Lakhani with Falik to obtain the invention as specified in **claims 26 and 27**.

Claim 27 is taught by Lakhani as:

The method of claim 26, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value. Column 13 lines 25-38 shows that a plurality of blocks can be selected at the same time.

Claim 28 is taught by Falik as shown supra with respect to claim 2.

Falik further teaches, at column 20 lines 60-65, that Page Size Block1 stores the size of the minimal segment of a flash array erasable upon a single erase command. Additionally, column 16 line 53 through column 17 line 24 shows that data can be written to a block of addresses by designating the starting address and performing a series of program continue operations.

Falik does not expressly teach using the block size attribute in performing a write operation that uses a transfer size that is equal to a multiple of the block size.

With respect to claim 28, Lakhani teaches, at column 18 lines 19-46, that predecoder 50 asserts sets of multiblock selection bits in response to control bits from the controller, which allows a designated number of blocks to be selected for writing at the same time.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to perform a write operation that uses a transfer size equal to the a block size attribute value that corresponds to a block size attribute of the first memory device.

The motivation for doing so would have been to reduce the time used to test the memory cells of the block, Lakhani column 8 lines 21-32.

Therefore, it would have been obvious to combine Lakhani with Falik to obtain the invention as specified in **claim 28**.

11. **Claims 29-44** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Rubinstein et al. (US 5,913,215).

Claim 29 is taught by Falik as:

Said method comprising: addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Wherein said second memory location is in a second memory device in the memory store. Column 6 lines 11-16 shows that the different parameters correspond to different memory arrays. Accordingly, the address corresponding to a different section may be in a second memory device.

Said first device profile representing a first set of attributes of said first memory device, and said second device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14

lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

Wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location. Column 20 line 49 through column 21 line 15 shows that the section properties register stores values representing the section of the flash device, and that there is a section properties register for each section of the flash device.

Wherein the memory store is coupled by at least one memory bus to a controller, and wherein the controller performs the memory transactions on the memory store. Figure 1 shows that main die interface controller connects to the flash die via bus 90, as discussed at column 10 lines 5-15. Column 27 lines 8-32 shows that the MD sends commands to the FD.

Wherein the first device profile and second device profile are each stored in the memory store. Column 18 lines 53-64 show that the control, status and capabilities registers 12 and 112 are located on the flash device, and can be kept in the flash device's own memory.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Falik does not expressly teach that the methods may be implemented using a non-transitory computer readable medium comprising computer executable instructions.

With respect to claim 29, Rubinstein teaches at column 10, lines 3-15, that computer methods may be performed either by a series of instructions, or by specific hardware components that contain hard-wired logic for performing the method, or by any combination of the two.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a computer readable medium comprising computer executable instructions.

The rationale for doing so would have been that it is a known technique to implement methods in computer systems using a non-transitory computer readable medium comprising computer executable instructions.

Therefore, it would have been obvious to combine Rubinstein with Falik to obtain the invention as recited in **claims 29-44**.

Claim 30 is taught by Falik as:

The computer readable medium of claim 29, wherein: said first memory location is part of a memory space associated with a first memory device, said second memory location is part of a memory space associated with a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

And said first and second memory devices comprise at least a portion of a memory store. Figure 3 shows that the address space is mapped to the memory devices.

Claim 31 is taught by Falik as:

The computer readable medium of claim 29, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of a first memory device and a block size value of a second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 32 is taught by Falik as:

The computer readable medium of claim 30, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 33 is taught by Falik as:

The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 34 is taught by Falik as:

The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes.

Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

Claim 35 is taught by Falik as:

The computer readable medium of claim 29, wherein said addressing further includes: said first and second device profiles having at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 36 is taught by Falik as:

The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from

said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 37 is taught by Falik as:

The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 38 is taught by Falik as:

The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 39 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 40 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 41 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 42 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 43 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 44 is taught by Falik as:

The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

12. **Claims 61 and 64-68** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Chin et al. (US 2001/0010066).

Claim 61 is taught by Falik as shown supra with respect to claim 59.

Falik further teaches:

The memory controller of claim 59, wherein said interface controller includes: A first memory bus controller coupled to said control device and said memory device interface. Falik figure 4b item 116.

And an IO bus controller coupled to said IO device interface and said control device. Falik figure 4b item 117.

With respect to claim 61, Chin figure 2 teaches a bridge unit 104, which connects to a CPU bus 108 and a memory bus 110, including control logic 242, shown in paragraph 0037 to direct the operations of the queue storage elements through a network of control signals. Figure 2 also illustrates a data path between the CPU bus 108 and memory bus 110 through queues 250 and 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a main control device coupled to the memory device interface and data path as taught by Chin in the interface controller of Falik.

The motivation for doing so would have been to provide a means to manage the transfer of data through the interface performed by the system of Falik, see Chin paragraph 0037.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as specified in **claim 61**.

Claim 64 is taught by Falik as shown supra with respect to claim 59.

Falik does not expressly teach that a buffer is a FIFO or that a data path includes a plurality of queue slots.

With respect to claim 64, Chin teaches:

Further including a buffer comprising a FIFO. Paragraph 0052 shows that queue 250 is a FIFO.

And a data path that includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory

Art Unit: 2187

device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory.

Figure 2 also shows read queue 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a FIFO and a data path including a plurality of queue slots in the system of Falik.

The motivation for doing so would have been to provide an interface that provides all devices in a computer system fair access to memory, Chin paragraph 0012.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as recited in **claim 64**.

Claim 65 is taught by Falik as shown supra with respect to claim 59.

Falik does not expressly teach that a data path includes a buffer having a plurality of queue slots.

With respect to claim 65, Chin teaches:

The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a FIFO and a data path including a plurality of queue slots in the system of Falik.

The motivation for doing so would have been to provide an interface that provides all devices in a computer system fair access to memory, Chin paragraph 0012.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as recited in **claims 65-67**.

Claim 66 is taught by Chin as:

The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a plurality of queue slots that buffer data from said IO device interface to said memory device interface. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory.

Claim 67 is taught by Chin as:

The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from said memory device interface to said IO device interface. Figure 2 also shows read queue 252.

Claim 68 is taught by Falik as shown supra with respect to claim 1.

Falik further teaches a memory bus controller, figure 4b item 116, coupled to bus 90.

Falik does not expressly teach that the memory bus controller is coupled to a main control device.

With respect to claim 68, Chin teaches:

A second memory bus controller coupled to said main control device and said memory device interface. Figure 2 teaches a bridge unit 104, which connects to a CPU bus 108 and a memory bus 110, including control logic 242, shown in paragraph 0037 to direct the operations of the queue storage elements through a network of control signals. Figure 2 also illustrates a data path between the CPU bus 108 and memory bus 110 through queues 250 and 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a main control device coupled to the memory device interface and data path as taught by Chin in the interface controller of Falik.

The motivation for doing so would have been to provide a means to manage the transfer of data through the interface performed by the system of Falik, see Chin paragraph 0037.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as specified in **claim 68**.

13. **Claims 62 and 63** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Chin et al. (US 2001/0010066) as applied to claim 61 above, and further in view of Tsuruta (US 2007/0174506).

Claim 62 is taught by the combination of Falik and Chin as shown supra with respect to claim 61.

The combination of Falik and Chin does not expressly teach that the IO bus controller is disposed to respond to said memory transaction request by acknowledging said request and providing status to said main control device.

With respect to claim 62, Tsuruta teaches:

Wherein said IO bus controller is disposed to respond to a memory transaction request by acknowledging said request and providing status to said main control device. Paragraph 0183 shows that in response to a read req from the CPU, MEM-DMAC 232 issues a read ack signal. Paragraph 0186 shows that after the read operation is performed, a sequencer in the memory controller 231 issues ack to a sequencer in the MEM-DMAC 232.

At the time of the invention, it would have been obvious to use the acknowledgement system of Tsuruta in the combination of Falik and Chin.

The motivation for doing so would have been to provide coordination between the CPU interface and the read/write queues to perform the requested memory operations.

Therefore, it would have been obvious to combine Tsuruta with Falik and Chin to obtain the invention as specified in **claims 62 and 63**.

Claim 63 is taught by Chin as:

The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction. Paragraph 0052 shows that control logic provides control signals to the input and output

selectors 351 and 353 that determine the values of the enable and select signals in response to a memory request from the CPU.

Coordinates the operation of said memory device interface. Paragraph 0052 shows that the data and address of each request is sent to the memory controller 200.

And manages the transfer of memory transaction data between said IO device interface and said memory device interface through a data path.

Paragraph 0052 shows that data is transferred through the queue 250.

Response to Arguments

14. Applicant's arguments filed 6/19/2014 have been fully considered but they are not persuasive.

15. In the fourth paragraph beginning on page 27, Applicant argues:

"However, Applicants respectfully argue that the structure tables in Figures 5A-5F of Falik are properties of registers 12, Wherein the registers 12 are not disposed within memory devices in a memory store and the registers 12 of Falik are instead disposed within the flash interface controller 10. Thus, Falik discloses the structure tables (of Figures 5A-5F) as stored into the controller 10 (Falik: Figure 4A) and not stored in the flash memory arrays 70. Therefore, Falik does not disclose and does not teach the "first device profile and second device profile are each stored in the memory store" as required in claim 1. Additionally, Falik does not disclose and does not teach "wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location" as required in claim 1."

16. The Examiner respectfully disagrees. Falik column 18 lines 53-64 show that the information in control, status, and capabilities registers 12 may be echoed in registers 112 on the memory device, and that the contents of registers 12 may be stored in

Art Unit: 2187

locations in the memory of the flash device. Column 15 line 63 through column 16 line 19 shows that the section capabilities register stored data for a section of the memory, including main block size and page size. Paragraph 0016 of the specification of the instant application shows that an attribute qualifier is a value or type that indicates a characteristic related to the memory attribute. Column 20 line 49 through column 21 line 15 of Falik shows that values representing the main block size, page size, among others, are stored in the section properties register.

17. In the eighth paragraph beginning on page 30, Applicant argues:

“The Office admits that Falik does not expressly teach that the methods may be implemented using a computer readable medium comprising computer executable instructions. In order to supply the missing limitations, the Office combines Falik with Rubinstein. The Office argues it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a computer readable medium comprising computer executable instructions (Office Action: page 44). The Applicants respectfully disagree with the assertions of the Office.”

18. The Examiner respectfully disagrees. The Examiner notes that Applicant has provided no explanation as to why it would not have been obvious to one of ordinary skill in the art to implement a method in a computer using a computer readable medium comprising computer executable instructions. The Examiner does not find this assertion persuasive, as the use of a computer readable medium storing instructions to implement a method in a computer is a well-known technique to one of ordinary skill in the art, as shown by Rubinstein.

Conclusion

19. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JARED RUTZ whose telephone number is (571)272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, April Blair can be reached on (571)270-1014. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2187

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jared I Rutz
Primary Examiner
Art Unit 2187

/JARED RUTZ/
Primary Examiner, Art Unit 2187

Search Notes 	Application/Control No. 12876113	Applicant(s)/Patent Under Reexamination BRUCE ET AL.
	Examiner JARED RUTZ	Art Unit 2187

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
inventor search in EAST	12/14/2012	jir
text search in EAST, see search history	12/14/2012	jir
internet search using google.com	12/14/2012	jir
updated search in EAST	5/7/2013	jir
updated search in EAST	3/8/2014	jir
updated search in EAST	7/7/2014	jir

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

--	--

<i>Index of Claims</i> 	Application/Control No. 12876113	Applicant(s)/Patent Under Reexamination BRUCE ET AL.
	Examiner JARED RUTZ	Art Unit 2187

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant						☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE									
Final	Original	12/14/2012	05/07/2013	03/08/2014	07/07/2014						
	1	✓	✓	✓	✓						
	2	✓	✓	✓	✓						
	3	✓	✓	✓	✓						
	4	✓	✓	✓	✓						
	5	✓	✓	✓	✓						
	6	✓	✓	✓	✓						
	7	✓	✓	✓	✓						
	8	✓	✓	✓	✓						
	9	✓	✓	✓	✓						
	10	✓	✓	✓	✓						
	11	✓	✓	✓	✓						
	12	✓	✓	✓	✓						
	13	✓	✓	✓	✓						
	14	✓	✓	✓	✓						
	15	✓	✓	✓	✓						
	16	✓	✓	✓	✓						
	17	✓	✓	✓	✓						
	18	✓	✓	✓	✓						
	19	✓	✓	✓	✓						
	20	✓	✓	✓	✓						
	21	✓	✓	✓	✓						
	22	✓	✓	✓	✓						
	23	✓	✓	✓	✓						
	24	✓	✓	✓	✓						
	25	✓	✓	✓	✓						
	26	✓	✓	✓	✓						
	27	✓	✓	✓	✓						
	28	✓	✓	✓	✓						
	29	✓	✓	✓	✓						
	30	✓	✓	✓	✓						
	31	✓	✓	✓	✓						
	32	✓	✓	✓	✓						
	33	✓	✓	✓	✓						
	34	✓	✓	✓	✓						
	35	✓	✓	✓	✓						
	36	✓	✓	✓	✓						

<i>Index of Claims</i> 	Application/Control No. 12876113	Applicant(s)/Patent Under Reexamination BRUCE ET AL.
	Examiner JARED RUTZ	Art Unit 2187

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		DATE							
Final	Original	12/14/2012	05/07/2013	03/08/2014	07/07/2014				
	37	✓	✓	✓	✓				
	38	✓	✓	✓	✓				
	39	✓	✓	✓	✓				
	40	✓	✓	✓	✓				
	41	✓	✓	✓	✓				
	42	✓	✓	✓	✓				
	43	✓	✓	✓	✓				
	44	✓	✓	✓	✓				
	45	✓	✓	✓	✓				
	46	✓	✓	✓	✓				
	47	✓	✓	✓	✓				
	48	✓	✓	✓	✓				
	49	✓	✓	✓	✓				
	50	✓	✓	✓	✓				
	51	✓	✓	✓	✓				
	52	✓	✓	✓	✓				
	53	✓	✓	✓	✓				
	54	✓	✓	✓	✓				
	55	✓	✓	✓	✓				
	56	✓	✓	✓	✓				
	57	✓	✓	✓	✓				
	58	✓	✓	✓	✓				
	59	✓	✓	✓	✓				
	60	✓	✓	✓	✓				
	61	✓	✓	✓	✓				
	62	✓	✓	✓	✓				
	63	✓	✓	✓	✓				
	64	✓	✓	✓	✓				
	65	✓	✓	✓	✓				
	66	✓	✓	✓	✓				
	67	✓	✓	✓	✓				
	68	✓	✓	✓	✓				
	69	✓	✓	✓	✓				
	70	✓	✓	✓	✓				
	71	✓	✓	✓	✓				
	72	✓	✓	✓	✓				

<i>Index of Claims</i> 	Application/Control No. 12876113	Applicant(s)/Patent Under Reexamination BRUCE ET AL.
	Examiner JARED RUTZ	Art Unit 2187

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		DATE							
Final	Original	12/14/2012	05/07/2013	03/08/2014	07/07/2014				
	73	✓	✓	✓	✓				
	74	✓	✓	✓	✓				
	75	✓	✓	✓	✓				
	76	✓	✓	✓	✓				
	77	✓	✓	✓	✓				
	78	✓	✓	✓	✓				
	79	✓	✓	✓	✓				
	80	✓	✓	✓	✓				
	81	✓	✓	✓	✓				
	82	✓	✓	✓	✓				
	83	✓	✓	✓	✓				
	84	✓	✓	✓	✓				
	85	✓	✓	✓	✓				
	86	✓	✓	✓	✓				
	87	✓	✓	✓	✓				
	88	✓	✓	✓	✓				
	89	✓	✓	✓	✓				
	90	✓	✓	✓	✓				
	91	✓	✓	✓	✓				
	92	✓	✓	✓	✓				
	93	✓	✓	✓	✓				
	94				✓				
	95				✓				
	96				✓				
	97				✓				

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	("5913215").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/07/07 16:08
S1	0	(bruce near2 ircardo).in. or (verdan near2 marlon).in. or (somera near2 margaret anne).in. or (jago-on near2 rowenah).in. or (de belen near2 maria).in. or (palacol near2 ron).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/03 15:36
S2	17	(bruce near2 ricardo).in. or (verdan near2 marlon).in. or (somera near2 margaret).in. or (jago-on near2 rowenah).in. or (de belen near2 maria).in. or (palacol near2 ron).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/03 15:38
S7	3204	(plural or multiple or seperate) with (profile or attribute or parameters) with (memory)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:03
S8	3335	(hybrid or heterogenous) near3 memory	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:04
S9	112740	(hybrid or heterogenous or different) near3 memory	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:04
S10	619	S7 and S9	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:04
S11	15	S7 and S8	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:04
S12	15	S11 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT;	ADJ	OFF	2012/12/05 17:05

			IBM_TDB			
S13	10	("20020184579" "20050090940" "20060059314" "20080183958" "20090319722").PN.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:13
S14	193506	(memory or device) near3 (parameter or attribute)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/05 17:36
S15	4741	(plural or multiple or seperate) with (profile or attribute or parameter) with (memory)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/05 17:36
S16	2473	S14 and S15	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/05 17:36
S17	20106	(parameter or attribute) with (flash or nand or nor)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/05 17:37
S18	204	S16 and S17	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/05 17:37
S19	181	S18 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:37
S20	10	S19 and (page near3 size)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:38
S21	28	("4309754" "4633437" "4683534" "4716527" "5113369" "5369754" "5423009" "5537624" "5537659" "5594874" "5761456" "5768560" "5778413" "5911053" "6016270" "6101565" "6202140" "6235554" "6298426" "6381664" "6442076" "6472747" "6605875" "6618790" "6657899" "6658508" "6721840" "7146510").PN. OR ("8200879").URPN.	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/12/06 12:54
S25	1	("6,430,663").PN.	US-PGPUB;	OR	OFF	2012/12/11

			USPAT; USOCR			15:23
S26	1	("5913215").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/12/13 10:22
S27	113091	(hybrid or heterogenous or different) near3 memory	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:03
S28	26	S27 and (DRAM same NAND same NOR same battery)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:03
S29	13	S28 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:03
S30	299	partial page program\$4	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:48
S31	192	S27 and S30	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:48
S32	13	S29 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:48
S33	165	S31 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:48
S34	53823	(short\$3 or shorten\$3 or truncat\$3) near3 (burst or transmission)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:50
S35	0	S33 and S34	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:50
S36	0	S30 and S34	US-PGPUB;	ADJ	OFF	2012/12/13

			USPAT; USOCR; EPO; DERWENT; IBM_TDB			11:50
S37	20	S30 and burst	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 12:26
S38	14	S37 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 12:26
S39	92	partial page with (size or attribute)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 12:29
S40	6	S33 and S39	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 12:29
S41	198032	(profile or attribute or parameter) with (memory)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/13 12:32
S42	54	S33 and S41	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/13 12:32
S43	1	("5860107").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/12/13 13:20
S44	11735	(short\$3 or shorten\$3 or truncat\$3) near3 (burst)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 15:18
S45	141	((multiple or plural or series) near3 (burst)) with (remaining or remainder or additional)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 15:19
S46	26	S44 and S45	US-PGPUB; USPAT; USOCR; EPO;	ADJ	OFF	2012/12/13 15:20

			DERWENT; IBM_TDB			
S47	24	S46 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 15:20
S48	135	S45 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 15:29
S49	1	("20060184723").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/12/13 17:13
S50	110530	(writ\$3 or program\$4) near3 block	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:33
S51	6832	(711/103).OCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/12/13 19:34
S52	3586	S50 and S51	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:34
S53	19	(writ\$3 or program\$4) near3 multiple blocks with (instruction or command)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:45
S54	299	(writ\$3 or program\$4) near3 multiple blocks	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:52
S55	44	S51 and S54	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:52
S57	37	S55 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:52
S58	285682	(flash or memory) near3 controller	US-PGPUB; USPAT; USOCR; EPO;	ADJ	OFF	2012/12/14 12:50

			DERWENT; IBM_TDB			
S59	6008	(flash or memory) near3 interface with (bus near3 (controller or master))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:51
S60	5308	S58 and S59	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:51
S61	10796	fifo with input with output	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:52
S62	101	S60 and S61	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:52
S63	4117	fifo with (slots or entries)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:53
S64	4	S62 and S63	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:53
S65	99	S62 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 13:00
S66	113091	(hybrid or heterogenous or different) near3 memory	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 13:15
S67	790	S60 and S66	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 13:15
S68	18560	(fifo or queue) with input with output	US-PGPUB; USPAT; USOCR; EPO;	ADJ	OFF	2012/12/14 13:16

			DERWENT; IBM_TDB			
S69	42	S67 and S68	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 13:16
S70	41	S69 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 13:16
S71	134	(acknowledg\$3 or acknoweledge ment or ack) with (bus near3 (controller or master)) with CPU	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:13
S72	5308	S58 and S59	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:13
S73	10	S59 and S71	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:14
S74	10	S73 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:14
S75	477	(status or complet\$3) with (bus near3 (controller or master)) with CPU	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:21
S76	43	S71 and S75	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:21
S77	43	S76 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:21
S78	58	(acknowledg\$3 or acknoweledge ment or ack) with (memory near3 (controller)) with CPU	US-PGPUB; USPAT; USOCR; EPO;	ADJ	OFF	2012/12/14 15:24

			DERWENT; IBM_TDB			
S79	57	S78 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:25
S80	1016	(status or complet\$3 or error) with (memory near3 (controller)) with CPU	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:25
S81	11	S79 and S80	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:25
S82	12083	(short\$3 or shorten\$3 or truncat\$3) near3 (burst)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2013/05/06 16:15
S83	143	((multiple or plural or series) near3 (burst)) with (remaining or remainder or additional)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2013/05/06 16:15
S84	26	S82 and S83	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2013/05/06 16:15
S85	24	S84 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2013/05/06 16:15
S86	1	("8200879").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/05/06 16:18
S87	203091	(memory or device) near3 (parameter or attribute)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2013/05/06 17:45
S88	5067	(plural or multiple or seperate) with (profile or attribute or parameter) with (memory)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2013/05/06 17:45
S89	2613	S87 and S88	US-PGPUB;	ADJ	ON	2013/05/06

			USPAT; USOCR; EPO; DERWENT; IBM_TDB			17:45
S90	21098	(parameter or attribute) with (flash or nand or nor)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2013/05/06 17:45
S91	222	S89 and S90	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2013/05/06 17:45
S92	185	S91 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2013/05/06 17:45
S95	3	((("7013376") or ("20070143569") or ("5627987"))).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/05/08 13:24
S96	226660	(memory or device) near3 (parameter or attribute)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2014/03/07 18:12
S97	5687	(plural or multiple or seperate) with (profile or attribute or parameter) with (memory)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2014/03/07 18:12
S98	2903	S96 and S97	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2014/03/07 18:12
S99	23258	(parameter or attribute) with (flash or nand or nor)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2014/03/07 18:12
S100	254	S98 and S99	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2014/03/07 18:12
S101	191	S100 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO;	ADJ	OFF	2014/03/07 18:12

			DERWENT; IBM_TDB			
S102	1227	(g06f13/1694 or g06f2212/7207 or g06f2213/16 or g06f2213/1602).cpc.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2014/03/07 18:18
S103	43	S97 and S102	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2014/03/07 18:18
S104	34	S103 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2014/03/07 18:18
S105	188	("20020073324" "20020141244" "20030182576" "20030204675" "20030223585" "20040128553" "20070019573" "20070083680" "20070130439" "20070174493" "20070195957" "20090094411" "4752871" "5222046" "5297148" "5341339" "5371709" "5379401" "5388083" "5396468" "5406529" "5432748" "5448577" "5459850" "5479638" "5485595" "5488711" "5500826" "5509134" "5513138" "5524231" "5530828" "5535328" "5535356" "5542082" "5548741" "5559956" "5568423" "5568439" "5572466" "5594883" "5602987" "5603001" "5606529" "5606532" "5619470" "5627783" "5640349" "5644784" "5737742" "5802554" "5819307" "5822251" "5875351" "5881264" "5918033" "5943421" "6000006" "6215875" "6230269" "6298071" "6363441" "6363444" "6404772" "6526506" "6529416" "6557095" "6857076" "6901499" "6970446" "6980795" "7103684" "7194766" "7283629" "7305548" "7372962" "7500063" "7620748" "7660941" "7716389" "7743202" "7765359" "7934052").PN.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2014/03/08 13:29
S106	341914	(flash or memory) near3 controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2014/07/02 10:13
S107	6686	(flash or memory) near3 interface with (bus near3 (controller or master))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2014/07/02 10:13

S108	5862	S106 and S107	US- PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2014/07/02 10:13
S109	133684	(hybrid or heterogenous or different) near3 memory	US- PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2014/07/02 10:13
S110	894	S108 and S109	US- PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2014/07/02 10:13
S111	20477	(fifo or queue) with input with output	US- PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2014/07/02 10:13
S112	44	S110 and S111	US- PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2014/07/02 10:13
S113	41	S112 and @ad<"20100904"	US- PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2014/07/02 10:13
S114	235975	(memory or device) near3 (parameter or attribute)	US- PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2014/07/02 10:33
S115	5962	(plural or multiple or seperate) with (profile or attribute or parameter) with (memory)	US- PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2014/07/02 10:33
S116	3025	S114 and S115	US- PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2014/07/02 10:33
S117	24212	(parameter or attribute) with (flash or nand or nor)	US- PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2014/07/02 10:33

S118	267	S116 and S117	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2014/07/02 10:33
S119	195	S118 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2014/07/02 10:33
S132	2	((("20080270694") or ("20100082901")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/07/07 13:19
S133	1	("20110307658").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/07/07 14:07

7/ 7/ 2014 4:21:46 PM
C:\ Users\ jrutz\ Documents\ EAST\ Workspaces\ 12876113.wsp

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	) Confirmation No.: 1607
Ricardo H. Bruce, et al.	)
	) Examiner: Jared Ian Rutz
Serial No.: 12/876,113	) Ph: 571-272-5535
	)
Filing Date: Sept. 4, 2010	) Art Unit: 2187
	)
Title: Multi-Profile Memory	) Atty. Docket No.: 6005.042
Controller For Computing	)
Devices	)
	)

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**RESPONSE TO FINAL OFFICE ACTION
AND AMENDMENT**

Dear Sir:

The following is in response to the final office
action mailed on 11 July 2013.

Amendments to the Claims are reflected in the listing of
claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 27 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising:

addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile, wherein said second memory location is in a second memory device in the memory store, wherein a memory read transaction or a memory write transaction is performed on at least one of the first memory location or second memory location, wherein data is transferred to the first memory location or second memory location from a host for a memory write transaction, wherein data is transferred from the first memory location or second memory location to the host for a memory read transaction;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;

wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location;

wherein the memory store is directly coupled [[by]]to at least one memory bus and wherein the at least one memory bus is directly coupled to a controller, and wherein the controller performs the memory read transaction and memory write transaction on the memory [[sore]]store;

wherein the host is directly coupled to the controller by a communication path as the controller performs the memory read transaction or memory write transaction;

wherein the first device profile and second device profile are each stored in the memory store; and

using attributes from said first and second device profiles.

2. (original) The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device.

3. (original) The method of claim 1, wherein said difference between said first and second device profiles includes different attributes; and said addressing said first memory location is made in response to a first memory transaction request; and

further including addressing said second memory location.

4. (original) The method of claim 1, wherein:
said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and
said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes.
5. (original) The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.
6. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute values.
7. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute types.
8. (original) The method of claim 5, wherein said shared attributes include a memory device type attribute.
9. (original) The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

10. (original) The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

11. (original) The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

12. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

13. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of attributes that differs in value from a second page size attribute from said second set of attributes.

14. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes.

15. (original) The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device, and said second memory device interface attribute corresponds to a DRAM device interface.

16. (original) The method of claim 2, wherein said using attributes from said first and second device profile further includes using a first partial page size attribute from said first set of attributes that differs in value from a second partial page size attribute from said second set of attributes.

17. (original) The method of claim 16:

said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute; and

further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute.

18. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

19. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a NAND flash

memory device and said second memory device type attribute corresponds to a NOR flash memory device.

20. (original) The method of claim 2, further including:
using an address corresponding to a memory location
from said first memory device and transferring a first data
set, and

using an address corresponding to a memory location
from said second memory device and transferring a second
data set.

21. (original) The method of claim 20, wherein:

said first set of attributes includes a first page
size attribute, and said first data set includes a first
data set size; and

if said first data set size is at most equal to said
first page size attribute, said transferring said first
data includes using a first transfer size equal to said
first data set size.

22. (original) The method of claim 20, wherein:

said second set of attributes includes a second page
size attribute, and said second data set includes a second
data set size; and

if said second data set size is greater than said
second page size attribute, said transferring said second
data set includes:

performing a set of write operations on said second
memory device that includes using a second transfer size
equal to said second page size attribute until a remaining

portion of said second data set that has not yet been written to said second device is less than said second page size attribute, and

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

23. (previously presented) The method of claim 20, wherein:

said first set of attributes includes a page size attribute and a block size attribute;

said first data set includes a first data set size;

if said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes:

performing a set of write operations on said first memory device that includes using a second transfer size equal to said page size attribute until a remaining portion of said first data set that has not yet been written to said first device is less than said page size attribute,

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

24. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes:

performing respective write operations on said first and second memory devices by at least using a transfer size at least equal to a partial page size attribute from said

first set of attributes and performing at least one write operation on said second memory device by at least using a transfer size at least equal to a partial page size attribute value from said second set of attributes; and
 said attribute difference includes different attribute values of said first and second partial page size attributes.

25. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size attribute of said first memory device.

26. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a block size attribute value that corresponds to a block size attribute of said first memory device.

27. (original) The method of claim 26, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

28. (original) The method of claim 2, wherein said using attributes from said first and second device profile

further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

29. (previously presented) A non-transitory computer readable medium comprising computer executable instructions adapted to cause a method of performing memory transactions on a first memory location and a second memory location, said method comprising:

addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory device, and said second device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles; and

using attributes from said first and second device profiles.

30. (original) The computer readable medium of claim 29, wherein:

said first memory location is part of a memory space associated with a first memory device;

said second memory location is part of a memory space associated with a second memory device; and

said first and second memory devices comprise at least a portion of a memory store.

31. (previously presented) The computer readable medium of claim 29, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of a first memory device and a block size value of a second memory device.

32. (previously presented) The computer readable medium of claim 30, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

33. (original) The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

34. (original) The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes.

35. (previously presented) The computer readable medium of claim 29, wherein said addressing further includes:

said first and second device profiles having at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

36. (original) The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

37. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values.

38. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types.

39. (original) The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute.

40. (original) The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

41. (original) The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

42. (original) The computer readable medium of claim 36, wherein said shared attributes includes any one of the

following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

43. (original) The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes.

44. (original) The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device.

45. (currently amended) A memory controller for performing memory transactions, said memory controller comprising:

a means for addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile;

said means for addressing is directly coupled to the first memory location and second memory location;

wherein said means for addressing includes an interface controller means for processing memory transaction requests;

said means for addressing is directly coupled to a host as said means for addressing addresses the first memory location or second memory location;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of

said second memory location, and a difference exists between said first and second device profiles; and

said means for addressing uses attributes from said first and second device profiles.

46. (original) The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

47. (original) The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

48. (original) The memory controller of claim 46, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said use of said attributes from said first and second device profiles by said means for addressing includes using said different attribute qualifiers for said shared attributes.

49. (original) The memory controller of claim 46, wherein said at least one attribute includes a block size and said

difference includes a block size value of said first memory device and a block size value of said second memory device.

50. (previously presented) The memory controller of claim 45, wherein said means for addressing further includes a means for addressing said second memory location.

51. (original) The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

52. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values.

53. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types.

54. (original) The memory controller of claim 51, wherein said shared attributes include a memory device type attribute.

55. (original) The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

56. (original) The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

57. (original) The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

58. (original) The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device.

59. (currently amended) A memory controller comprising:
 an interface controller coupled to a memory device interface and an input/output (IO) device interface;
a memory store;
wherein the memory device interface is directly coupled to the memory store;

said interface controller disposed to perform a memory transaction by addressing a first memory location in the memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile;

said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said addressing of said first memory location includes using said attributes from said first device profile.

60. (original) The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile.

61. (previously presented) The memory controller of claim 59, wherein said interface controller includes:

- a main control device coupled to said memory device interface and to a data path;

- a first memory bus controller coupled to said control device and said memory device interface; and

- an IO bus controller coupled to said IO device interface and said control device.

62. (previously presented) The memory controller of claim 61, wherein said IO bus controller is disposed to respond to a memory transaction request by acknowledging said request and providing status to said main control device.

63. (original) The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction, coordinates the operation of said memory device interface, and manages the transfer of memory transaction data between said IO device interface and said memory device interface through a data path.

64. (previously presented) The memory controller of claim 59, further including a buffer comprising a FIFO and a data path that includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface.

65. (original) The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots.

66. (original) The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a plurality of queue slots that buffer data from said IO device interface to said memory device interface.

67. (original) The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from said memory device interface to said IO device interface.

68. (previously presented) The memory controller of claim 59, further including a second memory bus controller coupled to a main control device and said memory device interface.

69. (original) The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes.

70. (original) The memory controller of claim 59, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

71. (original) The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

72. (original) The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute.

73. (original) The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values.

74. (original) The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values.

75. (original) The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type.

76. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values.

77. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types.

78. (original) The memory controller of claim 71, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

79. (original) The memory controller of claim 71, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

80. (currently amended) An electronic storage device, comprising:

a memory controller directly coupled to and disposed to address a first memory location and a second memory

location which are respectively associated with a first device profile and a second device profile;

said memory controller directly coupled to a host as said memory controller addresses the first memory location or second memory location;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said memory controller using attributes from said first and second device profiles.

81. (original) The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

82. (original) The electronic storage device of claim 80, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

83. (previously presented) The electronic storage device of claim 80, said memory controller further disposed to:

perform a write operation on said first memory device, if a memory transaction request is associated with a write request;

perform a read operation on said first memory device, if said memory transaction request is associated with a read request; and

wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using said second device profile in response to receiving a second memory transaction request.

84. (original) The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

85. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values.

86. (original) The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute.

87. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types.

88. (original) The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said shared attributes.

89. (original) The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device.

90. (original) The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

91. (original) The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

92. (original) The electronic storage device of claim 84, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

93. (original) The electronic storage device of claim 80, wherein said memory controller is further adapted to:

use a first partial page size attribute by performing a write operation on said first memory device and using a transfer size at least equal to said partial page size attribute; and

use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute.

94. (previously presented) The method of claim 1, wherein the first memory location and the second memory location are addressable memory locations.

95. (previously presented) The memory controller of claim 45, wherein the first memory location and the second memory location are addressable memory locations.

96. (previously presented) The memory controller of claim 59, wherein the first memory location and the second memory location are addressable memory locations.

97. (previously presented) The electronic device of claim 80, wherein the first memory location and the second memory location are addressable memory locations.

98. (new) An electronic storage device, comprising:

a memory controller directly coupled to and disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile;

wherein the memory controller is directly coupled to a host as the memory controller addresses the first memory location or the second memory location;

the first device profile representing a first set of attributes of the first memory location, and the second device profile representing a second set of attributes of the second memory location; and

wherein said memory controller uses attributes from the first and second device profiles.

99. (new) The electronic devices of claim 98, wherein the memory controller comprises:

an interface controller;

a memory device interface directly coupled to the first memory location and to the second memory location and coupled to the interface controller;

an input/output (IO) device interface coupled to the interface controller and directly coupled to the host as the memory controller addresses the first memory location or the second memory location.

100. (new) A method for performing memory transactions, the method comprising:

addressing a first memory location in a first memory device in a memory store, the first memory location and a second memory location respectively associated with a first device profile and a second device profile;

the first device profile representing a first set of attributes of the first memory location, and the second device profile representing a second set of attributes of the second memory location;

wherein the memory store is directly coupled to a memory controller, and wherein the memory controller performs a memory transaction;

wherein the host is directly coupled to the memory controller as the memory controller performs the memory transaction; and

using attributes from the first and second device profiles.

101. (new) The method of claim 100, wherein the memory controller comprises:

an interface controller;

a memory device interface directly coupled to the first memory location and to the second memory location and coupled to the interface controller;

an input/output (IO) device interface coupled to the interface controller and directly coupled to the host as the memory controller addresses the first memory location or the second memory location.

REMARKS/ARGUMENTSNew Claims

Claims 98-101 are being added and are supported in the filed application in, for example, Figures 1, 2A, 2B, 2C, 4, 5, and 6 and accompanying text. New claims 98-101 recite at least some features that are not disclosed and are not suggested in the cited references in the final office action dated 11 July 2014.

Since the cited references do not disclose and do not teach all the limitations of claims 98-101, claims 98-101 are not rendered obvious in view of the cited references. Claims 98-101 are each otherwise allowable.

Applicant respectfully requests the allowance of claims 98-101.

Claim Rejections35 USC 102

Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-97

Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-97 are rejected under 35 U.S.C. 102(e) as allegedly being anticipated by US 8,200,879 to Falik et al. ("Falik"). Claims 1, 45, 59, and 80 are independent claims. Applicants respectfully traverse this rejection.

Applicants respectfully disagree with this rejection, but to expedite allowance of the claims, Applicants amend independent claim 1 herein to recite various features as shown above. Support for the amendment in claim 1 is found

in the filed application in, for example, Figures 1, 2A, 2B, 2C, 4, 5, and 6 and accompanying text.

Falik discloses a dual-controllers configuration having a main die controller 110 in a semiconductor main die 110, a flash die controller in a flash die 80, and a bus 90 directly coupled between the controller 110 and controller 10 (Falik: Figures 1, 4A, and 4B). Falik's dual-controllers configuration permits the semiconductor main die 10 to communicate with the flash die 80.

In contrast, claim 1 recites the features of, for example, a controller that is directly coupled by at least one memory bus to a memory store and the controller is also directly coupled to a host as the controller performs a memory transaction. The recited features in claim 1 are not disclosed in Falik. The recited features in claim 1 also advantageously avoids, for example, the complex circuitries (and increased die area and increased power requirements) of the dual-controllers configuration of Falik. Such advantages provided by the recited features of claim 1 are neither disclosed nor suggested in Falik, and it would be unreasonable to impart such advantageous limitations of claim 1 into Falik. Therefore, claim 1 recites limitations that are distinguishable from Falik based on at least the above-discussed advantages and/or based on the above-discussed claim 1 limitations that are absent in Falik.

Accordingly, Falik does not disclose all the limitations of claim 1. Since Falik does not disclose and does not teach all the limitations of claim 1, claim 1 is

not anticipated by the cited reference. Claim 1 is otherwise allowable.

Claims 2-14, 20, 21, and 25 depend from allowable claim 1; as such, they are also allowable for at least the same reasons as claim 1.

The withdrawal of the rejections to claims 1-14, 20, 21, 25 and 94 is respectfully requested.

Independent claims 45, 59, and 80 recite at least some limitations similar to that as claim 1. Although claims 45, 59, and 80 are different, Applicants respectfully argue that in this case the above arguments regarding the patentability of claim 1 apply with equal force with respect to claims 45, 59, and 80. Since Falik does not disclose and does not teach all the limitations of claims 45, 59, and 80, claims 45, 59, and 80 are not anticipated by the cited reference. Claims 45, 59, and 80 are otherwise allowable.

Claims 46-58 and 95 depend from allowable claim 45; as such, they are also allowable for at least the same reasons as claim 45.

Claims 60, 69-79, and 96 depend from allowable claim 59; as such, they are also allowable for at least the same reasons as claim 59.

Claims 81-92 and 97 depend from allowable claim 80; as such, they are also allowable for at least the same reasons as claim 80.

The withdrawal of the rejection to claims 45-60, 69-92, and 95-97 is respectfully requested.

Claims 15, 18, and 19

Claims 15, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 7,330,954 to Nangle.

Claims 15, 18, and 19 depend from allowable claim 1; as such, they are also allowable for at least the same reasons a claim 1.

The withdrawal of the rejection of claims 15, 18, and 19 is respectfully requested.

Claims 16, 17, 22-24, and 93

Claims 16, 17, 22-24, and 93 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 2006/0184723 to Sinclair.

Claims 16, 17, and 22-24 depend from allowable claim 1; as such, they are also allowable for at least the same reasons a claim 1.

Claim 93 depends from allowable claim 80; as such, claim 93 is also allowable for at least the same reasons a claim 1.

The withdrawal of the rejection of claims 16, 17, 22-24, and 93 is respectfully requested.

Claims 26-28

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 6961,805 to Lakhani et al.

Claims 26-28 depend from allowable claim 1; as such, they are also allowable for at least the same reasons a claim 1.

The withdrawal of the rejection of claims 26-28 is respectfully requested.

Claims 29-44

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 5,913,215 to Rubinstein.

The Office admits that Falik does not expressly teach that the methods may be implemented using a computer readable medium comprising computer executable instructions. In order to supply the missing limitations, the Office combines Falik with Rubinstein. The Office argues it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a computer readable medium comprising computer executable instructions (Office Action: page 44). The Applicants respectfully disagree with the assertions of the Office.

Independent claim 29 recite at least some limitations similar to that as claim 1. Although claim 29 is different, Applicants respectfully argue that in this case the above arguments regarding the patentability of claim 1 apply with equal force with respect to claim 29.

Since Falik and Rubinstein, considered individually or in combination, do not disclose and does not teach all the limitations of claim 29, claim 29 is not rendered obvious in view the cited references. Claim 29 is otherwise allowable.

Claims 30-44 depend from allowable claim 29; as such, they are also allowable for at least the same reasons a claim 29.

The withdrawal of the rejection of claims 29-44 is respectfully requested.

Claims 61 and 64-68

Claims 61 and 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 2001/0010066 to Chin et al.

Claims 61 and 64-68 depend from allowable claim 59; as such, they are also allowable for at least the same reasons a claim 59.

The withdrawal of the rejection of claims 61 and 64-68 is respectfully requested.

Claims 62 and 63

Claims 61 and 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of Chin as applied to claim 61 above, and further in view of US 2007/0174506 to Tsuruta.

Claims 62 and 63 depend from allowable claim 59; as such, they are also allowable for at least the same reasons a claim 59.

The withdrawal of the rejection of claims 62 and 63 is respectfully requested.

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, the Applicants are not conceding in this application that previously pending claims are unpatentable over the cited references. Rather, any alterations or characterizations

are being made to facilitate expeditious prosecution of
this application.

Conclusion

Claims 1-101 herein are allowable, and a timely Notice of Allowance is respectfully requested.

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (805) 569-1600.

Date: October 7, 2014

Respectfully submitted,

_____/Arnold de Guzman/_____
 Arnold de Guzman
 Attorney for Applicant(s)
 Reg. No. 39,955
 805-569-1600

Please send correspondence to:
 Customer No. 64180

CERTIFICATE OF TRANSMISSION OR MAILING 37 C.F.R. 1.8			
I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office in accordance with 37 C.F.R. § 1.6(d), or is being transmitted via the Office electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4), or is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below:			
Signature:			
Typed or Printed Name:	Arnold de Guzman	Dated:	7 October 2014
Express Mail Mailing Number (optional):			

Electronic Patent Application Fee Transmittal

Application Number:	12876113			
Filing Date:	04-Sep-2010			
Title of Invention:	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES			
First Named Inventor/Applicant Name:	Ricardo H. BRUCE			
Filer:	Stephen Radcliff Uriarte/Arnold deGuzman			
Attorney Docket Number:	6005.042			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Claims in Excess of 20	1202	4	80	320
Independent claims in excess of 3	1201	2	420	840
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1160

Electronic Acknowledgement Receipt

EFS ID:	20356628
Application Number:	12876113
International Application Number:	
Confirmation Number:	1607
Title of Invention:	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES
First Named Inventor/Applicant Name:	Ricardo H. BRUCE
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte/Arnold deGuzman
Filer Authorized By:	Stephen Radcliff Uriarte
Attorney Docket Number:	6005.042
Receipt Date:	07-OCT-2014
Filing Date:	04-SEP-2010
Time Stamp:	23:30:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 1160
RAM confirmation Number	6567
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
-----------------	----------------------	-----------	-------------------------------------	------------------	------------------

1	Response After Final Action	6005_042_AF_Response.pdf	95681	no	34
			2312d7c73d925bb9992823d64bca21adf426d371		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	31976	no	2
			c117a7f63db879472530e4b13c445d62584aa273		
Warnings:					
Information:					
Total Files Size (in bytes):			127657		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/876,113	Filing Date 09/04/2010	☐ To be Mailed
---	---	----------------------------------	---------------------------------------

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO**APPLICATION AS FILED – PART I**

(Column 1)

(Column 2)

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	10/07/2014	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 101	Minus	** 97	= 4	X \$40 =	160
	Independent (37 CFR 1.16(h))	* 8	Minus	***5	= 3	X \$210 =	630
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
TOTAL ADD'L FEE						790	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
TOTAL ADD'L FEE						

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/BRENDA HINES/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/876,113	09/04/2010	Ricardo H. BRUCE	6005.042	1607
64180	7590	10/16/2014		
URIARTE LAW Attn: Stephen R. Uriarte 2021 The Alameda Suite 225 San Jose, CA 95126			EXAMINER RUTZ, JARED IAN	
			ART UNIT 2133	PAPER NUMBER
			NOTIFICATION DATE 10/16/2014	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

stephen@uriartelaw.com
labid@uriartelaw.com
arnold@uriartelaw.com

Advisory Action Before the Filing of an Appeal Brief	Application No. 12/876,113	Applicant(s) BRUCE ET AL.	
	Examiner JARED RUTZ	Art Unit 2133	AIA (First Inventor to File) Status No

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 07 October 2014 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

NO NOTICE OF APPEAL FILED

1. ☒ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance;
 (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection. The current period for reply expires _____ months from the mailing date of the prior Advisory Action or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.

Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANT'S FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because

a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);

b) ☐ They raise the issue of new matter (see NOTE below);

c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

d) ☒ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: See Continuation Sheet. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).

5. ☐ Applicant's reply has overcome the following rejection(s): _____.

6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

7. ☒ For purposes of appeal, the proposed amendment(s): (a) ☒ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

9. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).

10. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

11. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

12. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.

13. ☐ Note the attached Information *Disclosure Statement(s)*. (PTO/SB/08) Paper No(s). _____

14. ☐ Other: _____.

STATUS OF CLAIMS

15. The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: _____.

Claim(s) objected to: _____.

Claim(s) rejected: 1-97.

Claim(s) withdrawn from consideration: _____.

/JARED RUTZ/ Supervisory Patent Examiner, Art Unit 2133	Jared I Rutz SPE
--	---------------------

Continuation of 3. NOTE: The proposed amendment also attempts to add claims 98-101 without cancelling a corresponding number of independent claims. With respect to Applicant's proposed amendments, The examiner notes that figures 4A and 4B show a host coupled to a controller by a communication path as recited in claims 1, 49, 59, and 80. Further, the Examiner notes that independent claim 29 does not include limitations commensurate in scope with those argued with respect to claim 1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	) Confirmation No.: 1607
Ricardo H. Bruce, et al.	)
	) Examiner: Jared Ian Rutz
Serial No.: 12/876,113	) Ph: 571-272-5535
	)
Filing Date: Sept. 4, 2010	) Art Unit: 2187
	)
Title: Multi-Profile Memory	) Atty. Docket No.: 6005.042
Controller For Computing	)
Devices	)
	)

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**RESPONSE TO FINAL OFFICE ACTION
AND AMENDMENT**

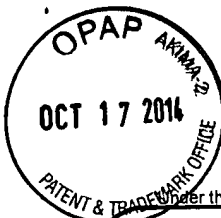
Dear Sir:

The following is in response to the final office
action mailed on 11 July 2013.

Amendments to the Claims are reflected in the listing of
claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 27 of this paper.

DO NOT ENTER: //J.R./



15m
RCE

PTO/SB/30 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

**Request
for
Continued Examination (RCE)
Transmittal**

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. **Submission required under 37 CFR 1.114** Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).
- a. ☒ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.
- i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ii. ☒ Other Response After Final Office Action (filed in USPTO on 07 October 2014)
- b. ☐ Enclosed
- i. ☐ Amendment/Reply
- iii. ☐ Information Disclosure Statement (IDS)
- ii. ☐ Affidavit(s)/ Declaration(s)
- iv. ☐ Other _____
2. **Miscellaneous**
- a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)
- b. ☐ Other _____
3. **Fees** The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
- The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to
- a. ☐ Deposit Account No. _____
- i. ☐ RCE fee required under 37 CFR 1.17(e)
- ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)
- iii. ☐ Other _____
- b. ☐ Check in the amount of \$ _____ enclosed
- c. ☒ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature		Date	14 October 2014
Name (Print/Type)	Arnold de Guzman	Registration No.	39,955

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature		Date	14 October 2014
Name (Print/Type)	Arnold de Guzman		

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

**TRANSMITTAL
FORM**

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

3

Application Number

12/876,113

Filing Date

September 4, 2010

First Named Inventor

Ricardo H. Bruce

Art Unit

2187

Examiner Name

Jared Ian Rutz

Attorney Docket Number

6005.042

ENCLOSURES (Check all that apply)

☐ Fee Transmittal Form	☐ Drawing(s)	☐ After Allowance Communication to TC
☐ Fee Attached	☐ Licensing-related Papers	☐ Appeal Communication to Board of Appeals and Interferences
☐ Amendment/Reply	☐ Petition	☐ Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
☐ After Final	☐ Petition to Convert to a Provisional Application	☐ Proprietary Information
☐ Affidavits/declaration(s)	☐ Power of Attorney, Revocation	☐ Status Letter
☐ Extension of Time Request	☐ Change of Correspondence Address	☒ Other Enclosure(s) (please identify below):
☐ Express Abandonment Request	☐ Terminal Disclaimer	return receipt postcard; signed/dated PTO-2038 authorizing payment of \$1700 (1 page); RCE (1 page)
☐ Information Disclosure Statement	☐ Request for Refund	
☐ Certified Copy of Priority Document(s)	☐ CD, Number of CD(s) _____	
☐ Reply to Missing Parts/Incomplete Application	☐ Landscape Table on CD	
☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53	☐ Remarks	

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name			
Signature			
Printed name	Arnold de Guzman		
Date	14 October 2014	Reg. No.	39,955

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature			
Typed or printed name	Arnold de Guzman	Date	14 October 2014

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 5,737,742	04-07-1998	Achiwa et al.	
		US- 5,802,554	09-01-1998	Caceres et al.	
		US- 5,819,307	10-06-1998	Iwamoto et al.	
		US- 2002/0141244	10-03-2002	Bruce et al.	
		US- 2009/0094411	04-09-2009	Que, Jinzhen	
		US- 2007/0130439	06-07-2007	Andersson et al.	
		US- 7,660,941	02-09-2010	Lee et al.	
		US- 5,644,784	07-01-1997	Peek	
		US- 2009/0158085	06-18-2009	Kern et al.	
		US- 2009/0172466	07-02-2009	Royer et al.	
		US- 2009/0172250	07-02-2009	Allen et al.	
		US- 2011/0264884	10-27-2011	Kim, Sung-joo	
		US- 8,713,417	04-29-014	Jo, Namphil	
		US- 8,510,631	08-13-2013	Wu et al.	
		US- 8,375,257	02-12-2013	Hong et al.	
		US- 8,707,134	04-22-2014	Takahashi et al.	
		US- 7,174,438	02-06-2007	Homma et al.	
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				

Examiner
SignatureDate
Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND**

TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known	
		Application Number	12/876,113
		Filing Date	September 4, 2010
		First Named Inventor	Ricardo H. Bruce
		Art Unit	2187
		Examiner Name	Jared Ian Rutz
Sheet 2	of 2	Attorney Docket Number	6005.042

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Office Action for U.S. Application No. 13/253,912 mailed on 16 July 2014.	
		Office Action for U.S. Application No. 13/475,878 mailed on 23 June 2014.	
		Office Action for U.S. Application No. 12/876,113 mailed on 11 July 2014.	
		Office Action for U.S. Application No. 12/876,113 mailed on 16 October 2014.	
		Notice of Allowance for U.S. Application No. 12/270,626 mailed 03 October 2014.	
		Notice of Allowance for U.S. Application No. 14/038,684 mailed 03 November 2014.	

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO:**

Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	20599912
Application Number:	12876113
International Application Number:	
Confirmation Number:	1607
Title of Invention:	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES
First Named Inventor/Applicant Name:	Ricardo H. BRUCE
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte/Arnold deGuzman
Filer Authorized By:	Stephen Radcliff Uriarte
Attorney Docket Number:	6005.042
Receipt Date:	04-NOV-2014
Filing Date:	04-SEP-2010
Time Stamp:	12:56:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	6005_042_IDS_transmittal_letter.pdf	24013 566feff2fde2fa0c92471545e4539c7556eec05f	no	3

Warnings:

Information:

2	Information Disclosure Statement (IDS) Form (SB08)	sb0008a_1.pdf	287994 7dcb584155aef7a82b23e01c89941b7ecf11b4e2	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Information Disclosure Statement (IDS) Form (SB08)	sb0008b_1.pdf	327394 ba924eb1cb6445f47c30403a5d5bec4877329b53	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
Total Files Size (in bytes):			639401		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	) Confirmation No.: 1607
Ricardo H. Bruce, et al.	)
	) Examiner: Jared Ian Rutz
Serial No.: 12/876,113	) Ph: 571-272-5535
	)
Filing Date: Sept. 4, 2010	) Art Unit: 2187
	)
Title: MULTI-PROFILE MEMORY	) Atty. Docket No.: 6005.042
CONTROLLER FOR COMPUTING	) Customer No. 64180
DEVICES	)
	)
	)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT TRANSMITTAL LETTER

Dear Sir:

Applicant respectfully requests the Office to consider the following Information Disclosure Statement being filed herewith.

Filing of Information Disclosure Statement Under 37 C.F.R. 1.56, 37 C.F.R. 1.97, and 37 C.F.R. 1.98

Pursuant to the provisions of 37 CFR 1.56, 37 CFR 1.97, and 37 C.F.R. 1.98, enclosed herewith is form PTO/SB/08 listing references which may be material to the examination of this application, and with respect to which there may be a duty to disclose. The filing of this Information Disclosure Statement shall not be construed as a representation regarding the completeness of the list of

references, or that inclusion of a reference in this list is an admission that it is prior art or is pertinent to this application, or that a search has been made, or as an admission that the information listed is, or may be considered to be, material to patentability, or that no other material information exists, and shall not be construed as an admission against interest in any manner.

A copy of each listed reference is enclosed herewith, unless no such copy is required pursuant to 37 CFR 1.98(d).

Pursuant to 37 CFR 1.97, this Information Disclosure Statement is being submitted under the following section: 37 CFR 1.97(b)(4). An information disclosure statement shall be considered by the Office if filed by the applicant within any one of the following time periods: Before the mailing of a first office action after the filing of a request for continued examination under section 1.114.

Consideration of the listed references and favorable action are respectfully solicited.

Conclusion

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (805) 569-1600

Date: 04 November 2014

Respectfully submitted,

_____/Arnold de Guzman/_____
 Arnold de Guzman
 Attorney for Applicant(s)
 Reg. No. 39,955

Please send correspondence to:
 Customer No. 64180

CERTIFICATE OF TRANSMISSION OR MAILING			
37 C.F.R. 1.8			
I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office in accordance with 37 C.F.R. § 1.6(d), or is being transmitted via the Office electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4), or is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below:			
Signature:	/Arnold de Guzman/		
Typed or Printed Name:	Arnold de Guzman	Dated:	04 November 2014
Express Mail Mailing Number (optional):			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 2003/0163624 A1	08-28-2003	Matsui et al.	
		US- 2007/0028040 A1	02-01-2007	Alan Welsh Sinclair	
		US- 2006/0095709 A1	05-04-2006	Kyosuke Achiwa	
		US- 20110113186	05-12-2011	Bruce et al.	
		US-			
		US- 20110202709	08-18-2011	Rychlik, Bohuslav	
		US- 8,447,908	04-21-2013	Bruce et al.	
		US- 8,788,725	07-22-2014	Bruce et al.	
		US- 8,560,804	10-15-2013	Bruce et al.	
		US- 2013/0246694	09-19-2013	Bruce et al.	
		US- 2011/0161568	06-30-2011	Bruce et al.	
		US- 2002/0083262	06-27-2002	Fukuzumi, Tomoya	
		US- 2009/0158085	06-18-2009	Kern et al.	
		US- 2009/0172466	07-02-2009	Royer et al.	
		US- 2009/0172250	07-02-2009	Allen et al.	
		US- 2011/0264884	10-27-2011	Sung-joo Kim	
		US- 2014/0104949	04-17-2014	Bruce et al.	
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				

Examiner
SignatureDate
Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT***(Use as many sheets as necessary)***Complete if Known**

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

Sheet 2 of 2

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Notice of Allowance/Allowability for U.S. Application No. 14/038,684 for 01 August 2014.	
		Office Action for U.S. Application No. 14/038,684 mailed on 17 March 2014.	
		Notice of Allowance/Allowability for U.S. Application No. 13/890,229 mailed on 20 February 2014.	
		Office Action for U.S. Application No. 12/270,626 mailed on 23 May 2014.	

Examiner
SignatureDate
Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO:**

Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	20722374
Application Number:	12876113
International Application Number:	
Confirmation Number:	1607
Title of Invention:	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES
First Named Inventor/Applicant Name:	Ricardo H. BRUCE
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte/Arnold deGuzman
Filer Authorized By:	Stephen Radcliff Uriarte
Attorney Docket Number:	6005.042
Receipt Date:	17-NOV-2014
Filing Date:	04-SEP-2010
Time Stamp:	20:34:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	6005_042_IDS_transmittal_letter2.pdf	24011 c0f9b26abd0de8d33769e60eba45c9e55b0649de	no	3

Warnings:

Information:

2	Information Disclosure Statement (IDS) Form (SB08)	sb0008a_1.pdf	287704 060029a54ce375ed488cdc5bb3aed99ef926ae08	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Information Disclosure Statement (IDS) Form (SB08)	sb0008b_1.pdf	326859 b850ff70ff81dc46a58c47246bb5379789465819	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
Total Files Size (in bytes):				638574	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	) Confirmation No.: 1607
Ricardo H. Bruce, et al.	)
	) Examiner: Jared Ian Rutz
Serial No.: 12/876,113	) Ph: 571-272-5535
	)
Filing Date: Sept. 4, 2010	) Art Unit: 2187
	)
Title: MULTI-PROFILE MEMORY	) Atty. Docket No.: 6005.042
CONTROLLER FOR COMPUTING	) Customer No. 64180
DEVICES	)
	)
	)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT TRANSMITTAL LETTER

Dear Sir:

Applicant respectfully requests the Office to consider the following Information Disclosure Statement being filed herewith.

Filing of Information Disclosure Statement Under 37 C.F.R. 1.56, 37 C.F.R. 1.97, and 37 C.F.R. 1.98

Pursuant to the provisions of 37 CFR 1.56, 37 CFR 1.97, and 37 C.F.R. 1.98, enclosed herewith is form PTO/SB/08 listing references which may be material to the examination of this application, and with respect to which there may be a duty to disclose. The filing of this Information Disclosure Statement shall not be construed as a representation regarding the completeness of the list of

references, or that inclusion of a reference in this list is an admission that it is prior art or is pertinent to this application, or that a search has been made, or as an admission that the information listed is, or may be considered to be, material to patentability, or that no other material information exists, and shall not be construed as an admission against interest in any manner.

A copy of each listed reference is enclosed herewith, unless no such copy is required pursuant to 37 CFR 1.98(d).

Pursuant to 37 CFR 1.97, this Information Disclosure Statement is being submitted under the following section: 37 CFR 1.97(b)(4). An information disclosure statement shall be considered by the Office if filed by the applicant within any one of the following time periods: Before the mailing of a first office action after the filing of a request for continued examination under section 1.114.

Consideration of the listed references and favorable action are respectfully solicited.

Conclusion

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (805) 569-1600

Date: 17 November 2014

Respectfully submitted,

_____/Arnold de Guzman/_____
 Arnold de Guzman
 Attorney for Applicant(s)
 Reg. No. 39,955

Please send correspondence to:
 Customer No. 64180

CERTIFICATE OF TRANSMISSION OR MAILING			
37 C.F.R. 1.8			
I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office in accordance with 37 C.F.R. § 1.6(d), or is being transmitted via the Office electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4), or is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below:			
Signature:	/Arnold de Guzman/		
Typed or Printed Name:	Arnold de Guzman	Dated:	17 November 2014
Express Mail Mailing Number (optional):			



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/876,113	09/04/2010	Ricardo H. BRUCE	6005.042	1607
64180	7590	12/05/2014		
URIARTE LAW Attn: Stephen R. Uriarte 2021 The Alameda Suite 225 San Jose, CA 95126			EXAMINER EDOUARD, JEAN C	
			ART UNIT	PAPER NUMBER
			2133	
			NOTIFICATION DATE	DELIVERY MODE
			12/05/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

stephen@uriartelaw.com
labid@uriartelaw.com
arnold@uriartelaw.com

Office Action Summary	Application No. 12/876,113	Applicant(s) BRUCE ET AL.	
	Examiner JEAN EDOUARD	Art Unit 2133	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10/17/2014.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-101 is/are pending in the application.
5a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) _____ is/are allowed.
- 7) ☒ Claim(s) 1-101 is/are rejected.
- 8) ☐ Claim(s) _____ is/are objected to.
- 9) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 09/04/2010 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date 11/17/2014, 11/04/2014
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 4) ☐ Other: _____

Art Unit: 2133

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

The present application is being examined under the pre-AIA first to invent provisions

Claims 1-101 are presented for examination.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/17/2014 has been entered.

4. Response to Arguments

5. Applicant's arguments filed on 10/07/2014 have been fully considered but they are not persuasive. Applicant argues on pages 2-3 in regards to claim 1, that "Falik does not all the limitation of claim 1"

Examiner respectfully disagrees. Estakhri is relied upon for that limitations. Falik teaches *first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and*

Art Unit: 2133

second device profiles. Col. 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

Claim Rejections - 35 USC § 112

4. The following is a quotation of 35 U.S.C. 112(b):
(b) CONCLUSION—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 100 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Regarding claim 100; the citation “the host” lacks antecedent basis.

Subsequently, claim 101 are also rejected because they inherit the deficiencies stated above.

Art Unit: 2133

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. **Claims 1-14, 20, 21, 25, 45-60, 69-92 and 94-101** are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri et al. (U.S. Pub. 20110167204) in view of Falik et al. (US 8,200,879).

Claim 1 is taught by Estakri as:

A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising: addressing a first memory location in a first memory device in a memory store. Estakri fig. 3 mass storage device 302 contains a volatile memory 100 with multiple locations and a non-volatile memory 104 with multiple locations and paragraph [0039]-[0041] wherein memory location are being addressed.

said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Estakri paragraph [0038]-[0040] a first memory location and a second memory location associated with multiple device profile

Art Unit: 2133

Wherein said second memory location is in a second memory device in the memory store. Estakri fig. 1-2 and paragraph [0032], [0037]-[0038] shows non-volatile memory 104 with multiple locations in the mass storage device 302. Wherein a memory read transaction or a memory write transaction is performed on at least one of the first memory location or second memory location. Estakri paragraph [0020], [0039]-[0040] shows memory read transaction is performed in the non-volatile memory 104 by controller 304.

wherein data is transferred to the first memory location or second memory location from a host for a memory write transaction. Estakri fig. 3 and paragraph [0036], [0041] shows data is transferred from the external signal system which is equivalent to a host to the volatile 100 and the non-volatile memory 104 via the controller and interfaces 140, 306 and 308 for a memory write transaction. wherein data is transferred from the first memory location or second memory location to the host for a memory read transaction. Estakri fig. 3 and paragraph [0039]-[0041] shows data is transferred from the external signal system which is equivalent to a host to the volatile 100 and the non-volatile memory 104 via the controller and interfaces 140, 306 and 308 for a memory read transaction.

Wherein the memory store is directly coupled to at least one memory bus and wherein the at least one memory bus is directly coupled to a controller, and wherein the controller performs the memory read transaction and memory write transaction on the memory store. Estakhri fig. 3 shows the volatile memory 100 connects to controller 304

Art Unit: 2133

via bus 140 and paragraph [0010], [0036], [0040] wherein controller 304 interacts in read and write transactions in the memory.

Wherein the host is directly coupled to the controller by a communication path as the controller performs the memory read transaction or memory write transaction; Estakhri fig. 3 shows the external digital signal 300 which is equivalent to host connects directly to controller 304 via interface 306 and 308 and the controller also connects to volatile memory 100 and nonvolatile memory 104 via interface 140 to perform read and write transaction.

Estakri does not explicitly teach Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location. Wherein the first device profile and second device profile are each stored in the memory store. And using attributes from said first and second device profiles.

However, Falik teaches Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Col. 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-

Art Unit: 2133

45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

Wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location. Column 20 line 49 through column 21 line 15 shows that the section properties register stores values representing the section of the flash device, and that there is a section properties register for each section of the flash device.

Wherein the first device profile and second device profile are each stored in the memory store. Column 18 lines 53-64 show that the control, status and capabilities registers 12 and 112 are located on the flash device, and can be kept in the flash device's own memory.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Falik does not explicitly teach Wherein the memory store is directly coupled to at least one memory bus and wherein the at least one memory bus is directly coupled to a controller, and wherein the controller performs the memory read transaction and memory write transaction on the memory store. Wherein the host is directly coupled to the controller by a communication path as the controller performs the memory read transaction or memory write transaction.

It would have been obvious to one of an ordinary skill in the art at the time the invention was made to have incorporated the teaching of *Said first device profile representing a first set of attributes of said first memory location, and said second*

Art Unit: 2133

device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location. Wherein the first device profile and second device profile are each stored in the memory store. And using attributes from said first and second device profiles as suggested in Falik into Estakhri's system because both of the system are addressing the need of managing and controlling the access to memory locations, and by incorporating the teaching of Falik into Estakhri would perform the benefit of avoiding program buffer being full by using the double buffer empty status bit in the device status and control register (Falik paragraph [0134].

Claim 2 is taught by Estakhri and Falik as:

The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device. Col. 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 3 is taught by Estakhri and Falik as:

The method of claim 1, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when

Art Unit: 2133

different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

And said addressing said first memory location is made in response to a first memory transaction request. Column 18 lines 24-34 shows that applications on the main die 100 issue read and program commands.

And further including addressing said second memory location. Figure 6 shows that both sections can be addressed.

Claim 4 is taught by Estakhri and Falik as:

The method of claim 1, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 5 is taught by Estakhri and Falik as:

Art Unit: 2133

The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 6 is taught by Estakhri and Falik as:

The method of claim 5, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 7 is taught by Estakhri and Falik as:

The method of claim 5, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 8 is taught by Estakhri and Falik as:

The method of claim 5, wherein said shared attributes include a memory device type attribute. Column 20 lines 30-36 shows that the registers can indicate if the device is self-timed type flash memory or not.

Claim 9 is taught by Estakhri and Falik as:

Art Unit: 2133

The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 10 is taught by Estakhri and Falik as:

The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 11 is taught by Estakhri and Falik as:

The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 12 is taught by Estakhri and Falik as:

Art Unit: 2133

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 13 is taught by Estakhri and Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of attributes that differs in value from a second page size attribute from said second set of attributes. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 14 is taught by Estakhri and Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes. Column 19 lines 56-59 shows that the Bus Widths

Art Unit: 2133

Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 20 is taught by Estakhri and Falik as:

The method of claim 2, further including: using an address corresponding to a memory location from said first memory device and transferring a first data set. Column 16 lines 53-62 shows that an address and data are sent for a programming operation.

And using an address corresponding to a memory location from said second memory device and transferring a second data set. Column 14 lines 51-65 show that the standard address space is mapped to the logical sections into which the arrays are grouped, showing that the second memory device is accessed using an address corresponding to the second memory device.

Claim 21 is taught by Estakhri and Falik as:

The method of claim 20, wherein: said first set of attributes includes a first page size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

And said first data set includes a first data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

Art Unit: 2133

And if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size. Column 27 lines 9-24 shows that when the number of bytes to be transferred to the FD have been transferred, the transfer process ends by setting the bus to a HiZ state.

Claim 25 is taught by Estakhri and Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size attribute of said first memory device. As discussed at column 27 lines 33-60, the program buffer corresponds to the batch size, which is the amount of data which can be programmed into the flash array at once.

Claim 45 is taught by Falik as:

A memory controller for performing memory transactions, said memory controller comprising: a means for addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that

Art Unit: 2133

arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Wherein said means for addressing includes an interface controller means for processing memory transaction requests. Figure 4B, flash bus transactions state machine 116.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Col. 20 line 49 through col. 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And said means for addressing uses attributes from said first and second device profiles. Col. 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Falik does not explicitly teach Said means for addressing is directly coupled to the first memory location and second memory location; Said means for addressing is directly coupled to a host as said means for addressing addresses the first memory location or second memory location.

However, Estakhri teaches Said means for addressing is directly coupled to the first memory location and second memory location; estakri fig. 3 paragraph [0033],

Art Unit: 2133

[0039], [0054] shows the controller 304, for addressing is connected directly to volatile memory 100 and nonvolatile memory 104 via interface 140.

Said means for addressing is directly coupled to a host as said means for addressing addresses the first memory location or second memory location. Estakhri fig. 3 and paragraph [0033], [0040]-[0041] shows controller 304 connects directly to external digital signal (host) via interface 306 and 308 wherein volatile memory 100 and nonvolatile memory 104 are addressable by the controller via interface 140.

It would have been obvious to one of an ordinary skill in the art at the time the invention was made to have incorporated the teaching of *Said means for addressing is directly coupled to the first memory location and second memory location*; Said means for addressing is directly coupled to a host as said means for addressing addresses the first memory location or second memory location as suggested in Estakhri into Talik's system because both of the system are addressing the need of managing and controlling the access to memory locations, and by incorporating the teaching of Talik into Estakhri would improve the performance system (Estakhri et al, paragraph [0051])).

Claim 46 is taught by Estakhri and Falik as:

The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second

Art Unit: 2133

memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 47 is taught by Estakhri and Falik as:

The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 48 is taught by Estakhri and Falik as:

The memory controller of claim 46, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said use of said attributes from said first and second device profiles by said means for addressing includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 49 is taught by Estakhri and Falik as:

The memory controller of claim 46, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 50 is taught by Estakhri and Falik as:

The memory controller of claim 45, wherein said means for addressing further includes a means for addressing said second memory location. Figure 6 shows that both sections can be addressed.

Claim 51 is taught by Estakhri and Falik as:

The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 52 is taught by Estakhri and Falik as:

The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths

Art Unit: 2133

Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 53 is taught by Estakhri and Falik as:

The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 54 is taught by Estakhri and Falik as:

The memory controller of claim 51, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 55 is taught by Estakhri and Falik as:

The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 56 is taught by Estakhri and Falik as:

Art Unit: 2133

The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 57 is taught by Estakhri and Falik as:

The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 58 is taught by Estakhri and Falik as:

The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

Claim 59 is taught by Estakri as:

A memory store. Estakri fig. 3 storage device 302.

Art Unit: 2133

teaches wherein the memory device interface is directly coupled to the memory store. See Estakhri fig. 3 controller 304 connected directly memory 100 via interface 140.

Estakri does not explicitly teach a memory controller comprising: an interface controller coupled to a memory device interface and an input/output (IO) device interface. Said interface controller disposed to perform a memory transaction by addressing a first memory location in a first memory device in the memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Said addressing of said first memory location includes using said attributes from said first device profile.

However, Falik teaches a memory controller comprising: an interface controller coupled to a memory device interface and an input/output (IO) device interface. Figure 4B shows interface controller 110 connected to bus 90 and internal bus 140.

Wherein the memory device interface is directly coupled to the memory store. See Estakhri fig. 3 controller 304 connected directly memory 100 via interface 140.

Said interface controller disposed to perform a memory transaction by addressing a first memory location in a first memory device in the memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory

Art Unit: 2133

location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

Said addressing of said first memory location includes using said attributes from said first device profile. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

It would have been obvious to one of an ordinary skill in the art at the time the invention was made to have incorporated the teaching of *a memory controller comprising: an interface controller coupled to a memory device interface and an input/output (IO) device interface. Said interface controller disposed to perform a memory transaction by addressing a first memory location in a first memory device in*

Art Unit: 2133

the memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Said addressing of said first memory location includes using said attributes from said first device profile as suggested in Falik into Estakhri's system because both of the system are addressing the need of managing and controlling the access to memory locations, and by incorporating the teaching of Talik into Estakhri would perform the benefit of reducing overall time for finishing a flash programming task (Falik paragraph [0082]).

Claim 60 is taught by Estakhri and Falik as:

The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile. Figure 6 shows that both sections can be addressed.

Claim 69 is taught by Estakhri and Falik as:

The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

Claim 70 is taught by Estakhri and Falik as:

The memory controller of claim 59, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 71 is taught by Estakhri and Falik as:

The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 72 is taught by Estakhri and Falik as:

The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that

Art Unit: 2133

Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 73 is taught by Estakhri and Falik as:

The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 74 is taught by Estakhri and Falik as:

The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 75 is taught by Estakhri and Falik as:

The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type.

Art Unit: 2133

Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 76 is taught by Estakhri and Falik as:

The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 77 is taught by Estakhri and Falik as:

The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 78 is taught by Estakhri and Falik as:

The memory controller of claim 71, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 79 is taught by Estakhri and Falik as:

Art Unit: 2133

The memory controller of claim 71, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 80 is taught by Estakhri as:

a memory controller directly coupled to and disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile. Estakhri fig. 1, 3 and paragraph [0033], [0036], [0054] shows controller 304 connects directly to memory 100 for addressing and wherein memory 100 contains multiple locations.

Said memory controller directly coupled to a host as said memory controller addresses the first memory location or second memory location. Estakhri fig. 3 and paragraph [0033], [0041], [0094] shows controller 304 directly coupled to memory 100 for addressing and wherein memory 100 has multiple locations.

Estakhri does not explicitly teach *an electronic storage device, comprising: Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Said memory controller using attributes from said first and second device profiles.*

However, Falik teaches an electronic storage device, comprising: Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

Said memory controller using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

It would have been obvious to one of an ordinary skill in the art at the time the invention was made to have incorporated the teaching of *an electronic storage device, comprising: Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Said memory controller using attributes from said first and second device profiles* as suggested in Falik into Estakhri's system because both of the system are addressing the need of managing and controlling the access to memory locations, and by incorporating the teaching of Talik into Estakhri would perform the benefit of reducing overall time for finishing a flash programming task (Falik paragraph [0082]).

Art Unit: 2133

Claim 81 is taught by Estakhri and Falik as:

The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command. Column 9 lines 5-18 shows that the interface performs appropriate requests for erasure.

Claim 82 is taught by Estakhri and Falik as:

The electronic storage device of claim 80, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 83 is taught by Estakhri and Falik as:

The electronic storage device of claim 80, said memory controller further disposed to: perform a write operation on said first memory device, if a memory transaction request is associated with a write request. Column 16 lines 53-64 shows that write transactions may be performed.

Perform a read operation on said first memory device, if said memory transaction request is associated with a read request. Column 16 lines 53-64 shows that read transactions may be performed.

Art Unit: 2133

And wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using said second device profile in response to receiving a second memory transaction request.

Column 19 line 4 through column 22 line 15 discuss how the different attributes are used for accesses to the groups of memory arrays.

Claim 84 is taught by Estakhri and Falik as:

The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 85 is taught by Estakhri and Falik as:

The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 86 is taught by Estakhri and Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that

Art Unit: 2133

Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 87 is taught by Estakhri and Falik as:

The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 88 is taught by Estakhri and Falik as:

The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 89 is taught by Estakhri and Falik as:

The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

Claim 90 is taught by Estakhri and Falik as:

Art Unit: 2133

The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 91 is taught by Estakhri and Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 92 is taught by Estakhri and Falik as:

The electronic storage device of claim 84, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 94 is taught by Estakhri and Falik as:

Art Unit: 2133

The method of claim 1, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 95 is taught by Estakhri and Falik as:

The memory controller of claim 45, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 96 is taught by Estakhri and Falik as:

The memory controller of claim 59, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Art Unit: 2133

Claim 97 is taught by Estakhri and Falik as:

The electronic device of claim 80, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 98 is taught by Estakhri as:

teaches a memory controller directly coupled to and disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile. Estakhri fig. 1, 3 and paragraph [0033], [0036], [0054] shows controller 304 connects directly to memory 100 for addressing and wherein memory 100 contains multiple locations.

Wherein the memory controller directly coupled to a host as said memory controller addresses the first memory location or second memory location. Estakhri fig. 3 and paragraph [0033], [0041], [0094] shows controller 304 directly coupled to memory 100 for addressing and wherein memory 100 has multiple locations.

Estakhri does not explicitly teach an electronic storage device, comprising:

The first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device

Art Unit: 2133

profiles. And wherein Said memory controller using attributes from said first and second device profiles.

However, Falik teaches an electronic storage device, comprising:

The first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And wherein Said memory controller using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

It would have been obvious to one of an ordinary skill in the art at the time the invention was made to have incorporated the teaching of *a memory controller directly coupled to and disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile. Said memory controller directly coupled to a host as said memory controller addresses the first memory location or second memory location* as suggested in Estakhri into Falik's system because both of the system are addressing the need of managing and controlling the access to memory locations, and by incorporating the

Art Unit: 2133

teaching of Falik into Estakhri would perform the benefit of reducing overall time for finishing a flash programming task (Falik paragraph [0082]).

Claim 99 is taught by Estakhri and Falik as:

The electronic device of claim 98, wherein the memory controller comprises: an interface controller. Falik interface controller 110;

A memory controller comprising: an interface controller coupled to a memory device interface and an input/output (IO) device interface. Figure 4B shows interface controller 110 connected to bus 90 and internal bus 140.

A memory store. Falik fig. 4A flash memory 70, wherein the memory device interface is directly coupled to the memory store. Falik fig. 4A-4B bus 90 interacts with flash memory 70

Said interface controller disposed to perform a memory transaction by addressing a first memory location in a first memory device in the memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having

Art Unit: 2133

identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

Said addressing of said first memory location includes using said attributes from said first device profile. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 100 is taught by Estakhri as:

*A method of performing memory transactions, the method comprising:
addressing a first memory location in a first memory device in a memory store. Estakri fig. 3 mass storage device 302 contains a volatile memory 100 with multiple locations and a non-volatile memory 104 with multiple locations and paragraph [0039]-[0041] wherein memory location are being addressed.*

Art Unit: 2133

Said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Estakri paragraph [0038]-[0040] a first memory location and a second memory location associated with multiple device profile.

Wherein the host is directly coupled to a memory controller performs a memory r transaction. Estakhri fig. 3 and [0039]-[0041] shows the external digital signal 300 which is equivalent to host connects directly to controller 304 via interface 306 and 308 and the controller also connects to volatile memory 100 and nonvolatile memory 104 via interface 140 to perform transactions.

Estakhri does not explicitly teach *the first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location. And using attributes from said first and second device profiles.*

However, Falik teaches the first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location. Col. 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

It would have been obvious to one of an ordinary skill in the art at the time the invention was made to have incorporated the teaching of *the first device profile*

Art Unit: 2133

representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location. And using attributes from said first and second device profiles as suggested in Falik into Estakhri's system because both of the system are addressing the need of managing and controlling the access to memory locations, and by incorporating the teaching of Talik into Estakhri would perform the benefit of reducing overall time for finishing a flash programming task (Falik paragraph [0082]).

Claim 101 is taught by Falik and Estakhri as:

The method of claim 100, wherein the memory controller comprises: an interface controller. Falik fig. 4B interface controller 110.

A memory device interface directly coupled to the first memory location and the second memory location and coupled to the interface controller. Falik fig. 4A-4B Bus interface 90 connects to interface controller 110 and the memory.

An input/output (IO) device interface coupled to the interface coupled to the interface controller. Falik fig. 4B bus 90 connects to interface controller 110; and directly coupled to the host as the memory controller addresses the first memory location or the second memory location. Estakhri fig. 3 and paragraph [0033], [0036], [0041] wherein bus 90 will connect directly to the external digital system (host) as controller 304 addresses.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. **Claims 15, 18, and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri et al. (U.S. 20110167204) in view of Falik et al. (US 8,200,879) in further view of Nangle (US 7,330,954).

Claim 15 is taught by Estakhri and Falik as:

The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device. Column 21 lines 7-10 shows that the information can correspond to a flash device FD.

Although Falik column 21 lines 7-10 shows that other memory technologies such as SRAM may be used, it does not expressly teach that the second memory device attribute corresponds to a DRAM device interface.

With respect to claim 15, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 lines 51-67 shows that the memory devices may be flash memory and DRAM.

Art Unit: 2133

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include flash memory and DRAM in the system of Falik.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 15**.

Claim 18 is taught by Estakhri and Falik as shown supra with respect to claim 8.

Falik does not expressly teach that said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

With respect to claim 18, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 line 51 through column 5 line 4 shows that the memory devices may be volatile memory that have a battery backup.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a volatile memory disposed to receive backup power from a portable power source.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Art Unit: 2133

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 18**.

Claim 19 is taught by Estakhri and Falik as shown supra with respect to claim 8.

Estakhri and Falik does not expressly teach that said first memory device type attribute corresponds to a NAND flash memory device and said second memory device type attribute corresponds to a NOR flash memory device.

With respect to claim 19, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 lines 51-65 shows that the memory devices may be NAND or NOR type flash memories.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a volatile memory disposed to receive backup power from a portable power source.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 19**.

Art Unit: 2133

9. **Claims 16, 17, 22-24, and 93** are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri et al. (U.S. 20110167204) in view of Falik et al. (US 8,200,879) in further view of Sinclair et al. (US 2006/0184723).

Claim 16 if taught by Estakhri and Falik as shown supra with respect to claim 2.

Although Falik teaches that the width of the array is the minimum programming size of the array at column 20 lines 62-65, and that the width of the array is stored at column 20 lines 49-52, Falik does not expressly teach that a first and second partial page size attribute is stored and used.

With respect to claim 16, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claims 16 and 17**.

Claim 17 is taught by Estakhri, Falik and Sinclair as:

The method of claim 16: said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute. Sinclair paragraph 0168 shows that in a flash memory that supports partial page programming, when sufficient data is transferred to the buffer, it is programmed to the page. Falik column 14 lines 51-60 and figure 3 shows that the first memory device group can be accessed.

And further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute. Sinclair paragraph 0168 shows that in a flash memory that supports partial page programming, when sufficient data is transferred to the buffer, it is programmed to the page. Falik column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

Claim 22 is taught by Estakhri and Falik as:

The method of claim 20, wherein: said second set of attributes includes a second page size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Art Unit: 2133

And said second data set includes a second data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

And if said second data set size is greater than said second page size attribute, said transferring said second data set includes: performing a set of write operations on said second memory device that includes using a second transfer size equal to said second page size attribute. Column 16 lines 48-52 shows that program buffer 19 may be a double buffer, allowing the programming of one chunk of data while another chunk of data is received. As discussed at column 27 lines 33-60, the program buffer corresponds to the batch size, which is the amount of data which can be programmed into the flash array at once.

Falik does not expressly teach that the transaction is made using a transfer size equal to the page size until a remaining portion of said second data set that has not yet been written to said second device is less than said second page size attribute and using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

With respect to claim 22, Sinclair teaches Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times. As discussed in paragraph 0168, when the end of the data group is received in the buffer and it is smaller than a full page of data, a partial page programming operation may be performed.

Art Unit: 2133

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 22**.

Claim 23 is taught by Estakhri and Falik as:

The method of claim 20, wherein: said first set of attributes includes a page size attribute and a block size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Said first data set includes a first data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

If said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes: performing a set of write operations on

Art Unit: 2133

said first memory device that includes using a second transfer size equal to said page size attribute [...]. Column 27 lines 14-24 shows that bytes of data are sent until all the bytes have been sent.

Falik does not expressly teach that the transaction is made using a transfer size equal to the page size until a remaining portion of said first data set that has not yet been written to said first device is less than said first page size attribute and using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

With respect to claim 23, Sinclair teaches Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times. As discussed in paragraph 0168, when the end of the data group is received in the buffer and it is smaller than a full page of data, a partial page programming operation may be performed.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 23**.

Art Unit: 2133

Claim 24 is taught by Estakhri and Falik as shown supra with respect to claim 1, and further as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes: performing respective write operations on said first and second memory devices by at least using a transfer size at least equal to a [...] page size attribute from said first set of attributes. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations.

And performing at least one write operation on said second memory device by at least using a transfer size at least equal to a [...] page size attribute value from said second set of attributes. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations. Column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

And said attribute difference includes different attribute values of said first and second [...] page size attributes. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Although Estakhri and Falik teaches storing a page size attribute, it does not expressly teach storing a partial page size attribute.

Art Unit: 2133

With respect to claim 24, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 24**.

Claim 93 is taught by Estakhri and Falik as shown supra with respect to claim 80, and further as:

The electronic storage device of claim 80, wherein said memory controller is further adapted to: use a first partial page size attribute by performing a write operation on said first memory device and using a transfer size at least equal to said partial page size attribute. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations.

And use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute. Column 16 lines 53-62 shows that programming is carried out

Art Unit: 2133

in a block to be stored in sequentially increasing address locations. Column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

Although Estakhri and Falik teach storing a page size attribute, it does not expressly teach storing a partial page size attribute.

With respect to claim 93, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 93**.

10. **Claims 26-28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri et al. (U.S. 20110167204) in view of Falik et al. (US 8,200,879) in further view of Lakhani et al. (US 6,961,805).

Claim 26 is taught by Estakhri and Falik as shown supra with respect to claim 1.

Art Unit: 2133

Falik further teaches, at column 20 lines 60-65, that Page Size Block1 stores the size of the minimal segment of a flash array erasable upon a single erase command. Additionally, column 16 line 53 through column 17 line 24 shows that data can be written to a block of addresses by designating the starting address and performing a series of program continue operations.

Estakhri and Falik does not expressly teach using the block size attribute in performing a write operation that uses a transfer size that corresponds to the block size.

With respect to claim 26, Lakhani teaches, at column 18 lines 19-46, that predecoder 50 asserts sets of multiblock selection bits in response to control bits from the controller, which allows a designated number of blocks to be selected for writing at the same time.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to perform a write operation that uses a transfer size equal to the a block size attribute value that corresponds to a block size attribute of the first memory device.

The motivation for doing so would have been to reduce the time used to test the memory cells of the block, Lakhani column 8 lines 21-32.

Therefore, it would have been obvious to combine Lakhani with Falik to obtain the invention as specified in **claims 26 and 27**.

Claim 27 is taught by Lakhani as:

Art Unit: 2133

The method of claim 26, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value. Column 13 lines 25-38 shows that a plurality of blocks can be selected at the same time.

Claim 28 is taught by Falik as shown supra with respect to claim 2.

Falik further teaches, at column 20 lines 60-65, that Page Size Block1 stores the size of the minimal segment of a flash array erasable upon a single erase command. Additionally, column 16 line 53 through column 17 line 24 shows that data can be written to a block of addresses by designating the starting address and performing a series of program continue operations.

Falik does not expressly teach using the block size attribute in performing a write operation that uses a transfer size that is equal to a multiple of the block size.

With respect to claim 28, Lakhani teaches, at column 18 lines 19-46, that predecoder 50 asserts sets of multiblock selection bits in response to control bits from the controller, which allows a designated number of blocks to be selected for writing at the same time.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to perform a write operation that uses a transfer size equal to the a block size attribute value that corresponds to a block size attribute of the first memory device.

Art Unit: 2133

The motivation for doing so would have been to reduce the time used to test the memory cells of the block, Lakhani column 8 lines 21-32.

Therefore, it would have been obvious to combine Lakhani with Falik to obtain the invention as specified in **claim 28**.

11. **Claims 29-44** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Rubinstein et al. (US 5,913,215).

Claim 29 is taught by Falik as:

Said method comprising: addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Wherein said second memory location is in a second memory device in the memory store. Column 6 lines 11-16 shows that the different parameters

Art Unit: 2133

correspond to different memory arrays. Accordingly, the address corresponding to a different section may be in a second memory device.

Said first device profile representing a first set of attributes of said first memory device, and said second device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

Wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location. Column 20 line 49 through column 21 line 15 shows that the section properties register stores values representing the section of the flash device, and that there is a section properties register for each section of the flash device.

Wherein the memory store is coupled by at least one memory bus to a controller, and wherein the controller performs the memory transactions on the memory store. Figure 1 shows that main die interface controller connects to the flash die via bus 90, as discussed at column 10 lines 5-15. Column 27 lines 8-32 shows that the MD sends commands to the FD.

Wherein the first device profile and second device profile are each stored in the memory store. Column 18 lines 53-64 show that the control, status and

Art Unit: 2133

capabilities registers 12 and 112 are located on the flash device, and can be kept in the flash device's own memory.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Falik does not expressly teach that the methods may be implemented using a non-transitory computer readable medium comprising computer executable instructions.

With respect to claim 29, Rubinstein teaches at column 10, lines 3-15, that computer methods may be performed either by a series of instructions, or by specific hardware components that contain hard-wired logic for performing the method, or by any combination of the two.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a computer readable medium comprising computer executable instructions.

The rationale for doing so would have been that it is a known technique to implement methods in computer systems using a non-transitory computer readable medium comprising computer executable instructions.

Therefore, it would have been obvious to combine Rubinstein with Falik to obtain the invention as recited in **claims 29-44**.

Claim 30 is taught by Falik as:

The computer readable medium of claim 29, wherein: said first memory location is part of a memory space associated with a first memory device, said second memory

Art Unit: 2133

location is part of a memory space associated with a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

And said first and second memory devices comprise at least a portion of a memory store. Figure 3 shows that the address space is mapped to the memory devices.

Claim 31 is taught by Falik as:

The computer readable medium of claim 29, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of a first memory device and a block size value of a second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 32 is taught by Falik as:

The computer readable medium of claim 30, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 33 is taught by Falik as:

Art Unit: 2133

The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 34 is taught by Falik as:

The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

Claim 35 is taught by Falik as:

The computer readable medium of claim 29, wherein said addressing further includes: said first and second device profiles having at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40

Art Unit: 2133

shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 36 is taught by Falik as:

The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 37 is taught by Falik as:

The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 38 is taught by Falik as:

The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 39 is taught by Falik as:

Art Unit: 2133

The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 40 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 41 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 42 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size,

Art Unit: 2133

block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 43 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 44 is taught by Falik as:

The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

12. **Claims 61 and 64-68** are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri et al. (U.S. 20110167204) in view of Falik et al. (US 8,200,879) in view of Chin et al. (US 2001/0010066).

Claim 61 is taught by Estakhri and Falik as shown supra with respect to claim 59.

Falik further teaches:

Art Unit: 2133

The memory controller of claim 59, wherein said interface controller includes: A first memory bus controller coupled to said control device and said memory device interface. Falik figure 4b item 116.

And an IO bus controller coupled to said IO device interface and said control device. Falik figure 4b item 117.

With respect to claim 61, Chin figure 2 teaches a bridge unit 104, which connects to a CPU bus 108 and a memory bus 110, including control logic 242, shown in paragraph 0037 to direct the operations of the queue storage elements through a network of control signals. Figure 2 also illustrates a data path between the CPU bus 108 and memory bus 110 through queues 250 and 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a main control device coupled to the memory device interface and data path as taught by Chin in the interface controller of Falik.

The motivation for doing so would have been to provide a means to manage the transfer of data through the interface performed by the system of Falik, see Chin paragraph 0037.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as specified in **claim 61**.

Claim 64 is taught by Estakhri and Falik as shown supra with respect to claim 59.

Falik does not expressly teach that a buffer is a FIFO or that a data path includes a plurality of queue slots.

Art Unit: 2133

With respect to claim 64, Chin teaches: *Further including a buffer comprising a FIFO.* Paragraph 0052 shows that queue 250 is a FIFO.

And a data path that includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory. Figure 2 also shows read queue 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a FIFO and a data path including a plurality of queue slots in the system of Falik.

The motivation for doing so would have been to provide an interface that provides all devices in a computer system fair access to memory, Chin paragraph 0012.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as recited in **claim 64**.

Claim 65 is taught by Estakhri and Falik as shown supra with respect to claim 59.

Falik does not expressly teach that a data path includes a buffer having a plurality of queue slots.

With respect to claim 65, Chin teaches: *The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots.*

Art Unit: 2133

Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a FIFO and a data path including a plurality of queue slots in the system of Falik.

The motivation for doing so would have been to provide an interface that provides all devices in a computer system fair access to memory, Chin paragraph 0012.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as recited in **claims 65-67**.

Claim 66 is taught by Chin as:

The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a plurality of queue slots that buffer data from said IO device interface to said memory device interface. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory.

Claim 67 is taught by Chin as:

The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from said memory device interface to said IO device interface. Figure 2 also shows read queue 252.

Art Unit: 2133

Claim 68 is taught by Estakhri and Falik as shown supra with respect to claim 1.

Falik further teaches a memory bus controller, figure 4b item 116, coupled to bus 90.

Falik does not expressly teach that the memory bus controller is coupled to a main control device.

With respect to claim 68, Chin teaches:

A second memory bus controller coupled to said main control device and said memory device interface. Figure 2 teaches a bridge unit 104, which connects to a CPU bus 108 and a memory bus 110, including control logic 242, shown in paragraph 0037 to direct the operations of the queue storage elements through a network of control signals. Figure 2 also illustrates a data path between the CPU bus 108 and memory bus 110 through queues 250 and 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a main control device coupled to the memory device interface and data path as taught by Chin in the interface controller of Falik.

The motivation for doing so would have been to provide a means to manage the transfer of data through the interface performed by the system of Falik, see Chin paragraph 0037.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as specified in **claim 68**.

Art Unit: 2133

13. **Claims 62 and 63** are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri et al. (U.S. 20110167204) in view of Falik et al. (US 8,200,879) in view of Chin et al. (US 2001/0010066) as applied to claim 61 above, and further in view of Tsuruta (US 2007/0174506).

Claim 62 is taught by the combination of Falik and Chin as shown supra with respect to claim 61.

The combination of Falik and Chin does not expressly teach that the IO bus controller is disposed to respond to said memory transaction request by acknowledging said request and providing status to said main control device.

With respect to claim 62, Tsuruta teaches:

Wherein said IO bus controller is disposed to respond to a memory transaction request by acknowledging said request and providing status to said main control device.

Paragraph 0183 shows that in response to a read req from the CPU, MEM-DMAC 232 issues a read ack signal. Paragraph 0186 shows that after the read operation is performed, a sequencer in the memory controller 231 issues ack to a sequencer in the MEM-DMAC 232.

At the time of the invention, it would have been obvious to use the acknowledgement system of Tsuruta in the combination of Falik and Chin.

The motivation for doing so would have been to provide coordination between the CPU interface and the read/write queues to perform the requested memory operations.

Art Unit: 2133

Therefore, it would have been obvious to combine Tsuruta with Falik and Chin to obtain the invention as specified in **claims 62 and 63**.

Claim 63 is taught by Chin as:

The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction. Paragraph 0052 shows that control logic provides control signals to the input and output selectors 351 and 353 that determine the values of the enable and select signals in response to a memory request from the CPU.

Coordinates the operation of said memory device interface. Paragraph 0052 shows that the data and address of each request is sent to the memory controller 200.

And manages the transfer of memory transaction data between said IO device interface and said memory device interface through a data path. Paragraph 0052 shows that data is transferred through the queue 250.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Solan et al. (U.S Patent 5850566) discloses Method for Storing Multiple Files without Header Information and for Each Storage Medium Maintaining a Separate Stored Index Including Header Information for Each File and Methods for its use.

Art Unit: 2133

Kern et al. (U.S. Publication 2009/0158085) discloses Power Safe Translation Table Operation in Flash Memory and methods for its use.

Que (U.S. Publication 2009/0094411) discloses Nand Flash Controller and Data Exchange Method between Nand Flash Memory and Nand Flash Controller.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEAN EDOUARD whose telephone number is (571)270-1683. The examiner can normally be reached on 8:30-4:30

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rutz Jared can be reached on 571-272-5535. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JEAN EDOUARD/
Examiner, Art Unit 2133

/Aimee Li/
Supervisory Patent Examiner, Art Unit 2137

Notice of References Cited	Application/Control No. 12/876,113		Applicant(s)/Patent Under Reexamination BRUCE ET AL.	
	Examiner JEAN EDOUARD		Art Unit 2133	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2009/0094411	04-2009	QUE, JINZHEN	711/103
*	B	US-2009/0158085	06-2009	Kern et al.	714/6
*	C	US-2011/0167204	07-2011	Estakhri et al.	711/103
*	D	US-2006/0095709	05-2006	Achiwa, Kyosuke	711/173
*	E	US-6,961,805	11-2005	Lakhani et al.	711/5
*	F	US-2007/0195957	08-2007	Arulambalam et al.	380/277
*	G	US-8,200,879	06-2012	Falik et al.	710/307
*	H	US-7,330,954	02-2008	Nangle, Peter	711/170
*	I	US-2006/0184723	08-2006	Sinclair et al.	711/103
*	J	US-6,961,805	11-2005	Lakhani et al.	711/5
*	K	US-5,913,215	06-1999	Rubinstein et al.	707/708
*	L	US-2001/0010066	07-2001	Chin et al.	711/108
*	M	US-2007/0174506	07-2007	Tsuruta, Toru	710/022

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT***(Use as many sheets as necessary)***Complete if Known**

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

Sheet 2 of 2

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Notice of Allowance/Allowability for U.S. Application No. 14/038,684 for 01 August 2014.	
		Office Action for U.S. Application No. 14/038,684 mailed on 17 March 2014.	
		Notice of Allowance/Allowability for U.S. Application No. 13/890,229 mailed on 20 February 2014.	
		Office Action for U.S. Application No. 12/270,626 mailed on 23 May 2014.	

Examiner
Signature

/Jean Edouard/

Date
Considered

11/20/2014

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO:**

Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.E./

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 5,737,742	04-07-1998	Achiwa et al.	
		US- 5,802,554	09-01-1998	Caceres et al.	
		US- 5,819,307	10-06-1998	Iwamoto et al.	
		US- 2002/0141244	10-03-2002	Bruce et al.	
		US- 2009/0094411	04-09-2009	Que, Jinzhen	
		US- 2007/0130439	06-07-2007	Andersson et al.	
		US- 7,660,941	02-09-2010	Lee et al.	
		US- 5,644,784	07-01-1997	Peek	
		US- 2009/0158085	06-18-2009	Kern et al.	
		US- 2009/0172466	07-02-2009	Royer et al.	
		US- 2009/0172250	07-02-2009	Allen et al.	
		US- 2011/0264884	10-27-2011	Kim, Sung-joo	
		US- 8,713,417	04-29-014	Jo, Namphil	
		US- 8,510,631	08-13-2013	Wu et al.	
		US- 8,375,257	02-12-2013	Hong et al.	
		US- 8,707,134	04-22-2014	Takahashi et al.	
		US- 7,174,438	02-06-2007	Homma et al.	
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				

Examiner
Signature

/Jean Edouard/

Date
Considered

11/20/2014

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND**

TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

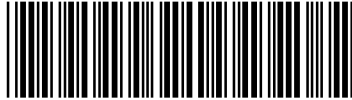
The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

<i>Index of Claims</i> 	Application/Control No. 12876113	Applicant(s)/Patent Under Reexamination BRUCE ET AL.
	Examiner JARED RUTZ	Art Unit 2187

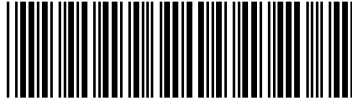
✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		DATE							
Final	Original	12/14/2012	05/07/2013	03/08/2014	07/07/2014	11/20/2014			
	1	✓	✓	✓	✓	✓			
	2	✓	✓	✓	✓	✓			
	3	✓	✓	✓	✓	✓			
	4	✓	✓	✓	✓	✓			
	5	✓	✓	✓	✓	✓			
	6	✓	✓	✓	✓	✓			
	7	✓	✓	✓	✓	✓			
	8	✓	✓	✓	✓	✓			
	9	✓	✓	✓	✓	✓			
	10	✓	✓	✓	✓	✓			
	11	✓	✓	✓	✓	✓			
	12	✓	✓	✓	✓	✓			
	13	✓	✓	✓	✓	✓			
	14	✓	✓	✓	✓	✓			
	15	✓	✓	✓	✓	✓			
	16	✓	✓	✓	✓	✓			
	17	✓	✓	✓	✓	✓			
	18	✓	✓	✓	✓	✓			
	19	✓	✓	✓	✓	✓			
	20	✓	✓	✓	✓	✓			
	21	✓	✓	✓	✓	✓			
	22	✓	✓	✓	✓	✓			
	23	✓	✓	✓	✓	✓			
	24	✓	✓	✓	✓	✓			
	25	✓	✓	✓	✓	✓			
	26	✓	✓	✓	✓	✓			
	27	✓	✓	✓	✓	✓			
	28	✓	✓	✓	✓	✓			
	29	✓	✓	✓	✓	✓			
	30	✓	✓	✓	✓	✓			
	31	✓	✓	✓	✓	✓			
	32	✓	✓	✓	✓	✓			
	33	✓	✓	✓	✓	✓			
	34	✓	✓	✓	✓	✓			
	35	✓	✓	✓	✓	✓			
	36	✓	✓	✓	✓	✓			

<i>Index of Claims</i> 	Application/Control No. 12876113	Applicant(s)/Patent Under Reexamination BRUCE ET AL.
	Examiner JARED RUTZ	Art Unit 2187

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		DATE							
Final	Original	12/14/2012	05/07/2013	03/08/2014	07/07/2014	11/20/2014			
	37	✓	✓	✓	✓	✓			
	38	✓	✓	✓	✓	✓			
	39	✓	✓	✓	✓	✓			
	40	✓	✓	✓	✓	✓			
	41	✓	✓	✓	✓	✓			
	42	✓	✓	✓	✓	✓			
	43	✓	✓	✓	✓	✓			
	44	✓	✓	✓	✓	✓			
	45	✓	✓	✓	✓	✓			
	46	✓	✓	✓	✓	✓			
	47	✓	✓	✓	✓	✓			
	48	✓	✓	✓	✓	✓			
	49	✓	✓	✓	✓	✓			
	50	✓	✓	✓	✓	✓			
	51	✓	✓	✓	✓	✓			
	52	✓	✓	✓	✓	✓			
	53	✓	✓	✓	✓	✓			
	54	✓	✓	✓	✓	✓			
	55	✓	✓	✓	✓	✓			
	56	✓	✓	✓	✓	✓			
	57	✓	✓	✓	✓	✓			
	58	✓	✓	✓	✓	✓			
	59	✓	✓	✓	✓	✓			
	60	✓	✓	✓	✓	✓			
	61	✓	✓	✓	✓	✓			
	62	✓	✓	✓	✓	✓			
	63	✓	✓	✓	✓	✓			
	64	✓	✓	✓	✓	✓			
	65	✓	✓	✓	✓	✓			
	66	✓	✓	✓	✓	✓			
	67	✓	✓	✓	✓	✓			
	68	✓	✓	✓	✓	✓			
	69	✓	✓	✓	✓	✓			
	70	✓	✓	✓	✓	✓			
	71	✓	✓	✓	✓	✓			
	72	✓	✓	✓	✓	✓			

<i>Index of Claims</i> 	Application/Control No. 12876113	Applicant(s)/Patent Under Reexamination BRUCE ET AL.
	Examiner JARED RUTZ	Art Unit 2187

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		DATE							
Final	Original	12/14/2012	05/07/2013	03/08/2014	07/07/2014	11/20/2014			
	73	✓	✓	✓	✓	✓			
	74	✓	✓	✓	✓	✓			
	75	✓	✓	✓	✓	✓			
	76	✓	✓	✓	✓	✓			
	77	✓	✓	✓	✓	✓			
	78	✓	✓	✓	✓	✓			
	79	✓	✓	✓	✓	✓			
	80	✓	✓	✓	✓	✓			
	81	✓	✓	✓	✓	✓			
	82	✓	✓	✓	✓	✓			
	83	✓	✓	✓	✓	✓			
	84	✓	✓	✓	✓	✓			
	85	✓	✓	✓	✓	✓			
	86	✓	✓	✓	✓	✓			
	87	✓	✓	✓	✓	✓			
	88	✓	✓	✓	✓	✓			
	89	✓	✓	✓	✓	✓			
	90	✓	✓	✓	✓	✓			
	91	✓	✓	✓	✓	✓			
	92	✓	✓	✓	✓	✓			
	93	✓	✓	✓	✓	✓			
	94				✓	✓			
	95				✓	✓			
	96				✓	✓			
	97				✓	✓			
	98					✓			
	99					✓			
	100					✓			
	101					✓			

Search Notes 	Application/Control No. 12876113	Applicant(s)/Patent Under Reexamination BRUCE ET AL.
	Examiner EDOUARD JEAN	Art Unit 2133

CPC- SEARCHED		
Symbol	Date	Examiner
G06F11/1451, 2064, 2082; G06F12/00, 12, 08, 122, 02, 10, 0238; G06F17/30215, 30578; G06F2201/84	11/11/2014	

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
inventor search in EAST	11/11/2014	/J.E./
text search in EAST, see search history	11/11/2014	/J.E./
internet search using google.com	11/12/2014	/J.E./
ip.com	11/12/2014	/J.E./
plus search	11/12/2014	/J.E./
Consulted with SPE Jared Rutz	11/12/2014	/J.E./

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/JEAN EDOUARD/ Examiner.Art Unit 2133	11/21/2014
--	------------

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187 2133
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 2003/0163624 A1	08-28-2003	Matsui et al.	
		US- 2007/0028040 A1	02-01-2007	Alan Welsh Sinclair	
		US- 2006/0095709 A1	05-04-2006	Kyosuke Achiwa	
		US- 20110113186	05-12-2011	Bruce et al.	
		US-			
		US- 20110202709	08-18-2011	Rychlik, Bohuslav	
		US- 8,447,908	04-21-2013	Bruce et al.	
		US- 8,788,725	07-22-2014	Bruce et al.	
		US- 8,560,804	10-15-2013	Bruce et al.	
		US- 2013/0246694	09-19-2013	Bruce et al.	
		US- 2011/0161568	06-30-2011	Bruce et al.	
		US- 2002/0083262	06-27-2002	Fukuzumi, Tomoya	
		US- 2009/0158085	06-18-2009	Kern et al.	
		US- 2009/0172466	07-02-2009	Royer et al.	
		US- 2009/0172250	07-02-2009	Allen et al.	
		US- 2011/0264884	10-27-2011	Sung-joo Kim	
		US- 2014/0104949	04-17-2014	Bruce et al.	
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				

Examiner
Signature

/Jean Edouard/

Date
Considered

11/25/2014

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.E./

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	(memory near2 location same first same second)	US-PGPUB; USPAT	OR	ON	2014/11/18 12:07
S5	2815	(memory near2 locations same host same controller)	US-PGPUB; USPAT	OR	ON	2014/11/18 12:10
S6	5	(host adj directly adj controller)	US-PGPUB; USPAT	OR	ON	2014/11/18 12:13
S10	5	(host adj coupl\$3 adj controller same memory)	US-PGPUB; USPAT	OR	ON	2014/11/18 12:15
S11	5	(host adj coupl\$3 adj controller same memory)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/11/18 12:16
S12	4	("20090240873" "20100082890" "20120144102" "20120170361").PN. OR ("8547745").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2014/11/18 13:50
S13	1	("8200879").PN.	US-PGPUB; USPAT	OR	OFF	2014/11/18 14:09
S14	5	(host adj directly adj controller)	US-PGPUB; USPAT	OR	ON	2014/11/18 16:32
S15	22	(host adj coupl\$3 adj controller)	US-PGPUB; USPAT	OR	ON	2014/11/18 16:32
S16	104	("6961805" "20070195957" "5379401" "5388083" "5479638" "5500826" "5530828" "5542082" "5548741" "5572466" "5606532" "5640349" "5918033" "6230269" "6298071" "7283629" "8560804" "20070174506" "20070083680" "20070130439" "5371709" "5488711" "5568423" "5602987" "6215875" "6404772" "6901499" "6970446" "7500063" "7660941" "8447908" "20010010066" "8200879" "20020141244" "20030182576" "5222046" "5341339" "5432748" "5509134" "5524231" "5627783" "5644784" "6529416" "20030163624" "20110161568" "20140104949" "20030223585" "20040128553" "20090094411" "5396468" "5535356" "5822251" "5881264" "7103684" "7716389" "20060095709" "20070019573" "5459850" "5485595" "5513138" "5535328" "5819307" "6857076" "7620748" "20020083262" "20090172250" "20110113186" "20110264884" "20030204675"	US-PGPUB; USPAT	OR	ON	2014/11/21 18:04

	"20070174493" "5297148" "5568439" "5594883" "5802554" "6000006" "6363444" "7765359" "20070028040" "20090158085" "20130246694" "20020073324" "4752871" "5406529" "5559956" "5603001" "5606529" "5875351" "5943421" "6363441" "6526506" "7194766" "7372962" "7743202" "20060184723" "5913215" "7330954" "5448577" "5619470" "5737742" "6557095" "6980795" "7305548" "7934052" "20110202709").PN.				
--	--	--	--	--	--

11 / 22 / 2014 7:21:44 PM

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT***(Use as many sheets as necessary)***Complete if Known**

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

Sheet 2 of 2

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Office Action for U.S. Application No. 13/253,912 mailed on 16 July 2014.	
		Office Action for U.S. Application No. 13/475,878 mailed on 23 June 2014.	
		Office Action for U.S. Application No. 12/876,113 mailed on 11 July 2014.	
		Office Action for U.S. Application No. 12/876,113 mailed on 16 October 2014.	
		Notice of Allowance for U.S. Application No. 12/270,626 mailed 03 October 2014.	
		Notice of Allowance for U.S. Application No. 14/038,684 mailed 03 November 2014.	

Examiner
Signature

/Jean Edouard/

Date

Considered

11/20/2014

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO:**

Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

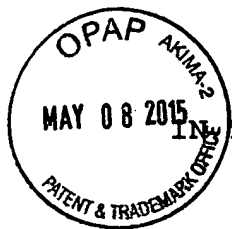
ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.E./

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



1 fm

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	) Confirmation No.: 1607
Ricardo H. Bruce, et al.	)
	) Examiner: Jared Ian Rutz
Serial No.: 12/876,113	) Ph: 571-272-5535
	)
Filing Date: Sept. 4, 2010	) Art Unit: 2187
	)
Title: Multi-Profile Memory	) Atty. Docket No.: 6005.042
Controller For Computing	)
Devices	) Customer No. 64180
	)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**RESPONSE TO OFFICE ACTION
AND AMENDMENT**

Dear Sir:

The following is in response to the office action
mailed on 05 December 2014.

Amendments to the Claims are reflected in the listing of
claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 21 of this paper.

05/08/2015 EEKUBAY1 00000004 12876113

01 FC:1252

600.00 OP

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising:

performing a memory transaction comprising addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile, wherein said second memory location is in a second memory device in the memory store, wherein a memory read transaction or a memory write transaction is performed on at least one of the first memory location or second memory location, wherein data is transferred to the first memory location or second memory location from a host for a memory write transaction, wherein data is transferred from the first memory location or second memory location to the host for a memory read transaction;

wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type;

said performing the memory transaction further comprising identifying command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;

after identifying the command details, obtaining the first set of attributes;

wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location;

wherein the memory store is directly coupled to at least one memory bus and wherein the at least one memory bus is directly coupled to a controller, and wherein the controller performs the memory read transaction and memory write transaction on the memory store;

wherein the host is directly coupled to the controller by a communication path as the controller performs the memory read transaction or memory write transaction;

wherein the first device profile and second device profile are each stored in the memory store; and

using attributes from said first and second device profiles; and

selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

2. (original) The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device.

3. (original) The method of claim 1, wherein said difference between said first and second device profiles includes different attributes; and said addressing said first memory location is made in response to a first memory transaction request; and

further including addressing said second memory location.

4. (original) The method of claim 1, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes.

5. (original) The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

6. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute values.
7. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute types.
8. (original) The method of claim 5, wherein said shared attributes include a memory device type attribute.
9. (original) The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.
10. (original) The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.
11. (original) The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.
12. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.
13. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of attributes that differs in value from a second page size attribute from said second set of attributes.
14. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes.

15. (original) The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device, and said second memory device interface attribute corresponds to a DRAM device interface.

16. (original) The method of claim 2, wherein said using attributes from said first and second device profile further includes using a first partial page size attribute from said first set of attributes that differs in value from a second partial page size attribute from said second set of attributes.

17. (original) The method of claim 16:
 said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute; and
 further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute.

18. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

19. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a NAND flash memory device and said second memory device type attribute corresponds to a NOR flash memory device.

20. (original) The method of claim 2, further including:
 using an address corresponding to a memory location from said first memory device and transferring a first data set, and
 using an address corresponding to a memory location from said second memory device and transferring a second data set.

21. (original) The method of claim 20, wherein:

said first set of attributes includes a first page size attribute, and said first data set includes a first data set size; and

if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size.

22. (original) The method of claim 20, wherein:

said second set of attributes includes a second page size attribute, and said second data set includes a second data set size; and

if said second data set size is greater than said second page size attribute, said transferring said second data set includes:

performing a set of write operations on said second memory device that includes using a second transfer size equal to said second page size attribute until a remaining portion of said second data set that has not yet been written to said second device is less than said second page size attribute, and

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

23. (previously presented) The method of claim 20, wherein:

said first set of attributes includes a page size attribute and a block size attribute;

said first data set includes a first data set size;

if said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes:

performing a set of write operations on said first memory device that includes using a second transfer size equal to said page size attribute until a remaining portion of said first data set that has not yet been written to said first device is less than said page size attribute,

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

24. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes:

performing respective write operations on said first and second memory devices by at least using a transfer size at least equal to a partial page size attribute from said first set of attributes and performing at least one write operation on said second memory device by at least using a transfer size at least equal to a partial page size attribute value from said second set of attributes; and

said attribute difference includes different attribute values of said first and second partial page size attributes.

25. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size attribute of said first memory device.

26. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a block size attribute value that corresponds to a block size attribute of said first memory device.

27. (original) The method of claim 26, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

28. (original) The method of claim 2, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

29. (currently amended) A non-transitory computer readable medium comprising computer executable instructions adapted to cause a method of performing memory transactions on a first memory location and a second memory location, said method comprising:

performing a memory transaction comprising addressing a first memory location, said first memory location and a

second memory location are respectively associated with a first device profile and a second device profile;

wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type;

said performing the memory transaction further comprising identifying command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;

said first device profile representing a first set of attributes of said first memory device, and said second device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles;

after identifying the command details, obtaining the first set of attributes; and

using attributes from said first and second device profiles; and

selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

30. (original) The computer readable medium of claim 29, wherein:

said first memory location is part of a memory space associated with a first memory device;

said second memory location is part of a memory space associated with a second memory device; and

said first and second memory devices comprise at least a portion of a memory store.

31. (previously presented) The computer readable medium of claim 29, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of a first memory device and a block size value of a second memory device.

32. (previously presented) The computer readable medium of claim 30, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

33. (original) The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

34. (original) The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes.

35. (previously presented) The computer readable medium of claim 29, wherein said addressing further includes:
 said first and second device profiles having at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and
 said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

36. (original) The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

37. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values.

38. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types.

39. (original) The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute.

40. (original) The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

41. (original) The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

42. (original) The computer readable medium of claim 36, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

43. (original) The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes.

44. (original) The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device.

45. (currently amended) A memory controller for performing memory transactions, said memory controller comprising:

means for performing a memory transaction comprising a means for addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile;

said means for addressing is directly coupled to the first memory location and second memory location;

wherein said means for addressing includes an interface controller means for processing memory transaction requests;

said means for addressing is directly coupled to a host as said means for addressing addresses the first memory location or second memory location;

wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type;

said performing the memory transaction further comprising identifying command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;

said means for addressing obtains the first set of attributes after identifying the command details; and

said means for addressing uses attributes from said first and second device profiles and selects a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

46. (original) The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

47. (original) The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

48. (original) The memory controller of claim 46, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and
said use of said attributes from said first and second device profiles by said means for addressing includes using said different attribute qualifiers for said shared attributes.

49. (original) The memory controller of claim 46, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

50. (previously presented) The memory controller of claim 45, wherein said means for addressing further includes a means for addressing said second memory location.

51. (original) The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

52. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values.

53. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types.

54. (original) The memory controller of claim 51, wherein said shared attributes include a memory device type attribute.

55. (original) The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

56. (original) The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

57. (original) The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

58. (original) The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device.

59. (currently amended) A memory controller comprising:
 an interface controller coupled to a memory device interface and an input/output (IO) device interface;
 a memory store;
 wherein the memory device interface is directly coupled to the memory store;
 said interface controller disposed to perform a memory transaction by addressing a first memory location in the memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile;
 wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said

data type comprises one of a random data type or a sequential data type;

said interface controller identifies command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;

said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;

said interface controller obtaining the first set of attributes after identifying the command details; and

said addressing of said first memory location includes using said attributes from said first device profile; and

said addressing of said first memory location includes selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

60. (original) The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile.

61. (previously presented) The memory controller of claim 59, wherein said interface controller includes:

a main control device coupled to said memory device interface and to a data path;

a first memory bus controller coupled to said control device and said memory device interface; and

an IO bus controller coupled to said IO device interface and said control device.

62. (previously presented) The memory controller of claim 61, wherein said IO bus controller is disposed to respond to a memory transaction request by acknowledging said request and providing status to said main control device.

63. (original) The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction, coordinates the operation of said memory device interface, and manages the transfer of memory transaction data between said IO device

interface and said memory device interface through a data path.

64. (previously presented) The memory controller of claim 59, further including a buffer comprising a FIFO and a data path that includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface.

65. (original) The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots.

66. (original) The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a plurality of queue slots that buffer data from said IO device interface to said memory device interface.

67. (original) The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from said memory device interface to said IO device interface.

68. (previously presented) The memory controller of claim 59, further including a second memory bus controller coupled to a main control device and said memory device interface.

69. (original) The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes.

70. (original) The memory controller of claim 59, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

71. (original) The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

72. (original) The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute.

73. (original) The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values.

74. (original) The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values.

75. (original) The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type.

76. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values.

77. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types.

78. (original) The memory controller of claim 71, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

79. (original) The memory controller of claim 71, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

80. (currently amended) An electronic storage device, comprising:

 a memory controller directly coupled to and disposed to address a first memory location and a second memory

location which are respectively associated with a first device profile and a second device profile;

said memory controller directly coupled to a host as said memory controller addresses the first memory location or second memory location;

wherein said first device profile is optimal for a data type subject to a memory transaction, wherein said data type comprises one of a random data type or a sequential data type;

said memory controller identifies command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;

said memory controller obtaining the first set of attributes after identifying the command details; and

said memory controller using attributes from said first and second device profiles; and

said memory controller selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

81. (original) The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

82. (original) The electronic storage device of claim 80, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

83. (previously presented) The electronic storage device of claim 80, said memory controller further disposed to:

- perform a write operation on said first memory device, if a memory transaction request is associated with a write request;
- perform a read operation on said first memory device, if said memory transaction request is associated with a read request; and

wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using said second device profile in response to receiving a second memory transaction request.

84. (original) The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

85. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values.

86. (original) The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute.

87. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types.

88. (original) The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said shared attributes.

89. (original) The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device.

90. (original) The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

91. (original) The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

92. (original) The electronic storage device of claim 84, wherein said shared attributes includes any one of the

following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

93. (original) The electronic storage device of claim 80, wherein said memory controller is further adapted to:

use a first partial page size attribute by performing a write operation on said first memory device and using a transfer size at least equal to said partial page size attribute; and

use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute.

94. (previously presented) The method of claim 1, wherein the first memory location and the second memory location are addressable memory locations.

95. (previously presented) The memory controller of claim 45, wherein the first memory location and the second memory location are addressable memory locations.

96. (previously presented) The memory controller of claim 59, wherein the first memory location and the second memory location are addressable memory locations.

97. (previously presented) The electronic device of claim 80, wherein the first memory location and the second memory location are addressable memory locations.

98. (previously presented) An electronic storage device, comprising: a memory controller directly coupled to and disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile;

wherein the memory controller is directly coupled to a host as the memory controller addresses the first memory location or the second memory location;

wherein said first device profile is optimal for a data type subject to a memory transaction, wherein said data type comprises one of a random data type or a sequential data type;

said memory controller identifies command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;

the first device profile representing a first set of attributes of the first memory location, and the second device profile representing a second set of attributes of the second memory location;

said memory controller obtaining the first set of attributes after identifying the command details; and
wherein said memory controller uses attributes from the first and second device profiles;
wherein said memory controller selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

99. (previously presented) The electronic devices of claim 98, wherein the memory controller comprises:

an interface controller;
 a memory device interface directly coupled to the first memory location and to the second memory location and coupled to the interface controller;
 an input/output (IO) device interface coupled to the interface controller and directly coupled to the host as the memory controller addresses the first memory location or the second memory location.

100. (currently amended) A method for performing memory transactions, the method comprising:

performing a memory transaction comprising addressing a first memory location in a first memory device in a memory store, the first memory location and a second memory location respectively associated with a first device profile and a second device profile;

wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type;

said performing the memory transaction further comprising identifying command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;

the first device profile representing a first set of attributes of the first memory location, and the second device profile representing a second set of attributes of the second memory location;

after identifying the command details, obtaining the first set of attributes;

wherein the memory store is directly coupled to a memory controller, and wherein the memory controller performs a memory transaction;

wherein ~~[[the]]~~ a host is directly coupled to the memory controller as the memory controller performs the memory transaction; and

using attributes from the first and second device profiles; and

selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

101. (previously presented) The method of claim 100, wherein the memory controller comprises:

an interface controller;

a memory device interface directly coupled to the first memory location and to the second memory location and coupled to the interface controller;

an input/output (IO) device interface coupled to the interface controller and directly coupled to the host as the memory controller addresses the first memory location or the second memory location.

REMARKS/ARGUMENTS

Claim 100 is amended to remove the lack of antecedent basis. Accordingly, the rejection to claim 100 is no longer applicable. Claim 100 is otherwise allowable.

Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-101 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Estakhri et al. (US 2011/0167204) in view of Falik et al. (US 8,200,879).

Applicants respectfully disagree with this rejection, but to expedite allowance of the claims, Applicants amend independent claim 1 herein to recite various features as shown above. Support for the amendment in claim 1 is found in the filed application in, for example, Figures 1, 2A, 2B, 2C, 4, 5, and 6 and accompanying text.

The Office admits that Estakhri does not disclose first and second device profiles as required in claim 1. Falik discloses reading tables in the registers 12 of the flash interface controller 10 (Falik: Figure 4A). However, Falik fails to disclose, fails to teach, and fails to suggest various features such as "wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type; said performing the memory transaction further comprising identifying command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device", "after identifying the command details, obtaining the first set of attributes", and "selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes" as required in claim 1. Accordingly, Estakhri and Falik do not disclose all the limitations of claim 1. Since Estakhri and Falik, considered individually or in combination do not disclose and do not teach and do not suggest all the limitations of claim 1, claim 1 is not rendered obvious by the cited references. Claim 1 is otherwise allowable.

Claims 2-14, 20, 21, and 25 depend from allowable claim 1; as such, they are also allowable for at least the same reasons as claim 1.

The withdrawal of the rejections to claims 1-14, 20, 21, 25 and 94 is respectfully requested.

Independent claims 29, 45, 59, 80, 98, and 100 recite at least some limitations similar to that as claim 1. Although claims 29, 45, 59, 80, 98, and 100 are different, Applicants respectfully argue that in this case the above arguments regarding the patentability of claim 1 apply with equal force with respect to claims 29, 45, 59, 80, 98, and 100. Since Estakhri and Falik and other cited references, considered individually or in combination, do not disclose, do not teach, and do not suggest all the limitations of claims 29, 45, 59, 80, 98, and 100, claims 29, 45, 59, 80, 98, and 100 are not rendered obvious by the cited references. Claims 29, 45, 59, 80, 98, and 100 are otherwise allowable.

Various dependent claims depend from the above allowable claims; as such, the dependent claims are also allowable for at least the same reasons as their respective independent claims.

Applicant hereby petitions and requests for a two-months extension of time to file this response. A payment of for the two-months extension of time petition is being included herewith in the signed and dated form PTO-2038.

Claims 1-101 herein are allowable, and a timely Notice of Allowance is respectfully requested.

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, the Applicants are not conceding in this application that previously pending claims are unpatentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application.

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (805) 569-1600.

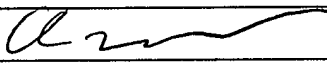
Date: May 5, 2015

Respectfully submitted,



Arnold de Guzman
Attorney for Applicant(s)
Reg. No. 39,955
805-569-1600

Please send correspondence to:
Customer No. 64180

CERTIFICATE OF TRANSMISSION OR MAILING			
37 C.F.R. 1.8			
I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office in accordance with 37 C.F.R. § 1.6(d), or is being transmitted via the Office electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4), or is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below:			
Signature:			
Typed or Printed Name:	Arnold de Guzman	Dated:	May 5, 2015
Express Mail Mailing Number (optional):			

**TRANSMITTAL
FORM**

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

25

Application Number

12/876,113

Filing Date

September 4, 2010

First Named Inventor

Ricardo H. Bruce

Art Unit

2187

Examiner Name

Jared Ian Rutz

Attorney Docket Number

6005.042

ENCLOSURES (Check all that apply)

☐ Fee Transmittal Form	☐ Drawing(s)	☐ After Allowance Communication to TC
☐ Fee Attached	☐ Licensing-related Papers	☐ Appeal Communication to Board of Appeals and Interferences
☐ Amendment/Reply	☐ Petition	☐ Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
☐ After Final	☐ Petition to Convert to a Provisional Application	☐ Proprietary Information
☐ Affidavits/declaration(s)	☐ Power of Attorney, Revocation	☐ Status Letter
☐ Extension of Time Request	☐ Change of Correspondence Address	☒ Other Enclosure(s) (please identify below):
☐ Express Abandonment Request	☐ Terminal Disclaimer	Amendment (23 pages); signed/dated PTO-2038 authorizing payment of \$600 (1 page).
☐ Information Disclosure Statement	☐ Request for Refund	
☐ Certified Copy of Priority Document(s)	☐ CD, Number of CD(s) _____	
☐ Reply to Missing Parts/Incomplete Application	☐ Landscape Table on CD	
☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53	Remarks	

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name			
Signature			
Printed name	Arnold de Guzman		
Date	May 5, 2015	Reg. No.	39,955

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature			
Typed or printed name	Arnold de Guzman	Date	May 5, 2015

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/876,113	Filing Date 09/04/2010	☐ To be Mailed
---	---	----------------------------------	---------------------------------------

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO**APPLICATION AS FILED – PART I**

(Column 1)

(Column 2)

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	05/08/2015	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 101	Minus	** 101	= 0	X \$40 =	0
	Independent (37 CFR 1.16(h))	* 7	Minus	*** 8	= 0	X \$210 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
TOTAL ADD'L FEE						0	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
TOTAL ADD'L FEE						

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/GOIGA DUCKETT/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

64180 7590 06/22/2015
URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

EXAMINER

EDOUARD, JEAN C

ART UNIT

PAPER NUMBER

2133

DATE MAILED: 06/22/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

12/876,113

09/04/2010

Ricardo H. BRUCE

6005.042

1607

TITLE OF INVENTION: MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$480	\$0	\$0	\$480	09/22/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

64180 7590 06/22/2015
URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/876,113	09/04/2010	Ricardo H. BRUCE	6005.042	1607

TITLE OF INVENTION: MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$480	\$0	\$0	\$480	09/22/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
EDOUARD, JEAN C	2133	711-103000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached. ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.	2. For printing on the patent front page, list (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____ (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____ 3 _____
---	---

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
☐ Applicant asserting small entity status. See 37 CFR 1.27
☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____
Typed or printed name _____ Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/876,113	09/04/2010	Ricardo H. BRUCE	6005.042	1607

64180 7590 06/22/2015
URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

EXAMINER

EDOUARD, JEAN C

ART UNIT	PAPER NUMBER
----------	--------------

2133

DATE MAILED: 06/22/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 12/876,113	Applicant(s) BRUCE ET AL.	
	Examiner JEAN EDOUARD	Art Unit 2133	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 05/08/2015.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-101. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>11/17/2014, 02/05/2014</u> 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	5. ☐ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
--	--

	/JARED RUTZ/ Supervisory Patent Examiner, Art Unit 2133
--	--

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Response to Amendment

The amendments filed on 05/08/2015, have been and made of record. In response to the most recent office action, dated 12/05/2014:

Claims 1-101 have been considered.

Reasons for Allowance

Claims 1-101are allowed.

The prior art does not teach or fairly suggest:

Claim 1 recites the limitations " Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; after identifying the command details, obtaining the first set of attributes; wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location; Wherein the first device profile and second device profile are each stored in the memory store; and using attributes from said first and second device profiles; and selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes".

Claim 29 recites the limitations " Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; after identifying the command details, obtaining the first set of attributes; and using attributes from said first and second device profiles; and selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attribute".

Claim 45 recites the limitations " Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles Said means for addressing obtains the first set of attributes after identifying the command details; and said means for addressing uses attributes from said first and second device profiles and selects a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes".

Claim 59 recites the limitations " said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; said interface controller obtaining the first set of attributes after identifying the command details; and said addressing of said first memory location includes using said attributes from said first device profile; and said addressing of said first memory location includes

Art Unit: 2133

selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

Claim 80 recites the limitations " said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; said memory controller obtaining the first set of attributes after identifying the command details; and said memory controller using attributes from said first and second device profiles; and said memory controller selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes".

Claim 98 recites the limitations "the first device profile representing a first set of attributes of the first memory location, and the second device profile representing a second set of attributes of the second memory location; said memory controller obtaining the first set of attributes after identifying the command details; and wherein said memory controller uses attributes from the first and second device profiles; wherein said memory controller selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes".

Art Unit: 2133

Claim 100 recites the limitations “the first device profile representing a first set of attributes of the first memory location, and the second device profile representing a second set of attributes of the second memory location; after identifying the command details, obtaining the first set of attributes; memory transaction; and using attributes from the first and second device profiles; and selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes”.

Said limitations are taught by the specification as originally filed at least at paragraphs {0015}-[0019 and [0033].

Claims 2-28, 30-44, 46-59, 60-80, 99 and 101 depend from claims 1, 29, 45, 59, 80, 98 and 100 and are considered allowable for at least the same reasons as claims 1, 29, 45, 59, 80, 98 and 100.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEAN EDOUARD whose telephone number is (571)270-1683. The examiner can normally be reached on 8:30 - 4:30.

Art Unit: 2133

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jared Rutz can be reached on 5712725535. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JEAN EDOUARD/
Examiner, Art Unit 2133

/JARED RUTZ/
Supervisory Patent Examiner, Art Unit 2133



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 1607

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
12/876,113	09/04/2010	711	2133	6005.042		
APPLICANTS INVENTORS Ricardo H. BRUCE, Union City, CA; Marlon B. VERDAN, Paranaque City, PHILIPPINES; Margaret Anne N. SOMERA, Caloocan City, PHILIPPINES; Rowenah Michelle D. JAGO-ON, Pasig City, PHILIPPINES; Maria Eliza B. DE BELEN, Quezon City, PHILIPPINES; Ron Kelvin B. PALACOL, Laguna, PHILIPPINES;						
** CONTINUING DATA ***** This appln claims benefit of 61/239,794 09/04/2009						
** FOREIGN APPLICATIONS *****						
** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** ** SMALL ENTITY ** 09/16/2010						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/JARED IAN RUTZ/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 4	TOTAL CLAIMS 93	INDEPENDENT CLAIMS 5
ADDRESS URIARTE LAW Attn: Stephen R. Uriarte 2021 The Alameda Suite 225 San Jose, CA 95126 UNITED STATES						
TITLE MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES						
FILING FEE RECEIVED 4125	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1 of 7

Complete if Known

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 5,822,251	10-13-1998	Bruce et al.	
		US- 4,752,871	06-21-1988	Sparks	
		US- 5,297,148	03-22-1994	Harari et al.	
		US- 5,379,401	01-03-1995	Robinson et al.	
		US- 5,388,083	02-07-1995	Assar et al.	
		US- 5,432,748	07-11-1995	Hsu et al.	
		US- 5,448,577	09-05-1995	Wells et al.	
		US- 5,479,638	12-26-1995	Assar et al.	
		US- 5,500,826	03-19-1996	Hsu et al.	
		US- 5,509,134	04-16-1996	Fandrich et al.	
		US- 5,513,138	04-30-1996	Manabe et al.	
		US- 5,524,231	06-04-1996	Brown	
		US- 5,530,828	06-25-1996	Kaki et al.	
		US- 5,535,328	07-09-1996	Harari et al.	
		US- 5,559,956	09-24-1996	Sukegawa	
		US- 5,568,439	10-22-1996	Harari	
		US- 5,572,466	11-05-1996	Sukegawa	
		US- 5,594,883	01-14-1997	Pricer	
		US- 5,602,987	02-11-1997	Harari et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
		WO 94/06210	03-17-1994	Prabhakar Goel		

Examiner
Signature

/Jean Edouard/

Date
Considered

06/11/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.E./

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known			
		Application Number	12/876,113		
		Filing Date	September 4, 2010		
		First Named Inventor	Ricardo H. Bruce		
		Art Unit	2187		
		Examiner Name	Jared Ian Rutz		
Sheet	7	of	7	Attorney Docket Number	6005.042

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Office Action mailed 08 October 2013 for US Application No. 13/890,229.	
		Notice of Allowability (and Examiner's Comment) mailed 30 May 2013 for US Application No. 12/882,059.	
		Notice of Allowability (and Examiner's Comment and Statement of Reasons for Allowance) mailed 14 February 2013 for US Application No. 12/882,059.	
		Office Action mailed 11 May 2012 for US Application No. 12/882,059.	
		Notice of Allowability (and Examiner's Comment and Statement of Reasons for Allowance) mailed 07 January 2013 for US Application No. 12/876,247.	
		Office Action mailed 14 September 2012 for US Application No. 12/876,247.	
		Office Action mailed 01 February 2012 for US Application No. 12/876,247.	

Examiner Signature	/Jean Edouard/	Date Considered	06/11/2015
--------------------	----------------	-----------------	------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form are welcome. This form is to be completed by the applicant and submitted to the Examiner, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO:

Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.E./

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 2

of 7

Complete if Known

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 5,603,001	02-11-1997	Sukegawa et al.	
		US- 5,606,529	02-25-1997	Honma et al.	
		US- 5,619,470	04-08-1997	Fukumoto	
		US- 5,627,783	05-06-1997	Miyauchi	
		US- 5,640,349	06-17-1997	Kakinuma et al.	
		US- 5,222,046	06-22-1993	Kreifels et al.	
		US- 6,000,006	12-07-1999	Bruce et al.	
		US- 5,341,339	08-23-1994	Wells	
		US- 5,371,709	12-06-1994	Fisher et al.	
		US- 5,396,468	03-07-1995	Harari et al.	
		US- 5,406,529	04-11-1995	Asano	
		US- 5,459,850	10-17-1995	Clay et al.	
		US- 5,485,595	01-16-1996	Assar et al.	
		US- 5,488,711	01-30-1996	Hewitt et al.	
		US- 5,535,356	07-09-1996	Kim et al.	
		US- 5,542,082	07-30-1996	Solhjell	
		US- 5,548,741	08-20-1996	Watanabe	
		US- 5,568,423	10-22-1996	Jou et al.	
		US- 5,606,532	02-25-1997	Lambrache et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				

Examiner
Signature

/Jean Edouard/

Date
Considered

06/11/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND**

TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.E./

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. //E//

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known	
		Application Number	12/876,113
		Filing Date	September 4, 2010
		First Named Inventor	Ricardo H. Bruce
		Art Unit	2187
		Examiner Name	Jared Ian Rutz
Sheet 6	of 7	Attorney Docket Number	6005.042

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		USPTO Notice of Allowability & attachment(s) mailed 7 January 2013 for US Application No. 12/876,247.	
		Office Action mailed 14 September 2012 for US Application No. 12/876,247.	
		Office Action mailed 01 February 2012 for US Application No. 12/876,247.	
		Office Action mailed 18 December 2013 for US Application No. 12/270,626.	
		Office Action mailed 15 March 2013 for US Application No. 12/270,626.	
		Office Action mailed 23 August 2012 for US Application No. 12/270,626.	
		Office Action mailed 03 February 2012 for US Application No. 12/270,626.	
		"Security Comes To SNMP: The SNMPv3 Proposed Internet Standards" http://www.cisco.com . vol. 3 no. 3, 8 pages.	
		Office Action mailed 05 October 2011 for US Application No. 12/270,626.	
		Office Action mailed 04 April 2011 for US Application No. 12/270,626.	

Examiner Signature	/Jean Edouard/	Date Considered	06/11/2015
--------------------	----------------	-----------------	------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. //J.E./

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 3

of 7

Complete if Known

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 5,737,742	04-07-1998	Achiwa et al.	
		US- 5,802,554	09-01-1998	Caceres et al.	
		US- 5,819,307	10-06-1998	Iwamoto et al.	
		US- 2002/0141244	10-03-2002	Bruce et al.	
		US- 2009/0094411	04-09-2009	Que, Jinzhen	
		US- 7,765,359	07-27-2010	Kang et al.	
		US- 2003/0204675	10-30-2003	Dover et al.	
		US- 7,103,684	09-05-2006	Chen et al.	
		US- 7,500,063	03-03-2009	Zohar et al.	
		US- 5,644,784	07-01-1997	Peek	
		US- 7,660,941	02-09-2010	Lee et al.	
		US- 2007/0130439	06-07-2007	Andersson et al.	
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				

Examiner
Signature

/Jean Edouard/

Date
Considered

06/11/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND**

TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

If you need assistance in completing the form, call 1-800-FWD-9199 (1-800-786-9199) and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. //J.E./

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 5

of 7

Complete if Known

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 2007/0174493	07-26-2007	Irish et al.	
		US- 2007/0195957	08-23-2007	Arulambalam et al.	
		US- 2004/0128553	07-01-2004	Buer et al.	
		US- 2003/0182576	09-25-2003	Morlang et al.	
		US- 2003/0223585	12-04-2003	Tardo et al.	
		US- 7,305,548	12-04-2007	Pierce et al.	
		US- 7,283,629	10-16-2007	Kaler et al.	
		US- 6,980,795	12-27-2005	Hermann et al.	
		US- 6,230,269	05-08-2001	Spies et al.	
		US- 6,215,875	04-10-2001	S. Nohda	
		US- 7,934,052	04-26-2011	Prins et al.	
		US- 6,901,499	05-31-2005	Aasheim et al.	
		US- 7,743,202	06-22-2010	Tsai et al.	
		US- 6,000,006	12-07-1999	Bruce et al.	
		US- 6,529,416	03-04-2003	Bruce et al.	
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
		JP 2005-309847	11-04-2005	Sharp Corp.		

Examiner
Signature

/Jean Edouard/

Date
Considered

06/11/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND**

TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.E./

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 4

of 7

Complete if Known

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 5,875,351	02-23-1999	D. Riley	
		US- 5,881,264	03-09-1999	Y. Kurosawa	
		US- 5,918,033	06-29-1999	Heeb et al.	
		US- 5,943,421	08-24-1999	R. Grabon	
		US- 6,298,071	10-02-2001	Taylor et al.	
		US- 6,363,441	03-26-2002	Beniz et al.	
		US- 6,363,444	03-36-2002	Platko et al.	
		US- 6,404,772	06-11-2002	Beach et al.	
		US- 6,526,506	02-25-2003	D. Lewis	
		US- 6,557,095	04-29-2003	A. Henstrom	
		US- 6,857,076	02-15-2005	D. Klein	
		US- 6,970,446	11-29-2005	Krischar et al.	
		US- 7,194,766	03-20-2007	Noehring et al.	
		US- 7,372,962	06-13-2008	Fujimoto et al.	
		US- 7,620,748	11-17-2009	Bruce et al.	
		US- 7,716,389	05-11-2010	Bruce et al.	
		US- 2002/0073324	06-13-2002	Hsu et al.	
		US- 2007/0019573	01-25-2007	M. Nishimura	
		US- 2007/0083680	04-12-2007	King et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				

Examiner Signature	/Jean Edouard/	Date Considered	06/11/2015
--------------------	----------------	-----------------	------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.E./

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 5,737,742	04-07-1998	Achiwa et al.	
		US- 5,802,554	09-01-1998	Caceres et al.	
		US- 5,819,307	10-06-1998	Iwamoto et al.	
		US- 2002/0141244	10-03-2002	Bruce et al.	
		US- 2009/0094411	04-09-2009	Que, Jinzhen	
		US- 2007/0130439	06-07-2007	Andersson et al.	
		US- 7,660,941	02-09-2010	Lee et al.	
		US- 5,644,784	07-01-1997	Peek	
		US- 2009/0158085	06-18-2009	Kern et al.	
		US- 2009/0172466	07-02-2009	Royer et al.	
		US- 2009/0172250	07-02-2009	Allen et al.	
		US- 2011/0264884	10-27-2011	Kim, Sung-joo	
		US- 8,713,417	04-29-014	Jo, Namphil	
		US- 8,510,631	08-13-2013	Wu et al.	
		US- 8,375,257	02-12-2013	Hong et al.	
		US- 8,707,134	04-22-2014	Takahashi et al.	
		US- 7,174,438	02-06-2007	Homma et al.	
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				

Examiner
Signature

/Jean Edouard/

Date
Considered

06/11/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND**

TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.E./

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.E./

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

Sheet 2 of 2

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Office Action for U.S. Application No. 13/253,912 mailed on 16 July 2014.	
		Office Action for U.S. Application No. 13/475,878 mailed on 23 June 2014.	
		Office Action for U.S. Application No. 12/876,113 mailed on 11 July 2014.	
		Office Action for U.S. Application No. 12/876,113 mailed on 16 October 2014.	
		Notice of Allowance for U.S. Application No. 12/270,626 mailed 03 October 2014.	
		Notice of Allowance for U.S. Application No. 14/038,684 mailed 03 November 2014.	

Examiner
Signature

/Jean Edouard/

Date

Considered

06/11/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. **ALL REFERENCES CONSIDERED EXCEPT WHERE SHOWN OTHERWISE. SEND TO:****Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. //J.E./

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 2003/0163624 A1	08-28-2003	Matsui et al.	
		US- 2007/0028040 A1	02-01-2007	Alan Welsh Sinclair	
		US- 2006/0095709 A1	05-04-2006	Kyosuke Achiwa	
		US- 20110113186	05-12-2011	Bruce et al.	
		US-			
		US- 20110202709	08-18-2011	Rychlik, Bohuslav	
		US- 8,447,908	04-21-2013	Bruce et al.	
		US- 8,788,725	07-22-2014	Bruce et al.	
		US- 8,560,804	10-15-2013	Bruce et al.	
		US- 2013/0246694	09-19-2013	Bruce et al.	
		US- 2011/0161568	06-30-2011	Bruce et al.	
		US- 2002/0083262	06-27-2002	Fukuzumi, Tomoya	
		US- 2009/0158085	06-18-2009	Kern et al.	
		US- 2009/0172466	07-02-2009	Royer et al.	
		US- 2009/0172250	07-02-2009	Allen et al.	
		US- 2011/0264884	10-27-2011	Sung-joo Kim	
		US- 2014/0104949	04-17-2014	Bruce et al.	
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				

Examiner
Signature

/Jean Edouard/

Date
Considered

06/11/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND**

TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Search Notes 	Application/Control No. 12876113	Applicant(s)/Patent Under Reexamination BRUCE ET AL.
	Examiner EDOUARD JEAN	Art Unit 2133

CPC- SEARCHED		
Symbol	Date	Examiner
G06F11/1451, 2064, 2082; G06F12/00, 12, 08, 122, 02, 10, 0238; G06F17/30215, 30578; G06F2201/84	11/11/2014	/J.E./

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
inventor search in EAST	11/11/2014	/J.E./
text search in EAST, see search history	11/11/2014	/J.E./
internet search using google.com	11/12/2014	/J.E./
ip.com	11/12/2014	/J.E./
plus search	11/12/2014	/J.E./
Consulted with SPE Jared Rutz	11/12/2014	/J.E./
consulted with primary Bansal Gurtej	05/27/2015	/J.E./
Consulted with my SPE Jared Rutz	05/29/2015	/J.E./

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
G06F13	/16	05/29/2015	/J.E./
G06F12	/02	05/29/2015	/J.E./
G11C16	/102	05/29/2015	/J.E./

/JEAN EDOUARD/ Examiner.Art Unit 2133	06/01/2015
--	------------

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
G06F3	/0679	05/29	/J.E./
G06F2212	2022, 7211	2015	

/JEAN EDOUARD/
Examiner.Art Unit 2133

06/01/2015

Issue Classification 	Application/Control No. 12876113	Applicant(s)/Patent Under Reexamination BRUCE ET AL.
	Examiner JEAN EDOUARD	Art Unit 2133

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION												
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED							
711		103				G	0	6	F	12 / 00 (2006.0)								
CROSS REFERENCE(S)																		
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																	

/JEAN EDOUARD/ Examiner.Art Unit 2133 (Assistant Examiner)	06/11/2015 (Date)	Total Claims Allowed: 101	
/JARED RUTZ/ Supervisory Patent Examiner.Art Unit 2133 (Primary Examiner)	06/15/2015 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

Issue Classification 	Application/Control No. 12876113	Applicant(s)/Patent Under Reexamination BRUCE ET AL.
	Examiner JEAN EDOUARD	Art Unit 2133

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17		33		49		65		81		97		
	2		18		34		50		66		82		98		
	3		19		35		51		67		83		99		
	4		20		36		52		68		84		100		
	5		21		37		53		69		85		101		
	6		22		38		54		70		86				
	7		23		39		55		71		87				
	8		24		40		56		72		88				
	9		25		41		57		73		89				
	10		26		42		58		74		90				
	11		27		43		59		75		91				
	12		28		44		60		76		92				
	13		29		45		61		77		93				
	14		30		46		62		78		94				
	15		31		47		63		79		95				
	16		32		48		64		80		96				

/JEAN EDOUARD/ Examiner.Art Unit 2133 (Assistant Examiner)	06/11/2015 (Date)	Total Claims Allowed: 101	
/JARED RUTZ/ Supervisory Patent Examiner.Art Unit 2133 (Primary Examiner)	06/15/2015 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known	
		Application Number	12/876,113
		Filing Date	September 4, 2010
		First Named Inventor	Ricardo H. Bruce
		Art Unit	2187
		Examiner Name	Jared Ian Rutz
Sheet 2	of 2	Attorney Docket Number	6005.042

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Notice of Allowance/Allowability for U.S. Application No. 14/038,684 for 01 August 2014.	
		Office Action for U.S. Application No. 14/038,684 mailed on 17 March 2014.	
		Notice of Allowance/Allowability for U.S. Application No. 13/890,229 mailed on 20 February 2014.	
		Office Action for U.S. Application No. 12/270,626 mailed on 23 May 2014.	

Examiner Signature	/Jean Edouard/	Date Considered	06/11/2015
--------------------	----------------	-----------------	------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO:**

Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. //J.E./

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	(memory near2 location same first same second)	US-PGPUB; USPAT	OR	ON	2014/11/18 12:07
S5	2815	(memory near2 locations same host same controller)	US-PGPUB; USPAT	OR	ON	2014/11/18 12:10
S6	5	(host adj directly adj controller)	US-PGPUB; USPAT	OR	ON	2014/11/18 12:13
S10	5	(host adj coupl\$3 adj controller same memory)	US-PGPUB; USPAT	OR	ON	2014/11/18 12:15
S11	5	(host adj coupl\$3 adj controller same memory)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/11/18 12:16
S12	4	("20090240873" "20100082890" "20120144102" "20120170361").PN. OR ("8547745").URFN.	US-PGPUB; USPAT; USOCR	OR	ON	2014/11/18 13:50
S13	1	("8200879").PN.	US-PGPUB; USPAT	OR	OFF	2014/11/18 14:09
S14	5	(host adj directly adj controller)	US-PGPUB; USPAT	OR	ON	2014/11/18 16:32
S15	22	(host adj coupl\$3 adj controller)	US-PGPUB; USPAT	OR	ON	2014/11/18 16:32
S16	0	("136659600").PN.	US-PGPUB; USPAT	OR	OFF	2014/12/02 10:43
S17	1	(13/659800).APP.	US-PGPUB; USPAT	OR	OFF	2014/12/02 10:45
S18	11744	(G06F13/16 G06F12/02 G06F12/0246 G06F3/0679 G11C16/102 G06F2212/2022 G06F2212/7211).CPC.	US-PGPUB; USPAT	OR	ON	2015/06/01 03:25
S19	22	((Ricardo) near2 (BRUCE)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/06/01 03:32
S20	0	((Marlon) near2 (VERDAN)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/06/01 03:32
S21	0	((("Margaret Anne") near2 (SOMERA)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/06/01 03:32
S22	0	(Margaret near2 Anne near2 SOMERA).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/06/01 03:34
S23	0	(Marlon near2 VERDAN).INV.	US-PGPUB; USPAT;	OR	ON	2015/06/01 03:35

			USOCR			
S24	0	((Rowenah) near2 (JAGO-ON)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/06/01 03:35
S25	15347	(plural multiple separate) with (profile attribute parameters) with (memory storage)	US-PGPUB; USPAT	OR	ON	2015/06/01 12:47
S26	4793	(hybrid heterogenous) near3 memory	US-PGPUB; USPAT	OR	ON	2015/06/01 12:48
S27	144581	(hybrid heterogenous different) near3 memory	US-PGPUB; USPAT	OR	ON	2015/06/01 12:49
S28	2276	S25 and S27	US-PGPUB; USPAT	OR	ON	2015/06/01 12:49
S29	84	S25 and S26	US-PGPUB; USPAT	OR	ON	2015/06/01 12:50
S30	38	S29 and @ad<"20100904"	US-PGPUB; USPAT	OR	ON	2015/06/01 12:51
S31	223407	(memory device) near3 (parameter attribute)	US-PGPUB; USPAT	OR	ON	2015/06/01 12:52
S32	15347	(plural multiple separate) with (profile attribute parameter) with (memory storage)	US-PGPUB; USPAT	OR	ON	2015/06/01 12:54
S33	6662	S31 and S32	US-PGPUB; USPAT	OR	ON	2015/06/01 12:55
S34	11744	(G06F13/16 G06F12/02 G06F12/0246 G06F3/0679 G11C16/102 G06F2212/2022 G06F2212/7211).CPC.	US-PGPUB; USPAT	OR	ON	2015/06/01 12:56
S35	172	S33 and S34	US-PGPUB; USPAT	OR	ON	2015/06/01 12:56
S36	24798	(parameter attribute) with (flash nand nor)	US-PGPUB; USPAT	OR	ON	2015/06/01 12:58
S37	593	S33 and S36	US-PGPUB; USPAT	OR	ON	2015/06/01 12:58
S38	73	S35 and S37	US-PGPUB; USPAT	OR	ON	2015/06/01 12:58
S39	42	S38 and @ad<"20100904"	US-PGPUB; USPAT	OR	ON	2015/06/01 13:00
S40	144581	(hybrid heterogenous different) near3 memory	US-PGPUB; USPAT	OR	ON	2015/06/01 13:01
S41	64	S40 and (DRAM same NAND same NOR same battery)	US-PGPUB; USPAT	OR	ON	2015/06/01 13:02
S42	15	S41 and @ad<"20100904"	US-PGPUB; USPAT	OR	ON	2015/06/01 13:03
S43	4543255	partial page program\$4	US-PGPUB; USPAT	OR	ON	2015/06/01 13:04
S44	635	partial near4 page near4 program\$4	US-PGPUB; USPAT	OR	ON	2015/06/01 13:05
S45	348	S44 and @ad<"20100904"	US-PGPUB; USPAT	OR	ON	2015/06/01 13:06
S46	525	S34 and (memory near2 locations same host same controller)	US-PGPUB; USPAT	OR	ON	2015/06/01 13:12
S47	308	S46 and @ad<"20100904"	US-PGPUB; USPAT	OR	ON	2015/06/01 13:13

S48	29	(BITMI CRO near2 NETWORKS near2 INC).as.	US-PGPUB; USPAT	OR	ON	2015/06/01 13:18
S49	16	S34 and S48	US-PGPUB; USPAT	OR	ON	2015/06/01 13:18
S50	2	S47 and S48	US-PGPUB; USPAT	OR	ON	2015/06/01 13:19
S51	6661	(Transaction map\$4 translat\$4) same address same Identif\$4 same write	US-PGPUB; USPAT	OR	ON	2015/06/01 13:23
S52	671	S34 and S51	US-PGPUB; USPAT	OR	ON	2015/06/01 13:24
S54	128	S52 and write near4 transaction	US-PGPUB; USPAT	OR	ON	2015/06/01 13:25
S55	57	S54 and @ad<"20100904"	US-PGPUB; USPAT	OR	ON	2015/06/01 13:26
S56	142	transaction with (command request) same (plural multiple separate) with (profile attribute parameter) with (memory storage)	US-PGPUB; USPAT	OR	ON	2015/06/01 13:31
S59	67042	(short\$3 shorten\$3 truncat\$3) near3 (burst transmission)	US-PGPUB; USPAT	OR	ON	2015/06/01 13:35
S60	201	S33 and (short\$3 shorten\$3 truncat\$3) near3 (burst transmission)	US-PGPUB; USPAT	OR	ON	2015/06/01 13:35
S62	0	patial near3 page with (size attribute)	US-PGPUB; USPAT	OR	ON	2015/06/01 13:37
S63	95910	patial page with (size attribute)	US-PGPUB; USPAT	OR	ON	2015/06/01 13:38
S64	0	patial with page with (size attribute)	US-PGPUB; USPAT	OR	ON	2015/06/01 13:38
S65	243	((multiple plural series) near3 (burst)) with (remaining remainder additional)	US-PGPUB; USPAT	OR	ON	2015/06/01 13:40
S66	4	S34 and S65	US-PGPUB; USPAT	OR	ON	2015/06/01 13:41
S67	143129	(writ\$3 program\$4) near3 block	US-PGPUB; USPAT	OR	ON	2015/06/01 13:42
S68	56	S65 and S67	US-PGPUB; USPAT	OR	ON	2015/06/01 13:43
S69	629	(writ\$3 program\$4) near3 multiple with blocks with (instruction command request)	US-PGPUB; USPAT	OR	ON	2015/06/01 13:45
S70	4	S65 and S69	US-PGPUB; USPAT	OR	ON	2015/06/01 13:45
S71	16	S52 and S69	US-PGPUB; USPAT	OR	ON	2015/06/01 13:47
S72	186	Memory near3 transaction with location with identif\$4	US-PGPUB; USPAT	OR	ON	2015/06/01 13:50
S73	4	S34 and Memory near3 transaction with location with identif\$4	US-PGPUB; USPAT	OR	ON	2015/06/01 13:50
S74	1828214	Memory near3 transaction with size wit (attribute profile)	US-PGPUB; USPAT	OR	ON	2015/06/01 13:52
S75	3	Memory near3 transaction with size with (attribute profile)	US-PGPUB; USPAT	OR	ON	2015/06/01 13:52
S76	153	Memory near3 transaction with size	US-PGPUB; USPAT	OR	ON	2015/06/01

		and (attribute profile)	USPAT			13:53
S77	21	S34 and Memory near3 transaction with size and (attribute profile)	US-PGPUB; USPAT	OR	ON	2015/06/01 13:53
S78	779	Memory near3 transaction with controller same read same (path interface bus)	US-PGPUB; USPAT	OR	ON	2015/06/01 13:57
S79	26	S34 and S78	US-PGPUB; USPAT	OR	ON	2015/06/01 13:57
S80	620	S78 and @ad<"20100904"	US-PGPUB; USPAT	OR	ON	2015/06/01 13:58
S81	8	S78 and S76	US-PGPUB; USPAT	OR	ON	2015/06/01 13:59
S82	10	S79 and @ad<"20100904"	US-PGPUB; USPAT	OR	ON	2015/06/01 14:00
S83	844	host same controller same memory near4 transaction	US-PGPUB; USPAT	OR	ON	2015/06/01 14:02
S84	80	S34 and S83	US-PGPUB; USPAT	OR	ON	2015/06/01 14:02
S85	46	S84 and @ad<"20100904"	US-PGPUB; USPAT	OR	ON	2015/06/01 14:03
S86	396	(plural multiple separate) with (profile attribute parameters) with (memory storage) same transaction	US-PGPUB; USPAT	OR	ON	2015/06/01 14:04
S87	6	S83 and (plural multiple separate) with (profile attribute parameters) with (memory storage) same transaction	US-PGPUB; USPAT	OR	ON	2015/06/01 14:05
S88	0	(plural multiple separate) with (profile attribute parameters) with (memory storage) with transaction with size same identifier	US-PGPUB; USPAT	OR	ON	2015/06/01 14:10
S89	7	(plural multiple separate) with (profile attribute parameters) with (memory storage) with transaction same size and identifier	US-PGPUB; USPAT	OR	ON	2015/06/01 14:10
S90	1843	(transfer\$3 access\$3 read\$3 writ\$3 transaction) near3 (size length) with (based function) with (attribute profile flag indicat\$3)	US-PGPUB; USPAT	OR	ON	2015/06/02 12:44
S91	1997	(transfer\$3 access\$3 read\$3 writ\$3 transaction) near3 (size length) with (based function) with (attribute profile flag indicat\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/06/02 12:44
S92	416	S91 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/06/02 12:45
S93	95	(transfer\$3 access\$3 read\$3 writ\$3 transaction) near3 (size length) with (based function) with (attribute flag indicat\$3) same2	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2015/06/02 12:47

		(profile policy)	JPO; DERWENT; IBM_TDB			
S94	13	S93 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/06/02 12:51
S95	16	(transfer\$3 access\$3 read\$3 writ\$3 transaction) near3 (size length) with (based function) with (attribute flag indicat\$3) same2 (profile policy) same2 (random\$2 sequential\$2 consecutiv\$3 continuos\$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/06/02 12:57
S96	1	(13/659800).APP.	US-PGPUB; USPAT	OR	OFF	2015/06/02 13:00
S99	11756	(G06F13/16 G06F12/02 G06F12/0246 G06F3/0679 G11C16/102 G06F2212/2022 G06F2212/7211).CPC.	US-PGPUB; USPAT	OR	ON	2015/06/02 13:48
S100	0	S99 and (transfer\$3 access\$3 read\$3 writ\$3 transaction) near3 (size length) with (based function) with (attribute flag indicat\$3) same2 (profile policy) same2 (random\$2 sequential\$2 consecutiv\$3 continuos\$2)	US-PGPUB; USPAT	OR	ON	2015/06/02 13:48
S101	58	S91 and S99	US-PGPUB; USPAT	OR	ON	2015/06/02 13:50
S102	5413	L and S99	US-PGPUB; USPAT	OR	ON	2015/06/02 13:50
S103	46	S92 and S99	US-PGPUB; USPAT	OR	ON	2015/06/02 13:51
S105	243	((multiple plural series) near3 (burst)) with (remaining remainder additional)	US-PGPUB; USPAT	OR	ON	2015/06/02 13:53
S106	0	S91 and S105	US-PGPUB; USPAT	OR	ON	2015/06/02 13:53
S107	6670	(Transaction map\$4 translat\$4) same address same Identif\$4 same write	US-PGPUB; USPAT	OR	ON	2015/06/02 13:54
S108	43	S91 and S107	US-PGPUB; USPAT	OR	ON	2015/06/02 13:54
S109	18	S99 and S108	US-PGPUB; USPAT	OR	ON	2015/06/02 13:54
S110	56	S93 and @ad<"20100904"	US-PGPUB; USPAT	OR	ON	2015/06/02 13:56
S111	26	S101 and @ad<"20100904"	US-PGPUB; USPAT	OR	ON	2015/06/02 13:56
S112	5	S109 and @ad<"20100904"	US-PGPUB; USPAT	OR	ON	2015/06/02 13:56
S113	24	"L25" and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2015/06/02 13:59

			JPO; DERWENT; IBM TDB			
--	--	--	-----------------------------	--	--	--

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S114	1013	(transfer\$3 access\$3 read\$3 writ\$3 transaction) near3 (size length) with (based function) with (attribute profile flag indicat\$3)	USPAT; UPAD	OR	ON	2015/06/02 13:57
S115	1013	(transfer\$3 access\$3 read\$3 writ\$3 transaction) near3 (size length) with (based function) with (attribute profile flag indicat\$3)	USPAT; UPAD	OR	ON	2015/06/02 13:58
S117	49	(transfer\$3 access\$3 read\$3 writ\$3 transaction) near3 (size length) with (based function) with (attribute flag indicat\$3) same2 (profile policy)	USPAT; UPAD	OR	ON	2015/06/02 13:59
S118	10	S117 and "711".clas.	USPAT; UPAD	OR	ON	2015/06/02 14:06
S119	15	(transfer\$3 access\$3 read\$3 writ\$3 transaction) near3 (size length) with (based function) with (attribute flag indicat\$3) same2 (profile policy) same2 (random\$2 sequential\$2 consecutiv\$3 continuos\$2)	USPAT; UPAD	OR	ON	2015/06/02 14:06
S120	4960	(G06F13/16 G06F12/02 G06F12/0246 G06F3/0679 G11C16/102 G06F2212/2022 G06F2212/7211).CPC.	USPAT; UPAD	OR	ON	2015/06/02 14:08
S121	24	S115 and S120	USPAT; UPAD	OR	ON	2015/06/02 14:08
S122	13	S121 and @ad<"20100904"	USPAT; UPAD	OR	ON	2015/06/02 14:09
S123	0	S117 and S120	USPAT; UPAD	OR	ON	2015/06/02 14:10
S124	145	((multiple plural series) near3 (burst)) with (remaining remainder additional)	USPAT; UPAD	OR	ON	2015/06/02 14:11
S125	4	S120 and S124	USPAT; UPAD	OR	ON	2015/06/02 14:11
S126	2270	(hybrid heterogenous) near3 memory	USPAT; UPAD	OR	ON	2015/06/02 14:12
S127	74277	(hybrid heterogenous different) near3 memory	USPAT; UPAD	OR	ON	2015/06/02 14:13
S128	7443	(plural multiple separate) with (profile attribute parameters) with (memory storage)	USPAT; UPAD	OR	ON	2015/06/02 14:14
S129	44	S126 and S128	USPAT; UPAD	OR	ON	2015/06/02 14:14
S130	27	S129 and @ad<"20100904"	USPAT; UPAD	OR	ON	2015/06/02 14:14
S131	139	S120 and S126	USPAT; UPAD	OR	ON	2015/06/02 14:15
S132	102	S120 and S128	USPAT; UPAD	OR	ON	2015/06/02 14:16
S133	76	S131 and @ad<"20100904"	USPAT;	OR	ON	2015/06/02

			UPAD			14:16
S134	66	S132 and @ad<"20100904"	USPAT; UPAD	OR	ON	2015/06/02 14:16

6/ 13/ 2015 6:08:59 PM
C:\ Users\ jedouard\ Documents\ EAST\ Workspaces\ 12876113.wsp

URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126



**Courtesy Reminder for
Application Serial No: 12/876,113**

Attorney Docket No: 6005.042
Customer Number: 64180
Date of Electronic Notification: 06/22/2015

This is a courtesy reminder that new correspondence is available for this application. If you have not done so already, please review the correspondence. The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

An email notification regarding the correspondence was sent to the following email address(es) associated with your customer number:

stephen@uriartelaw.com
labid@uriartelaw.com
arnold@uriartelaw.com

To view your correspondence online or update your email addresses, please visit us anytime at <https://sportal.uspto.gov/secure/myportal/privatepair>. If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov or call 1-866-217-9197.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

64180 7590 06/22/2015
URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Arnold deGuzman	(Depositor's name)
	(Signature)
08 August 2015	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/876.113	09/04/2010	Ricardo H. BRUCE	6005.042	1607

TITLE OF INVENTION: MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$480	\$0	\$0	\$480	09/22/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
EDOUCARD, JEAN C	2133	711-103000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 **Stephen Uriarte**
 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

BITMICRO Networks, Inc.

Fremont, California

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☒ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Typed or printed name _____

Arnold deGuzman

Date _____

Registration No. _____

08 August 2015

39,955

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	) Confirmation No.: 1607
Ricardo H. Bruce et al.	)
	) Examiner: Jean C. Edouard
Serial No.: 12/876,113	) Ph: 571-270-1683
	)
Filing Date: Sept. 4, 2010	) Art Unit: 2133
	)
Title: Multi-Profile Memory	) Atty. Docket No.: 6005.042
Controller For Computing	)
Devices	) Customer No. 64180
	)

Mail Stop ISSUE FEE
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

COMMENTS ON STATEMENT OF REASONS OR ALLOWANCE

Dear Sir:

Applicants thank the Examiner for the granting an allowance of the claims in the above-identified application.

Applicants agree that the Examiner has accurately stated one or more reasons for allowance of the claims. However, the claims may include other patentable aspects that were not identified by the Examiner. This response is submitted to avoid the possibility of any unnecessary limitation on the scope of the claims which might result from the stated reason for allowance. This response is being submitted concurrently with the issue fee payment.

REMARKS/ARGUMENTS

Favorable action is respectfully requested.

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (805) 569-1600.

Date: August 8, 2015

Respectfully submitted,

_____/Arnold de Guzman/_____
 Arnold de Guzman
 Attorney for Applicant(s)
 Reg. No. 39,955
 805-569-1600

Please send correspondence to:
 Customer No. 64180

CERTIFICATE OF TRANSMISSION OR MAILING 37 C.F.R. 1.8			
I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office in accordance with 37 C.F.R. § 1.6(d), or is being transmitted via the Office electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4), or is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below:			
Signature:	/Arnold de Guzman/		
Typed or Printed Name:	Arnold de Guzman	Dated:	August 8, 2015
Express Mail Mailing Number (optional):			

Electronic Patent Application Fee Transmittal				
Application Number:		12876113		
Filing Date:		04-Sep-2010		
Title of Invention:		MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES		
First Named Inventor/Applicant Name:		Ricardo H. BRUCE		
Filer:		Stephen Radcliff Uriarte/Arnold deGuzman		
Attorney Docket Number:		6005.042		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt

EFS ID:	23155878
Application Number:	12876113
International Application Number:	
Confirmation Number:	1607
Title of Invention:	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES
First Named Inventor/Applicant Name:	Ricardo H. BRUCE
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte/Arnold deGuzman
Filer Authorized By:	Stephen Radcliff Uriarte
Attorney Docket Number:	6005.042
Receipt Date:	08-AUG-2015
Filing Date:	04-SEP-2010
Time Stamp:	18:30:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$960
RAM confirmation Number	6711
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	fees_transmittal.pdf	1770214	no	1
			872641a15530f1e98f9ee3ec4eca71db9f727864		
Warnings:					
Information:					
2	Miscellaneous Incoming Letter	6005_042_comments.pdf	21312	no	2
			cd0a5f232db74f155605b714a158327f18df8702		
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30907	no	2
			d0a277b439ddc64cea61feebacef167d5bd3cd96		
Warnings:					
Information:					
Total Files Size (in bytes):			1822433		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 2003/0163624 A1	08-28-2003	Matsui et al.	
		US- 2007/0028040 A1	02-01-2007	Alan Welsh Sinclair	
		US- 2006/0095709 A1	05-04-2006	Kyosuke Achiwa	
		US- 20110113186	05-12-2011	Bruce et al.	
		US-			
		US- 20110202709	08-18-2011	Rychlik, Bohuslav	
		US- 8,447,908	04-21-2013	Bruce et al.	
		US- 8,788,725	07-22-2014	Bruce et al.	
		US- 8,560,804	10-15-2013	Bruce et al.	
		US- 2013/0246694	09-19-2013	Bruce et al.	
		US- 2011/0161568	06-30-2011	Bruce et al.	
		US- 2002/0083262	06-27-2002	Fukuzumi, Tomoya	
		US- 2009/0158085	06-18-2009	Kern et al.	
		US- 2009/0172466	07-02-2009	Royer et al.	
		US- 2009/0172250	07-02-2009	Allen et al.	
		US- 2011/0264884	10-27-2011	Sung-joo Kim	
		US- 2014/0104949	04-17-2014	Bruce et al.	
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				

Examiner
Signature

/Jean Edouard/

Date
Considered

06/11/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND**

TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 5,737,742	04-07-1998	Achiwa et al.	
		US- 5,802,554	09-01-1998	Caceres et al.	
		US- 5,819,307	10-06-1998	Iwamoto et al.	
		US- 2002/0141244	10-03-2002	Bruce et al.	
		US- 2009/0094411	04-09-2009	Que, Jinzhen	
		US- 2007/0130439	06-07-2007	Andersson et al.	
		US- 7,660,941	02-09-2010	Lee et al.	
		US- 5,644,784	07-01-1997	Peek	
		US- 2009/0158085	06-18-2009	Kern et al.	
		US- 2009/0172466	07-02-2009	Royer et al.	
		US- 2009/0172250	07-02-2009	Allen et al.	
		US- 2011/0264884	10-27-2011	Kim, Sung-joo	
		US- 8,713,417	04-29-2014	Jo, Namphil	
		US- 8,510,631	08-13-2013	Wu et al.	
		US- 8,375,257	02-12-2013	Hong et al.	
		US- 8,707,134	04-22-2014	Takahashi et al.	
		US- 7,174,438	02-06-2007	Homma et al.	
		US-			
		US-			

Change(s) applied
to document,
/J.E./
7/8/2015

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				

Examiner
Signature

/Jean Edouard/

Date
Considered

06/11/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND**

TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.E./

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 4

of 7

Complete if Known

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 5,875,351	02-23-1999	D. Riley	
		US- 5,881,264	03-09-1999	Y. Kurosawa	
		US- 5,918,033	06-29-1999	Heeb et al.	
		US- 5,943,421	08-24-1999	R. Grabon	
		US- 6,298,071	10-02-2001	Taylor et al.	
		US- 6,363,441	03-26-2002	Beniz et al.	
		US- 6,363,444	03-36-2002	Platko et al.	
		US- 6,404,772	06-11-2002	Beach et al.	
		US- 6,526,506	02-25-2003	D. Lewis	
		US- 6,557,095	04-29-2003	A. Henstrom	
		US- 6,857,076	02-15-2005	D. Klein	
		US- 6,970,446	11-29-2005	Krischar et al.	
		US- 7,194,766	03-20-2007	Noehring et al.	
		US- 7,372,962	06-13-2008	Fujimoto et al.	
		US- 7,620,748	11-17-2009	Bruce et al.	
		US- 7,716,389	05-11-2010	Bruce et al.	
		US- 2002/0073324	06-13-2002	Hsu et al.	
		US- 2007/0019573	01-25-2007	M. Nishimura	
		US- 2007/0083680	04-12-2007	King et al.	

Change(s) applied
to document,
/J.E./
7/8/2015

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				

Examiner
Signature

/Jean Edouard/

Date
Considered

06/11/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.E./



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/876,113	09/15/2015	9135190	6005.042	1607

64180 7590 08/26/2015
URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 277 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Ricardo H. BRUCE, Union City, CA;
Marlon B. VERDAN, Paranaque City, PHILIPPINES;
Margaret Anne N. SOMERA, Caloocan City, PHILIPPINES;
Rowenah Michelle D. JAGO-ON, Pasig City, PHILIPPINES;
Maria Eliza B. DE BELEN, Quezon City, PHILIPPINES;
Ron Kelvin B. PALACOL, Laguna, PHILIPPINES;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT4586333

SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	ASSIGNMENT	
CONVEYING PARTY DATA		
Name		Execution Date
BITMICRO NETWORKS, INC.		06/30/2017
RECEIVING PARTY DATA		
Name:	BITMICRO LLC	
Street Address:	1620 N. WACCAMAW DRIVE	
Internal Address:	SUITE 109	
City:	MURRELLS INLET	
State/Country:	SOUTH CAROLINA	
Postal Code:	29576	
PROPERTY NUMBERS Total: 34		
Property Type	Number	
Patent Number:	6496939	
Patent Number:	9372755	
Patent Number:	6970890	
Patent Number:	7729370	
Patent Number:	7826243	
Patent Number:	8093103	
Patent Number:	6317330	
Patent Number:	9423457	
Patent Number:	9552848	
Patent Number:	6744635	
Patent Number:	7716389	
Patent Number:	8165301	
Patent Number:	7620748	
Patent Number:	9400617	
Patent Number:	9672178	
Patent Number:	9043669	
Patent Number:	7613876	
Patent Number:	8032700	
Patent Number:	9430386	

Property Type	Number
Patent Number:	9734067
Patent Number:	6000006
Patent Number:	5822251
Patent Number:	9099187
Patent Number:	8560804
Patent Number:	9484103
Patent Number:	8010740
Patent Number:	7506098
Patent Number:	8447908
Patent Number:	8788725
Application Number:	14297628
Patent Number:	6529416
Patent Number:	5956743
Patent Number:	9135190
Patent Number:	6757845

CORRESPONDENCE DATA

Fax Number: (512)391-2173

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 512.236.2023

Email: rdewanipdocket@jw.com

Correspondent Name: JACKSON WALKER L.L.P.

Address Line 1: 100 CONGRESS AVENUE

Address Line 2: SUITE 1100

Address Line 4: AUSTIN, TEXAS 78701

NAME OF SUBMITTER:	HEATHER BUCEK
SIGNATURE:	/heather bucek/
DATE SIGNED:	09/08/2017
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 8

source=BitMicro Recordable Assignment#page1.tif

source=BitMicro Recordable Assignment#page2.tif

source=BitMicro Recordable Assignment#page3.tif

source=BitMicro Recordable Assignment#page4.tif

source=BitMicro Recordable Assignment#page5.tif

source=BitMicro Recordable Assignment#page6.tif

source=BitMicro Recordable Assignment#page7.tif

source=BitMicro Recordable Assignment#page8.tif

RECORDABLE ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, **BITMICRO Networks, Inc.**, a California company having offices at 47929 Fremont Blvd., Fremont, CA 94538 ("*Assignor*") and **BITMICRO LLC**, a Delaware Company having offices at 1620 N. Waccamaw Drive, Suite 109, Murrells Inlet, SC 29576 does hereby sell, assign, transfer, and convey unto (hereafter "*Assignee*") all its right, title, and interest in and to any and all of the following (collectively, the "*Patent Rights*");

(a) the patent applications and patents listed in the table below and any issued patent or patent application that directly or indirectly claims or is amended to claim priority to any of the above, in whole or in part (the "*Patents*");

(b) to the extent not included in Section (a) above, all issued patents, rights to inventions and pending and future applications for patents under U.S. law or regulation or any foreign country with respect to the patentable inventions from which such Patents arise, including without limitation, utility patents, utility models, design patents, invention certificates, provisional, reissues, reexaminations, extensions, continuations, continuations-in-part, continuing prosecution applications, requests for continuing examinations, divisionals, renewals, and registrations in all countries of the world, as well as any patents and patent applications to which any of the Patents or the foregoing directly or indirectly claim priority, in whole or in part;

(c) all related patent filing and prosecution documents;

(d) rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections, or other governmental grants or issuances of any type related to any of the Patents and the inventions, invention disclosures, and discoveries therein;

(e) all inventions and discoveries described in any of the Patents or subject matter capable of being reduced to a patent claim in any of the Patents based on the specification of any of the Patents;

(f) priority rights in any and all patent filings available from and/or through the Patents; and

(g) causes of action (whether known or unknown or whether currently pending, filed, or otherwise) and other enforcement rights under, or on account of any of the Patents or of any patent that issues from any of the Patents, including, without limitation, all causes of action and other enforcement rights for (1) damages, (2) injunctive relief, and (3) any other remedies of any kind for past, current and future infringement and all of the proceeds from the foregoing, that are accrued and unpaid or that are hereafter accruing;

(h) rights to collect royalties or other payments under or on account of any of the Patents and/or any of the foregoing categories (a) through (g); and

(i) rights of cooperation assigned or granted by any third party under or on account of any of the Patents and/or any of the foregoing categories (a) through (h).

Assignor represents, warrants and covenants that:

Assignor has the full power and authority, and has obtained all third-party consents, approvals and/or other authorizations required to enter into this Agreement and to carry out its obligations hereunder, including the assignment of the Patent Rights to Assignee.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

The terms and conditions of this Assignment of Patent Rights will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed at

Fremont, CA on 30 JUNE 2017

Assignor:

BITMICRO Networks, Inc.

By: [Signature]

Name: Stephen R. Uriarte

Title: President & General Counsel

STATE OF CALIFORNIA)

COUNTY OF Alameda) ss.

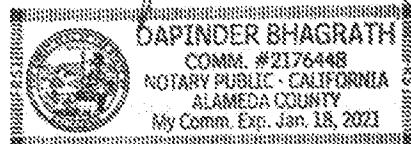
On June 30th, 2017, before me, DAPINDER BHAGRATH, Notary Public in and for said State, personally appeared STEPHEN R. URIARTE, personally known to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed to the within instrument and acknowledged to me that he/she executed the same in his/her authorized capacity, and that by his/her signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

WITNESS my hand and official seal.

Signature

[Signature]

(Seal)



Group No. 1: PowerGuard and Data Recovery				NVM-only. (Volatile RAM + NVM) Solutions
Group No.	Country	Patent Number	Issue/Priority	Title
1	(A) US	6496939**	2002-12-17/ 1999-09-21	Method and System for Controlling data in a Computer System in the event of a power failure
1	(A) Taiwan	189445	2004-02-20 / 1999-09-21	Method and System for Controlling data in a Computer System
1	(A) Canada	2,388,496	2002-12-17/ 1999-09-21	Method and System for Controlling data in a Computer System
1	(A) EP	App. No: 00961417.3	Filed 2002- 04-18 / Priority 1999- 09-21	Method and System for Controlling data in a Computer System
1	(B) US	9,372,755	2106-06-21/ 2011-10-05	Adaptive power cycle sequences for data recovery
1	(B) US	App. No. 15/176,156	Filed 2016- 06-08 / Priority 2011- 10-05	Adaptive power cycle sequences for data recovery
1	US	6,970,890	2005-11-29/ 2000-12-20	Method and apparatus for data recovery

(A & B) Identifies Different Priority Families; All Others Are Single Patents

Group No. 2: Networking+ Flash				Networked-attached Storage Devices (Filesystem / Block IO)
Group No.	Country	Patent Number	Issue/Priority	
2	US	6981070**	2005-12-27/ 2000-07-12 (+552 PTA)	Network storage device having solid-state non-volatile memory
2	US	7,729,370	2010-06-01/ 2005-08-19 (+861 PTA)	Apparatus for networking devices having fibre channel node functionality

Group No. 3: Casings, PCB, and ASIC				SSD/Acceleration Devices/ASIC design
Group No.	Country	Patent Number	Issue/Priority	
3	(C) US	7826243**	2010-11-2 / 2005-12-29 (+747 PTA)	Multiple chip module and package stacking for storage devices
3	(C) US	8093103	2012-1-10 / 2005-12-29	Multiple chip module and package stacking for storage devices
3	(C) Taiwan	I332701853	2010-11-1 / 2005-12-29	Multiple Chip Module and Package Stacking Method For Storage Devices
3	(C) Korea	10-1391068	2014-4-24 / 2005-12-29	Multiple Chip Module and Package Stacking Method For Storage Devices
3	(C) Japan	5,745,730	2015-04-27 / 2005-12-29	Multiple Chip Module and Package Stacking Method For Storage Devices
3	(C) Japan	5,859,181	2015-12-08 / 2005-12-29	Multiple Chip Module and Package Stacking Method For Storage Devices
3	(C) China	101375391B	2010-12-28 / 2005-12-29	Multiple Chip Module and Package Stacking Method For Storage Devices
3	(D) US	6317330	2001-11-13 / 2000-2-15	Printed circuit board assembly
3	(D) China	CN 1423917	2006-02-08 / 2000-2-15	Printed circuit board assembly
3	(D) Israel	151278	2007-06-01 / 2000-2-15	Printed circuit board assembly
3	(D) Taiwan	I228211	2005-02-21 / 2000-2-15	Printed circuit board assembly
3	(D) Japan	4,397,143	2009-10-30 / 2000-2-15	Printed circuit board assembly
3	(E) US	9,423,457	2016-8-23 / 2013-3-14 (+102 PTA)	Self-Test Solution For Delay Locked Loops
3	(E) US	App. No. 15/232,801	Filed 2016- 08-09 / priority 2013- 3-14	Self-Test Solution For Delay Locked Loops
3	(F) US	8665601	2014-3-4 / 2009-9-4 (+500 PTA)	Solid state drive with improved enclosure assembly
3	(F) US	9,552,848	Filed 2014--2- 18 / priority 2010-9-4	Solid state drive with improved enclosure assembly

3	(F) US	App. No. 15/414,504	Filed 2017-1-24 / priority 2010-9-4	Solid state drive with improved enclosure assembly
3	US	6,744,635	2004-6-1 / 2000-2-15	Removable Visual Indication Structure For A Printed Circuit Board

(C thru F) Identifies Different Priority Families; All Others Are Single Patents

Group No. 4: DMA and Security			Performance, Hardware Acceleration, Security for NVM and Non-NVM	
Group No.	Country	Patent Number	Issue/Priority	
4	US	7716389	2010-05-11 / 2006-03-17	Direct memory access controller with encryption and decryption for non-blocking high bandwidth I/O transactions
4	US	8165301	2012-04-24 / 2006-04-04	Input-output device and storage controller handshake protocol using key exchange for data security
4	US	7620748	2009-11-17 / 2006-04-06	Hardware assisted non-volatile memory-to-input/output direct memory access (DMA) transfer
4	(G) US	9400617	2016-07-26 / 2013-03-15	Hardware-assisted DMA transfer with dependency table configured to permit-in parallel-data drain from cache without processor intervention when filled or drained
4	(G) US	App. No. 15/217,947	Filed 2016-07-22 / Priority 2013-03-15	Hardware-Assisted DMA Transfer with Dependency
4	(G) US	9672178	2017-06-06 / Priority 2013-03-15	Bit-Mapped Dependency Table
4	(G) US	App. No. 15/603,434	Filed 2017-05-23 / Priority 2013-03-15	Bit-Mapped Dependency Table

(G) Identifies A Priority Family; All Others Are Single Patents

Group No. 5: Flash-and-ECC related Patents			SSDs / FlashDevices (Flash, Profile, ECC, Firmware)	
Group No.	Country	Patent Number	Issue/Priority	
5	(H) US	9043669++	2015-05-26 / 2012-05-18	Distributed ECC engine for storage media
5	(H) US	App. No. 14/708,246	Filed 2015-05-09 / Priority 2012-05-18	Storage System With Distributed ECC Capability
5	(I) US	8959307++	2015-02-17 / 2007-11-16	Reduced latency memory read transactions in storage devices

5	(I) US	App. No. 14/616,700	Filed 2015- 02-02 / Priority 2007- 11-16	Memory Transaction With Reduced Latency
5	(I) US	App. No. 14/866,946	Filed 2015- 09-26 / Priority 2007- 11-16	Reduced latency memory read transactions in storage devices
5	(I) US	App. No. 15/268,533	Filed 2016- 09-16 / Priority 2007- 11-16	Memory Interface With An Expandable Architecture That Provides Reduced Latency
5	(I) US	App. No. 15/268,536	Filed 2016- 09-16 / Priority 2007- 11-16	Multi-Dimensional Memory
5	(I) US	App. No. 15/368,598	Filed 2016- 12-03 / Priority 2006- 11-16	Computer Storage System With Reduced Latency
5	(J) US	7613876++	2009-11-03 / 2006-06-08	HYBRID MULTI-TIERED CACHING STORAGE SYSTEM
5	(J) US	8032700++	2011-10-04 / 2006-06-08	HYBRID MULTI-TIERED CACHING STORAGE SYSTEM
5	(J) Taiwan	I438628	2014-05-21 / 2006-06-08	DATA STORAGE SYSTEM AND DATA STORAGE MEDIUM
5	(J) Taiwan	I525431	Filed 2014- 02-17 / 2006- 06-08	Data Storage System, Data Structure and Data Storage Method
5	(N) Taiwan	I420307	2013-12-21 / 2006-06-08	Optimized placement policy for solid state storage devices
5	(N) Taiwan	I540430	2016-07-01 / 2005-06-08	Method for data storage
5	(K) US	9430386++	2016-08-30 / 2013-03-15	Multi-leveled cache management in a hybrid storage system
5	(K) US	App. No. 15/249,475	Filed 2016- 08-29 / Priority 2013- 03-15	Multi-leveled cache management in a hybrid storage system
5	(K) US	App. No. 14/689,045	Filed 2015- 04-16 / Priority 2013- 03-15	Write Buffering
5	(L) US	6000006	1999-12-07 / 1997-08-25	UNIFIED RE-MAP AND CACHE-INDEX TABLE WITH DUAL WRITE-COUNTERS FOR WEAR-LEVELING OF NON-VOLATILE FLASH RAM MASS STORAGE

5	(L) US	5822251	1998-10-13 / 1997-09-29	Expandable flash-memory mass-storage using shared buddy lines and intermediate flash-bus between device-specific buffers and flash-intelligent DMA controllers
5	(M) US	9099187	2015-08-04 / 2009-09-14	Reducing erase cycles in an electronic storage device that uses at least one erase-limited memory device
5	(M) US	8560804	2013-10-15 / 2009-09-14	Reducing erase cycles in an electronic storage device that uses at least one erase-limited memory device
5	(M) US	9484103	2016-11-1 / 2009-09-14	Electronic Storage Device
5	(M) US	App. No. 15/269,967	Filed 2016- 09-19 / priority 2009- 09-14	Electronic Storage Device
5	(N) US	8010740	2011-08-30 / 2008-11-25	Optimizing memory operations in an electronic storage device
5	(N) US	7506098	2009-03-17 / 2006-06-08	Optimized placement policy for solid state storage devices
5	(O) US	8447908	2013-04-21 / 2009-09-07	Multilevel memory bus system for solid-state mass storage
5	(O) US	8788725	2014-7-22 / 2009-09-07	Multilevel memory bus system for solid-state mass storage
5	(O) US	App. No. 14/297,628	2014-06-06 / 2009-09-07	Multilevel memory bus system
5	US	6529416	2003-03-04 / 2000-11-30	Parallel erase operations in memory systems
5	US	5956743	1999-09-21 / 1997-09-29	TRANSPARENT MANAGEMENT AT HOST INTERFACE OF FLASH-MEMORY OVERHEAD-BYTES USING FLASH-SPECIFIC DMA HAVING PROGRAMMABLE PROCESSOR-INTERRUPT OF HIGH-LEVEL OPERATIONS
5	US	9135190	2015-09-15 / 2009-09-04	Multi-profile memory controller for computing devices
5	US	6757845	2004-06-29 / 2000-11-30	Method and apparatus for testing a storage device
5	US	Appl. No. 15/482,684	Filed 2017- 04-07	Multi-Dimensional Computer Storage System Note: this application was decided to be filed without any priority claim; option available for this application to be a continuation application that claims benefit to 15/268,536 and/or 15/268,533 (family (I))

(H thru O) Identifies Different Priority Families; All Others Are Single Patents

Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

**PATENT - POWER OF ATTORNEY
OR
REVOCATION OF POWER OF ATTORNEY
WITH A NEW POWER OF ATTORNEY
AND
CHANGE OF CORRESPONDENCE ADDRESS**

Patent Number	9135190
Issue Date	09/15/2015
First Named Inventor	Ricardo Bruce
Title	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES
Attorney Docket No.	150962.00001

I hereby revoke all previous powers of attorney given in the above-identified patent.

☐ A Power of Attorney is submitted herewith.

OR
☒ I hereby appoint Practitioner(s) associated with the Customer Number identified in the box at right as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

67942

OR
☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified patent to:

☒ The address associated with the above-identified Customer Number.

OR

☐ The address associated with the Customer Number identified in the box at right:

OR

☐ Firm or
Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the:

☐ Inventor, having ownership of the patent.

OR

☒ Patent owner.

Statement under 37 CFR 3.73(c) (Form PTO/SB/96) submitted herewith or filed on _____

SIGNATURE of Inventor or Patent Owner

Signature

Name

Title and Company

Manager, BITMICRO LLC

Date

Telephone

NOTE: Signatures of all the inventors or patent owners of the entire interest or their representative(s) are required. If more than one signature is required, submit multiple forms, check the box below, and identify the total number of forms submitted in the blank below.

☐ A total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 15 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 3.

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: Bitmicro LLCApplication No./Patent No.: 9135190Filed/Issue Date: 09/15/2015Titled: MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICESBitmicro LLC, a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):1. ☒ The assignee of the entire right, title, and interest.2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):☐ The extent (by percentage) of its ownership interest is ____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:1. From: Inventors To: Bitmicro Networks, Inc.

The document was recorded in the United States Patent and Trademark Office at

Reel 025149, Frame 0398, or for which a copy thereof is attached.2. From: Inventor To: Bitmicro Networks, Inc.

The document was recorded in the United States Patent and Trademark Office at

Reel 025314, Frame 0661, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)3. From: Bitmicro Networks, Inc. To: Bitmicro, LLC

The document was recorded in the United States Patent and Trademark Office at
 Reel 043536, Frame 0407, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature

Bruce K. Lagerman

Printed or Typed Name

Date

Manager

Title or Registration Number

[Page 2 of 2]

Electronic Acknowledgement Receipt

EFS ID:	30553892
Application Number:	12876113
International Application Number:	
Confirmation Number:	1607
Title of Invention:	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES
First Named Inventor/Applicant Name:	Ricardo H. BRUCE
Customer Number:	64180
Filer:	Raman N. Dewan/Heather Bucek
Filer Authorized By:	Raman N. Dewan
Attorney Docket Number:	6005.042
Receipt Date:	03-OCT-2017
Filing Date:	04-SEP-2010
Time Stamp:	15:38:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		9135190_POA.pdf	3804524	yes	3
			e5d77c7c33502a0316104a95a75a528066a ebd49		

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Power of Attorney	1	1
	Assignee showing of ownership per 37 CFR 3.73	2	3
Warnings:			
Information:			
Total Files Size (in bytes):		3804524	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/876,113	09/04/2010	Ricardo H. BRUCE	6005.042

64180
Uriarte Law
5255 Stevens Creek Blvd.
Santa Clara, CA 95051

CONFIRMATION NO. 1607
POWER OF ATTORNEY NOTICE



OC00000094618004

Date Mailed: 10/10/2017

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/03/2017.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/yfeferra/



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/876,113	09/04/2010	Ricardo H. BRUCE	150962.00001

CONFIRMATION NO. 1607

POA ACCEPTANCE LETTER



67942
JACKSON WALKER L.L.P.
ATTN: INTELLECTUAL PROPERTY DEPARTMENT
100 CONGRESS AVENUE
SUITE 1100
AUSTIN, TX 78701

Date Mailed: 10/10/2017

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/03/2017.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/yfeferra/

Organization

Bldg./Room

UNITED STATES PATENT AND TRADEMARK OFFICE

P.O. Box 1450

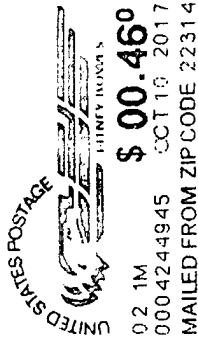
Alexandria, VA. 22313-1450

If Undeliverable Return In Ten Days

Official Business

Penalty For Private Use, \$300

AN EQUAL OPPORTUNITY EMPLOYER



02 1M
000 424 4945
OCT 19 2017
\$ 00.46⁰
MAILED FROM ZIP CODE 22314

NIXIE 296 DE 1 0010/23/17

RETURN TO SENDER
INSUFFICIENT ADDRESS
UNABLE TO FORWARD

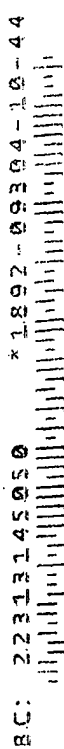
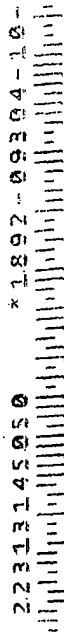
BC: 22313145050 *1892-09304-10-44

22313>1450

VS 0300

VS 0300

31

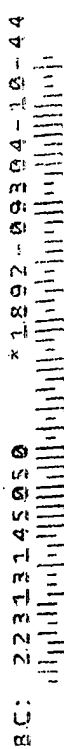
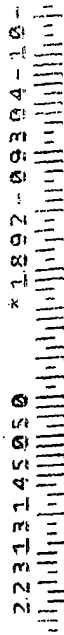


22313>1450

VS 0300

VS 0300

31



22313>1450



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/876,113	09/04/2010	Ricardo H. BRUCE	150962.00001

CONFIRMATION NO. 1607

POA ACCEPTANCE LETTER



67942
JACKSON WALKER L.L.P.
ATTN: INTELLECTUAL PROPERTY DEPARTMENT
100 CONGRESS AVENUE
SUITE 1100
AUSTIN, TX 78701

Date Mailed: 10/10/2017

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/03/2017.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/yterferra/

Organization _____ Bldg./Room _____

UNITED STATES PATENT AND TRADEMARK OFFICE

P.O. Box 1450

Alexandria, VA. 22313-1450

If Undeliverable Return In Ten Days

Official Business

Penalty For Private Use, \$300

AN EQUAL OPPORTUNITY EMPLOYER



UNITED STATES POSTAGE
02 1M
0004244945
MAILED FROM ZIP CODE 22314

\$ 00.46⁰

OCT 10 2017

MAILED FROM ZIP CODE 22314

PTS NO SUCH RECIPIENT
NO LONGER HERE

Added

NIXIE 957 FE 1 0002/18/18

RETURN TO SENDER
NOT DELIVERABLE AS ADDRESSED
UNABLE TO FORWARD

BC: 22313145050 ~ 2892-09303-10-44

9505136554 UTC CO

9505136554



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/876,113	09/04/2010	Ricardo H. BRUCE	6005.042

64180
Uriarte Law
5255 Stevens Creek Blvd.
Santa Clara, CA 95051



CONFIRMATION NO. 1607
POWER OF ATTORNEY NOTICE



Date Mailed: 10/10/2017

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/03/2017.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/yterferra/

TO: **Mail Stop 8**
Director of the U.S. Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

**REPORT ON THE
FILING OR DETERMINATION OF AN
ACTION REGARDING A PATENT OR
TRADEMARK**

In Compliance with 35 § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Northern District of California on the following:

(X) Patents or () Trademarks

DOCKET NO:
18-cv-03505-NC

DATE FILED:
June 12, 2018

UNITED STATES DISTRICT COURT
Robert F. Peckham Federal Building
280 South 1st Street
San Jose, CA 95113

PLAINTIFF:
SK hynix Inc.

DEFENDANT:
BiTMICRO, LLC

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1. No. 6,529,416	March 4, 2003	BiTMICRO
2. No. 7,826,243	November 2, 2010	BiTMICRO
3.No. 8,093,103	January 10, 2012	BiTMICRO
4.No 9,135,190	September 15, 2015	BiTMICRO
5.		

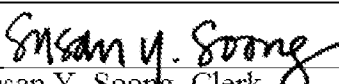
In the above-entitled case, the following patent(s) have been included.

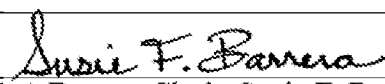
DATE INCLUDED INCLUDED BY:
() Amendment () Answer () Cross Bill () Other Pleading

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1.		
2.		
3.		
4.		
5.		

In the above-entitled case, the following decision has been rendered or judgment issued:

DECISION/JUDGEMENT:


Susan Y. Soong, Clerk


(by) Deputy Clerk, Susie F. Barrera

Copy 1 – Upon initiation of action, mail this copy to Commissioner
Copy 2 – Upon filing document adding patent(s) mail this copy to Commissioner
Copy 3 – Upon termination of action, mail this copy to the Commissioner
Copy 4 – Case file copy



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY.DOCKET NO./TITLE	REQUEST ID
12/876,113	09/04/2010	Ricardo H. BRUCE	150962.00066	80469

Acknowledgement of Change to Small Entity Status

The entity status change request below filed through Private PAIR on 01/30/2019 has been accepted.

CERTIFICATIONS:

Change of Entity Status:

× Applicant asserting small entity status. See 37 CFR 1.27.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

This portion must be completed by the signatory or signatories making the entity status change in accordance with 37 CFR 1.4(d)(4).

Signature:	/joseph p lally/
Name:	Joseph P. Lally
Registration Number:	38947



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY.DOCKET NO./TITLE	REQUEST ID
12/876,113	09/04/2010	Ricardo H. BRUCE	150962.00066	148590

Acknowledgement of Loss of Entitlement to Entity Status Discount

The entity status change request below filed through Private PAIR on 09/27/2021 has been accepted.

CERTIFICATIONS:

Change of Entity Status:

× Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be notification of loss of entitlement to small or micro entity status, as applicable.

This portion must be completed by the signatory or signatories making the entity status change in accordance with 37 CFR 1.4(d)(4).

Signature:	/joseph p lally/
Name:	Joseph P. Lally
Registration Number:	38947



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	REQUEST ID
12/876,113	9135190	2133	149252

PAIR Correspondence Address/Fee Address Change

The following fields have been changed to Customer Number 183214 on 10/05/2021 via Private PAIR in view of the certification copied below that authorized the change.

- Correspondence Address

The address for Customer Number 183214 is:

183214

Jackson Walker LLP

Bitmicro / Oyster Optics

100 CONGRESS AV

STE 1100

AUSTIN, TX 78701

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

An attorney or Agent of Record registered to practice before the Patent and Trademark Office who has been given power of attorney in this application

Signature:	/joseph p lally/
Name:	Joseph P. Lally
Registration Number:	38947



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	REQUEST ID
12/876,113	9135190	2133	149252

PAIR Correspondence Address/Fee Address Change

The following fields have been changed to Customer Number 183214 on 10/05/2021 via Private PAIR in view of the certification copied below that authorized the change.

- Maintenance Fee Address

The address for Customer Number 183214 is:

183214

Jackson Walker LLP

Bitmicro / Oyster Optics

100 CONGRESS AV

STE 1100

AUSTIN, TX 78701

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

An attorney or Agent of Record registered to practice before the Patent and Trademark Office who has been given power of attorney in this application

Signature:	/joseph p lally/
Name:	Joseph P. Lally
Registration Number:	38947

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
---	---

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 6:22-cv-331	DATE FILED	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF BiTMICRO LLC		DEFENDANT KIOXIA AMERICA, INC.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 9,135,190	9/15/2015	BiTMICRO LLC
2 8,010,740	8/30/2011	BiTMICRO LLC
3 6,496,939	12/17/2002	BiTMICRO LLC
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
-------	-------------------	------

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AD 126 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
---	--

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
 filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.)

DOCKET NO. 6:22-cv-335	DATE FILED 3/30/2022	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF BITMICRO LLC		DEFENDANT INTEL CORPORATION
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,826,243	11/2/2010	BITMICRO LLC
2 9,135,190	9/15/2015	BITMICRO LLC
3 8,010,740	3/30/2011	BITMICRO LLC
4 9,858,084	1/2/2013	BITMICRO LLC
5 10,120,694	11/6/2018	BITMICRO LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading		
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK	
1			
2			
3			
4			
5			

In the above—entitled case, the following decision has been rendered or judgment issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
-------	-------------------	------

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
---	---

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas on the following:

☐ Trademarks or ☒ Patents (☐ the patent action involves 35 U.S.C. § 292.)

DOCKET NO. 6:22-cv-335	DATE FILED 3/30/2022	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF BITMICRO LLC		DEFENDANT INTEL CORPORATION
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
6 6,496,939	12/17/2002	BITMICRO LLC
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY	
	☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy