

Technical Article

Selecting And Implementing NAND Flash Mass Storage In Embedded Applications

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Mass storage densities are in an unprecedented state of growth in embedded applications. Consumer devices such as portable media players, cellular phones, digital still cameras, portable navigation devices, air cards, and thumb drives are requiring higher densities of mass storage due to widespread demand for increased multimedia capacity.

NAND flash has become the prevalent choice for mass storage in consumer applications due to its lower cost per bit and higher density advantages over **NOR Flash**, as well as its smaller size, power, and robustness advantages over Hard Disk Drives.

Because demands are so high for NAND flash in the consumer market, storage prices are decreasing dramatically and other devices such as point of sale (POS) terminals, printers, and other applications, can take advantage and use higher density storage at these lower costs.

However, as the demand for increased NAND flash density surges in these embedded applications, designers are faced with the challenge of selecting from a variety of NAND flash types, densities, vendors, and roadmaps as well as implementations.

The first and most important selection criterion for using NANDflash is the implementation of the NAND controller. All NAND flash devices require maintenance overhead located in the software and hardware of an external controller to ensure reliable data, maximize the lifespan of the NAND flash device and to enhance performance. The three main functions of the NAND controller are Bad Block Management, Wear-Leveling, and Error Correction Coding (ECC).

NAND flash stores memory in clusters called blocks. Most NAND flash devices will inherently be built with some bad blocks that will be found upon testing conducted during manufacturing, and these blocks will be labeled as bad in the device specification by the vendor.

In addition, good blocks may degrade over the life cycle of the NAND and must be tracked via software, aka, Bad Block Management. Additionally, consistent reads and writes to a particular block may cause the block to "wear out" and become a bad block. In order to ensure maximum life of the NAND and limit the amount of blocks that wear out, all blocks should be read and written to evenly in a process called Wear-Leveling.

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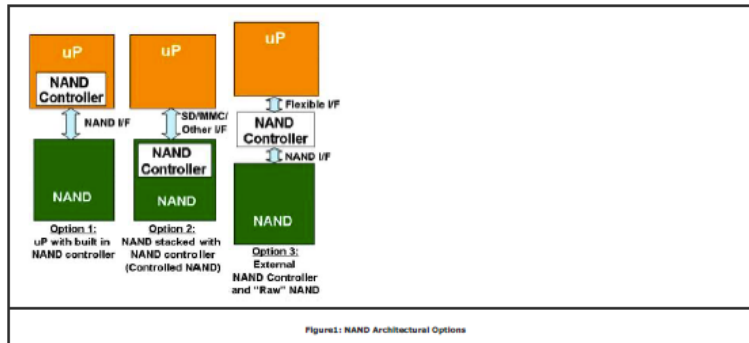


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Finally, bit errors may occur due to inactivity or operation of a particular cell and ECC must be implemented in either software or hardware to detect and correct these errors. ECC is typically defined by the industry as the number of bits the code can correct per 528-byte sector. In a system, this NAND controller can be combined with the NAND in the three different configurations as shown in Figure 1 below.



In conjunction with selecting from the three options of NAND solutions shown in Figure 1 above, a designer must also choose between two types of NAND flash devices, SLC (Single-Level Cell) NAND and MLC (Multi-Level Cell) NAND, each of which offers its own benefits.

SLC NAND provides longer life cycle and reliability of each block, therefore requiring less ECC and offering superior performance. MLC NAND offers less performance and is more difficult to implement since it requires higher levels of bad block management, wear-leveling and ECC.

However, it is also roughly 1/3rd of the price of SLC NAND per bit. Because of the increasing differential of cost between SLC and MLC NAND, most applications are moving to MLC NAND, especially in high-density type applications, in order to substantially decrease bill of material costs.

The selection of one of the three options in Figure 1 above is based upon multiple factors including Microprocessor NAND controller support, the type of NAND being used (SLC or MLC), and the density of NAND required on the platform.

In platforms where designers are using a Microprocessor that has a full NAND interface and controller, Option 1 is typically the preferred choice. Most contemporary microprocessors, if they have any support for NAND at all, typically only support SLC NAND in lower densities.

The process technology limits the amount of storage on a die of SLC or MLC NAND, as currently this density is at about one gigabyte of storage per die. Therefore, in order to support higher densities of NAND, a controller must be able to support multiple NANDs.

This is usually done using an interleaving process and multiple chip-enables. The addition of multiple chip-enables to support multiple NANDs can drive the pin count of a microprocessor higher, which makes inclusion of this type of NAND controller into the microprocessor less prevalent.

Also, the MLC NAND interface is very rarely seen on microprocessors for a number of reasons. As process technologies nodes of MLC NAND move lower, the levels of Error Correction Coding required to support this type of NAND become higher.

Currently, the levels of ECC needed for MLC NAND are at 4-bit, but are quickly moving to 8- and 12-bit. The higher amounts of ECC require hardware in the NAND controller. However, microprocessor evolution is proceeding at a slower pace than the rapidly evolving MLC NAND.

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The "Controlled NAND" approach (Option 2) is useful with many different embedded and removable types of storage. All portable SD/MMC cards use this type of implementation, and there are several choices for embedded controlled NANDs in the marketplace. This approach has its advantages as the Microprocessor only needs to support an SD/MMC type interface to add system support for either SLC or MLC NAND.

The controller is stacked with the NAND and handles all Bad Block Management, Wear-Leveling, and ECC for the NAND. Controlled NAND implementations are seen currently at roughly 4 Gigabyte densities in embedded applications and at 8 Gigabyte in removable cards.

The disadvantage with this approach is that each NAND vendor supports different interfaces on their variety of controlled NAND (one may use SD, one may use MMC, another may have a proprietary interface), and switching from one NAND vendor to another requires a complete software overhaul.

Option 3 gives designers the most flexibility in choosing the type of NAND as well as in choosing from different vendors. Almost all NAND controllers support different types, vendors, and densities of NANDs, and because the NAND controller will always utilize the same interface to the processor, the designer is free to choose different types and vendors of NAND without having to change any software.

The block diagram shown in **Figure 2 below** shows a [West Bridge implementation](#) using a multimedia mass storage controller with full SLC and MLC NAND management.



Using a West Bridge interface "similar in nature and purpose to the North and bridges used in PC designs" supports multiple processor interfaces such as SRAM, ADMUX, SPI, and NAND and up to 16 SLC or MLC NAND devices from any NAND vendor with 4-bit ECC.

This gives designers the flexibility of choice regarding density as well as the ability to change NAND vendors on the fly with little to no software changes on the microprocessor. Using an external NAND controller can also provide other benefits.

For instance, a West Bridge that supports a High-Speed USB interface can bypass the main processor and provide a direct path to mass storage from a PC in applications such as portable media players and handsets, giving optimal sideloading performance. Support for SD, MMC, and SDIO interfaces also enables designers to connect an SDIO type device such as WiFi, or Bluetooth if the system's microprocessor is limited on SDIO interfaces.

When considering the combination of requirements for a system's NAND budget, including density, cost, size, and flexibility, designers have several NAND implementation options, each with its own benefits and disadvantages. If the system microprocessor has a built-in SLC or MLC NAND controller, no external device or logic is required.

Otherwise, a controlled NAND approach can be beneficial since it is packaged by the NAND vendor and also requires no external logic or chip. However, for the most flexibility, developers will utilize an external NAND controller to support all NAND types and flavors. This approach also provides additional benefits such as performance and interfaces, but does require an external chip to do so.

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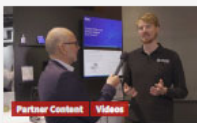
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