

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

BiTMICRO, LLC,
Patent Owner.

Case IPR2023-00779
U.S. Patent No. 9,135,190

PATENT OWNER'S PRELIMINARY RESPONSE

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Pursuant to 37 C.F.R. § 42.107, Patent Owner BiTMICRO, LLC (“BiTMICRO” or “Patent Owner”) files this preliminary response to the Petition, setting forth reasons why the Petition for *inter partes* review (“IPR”) of claims 1-2, 5-8, 11, 19, 29-30, 33, 36-39, 42, 94, and 100 of U.S. Patent No. 9,135,190 (the “’190 Patent”), as requested by Intel Corporation (“Petitioner”), should be denied.¹

I. INTRODUCTION

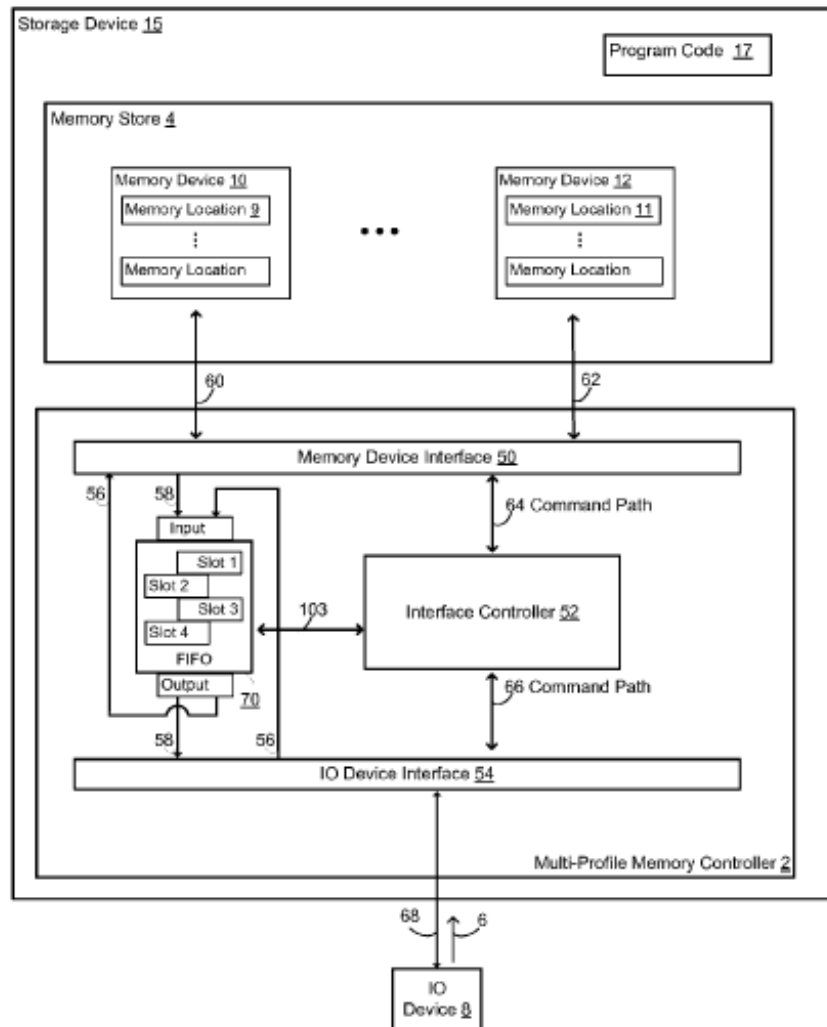
A. The ’190 Patent Discloses and Claims a Novel Memory Controller that Selects a Transfer Size for a Memory Transaction According to Specifically-Claimed Elements

The ’190 Patent discloses a multi-profile memory controller “that can operate with memory locations, memory devices, or both which are associated with different memory attributes, different attribute qualifiers, or the like,” while improving on shortcomings of prior memory controllers. ’190 Pat., Abst. As the ’190 Patent discloses, “[m]ulti-profile memory controllers have been traditionally designed to operate with memory stores or modules that comprise of memory devices which use the *same* memory device characteristics, such as block size.” ’190 Pat., 1:20-24 (emphasis added). For example, the ’190 Patent describes a legacy multi-profile memory controller specifically designed to operate with memory devices that use flash memory cells having “relatively large block sizes.”

¹ By submitting this Preliminary Response, no waiver of any argument is intended by Patent Owner. Patent Owner will have a right to file a complete response to the Petition, should the Board institute *inter partes* review. 37 C.F.R. § 42.120(a).

'190 Pat., 1:24-27. While relatively large block sizes pose some advantages for the memory density and cost efficiency of a device, the '190 Patent also explains some associated disadvantages, including “higher read-modify-write cycle latency, higher random memory access latency and lower random IOPS (input/output operations per second).” '190 Pat., 1:31-43.

The '190 Patent's invention “pertains to a multi-profile memory controller and related methods and systems that can operate with memory locations, memory devices, or both which are associated with different memory attributes, different attribute qualifiers, or the like, while minimizing or avoiding some or all of the disadvantages of the prior art.” '190 Pat., 1:52-60. To further explain these features, the '190 Patent discloses an exemplary storage device 15 having a multi-profile memory controller 2 and a memory store 4. '190 Pat., Fig. 1. The memory store 4 includes a first memory device 10 having a first memory location 9, and a second memory device 12 having a second memory location 11. *Id.* These features are shown in FIG. 1, reproduced below:

**FIG. 1**

Each memory location may have a set of memory attributes, with an attribute defined in the '190 Patent as “a characteristic of a memory location that is related to accessing or addressing the memory location.” '190 Pat., 2:65-3:2.

Attributes may be represented in a device profile 14, such as shown in FIG. 2A.

Page Size <u>16</u>	(# of pages)
Block Size <u>18</u>	(# of blocks)
Memory Protocol <u>20</u>	(Protocol Type Supported)
Mem. Dev. Type <u>22</u>	(Mem. Type)
Partial Page Size <u>23</u>	(# of pages)

FIG. 2A

As described in the '190 Patent, a device profile may include attributes including page size 16, block size 18, memory protocol 20, memory device type 22, and partial page size 23. The page size 16 “corresponds to an attribute value in bytes per page,” block size 18 “corresponds to an attribute value in pages per block,” memory protocol 20 “corresponds to a memory device specification or protocol supported by the memory device associated with the memory location,” memory device type 22 “corresponds to a memory device type of the memory device associated with the memory location,” and partial page size 23 “corresponds to an attribute value in bytes per partial page.” '190 Pat., 3:30-39.

In the memory store 4 of FIG. 1, first memory location 9 and second memory location 11 may have different attributes as reflected on their respective device profiles. As disclosed in FIG. 2B, first memory location 9 may have a device profile 26 with a page size of 1024 bytes per page, a block size of 2048

pages, and a partial page size of 512 bytes per partial page. This device profile 26 is shown in FIG. 2B:

26

Page Size	<u>28</u>	1024
Block Size	<u>30</u>	2048
Memory Protocol	<u>32</u>	ONFi
Mem. Dev. Type	<u>34</u>	NAND Flash
Partial Page Size	<u>36</u>	512

FIG. 2B

As disclosed in FIG. 2C, second memory location 11 may have a device profile 38 with a page size of 512 bytes per page, a block size of 8192 pages, and a partial page size of 256 bytes per partial page. This device profile 38 for second memory location 11 is shown in FIG. 2C:

38

Page Size	<u>40</u>	512
Block Size	<u>42</u>	8192
Memory Protocol	<u>44</u>	ONFi
Mem. Dev. Type	<u>46</u>	NAND Flash
Partial Page Size	<u>48</u>	256

FIG. 2C

As disclosed, multi-profile memory controller 2 serves as a memory controller for both the first memory location 9 and the second memory location 11,

which respectively have different page sizes, block sizes, and partial page sizes from each other.

The '190 Patent describes exemplary embodiments of a transfer size selection as “a function of the data size of the subject to memory transaction request 6, and the attributes in a device profile associated with a target memory location.” '190 Pat., 8:39-42. In an exemplary embodiment, “if the data size is greater than the page size attribute value in device profile 26, multi-profile memory controller 2 uses a transfer size equal to at least the page size attribute value for each memory operation transfer for the memory transaction requested until the remaining data not yet transferred from a requesting IO device is less than the page size attribute.” '190 Pat., 8:50-57. Where the remaining data to be transferred is smaller than the page size attribute value, “multi-profile memory controller can then use a partial page size attribute value for the transfer size of the next memory operation transfer until all of the data has been transferred to memory location 9.” '190 Pat., 8:57-61.

The '190 Patent also discloses “[i]f the data size is greater than the block size attribute value in device profile 24, multi-profile memory controller 2 uses a transfer size equal to at least the block size value for each memory operation transfer for the memory transaction requested until the remaining data not yet transferred is less than the block size attribute value.” '190 Pat., 8:61-66.

Depending on the remaining data size to be transferred, the memory controller selects a transfer size equal to either the page size attribute value or the partial page size attribute value. ’190 Pat., 8:66-9:6. Thus, in these exemplary embodiments, the transfer size for the memory transaction is selected as a function of, *inter alia*, a data size of the memory transaction.

Consistent with this disclosure, the challenged claims are directed generally to a solid-state storage device having a memory controller able to operate with memory devices with different attributes, and related methods. The claimed memory controller can perform a variety of memory transactions that were previously not performed by a single memory controller.

Claim 1’s “method of performing transactions on a set of memory locations” includes, in relevant part, the step of “selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.”² Independent claims 29 and 100 each recite features substantially similar to these, as Petitioner concedes. Pet., 54 (“The limitations recited in claim 29 are substantially identical to limitations in claim 1.”). For example, claim 29 is directed to a “non-transitory computer readable

² Claim 1 also recites that “each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location.”

medium comprising computer executable instructions adapted to cause a method of performing memory transactions on a first memory location and a second memory location,” where the claimed “method for performing memory transactions” includes in relevant part “selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.” Relatedly, claim 100 is directed to a “method for performing memory transactions” and includes in relevant part, “selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.” *See also* Pet., 59-62 (comparing claim 1 and claim 100).

B. Petitioner’s Deficient Combination of References Fails to Disclose or Suggest All Claimed Features

Petitioner asserts a single ground against these challenged claims. Petitioner contends that each of the challenged claims is obvious over the Danilak³ reference in view of the Cornwell⁴ reference.

However, Danilak and Cornwell, whether considered alone or in combination, fail to disclose every relied-upon feature of the challenged claims. In

³ U.S. Patent Application Publication No. 2008/0086588 to Danilak *et al.* (“Danilak”).

⁴ U.S. Patent Application Publication No. 2007/0180186 to Cornwell *et al.* (“Cornwell”).

particular, Petitioner relies upon Danilak to allegedly disclose selecting a transfer size for a memory transaction as a function of the specifically-claimed elements in the challenged claims, but Danilak includes no such disclosure. Instead, according to Petitioner's theory of Danilak, Danilak uses a flash memory's page size as the transfer size regardless of the data size of the memory transaction. Further, rather than identify these claimed features in a patent or printed publication as required under the statute and rules governing IPRs, Petitioner relies upon its expert to provide disclosures missing from Danilak. This is impermissible, and Danilak's failure to disclose or suggest these claimed features renders the challenge plainly deficient.

Petitioner also improperly relies upon its expert testimony as a substitute for additional required prior art disclosures. While each of the challenged claims recite, in relevant part, "said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type," Petitioner identifies no asserted reference that discloses this feature. Instead, Petitioner presents its asserted combination of Danilak and Cornwell, and then improperly relies upon its expert testimony to further modify this combination by adding a memory management function that behaves in a manner consistent with this challenged claim feature. This is

impermissible, and represents an additional fatal flaw requiring denial of this proceeding.

As such, the Petition's sole ground fails to establish unpatentability of any challenged claim, and the Petition should be denied without institution.

II. THE BOARD NEED NOT REACH ANY CLAIM CONSTRUCTION ISSUES TO DENY THE PETITION

In the Petition, Petitioner states that it “does not believe any terms require construction in this IPR proceeding,” and contends that it has “applied the plain and ordinary meaning to each claim term.” Pet., 5. Without expressly agreeing whether Petitioner has actually applied the plain and ordinary meaning to each claim term, and without waiving its right to submit its proposed constructions in a Patent Owner Response, Patent Owner submits that the Board need not engage in any pre-institution claim construction. For the reasons presented in Section III below, Petitioner's challenge includes a fatal flaw and fails to establish the disclosure of every claimed element in each independent claim. The Board need not conduct any pre-institution claim construction in order to deny the Petition and terminate this proceeding without institution.

III. PETITIONER'S CHALLENGE FAILS ON THE MERITS

A. The Challenged Claims Require Selecting a Transfer Size for a Memory Transaction

Claim 1's “method of performing transactions on a set of memory locations” includes, in relevant part, the step of “selecting a transfer size for the memory

transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.” This “selecting” step is identified by Petitioner as Element [1E] in the Petition. *See* Pet., 48. Independent claims 29 and 100 each recite substantially similar features as charted and identified below.

Claim number	Claimed feature and Petition’s Identifier
Claim 29	A non-transitory computer readable medium comprising computer executable instructions adapted to cause a method of performing memory transactions on a first memory location and a second memory location, said method comprising: ... selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes. This “selecting” element is referred to as Element [29E/Action] per the Petition. <i>See</i> Pet., 58.
Claim 100	A method for performing memory transactions, the method comprising: ... selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes. This “selecting” element is referred to as Element [100E/Action] per the Petition. <i>See</i> Pet., 62.

Providing support for these claimed features, the ’190 Patent discloses that the “[m]ulti-profile memory controller 2 also determines the transfer sizes to use when causing a memory transaction to be performed on the target memory device.” ’190 Pat., 8:4-6. In an embodiment, “the transfer size selected is a function of the

data size of the subject to memory transaction request 6, and the attributes in a device profile associated with a target memory location.” ’190 Pat., 8:39-42. The ’190 Patent discloses exemplary attributes, including “any combination of the following: the page size attribute, the block size attribute, and the partial page size attribute in device profile 26 of memory location 9” ’190 Pat., 8:42-47.

Discussion of the selection of transfer size based on the data size of the memory transaction is provided in the ’190 Patent and introduced in Section I.A above. *See, e.g.*, ’190 Pat., 8:47-9:6. As discussed above, “if the data size is greater than the page size attribute value in device profile 26, multi-profile memory controller 2 uses a transfer size equal to at least the page size attribute value for each memory operation transfer for the memory transaction requested until the remaining data not yet transferred from a requesting IO device is less than the page size attribute.” ’190 Pat., 8:50-57. Where the remaining data to be transferred is smaller than the page size attribute value, “multi-profile memory controller can then use a partial page size attribute value for the transfer size of the next memory operation transfer until all of the data has been transferred to memory location 9.” ’190 Pat., 8:57-61. “If the data size is greater than the block size attribute value in device profile 24, multi-profile memory controller 2 uses a transfer size equal to at least the block size value for each memory operation transfer for the memory transaction requested until the remaining data not yet transferred is less than the

block size attribute value.” ’190 Pat., 8:61-66. Depending on the remaining data size to be transferred, the memory controller selects a transfer size equal to either the page size attribute value or the partial page size attribute value. ’190 Pat., 8:66-9:6. Thus, in these exemplary embodiments, the transfer size for the memory transaction is selected by the memory controller as a function of, *inter alia*, a data size of the memory transaction.

B. Danilak in view of Cornwell Fails to Disclose any Selection of Transfer Size

As introduced above, claim 1 recites, in relevant part, “selecting a transfer size for the memory transaction, wherein *the transfer size is a function of a data size of the memory transaction* and the first set of attributes.” (emphasis added). Petitioner refers to this element as element [1E], and asserts that Danilak teaches this claimed feature. Pet., 48-50. Contrary to Petitioner’s assertion, Danilak fails to disclose at least this claimed feature. First, Danilak is silent about any selection of transfer size, and Petitioner improperly relies on its own unsupported expert testimony to manufacture this claimed feature in the asserted combination. Second, even under Petitioner’s forced reading of Danilak, there is no instance where a transfer size is anything other than a page size, and a transfer size is not selected. Further, a transfer size is not selected as a function of at least a “data size of the memory transaction.” As such, Danilak fails to disclose “selecting a transfer

size for the memory transaction,” where the transfer size is a function of at least “a data size of the memory transaction” as claimed.

Initially, Petitioner’s sole citation to Danilak for this element [1E] is to Danilak’s paragraph [0073], which does not disclose any selection of transfer size, much less a selection based on “a data size of the memory transaction” as claimed. *See* Pet., 48-50; Danilak, [0073]. Petitioner’s remaining citations for this element [1E] are to the declaration of Dr. Alpert, identified as INTEL-1003. *Id.* Without citing to any patent or printed publication, Petitioner contends that it “was well-known that the transfer size of a memory operation to a memory device is dictated by the size of the largest addressable unit for that device (e.g., page size for flash memory).” Pet., 48 (citing INTEL-1003, ¶164). Petitioner also relies on its expert rather than any prior art patent or printed publication to assert that it “was also well-known that the transfer size of a memory operation is a function of the data size of the transaction requested (e.g., transfer size is either equal to or a fraction of the data size).” Pet., 48 (citing INTEL-1003, ¶164).

Petitioner cites to Danilak’s [0073] to introduce the circumstance in which “the virtual page size ... is larger than the discovered page size.” Pet., 48. In this situation, Danilak discloses that “the memory request may be performed to multiple flash memory devices to form a page of the configured size.” Danilak, [0073]. Danilak also discloses that “[i]f the configured page size is larger than the

discovered page size multiplied by the number of flash memory devices, the request may be performed as multiple operations to multiple pages on each device to form a page of the configured size.” Danilak, [0073]. But in none of these disclosures does Danilak address any transfer size of an operation, much less any selection of transfer size.

Petitioner cites to its expert’s declaration, INTEL-1003, again—rather than Danilak—to fill in the disclosures missing from Danilak. Petitioner argues that “Danilak’s flash interface circuit therefore *selects* a set of available memory devices to perform the requested transaction *based on their page sizes* (transfer size) *and the data size of the transaction.*” Pet., 49 (citing INTEL-1003, ¶165) (emphasis added). This is wrong. Contrary to Petitioner’s assertion, Danilak never discloses any *selection* of available memory devices, and never discloses any *selection* of transfer size as part of the actions performed by translations unit 509. Confirming this failure of Danilak, Petitioner does not cite to a single instance of selecting memory devices or transfer size in Danilak.

Even in Dr. Alpert’s manufactured example presented in paragraph 165 of INTEL-1003, he fails to explain how any transfer size is selected as a function of a “data size of the memory transaction” as required by the claim. Rather, according to Dr. Alpert, each memory transaction must be equal to a page size of the destination memory device, and has no relationship to any “data size of the

memory transaction” as required by the challenged claim. Petitioner and Dr. Alpert allege that Danilak’s “translation units in Danilak’s flash interface circuit therefore selects a set of available memory devices to perform the requested transaction based on their page sizes,” but this assertion is unsupported by Danilak. Once again, Petitioner is improperly relying upon Dr. Alpert’s testimony to correlate transfer size and page size, and therefore fill in gaps in Danilak’s disclosures. There is no mention in Danilak of selecting memory devices, or selecting them based on their page sizes, or even correlating page size to transfer size. As a result, Petitioner improperly relies upon Dr. Alpert’s testimony to argue that claimed features were known in the prior art. This is improper in IPRs. Danilak and Cornwell, even if combined, fail to disclose at least “selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.”

Moreover, Petitioner’s attempt to correlate transfer size with a memory device’s page size is incorrect and improper. Petitioner alleges that “the transfer size of a memory operation to a memory device is dictated by the size of the largest addressable unit for that device (e.g., page size for flash memory).” Pet., 48 (citing INTEL-1003, ¶164). This statement is faulty for at least two reasons.

First, this statement is flatly contradicted by the ’190 Patent itself, which discloses no fewer than three potential transfer sizes, including “a transfer size

equal to at least the page size attribute value,” “a partial page size attribute value for the transfer size,” and “a transfer size equal to at least the block size value.” *See* ’190 Pat., 8:50-57, 8:57-61, 8:61-66, 8:66-9:6. Contrary to Danilak, the ’190 Patent recognizes potential transfer sizes and discloses a framework for selecting a transfer size based on certain disclosed and claimed factors, including the data size of the memory transaction.

Second, Petitioner’s only citation for its correlation of transfer size with a memory device’s page size is to INTEL-1003, Dr. Alpert’s declaration. But Dr. Alpert provides no further support for this statement, and simply repeats this same self-serving sentence from the Petition, verbatim. Ex. 1003, ¶164 (“It was well-known that the transfer size of a memory operation to a memory device is dictated by the size of the largest addressable unit for that device (e.g., page size for flash memory).” Unsupported conclusory statements like this are entitled to no weight. *See* 37 C.F.R. § 42.65(a); *Samsung Electronics Co., Ltd. v. Rightquestion, LLC*, IPR2022-00251, Paper 17 at 25 (PTAB June 9, 2022) (declining to credit testimony where “declarant makes these same statements verbatim, without more, and with no additional citations to evidence”).

Finally, Petitioner incorrectly contends that the “size translation function performed by Danilak’s flash interface circuit is consistent with the example of transfer size selection described in the ’190 patent.” Pet., 49 (citing INTEL-1003,

¶166). This is wrong. As already explained, the '190 Patent discloses transfer size selection based on the data size to be transferred, and discloses no fewer than three potential and selectable transfer sizes, including “a transfer size equal to at least the page size attribute value,” “a partial page size attribute value for the transfer size,” and “a transfer size equal to at least the block size value.” *See* '190 Pat., 8:50-57, 8:57-61, 8:61-66, 8:66-9:6. Danilak is silent regarding transfer size, and does not disclose selection of a transfer size, much less a selection of transfer size based on the data size of the memory transaction.

The Petition only relies upon Danilak—and Dr. Alpert's unsupported testimony—to allegedly disclose this claimed feature [1E], but this feature is not disclosed or suggested in Danilak. Further, Cornwell is not relied upon to remedy the shortcomings of Danilak for this feature.

Whether considered alone or in combination, Danilak in view of Cornwell fail to disclose or suggest at least these claimed features. For this reason, challenged independent claim 1 is not obvious over Danilak in view of Cornwell. Further, Petitioner relies upon its analysis for element [1E] to challenge the substantially similar language appearing in challenged claims 29 and 100. *See* Pet., 58-59, 62. Thus, for these same reasons presented in this Section III.B, challenged independent claims 29 and 100 are not obvious over Danilak in view of Cornwell.

C. Petitioner's Challenge Improperly Relies on Expert Testimony to Provide Elements Missing from the Cited References

Claim 1 also recites, in relevant part, “wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type.” Petitioner refers to this element as element [1A.6], and addresses this claimed feature at pp. 37-40 of the Petition. However, Petitioner fails to identify this claimed feature in any asserted reference, and instead improperly uses its expert testimony as a substitute for finding this element in any asserted references. This is not permitted in *inter partes* reviews, and Petitioner's failure to identify this claimed feature in a patent or printed publication serves as an additional reason that the Petition is deficient and should be denied.

Under the statute governing IPRs, “[a] petitioner in an inter partes review may request to cancel as unpatentable 1 or more claims of a patent ... only on the basis of prior art consisting of patents or printed publications.” 35 U.S.C. § 311(b). Further, as the Board has explained in the Consolidated Trial Practice Guide, “Expert testimony ... cannot take the place of a disclosure in a prior art reference, when that disclosure is required as part of the unpatentability analysis.” See Consolidated Trial Practice Guide, Nov. 2019, at 36 (available at <https://www.uspto.gov/TrialPracticeGuideConsolidated>). “[B]ecause an inter partes review may only be requested ‘on the basis of prior art consisting of patents

or printed publications,’ 35 U.S.C. § 311(b), expert testimony cannot take the place of disclosure from patents or printed publications. In other words, expert testimony may explain ‘patents and printed publications,’ but *is not a substitute for disclosure in a prior art reference itself.*” *Id.* (emphasis added). Petitioner’s challenge of element [1A.6] violates this restriction and the governing statute by using its expert testimony as a substitute for a required disclosure in a prior art reference.

In addressing element [1A.6], Petitioner initially alleges that the “combination of Danilak and Cornwell discloses or at least suggests ‘memory device profiles’ that are ‘optimal’ for sequential and random data accesses consistent with the examples identified by PO.” Pet., 37. But Petitioner’s citation for this statement is not to either Danilak or Cornwell. Rather, Petitioner cites only to its expert declaration, INTEL-1003. Pet., 37. Petitioner next recounts the alleged advantages of NAND and NOR flash memory. Pet., 37-38. Although Petitioner contends that its asserted “combination of Danilak and Cornwell ... includes both NAND and NOR flash memory devices,” Petitioner identifies no disclosure in either Danilak or Cornwell that addresses how these memory devices are managed. Instead, without citing to any patent or printed publication, Petitioner alleges that a “POSITA would have been further motivated to incorporate a memory management function that (1) selects NOR flash when a transaction is received requiring writing or reading code because NOR flash is

‘optimal’ for code execution which requires fast random-access reads and (2) selects NAND flash when a transaction is received for writing and reading data (e.g., audio or image storage) which requires faster sequential write and read accesses.” Pet. 38 (citing INTEL-1003, ¶137). This statement represents Petitioner’s improper use of its expert to manufacture a “memory management function” that operates in the manner claimed by the challenged claim, despite no such memory management function being disclosed or suggested in either Danilak or Cornwell. In violation of § 311(b) and the Consolidated Trial Practice Guide, Petitioner is using its expert testimony as a substitute for disclosure required in a prior art reference. This is plainly improper in IPRs.

Concluding this section addressing element [1A.6], Petitioner also discusses Cornwell’s disclosure that “[f]lash is available in a variety of block sizes” and that block sizes and page sizes are configurable. Pet., 39. But Petitioner then again relies on its expert testimony, rather than Cornwell’s or Danilak’s disclosures, to modify its asserted combination by adding a memory management function that operates in the manner claimed in the ’190 Patent. Pet., 40. Once again, this is an improper use of expert testimony to modify the asserted Danilak/Cornwell combination to include all claimed features, rather than locating and identifying those claimed features in any patent or printed publication.

Independent claims 29 and 100 each recite features substantially similar to element [1A.6], as Petitioner concedes. Pet., 54 (“The limitations recited in claim 29 are substantially identical to limitations in claim 1.”); *id.*, 57 (relying on its claim 1 analysis for element [29A.2] of claim 29); *id.*, 61 (relying on its claim 1 analysis for element [100A.2] of claim 100). As such, Petitioner’s improper use of expert testimony in its challenges infects each of the challenged independent claims.

Because Petitioner has improperly relied upon expert testimony as a substitute for a required disclosure in a patent or printed publication, the Ground is deficient and should be denied.

IV. CONCLUSION

For the reasons presented above, Petitioner’s challenge is deficient and no *inter partes* review should be instituted.

Dated: September 20, 2023

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word-processing system's word count, the brief contains 4,683 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(a).

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CERTIFICATE OF SERVICE

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