

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

BiTMICRO LLC,
Patent Owner.

IPR2023-00779
Patent 9,135,190 B1

Before KEN B. BARRETT, TERRENCE W. McMILLIN, and
KEVIN C. TROCK, *Administrative Patent Judges*.

McMILLIN, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Intel Corporation (“Petitioner”) filed a Petition to institute an *inter partes* review of claims 1, 2, 5–8, 11, 19, 29, 30, 33, 36–39, 42, 94, and 100 (“the challenged claims”) of U.S. Patent No. 9,135,190 B1 (Ex. 1001, “the ’190 patent”) pursuant to 35 U.S.C. § 311 *et seq.* Paper 2 (“Petition” or “Pet.”). BiTMicro, LLC (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Preliminary Response” or “Prelim. Resp.”).

We have authority under 35 U.S.C. § 314, which provides that an *inter partes* review may not be instituted unless the information presented in the Petition and the Preliminary Response shows that “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). For the reasons discussed below, we deny institution.

A. Related Matters

The parties identify the following related district court proceedings: *BiTMICRO LLC v. KIOXIA Am. Inc., et al.*, No. 6:22-cv-00331 (W.D. Tex. 2022); *BiTMICRO LLC v. Intel Corp.*, No. 5:23-cv-00625 (N.D. Cal.).¹ Pet. 69; Paper 4, 2.

The ’190 patent is also challenged in the following *inter partes* review proceedings: *KIOXIA America, Inc. v. BiTMICRO, LLC*, IPR 2023-00741;² *Intel Corporation v. BiTMICRO, LLC*, IPR2023-00780.³ Pet. 69; Paper 4, 2.

¹ Petitioner references this case as No. 6-22-cv-00335 (W.D. Tex.), but Patent Owner notes it has been transferred to the Northern District of California.

² Institution was denied in IPR2023-00741, Paper 8.

³ IPR2023-00780 was filed by Petitioner on the same day as this proceeding, but challenges a different set of claims of the ’190 patent. Petitioner relies on the same combination of references in both proceedings.

B. The '190 Patent

The '190 patent is titled “Multi-Profile Memory Controller for Computing Devices.” Ex. 1001, code (54). The '190 patent is directed to a “a multi-profile memory controller . . . that can operate with memory locations, memory devices, or both which are associated with different memory attributes, different attribute qualifiers, or the like.” *Id.* at code (57).

Figure 1 of the '190 patent, reproduced below, “illustrates a multi-profile memory controller.” *Id.* at 1:64.

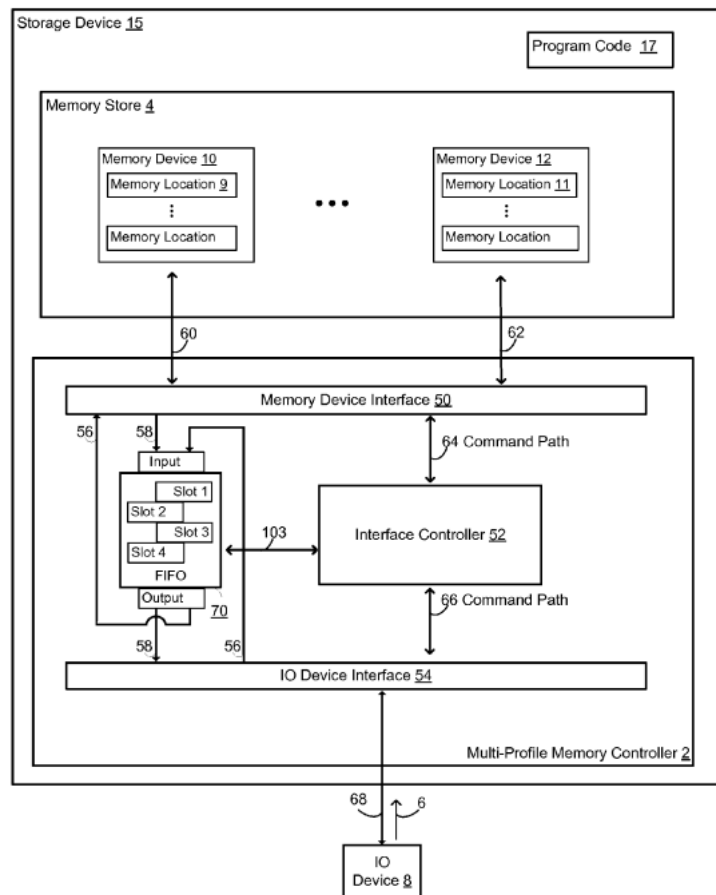


FIG. 1

Figure 1 depicts an exemplary storage device 15 having a multi-profile memory controller 2 and a memory store 4 that includes a first memory device 10 having a first memory location 9 and a second memory device 12 having a second memory location 11. *Id.* at 2:50–65, 3:7–8. Each memory location is “associated with a set of at least one memory attribute,” which “is defined to include a characteristic of a memory location that is related to accessing or addressing the memory location.” *Id.* at 2:63–3:2. “[E]xamples of an attribute of a memory location may include . . . the block size used by the memory device, the page size used by the memory device, the memory protocol or specification supported by the memory device, and the partial page size used by the memory device.” *Id.* at 3:8–13.

Figure 2A of the ’190 patent, reproduced below, illustrates a device profile for use with the multi-profile memory controller. *Id.* at 2:1–3.

24		25
Page Size	16	(# of pages)
Block Size	18	(# of blocks)
Memory Protocol	20	(Protocol Type Supported)
Mem. Dev. Type	22	(Mem. Type)
Partial Page Size	23	(# of pages)

FIG. 2A

Figure 2A depicts a device profile 14, which “may be used to represent at least one attribute 24 of a memory location, and each attribute respectively corresponds to an attribute qualifier 25.” *Id.* at 3:22–25. “These attributes include a page size 16, a block size 18, a memory protocol 20 supported by the memory device in which the memory location is addressable, a memory device type 22, and a partial page size 23,” and the “[a]ttribute qualifier 25 is in the form of a value or type.” *Id.* at 3:25–30.

The '190 patent discloses that the “[m]ulti-profile memory controller 2 can perform memory transactions using different device profiles,” and “memory locations 9 and 11 [can] have different device profiles.” *Id.* at 3:61–64.

C. Challenged Claims

Petitioner challenge claims 1, 2, 5–8, 11, 19, 29, 30, 33, 36–39, 42, 94, and 100 of the '190 patent. Pet. 1. Challenged claims 1, 29, and 100 are independent claims. Ex. 1001, 12:57–13:42, 15:59–16:21, 22:22–53.

Claim 1 recites:

1. A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising:
performing a memory transaction comprising addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile, wherein said second memory location is in a second memory device in the memory store, wherein a memory read transaction or a memory write transaction is performed on at least one of the first memory location or second memory location, wherein data is transferred to the first memory location or second memory location from a host for a memory write transaction, wherein data is transferred from the first memory location or second memory location to the host for a memory read transaction;
wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type;
said performing the memory transaction further comprising identifying command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;

after identifying the command details, obtaining the first set of attributes;

wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location;

wherein the memory store is directly coupled to at least one memory bus and wherein the at least one memory bus is directly coupled to a controller, and wherein the controller performs the memory read transaction and memory write transaction on the memory store;

wherein the host is directly coupled to the controller by a communication path as the controller performs the memory read transaction or memory write transaction;

wherein the first device profile and second device profile are each stored in the memory store; and

using attributes from said first and second device profiles; and
selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

Id. at 12:57–13:42 (emphasis added to disputed limitation).

D. The Asserted Ground

Petitioner challenges claims 1, 2, 5–8, 11, 19, 29, 30, 33, 36–39, 42, 94, and 100 of the '190 patent based on the ground set forth in the table below. Pet. 2.

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 5–8, 11, 19, 29, 30, 33, 36–39, 42, 94, 100	103(a)	Danilak ⁴ , Cornwell ⁵

⁴ US 2008/0086588 A1, published Apr. 10 2008 (Ex. 1005).

⁵ US 2007/0180186 A1, published Aug. 2, 2007 (Ex. 1006).

II. ANALYSIS

A. *Legal Standards*

A patent claim is unpatentable as obvious if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of obviousness or non-obviousness.⁶ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). Petitioner cannot satisfy their burden of proving obviousness by employing “mere conclusory statements.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

B. *Level of Ordinary Skill in the Art*

With regard to the level of ordinary skill in the art, Petitioner contends a person of ordinary skill in the art “would have had at least a bachelor’s degree in electrical or computer engineering and two years of experience

⁶ The parties do not submit objective evidence of obviousness or non-obviousness. *See generally* Pet.; Prelim. Resp.

working with storage systems (including storage systems made up of different types of storage devices), file management policies, and different data access patterns, or an equivalent combination of education and experience.” Pet. 4–5 (citing Ex. 1003 ¶ 57). Patent Owner does not address the level of ordinary skill in the art. *See generally* Prelim. Resp.

For purposes of this Decision, we adopt Petitioner’s definition of the level of ordinary skill in the art because it is consistent with the ’190 patent and the asserted prior art.

C. Claim Construction

In an *inter partes* review for a petition filed on or after November 13, 2018, “[claims] of a patent . . . shall be construed using the same claim construction standard that would be used to construe the [claims] in a civil action under 35 U.S.C. § 282(b), including construing the [claims] in accordance with the ordinary and customary meaning of such claims as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b) (2018); *see also Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–14 (Fed. Cir. 2005). “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). There is a “heavy presumption,” however, that a claim term carries its ordinary and customary meaning. *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002) (citation omitted).

The Petition indicates “Petitioner does not believe any terms require construction in this IPR proceeding,” and that “Petitioner and its expert have

applied the plain and ordinary meaning to each claim term.” Pet. 5. Patent Owner “submits that the Board need not engage in any pre-institution claim construction.” Prelim. Resp. 10.

We determine that no terms require express construction for purposes of this Decision. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Ltd.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). In this Decision, we give the claim terms their plain and ordinary meanings.

D. Summaries of Cited Art

In the challenges to the claims, Petitioner relies on Danilak (Ex. 1005) and Cornwell (Ex. 1006). Summaries of these references are provided below.

1. Danilak (Ex. 1005)

Danilak is titled “System and Method for Increasing Capacity, Performance, and Flexibility of Flash Storage.” Ex. 1005, code (54). Danilak “relates to memory, and more particularly to enhanced capacity, performance, flexibility, and reliability in multiple flash memory circuit systems,” and discloses “numerous embodiments of flash devices and flash interface circuits.” *Id.* ¶¶ 2, 16. Danilak seeks “to increase capacity, performance, and flexibility of flash while still resulting in cost effective implementations.” *Id.* ¶ 3.

Figure 2 of Danilak, reproduced below, illustrates connections between a flash interface circuit and flash memory devices for one embodiment. *Id.* ¶ 6.

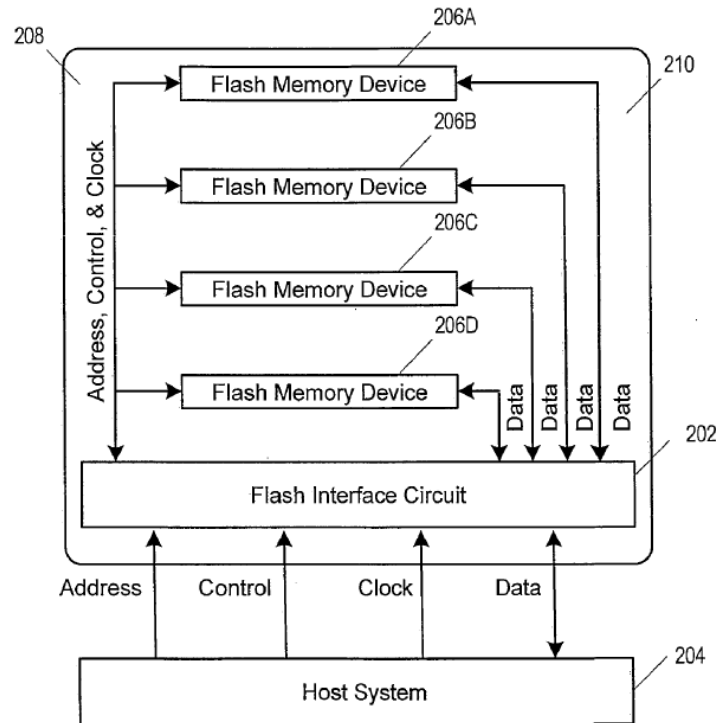


Figure 2 illustrates host system 204, flash interface circuit 202, flash memory devices 206A–D, address, control, and clock signals 208, and data signals 210. *Id.* ¶ 22.

Danilak discloses “a test to ensure that the amount of configured memory reported to the host is the same as or less than the amount of physically-attached memory.” *Id.* ¶ 73. Danilak describes an example as follows:

[I]f the configured page size is larger than the discovered page size, the memory request may be performed to multiple flash memory devices to form a page of the configured size. If the configured page size is larger than the discovered page size multiplied by the number of flash memory devices, the request may be performed as multiple operations to multiple pages on each device to form a page of the configured size.

Id.

2. *Cornwell (Ex. 1006)*

Cornwell is titled “Non-Volatile Memory Management.” Ex. 1006, code (54). Cornwell discloses a memory management system comprising “a memory controller [that] is operatively coupled to the one or more non-volatile memory devices and configurable to access the one or more non-volatile memory devices in accordance with a memory management policy.” *Id.* ¶ 7. The “device data,” used to identify each memory device and its manufacturer, “can include an electronic signature or serial number that includes a manufacturer code and/or device code,” “device type,” “device density,” “page size,” “spare area size,” “sequential access time,” “block size,” “bus width,” “bad block identification, and any other information that is associated with attributes, properties or characteristics of the memory device.” *Id.* ¶ 42.

Figure 1 of Cornwell, reproduced below, illustrates an exemplary non-volatile memory management system. *Id.* ¶ 11.

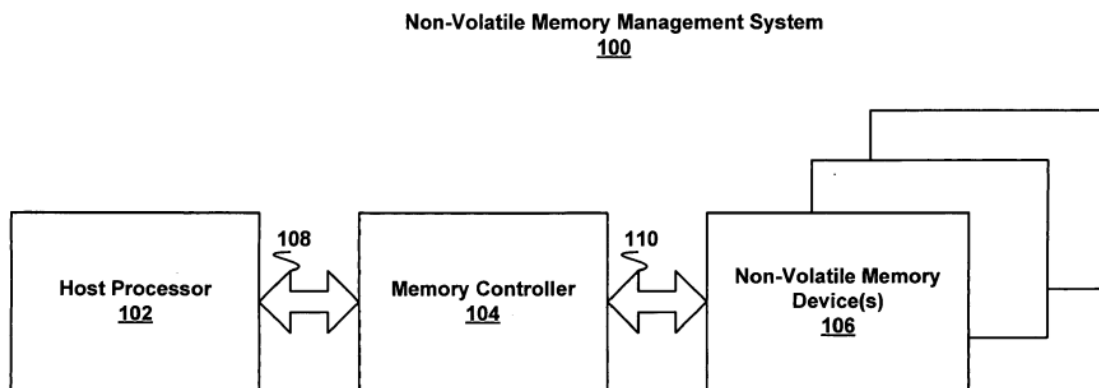


Figure 1

Figure 1 depicts a memory controller 104 coupled to one or more non-volatile memory devices 106.

Figure 3 of Cornwell, reproduced below, illustrates a non-volatile memory device. *Id.* ¶ 13.

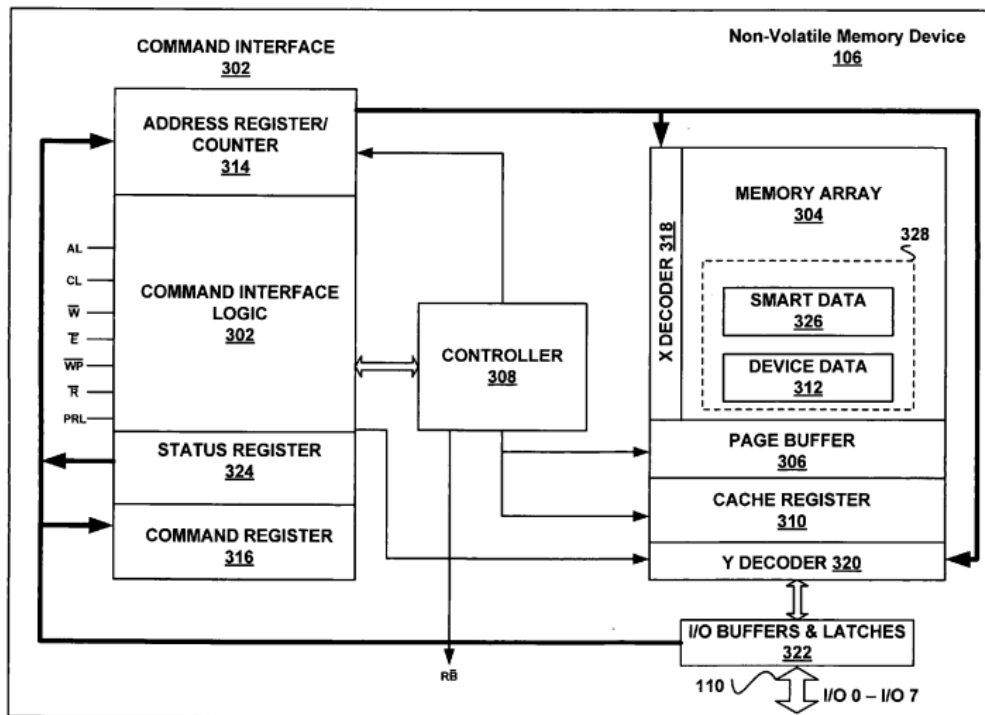


Figure 3

Figure 3 depicts the device data contained in each memory device.

E. Discussion of Challenge to the Claims

The Petition presents a single ground of alleged unpatentability against the challenged claims of the '190 patent. Pet. 2. Petitioner contends that each of the challenged claims is obvious over the combination of Danilak and Cornwell. *Id.*

Patent Owner opposes institution on the basis that Petitioner has failed to establish that the cited art teaches or suggests all the limitations of any challenged claim. Prelim. Resp. 8 ("Danilak and Cornwell, whether considered alone or in combination, fail to disclose every relied-upon feature of the challenged claims."). Specifically, Patent Owner argues:

Petitioner relies upon Danilak to allegedly disclose selecting a transfer size for a memory transaction as a function of the specifically-claimed elements in the challenged claims, but Danilak includes no such disclosure. Instead, according to Petitioner's theory of Danilak, Danilak uses a flash memory's page size as the transfer size regardless of the data size of the memory transaction.

Id. at 9. Accordingly, we consider whether the Petition establishes that the cited art teaches or suggests “selecting a transfer size for the memory transaction, wherein the transfer size is a function of the data size of the memory transaction and the first set of attributes” as recited in claim 1 of the '190 patent (Ex. 1001, 13:40–42) and as identically recited in the additional challenged independent claims. *Id.* at 16:19–21 (claim 29), 22:51–53 (claim 100); *see also* Prelim. Resp. 11 (chart showing the “selecting” limitation in challenged independent claims 29 and 100).

Petitioner relies on a single paragraph in Danilak (Ex. 1005 ¶ 73) for allegedly disclosing the “selecting” limitation as recited in each of the challenged independent claims of the '190 patent. *See* Pet. 48–50 (claim 1), 58 (claim 29), 62 (claim 100). The Petition states:

As Danilak explains, in the circumstance where the virtual page size (and hence the data size) is larger than the discovered page size, “the memory request may be performed to multiple flash memory devices to form a page of the configured size.” (INTEL-1005, ¶73; INTEL-1003, ¶165.^[7]) That is, in Danilak's size translation example, the data size for the requested memory transaction is larger than the transfer size any individual memory device can accept in a single operation,

⁷ INTEL-1003 is the Declaration of Donald Alpert, PhD, Exhibit 1003. Dr. Alpert also relies solely on paragraph 73 of Danilak as allegedly teaching or suggesting the “selecting” limitation. *See* Ex. 1003 ¶¶ 164–167. We have considered the Alpert Declaration and determine that it does not establish that paragraph 73 of Danilak teaches or suggests the “selecting” limitation.

requiring multiple memory operations to be performed. (*See INTEL-1005, ¶73.*) Danilak's flash interface circuit therefore selects a set of available memory devices to perform the requested transaction based on their page sizes (transfer size) and the data size of the transaction. (INTEL-1003, ¶165.) Therefore, the transfer size of each individual memory operation needed to perform the requested memory transaction is a function of the page size of the memory device (e.g., "*first set of attributes*") and the "*data size of the memory transaction*" (e.g., a fraction of the data size of the transaction requested by the host). (*Id.*)

Id. at 48–49 (emphasis added). Contrary to Petitioner's contention, we determine that Petitioner has failed to adequately and persuasively demonstrate that there is a teaching or suggestion in paragraph 73 of Danilak of "selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction."

Paragraph 73 of Danilak states:

Other translations that may be performed by the other translations unit 509 may include a test to ensure that the amount of configured memory reported to the host is the same as or less than the amount of physically-attached memory. Addition, if the configured page size reported to the host is different than the discovered page size in the attached devices, a translation may be performed by the other translations unit 509. For example, **if the configured page size is larger than the discovered page size, the memory request may be performed to multiple flash memory devices to form a page of the configured size.** If the configured page size is larger than the discovered page size multiplied by the number of flash memory devices, the request may be performed as multiple operations to multiple pages on each device to form a page of the configured size. Similarly, if the redundant area size differs between the configured size reported to the host and the attached flash devices, the other translation unit 509 may concatenate two blocks and their redundant areas. If the organization reported to the host is narrower than the

organization of the attached devices, the translation unit 509 may select a byte or bytes from the data provided by the attached devices to be output as the data for the request.

Ex. 1005 ¶ 73 (emphasis added).⁸ We discern no teaching or suggestion in paragraph 73 of Danilak that “the transfer size is a function of a data size of the memory transaction” or of any consideration of the “data size of the memory transaction.”

Petitioner argues that “[a]s Danilak explains, **in the circumstance where the virtual page size (and hence the data size)** is larger than the discovered page size, ‘the memory request may be performed to multiple flash memory devices to form a page of the configured size.’” Pet. 48 (citing Ex. 1005 ¶ 73) (emphasis added). However, the quoted sentence in Danilak states, “**if the configured page size** is larger than the discovered page size, the memory request may be performed to multiple flash memory devices to form a page of the configured size.” Ex. 1005 ¶ 73 (emphasis added). This passage in Danilak refers to “configured page size” and not “data size” as argued by Petitioner. And, Petitioner does not adequately explain why “configured page size” as referred to in this passage of Danilak is the equivalent of “data size of the memory transaction” as recited in the independent claims of the ’190 patent. *See* Pet. 48–49.

As noted above in discussing claim construction (Section II.C.), Petitioner applies the plain and ordinary meaning to each claim term. *See* Pet. 5–6. Petitioner has not shown, or even meaningfully argued, that the

⁸ The translation process performed by the translation unit 509 is further described in paragraph 56 of Danilak. Ex. 1003 ¶ 56. This description makes no reference to “data size of the memory transaction” or any similar or related concept. *See id.*

plain and ordinary meaning of “data size of the memory transaction” in the context of the independent claims of the ’190 patent is “configured page size” as disclosed in paragraph 73 of Danilak.

Contrary to Petitioner’s assertions, “configured page size” in paragraph 73 of Danilak does not refer or relate to “data size of the memory transaction” as recited in the independent claims of the ’190 patent. With regard to the meaning of this claim language, the Petition states:

A host memory transaction has a “data size” which is the amount of data to be read or written by the transaction. (INTEL-1003, ¶164.) This host memory transaction is translated by a memory controller into one or more operations sent to the physical memory devices. (*Id.*) The amount of data read or written by an operation from/to an individual memory device is the “transfer size.” (*Id.*)

Id. at 48. In Danilak, the “configured page size” refers to the page size reported to the system as exemplified by the “PAGE”/“Page size (1, 2, 4, 8 KB)” entries (“Byte 4, Bits 1:0”) in the configuration blocks of Figures 7–9 of Danilak. *See* Ex. 1005 ¶¶ 11–13, 60–72. The sentence in paragraph 73 that Petitioner relies on is directed to determining how to handle a situation where the page size reported to the system is larger than the page size discovered in “a test to ensure that the amount of configured memory is the same as or less than the amount of physically-attached memory.” *Id.* at ¶ 73 (first sentence). “[I]f the configured page size reported to the host is different than the discovered page size in the attached devices, a translation may be performed by the other translations unit 509.” *Id.* at ¶ 73 (second sentence). Thus, in paragraph 73 of Danilak, “[t]he amount of data which can be read or written by an operation from/to an individual memory device” or “the ‘transfer size’” (Pet. 48) is “discovered” and used for the translation.

We discern no reference in paragraph 73 of Danilak to the “amount of data to be read or written by the transaction” (Pet. 48) or the “data size of the memory transaction.” We determine that Petitioner’s interpretation of the third sentence of paragraph 73 of Danilak in which “configured page size” is treated as the equivalent of “data size of the memory transaction” is not supported, but rather is contradicted, by the text of paragraph 73 of Danilak.

Patent Owner also points out that Petitioner does not even show that Danilak teaches or suggests “selecting a transfer size for the memory transaction.” Prelim Resp. 15 (“[I]n none of these disclosures [in paragraph 73 of Danilak] does Danilak address any transfer size of an operation, much less any selection of transfer size.”). The Petition states, “Danilak’s flash interface circuit therefore **selects a set of available memory devices** to perform the requested transaction based on their page sizes (transfer size) and the data size of the transaction.” Pet. 49 (emphasis added). Patent Owner contends that this statement is wrong. Prelim. Resp. 15.

Specifically, Patent Owner argues:

Contrary to Petitioner’s assertion, Danilak never discloses any *selection* of available memory devices, and never discloses any *selection* of transfer size as part of the actions performed by translations unit 509. Confirming this failure of Danilak, Petitioner does not cite to a single instance of selecting memory devices or transfer size in Danilak.

Id. And, Patent Owner argues, “[t]here is no mention in Danilak of selecting memory devices, or selecting them based on their page sizes, or even correlating page size to transfer size.” *Id.* at 16. We agree with Patent Owner. The Petition provides no showing of a teaching or suggestion in Danilak of “selecting a transfer size for the memory transaction.”

In summary, the Petitioner fails to show that the cited art teaches or suggests “selecting a transfer size for the memory transaction, wherein the transfer size is a function of the data size of the memory transaction and the first set of attributes” as recited in the challenged independent claims of the ’190 patent.

III. CONCLUSION

On the record before us, we conclude that there is not a reasonable likelihood that the Petitioner would prevail with respect to at least one of the claims challenged in the Petition. Therefore, we deny the Petition and do not institute *inter partes* review of the ’190 patent.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that the Petition is *denied* and we do not institute *inter partes* review of any challenged claim of U.S. Patent No. 9,135,190 B1.

IPR2023-00779
Patent 9,135,190 B1

FOR PETITIONER:

Lori Gordon
Gordon-ptab@perkinscoie.com

Sarah Fowler
Stahnke-ptab@perkinscoie.com

Tyler Bowen
Bowen-ptab@perkinscoie.com

FOR PATENT OWNER:

Wayne Helge
whelge@nossaman.com

James Wilson
jwilson@dbjg.com