RECORDATION FORM COVER SHEET
PATENTS ONLY

To the Director of the U.S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

1. Name of conveying party(ies)
Ricardo H. BRUCE;
Marlon B. VERDAN;
Rowenah Michelle JAGO-ON;
Maria Eliza B. DE BELEN; and
Ron Kelvin B. PALACOL
Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies)
Name: BiTMICRO Networks, Inc.
Internal Address:
Street Address: 47929 Fremont Blvd
City: Fremont
State: CA
Country: US Zip: 94538
Additional name(s) & address(es) attached? ☐ Yes ☒ No

3. Nature of conveyance/Execution Date(s):
Execution Date(s) 31 Aug 2010 (All Assignors)
☒ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☐ Joint Research Agreement
☐ Government Interest Assignment
☐ Executive Order 9424, Confirmatory License
☐ Other

4. Application or patent number(s):
☒ This document is being filed together with a new application.
A. Patent Application No.(s)
B. Patent No.(s)
Additional numbers attached? ☐ Yes ☐ No

5. Name and address to whom correspondence concerning document should be mailed:
Name: The Uriarte Law Firm
Internal Address:
Street Address: 2021 The Alameda, Suite 225
City: San Jose
State: CA Zip: 95126
Phone Number: 408.244.2164 x111
Fax Number: 408.716.2651
Email Address: mail@uriartelaw.com

6. Total number of applications and patents involved:

7. Total fee (37 CFR 1.21(h) & 3.41) $40.00
☒ Authorized to be charged to deposit account
☒ Enclosed
☐ None required (government interest not affecting title)

8. Payment Information
Deposit Account Number 504068
Authorized User Name Uriarte Law

9. Signature:
/Stephen R. Uriarte/ — Signature
4 Sep 2010 — Date
Stephen R. Uriarte Reg. No. 40,854 — Name of Person Signing
Total number of pages including cover sheet, attachments, and documents: 5

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:
Mail Stop Assignment Recordation Services, Director of the USPTO, P.O.Box 1450, Alexandria, V.A. 22313-1450

INTEL-1002
9,135,190

Guidelines for Completing Patents Cover Sheets (PTO-1595)

Cover Sheet information must be submitted with each document to be recorded. If the document to be recorded concerns both patents and trademarks separate patent and trademark cover sheets, including any attached pages for continuing information, must accompany the document. All pages of the cover sheet should be numbered consecutively, for example, if both a patent and trademark cover sheet is used, and information is continued on one additional page for both patents and trademarks, the pages of the cover sheet would be numbered from 1 to 4.

Item 1. Name of Conveying Party(ies).

Enter the full name of the party(ies) conveying the interest. If there is insufficient space, enter a check mark in the "Yes" box to indicate that additional information is attached. The name of the additional conveying party(ies) should be placed on an attached page clearly identified as a continuation of the information Item 1. Enter a check mark in the "No" box, if no information is contained on an attached page. If the document to be recorded is a joint research agreement, enter the name(s) of the party(ies) other than the owner of the patent or patent application as the conveying party(ies).

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Item 4. Application Number(s) or Patent Number(s).

Indicate the application number(s), and/or patent number(s) against which the document is to be recorded. National application numbers must include both the series code and a six-digit number (e.g., 07/123,456), and international application numbers must be complete (e.g., PCT/US91/12345).

Enter a check mark in the appropriate box: "Yes" or "No " if additional numbers appear on attached pages. Be sure to identify numbers included on attached pages as the continuation of Item 4. Also enter a check mark if this Assignment is being filed with a new application.

Item 5. Name and Address of Party to whom correspondence concerning the document should be mailed. Enter the name and full address of the party to whom correspondence is to be mailed.

Item 6. Total Applications and Patents involved.

Enter the total number of applications and patents identified for recordation. Be sure to include all applications and patents identified on the cover sheet and on additional pages.

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Enter the total fee enclosed or authorized to be charged. A fee is required for each application and patent against which the document is recorded.

Item 8. Payment Information.

Enter the deposit account number and authorized user name to authorize charges.

Item 9. Signature.

Enter the name of the person submitting the document. The submitter must sign and date the cover sheet. Enter the total number of pages including the cover sheet, attachments, and document.

This collection of information is required by 35 USC 261 and 262 and 15 USC 1057 and 1060. The information is used by the public to submit (and by the USPTO to process) patent and trademark assignment requests. After the USPTO records the information, the records for patent and trademarks, assignments, and other associated documents can be inspected by the public. To view documents recorded under secrecy orders or documents recorded due to the interest of the federal government, a written authorization must be submitted. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the form to the USPTO. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Manager of the Assignment Division, USPTO, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop Assignment Recordation Services, Director of the USPTO, P.O. Box 1450, Alexandria, VA 22313-1450.

Privacy Act Statement for Patent Assignment Recordation Form Cover Sheet

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with the above request for information. This collection of information is authorized by 35 U.S.C. 1, 2, 261 and E.O. 9424. This information will primarily be used by the USPTO for the recordation of assignments related to patents and patent applications. Submission of this information is voluntary but is required in order for the USPTO to record the requested assignment. If you do not provide the information required on the cover sheet, the assignment will not be recorded, and all documents will be returned to you.

After the information is recorded, the records and associated documents can be inspected by the public and are not confidential, except for documents that are sealed under secrecy orders or related to unpublished patent applications. Assignment records relating to unpublished patent applications are maintained in confidence in accordance with 35 U.S.C. 122. Records open to the public are searched by users for the purpose of determining ownership for other property rights with respect to patents and trademarks.

Routine uses of the information you provide may also include disclosure to appropriate Federal, state, local, or foreign agencies in support of their enforcement duties and statutory or regulatory missions, including investigating potential violations of law or contract and awarding contracts or other benefits; to a court, magistrate, or administrative tribunal in the course of presenting evidence; to members of Congress responding to requests for assistance from their constituents; to the Office of Management and Budget in connection with the review of private relief legislation; to the Department of Justice in connection with a Freedom of Information Act request; to a contractor in the performance of their duties; to the Office of Personnel Management for personnel studies; and to the General Services Administration (GSA) as part of their records management responsibilities under the authority of 44 U.S.C. 2904 and 2906. Such disclosure to GSA shall not be used to make determinations about individuals.

ASSIGNMENT

For good and valuable consideration, the receipt of which is hereby acknowledged, the person(s) named below (referred to as "INVENTOR" whether singular or plural) has sold, assigned, and transferred and does hereby sell, assign, and transfer to **BiTMICRO Networks, Inc., a California corporation, having a place of business at 47929 Fremont Blvd., Fremont, CA 94538** ("ASSIGNEE"), for itself and its successors, transferees, and assignees, the following:

1. The entire worldwide right, title, and interest in all inventions and improvements ("SUBJECT MATTER") that are disclosed in the application for United States Letters Patent entitled: **MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES** ("APPLICATION"), which:

☒ is to be filed herewith;

☐ was filed on _____, now bearing U.S. serial number _____ and for which a Declaration was executed by INVENTOR on the date(s) below; and

2. The entire worldwide right, title, and interest in and to: (a) the APPLICATION, including any right of priority; (b) any divisional, continuation, substitute, renewal, reissue, and other related applications thereto which have been or may be filed in the United States or elsewhere in the world; and (c) any patents which may be granted on the applications set forth in (a) and (b) above.

INVENTOR agrees that ASSIGNEE may apply for and receive patents for SUBJECT MATTER in ASSIGNEE's own name.

INVENTOR agrees to do the following, when requested, and without further consideration, in order to carry out the intent of this Assignment: (1) execute all oaths, assignments, powers of attorney, applications, and other papers necessary or desirable to fully secure to ASSIGNEE the rights, titles and interests herein conveyed; (2) communicate to ASSIGNEE all known facts relating to the SUBJECT MATTER; and (3) generally do all lawful acts that ASSIGNEE shall consider desirable for securing, maintaining, and enforcing worldwide patent protection relating to the SUBJECT MATTER and for vesting in ASSIGNEE the rights, titles, and interests herein conveyed. INVENTOR further agrees to provide any successor, assign, or legal representative of ASSIGNEE with the benefits and assistance provided to ASSIGNEE hereunder.

INVENTOR represents that INVENTOR has the rights, titles, and interests to convey as set forth herein, and covenants with ASSIGNEE that the INVENTOR has made or will make hereafter no assignment, grant, mortgage, license, or other agreement affecting the rights, titles, and interests herein conveyed.

INVENTOR grants the attorney of record the power to insert on this Assignment any further identification which may be necessary or desirable in order to comply with the rules of the United States Patent and Trademark Office for recordation of this document.

Title of Document:	**ASSIGNMENT**
In Re Application of:	Ricardo H. Bruce et al.
Title:	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES
Filed: (if applicable)	N/A
Serial No.: (if applicable)	N/A

This Assignment may be executed in one or more counterparts, each of which shall be deemed an original and all of which may be taken together as one and the same Assignment.

First Inventor Signature — **Date of Signature** — **Date Inventor Declaration Signed by Inventor**

Name: Ricardo H. Bruce — AUGUST 31, 2010 — AUGUST 31, 2010

Second Inventor Signature — **Date of Signature** — **Date Inventor Declaration Signed by Inventor**

Name: Marlon B. Verdan — AUGUST 31, 2010 — AUGUST 31, 2010

Third Inventor Signature — **Date of Signature** — **Date Inventor Declaration Signed by Inventor**

Name: Margaret Anne N. Somera — _____, 2010 — _____, 2010

Fourth Inventor Signature — **Date of Signature** — **Date Inventor Declaration Signed by Inventor**

Name: Rowenah Michelle D. Jago-on — AUGUST 31, 2010 — AUGUST 31, 2010

Fifth Inventor Signature — **Date of Signature** — **Date Inventor Declaration Signed by Inventor**

Name: Maria Eliza B. De Belen — AUGUST 31, 2010 — AUGUST 31, 2010

Sixth Inventor Signature — **Date of Signature** — **Date Inventor Declaration Signed by Inventor**

Name: Ron Kelvin B. Palacol — AUGUST 31, 2010 — AUGUST 31, 2010

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES
First Named Inventor/Applicant Name:	Ricardo H. Bruce
Filer:	Stephen Radcliff Uriarte
Attorney Docket Number:	6005.042

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility filing Fee (Electronic filing)	4011	1	82	82
Utility Search Fee	2111	1	270	270
Utility Examination Fee	2311	1	110	110
Pages:				
Claims:				
Claims in excess of 20	2202	73	26	1898
Independent claims in excess of 3	2201	2	110	220
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**2580**

Electronic Acknowledgement Receipt

EFS ID:	8358918
Application Number:	12876113
International Application Number:	
Confirmation Number:	1607
Title of Invention:	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES
First Named Inventor/Applicant Name:	Ricardo H. Bruce
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.042
Receipt Date:	04-SEP-2010
Filing Date:	
Time Stamp:	05:31:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$2580
RAM confirmation Number	5343
Deposit Account	504068
Authorized User	URIARTE,STEPHEN R.

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Drawings-only black and white line drawings	6005_042_FIGs_20100904.pdf	70637 a00b5f91699eac2767485e0ef0a8cd1fff7cc5da	no	4
Warnings:					
Information:					
2	Application Data Sheet	6005_042_ADS_20100904.pdf	968267 3481c19d26935385aea58228c6db3df261967b73	no	6
Warnings:					
Information:					
3	Specification	6005_042_Spec_20100904B.pdf	227264 d076216f12b1f7c1fb50fc3bb268f24dba7de049	no	41
Warnings:					
Information:					
4	Miscellaneous Incoming Letter	6005_042_RecordationCoverSheet_20100904.pdf	1455799 c721283a03aec96fac8bec2f62968c1d204e0b69	no	3
Warnings:					
Information:					
5	Miscellaneous Incoming Letter	6005_042_Assign4SigsExceptSOMERA_20100904.pdf	343774 b395db5da5f3e3ae118b5c46d3b4632dcca88f2f	no	2
Warnings:					
Information:					
6	Fee Worksheet (PTO-875)	fee-info.pdf	38199 2fcc1e834f3198ad02780f304967658c44bca6a8	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	3103940		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

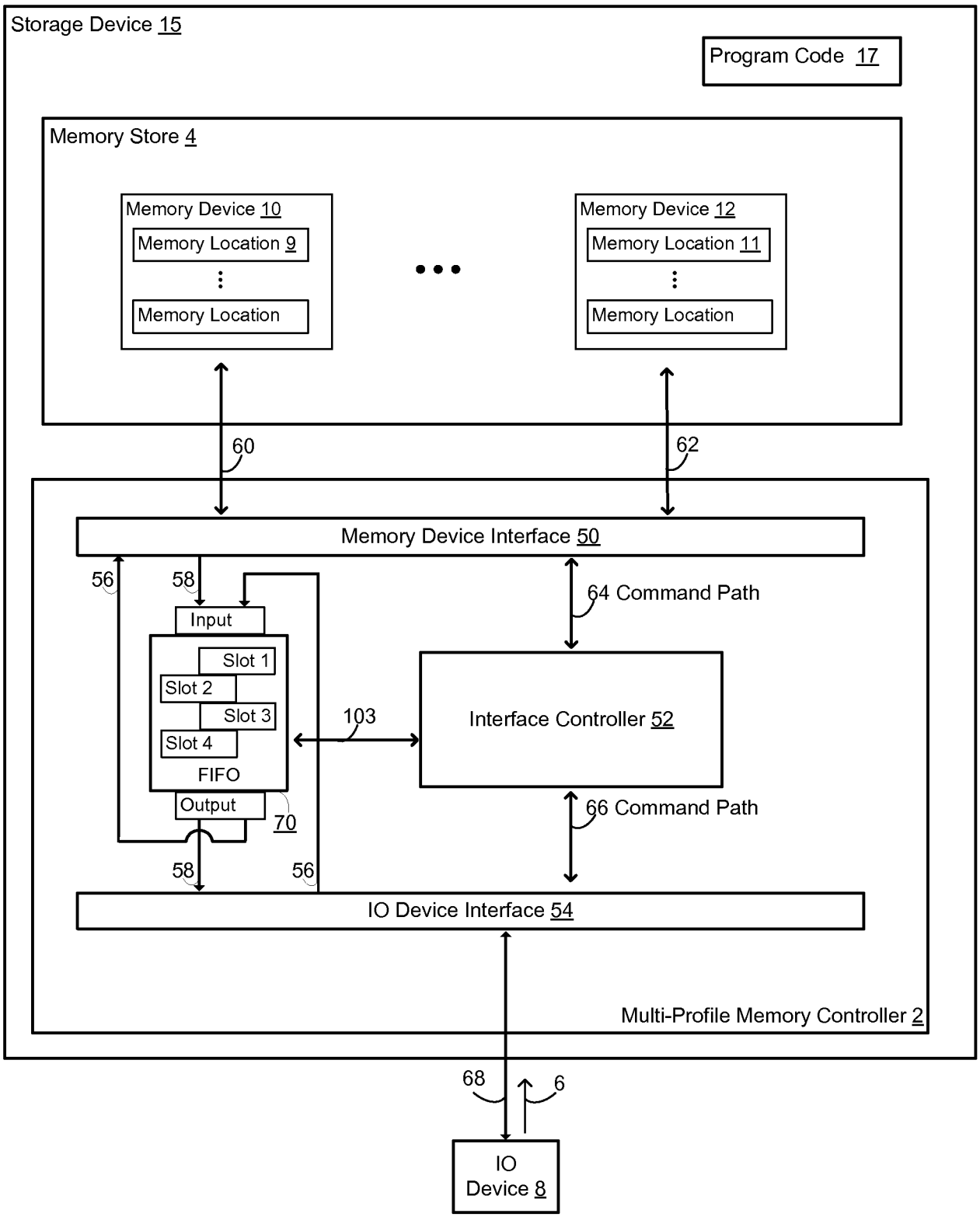
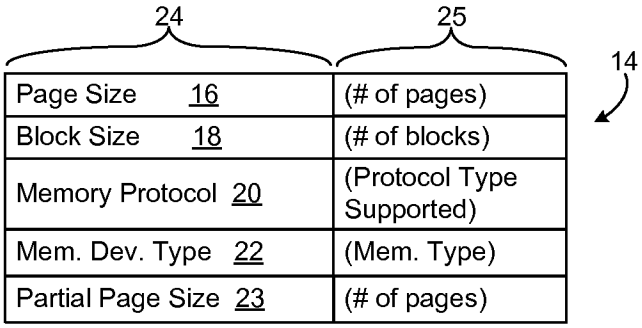
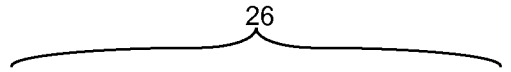

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Program Code 17
Memory Store 4
Memory Device 10
Memory Location 9
Memory Location
Memory Device 12
Memory Location 11
Memory Location
60
62
Memory Device Interface 50
56
58
64 Command Path
Input
Slot 1
Slot 2
Slot 3
Slot 4
FIFO
Output
70
103
Interface Controller 52
66 Command Path
58
56
IO Device Interface 54
Multi-Profile Memory Controller 2
68
6
IO
Device 8

FIG. 1



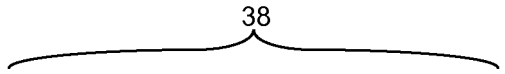
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Block Size 18	(# of blocks)
Memory Protocol 20	(Protocol Type Supported)
Mem. Dev. Type 22	(Mem. Type)
Partial Page Size 23	(# of pages)

FIG. 2A



Page Size 28	1024
Block Size 30	2048
Memory Protocol 32	ONFi
Mem. Dev. Type 34	NAND Flash
Partial Page Size 36	512

FIG. 2B



Page Size 40	512
Block Size 42	8192
Memory Protocol 44	ONFi
Mem. Dev. Type 46	NAND Flash
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FIG. 2C

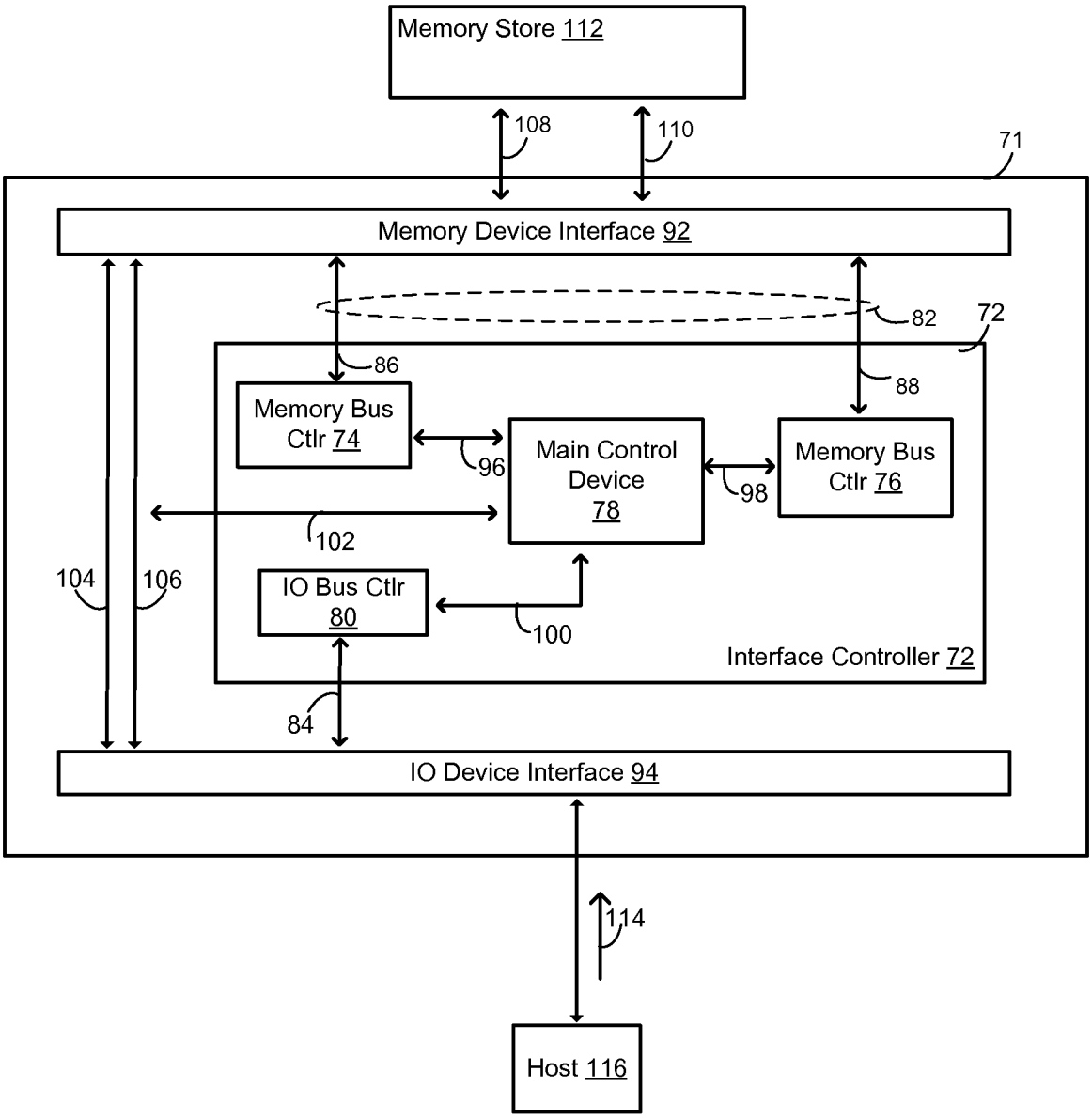

Memory Store 112
108
110
71
Memory Device Interface 92
82
72
86
88
Memory Bus Ctlr 74
96
Main Control Device 78
98
Memory Bus Ctlr 76
102
104
106
IO Bus Ctlr 80
100
Interface Controller 72
84
IO Device Interface 94
114
Host 116

FIG. 3

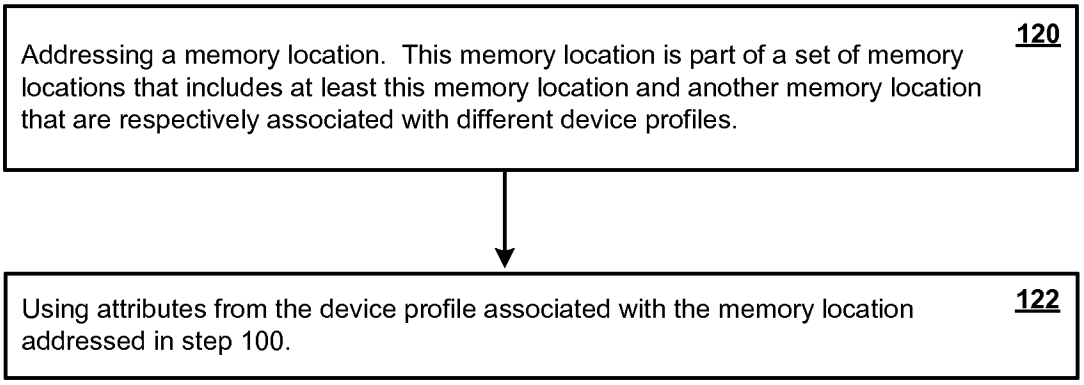


FIG. 4

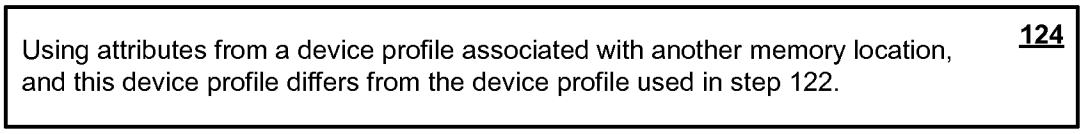


FIG. 5

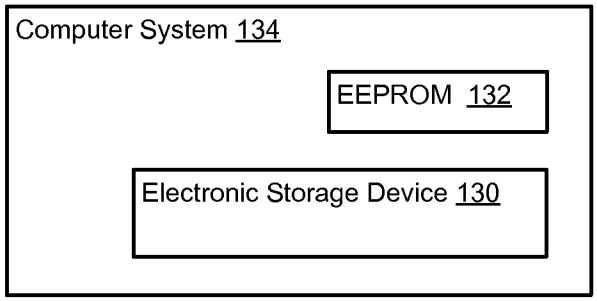


FIG. 6

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	6005.042
	Application Number	
Title of Invention	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1 Remove

Applicant Authority	◉ Inventor	○ Legal Representative under 35 U.S.C. 117	○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Ricardo	H.	BRUCE	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Union City	State/Province	CA	Country of Residence[i]	US

Citizenship under 37 CFR 1.41(b)[i]	US

Mailing Address of Applicant:

Address 1	33041 Regents Blvd		
Address 2			
City	Union City	State/Province	CA
Postal Code	94587	Country[i]	US

Applicant 2 Remove

Applicant Authority	◉ Inventor	○ Legal Representative under 35 U.S.C. 117	○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Marlon	B.	VERDAN	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Paranaque City, Metro Manila	Country Of Residence[i]	PH

Citizenship under 37 CFR 1.41(b)[i]	PH

Mailing Address of Applicant:

Address 1	905 Leon Allanigue St.		
Address 2	Barangay Village Sucat		
City	Paranaque City, Metro Manila	State/Province	
Postal Code	1700	Country[i]	PH

Applicant 3 Remove

Applicant Authority	◉ Inventor	○ Legal Representative under 35 U.S.C. 117	○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Margaret Anne	N.	SOMERA	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Caloocan City Metro Manila	Country Of Residence[i]	PH

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	6005.042
	Application Number	
Title of Invention	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES	

Citizenship under 37 CFR 1.41(b) i	PH		
Mailing Address of Applicant:			
Address 1	124 Madocay St.		
Address 2			
City	Caloocan City, Metro Manila	**State/Province**	
Postal Code	1400	**Country**i	PH

Applicant 4 Remove

Applicant Authority (•) Inventor ( ) Legal Representative under 35 U.S.C. 117 ( ) Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Rowenah Michelle	D.	JAGO-ON	

Residence Information (Select One) ( ) US Residency (•) Non US Residency ( ) Active US Military Service

City	Pasig City	**Country Of Residence**i	PH
Citizenship under 37 CFR 1.41(b) i	PH		
Mailing Address of Applicant:			
Address 1	Unit 302 Missouri Riverfront Residences		
Address 2	Dr. Sixto Antonio Ave., Caniogan		
City	Pasig City	**State/Province**	
Postal Code	1606	**Country**i	PH

Applicant 5 Remove

Applicant Authority (•) Inventor ( ) Legal Representative under 35 U.S.C. 117 ( ) Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Maria Eliza	B.	DE BELEN	

Residence Information (Select One) ( ) US Residency (•) Non US Residency ( ) Active US Military Service

City	Quezon City	**Country Of Residence**i	PH
Citizenship under 37 CFR 1.41(b) i	PH		
Mailing Address of Applicant:			
Address 1	20-A Latukan St., Manresa		
Address 2			
City	Quezon City	**State/Province**	
Postal Code	1115	**Country**i	PH

Applicant 6 Remove

Applicant Authority (•) Inventor ( ) Legal Representative under 35 U.S.C. 117 ( ) Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Ron Kelvin	B.	PALACOL	

Residence Information (Select One) ( ) US Residency (•) Non US Residency ( ) Active US Military Service

City	Laguna	**Country Of Residence**i	PH
Citizenship under 37 CFR 1.41(b) i	PH		

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	6005.042
	Application Number	
Title of Invention	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES	

Mailing Address of Applicant:			
Address 1	10 Duhat St., Phase 2 Pacita Complex II San Pedro		
Address 2			
City	Laguna	State/Province	
Postal Code	4023	Country[i]	PH

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	64180		
Email Address	mail@uriartelaw.com	Add Email	Remove Email

Application Information:

Title of the Invention	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES		
Attorney Docket Number	6005.042	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	4	Suggested Figure for Publication (if any)	1

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☒ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	6005.042
	Application Number	
Title of Invention	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES	

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Prior Application Status	Pending		Remove
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Signature	/Stephen Uriarte/	Date (YYYY-MM-DD)	2010-09-04

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	6005.042
	Application Number	
Title of Invention	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES	

First Name	Stephen	Last Name	Uriarte	Registration Number	40854

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This patent application is submitted in the names of inventor, Ricardo H. Bruce, Marlon B. Verdan, Margaret Anne N. Somera, Rowenah Michelle D. Jago-on, Maria Eliza B. DeBelen, and Ron Kelvin B. Palacol, assignors to BiTMICRO Networks, Inc. Inc. of Fremont, California.

TITLE OF THE INVENTION

Multi-Profile Memory Controller for Computing Devices

CROSS-REFERENCE(S) TO RELATED APPLICATIONS

[001] This application claims the benefit of United States Provisional Application, entitled "Multi-Profile Memory Controller for Computing Devices", filed on 04 September 2009 and having Serial No. 61/239,794, which is hereby incorporated by reference as if fully set forth herein.

BACKGROUND

(1) Technical Field

[002]The present invention relates to multi-profile memory controllers and computing devices, such as solid-state storage devices, that use these multi-profile memory controllers.

(2) Background Art

[003]Multi-profile memory controllers have been traditionally designed to operate with memory stores or modules that comprise of memory devices which use the same memory device characteristics, such as block size. Some of these multi-profile memory controllers are disposed to operate with memory devices that use flash memory cells which utilize relatively large block sizes, such as 128 Kb or greater. Flash memory devices that have a relatively large block size generally provide better sequential memory access performance than flash memory devices that have a relatively small block size. Larger block sizes are commonly employed because flash

memory devices that are disposed with larger block sizes tend to exhibit greater memory density than flash memory devices that use smaller block sizes. In addition, these higher density flash memory devices tend to be generally more cost effective than flash memory devices with less memory density.

[004]A multi-profile memory controller that employs flash memory devices that have relatively large block sizes incurs some disadvantages, however, because it suffers from relatively higher read-modify-write cycle latency, higher random memory access latency and lower random IOPS (input/output operations per second). Consequently, there is a need for a multi-profile memory controller that can operate with memory locations, memory devices, or both that are associated with different memory attributes, different attribute qualifiers, or the like, while minimizing or avoiding some or all of the above described disadvantages.

SUMMARY

[005] The present invention pertains to a multi-profile memory controller and devices that use multi-profile memory controllers. More particularly, the present invention pertains to a multi-profile memory controller and related methods and systems that can operate with memory locations, memory devices, or both which are associated with different memory attributes, different attribute qualifiers, or the like, while minimizing or avoiding some or all of the disadvantages of the prior art.

BRIEF DESCRIPTION OF THE DRAWINGS

[006] ***FIG. 1*** illustrates a multi-profile memory controller, which is disposed to receive and process memory transaction requests from a host, in accordance with one embodiment of the present invention;

[007] ***FIGS. 2A-2C*** illustrate device profiles for use with a multi-profile memory controller in accordance with yet another embodiment of the present invention;

[008] ***FIG. 3*** illustrates a multi-profile memory controller in accordance with yet another embodiment of the present invention;

[009] ***FIG. 4*** illustrates a method of performing memory transactions on memory locations that are associated with different device profiles in accordance with yet another embodiment of the present invention;

[0010] ***FIG. 5*** illustrates a further embodiment of the method illustrated in ***FIG. 4***.

[0011] ***FIG. 6*** illustrates a block diagram of a computer system that uses an electronic storage device which employs a multi-profile memory controller to perform one or both of the methods disclosed in ***FIGS 4*** and ***5*** above in accordance with yet another embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0012] In the following detailed description, for purposes of explanation, numerous specific details are set forth to provide a thorough understanding of the various embodiments of the present invention. Those of ordinary skill in the art will realize that these various embodiments of the present invention are illustrative only and are not intended to be limiting in any way. Other embodiments of the present invention will readily suggest themselves to such skilled persons having the benefit of this disclosure.

[0013] In addition, for clarity purposes, not all of the routine features of the embodiments described herein are shown or described. It is appreciated that in the development of any such actual implementation, numerous implementation-specific decisions must be made to achieve the developer's specific goals. These specific goals will vary from one implementation to another and from one developer to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming but would nevertheless be a routine engineering undertaking for those of ordinary skill in the art having the benefit of this disclosure.

[0014] The present invention relates to multi-profile memory controllers and computing devices that use these multi-profile memory controllers, such as storage devices, computers, and other types of devices that use memory. More particularly, the present invention relates to a multi-profile memory controller disposed to perform memory transactions using different device profiles. This type of multi-profile memory controller may be referred to herein as a "multi-profile memory controller". In accordance with one embodiment of the present invention, ***FIG. 1*** illustrates a multi-profile memory controller **2** for performing a memory transaction on a memory store **4** in response to receiving a memory transaction request **6**. Memory transaction request **6** may be initiated by an IO device, such as IO device **8**, or other device disposed to initiate such a request. Memory store 4 may be part of a computing device or equivalent device, such as storage device **15**, that includes multi-profile memory controller 2. In the example shown, multi-profile memory controller 2 executes computer or machine executable instructions, such as program code 17, which enables multi-profile memory controller 2 to manage, control or both the flow of data between IO device 8 and memory store 4.

[0015] Memory store 4 includes addressable memory locations, such as memory locations ***9*** and ***11***, that are respectively associated with a set of at least one memory attribute. The term "memory attribute", which may also be referred to as "attribute" herein, is defined to include a characteristic of a memory location that is related to accessing or addressing the memory location. For example, an attribute that is associated with a particular memory location may include the memory device type of a memory device in which the memory location is located or addressable, or of a memory device associated with a memory space in which the memory location is subset. In ***FIG. 1***, memory locations 9 and 11 are located or addressable in memory devices **10** and **12**, respectively. Other examples of an attribute of a memory location may include, where applicable, the block size used by the memory device, the page size used by the memory device, the memory protocol or specification supported by the memory device, and the partial page size used by the memory device.

[0016] In one embodiment of the present invention, each set of memory attributes may be organized into a device profile. Each attribute kept in a device profile is associated with data, named "attribute qualifier," that qualifies the attribute, such as an attribute value or attribute type. The association between an attribute and its corresponding attribute qualifier may be accomplished by using any known means, such as by using a database, a table, index, or an equivalent device, that is accessible to multi-profile memory controller **2**. For example, device profile **14** in ***FIG. 2A*** may be used to represent at least one attribute **24** of a memory location, and each attribute respectively corresponds to an attribute qualifier **25**. These attributes include a page size **16**, a block size **18**, a memory protocol **20** supported by the memory device in which the memory location is addressable, a memory device type

22, and a partial page size **23**. Attribute qualifier **25** is in the form of a value or type. In ***FIG. 2A***, attribute page size **16** corresponds to an attribute value in bytes per page, attribute block size **18** corresponds to an attribute value in pages per block, attribute memory protocol **20** corresponds to a memory device specification or protocol supported by the memory device associated with the memory location, attribute memory device type **22** corresponds to a memory device type of the memory device associated with the memory location, attribute partial page size **23** corresponds to an attribute value in bytes per partial page.

[0017] Referring to ***FIGS. 1 and 2B*** for example, memory location **9** in memory store **4** may have a device profile **26** that includes the following attributes: a page size **28** associated with an attribute value of 1024 bytes, a block size **30** associated with an attribute value of 2048 pages, a memory protocol **32** associated with an attribute type that represents the ONFi specification, a memory device type **34** associated with an attribute type that represents a NAND flash memory device, and a partial page size ***36*** associated with an attribute value of 512 bytes. In another example as shown in ***FIG. 2C***, memory location 11 in memory store 4 may have a device profile **38** that includes the following attributes: a page size **40** associated with an attribute value of 512 bytes, a block size **42** associated with an attribute value of 8192 pages, a memory protocol **44** associated with an attribute type that represents the ONFi protocol, a memory device type **46** associated with an attribute type that represents a NAND flash memory device, and a partial page size **48** associated with an attribute value of 256 bytes.

[0018] A device profile may have any number of attributes, while any two device profiles may have any number of shared attributes equal to or greater than zero.

Multi-profile memory controller 2 can perform memory transactions using different device profiles. In this example, memory locations 9 and 11 have different device profiles. Memory locations that are addressable from the same memory device may share the same device profile although this approach is not intended to be limiting in any way. In another embodiment, different device profiles may be respectively associated with different memory locations that are addressable from the same memory device but which have different attributes, shared attributes having different attribute qualifiers, or both. Device profiles are different if they differ by attribute, by number of attributes, by attribute qualifier for shared attributes, or any combination of these. Shared attributes include at least two attributes that are the same. In ***FIGS. 2B*** and ***2C***, device profiles 26 and 38 have the following shared attributes: a page size, block size, memory device type, memory protocol, and partial page size. In the example shown, device profiles 26 and 38 neither differ by their number of attributes nor by their attributes but differ by attribute qualifier for their sets of shared attributes. Specifically, page sizes 28 and 40; block sizes 30 and 42, and partial page sizes 36 and 48 differ by their attribute values, while memory protocols 32 and 44, and memory device types 34 and 46 differ by their attribute types. In another embodiment (not shown), device profiles 26 and 38 may have the same attributes but at least one set of shared attributes differs by an attribute qualifier, such an attribute value or attribute type. In yet another embodiment (not shown) device profiles 26 and 38 have a different number of attributes. These alternative embodiments are not intended to be exhaustive but are provide to illustrate the variety in which device profiles may differ.

[0019] The type and location of a memory device or memory store used to store device profiles are not intended to limit the scope of the invention in any way. In the example shown in ***FIG. 1***, the device profiles 26 and 38 for memory locations 9 and 11 are stored in memory store 4. In an alternative embodiment, device profiles 26 and 38 may be stored in another type of non-volatile memory, such as an EPROM, battery-backed volatile memory, or their respective equivalent, which is not shown to avoid overcomplicating this disclosure. The term "memory device" refers to any type of memory device that can write to or read data from an addressable location in response to a memory device command, such as a read or write command. For example, memory devices 10 and 12 may be each disposed to be in the form of a NAND flash memory device integrated circuit, sometimes referred to as a flash chip. Using a NAND flash memory device is not intended to be limiting in any way, and any form of non-volatile memory, such as a NOR flash memory device, may be used. A NAND flash memory device includes a set of addressable non-volatile memory cells, named flash blocks, and each memory cell may be single or multi-level.

[0020] A flash memory device permits memory operations, such as a write or read operation, to be performed on these flash blocks according to a protocol supported by the flash memory device. Memory device 10 and 12 may each be implemented using a NAND flash memory device that complies with the Open NAND Flash Interface Specification, commonly referred to as ONFI Specification. The term "ONFI Specification" is a known device interface standard created by a consortium of technology companies, called the "ONFI Workgroup". The ONFI Workgroup develops open standards for NAND flash memory devices and for devices that communicate with these NAND flash memory devices. The ONFI Workgroup is headquartered in

Hillsboro, Oregon. Using a flash memory device that complies with the ONFI Specification is not intended to limit the embodiment disclosed. One of ordinary skill in the art having the benefit of this disclosure would readily recognize that other types of flash memory devices employing different device interface protocols may be used, such as protocols compatible with the standards created through the Non-Volatile Memory Host Controller Interface ("NVMHCI") working group. Members of the NVMHCI working group include Intel Corporation of Santa Clara, California, Dell Inc. of Round Rock, Texas and Microsoft Corporation of Redmond, Washington.

[0021] Memory store 4 is not intended to be limited to flash memory devices, and may include other types of memory devices, such as volatile memory like SRAM or DRAM; non-volatile memory, such as a NOR flash memory device or battery-backed volatile memory; a hard disk drive; and the like. The term "IO device" is intended to cover a broad range of devices that can request a memory transaction, such as a read or write transaction. For example, a computing system or computing-enabled device that is configured to include the function of requesting a memory transaction from memory store 4 is an IO device for purposes of this disclosure. An IO device may or may not have the capability to map data that is subject to a memory transaction request in a memory map table. This data may include a file or data portions of the file. IO memory mapping and memory tables are known and thus, are not further described herein. An IO device may also be referred to herein as a "host".

[0022] In ***FIG. 1***, multi-profile memory controller 2 may be configured to include a memory device interface **50**, an interface controller **52** and an IO device interface **54**. Communication path **64** couples memory device interface 50 with interface controller 52, while communication path **66** couples interface controller 52 with IO

device interface 54, which enables these coupled devices to assert or transmit signals across their respective communication paths. Interface controller 52 and memory device interface 50 communicate through communication bus 64. Communication through communication path 64 includes interface controller 52 sending information, such as command details, to memory device interface 50 and receiving status from memory device interface 50. In addition, interface controller 52 communicates with IO device interface 54 though communication path 66. Communication through communication path 66 includes interface controller 52 receiving status and request information from IO device interface 54 and sending commands to IO device interface 54. Communication paths 64 and 66 may be implemented in the form of a bus that includes control or command lines. A set of control or command lines are sometimes generically referred to as a control bus or a command line bus, respectively.

Data Paths 56 & 58

[0023] At least one data path, such as data paths **56** and **58**, are used to couple IO device interface 54 with memory device interface 50, enabling these devices to transfer data, such as data that will be read from or written to memory store **4**, with each other. In one embodiment of the present invention, data paths 56 and 58 may be implemented logically by using a single FIFO buffer 70, named "FIFO". FIFO **70** includes a set of queue slots and may be used to provide more than one logical data path by associating certain queue slots as a particular data path. For example, all odd numbered queue slots in FIFO 70 may be designated as one data path, such as data path 56, while all even numbered queue slots in FIFO 70 another data path, such as data path 58. Interface controller 52 is also coupled to FIFO 70 to provide FIFO status to memory device interface 50 and IO device interface 54. When implemented

in this manner, FIFO 70 functions as a logical form of data paths 56 and 58 because although a single instance of FIFO is used, it provides two logical data paths through which data may be transferred between memory device interface 50 and IO device interface 54. In another embodiment of the present invention, data paths 56 and 58 may each be implemented separately in the form of a FIFO, respectively. Each FIFO (not shown) may be used to queue data transferred between memory device interface 50 and IO device interface 54 with interface controller providing FIFO status to memory device interface 50 and IO device interface 54.

[0024] Data paths 56 and 58, whether implemented logically or physically, may be used as bi-directional or unidirectional data paths. When used as a bi-directional data path, data may travel in both directions. For example, bi-directional data path 56, data path 58 or both may be used to transfer both read and write data. When used as a one way data path, data may travels only in one direction on a particular data path. For example, data path 56 may be used solely to transfer data from IO device interface 54 to memory device interface 50, while data path 58 may be used solely to transfer data from memory device interface 50 to IO device interface 54. Figure 1 illustrates an embodiment of multi-profile memory controller 2 that uses FIFO 70 configured to provide unidirectional data paths 56 and 58 in logical form.

Memory Buses 60 & 62

[0025] Memory device interface 50 is coupled to memory store 4 through at least one bus, such as buses **60** and **62**. Buses 60 and 62 are shown respectively coupled to memory devices 10 and 12. The number of memory buses used to couple multi-profile memory controller 2 to memory devices associated with memory store 4 is not intended to be limiting. More than one memory device may be coupled to

memory device interface 50. The means and method of selecting a memory device or addressing a memory location from a set of memory devices by using a single memory bus are known. For example, select lines (not shown) may be used. In addition, the number of data buses or FIFOs used is also not intended to be limiting. As would be evident to one of ordinary skill having the benefit of this disclosure, using more than one data bus, FIFO, or both, increases the available pathways through which data may be transmitted between IO device interface 54 and memory device interface 50.

[0026] Memory device interface 50 operates as the communication interface between memory store 4 and devices that form part of multi-profile memory controller 2, such as interface controller 52 and IO device interface 54. Memory device interface 50 monitors the availability of a memory device that has been targeted for a memory device operation, and routes commands and data between multi-profile memory controller 2 and the memory device, such as memory device 10 or 12,. Memory device interface 50 also provides the required physical signaling, such as by asserting electrical signals on memory bus 60, memory bus 62, or both, that will enable memory device interface 50 to use the memory bus to transfer commands and data associated with the memory device operation.

Memory Device Interface 50

[0027] Memory device interface 50 is responsive to commands received from interface controller 52 via a suitable communication path or bus, such as communication path 64, which enables interface controller 52 to perform a memory transaction operation, such as a read or write memory operation on a selected memory device, such as memory device 10 or 12. Data associated with this read or

write memory operation is transferred between memory device interface 50 and IO device interface 54 via at least one data path, such as data path 56, data path 58 or both. In the examples shown in ***FIGS. 1*** and ***2B-2C***, memory device interface 50 supports the ONFi memory protocol, which renders it compatible with memory device 10 and 12 since they are NAND flash memory devices that support the ONFi memory protocol.

IO Device Interface 54

[0028] IO device interface 54 operates as the communication interface between an IO device, such as IO device 8, and devices that form part of multi-profile memory controller 2, such as memory device interface 50 and interface controller 52. IO device interface 54 enables multi-profile memory controller 2 and IO device 8 to communicate with each other through a protocol supported by both devices, enabling multi-profile memory controller 2 to receive a memory transaction request 6 that was sent by IO device 8 through a suitable communication pathway, such as communication bus 66. The type of protocol used is not intended to be limiting in any way although this protocol should be supported by IO device interface 54 and any IO device that is selected to operate with IO device interface 54. IO device interface 54 also provides the required physical signaling, such as by asserting electrical signals on communication path **68**, that will enable IO device interface 54 to use path 68 when communicating with an IO device, such as by receiving memory transaction request 6. The number of IO devices through which IO device interface can communicate is not intended to be limiting in any way.

Operation

[0029] After receiving memory transaction request 6 from an IO device, IO device interface 54 transfers this request to interface controller 52 through communication path 66. Interface controller 52 processes memory transaction request 6 by interpreting the memory transaction request and performing a memory transaction on a memory location. Performing a memory transaction includes addressing a memory location that is associated with a device profile, and that is located in or addressable in a memory device. The addressing of this memory location by interface controller 52 may be part of the memory read or write transaction indicated in the memory transaction request. Interpreting memory transaction request 6 includes determining whether the memory transaction pertains to a memory read or a memory write transaction, and identifying an address from the memory transaction request. In the embodiment shown, this identified address is a logical address, and interface controller **52** translates this logical address into a physical address, which points to the memory location, which may also be referred to herein as "target memory location". The manner of translating a logical address to a physical address is also not intended to be limiting in any way. Any method may be used that is commonly known by those of ordinary skill in the art. For example, a logical to physical address memory map that maps each logical address to target memory locations may be used. In addition, more than one physical address may be mapped to a single logical address. In the embodiment shown in *FIG. 1*, if multiple physical addresses or target memory locations are mapped to a single logical address, all of these target memory locations are associated with the same device profile although this arrangement is not intended to limit the scope or spirit of the herein invention in any way. Thus, in this particular non-limiting embodiment, for each memory transaction requested, multi-profile memory controller 2 can perform

memory operations on more than one memory location. These memory locations are associated with device profiles that are either the same, or at the very least have at least one shared attribute in common that have the same attribute qualifier. For example, these memory locations may have device profiles that have a shared attribute of block size and the same block size attribute value.

[0030] Interface controller 52 also determines command details necessary to cause the interpreted memory transaction to be performed by multi-profile memory controller 2 through its components. These command details include the memory device from which the target memory location is addressable by a multi-profile memory controller component, such as memory device interface 50. This memory device may also be referred to herein as a "target memory device". In one embodiment of the present invention, multi-profile memory controller 2 through interface controller 52 uses a memory map (not shown) that associates memory devices with physical addresses. Multi-profile memory controller 2 also determines the transfer sizes to use when causing a memory transaction to be performed on the target memory device.

[0031] After identifying these command details, the multi-profile memory controller obtains attributes from the device profile associated with the target memory location, and determines whether the target memory location is available by causing memory device interface 50 to determine the status of the target memory device and to inform interface controller 52 when this target memory device is ready for a memory operation. When the target memory device is ready, multi-profile memory controller 2 performs the memory transaction by causing memory device interface 50 to perform a memory operation on the target memory location and target memory

device. Multi-profile memory controller 2 also causes data to be transferred via at least one suitable bus or communication path, such as data paths 56 and 58, to the target memory location and the target memory device from IO device interface 54 if the memory transaction request pertains to a memory write transaction, or from the target memory location and the target memory device to IO device interface 54 if the memory transaction request pertains to a memory read transaction.

[0032] In ***FIG. 1*** for example, if the logical address translates to a physical address pointing to memory location 9 in memory device 10, multi-profile memory controller 2 instructs memory device interface 50 to check the status of memory device 10. When multi-profile memory controller 2 through memory device interface 50 detects that memory device 10 is ready for a memory transaction, multi-profile memory controller 2 through interface controller 52 provides the instructions necessary for causing memory device interface 50 to perform at least one memory operation as required by the memory transaction requested by memory transaction request 6.

[0033] In one embodiment of the present invention, the transfer size selected is a function of the data size of the subject to memory transaction request 6, and the attributes in a device profile associated with a target memory location. These attributes may include any combination of the following: the page size attribute, the block size attribute, and the partial page size attribute in device profile 26 of memory location 9 although this example is not intended to be limiting in any way. Any transfer size can be selected using any method and more than one transfer size can be used for memory transactions that require multiple transfers arising from more than one memory operation. In addition, for illustration purposes only and in one

example embodiment, if the data size is greater than the page size attribute value in device profile 26, multi-profile memory controller 2 uses a transfer size equal to at least the page size attribute value for each memory operation transfer for the memory transaction requested until the remaining data not yet transferred from a requesting IO device is less than the page size attribute. In this case, multi-profile memory controller 2 can then use a partial page size attribute value for the transfer size of the next memory operation transfer until all of the data has been transferred to memory location 9. If the data size is greater than the block size attribute value in device profile 24, multi-profile memory controller 2 uses a transfer size equal to at least the block size attribute value for each memory operation transfer for the memory transaction requested until the remaining data not yet transferred is less than the block size attribute value. If the remaining data not yet transferred reduces to less than the block size attribute value, multi-profile memory controller 2 then selects a transfer size equal to the page size attribute value if this remaining data has a data size, named "remaining data size", that is at least equal to the page size attribute, or equal to the partial page size attribute value if this remaining data size is less than the page size attribute.

[0034] In another example, by using a multi-profile memory controller 2, which supports memory locations that have different device profiles, a host or IO device, such as IO device 8, can use a logical address that maps to at least one target memory location that is associated with a device profile that is optimal for the type of data subject to a memory transaction request initiated by IO device 8, and another target memory location that is associated with another device profile that is optimal for the type of data subject to another memory transaction request initiated by IO

device 8. IO device 8 may use a memory write transaction request that uses a logical address that maps to at least one target memory location that is associated with a device profile that includes a block size attribute value that is the largest available from the other device profiles associated with a set of memory locations available for addressing by multi-profile memory controller 2. This transaction command detail may be desired if the data subject to the memory transaction request is of a sequential type, and the memory type attribute value also associated with the device profile is a NAND flash memory device.

[0035] In yet another example, IO device 8 may use a memory transaction request that uses a logical address that maps to at least one target memory location which is associated with a device profile that includes a block size attribute value that is the smallest available from the other device profiles associated with a set of memory locations available for addressing by multi-profile memory controller 2. This transaction command detail may be desired if the data subject to the memory transaction request is random nature. In yet another further example, IO device 8 may use a memory transaction request that uses a logical address that maps to at least one target memory location that is associated with a device profile that includes a partial page size attribute value. This transaction command detail may be desired if the data subject to the memory transaction request is random in nature, and if the data size of the data subject to the write transaction is at most equal to the partial page size attribute value. The above examples are not intended to be limiting in any way. For instance, instead of IO device 8, multi-profile memory controller 2 includes program code or uses a memory map that determines or causes which target memory location is used to support a memory transaction for a particular data type.

[0036] Referring now to ***FIG. 3***, another embodiment of a multi-profile memory controller **71** is illustrated. Multi-profile memory controller 71 includes an interface controller **72** that may be implemented using a set of memory bus controllers, such as memory bus controller **74** and **76**, a main control device **78**, an IO bus controller **80**, communication paths **82** and **84**, and a control path **102**. Communication path 82 includes control paths **86** and **88**, which are used by memory bus controllers 74 and 76 and main control device 78, respectively, to assert commands and certain information on a memory device interface **92**, such as the physical or actual address of a memory location targeted for a memory transaction, and commands supported by the memory devices, such as commands supported by ONFi compliant memory devices. For instance, a value of 70h is a request for status from a memory device by a memory bus controller, while 80h is commands a memory device to write the data asserted on an address line coupled to the memory device. In the embodiment disclosed in FIG. 3, the commands, information, memory and device status are routed to main control device 78 via control path 86 or 88 and communication path 96 or 98 by memory bus controllers, such as 74 or 76, respectively, depending on which memory bus controller is associated with the memory device providing the memory device status. Although as further described below, main control device 78 determines whether a target memory location is available, a memory bus controller performs the transfer of this availability status from the target memory location to main control device 78.

[0037] Each memory bus controller is disposed to access memory devices and to load the selected flash profile attributes as part of a memory read or memory write transaction. In accordance with one embodiment of the present invention, the

memory devices in memory store 112 are grouped so that each of these memory devices are associated with only one memory bus controller, such as memory bus controller 74 or 76. Associating each memory device with only one memory bus controller permits simultaneous memory device accesses that equal in number to the memory bus controllers used by interface controller 72. In FIG. 3, interface controller 72 includes two (2) memory bus controllers but the number of memory bus controllers is not intended to be limiting in any way, and any number of memory bus controllers may be employed. For instance, (not illustrated), interface controller 72 may be disposed with four (4) memory bus controllers, which permits each of these memory bus controllers to access collectively a maximum of four memory devices simultaneously.

[0038] Communication path **84** couples interface controller 72 with IO device interface **94**, enabling main control device 78 to receive status from IO device interface 94 via IO bus controller 80. Communication paths **96** and **98** enable main control device 78 to communicate with memory bus controllers 74 and 76, respectively, while communication path **100** enables main control device 78 to communicate with IO bus controller 80. IO bus controller 80 functions as the controller for IO Device Interface 94, and enables main control device 78 to receive status and request information from IO device interface 94 and to send commands to IO device interface 94.

[0039] Control path **102** couples main control device 78 with data paths that are used by memory device interface 92 and IO device interface 94 to transfer data between each other, such as bidirectional data paths 104 and 106. Main control device 78 uses control path 102 to associate data transferred on a bidirectional data

path 104 or 106 with commands sent by a particular memory bus controller, such as memory bus controller 74 or 76. Bidirectional data paths 104 or 106 may be implemented in to have substantially the same form and function as unidirectional data paths 56 and 58 previously discussed with respect to FIG. 1 above. In addition, although FIG. 3 illustrates two bidirectional data paths 104 and 106, any number of bidirectional data paths may be employed.

[0040] Memory buses 108 and 110 couple memory device interface 92 to at least two memory locations, such as memory locations in memory devices (not shown) that form a memory store 112. These memory buses enable data to be read from or written to a memory device in memory store 112. The number of memory bus controllers used by interface controller 72 is not intended to be limiting in any way although in the example shown in ***FIG. 3***, one memory bus controller may be used for each memory bus supported by multi-profile memory controller 71. Interface controller 72, communication paths 82 and 84, memory device interface 92, IO device interface 94, and control path 102 have substantially the same functionality as interface controller 52, communication paths 64 and 66, control path 103, and memory buses 60 and 62, respectively, disclosed above in ***FIG. 1***.

[0041] Main control device 78 functions by receiving status from and by sending commands to memory control bus controllers 74 and 76, data paths 104 and 106 and IO bus controller 80. For example, after receiving a memory transaction request **114** from a host **116** through IO device interface 94 via communication path 84; IO bus controller 80 acknowledges memory transaction request 114 and informs main control device 78 via communication path 100 that a new memory transaction request, such as memory transaction request 114, has been received. Interface controller 72 via

main control device 78 interprets this memory transaction and performs the requested memory transaction. Main control device 78 performs the requested memory transaction by using at least one memory bus controller, such as memory bus controllers 74 or 76, to address, via memory device interface 92, a target memory location that is associated with a device profile, and that is located in or addressable in a memory device. The addressing of this memory location may be part of the memory read or write transaction indicated in memory transaction request 114. Main control device 78 interprets memory transaction request 114 by determining whether the memory transaction involves a memory read or a memory write transaction, and identifies an address from the memory transaction request.

[0042] In the embodiment shown, this identified address may be a logical address, which is translated by main control device 78 into a physical address, which points the target memory location. Interface controller 72 via main control device 78 also determines the command details necessary to cause the interpreted memory transaction to be performed by multi-profile memory controller 71 through its components. These command details include the memory device (not shown) in memory store 112 that is addressable by a multi-profile memory controller component, such as memory device interface 92. Main control device 78 also determines the transfer sizes to use when causing a memory transaction to be performed on the target memory device.

[0043] After identifying these command details, multi-profile memory controller 71 through main control device 78 obtains attributes from the device profile associated with the target memory location, and determines whether the target memory location is available by causing memory device interface 92 to determine or

monitor the status of the target memory device and to inform main control device 78 via control path 86 or 88 when this target memory device is ready for a memory operation. If memory device interface 92 indicates that this memory device is ready, main control device 78 performs the memory transaction by causing memory device interface 92 via a memory bus controller, such as 74 or 76, to perform a memory operation on the target memory location and target memory device in memory store 112. Main control device 78 also causes data to be transferred via at least one suitable bus or communication path, such as data paths 104 and 106, to the target memory location and the target memory device from IO device interface 94 if the memory transaction request pertains to a memory write transaction, or from the target memory location and the target memory device to IO device interface 94 if the memory transaction request pertains to a memory read transaction. In the example shown, main control device uses a control path 102 to manage data paths 104 and 106. After memory device interface 92 performs the memory operation on a target memory location, it provides operation status to interface controller 72 via control *path 90*. Interface controller 72 via main control device 78, in response, sends a memory transaction status to IO device interface 94 via IO bus controller 80, which causes IO device interface 94 to send status to a host.

[0044] ***FIG. 4*** illustrates a method of performing memory transactions on memory locations that are associated with different device profiles in accordance with yet another embodiment of the present invention. For example, also shown in ***FIGS. 1*** and ***2B-2C,*** these memory locations may be in the form of memory locations 9 and 11, while these different device profiles may be in the form of device profiles 26 and 38. In response to a memory transaction request, such as memory transaction

request 6, a memory location is addressed **120**. The addressing of this memory location may be addressed by a multi-profile memory controller, such as multi-profile memory controller 2. The addressing of this memory location may be part of a memory transaction indicated in the memory transaction request. The multi-profile memory controller also uses **122** attributes from a device profile associated with the memory location. ***FIG. 5*** illustrates a further embodiment of the method illustrated in ***FIG. 4***. In response to another memory transaction request, the attributes from a device profile that is associated with another memory location and that is different from the device profile used in step 122 is also used **124** by multi-profile memory controller 2. For example, the block attribute value in device profile 12 is used by multi-profile memory controller 2 to perform another memory transaction. For example, multi-profile memory controller 2 selects a transfer size that is equal to the block attribute value, and transfers the data subject to the memory transaction request.

[0045] The methods shown in ***FIGS. 4*** and ***5*** may be implemented by using the embodiments described herein, such as the embodiments discussed with respect to ***FIGS. 1*** through ***2C***. In addition, these methods may also be saved onto a computer readable medium, such as flash memory, EEPROM memory, USB memory device (such as a USB flash drive or USB memory key), hard disk drive, and the like, which can be read and executed by a machine, such as by an electronic storage device that employs a multi-profile memory controller. For example in ***FIG. 6***, electronic storage device **130** may be configured to access an EEPROM **132** on which at least one of the above methods is stored in a machine-readable form. In this example, electronic storage device 130 is part of a computer system **134** although this is not intended to

be limiting in any way. For example, electronic storage device 130 may be disposed to be function as a stand-alone mass storage device, whether configured as a direct-attached, network-attached storage (NAS), or storage area networking (SAN) device. In addition, the remaining components of computer system 134 is not illustrated to avoid overcomplicating the herein disclosure, and since a computer system that have the capability to access or use an electronic storage device is commonly known by those of ordinary skill in the art.

[0046] While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not be construed as limited by such embodiments. Rather, the present invention should be construed according to the claims below.

IN THE CLAIMS

We claim:

1. A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising:

addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

using attributes from said first and second device profiles.

2. The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device.

3. The method of claim 1, wherein said difference between said first and second device profiles includes different attributes; and said addressing said first memory location is made in response to a first memory transaction request; and

further including addressing said second memory location.

4. The method of claim 1, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes.

5. The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

6. The method of claim 5, wherein said different attribute qualifiers include different attribute values.

7. The method of claim 5, wherein said different attribute qualifiers include different attribute types.

8. The method of claim 5, wherein said shared attributes include a memory device type attribute.

9. The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

10. The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

11. The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

12. The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

13. The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of

attributes that differs in value from a second page size attribute from said second set of attributes.

14. The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes.

15. The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device, and said second memory device interface attribute corresponds to a DRAM device interface.

16. The method of claim 2, wherein said using attributes from said first and second device profile further includes using a first partial page size attribute from said first set of attributes that differs in value from a second partial page size attribute from said second set of attributes.

17. The method of claim 16:

said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute; and

further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute.

18. The method of claim 8, wherein said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

19. The method of claim 8, wherein said first memory device type attribute corresponds to a NAND flash memory device and said second memory device type attribute corresponds to a NOR flash memory device.

20. The method of claim 2, further including:

using an address corresponding to a memory location from said first memory device and transferring a first data set, and

using an address corresponding to a memory location from said second memory device and transferring a second data set.

21. The method of claim 20, wherein:

said first set of attributes includes a first page size attribute, and said first data set includes a first data set size; and

if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size.

22. The method of claim 20, wherein:

said second set of attributes includes a second page size attribute, and said second data set includes a second data set size; and

if said second data set size is greater than said second page size attribute, said transferring said second data set includes:

performing a set of write operations on said second memory device that includes using a second transfer size equal to said second page size attribute until a remaining portion of said second data set that has not yet been written to said second device is less than said second page size attribute, and

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

23. The method of claim 20, wherein:

said first set of attributes includes a page size attribute and a block size attribute;

said first data set includes a first data set size;

if said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes:

performing a set of write operations on said first memory device that includes using a second transfer size equal to said page size attribute until a remaining portion of said first data set that has not yet been written to said first device is less than said page size attribute,

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size; and

said second device profile.

24. The method of claim 1, wherein said using attributes from said first and second device profile further includes:

performing respective write operations on said first and second memory devices by at least using a transfer size at least equal to a partial page size attribute from said first set of attributes and performing at least one write operation on said second memory device by at least using a transfer size at least equal to a partial page size attribute value from said second set of attributes; and

said attribute difference includes different attribute values of said first and second partial page size attributes.

25. The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size attribute of said first memory device.

26. The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a block size attribute value that corresponds to a block size attribute of said first memory device.

27. The method of claim 26, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

28. The method of claim 2, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

29. A computer readable medium comprising computer executable instructions adapted to cause a method of performing memory transactions on a first memory location and a second memory location, said method comprising:

addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory device, and said second device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles; and

using attributes from said first and second device profiles.

30. The computer readable medium of claim 29, wherein:

said first memory location is part of a memory space associated with a first memory device;

said second memory location is part of a memory space associated with a second memory device; and

said first and second memory devices comprise at least a portion of a memory store.

31. The computer readable medium of claim 30, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

32. The computer readable medium of claim 30, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

33. The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

34. The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes.

35. The computer readable medium of claim 29, wherein said means for addressing further includes:

said first and second device profiles having at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

36. The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

37. The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values.

38. The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types.

39. The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute.

40. The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

41. The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

42. The computer readable medium of claim 36, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

43. The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes.

44. The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device.

45. A memory controller for performing memory transactions, said memory controller comprising:

a means for addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said means for addressing uses attributes from said first and second device profiles.

46. The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

47. The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

48. The memory controller of claim 46, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said use of said attributes from said first and second device profiles by said means for addressing includes using said different attribute qualifiers for said shared attributes.

49. The memory controller of claim 46, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

50. The memory controller of claim 45, wherein said means for addressing further includes addressing said second memory location.

51. The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

52. The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values.

53. The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types.

54. The memory controller of claim 51, wherein said shared attributes include a memory device type attribute.

55. The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

56. The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

57. The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

58. The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device.

59. A memory controller comprising:

an interface controller coupled to a memory device interface and an IO device interface;

said interface controller disposed to perform a memory transaction by addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile;

said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said addressing of said first memory location includes using said attributes from said first device profile.

60. The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile.

61. The memory controller of claim 59, wherein said interface controller includes:

a main control device coupled to said memory device interface and to said data path;

a first memory bus controller coupled to said control device and said memory device interface; and

an IO bus controller coupled to said IO device interface and said control device.

62. The memory controller of claim 61, wherein said IO bus controller is disposed to respond to said memory transaction request by acknowledging said request and providing status to said main control device.

63. The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction, coordinates the operation of said memory device interface, and manages the transfer of memory transaction data between said IO device interface and said memory device interface through a data path.

64. The memory controller of claim 59, wherein said buffer is a FIFO and said data path includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface.

65. The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots.

66. The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a plurality of queue slots that buffer data from said IO device interface to said memory device interface.

67. The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from said memory device interface to said IO device interface.

68. The memory controller of claim59, further including a second memory bus controller coupled to said main control device and said memory device interface.

69. The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes.

70. The memory controller of claim 59, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

71. The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

72. The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute.

73. The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values.

74. The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values.

75. The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type.

76. The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values.

77. The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types.

78. The memory controller of claim 71, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

79. The memory controller of claim 71, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

80. An electronic storage device, comprising:

a memory controller disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said memory controller using attributes from said first and second device profiles.

81. The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that

differs in attribute value from a second block size attribute from said second set of attributes.

82. The electronic storage device of claim 80, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

83. The electronic storage device of claim 80, said memory controller further disposed to:

perform a write operation on said first memory device, if said memory transaction request is associated with a write request;

perform a read operation on said first memory device, if said memory transaction request is associated with a read request; and

wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using said second device profile in response to receiving a second memory transaction request.

84. The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

85. The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values.

86. The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute.

87. The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types.

88. The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said shared attributes.

89. The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device.

90. The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

91. The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

92. The electronic storage device of claim 84, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

93. The electronic storage device of claim 80, wherein said memory controller is further adapted to:

use a first partial page size attribute by performing a write operation on said first memory device and using a transfer size at least equal to said partial page size attribute; and

use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute.

ABSTRACT

The present invention pertains to a multi-profile memory controller and devices that use multi-profile memory controllers. More particularly, the present invention pertains to a multi-profile memory controller and related methods and systems that can operate with memory locations, memory devices, or both which are associated with different memory attributes, different attribute qualifiers, or the like, while minimizing or avoiding some or all of the disadvantages of the prior art.

Date: 09/04/10

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PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

Application or Docket Number
12/876,113

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	82		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	270		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	110		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	93 minus 20 =	73	x$26	1898	OR	x$52	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	5 minus 3 =	* 2	x$110	220		x$220	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $270 ($135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			195			390	
			TOTAL	2580		TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 09/13/2010

KNGUYEN1 SALE #00000002 Mailroom Dt: 09/10/2010 504068 12876113
01 FC : 8021 40.00 DA

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/876,113	09/04/2010	Ricardo H. BRUCE	6005.042

CONFIRMATION NO. 1607

64180
URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

FORMALITIES LETTER

OC000000043564802

Date Mailed: 09/21/2010

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
  Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of $**65** for a small entity in compliance with 37 CFR 1.27, must be submitted with the missing items identified in this notice.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is $**65** for a small entity
- $**65** Surcharge.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/tnguyen/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/876,113	09/04/2010	2841	2580	6005.042	93	5

CONFIRMATION NO. 1607

64180
URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

FILING RECEIPT

OC000000043564801

Date Mailed: 09/21/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Ricardo H. BRUCE, Union City, CA;
Marlon B. VERDAN, Paranaque City, PHILIPPINES;
Margaret Anne N. SOMERA, Caloocan City, PHILIPPINES;
Rowenah Michelle D. JAGO-ON, Pasig City, PHILIPPINES;
Maria Eliza B. DE BELEN, Quezon City, PHILIPPINES;
Ron Kelvin B. PALACOL, Laguna, PHILIPPINES;

Assignment For Published Patent Application

BITMICRO NETWORKS, INC., Fremont, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/239,794 09/04/2009

Foreign Applications

If Required, Foreign Filing License Granted: 09/16/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/876,113**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No
** **SMALL ENTITY** **

Title

MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES

Preliminary Class

361

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

UNITED STATES PATENT AND TRADEMARK OFFICE
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URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

Courtesy Reminder for
Application Serial No: 12/876,113

Attorney Docket No: 6005.042
Customer Number: 64180
Date of Electronic Notification: 09/21/2010

This is a courtesy reminder that new correspondence is available for this application. The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

An email notification regarding the correspondence was sent to the following email address(es) associated with your customer number:

mail@URIARTELAW.COM
stephen@uriartelaw.com
labid@uriartelaw.com

Please verify that these email addresses are correct.

To view your correspondence online or update your email addresses, please visit us anytime at **https://sportal.uspto.gov/secure/myportal/privatepair.** If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov or call 1-866-217-9197.

PTO/SB/80 (11-08)
Approved for use through 11/30/2011. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

☑ Practitioners associated with the Customer Number: 64180

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

☑ The address associated with Customer Number: 64180

OR

☐ Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

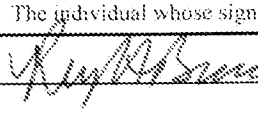
Assignee Name and Address:

BiTMICRO Networks, Inc.
47929 Fremont Blvd.
Fremont, CA 94538

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	April 15, 2009
Name	Rey H. Bruce	Telephone	510.743.3101
Title	President & CEO		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal

Application Number:	12876113
Filing Date:	04-Sep-2010
Title of Invention:	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES
First Named Inventor/Applicant Name:	Ricardo H. BRUCE
Filer:	Stephen Radcliff Uriarte
Attorney Docket Number:	6005.042

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Late filing fee for oath or declaration	2051	1	65	65
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**65**

Electronic Acknowledgement Receipt

EFS ID:	8883519
Application Number:	12876113
International Application Number:	
Confirmation Number:	1607
Title of Invention:	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES
First Named Inventor/Applicant Name:	Ricardo H. BRUCE
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.042
Receipt Date:	22-NOV-2010
Filing Date:	04-SEP-2010
Time Stamp:	04:21:35
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$65
RAM confirmation Number	7884
Deposit Account	504068
Authorized User	URIARTE,STEPHEN R.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	6005_042_Rsp2MP_20101121B.pdf	82701 23a966c8d8a5e93895fc8d42cec1c0f948783557	no	2
Warnings:					
Information:					
2	Oath or Declaration filed	6005_042_Decl_Allsigned_20101122.pdf	824216 e3f3ed55466a2bb12a833dc3216b7b9093f15725	no	5
Warnings:					
Information:					
3	Assignee showing of ownership per 37 CFR 3.73(b).	6005_042_3_73bSttmnt_ALL_20101122B.pdf	907633 73cfb7c7789da1c5359a1ea0864c018401b79aef	no	6
Warnings:					
Information:					
4	Power of Attorney	6005_GenPwr_64180_20090415B.pdf	525719 18653bd81875bad8136243791bb50eda725d039f	no	1
Warnings:					
Information:					
5	Fee Worksheet (PTO-875)	fee-info.pdf	30105 bfd21576533df982c788923e9d615fd9f048f35f	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2370374		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Ricardo H. BRUCE et al.	)	Group Art Unit: 2841
Serial No.: 12/876,113	)	Examiner: Not Yet Assigned
Application Filing Date: 04 Sep 2010	)	
For: MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE TO FILE MISSING PARTS

NON-PROVISIONAL APPLICATION

Dear Sir/Madam:

In Response to the Notice to File Missing Parts of Non-Provisional Application, dated 21 Sep 2010, please accept the following.

A. Enclosures

Sub-mitted?	Enclosure Description	Sheets Submitted
YES	Oath/Declaration of Inventorship under 37 CFR 152 or 1.53	5
YES	37 CFR 3.73(b) Statement with copies of assignment papers	6
YES	General Power of Attorney	1
NO	Request to Correct Official Filing Receipt, including Notice of Missing Parts *Annotated with Corrections*	n/a
NO	Copy of Notice of Missing Parts – *Original* (Required Only if Not Using EFS-Web for Reply)	n/a

B. Extensions of Time

The requested extension and fee are as follows, indicated below:

____ One month (37 CFR 1.17(a)(1)) Fee (small entity: $65.00) 0.00

____ Two months (37 CFR 1.17(a)(2)) Fee (small entity: $245.00) 0.00

____ Three months (37 CFR 1.17(a)(3)) Fee (small entity: $555.00) 0.00

C. Payment Submitted Via EFS-Web

_X_ Payment of the surcharge as set forth in 37 CFR 1.16(f) of **$65.00** (small entity) is made by credit card through EFS-web.

____ Payment of the Extension of Time noted above as set forth in 37 CFR 1.17(a) is made by credit card through EFS-web.

D. Constructive Petition for An Extension of Time - All Replies and Authorization to Charge/Credit Fees to Deposit Account

_X_ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number: **50-4068**.

_X_ Please treat this authorization to charge all required fees under 37 CFR 1.17 as a constructive petition for an extension of time in accordance with 37 CFR 1.136(a)(3).

Sincerely,

Signature: /Stephen R. Uriarte/
Name: Stephen R. Uriarte, Reg. No. 40,854
Date: 22 November 2010

Uriarte Law
2021 The Alameda, Suite 225
San Jose, CA 95126
Tel: 408.244.2164 ext. 111
Fax: 408.716.2651
Email: mail@uriartelaw.com

PTO/SB/01A (01-09)
Approved for use through 09/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES

As the below named inventor(s), I/we declare that:

This declaration is directed to:

☐ The attached application, or

☑ Application No 12/876,113 filed on 04 September 2010

☐ As amended on _____ (if applicable).

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought;

I/we have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;

I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

All statements made herein of my/our own knowledge are true, all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and may jeopardize the validity of the application or any patent issuing thereon.

FULL NAME OF INVENTOR(S)

Inventor one: Ricardo H. BRUCE Date: 22 NOV 2010

Signature: Ricardo H. Bruce Citizen of: U.S.

Inventor two: Marlon B. VERDAN Date: 22 NOV 2010

Signature: Marlon Verdan Citizen of: Philippines

☑ Additional inventors or a legal representative are being named on TWO additional form(s) attached hereto.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/02A (07-07)
Approved for use through 09/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

DECLARATION

ADDITIONAL INVENTOR(S)
Supplemental Sheet

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle (if any))	Family Name or Surname
Margaret Anne N.	SOMERA

Inventor's Signature: MARGARET ANNE N. SOMERA — Date: 13 Oct 2010

Caloocan City, Metro Manila Residence: City	State	PH (Philippines) Country	PH (Philippines) Citizenship

124 Madocay Street
Mailing Address

Caloocan City, Metro Manila City	State	1400 Zip	PH (Philippines) Country

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle (if any))	Family Name or Surname
Rowenah Michelle G.	JAGO-ON

Inventor's Signature — Date

Pasig City Residence: City	State	PH (Philippines) Country	PH (Philippines) Citizenship

Unit 302, Missouri Riverfront Residences
Dr. Sixto Antonio Ave, Caniogan
Mailing Address

Pasig City City	State	1606 Zip	PH (Philippines) Country

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle (if any))	Family Name or Surname
Maria Eliza B.	DE BELEN

Inventor's Signature — Date

Quezon City Residence: City	State	PH (Philippines) Country	PH (Philippines) Citizenship

20-A Latukan St. Manresa
Mailing Address

Quezon City City	State	1115 Zip	PH (Philippines) Country

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PTO/SB/02A (07-07)
Approved for use through 06/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

DECLARATION

ADDITIONAL INVENTOR(S)
Supplemental Sheet

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle (if any))	Family Name or Surname
Margaret Anne N.	SOMERA

Inventor's Signature _____ Date _____

Caloocan City, Metro Manila		PH (Philippines)	PH (Philippines)
Residence: City	State	Country	Citizenship

124 Madocay Street

Mailing Address

Caloocan City, Metro Manila		1400	PH (Philippines)
City	State	Zip	Country

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle (if any))	Family Name or Surname
Rowenah Michelle D.	JAGO-ON

Inventor's Signature Rowenah Michelle Jago-on Date 31 August 2010

Pasig City		PH (Philippines)	PH (Philippines)
Residence: City	State	Country	Citizenship

Unit 302, Missouri Riverfront Residences
Dr. Sixto Antonio Ave, Caniogan

Mailing Address

Pasig City		1608	PH (Philippines)
City	State	Zip	Country

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle (if any))	Family Name or Surname
Maria Eliza B.	DE BELEN

Inventor's Signature MARIA ELIZA B. DE BELEN Date 31 August 2010

Quezon City		PH (Philippines)	PH (Philippines)
Residence: City	State	Country	Citizenship

30-A Latukan St., Manresa

Mailing Address

Quezon City		1115	PH (Philippines)
City	State	Zip	Country

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If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

DECLARATION

ADDITIONAL INVENTOR(S)
Supplemental Sheet

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle (if any))	Family Name or Surname		
Ron Kelvin B. RON KELVIN PALACOL	PALACOL		
Inventor's Signature			31 AUGUST 2018 Date
Laguna Residence: City	State	PH (Philippines) Country	PH (Philippines) Citizenship
10 Duhat St., Phase 2 Pacita Complex II San Pedro Mailing Address			
Laguna City	State	4023 Zip	PH (Philippines) Country
Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle (if any))	Family Name or Surname		
Inventor's Signature			Date
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country
Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle (if any))	Family Name or Surname		
Inventor's Signature			Date
Residence: City	State	Country	Citizenship
Mailing Address			
Quezon City City	State	Zip	Country

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/96 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: R. BRUCE, M. VERDAN, R.M. JAGO-ON, M.E. DE BELEN, R.K. PALACOL, and M. SOMERA

Application No./Patent No.: 12/876,113 Filed/Issue Date: 4 September 2010

Titled: MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES

BITMICRO NETWORKS, INC., a A Corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. [X] the assignee of the entire right, title, and interest in;

2. [ ] an assignee of less than the entire right, title, and interest in (The extent (by percentage) of its ownership interest is _____ %); or

3. [ ] the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made) the patent application/patent identified above, by virtue of either:

A. [X] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy therefore is attached.

OR

B. [ ] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet(s).

[X] As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Ray H. Bruce — 11/22/2010
Signature — Date

Ray H. Bruce — Chairman & CEO
Printed or Typed Name — Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ASSIGNMENT

For good and valuable consideration, the receipt of which is hereby acknowledged, the person(s) named below (referred to as "INVENTOR" whether singular or plural) has sold, assigned, and transferred and does hereby sell, assign, and transfer to **BiTMICRO Networks, Inc., a California corporation, having a place of business at 47929 Fremont Blvd., Fremont, CA 94538** ("ASSIGNEE"), for itself and its successors, transferees, and assignees, the following:

1. The entire worldwide right, title, and interest in all inventions and improvements ("SUBJECT MATTER") that are disclosed in the application for United States Letters Patent entitled: **MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES** ("APPLICATION"), which:

☒ is to be filed herewith;

☐ was filed on _____, now bearing U.S. serial number _____ and for which a Declaration was executed by INVENTOR on the date(s) below; and

2. The entire worldwide right, title, and interest in and to: (a) the APPLICATION, including any right of priority; (b) any divisional, continuation, substitute, renewal, reissue, and other related applications thereto which have been or may be filed in the United States or elsewhere in the world; and (c) any patents which may be granted on the applications set forth in (a) and (b) above.

INVENTOR agrees that ASSIGNEE may apply for and receive patents for SUBJECT MATTER in ASSIGNEE's own name.

INVENTOR agrees to do the following, when requested, and without further consideration, in order to carry out the intent of this Assignment: (1) execute all oaths, assignments, powers of attorney, applications, and other papers necessary or desirable to fully secure to ASSIGNEE the rights, titles and interests herein conveyed; (2) communicate to ASSIGNEE all known facts relating to the SUBJECT MATTER; and (3) generally do all lawful acts that ASSIGNEE shall consider desirable for securing, maintaining, and enforcing worldwide patent protection relating to the SUBJECT MATTER and for vesting in ASSIGNEE the rights, titles, and interests herein conveyed. INVENTOR further agrees to provide any successor, assign, or legal representative of ASSIGNEE with the benefits and assistance provided to ASSIGNEE hereunder.

INVENTOR represents that INVENTOR has the rights, titles, and interests to convey as set forth herein, and covenants with ASSIGNEE that the INVENTOR has made or will make hereafter no assignment, grant, mortgage, license, or other agreement affecting the rights, titles, and interests herein conveyed.

INVENTOR grants the attorney of record the power to insert on this Assignment any further identification which may be necessary or desirable in order to comply with the rules of the United States Patent and Trademark Office for recordation of this document.

Title of Document:	ASSIGNMENT
In Re Application of:	Ricardo H. Bruce et al.
Title:	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES
Filed: (if applicable)	N/A
Serial No.: (if applicable)	N/A

This Assignment may be executed in one or more counterparts, each of which shall be deemed an original and all of which may be taken together as one and the same Assignment.

First Inventor Signature — **Date of Signature** — **Date Inventor Declaration Signed by Inventor**

Name: Ricardo H. Bruce — August 31, 2010 — August 31, 2010

Second Inventor Signature — **Date of Signature** — **Date Inventor Declaration Signed by Inventor**

Name: Marlon B. Verdan — August 31, 2010 — August 31, 2010

Third Inventor Signature — **Date of Signature** — **Date Inventor Declaration Signed by Inventor**

Name: Margaret Anne N. Somera — _____, 2010 — _____, 2010

Fourth Inventor Signature — **Date of Signature** — **Date Inventor Declaration Signed by Inventor**

Name: Rowenaly Michelle D. Jago-on — August 31, 2010 — August 31, 2010

Fifth Inventor Signature — **Date of Signature** — **Date Inventor Declaration Signed by Inventor**

Name: Maria Eliza B. De Belen — August 31, 2010 — August 31, 2010

Sixth Inventor Signature — **Date of Signature** — **Date Inventor Declaration Signed by Inventor**

Name: Ron Kelvin B. Palacol — August 31, 2010 — August 31, 2010

ASSIGNMENT

For good and valuable consideration, the receipt of which is hereby acknowledged, the person(s) named below (referred to as "INVENTOR" whether singular or plural) has sold, assigned, and transferred and does hereby sell, assign, and transfer to **BiTMICRO Networks, Inc., a California corporation, having a place of business at 47929 Fremont Blvd., Fremont, CA 94538** ("ASSIGNEE"), for itself and its successors, transferees, and assignees, the following:

1. The entire worldwide right, title, and interest in all inventions and improvements ("SUBJECT MATTER") that are disclosed in the application for United States Letters Patent entitled: **MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES** ("APPLICATION"), which:

☐ is to be filed herewith;

☒ was filed on **04 September 2010**, now bearing U.S. serial number **12/876,113**; and

2. The entire worldwide right, title, and interest in and to: (a) the APPLICATION, including any right of priority; (b) any divisional, continuation, substitute, renewal, reissue, and other related applications thereto which have been or may be filed in the United States or elsewhere in the world; and (c) any patents which may be granted on the applications set forth in (a) and (b) above.

INVENTOR agrees that ASSIGNEE may apply for and receive patents for SUBJECT MATTER in ASSIGNEE's own name.

INVENTOR agrees to do the following, when requested, and without further consideration, in order to carry out the intent of this Assignment: (1) execute all oaths, assignments, powers of attorney, applications, and other papers necessary or desirable to fully secure to ASSIGNEE the rights, titles and interests herein conveyed; (2) communicate to ASSIGNEE all known facts relating to the SUBJECT MATTER; and (3) generally do all lawful acts that ASSIGNEE shall consider desirable for securing, maintaining, and enforcing worldwide patent protection relating to the SUBJECT MATTER and for vesting in ASSIGNEE the rights, titles, and interests herein conveyed. INVENTOR further agrees to provide any successor, assign, or legal representative of ASSIGNEE with the benefits and assistance provided to ASSIGNEE hereunder.

INVENTOR represents that INVENTOR has the rights, titles, and interests to convey as set forth herein, and covenants with ASSIGNEE that the INVENTOR has made or will make hereafter no assignment, grant, mortgage, license, or other agreement affecting the rights, titles, and interests herein conveyed.

INVENTOR grants the attorney of record the power to insert on this Assignment any further identification which may be necessary or desirable in order to comply with the rules of the United States Patent and Trademark Office for recordation of this document.

Title of Document:	**ASSIGNMENT**
In Re Application of:	Ricardo H. Bruce et al.
Title:	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES
Filed: (if applicable)	N/A
Serial No.: (if applicable)	N/A

This Assignment may be executed in one or more counterparts, each of which shall be deemed an original and all of which may be taken together as one and the same Assignment.

First Inventor Signature	**Date of Signature**	**Date Inventor Declaration Signed by Inventor**
Name: Ricardo H. Bruce	_____, 2010	_____, 2010
Second Inventor Signature	**Date of Signature**	**Date Inventor Declaration Signed by Inventor**
Name: Marlon B. Verdan	_____, 2010	_____, 2010
Third Inventor Signature	**Date of Signature**	**Date Inventor Declaration Signed by Inventor**
Name: Margaret Anne N. Somera	18 Oct, 2010	18 Oct, 2010
Fourth Inventor Signature	**Date of Signature**	**Date Inventor Declaration Signed by Inventor**
Name: Rowenah Michelle D. Jago-on	_____, 2010	_____, 2010
Fifth Inventor Signature	**Date of Signature**	**Date Inventor Declaration Signed by Inventor**
Name: Maria Eliza B. De Belen	_____, 2010	_____, 2010
Sixth Inventor Signature	**Date of Signature**	**Date Inventor Declaration Signed by Inventor**
Name: Ron Kelvin B. Palacol	_____, 2010	_____, 2010

Form **PTO-1595** (Rev. 03-09)
OMB No. 0651-0027 (exp. 03/31/2009)

U.S. DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

RECORDATION FORM COVER SHEET
PATENTS ONLY

To the Director of the U.S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

1. Name of conveying party(ies)

Margaret Anne N. SOMERA

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies)

Name: BiTMICRO Networks, Inc.

Internal Address:

Street Address: 47929 Fremont Blvd

City: Fremont

State: CA

Country: US Zip: 94538

Additional name(s) & address(es) attached? ☐ Yes ☒ No

3. Nature of conveyance/Execution Date(s):

Execution Date(s) 13 Oct 2010

☒ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☐ Joint Research Agreement
☐ Government Interest Assignment
☐ Executive Order 9424, Confirmatory License
☐ Other

4. Application or patent number(s): ☐ This document is being filed together with a new application.

A. Patent Application No.(s)

12/876,113

B. Patent No.(s)

Additional numbers attached? ☐ Yes ☐ No

5. Name and address to whom correspondence concerning document should be mailed:

Name: The Uriarte Law Firm

Internal Address:

Street Address: 2021 The Alameda, Suite 225

City: San Jose

State: CA Zip: 95126

Phone Number: 408.244.2164 x111

Fax Number: 408.716.2651

Email Address: mail@uriartelaw.com

6. Total number of applications and patents involved: ONE (1)

7. Total fee (37 CFR 1.21(h) & 3.41) $40.00

☒ Authorized to be charged to deposit account
☒ Enclosed
☐ None required (government interest not affecting title)

8. Payment Information

Deposit Account Number 504068

Authorized User Name Uriarte Law

9. Signature:

/Stephen R. Uriarte/
Signature

22 Nov 2010
Date

Stephen R. Uriarte Reg. No. 40,854
Name of Person Signing

Total number of pages including cover sheet, attachments, and documents: 5

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:
Mail Stop Assignment Recordation Services, Director of the USPTO, P.O.Box 1450, Alexandria, V.A. 22313-1450

Guidelines for Completing Patents Cover Sheets (PTO-1595)

Cover Sheet information must be submitted with each document to be recorded. If the document to be recorded concerns both patents and trademarks separate patent and trademark cover sheets, including any attached pages for continuing information, must accompany the document. All pages of the cover sheet should be numbered consecutively, for example, if both a patent and trademark cover sheet is used, and information is continued on one additional page for both patents and trademarks, the pages of the cover sheet would be numbered from 1 to 4.

Item 1. Name of Conveying Party(ies).

Enter the full name of the party(ies) conveying the interest. If there is insufficient space, enter a check mark in the "Yes" box to indicate that additional information is attached. The name of the additional conveying party(ies) should be placed on an attached page clearly identified as a continuation of the information Item 1. Enter a check mark in the "No" box, if no information is contained on an attached page. If the document to be recorded is a joint research agreement, enter the name(s) of the party(ies) other than the owner of the patent or patent application as the conveying party(ies).

Item 2. Name and Address of Receiving Party(ies).

Enter the name and full address of the first party receiving the interest. If there is more than one party receiving the interest, enter a check mark in the "Yes" box to indicate that additional information is attached. Enter a check mark in the "No" box, if no information is contained on an attached page. If the document to be recorded is a joint research agreement, enter the name(s) of the patent or patent application owner(s) as the receiving party.

Item 3. Nature of Conveyance/Execution Date(s).

Enter the execution date(s) of the document. It is preferable to use the name of the month, or an abbreviation of that name, in order that confusion over dates is minimized. Place a check mark in the appropriate box describing the nature of the conveying document. If the "Other" box is checked, specify the nature of the conveyance.

Item 4. Application Number(s) or Patent Number(s).

Indicate the application number(s), and/or patent number(s) against which the document is to be recorded. National application numbers must include both the series code and a six-digit number (e.g., 07/123,456), and international application numbers must be complete (e.g., PCT/US91/12345).

Enter a check mark in the appropriate box: "Yes" or "No " if additional numbers appear on attached pages. Be sure to identify numbers included on attached pages as the continuation of Item 4. Also enter a check mark if this Assignment is being filed with a new application.

Item 5. Name and Address of Party to whom correspondence concerning the document should be mailed. Enter the name and full address of the party to whom correspondence is to be mailed.

Item 6. Total Applications and Patents involved.

Enter the total number of applications and patents identified for recordation. Be sure to include all applications and patents identified on the cover sheet and on additional pages.

Block 7. Total Fee Enclosed.

Enter the total fee enclosed or authorized to be charged. A fee is required for each application and patent against which the document is recorded.

Item 8. Payment Information.

Enter the deposit account number and authorized user name to authorize charges.

Item 9. Signature.

Enter the name of the person submitting the document. The submitter must sign and date the cover sheet. Enter the total number of pages including the cover sheet, attachments, and document.

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with the above request for information. This collection of information is authorized by 35 U.S.C. 1, 2, 261 and E.O. 9424. This information will primarily be used by the USPTO for the recordation of assignments related to patents and patent applications. Submission of this information is voluntary but is required in order for the USPTO to record the requested assignment. If you do not provide the information required on the cover sheet, the assignment will not be recorded, and all documents will be returned to you.

After the information is recorded, the records and associated documents can be inspected by the public and are not confidential, except for documents that are sealed under secrecy orders or related to unpublished patent applications. Assignment records relating to unpublished patent applications are maintained in confidence in accordance with 35 U.S.C. 122. Records open to the public are searched by users for the purpose of determining ownership for other property rights with respect to patents and trademarks.

Routine uses of the information you provide may also include disclosure to appropriate Federal, state, local, or foreign agencies in support of their enforcement duties and statutory or regulatory missions, including investigating potential violations of law or contract and awarding contracts or other benefits; to a court, magistrate, or administrative tribunal in the course of presenting evidence; to members of Congress responding to requests for assistance from their constituents; to the Office of Management and Budget in connection with the review of private relief legislation; to the Department of Justice in connection with a Freedom of Information Act request; to a contractor in the performance of their duties; to the Office of Personnel Management for personnel studies; and to the General Services Administration (GSA) as part of their records management responsibilities under the authority of 44 U.S.C. 2904 and 2906. Such disclosure to GSA shall not be used to make determinations about individuals.

ASSIGNMENT

For good and valuable consideration, the receipt of which is hereby acknowledged, the person(s) named below (referred to as "INVENTOR" whether singular or plural) has sold, assigned, and transferred and does hereby sell, assign, and transfer to **BiTMICRO Networks, Inc., a California corporation, having a place of business at 47929 Fremont Blvd., Fremont, CA 94538** ("ASSIGNEE"), for itself and its successors, transferees, and assignees, the following:

1. The entire worldwide right, title, and interest in all inventions and improvements ("SUBJECT MATTER") that are disclosed in the application for United States Letters Patent entitled: **MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES** ("APPLICATION"), which:

☐ is to be filed herewith;

☒ was filed on **04 September 2010**, now bearing U.S. serial number **12/876,113**; and

2. The entire worldwide right, title, and interest in and to: (a) the APPLICATION, including any right of priority; (b) any divisional, continuation, substitute, renewal, reissue, and other related applications thereto which have been or may be filed in the United States or elsewhere in the world; and (c) any patents which may be granted on the applications set forth in (a) and (b) above.

INVENTOR agrees that ASSIGNEE may apply for and receive patents for SUBJECT MATTER in ASSIGNEE's own name.

INVENTOR agrees to do the following, when requested, and without further consideration, in order to carry out the intent of this Assignment: (1) execute all oaths, assignments, powers of attorney, applications, and other papers necessary or desirable to fully secure to ASSIGNEE the rights, titles and interests herein conveyed; (2) communicate to ASSIGNEE all known facts relating to the SUBJECT MATTER; and (3) generally do all lawful acts that ASSIGNEE shall consider desirable for securing, maintaining, and enforcing worldwide patent protection relating to the SUBJECT MATTER and for vesting in ASSIGNEE the rights, titles, and interests herein conveyed. INVENTOR further agrees to provide any successor, assign, or legal representative of ASSIGNEE with the benefits and assistance provided to ASSIGNEE hereunder.

INVENTOR represents that INVENTOR has the rights, titles, and interests to convey as set forth herein, and covenants with ASSIGNEE that the INVENTOR has made or will make hereafter no assignment, grant, mortgage, license, or other agreement affecting the rights, titles, and interests herein conveyed.

INVENTOR grants the attorney of record the power to insert on this Assignment any further identification which may be necessary or desirable in order to comply with the rules of the United States Patent and Trademark Office for recordation of this document.

Title of Document:	**ASSIGNMENT**
In Re Application of:	Ricardo H. Bruce et al.
Title:	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES
Filed: (if applicable)	N/A
Serial No.: (if applicable)	N/A

This Assignment may be executed in one or more counterparts, each of which shall be deemed an original and all of which may be taken together as one and the same Assignment.

First Inventor Signature	**Date of Signature**	**Date Inventor Declaration Signed by Inventor**
Name: Ricardo H. Bruce	_____, 2010	_____, 2010
Second Inventor Signature	**Date of Signature**	**Date Inventor Declaration Signed by Inventor**
Name: Marlon B. Verdan	_____, 2010	_____, 2010
Third Inventor Signature	**Date of Signature**	**Date Inventor Declaration Signed by Inventor**
Name: Margaret Anne N. Somera	13 Oct, 2010	13 Oct, 2010
Fourth Inventor Signature	**Date of Signature**	**Date Inventor Declaration Signed by Inventor**
Name: Rowenah Michelle D. Jago-on	_____, 2010	_____, 2010
Fifth Inventor Signature	**Date of Signature**	**Date Inventor Declaration Signed by Inventor**
Name: Maria Eliza B. De Belen	_____, 2010	_____, 2010
Sixth Inventor Signature	**Date of Signature**	**Date Inventor Declaration Signed by Inventor**
Name: Ron Kelvin B. Palacol	_____, 2010	_____, 2010

Electronic Acknowledgement Receipt

EFS ID:	8883529
Application Number:	12876113
International Application Number:	
Confirmation Number:	1607
Title of Invention:	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES
First Named Inventor/Applicant Name:	Ricardo H. BRUCE
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.042
Receipt Date:	22-NOV-2010
Filing Date:	04-SEP-2010
Time Stamp:	05:04:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Assignee showing of ownership per 37 CFR 3.73(b).	6005_042_Record_ALL_SOMERA_20101122.pdf	194522 c229b6fc77078c661e734a901efcbf544800 99cd	no	5

Warnings:	
Information:	

Total Files Size (in bytes):	194522

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 11/29/2010

KWHITE1 SALE #00000029 Mailroom Dt: 11/29/2010 504068 12876113
01 FC : 8021 40.00 DA

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 12/876,113

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	82		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	270		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	110		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	93 minus 20 =	* 73	x 26 =	1898	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	5 minus 3 =	* 2	x 110 =	220			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $270 ($135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	2580		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/876,113	09/04/2010	2841	2645	6005.042	93	5

CONFIRMATION NO. 1607

UPDATED FILING RECEIPT

64180
URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

OC000000045803386

Date Mailed: 02/03/2011

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Ricardo H. BRUCE, Union City, CA;
Marlon B. VERDAN, Paranaque City, PHILIPPINES;
Margaret Anne N. SOMERA, Caloocan City, PHILIPPINES;
Rowenah Michelle D. JAGO-ON, Pasig City, PHILIPPINES;
Maria Eliza B. DE BELEN, Quezon City, PHILIPPINES;
Ron Kelvin B. PALACOL, Laguna, PHILIPPINES;

Assignment For Published Patent Application

BITMICRO NETWORKS, INC., Fremont, CA

Power of Attorney: The patent practitioners associated with Customer Number 64180

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/239,794 09/04/2009

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)

If Required, Foreign Filing License Granted: 09/16/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/876,113**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No
** **SMALL ENTITY** **

Title

MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES

Preliminary Class

361

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

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NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/876,113	09/04/2010	Ricardo H. BRUCE	6005.042

CONFIRMATION NO. 1607

POA ACCEPTANCE LETTER

64180
URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

OC000000045803225

Date Mailed: 02/03/2011

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/22/2010.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/tchaka/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/876,113	09/04/2010	Ricardo H. BRUCE	6005.042	1607

64180 7590 12/21/2012

URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

EXAMINER	
RUTZ, JARED IAN	
ART UNIT	PAPER NUMBER
2187	

NOTIFICATION DATE	DELIVERY MODE
12/21/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mail@URIARTELAW.COM
stephen@uriartelaw.com
labid@uriartelaw.com

Office Action Summary	Application No.	Applicant(s)	
	12/876,113	BRUCE ET AL.	
	Examiner	Art Unit	
	JARED RUTZ	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-93* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-93* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *04 September 2010* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-93, as originally filed on 9/4/2010, are pending in the instant application. Of these, there are 5 independent and 88 dependent claims.

Double Patenting

2. Applicant is advised that should claim 31 be found allowable, claim 32 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Objections

3. **Claim 68** is objected to because of the following informalities:

   a. **Claim 68** recites “The memory controller of claim59", the Examiner respectfully submits that there should be a space between claim and 59.

4. Appropriate correction is required.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. **Claims 29-44** are rejected under 35 U.S.C. 101 because they are directed to non-statutory subject matter.

7. As per **claims 29-44**, they are rejected because the applicant has provided evidence that the applicant intends the term "computer-readable storage medium" to include non-statutory matter. The applicant describes a computer-readable storage medium as including open ended language and thus it is reasonable to interpret it to include all possible mediums, including non-statutory mediums (see paragraph 0045). The words "storage" and/or "recording" are insufficient to convey only statutory embodiments to one of ordinary skill in the art absent an explicit and deliberate limiting definition or clear differentiation between storage media and transitory media in the disclosure. As such, the claim(s) is/are drawn to a form of energy. Energy is not one of the four categories of invention and therefore this/these claim(s) is/are not statutory. Energy is not a series of steps or acts and thus is not a process. Energy is not a physical article or object and as such is not a machine or manufacture. Energy is not a combination of substances and therefore not a composition of matter.

8. The Examiner suggests amending the claim(s) to read as a “non-transitory machine-readable storage medium”.

Claim Rejections - 35 USC § 112

9. The following is a quotation of 35 U.S.C. 112(a):
(a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), first paragraph:
The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. **Claims 45-58** are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 45 recites “a means for addressing”, and recites further details of said means. Claim 45 is a single means claim. As per MPEP 2164.08(a), a means recitation which does not appear in combination with another recited element of means is subject to an undue breadth rejection under 35 USC 112 first paragraph. A single means claim which covers every conceivable means for achieving the stated purpose is non-enabling for the scope of the claim because the specification discloses at most only those means known to the inventor. See *In re Hyatt*, 708 F.2d 712, 714-715, 218 USPQ 195, 197 (Fed. Cir. 1983). Claims 46-58 do not recite additional elements, and accordingly are rejected for the same reasons as claim 45.

11. The following is a quotation of 35 U.S.C. 112(b):

(B) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. **Claims 23, 31, 32, 35, 50, 61-64, 68, and 83** are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

13. **Claim 23** recites “and second device profile” in lines 12-13. The Examiner respectfully notes that this limitation has no apparent relationship to the rest of the claim, and its meaning in the claim is unclear.

14. **Claims 31 and 32** each recite the limitation "*said at least one attribute*" in line 1. There is insufficient antecedent basis for this limitation in the claim.

15. **Claim 35** recites the limitation "*said means for addressing*" in line 1. There is insufficient antecedent basis for this limitation in the claim.

16. **Claim 50** recites the limitation “*wherein said means for addressing further includes addressing said second memory location*”. It is unclear how a means for addressing, which is a structure, can include addressing, which is an action.

17. **Claim 61** recites the limitation "*said data path*" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

18. **Claims 62 and 63** depend from claim 61, and are rejected for the same reasons as claim 61.

19. **Claim 62** recites the limitation "*said memory transaction request*" in line 2. There is insufficient antecedent basis for this limitation in the claim.

20. **Claim 63** depends from claim 62, and is rejected for the same reason as claim 62.

21. **Claim 64** recites the limitation "*said buffer is a FIFO*" in line 1. There is insufficient antecedent basis for this limitation in the claim.

22. **Claim 64** recites the limitation "*said data path*" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

23. **Claim 68** recites the limitation "*said main control device*" in line 2. There is insufficient antecedent basis for this limitation in the claim.

24. **Claim 83** recites the limitation "*said memory transaction request*" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

25. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

26. **Claims 1-14, 20, 21, 25, 45-60, and 69-92** are rejected under 35 U.S.C. 102(e) as being anticipated by Falik et al. (US 8,200,879).

Claim 1 is taught by Falik as:

A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising: addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 2 is taught by Falik as:

The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 3 is taught by Falik as:

The method of claim 1, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

And said addressing said first memory location is made in response to a first memory transaction request. Column 18 lines 24-34 shows that applications on the main die 100 issue read and program commands.

And further including addressing said second memory location. Figure 6 shows that both sections can be addressed.

Claim 4 is taught by Falik as:

The method of claim 1, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 5 is taught by Falik as:

The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 6 is taught by Falik as:

The method of claim 5, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 7 is taught by Falik as:

The method of claim 5, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 8 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a memory device type attribute. Column 20 lines 30-36 shows that the registers can indicate if the device is self timed type flash memory or not.

Claim 9 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 10 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line

61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 11 is taught by Falik as:

The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 12 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 13 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of attributes that differs in value from a second page size attribute from

said second set of attributes. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 14 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 20 is taught by Falik as:

The method of claim 2, further including: using an address corresponding to a memory location from said first memory device and transferring a first data set. Column 16 lines 53-62 shows that an address and data are sent for a programming operation.

And using an address corresponding to a memory location from said second memory device and transferring a second data set. Column 14 lines 51-65 show that the standard address space is mapped to the logical sections into

which the arrays are grouped, showing that the second memory device is accessed using an address corresponding to the second memory device.

Claim 21 is taught by Falik as:

The method of claim 20, wherein: said first set of attributes includes a first page size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

And said first data set includes a first data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

And if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size. Column 27 lines 9-24 shows that when the number of bytes to be transferred to the FD have been transferred, the transfer process ends by setting the bus to a HiZ state.

Claim 25 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size

attribute of said first memory device. As discussed at column 27 lines 33-60, the program buffer corresponds to the batch size, which is the amount of data which can be programmed into the flash array at once.

Claim 45 is taught by Falik as:

A memory controller for performing memory transactions, said memory controller comprising: a means for addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14

lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And said means for addressing uses attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 46 is taught by Falik as:

The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 47 is taught by Falik as:

The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 48 is taught by Falik as:

The memory controller of claim 46, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said use of said attributes from said first and second device profiles by said means for addressing includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 49 is taught by Falik as:

The memory controller of claim 46, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 50 is taught by Falik as:

The memory controller of claim 45, wherein said means for addressing further includes addressing said second memory location. Figure 6 shows that both sections can be addressed.

Claim 51 is taught by Falik as:

The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 52 is taught by Falik as:

The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 53 is taught by Falik as:

The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 54 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 55 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 56 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 57 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 58 is taught by Falik as:

The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

Claim 59 is taught by Falik as:

A memory controller comprising: an interface controller coupled to a memory device interface and an IO device interface. Figure 4B shows interface controller 110 connected to bus 90 and internal bus 140.

Said interface controller disposed to perform a memory transaction by addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities

registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And said addressing of said first memory location includes using said attributes from said first device profile. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 60 is taught by Falik as:

The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile. Figure 6 shows that both sections can be addressed.

Claim 69 is taught by Falik as:

The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

Claim 70 is taught by Falik as:

The memory controller of claim 59, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 71 is taught by Falik as:

The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 72 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 73 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 74 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column

20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 75 is taught by Falik as:

The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 76 is taught by Falik as:

The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 77 is taught by Falik as:

The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20

line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 78 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 79 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 80 is taught by Falik as:

An electronic storage device, comprising: a memory controller disposed to address a first memory location and a second memory location which are

respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And said memory controller using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 81 is taught by Falik as:

The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command. Column 9 lines 5-18 shows that the interface performs appropriate requests for erasure.

Claim 82 is taught by Falik as:

The electronic storage device of claim 80, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 83 is taught by Falik as:

The electronic storage device of claim 80, said memory controller further disposed to: perform a write operation on said first memory device, if said memory transaction request is associated with a write request. Column 16 lines 53-64 shows that write transactions may be performed.

Perform a read operation on said first memory device, if said memory transaction request is associated with a read request. Column 16 lines 53-64 shows that read transactions may be performed.

And wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using said second device profile in response to receiving a second memory transaction request. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used for accesses to the groups of memory arrays.

Claim 84 is taught by Falik as:

The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 85 is taught by Falik as:

The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 86 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20

line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 87 is taught by Falik as:

The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 88 is taught by Falik as:

The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 89 is taught by Falik as:

The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

Claim 90 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 91 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 92 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim Rejections - 35 USC § 103

27. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

28. **Claims 15, 18, and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Nangle (US 7,330,954).

Claim 15 is taught by Falik as:

The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device. Column 21 lines 7-10 shows that the information can correspond to a flash device FD.

Although Falik column 21 lines 7-10 shows that other memory technologies such as SRAM may be used, it does not expressly teach that the second memory device attribute corresponds to a DRAM device interface.

With respect to claim 15, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 lines 51-67 shows that the memory devices may be flash memory and DRAM.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include flash memory and DRAM in the system of Falik.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 15**.

Claim 18 is taught by Falik as shown supra with respect to claim 8.

Falik does not expressly teach that said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

With respect to claim 18, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 line 51 through column 5 line 4 shows that the memory devices may be volatile memory that have a battery backup.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a volatile memory disposed to receive backup power from a portable power source.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 18**.

Claim 19 is taught by Falik as shown supra with respect to claim 8.

Falik does not expressly teach that said first memory device type attribute corresponds to a NAND flash memory device and said second memory device type attribute corresponds to a NOR flash memory device.

With respect to claim 19, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 lines 51-65 shows that the memory devices may be NAND or NOR type flash memories.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a volatile memory disposed to receive backup power from a portable power source.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 19**.

29. **Claims 16, 17, 22-24, and 93** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Sinclair et al. (US 2006/0184723).

Claim 16 if taught by Falik as shown supra with respect to claim 2.

Although Falik teaches that the width of the array is the minimum programming size of the array at column 20 lines 62-65, and that the width of the array is stored at column 20 lines 49-52, Falik does not expressly teach that a first and second partial page size attribute is stored and used.

With respect to claim 16, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claims 16 and 17**.

Claim 17 is taught by Falik and Sinclair as:

The method of claim 16: said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute. Sinclair paragraph 0168 shows that in a flash memory that supports

partial page programming, when sufficient data is transferred to the buffer, it is programmed to the page. Falik column 14 lines 51-60 and figure 3 shows that the first memory device group can be accessed.

And further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute. Sinclair paragraph 0168 shows that in a flash memory that supports partial page programming, when sufficient data is transferred to the buffer, it is programmed to the page. Falik column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

Claim 22 is taught by Falik as:

The method of claim 20, wherein: said second set of attributes includes a second page size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

And said second data set includes a second data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

And if said second data set size is greater than said second page size attribute, said transferring said second data set includes: performing a set of

write operations on said second memory device that includes using a second transfer size equal to said second page size attribute. Column 16 lines 48-52 shows that program buffer 19 may be a double buffer, allowing the programming of one chunk of data while another chunk of data is received. As discussed at column 27 lines 33-60, the program buffer corresponds to the batch size, which is the amount of data which can be programmed into the flash array at once.

Falik does not expressly teach that the transaction is made using a transfer size equal to the page size until a remaining portion of said second data set that has not yet been written to said second device is less than said second page size attribute and using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

With respect to claim 22, Sinclair teaches Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times. As discussed in paragraph 0168, when the end of the data group is received in the buffer and it is smaller than a full page of data, a partial page programming operation may be performed.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 22**.

Claim 23 is taught by Falik as:

The method of claim 20, wherein: said first set of attributes includes a page size attribute and a block size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Said first data set includes a first data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

If said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes: performing a set of write operations on said first memory device that includes using a second transfer size equal to said page size attribute […]. Column 27 lines 14-24 shows that bytes of data are sent until all the bytes have been sent.

And said second device profile. Column 14 lines 4-20 shows that each group of arrays has characteristics stored in the control, status, and capabilities registers 12.

Falik does not expressly teach that the transaction is made using a transfer size equal to the page size until a remaining portion of said first data set that has not yet been written to said first device is less than said first page size attribute and using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

With respect to claim 23, Sinclair teaches Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times. As discussed in paragraph 0168, when the end of the data group is received in the buffer and it is smaller than a full page of data, a partial page programming operation may be performed.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 23**.

Claim 24 is taught by Falik as shown supra with respect to claim 1, and further as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes: performing respective write operations on

said first and second memory devices by at least using a transfer size at least equal to a […] *page size attribute from said first set of attributes*. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations.

And performing at least one write operation on said second memory device by at least using a transfer size at least equal to a […] *page size attribute value from said second set of attributes*. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations. Column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

And said attribute difference includes different attribute values of said first and second […] *page size attributes*. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Although Falik teaches storing a page size attribute, it does not expressly teach storing a partial page size attribute.

With respect to claim 24, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 24**.

Claim 93 is taught by Falik as shown supra with respect to claim 80, and further as:

The electronic storage device of claim 80, wherein said memory controller is further adapted to: use a first partial page size attribute by performing a write operation on said first memory device and using a transfer size at least equal to said partial page size attribute. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations.

And use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations. Column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

Although Falik teaches storing a page size attribute, it does not expressly teach storing a partial page size attribute.

With respect to claim 93, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 93**.

30. **Claims 26-28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Lakhani et al. (US 6,961,805).

Claim 26 is taught by Falik as shown supra with respect to claim 1.

Falik further teaches, at column 20 lines 60-65, that Page Size Block1 stores the size of the minimal segment of a flash array erasable upon a single erase command. Additionally, column 16 line 53 through column 17 line 24 shows that data can be

written to a block of addresses by designating the starting address and performing a series of program continue operations.

Falik does not expressly teach using the block size attribute in performing a write operation that uses a transfer size that corresponds to the block size.

With respect to claim 26, Lakhani teaches, at column 18 lines 19-46, that predecoder 50 asserts sets of multiblock selection bits in response to control bits from the controller, which allows a designated number of blocks to be selected for writing at the same time.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to perform a write operation that uses a transfer size equal to the a block size attribute value that corresponds to a block size attribute of the first memory device.

The motivation for doing so would have been to reduce the time used to test the memory cells of the block, Lakhani column 8 lines 21-32.

Therefore, it would have been obvious to combine Lakhani with Falik to obtain the invention as specified in **claims 26 and 27**.

Claim 27 is taught by Lakhani as:

> *The method of claim 26, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value*. Column 13 lines 25-38 shows that a plurality of blocks can be selected at the same time.

Claim 28 is taught by Falik as shown supra with respect to claim 2.

Falik further teaches, at column 20 lines 60-65, that Page Size Block1 stores the size of the minimal segment of a flash array erasable upon a single erase command. Additionally, column 16 line 53 through column 17 line 24 shows that data can be written to a block of addresses by designating the starting address and performing a series of program continue operations.

Falik does not expressly teach using the block size attribute in performing a write operation that uses a transfer size that is equal to a multiple of the block size.

With respect to claim 28, Lakhani teaches, at column 18 lines 19-46, that predecoder 50 asserts sets of multiblock selection bits in response to control bits from the controller, which allows a designated number of blocks to be selected for writing at the same time.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to perform a write operation that uses a transfer size equal to the a block size attribute value that corresponds to a block size attribute of the first memory device.

The motivation for doing so would have been to reduce the time used to test the memory cells of the block, Lakhani column 8 lines 21-32.
Therefore, it would have been obvious to combine Lakhani with Falik to obtain the invention as specified in **claim 28**.

31. **Claims 29-44** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Rubinstein et al. (US 5,913,215).

Claim 29 is taught by Falik as:

Said method comprising: addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said first device profile representing a first set of attributes of said first memory device, and said second device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Falik does not expressly teach that the methods may be implemented using a computer readable medium comprising computer executable instructions.

With respect to claim 29, Rubinstein teaches at column 10, lines 3-15, that computer methods may be performed either by a series of instructions, or by specific hardware components that contain hard-wired logic for performing the method, or by any combination of the two.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a computer readable medium comprising computer executable instructions.

The rationale for doing so would have been that it is a known technique to implement methods in computer systems using a computer readable medium comprising computer executable instructions.

Therefore, it would have been obvious to combine Rubinstein with Falik to obtain the invention as recited in **claims 29-44**.

Claim 30 is taught by Falik as:

The computer readable medium of claim 29, wherein: said first memory location is part of a memory space associated with a first memory device, said second memory location is part of a memory space associated with a second

memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

And said first and second memory devices comprise at least a portion of a memory store. Figure 3 shows that the address space is mapped to the memory devices.

Claim 31 is taught by Falik as:

The computer readable medium of claim 30, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 32 is taught by Falik as:

The computer readable medium of claim 30, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 33 is taught by Falik as:

The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 34 is taught by Falik as:

The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

Claim 35 is taught by Falik as:

The computer readable medium of claim 29, wherein said means for addressing further includes: said first and second device profiles having at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 36 is taught by Falik as:

The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 37 is taught by Falik as:

The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 38 is taught by Falik as:

The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 39 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 40 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 41 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 42 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 43 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 44 is taught by Falik as:

The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

32. **Claims 61 and 64-68** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Chin et al. (US 2001/0010066).

Claim 61 is taught by Falik as shown supra with respect to claim 59.

Falik further teaches:

The memory controller of claim 59, wherein said interface controller includes: A first memory bus controller coupled to said control device and said memory device interface. Falik figure 4b item 116.

And an IO bus controller coupled to said IO device interface and said control device. Falik figure 4b item 117.

With respect to claim 61, Chin figure 2 teaches a bridge unit 104, which connects to a CPU bus 108 and a memory bus 110, including control logic 242, shown in paragraph 0037 to direct the operations of the queue storage elements through a network of control signals. Figure 2 also illustrates a data path between the CPU bus 108 and memory bus 110 through queues 250 and 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a main control device coupled to the memory device interface and data path as taught by Chin in the interface controller of Falik.

The motivation for doing so would have been to provide a means to manage the transfer of data through the interface performed by the system of Falik, see Chin paragraph 0037.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as specified in **claim 61**.

Claim 64 is taught by Falik as shown supra with respect to claim 59.

Falik does not expressly teach that a buffer is a FIFO or that a data path includes a plurality of queue slots.

With respect to claim 64, Chin teaches:

Wherein said buffer is a FIFO. Paragraph 0052 shows that queue 250 is a FIFO.

And said data path includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory. Figure 2 also shows read queue 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a FIFO and a data path including a plurality of queue slots in the system of Falik.

The motivation for doing so would have been to provide an interface that provides all devices in a computer system fair access to memory, Chin paragraph 0012.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as recited in **claim 64**.

Claim 65 is taught by Falik as shown supra with respect to claim 59.

Falik does not expressly teach that a data path includes a buffer having a plurality of queue slots.

With respect to claim 65, Chin teaches:

The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a FIFO and a data path including a plurality of queue slots in the system of Falik.

The motivation for doing so would have been to provide an interface that provides all devices in a computer system fair access to memory, Chin paragraph 0012.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as recited in **claims 65-67**.

Claim 66 is taught by Chin as:

The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a plurality of queue slots that buffer data from said IO device interface to said memory device interface. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory.

Claim 67 is taught by Chin as:

The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from

said memory device interface to said IO device interface. Figure 2 also shows read queue 252.

Claim 68 is taught by Falik as shown supra with respect to claim 1.

Falik further teaches a memory bus controller, figure 4b item 116, coupled to bus 90.

Falik does not expressly teach that the memory bus controller is coupled to a main control device.

With respect to claim 68, Chin teaches:

A second memory bus controller coupled to said main control device and said memory device interface. Figure 2 teaches a bridge unit 104, which connects to a CPU bus 108 and a memory bus 110, including control logic 242, shown in paragraph 0037 to direct the operations of the queue storage elements through a network of control signals. Figure 2 also illustrates a data path between the CPU bus 108 and memory bus 110 through queues 250 and 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a main control device coupled to the memory device interface and data path as taught by Chin in the interface controller of Falik.

The motivation for doing so would have been to provide a means to manage the transfer of data through the interface performed by the system of Falik, see Chin paragraph 0037.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as specified in **claim 68**.

33. **Claims 62 and 63** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Chin et al. (US 2001/0010066) as applied to claim 61 above, and further in view of Tsuruta (US 2007/0174506).

Claim 62 is taught by the combination of Falik and Chin as shown supra with respect to claim 61.

The combination of Falik and Chin does not expressly teach that the IO bus controller is disposed to respond to said memory transaction request by acknowledging said request and providing status to said main control device.

With respect to claim 62, Tsuruta teaches:

Wherein said IO bus controller is disposed to respond to said memory transaction request by acknowledging said request and providing status to said main control device. Paragraph 0183 shows that in response to a read req from the CPU, MEM-DMAC 232 issues a read ack signal. Paragraph 0186 shows that after the read operation is performed, a sequencer in the memory controller 231 issues ack to a sequencer in the MEM-DMAC 232.

At the time of the invention, it would have been obvious to use the acknowledgement system of Tsuruta in the combination of Falik and Chin.

The motivation for doing so would have been to provide coordination between the CPU interface and the read/write queues to perform the requested memory operations.

Therefore, it would have been obvious to combine Tsuruta with Falik and Chin to obtain the invention as specified in **claims 62 and 63**.

Claim 63 is taught by Chin as:

The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction. Paragraph 0052 shows that control logic provides control signals to the input and output selectors 351 and 353 that determine the values of the enable and select signals in response to a memory request from the CPU.

Coordinates the operation of said memory device interface. Paragraph 0052 shows that the data and address of each request is sent to the memory controller 200.

And manages the transfer of memory transaction data between said IO device interface and said memory device interface through a data path. Paragraph 0052 shows that data is transferred through the queue 250.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JARED RUTZ whose telephone number is (571)272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Christian Chace can be reached on (571)272-4190. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Notice of References Cited	Application/Control No. 12/876,113	Applicant(s)/Patent Under Reexamination BRUCE ET AL.	
	Examiner JARED RUTZ	Art Unit 2187	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-8,200,879	06-2012	Falik et al.	710/307
*	B	US-5,913,215	06-1999	Rubinstein et al.	707/708
*	C	US-7,330,954	02-2008	Nangle, Peter	711/170
*	D	US-2006/0184723	08-2006	Sinclair et al.	711/103
*	E	US-6,961,805	11-2005	Lakhani et al.	711/5
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*	G	US-2007/0174506	07-2007	Tsuruta, Toru	710/022
	H	US-			
	I	US-			
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NON-PATENT DOCUMENTS

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12876113	BRUCE ET AL.
	Examiner	Art Unit
	JARED RUTZ	2187

SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
inventor search in EAST	12/14/2012	jir
text search in EAST, see search history	12/14/2012	jir
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**** CONTINUING DATA **************************

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**** FOREIGN APPLICATIONS **************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **
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TITLE

MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES

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2645	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	(bruce near2 ircardo).in. or (verdan near2 marlon).in. or (somera near2 margaret anne).in. or (jago-on near2 rowenah).in. or (de belen near2 maria).in. or (palacol near2 ron).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/03 15:36
S2	17	(bruce near2 ricardo).in. or (verdan near2 marlon).in. or (somera near2 margaret).in. or (jago-on near2 rowenah).in. or (de belen near2 maria).in. or (palacol near2 ron).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/03 15:38
S7	3204	(plural or multiple or seperate) with (profile or attribute or parameters) with (memory)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:03
S8	3335	(hybrid or heterogenous) near3 memory	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:04
S9	112740	(hybrid or heterogenous or different) near3 memory	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:04
S10	619	S7 and S9	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:04
S11	15	S7 and S8	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:04
S12	15	S11 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:05
S13	10	("20020184579" | "20050090940" | "20060059314" | "20080183958" |	US-PGPUB; USPAT;	ADJ	OFF	2012/12/05 17:13

		"20090319722").PN.	USOCR; EPO; DERWENT; IBM_TDB			
S14	193506	(memory or device) near3 (parameter or attribute)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/05 17:36
S15	4741	(plural or multiple or seperate) with (profile or attribute or parameter) with (memory)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/05 17:36
S16	2473	S14 and S15	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/05 17:36
S17	20106	(parameter or attribute) with (flash or nand or nor)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/05 17:37
S18	204	S16 and S17	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/05 17:37
S19	181	S18 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:37
S20	10	S19 and (page near3 size)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:38
S21	28	("4309754" | "4633437" | "4683534" | "4716527" | "5113369" | "5369754" | "5423009" | "5537624" | "5537659" | "5594874" | "5761456" | "5768560" | "5778413" | "5911053" | "6016270" | "6101565" | "6202140" | "6235554" | "6298426" | "6381664" | "6442076" | "6472747" | "6605875" | "6618790" | "6657899" | "6658508" | "6721840" | "7146510").PN. OR ("8200879").URPN.	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/12/06 12:54
S25	1	("6,430,663").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/12/11 15:23
S26	1	("5913215").PN.	US-PGPUB;	OR	OFF	2012/12/13

			USPAT; USOCR			10:22
S27	113091	(hybrid or heterogenous or different) near3 memory	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:03
S28	26	S27 and (DRAM same NAND same NOR same battery)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:03
S29	13	S28 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:03
S30	299	partial page program$4	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:48
S31	192	S27 and S30	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:48
S32	13	S29 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:48
S33	165	S31 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:48
S34	53823	(short$3 or shorten$3 or truncat$3) near3 (burst or transmission)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:50
S35	0	S33 and S34	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:50
S36	0	S30 and S34	US-PGPUB; USPAT; USOCR; EPO;	ADJ	OFF	2012/12/13 11:50

			DERWENT; IBM_TDB			
S37	20	S30 and burst	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 12:26
S38	14	S37 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 12:26
S39	92	partial page with (size or attribute)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 12:29
S40	6	S33 and S39	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 12:29
S41	198032	(profile or attribute or parameter) with (memory)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/13 12:32
S42	54	S33 and S41	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/13 12:32
S43	1	("5860107").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/12/13 13:20
S44	11735	(short$3 or shorten$3 or truncat$3) near3 (burst)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 15:18
S45	141	((multiple or plural or series) near3 (burst)) with (remaining or remainder or additional)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 15:19
S46	26	S44 and S45	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 15:20
S47	24	S46 and @ad<"20100904"	US-PGPUB;	ADJ	OFF	2012/12/13

			USPAT; USOCR; EPO; DERWENT; IBM_TDB			15:20
S48	135	S45 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 15:29
S49	1	("20060184723").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/12/13 17:13
S50	110530	(writ$3 or program$4) near3 block	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:33
S51	6832	(711/103).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/12/13 19:34
S52	3586	S50 and S51	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:34
S53	19	(writ$3 or program$4) near3 multiple blocks with (instruction or command)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:45
S54	299	(writ$3 or program$4) near3 multiple blocks	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:52
S55	44	S51 and S54	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:52
S57	37	S55 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:52
S58	285682	(flash or memory) near3 controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:50
S59	6008	(flash or memory) near3 interface with	US-PGPUB;	ADJ	OFF	2012/12/14

		(bus near3 (controller or master))	USPAT; USOCR; EPO; DERWENT; IBM_TDB			12:51
S60	5308	S58 and S59	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:51
S61	10796	fifo with input with output	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:52
S62	101	S60 and S61	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:52
S63	4117	fifo with (slots or entries)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:53
S64	4	S62 and S63	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:53
S65	99	S62 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 13:00
S66	113091	(hybrid or heterogenous or different) near3 memory	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 13:15
S67	790	S60 and S66	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 13:15
S68	18560	(fifo or queue) with input with output	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 13:16
S69	42	S67 and S68	US-PGPUB;	ADJ	OFF	2012/12/14

			USPAT; USOCR; EPO; DERWENT; IBM_TDB			13:16
S70	41	S69 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 13:16
S71	134	(acknowledg$3 or acknoweledgement or ack) with (bus near3 (controller or master)) with CPU	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:13
S72	5308	S58 and S59	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:13
S73	10	S59 and S71	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:14
S74	10	S73 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:14
S75	477	(status or complet$3) with (bus near3 (controller or master)) with CPU	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:21
S76	43	S71 and S75	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:21
S77	43	S76 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:21
S78	58	(acknowledg$3 or acknoweledgement or ack) with (memory near3 (controller)) with CPU	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:24
S79	57	S78 and @ad<"20100904"	US-PGPUB;	ADJ	OFF	2012/12/14

			USPAT; USOCR; EPO; DERWENT; IBM_TDB			15:25
S80	1016	(status or complet$3 or error) with (memory near3 (controller)) with CPU	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:25
S81	11	S79 and S80	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:25

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12876113	BRUCE ET AL.
	Examiner	Art Unit
	JARED RUTZ	2187

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/14/2012								
	1	✓								
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	36	✓								

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
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	Examiner	Art Unit
	JARED RUTZ	2187

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/14/2012								
	37	✓								
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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
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	Examiner	Art Unit
	JARED RUTZ	2187

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/14/2012								
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URIARTE LAW
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2021 The Alameda
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San Jose, CA 95126

Courtesy Reminder for
Application Serial No: 12/876,113

Attorney Docket No: 6005.042
Customer Number: 64180
Date of Electronic Notification: 12/21/2012

This is a courtesy reminder that new correspondence is available for this application. If you have not done so already, please review the correspondence. The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

An email notification regarding the correspondence was sent to the following email address(es) associated with your customer number:
mail@URIARTELAW.COM
stephen@uriartelaw.com
labid@uriartelaw.com

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Ricardo H. Bruce, et al.	Confirmation No.: 1607
Serial No.: 12/876,113	Examiner: Jared Ian Rutz Ph: 571-272-5535
Filing Date: Sept. 4, 2010	Art Unit: 2187
Title: Multi-Profile Memory Controller For Computing Devices	Atty. Docket No.: 6005.042

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE AND AMENDMENT

Sir:

The following is in response to the office action mailed on 21 December 2012.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 24 of this paper.

03/27/2013 MBLANCO 00000012 12876113
01 FC:2202 320.00 OP

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising:

addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

using attributes from said first and second device profiles.

2. (original) The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device.

3. (original) The method of claim 1, wherein said difference between said first and second device profiles includes different attributes; and said addressing said first memory location is made in response to a first memory transaction request; and

further including addressing said second memory location.

4. (original) The method of claim 1, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes.

5. (original) The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

6. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute values.

7. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute types.

8. (original) The method of claim 5, wherein said shared attributes include a memory device type attribute.

9. (original) The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

10. (original) The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

11. (original) The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

12. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

13. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of attributes that differs in value from a second page size attribute from said second set of attributes.

14. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes.

15. (original) The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device, and said second memory device interface attribute corresponds to a DRAM device interface.

16. (original) The method of claim 2, wherein said using attributes from said first and second device profile further includes using a first partial page size attribute from said first set of attributes that differs in value from a second partial page size attribute from said second set of attributes.

17. (original) The method of claim 16:

said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute; and

further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute.

18. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

19. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a NAND flash memory device and said second memory device type attribute corresponds to a NOR flash memory device.

20. (original) The method of claim 2, further including:

using an address corresponding to a memory location from said first memory device and transferring a first data set, and

using an address corresponding to a memory location from said second memory device and transferring a second data set.

21. (original) The method of claim 20, wherein:

said first set of attributes includes a first page size attribute, and said first data set includes a first data set size; and

if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size.

22. (original) The method of claim 20, wherein:

said second set of attributes includes a second page size attribute, and said second data set includes a second data set size; and

if said second data set size is greater than said second page size attribute, said transferring said second data set includes:

performing a set of write operations on said second memory device that includes using a second transfer size equal to said second page size attribute until a remaining portion of said second data set that has not yet been written to said second device is less than said second page size attribute, and

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

23. (currently amended) The method of claim 20, wherein:

said first set of attributes includes a page size attribute and a block size attribute;

said first data set includes a first data set size;

if said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes:

performing a set of write operations on said first memory device that includes using a second transfer size

equal to said page size attribute until a remaining portion of said first data set that has not yet been written to said first device is less than said page size attribute,

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size; [[and

said second device profile]].

24. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes:

performing respective write operations on said first and second memory devices by at least using a transfer size at least equal to a partial page size attribute from said first set of attributes and performing at least one write operation on said second memory device by at least using a transfer size at least equal to a partial page size attribute value from said second set of attributes; and

said attribute difference includes different attribute values of said first and second partial page size attributes.

25. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size attribute of said first memory device.

26. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a block size attribute value that corresponds to a block size attribute of said first memory device.

27. (original) The method of claim 26, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

28. (original) The method of claim 2, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

29. (currently amended) A non-transitory computer readable medium comprising computer executable instructions adapted to cause a method of performing memory transactions on a first memory location and a second memory location, said method comprising:

addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory device, and said second

device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles; and

using attributes from said first and second device profiles.

30. (original) The computer readable medium of claim 29, wherein:

said first memory location is part of a memory space associated with a first memory device;

said second memory location is part of a memory space associated with a second memory device; and

said first and second memory devices comprise at least a portion of a memory store.

31. (currently amended) The computer readable medium of claim [[30]]29, wherein [[said]] at least one attribute of said attributes includes a block size and said difference includes a block size value of [[said]]a first memory device and a block size value of [[said]]a second memory device.

32. (currently amended) The computer readable medium of claim 30, wherein [[said]] at least one attribute of said attributes includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

33. (original) The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

34. (original) The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes.

35. (currently amended) The computer readable medium of claim 29, wherein said [[means for]] addressing further includes:

said first and second device profiles having at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

36. (original) The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

37. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values.

38. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types.

39. (original) The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute.

40. (original) The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

41. (original) The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

42. (original) The computer readable medium of claim 36, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

43. (original) The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes.

44. (original) The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device.

45. (currently amended) A memory controller for performing memory transactions, said memory controller comprising:

a means for addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile;

wherein said means for addressing includes an interface controller means for processing memory transaction requests;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said means for addressing uses attributes from said first and second device profiles.

46. (original) The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

47. (original) The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute

value from a second block size attribute from said second set of attributes.

48. (original) The memory controller of claim 46, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said use of said attributes from said first and second device profiles by said means for addressing includes using said different attribute qualifiers for said shared attributes.

49. (original) The memory controller of claim 46, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

50. (currently amended) The memory controller of claim 45, wherein said means for addressing further includes a means for addressing said second memory location.

51. (original) The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

52. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values.

53. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types.

54. (original) The memory controller of claim 51, wherein said shared attributes include a memory device type attribute.

55. (original) The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

56. (original) The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

57. (original) The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

58. (original) The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device.

59. (original) A memory controller comprising:

an interface controller coupled to a memory device interface and an IO device interface;

said interface controller disposed to perform a memory transaction by addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile;

said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said addressing of said first memory location includes using said attributes from said first device profile.

60. (original) The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile.

61. (currently amended) The memory controller of claim 59, wherein said interface controller includes:

a main control device coupled to said memory device interface and to [[said]]a data path;

a first memory bus controller coupled to said control device and said memory device interface; and

an IO bus controller coupled to said IO device interface and said control device.

62. (currently amended) The memory controller of claim 61, wherein said IO bus controller is disposed to respond to [[said]]a memory transaction request by acknowledging said request and providing status to said main control device.

63. (original) The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction, coordinates the operation of said memory device interface, and manages the transfer of memory transaction data between said IO device interface and said memory device interface through a data path.

64. (currently amended) The memory controller of claim 59, [[wherein]]further including [[said]]a buffer [[is]]comprising a FIFO and [[said]]a data path that includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface.

65. (original) The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots.

66. (original) The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a

plurality of queue slots that buffer data from said IO device interface to said memory device interface.

67. (original) The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from said memory device interface to said IO device interface.

68. (currently amended) The memory controller of [[claim59]]claim 59, further including a second memory bus controller coupled to [[said]]a main control device and said memory device interface.

69. (original) The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes.

70. (original) The memory controller of claim 59, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

71. (original) The memory controller of claim 59, wherein said difference includes different attribute qualifiers for

at least one set of shared attributes from said first and second device profiles.

72. (original) The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute.

73. (original) The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values.

74. (original) The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values.

75. (original) The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type.

76. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values.

77. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types.

78. (original) The memory controller of claim 71, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

79. (original) The memory controller of claim 71, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

80. (original) An electronic storage device, comprising:

a memory controller disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said memory controller using attributes from said first and second device profiles.

81. (original) The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

82. (original) The electronic storage device of claim 80, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

83. (currently amended) The electronic storage device of claim 80, said memory controller further disposed to:

perform a write operation on said first memory device, if [[said]]a memory transaction request is associated with a write request;

perform a read operation on said first memory device, if said memory transaction request is associated with a read request; and

wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using said second device profile in response to receiving a second memory transaction request.

84. (original) The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

85. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values.

86. (original) The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute.

87. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types.

88. (original) The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said shared attributes.

89. (original) The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device.

90. (original) The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

91. (original) The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

92. (original) The electronic storage device of claim 84, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

93. (original) The electronic storage device of claim 80, wherein said memory controller is further adapted to:

use a first partial page size attribute by performing a write operation on said first memory device and using a

transfer size at least equal to said partial page size attribute; and

use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute.

94. (new) The method of claim 1, wherein the first memory location and the second memory location are addressable memory locations.

95. (new) The memory controller of claim 45, wherein the first memory location and the second memory location are addressable memory locations.

96. (new) The memory controller of claim 59, wherein the first memory location and the second memory location are addressable memory locations.

97. (new) The electronic device of claim 80, wherein the first memory location and the second memory location are addressable memory locations.

REMARKS/ARGUMENTS

Double Patenting

Claim 31 is being amended to depend on claim 29. Accordingly, the double-patenting rejection is no longer applicable. The withdrawal of the double-patenting rejection to claims 31 and 32 is respectfully requested.

Claim Objections

A clerical correction is made on claim 68. Accordingly, the claim objection to claim 68 is no longer applicable. The withdrawal of the objection to claim 68 is respectfully requested.

Claim Rejections 35 USC 101

Claim 29 is being amended to recite the language, "non-transitory computer readable medium" in the preamble. Accordingly, the claim rejection to claims 29-44 is no longer applicable. The withdrawal of the rejection to claims 29-44 is respectfully requested.

Claim Rejections 35 USC 112

Claim 45 is being amended as shown above. Support for this claim amendment is found in, for example, paragraph [0029] of the filed application. Accordingly, the claim rejection to claims 45-58 is no longer applicable. The withdrawal of the rejection to claims 45-58is respectfully requested.

35 USC 102

Claims 1-14, 20, 21, 25, 45-60, and 69-92

Claims 1-11 and 16-33 are rejected under 35 U.S.C. 102(e) as allegedly being anticipated by US 8,200,879 to Falik et al. ("Falik"). Claims 1, 45, 59, and 80 are independent claims. Applicants respectfully traverse this rejection.

Applicants respectfully contend that independent claim 1 recites the following limitations that are not disclosed within the four corners of Falik: addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile; said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and using attributes from said first and second device profiles.

The Office implies that information in the registers 12 disclose the first and second set of attributes of claim 1 (Office Action: page 7). Applicants respectfully disagree with the Office based on at least the reasons presented below.

Falik discloses the device and status control register (Falik: Figure 5A) which provides status and control information for an entire memory device (Falik: column 19, lines 4-8). Falik also discloses a flash device capabilities register (Falik: Figure 5B) that provides

capabilities and properties information on the same entire memory device (Falik: column 19, lines 49-53). Therefore, these registers contain information directed to the same entire memory device and not directed to different memory locations. These registers do not contain a first set of attributes of a first memory location and also do not contain a second set of attributes of a second memory location.

Falik also discloses section properties registers that provide information on structural properties of sections of a flash device (Falik: column 20, lines 49-55). However, Falik discloses these sections as logical sections which are not memory locations (Falik: column 14, lines 51-60 and column 20, lines 49-56). These registers do not contain a first set of attributes of a first memory location and also do not contain a second set of attributes of a second memory location.

Based on at least the above discussion, Falik does not disclose and does not teach "said first memory location and a second memory location respectively associated with a first device profile and a second device profile; said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles" as required in claim 1.

Since Falik does not disclose and does not teach all the limitations of claim 1, claim 1 is not anticipated by the cited reference. Claim 1 is otherwise allowable.

Claims 2-14, 20, 21, and 25 depend from allowable claim 1; as such, they are also allowable for at least the same reasons as claim 1.

The withdrawal of the rejections to claims 1-14, 20, 21, and 25 is respectfully requested.

Independent claims 45, 59, and 80 recite at least some limitations similar to that as claim 1. Although claims 45, 59, and 80 are different, Applicants respectfully argue that in this case the above arguments regarding the patentability of claim 1 apply with equal force with respect to claims 45, 59, and 80. Since Falik does not disclose and does not teach all the limitations of claims 45, 59, and 80, claims 45, 59, and 80 are not anticipated by the cited reference. Claims 45, 59, and 80 are otherwise allowable.

Claims 46-58 depend from allowable claim 45; as such, they are also allowable for at least the same reasons as claim 45.

Claims 60 and 69-79 depend from allowable claim 59; as such, they are also allowable for at least the same reasons as claim 59.

Claims 81-92 depend from allowable claim 80; as such, they are also allowable for at least the same reasons as claim 80.

The withdrawal of the rejection to claims 45-60 and 69-92 is respectfully requested.

Claims 15, 18, and 19

Claims 15, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 7,330,954 to Nangle.

Claims 15, 18, and 19 depend from allowable claim 1; as such, they are also allowable for at least the same reasons a claim 1.

The withdrawal of the rejection of claims 15, 18, and 19 is respectfully requested.

Claims 16, 17, 22-24, and 93

Claims 16, 17, 22-24, and 93 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 2006/0184723 to Sinclair.

Claims 16, 17, and 22-24 depend from allowable claim 1; as such, they are also allowable for at least the same reasons a claim 1.

Claim 93 depends from allowable claim 80; as such, claim 93 is also allowable for at least the same reasons a claim 1.

The withdrawal of the rejection of claims 16, 17, 22-24, and 93 is respectfully requested.

Claims 26-28

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 6961,805 to Lakhani et al.

Claims 26-28 depend from allowable claim 1; as such, they are also allowable for at least the same reasons a claim 1.

The withdrawal of the rejection of claims 26-28 is respectfully requested.

Claims 29-44

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 5,913,215 to Rubinstein.

The Office admits that Falik does not expressly teach that the methods may be implemented using a computer readable medium comprising computer executable instructions. In order to supply the missing limitations, the Office combines Falik with Rubinstein. The Office argues it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a computer readable medium comprising computer executable instructions (Office Action: page 44). The Applicants respectfully disagree with the assertions of the Office.

Independent claim 29 recite at least some limitations similar to that as claim 1. Although claim 29 is different, Applicants respectfully argue that in this case the above arguments regarding the patentability of claim 1 apply with equal force with respect to claim 29.

Since Falik and Rubinstein, considered individually or in combination, do not disclose and does not teach all the limitations of claim 29, claim 29 is not rendered obvious in view the cited references. Claim 29 is otherwise allowable.

Claims 30-44 depend from allowable claim 29; as such, they are also allowable for at least the same reasons a claim 29.

The withdrawal of the rejection of claims 29-44 is respectfully requested.

Claims 61 and 64-68

Claims 61 and 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 2001/0010066 to Chin et al.

Claims 61 and 64-68 depend from allowable claim 59; as such, they are also allowable for at least the same reasons a claim 59.

The withdrawal of the rejection of claims 61 and 64-68 is respectfully requested.

Claims 62 and 63

Claims 61 and 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of Chin as applied to claim 61 above, and further in view of US 2007/0174506 to Tsuruta.

Claims 62 and 63 depend from allowable claim 59; as such, they are also allowable for at least the same reasons a claim 59.

The withdrawal of the rejection of claims 62 and 63 is respectfully requested.

New dependent claims 94-97

New dependent claims 94-97 are being added. The new claims are supported in the filed application, for example, in Figures 1, 2A, 2B, and 2C, and accompanying text, and in paragraph [0015]. Applicants respectfully request the allowance of these claims.

Applicants respectfully request the allowance of the claims.

Conclusion

Claims 1-97 herein are allowable, and a timely Notice of Allowance is respectfully requested.

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (408) 256-0244.

Date: March 21, 2013

Respectfully submitted,

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Total Number of Pages in This Submission	34

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First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
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- ☐ Certified Copy of Priority Document(s)
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- ☐ Status Letter
- ☑ Other Enclosure(s) (please Identify below):

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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/876,113	Filing Date 09/04/2010	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **03/26/2013**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 97	Minus	** 93	= 4	X $40 =	160
Independent (37 CFR 1.16(h))	* 5	Minus	***5	= 0	X $210 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	**160**

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/876,113	09/04/2010	Ricardo H. BRUCE	6005.042	1607

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EXAMINER	
RUTZ, JARED IAN	
ART UNIT	PAPER NUMBER
2187	

NOTIFICATION DATE	DELIVERY MODE
05/14/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 12/876,113	Applicant(s) BRUCE ET AL.	
	Examiner JARED RUTZ	Art Unit 2187	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2013*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-97* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-97* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some * c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Interim copies:

a)☐ All b)☐ Some c)☐ None of the: Interim copies of the priority documents have been received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-97, as amended on 3/26/2013, are pending in the instant application. Applicant's arguments submitted 3/26/2013 have been carefully and fully considered, but are not found fully persuasive. The instant Office action is made **FINAL**.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-97** are rejected under 35 U.S.C. 102(e) as being anticipated by Falik et al. (US 8,200,879).

Claim 1 is taught by Falik as:

A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising: addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and

capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 2 is taught by Falik as:

The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 3 is taught by Falik as:

The method of claim 1, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

And said addressing said first memory location is made in response to a first memory transaction request. Column 18 lines 24-34 shows that applications on the main die 100 issue read and program commands.

And further including addressing said second memory location. Figure 6 shows that both sections can be addressed.

Claim 4 is taught by Falik as:

The method of claim 1, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 5 is taught by Falik as:

The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 6 is taught by Falik as:

The method of claim 5, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 7 is taught by Falik as:

The method of claim 5, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 8 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a memory device type attribute. Column 20 lines 30-36 shows that the registers can indicate if the device is self timed type flash memory or not.

Claim 9 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 10 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 11 is taught by Falik as:

The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size,

memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 12 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 13 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of attributes that differs in value from a second page size attribute from said second set of attributes. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 14 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 20 is taught by Falik as:

The method of claim 2, further including: using an address corresponding to a memory location from said first memory device and transferring a first data set. Column 16 lines 53-62 shows that an address and data are sent for a programming operation.

And using an address corresponding to a memory location from said second memory device and transferring a second data set. Column 14 lines 51-65 show that the standard address space is mapped to the logical sections into which the arrays are grouped, showing that the second memory device is accessed using an address corresponding to the second memory device.

Claim 21 is taught by Falik as:

The method of claim 20, wherein: said first set of attributes includes a first page size attribute. Column 20 lines 62-65 shows that the minimum

programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

And said first data set includes a first data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

And if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size. Column 27 lines 9-24 shows that when the number of bytes to be transferred to the FD have been transferred, the transfer process ends by setting the bus to a HiZ state.

Claim 25 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size attribute of said first memory device. As discussed at column 27 lines 33-60, the program buffer corresponds to the batch size, which is the amount of data which can be programmed into the flash array at once.

Claim 45 is taught by Falik as:

A memory controller for performing memory transactions, said memory controller comprising: a means for addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Wherein said means for addressing includes an interface controller means for processing memory transaction requests. Figure 4B, flash bus transactions state machine 116.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And said means for addressing uses attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 46 is taught by Falik as:

The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 47 is taught by Falik as:

The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 48 is taught by Falik as:

The memory controller of claim 46, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows

that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said use of said attributes from said first and second device profiles by said means for addressing includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 49 is taught by Falik as:

The memory controller of claim 46, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 50 is taught by Falik as:

The memory controller of claim 45, wherein said means for addressing further includes a means for addressing said second memory location. Figure 6 shows that both sections can be addressed.

Claim 51 is taught by Falik as:

The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 52 is taught by Falik as:

The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 53 is taught by Falik as:

The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 54 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6

shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 55 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 56 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 57 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size,

block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 58 is taught by Falik as:

The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

Claim 59 is taught by Falik as:

A memory controller comprising: an interface controller coupled to a memory device interface and an IO device interface. Figure 4B shows interface controller 110 connected to bus 90 and internal bus 140.

Said interface controller disposed to perform a memory transaction by addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column

16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And said addressing of said first memory location includes using said attributes from said first device profile. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 60 is taught by Falik as:

The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile. Figure 6 shows that both sections can be addressed.

Claim 69 is taught by Falik as:

The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-

48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

Claim 70 is taught by Falik as:

The memory controller of claim 59, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 71 is taught by Falik as:

The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 72 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 73 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 74 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 75 is taught by Falik as:

The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 76 is taught by Falik as:

The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 77 is taught by Falik as:

The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 78 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block

size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 79 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 80 is taught by Falik as:

An electronic storage device, comprising: a memory controller disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the

standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And said memory controller using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 81 is taught by Falik as:

The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command. Column 9 lines 5-18 shows that the interface performs appropriate requests for erasure.

Claim 82 is taught by Falik as:

The electronic storage device of claim 80, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 83 is taught by Falik as:

The electronic storage device of claim 80, said memory controller further disposed to: perform a write operation on said first memory device, if a memory transaction request is associated with a write request. Column 16 lines 53-64 shows that write transactions may be performed.

Perform a read operation on said first memory device, if said memory transaction request is associated with a read request. Column 16 lines 53-64 shows that read transactions may be performed.

And wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using said second device profile in response to receiving a second memory transaction request. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used for accesses to the groups of memory arrays.

Claim 84 is taught by Falik as:

The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 85 is taught by Falik as:

The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 86 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 87 is taught by Falik as:

The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20

line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 88 is taught by Falik as:

The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 89 is taught by Falik as:

The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

Claim 90 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 91 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 92 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 94 is taught by Falik as:

The method of claim 1, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 95 is taught by Falik as:

The memory controller of claim 45, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 96 is taught by Falik as:

The memory controller of claim 59, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 97 is taught by Falik as:

The electronic device of claim 80, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which

may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 15, 18, and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Nangle (US 7,330,954).

Claim 15 is taught by Falik as:

The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device. Column 21 lines 7-10 shows that the information can correspond to a flash device FD.

Although Falik column 21 lines 7-10 shows that other memory technologies such as SRAM may be used, it does not expressly teach that the second memory device attribute corresponds to a DRAM device interface.

With respect to claim 15, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 lines 51-67 shows that the memory devices may be flash memory and DRAM.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include flash memory and DRAM in the system of Falik.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 15**.

Claim 18 is taught by Falik as shown supra with respect to claim 8.

Falik does not expressly teach that said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

With respect to claim 18, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 line 51 through column 5 line 4 shows that the memory devices may be volatile memory that have a battery backup.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a volatile memory disposed to receive backup power from a portable power source.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 18**.

Claim 19 is taught by Falik as shown supra with respect to claim 8.

Falik does not expressly teach that said first memory device type attribute corresponds to a NAND flash memory device and said second memory device type attribute corresponds to a NOR flash memory device.

With respect to claim 19, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 lines 51-65 shows that the memory devices may be NAND or NOR type flash memories.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a volatile memory disposed to receive backup power from a portable power source.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 19**.

6. **Claims 16, 17, 22-24, and 93** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Sinclair et al. (US 2006/0184723).

Claim 16 if taught by Falik as shown supra with respect to claim 2.

Although Falik teaches that the width of the array is the minimum programming size of the array at column 20 lines 62-65, and that the width of the array is stored at column 20 lines 49-52, Falik does not expressly teach that a first and second partial page size attribute is stored and used.

With respect to claim 16, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claims 16 and 17**.

Claim 17 is taught by Falik and Sinclair as:

The method of claim 16: said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute. Sinclair paragraph 0168 shows that in a flash memory that supports partial page programming, when sufficient data is transferred to the buffer, it is programmed to the page. Falik column 14 lines 51-60 and figure 3 shows that the first memory device group can be accessed.

And further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute. Sinclair paragraph 0168 shows that in a flash memory that supports partial page programming, when sufficient data is transferred to the buffer, it is programmed to the page. Falik column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

Claim 22 is taught by Falik as:

The method of claim 20, wherein: said second set of attributes includes a second page size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

And said second data set includes a second data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

And if said second data set size is greater than said second page size attribute, said transferring said second data set includes: performing a set of write operations on said second memory device that includes using a second transfer size equal to said second page size attribute. Column 16 lines 48-52 shows that program buffer 19 may be a double buffer, allowing the programming of one chunk of data while another chunk of data is received. As discussed at column 27 lines 33-60, the program buffer corresponds to the batch size, which is the amount of data which can be programmed into the flash array at once.

Falik does not expressly teach that the transaction is made using a transfer size equal to the page size until a remaining portion of said second data set that has not yet been written to said second device is less than said second page size attribute and using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

With respect to claim 22, Sinclair teaches Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times. As discussed in paragraph 0168, when the end of the data group is received in the buffer and it is smaller than a full page of data, a partial page programming operation may be performed.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 22**.

Claim 23 is taught by Falik as:

The method of claim 20, wherein: said first set of attributes includes a page size attribute and a block size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Said first data set includes a first data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

If said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes: performing a set of write

operations on said first memory device that includes using a second transfer size equal to said page size attribute [...]. Column 27 lines 14-24 shows that bytes of data are sent until all the bytes have been sent.

Falik does not expressly teach that the transaction is made using a transfer size equal to the page size until a remaining portion of said first data set that has not yet been written to said first device is less than said first page size attribute and using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

With respect to claim 23, Sinclair teaches Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times. As discussed in paragraph 0168, when the end of the data group is received in the buffer and it is smaller than a full page of data, a partial page programming operation may be performed.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 23**.

Claim 24 is taught by Falik as shown supra with respect to claim 1, and further as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes: performing respective write operations on said first and second memory devices by at least using a transfer size at least equal to a […] *page size attribute from said first set of attributes*. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations.

And performing at least one write operation on said second memory device by at least using a transfer size at least equal to a […] *page size attribute value from said second set of attributes*. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations. Column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

And said attribute difference includes different attribute values of said first and second […] *page size attributes*. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Although Falik teaches storing a page size attribute, it does not expressly teach storing a partial page size attribute.

With respect to claim 24, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 24**.

Claim 93 is taught by Falik as shown supra with respect to claim 80, and further as:

The electronic storage device of claim 80, wherein said memory controller is further adapted to: use a first partial page size attribute by performing a write operation on said first memory device and using a transfer size at least equal to said partial page size attribute. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations.

And use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing

address locations. Column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

Although Falik teaches storing a page size attribute, it does not expressly teach storing a partial page size attribute.

With respect to claim 93, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 93**.

7. **Claims 26-28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Lakhani et al. (US 6,961,805).

Claim 26 is taught by Falik as shown supra with respect to claim 1.

Falik further teaches, at column 20 lines 60-65, that Page Size Block1 stores the size of the minimal segment of a flash array erasable upon a single erase command.

Additionally, column 16 line 53 through column 17 line 24 shows that data can be written to a block of addresses by designating the starting address and performing a series of program continue operations.

Falik does not expressly teach using the block size attribute in performing a write operation that uses a transfer size that corresponds to the block size.

With respect to claim 26, Lakhani teaches, at column 18 lines 19-46, that predecoder 50 asserts sets of multiblock selection bits in response to control bits from the controller, which allows a designated number of blocks to be selected for writing at the same time.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to perform a write operation that uses a transfer size equal to the a block size attribute value that corresponds to a block size attribute of the first memory device.

The motivation for doing so would have been to reduce the time used to test the memory cells of the block, Lakhani column 8 lines 21-32.

Therefore, it would have been obvious to combine Lakhani with Falik to obtain the invention as specified in **claims 26 and 27**.

Claim 27 is taught by Lakhani as:

The method of claim 26, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a

transfer size equal to a multiple of said block size attribute value. Column 13 lines 25-38 shows that a plurality of blocks can be selected at the same time.

Claim 28 is taught by Falik as shown supra with respect to claim 2.

Falik further teaches, at column 20 lines 60-65, that Page Size Block1 stores the size of the minimal segment of a flash array erasable upon a single erase command. Additionally, column 16 line 53 through column 17 line 24 shows that data can be written to a block of addresses by designating the starting address and performing a series of program continue operations.

Falik does not expressly teach using the block size attribute in performing a write operation that uses a transfer size that is equal to a multiple of the block size.

With respect to claim 28, Lakhani teaches, at column 18 lines 19-46, that predecoder 50 asserts sets of multiblock selection bits in response to control bits from the controller, which allows a designated number of blocks to be selected for writing at the same time.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to perform a write operation that uses a transfer size equal to the a block size attribute value that corresponds to a block size attribute of the first memory device.

The motivation for doing so would have been to reduce the time used to test the memory cells of the block, Lakhani column 8 lines 21-32.

Therefore, it would have been obvious to combine Lakhani with Falik to obtain the invention as specified in **claim 28**.

8. **Claims 29-44** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Rubinstein et al. (US 5,913,215).

Claim 29 is taught by Falik as:

Said method comprising: addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said first device profile representing a first set of attributes of said first memory device, and said second device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14

lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Falik does not expressly teach that the methods may be implemented using a non-transitory computer readable medium comprising computer executable instructions.

With respect to claim 29, Rubinstein teaches at column 10, lines 3-15, that computer methods may be performed either by a series of instructions, or by specific hardware components that contain hard-wired logic for performing the method, or by any combination of the two.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a computer readable medium comprising computer executable instructions.

The rationale for doing so would have been that it is a known technique to implement methods in computer systems using a non-transitory computer readable medium comprising computer executable instructions.

Therefore, it would have been obvious to combine Rubinstein with Falik to obtain the invention as recited in **claims 29-44**.

Claim 30 is taught by Falik as:

The computer readable medium of claim 29, wherein: said first memory location is part of a memory space associated with a first memory device, said

second memory location is part of a memory space associated with a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

And said first and second memory devices comprise at least a portion of a memory store. Figure 3 shows that the address space is mapped to the memory devices.

Claim 31 is taught by Falik as:

The computer readable medium of claim 29, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of a first memory device and a block size value of a second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 32 is taught by Falik as:

The computer readable medium of claim 30, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 33 is taught by Falik as:

The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 34 is taught by Falik as:

The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

Claim 35 is taught by Falik as:

The computer readable medium of claim 29, wherein said addressing further includes: said first and second device profiles having at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 36 is taught by Falik as:

The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 37 is taught by Falik as:

The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 38 is taught by Falik as:

The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 39 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 40 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 41 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 42 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 43 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 44 is taught by Falik as:

The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

9. **Claims 61 and 64-68** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Chin et al. (US 2001/0010066).

Claim 61 is taught by Falik as shown supra with respect to claim 59.

Falik further teaches:

The memory controller of claim 59, wherein said interface controller includes: A first memory bus controller coupled to said control device and said memory device interface. Falik figure 4b item 116.

And an IO bus controller coupled to said IO device interface and said control device. Falik figure 4b item 117.

With respect to claim 61, Chin figure 2 teaches a bridge unit 104, which connects to a CPU bus 108 and a memory bus 110, including control logic 242, shown in paragraph 0037 to direct the operations of the queue storage elements through a network of control signals. Figure 2 also illustrates a data path between the CPU bus 108 and memory bus 110 through queues 250 and 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a main control device coupled to the memory device interface and data path as taught by Chin in the interface controller of Falik.

The motivation for doing so would have been to provide a means to manage the transfer of data through the interface performed by the system of Falik, see Chin paragraph 0037.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as specified in **claim 61**.

Claim 64 is taught by Falik as shown supra with respect to claim 59.

Falik does not expressly teach that a buffer is a FIFO or that a data path includes a plurality of queue slots.

With respect to claim 64, Chin teaches:

Further including a buffer comprising a FIFO. Paragraph 0052 shows that queue 250 is a FIFO.

And a data path that includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory. Figure 2 also shows read queue 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a FIFO and a data path including a plurality of queue slots in the system of Falik.

The motivation for doing so would have been to provide an interface that provides all devices in a computer system fair access to memory, Chin paragraph 0012.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as recited in **claim 64**.

Claim 65 is taught by Falik as shown supra with respect to claim 59.

Falik does not expressly teach that a data path includes a buffer having a plurality of queue slots.

With respect to claim 65, Chin teaches:

The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a FIFO and a data path including a plurality of queue slots in the system of Falik.

The motivation for doing so would have been to provide an interface that provides all devices in a computer system fair access to memory, Chin paragraph 0012.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as recited in **claims 65-67**.

Claim 66 is taught by Chin as:

The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a plurality of queue slots that buffer data from said IO device interface to said memory device interface. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory.

Claim 67 is taught by Chin as:

The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from

said memory device interface to said IO device interface. Figure 2 also shows read queue 252.

Claim 68 is taught by Falik as shown supra with respect to claim 1.

Falik further teaches a memory bus controller, figure 4b item 116, coupled to bus 90.

Falik does not expressly teach that the memory bus controller is coupled to a main control device.

With respect to claim 68, Chin teaches:

A second memory bus controller coupled to said main control device and said memory device interface. Figure 2 teaches a bridge unit 104, which connects to a CPU bus 108 and a memory bus 110, including control logic 242, shown in paragraph 0037 to direct the operations of the queue storage elements through a network of control signals. Figure 2 also illustrates a data path between the CPU bus 108 and memory bus 110 through queues 250 and 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a main control device coupled to the memory device interface and data path as taught by Chin in the interface controller of Falik.

The motivation for doing so would have been to provide a means to manage the transfer of data through the interface performed by the system of Falik, see Chin paragraph 0037.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as specified in **claim 68**.

10. **Claims 62 and 63** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Chin et al. (US 2001/0010066) as applied to claim 61 above, and further in view of Tsuruta (US 2007/0174506).

Claim 62 is taught by the combination of Falik and Chin as shown supra with respect to claim 61.

The combination of Falik and Chin does not expressly teach that the IO bus controller is disposed to respond to said memory transaction request by acknowledging said request and providing status to said main control device.

With respect to claim 62, Tsuruta teaches:

Wherein said IO bus controller is disposed to respond to a memory transaction request by acknowledging said request and providing status to said main control device. Paragraph 0183 shows that in response to a read req from the CPU, MEM-DMAC 232 issues a read ack signal. Paragraph 0186 shows that after the read operation is performed, a sequencer in the memory controller 231 issues ack to a sequencer in the MEM-DMAC 232.

At the time of the invention, it would have been obvious to use the acknowledgement system of Tsuruta in the combination of Falik and Chin.

The motivation for doing so would have been to provide coordination between the CPU interface and the read/write queues to perform the requested memory operations.

Therefore, it would have been obvious to combine Tsuruta with Falik and Chin to obtain the invention as specified in **claims 62 and 63**.

Claim 63 is taught by Chin as:

The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction. Paragraph 0052 shows that control logic provides control signals to the input and output selectors 351 and 353 that determine the values of the enable and select signals in response to a memory request from the CPU.

Coordinates the operation of said memory device interface. Paragraph 0052 shows that the data and address of each request is sent to the memory controller 200.

And manages the transfer of memory transaction data between said IO device interface and said memory device interface through a data path. Paragraph 0052 shows that data is transferred through the queue 250.

Response to Arguments

2. Applicant's arguments, see the first paragraph beginning on page 24 of the remarks filed 3/26/2013, with respect to the double patenting objection to claims 31 and

32 have been fully considered and are persuasive. The double patenting objection to claims 31 and 32 has been withdrawn.

3. Applicant's arguments, see the second paragraph beginning on page 24 of the remarks filed 3/26/2013, with respect to the objection to claim 68 have been fully considered and are persuasive. The objection to claim 68 has been withdrawn.

4. Applicant's arguments, see the third paragraph beginning on page 24 of the remarks filed 3/26/2013, with respect to the rejection of claims 29-44 under 35 USC 101 have been fully considered and are persuasive. The rejection of claims 29-44 under 35 USC 101 has been withdrawn.

5. Applicant's arguments, see the fourth paragraph beginning on page 24 of the remarks filed 3/26/2013, with respect to the rejection of claims 45-58 under 35 USC 112 second paragraph have been fully considered and are persuasive. The rejection of claims 45-58 under 35 USC 112 second paragraph has been withdrawn.

6. In the fourth paragraph beginning on page 25 and continuing in the first paragraph beginning on page 26, with respect to the teachings of Falik, Applicant argues:

> "Falik discloses the device and status control register (Falik: Figure 5A) which provides status and control information for an entire memory device (Falik: column 19, lines 4-8). Falik also discloses a flash device capabilities register (Falik: Figure 5B), that provides capabilities and properties information on the same entire memory device (Falik: column 19, lines 49-53). Therefore, these registers contain information directed to the same entire memory device and not

directed to different memory locations. These registers do not contain a first set of attributes of a first memory location and also do not contain a second set of attributes of a second memory location.

Falik also discloses section properties registers that provide information on structural properties of sections of a flash device (Falik: column 20, lines 49-55). However, Falik discloses these sections as logical sections which are not memory locations (Falik: column 14, lines 51-60 and column 20, lines 49-56). These registers do not contain a first set of attributes of a first memory location and also do not contain a second set of attributes of a second memory location."

7. The Examiner respectfully disagrees. As noted at column 19 lines 49-55, the flash device capabilities register stores information on the capabilities and properties of the flash device. As noted at column 6 lines 11-19, the flash device may have multiple arrays, each having different parameters. As shown at column 14 lines 40-65, the arrays having identical structure are logically grouped into sections, and that the address space of each logical block is divided into a plurality of sections that correspond to the logical groups. As the sections are included in the address map, each section includes a plurality of addressable memory locations. Column 15 lines 63-67 shows that characteristics of each section 57, in the information block and its assignment to a sub-block, are stored in a corresponding Section Capabilities Register. As noted at column 20 lines 49-56, there is a section properties register that stores structural properties of each of the sections of the device. Column 20 lines 60-67 shows that the section properties register includes PageSizeBlock1 which indicates the size of the

minimum segment of the array which may be erased with a single erase command, which is specifically mentioned in the specification of the instant application at paragraph 0015 as an example of an attribute of a memory region.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JARED RUTZ whose telephone number is (571)272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Christian Chace can be reached on (571)272-4190. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jared I Rutz
Primary Examiner
Art Unit 2187

/Jared I Rutz/
Primary Examiner, Art Unit 2187

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	(bruce near2 ircardo).in. or (verdan near2 marlon).in. or (somera near2 margaret anne).in. or (jago-on near2 rowenah).in. or (de belen near2 maria).in. or (palacol near2 ron).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/03 15:36
S2	17	(bruce near2 ricardo).in. or (verdan near2 marlon).in. or (somera near2 margaret).in. or (jago-on near2 rowenah).in. or (de belen near2 maria).in. or (palacol near2 ron).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/03 15:38
S7	3204	(plural or multiple or seperate) with (profile or attribute or parameters) with (memory)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:03
S8	3335	(hybrid or heterogenous) near3 memory	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:04
S9	112740	(hybrid or heterogenous or different) near3 memory	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:04
S10	619	S7 and S9	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:04
S11	15	S7 and S8	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:04
S12	15	S11 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:05
S13	10	("20020184579" | "20050090940" | "20060059314" | "20080183958" |	US-PGPUB; USPAT;	ADJ	OFF	2012/12/05 17:13

		"20090319722").PN.	USOCR; EPO; DERWENT; IBM_TDB			
S14	193506	(memory or device) near3 (parameter or attribute)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/05 17:36
S15	4741	(plural or multiple or seperate) with (profile or attribute or parameter) with (memory)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/05 17:36
S16	2473	S14 and S15	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/05 17:36
S17	20106	(parameter or attribute) with (flash or nand or nor)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/05 17:37
S18	204	S16 and S17	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/05 17:37
S19	181	S18 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:37
S20	10	S19 and (page near3 size)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:38
S21	28	("4309754" | "4633437" | "4683534" | "4716527" | "5113369" | "5369754" | "5423009" | "5537624" | "5537659" | "5594874" | "5761456" | "5768560" | "5778413" | "5911053" | "6016270" | "6101565" | "6202140" | "6235554" | "6298426" | "6381664" | "6442076" | "6472747" | "6605875" | "6618790" | "6657899" | "6658508" | "6721840" | "7146510").PN. OR ("8200879").URPN.	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/12/06 12:54
S25	1	("6,430,663").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/12/11 15:23
S26	1	("5913215").PN.	US-PGPUB;	OR	OFF	2012/12/13

			USPAT; USOCR			10:22
S27	113091	(hybrid or heterogenous or different) near3 memory	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:03
S28	26	S27 and (DRAM same NAND same NOR same battery)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:03
S29	13	S28 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:03
S30	299	partial page program$4	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:48
S31	192	S27 and S30	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:48
S32	13	S29 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:48
S33	165	S31 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:48
S34	53823	(short$3 or shorten$3 or truncat$3) near3 (burst or transmission)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:50
S35	0	S33 and S34	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:50
S36	0	S30 and S34	US-PGPUB; USPAT; USOCR; EPO;	ADJ	OFF	2012/12/13 11:50

			DERWENT; IBM_TDB			
S37	20	S30 and burst	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 12:26
S38	14	S37 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 12:26
S39	92	partial page with (size or attribute)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 12:29
S40	6	S33 and S39	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 12:29
S41	198032	(profile or attribute or parameter) with (memory)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/13 12:32
S42	54	S33 and S41	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/13 12:32
S43	1	("5860107").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/12/13 13:20
S44	11735	(short$3 or shorten$3 or truncat$3) near3 (burst)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 15:18
S45	141	((multiple or plural or series) near3 (burst)) with (remaining or remainder or additional)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 15:19
S46	26	S44 and S45	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 15:20
S47	24	S46 and @ad<"20100904"	US-PGPUB;	ADJ	OFF	2012/12/13

			USPAT; USOCR; EPO; DERWENT; IBM_TDB			15:20
S48	135	S45 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 15:29
S49	1	("20060184723").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/12/13 17:13
S50	110530	(writ$3 or program$4) near3 block	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:33
S51	6832	(711/103).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/12/13 19:34
S52	3586	S50 and S51	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:34
S53	19	(writ$3 or program$4) near3 multiple blocks with (instruction or command)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:45
S54	299	(writ$3 or program$4) near3 multiple blocks	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:52
S55	44	S51 and S54	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:52
S57	37	S55 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:52
S58	285682	(flash or memory) near3 controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:50
S59	6008	(flash or memory) near3 interface with	US-PGPUB;	ADJ	OFF	2012/12/14

		(bus near3 (controller or master))	USPAT; USOCR; EPO; DERWENT; IBM_TDB			12:51
S60	5308	S58 and S59	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:51
S61	10796	fifo with input with output	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:52
S62	101	S60 and S61	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:52
S63	4117	fifo with (slots or entries)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:53
S64	4	S62 and S63	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:53
S65	99	S62 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 13:00
S66	113091	(hybrid or heterogenous or different) near3 memory	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 13:15
S67	790	S60 and S66	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 13:15
S68	18560	(fifo or queue) with input with output	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 13:16
S69	42	S67 and S68	US-PGPUB;	ADJ	OFF	2012/12/14

			USPAT; USOCR; EPO; DERWENT; IBM_TDB			13:16
S70	41	S69 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 13:16
S71	134	(acknowledg$3 or acknoweledgement or ack) with (bus near3 (controller or master)) with CPU	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:13
S72	5308	S58 and S59	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:13
S73	10	S59 and S71	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:14
S74	10	S73 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:14
S75	477	(status or complet$3) with (bus near3 (controller or master)) with CPU	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:21
S76	43	S71 and S75	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:21
S77	43	S76 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:21
S78	58	(acknowledg$3 or acknoweledgement or ack) with (memory near3 (controller)) with CPU	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:24
S79	57	S78 and @ad<"20100904"	US-PGPUB;	ADJ	OFF	2012/12/14

			USPAT; USOCR; EPO; DERWENT; IBM_TDB			15:25
S80	1016	(status or complet$3 or error) with (memory near3 (controller)) with CPU	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:25
S81	11	S79 and S80	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:25
S82	12083	(short$3 or shorten$3 or truncat$3) near3 (burst)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2013/05/06 16:15
S83	143	((multiple or plural or series) near3 (burst)) with (remaining or remainder or additional)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2013/05/06 16:15
S84	26	S82 and S83	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2013/05/06 16:15
S85	24	S84 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2013/05/06 16:15
S86	1	("8200879").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/05/06 16:18
S87	203091	(memory or device) near3 (parameter or attribute)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2013/05/06 17:45
S88	5067	(plural or multiple or seperate) with (profile or attribute or parameter) with (memory)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2013/05/06 17:45
S89	2613	S87 and S88	US-PGPUB; USPAT; USOCR; EPO;	ADJ	ON	2013/05/06 17:45

			DERWENT; IBM_TDB			
S90	21098	(parameter or attribute) with (flash or nand or nor)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2013/05/06 17:45
S91	222	S89 and S90	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2013/05/06 17:45
S92	185	S91 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2013/05/06 17:45

5/7/2013 4:52:16 PM
C:\Users\jrutz\Documents\EAST\Workspaces\12876113.wsp

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12876113	BRUCE ET AL.
	Examiner	**Art Unit**
	JARED RUTZ	2187

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/14/2012	05/07/2013							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
	8	✓	✓							
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	35	✓	✓							
	36	✓	✓							

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	Examiner	**Art Unit**
	JARED RUTZ	2187

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
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☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/14/2012	05/07/2013							
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	38	✓	✓							
	39	✓	✓							
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	71	✓	✓							
	72	✓	✓							

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	Examiner	**Art Unit**
	JARED RUTZ	2187

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/14/2012	05/07/2013							
	73	✓	✓							
	74	✓	✓							
	75	✓	✓							
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	90	✓	✓							
	91	✓	✓							
	92	✓	✓							
	93	✓	✓							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12876113	BRUCE ET AL.
	Examiner	Art Unit
	JARED RUTZ	2187

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
inventor search in EAST	12/14/2012	jir
text search in EAST, see search history	12/14/2012	jir
internet search using google.com	12/14/2012	jir
updated search in EAST	5/7/2013	jir

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

OPAP
AUG 19 2013
AKIMA-9
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Ricardo H. Bruce, et al.	Confirmation No.: 1607
Serial No.: 12/876,113	Examiner: Jared Ian Rutz Ph: 571-272-5535
Filing Date: Sept. 4, 2010	Art Unit: 2187
Title: Multi-Profile Memory Controller For Computing Devices	Atty. Docket No.: 6005.042

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO FINAL OFFICE ACTION AND AMENDMENT

Sir:

The following is in response to the final office action mailed on 14 May 2013.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 24 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising:

addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

using attributes from said first and second device profiles.

2. (original) The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device.

3. (original) The method of claim 1, wherein said difference between said first and second device profiles includes different attributes; and said addressing said first memory location is made in response to a first memory transaction request; and

further including addressing said second memory location.

4. (original) The method of claim 1, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes.

5. (original) The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

6. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute values.

7. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute types.

8. (original) The method of claim 5, wherein said shared attributes include a memory device type attribute.

9. (original) The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

10. (original) The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

11. (original) The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

12. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

13. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of attributes that differs in value from a second page size attribute from said second set of attributes.

14. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes.

15. (original) The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device, and said second memory device interface attribute corresponds to a DRAM device interface.

16. (original) The method of claim 2, wherein said using attributes from said first and second device profile further includes using a first partial page size attribute from said first set of attributes that differs in value from a second partial page size attribute from said second set of attributes.

17. (original) The method of claim 16:

said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute; and

further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute.

18. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

19. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a NAND flash memory device and said second memory device type attribute corresponds to a NOR flash memory device.

20. (original) The method of claim 2, further including:

using an address corresponding to a memory location from said first memory device and transferring a first data set, and

using an address corresponding to a memory location from said second memory device and transferring a second data set.

21. (original) The method of claim 20, wherein:

said first set of attributes includes a first page size attribute, and said first data set includes a first data set size; and

if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size.

22. (original) The method of claim 20, wherein:

said second set of attributes includes a second page size attribute, and said second data set includes a second data set size; and

if said second data set size is greater than said second page size attribute, said transferring said second data set includes:

performing a set of write operations on said second memory device that includes using a second transfer size equal to said second page size attribute until a remaining portion of said second data set that has not yet been written to said second device is less than said second page size attribute, and

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

23. (currently amended) The method of claim 20, wherein:

said first set of attributes includes a page size attribute and a block size attribute;

said first data set includes a first data set size;

if said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes:

performing a set of write operations on said first memory device that includes using a second transfer size

equal to said page size attribute until a remaining portion of said first data set that has not yet been written to said first device is less than said page size attribute,

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size[[;]].

24. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes:

performing respective write operations on said first and second memory devices by at least using a transfer size at least equal to a partial page size attribute from said first set of attributes and performing at least one write operation on said second memory device by at least using a transfer size at least equal to a partial page size attribute value from said second set of attributes; and

said attribute difference includes different attribute values of said first and second partial page size attributes.

25. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size attribute of said first memory device.

26. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a block size attribute value that corresponds to a block size attribute of said first memory device.

27. (original) The method of claim 26, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

28. (original) The method of claim 2, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

29. (previously presented) A non-transitory computer readable medium comprising computer executable instructions adapted to cause a method of performing memory transactions on a first memory location and a second memory location, said method comprising:

addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory device, and said second

device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles; and

using attributes from said first and second device profiles.

30. (original) The computer readable medium of claim 29, wherein:

said first memory location is part of a memory space associated with a first memory device;

said second memory location is part of a memory space associated with a second memory device; and

said first and second memory devices comprise at least a portion of a memory store.

31. (previously presented) The computer readable medium of claim 29, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of a first memory device and a block size value of a second memory device.

32. (previously presented) The computer readable medium of claim 30, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

33. (original) The computer readable medium of claim 29, wherein said first memory location is located in a first

memory device and said second memory location is located in a second memory device.

34. (original) The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes.

35. (previously presented) The computer readable medium of claim 29, wherein said addressing further includes:

said first and second device profiles having at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

36. (original) The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

37. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values.

38. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types.

39. (original) The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute.

40. (original) The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

41. (original) The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

42. (original) The computer readable medium of claim 36, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

43. (original) The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes.

44. (original) The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device.

45. (previously presented) A memory controller for performing memory transactions, said memory controller comprising:

a means for addressing a first memory location, said first memory location and a second memory location are

respectively associated with a first device profile and a second device profile;

wherein said means for addressing includes an interface controller means for processing memory transaction requests;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said means for addressing uses attributes from said first and second device profiles.

46. (original) The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

47. (original) The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

48. (original) The memory controller of claim 46, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said use of said attributes from said first and second device profiles by said means for addressing includes using said different attribute qualifiers for said shared attributes.

49. (original) The memory controller of claim 46, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

50. (previously presented) The memory controller of claim 45, wherein said means for addressing further includes a means for addressing said second memory location.

51. (original) The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

52. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values.

53. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types.

54. (original) The memory controller of claim 51, wherein said shared attributes include a memory device type attribute.

55. (original) The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

56. (original) The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

57. (original) The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

58. (original) The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device.

59. (original) A memory controller comprising:

an interface controller coupled to a memory device interface and an IO device interface;

said interface controller disposed to perform a memory transaction by addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile;

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63. (original) The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction, coordinates the operation of said memory device interface, and manages the transfer of memory transaction data between said IO device interface and said memory device interface through a data path.

64. (previously presented) The memory controller of claim 59, further including a buffer comprising a FIFO and a data path that includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface.

65. (original) The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots.

66. (original) The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a plurality of queue slots that buffer data from said IO device interface to said memory device interface.

67. (original) The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from said memory device interface to said IO device interface.

68. (previously presented) The memory controller of claim 59, further including a second memory bus controller

said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said addressing of said first memory location includes using said attributes from said first device profile.

60. (original) The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile.

61. (previously presented) The memory controller of claim 59, wherein said interface controller includes:

a main control device coupled to said memory device interface and to a data path;

a first memory bus controller coupled to said control device and said memory device interface; and

an IO bus controller coupled to said IO device interface and said control device.

62. (previously presented) The memory controller of claim 61, wherein said IO bus controller is disposed to respond to a memory transaction request by acknowledging said request and providing status to said main control device.

coupled to a main control device and said memory device interface.

69. (original) The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes.

70. (original) The memory controller of claim 59, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

71. (original) The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

72. (original) The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute.

73. (original) The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values.

74. (original) The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values.

75. (original) The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type.

76. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values.

77. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types.

78. (original) The memory controller of claim 71, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

79. (original) The memory controller of claim 71, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

80. (original) An electronic storage device, comprising:

a memory controller disposed to address a first memory location and a second memory location which are

respectively associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said memory controller using attributes from said first and second device profiles.

81. (original) The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

82. (original) The electronic storage device of claim 80, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

83. (previously presented) The electronic storage device of claim 80, said memory controller further disposed to:

perform a write operation on said first memory device, if a memory transaction request is associated with a write request;

perform a read operation on said first memory device, if said memory transaction request is associated with a read request; and

wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using said second device profile in response to receiving a second memory transaction request.

84. (original) The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

85. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values.

86. (original) The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute.

87. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types.

88. (original) The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said shared attributes.

89. (original) The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device.

90. (original) The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

91. (original) The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

92. (original) The electronic storage device of claim 84, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

93. (original) The electronic storage device of claim 80, wherein said memory controller is further adapted to:

use a first partial page size attribute by performing a write operation on said first memory device and using a transfer size at least equal to said partial page size attribute; and

use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute.

94. (previously presented) The method of claim 1, wherein the first memory location and the second memory location are addressable memory locations.

95. (previously presented) The memory controller of claim 45, wherein the first memory location and the second memory location are addressable memory locations.

96. (previously presented) The memory controller of claim 59, wherein the first memory location and the second memory location are addressable memory locations.

97. (previously presented) The electronic device of claim 80, wherein the first memory location and the second memory location are addressable memory locations.

REMARKS/ARGUMENTS

Claim Rejections

35 USC 102

Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-97

Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-97 are rejected under 35 U.S.C. 102(e) as allegedly being anticipated by US 8,200,879 to Falik et al. ("Falik"). Claims 1, 45, 59, and 80 are independent claims. Applicants respectfully traverse this rejection.

Applicants respectfully contend that independent claim 1 recites the following limitations that are not disclosed within the four corners of Falik: addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile; said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and using attributes from said first and second device profiles.

Falik discloses characteristics of each logical section 57 (Falik: column 15, line 63), and these logical sections contain logical blocks (and these logical blocks are Main Block 51 and Information Block 52) (Falik: column 14, line 51-56). Therefore, Falik discloses logical sections as associated with these characteristics.

However, these logical blocks in these logical sections are for storing data used by any application in a Main Device, or for storing auxiliary data (e.g., configuration data or control data) used by the Main Device or application programs (Falik: column 14, lines 21-31 and lines 51-58). Therefore, these logical blocks (and logical sections that contain these logical blocks) are not addressable sections. Therefore, Falik does not disclose these logical sections as memory locations that are addressed. Accordingly, Falik does not disclose all the limitations of claim 1.

Falik further discloses the device and status control register (Falik: Figure 5A) which provides status and control information for an entire memory device (Falik: column 19, lines 4-8). Falik also discloses a flash device capabilities register (Falik: Figure 5B) that provides capabilities and properties information on the same entire memory device (Falik: column 19, lines 49-53). Therefore, these registers contain information directed to the same entire memory device and not directed to different memory locations. These registers do not contain a first set of attributes of a first memory location and also do not contain a second set of attributes of a second memory location.

Based on at least the above discussion, Falik does not disclose and does not teach "addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile" and "said first memory location and a second memory location respectively

associated with a first device profile and a second device profile; said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles" as required in claim 1.

Since Falik does not disclose and does not teach all the limitations of claim 1, claim 1 is not anticipated by the cited reference. Claim 1 is otherwise allowable.

Claims 2-14, 20, 21, and 25 depend from allowable claim 1; as such, they are also allowable for at least the same reasons as claim 1.

The withdrawal of the rejections to claims 1-14, 20, 21, 25 and 94 is respectfully requested.

Independent claims 45, 59, and 80 recite at least some limitations similar to that as claim 1. Although claims 45, 59, and 80 are different, Applicants respectfully argue that in this case the above arguments regarding the patentability of claim 1 apply with equal force with respect to claims 45, 59, and 80. Since Falik does not disclose and does not teach all the limitations of claims 45, 59, and 80, claims 45, 59, and 80 are not anticipated by the cited reference. Claims 45, 59, and 80 are otherwise allowable.

Claims 46-58 and 95 depend from allowable claim 45; as such, they are also allowable for at least the same reasons as claim 45.

Claims 60, 69-79, and 96 depend from allowable claim 59; as such, they are also allowable for at least the same reasons as claim 59.

Claims 81-92 and 97 depend from allowable claim 80; as such, they are also allowable for at least the same reasons as claim 80.

The withdrawal of the rejection to claims 45-60, 69-92, and 95-97 is respectfully requested.

Claims 15, 18, and 19

Claims 15, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 7,330,954 to Nangle.

Claims 15, 18, and 19 depend from allowable claim 1; as such, they are also allowable for at least the same reasons a claim 1.

The withdrawal of the rejection of claims 15, 18, and 19 is respectfully requested.

Claims 16, 17, 22-24, and 93

Claims 16, 17, 22-24, and 93 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 2006/0184723 to Sinclair.

Claims 16, 17, and 22-24 depend from allowable claim 1; as such, they are also allowable for at least the same reasons a claim 1.

Claim 93 depends from allowable claim 80; as such, claim 93 is also allowable for at least the same reasons a claim 1.

The withdrawal of the rejection of claims 16, 17, 22-24, and 93 is respectfully requested.

Claims 26-28

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 6961,805 to Lakhani et al.

Claims 26-28 depend from allowable claim 1; as such, they are also allowable for at least the same reasons a claim 1.

The withdrawal of the rejection of claims 26-28 is respectfully requested.

Claims 29-44

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 5,913,215 to Rubinstein.

The Office admits that Falik does not expressly teach that the methods may be implemented using a computer readable medium comprising computer executable instructions. In order to supply the missing limitations, the Office combines Falik with Rubinstein. The Office argues it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a computer readable medium comprising computer executable instructions (Office Action: page 44). The Applicants respectfully disagree with the assertions of the Office.

Independent claim 29 recite at least some limitations similar to that as claim 1. Although claim 29 is different, Applicants respectfully argue that in this case

the above arguments regarding the patentability of claim 1 apply with equal force with respect to claim 29.

Since Falik and Rubinstein, considered individually or in combination, do not disclose and does not teach all the limitations of claim 29, claim 29 is not rendered obvious in view the cited references. Claim 29 is otherwise allowable.

Claims 30-44 depend from allowable claim 29; as such, they are also allowable for at least the same reasons a claim 29.

The withdrawal of the rejection of claims 29-44 is respectfully requested.

Claims 61 and 64-68

Claims 61 and 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 2001/0010066 to Chin et al.

Claims 61 and 64-68 depend from allowable claim 59; as such, they are also allowable for at least the same reasons a claim 59.

The withdrawal of the rejection of claims 61 and 64-68 is respectfully requested.

Claims 62 and 63

Claims 61 and 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of Chin as applied to claim 61 above, and further in view of US 2007/0174506 to Tsuruta.

Claims 62 and 63 depend from allowable claim 59; as such, they are also allowable for at least the same reasons a claim 59.

The withdrawal of the rejection of claims 62 and 63 is respectfully requested.

Applicants respectfully request the allowance of the claims.

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, the Applicants are not conceding in this application that previously pending claims are not patentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application.

Conclusion

Claims 1-97 herein are allowable, and a timely Notice of Allowance is respectfully requested.

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (408) 256-0244.

Date: August 14, 2013

Respectfully submitted,

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US006102353A

United States Patent [19]

Dichter

[11] Patent Number: 6,102,353

[45] Date of Patent: Aug. 15, 2000

[54] **TILT MOUNTING**

[75] Inventor: **Carl R. Dichter**, Chandler, Ariz.

[73] Assignee: **Intel Corporation**, Santa Clara, Calif.

[21] Appl. No.: **09/084,071**

[22] Filed: **May 22, 1998**

[51] **Int. Cl.**[7] **A47G 29/00**

[52] **U.S. Cl.** **248/371**; 108/5; 248/454

[58] **Field of Search** 248/371, 372.1, 248/396, 397, 917, 919, 920, 923, 160, 161, 178.1, 454; 108/1, 5, 138; 297/423.41, 423.39

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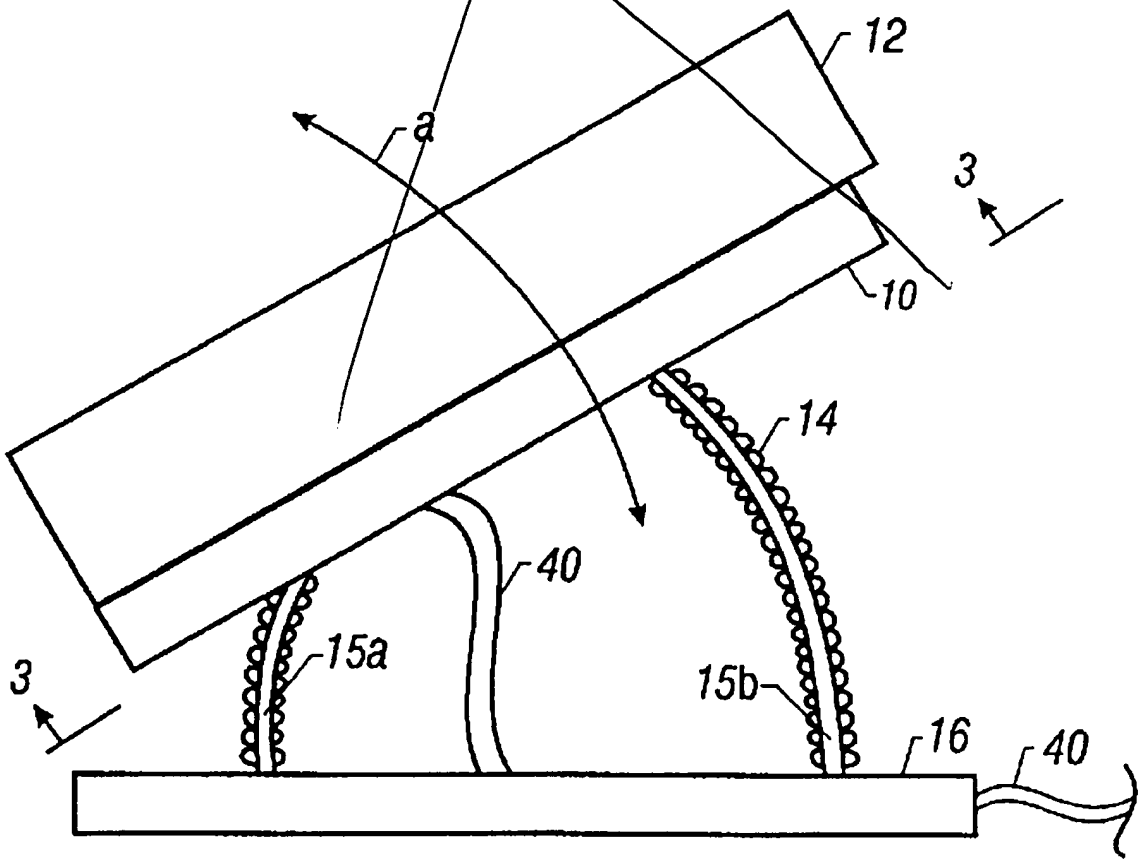
Primary Examiner—Anita M. King

Attorney, Agent, or Firm—Trop, Pruner & Hu, P.C.

[57] **ABSTRACT**

An object may be adjustably mounted with respect to a base on one or more plastic straps which extend between the base and the object. The object may be translated with respect to the straps which may be fixed so as to vary the extension of the strap or straps into the object. In this way, the position of the object may be rotationally adjusted with respect to the base and translated towards and away form the base as well. This arrangement may be particularly suitable for mounting flat screen displays for computer systems in a low profile, low cost arrangement that allows multiple degrees of freedom of movement.

32 Claims, 3 Drawing Sheets



CONTAINMENT HIERARCHY GRAPH 320

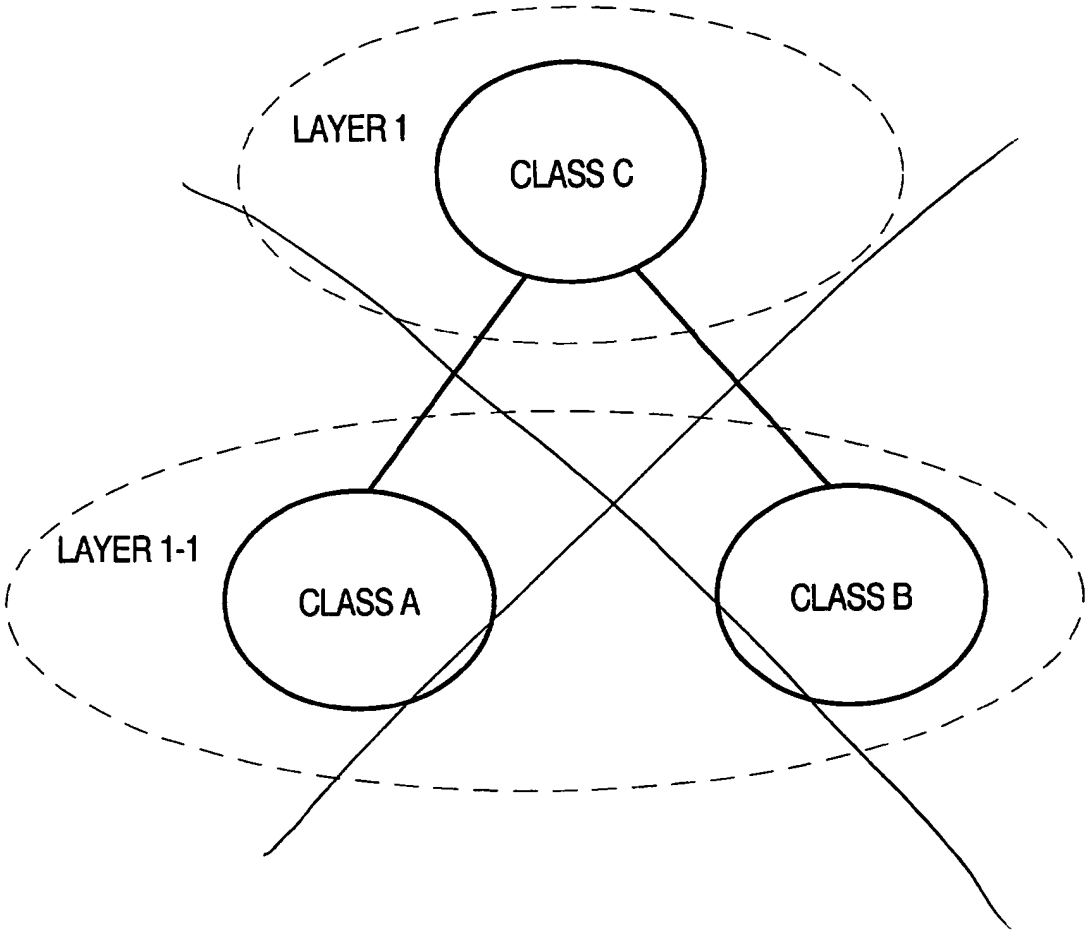
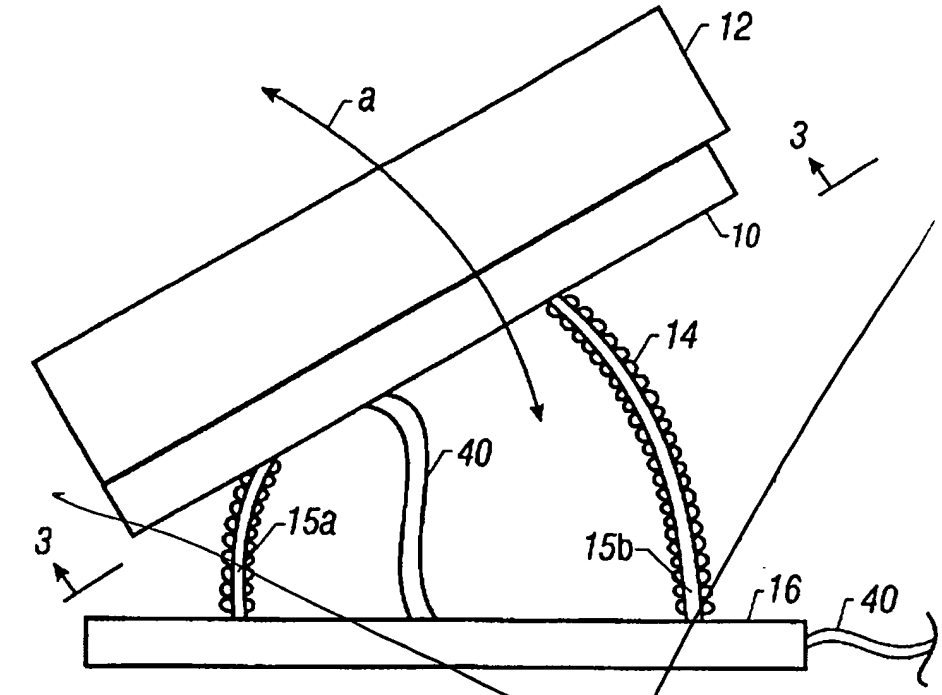


FIG. 3B

Figure 1



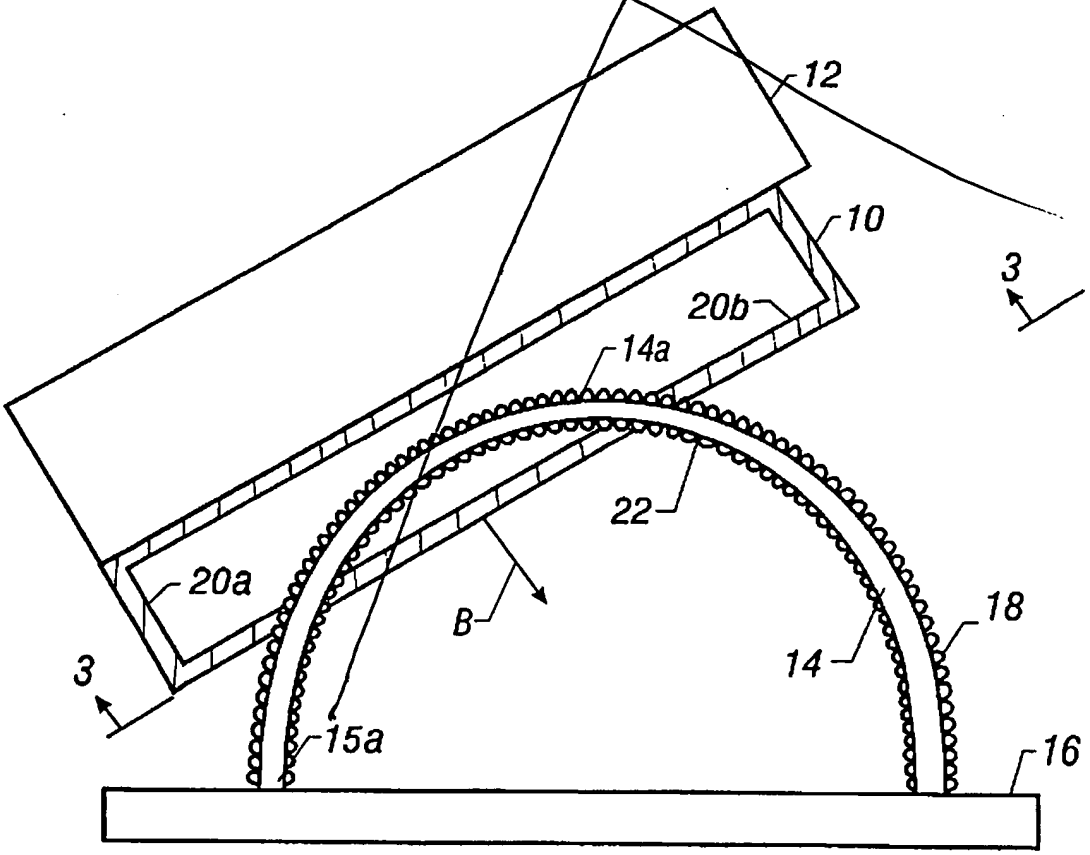


Figure 2

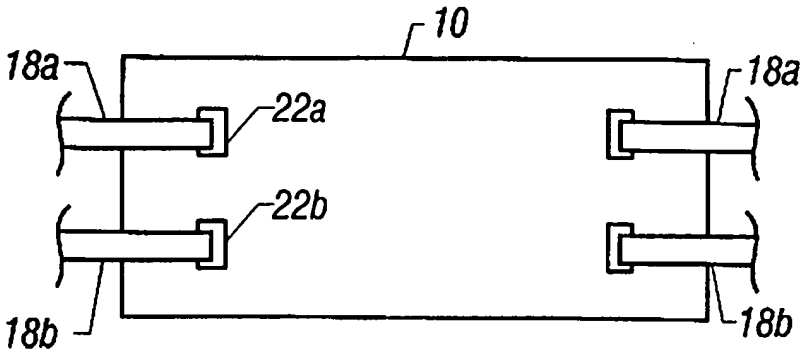


Figure 3

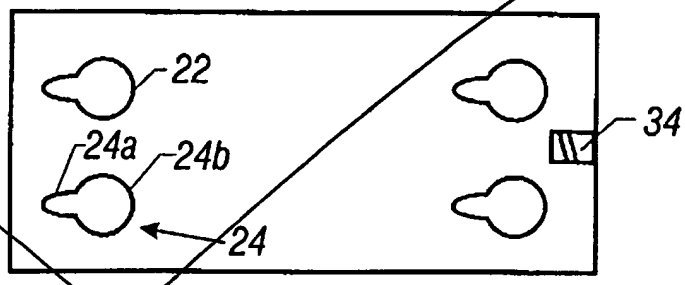


Figure 4

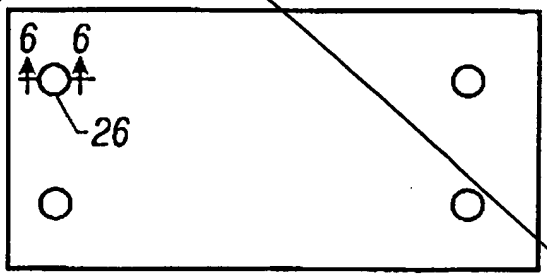


Figure 5

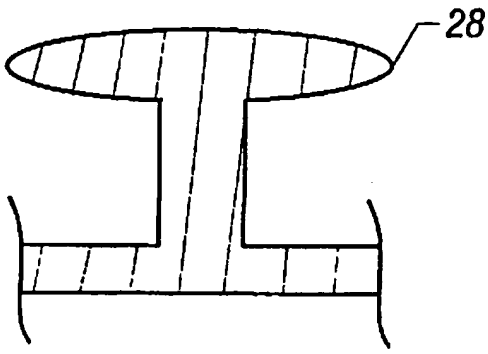


Figure 6

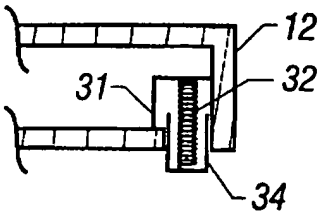


Figure 7a

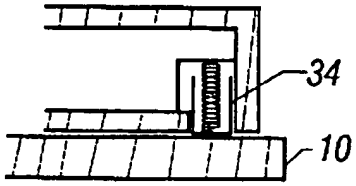


Figure 7b

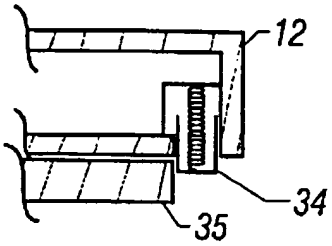


Figure 7c

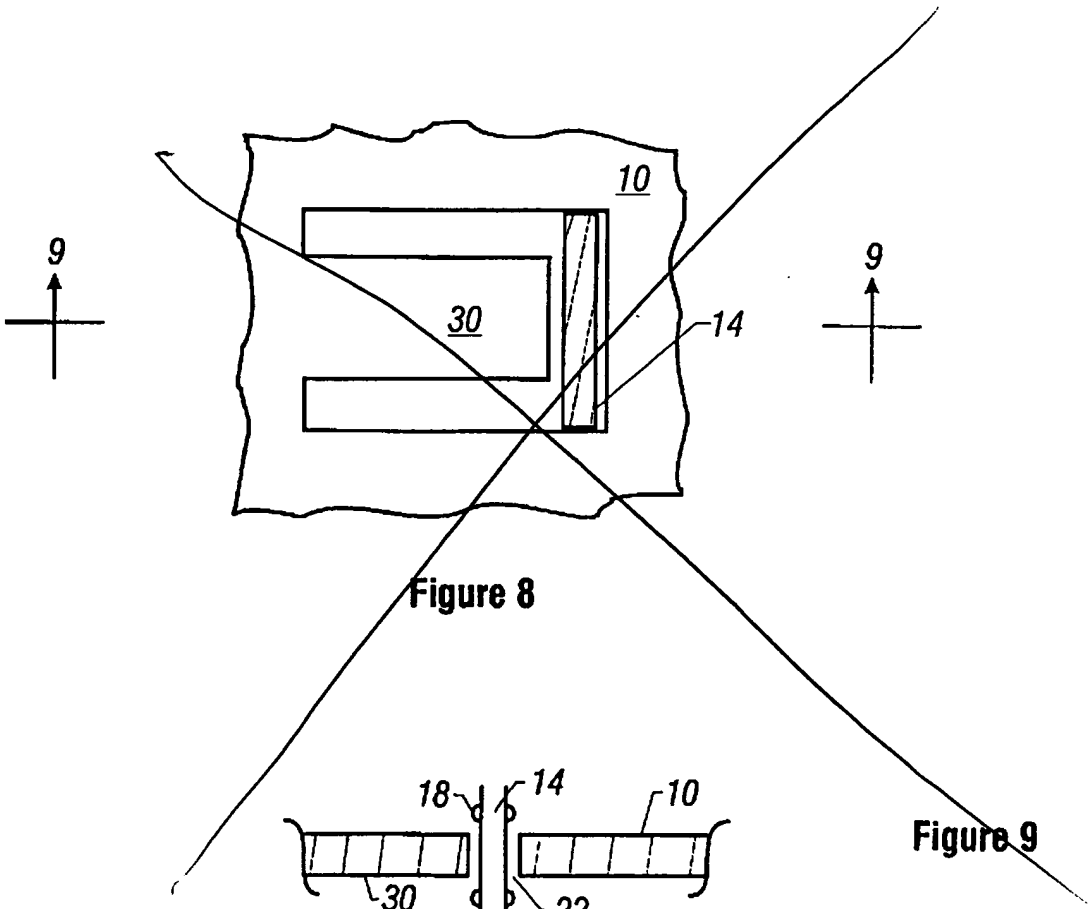


Figure 8

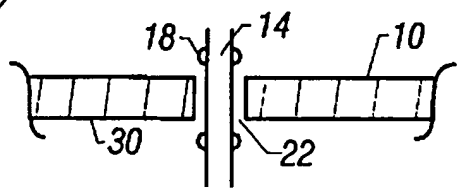


Figure 9

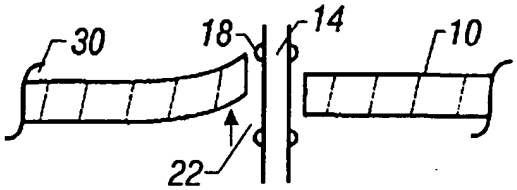


Figure 10

CONTAINMENT HIERARCHY GRAPH 310

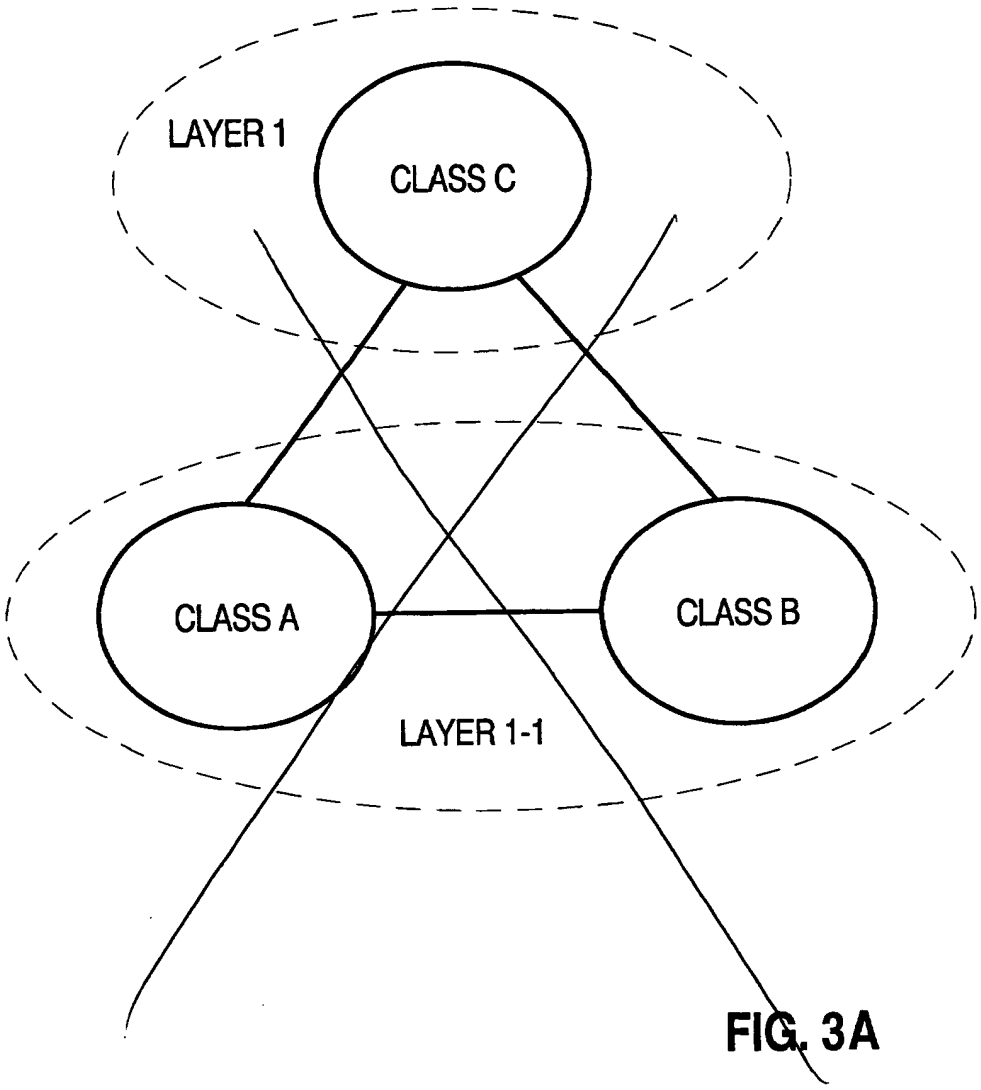
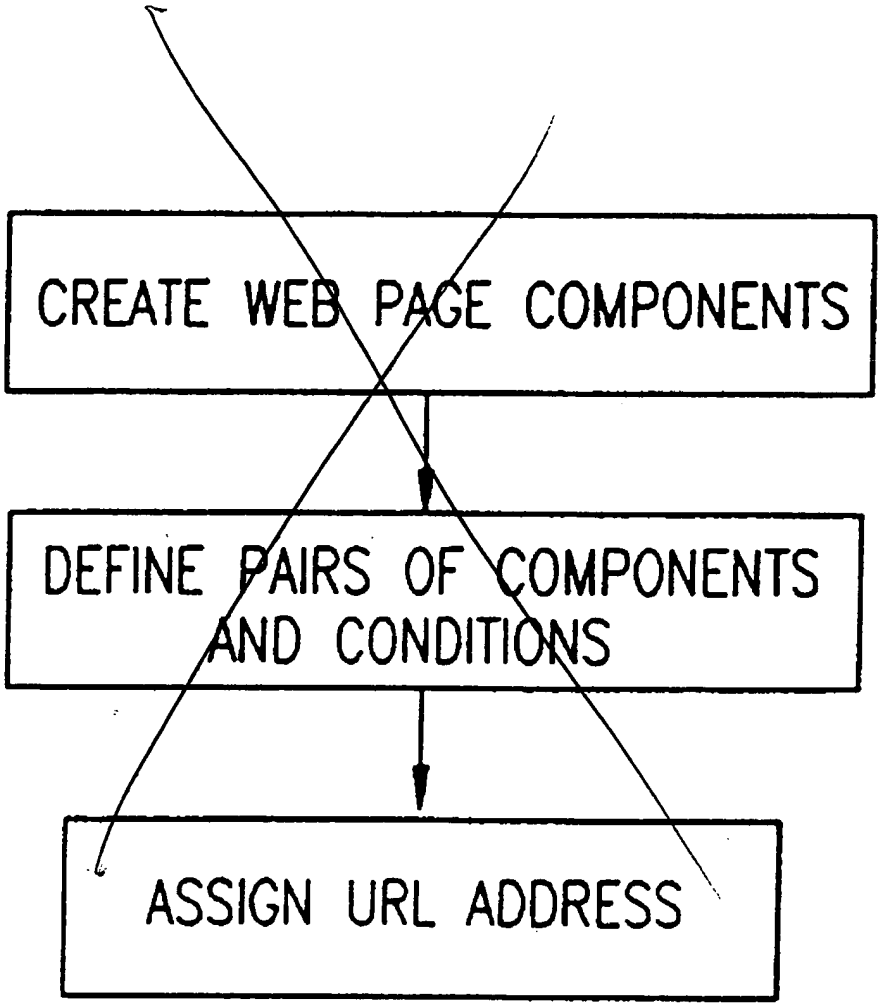


FIG. 3A

FIG. 7


CREATE WEB PAGE COMPONENTS
DEFINE PAIRS OF COMPONENTS AND CONDITIONS
ASSIGN URL ADDRESS

US006434343B1

(12) **United States Patent**
Kobayashi et al.

(10) **Patent No.: US 6,434,343 B1**
(45) **Date of Patent: Aug. 13, 2002**

(54) **COMPOSITE MACHINE, SERVER, COMPOSITE MACHINE-SERVER SYSTEM, AND PROGRAM RECORDING MEDIUM**

(75) Inventors: **Sumitake Kobayashi**; **Keiji Ishiguro**; **Ken Murata**; **Takashi Kawasaki**, all of Kawasaki (JP)

(73) Assignee: **Fujitsu Limited**, Kawasaki (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/100,320**

(22) Filed: **Jun. 19, 1998**

(30) **Foreign Application Priority Data**

Jan. 8, 1998 (JP) 10-002642

(51) **Int. Cl.**[7] **G03G 15/00**; G06F 15/16

(52) **U.S. Cl.** **399/8**; 399/82; 709/201; 709/224

(58) **Field of Search** 709/203, 206, 709/202, 224, 207, 201; 399/83, 82, 87, 10, 8, 11

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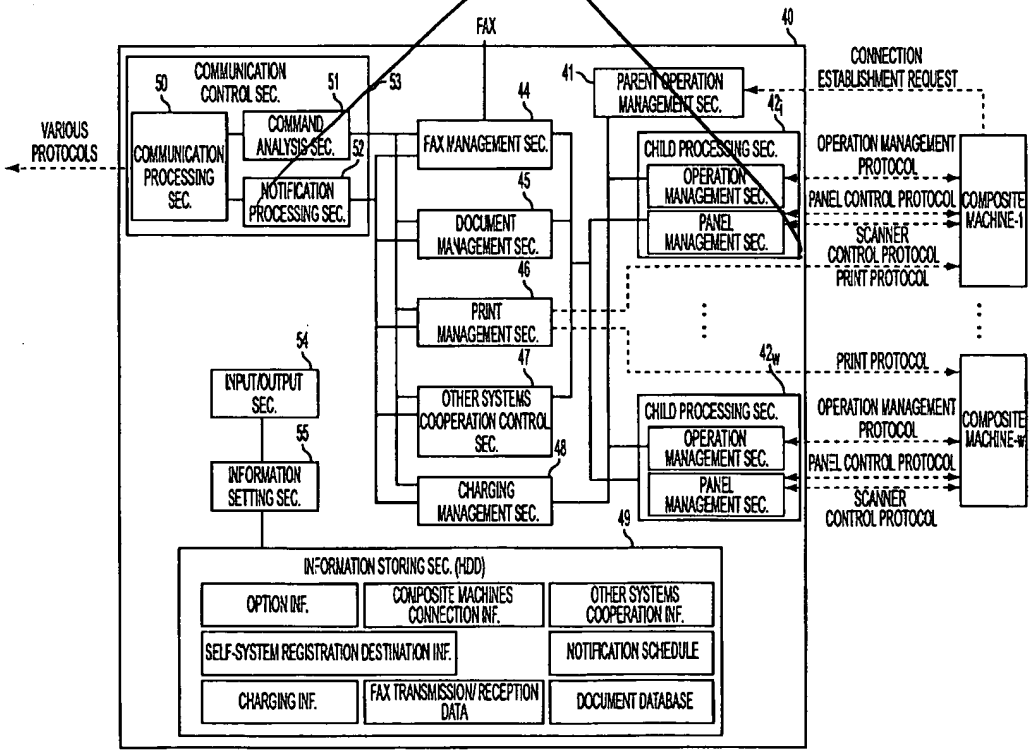
* cited by examiner

Primary Examiner—Mark H. Rinehart
Assistant Examiner—Paul Kang
(74) *Attorney, Agent, or Firm*—Staas & Halsey LLP

(57) **ABSTRACT**

It is intended to provide a composite machine-server system which can handle electronic documents more efficiently and can be realized at a low cost. A composite machine-server system is constructed by connecting a plurality of composite machines and a server to a network. Each of the composite machines has a second-kind process function of executing a second-kind process without cooperating with the server when requested to execute the second-kind process, as well as a first-kind process function of sending, when requested to execute a first-kind process, an electronic document necessary for execution of the first-kind process to the server and requesting the server to execute the first-kind process on the electronic document. The server has a function of executing first-kind processes whose execution is requested by the composite machines.

6 Claims, 26 Drawing Sheets



STABILIZED FLAT PANEL TOUCH MONITOR

Some embodiments of the present invention are shown in commonly assigned co-pending U.S. Design Patent Application filed even date herewith, application number unknown, our docket 57312US002, entitled FLAT PANEL MONITOR STAND, which is hereby incorporated herein by reference in its entirety.

This invention relates to monitors and monitor stands. The invention more particularly relates to a monitor stand for a monitor with touch input capabilities.

BACKGROUND

Monitors, particularly desktop computer monitors, typically include a stand with a base unit and an attachment feature such as a monitor stand to secure the monitor to the base. Known monitor stands often implement a pivoting feature that allows the monitor to pivot relative to the base unit to adjust the direction in which a screen of the monitor faces. For example, a vertical pivoting feature allows the monitor to move up and down between a generally upright position, typically perpendicular to the base unit, and a position angled relative to the upright position.

One drawback of known monitor stands is the limited angle through which the monitor can rotate. For example, many monitors rotate back from an upright position only about 30 degrees, and most monitors have an even more limited forward rotation from upright, for example, 0 to 15 degrees. A limited backward rotation makes viewing the monitor from above, as required by some monitor applications, very difficult or impossible. However, a limited rotation of the monitor can provide stability of the monitor given the design of known monitors and monitor stands.

Another disadvantage of known monitors relates to the stability of monitors with touch sensor capabilities, whether the touch sensor capabilities are built into the monitor when manufactured or added to the monitor after manufacture. Monitors with touch sensor capabilities inherently require touch forces to activate the touch sensors associated with the monitor screen. Touch inputs can create various stability issues in the monitor and monitor stand depending on the location of the touch on the screen, the direction in which the touch is applied to the screen, and the force with which the touch is applied. Touch inputs applied to the monitor screen when the monitor is at a rotated position can create additional stability issues. Also, repetitious touches and single touches at certain locations may cause vibrations and resonant oscillations that affect stability and usability of the monitor. A monitor and monitor stand that address these and other disadvantages of known monitor stands would be an advance in the art.

SUMMARY OF THE INVENTION

Generally, the present invention relates to a monitor with touch sensor capabilities having enhanced stability features. One embodiment of the invention is a monitor with touch input capabilities that includes a monitor panel, a base, an upper support member, and a lower support member. The upper support member is secured to the monitor panel at first and second locations, and is further secured to the base. The lower support member is secured to the panel at third and fourth locations that are lower relative to the first and second positions. The lower support member is also secured to the base. In some embodiments of the invention, the upper support member is adjustable to allow the monitor panel to rotate about the lower support member from an upright position to an angled position relative to the base.

The invention also provides for a method of pivotally mounting a monitor to a monitor stand. The monitor stand includes a base member, an upper support member with first and second portions that adjustably engage each other, and a lower support member. According to the method, the first portion of the upper support member is secured to the monitor at first and second locations, and the second portion of the upper support member is secured to the monitor at third and fourth locations. In a further step, the monitor pivots about the lower support member by adjusting the first and second upper support members relative to each other.

The above summary of the present invention is not intended to describe each disclosed embodiment or every implementation of the present invention. The Figures and the detailed description that follow more particularly exemplify these embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be more completely understood in consideration of the following detailed description of various embodiments of the invention in connection with the accompanying drawings, wherein like numerals represent like parts throughout several views, in which:

FIG. **1** is a rear perspective view of a monitor assembly according to the invention;

FIG. **2** is a rear perspective view of an alternative embodiment of a monitor assembly according to the invention;

FIG. **3** is a side view of the monitor assembly of FIG. **2**;

FIG. **4** is a rear perspective view of another alternative embodiment of a monitor assembly according to the invention;

FIG. **5** is a rear perspective view of another alternative embodiment of a monitor assembly according to the invention;

FIG. **6** is a side view of another alternative embodiment of a monitor assembly according to the invention;

FIG. **7** is a rear view of the monitor assembly of FIG. **6**;

FIG. **8** is a rear perspective view of another alternative embodiment of a monitor stand assembly according to the invention; and

FIG. **9** is a rear perspective view of another alternative embodiment of a monitor stand assembly according to the invention.

While the invention is amenable to various modifications in alternative forms, the specifics thereof have been shown by way of example in the drawings and will be described in detail. It should be understood, however, that the intention is not to limit the invention of the particular embodiments described. On the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention is generally applicable to monitors with increased stability. The invention is particularly related to flat panel monitor assemblies having touch screens with touch sensor capability. The monitor assembly is stable in an upright position when touch inputs are entered at any location on the touch screen and when successive touches are entered on the touch screen. The monitor assembly also maintains stability when touch inputs are entered on the

touch screen when the monitor panel is tilted at angles relative to a base portion of the monitor assembly.

"Touch inputs" as used herein refers to a touch to a touch screen that generates a touch signal capable of recognition by a touch system. A touch signal may be generated by a proximity touch input such that the signal is created without actually touching the touch screen. However, it is most common that a touch signal is created with a physical touch input to the touch screen. Typically, the amount of force required to induce a touch signal in a touch sensor ranges from about 3 to 10 oz. (85 to 280 g) over the area of an average fingertip. The average amount of force actually used to generate a touch signal in normal use of touch screens is about 10 to 20 oz. (255 to 510 g). Depending on the application, the user, and other variables, the touch forces that can be expected to be applied can range from as little as 3 oz. to as much as 5 lbs. (85 g to 2.3 kg) over the area provided by a finger tip. The present invention provides monitor assemblies that are stable within the normal or expected ranges of touch forces given the anticipated use of the monitor, and may be stable when even greater forces are applied to the touch screen of the monitor panel. An upper limit on the amount of force that can be applied to the touch screen to generate a touch signal while maintaining stability in the monitor assembly may the point at which the monitor begins to tip over, slide on its support surface, or twist.

For purposes of this application, it will be assumed that a touch input to a touch screen of a monitor panel may be made at any location on an active area of the touch screen. In many cases, the active area of the touch screen covers the viewable area of the monitor panel, or major portion thereof, which in turn often covers the majority of the surface area of the front side of the monitor panel. It is further assumed for purposes of this application that a touch input may be made at or near the top and bottom corners and the top center of the front surface of a monitor panel to which the touch screen is mounted.

Further, when a monitor panel is described herein as being in an "upright" position, the monitor is assumed to be at a generally perpendicular orientation relative to a base of the monitor. Thus, when the monitor panel is described as being "angled relative to the monitor base," the orientation of the monitor panel is one other than an "upright" position. The present invention, as described below, addresses the adjustability and stability of a monitor, preferably a flat panel monitor, which utilizes a touch screen for receiving touch inputs.

Now referring to the rear perspective view of FIG. **1**, one example of a monitor assembly **10** of the present invention includes a monitor panel **12**, a monitor base **14**, an upper support member **16**, and a lower support member **18**. Monitor panel **12** is secured to base **14** through the support members at four or more attachment points on the monitor panel to create a four point attachment configuration. A four point attachment configuration is advantageous in many respects over a attachment configuration that use fewer points and that are common in known monitor assemblies. A four point attachment configuration may improve stability of the monitor assembly and reduce vibrations and resonant oscillations in the monitor assembly through improved damping of vibrations.

In the embodiment shown in FIG. **1**, upper and lower support members **16** and **18** are fixed in a particular position on both the monitor panel **12** and monitor base **14**. In alternative embodiments, the attachment position of the upper and lower support members to either the monitor panel **12** or monitor base **14** may be adjustable, movable, or in some way configured to allow the position of monitor panel **12** to be adjusted relative to the position of base **14**.

Monitor panel **12** is a "flat panel" monitor that utilizes technology that requires very little monitor depth (the distance between front and rear surfaces of the monitor panel) for the monitor components. For example, monitor panel **12** may include a liquid crystal display (LCD) screen, a plasma display screen, an organic electroluminescent display screen, or other flat panel electronic displays. The integration of electronic displays with touch screen input devices is known, the specifics of which depend on the type of display and touch device being used. A touch screen device can be a capacitive device, a resistive device, an optical device, a force sensing device, or a surface acoustic wave device, and may include an X-Y electrode grid, force sensors, infrared diodes and sensors, or an array of electrode bars.

Monitor panel **12**, as shown in FIG. **1**, includes a front surface **20** into which a monitor screen is integrated, and a rear panel surface **22** to which the monitor assembly support members are typically secured. Monitor panel **12** may be divided into upper and lower halves **24** and **26** vertically divided by a horizontal centerline A. Monitor panel **12** may also be vertically divided into first and second panel halves **28** and **30** defined by a vertical centerline B. Centerlines A and B generally define four quadrants I, II, III and IV of the monitor panel which may be relevant to the placement of the support members to the monitor panel as it relates to stability of the monitor assembly. In the various embodiments shown, the center lines A and B can be geometric center lines that divide the monitor into symmetric halves, can be weight distribution center lines that divide the monitor into halves of equal weight and/or halves with symmetric centers of gravity, or can divide the monitor into any other suitable configuration that may be meaningful in considering stability.

In this embodiment, monitor panel **12** is generally rectangular-shaped. In other embodiments, monitor panel **12** may have other shapes, for example, circular, hemispherical, triangular, or a shape with five or more sides, so long as the monitor panel **12** is able to integrate a monitor screen with touch input capabilities. In other alternative-shaped embodiments, the monitor panel **12** may still be divided into generally upper and lower halves and first and second halves defined by generally horizontal and vertical centerlines, such as centerlines A and B shown in FIG. **1**.

Monitor base **14** includes a front side **40**, a rear side **42**, a first side **44**, and a second side **46** that define a generally rectangular-shaped member. Monitor base **14** has a length L between front and rear sides **40** and **42**, and a width W measured between first and second sides **44** and **46**. The width and length of base **14** define a footprint of the monitor assembly selected to satisfy stability requirements. For example, the length L between front and rear sides **40** and **42** extends to counterbalance moment and torque forces translated through support members **16** and **18**. Similarly, the width W between first and second sides **44** and **46** extends to counterbalance moment and torque forces, especially those at or near the upper and lower corners of monitor panel **12**.

Width W, as shown in FIG. **1**, can be centered about the vertical centerline B of monitor panel **12** so that the monitor assembly is in balance when in the rest position prior to touch inputs being made to monitor panel **12**. Monitor panel **12** can be positioned relative to base **14** so that a necessary portion of the base length L extends in front of and rearward

of the position of monitor panel **12** so that the monitor assembly is able to reside in balance prior to touch inputs being made to monitor panel **12**. In some embodiments, the height H measured between a generally upper surface **48** and a lower surface **49** of base **14** can be significant. Height H may be relevant when considering how the moment and other forces are translated from a touch input to the monitor panel through the upper and lower support members and into monitor base **14**. For example, in configurations where the ratio of the height H to the length L or the ratio or the height H to the width W is relatively large, H may be a significant factor in determining stability.

In other embodiments, base **14** may have a shape different from the rectangular shape of FIG. **1**. For example, the base width W may vary along base length L. In another embodiment, base **14** may be circular or oval-shaped, the base height H may vary across the base width W and length L, or may have more than four sides, for example, to match a multi-sided shape of the monitor panel **12** in an alternative monitor panel configuration.

In some embodiments, base **14** may include a weighted plate, keyhole plate, or other type of additional feature strategically placed within base **14** to provide for stability and/or security. For example, a weighted plate may be secured to a bottom surface **49** of base **14** so as to be concealed from view while providing additional stability. In other embodiments, a weighted plate or shaped weights may be integrally formed into base **14**, for example, by injection molding base **14** around a metal or metal alloy plate or other shaped weight. In yet further embodiments of base **14**, materials may be added to the bottom surface of base **14** that would create a high friction interface between base **14** and a surface on which the monitor assembly **10** resides, to improve stability of the monitor. For example, a specialized material may be an adhesive or may be shaped in the form of pads, suction cups or the like design, possibly placed at strategic points near or around the periphery of base **14**.

The lower support member **18** includes a first end **50**, a second end **52**, a first side **54** and a second side **56**. Lower support member **18** is secured to monitor panel **12** at two or more attachment points **58** and **60** that are located along first end **50** at or near first and second sides **54** and **56**, respectively. Lower support member **18** is secured to base **14** at second end **52**. It is common for known monitor assemblies to include only a single support member to support the monitor panel and connect the panel to the base. In many known monitor assemblies, the monitor panel is rotatably mounted to the support member. The rotatable mounting configuration of known monitor assemblies allows a user of the monitor assembly to adjust the viewing angle of a monitor screen on the front surface of the monitor panel. However, despite the advantages of having a rotatably adjustable monitor panel, such a configuration typically lacks stability during touch inputs if a touch screen is integrated with such a monitor.

To assist in providing stability in monitor assembly **10** having touch input capabilities, the monitor assembly includes an upper support member **16**. Upper support member **16** includes a first end **70**, a second end **72**, a first side **74**, and a second side **76**. Upper support member **16** is secured to monitor panel **12** at two or more attachment points **78** and **80** located along first end **70** at or near first and second sides **74** and **76**, respectively. Upper support member **16** is secured to base **14** at second end **72**, at a location generally rearward along base length L from the connecting point of lower support member **18** to base **14**. Upper support member **16** is preferably symmetrically positioned about vertical centerline B of monitor panel **12** so that forces from touch inputs to a touch screen of the monitor panel are more evenly distributed through support member **16** into base **14**. Upper support member **16** assists in stabilizing the monitor assembly when touch inputs are made in either the upper half **24** or the lower half **26** of the monitor panel.

Preferably, upper support member **16** is secured to the upper half **24** of monitor panel **12** and the lower support member **18** is secured to the lower half **26** of panel **12**. Furthermore, it is preferred that the attachment points **58**, **60**, **78** and **80** of the upper and lower support members are each located in a separate quadrant I–IV of the monitor panel **12**, as shown in FIG. **1**.

In this embodiment, the upper and lower support members **16** and **18** are fixed in a particular position on both the monitor panel **12** (with attachment points in each of the four quadrants) and the monitor base **14**, thus fixing monitor panel **12** in the generally upright position illustrated in FIG. **1**. In other embodiments, the size and position of one or both of the upper and lower support members **16** and **18** may vary to change the fixed position of monitor panel **12** to an angled position relative to base **14**. In yet further embodiments, shown and illustrated herein, upper and lower support members **16** and **18** may be adjustable and adjustably attached to panel **12** such that the position of monitor panel **112** relative to base **114** is adjustable by a user of the monitor assembly.

Referring now to FIGS. **2** and **3**, an alternative monitor assembly **100** is shown having adjustment capabilities. Monitor assembly **100** includes a monitor panel **112**, a monitor base **114**, an upper support member **116**, and a lower support member **118**. The lower support member **118** is rotatably secured to panel **112** to allow rotation of panel **112** relative to base **114**. Upper support member **116** is configured to lock and hold panel **112** in a given rotated position while providing necessary stability and support for the monitor assembly **100** when touch inputs are entered to a touch panel of the assembly.

Monitor panel **112** includes upper and lower halves **124** and **126** divided by a horizontal centerline A1, and further includes first and second halves **128** and **130** divided by vertical centerline B1. The horizontal and vertical centerlines A1 and B1 define quadrants I, II, III and IV of monitor panel **112**. Panel **112** also includes a front surface **120** into which a monitor screen is integrated, and a rear surface **122** to which upper and lower support members **116** and **118** are mounted.

The monitor base **114** of monitor assembly **100** has a length L1 from a front end **140** to a rear end **142**, and a width W1 between a first side **144** and a second side **146**. Base **114** also has a height H1 between an uppermost surface **148** and a bottom surface **149**. As shown in FIG. **3**, front end **140** has a curved shape and upper surface **148** is contoured across the width and length of the base **114** W1. Width W1 varies between front end **140** and rear end **142** due to the contoured shape of the first and second sides **144** and **146**. The contours and curved features of base **114** provide an aesthetically pleasing base member that maintains the stability of the monitor assembly when used in an upright position and when used at various angled positions relative to the base.

Base **114** also includes a cable management system for consolidating and arranging cables extending from monitor panel **112**. The cable management system includes a first cover **132** and a second cover **133** that are removable from base **114** and cover a portion of apertures **136** and **137** formed in base **114**. Covers **132** and **133** may be formed as a unitary member with connecting portion **131** extending

between the two covers that can easily be removed with release tabs **134** and **135**, or can be formed as separately removable items. When in use, cables secured to panel **112** extend through apertures **136** and **137**, are captured by covers **132** and **133**, and extend out through rear portion **142** of the base member from apertures **138** and **139** formed in either a rear portion of the base or from the cover members **132** and **133**.

In addition to the cable consolidation and arrangement benefits of the cable management system, the cable management system may also be used to create a amount of slack in the cable between apertures **136** and **137** and an attachment point of the cables to monitor panel **112**. Clipping or otherwise fixing the cable between the covers **132** and **133** and the base **114** may help maintain slack in the cable between the base and the monitor panel. This amount of slack (not shown) can allow the monitor panel to rotate between an upright position and an angled position relative to base **114** without a rearward or downward directed forces typically exerted by cables as they extend from a monitor panel to a power source, CPU, printer or other system. Thus, by ensuring an amount of slack in a cable attached to panel **112** using the cable management system of the present invention, the cable management system may, under certain circumstances, provide additional stability to the monitor assembly **100**.

The lower support member **118** of monitor assembly **100** has a first end **150** rotatably attached to the monitor panel, and a second end **152** secured to base **114**. Lower support member **118** provides at least two attachment points **158** and **160** that are horizontally spaced apart and positioned in separate quadrants IV and III in the lower half **126** of monitor panel **112**.

The rotatable mounting of the panel **112** to lower support member **118** may be enabled using a shaft that extends between a first side **154** and a second side **156** of lower support member **118** that engages a laterally extending bore **162** on the rear surface **122** of panel **112**. In another embodiment, feature **162** may include protrusions that extend horizontally outward from feature **162** and engage apertures formed in first end **150** of the lower support member. In another embodiment lower support member **118** is fixed to panel **112** and rotates relative to base **114**.

Upper support member **116** includes a first portion **184** and a second portion **186** that adjustably mate with each other and secure panel **112** to base **114**. First portion **184** is "Y" or yoke-shaped with a first arm **183** and a second arm **185** that each attach separately to panel **112** via an attachment plate **182** or other means. The point at which first and second arms **183** and **185** are secured to panel **112** defines attachment points **178** and **180**. Preferably, attachment point **178** is in quadrant I and attachment point **180** is in quadrant II of upper half **124** of the panel. In other embodiments, first and second portions **183** and **185** connect directly to the monitor panel without an attachment plate **182**.

First and second portions **183** and **185** come together to form a single neck portion **179** of first portion **184** that mates with second portion **186**. The neck portion **179** includes an aperture **189** into which a thumb turn **188** is mounted for engaging adjustment features of the second portion **186**.

Second portion **186** includes a track surface **187** adjacent a slot **191** formed along a length of second portion **186**. A portion of thumb turn **188** engages the slot **191** and the adjustment features of track **187** to hold monitor panel **112** in an adjusted angled position relative to base **114**. Thumb turn **188** may be configured in a variety of different ways to accomplish the same purpose of releasably securing the first portion **184** to the second portion **186**. For example, the thumb turn **188** may be spring loaded such that the thumb turn must be pulled outwardly to disengage the features of track **187**, thus allowing the first and second portions **184** and **186** to move relative to each other to alter a rotated position of panel **112**. Thumb turn **188** may, in another embodiment, include a threaded shaft that extends through slot **191** and engages a threaded nut on an opposing side of second portion **186**, such that rotation of thumb turn **188** causes adjustment features of first portion **184** to engage the adjustment features of track **187** to secure the first and second portions **184** and **186** together. In exemplary embodiments, the thumb turn can be easily disengaged, the monitor can be tilted, and the thumb turn can be re-engaged to secure the monitor at the desired angle of tilt, all while the user is gripping the thumb turn and using a single hand.

As shown in FIG. **3**, first portion **184** has a curve or contoured shape that substantially matches the contour and shape of second portion **186**. Further, first and second portions **184** and **186** are mounted to the panel and the base, respectively, in a specific direction that allows the first and second portion to maintain contact during rotation of panel **112** about lower support member **118**. In other embodiments, the first and second portions of the upper support member need not be curved but may have linear features that perform the same function of allowing rotation of the monitor panel and locking the panel in a particular position relative to base **114**.

Second portion **186** is secured to base **114** at a distance L2 from end **142**. The distance L2 may vary depending on the shape and size of upper support member **116**, the size and weight of panel **112**, and the available rotation angles for the panel relative to the base.

The monitor panel **112** of monitor assembly **100** shown in FIGS. **2** and **3** may rotate between a generally upright position (0 degrees, as shown in FIGS. **2** and **3**) and an angled position relative to base **114** of up to about 60 degrees. In other embodiments, monitor panel **112** may rotate between about −10 degrees to about 90 degrees with a few modifications to the embodiment illustrated in FIGS. **2** and **3**. All positions of monitor panel **112** are stable under normal touch input forces at any location on a monitor screen that is integrated into a front surface of the monitor panel **112**.

Touch forces exerted on monitor assembly **100** due to touch inputs to a touch screen of the monitor panel **112**, may include X, Y and Z components (as defined by the axes shown in FIG. **3**). Known monitor assemblies fail to provide adequate stability in the front-to-back and side-to-side directions particularly when touch forces are applied at the upper and outermost corners of the touch screen, and at various locations on the touch screen when the monitor panel is at an angled position relative to the base. Monitor assembly **100** provides a four point attachment configuration with upper and lower support members and a base design to provide and maintain stability for any touch input having any direction of force applied to the touch screen of the monitor panel **112**.

Referring now to FIG. **4**, a monitor assembly **200** is shown having an alternative upper and lower support member configuration. Monitor assembly **200** includes a monitor panel **212** and monitor base **214** similar to the corresponding features of monitor assembly **100**. Assembly **200** includes an upper support member **216** that is integrated as a single unitary piece, such as the upper support member **16** of

assembly **10**. Assembly **200** also includes a lower support member **218** that is attached to panel **212** such that the panel is fixed in a predetermined position relative to base **214**. As with assemblies **10** and **100**, assembly **200** includes a four point attachment configuration with first and second contact points **258** and **260** of the lower support member positioned in separate quadrants IV and III of a lower half **226** of panel **212**, and first and second contact points **278** and **280** of the upper support member positioned in separate quadrants I and II of an upper half **224** of the monitor panel **212**. All four attachment points are located in separate quadrants I, II, III or IV defined by horizontal and vertical centerlines A2 and B2, respectively.

Monitor assembly **200** has enhanced stability compared to known monitor assemblies. The stability of assembly **200** is particularly relevant for a monitor panel having touch input capabilities. Assembly **200** is less susceptible to vibrations and reduces resonant oscillations due to repetitious touch inputs, as compared to known monitor assemblies with three or less attachment points on the monitor panel. Assembly **200** may reduce the magnitude and duration of vibrations due to touch inputs by providing improved damping of vibrations.

Referring now to FIG. **5**, an alternative embodiment of a monitor assembly **300** is shown. Assembly **300** includes a monitor panel **312**, a base **314**, an upper support member **316**, and a lower support member **318**. Monitor panel **312** and base **314** are similar to corresponding features of monitor assemblies **10**, **100** and **200**. Upper support member **316** is comparable to the upper support first portion **184** of assembly **100**. Lower support member **318** integrates the comparable features of lower support member **118** as well as upper support second portion **186** of assembly **100**.

The size and shape of lower support member **318**, and the amount of surface area interfacing between the lower support member **318** and base **314** provides enhanced stability of monitor assembly **300**. Lower support member **318** includes an engagement track or slot **387** that is engaged by a portion of thumb turn **388** that extends through a portion of upper support member **316**. Thus, as thumb turn **388** engages or disengages track **387**, the rotation of panel **312** relative to base **314** is controlled.

Upper support member **316** includes a Y or yoke-shaped design that is aesthetically pleasing while providing distinct two point attachment of the upper support member to panel **312** at attachment points **378** and **380**. Lower support member **318** is also connected or attached to monitor panel **312** at two locations **358** and **360**. FIG. **5** illustrates monitor panel **312** in an angled position, rotated at approximately 60 degrees from an upright position. The available angle of rotation of panel **312** is determined in part by the size and shape of lower support member **318**, the size of upper support member **316**, the length of track portion **387** formed in the lower support member **318**, and the location of attachment points **358**, **360**, **378** and **380** on panel **312**.

Monitor panel **312** is divided into four quadrants I, II, III and IV by horizontal centerline A3 and vertical centerline B3. The first portion attachment points **378** and **380** of upper support member **316** are in separate quadrants I and II, respectively. The attachment points **358** and **360** of lower support member **318** are in separate quadrants IV and III, respectively.

Monitor assembly **300** includes a cable management system where cables extending from a bottom or back portion of panel **312** extend through lower support member **318** and exit assembly **300** through aperture **338**. According to this cable management system, the cables are concealed and consolidated in an aesthetically pleasing way. In some embodiments, lower support member **318** may have a hollow interior sufficient in size to maintain a certain amount of slack in the cables extending from the monitor panel so that the panel can rotate through its rotation angle without tension being exerted on the panel from the cables. A hollow interior of lower support member **318** may also be used to conceal a power brick of the power cord.

Referring now to FIGS. **6** and **7**, a monitor assembly **400** is shown having some alternative features of the present invention. Assembly **400** includes a monitor panel **412**, a monitor base **414**, an upper support member **416** and a lower support member **418**. The support members **416** and **418** provide a four point attachment of the support members to panel **412** to provide necessary support and stability of the assembly when touch inputs are entered to a touch screen integrated into a front surface **420** of monitor panel **412**.

Base **414** includes an upper surface **448**, first and second sides **444** and **446**, and retaining slots **466** and **468** that are formed in base **414** along first side **444** and corresponding retaining slots (not shown) that are formed in base **414** along second side **446**. The retaining slots are provided in pairs with each slot of the pair of slots being aligned parallel to the other slot across a width of base **414** between first and second sides **444** and **446**. The engagement slots are configured to receive a portion of first and second leg members **483** and **485** of the upper support member **416**. Each pair of engagement slots, when engaging the first and second leg members, represents a different position for panel **412**. In other embodiments, there may be fewer or more pairs of slots formed in base **414**, with each pair of slots representing a different position for panel **412**.

Upper support member **416** may be rotatably secured to panel **412** such that a high amount of torque is required to rotate member **416** relative to the panel. Upper support member **416** may further include a position stop feature that defines a fully extended position of the upper support member and limits an angle through which member **416** may rotate relative to the panel. Upper support member **416** may be rotated to a position that places leg member **483** and **485** away from base **414** so that the leg members do not engage a pair of slots in the base. When the leg members are positioned outside of the base slots, panel **412** may be angled even further from an upright position than that angled position shown in FIG. **6**.

Further, the upper support member may stabilize the monitor panel even when the leg members are disengaged from the slots. Stabilization of the panel may be enabled by the high torque connection of the upper support member to the panel that holds the panel in a given rotated poison. The panel may also be help in a stable position when the upper support member is fully extended and held from further extension by the position stop. In use, the rearward positioned pair of slots may, for example, provide for a 45 degree rotation of panel **412** from an upright position, while the fully extended position of the upper support member may provide for a 65 degree rotation of panel **412** from the upright position.

When leg members **483** and **485** are retained within slots **466** and **468**, monitor panel **412** is in a generally upright position, perpendicular to base **414**. When members **483** and **485** are retained within slots **467** and **469**, monitor panel **412** is in an angled position relative to an upright position of the panel. In order for upper support member **416** to provide support for panel **412**, it must engage one of the pairs of slots in base **414**.

The upper surface **448** of base **414** includes a contact portion **457** that engages a rotation surface **453** of lower support member **418** so that lower support member **418** is able to rotate relative to base **414**, but does not inadvertently lose contact with the base. In other embodiments, lower support member **418** may be rotatably secured to base **414** in a different manner, such as by the pin and aperture design used for securing upper support member **416** to panel **412**.

Monitor panel **412** is divided into four quadrants I, II, III and IV, that are defined by horizontal and vertical centerlines A4 and B4 of the panel. Attachment points **458** and **460** are maintained between base **414** and the lower support member **418** at first and second sides **454** and **456** of the lower support member in separate quadrants IV and III of a lower half **426** of panel **412**. Attachment points **478** and **480** between upper support member **416** and panel **412** are positioned at or above centerline A3 in separate quadrants I and II of upper half **424** of panel **412**.

Rear surface **422** of panel **412** may include brackets **462** and **463** configured to receive attachment features such as pins **464** and **465**, respectively, of the upper support member **416**. Attachment features **464** may extend through horizontally aligned apertures of the brackets **462** and **463** so that the monitor panel is able to rotate relative to the upper support member **416**, and thus rotate relative to base **414**.

Referring now to FIG. **8**, a monitor assembly **500** is shown having an alternative adjustable upper support member **516** configuration. Monitor assembly **500** includes a monitor panel **512**, a base **514** and a lower support member **518** that are similar to corresponding members of assemblies **10, 100** and **200**. The lower support member **518** is fixed to base **514** and is rotatably secured to panel **512** at two attachment points, one of which attachment points **560** is shown. The upper support member **516** includes a first portion **584** and a second portion **586** that adjustably mate with each other and secure panel **512** to base **514**. A first end **570** of upper support member **516** is secured to panel **512** at attachment points **578** and **580**. A second end **572** of upper support member **516** is secured to base **514** rearward of the attachment point of lower support member **518** to base **514**.

As shown in FIG. **8**, first portion **584** is insertable into second portion **586** to allow rotation of monitor panel **512** about lower support member **518**. Second portion **586** includes an aperture **589** into which a thumb knob **588** is inserted to engage a slot **591** formed in first portion **584**. Thumb knob **588** is adjustable to release the first and second portions so they can move relative to each other, and to hold the first and second portions together to retain panel **512** in a given position relative to base **514**.

In order for the first and second portions to move relative to each other, the attachment points of upper support member **516** to the panel (at first end **570**) and to the base (at second end **572**) must be rotatable. The attachment point **560** of lower support member **518** to the panel must also be rotatable to allow the first and second portions to rotate as the panel rotates relative to the base. An example of a rotatable attachment of an upper support member to a monitor panel is shown in FIGS. **6** and **7**, and may be used as the rotatable attachment for upper support member **516** to panel **512** and base **514**. In other embodiments, the configurations of the first and second portions **584** and **586** may be reversed so that second portion **586** is insertable into first portion **584**.

Monitor assembly **500** may also require that one or both of the first and second portions **584** and **586** of upper support member **516** must be able to move both rotatably and linearly relative to the panel and base. For example, a vertical slot may be formed on an upper half of the rear surface **522** of panel **512** that extends parallel to centerline B5 and is configured to receive end **570** of the upper support member. The vertical slot may be associated with a locking feature similar to thumb knob **588**, that engages end **570** to lock the upper support member in a given vertical position on the panel. When adjusting the rotated position of panel **512** relative to base **514**, thumb knob **588** and the locking feature of end **570** would be released, the panel position adjusted by allow both member **584** to slide relative to member **586** and allowing end **570** to move within the vertical slot on the panel, and the thumb knob and locking feature tightened again to hold the panel in the adjusted position. A similar slot may be formed in base **514** that is associated with a locking feature that locks end **572** and provides similar adjustment capabilities as the slot formed in panel **512** described above.

In a yet further embodiment, lower support member **518** may be movable relative to base **514**, for example in a slot formed in base **514** that is aligned with the upper support member. Providing a second linear motion via the lower support member in addition to the linear motion between members **584** and **586** as they move relative to each other permits rotation of the panel from an upright position.

The location at which the first and second portions of upper support member **516** are secured to panel **512** and base **514** may be configured so that the first and second portions move into or out of the panel or base. For example, panel **512** may have a sufficient thickness between a front surface and rear surface of the panel so that an aperture may be formed in the rear surface of the panel that allows for end **570** of the upper support member to be inserted into the panel a given distance. A locking feature would be associated with the aperture in the panel to lock the upper support member in a given inserted position in the panel. Thus, when adjusting the rotated position of the panel, the thumb knob **588** is released, the locking feature associated with the aperture is released, members **584** and **586** are moved relative to each other, and the thumb knob and locking feature are tightened to lock the panel in a given position. A similar aperture could be formed in base **514** if the base was provided with a thickness sufficient to allow end **572** of the upper support member to be inserted into the base and adjusted to different inserted positions within the base.

Monitor panel **512** may be divided into four quadrants I, II, III and IV by horizontal centerline A5 and vertical centerline B5. The first portion attachment points **578** and **580** of upper support member **516** are in separate quadrants I and II, respectively. The attachment points of lower support member **518** are in separate quadrants IV and III, respectively.

Referring now to FIG. **9**, a monitor assembly **600** is shown having an alternative adjustable upper support member **616**. Monitor assembly **600** includes a monitor panel **612**, a base **614** and a lower support member **618** that are similar to corresponding members of assemblies **100, 200** and **500**. The lower support member **618** is secured to base **614** and is rotatably secured to panel **612** at two attachment points, including attachment point **660**. The upper support member **616** includes a first portion **684** and a second portion **686** that adjustably mate with each other and secure panel **612** to base **614**. A first end **670** of upper support member **616** is secured to panel **612** at attachment points **678** and **680**. A second end **672** of upper support member **616** is secured to base **614** rearward of the attachment point of lower support member **618** to base **614**.

As shown in FIG. **9**, second portion **686** is insertable into first portion **684** to allow rotation of monitor panel **612** about lower support member **618**. First portion **686** includes an aperture **689** into which a thumb knob **688** is inserted to engage a slot **691** formed in second portion **684**. Thumb knob **688** is adjustable to release the first and second portions so they can move relative to each other, and to hold the first and second portions together to retain panel **612** in a given position relative to base **614**.

Monitor panel **612** is divided into four quadrants I, II, III and IV by horizontal centerline A6 and vertical centerline B6. The first portion attachment points **678** and **680** of upper support member **616** are in separate quadrants I and II, respectively. The attachment points of lower support member **618** are in separate quadrants IV and III, respectively.

The above specification, examples and data provide a complete description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention resides in the claims hereinafter appended.

We claim:

1. A touch input monitor comprising:

a monitor panel having a front surface integrating a monitor screen and a rear surface;

a base;

a lower support member secured to the base and pivotally secured to the rear surface of the monitor panel for tilting the monitor panel relative to the base; and

an upper support member comprising a first portion secured to the rear surface of the monitor and a second portion secured to the base, the first portion and second portion adjustably engaging each other to allow tilting of the monitor panel about the lower support member, wherein one of the first portion and second portion comprises an aperture and the other of the first portion and second portion comprises a slot aligned with the aperture such that a fastener inserted through the aperture engages the slot to releasably secure the first and second portions together, wherein the slot comprises ribs that mate with a mating surface of the opposing first portion or second portion to prevent relative movement between the first portion and the second portion when the fastener is tightened.

2. The touch input monitor of claim **1**, wherein the monitor screen comprises a touch panel.

3. The touch input monitor of claim **1**, wherein the monitor panel tilts between about 0 to 60 degrees relative to an axis perpendicular to the base.

4. The touch input monitor of claim **1**, wherein the base includes a cable management system comprising apertures formed in the base to receive cables and a cover removably secured to the base that captures the cables between the cover and base.

5. The touch input monitor of claim **1**, wherein the first portion of the upper support member is secured to the monitor at two points and the lower support member is secured to the monitor at two points.

* * * * *

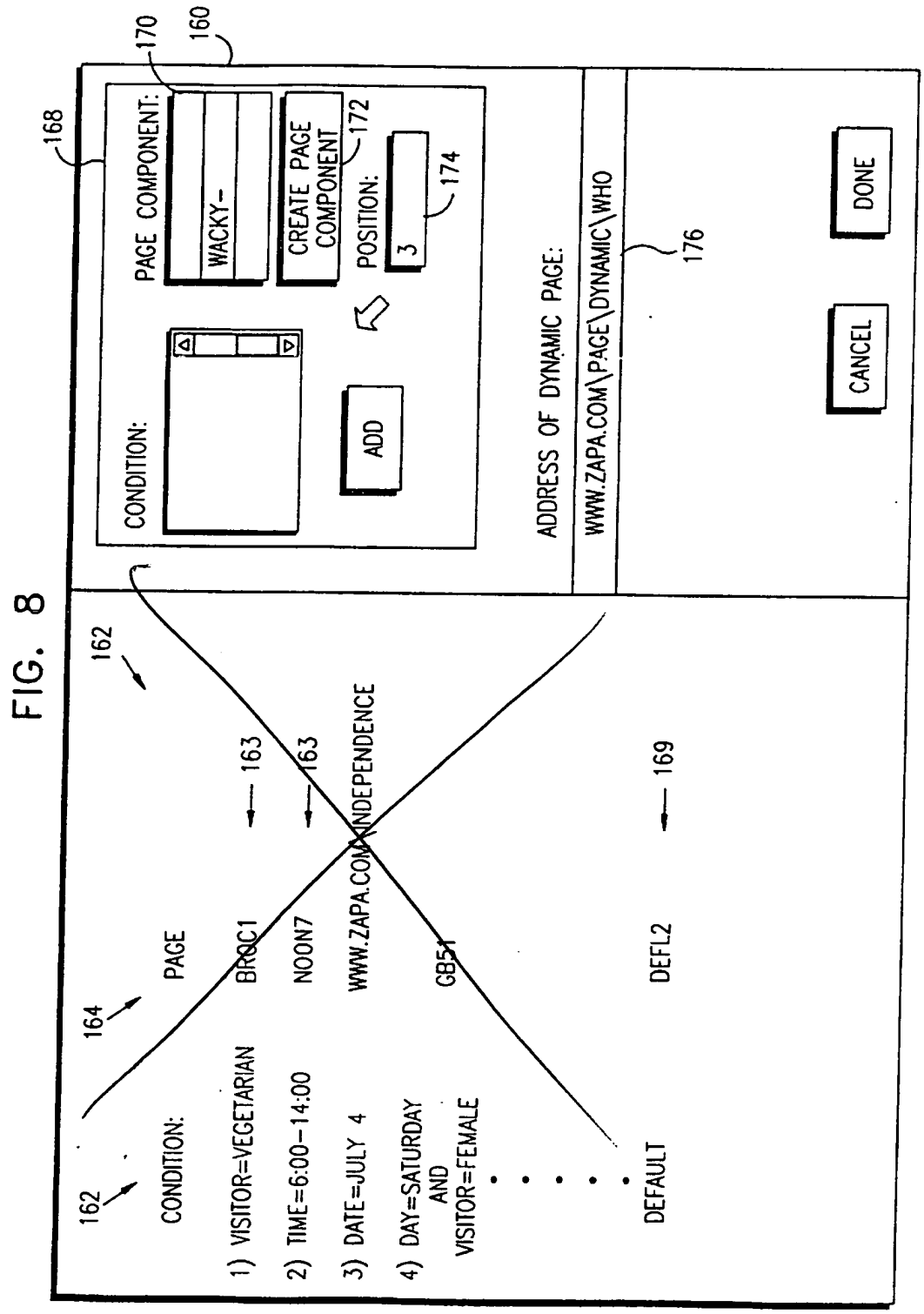
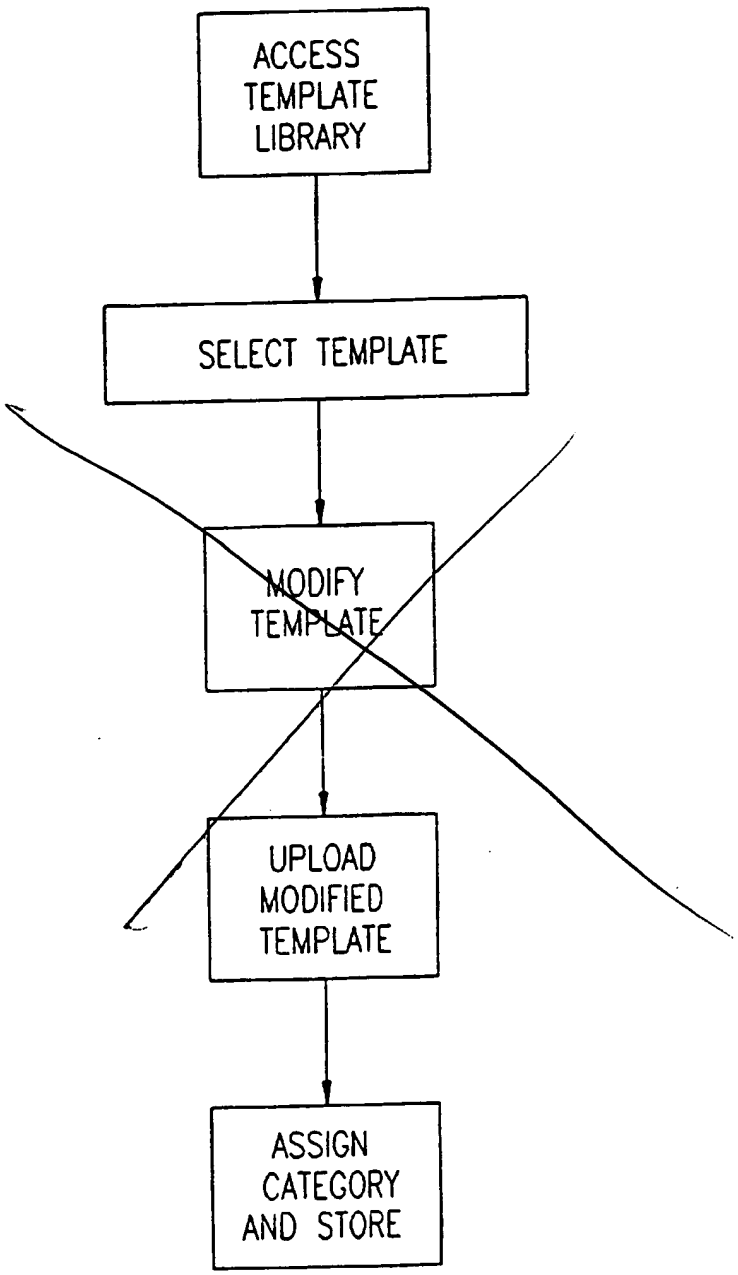

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WACKY-
CREATE PAGE COMPONENT
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3
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CONDITION:
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176
CANCEL
DONE
162
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CONDITION:
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163
3) DATE=JULY 4
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4) DAY=SATURDAY AND VISITOR=FEMALE
GB51
DEFAULT
DEFL2
169

FIG. 8

FIG. 9


ACCESS TEMPLATE LIBRARY
SELECT TEMPLATE
MODIFY TEMPLATE
UPLOAD MODIFIED TEMPLATE
ASSIGN CATEGORY AND STORE

SIMPLIFIED ON-LINE PREPARATION OF DYNAMIC WEB SITES

FIELD OF THE INVENTION

The present invention relates generally to preparation of Web home pages and components to be used thereon, and specifically to simplified on-line preparation of such home pages and components.

BACKGROUND OF THE INVENTION

In recent years, the use of the World Wide Web (WWW) has been rapidly growing. In use of the Web, a client computer user connects to a Web site on a server and requests that the server download and display Web pages on the client computer. In response to the request, the server sends to the client computer graphic files, usually in Hypertext Mark-up Language (HTML), which include media elements (pictures, animations, texts, sound), scripts of instructions to be performed by an Internet browser program running on the computer, and in some cases executable software code, e.g., Java code.

The number of companies, organizations and individuals who have Web home pages is rapidly growing. Companies feel the need to prepare interesting Web sites and Web advertisements in order to attract customers and maintain their standing in the market. Furthermore, many individuals prepare Web pages to convey information in graphical and/or animation formats to their friends and family.

Existing tools for preparing Web pages, such as Dreamweaver, produced by Macromedia, are relatively complex. A small company, organization or home user does not need such tools and in many cases does not know how to take advantage of their sophisticated features. There are on-line services for preparing Web pages, such as the GeoBuilder program offered by Geocities. Other Web sites include programs that aid users in adding features to their Web pages. However, these sites offer the user only limited flexibility, and do not generally support sophisticated features such as Java-based animation.

On-line greeting card companies allow users to select a greeting card and add and/or change text inscriptions associated with the card. Some of these greeting cards include animation sequences, but the animation sequences are generally fixed and cannot be substantially altered by the user.

The above-mentioned Geocities Web site allows a user to prepare a Web page component which includes animation. However, in order to prepare such Web page components and in order to view such components, normal HTML and Java tools are not sufficient, and the user must download a proprietary software client.

Web page components may be programmed to respond differently to different users and/or at different times. For example, an Internet banner prepared by Doubleclick for inclusion in a Web page selects different advertisements to display according to input received from or about a user viewing the Web page, indicative of the user's interests or demographic factors. As another example, the IBM Patent Server Web page, allows a user to subscribe to a patent service and receive the service between certain selected hours on the user's local time.

SUMMARY OF THE INVENTION

It is an object of some aspects of the present invention to provide improved methods and apparatus for simplified generation of Web page components which include animation.

It is another object of some aspects of the present invention to provide improved methods and apparatus for simplified generation of Web page components which respond differently at different times.

It is still another object of some aspects of the present invention to provide improved methods and apparatus for simplified generation of Web page components which respond differently to different users.

In preferred embodiments of the present invention, a server provides a Web site to which a user connects in order to create one or more individualized Web page components. To create such components, the user selects from a plurality of basic animation sequences one or more animation sequence to be displayed on the Web page. Preferably, the user is able to change at least some of the attributes of the selected animation sequence, such as the colors, texts, fonts, characters, borders, sounds, embedded pictures and models. A Web page including the one or more selected animation sequences is then posted at a Web address chosen by or allocated to the user.

In some preferred embodiments of the present invention, the user manipulates the animation sequence by removing and/or repeating scenes or frames of the sequence. Alternatively or additionally, the user adds conditional flow directives to the sequence.

In some preferred embodiments of the present invention, the user assigns conditional values to the attributes of the animation sequence. For example, the user may create a Web page component based on an animation sequence which includes a character (i.e., an animated figure) and may change the character to a conditional character. When a visitor views the Web page, the character actually displayed in place of the conditional character is chosen according to data pertaining to the visitor received by the server on which the Web page is maintained.

In some preferred embodiments of the present invention, the Web site enables the user to create a dynamic Web page component which reacts differently, i.e., which presents a different display to visitors connecting thereto, according to a predetermined scheme. Preferably, the user selects a plurality of Web page components and for each Web page component states a condition that must be fulfilled in order for the particular Web page component to be displayed. Preferably, the Web page components are assigned priorities which determine, for example, which component is displayed when more than one condition is fulfilled, or which component is displayed as a default when none of the conditions is fulfilled. Preferably, the predetermined scheme depends on information pertaining to the visitor, information pertaining to other visitors, or to other unrelated information received by the server on which the Web page component is maintained.

In some preferred embodiments of the present invention, the created Web page component includes a default component and other components which are directed to specific users who identify themselves as belonging to a list of visitors defined by the user. Thus, the user is able to use the components to post messages on the Web page to specific visitors on the list.

In some preferred embodiments of the present invention, the Web site allows the user to create a dynamic Web page component, which is displayed differently to visitors at different times. Preferably, the Web site responds according to the time of day at the geographic location of the visitor. Alternatively, the Web site responds according to the time of day at the geographic location of the user who created the

page. Further alternatively or additionally, the Web site responds according to the day of week, date, month, season and/or year. For example, a user may create a family photo album with a background in accordance with the time or season at which the visitor visits the site.

In other preferred embodiments of the present invention, the dynamic Web page component responds differently according to the total number of visits to the Web page on which it resides, or according to the number of visits by a specific visitor.

Preferably, the user is able to access the Web site without use of a special software client. Further preferably, the created Web page component which includes the animation sequence does not require the use of any special software client for viewing. Rather, the component is based on standard HTML and Java programs.

There is therefore provided, in accordance with a preferred embodiment of the present invention, a method for creating a Web page component, including:

opening a remote connection to a server provided with a plurality of basic animation sequences having variable attributes associated therewith;

choosing, via the connection, at least one of the basic animation sequences to be used in the Web page component;

changing one or more of the variable attributes of the chosen animation sequence; and

posting the Web page component including the animation sequence with the changed attributes to a Web page.

Preferably, opening the remote connection includes opening a connection over the Internet.

In a preferred embodiment, choosing the at least one animation sequence includes choosing an animation sequence which substantially covers an entire Web page.

Preferably, changing one or more of the attributes of the animation sequence includes inserting data into the animation sequence. Preferably inserting data into the animation sequence includes inserting images or, alternatively or additionally, inserting hypertext links.

Preferably, changing one or more of the attributes of the animation sequence includes changing a color setting in the animation sequence and/or changing a character which appears in the animation sequence.

In a preferred embodiment, the animation sequence includes a plurality of frames in a predetermined order and changing one or more of the attributes includes manipulating the frames in the sequence. Preferably, manipulating the frames in the sequence includes deleting one or more frames from the animation sequence or, alternatively or additionally, repeating one or more frames in the animation sequence.

In another preferred embodiment, changing one or more of the attributes of the animation sequence includes assigning to at least one of the one or more attributes a plurality of values which are respectively chosen responsive to a condition evaluated when the Web page component is viewed. Preferably, changing one or more of the attributes of the animation sequence includes adding conditional flow directives to the animation sequence.

Preferably, posting the Web page component includes posting a link to the animation sequence, wherein posting the Web page component includes posting a list of the changes performed on the animation sequence.

Further preferably, posting the Web page component includes posting a Web page component which does not require any proprietary software in order to be viewed by a viewer, and changing the one or more attributes does not require use of any proprietary software.

There is also provided, in accordance with a preferred embodiment of the present invention, a method for creating a Web page component, including:

providing a plurality of basic animation sequences on a server, the sequences having variable attributes associated therewith;

receiving from a remote processor a selection of at least one of the basic animation sequences to be used in the Web page component;

changing one or more of the attributes of the chosen animation sequence responsive to a command received from the remote processor; and

posting the Web page component including the animation sequence with the changed attributes to a Web page.

In a preferred embodiment, providing the plurality of basic animation sequences includes receiving an animation template uploaded to the server by a user.

Preferably, changing one or more of the attributes includes inserting data into the sequence. Alternatively or additionally, changing one or more of the attributes of the animation sequence includes changing a color setting in the animation sequence.

In a preferred embodiment, the animation sequence includes a plurality of frames in a predetermined order and wherein changing one or more of the attributes includes manipulating the frames in the sequence.

In another preferred embodiment, changing one or more of the attributes of the animation sequence includes assigning to at least one of the one or more attributes a plurality of values which are respectively chosen responsive to a condition evaluated when the Web page component is viewed. Preferably, changing one or more of the attributes includes adding conditional flow directives to the animation sequence.

Preferably, posting the Web page component includes posting a link to the animation sequence. Most preferably, posting the Web page component includes posting a list of the changes performed on the animation sequence.

Further preferably, posting the Web page component includes posting a Web page component which does not require any proprietary software in order to be viewed by a viewer, and changing the one or more parameters does not require installing any proprietary software on the processor.

There is further provided, in accordance with a preferred embodiment of the present invention, a method for creating a dynamic Web page component on a server which presents a plurality of different Web page component displays at different visits to a page containing the component by visitors connecting to the server, including:

generating representations of the plurality of different displays;

receiving from a remote processor a dynamic scheme for presenting the displays differently at different visits to the page containing the component by the visitors; and

presenting the displays to the visitors responsive to the dynamic scheme.

Preferably, generating the representations includes generating a script which creates the display.

Alternatively or additionally, generating the representations includes receiving a link to a Web page which contains the display, wherein generating the representations preferably includes generating a list of changes to the Web page component referenced by the link.

Preferably, generating the representations includes creating at least one of the representations interactively responsive to commands from a user of the remote processor.

Alternatively or additionally, generating the representations includes importing at least one of the representations from the remote processor.

Preferably, receiving the scheme from the remote processor includes receiving a scheme over the Internet.

In a preferred embodiment, receiving the scheme includes receiving a scheme including a condition associated with each of the plurality of displays. Preferably, receiving the scheme includes setting an order of precedence for the plurality of displays, and further includes setting a default display. Preferably, receiving the scheme includes receiving a scheme which depends on the time at which the dynamic page component is viewed and/or on the number of times the dynamic page component was viewed and/or on data related to one of the visitors who view the dynamic page component.

There is additionally provided, in accordance with a preferred embodiment of the present invention, apparatus for creating a Web page component, including:

a server which displays a plurality of basic animation sequences, and allows a user of a remote processor to select at least one basic animation sequence and change one or more attributes of the sequence; and

a communication interface which receives a connection from the remote processor to the server, whereby the user thereof selects the sequence.

In a preferred embodiment, the at least one basic animation sequence covers an entire Web page.

Preferably, the one or more attributes include colors associated with the sequence.

Further preferably, the server allows addition of data into the sequence by the user.

In a preferred embodiment, the animation sequence includes a plurality of frames, and the server allows the user to manipulate the frames. Preferably, the server allows the user to delete frames and/or to duplicate frames.

In another preferred embodiment, the server assigns a plurality of values to the one or more attributes together with a scheme which determines which of the values is to be used each time the Web page component is displayed.

Preferably, the server adds a conditional flow directive to the sequence responsive to a command from the user.

Preferably, the server allows the user to select and change the sequence using substantially only non-proprietary software.

There is moreover provided, in accordance with a preferred embodiment of the present invention, apparatus for creating a dynamic Web page component, including:

a server which generates a plurality of representations of different displays; and

a communication interface which receives a connection from a remote processor to the server and allows the user of the remote processor to determine a dynamic scheme for presenting the displays differently at different visits to a Web page that includes the component.

Preferably, the plurality of representations include scripts which generate the display.

Further preferably, at least one of the representations includes a link to a Web page on an external server, wherein the representation most preferably includes a list of changes to the Web page component on the external server.

Preferably, the server generates the representations responsive to commands from the remote processor.

In a preferred embodiment, the dynamic scheme includes a respective condition for selecting each of the different displays. Preferably, the dynamic scheme includes a an order of precedence of the different displays. Alternatively or additionally the dynamic scheme depends on the time of a visit to the page that includes the component and/or on the identity of a visitor viewing the page.

There is also provided, in accordance with a preferred embodiment of the present invention, a software package for creating Web page components, including an executable file which is run by a server to display on a Web page a selected basic animation sequence from among a plurality of basic animation sequences having variable attributes associated therewith, responsive to selection of the sequence by a remote user, and which allows the remote user to change one or more of the variable attributes of the selected sequence.

Preferably, the variable attributes include one or more attributes selected from a group of attributes that includes colors, characters, pictures, texts, links, and sound files.

Further preferably, the software package includes a plurality of data files which include data representative of the basic animation sequences, wherein the executable file performs changes to the animation sequence by changing a copy of a respective one of the data files. In a preferred embodiment, the executable file performs changes to the animation sequence by associating a list of changes with a pointer to a respective one of the data files.

There is additionally provided, in accordance with a preferred embodiment of the present invention, a Web site, including:

a display of a plurality of basic animation sequences having variable attributes associated therewith; and

an interface for receiving a selection of one of the animation sequences and for performing changes to the selected animation sequence.

There is further provided, in accordance with a preferred embodiment of the present invention, a software package for creating Web page components, including an executable file which is run by a server to display an interface, which receives from a user data representative of each of a plurality of different displays of a Web page component, and which receives from the user a scheme for determining which of the different displays is to be displayed upon each visit to a Web page including the component by visitors connecting to the page.

There is also provided, in accordance with a preferred embodiment of the present invention, a Web site, including an interface for receiving data representative of each of a plurality of different displays of a Web page component, and for receiving a scheme for determining which of the different displays is to be displayed upon each visit to a Web page including the component by visitors connecting to the page.

There is additionally provided, in accordance with a preferred embodiment of the present invention, a method for creating an animation template for generating a computer animation, including:

downloading a basic animation template from a server via a network, the basic template including one or more placeholders corresponding to respective fields in a database, such that an animation is generated responsive to the template including objects stored in the database;

modifying the basic template to generate a new animation template including the placeholders so as to produce a computer animation having a substantially different graphic appearance from that of the basic template; and

uploading the new template to the server, so that the new template is accessible to a client of the server.

Preferably, the client selects the new template and changes one or more attributes thereof to produce an animation sequence to be posted to a Web page.

There is furthermore provided, in accordance with a preferred embodiment of the present invention, a software package for creating an animation template, including an executable file which is run by a client computer to download a basic animation template from a server via a network, the basic template including one or more placeholders corresponding to respective fields in a database, such that an animation is generated responsive to the template including objects stored in the database, and to modify the basic template to generate a new animation template including the placeholders so as to produce a computer animation having a substantially different graphic appearance from that of the basic template.

Preferably, the new template is uploaded to the server, where it is accessible to other clients who select the new template and change one or more attributes thereof to produce an animation sequence to be posted to a Web page.

The present invention will be more fully understood from the following detailed description of the preferred embodiments thereof, taken together with the drawings in which:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic illustration of a system for creation of a Web page, in accordance with a preferred embodiment of the present invention;

FIG. **2** is a flow chart that schematically illustrates a method for preparing a Web-page component, in accordance with a preferred embodiment of the present invention;

FIG. **3** is a schematic view of an animation editing window, in accordance with a preferred embodiment of the present invention;

FIG. **4** is a schematic illustration of a Web page component description, in accordance with a preferred embodiment of the present invention;

FIG. **5** is a schematic illustration of a sequence editor interface, in accordance with a preferred embodiment of the present invention;

FIG. **6** is a schematic illustration of a condition editor interface, in accordance with a preferred embodiment of the present invention;

FIG. **7** is a flow chart schematically illustrating a method for preparing a dynamic Web page component, in accordance with a preferred embodiment of the present invention;

FIG. **8** is a schematic illustration of a dynamic component editor interface, in accordance with a preferred embodiment of the present invention; and

FIG. **9** is a flow chart that schematically illustrates a method for preparing a dynamic Web page template, in accordance with a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

FIG. **1** is a schematic illustration of a system **18** for creating Web page components, in accordance with a preferred embodiment of the present invention. A server **26**, preferably a Web server, as is known in the art, hosts a Web site for creating the Web page components, which may also be used to create entire Web pages. A user uses a processor **20** to connect, for example using a modem **24**, to server **26** via a network **28**, preferably via the Internet. Processor **20** is preferably coupled to a display **22** on which the Web site of server **26** is displayed. Using the Web site, the user creates a Web page component as described hereinbelow. During the creation of the Web page component, the description of the Web page is stored in a work-area allocated to the user on a memory associated with server **26**.

FIG. **2** is a flow chart which schematically illustrates actions taken by the user of processor **20** in preparing the Web page component, in accordance with a preferred embodiment of the present invention. The Web site of server **26** displays a list of categories from which the user may select for inclusion in the Web page. The categories may include, for example, photo albums, advertisements, greeting cards, and resumes. Alternatively or additionally, the categories may be defined according to any other classification. According to the selected category, the user is provided with a list of titles of basic animation sequences. Each of the animation sequences is generated by a respective script, preferably written in the JavaScript language, or as an executable Java program, which is stored on server **26**. The user may preview any of the animation sequences on display **22** in order to select an animation sequence which forms a basis of the Web page to be created for the user.

Preferably, the script describing the selected animation sequence is copied to a work area on server **26** that is assigned to the user. Alternatively or additionally, a link is placed in the work area referring to the script, and there is no need to produce an additional copy of the script.

Preferably, the user is able to change attributes of the selected animation sequence, such as colors and choice of images. Further preferably, the user enters data, such as text, hypertext links, and pictures, to the animation sequence at locations assigned in the sequence for receiving the data. Alternatively or additionally, the user may manipulate the animation sequence, by removing or repeating one or more frames or scenes of the sequence. One preferred method of performing these changes to the animation sequence is described hereinbelow with reference to FIGS. **3**, **4**, **5**, and **6**.

Preferably, the revised animation sequence is assigned a URL address and is posted on a network server, either server **26** or a different Internet server. The assigned URL address can then be incorporated inside another Web site as a link or, preferably, another URL address may be used to incorporate the animation sequence in another Web page, either in an open or hidden incorporation scheme. Alternatively or additionally, the animation sequence is assigned an identification name, which is used to incorporate the sequence as a dynamic Web page component, as described further hereinbelow. Further alternatively or additionally, the script describing the animation sequence is downloaded to processor **20**.

Preferably, the user is able to select one or more such animation sequences and paste them onto a Web page assigned to the user. Changes to the sequences, if needed, are preferably performed by returning to the Web site on server **26**. The user creates other parts of the Web page in accordance with on-line or off-line methods known in the art.

It is noted that although the above description refers to an animation sequence which is used as a component of a Web page, the present invention can also be adapted for building entire Web pages.

FIG. **3** is a schematic view of an animation editing window **38** shown on display **22**, in accordance with a preferred embodiment of the present invention. Editing window **38** comprises a display window **40** in which the selected animation sequence is displayed. A control panel **42** preferably comprises a play control **44**; a freeze control **46**, which allows a user to stop the sequence on a specific frame; and direction icons **48**, which allow the user to scan the

animation sequence. Alternatively or additionally, control panel **42** includes other suitable controls, such as a frame counter **49** and/or a scene counter **47**.

Window **38** preferably comprises a plurality of image attribute controls **52**, which allow the user to change attributes of images shown in the animation sequence. The user preferably changes the attributes by selecting from a predefined group of replacements available from server **26**. For example, in order to change a character **60** seen in the animation, the user selects the character, typically using a mouse or other pointing device, and actuates the appropriate control **52**. A pop-up window **54** displays a plurality of characters from which the user may select a replacement for character **60**. Preferably, the user is also able to change attributes of the selected character **56**, such as the behavior of the character. Such behaviors are described, for example, in U.S. patent application Ser. No. 08/819,607, which is assigned to the assignee of the present patent application and is incorporated herein by reference, and in a corresponding PCT patent application published as WO97/35280. Likewise, the user may change border widths and colors of objects and of background regions in the animation sequence. Alternatively or additionally, window **38** allows changing of any other suitable attributes, such as the fonts and sizes of letters and background patterns.

Preferably, the changes made in the animation are stored by modifying the script associated with the created page. Alternatively, the reference to the script is accompanied by a list of changes to be made in the script, and the list is taken into account when displaying the page. Preferably, a script control **45** allows the user to request to see the script corresponding to the animation sequence.

Window **38** preferably includes additional controls **50**, **51**, **53** and **55**, which are used to enter data to be associated with the animation sequence. For example, the user selects a text field **62** in display window **40** and actuates the text control **53**. In response, a pop-up window **58** preferably opens, in which the user may enter a replacement text to display in field **62**. Likewise, the user may select a link address **64** in the display window, and using "links" control **55**, along with a respective entry window, may change the address of the link.

Picture control **50** is similarly used to enter pictures into the animation sequence. Preferably, the user may import pictures which are represented in substantially any standard format. The picture is passed to server **26**, where it is converted if necessary into a standard format suitable for use in the animation sequence, and the description in the standard format is stored in the location allocated for the created Web page component. Further preferably, when a viewer views the page, the picture is passed to the viewer in a format most suitable for the user and at a size and resolution chosen such that the picture can be transmitted and viewed even over slow network connections in a reasonable amount of time.

In a similar manner, the user is preferably able to change sound segments included in the animation sequence, using control **51**. Preferably, sound files received from the user are passed to server **26**, where they are stored in conjunction with the pictures, text and list of changes.

In some preferred embodiments of the present invention, the above-described changes and data input may be made dependent upon a predefined condition. Thus, the user may, for example, choose to replace character **60** by a male character which is displayed when the animation sequence is viewed by a female visitor, and by a female character which is displayed to male visitors. Preferably, the condition is entered using the condition editor described hereinbelow.

Preferably, editing-window **38** further includes a sequence control **68**, which invokes a sequence editor for controlling the length and flow of the animation sequence, as described hereinbelow.

In an alternative preferred embodiment, not shown in the figures, a "Wizard" guides the user through the initial creation of the animation sequence. Such a Wizard presents the user with a series of guided questions and choices, as are known in the art, so that the animation sequence is initially created without the need for the user to use the interface tools and controls of window **38**. Thereafter, the user can make changes to the sequence using window **38**, if desired.

Table I below is an XML file, as is known in the art, defining the properties of Web page components to be created on-line by a user of the Web site described hereinabove, and then the implementation of these properties using specified HTML and JavaScript instructions which build up the animation sequence. The animation is carried out using a suitable Java player, which is downloaded implicitly to the computer of a visitor viewing the animation sequence. Further details regarding implementation of such a Java player are described in the above-mentioned U.S. patent application Ser. No. 08/819,607 and in U.S. patent application Ser. No. 09/121,062, which are assigned to the assignee of the present patent application and incorporated herein by reference. In the example given in Table I, the user creates an on-line "photo album," including animation effects, using editing window **38** or, most preferably, guided by the Wizard mentioned above.

The value of the parameter "hidden" with respect to each of the properties or property groups indicates whether the property is assigned by the system, i.e., automatically by the Web site, in which case hidden=1, or whether it is to be modified by the user by means of the Wizard, in which case hidden=0. For example, the property "baby's first name" in the seventh line of the table is a placeholder for the first name of a baby shown in an image, which is also incorporated in the photo album. The table indicates that the name, to be entered by the user, is a text string of up to 15 characters. An image of the baby is introduced by the property "current image." Similarly, the user can modify animations and sounds associated with the image by changing the "current animation" and "current sound" properties. As shown in the table, a number of different images and animation sequences can be incorporated in this manner.

TABLE I

```
<?xml version="1.0"?>
<Component ID="1"customization="step0.asp">
    <Properties>
        <PropertyGroup name="step0" hidden="0">
            <PropertyGroup name="Text" hidden="0 ">
                <SharedProperty name="first_name"
displayname="baby's first name" type="String" value="First
name" hidden="0" length="15"/>
                <SharedProperty name="family_name"
displayname="baby's last name" type="String" value="Last
name" hidden="0" length="15"/>
                </PropertyGroup>
            </PropertyGroup>
            <PropertyGroup name="step1" hidden="0">
            <SharedProperty name="p1" displayname="Current
image" type="Image" value="baby_maya.gif" hidden="0"
width="200" height="200"/>
            <SharedProperty name="animl"
displayname="Current animation" type="Animation"
```

TABLE I-continued

```
value="Fairy_flip.gif" hidden="0" width="60" height="60"/>
            <SharedProperty name="Click_sound"
displayname="Current sound" type="Sound" value="cameral.au"
hidden="0"/>
            <SharedProperty name="Ad_image_albumz"
displayname="Ad image_albumz" type="Image"
value="Ad_image_albumz.gif" hidden="1" width="176"
height="31"/>
            <SharedProperty name="Zapa_logo"
displayname="Zapa_logo" type="Image" value="zapa_logo.gif"
hidden="1" width="72" height="33"/>
            <PropertyGroup name="Text" hidden="0">
                <SharedProperty name="tl_1"
displayname="Picture 1 text" type="String" value="This text"
hidden="0" length="18"/>
                <SharedProperty name="tl_2" displayname=" "
type="String" value="goes along" hidden="0" length="18"/>
                <SharedProperty name="tl_3" displayname=" "
type="String" value="with your" hidden="0" length="18"/>
                <SharedProperty name="tl_4" displayname=" "
type="String" value="picture" hidden="0" length="18"/>
                <SharedProperty name="tl_5" displayname=" "
type="String" value=" " hidden="0" length="18"/>
                <SharedProperty name="tl 6_" displayname=" "
type="String" value=" " hidden="0" length="18"/>
            </PropertyGroup>
        </PropertyGroup>
        <PropertyGroup name="step2" hidden="0">
            <SharedProperty name="p2" displayname="Current
image" type="Image" value="200.gif" hidden="0" width="200"
height="200"/>
            <PropertyGroup name="Text" hidden="0">
                <SharedProperty name="t2_1"
displayname="Picture 2 text" type="String" value="This text"
hidden="0" length="18"/>
                <SharedProperty name="t2_2" displayname=" "
type="String" value="goes along" hidden="0" length="18"/>
                <SharedProperty name="t2_3" displayname=" "
type="String" value="with your" hidden="0" length="18"/>
                <SharedProperty name="t2_4" displayname=" "
type="String" value="picture" hidden="0" length="18"/>
                <SharedProperty name="t2_5" displayname=" "
type="String" value=" " hidden="0" length="18"/>
                <SharedProperty name="t2_6" displayname=" "
type="String" value=" " hidden="0" length="18"/>
            </PropertyGroup>
        </PropertyGroup>
        <PropertyGroup name="step3" hidden="0">
            <SharedProperty name="p3" displayname="p3"
type="Image" value="200.gif" hidden="0" width="200"
height="200"/>
            <SharedProperty name="anim3"
displayname="Current animation" type="Animation"
value="output.gif" hidden="0" width="60" height="60"/>
            <PropertyGroup name="Text" hidden="0">
                <Sharedproperty name="t3_1"
displayname="Picture 3 text" type="String" value="This text"
hidden="0" length="18"/>
                <SharedProperty name="t3_2" displayname=" "
type="String" value="goes along" hidden="0" length="18"/>
                <SharedProperty name="t3_3"displayname=" "
type="String" value="with your" hidden="0" length="18"/>
                <SharedProperty name="t3_4"displayname=" "
type="String" value="picture" hidden="0" length="18"/>
                <SharedProperty name="t3_5" displayname=" "
type="String" value=" " hidden="0" length="18"/>
                <SharedProperty name="t3_6" displayname=" "
type="String" value=" " hidden="0" length="18"/>
            </PropertyGroup>
        </PropertyGroup>
        <PropertyGroup name="step4" hidden="0">
            <SharedProperty name="p4"displayname="Current
image" type="Image" value="200.gif" hidden="0" width="200"
height="200"/>
            <PropertyGroup name="Text" hidden="0">
                <SharedProperty name="t4_1"
displayname="Picture 4 text" type="String" value="This text"
hidden="0" length="18"/>
                <SharedProperty name="t4_2" displayname=" "
type="String" value="goes along" hidden="0" length="18">
                <SharedProperty name="t4_3"displayname=" "
type="String" value="with your" hidden="0" length="18"/>
                <SharedProperty name="t4_4"displayname=" "
type="String" value="picture" hidden="0" length="18"/>
                <SharedProperty name="t4_5"displayname=" "
type="String" value=" " hidden="0" length="18"/>
                <SharedProperty name="t4_6"displayname=" "
type="String" value=" " hidden="0" length="18"/>
            </PropertyGroup>
        </PropertyGroup>
        <PropertyGroup name="step5" hidden="0">
            <SharedProperty name="p5" displayname="Current
image" type="Image" value="200.gif" hidden="0" width="200"
height="200"/>
            <SharedProperty name="anim5"
displayname="Current animation" type="Animation"
value="Elephant_2.gif" hidden="0" width="60" height="60"/>
            <PropertyGroup name="Text" hidden="0">
                <SharedProperty name="t5_1"
displayname="Picture 5 text" type="String" value="This text"
hidden="0" length="8"/>
                <SharedProperty name="t5_2" displayname=" "
type="String value="goes along"hidden="0"length="19"/>
                <SharedProperty name=" t5_3"displayname="
type="String" value="with your" hidden="0" length="18"/>
                <SharedProperty name="t5_4" displayname=" "
type="String" value="picture" hidden="0" length="18"/>
                <SharedProperty name="t5_5" displayname=" "
type="String" value=" " hidden="0" length="18"/>
                <SharedProperty name="t5_6" displayname=" "
type="String" value=" " hidden="0" length="18"/>
            </PropertyGroup>
        </PropertyGroup>
        <PropertyGroup name="step6" hidden="0">
            <PropertyGroup name="Text" hidden="0">
                <SharedProperty name="user_name"
displayname="Your name" type="String" value="Your name"
hidden="0" length="25"/>
                <SharedProperty name="personal_text1"
displayname="Your personal text" type="String" value="I made
this myself!" hidden="0" length="35"/>
                <SharedProperty name="personal_text2"
displayname=" " type="String" value="Make your own at
zapa.com" hidden="0" length="35"/>
                <SharedProperty name="user_email"
displayname="Your email" type="String"
value="support@zapa.com" hidden="0 " length="25"/>
            </PropertyGroup>
        </PropertyGroup>
    </Properties>
    <Implementations>
        <Variation name="var1">
            <Implementation type="General">
                <File source="Wrapper.js"/>
                <File source="Wrapper.htm"/>
                <File source="publish"/>
                <File source="gizmo.htm"/>
                <File source="preview.htm"/>
            </Implementation>
            <Implementation type="MS">
                <File source="params txt"/>
            </Implementation>
        </Variation>
    </Implementations>
</Component>
```

FIG. 4 is a schematic illustration of a Web page component description **80** stored on server **26**, in accordance with a preferred embodiment of the present invention. Description **80** comprises a reference **82** to the basic script chosen by the user. Preferably, description **80** includes a list **84** of changes made with respect to the basic script. Alternatively, reference **82** and list **84** are replaced by an actual copy of the script, and the changes from list **84** are entered into the script. Further alternatively, server **26** determines whether to store reference **82** or the actual copy of the script based on

the complexity of the changes entered by the user. Description **80** preferably further comprises a list **86** of data entered by the user, such as links, text segments, pictures, and sound files, as described hereinabove. Preferably, list **86** includes pointers to data files **88** annexed at the end of description **88**. Alternatively or additionally, the data is entered within list **86**.

FIG. **5** is a schematic illustration of an optional sequence editor interface **100**, in accordance with a preferred embodiment of the present invention. The sequence editor is used to alter the animation sequence by removing and/or adding scenes, and/or by adding flow directives, such as conditional branches into the sequence.

Preferably, interface **100** includes a selection control **102**, which is used to indicate a sub-sequence of the animation sequence that is to be manipulated by the editor. Preferably, selection control **102** allows the user to indicate the sub-sequence in terms of frames or scenes. Alternatively or additionally, the sub-sequence is defined in any other desired form. Preferably, when the sub-sequence is indicated in terms of scenes, interface **100** displays the frame numbers included in the scenes, so that the user may perform fine adjustment of the sub-sequence. Interface **100** preferably includes a plurality of controls **104**, **106** and **108**, which are used to manipulate the selected sub-sequence. Preferably, actuating control **104** deletes the sub-sequence from the animation sequence. Control **106** moves the selected sub-sequence to a different location in the animation sequence. Preferably, the new location is stated using an input field **110**, in which the new location is stated either according to scenes or frames.

Preferably, server **26** determines the precise lines of the script which correspond to the selected sub-sequence. In some preferred embodiments of the present invention, window **100** allows selection only of sub-sequences which are represented by modular parts of the script. Alternatively or additionally, server **26** determines lines of the script which must be duplicated when the sub-sequence is moved to the new location. Preferably, deletions and/or movements of sub-sequences are indicated in list **84** in description **80**. Alternatively, the deletions and/or movements are performed in the copy of the script.

Control **108** is preferably used to repeat the occurrence of the selected sub-sequence any desired number of times. A data entry window **112** is preferably used to enter the desired number of copies of the sub-sequence. Preferably, the user indicates in a check list **114** whether the repeated copies are to be identical, or whether the user plans to make changes, and to what extent. Accordingly, server **26** decides whether to repeat the sequence by inserting a "for-next" loop into the script, or by duplicating the lines of script corresponding to the selected sub-sequence.

Preferably, after the user operates control **104**, **106** or **108**, the animation sequence is immediately updated, and the frame numbers and/or scene numbers are re-allocated. Alternatively or additionally, the user may choose whether to re-allocate the frame and scene numbers or to assign a separate numbering scheme to newly added parts of the sequence. Preferably, the user is able to change the added parts of the sequence in the same way that the rest of the sequence is altered, as described hereinabove.

Preferably, interface **100** includes a command section **120** for adding conditional branch commands. Preferably, the user defines a scene after which the branch command is to be inserted in an input section **122**. An additional branch destination section **124** is preferably used to input the destination of the branch command. The destination is preferably stated either in terms of scenes or in terms of frames. The condition of the branch is preferably shown in a display window **126** and is preferably altered using a condition editor interface, which is invoked by a condition control **128**.

Preferably, other control commands may be added similarly to the animation sequence, such as sub-routine calls, loops, etc.

FIG. **6** is a schematic illustration of a condition editor interface **140**, in accordance with a preferred embodiment of the present invention. Condition editor interface **140** preferably comprises a selection window **150**, which shows the condition being prepared, on which the animation sequence is to branch. Preferably, the condition comprises one or more clauses connected by conjunction and/or disjunction operations.

Three sections **142**, **144** and **146** of interface **140** are used to prepare the clauses of the condition. Section **142** is used to select a variable upon which the clause depends, section **144** is used to select a comparison condition to be applied to the variable, and section **146** is used to select a value against which the variable is compared to complete the condition clause. Preferably, the condition clause can be made dependent on any suitable variable for which information is available on the server which is to host the Web page which includes the condition. The variable may depend, for example, on the name of the visitor, the visitor's preferences and hobbies, the visitor's address, the number of times the visitor visited the page and the number of total visits in the page. Alternatively or additionally, the variable may depend on the time, date and/or day of the week of the visit or on whether other visitors have visited within a predetermined period. Further alternatively or additionally, the variable may depend on the type and capabilities of the browser being used by the visitor, which is determined by the server using methods known in the art. For example, if the server determines that the browser does not support Java, it may instead download a "gif" animation, rather than a Java applet.

The condition is preferably stated using the logical operators greater than, smaller than, and equal, and their inverses. Alternatively or additionally, the condition may be stated as a range, according to the nature of the variable. In any case, the allowed values of the variable are dependent on the nature of the variable. Preferably, section **146** lists possible values, and the user chooses the desired values. Alternatively or additionally, the user enters the desired values.

When a clause has been completely defined, the user adds the clause to the condition by actuating an add button **152**. The clause is added to the condition shown in window **150** with a context operator (or, and) selected by the user in a section **154**. Preferably, the user selects whether the context operator is applied between the new clause shown in section **146** and the most recent preceding clause, or between the new clause and all the previous clauses. To enter the condition, the user preferably actuates a "done" control **156**.

FIG. **7** is a flow chart that schematically illustrates the actions of a user of processor **20** in preparing a dynamic Web page component, in accordance with a preferred embodiment of the present invention. In the context of the present patent application and in the claims, a "dynamic page component" is a Web page component which has a single address but shows different displays according to input about the viewer and/or the circumstances in which the viewer accesses the page. Thus, a user may prepare a

dynamic page component which changes according to the identity of the viewer, the time and date when the viewer accesses the page, and/or any other conditions. Preferably, the user creates a plurality of Web page components each of which is assigned a unique label. Preferably, the Web page components are prepared in accordance with the methods described hereinabove, although other suitable methods may also be used. Alternatively or additionally, the components are imported into server **26** from an external source. Further alternatively or additionally, one or more of the plurality of Web page components used to form the dynamic Web page are not actually situated on server **26** but are only referenced by their URL address. Preferably, the condition editor of FIG. **6** is used to determine which of various ones of the plurality of Web page component are to be presented under different predetermined conditions.

Reference is also made to FIG. **8**, which is a schematic illustration of an interface **160** to a dynamic page component editor, in accordance with a preferred embodiment of the present invention. Interface **160** displays, for a single URL address, a list **166** of pairs **163**, each pair including a condition **162** and a page component identity **164** of a page component which is to be displayed if the condition is fulfilled. Preferably, a default page component **169** is defined for cases in which none of conditions **162** are fulfilled. Preferably, the user defines an order of precedence of pages **164** in case more than one of conditions **162** is fulfilled for a single visitor, most preferably according to the order of pages in list **166**.

A frame **168** enables the user to add pairs **163** to list **166**. Preferably, the user enters a condition **162** using the condition editor described above with respect to FIG. **6**.

A page component field **170** allows the user to invoke a pre-created page by name. Alternatively or additionally, the user actuates control **172** which invokes a page component editor to create a new Web page component, for example, the page component editor described hereinabove. Further alternatively or additionally, the user may identify an external page component using a URL address. Preferably, a field **174** allows the user to specify the position of pair **163** in list **166**, in accordance with the priority of the pair. Alternatively, methods of "drag and drop" editing may be used, as are known in the art, to create list **166**.

A field **176** in interface **160** is preferably used to state the URL address of the dynamic page component. Preferably, the address is assigned to the user by server **26**. Alternatively or additionally, the user can define the URL address of the dynamic page component.

The dynamic page component is then placed on a server, where it is accessible for viewing by visitors, as is known in the art. Preferably, the dynamic page component is located on a server which receives and stores information about some or all of the visitors to the page. The visitors may provide the information to the server when connecting for a first time to a home page on the server. At later times the visitor may be asked to provide a name or other identification when connecting to the server. Alternatively or additionally, the server determines the address and/or user name under which the visitor connects to the server.

When a visitor connects to the server and requests to view a dynamic page, the server determines which of the sequences included in the dynamic page component is to be displayed. Preferably, the server checks the conditions **162** in list **166** of the dynamic page component, and the page component displayed corresponds to the first condition **162** which is fulfilled. Information relative to the conditions may be obtained from the visitor using any suitable method known in the art. For example, the visitor may be prompted to enter a name and/or password, and possibly to answer further questions about his/her identity and preferences. The server may also record a "cookie" on the visitor's disk, as is known in the art, in order to identify the visitor and retrieve stored identification information during subsequent visits to the page.

As described hereinabove, the user of the Web site creates the dynamic Web page component by selecting elements and attributes to be applied to one of the basic animation sequences available at the site, such as that described in Table I. Typically, such sequences are created and supplied to the user by an operator of the Web site.

FIG. **9** is a flow chart that schematically illustrates a method for creating templates for dynamic Web page components, in accordance with an alternative embodiment of the present invention. This method enable "power users" of the Web site to create their own basic animation sequences and, optionally, to post such sequences at the site, where they may be selected by other users. Preferably, the templates are created and modified using techniques described in the above-mentioned U.S. patent application Ser. No. 09/121,062.

The "power user" receives a software package which enables him or her to access a library of templates and select one of the templates to work on. The templates themselves comprise animation sequences, as described hereinabove and in U.S. patent application Ser. No. 09/121,062, with predefined placeholders embedded in them to receive objects for inclusion in the animation. The user can then modify the template by changing substantially all of its attributes other than the placeholders. For example, the user can insert completely new graphics, or can modify the motion path of one of the animated objects. These are changes that typically would not be available to users creating dynamic Web page components online, as described with reference to the preceding figures.

After creating the new template, the user can upload it to the Web site, where the template is stored under an appropriately-assigned category. Subsequently, online users are able to create their own new components based on the new template.

Those skilled in the art will appreciate that software for performing the functions described hereinabove can be sold and/or distributed on media, such as diskettes or CD-ROM, as well as in a medialess format via a network, for example. It will be appreciated generally that the preferred embodiments described above are cited by way of example, and the full scope of the invention is limited only by the claims.

What is claimed is:

1. A method for creating a Web page component, comprising:

opening a remote connection to a server provided with a plurality of basic animation sequences represented by corresponding files in a markup language held on the server, the sequences having variable attributes represented by placeholder tags in the markup language files;

choosing, via the connection, at least one of the basic animation sequences to be used in the Web page component;

changing one or more of the variable attributes of the chosen animation sequence by inputting, over the remote connection to the server, values to be assigned to the corresponding placeholder tags; and

posting the Web page component including the animation sequence with the changed attributes to a Web page.

2. method according to claim 1, wherein opening the remote connection comprises opening a connection over the Internet.

3. A method according to claim 1, wherein choosing the at least one animation sequence comprises choosing an animation sequence which substantially covers an entire Web page.

4. A method according to claim 1, wherein changing one or more of the attributes of the animation sequence comprises inserting data into the animation sequence.

5. A method according to claim 4, wherein inserting data into the animation sequence comprises inserting images.

6. A method according to claim 4, wherein inserting data into the animation sequence comprises inserting hypertext links.

7. A method according to claim 1, wherein changing one or more of the attributes of the animation sequence comprises changing a color setting in the animation sequence.

8. A method according to claim 1, wherein changing one or more of the attributes of the animation sequence comprises changing a character which appears in the animation sequence.

9. A method according to claim 1, wherein the animation sequence comprises a plurality of frames in a predetermined order and wherein changing one or more of the attributes comprises manipulating the frames in the sequence.

10. A method according to claim 9, wherein manipulating the frames in the sequence comprises deleting one or more frames from the animation sequence.

11. A method according to claim 9, wherein manipulating the frames in the sequence comprises repeating one or more frames in the animation sequence.

12. A method according to claim 1, wherein changing one or more of the attributes of the animation sequence comprises assigning to at least one of the one or more attributes a plurality of values which are respectively chosen responsive to a condition evaluated when the Web page component is viewed.

13. A method according to claim 1, wherein changing one or more of the attributes of the animation sequence comprises adding conditional flow directives to the animation sequence.

14. A method according to claim 1, wherein posting the Web page component comprises posting a link to the animation sequence.

15. A method according to claim 13, wherein posting the Web page component comprises posting a list of the changes performed on the animation sequence.

16. A method according to claim 1, wherein posting the Web page component comprises posting a Web page component which does not require any proprietary software in order to be viewed by a viewer.

17. A method according to claim 1, wherein changing the one or more attributes does not require use of any proprietary software.

18. A method for creating a Web page component, comprising:

providing a plurality of basic animation sequences represented by corresponding files in a markup language held on a server, the sequences having variable attributes represented by placeholder tags in the markup language files;

receiving from a remote processor a selection of at least one of the basic animation sequences to be used in the Web page component;

changing one or more of the attributes of the chosen animation sequence responsive to an input from the remote processor to the server of values to be assigned to the corresponding placeholder tags; and

posting the Web page component including the animation sequence with the changed attributes to a Web page.

19. A method according to claim 18, wherein providing the plurality of basic animation sequences comprises receiving an animation template uploaded to the server by a user.

20. A method according to claim 18, wherein changing one or more of the attributes comprise s inserting data into the sequence.

21. A method according to claim 18, wherein changing one or more of the attributes of the animation sequence comprises changing a color setting in the animation sequence.

22. A method according to claim 18, wherein the animation sequence comprises a plurality of frames in a predetermined order and wherein changing one or more of the attributes comprises manipulating the frames in the sequence.

23. A method according to claim 18, wherein changing one or more of the attributes of the animation sequence comprises assigning to at least one of the one or more attributes a plurality of values which are respectively chosen responsive to a condition evaluated when the Web page component is viewed.

24. A method according to claim 18, wherein changing one or more of the attributes comprises adding conditional flow directives to the animation sequence.

25. A method according to claim 18, wherein posting the Web page component comprises posting a link to the animation sequence.

26. A method according to claim 25, wherein posting the Web page component comprises posting a list of the changes performed on the animation sequence.

27. A method according to claim 18, wherein posting the Web page component comprises posting a Web page component which does not require any proprietary software in order to be viewed by a viewer.

28. A method according to claim 18, wherein changing the one or more parameters does not require installing any proprietary software on the processor.

29. Apparatus for creating a Web page component, comprising:

a server which displays a plurality of basic animation sequences represented by corresponding files in a markup language held on the server, the sequences having variable attributes represented by placeholder tags in the markup language files, and which allows a user of a remote processor to select at least one basic animation sequence and change one or more of the variable attributes of the sequence by inputting values to be assigned to the corresponding placeholder tags; and

a communication interface which receives a connection from the remote processor to the server, whereby the user thereof selects the sequence and inputs the values to be assigned to the placeholder tags.

30. Apparatus according to claim 29, wherein the at least one basic animation sequence covers an entire Web page.

31. Apparatus according to claim 29, wherein the one or more attributes comprise colors associated with the sequence.

32. Apparatus according to claim 29, wherein the server allows addition of data into the sequence by the user.

33. Apparatus according to claim 29, wherein the animation sequence includes a plurality of frames, and the server allows the user to manipulate the frames.

34. Apparatus according to claim 33, wherein the server allows the user to delete frames.

35. Apparatus according to claim 33, wherein the server allows the user to duplicate frames.

36. Apparatus according to claim 29, wherein the server assigns a plurality of values to the one or more attributes together with a scheme which determines which of the values is to be used each time the Web page component is displayed.

37. Apparatus according to claim 29, wherein the server adds a conditional flow directive to the sequence responsive to a command from the user.

38. Apparatus according to claim 29, wherein the server allows the user to select and change the sequence using substantially only non-proprietary software.

39. A software package for creating Web page components, comprising an executable file on a machine readable medium which is run by a server having a communication interface adapted to receive a connection from a remote processor, such that running the file causes the server to display on a Web page a selected basic animation sequence from among a plurality of basic animation sequences represented by corresponding files in a markup language held on the server and having variable attributes represented by placeholder tags in the markup language files, responsive to selection of the sequence by a user of the remote processor via the connection, and causes the server to allow the user to change one or more of the variable attributes of the selected sequence by inputting values to the server via the connection to be assigned to the corresponding placeholder tags.

40. A software package according to claim 39, wherein the variable attributes comprise one or more attributes selected from a group of attributes that includes colors, characters, pictures, texts, links, and sound files.

41. A software package according to claim 39, and comprising a plurality of data files which include data representative of the basic animation sequences.

42. A software package according to claim 41, wherein the executable file performs changes to the animation sequence by changing a copy of a respective one of the data files.

43. A software package according to claim 41, wherein the executable file performs changes to the animation sequence by associating a list of changes with a pointer to a respective one of the data files.

* * * * *

US005506755A

United States Patent [19]

Miyagi et al.

[11] Patent Number: 5,506,755

[45] Date of Patent: Apr. 9, 1996

[54] **MULTI-LAYER SUBSTRATE**

[75] Inventors: **Takeshi Miyagi**, Fujisawa; **Kazuhiro Matsumoto**; **Tomiya Sasaki**, both of Yokohama; **Hideo Iwasaki**, Kawasaki; **Katsumi Hisano**, Yokohama, all of Japan

[73] Assignee: **Kabushiki Kaisha Toshiba**, Kanagawa, Japan

[21] Appl. No.: **291,508**

[22] Filed: **Aug. 18, 1994**

Related U.S. Application Data

[63] Continuation of Ser. No. 29,656, Mar. 10, 1993, abandoned.

[30] **Foreign Application Priority Data**

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Mar. 26, 1992 [JP] Japan 4-068009

[51] **Int. Cl.**[6] **H05K 7/20**

[52] **U.S. Cl.** **361/720**; 174/252; 257/712; 257/723; 361/792

[58] **Field of Search** 174/16.3, 252; 257/706–707, 712, 717, 723–724; 361/704, 707, 712, 717–723, 778, 792–794

[56] **References Cited**

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4,855,537 8/1989 Nakai et al. 174/68.5

FOREIGN PATENT DOCUMENTS

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303745 7/1989 Japan 361/386

Primary Examiner—Gregory D. Thompson
Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett & Dunner

[57] **ABSTRACT**

A multi-layer wiring substrate includes an aluminum nitride ceramic substrate, a multi-layer wiring part having an electric insulating layer of an organic polymer, a die pad for mounting thereon an electronic part, and a thermal via of a column shape for effectively dissipating heat generated in the mounted electric part. The multi-layer wiring part is integrally formed on the ceramic substrate. The die pad is provided on a surface of the multi-layer wiring part. One end of the thermal via connects to the die pad, while the other end of the thermal via passes through the multi-layer wiring part and extends at least to the ceramic substrate. The thermal via is electrically insulated from the multi-layer wiring part. In the second multi-layer wiring substrate, at least one of end portions of the above thermal via is wider than a section of the other portion of the thermal via, resulting in further improvement of the heat dissipating property.

11 Claims, 5 Drawing Sheets

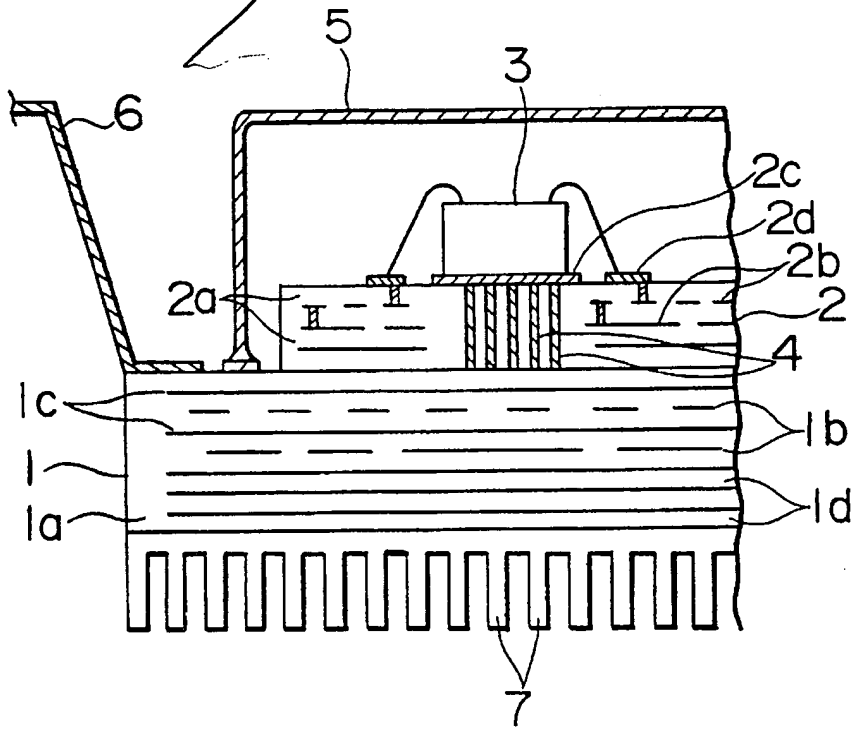


FIG. 1

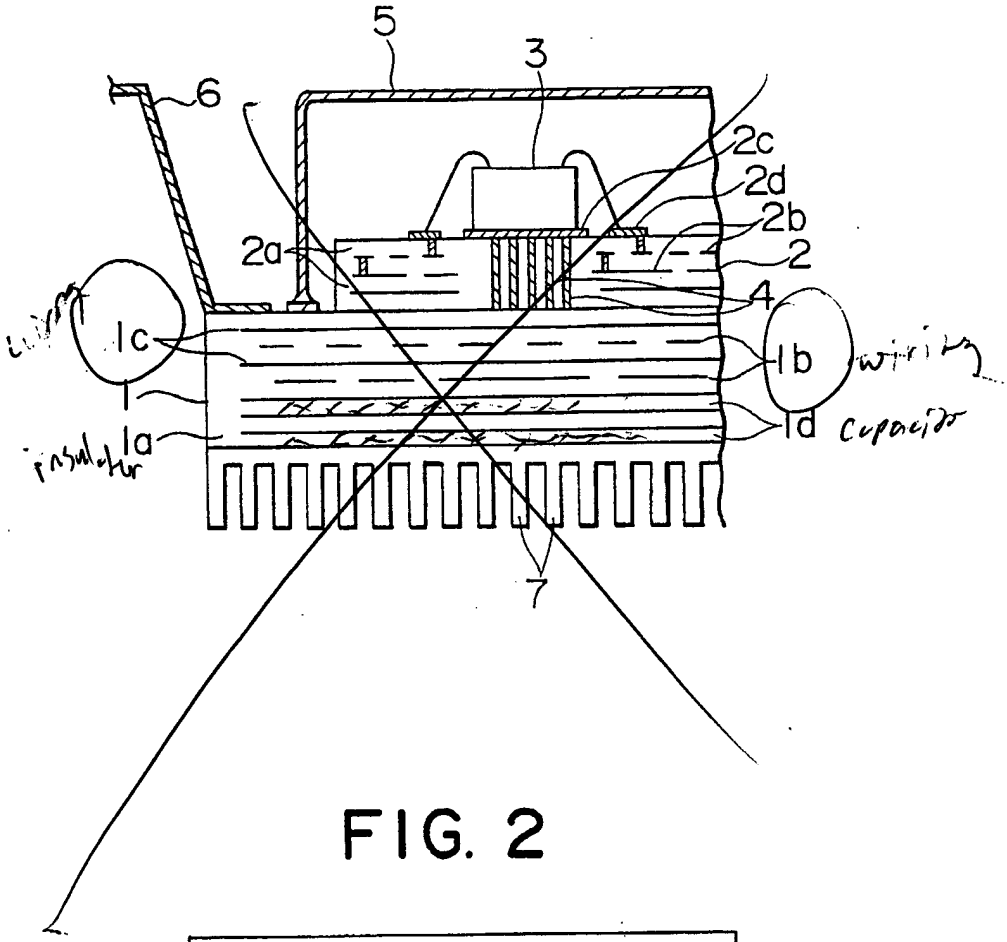

5
3
6
2c
2d
2b
2a
2
4
1c
1b
1d
1a
7

FIG. 2

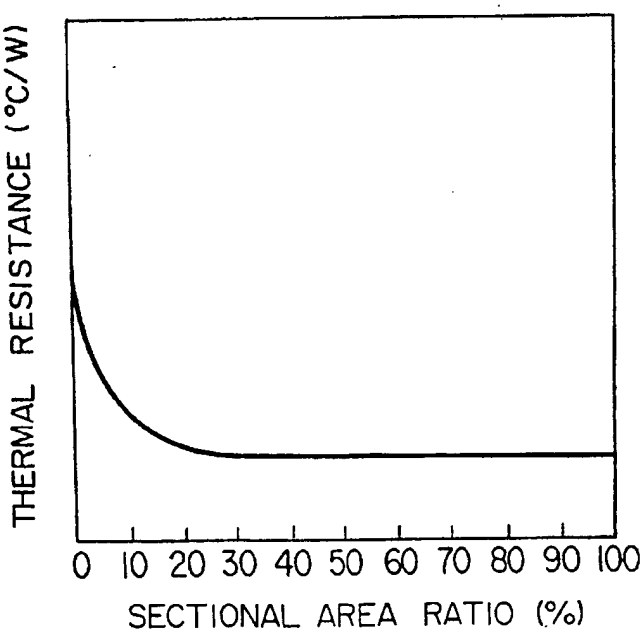

THERMAL RESISTANCE (°C/W)
0 10 20 30 40 50 60 70 80 90 100
SECTIONAL AREA RATIO (%)

FIG. 3

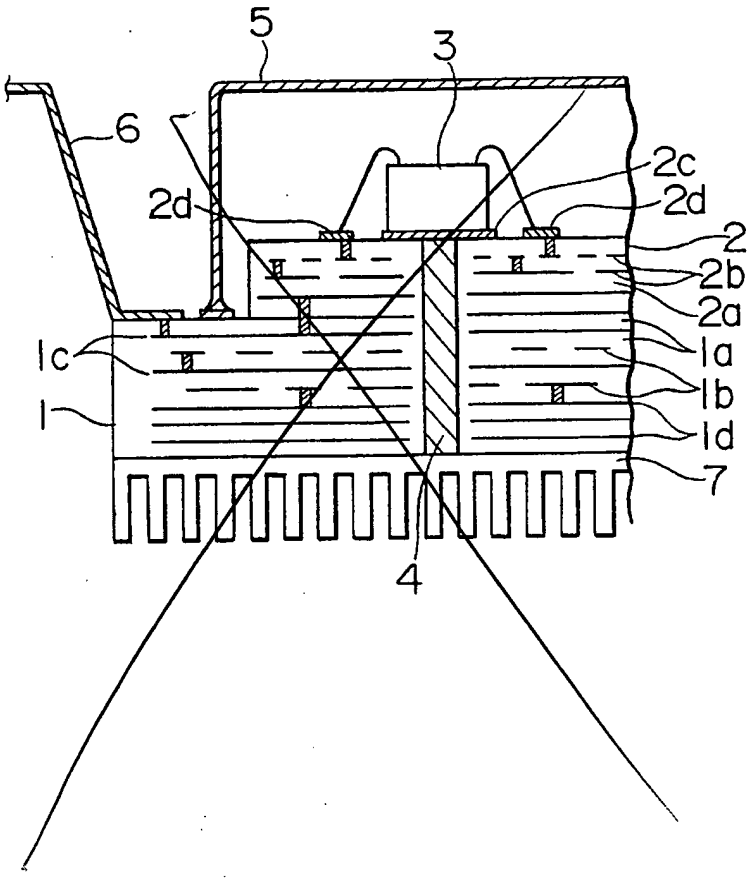


FIG. 4

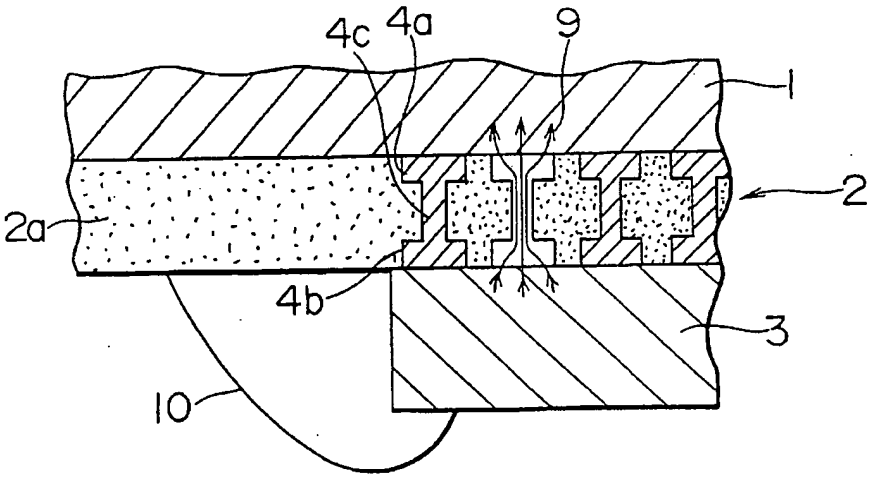


FIG. 5

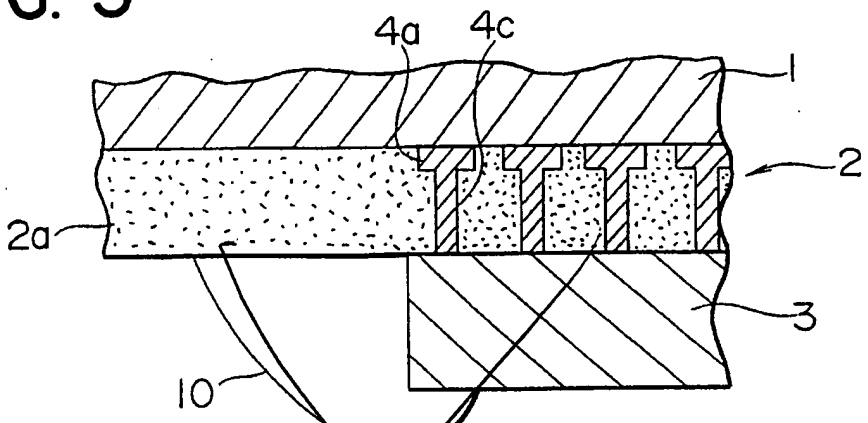


FIG. 6

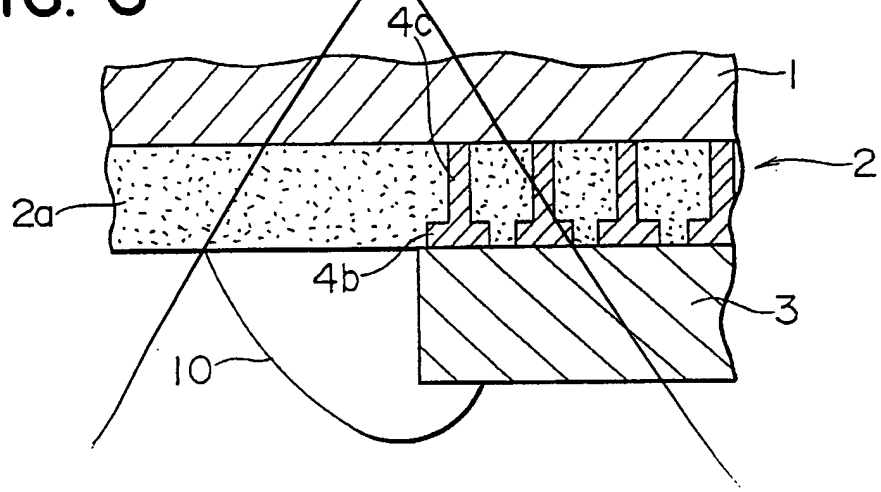


FIG. 7

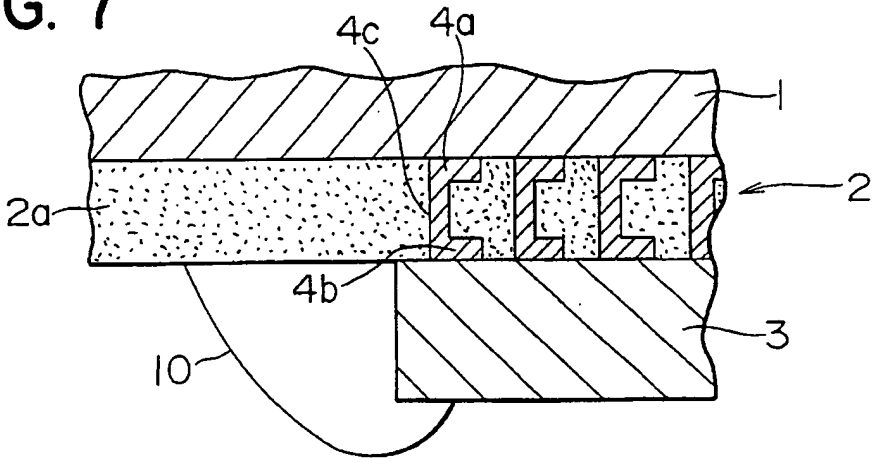


FIG. 8

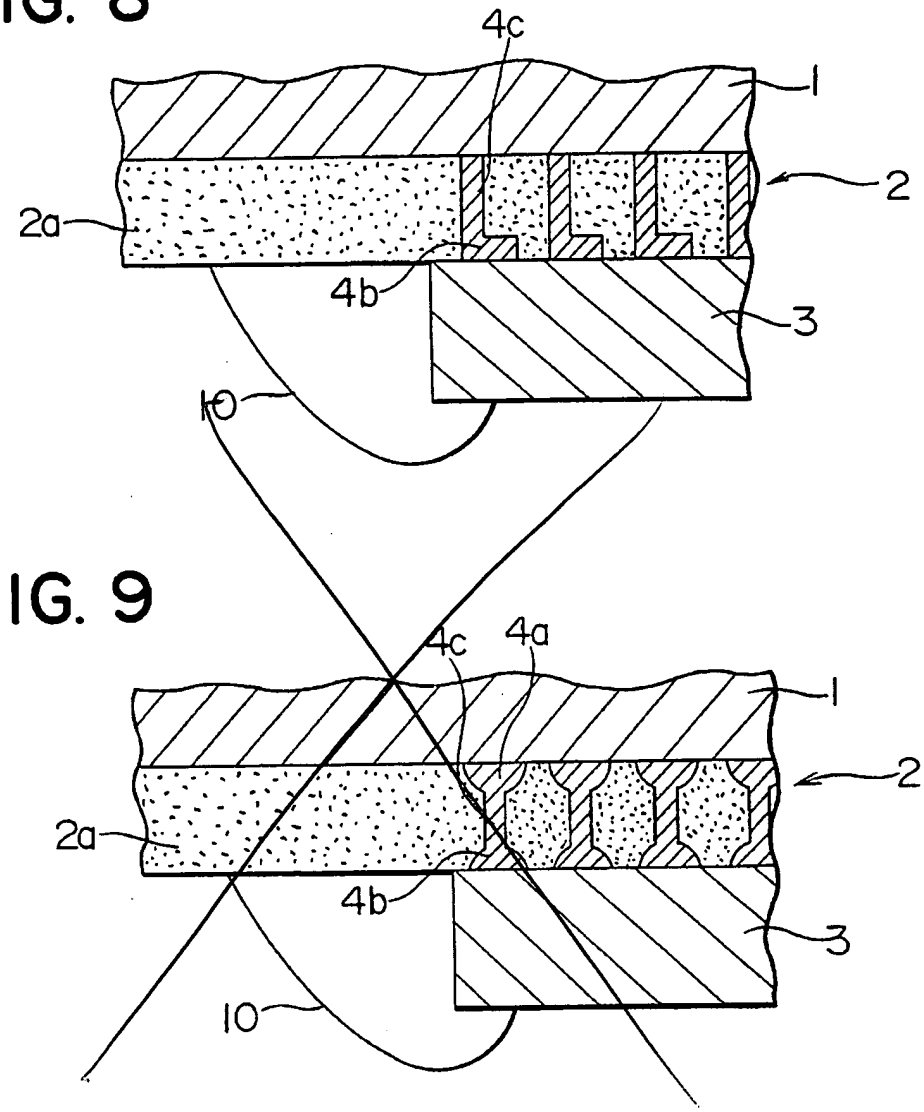
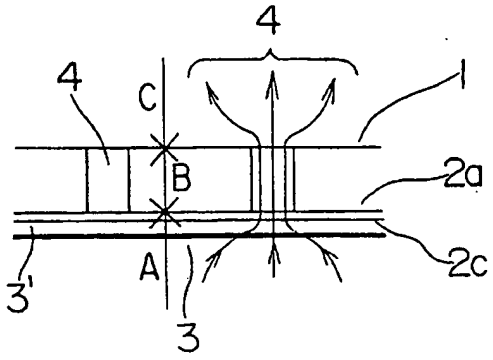


FIG. 9

FIG. 10



IFW / AF

Doc Code: TRAN.LET

Document Description: Transmittal Letter

CPAP YAKIMA-9
AUG 19 2013
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	32

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
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- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
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- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☑ Other Enclosure(s) (please Identify below):

return receipt postcard; Response (31 pages).

Remarks

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Firm Name	Uriarte Law		
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Date	14 August 2013	Reg. No.	39,955

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/876,113	Filing Date 09/04/2010	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **08/19/2013**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 97	Minus	** 97	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 5	Minus	***5	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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/BRENDA HARRISON/

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12/876,113	09/04/2010	Ricardo H. BRUCE	6005.042	1607

64180 7590 09/06/2013

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EXAMINER	
RUTZ, JARED IAN	

ART UNIT	PAPER NUMBER
2187	

NOTIFICATION DATE	DELIVERY MODE
09/06/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

stephen@uriartelaw.com
labid@uriartelaw.com
arnold@uriartelaw.com

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 12/876,113	**Applicant(s)** BRUCE ET AL.	
	Examiner JARED RUTZ	**Art Unit** 2187	**AIA (First Inventor to File) Status** No

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 19 August 2013 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

NO NOTICE OF APPEAL FILED

1. ☒ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires *3* months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
   c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection. The current period for reply expires months from the mailing date of *the prior Advisory Action* or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.
   Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANT'S FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   b) ☐ They raise the issue of new matter (see NOTE below);
   c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): (a) ☐ will not be entered, or (b) ☒ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
9. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
10. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
11. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

12. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: see continuation sheet.
13. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
14. ☐ Other: _____.

STATUS OF CLAIMS

15. The status of the claim(s) is (or will be) as follows:
    Claim(s) allowed: .
    Claim(s) objected to: .
    Claim(s) rejected: 1-97.
    Claim(s) withdrawn from consideration: .

/Jared I Rutz/
Primary Examiner, Art Unit 2187

Claims 1-97 are rejected on the same grounds and art as presented in the final rejection mailed 5/14/2013.

Continuation of 12: With respect to Applicant's argument that the logical sections are not addressable sections, see the third paragraph beginning on page 24 of the remarks submitted 8/19/2013, the Examiner respectfully disagrees. Initially, the Examiner respectfully notes that Applicant has misconstrued the disclosuer of Falik. As discussed at column 14 lines 51-65 shows that the address space of each of logical block MB 51 and IB 52 are divided into a plurality of sections 57 and 58. Accordingly, the logical blocks are divided into sections, as illustrated in figure 3. Column 14 lines 51-65 shows that the addresses within any one section of the address space are mapped to a corresponding section of the memory device. Accordingly Falik teaches that the sections 57 and 58 are addressible. As the sections represent portions of the address space, they each contain a plurality of addressable memory locations.

With respect to applicant's argument that the registers contain information directed to the same entire memory device and not directed to different memory locations, see the first paragraph beginning on page 25 of the remarks submitted 8/19/2013, the Examiner respectfully disagrees. Falik column 20 lines 49-55, discussing the section properties register, expressly states "There is one such register for each of the sections in the device". As discussed at column 15 line 63 through column 16 line 19, the information stored in the section capabilities register is used to control the operation of accesses within the memory arrays.

In the second paragraph beginning on page 26 through the first paragraph beginning on page 30 of the remarks submitted 8/19/2013, Applicant argues that claims 2-97 are allowable for the same reasons as claim 1. The Examiner respectfully disagrees for the reasons presented supra with respect to claim 1.

OPAP AUG 19 2013 AKIMA-9 PATENT & TRADEMARK OFFICE

Attorney Docket: 6005.042

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Ricardo H. Bruce, et al.	Confirmation No.: 1607
Serial No.: 12/876,113	Examiner: Jared Ian Rutz Ph: 571-272-5535
Filing Date: Sept. 4, 2010	Art Unit: 2187
Title: Multi-Profile Memory Controller For Computing Devices	Atty. Docket No.: 6005.042

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO FINAL OFFICE ACTION AND AMENDMENT

Sir:

The following is in response to the final office action mailed on 14 May 2013.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 24 of this paper.

OK TO ENTER: /J.R./

OPAP AKIMA-2
OCT 2 1 2013
PATENT & TRADEMARK OFFICE

1 RCE

PTO/SB/30 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Request for Continued Examination (RCE) Transmittal

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

   a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

      i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

      ii. ☐ Other _____

   b. ☑ Enclosed

      i. ☑ Amendment/Reply

      ii. ☐ Affidavit(s)/ Declaration(s)

      iii. ☐ Information Disclosure Statement (IDS)

      iv. ☐ Other _____

2. Miscellaneous

   a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

   b. ☐ Other _____

3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

   a. ☐ The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Deposit Account No. _____.

      i. ☐ RCE fee required under 37 CFR 1.17(e)

      ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)

      iii. ☐ Other _____

   b. ☐ Check in the amount of $ _____ enclosed

   c. ☑ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature		Date	15 October 2013
Name (Print/Type)	Arnold de Guzman	Registration No.	39,955

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature			
Name (Print/Type)	Arnold de Guzman	Date	15 October 2013

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Document Code: IMIS

Notice of Fee Due

Application Number: 12876113 Date: 10-21-13

Fees are due for the application or document dated 10-21-13. The payment was not collectable for the reason indicated below.

Note: If the fee due is for any of the filing fees, the surcharge for late payment of the filing fees is now due as well.

- ☐ Insufficient payment by check or money order.
- ☐ No authorization to charge a deposit account.
- ☐ Invalid deposit account number.
- ☐ User name not listed in deposit account _____ at ____:____ (time).
- ☐ Insufficient funds in deposit account _____ at ____:____ (time).
- ☐ Insufficient payment by credit card.
- ☒ Declined credit card 11:54 A-M (time).

Fee code(s) to be applied:	1821	$ 120000
	1252	$ 60000
		$
		$
		$
Amount in holding fee code:	1506	$
	1622/2622	$
	1206/2206	$
	1999	$

Total remaining due from applicant: $ 180000

RAM Operator E E

Rev. 04/10/2013

Unsuccessful Authorization

Date: 10-21-2013

User ID: EEKUBAY1

Processing Center Response

Charge was declined

Local Response

The card has been declined, the transaction will not be processed.

Retry | Dial | New Card | Cancel | Print Screen

12876113

11:54 Am

10/21/13

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OCT 2 1 2013
PATENT & TRADEMARK OFFICE

Doc Code: TRAN.LET
Document Description: Transmittal Letter

PTO/SB/21 (07-09)
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	35

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☑ Other Enclosure(s) (please Identify below):

return receipt postcard; Amendment (32 pages); signed/dated PTO-2038 authorizing payment of $1800 (1 page); RCE (1 page)

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Uriarte Law		
Signature			
Printed name	Arnold de Guzman		
Date	15 October 2013	Reg. No.	39,955

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature			
Typed or printed name	Arnold de Guzman	Date	15 October 2013

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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OPAP AKIMA-2
OCT 2 1 2013
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Ricardo H. Bruce, et al.	Confirmation No.: 1607
Serial No.: 12/876,113	Examiner: Jared Ian Rutz Ph: 571-272-5535
Filing Date: Sept. 4, 2010	Art Unit: 2187
Title: Multi-Profile Memory Controller For Computing Devices	Atty. Docket No.: 6005.042

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO FINAL OFFICE ACTION AND AMENDMENT

Dear Sir:

The following is in response to the final office action mailed on 14 May 2013. An RCE is being filed herewith.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 24 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising:

addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile, wherein a memory read transaction or a memory write transaction is performed on at least one of the first memory location or second memory location, wherein data is transferred to the first memory location or second memory location for a memory write transaction, wherein data is transferred from the first memory location or second memory location for a memory read transaction;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

using attributes from said first and second device profiles.

2. (original) The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device.

3. (original) The method of claim 1, wherein said difference between said first and second device profiles includes different attributes; and said addressing said first memory location is made in response to a first memory transaction request; and

further including addressing said second memory location.

4. (original) The method of claim 1, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes.

5. (original) The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

6. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute values.

7. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute types.

8. (original) The method of claim 5, wherein said shared attributes include a memory device type attribute.

9. (original) The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

10. (original) The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

11. (original) The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

12. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

13. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of attributes that differs in value from a second page size attribute from said second set of attributes.

14. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes.

15. (original) The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device, and said second memory device interface attribute corresponds to a DRAM device interface.

16. (original) The method of claim 2, wherein said using attributes from said first and second device profile further includes using a first partial page size attribute from said first set of attributes that differs in value from a second partial page size attribute from said second set of attributes.

17. (original) The method of claim 16:

said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute; and

further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute.

18. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

19. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a NAND flash memory device and said second memory device type attribute corresponds to a NOR flash memory device.

20. (original) The method of claim 2, further including:

using an address corresponding to a memory location from said first memory device and transferring a first data set, and

using an address corresponding to a memory location from said second memory device and transferring a second data set.

21. (original) The method of claim 20, wherein:

said first set of attributes includes a first page size attribute, and said first data set includes a first data set size; and

if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size.

22. (original) The method of claim 20, wherein:

said second set of attributes includes a second page size attribute, and said second data set includes a second data set size; and

if said second data set size is greater than said second page size attribute, said transferring said second data set includes:

performing a set of write operations on said second memory device that includes using a second transfer size equal to said second page size attribute until a remaining portion of said second data set that has not yet been written to said second device is less than said second page size attribute, and

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

23. (currently amended) The method of claim 20, wherein:

said first set of attributes includes a page size attribute and a block size attribute;

said first data set includes a first data set size;

if said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes:

performing a set of write operations on said first memory device that includes using a second transfer size equal to said page size attribute until a remaining portion of said first data set that has not yet been written to said first device is less than said page size attribute,

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size[[;]].

24. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes:

performing respective write operations on said first and second memory devices by at least using a transfer size at least equal to a partial page size attribute from said first set of attributes and performing at least one write operation on said second memory device by at least using a transfer size at least equal to a partial page size attribute value from said second set of attributes; and

said attribute difference includes different attribute values of said first and second partial page size attributes.

25. (original) The method of claim 1, wherein said using attributes from said first and second device profile

further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size attribute of said first memory device.

26. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a block size attribute value that corresponds to a block size attribute of said first memory device.

27. (original) The method of claim 26, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

28. (original) The method of claim 2, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

29. (previously presented) A non-transitory computer readable medium comprising computer executable instructions adapted to cause a method of performing memory transactions on a first memory location and a second memory location, said method comprising:

addressing a first memory location, said first memory location and a second memory location are respectively

associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory device, and said second device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles; and

using attributes from said first and second device profiles.

30. (original) The computer readable medium of claim 29, wherein:

said first memory location is part of a memory space associated with a first memory device;

said second memory location is part of a memory space associated with a second memory device; and

said first and second memory devices comprise at least a portion of a memory store.

31. (previously presented) The computer readable medium of claim 29, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of a first memory device and a block size value of a second memory device.

32. (previously presented) The computer readable medium of claim 30, wherein at least one attribute of said

attributes includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

33. (original) The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

34. (original) The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes.

35. (previously presented) The computer readable medium of claim 29, wherein said addressing further includes:

said first and second device profiles having at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

36. (original) The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

37. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values.

38. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types.

39. (original) The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute.

40. (original) The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

41. (original) The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

42. (original) The computer readable medium of claim 36, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

43. (original) The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes.

44. (original) The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device.

45. (previously presented) A memory controller for performing memory transactions, said memory controller comprising:

a means for addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile;

wherein said means for addressing includes an interface controller means for processing memory transaction requests;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said means for addressing uses attributes from said first and second device profiles.

46. (original) The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

47. (original) The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

48. (original) The memory controller of claim 46, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said use of said attributes from said first and second device profiles by said means for addressing includes using said different attribute qualifiers for said shared attributes.

49. (original) The memory controller of claim 46, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

50. (previously presented) The memory controller of claim 45, wherein said means for addressing further includes a means for addressing said second memory location.

51. (original) The memory controller of claim 45, wherein said difference includes different attribute qualifiers for

at least one set of shared attributes from said first and second device profiles.

52. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values.

53. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types.

54. (original) The memory controller of claim 51, wherein said shared attributes include a memory device type attribute.

55. (original) The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

56. (original) The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

57. (original) The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

58. (original) The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device.

59. (original) A memory controller comprising:

an interface controller coupled to a memory device interface and an IO device interface;

said interface controller disposed to perform a memory transaction by addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile;

said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said addressing of said first memory location includes using said attributes from said first device profile.

60. (original) The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile.

61. (previously presented) The memory controller of claim 59, wherein said interface controller includes:

a main control device coupled to said memory device interface and to a data path;

a first memory bus controller coupled to said control device and said memory device interface; and

an IO bus controller coupled to said IO device interface and said control device.

62. (previously presented) The memory controller of claim 61, wherein said IO bus controller is disposed to respond to a memory transaction request by acknowledging said request and providing status to said main control device.

63. (original) The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction, coordinates the operation of said memory device interface, and manages the transfer of memory transaction data between said IO device interface and said memory device interface through a data path.

64. (previously presented) The memory controller of claim 59, further including a buffer comprising a FIFO and a data path that includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface.

65. (original) The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots.

66. (original) The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a plurality of queue slots that buffer data from said IO device interface to said memory device interface.

67. (original) The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from said memory device interface to said IO device interface.

68. (previously presented) The memory controller of claim 59, further including a second memory bus controller coupled to a main control device and said memory device interface.

69. (original) The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes.

70. (original) The memory controller of claim 59, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

71. (original) The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

72. (original) The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute.

73. (original) The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values.

74. (original) The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values.

75. (original) The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type.

76. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values.

77. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types.

78. (original) The memory controller of claim 71, wherein said shared attributes include a block size attribute, and

said different attribute qualifiers include different block size values.

79. (original) The memory controller of claim 71, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

80. (original) An electronic storage device, comprising:

a memory controller disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and

said memory controller using attributes from said first and second device profiles.

81. (original) The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

82. (original) The electronic storage device of claim 80, wherein said first memory location is located in a first

memory device and said second memory location is located in a second memory device.

83. (previously presented) The electronic storage device of claim 80, said memory controller further disposed to:

perform a write operation on said first memory device, if a memory transaction request is associated with a write request;

perform a read operation on said first memory device, if said memory transaction request is associated with a read request; and

wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using said second device profile in response to receiving a second memory transaction request.

84. (original) The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

85. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values.

86. (original) The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute.

87. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types.

88. (original) The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said shared attributes.

89. (original) The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device.

90. (original) The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

91. (original) The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

92. (original) The electronic storage device of claim 84, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

93. (original) The electronic storage device of claim 80, wherein said memory controller is further adapted to:

use a first partial page size attribute by performing a write operation on said first memory device and using a

transfer size at least equal to said partial page size attribute; and

use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute.

94. (previously presented) The method of claim 1, wherein the first memory location and the second memory location are addressable memory locations.

95. (previously presented) The memory controller of claim 45, wherein the first memory location and the second memory location are addressable memory locations.

96. (previously presented) The memory controller of claim 59, wherein the first memory location and the second memory location are addressable memory locations.

97. (previously presented) The electronic device of claim 80, wherein the first memory location and the second memory location are addressable memory locations.

REMARKS/ARGUMENTS

Claim Rejections

35 USC 102

Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-97

Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-97 are rejected under 35 U.S.C. 102(e) as allegedly being anticipated by US 8,200,879 to Falik et al. ("Falik"). Claims 1, 45, 59, and 80 are independent claims. Applicants respectfully traverse this rejection.

Applicants respectfully disagree with this rejection, but to expedite allowance of the claims, Applicants amend independent claim 1 herein to recite: addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile, wherein a memory read transaction or a memory write transaction is performed on at least one of the first memory location or second memory location, wherein data is transferred to the first memory location or second memory location for a memory write transaction, wherein data is transferred from the first memory location or second memory location for a memory read transaction. Support for the amendment in claim 1 is found in the filed application in, for example, Figures 1 and 2 and accompanying text, and paragraphs [0029], [0030], and [0031]. In contrast, Falik does not disclose associating any device profiles with a memory location used for a memory read or memory write transaction.

Applicants further respectfully contend that independent claim 1 recites the following limitations that are not disclosed within the four corners of Falik: addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile; said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles; and using attributes from said first and second device profiles. In contrast, Falik discloses characteristics of each logical section 57 (Falik: column 15, line 63), and these logical sections contain logical blocks (and these logical blocks are Main Block 51 and Information Block 52) (Falik: column 14, line 51-56). Therefore, Falik discloses logical sections as associated with these characteristics. However, these logical blocks in these logical sections are for storing data used by any application in a Main Device, or for storing auxiliary data (e.g., configuration data or control data) used by the Main Device or application programs (Falik: column 14, lines 21-31 and lines 51-58). Therefore, these logical blocks (and logical sections that contain these logical blocks) are not addressable sections used for a memory read or memory write transaction. Therefore, Falik does not disclose these logical sections as memory locations that are addressed. Accordingly, Falik does not disclose all the limitations of claim 1.

Falik further discloses the device and status control register (Falik: Figure 5A) which provides status and control information for an entire memory device (Falik: column 19, lines 4-8). Falik also discloses a flash device capabilities register (Falik: Figure 5B) that provides capabilities and properties information on the same entire memory device (Falik: column 19, lines 49-53). Therefore, these registers contain information directed to the same entire memory device and not directed to different memory locations. These registers do not contain a first set of attributes of a first memory location and also do not contain a second set of attributes of a second memory location.

Based on at least the above discussion, Falik does not disclose and does not teach "addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile" and "said first memory location and a second memory location respectively associated with a first device profile and a second device profile; said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles" as required in claim 1.

Since Falik does not disclose and does not teach all the limitations of claim 1, claim 1 is not anticipated by the cited reference. Claim 1 is otherwise allowable.

Claims 2-14, 20, 21, and 25 depend from allowable claim 1; as such, they are also allowable for at least the same reasons as claim 1.

The withdrawal of the rejections to claims 1-14, 20, 21, 25 and 94 is respectfully requested.

Independent claims 45, 59, and 80 recite at least some limitations similar to that as claim 1. Although claims 45, 59, and 80 are different, Applicants respectfully argue that in this case the above arguments regarding the patentability of claim 1 apply with equal force with respect to claims 45, 59, and 80. Since Falik does not disclose and does not teach all the limitations of claims 45, 59, and 80, claims 45, 59, and 80 are not anticipated by the cited reference. Claims 45, 59, and 80 are otherwise allowable.

Claims 46-58 and 95 depend from allowable claim 45; as such, they are also allowable for at least the same reasons as claim 45.

Claims 60, 69-79, and 96 depend from allowable claim 59; as such, they are also allowable for at least the same reasons as claim 59.

Claims 81-92 and 97 depend from allowable claim 80; as such, they are also allowable for at least the same reasons as claim 80.

The withdrawal of the rejection to claims 45-60, 69-92, and 95-97 is respectfully requested.

Claims 15, 18, and 19

Claims 15, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 7,330,954 to Nangle.

Claims 15, 18, and 19 depend from allowable claim 1; as such, they are also allowable for at least the same reasons a claim 1.

The withdrawal of the rejection of claims 15, 18, and 19 is respectfully requested.

Claims 16, 17, 22-24, and 93

Claims 16, 17, 22-24, and 93 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 2006/0184723 to Sinclair.

Claims 16, 17, and 22-24 depend from allowable claim 1; as such, they are also allowable for at least the same reasons a claim 1.

Claim 93 depends from allowable claim 80; as such, claim 93 is also allowable for at least the same reasons a claim 1.

The withdrawal of the rejection of claims 16, 17, 22-24, and 93 is respectfully requested.

Claims 26-28

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 6961,805 to Lakhani et al.

Claims 26-28 depend from allowable claim 1; as such, they are also allowable for at least the same reasons a claim 1.

The withdrawal of the rejection of claims 26-28 is respectfully requested.

Claims 29-44

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 5,913,215 to Rubinstein.

The Office admits that Falik does not expressly teach that the methods may be implemented using a computer readable medium comprising computer executable instructions. In order to supply the missing limitations, the Office combines Falik with Rubinstein. The Office argues it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a computer readable medium comprising computer executable instructions (Office Action: page 44). The Applicants respectfully disagree with the assertions of the Office.

Independent claim 29 recite at least some limitations similar to that as claim 1. Although claim 29 is different, Applicants respectfully argue that in this case the above arguments regarding the patentability of claim 1 apply with equal force with respect to claim 29.

Since Falik and Rubinstein, considered individually or in combination, do not disclose and does not teach all the limitations of claim 29, claim 29 is not rendered obvious in view the cited references. Claim 29 is otherwise allowable.

Since 14 October 2013 falls on a Federal Holiday, this Response is timely filed on 15 October 2013.

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, the Applicants are not conceding in this application that previously pending claims are not patentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application.

Claims 30-44 depend from allowable claim 29; as such, they are also allowable for at least the same reasons a claim 29.

The withdrawal of the rejection of claims 29-44 is respectfully requested.

Claims 61 and 64-68

Claims 61 and 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 2001/0010066 to Chin et al.

Claims 61 and 64-68 depend from allowable claim 59; as such, they are also allowable for at least the same reasons a claim 59.

The withdrawal of the rejection of claims 61 and 64-68 is respectfully requested.

Claims 62 and 63

Claims 61 and 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of Chin as applied to claim 61 above, and further in view of US 2007/0174506 to Tsuruta.

Claims 62 and 63 depend from allowable claim 59; as such, they are also allowable for at least the same reasons a claim 59.

The withdrawal of the rejection of claims 62 and 63 is respectfully requested.

Applicants respectfully request the allowance of the claims. Applicant respectfully requests and petitions for a two-months extension of time to file this response.

Conclusion

Claims 1-97 herein are allowable, and a timely Notice of Allowance is respectfully requested.

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (408) 256-0244.

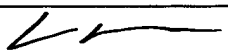
Date: October 15, 2013

Respectfully submitted,



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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/876,113	Filing Date 09/04/2010	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	10/21/2013	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 97	Minus	** 97	= 0	X $40 =	0
	Independent (37 CFR 1.16(h))	* 5	Minus	***5	= 0	X $210 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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(Use as many sheets as necessary)

Sheet 1 of 7

Complete if Known	
Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 5,822,251	10-13-1998	Bruce et al.	
		US- 4,752,871	06-21-1988	Sparks	
		US- 5,297,148	03-22-1994	Harari et al.	
		US- 5,379,401	01-03-1995	Robinson et al.	
		US- 5,388,083	02-07-1995	Assar et al.	
		US- 5,432,748	07-11-1995	Hsu et al.	
		US- 5,448,577	09-05-1995	Wells et al.	
		US- 5,479,638	12-26-1995	Assar et al.	
		US- 5,500,826	03-19-1996	Hsu et al.	
		US- 5,509,134	04-16-1996	Fandrich et al.	
		US- 5,513,138	04-30-1996	Manabe et al.	
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		US- 5,530,828	06-25-1996	Kaki et al.	
		US- 5,535,328	07-09-1996	Harari et al.	
		US- 5,559,956	09-24-1996	Sukegawa	
		US- 5,568,439	10-22-1996	Harari	
		US- 5,572,466	11-05-1996	Sukegawa	
		US- 5,594,883	01-14-1997	Pricer	
		US- 5,602,987	02-11-1997	Harari et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
		WO 94/06210	03-17-1994	Prabhakar Goel		

Examiner Signature		Date Considered	

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(Use as many sheets as necessary)

Sheet 7 of 7

Complete if Known	
Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Office Action mailed 08 October 2013 for US Application No. 13/890,229.	
		Notice of Allowability (and Examiner's Comment) mailed 30 May 2013 for US Application No. 12/882,059.	
		Notice of Allowability (and Examiner's Comment and Statement of Reasons for Allowance) mailed 14 February 2013 for US Application No. 12/882,059.	
		Office Action mailed 11 May 2012 for US Application No. 12/882,059.	
		Notice of Allowability (and Examiner's Comment and Statement of Reasons for Allowance) mailed 07 January 2013 for US Application No. 12/876,247.	
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Electronic Acknowledgement Receipt

EFS ID:	18127340
Application Number:	12876113
International Application Number:	
Confirmation Number:	1607
Title of Invention:	MULTI-PROFILE MEMORY CONTROLLER FOR COMPUTING DEVICES
First Named Inventor/Applicant Name:	Ricardo H. BRUCE
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte/Arnold deGuzman
Filer Authorized By:	Stephen Radcliff Uriarte
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Application Type:	Utility under 35 USC 111(a)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Ricardo H. Bruce, et al.	Confirmation No.: 1607
	Examiner: Jared Ian Rutz
Serial No.: 12/876,113	Ph: 571-272-5535
Filing Date: Sept. 4, 2010	Art Unit: 2187
Title: Multi-Profile Memory Controller For Computing Devices	Atty. Docket No.: 6005.042

Mail Stop Amendment
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Pursuant to the provisions of 37 CFR 1.56, 37 CFR 1.97, and 37 C.F.R. 1.98, enclosed herewith is form PTO/SB/08 listing references which may be material to the examination of this application, and with respect to which there may be a duty to disclose. The filing of this Information Disclosure Statement shall not be construed as a representation regarding the completeness of the list of references, or that

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A copy of each listed reference is enclosed herewith, unless no such copy is required pursuant to 37 CFR 1.98(d).

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Consideration of the listed references and favorable action are respectfully solicited.

Conclusion

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (408) 256-0244.

Date: 05 February 2014

Respectfully submitted,

/Arnold de Guzman/
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(22)Date of filing : **22.04.2004**

(71)Applicant : **SHARP CORP**

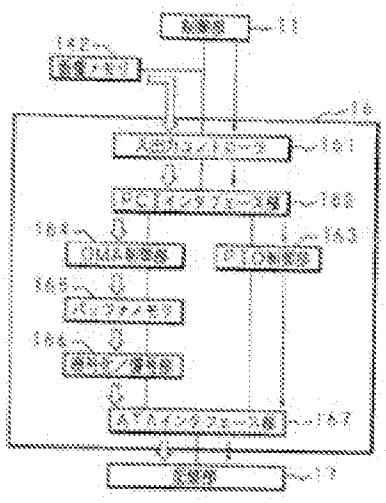
(72)Inventor : **NAKAI YOSHIYUKI**
TSUNODA KOICHI
YAMANOUCHI
TAKAO
SHIMAZAWA YOICHI

(54) DATA PROCESSOR

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a data processor capable of reducing the load of a control part for encryption and decoding of data stored by a storage means.

SOLUTION: In an image processing device (data processor), data are stored in a storage part (storage means) 17, data are output and input to the storage part 17 through a storage control part (input and output means) 16, and the data outputted from the storage part 17 are processed in a control part (processing means) 11. The storage control part 16 inputs and outputs image data by DMA system through a route via a DMA control part 164 to the





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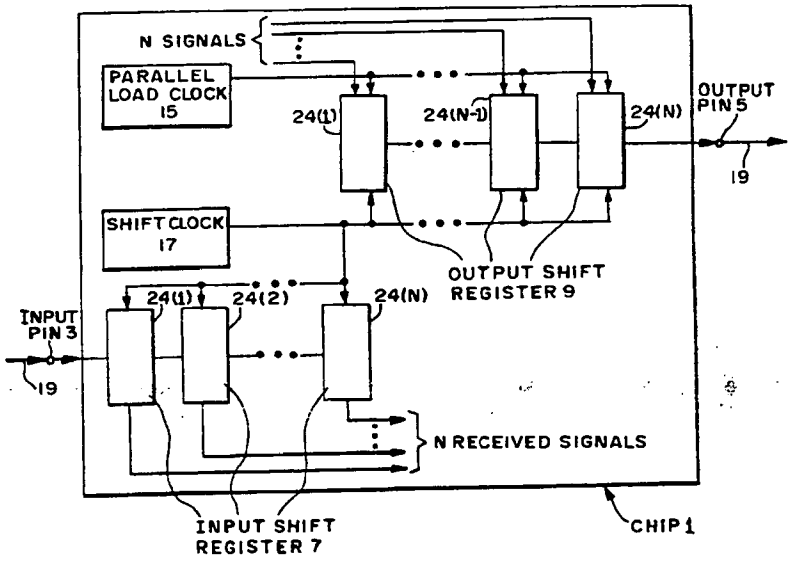
(71)(72) Applicant and Inventor: GOEL, Prabhakar [US/US]; 2050 Valparaiso Avenue, Menlo Park, CA 94025 (US).

(74) Agents: RADLO, Edward, J. et al.; Fenwick & West, 2 Palo Alto Square, Suite 500, Palo Alto, CA 94306 (US).

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Published
With international search report.

(54) Title: MULTICHIP IC DESIGN USING TDM



(57) Abstract

In a multichip integrated circuit module (4), the number of effective input/output pins (3, 5, respectively) is increased by using techniques of TDM (time division multiplexing). A first chip (1) has at least one output shift register (9). A second chip (1) has at least one input shift register (7). Interconnection wires (19) couple the output shift registers (9) and the input shift registers (7). Means (15) are provided for loading data in parallel to the output shift registers (9). Means (17) are provided for sequentially shifting data through the output shift registers (9) over the interconnections (19) and into the shift input registers (7). Embodiments of the invention are described for use in conjunction with bi-directional pins (25), tri-state output drivers (21), and asynchronous logic (18).

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Description
MULTICHIP IC DESIGN USING TDM

Field of the Invention

This invention pertains to the field of designing circuits having a plurality of integrated circuit (i.c.) chips, said design using techniques of TDM (time division multiplexing).

Description of Background Art

Dobbelaere et al., "Field Programmable MCM Systems -- Design of an Interconnection Frame", IEEE 1992 Custom Integrated Circuits Conference, pp. 4.6.1-4.6.4, addresses the same problem addressed by the present invention -- increasing the number of effective input/output pins in a multichip i.c. module -- by different techniques. The references teaches programming a matrix at the corner of each chip to determine the interconnects among the inputs and outputs. The chips are FPGA's (field programmable gate arrays). The reference does not disclose the use of shift registers or TDM.

"Programmable Interconnect Architecture", Aptix Corporation Technology Backgrounder, Nov. 1991, pp. 1-14, and an Aptix press release dated January 1, 1992, describe use of an areal grid to preserve the ability to change the interconnects among a set of integrated circuit chips in applications where a logic is being implemented onto a set of multiple i.c.'s. These references do not disclose techniques of TDM. Shift registers are used, but only to determine which i.c.'s get connected to each other. The present invention uses shift registers to convey signal information from chip to chip.

U.S. patent 5,036,473 uses dedicated FPGA's solely to determine what active FPGA's get connected to which others. The reference discloses the use of software to drive and observe signals, but does not disclose the use of shift registers or TDM.

U.S. patent 5,109,353 discloses an array of programmable gate elements for emulating electronic

circuits and systems. It does not disclose the use of shift registers or TDM.

"Handbook of Hardware Modeling", Logic Modeling Systems Incorporated, February 1992, describes the use of software to drive and observe signals in a multichip module. Techniques disclosed in this reference can be used in conjunction with the invention described herein.

"Computer-Aided Prototyping", Quickturn Systems, Inc., 1991, pp. 1-4, discloses partitioning logic for a set of interconnected FPGA's and providing software stimulus to capture and observe the response. There is no disclosure of shift registers or TDM. This technology is further described in "FastForward", LSI Logic, September 1991, and "MARS Product Overview", PiE Design Systems, Inc. Similar technology is described in three press releases by InCA Integrated Circuit Applications: "InCA 'Virtual ASIC' Emulation System supports Xilinx 4000 family FPGAS", June 8, 1992; "Virtual ASIC, Automatic ASIC Emulation from InCA", 1991; and "Concept Silicon partitions your design onto multiple FPGAs".

Disclosure of Invention

The present invention is a multichip integrated circuit module (4) comprising at least two integrated circuit chips (1). The first chip (1) has at least one output shift register (9). The second chip (1) has at least one input shift register (7). Interconnections (19) couple the output register(s) (9) and the input shift register(s) (7). Means (15) are provided for loading data in parallel to the output shift register(s) (9). Means (17) are provided for sequentially shifting data through the output shift register(s) (9) over the interconnections (19) and into the input shift register(s) (7).

Brief Description of the Drawings

These and other more detailed and specific objects and features of the present invention are more fully disclosed in the following specification, reference being had to the accompanying drawings, in which:

Figure 1 is a sketch of an embodiment of the present invention in which an integrated circuit chip 1 uses at least one input shift register 7 and one output shift register 9.

Figure 2 is a sketch showing how the techniques of the present invention reduce the number of interconnection wires 19 among chips 1.

Figure 3 is a sketch of an embodiment of the present invention in which the number of stages 24 in an input shift register 7 and output shift register 9 can be reduced by one.

Figure 4 is a sketch of a chip 1 using tri-state output drivers 21.

Figure 5 is a sketch of an embodiment of the present invention in which two output shift registers 9 are used in conjunction with a single output driver 21.

Figure 6 is a sketch showing a plurality of tri-state output drivers 21, each having a common gating signal 23.

Figure 7 is a sketch showing how a single output shift register 9 can be used when the output drivers 21 have a common gating signal 23.

Figure 8 is a sketch showing the use of bi-directional pins and a plurality of tri-state output drivers 21 having a common gating signal 23.

Figure 9 is a sketch showing how a single bi-directional pin 25 can be used when a plurality of tri-state output drivers 21 have a common gating signal 23.

Figure 10 shows a chip 1 having a plurality of bi-directional pins 25, each coupled to an output driver 21 that has a different gating signal.

Figure 11 shows a single pin 25 equivalent to the embodiment depicted in Figure 10.

Figure 12 shows an embodiment of the present invention in which asynchronous logic 18 is employed.

Figure 13 shows an embodiment of the present invention in which a plurality of output shift registers 9 are daisy chained together.

Figure 14 shows an embodiment of the present invention in which a plurality of test shift registers 12 are multiplexed together.

Figure 15 shows an embodiment of the present invention in which the TDM sequence must be applied twice.

Figure 16 shows an embodiment of the present invention in which an interconnect 19 couples two chips 1.

Figure 17 shows how the interconnect 19 of Figure 16 can be reconfigured by reprogramming the first chip 1(1).

Figure 18 shows a single interconnect 19 coupling four chips 1.

Figure 19 shows how the interconnect 19 of Figure 18 can be reprogrammed by reprogramming the source chip 1(1).

Figure 20 shows an embodiment of the present invention in which an interconnect wire 19 couples two chips 1.

Figure 21 shows how the interconnect 19 of Figure 20 can be reprogrammed by adding a new signal S3 to the source chip 1(1).

Figure 22 shows an embodiment of the present invention in which the number of stages 24 in an input shift register 7 can be reduced by one.

Detailed Description of the Preferred Embodiments

A major purpose of this invention is to increase the effective number of input/output (I/O) pins 3,5 on integrated circuit chips 1 within a module 4 that comprises a plurality of said chips 1. The invention can be thought of as creating a number of virtual I/O pins 3,5 that is greater than the number of actual pins 3,5. The invention also eases pressures on the system designer when the number of interconnect wires 19 on the module 4 is limited. Further, the invention enhances the reconfigurability of signal flow across chips 1.

An example where the invention is useful is in the design of a system 4 in which there is a need to fit a given amount of logic, which may be provided in the form of a netlist, into one or more of the chips 1. Normally, said chips 1 come with a fixed number of I/O pins 3,5 that are used for interconnections 19 among the chips 1.

The limited number of I/O pins 3,5 can greatly reduce the efficiency of utilizing the chips 1, and in some cases make the task of fitting the logic into the chips 1 extremely difficult.

The module 4 can be a production module, in which the chips 1 are executable and application-ready. Alternatively, module 4 can be a prototype module, in which the chips 1 are experimented with by the designer to create a system design. Changes in such a prototyping environment are typically done by a combination of hardware and software changes. Alternatively, module 4 can contain some production chips 1 and some programmable chips 1.

Chips 1 are any chips for which the user has control over the contents, such as FPGA's (field programmable gate arrays), non-field-programmable gate arrays, custom i.c.'s, semi-custom i.c.'s (application specific integrated circuits), and standard cell i.c.'s. FPGA's are normally preferable, because of their flexibility.

The present invention makes use of techniques of TDM (time division multiplexing or time domain multiplexing). The execution of the system embodied in module 4 takes longer because of this, but in many applications this is of no concern. The TDM process is transparent to the operation of the logic embodied in module 4.

Typically the TDM is implemented by shift registers 7,9, as illustrated in Figure 1. Each input pin 3 and each output pin 5 on a chip 1 is assigned a dedicated shift register, 7,9, respectively. The number of stages 24 in a shift register 7,9 is referred to as N. N is any positive integer greater than or equal to 2, and could be typically between 2 and 5. Preferably, N is the same for all shift registers 7,9 on a chip 1. If N were not the same, a separate shift clock 17 would be needed for each different value of N. In the chip 1 illustrated in Figure 1, the value of N is the same, and therefore there is but one shift clock 17.

Each chip 1 can have a plurality of input pins 3 and a different number of output pins 5. The different chips 1 on a module 4 can have different numbers of input pins 3 and output pins 5.

The individual stages 24 of the shift registers 7,9 can be, for example, flip-flops, edge triggered latches, and pairs of polarity hold latches. When polarity hold latches are used, a pair of shift clocks 17 is required for use with the corresponding shift register 7,9.

The shift register 9 attached to an output pin 5 is referred to as an output shift register (OSR) 9, and functions as N virtual output pins 5. N internal signals from within the chip 1 can be loaded into the OSR 9 in parallel by means of activating a parallel load clock 15 associated with the OSR 9. These signals are then serially shifted out of the OSR 9 over the corresponding output pin 5 using the shift clock 17 associated with said OSR 9. The signals travel over interconnection wires 19 to other chips 1 that need to receive the signals.

Similarly, the shift register 7 attached to an input pin 3 is referred to as an input shift register (ISR) 7, and functions as N virtual input pins 3. It can receive serially N signals from a board interconnect 19 through the associated input pin 3 by means of the shift clock 17 that is connected to said ISR 7. The received signals can then simultaneously be applied inside the chip 1 using their stored states within the stages of the ISR 7. No special clock is needed to unload the signals from the ISR 7, because once these signals are in the ISR 7, they are visible to the logic within the chip 1.

Preferably, a single parallel load clock 15 and a single shift clock 17 are used for all the ISR's 7 and OSR's 9 on the board 4.

Preferably, the OSR's 9, ISR's 7, and attendant parallel load and shift clocks 15, 17 are customized within peripheral regions of the gate arrays 1. Alternatively, the OSR's 9 and ISR's 7 are fabricated from logic normally present on the gate arrays 1.

Figure 2 illustrates how the invention minimizes the number of interconnect wires 19 among chips 1,2 and minimizes the number of I/O pins 3,5 within a chip 1. Figure 2 illustrates the interconnections of OSR 9 within a source chip 1 and three ISR's 7 residing within three target (sink) chips 1. The target chips 1 could be identical or different in a hardware sense. A single interconnect wire 19 couples the chips 1. Three signals S1, S2, and S3 from the source chip 1 are conveyed to the three sink chips 1. If the TDM and shift register technique were not used, three interconnects 19 would be required. The interconnect wire 19 can be thought of as a TDM bus which bundles in the time domain the three signals S1, S2 and S3. Said TDM bus 19 is visible to all three sink chips 1.

As illustrated in Figure 2, not all of the three signals need to be used in each sink chip 1. (The signals within the sink chips 1 are primed for notational purposes.)

The TDM process described herein is transparent to the intended logic design. This transparency can be achieved in different ways, depending upon the degree of transparency needed. For example, if all chips 1 on the module 4 are synchronously clocked (which is preferable), the following two-step TDM process can be used, at a safe time after the application of each pulse from the system clock (not illustrated). The safe time is that amount of time needed for all of the signals in the logic to achieve a steady state, i.e., when the intended design has been programmed into the chips 1.

Step 1. The parallel load clock 15 (which is preferably a single clock applied to all output shift registers 9 on the board 4) is applied to effect a parallel capture of signals into all of the OSR's 9 on all the chips 1.

Step 2. Using the shift clock 17 (preferably a single clock used by all the ISR's 7 and OSR's 9 on all the chips 1), the contents of all of the OSR's 9 are shifted into the target ISR's 7 via the interconnects

19. This shifting process involves N applications of shift clock 17 to all of the chips 1.

Exceptions to the above scheme exist for various reasons, such as: (1) Certain I/O pins are bi-directional pins 25 (see Figure 8). Such bi-directional pins 25 could be left unmodified. Signals involving such pins 25 are not affected by the above two steps. (2) Inputs 3 that receive direct clock signals (as opposed to data signals) do not require the use of an ISR 7. Such would be undesirable, because it would cause the clock to jiggle. Similarly, output pins 5 that carry clock signals going to other chips 1 do not require the use of OSR's 9. Clock signals cannot be transferred across chips 1 using TDM without significant impact to the intended logic. As such, it is not desirable to use such techniques for I/O pins 3,5 that carry clock signals.

Figure 12 shows that if the logic being prototyped is asynchronous, an additional latch 29 is needed for each ISR 7 stage 24 that drives a piece of asynchronous logic 18. Such a latch 29 is a voltage level or logic level sensitive latch that receives its data from an ISR 7 stage output and is clocked by yet another clock called the P clock 27. P clock 27 is shared among all chips 1 that have asynchronous logic. The function of this added latch 29 is to screen the shifting of the ISR 7 from the asynchronous logic 18. P clock 27 is pulsed once after the completion of the two usual TDM steps, described earlier, that are used to effectuate the transfer of signals across chip 1 boundaries using TDM. As shown in Figure 12, some of the stages 24 of the ISR 7 can drive synchronous logic 16, and others of the stages 24 can drive asynchronous logic 18.

As illustrated in Figures 13 and 14, multiple OSR's 9 can be connected into one daisy-chained composite "test shift register" (TSR) 12 on each chip 1 to facilitate the observation of the captured signals externally by shifting out the TSR 12. All of the observation can be performed at the output of pin 5(M). These observed signals can be used for debugging the prototype hardware,

depending upon the availability of extra board 4 logic and pins 3,5. The contents of the TSR 12 can then be reloaded from the output 5(M) of the TSR 12 to the shift register data input 3 on the same chip 1 if it is desired to continue with the operation of the hardware. A preferred way of accomplishing this reloading is to make a connection on the chip 1 itself from output 5(M) to input 3, thereby creating a circular shift register.

The set of TSR's 12 can be multiplexed to be observable at the output 10 of the board 4 as illustrated in Figure 14. Multiplexer select signals 14 control the selection of the individual TSR 12 outputs by multiplexer 8. The input to all the TSR's 12 is injected via board input 6. The scheme depicted in Figure 14 is useful when there are more chip output pins 5 that the designer wants to observe than there are available board output pins 10.

Since the OSR's 9 are usable for debugging purposes, the designer can choose to provide extra, initially unused, stages 24 within some OSR's 9. These stages 24 are then available to be used for observing internal signals that the hardware designer may not have thought about earlier, for example, by changing the programming on the chip 1 to look at these stages 24.

It is possible to reconfigure the interconnects 19 among the chips 1 by sending a different set of signals on each interconnect 19 than was previously intended. When combined with the internal reconfigurability of the FPGA 1 itself, a powerful new type of reconfigurability is thereby created. Figure 14 shows a module 4 with a number of FPGA's 1 and set up for using TDM. To achieve a reprogrammable board 4, it is required that one must able to reprogram both the logic on the chips 1 as well as the interconnects 19. The on-chip logic is already rather reprogrammable through the use of the FPGA's 1. To reprogram the interconnects 19, an FPGA 1 can be used as a programmable interconnect chip as in U.S. patent 5,036,473, cited above; or a programmable interconnect chip as described in the Aptix references cited above can be used. Alternatively, several programmable

interconnect chips 1 may be used. A limited reprogrammability of interconnects is described in Figures 16-21.

Figure 16 shows three signals, S1, S2, S3, TDM'ed between chips 1(1) and 1(2). By reprogramming the first FPGA 1(1), the manner in which the three signals S1, S2, S3 connect can be changed, as shown in Figure 17. In effect, the connections 19 between the two chips 1 have been rewired.

Figure 18 shows four chips 1 with signals S1, S2, S3 connected as shown. By reprogramming the first chip 1(1), as shown in Figure 19, signal S3 crossing between chips 1(1) and chips 1(4) is changed to S4.

In Figure 20, two interconnected chips 1 are shown. Figure 21 shows how a signal can be added to the interconnect 19 just by reprogramming the individual chip 1(1) and not touching the interconnect 19.

The flexibility described herein results from chip 1 being able to reprogram a number of signals that are TDM'ed across to other chips 1. Traditional techniques limit the reprogramability to a single signal.

Once the value N is fixed for a given system 4, the total number of signals that can be moved across the chip 1 boundaries is predetermined. The total number of signals movable is N multiplied by the number of unique interconnect wires 19 on the board 4. It is apparent that by increasing N, a capacity greater than what is initially needed for the total number of signals can be achieved. The additional capability is usable for greater flexibility in reconfiguring the interconnects 19.

Theoretically, it is possible to accomplish all interconnections between any two chips 1 by using two interconnect wires 19 between them: one to carry signals flowing in one direction, and the second to carry signals flowing in the opposition direction. In this extreme situation of maximum multiplexing, the shift registers 7,9 must have an N greater than or equal to the larger of the number of the input signals and the number of the

output signals on any single chip 1. (One signal is associated with each stage 24 of a shift register 7,9.)

The techniques of the present invention can be selectively applied to areas of logic that are considered susceptible to change or require use of TDM to accommodate the number of signals that need to traverse across chip 1 boundaries. As such, ISR's 7 and OSR's 9 need not be placed on all qualifying I/O pins 3,5. Instead, if there are insufficient resources on the chip 1, the ISR's and OSR's 7,9 may be deployed only on enough I/O pins 3,5 to allow adequate signal flow through the chips 1. It should be noted that an interconnect 19 must have either ISR's 7 and OSR's 9 on all terminals of that interconnect 19, or else must have no ISR's 7 or OSR's 9 at all.

When the chips 1 are FPGA's, it is possible to make engineering changes to prototype hardware 4 by reprogramming the affected FPGA's 1 to (1) change the logic realized by certain FPGA's 1 and/or (2) modify the effective interconnects 19 by capturing different signals into one or more of the OSR's 9 and/or (3) change the signals that are made observable by capturing them into unused stages 24 of OSR's 9.

Figure 22 shows an optimized version of the scheme in Figure 2. Here, the contents of the OSR 9 can be made observable, while reducing the number of stages 24 in an ISR 7 by one. In this embodiment, the state of the last stage 24 of an OSR 9 is used as a substitute for the eliminated stage 24 of an ISR 7.

In certain prototyping situations, it may not be necessary to observe the contents of the OSR's 9. In these cases, the number of stages 24 needed in an ISR 7 and OSR 9 can be reduced by one, corresponding to the stage 24 the system designer does not need to observe. This reduction is achieved by using the scheme depicted in Figure 3. Figure 3 shows how N equals 2 can provide the capability to multiplex three signals across a single interconnect 19. In this embodiment, the final state of the interconnect 19 after application of the TDM sequence

is used as one of the multiplexed signals for the sink chip 1(2). In contrast, the scheme depicted in Figure 2 does not have the sink chips 1 dependent upon the final state of the interconnect 19, but only on the states of the ISR's 7.

The scheme depicted in Figure 1 uses ISR's 7 and OSR's 9 to multiplex signals across chip 1 boundaries. Such a TDM sequence serves to transfer signals once across an interconnect 19. However, if there is a logic path that is not interrupted by a latch or other sequential logic (other than ISR's 7 and OSR's 9) and spans more than two FPGA chips 1, then the TDM sequence needs to be repeated. The total number of TDM sequence applications required is equal to the number of distinct board level interconnect wires 19 that are included in the logic path. Figure 15 shows a logic path of combinational logic 22 that spans two board level interconnect wires 19(1) and 19(2). There are no latches other than ISR's 7 and OSR's 9 in the path. As such, the TDM sequence needs to be applied twice to move the signal through the three chips 1. Notice that ISR's 7 and OSR's 9 force the use of TDM. Without ISR's 7 and OSR's 9, the signal from chip 1(1) to chip 1(2) to chip 1(3) would flow without any clocking.

The techniques of the present invention can be extended to bi-directional pins 25 and/or three state output drivers 21. (See Figure 4). Such a driver 21 typically has outputs of logical zero, logical one, and high impedance.

Buses 19 generally employ tri-state drivers 21 to allow multiple source chips 1 onto a single wire. Such buses 19 are intended by the designer to achieve efficient interconnects between a multitude of source chips 1 and some number of sink chips 1. Generally, one source chip output driver 21 is active while others are in a high impedance state, so that one source chip output driver 21 is driving all receivers in the bus 19. The architecture shown in Figure 1 cannot be employed directly in such a case. Figure 4 shows N output pins 5,

with a tri-state driver 21 on each pin 5. The OSR 9 scheme of Figure 1 will not work here, because the high impedance state cannot be transmitted via an OSR 9 and an ISR 7. Instead, the scheme shown in Figure 5 needs to be employed. It should be noted that this scheme uses two OSR's 9 instead of one: the first OSR 9(1) to capture the N gating signals and the second OSR 9(2) to capture the N data signals. Output driver 21 sees the corresponding gate-data combination as the OSR's 9 are shifted out. Thus, output pin 5 sees the gated output from output driver 21. The generated TDM sequence of signals on output pin 5 combines with similarly generated TDM sequences from other output pins 5 that are connected with this first output pin 5.

Figure 6 shows N output pins 5 with high impedance drivers 21 that share a common output gating signal 23. Signal 23 either produces a high impedance on the outputs of drivers 21 or else transmits the input signals to the outputs. Figure 7 shows a corresponding single pin architecture that avoids the use of two OSR's 9 but still places output driver 21 between the single OSR 9 and the output pin 5. The use of two OSR's 9 is avoided because of the presence of the common gating signal 23.

Figure 8 shows a typical N bi-directional pin 25 configuration with a common output gating signal 23. In Figure 8, the same pin 25 is used to both output a signal from the chip 1 as well as to receive signals from the outside. To achieve a single pin 25 architecture for TDM of the N signals, the scheme of Figure 9 is employed. In Figure 9, the architecture of Figure 7 is used to feed the outputs of the N drivers 21, and a single ISR 7 is used for the N input signals as in the Figure 1 embodiment.

Figure 10 shows N bi-directional pins 25, each with a different gating output signal. The single-pin 25 architecture equivalent for TDM of the N signals uses the scheme shown in Figure 11. In Figure 11, the architecture of Figure 5 is employed for the N output

drivers 21, and a single ISR 7 is applied to the N input signals as in the Figure 1 embodiment.

Personalization instructions are injected into module 4, e.g., by techniques described in U.S. patent 5,109,353 cited above. More than one logic design can be introduced into the module 4 by different personalization instructions. Software that is intended to provide automatic or interactive partitioning of the intended system design, such as Concept Silicon from InCA cited above, can exploit the knowledge of the existence of ISR's 7 and OSR's 9 to help pack more logic into each of the programmable chips 1 and/or to minimize the number of interconnection wires 19.

The software is executed on a computer external to module 4, e.g., a workstation. The software can be standalone (not physically coupled to module 4) software that exploits the hardware architecture of the module 4 as introduced by the invention. Alternatively, there can be physical coupling between the software and the module 4, e.g., the computer on which the software is executed can have an electrical connection to the module 4, over which the personalization created by the software is downloaded into the module 4.

The benefit of minimizing the number of chips 1 is obvious. The benefit of minimizing the number of interconnects 19 is significant. If the prototype board 4 is intended to utilize Aptix-type programmable interconnect chips, minimizing the number of interconnects 19 will reduce the number of Aptix components needed to achieve programmable interconnects. Either the software is told the number of virtual I/O's 3,5 rather than the actual number; or else the software is told all about the ISR's 7 and OSR's 9 so that it will take this information into account when it does the partitioning. The programmable interconnect chip does not always need to be changed. Rather, ISR's 7 and/or OSR's 9 are placed on the chips 1 to which the programmable interconnect chip is connected, thereby enhancing the programmable interconnect chip.

Combining the use of the present invention with the use of one or more programmable interconnect chips can allow the board 4 designer the flexibility of creating additional interconnects 19 among chips 1. Programmable interconnect chips are used to interconnect among two or more I/O pins 3,5. These I/O pins 3,5 could also have ISR's 7 and OSR's 9 on board the chip 1, thus providing a greatly increased number of programmable interconnects.

The configuration of the prototype board 4 is changed by a combination of hardware and software. For hardware changes, interconnects 19 are reprogrammed, FPGA's and/or programmable interconnect chips 1 are reprogrammed, FPGA's 1 are added or subtracted, and connections are obliterated using lasers. For software changes, software other than the partitioning software is used to, e.g., reprogram the Aptix chip(s) 1.

The above description is included to illustrate the operation of the preferred embodiments and is not meant to limit the scope of the invention. The scope of the invention is to limited only by the following claims. From the above discussion, many variations will be apparent to one skilled in the art that would yet be encompassed by the spirit and scope of the invention.

What is claimed is:

Claims

1. A multichip i.c. module comprising:

at least two integrated circuit chips, a first chip having at least one output shift register and a second chip having at least one input shift register;

interconnections coupling the output shift register(s) and the input shift register(s);

means for loading signals in parallel to the output shift register(s); and

means for sequentially shifting signals through the output shift register(s) over the interconnections and into the input shift register(s).

2. The multichip i.c. module of claim 1 wherein all chips are clocked synchronously.

3. The multichip i.c. module of claim 1 wherein at least one chip contains asynchronous logic, said chip comprising an input shift register that is coupled to said asynchronous logic via a polarity hold latch; wherein:

said polarity hold latch is clocked by a P clock.

4. The multichip i.c. module of claim 1 wherein at least some of the chips are gate arrays from the set comprising FPGA's and non-field-programmable gate arrays.

5. The multichip i.c. module of claim 4 wherein the output shift register(s), the input shift register(s), and associated clocking are customized within peripheral regions of the gate arrays.

6. The multichip i.c. module of claim 4 wherein the output shift register(s) and input shift register(s) are fabricated from logic normally present on the gate arrays.

7. The multichip i.c. module of claim 1 wherein the means for loading signals is a parallel load clock.

8. The multichip i.c. module of claim 1 wherein the module is a production module containing executable chips.

9. The multichip i.c. module of claim 1 wherein the multichip module is a prototype module containing at least some experimental chips.

10. The multichip i.c. module of claim 1 further comprising software means to partition logic among the chips, said software means exploiting information concerning the particular architecture of the module.

11. The multichip i.c. module of claim 1 wherein said module contains a programmable interconnect chip.

12. In a multichip i.c. module comprising at least two integrated circuit chips, each chip having a plurality of I/O pins, said module having inter-i.c. connection wires interconnecting said pins, a method for increasing the effective number of I/O pins, said method comprising the steps of:

time division multiplexing signals at an output pin of a first chip; and

sending said signals over a connection wire to an input pin of a second chip.

13. The method of claim 12 wherein all chips are clocked synchronously.

14. The method of claim 12 wherein said step of time division multiplexing comprises the substeps of:

parallel loading signals into an output shift register within a first chip; and

accessing signals in parallel from an input shift register within a second chip.

15. The method of claim 14 wherein at least some of the chips are gate arrays from the set comprising FPGA's and non-field-programmable gate arrays.

16. The method of claim 15 wherein the output shift register(s) and input shift register(s) are customized within peripheral regions of said gate arrays.

17. The method of claim 15 wherein the output shift register(s) and input shift register(s) are fabricated from logic normally present on said gate arrays.

18. The method of claim 14 wherein the input and output shift registers comprise stages fabricated from

items from the group of items comprising flip-flops, edge triggered latches, and pairs of polarity hold latches.

19. The method of claim 18 wherein one of said stages in reserved for debugging purposes.

20. The method of claim 12 further comprising the additional step of determining a logic design for the module by use of partitioning software that exploits information concerning the particular architecture of the module.

21. The method of claim 12 further comprising the step of observing said signals at said output pin for test purposes.

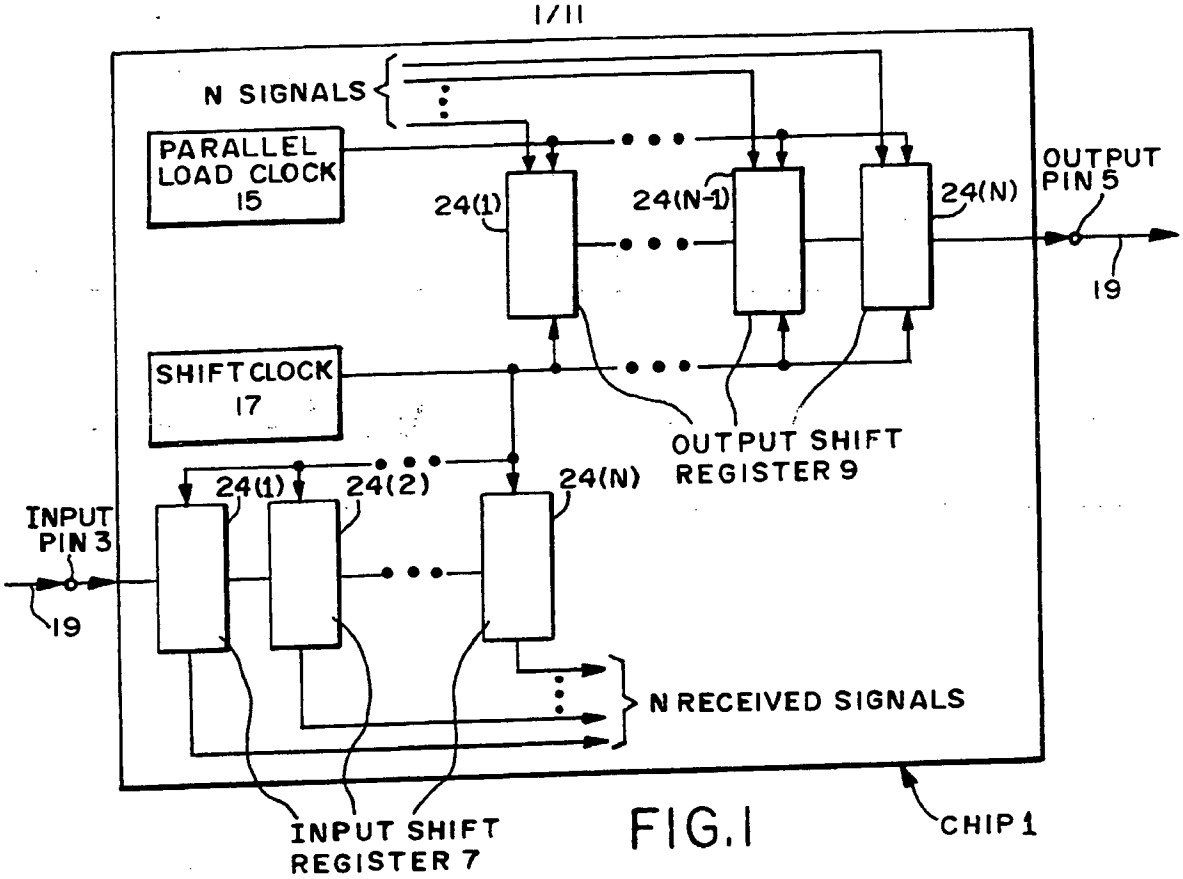

N SIGNALS
PARALLEL LOAD CLOCK 15
24(1)
24(N-1)
24(N)
OUTPUT PIN 5
19
SHIFT CLOCK 17
OUTPUT SHIFT REGISTER 9
24(1)
24(2)
24(N)
INPUT PIN 3
19
N RECEIVED SIGNALS
INPUT SHIFT REGISTER 7
CHIP 1

FIG.1

FIG.2

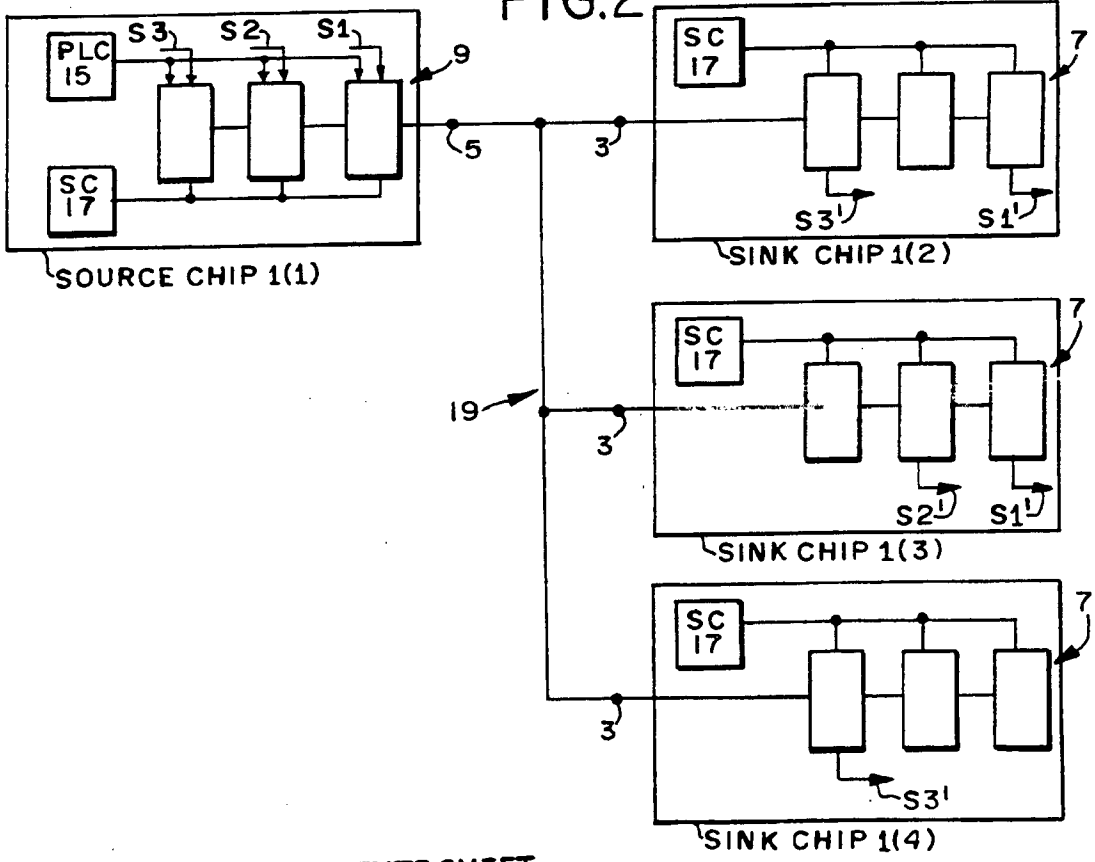

PLC 15
S3
S2
S1
9
SC 17
5
SOURCE CHIP 1(1)
3
SC 17
7
S3'
S1'
SINK CHIP 1(2)
19
3
SC 17
7
S2'
S1'
SINK CHIP 1(3)
3
SC 17
7
S3'
SINK CHIP 1(4)

FIG.3

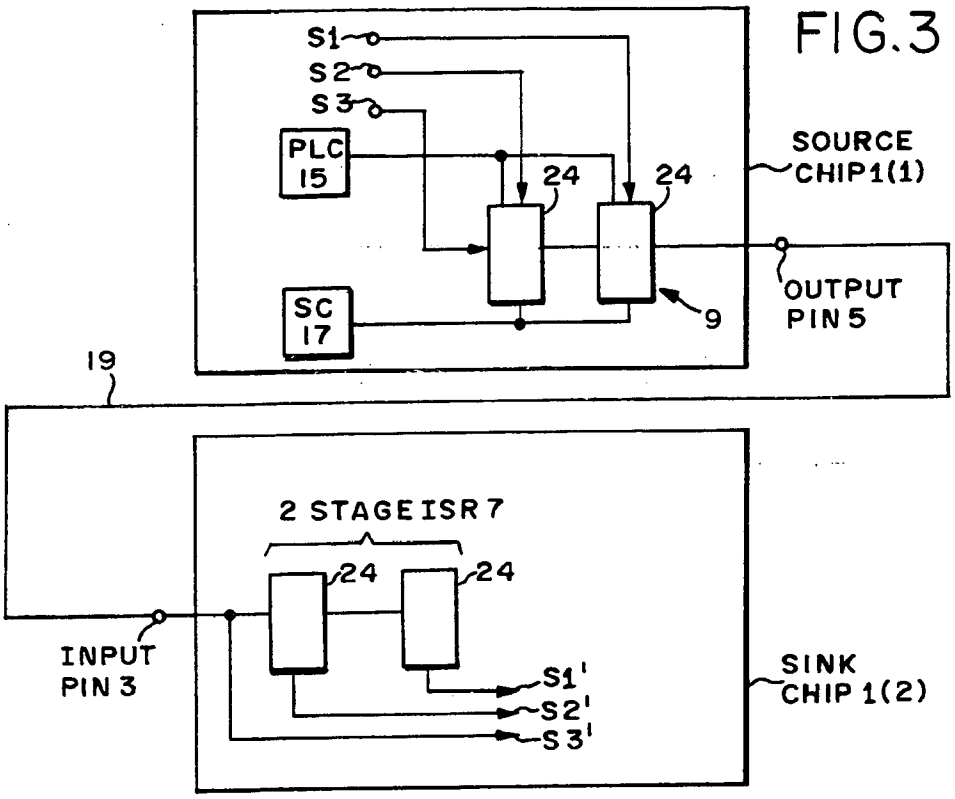

S1
S2
S3
PLC 15
24
24
SOURCE CHIP1(1)
SC 17
9
OUTPUT PIN 5
19
2 STAGE ISR 7
24
24
INPUT PIN 3
S1'
S2'
S3'
SINK CHIP 1(2)

FIG.4

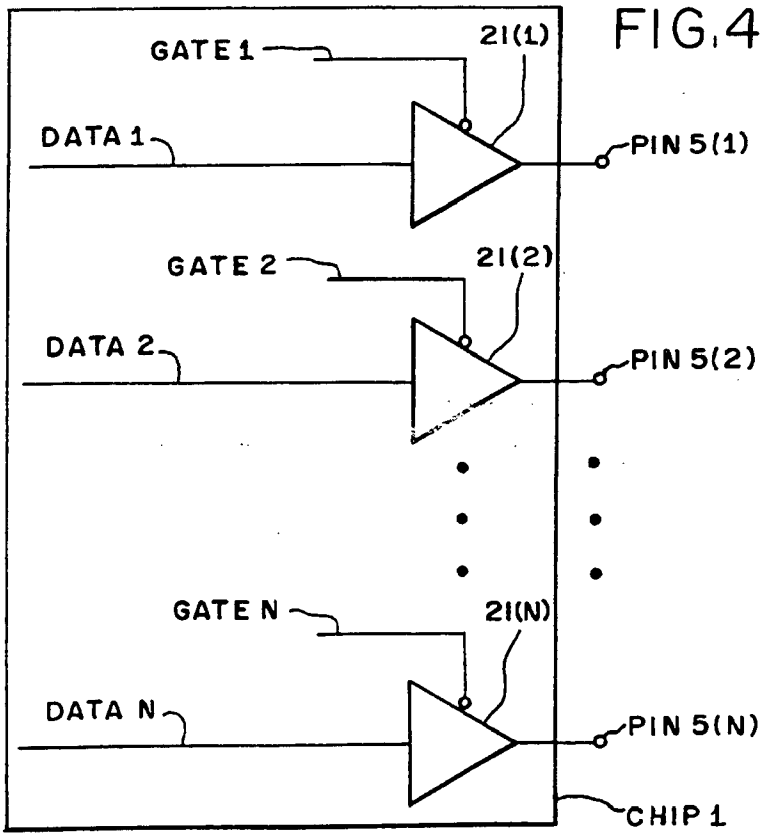

GATE 1
21(1)
DATA 1
PIN 5(1)
GATE 2
21(2)
DATA 2
PIN 5(2)
GATE N
21(N)
DATA N
PIN 5(N)
CHIP 1

FIG.5

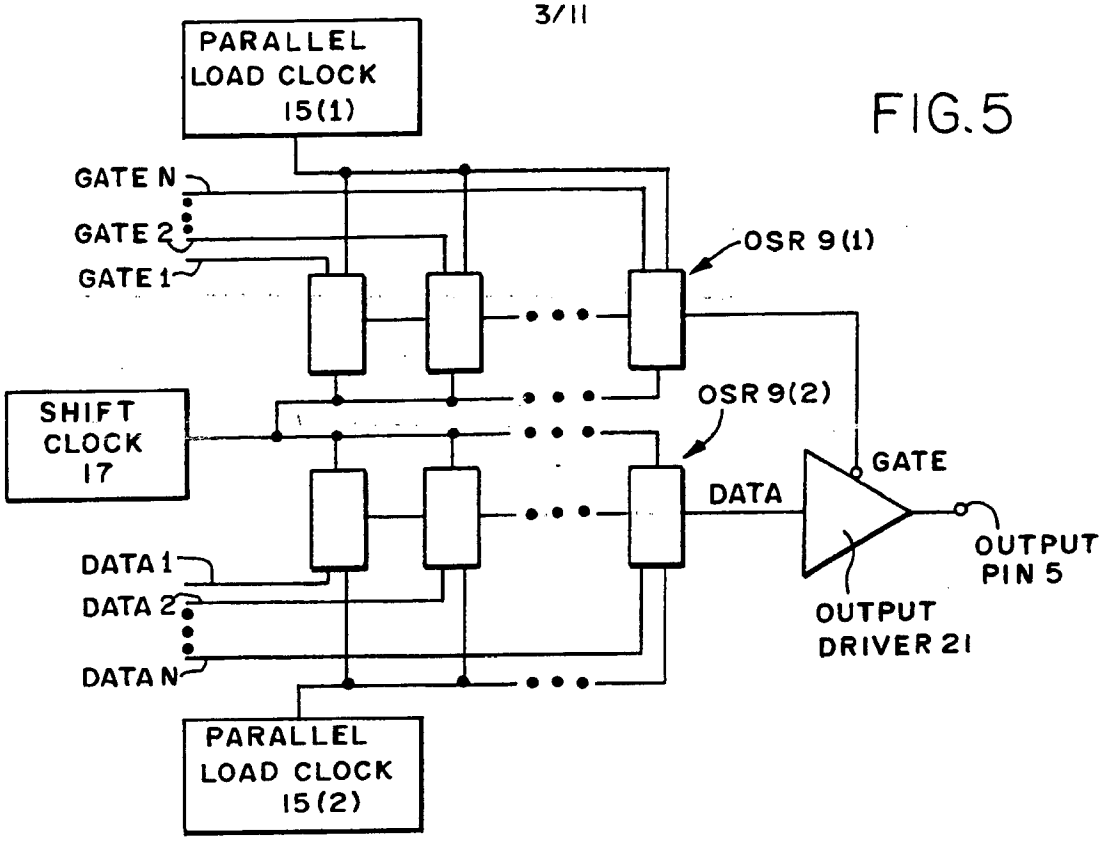

PARALLEL LOAD CLOCK 15(1)
GATE N
GATE 2
GATE 1
OSR 9(1)
OSR 9(2)
SHIFT CLOCK 17
GATE
DATA
OUTPUT PIN 5
DATA 1
DATA 2
DATA N
OUTPUT DRIVER 21
PARALLEL LOAD CLOCK 15(2)

FIG.6

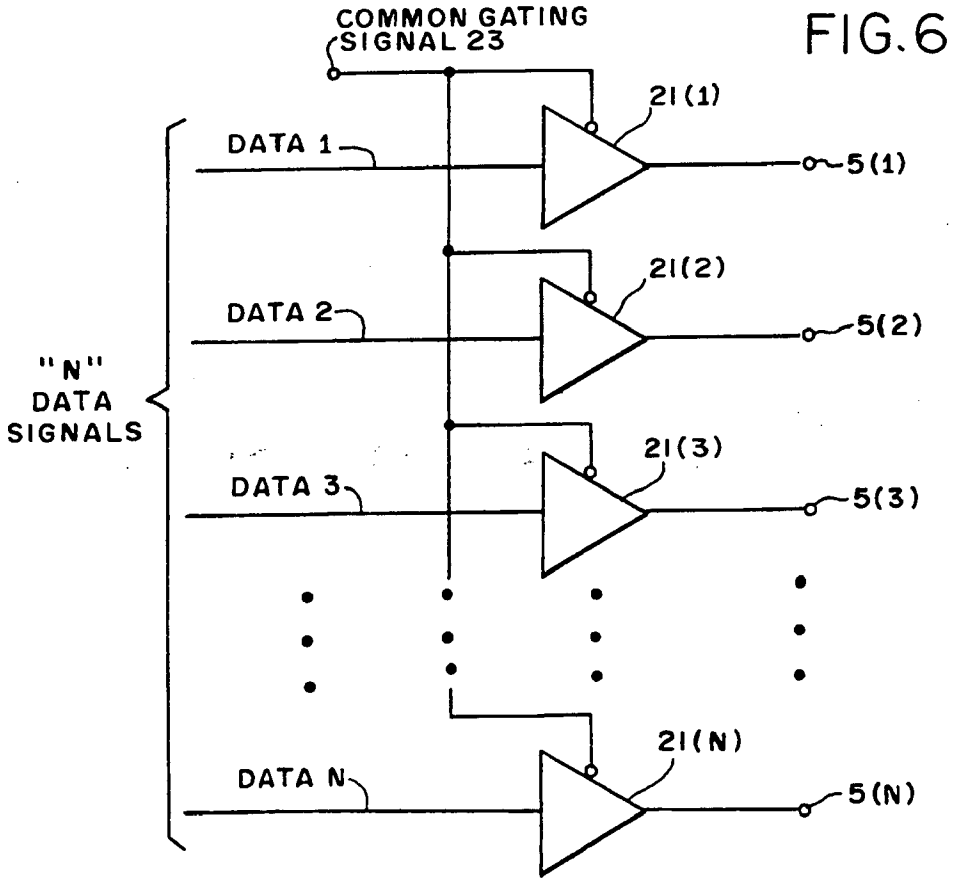

COMMON GATING SIGNAL 23
21(1)
DATA 1
5(1)
21(2)
DATA 2
5(2)
"N" DATA SIGNALS
21(3)
DATA 3
5(3)
21(N)
DATA N
5(N)

FIG.7

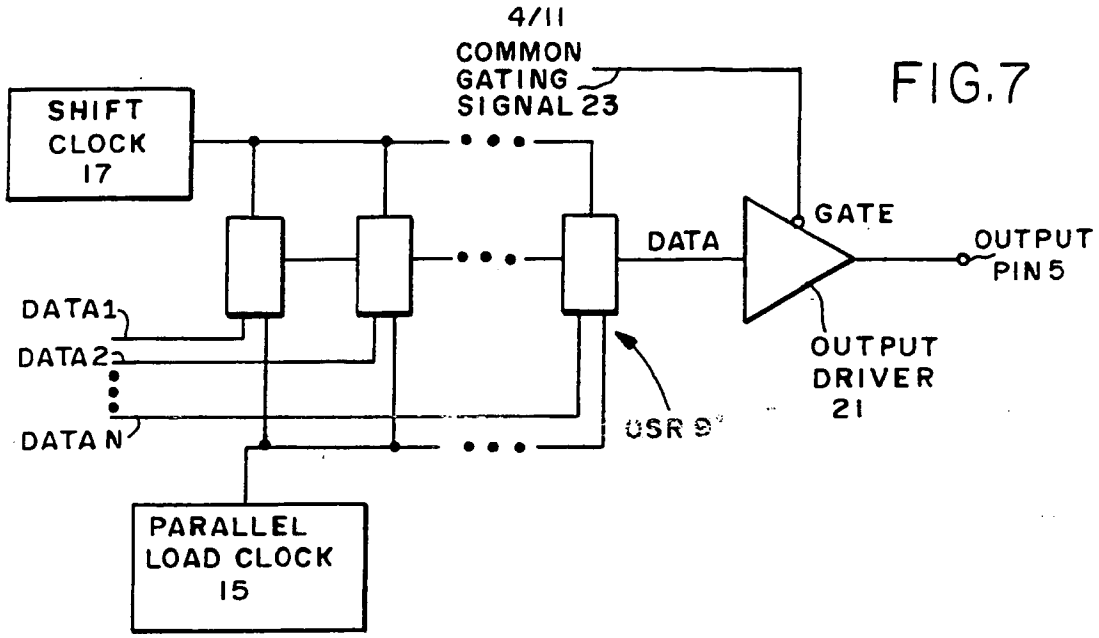
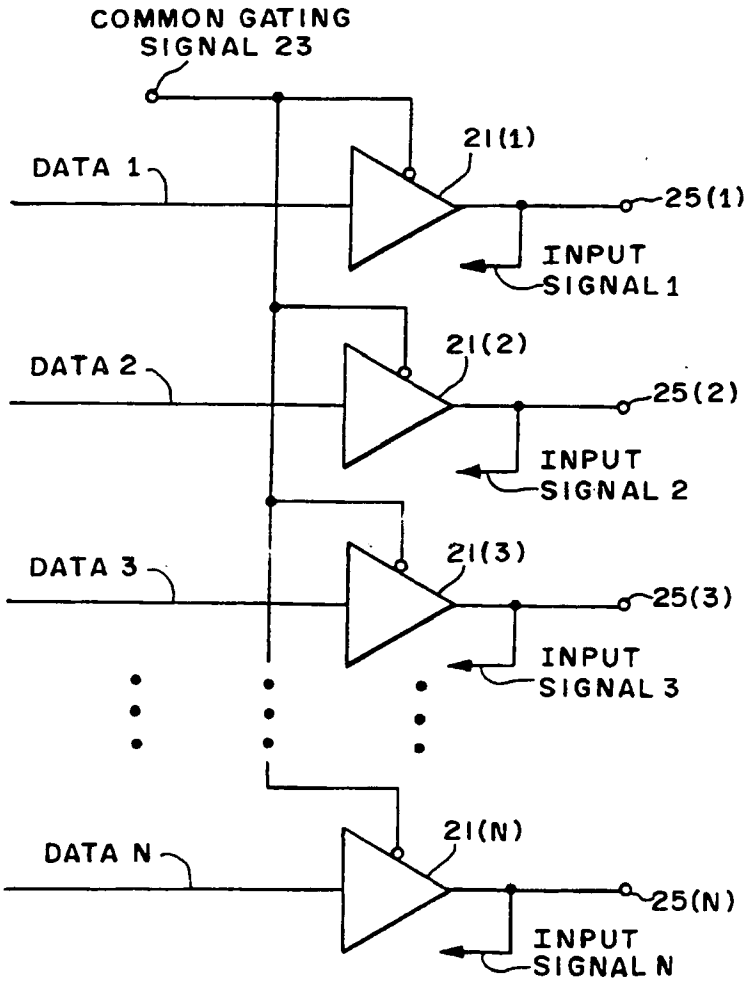

COMMON GATING SIGNAL 23
SHIFT CLOCK 17
DATA1
DATA2
DATA N
DATA
GATE
OUTPUT PIN 5
OUTPUT DRIVER 21
USR 9
PARALLEL LOAD CLOCK 15

FIG.8


COMMON GATING SIGNAL 23
DATA 1
21(1)
25(1)
INPUT SIGNAL 1
DATA 2
21(2)
25(2)
INPUT SIGNAL 2
DATA 3
21(3)
25(3)
INPUT SIGNAL 3
DATA N
21(N)
25(N)
INPUT SIGNAL N

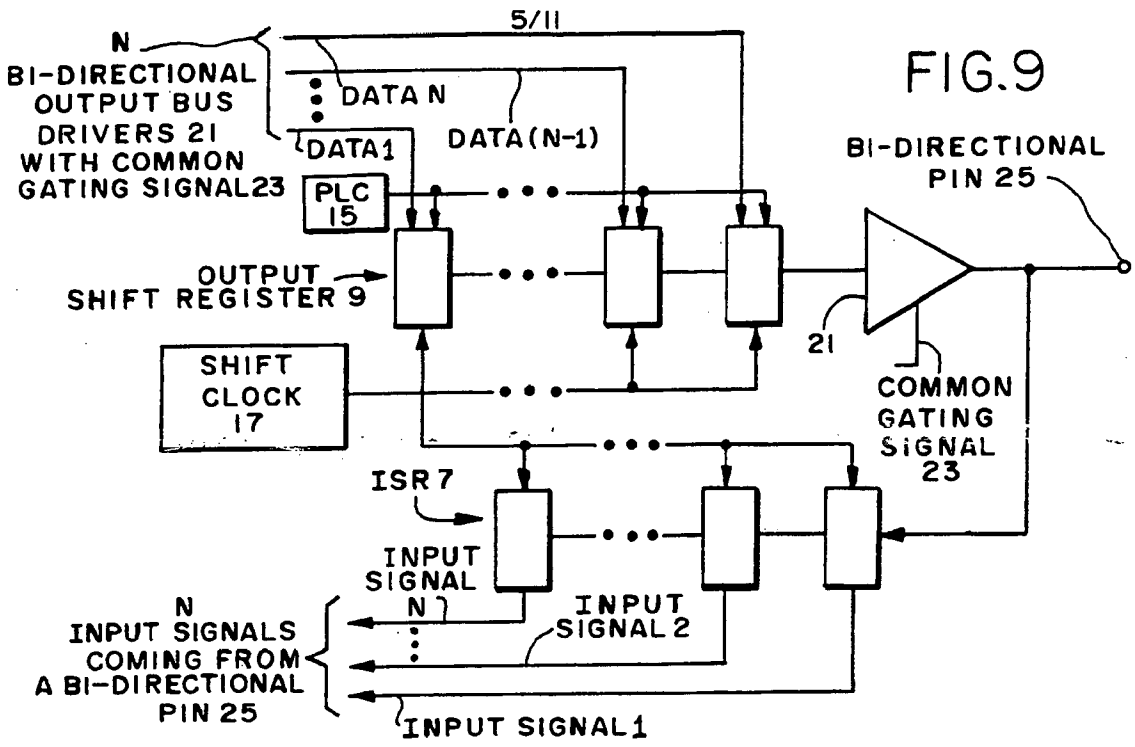

5/11
N
BI-DIRECTIONAL
OUTPUT BUS
DRIVERS 21
WITH COMMON
GATING SIGNAL23
DATA N
DATA1
DATA(N-1)
PLC
15
OUTPUT
SHIFT REGISTER 9
SHIFT
CLOCK
17
ISR 7
INPUT
SIGNAL
N
N
INPUT SIGNALS
COMING FROM
A BI-DIRECTIONAL
PIN 25
INPUT
SIGNAL 2
INPUT SIGNAL1
BI-DIRECTIONAL
PIN 25
21
COMMON
GATING
SIGNAL
23

FIG.9

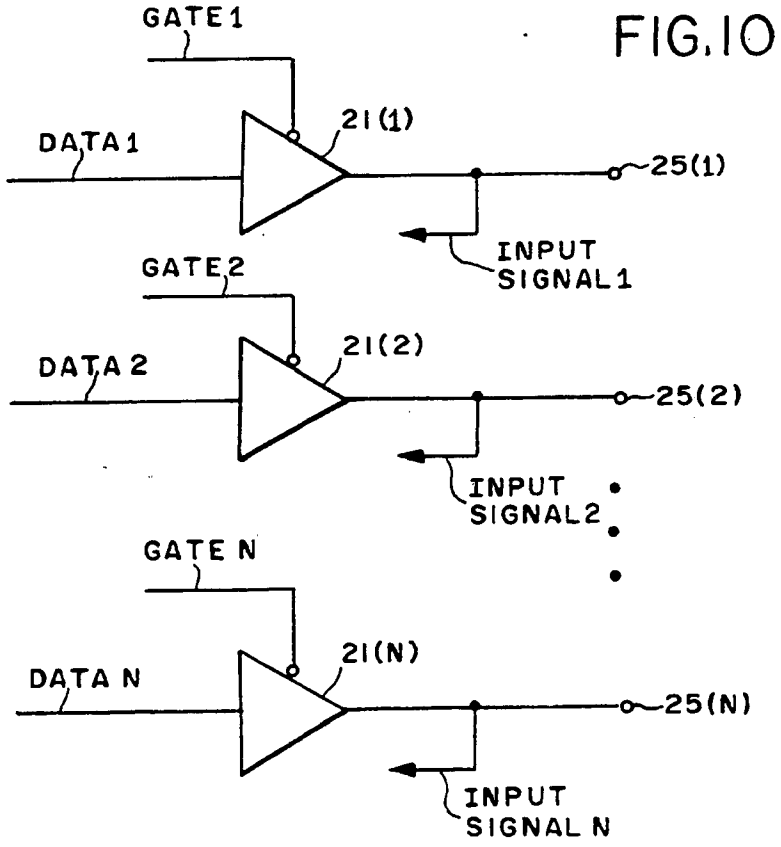

GATE1
DATA1
21(1)
25(1)
INPUT
SIGNAL1
GATE2
DATA 2
21(2)
25(2)
INPUT
SIGNAL2
GATE N
DATA N
21(N)
25(N)
INPUT
SIGNAL N

FIG.10

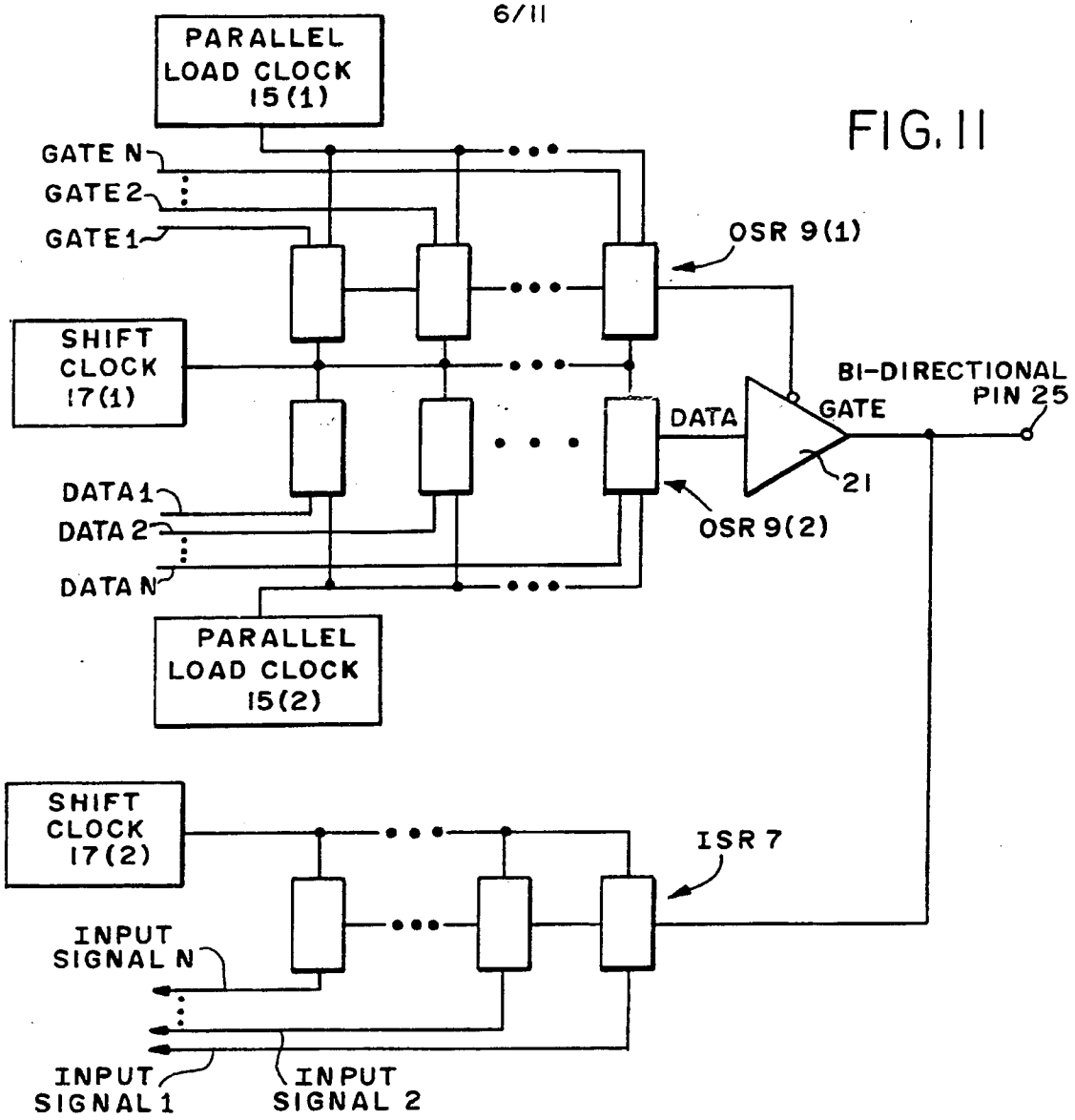

PARALLEL LOAD CLOCK 15(1)
GATE N
GATE 2
GATE 1
OSR 9(1)
SHIFT CLOCK 17(1)
BI-DIRECTIONAL PIN 25
DATA
GATE
21
DATA 1
DATA 2
DATA N
OSR 9(2)
PARALLEL LOAD CLOCK 15(2)
SHIFT CLOCK 17(2)
ISR 7
INPUT SIGNAL N
INPUT SIGNAL 1
INPUT SIGNAL 2

FIG. 11

FIG. 12

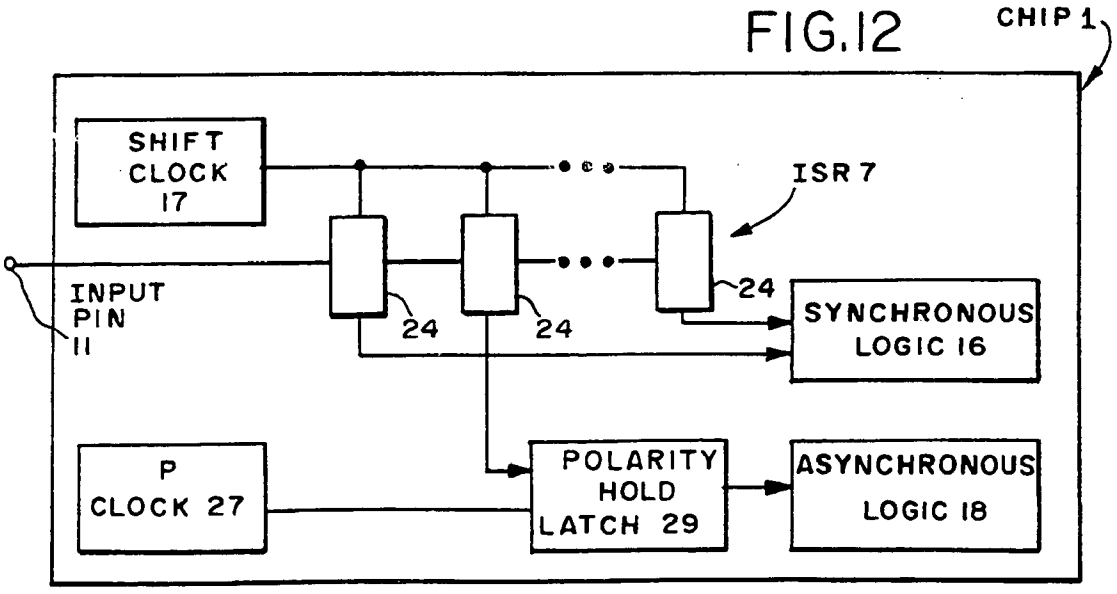

CHIP 1
SHIFT CLOCK 17
ISR 7
INPUT PIN 11
24
24
24
SYNCHRONOUS LOGIC 16
P CLOCK 27
POLARITY HOLD LATCH 29
ASYNCHRONOUS LOGIC 18

FIG.13

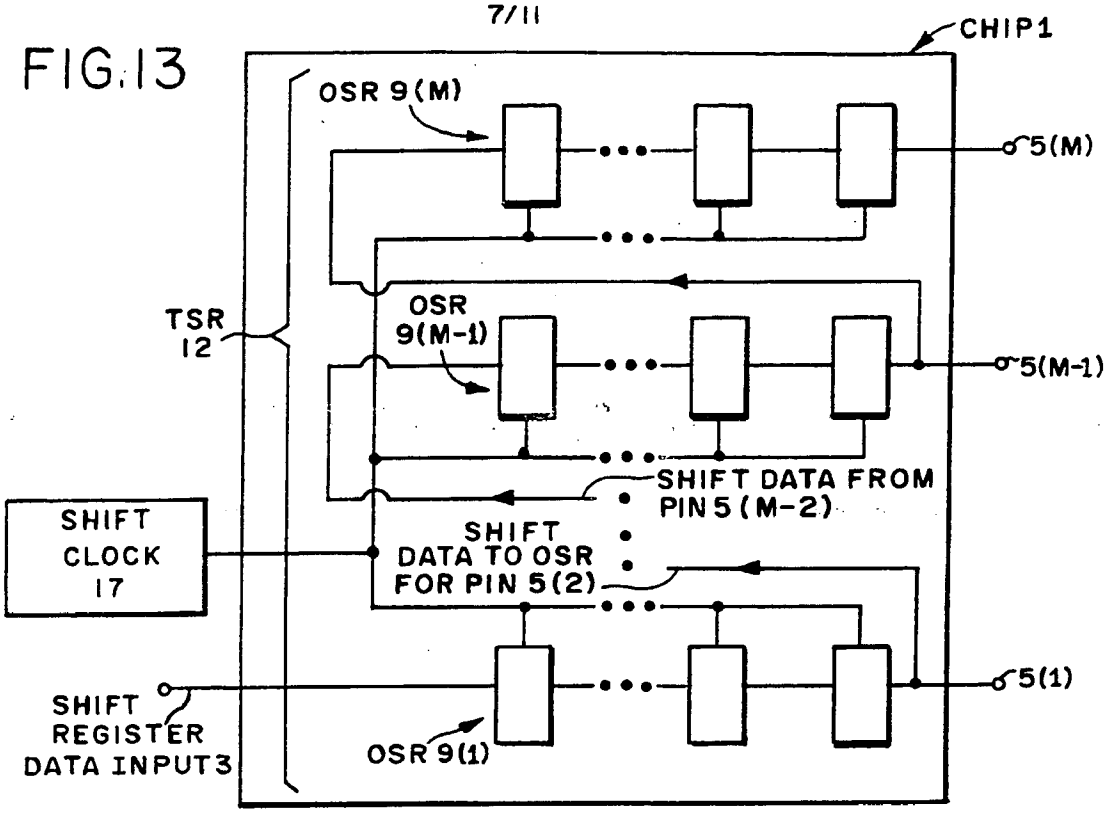

CHIP1
OSR 9(M)
5(M)
TSR 12
OSR 9(M-1)
5(M-1)
SHIFT DATA FROM PIN 5(M-2)
SHIFT CLOCK 17
SHIFT DATA TO OSR FOR PIN 5(2)
5(1)
SHIFT REGISTER DATA INPUT 3
OSR 9(1)

FIG.14

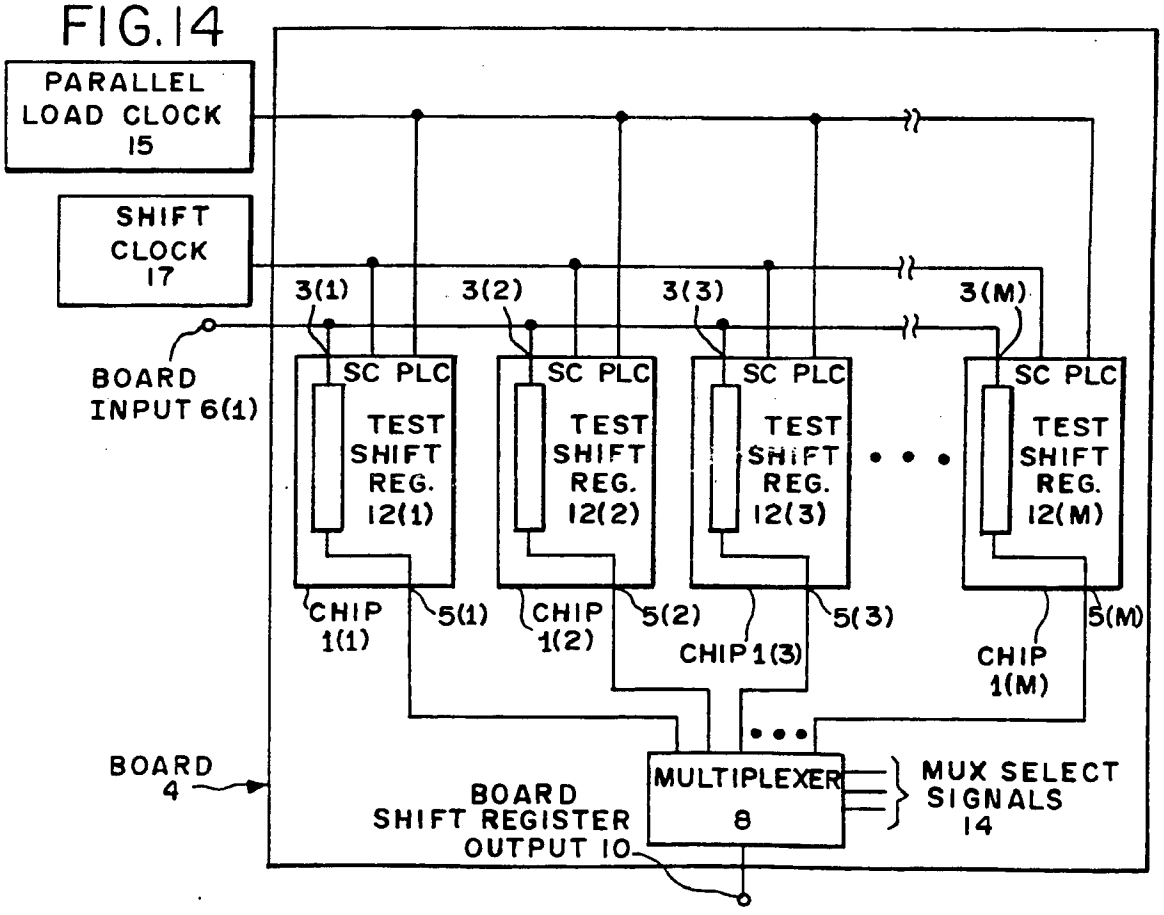

PARALLEL LOAD CLOCK 15
SHIFT CLOCK 17
3(1)
3(2)
3(3)
3(M)
BOARD INPUT 6(1)
SC PLC
TEST SHIFT REG. 12(1)
TEST SHIFT REG. 12(2)
TEST SHIFT REG. 12(3)
TEST SHIFT REG. 12(M)
CHIP 1(1)
5(1)
CHIP 1(2)
5(2)
CHIP 1(3)
5(3)
CHIP 1(M)
5(M)
BOARD 4
MULTIPLEXER 8
MUX SELECT SIGNALS 14
BOARD SHIFT REGISTER OUTPUT 10

FIG.15

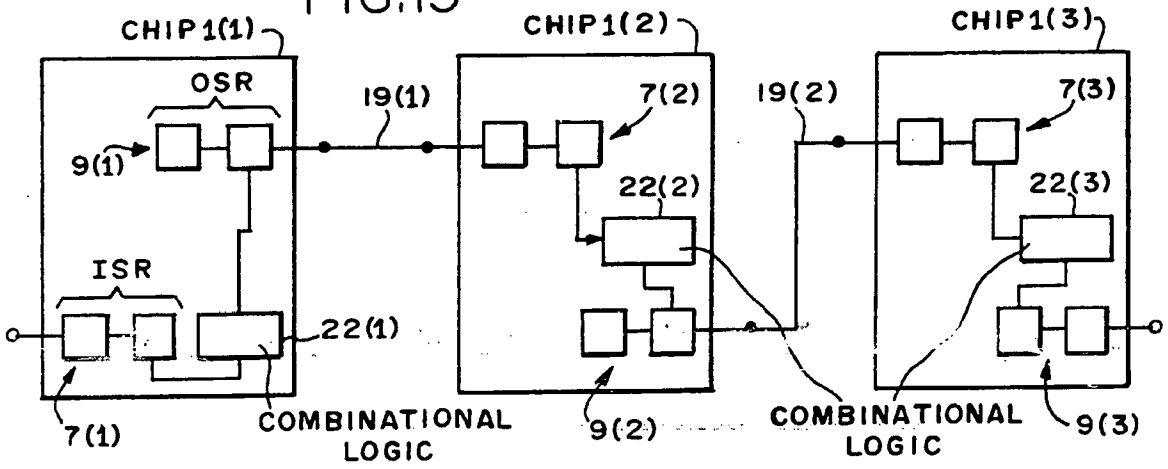


FIG.16

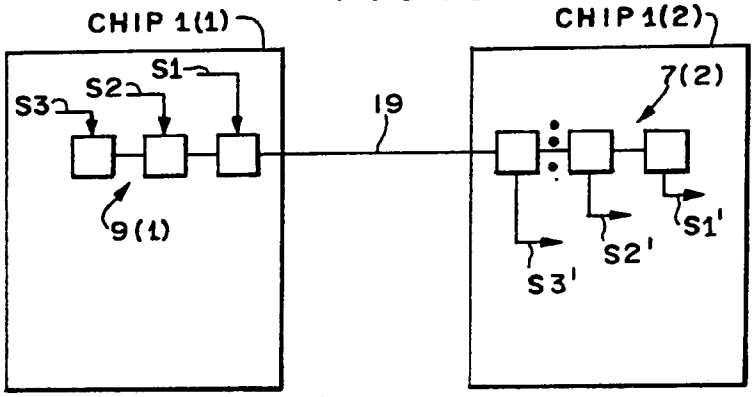


FIG.17

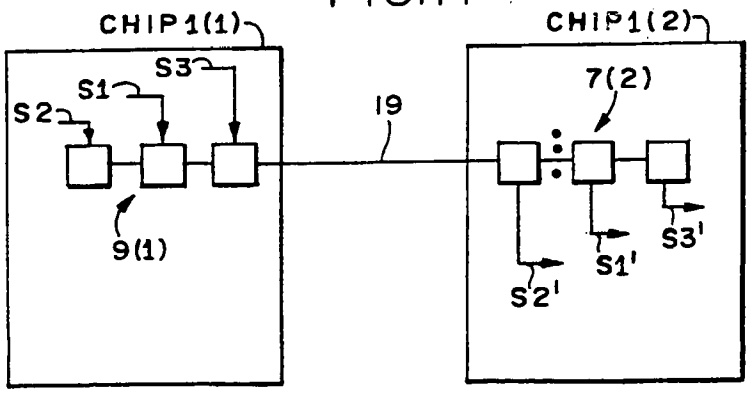
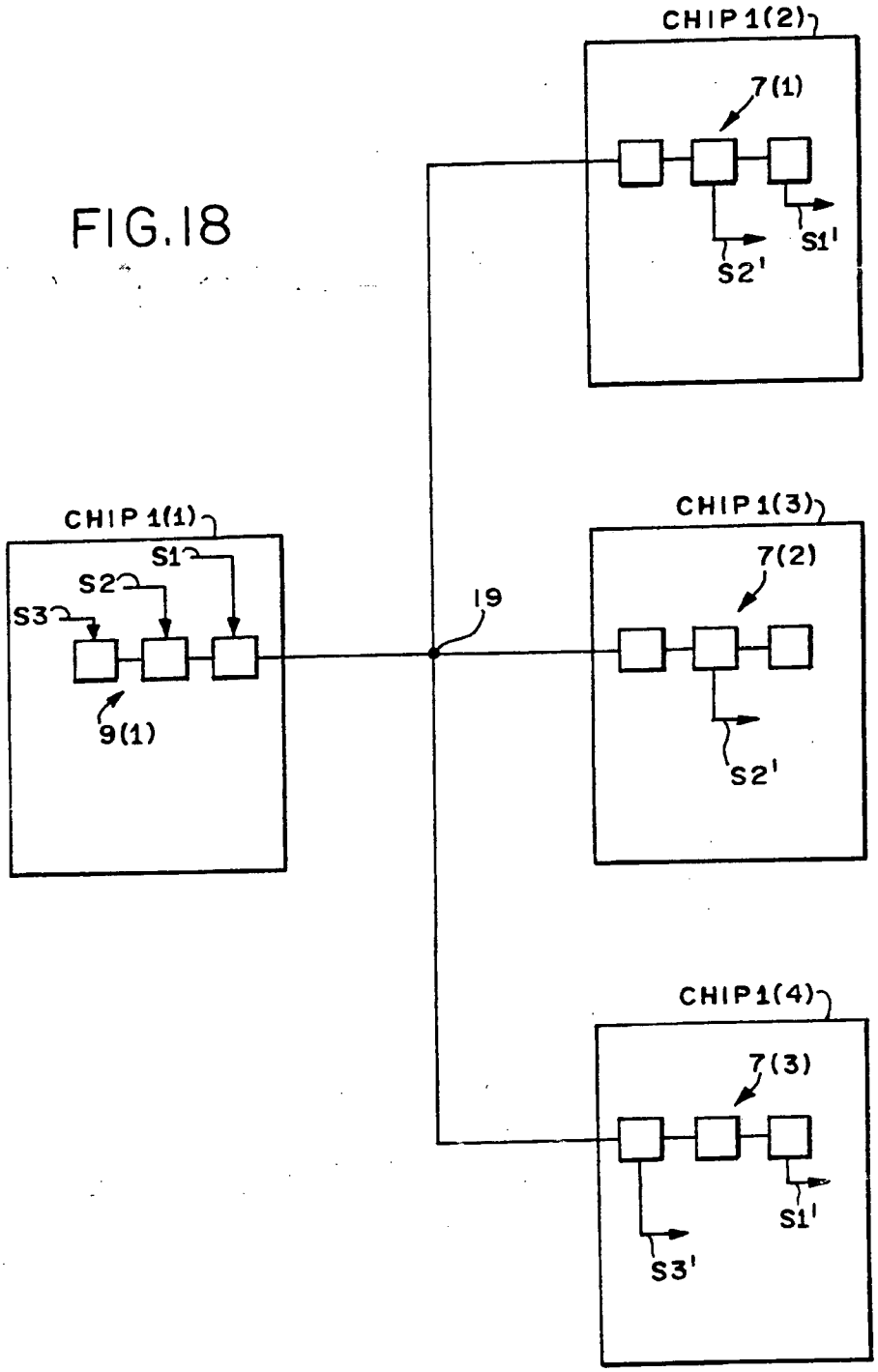


FIG.18


CHIP 1(2)
7(1)
S1'
S2'
CHIP 1(1)
S1
S2
S3
9(1)
19
CHIP 1(3)
7(2)
S2'
CHIP 1(4)
7(3)
S1'
S3'

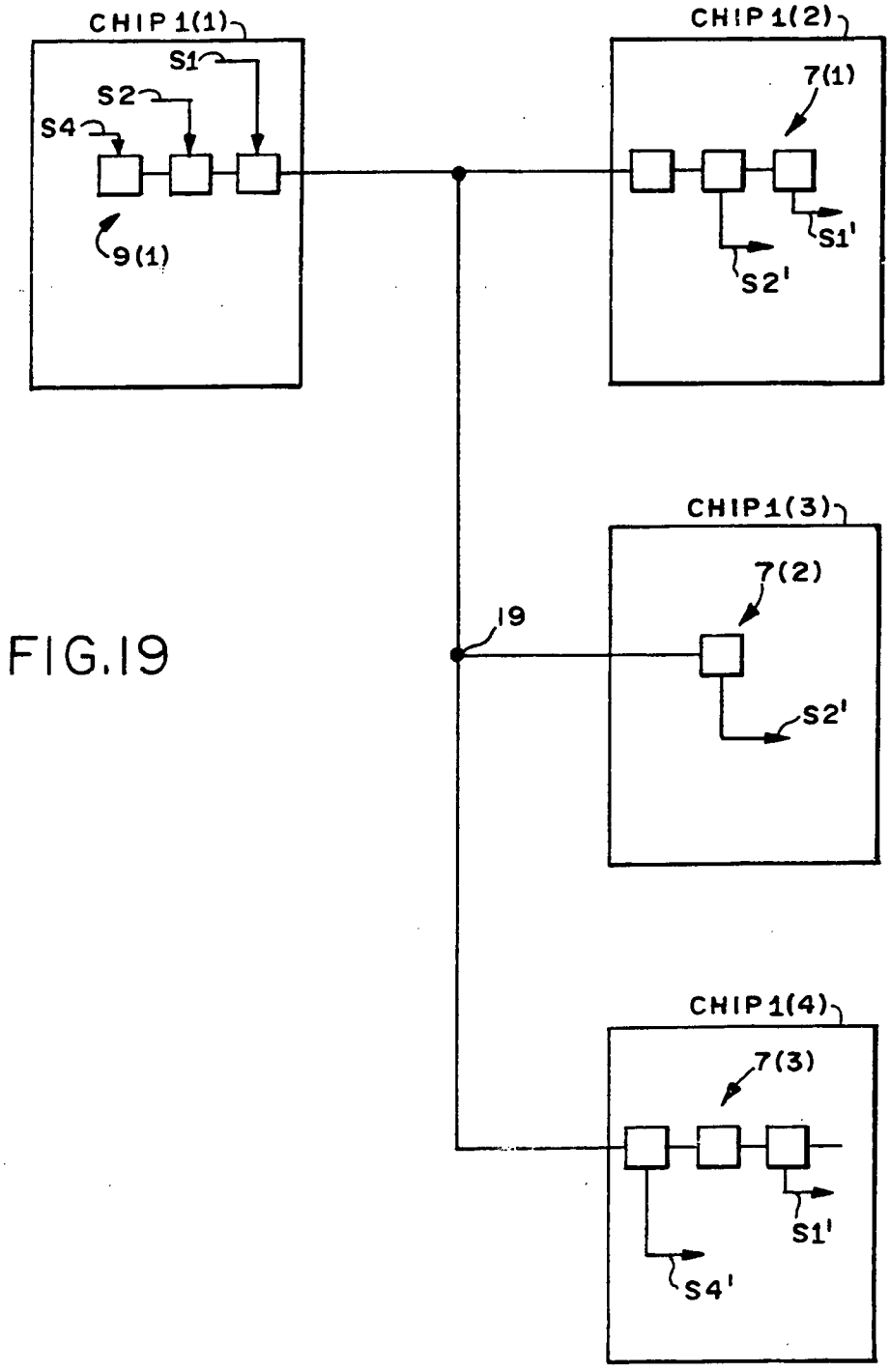

CHIP 1(1)
S1
S2
S4
9(1)
CHIP 1(2)
7(1)
S1'
S2'
CHIP1(3)
7(2)
19
S2'
CHIP1(4)
7(3)
S1'
S4'

FIG.19

FIG.20

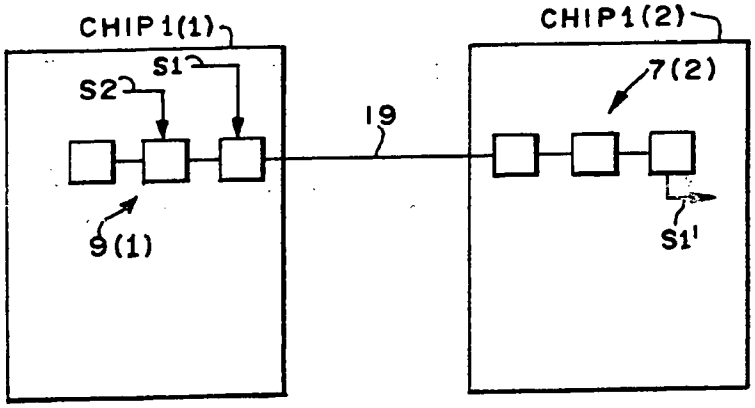


FIG.21

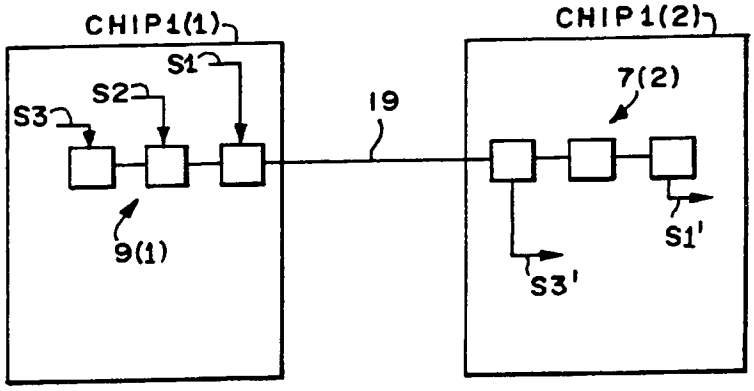
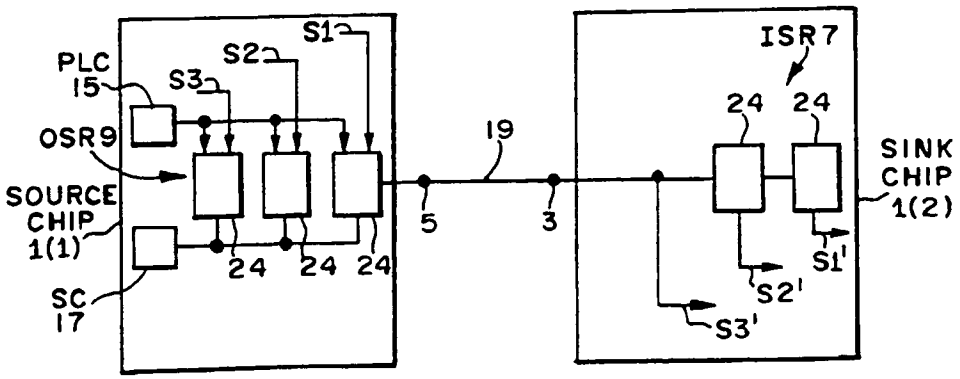


FIG.22



INTERNATIONAL SEARCH REPORT

International Application No PCT/US 92/07299

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H03K19/173; G06F1/22

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	H03K ; G06F

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No.[13]
X	MINI MICRO CONFERENCE RECORD May 1984, NEW YORK US pages 1 - 6 STANLEY 'versatile serial protocol for a microcomputer-peripheral interface' see the whole document	1,2,7, 12,13,14
Y		3
Y	GB,A,2 164 769 (INTERNATIONAL STANDARD ELECTRIC CORPORATION) 26 March 1986 see the whole document	3
A		4
A	PATENT ABSTRACTS OF JAPAN vol. 14, no. 238 (P-1050)21 May 1990 & JP,A,20 58 790 (MITSUBISHI ELECTRIC CORP.) 27 February 1990 see abstract	1,6,7

-/--

° Special categories of cited documents : [10]

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
28 APRIL 1993	11. 05. 93
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	FEUER F.S.

Form PCT/ISA/210 (second sheet) (January 1985)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A	EP,A,0 439 199 (ADVANCED MICRO DEVICES INC.) 31 July 1991 see the whole document	1,4

ANNEX TO THE INTERNATIONAL SEARCH REPORT
ON INTERNATIONAL PATENT APPLICATION NO. US 9207299
SA 64251

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB-A-2164769	26-03-86	US-A- 4656620	07-04-87
EP-A-0439199	31-07-91	US-A- 4758747	19-07-88
		EP-A- 0247809	02-12-87
		EP-A- 0428504	22-05-91
		JP-A- 63001215	06-01-88
		US-A- 4939391	03-07-90
		US-A- 5168177	01-12-92

EPO FORM P0479

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 7

Complete if Known	
Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 5,603,001	02-11-1997	Sukegawa et al.	
		US- 5,606,529	02-25-1997	Honma et al.	
		US- 5,619,470	04-08-1997	Fukumoto	
		US- 5,627,783	05-06-1997	Miyauchi	
		US- 5,640,349	06-17-1997	Kakinuma et al.	
		US- 5,222,046	06-22-1993	Kreifels et al.	
		US- 6,000,006	12-07-1999	Bruce et al.	
		US- 5,341,339	08-23-1994	Wells	
		US- 5,371,709	12-06-1994	Fisher et al.	
		US- 5,396,468	03-07-1995	Harari et al.	
		US- 5,406,529	04-11-1995	Asano	
		US- 5,459,850	10-17-1995	Clay et al.	
		US- 5,485,595	01-16-1996	Assar et al.	
		US- 5,488,711	01-30-1996	Hewitt et al.	
		US- 5,535,356	07-09-1996	Kim et al.	
		US- 5,542,082	07-30-1996	Solhjell	
		US- 5,548,741	08-20-1996	Watanabe	
		US- 5,568,423	10-22-1996	Jou et al.	
		US- 5,606,532	02-25-1997	Lambrache et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 6 of 7

Complete if Known	
Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		USPTO Notice of Allowability & attachment(s) mailed 7 January 2013 for US Application No. 12/876,247.	
		Office Action mailed 14 September 2012 for US Application No. 12/876,247.	
		Office Action mailed 01 February 2012 for US Application No. 12/876,247.	
		Office Action mailed 18 December 2013 for US Application No. 12/270,626.	
		Office Action mailed 15 March 2013 for US Application No. 12/270,626.	
		Office Action mailed 23 August 2012 for US Application No. 12/270,626.	
		Office Action mailed 03 February 2012 for US Application No. 12/270,626.	
		"Security Comes To SNMP: The SNMPv3 Proposed Internet Standards" http://www.cisco.com. vol. 3 no. 3, 8 pages.	
		Office Action mailed 05 October 2011 for US Application No. 12/270,626.	
		Office Action mailed 04 April 2011 for US Application No. 12/270,626.	

Examiner Signature		Date Considered	

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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 3 of 7

Complete if Known	
Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 5,737,742	04-07-1998	Achiwa et al.	
		US- 5,802,554	09-01-1998	Caceres et al.	
		US- 5,819,307	10-06-1998	Iwamoto et al.	
		US- 2002/0141244	10-03-2002	Bruce et al.	
		US- 2009/0094411	04-09-2009	Que, Jinzhen	
		US- 7,765,359	07-27-2010	Kang et al.	
		US- 2003/0204675	10-30-2003	Dover et al.	
		US- 7,103,684	09-05-2006	Chen et al.	
		US- 7,500,063	03-03-2009	Zohar et al.	
		US- 5,644,784	07-01-1997	Peek	
		US- 7,660,941	02-09-2010	Lee et al.	
		US- 2007/0130439	06-07-2007	Andersson et al.	
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]–Number[4]–Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
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PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 5 of 7

Complete if Known	
Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 2007/0174493	07-26-2007	Irish et al.	
		US- 2007/0195957	08-23-2007	Arulambalam et al.	
		US- 2004/0128553	07-01-2004	Buer et al.	
		US- 2003/0182576	09-25-2003	Morlang et al.	
		US- 2003/0223585	12-04-2003	Tardo et al.	
		US- 7,305,548	12-04-2007	Pierce et al.	
		US- 7,283,629	10-16-2007	Kaler et al.	
		US- 6,980,795	12-27-2005	Hermann et al.	
		US- 6,230,269	05-08-2001	Spies et al.	
		US- 6,215,875	04-10-2001	S. Nohda	
		US- 7,934,052	04-26-2011	Prins et al.	
		US- 6,901,499	05-31-2005	Aasheim et al.	
		US- 7,743,202	06-22-2010	Tsai et al.	
		US- 6,000,006	12-07-1999	Bruce et al.	
		US- 6,529,416	03-04-2003	Bruce et al.	
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
		JP 2005-309847	11-04-2005	Sharp Corp.		

Examiner Signature		Date Considered	

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(Use as many sheets as necessary)

Sheet 4 of 7

Complete if Known	
Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 5,875,351	02-23-1999	D. Riley	
		US- 5,881,264	03-09-1999	Y. Kurosawa	
		US- 5,918,033	06-29-1999	Heeb et al.	
		US- 5,943,421	08-24-1999	R. Grabon	
		US- 6,298,071	10-02-2001	Taylor et al.	
		US- 6,363,441	03-26-2002	Beniz et al.	
		US- 6,363,444	03-36-2002	Platko et al.	
		US- 6,404,772	06-11-2002	Beach et al.	
		US- 6,526,506	02-25-2003	D. Lewis	
		US- 6,557,095	04-29-2003	A. Henstrom	
		US- 6,857,076	02-15-2005	D. Klein	
		US- 6,970,446	11-29-2005	Krischar et al.	
		US- 7,194,766	03-20-2007	Noehring et al.	
		US- 7,372,962	06-13-2008	Fujimoto et al.	
		US- 7,620,748	11-17-2009	Bruce et al.	
		US- 7,716,389	05-11-2010	Bruce et al.	
		US- 2002/0073324	06-13-2002	Hsu et al.	
		US- 2007/0019573	01-25-2007	M. Nishimura	
		US- 2007/0083680	04-12-2007	King et al.	

FOREIGN PATENT DOCUMENTS

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Examiner Signature		Date Considered	

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/876,113	09/04/2010	Ricardo H. BRUCE	6005.042	1607

64180 7590 03/13/2014

URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

EXAMINER	
RUTZ, JARED IAN	
ART UNIT	PAPER NUMBER
2187	

NOTIFICATION DATE	DELIVERY MODE
03/13/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

stephen@uriartelaw.com
labid@uriartelaw.com
arnold@uriartelaw.com

Office Action Summary	Application No. 12/876,113	Applicant(s) BRUCE ET AL.	
	Examiner JARED RUTZ	Art Unit 2187	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/5/2014*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-97* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-97* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *2/5/2014*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

2. Claims 1-97, as amended on 10/21/2013, are pending in the instant application. Applicant's arguments submitted 10/21/2013 have been carefully and fully considered, but are not found persuasive. The instant Office action is made **FINAL**.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/21/2013 has been entered.

4. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Information Disclosure Statement

5. The information disclosure statement (IDS) submitted on 2/5/2014 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. **Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-97** are rejected under 35 U.S.C. 102(e) as being anticipated by Falik et al. (US 8,200,879).

Claim 1 is taught by Falik as:

A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising: addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Wherein a memory read transaction or a memory write transaction is performed on at least one of the first memory location or second memory location, wherein data is transferred to the first memory location of second memory location for a memory write transaction, wherein data is transferred from the first memory location or second memory location for a memory read transaction. Column 22 lines 16-20 shows that reading of data from memory and

modifying contents of the memory (i.e. erasing and programming) are carried out as transactions, initiated by appropriate commands and affected by the contents of the specified registers. Column 16 line 53 through column 17 line 24 further discusses the use of addresses to read and write data from the memory. Column 6 is an illustration of reads and writes to different addresses in different sections of the memory.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 2 is taught by Falik as:

The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 3 is taught by Falik as:

The method of claim 1, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

And said addressing said first memory location is made in response to a first memory transaction request. Column 18 lines 24-34 shows that applications on the main die 100 issue read and program commands.

And further including addressing said second memory location. Figure 6 shows that both sections can be addressed.

Claim 4 is taught by Falik as:

The method of claim 1, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 5 is taught by Falik as:

The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 6 is taught by Falik as:

The method of claim 5, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 7 is taught by Falik as:

The method of claim 5, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 8 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a memory device type attribute. Column 20 lines 30-36 shows that the registers can indicate if the device is self timed type flash memory or not.

Claim 9 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 10 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 11 is taught by Falik as:

The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size,

memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 12 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 13 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of attributes that differs in value from a second page size attribute from said second set of attributes. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 14 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 20 is taught by Falik as:

The method of claim 2, further including: using an address corresponding to a memory location from said first memory device and transferring a first data set. Column 16 lines 53-62 shows that an address and data are sent for a programming operation.

And using an address corresponding to a memory location from said second memory device and transferring a second data set. Column 14 lines 51-65 show that the standard address space is mapped to the logical sections into which the arrays are grouped, showing that the second memory device is accessed using an address corresponding to the second memory device.

Claim 21 is taught by Falik as:

The method of claim 20, wherein: said first set of attributes includes a first page size attribute. Column 20 lines 62-65 shows that the minimum

programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

And said first data set includes a first data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

And if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size. Column 27 lines 9-24 shows that when the number of bytes to be transferred to the FD have been transferred, the transfer process ends by setting the bus to a HiZ state.

Claim 25 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size attribute of said first memory device. As discussed at column 27 lines 33-60, the program buffer corresponds to the batch size, which is the amount of data which can be programmed into the flash array at once.

Claim 45 is taught by Falik as:

A memory controller for performing memory transactions, said memory controller comprising: a means for addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Wherein said means for addressing includes an interface controller means for processing memory transaction requests. Figure 4B, flash bus transactions state machine 116.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And said means for addressing uses attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 46 is taught by Falik as:

The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 47 is taught by Falik as:

The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 48 is taught by Falik as:

The memory controller of claim 46, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows

that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said use of said attributes from said first and second device profiles by said means for addressing includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 49 is taught by Falik as:

The memory controller of claim 46, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 50 is taught by Falik as:

The memory controller of claim 45, wherein said means for addressing further includes a means for addressing said second memory location. Figure 6 shows that both sections can be addressed.

Claim 51 is taught by Falik as:

The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 52 is taught by Falik as:

The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 53 is taught by Falik as:

The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 54 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6

shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 55 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 56 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 57 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size,

block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 58 is taught by Falik as:

The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

Claim 59 is taught by Falik as:

A memory controller comprising: an interface controller coupled to a memory device interface and an IO device interface. Figure 4B shows interface controller 110 connected to bus 90 and internal bus 140.

Said interface controller disposed to perform a memory transaction by addressing a first memory location, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column

16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And said addressing of said first memory location includes using said attributes from said first device profile. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 60 is taught by Falik as:

The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile. Figure 6 shows that both sections can be addressed.

Claim 69 is taught by Falik as:

The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-

48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

Claim 70 is taught by Falik as:

The memory controller of claim 59, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 71 is taught by Falik as:

The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 72 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 73 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 74 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 75 is taught by Falik as:

The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 76 is taught by Falik as:

The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 77 is taught by Falik as:

The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 78 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block

size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 79 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 80 is taught by Falik as:

An electronic storage device, comprising: a memory controller disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the

standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And said memory controller using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 81 is taught by Falik as:

The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command. Column 9 lines 5-18 shows that the interface performs appropriate requests for erasure.

Claim 82 is taught by Falik as:

The electronic storage device of claim 80, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 83 is taught by Falik as:

The electronic storage device of claim 80, said memory controller further disposed to: perform a write operation on said first memory device, if a memory transaction request is associated with a write request. Column 16 lines 53-64 shows that write transactions may be performed.

Perform a read operation on said first memory device, if said memory transaction request is associated with a read request. Column 16 lines 53-64 shows that read transactions may be performed.

And wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using said second device profile in response to receiving a second memory transaction request. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used for accesses to the groups of memory arrays.

Claim 84 is taught by Falik as:

The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 85 is taught by Falik as:

The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 86 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 87 is taught by Falik as:

The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20

line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 88 is taught by Falik as:

The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 89 is taught by Falik as:

The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

Claim 90 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 91 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 92 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 94 is taught by Falik as:

The method of claim 1, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 95 is taught by Falik as:

The memory controller of claim 45, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 96 is taught by Falik as:

The memory controller of claim 59, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 97 is taught by Falik as:

The electronic device of claim 80, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which

may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claims 15, 18, and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Nangle (US 7,330,954).

Claim 15 is taught by Falik as:

The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device. Column 21 lines 7-10 shows that the information can correspond to a flash device FD.

Although Falik column 21 lines 7-10 shows that other memory technologies such as SRAM may be used, it does not expressly teach that the second memory device attribute corresponds to a DRAM device interface.

With respect to claim 15, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 lines 51-67 shows that the memory devices may be flash memory and DRAM.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include flash memory and DRAM in the system of Falik.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 15**.

Claim 18 is taught by Falik as shown supra with respect to claim 8.

Falik does not expressly teach that said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

With respect to claim 18, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 line 51 through column 5 line 4 shows that the memory devices may be volatile memory that have a battery backup.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a volatile memory disposed to receive backup power from a portable power source.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 18**.

Claim 19 is taught by Falik as shown supra with respect to claim 8.

Falik does not expressly teach that said first memory device type attribute corresponds to a NAND flash memory device and said second memory device type attribute corresponds to a NOR flash memory device.

With respect to claim 19, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 lines 51-65 shows that the memory devices may be NAND or NOR type flash memories.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a volatile memory disposed to receive backup power from a portable power source.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 19**.

10. **Claims 16, 17, 22-24, and 93** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Sinclair et al. (US 2006/0184723).

Claim 16 if taught by Falik as shown supra with respect to claim 2.

Although Falik teaches that the width of the array is the minimum programming size of the array at column 20 lines 62-65, and that the width of the array is stored at column 20 lines 49-52, Falik does not expressly teach that a first and second partial page size attribute is stored and used.

With respect to claim 16, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claims 16 and 17**.

Claim 17 is taught by Falik and Sinclair as:

The method of claim 16: said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute. Sinclair paragraph 0168 shows that in a flash memory that supports partial page programming, when sufficient data is transferred to the buffer, it is programmed to the page. Falik column 14 lines 51-60 and figure 3 shows that the first memory device group can be accessed.

And further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute. Sinclair paragraph 0168 shows that in a flash memory that supports partial page programming, when sufficient data is transferred to the buffer, it is programmed to the page. Falik column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

Claim 22 is taught by Falik as:

The method of claim 20, wherein: said second set of attributes includes a second page size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

And said second data set includes a second data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

And if said second data set size is greater than said second page size attribute, said transferring said second data set includes: performing a set of write operations on said second memory device that includes using a second transfer size equal to said second page size attribute. Column 16 lines 48-52 shows that program buffer 19 may be a double buffer, allowing the programming of one chunk of data while another chunk of data is received. As discussed at column 27 lines 33-60, the program buffer corresponds to the batch size, which is the amount of data which can be programmed into the flash array at once.

Falik does not expressly teach that the transaction is made using a transfer size equal to the page size until a remaining portion of said second data set that has not yet been written to said second device is less than said second page size attribute and using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

With respect to claim 22, Sinclair teaches Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times. As discussed in paragraph 0168, when the end of the data group is received in the buffer and it is smaller than a full page of data, a partial page programming operation may be performed.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 22**.

Claim 23 is taught by Falik as:

The method of claim 20, wherein: said first set of attributes includes a page size attribute and a block size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Said first data set includes a first data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

If said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes: performing a set of write

operations on said first memory device that includes using a second transfer size equal to said page size attribute [...]. Column 27 lines 14-24 shows that bytes of data are sent until all the bytes have been sent.

Falik does not expressly teach that the transaction is made using a transfer size equal to the page size until a remaining portion of said first data set that has not yet been written to said first device is less than said first page size attribute and using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

With respect to claim 23, Sinclair teaches Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times. As discussed in paragraph 0168, when the end of the data group is received in the buffer and it is smaller than a full page of data, a partial page programming operation may be performed.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 23**.

Claim 24 is taught by Falik as shown supra with respect to claim 1, and further as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes: performing respective write operations on said first and second memory devices by at least using a transfer size at least equal to a […] *page size attribute from said first set of attributes*. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations.

And performing at least one write operation on said second memory device by at least using a transfer size at least equal to a […] *page size attribute value from said second set of attributes*. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations. Column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

And said attribute difference includes different attribute values of said first and second […] *page size attributes*. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Although Falik teaches storing a page size attribute, it does not expressly teach storing a partial page size attribute.

With respect to claim 24, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 24**.

Claim 93 is taught by Falik as shown supra with respect to claim 80, and further as:

The electronic storage device of claim 80, wherein said memory controller is further adapted to: use a first partial page size attribute by performing a write operation on said first memory device and using a transfer size at least equal to said partial page size attribute. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing address locations.

And use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute. Column 16 lines 53-62 shows that programming is carried out in a block to be stored in sequentially increasing

address locations. Column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

Although Falik teaches storing a page size attribute, it does not expressly teach storing a partial page size attribute.

With respect to claim 93, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 93**.

11. **Claims 26-28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Lakhani et al. (US 6,961,805).

Claim 26 is taught by Falik as shown supra with respect to claim 1.

Falik further teaches, at column 20 lines 60-65, that Page Size Block1 stores the size of the minimal segment of a flash array erasable upon a single erase command.

Additionally, column 16 line 53 through column 17 line 24 shows that data can be written to a block of addresses by designating the starting address and performing a series of program continue operations.

Falik does not expressly teach using the block size attribute in performing a write operation that uses a transfer size that corresponds to the block size.

With respect to claim 26, Lakhani teaches, at column 18 lines 19-46, that predecoder 50 asserts sets of multiblock selection bits in response to control bits from the controller, which allows a designated number of blocks to be selected for writing at the same time.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to perform a write operation that uses a transfer size equal to the a block size attribute value that corresponds to a block size attribute of the first memory device.

The motivation for doing so would have been to reduce the time used to test the memory cells of the block, Lakhani column 8 lines 21-32.

Therefore, it would have been obvious to combine Lakhani with Falik to obtain the invention as specified in **claims 26 and 27**.

Claim 27 is taught by Lakhani as:

The method of claim 26, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a

transfer size equal to a multiple of said block size attribute value. Column 13 lines 25-38 shows that a plurality of blocks can be selected at the same time.

Claim 28 is taught by Falik as shown supra with respect to claim 2.

Falik further teaches, at column 20 lines 60-65, that Page Size Block1 stores the size of the minimal segment of a flash array erasable upon a single erase command. Additionally, column 16 line 53 through column 17 line 24 shows that data can be written to a block of addresses by designating the starting address and performing a series of program continue operations.

Falik does not expressly teach using the block size attribute in performing a write operation that uses a transfer size that is equal to a multiple of the block size.

With respect to claim 28, Lakhani teaches, at column 18 lines 19-46, that predecoder 50 asserts sets of multiblock selection bits in response to control bits from the controller, which allows a designated number of blocks to be selected for writing at the same time.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to perform a write operation that uses a transfer size equal to the a block size attribute value that corresponds to a block size attribute of the first memory device.

The motivation for doing so would have been to reduce the time used to test the memory cells of the block, Lakhani column 8 lines 21-32.

Therefore, it would have been obvious to combine Lakhani with Falik to obtain the invention as specified in **claim 28**.

12. **Claims 29-44** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Rubinstein et al. (US 5,913,215).

Claim 29 is taught by Falik as:

Said method comprising: addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Said first device profile representing a first set of attributes of said first memory device, and said second device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14

lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Falik does not expressly teach that the methods may be implemented using a non-transitory computer readable medium comprising computer executable instructions.

With respect to claim 29, Rubinstein teaches at column 10, lines 3-15, that computer methods may be performed either by a series of instructions, or by specific hardware components that contain hard-wired logic for performing the method, or by any combination of the two.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a computer readable medium comprising computer executable instructions.

The rationale for doing so would have been that it is a known technique to implement methods in computer systems using a non-transitory computer readable medium comprising computer executable instructions.

Therefore, it would have been obvious to combine Rubinstein with Falik to obtain the invention as recited in **claims 29-44**.

Claim 30 is taught by Falik as:

The computer readable medium of claim 29, wherein: said first memory location is part of a memory space associated with a first memory device, said

second memory location is part of a memory space associated with a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

And said first and second memory devices comprise at least a portion of a memory store. Figure 3 shows that the address space is mapped to the memory devices.

Claim 31 is taught by Falik as:

The computer readable medium of claim 29, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of a first memory device and a block size value of a second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 32 is taught by Falik as:

The computer readable medium of claim 30, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 33 is taught by Falik as:

The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 34 is taught by Falik as:

The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

Claim 35 is taught by Falik as:

The computer readable medium of claim 29, wherein said addressing further includes: said first and second device profiles having at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 36 is taught by Falik as:

The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 37 is taught by Falik as:

The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 38 is taught by Falik as:

The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 39 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 40 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 41 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 42 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 43 is taught by Falik as:

The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 44 is taught by Falik as:

The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

13. **Claims 61 and 64-68** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Chin et al. (US 2001/0010066).

Claim 61 is taught by Falik as shown supra with respect to claim 59.

Falik further teaches:

The memory controller of claim 59, wherein said interface controller includes: A first memory bus controller coupled to said control device and said memory device interface. Falik figure 4b item 116.

And an IO bus controller coupled to said IO device interface and said control device. Falik figure 4b item 117.

With respect to claim 61, Chin figure 2 teaches a bridge unit 104, which connects to a CPU bus 108 and a memory bus 110, including control logic 242, shown in paragraph 0037 to direct the operations of the queue storage elements through a network of control signals. Figure 2 also illustrates a data path between the CPU bus 108 and memory bus 110 through queues 250 and 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a main control device coupled to the memory device interface and data path as taught by Chin in the interface controller of Falik.

The motivation for doing so would have been to provide a means to manage the transfer of data through the interface performed by the system of Falik, see Chin paragraph 0037.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as specified in **claim 61**.

Claim 64 is taught by Falik as shown supra with respect to claim 59.

Falik does not expressly teach that a buffer is a FIFO or that a data path includes a plurality of queue slots.

With respect to claim 64, Chin teaches:

Further including a buffer comprising a FIFO. Paragraph 0052 shows that queue 250 is a FIFO.

And a data path that includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory. Figure 2 also shows read queue 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a FIFO and a data path including a plurality of queue slots in the system of Falik.

The motivation for doing so would have been to provide an interface that provides all devices in a computer system fair access to memory, Chin paragraph 0012.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as recited in **claim 64**.

Claim 65 is taught by Falik as shown supra with respect to claim 59.

Falik does not expressly teach that a data path includes a buffer having a plurality of queue slots.

With respect to claim 65, Chin teaches:

The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a FIFO and a data path including a plurality of queue slots in the system of Falik.

The motivation for doing so would have been to provide an interface that provides all devices in a computer system fair access to memory, Chin paragraph 0012.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as recited in **claims 65-67**.

Claim 66 is taught by Chin as:

The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a plurality of queue slots that buffer data from said IO device interface to said memory device interface. Paragraph 0052 shows that queue 250 has a plurality of slots for data being written from the CPU to memory.

Claim 67 is taught by Chin as:

The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from

said memory device interface to said IO device interface. Figure 2 also shows read queue 252.

Claim 68 is taught by Falik as shown supra with respect to claim 1.

Falik further teaches a memory bus controller, figure 4b item 116, coupled to bus 90.

Falik does not expressly teach that the memory bus controller is coupled to a main control device.

With respect to claim 68, Chin teaches:

A second memory bus controller coupled to said main control device and said memory device interface. Figure 2 teaches a bridge unit 104, which connects to a CPU bus 108 and a memory bus 110, including control logic 242, shown in paragraph 0037 to direct the operations of the queue storage elements through a network of control signals. Figure 2 also illustrates a data path between the CPU bus 108 and memory bus 110 through queues 250 and 252.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a main control device coupled to the memory device interface and data path as taught by Chin in the interface controller of Falik.

The motivation for doing so would have been to provide a means to manage the transfer of data through the interface performed by the system of Falik, see Chin paragraph 0037.

Therefore, it would have been obvious to combine Chin with Falik to obtain the invention as specified in **claim 68**.

14. **Claims 62 and 63** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Chin et al. (US 2001/0010066) as applied to claim 61 above, and further in view of Tsuruta (US 2007/0174506).

Claim 62 is taught by the combination of Falik and Chin as shown supra with respect to claim 61.

The combination of Falik and Chin does not expressly teach that the IO bus controller is disposed to respond to said memory transaction request by acknowledging said request and providing status to said main control device.

With respect to claim 62, Tsuruta teaches:

Wherein said IO bus controller is disposed to respond to a memory transaction request by acknowledging said request and providing status to said main control device. Paragraph 0183 shows that in response to a read req from the CPU, MEM-DMAC 232 issues a read ack signal. Paragraph 0186 shows that after the read operation is performed, a sequencer in the memory controller 231 issues ack to a sequencer in the MEM-DMAC 232.

At the time of the invention, it would have been obvious to use the acknowledgement system of Tsuruta in the combination of Falik and Chin.

The motivation for doing so would have been to provide coordination between the CPU interface and the read/write queues to perform the requested memory operations.

Therefore, it would have been obvious to combine Tsuruta with Falik and Chin to obtain the invention as specified in **claims 62 and 63**.

Claim 63 is taught by Chin as:

The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction. Paragraph 0052 shows that control logic provides control signals to the input and output selectors 351 and 353 that determine the values of the enable and select signals in response to a memory request from the CPU.

Coordinates the operation of said memory device interface. Paragraph 0052 shows that the data and address of each request is sent to the memory controller 200.

And manages the transfer of memory transaction data between said IO device interface and said memory device interface through a data path. Paragraph 0052 shows that data is transferred through the queue 250.

Response to Arguments

15. Applicant's arguments filed 10/21/2013 have been carefully and fully considered but they are not persuasive.

16. In the second paragraph beginning on page 24 of the remarks submitted 10/21/2013, Applicant argues:

> "In contrast, Falik does not disclose associating any device profiles with a memory location used for a memory read or memory write transaction."

17. The Examiner respectfully disagrees. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

18. In the first paragraph beginning on page 25 of the remarks submitted 10/21/2013, Applicant argues:

> "In contrast, Falik discloses characteristics of each logical section 57 (Falik: column 15, line 63), and these logical sections contain logical blocks (and these logical blocks are Main Block 51 and Information Block 52) (Falik: column 14, line 51-56). Therefore, Falik discloses logical sections as associated with these characteristics. However, these logical blocks in these logical sections are for storing data used by any application in a Main Device, or for storing auxiliary data (e.g., configuration data or control data) used by the Main Device or application programs (Falik: column 14, lines 21-31 and lines 51-58). Therefore, these logical blocks (and logical sections that contain these logical blocks) are not addressable sections used for a memory read or memory write transaction. Therefore, Falik does not disclose these logical sections as memory locations that are addressed. Accordingly, Falik does not disclose all the limitations of claim 1."

19. The Examiner respectfully disagrees. Initially, the Examiner respectfully notes that Applicant has provided no rational support for the statement that data used by a device is not read or written. Further, the Examiner respectfully notes that Falik column 22 lines 16-20 expressly states that reading of data from memory and modifying contents of the memory (i.e. erasing and programming) are carried out as transactions, initiated by appropriate commands and affected by the contents of the specified

registers. Column 16 line 53 through column 17 line 24 further discusses the use of addresses to read and write data from the memory.

20. In the first paragraph beginning on page 26 of the remarks submitted 10/21/2013, Applicant argues:

> "Falik further discloses the device and status control register (Falik: Figure 5A) which provides status and control information for an entire memory device (Falik: column 19, lines 4-8). Falik also discloses a flash device capabilities register (Falik: Figure 5B) that provides capabilities and properties information on the same entire memory device (Falik: column 19, lines 49-53). Therefore, these registers contain information directed to the same entire memory device and not directed to different memory locations. These registers do not contain a first set of attributes of a first memory location and also do not contain a second set of attributes of a second memory location."

21. The Examiner respectfully disagrees. Falik column 20 lines 49-55 states: Section Properties Register 'i' (FIG. 5C) is a read-only register, of double-word length, that provides to the MD (By means of the Section Properties Read command) information on the structural properties of Section 'i' of the flash device. There is one such register for each of the sections in the device..." Accordingly, there are a first set of attributes of a first memory location and a second set of attributes of a second memory location.

22. In the fourth paragraph beginning on page 29 of the remarks submitted 10/21/2013, Applicant argues:

> "The Office admits that Falik does not expressly teach that the methods may be implemented using a computer readable medium comprising computer executable instructions. In order to supply the missing limitations, the Office combines Falik with Rubinstein. The Office argues it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a computer readable medium comprising computer executable instructions (Office Action: page 44). The Applicants respectfully disagree with the assertions of the Office."

23. The Examiner respectfully disagrees, and notes that as shown by Rubinstein, the implementation of methods in software stored in computer readable media is well known to one of ordinary skill in the art.

Conclusion

24. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JARED RUTZ whose telephone number is (571)272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, April Blair can be reached on (571)270-1014. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jared I Rutz
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Art Unit 2187

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

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Complete if Known	
Application Number	12/876,113
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First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
		JP 2005-309847	11-04-2005	Sharp Corp.		

Examiner Signature	/Jared Rutz/	Date Considered	03/10/2014

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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PTO/SB/08a (07-09)
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 7

Complete if Known	
Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 5,603,001	02-11-1997	Sukegawa et al.	
		US- 5,606,529	02-25-1997	Honma et al.	
		US- 5,619,470	04-08-1997	Fukumoto	
		US- 5,627,783	05-06-1997	Miyauchi	
		US- 5,640,349	06-17-1997	Kakinuma et al.	
		US- 5,222,046	06-22-1993	Kreifels et al.	
		US- 6,000,006	12-07-1999	Bruce et al.	
		US- 5,341,339	08-23-1994	Wells	
		US- 5,371,709	12-06-1994	Fisher et al.	
		US- 5,396,468	03-07-1995	Harari et al.	
		US- 5,406,529	04-11-1995	Asano	
		US- 5,459,850	10-17-1995	Clay et al.	
		US- 5,485,595	01-16-1996	Assar et al.	
		US- 5,488,711	01-30-1996	Hewitt et al.	
		US- 5,535,356	07-09-1996	Kim et al.	
		US- 5,542,082	07-30-1996	Solhjell	
		US- 5,548,741	08-20-1996	Watanabe	
		US- 5,568,423	10-22-1996	Jou et al.	
		US- 5,606,532	02-25-1997	Lambrache et al.	

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(Use as many sheets as necessary)

Sheet 6 of 7

Complete if Known	
Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		USPTO Notice of Allowability & attachment(s) mailed 7 January 2013 for US Application No. 12/876,247.	
		Office Action mailed 14 September 2012 for US Application No. 12/876,247.	
		Office Action mailed 01 February 2012 for US Application No. 12/876,247.	
		Office Action mailed 18 December 2013 for US Application No. 12/270,626.	
		Office Action mailed 15 March 2013 for US Application No. 12/270,626.	
		Office Action mailed 23 August 2012 for US Application No. 12/270,626.	
		Office Action mailed 03 February 2012 for US Application No. 12/270,626.	
		"Security Comes To SNMP: The SNMPv3 Proposed Internet Standards" http://www.cisco.com. vol. 3 no. 3, 8 pages.	
		Office Action mailed 05 October 2011 for US Application No. 12/270,626.	
		Office Action mailed 04 April 2011 for US Application No. 12/270,626.	

Examiner Signature	/Jared Rutz/	Date Considered	03/10/2014

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12876113	BRUCE ET AL.
	Examiner	Art Unit
	JARED RUTZ	2187

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
inventor search in EAST	12/14/2012	jir
text search in EAST, see search history	12/14/2012	jir
internet search using google.com	12/14/2012	jir
updated search in EAST	5/7/2013	jir
updated search in EAST	3/8/2014	jir

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 7

Complete if Known	
Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

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		US- 5,822,251	10-13-1998	Bruce et al.	
		US- 4,752,871	06-21-1988	Sparks	
		US- 5,297,148	03-22-1994	Harari et al.	
		US- 5,379,401	01-03-1995	Robinson et al.	
		US- 5,388,083	02-07-1995	Assar et al.	
		US- 5,432,748	07-11-1995	Hsu et al.	
		US- 5,448,577	09-05-1995	Wells et al.	
		US- 5,479,638	12-26-1995	Assar et al.	
		US- 5,500,826	03-19-1996	Hsu et al.	
		US- 5,509,134	04-16-1996	Fandrich et al.	
		US- 5,513,138	04-30-1996	Manabe et al.	
		US- 5,524,231	06-04-1996	Brown	
		US- 5,530,828	06-25-1996	Kaki et al.	
		US- 5,535,328	07-09-1996	Harari et al.	
		US- 5,559,956	09-24-1996	Sukegawa	
		US- 5,568,439	10-22-1996	Harari	
		US- 5,572,466	11-05-1996	Sukegawa	
		US- 5,594,883	01-14-1997	Pricer	
		US- 5,602,987	02-11-1997	Harari et al.	

FOREIGN PATENT DOCUMENTS

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		WO 94/06210	03-17-1994	Prabhakar Goel		

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Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 5,737,742	04-07-1998	Achiwa et al.	
		US- 5,802,554	09-01-1998	Caceres et al.	
		US- 5,819,307	10-06-1998	Iwamoto et al.	
		US- 2002/0141244	10-03-2002	Bruce et al.	
		US- 2009/0094411	04-09-2009	Que, Jinzhen	
		US- 7,765,359	07-27-2010	Kang et al.	
		US- 2003/0204675	10-30-2003	Dover et al.	
		US- 7,103,684	09-05-2006	Chen et al.	
		US- 7,500,063	03-03-2009	Zohar et al.	
		US- 5,644,784	07-01-1997	Peek	
		US- 7,660,941	02-09-2010	Lee et al.	
		US- 2007/0130439	06-07-2007	Andersson et al.	
		US-			
		US-			
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		US-			
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		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature	/Jared Rutz/	Date Considered	03/10/2014

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.R./

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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PTO/SB/08a (07-09)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 4 of 7

Complete if Known	
Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 5,875,351	02-23-1999	D. Riley	
		US- 5,881,264	03-09-1999	Y. Kurosawa	
		US- 5,918,033	06-29-1999	Heeb et al.	
		US- 5,943,421	08-24-1999	R. Grabon	
		US- 6,298,071	10-02-2001	Taylor et al.	
		US- 6,363,441	03-26-2002	Beniz et al.	
		US- 6,363,444	03-36-2002	Platko et al.	
		US- 6,404,772	06-11-2002	Beach et al.	
		US- 6,526,506	02-25-2003	D. Lewis	
		US- 6,557,095	04-29-2003	A. Henstrom	
		US- 6,857,076	02-15-2005	D. Klein	
		US- 6,970,446	11-29-2005	Krischar et al.	
		US- 7,194,766	03-20-2007	Noehring et al.	
		US- 7,372,962	06-13-2008	Fujimoto et al.	
		US- 7,620,748	11-17-2009	Bruce et al.	
		US- 7,716,389	05-11-2010	Bruce et al.	
		US- 2002/0073324	06-13-2002	Hsu et al.	
		US- 2007/0019573	01-25-2007	M. Nishimura	
		US- 2007/0083680	04-12-2007	King et al.	

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Examiner Signature	/Jared Rutz/	Date Considered	03/10/2014

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Sheet 7 of 7

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Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Office Action mailed 08 October 2013 for US Application No. 13/890,229.	
		Notice of Allowability (and Examiner's Comment) mailed 30 May 2013 for US Application No. 12/882,059.	
		Notice of Allowability (and Examiner's Comment and Statement of Reasons for Allowance) mailed 14 February 2013 for US Application No. 12/882,059.	
		Office Action mailed 11 May 2012 for US Application No. 12/882,059.	
		Notice of Allowability (and Examiner's Comment and Statement of Reasons for Allowance) mailed 07 January 2013 for US Application No. 12/876,247.	
		Office Action mailed 14 September 2012 for US Application No. 12/876,247.	
		Office Action mailed 01 February 2012 for US Application No. 12/876,247.	

Examiner Signature	/Jared Rutz/	Date Considered	03/10/2014

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12876113	BRUCE ET AL.
	Examiner	**Art Unit**
	JARED RUTZ	2187

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/14/2012	05/07/2013	03/08/2014						
	1	✓	✓	✓						
	2	✓	✓	✓						
	3	✓	✓	✓						
	4	✓	✓	✓						
	5	✓	✓	✓						
	6	✓	✓	✓						
	7	✓	✓	✓						
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	33	✓	✓	✓						
	34	✓	✓	✓						
	35	✓	✓	✓						
	36	✓	✓	✓						

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	12876113	BRUCE ET AL.
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CLAIM		DATE								
Final	Original	12/14/2012	05/07/2013	03/08/2014						
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	38	✓	✓	✓						
	39	✓	✓	✓						
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	69	✓	✓	✓						
	70	✓	✓	✓						
	71	✓	✓	✓						
	72	✓	✓	✓						

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	73	✓	✓	✓						
	74	✓	✓	✓						
	75	✓	✓	✓						
	76	✓	✓	✓						
	77	✓	✓	✓						
	78	✓	✓	✓						
	79	✓	✓	✓						
	80	✓	✓	✓						
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	85	✓	✓	✓						
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	87	✓	✓	✓						
	88	✓	✓	✓						
	89	✓	✓	✓						
	90	✓	✓	✓						
	91	✓	✓	✓						
	92	✓	✓	✓						
	93	✓	✓	✓						

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	(bruce near2 ircardo).in. or (verdan near2 marlon).in. or (somera near2 margaret anne).in. or (jago-on near2 rowenah).in. or (de belen near2 maria).in. or (palacol near2 ron).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/03 15:36
S2	17	(bruce near2 ricardo).in. or (verdan near2 marlon).in. or (somera near2 margaret).in. or (jago-on near2 rowenah).in. or (de belen near2 maria).in. or (palacol near2 ron).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/03 15:38
S7	3204	(plural or multiple or seperate) with (profile or attribute or parameters) with (memory)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:03
S8	3335	(hybrid or heterogenous) near3 memory	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:04
S9	112740	(hybrid or heterogenous or different) near3 memory	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:04
S10	619	S7 and S9	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:04
S11	15	S7 and S8	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:04
S12	15	S11 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:05
S13	10	("20020184579" | "20050090940" | "20060059314" | "20080183958" |	US-PGPUB; USPAT;	ADJ	OFF	2012/12/05 17:13

		"20090319722").PN.	USOCR; EPO; DERWENT; IBM_TDB			
S14	193506	(memory or device) near3 (parameter or attribute)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/05 17:36
S15	4741	(plural or multiple or seperate) with (profile or attribute or parameter) with (memory)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/05 17:36
S16	2473	S14 and S15	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/05 17:36
S17	20106	(parameter or attribute) with (flash or nand or nor)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/05 17:37
S18	204	S16 and S17	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/05 17:37
S19	181	S18 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:37
S20	10	S19 and (page near3 size)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/05 17:38
S21	28	("4309754" | "4633437" | "4683534" | "4716527" | "5113369" | "5369754" | "5423009" | "5537624" | "5537659" | "5594874" | "5761456" | "5768560" | "5778413" | "5911053" | "6016270" | "6101565" | "6202140" | "6235554" | "6298426" | "6381664" | "6442076" | "6472747" | "6605875" | "6618790" | "6657899" | "6658508" | "6721840" | "7146510").PN. OR ("8200879").URPN.	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/12/06 12:54
S25	1	("6,430,663").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/12/11 15:23
S26	1	("5913215").PN.	US-PGPUB;	OR	OFF	2012/12/13

			USPAT; USOCR			10:22
S27	113091	(hybrid or heterogenous or different) near3 memory	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:03
S28	26	S27 and (DRAM same NAND same NOR same battery)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:03
S29	13	S28 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:03
S30	299	partial page program$4	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:48
S31	192	S27 and S30	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:48
S32	13	S29 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:48
S33	165	S31 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:48
S34	53823	(short$3 or shorten$3 or truncat$3) near3 (burst or transmission)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:50
S35	0	S33 and S34	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 11:50
S36	0	S30 and S34	US-PGPUB; USPAT; USOCR; EPO;	ADJ	OFF	2012/12/13 11:50

			DERWENT; IBM_TDB			
S37	20	S30 and burst	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 12:26
S38	14	S37 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 12:26
S39	92	partial page with (size or attribute)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 12:29
S40	6	S33 and S39	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 12:29
S41	198032	(profile or attribute or parameter) with (memory)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/13 12:32
S42	54	S33 and S41	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2012/12/13 12:32
S43	1	("5860107").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/12/13 13:20
S44	11735	(short$3 or shorten$3 or truncat$3) near3 (burst)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 15:18
S45	141	((multiple or plural or series) near3 (burst)) with (remaining or remainder or additional)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 15:19
S46	26	S44 and S45	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 15:20
S47	24	S46 and @ad<"20100904"	US-PGPUB;	ADJ	OFF	2012/12/13

			USPAT; USOCR; EPO; DERWENT; IBM_TDB			15:20
S48	135	S45 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 15:29
S49	1	("20060184723").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/12/13 17:13
S50	110530	(writ$3 or program$4) near3 block	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:33
S51	6832	(711/103).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/12/13 19:34
S52	3586	S50 and S51	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:34
S53	19	(writ$3 or program$4) near3 multiple blocks with (instruction or command)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:45
S54	299	(writ$3 or program$4) near3 multiple blocks	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:52
S55	44	S51 and S54	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:52
S57	37	S55 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/13 19:52
S58	285682	(flash or memory) near3 controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:50
S59	6008	(flash or memory) near3 interface with	US-PGPUB;	ADJ	OFF	2012/12/14

		(bus near3 (controller or master))	USPAT; USOCR; EPO; DERWENT; IBM_TDB			12:51
S60	5308	S58 and S59	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:51
S61	10796	fifo with input with output	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:52
S62	101	S60 and S61	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:52
S63	4117	fifo with (slots or entries)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:53
S64	4	S62 and S63	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 12:53
S65	99	S62 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 13:00
S66	113091	(hybrid or heterogenous or different) near3 memory	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 13:15
S67	790	S60 and S66	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 13:15
S68	18560	(fifo or queue) with input with output	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 13:16
S69	42	S67 and S68	US-PGPUB;	ADJ	OFF	2012/12/14

			USPAT; USOCR; EPO; DERWENT; IBM_TDB			13:16
S70	41	S69 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 13:16
S71	134	(acknowledg$3 or acknoweledgement or ack) with (bus near3 (controller or master)) with CPU	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:13
S72	5308	S58 and S59	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:13
S73	10	S59 and S71	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:14
S74	10	S73 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:14
S75	477	(status or complet$3) with (bus near3 (controller or master)) with CPU	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:21
S76	43	S71 and S75	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:21
S77	43	S76 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:21
S78	58	(acknowledg$3 or acknoweledgement or ack) with (memory near3 (controller)) with CPU	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:24
S79	57	S78 and @ad<"20100904"	US-PGPUB;	ADJ	OFF	2012/12/14

			USPAT; USOCR; EPO; DERWENT; IBM_TDB			15:25
S80	1016	(status or complet$3 or error) with (memory near3 (controller)) with CPU	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:25
S81	11	S79 and S80	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/12/14 15:25
S82	12083	(short$3 or shorten$3 or truncat$3) near3 (burst)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2013/05/06 16:15
S83	143	((multiple or plural or series) near3 (burst)) with (remaining or remainder or additional)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2013/05/06 16:15
S84	26	S82 and S83	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2013/05/06 16:15
S85	24	S84 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2013/05/06 16:15
S86	1	("8200879").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/05/06 16:18
S87	203091	(memory or device) near3 (parameter or attribute)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2013/05/06 17:45
S88	5067	(plural or multiple or seperate) with (profile or attribute or parameter) with (memory)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2013/05/06 17:45
S89	2613	S87 and S88	US-PGPUB; USPAT; USOCR; EPO;	ADJ	ON	2013/05/06 17:45

			DERWENT; IBM_TDB			
S90	21098	(parameter or attribute) with (flash or nand or nor)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2013/05/06 17:45
S91	222	S89 and S90	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2013/05/06 17:45
S92	185	S91 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2013/05/06 17:45
S95	3	(("7013376") or ("20070143569") or ("5627987")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/05/08 13:24
S96	226660	(memory or device) near3 (parameter or attribute)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2014/03/07 18:12
S97	5687	(plural or multiple or seperate) with (profile or attribute or parameter) with (memory)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2014/03/07 18:12
S98	2903	S96 and S97	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2014/03/07 18:12
S99	23258	(parameter or attribute) with (flash or nand or nor)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2014/03/07 18:12
S100	254	S98 and S99	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2014/03/07 18:12
S101	191	S100 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2014/03/07 18:12
S102	1227	(g06f13/1694 or g06f2212/7207 or	US-PGPUB;	ADJ	OFF	2014/03/07

		g06f2213/16 or g06f2213/1602).cpc.	USPAT; USOCR; EPO; DERWENT; IBM_TDB			18:18
S103	43	S97 and S102	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2014/03/07 18:18
S104	34	S103 and @ad<"20100904"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2014/03/07 18:18
S105	188	("20020073324" | "20020141244" | "20030182576" | "20030204675" | "20030223585" | "20040128553" | "20070019573" | "20070083680" | "20070130439" | "20070174493" | "20070195957" | "20090094411" | "4752871" | "5222046" | "5297148" | "5341339" | "5371709" | "5379401" | "5388083" | "5396468" | "5406529" | "5432748" | "5448577" | "5459850" | "5479638" | "5485595" | "5488711" | "5500826" | "5509134" | "5513138" | "5524231" | "5530828" | "5535328" | "5535356" | "5542082" | "5548741" | "5559956" | "5568423" | "5568439" | "5572466" | "5594883" | "5602987" | "5603001" | "5606529" | "5606532" | "5619470" | "5627783" | "5640349" | "5644784" | "5737742" | "5802554" | "5819307" | "5822251" | "5875351" | "5881264" | "5918033" | "5943421" | "6000006" | "6215875" | "6230269" | "6298071" | "6363441" | "6363444" | "6404772" | "6526506" | "6529416" | "6557095" | "6857076" | "6901499" | "6970446" | "6980795" | "7103684" | "7194766" | "7283629" | "7305548" | "7372962" | "7500063" | "7620748" | "7660941" | "7716389" | "7743202" | "7765359" | "7934052").PN.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2014/03/08 13:29

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Attn: Stephen R. Uriarte
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Courtesy Reminder for
Application Serial No: 12/876,113

Attorney Docket No: 6005.042
Customer Number: 64180
Date of Electronic Notification: 03/13/2014

This is a courtesy reminder that new correspondence is available for this application. If you have not done so already, please review the correspondence. The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

An email notification regarding the correspondence was sent to the following email address(es) associated with your customer number:

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Request for Continued Examination (RCE) Transmittal

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

   a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

      i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

      ii. ☐ Other _____

   b. ☑ Enclosed

      i. ☑ Amendment/Reply

      ii. ☐ Affidavit(s)/ Declaration(s)

      iii. ☐ Information Disclosure Statement (IDS)

      iv. ☐ Other _____

2. Miscellaneous

   a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

   b. ☐ Other _____

3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

   a. ☐ The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Deposit Account No. _____.

      i. ☐ RCE fee required under 37 CFR 1.17(e)

      ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)

      iii. ☐ Other _____

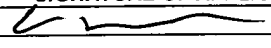
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   b. ☐ Check in the amount of $ _____ enclosed

   c. ☑ Payment by credit card (Form PTO-2038 enclosed)

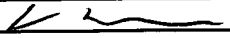
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature		Date	13 June 2014
Name (Print/Type)	Arnold de Guzman	Registration No.	39,955

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature			
Name (Print/Type)	Arnold de Guzman	Date	13 June 2014

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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Application Number	12/876,113
Filing Date	September 4, 2010
First Named Inventor	Ricardo H. Bruce
Art Unit	2187
Examiner Name	Jared Ian Rutz
Attorney Docket Number	6005.042

Total Number of Pages in This Submission: 36

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
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  - ☐ Affidavits/declaration(s)
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- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
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return receipt postcard; Amendment (33 pages); signed/dated PTO-2038 authorizing payment of $1700 (1 page); RCE (1 page)

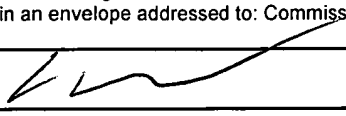
Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name			
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Date	13 June 2014	Reg. No.	39,955

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Ricardo H. Bruce, et al.	Confirmation No.: 1607
	Examiner: Jared Ian Rutz
Serial No.: 12/876,113	Ph: 571-272-5535
Filing Date: Sept. 4, 2010	Art Unit: 2187
Title: Multi-Profile Memory Controller For Computing Devices	Atty. Docket No.: 6005.042

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RESPONSE TO FINAL OFFICE ACTION AND AMENDMENT

Dear Sir:

The following is in response to the final office action mailed on 13 March 2014. An RCE is being filed herewith.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 27 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising:

addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile, wherein said second memory location is in a second memory device in the memory store, wherein a memory read transaction or a memory write transaction is performed on at least one of the first memory location or second memory location, wherein data is transferred to the first memory location or second memory location for a memory write transaction, wherein data is transferred from the first memory location or second memory location for a memory read transaction;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;

wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location;

wherein the memory store is coupled by at least one memory bus to a controller, and wherein the controller performs the memory transactions on the memory store;

wherein the first device profile and second device profile are each stored in the memory store; and

using attributes from said first and second device profiles.

2. (original) The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device.

3. (original) The method of claim 1, wherein said difference between said first and second device profiles includes different attributes; and said addressing said first memory location is made in response to a first memory transaction request; and

further including addressing said second memory location.

4. (original) The method of claim 1, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes.

5. (original) The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

6. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute values.

7. (original) The method of claim 5, wherein said different attribute qualifiers include different attribute types.

8. (original) The method of claim 5, wherein said shared attributes include a memory device type attribute.

9. (original) The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

10. (original) The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

11. (original) The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

12. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

13. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of attributes that differs in value from a second page size attribute from said second set of attributes.

14. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes.

15. (original) The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device, and said second memory device interface attribute corresponds to a DRAM device interface.

16. (original) The method of claim 2, wherein said using attributes from said first and second device profile further includes using a first partial page size attribute from said first set of attributes that differs in value from a second partial page size attribute from said second set of attributes.

17. (original) The method of claim 16:

said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute; and

further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute.

18. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

19. (original) The method of claim 8, wherein said first memory device type attribute corresponds to a NAND flash memory device and said second memory device type attribute corresponds to a NOR flash memory device.

20. (original) The method of claim 2, further including:

using an address corresponding to a memory location from said first memory device and transferring a first data set, and

using an address corresponding to a memory location from said second memory device and transferring a second data set.

21. (original) The method of claim 20, wherein:

said first set of attributes includes a first page size attribute, and said first data set includes a first data set size; and

if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size.

22. (original) The method of claim 20, wherein:

said second set of attributes includes a second page size attribute, and said second data set includes a second data set size; and

if said second data set size is greater than said second page size attribute, said transferring said second data set includes:

performing a set of write operations on said second memory device that includes using a second transfer size equal to said second page size attribute until a remaining

portion of said second data set that has not yet been written to said second device is less than said second page size attribute, and

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

23. (previously presented) The method of claim 20, wherein:

said first set of attributes includes a page size attribute and a block size attribute;

said first data set includes a first data set size;

if said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes:

performing a set of write operations on said first memory device that includes using a second transfer size equal to said page size attribute until a remaining portion of said first data set that has not yet been written to said first device is less than said page size attribute,

using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

24. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes:

performing respective write operations on said first and second memory devices by at least using a transfer size at least equal to a partial page size attribute from said first set of attributes and performing at least one write operation on said second memory device by at least using a transfer size at least equal to a partial page size attribute value from said second set of attributes; and

said attribute difference includes different attribute values of said first and second partial page size attributes.

25. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size attribute of said first memory device.

26. (original) The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a block size attribute value that corresponds to a block size attribute of said first memory device.

27. (original) The method of claim 26, wherein said using attributes from said first and second device profile

further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

28. (original) The method of claim 2, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a multiple of said block size attribute value.

29. (currently amended) A non-transitory computer readable medium comprising computer executable instructions adapted to cause a method of performing memory transactions on a first memory location and a second memory location, said method comprising:

addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile, wherein said second memory location is in a second memory device in the memory store;

said first device profile representing a first set of attributes of said first memory device, and said second device profile representing a second set of attributes of said second memory device, and a difference exists between said first and second device profiles;

wherein each attribute in the first set of attributes and second set of attributes is associated with a

respective attribute qualifier that qualifies a respective memory location;

wherein the memory store is coupled by at least one memory bus to a controller, and wherein the controller performs the memory transactions on the memory store;

wherein the first device profile and second device profile are each stored in the memory store; and

using attributes from said first and second device profiles.

30. (original) The computer readable medium of claim 29, wherein:

said first memory location is part of a memory space associated with a first memory device;

said second memory location is part of a memory space associated with a second memory device; and

said first and second memory devices comprise at least a portion of a memory store.

31. (previously presented) The computer readable medium of claim 29, wherein at least one attribute of said attributes includes a block size and said difference includes a block size value of a first memory device and a block size value of a second memory device.

32. (previously presented) The computer readable medium of claim 30, wherein at least one attribute of said

attributes includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

33. (original) The computer readable medium of claim 29, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

34. (original) The computer readable medium of claim 29, wherein said difference between said first and second device profiles includes different attributes.

35. (previously presented) The computer readable medium of claim 29, wherein said addressing further includes:

said first and second device profiles having at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

36. (original) The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

37. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values.

38. (original) The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute types.

39. (original) The computer readable medium of claim 36, wherein said shared attributes include a memory device type attribute.

40. (original) The computer readable medium of claim 36, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

41. (original) The computer readable medium of claim 36, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

42. (original) The computer readable medium of claim 36, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

43. (original) The computer readable medium of claim 36, wherein said shared attributes are memory device type attributes.

44. (original) The computer readable medium of claim 43, wherein said memory device type attributes each correspond to a non-volatile memory device.

45. (currently amended) A memory controller for performing memory transactions, said memory controller comprising:

a means for addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile, wherein said second memory location is in a second memory device in the memory store;

wherein said means for addressing includes an interface controller means for processing memory transaction requests;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;

wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location;

wherein the memory store is coupled by at least one memory bus to the interface controller means, and wherein

the interface controller means performs the memory transactions on the memory store;

wherein the first device profile and second device profile are each stored in the memory store; and

said means for addressing uses attributes from said first and second device profiles.

46. (original) The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

47. (original) The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

48. (original) The memory controller of claim 46, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said use of said attributes from said first and second device profiles by said means for addressing includes using

said different attribute qualifiers for said shared attributes.

49. (original) The memory controller of claim 46, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device.

50. (previously presented) The memory controller of claim 45, wherein said means for addressing further includes a means for addressing said second memory location.

51. (original) The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

52. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values.

53. (original) The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types.

54. (original) The memory controller of claim 51, wherein said shared attributes include a memory device type attribute.

55. (original) The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

56. (original) The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

57. (original) The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

58. (original) The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device.

59. (currently amended) A memory controller comprising:

an interface controller coupled to a memory device interface and an IO device interface;

said interface controller disposed to perform a memory transaction by addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile, wherein said second memory location is in a second memory device in the memory store;

said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;

wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location;

wherein the memory store is coupled by at least one memory bus to the interface controller, and wherein the interface controller performs the memory transactions on the memory store;

wherein the first device profile and second device profile are each stored in the memory store; and

said addressing of said first memory location includes using said attributes from said first device profile.

60. (original) The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile.

61. (previously presented) The memory controller of claim 59, wherein said interface controller includes:

a main control device coupled to said memory device interface and to a data path;

a first memory bus controller coupled to said control device and said memory device interface; and

an IO bus controller coupled to said IO device interface and said control device.

62. (previously presented) The memory controller of claim 61, wherein said IO bus controller is disposed to respond to a memory transaction request by acknowledging said request and providing status to said main control device.

63. (original) The memory controller of claim 62, wherein said interface controller interprets command details associated with said memory transaction, coordinates the operation of said memory device interface, and manages the transfer of memory transaction data between said IO device interface and said memory device interface through a data path.

64. (previously presented) The memory controller of claim 59, further including a buffer comprising a FIFO and a data path that includes a plurality of queue slots, including a first set of queue slots that buffer data from said IO device interface to said memory device interface, a second set of queue slots that buffer data from said memory device interface to said IO device interface.

65. (original) The memory controller of claim 59, further including a data path that includes a buffer having a plurality of queue slots.

66. (original) The memory controller of claim 65, wherein said buffer is a FIFO and said data path includes a plurality of queue slots that buffer data from said IO device interface to said memory device interface.

67. (original) The memory controller of claim 66, further including another data path that includes a second buffer having a plurality of queue slots that buffer data from said memory device interface to said IO device interface.

68. (previously presented) The memory controller of claim 59, further including a second memory bus controller coupled to a main control device and said memory device interface.

69. (original) The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes.

70. (original) The memory controller of claim 59, wherein:

said first and second device profiles have at least one set of shared attributes, and said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes; and

said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes.

71. (original) The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

72. (original) The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute.

73. (original) The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values.

74. (original) The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values.

75. (original) The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type.

76. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values.

77. (original) The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types.

78. (original) The memory controller of claim 71, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

79. (original) The memory controller of claim 71, wherein said shared attributes include a page size attribute and

said different attribute qualifiers include different page size values.

80. (currently amended) An electronic storage device, comprising:

a memory controller disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile;

wherein the first memory location is in a first memory device in a memory store;

wherein the second memory location is in a second memory device in the memory store;

said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;

wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location;

wherein the memory store is coupled by at least one memory bus to the memory controller, and wherein the memory controller performs the memory transactions on the memory store;

wherein the first device profile and second device profile are each stored in the memory store; and

said memory controller using attributes from said first and second device profiles.

81. (original) The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes.

82. (original) The electronic storage device of claim 80, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device.

83. (previously presented) The electronic storage device of claim 80, said memory controller further disposed to:

perform a write operation on said first memory device, if a memory transaction request is associated with a write request;

perform a read operation on said first memory device, if said memory transaction request is associated with a read request; and

wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using

said second device profile in response to receiving a second memory transaction request.

84. (original) The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.

85. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values.

86. (original) The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute.

87. (original) The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types.

88. (original) The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said shared attributes.

89. (original) The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device.

90. (original) The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values.

91. (original) The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values.

92. (original) The electronic storage device of claim 84, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type.

93. (original) The electronic storage device of claim 80, wherein said memory controller is further adapted to:

use a first partial page size attribute by performing a write operation on said first memory device and using a transfer size at least equal to said partial page size attribute; and

use a second partial page size attribute by performing a write operation on said second memory device and using a transfer size at least equal to said second partial page size attribute.

94. (previously presented) The method of claim 1, wherein the first memory location and the second memory location are addressable memory locations.

95. (previously presented) The memory controller of claim 45, wherein the first memory location and the second memory location are addressable memory locations.

96. (previously presented) The memory controller of claim 59, wherein the first memory location and the second memory location are addressable memory locations.

97. (previously presented) The electronic device of claim 80, wherein the first memory location and the second memory location are addressable memory locations.

REMARKS/ARGUMENTS

Claim Rejections

35 USC 102

Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-97

Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-97 are rejected under 35 U.S.C. 102(e) as allegedly being anticipated by US 8,200,879 to Falik et al. ("Falik"). Claims 1, 45, 59, and 80 are independent claims. Applicants respectfully traverse this rejection.

Applicants respectfully disagree with this rejection, but to expedite allowance of the claims, Applicants amend independent claim 1 herein to recite the above-noted features. Support for the amendment in claim 1 is found in the filed application in, for example, Figures 1 and 2 and accompanying text, and paragraphs [0015], [0016], [0017], [0018], [0019], [0025], and [0029].

The Office equates the first device profile and second device profile of claim 1 with the structure tables (Falik: Figures 5A-5F) of various registers 12 (Falik: Figure 4A) in the flash interface controller 10 of Falik (Final Office Action: page 5).

However, Applicants respectfully argue that the structure tables in Figures 5A-5F of Falik are properties of registers 12, wherein the registers 12 are not disposed within memory devices in a memory store and the registers 12 of Falik are instead disposed within the flash interface controller 10. Thus, Falik discloses the structure tables

(of Figures 5A-5F) as stored into the controller 10 (Falik: Figure 4A) and not stored in the flash memory arrays 70. Therefore, Falik does not disclose and does not teach the "first device profile and second device profile are each stored in the memory store" as required in claim 1. Additionally, Falik does not disclose and does not teach "wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location" as required in claim 1.

Since Falik does not disclose and does not teach all the limitations of claim 1, claim 1 is not anticipated by the cited reference. Claim 1 is otherwise allowable.

Claims 2-14, 20, 21, 25, and 94 depend from allowable claim 1; as such, they are also allowable for at least the same reasons as claim 1.

The withdrawal of the rejections to claims 1-14, 20, 21, 25, and 94 is respectfully requested.

Independent claims 45, 59, and 80 recite at least some limitations similar to that as claim 1. Although claims 45, 59, and 80 are different, Applicants respectfully argue that in this case the above arguments regarding the patentability of claim 1 apply with equal force with respect to claims 45, 59, and 80. Since Falik does not disclose and does not teach all the limitations of claims 45, 59, and 80, claims 45, 59, and 80 are not anticipated

by the cited reference. Claims 45, 59, and 80 are otherwise allowable.

Claims 46-58 and 95 depend from allowable claim 45; as such, they are also allowable for at least the same reasons as claim 45.

Claims 60, 69-79, and 96 depend from allowable claim 59; as such, they are also allowable for at least the same reasons as claim 59.

Claims 81-92 and 97 depend from allowable claim 80; as such, they are also allowable for at least the same reasons as claim 80.

The withdrawal of the rejection to claims 45-60, 69-92, and 95-97 is respectfully requested.

Claims 15, 18, and 19

Claims 15, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 7,330,954 to Nangle.

Claims 15, 18, and 19 depend from allowable claim 1; as such, they are also allowable for at least the same reasons as claim 1.

The withdrawal of the rejection of claims 15, 18, and 19 is respectfully requested.

Claims 16, 17, 22-24, and 93

Claims 16, 17, 22-24, and 93 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 2006/0184723 to Sinclair.

Claims 16, 17, and 22-24 depend from allowable claim 1; as such, they are also allowable for at least the same reasons as claim 1.

Claim 93 depends from allowable claim 80; as such, claim 93 is also allowable for at least the same reasons as claim 1.

The withdrawal of the rejection of claims 16, 17, 22-24, and 93 is respectfully requested.

Claims 26-28

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 6961,805 to Lakhani et al.

Claims 26-28 depend from allowable claim 1; as such, they are also allowable for at least the same reasons as claim 1.

The withdrawal of the rejection of claims 26-28 is respectfully requested.

Claims 29-44

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 5,913,215 to Rubinstein.

The Office admits that Falik does not expressly teach that the methods may be implemented using a computer readable medium comprising computer executable instructions. In order to supply the missing limitations, the Office combines Falik with Rubinstein. The Office argues it would have been obvious to one of ordinary skill in the art to implement the method of Falik using a

computer readable medium comprising computer executable instructions (Office Action: page 44). The Applicants respectfully disagree with the assertions of the Office.

Independent claim 29 recite at least some limitations similar to that as claim 1. Although claim 29 is different, Applicants respectfully argue that in this case the above arguments regarding the patentability of claim 1 apply with equal force with respect to claim 29.

Since Falik and Rubinstein, considered individually or in combination, do not disclose and does not teach all the limitations of claim 29, claim 29 is not rendered obvious in view the cited references. Claim 29 is otherwise allowable.

Claims 30-44 depend from allowable claim 29; as such, they are also allowable for at least the same reasons as claim 29.

The withdrawal of the rejection of claims 29-44 is respectfully requested.

Claims 61 and 64-68

Claims 61 and 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of US 2001/0010066 to Chin et al.

Claims 61 and 64-68 depend from allowable claim 59; as such, they are also allowable for at least the same reasons a claim 59.

The withdrawal of the rejection of claims 61 and 64-68 is respectfully requested.

Claims 62 and 63

Claims 61 and 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik in view of Chin as applied to claim 61 above, and further in view of US 2007/0174506 to Tsuruta.

Claims 62 and 63 depend from allowable claim 59; as such, they are also allowable for at least the same reasons a claim 59.

The withdrawal of the rejection of claims 62 and 63 is respectfully requested.

Applicant also maintain the arguments presented in the amendment filed on 15 October 2013 for this application.

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, the Applicants are not conceding in this application that previously pending claims are unpatentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application.

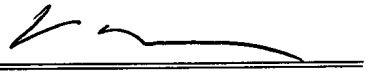
Conclusion

Claims 1-97 herein are allowable, and a timely Notice of Allowance is respectfully requested.

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (805) 569-1600.

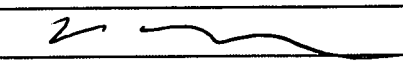
Date: June 13, 2014

Respectfully submitted,



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CERTIFICATE OF TRANSMISSION OR MAILING 37 C.F.R. 1.8			
I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office in accordance with 37 C.F.R. § 1.6(d), or is being transmitted via the Office electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4), or is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below:			
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/876,113	09/04/2010	Ricardo H. BRUCE	6005.042	1607

64180 7590 07/11/2014

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EXAMINER	
RUTZ, JARED IAN	

ART UNIT	PAPER NUMBER
2187	

NOTIFICATION DATE	DELIVERY MODE
07/11/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

stephen@uriartelaw.com
labid@uriartelaw.com
arnold@uriartelaw.com

Office Action Summary	Application No. 12/876,113	Applicant(s) BRUCE ET AL.	
	Examiner JARED RUTZ	Art Unit 2187	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/19/2014*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-97* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-97* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

2. Claims 1-97, as amended on 6/19/2014, are pending in the instant application. Applicant' arguments submitted 6/19/2014 have been carefully and fully considered, but are not found persuasive. The instant Office action is made **FINAL**.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/19/2014 has been entered.

4. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1-14, 20, 21, 25, 45-60, 69-92, and 94-97** are rejected under 35 U.S.C. 102(e) as being anticipated by Falik et al. (US 8,200,879).

Claim 1 is taught by Falik as:

A method of performing memory transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising: addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Wherein said second memory location is in a second memory device in the memory store. Column 6 lines 11-16 shows that the different parameters correspond to different memory arrays. Accordingly, the address corresponding to a different section may be in a second memory device.

Wherein a memory read transaction or a memory write transaction is performed on at least one of the first memory location or second memory location, wherein data is transferred to the first memory location of second memory location for a memory write transaction, wherein data is transferred from the first memory location or second memory location for a memory read

transaction. Column 22 lines 16-20 shows that reading of data from memory and modifying contents of the memory (i.e. erasing and programming) are carried out as transactions, initiated by appropriate commands and affected by the contents of the specified registers. Column 16 line 53 through column 17 line 24 further discusses the use of addresses to read and write data from the memory. Column 6 is an illustration of reads and writes to different addresses in different sections of the memory.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

Wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location. Column 20 line 49 through column 21 line 15 shows that the section properties register stores values representing the section of the flash device, and that there is a section properties register for each section of the flash device.

Wherein the memory store is coupled by at least one memory bus to a controller, and wherein the controller performs the memory transactions on the

memory store. Figure 1 shows that main die interface controller connects to the flash die via bus 90, as discussed at column 10 lines 5-15. Column 27 lines 8-32 shows that the MD sends commands to the FD.

Wherein the first device profile and second device profile are each stored in the memory store. Column 18 lines 53-64 show that the control, status and capabilities registers 12 and 112 are located on the flash device, and can be kept in the flash device's own memory.

And using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 2 is taught by Falik as:

The method of claim 1, wherein said first memory location is located in a first memory device, and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 3 is taught by Falik as:

The method of claim 1, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

And said addressing said first memory location is made in response to a first memory transaction request. Column 18 lines 24-34 shows that applications on the main die 100 issue read and program commands.

And further including addressing said second memory location. Figure 6 shows that both sections can be addressed.

Claim 4 is taught by Falik as:

The method of claim 1, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles further includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 5 is taught by Falik as:

The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second

device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 6 is taught by Falik as:

The method of claim 5, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 7 is taught by Falik as:

The method of claim 5, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 8 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a memory device type attribute. Column 20 lines 30-36 shows that the registers can indicate if the device is self timed type flash memory or not.

Claim 9 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 10 is taught by Falik as:

The method of claim 5, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 11 is taught by Falik as:

The method of claim 5, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 12 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 13 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first page size attribute from said first set of attributes that differs in value from a second page size attribute from said second set of attributes. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 14 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes using a first memory device interface attribute from said first set of attributes that differs from a second memory device interface attribute from said second set of attributes. Column 19 lines 56-59

shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 20 is taught by Falik as:

The method of claim 2, further including: using an address corresponding to a memory location from said first memory device and transferring a first data set. Column 16 lines 53-62 shows that an address and data are sent for a programming operation.

And using an address corresponding to a memory location from said second memory device and transferring a second data set. Column 14 lines 51-65 show that the standard address space is mapped to the logical sections into which the arrays are grouped, showing that the second memory device is accessed using an address corresponding to the second memory device.

Claim 21 is taught by Falik as:

The method of claim 20, wherein: said first set of attributes includes a first page size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

And said first data set includes a first data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

And if said first data set size is at most equal to said first page size attribute, said transferring said first data includes using a first transfer size equal to said first data set size. Column 27 lines 9-24 shows that when the number of bytes to be transferred to the FD have been transferred, the transfer process ends by setting the bus to a HiZ state.

Claim 25 is taught by Falik as:

The method of claim 1, wherein said using attributes from said first and second device profile further includes performing a write operation that uses a transfer size equal to a page size attribute value that corresponds to a page size attribute of said first memory device. As discussed at column 27 lines 33-60, the program buffer corresponds to the batch size, which is the amount of data which can be programmed into the flash array at once.

Claim 45 is taught by Falik as:

A memory controller for performing memory transactions, said memory controller comprising: a means for addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is

addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Wherein said means for addressing includes an interface controller means for processing memory transaction requests. Figure 4B, flash bus transactions state machine 116.

Wherein said second memory location is in a second memory device in the memory store Column 6 lines 11-16 shows that the different parameters correspond to different memory arrays. Accordingly, the address corresponding to a different section may be in a second memory device.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

Wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location. Column 20 line 49 through column 21 line 15 shows that the section properties register stores values representing the section of the flash device, and that there is a section properties register for each section of the flash device.

Wherein the memory store is coupled by at least one memory bus to the interface controller means, and wherein the interface controller means performs the memory transactions on the memory store. Figure 1 shows that main die interface controller connects to the flash die via bus 90, as discussed at column 10 lines 5-15. Column 27 lines 8-32 shows that the MD sends commands to the FD.

Wherein the first device profile and second device profile are each stored in the memory store. Column 18 lines 53-64 show that the control, status and capabilities registers 12 and 112 are located on the flash device, and can be kept in the flash device's own memory.

And said means for addressing uses attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 46 is taught by Falik as:

The memory controller of claim 45, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 47 is taught by Falik as:

The memory controller of claim 46, wherein said using attributes from said first and second device profile further includes using a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 48 is taught by Falik as:

The memory controller of claim 46, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said use of said attributes from said first and second device profiles by said means for addressing includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 49 is taught by Falik as:

The memory controller of claim 46, wherein said at least one attribute includes a block size and said difference includes a block size value of said first memory device and a block size value of said second memory device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 50 is taught by Falik as:

The memory controller of claim 45, wherein said means for addressing further includes a means for addressing said second memory location. Figure 6 shows that both sections can be addressed.

Claim 51 is taught by Falik as:

The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths

Support indicates the logical bus width values that a particular flash device supports.

Claim 52 is taught by Falik as:

The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 53 is taught by Falik as:

The memory controller of claim 51, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 54 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 55 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 56 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 57 is taught by Falik as:

The memory controller of claim 51, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 58 is taught by Falik as:

The memory controller of claim 57, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

Claim 59 is taught by Falik as:

A memory controller comprising: an interface controller coupled to a memory device interface and an IO device interface. Figure 4B shows interface controller 110 connected to bus 90 and internal bus 140.

Said interface controller disposed to perform a memory transaction by addressing a first memory location in a first memory device in a memory store, said first memory location and a second memory location respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Wherein said second memory location is in a second memory device in the memory store. Column 6 lines 11-16 shows that the different parameters

correspond to different memory arrays. Accordingly, the address corresponding to a different section may be in a second memory device.

Said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

Wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location. Column 20 line 49 through column 21 line 15 shows that the section properties register stores values representing the section of the flash device, and that there is a section properties register for each section of the flash device.

Wherein the memory store is coupled by at least one memory bus to the interface controller, and wherein the interface controller performs the memory transactions on the memory store. Figure 1 shows that main die interface controller connects to the flash die via bus 90, as discussed at column 10 lines 5-15. Column 27 lines 8-32 shows that the MD sends commands to the FD.

Wherein the first device profile and second device profile are each stored in the memory store. Column 18 lines 53-64 show that the control, status and

capabilities registers 12 and 112 are located on the flash device, and can be kept in the flash device's own memory.

And said addressing of said first memory location includes using said attributes from said first device profile. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 60 is taught by Falik as:

The memory controller of claim 59, wherein said interface controller is further disposed to perform another memory transaction by addressing said second memory location by at least using said attributes from said second device profile. Figure 6 shows that both sections can be addressed.

Claim 69 is taught by Falik as:

The memory controller of claim 59, wherein said difference between said first and second device profiles includes different attributes. Column 20 lines 44-48 shows that when different memory technologies are used, such as SRAM, other properties relating to the different memory technologies will be reported.

Claim 70 is taught by Falik as:

The memory controller of claim 59, wherein: said first and second device profiles have at least one set of shared attributes. Column 14 lines 4-20 shows

that the groups have the same types of characteristics, including parameters and structure.

And said difference between said first and second device profiles includes different attribute qualifiers for said set of shared attributes. Column 14 lines 40-50 show that arrays having different structure are separated into different groups.

And said using said attributes from said first and second device profiles includes using said different attribute qualifiers for said shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 71 is taught by Falik as:

The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 72 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 73 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a block size and said difference includes block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 74 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes includes a page size and said difference includes page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 75 is taught by Falik as:

The memory controller of claim 71, wherein said difference includes different attribute values for said shared attributes, said shared attributes including any one of a partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 76 is taught by Falik as:

The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 77 is taught by Falik as:

The memory controller of claim 71, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 78 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 79 is taught by Falik as:

The memory controller of claim 71, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 80 is taught by Falik as:

An electronic storage device, comprising: a memory controller disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile. Column 25 lines 15-22 shows that a memory location is addressed. Column 18 lines 53-64 shows that control, status and capabilities registers 12 are used to store information required for appropriate functioning of the interface. Column 14 lines 40-45 shows that arrays are grouped into sections having identical structure. Column 14 lines 51-60 shows that the groups are mapped into the standard address space. Column 15 line 63 through column 16 line 19 shows that characteristics used to program the memory sections are stored in a section capabilities register.

Wherein the first memory location is in a first memory device in a memory store; wherein the second memory location is in a second memory device in the

memory store. Column 6 lines 11-16 shows that the different parameters correspond to different memory arrays. Accordingly, the first location may be in a different memory device than the second location.

Said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles. Column 20 line 49 through column 21 line 15 discusses the information stored in the section properties register. Column 14 lines 40-45 shows that arrays in different groups have different structure, and therefore there are differences between the device profiles.

Wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location. Column 20 line 49 through column 21 line 15 shows that the section properties register stores values representing the section of the flash device, and that there is a section properties register for each section of the flash device.

Wherein the memory store is coupled by at least one memory bus to the memory controller, and wherein the memory controller performs the memory transactions on the memory store. Figure 1 shows that main die interface controller connects to the flash die via bus 90, as discussed at column 10 lines 5-15. Column 27 lines 8-32 shows that the MD sends commands to the FD.

Wherein the first device profile and second device profile are each stored in the memory store. Column 18 lines 53-64 show that the control, status and capabilities registers 12 and 112 are located on the flash device, and can be kept in the flash device's own memory.

And said memory controller using attributes from said first and second device profiles. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used.

Claim 81 is taught by Falik as:

The electronic storage device of claim 80, wherein said memory controller is further disposed to use a first block size attribute from said first set of attributes that differs in attribute value from a second block size attribute from said second set of attributes. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command. Column 9 lines 5-18 shows that the interface performs appropriate requests for erasure.

Claim 82 is taught by Falik as:

The electronic storage device of claim 80, wherein said first memory location is located in a first memory device and said second memory location is located in a second memory device. Column 14 lines 51-60 and figure 3 shows that different addresses correspond to different memory device groups.

Claim 83 is taught by Falik as:

The electronic storage device of claim 80, said memory controller further disposed to: perform a write operation on said first memory device, if a memory transaction request is associated with a write request. Column 16 lines 53-64 shows that write transactions may be performed.

Perform a read operation on said first memory device, if said memory transaction request is associated with a read request. Column 16 lines 53-64 shows that read transactions may be performed.

And wherein said using said first and second device profiles includes using said first device profile in response to a first memory transaction request, and using said second device profile in response to receiving a second memory transaction request. Column 19 line 4 through column 22 line 15 discuss how the different attributes are used for accesses to the groups of memory arrays.

Claim 84 is taught by Falik as:

The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles. Column 19 lines 56-59 shows that the Bus Widths Support indicates the logical bus width values that a particular flash device supports.

Claim 85 is taught by Falik as:

The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values. Column 19 lines 56-59 shows that the Bus Widths Support stores bits which indicate the logical bus width values that a particular flash device supports.

Claim 86 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a memory device type attribute. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 87 is taught by Falik as:

The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute types. Column 19 line 66 through column 20 line 6 shows that Read While Program indicates if the FD is capable of supporting simultaneous read and program operations.

Claim 88 is taught by Falik as:

The electronic storage device of claim 87, wherein said memory controller using different attributes includes using said different attribute qualifiers for said

shared attributes. Column 19 lines 37-40 shows that the Clock Frequency indicates the frequency of the clock signal used to access a memory device.

Claim 89 is taught by Falik as:

The electronic storage device of claim 87, wherein said memory device type attributes each correspond to a non-volatile memory device. Figure 4A shows that flash memory arrays can include a plurality of nonvolatile memories.

Claim 90 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a block size attribute, and said different attribute qualifiers include different block size values. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 91 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes include a page size attribute and said different attribute qualifiers include different page size values. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash

device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

Claim 92 is taught by Falik as:

The electronic storage device of claim 84, wherein said shared attributes includes any one of the following memory device attributes: partial page size, page size, block size, memory protocol, and memory device type. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Claim 94 is taught by Falik as:

The method of claim 1, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 95 is taught by Falik as:

The memory controller of claim 45, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address

into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 96 is taught by Falik as:

The memory controller of claim 59, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim 97 is taught by Falik as:

The electronic device of claim 80, wherein the first memory location and the second memory location are addressable memory locations. Column 13 lines 45-60 shows that the standard address space is used to map an address into the internal memory addresses of the particular flash memory device, which may include multiple arrays. As noted at column 6 lines 11-19, the different arrays may have different parameters.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 15, 18, and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Nangle (US 7,330,954).

Claim 15 is taught by Falik as:

The method of claim 14, where said first memory device interface attribute corresponds to a flash memory device. Column 21 lines 7-10 shows that the information can correspond to a flash device FD.

Although Falik column 21 lines 7-10 shows that other memory technologies such as SRAM may be used, it does not expressly teach that the second memory device attribute corresponds to a DRAM device interface.

With respect to claim 15, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 lines 51-67 shows that the memory devices may be flash memory and DRAM.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include flash memory and DRAM in the system of Falik.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 15**.

Claim 18 is taught by Falik as shown supra with respect to claim 8.

Falik does not expressly teach that said first memory device type attribute corresponds to a volatile memory disposed to receive backup power from a portable power source.

With respect to claim 18, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 line 51 through column 5 line 4 shows that the memory devices may be volatile memory that have a battery backup.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a volatile memory disposed to receive backup power from a portable power source.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 18**.

Claim 19 is taught by Falik as shown supra with respect to claim 8.

Falik does not expressly teach that said first memory device type attribute corresponds to a NAND flash memory device and said second memory device type attribute corresponds to a NOR flash memory device.

With respect to claim 19, Nangle teaches a system including memories 130, 140, and 150 having different physical characteristics, see column 2 lines 59-67. Column 4 lines 51-65 shows that the memory devices may be NAND or NOR type flash memories.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a volatile memory disposed to receive backup power from a portable power source.

The motivation for doing so would have been to allow the storage of data in a memory device having characteristics appropriate to the data being stored, Nangle column 5 lines 27-56.

Therefore, it would have been obvious to combine Nangle with Falik to obtain the invention as recited in **claim 19**.

9. **Claims 16, 17, 22-24, and 93** are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al. (US 8,200,879) in view of Sinclair et al. (US 2006/0184723).

Claim 16 if taught by Falik as shown supra with respect to claim 2.

Although Falik teaches that the width of the array is the minimum programming size of the array at column 20 lines 62-65, and that the width of the array is stored at column 20 lines 49-52, Falik does not expressly teach that a first and second partial page size attribute is stored and used.

With respect to claim 16, Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claims 16 and 17**.

Claim 17 is taught by Falik and Sinclair as:

The method of claim 16: said using a first partial page size attribute includes performing a write operation on said first memory device by at least using a transfer size at least equal to a value of said first partial page size attribute. Sinclair paragraph 0168 shows that in a flash memory that supports

partial page programming, when sufficient data is transferred to the buffer, it is programmed to the page. Falik column 14 lines 51-60 and figure 3 shows that the first memory device group can be accessed.

And further including using said second partial page size attribute by at least performing a write operation on said second memory device that includes using a transfer size at least equal to a value of said second partial page size attribute. Sinclair paragraph 0168 shows that in a flash memory that supports partial page programming, when sufficient data is transferred to the buffer, it is programmed to the page. Falik column 14 lines 51-60 and figure 3 shows that the second memory device group can be accessed.

Claim 22 is taught by Falik as:

The method of claim 20, wherein: said second set of attributes includes a second page size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device.

And said second data set includes a second data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

And if said second data set size is greater than said second page size attribute, said transferring said second data set includes: performing a set of

write operations on said second memory device that includes using a second transfer size equal to said second page size attribute. Column 16 lines 48-52 shows that program buffer 19 may be a double buffer, allowing the programming of one chunk of data while another chunk of data is received. As discussed at column 27 lines 33-60, the program buffer corresponds to the batch size, which is the amount of data which can be programmed into the flash array at once.

Falik does not expressly teach that the transaction is made using a transfer size equal to the page size until a remaining portion of said second data set that has not yet been written to said second device is less than said second page size attribute and using a last transfer size equal to said remaining portion if said remaining portion is less than said page size.

With respect to claim 22, Sinclair teaches Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times. As discussed in paragraph 0168, when the end of the data group is received in the buffer and it is smaller than a full page of data, a partial page programming operation may be performed.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 22**.

Claim 23 is taught by Falik as:

The method of claim 20, wherein: said first set of attributes includes a page size attribute and a block size attribute. Column 20 lines 62-65 shows that the minimum programming size is the width of the array. Column 20 lines 49-52 shows that the section properties register stores the structural properties of the section of the flash device. Column 13 line 61 through column 14 line 3 shows that width is a structural property of the flash device. Column 20 lines 60-67 shows that Page Size Block1 indicates the size of the minimal segment of a flash array erasable upon a single erase command.

Said first data set includes a first data set size. Column 27 lines 8-24 shows that the data to be sent comprises a number of bytes.

If said first data set has a first data set size greater than said page size attribute, said transferring of said first data set includes: performing a set of write operations on said first memory device that includes using a second transfer size equal to said page size attribute […]. Column 27 lines 14-24 shows that bytes of data are sent until all the bytes have been sent.

Falik does not expressly teach that the transaction is made using a transfer size equal to the page size until a remaining portion of said first data set that has not yet been written to said first device is less than said first page size attribute and using a last

transfer size equal to said remaining portion if said remaining portion is less than said page size.

With respect to claim 23, Sinclair teaches Sinclair teaches at paragraph 0161 that some flash memories allow partial page programming, which allows portions of a page to be programmed at different times. As discussed in paragraph 0168, when the end of the data group is received in the buffer and it is smaller than a full page of data, a partial page programming operation may be performed.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify Falik to record and use partial page size attributes for the first and second memory groups.

The motivation for doing so would have been to allow the storage space of a page in flash memory to be utilized more efficiently by storing multiple data items having a size smaller than the full page in a single page, Sinclair paragraph 163.

Therefore, it would have been obvious to combine Sinclair with Falik to obtain the invention as recited in **claim 23**.

Claim 24 is taught by Falik as shown supra with respect to claim 1, and further as:

> *The method of claim 1, wherein said using attributes from said first and second device profile further includes: performing respective write operations on said first and second memory devices by at least using a transfer size at least equal to a* […] *page size attribute from said first set of attributes.* Column 16