

Technical Article

PoP, SiP, MCM, MCP or SoC? Assessing the mobile/embedded design tradeoffs

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Multichip packages (MCPs) have long met the need to pack more performance and features into an increasingly small space. It seems natural to see the [extension](#) of the [memory](#) MCP to include ASICs such as [basebands](#) or [multimedia](#) processors. But here, we run into the difficulties of development and ownership/reduction costs.

How do we address these problems?

Today, a package-on-package (PoP) concept is becoming widely accepted. Combo memory (flash and RAM) products combining multiple [flash](#) NOR and NAND with a [RAM](#) in a single package are widely used in [cellphone](#) applications. These single-package solutions are the MCP, [system-in-package](#) (SiP) and [multichip module](#) (MCM).

The MCP in cellphone applications began by combining what is now considered to be relatively low-density combinations, such as an 8Mbit flash and 2Mbit SRAM.

As the memory requirements of the cellphone grew, the flash density increased with the NOR flash and the introduction of the NAND, and the SRAM was replaced by the pseudo SRAM (PSRAM).

Size, performance issues

The demand for more features in the ever-smaller form factor of cellphones contributes to the need for MCPs. However, developing solutions to enhance performance and keeping the small size pose additional challenges.

Size and performance are an issue when working with a [baseband chip set](#) or multimedia coprocessor in cellphones. In such instances, MCP memories with SDRAM and double data rate (DDR) interface are used.

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The basic concept of the **SoC** is to integrate more components into the same piece of silicon to reduce size and cost while enhancing performance. In the cellphone market where project life spans are short and costs are aggressive, however, SoC solutions have a limitation.

From the memory-configuration point of view, where a large amount of logic is required with various types of memories, mastering the different disciplines in design and technology can be a challenge that may affect the development time and flexibility required by the application.

From a silicon point of view, having the basic components separated yet manufactured in a different technology would address the problem. The memory and the **ASIC** are assembled in the same package. However, there are two main areas of concern: SiP's cost of production with respect to yield and SiP inflexibility.

SiP's cost of production with respect to yield—In developing MCP of any configuration, the final package and assembly yield is a product of all the MCP elements' yields. For example, let's consider that each component has a yield of 90 percent and the MCP is made of four dice. Its overall yield is 90 percent x 90 percent x 90 percent x 90 percent.

A low yield cannot be considered mass-producible to serve a very high-volume consumer market, where there is continuous pressure on price. Known good-die programs are normal practice when considering MCP configuration to keep yields at an acceptable level.

The memory and the baseband can contribute to about 25 percent of a cellphone's BOM, depending on the features and specifications. The SiP that combines memories with a baseband or co-processor will have a relatively high cost, and the complete SiP will be rejected if any of the components inside does not meet the spec.

SiP inflexibility

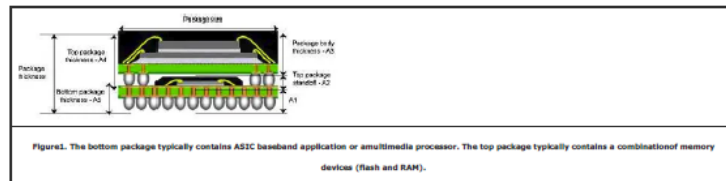
The introduction of SiP is also limited by the availability of all the components at the same time. And to achieve a competitive solution, all the components must be produced in the most cost-effective technology from the beginning.

This is further complicated by the fact that the development resources and time required are different between the **ASIC** and the memory. In many cases, these are produced by different companies.

This means that synchronizing on the availability is very difficult. Only a broad-range IC supplier can source most components internally and meet timing demands.

Once the SiP is developed and available to the cellphone manufacturer, changing any component inside the SiP for cost reduction (due to availability of new technology, for instance) could require re-qualifications of the complete SiP. This is a long and costly process.

The PoP concept separates the ASIC from the memory. The development and introduction of each component can take individual paths. The solution is achieved by assembling the two packages on top of each other. The top package's solder balls bond directly onto landing pads on the top surface of the bottom package (**Figure 1, below**).



The bottom package typically contains ASIC baseband application or multimedia processor. Memory modules for the bottom package are also available, allowing multiple stacks of memories, if required. The top package typically contains a combination of memory devices (flash and RAM).

The PoP solution provides greater PCB-space savings, compared with a two-package solution. The proximity of the two components means that performance can be optimized. Working with a memory interface that runs at 100MHz and above, special guidelines and techniques are used for the signals and power lines in the design of the packages to ensure signal integrity.

The package characteristics play a key role in the overall performance of the system. Design verification and simulation methodology that were once part of the system design are now used to develop the PoP.

Standardization

The PoP solution allows the manufacturer to independently source the bottom and top package from different suppliers. As with many new developments, there can be various proposals, as in this case for the physical size and the ball-out of the respective pieces.

Within the Jedec standard, multiple options for the packages are included with variations in physical size and the electrical ball-out. The choice of standard to be used is based on the availability of both the top and bottom package. The Jedec standard JC63 covers ball-outs and [bus](#) combinations, while the Jedec standard JC11 covers mechanical dimensions.

Physical dimensions

The package size governs the area used on the PCB, and the package thickness controls the profile, which is made up of A1+A2+A3 (Figure 1). The overall package height needs to be maintained while allowing for the top package standoff A2.

This dictates the space available for the bottom die and mould cap. The balls of the package are arranged in two rows around the perimeter. As seen in **Figure 2, below**, dimensions D and E provide the body size, and e and b define the ball pitch and ball diameter.



Reducing the ball size and pitch would make additional signals on the given parameters available and thus allow additional functionality. Finer ball size and pitch packages are in development and are included in the [JEDEC standards](#).

Manufacturability

There are two main concerns about using the PoP above the normal [BGAP package](#) in [SMT](#) line:

1. Pre- and post-reflow ball height that will dictate the standoff A2 in Figure 1 in the end;
2. Top and bottom warpage characteristics across the applications' temperature range and the reflow temperature profile.

In applications requiring a small form factor and high performance, the PoP provides a way for the components to follow an independent development path. Additionally, the two elements can be separated, giving flexibility greater than that achieved by an SIP or SoC solution.

The PoP solution minimizes the space requirement and increases memory flexibility for the system designer. In the manufacturing process, it allows for separate sourcing and testing of the typically complex memory system and logic device, simplifying assembly flow for high performance mobile multimedia products.

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