

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION**

BiTMICRO LLC,

Plaintiff,

v.

KIOXIA AMERICA, INC.
and KIOXIA CORPORATION,

Defendants.

Civil Action No.: 6:22-cv-00331-ADA

BiTMICRO LLC,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

Civil Action No.: 6:22-cv-00335-ADA

PLAINTIFF BITMICRO LLC'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

REDACTED

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Plaintiff BiTMICRO LLC (“BiTMICRO”) submits this responsive brief in support of its constructions, which are consistent with the plain language of the claims and the intrinsic record.

I. LEGAL STANDARD

As the Court is well-versed in the law governing the interpretation of patent claims, BiTMICRO dispenses with a recitation of that authority generally, and highlights two issues.

A. Indefiniteness

Definiteness is evaluated from the perspective of someone skilled in the art. *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 909 (2014). “One must bear in mind, moreover, that patents are ‘not addressed to lawyers, or even to the public generally,’ but rather to those skilled in the relevant art.” *Id.* (quoting *Carnegie Steel Co. v. Cambria Iron Co.*, 185 U.S. 403, 437 (1902)). “[T]he certainty which the law requires in patents is not greater than is reasonable, having regard to their subject-matter.” *Id.* at 910 (quoting *Minerals Separation, Ltd. v. Hyde*, 242 U.S. 261, 270 (1916)). Terms of degree are not “inherently indefinite,” and “absolute or mathematical precision is not required.” *One-E-Way, Inc. v. Int’l Trade Comm’n*, 859 F.3d 1059, 1068 (Fed. Cir. 2017) (quoting *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1370 (Fed. Cir. 2014)).

Proof of indefiniteness requires an accused infringer to show “by clear and convincing evidence that a skilled artisan could not discern the boundaries of the claim based on the claim language, the specification, and the prosecution history, as well as her knowledge of the relevant art area.” *Halliburton Energy Servs., Inc. v. M-I LLC*, 514 F.3d 1244, 1249-50 (Fed. Cir. 2008). Defendants cannot meet that burden because they have not even defined who a person of ordinary skill in the art (POSITA) would be for the patents on which they are asserting indefiniteness. Nor have they provided any expert testimony to support their indefiniteness arguments. The Court can and therefore should summarily deny all of those arguments. *See Williamson v. Google Inc.*, No. 15-cv-00966-BLF, 2017 WL 3232582, at *10 (N.D. Cal. July 27, 2017) (defendant could not meet its burden on indefiniteness without expert opinion supporting its assertion that POSITA would not understand claim term “best suited” based on examples in specification); *WesternGeco L.L.C. v. ION Geophysical Corp.*, 876 F. Supp. 2d. 857, 875 (S.D. Tex. 2012) (“Defendants’ unsupported

attorney argument fails to prove indefiniteness by clear and convincing evidence.”); *Cacace v. Meyer Mktg. (Macau Commercial Offshore) Co.*, 812 F. Supp. 2d 547, 561 (S.D.N.Y. 2011) (“[M]ere attorney argument is insufficient to establish invalidity based on indefiniteness.”).

B. Means-Plus-Function Limitations

“An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.” 35 U.S.C. § 112(f). Moreover, “[a] limitation has sufficient structure when it recites a claim term with a structural definition that is ***either provided in the specification or generally known in the art.***” *Apple Inc. v. Motorola, Inc.*, 757 F.3d 1286, 1298-99 (Fed. Cir. 2014) (emphasis added). In the context of computer-implemented inventions, “the ‘structure’ of computer software is understood through, for example, an outline of an algorithm, a flowchart, or a specific set of instructions or rules.” *Id.* “[A] challenge to a claim containing a means-plus-function limitation as lacking structural support requires a finding, by clear and convincing evidence, that the specification lacks disclosure of structure sufficient to be understood by one skilled in the art as being adequate to perform the recited function.” *Budde v. Harley-Davidson, Inc.*, 250 F.3d 1369, 1376–77 (Fed. Cir. 2001); *Intel Corp. v. VIA Techs., Inc.*, 319 F.3d 1357, 1366 (Fed. Cir. 2003). Defendants have not met that burden. *Intelligent Automation Design, LLC v. Zimmer Biomet CMF & Thoracic, LLC*, 799 F. App’x 847, 852 (Fed. Cir. 2020).

II. ’939 PATENT

The ’939 Patent relates to systems and methods for managing data in a computer or memory system when the system loses external power. ’939 Patent (Ex. 1),¹ Abstract. Specifically, the ’939 Patent describes a plurality of capacitors configured to supply power to the computer or memory system, activating those capacitors to supply power in the event of a loss of external power, and reconfiguring the data in the computer or memory system while that auxiliary power

¹ Unless otherwise noted, references herein to “Ex.” refer to exhibits attached to the supporting declaration of Richard Lin filed concurrently with this brief.

is supplied. *Id.* at 2:24-31. Using the claimed systems and methods of the '939 Patent, newly written and/or modified data can be stored (or flushed) from the volatile memory to the non-volatile memory in the event of a power loss, and/or enable the data to be erased automatically or manually—thus, preserving the security of the stored data. *Id.* at 2:32-42.

The '939 Patent explains that computing systems generally utilized volatile memory for main memory and cache, but that one disadvantage of volatile memory is that it requires a constant source of power and if there is sudden loss of external power, there is insufficient time to safely write all the newly written and/or modified data (“in flight”) from the volatile memory to the hard disk drive before the system shuts down. *Id.* at 1:14-45. Prior art solutions, including batteries and/or uninterruptable power supplies (UPS), could be coupled to the internal power system, but had a number of disadvantages, including a limited number of charge-drain cycles, and large internal resistance, size, and weight. *Id.* at 1:46-2:21. The inventions of the '939 Patent overcame these various limitations by disclosing systems and methods comprised of a plurality of capacitors configured to supply power to the computer system, activating those capacitors to supply power in the event of a sudden loss of external power, reconfiguring the data in the computer system (e.g., transferring any data from the volatile to non-volatile memory or erasing that unsecured data) while that auxiliary power is supplied, and then deactivating those capacitors. *Id.* at 2:24-37.

A. “predetermined level”

Patent	BiTMICRO’s Proposal	Defendants’ Proposal
'939 Patent Claims 1, 10	Plain and ordinary meaning.	“a preset minimum operating voltage necessary for proper operation, in which the super capacitors are not fully discharged”

No construction of this term is necessary. The term “predetermined level” is an ordinary term that both laypersons and POSITAs readily understand. *See Ferguson Beauregard/Logic Controls, Div. of Dover Res., Inc. v. Mega Sys., LLC*, 350 F.3d 1327, 1340 (Fed. Cir. 2003) (“The ordinary meaning of ‘predetermine’ is ‘to determine beforehand.’”). The claims use the term consistent with its plain meaning: “A [method/system] for controlling data in a computer system

when the computer system loses power . . . comprising . . . deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.” ’939 Patent, Cls. 1, 10. Defendants have not supplied any reason for diverging from that meaning. *See e.g., Vitronics Corp v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996) (explaining that terms are “given their ordinary and customary meaning” unless a “special definition of the term is clearly stated in the patent specification or file history”); *Innovative Sonic Ltd. v. Research in Motion Ltd.*, No. 3:11-CV-0706, 2012 WL 4928897, at *10 (N.D. Tex. Oct. 17, 2012) (“[i]f a claim term is readily understood by a jury, there is no need for the court to construe the term”); *Skyhook Wireless, Inc. v. Google, Inc.*, No. 10-11571, 2012 WL 4076180, at *13, *18 (D. Mass. Sept. 14, 2012) (declining to construe terms where the proposed construction “would only complicate the term”); *Gen-Probe Inc. v. Becton Dickinson & Co.*, No. 09CV2319, 2011 WL 7167137, at *17 (S.D. Cal. Nov. 22, 2011) (declining to construe terms where the terms are “common terms that need no clarification”).

Defendants’ use of the term “predetermined level” in the claims of their own patents on the same subject matter confirm that the term requires no construction. For example, Intel’s U.S. Patent No. 9,977,478 is directed to a solid state drive (SSD) coupled to a host computing system, where “in the event of a power failure in the SSD, a backup energy reservoir, such as a capacitor, may allow the SSD to save in-flight data by storing the in-flight data persistently in the non-volatile memory of the SSD.” Ex. 2 (’478 Patent), 1:8-25. Intel uses the term “predetermined level” in 18 of the 22 claims (and all the independent claims) of that patent, and in the same – plain and ordinary – way as it is used the claims of the ’939 Patent. *See e.g., id.* at Cl. 1 (“a power management module configurable to provide read access to the non-volatile memory in response to the energy store being charged to an amount that is at least of a first **predetermined level**, and to provide write access to the non-volatile memory in response to the energy store being charged to an amount that is at least of a second **predetermined level** that is greater than the first **predetermined level**.”). Intel understood the plain meaning of that term when drafting the ’478 Patent; Defendants cannot now claim to be confused by the plain meaning in this case.

Defendants nevertheless seek to import the limitation “a preset minimum operating voltage necessary for proper operation, in which the super capacitors are not fully discharged” into the claim language. But “it is important not to import into a claim limitations that are not part of the claim.” *Superguide Corp. v. DirecTV Enters., Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004). Defendants claim that “the patentee acted as its own lexicographer” (Defs. Br. at 4), but there is no definition of “predetermined level” in the portions of the specification cited in their brief. *See* Defs. Br. at 3 (citing ’939 Patent at 5:39-52, 6:40-53). Nor do any of the statements in the specification relied upon by Defendants rise to the level of “a clear and unmistakable disclaimer.” *See Cont’l Circuits LLC v. Intel Corp.*, 915 F.3d 788, 797 (Fed. Cir. 2019) (“To disavow claim scope, the specification must contain ‘expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope.’”) (quoting *Retractable Techs., Inc. v. Becton, Dickinson & Co.*, 653 F.3d 1296, 1306 (Fed. Cir. 2011)).

Nor do any of the cited statements in the prosecution history limit the meaning as Defendants contend. Instead, the applicant undertook the unremarkable task of distinguishing a reference (Manson) cited by the examiner. *See* Ta Decl., Ex. I at 7. That act alone does not create a disclaimer. *See e.g., Cont’l Circuits*, 915 F.3d at 797-798 (“comparing and contrasting the present technique to that of the prior art does not ‘rise to the level of [a] clear disavowal’ of claim scope”). Moreover, the actual language used by the applicant in those portions was exemplary: “The predetermined level **can be set** above the minimum operating voltage of the computer system, preventing the computer system from running with unpredictable results. . . . Furthermore, the predetermined level **can be set** above a zero level of power for the computer system.” Ta Decl., Ex. I at 7 (emphasis added). These statements do not represent a clear disavowal of claim scope.

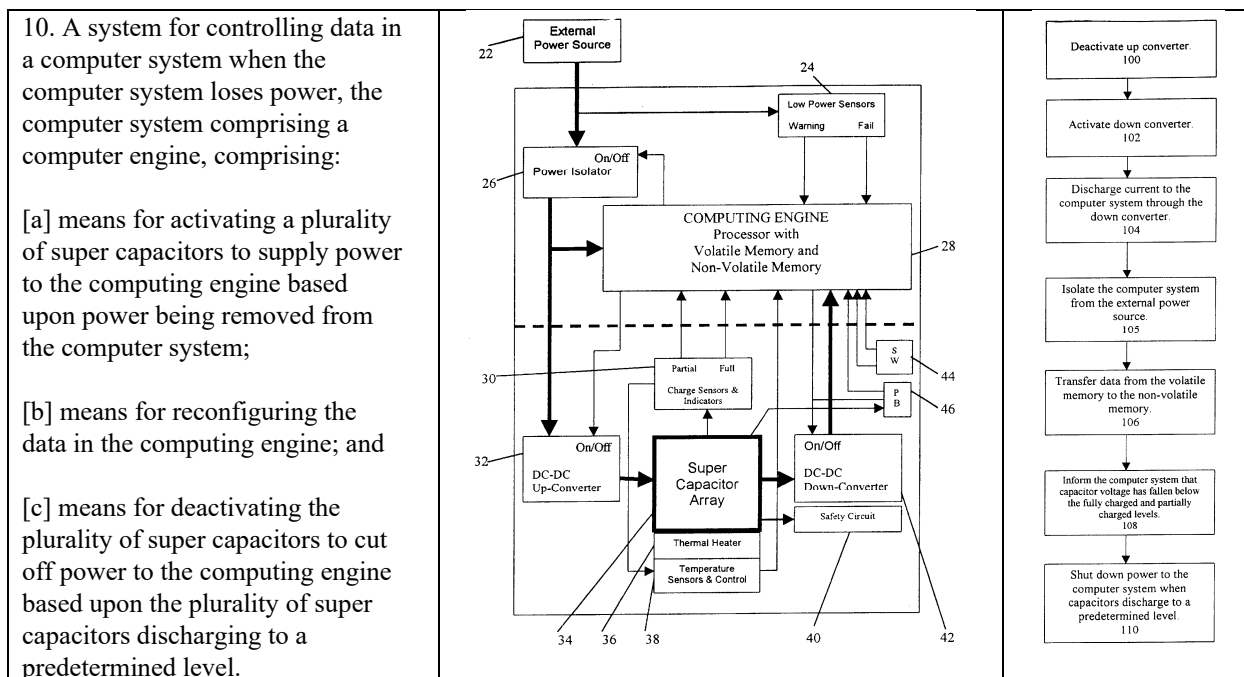
B. “means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level”

Patent	BiTMICRO’s Proposal	Defendants’ Proposal
’939 Patent Claim 10	<u>Function</u> : deactivating the plurality of super capacitors to cut off power to the computing engine based upon	Indefinite under 35 U.S.C. § 112(6):

	the plurality of super capacitors discharging to a predetermined level. <u>Structure:</u> Col. 3:3-12, 3:28-4:8, 5:35-42, 6:37-44, Figs. 1, 3, 5, of the '939 Patent, and equivalents thereof. ²	Lacks corresponding structure.
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This term is not indefinite. The “means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level” is fully and adequately described in the specification of the '939 Patent.

The claim at issue, along with Figures 1 and 3 from the specification, are recited below:



As a preliminary matter, it will be apparent to the Court (as it would be apparent to the jury and POSITAs), that limitation [a] is the mirror image of limitation [c]. The former recites “means for activating a plurality of super capacitors to supply power to the computing engine,” whereas the latter recites “means for deactivating the plurality of super capacitors to cut off power to the computing engine.” See '939 Patent, Cl. 10. Accordingly, disclosures of structure, acts, and methods relevant to limitation [a] are also equally relevant to limitation [c]. Defendants have not challenged limitation [a], and for good reason. Nor should they have challenged limitation [c].

In the portions cited by Plaintiff in its proposed construction, the specification describes an

² Plaintiff has revised its proposal slightly to omit the disclosures 4:20-35, 4:46-52, and 4:64-5:5 from its proposal.

embodiment wherein a “computing engine CE 28 . . . is supplied power from the external power source EPS 22 through the power isolator PI 26.” The specification continues to explain:

The PI 26 isolates the CE 28 from the EPS 22. Power sensors 24 are implemented to notify the CE 26 of any sudden loss of power from the EPS 22.

An up-converter 32 is coupled to a plurality of super-capacitors SC 34 in order to convert the voltage supplied by the EPS 22 and charge the super-capacitors 34. Two charge level sensors 30 inform the CE 28 when the SC 34 are partially and fully charged. Once the SC 34 are fully charged, the demand for current is minimal and the charging circuit goes into trickle charge mode to keep the SC 34 at their peak charge value. A down converter DC 42 is also coupled to the SC 34 to convert the voltage from the SC 34 to supply power to the CE 28.

’939 Patent, 3:28-3:48 (emphasis added). The specification describes the latter elements, along with certain temperature sensors and controls, as “the SC 34 and the associated circuitry 30, 32, 36, 38, 42.” *Id.* at 3:49-4:8. Indeed, the specification contemplates “the SC 34 and the associated circuitry 30, 32, 36, 38, 42” as “a removable option to the system.” *Id.*; see Fig. 1 (dashed line).³

The specification also explains how this “circuitry” works in the context of limitations [a] and [c]. For example, in one exemplary embodiment (“save mode”), the specification explains:

To better understand the operation of the “save mode” feature of the method in accordance with the present invention, please refer to the flowchart of **FIG. 3**.

[a] First, once the computer system detects that the external system power has fallen below a certain threshold amount via the power sensors, the up-converter is deactivated, via step 100. Next, the down-converter is activated to maintain the internal power of the system, via step 102. This reverses the flow of current between the computer system and the super-capacitors. The super-capacitors then begin to slowly discharge current to the computer system through the down-converter, via step 104. Then the computer system is isolated from the external power source, via step 105. This prevents any contention between the external power source and the down-converter. The rate of discharge depends on the amount of capacitance and the amount of current needed by the computer system.

[b] While the computer system is receiving current from the super-capacitors, data is transferred from the volatile memory to the non-volatile memory, via step 106.

[c] Next, the two charge level sensors inform the computer system that the super-capacitor voltage has fallen below the fully charged and partially charged levels, via step 108. Finally, once the super-capacitors discharge to a predetermined level,

³ The specification further notes that “one of ordinary skill in the art will readily recognize that a variety of voltages could be used in this system” and “the number of converters utilized could vary without departing from the spirit and scope of the present invention.” ’939 Patent, 4:4-8.

the down-converter has insufficient voltage differential to continue proper operation and shuts down, thus turning off the power to the computer system, via step 110.

'939 Patent, 5:17-43. The specification includes other related embodiments. *Id.* at 6:20-44. Though not expressly stated herein, but obvious to laypersons and POSITAs alike, when the capacitors have discharged to a predetermined level and the down-converter shuts down (or turns “off” as shown in Fig. 1), other elements of the circuitry may revert (or reverse) to their original states (e.g., power isolator and up-converter both turn “on”) for when external power is restored. *See id.*⁴

Accordingly, this term or limitation [c]—“means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level”—has sufficient “corresponding structure, material, or acts described in the specification.” They are the “circuitry” disclosed and the equivalents thereof.

Defendants have not—and cannot—meet their burden to show “by clear and convincing evidence, that the specification lacks disclosure of structure sufficient to be understood by one skilled in the art as being adequate to perform the recited function.” *Budde v. Harley-Davidson, Inc.*, 250 F.3d at 1376–77; *Intelligent Automation Design*, 799 F. App'x at 852 (Fed. Cir. 2020). Indeed, Defendants’ failure to put forward an expert evidence in support of their indefiniteness argument of this—and the other challenged MPF limitation—is fatal to their case. *Cf. Williamson*, 2017 WL 3232582, at *10; *WesternGeco*, 876 F. Supp. 2d. at 875; *Cacace*, 812 F. Supp. 2d at 561.

Defendants’ arguments to the contrary are also unavailing. The notion that the specification “simply states a result... rather than describing a structure that achieves the result” (Defs. Br. at 6) is contradicted by the disclosures above.⁵ And Defendants’ attempt to distinguish between the

⁴ A reasonable jury would consider “activating the super-capacitor” and “deactivating the super-capacitor,” as well as “supply power” and “cut off power” are two sides of the very same coins.

⁵ Defendants’ cases are also inapposite. In each of the three cited cases, the disputed term was a means-plus-function term implemented in software for which the patentee had not disclosed an algorithm for performing the recited function. *See Ergo Licensing, LLC v. CareFusion 303, Inc.*, 673 F.3d 1361, 1365 (Fed. Cir. 2012); *Arendi S.A.R.L. v. LG Elecs., Inc.*, No. 12-1595-LPS, 2019 WL 3891150, at *14 (D. Del. Aug. 19, 2019); *Pi-Net Int'l Inc. v. JPMorgan Chase & Co.*, No. 12-282-SLR, 2014 WL 1997039, at *9 (D. Del. May 14, 2014). By contrast, the issue here is whether the circuitry disclosed in the specification constitute a sufficient structure. It does.

disclosed “up-converter” and “down-converter,” on the one hand, and the “super capacitor array” on the other, and to argue that the specification needs to “identify a specific structure for deactivating a plurality of super capacitors” does not make any sense. *See* Defs. Br. at 6-8. For example, it is not clear what Defendants think “deactivating” capacitors means in this context and what sort of “structure,” if disclosed, would satisfy that meaning. Defendants refer to “render[ing] the super capacitors inactive.” *See* Defs. Br. at 8. Does that mean the capacitors are unable to take a charge again? That does not make sense in the context of these claims or inventions. Does that mean something else? Are Defendants sure that they understand how capacitors work? Notably, Defendants do not appear to have been able to find a POSITA to support any of these criticisms.⁶

Defendants require too much regardless. The claim language explains what “deactivating the plurality of super capacitors” means in this context: “[i] to cut off power to the computing engine [ii] based upon the plurality of super capacitors discharging to a predetermined level.” ’939 Patent, Cl. 10. The specification clearly discloses corresponding structure for both aspects.

Finally, Defendants take issue with Plaintiff’s proposed construction because it does not describe the corresponding structure in words. Defs. Br. at 8-9. Plaintiff does not understand that to be a requirement in this or other courts when confronting §112(6) arguments. *See e.g.*, Ex. 3 (Claim Construction Order in *Viatech Tech., Inc. v. Adobe Inc.*, Case No. 20-358-RGA (D. Del., Nov. 1, 2021)) at 2-3 (identifying corresponding structure for MPF terms with string cites to the specification). To the extent this Court believes words are required, Plaintiff proposes “the circuitry (including sensors and converters) disclosed in ... and equivalents thereof.”

C. “reversing the flow of current between the computing engine and the plurality of super capacitors”

Patent	BiTMICRO’s Proposal	Defendants’ Proposal
’939 Patent Claim 6	Plain and ordinary meaning; not indefinite.	Indefinite.

This term is not indefinite. Again, Defendants ignore the context in which this appears in

⁶ To the extent Defendants have in mind some structure “generally known in the art,” that is also unavailing. *See Apple Inc. v. Motorola, Inc.*, 757 F.3d 1286, 1298-99 (Fed. Cir. 2014).

the claims, the corresponding discussion in the specification, and general common sense.

1. A method for controlling data in a computer system when the computer system loses power, the computer system comprising a computing engine, comprising the steps of: (a) activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system; (b) reconfiguring the data in the computing engine; and (c) deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level. 6. The method of claim 3 wherein the activating step (a) further comprises: (a1) reversing the flow of current between the computing engine and the plurality of super capacitors; and (a2) discharging current from the plurality of super capacitors to the computing engine.	
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Defendants are correct that this term appears twice in the specification. Defs. Br. at 10-11.

Indeed, these references occur in the same passages discussed with respect to the previous term.

To better understand the operation of the “save mode” feature of the method in accordance with the present invention, please refer to the flowchart of FIG. 3. [a] First, once the computer system detects that the external system power has fallen below a certain threshold amount via the power sensors, the up-converter is deactivated, via step 100. Next, the down-converter is activated to maintain the internal power of the system, via step 102. This reverses the flow of current between the computer system and the super-capacitors. The super-capacitors then begin to slowly discharge current to the computer system through the down-converter, via step 104. Then the computer system is isolated from the external power source, via step 105. This prevents any contention between the external power source and the down-converter. The rate of discharge depends on the amount of capacitance and the amount of current needed by the computer system. [b] While the computer system is receiving current from the super-capacitors, data is transferred from the	To further understand the operation of the “erase mode” feature of the method in accordance with the present invention, please refer to the flowchart of FIG. 5. [a] First, once the computer system detects that the external system power has fallen below a certain threshold amount, the up-converter is deactivated, via step 300. Next, the down-converter is activated to maintain the internal power of the system, via step 302. This reverses the flow of current between the volatile memory and the super-capacitors. The super-capacitors then begin to slowly discharge current to the computer system through the down-converter, via step 304. The computer system is then isolated from the external power source, via step 305. This prevents any contention between the external power source and the down-converter. The rate of discharge depends on the amount of capacitance and the amount of current needed by the computer system. [b] While the computer system is receiving current from the super-capacitors, all traces of data in the volatile memory is completely erased, via step 306.
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volatile memory to the non-volatile memory, via step 106. [c] Next, the two charge level sensors inform the computer system that the super-capacitor voltage has fallen below the fully charged and partially charged levels, via step 108. Finally, once the super-capacitors discharge to a predetermined level, the down-converter has insufficient voltage differential to continue proper operation and shuts down, thus turning off the power to the computer system, via step 110.	[c] Next, the two charge level sensors inform the computer system that the super-capacitor voltage has fallen below the fully charged and partially charged levels, via step 308. Finally, once the super-capacitors discharge to a predetermined level, the down-converter has insufficient voltage differential to continue proper operation and shuts down, thus turning off the power to the computer system, via step 310.
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'939 Patent, at 5:17-43; 6:20-44. These disclosures in the specification make clear that “reverse” in the claim language is referring to the change in the flow of current in the system from the normal state (when power is supplied by the EPS to the computing engine and to the capacitors to charge them) and backup state (when power is supplied from the capacitors to the computer engine).

Defendants appear to take issue with the word “reversing,” but it appears that they may just be pretending not to understand how capacitors work—or what Figure 1 actually conveys to a reasonable observer. Defs. Br. at 10-11. As the specification explains, the method/system uses capacitors as a backup power source in the event of a sudden power loss. During normal operation, the external power supply (EPS) supplies current to the Computing Engine and capacitor (via a voltage converter) from the same power plane. This charges the capacitor, draining current that would otherwise go to the CE. Laypersons and POSITAs alike would thus understand that the current charging to the capacitor needs to pass through the capacitors’ plate to ground. It is beyond dispute that a capacitor has two terminals. See *e.g.*, <https://en.wikipedia.org/wiki/Capacitor>. In other words, the current is going toward the capacitors. And then, after a sudden power loss, the EPS supplies no current and capacitor begins discharging current, *i.e.*, current flows from the same capacitor plate (via a voltage convertor) to the shared power plane of the EPS, Power Isolator, and CE. Therefore, the current flows in “reverse” direction at the charged plate.

Accordingly, this term is not indefinite and should be given its plain and ordinary meaning.

D. “means for reversing the flow of current between the computing engine and the plurality of super-capacitors”

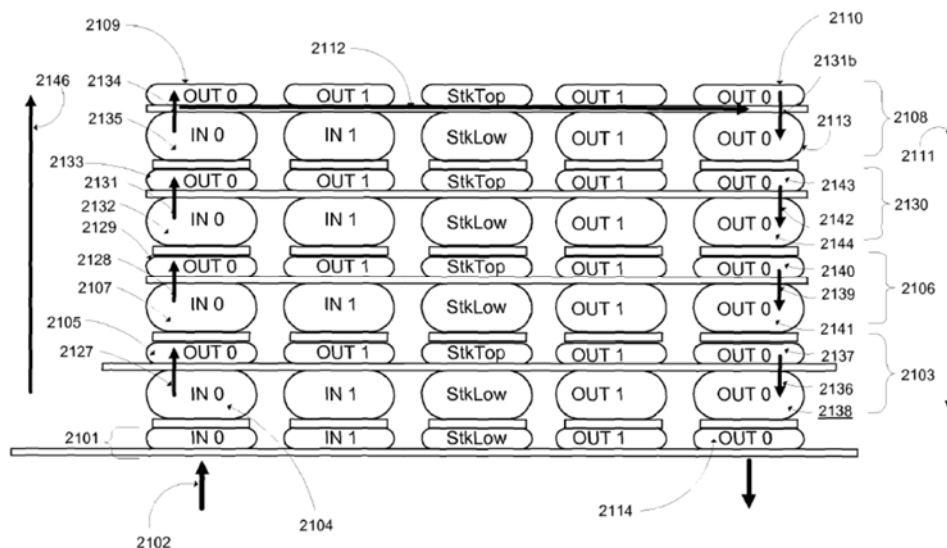
Patent	BiTMICRO’s Proposal	Defendants’ Proposal
'939 Patent Claim 15	<u>Function</u>: reversing the flow of current between the computing engine and the plurality of super capacitors. <u>Structure</u>: Col. 3:3-12, 3:28-4:8, 6:22-28, Figs. 1, 3, 5, of the '939 Patent, and equivalents thereof.	Indefinite under 35 U.S.C. § 112(6): Lacks corresponding structure.

This term is not indefinite for the same reasons as discussed with respect to the previous term. And the disclosures recited with respect to that term and the “deactivating” term above also identify the corresponding structure, i.e., the “circuitry” in the cited passages of the specification.

III. '243 PATENT

The '243 Patent describes module stacking and packaging for electronic devices. Specifically, multiple modules, such as semiconductor dies, are stacked together and connected to create a stacked module. '243 Patent (Ex. 4), 1:32-36. A stacked module creates a package with specific functions or a range of memory capacity. *Id.* Multiple packages can be stacked to create a desired memory capacity or different packages can be stacked to create a desired functionality. *Id.* at 1:47-49. The stacking techniques described in the '243 Patent allow large capacity storage and high functionality devices to be implemented in a smaller package, saving space on an integrated circuit board and thus allowing smaller devices to include memory capacity or functionality that may otherwise be unachievable. *Id.* at 1:54-62. The modules within the stack can be a variety of chips, such as flash memory modules, SDRAM memory modules, and controller modules. *See, e.g., id.* at 6:44-7:7, Fig. 12a. The '243 Patent further describes interconnections and signal routing between the modules within the stack. *See id.* at 8:61-10:35. And the '243 specification notes that the disclosed stacking designs are “very flexible depending on the specific application, capacity, board size and height limit.” *Id.* at 10:39-40.

An exemplary embodiment is depicted in Figure 21a of the '243 Patent as follows:



As shown in Figure 21a, a main board 2101 has multiple chip modules 2103, 2106, 2130, and 2108 stacked on top of it. The modules are electrically connected to each other through a series of ball and pad connections. For example, an input signal 2102 can be passed from the main board through the IN ball 2104 to the OUT pad 2105 of base module 2103. From there the input signal can be passed through the IN balls and OUT pads of the other modules stacked above in a serial chain until the signal reaches the end module 2108. In the end module, the signal can be routed internally through the module via connection 2112 to another pad 2110 on the end module. The signal can then be passed back down through the stack of modules to the main board through a similar serial chain of ball and pad connections between the modules. *Id.* at 9:61-10:35.

A. “passive port”

Patent	BiTMICRO’s Proposal	Intel’s Proposal
'243 Patent Claims 1, 2	“connection between a passive ball and a passive pad”	“connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module”

The '243 specification refers to “passive port” generally as a connection between a passive ball and a passive pad:

- “[A]t least one passive port connecting a passive ball and passive pad, such as the passive ports 1905 . . .” Ex. 5 ('243 Certificate of Correction) at 9:12; Ta Decl., Ex. F

at 3;

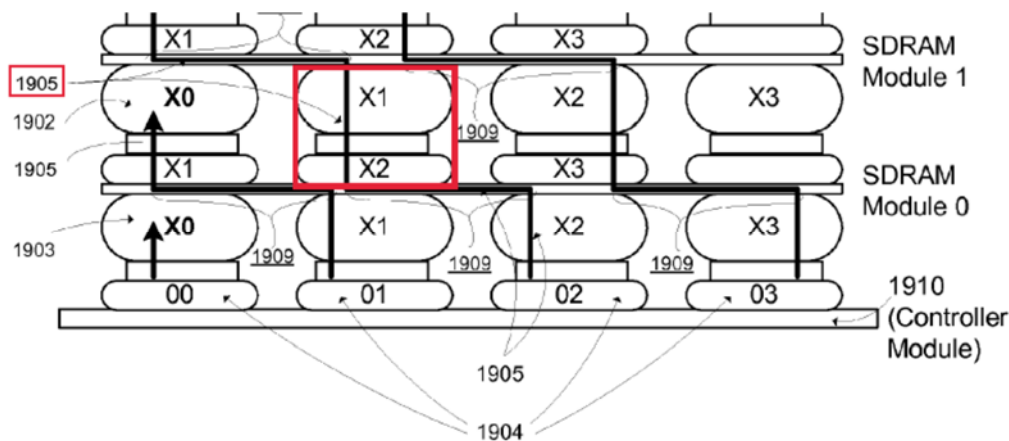
- “At least one of the balls and pads that are coupled to their respective chain circuit may be in the form of a passive ball and passive pad, respectively In effect, each of these serial chain circuits functions as a passive port.” Ex. 5 (’243 Certificate of Correction) at 10:8; Ta Decl., Ex. F at 5.

BiTMICRO’s proposed construction of “passive port” is therefore consistent with the usage of that term in the specification.

Intel’s proposed construction of “passive port” is unduly narrow because: 1) it is limited to connections within an SDRAM module; and 2) it requires the passive ball and passive pad to be on different surfaces of the same module. With respect to the first issue, there is nothing in the specification limiting “passive port” to connections within an SDRAM module. Indeed, the specification describes various embodiments where the stacked chips are all flash or other memory modules, rather than SDRAM modules. *See, e.g.*, ’243 Patent, 2:27-30, 2:34-36, 2:51-54, 3:30-47, 4:43-61, 5:9-21, 6:10-21, 9:23-10:35, Figs 3a-c, 5a-b, 10, 20a-b, 21a-b. And the specification notes that the disclosed stacking technique “is very flexible depending on the specific application, capacity, board size and height limit.” *Id.* at 10:39-40.

Even the embodiment in Figures 21a-b, which Intel contends to be the sole embodiment with the “serial chain” and “control circuit” components of claims 1, 2, 11, and 12, is not limited to SDRAM modules. *See id.* at 9:61-10:35. Rather, that embodiment simply refers generally to a connection technique “used for serial routing of ***all modules*** in the stack,” without limitation to any type of module. *Id.* at 9:61-64 (emphasis added). Intel’s construction is therefore incorrect, as it would exclude multiple embodiments from the scope of the claims, including at least one embodiment that Intel agrees should be covered by the claims. *See Kaufman v. Microsoft Corp.*, 34 F.4th 1360, 1372 (Fed. Cir. 2022) (“A claim construction that excludes a preferred embodiment is rarely, if ever correct”) (quotations omitted).

Intel's construction is also incorrect because it would require the passive ball and passive pad to be on different surfaces of the same module. Again, this construction is wrong because it would exclude a preferred embodiment. Specifically, for the Figure 19 embodiment, the specification identifies "passive ports 1905 connecting passive ball X2 to passive pad X2 and passive ball X1 to passive pad X2." Ex. 5 ('243 Certificate of Correction), at 9:8; Ta Decl., Ex. F at 3. "Passive ports 1905 connecting . . . passive ball X1 to passive pad X2" refers to the following connection in Figure 19 highlighted in red:



As shown in Figure 19, this connection is between a ball and pad on different modules (ball X1 on SDRAM Module 1 and pad X2 on SDRAM Module 0), rather than the same module as proposed by Intel. Intel's construction would improperly exclude this embodiment.

Intel's construction is also wrong under principles of claim differentiation. Claim 2 recites "[t]he stacked module of claim 1 wherein . . . the passive port connects a passive ball on one surface of a module to a passive pad on another surface of the module." The presence of this narrowing limitation in dependent claim 2 supports that it is not a requirement of the "passive port" in claim 1. See *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 910 (Fed. Cir. 2004) ("[T]he presence of a dependent claim that adds a particular limitation raises a presumption that the limitation in question is not found in the independent claim.").

Intel mischaracterizes the applicants' statements to the examiner regarding "passive port" during prosecution. To overcome the examiner's indefiniteness rejection, the applicants cited to a

section of the specification discussing a “connection between a passive ball . . . and passive pad” and emphasized the word “connection” as the critical word in this section. Ta Decl., Ex. F at 23. Applicants further stated: “The above description should be read in conjunction with amended Figure 19, which shows that a passive port 1909 **connects** ‘a passive ball’, such as passive ball X2, ‘on one surface of a SDRAM module’, such as SDRAM module 0, and a passive pad’, such as passive pad X3, ‘on another surface of the same DRAM module,’ such as SDRAM module 0.” *Id.* (emphasis in original). Applicants’ repeated emphasis of the words “connection” and “connects” indicates the defining characteristic of “passive port” is a connection, consistent with BiTMICRO’s construction. And the applicants’ repeated use of the phrase “such as” further shows that they were merely pointing out example connections to the examiner.

Applicants were not defining “passive port” to be limited to the particular connection between a passive ball and pad on different surfaces of an SDRAM module, as Intel contends. The Federal Circuit implements an “exacting” standard for lexicography. *Luminara v. Worldwide, LLC v. Liown Elecs. Co.*, 814 F.3d 1343, 1353 (Fed. Cir. 2016) (“To act as a lexicographer, a patentee must clearly set forth a definition of the disputed claim term and clearly express an intent to redefine the term.”) (internal quotations omitted). That standard is not met here. Applicants were merely providing the examiner with an example of a “passive port” – namely, one of the passive ports in Figure 19, which the specification repeatedly refers to as a non-limiting “example embodiment.” ’243 Patent, 9:12-13, 9:21-22. This is further confirmed by the fact that, when the applicants wanted to define a term in the specification, they used the different phrasing of “referred to as.” See Ex. 5 (’243 Certificate of Correction) at 9:3 (“An active pad may also be referred to herein as an ‘active port.’); 10:2 (“A signal route that includes a serial chain circuit coupling an ball and pad is herein after referred to as a ‘serial chain connection’ . . .”). This difference in phraseology shows there was no intention to limit “passive port” to just one example in Figure 19. See *Medicines Co. v. Mylan, Inc.*, 853 F.3d 1296, 1306 (Fed. Cir. 2017) (description of “efficient mixing” in specification was not a definition because patentee used different language of “refers to” or “as defined herein” when defining terms).

Finally, Intel overstates the significance of the applicants' statement during prosecution that "[a]pplicants may be their own lexicographers." The applicants made that statement as part of a general recitation of MPEP rules for the examiner to consider:

Definiteness of claim language must be analyzed, not in a vacuum, but in light of Applicants written disclosure, the prior art, and the claim interpretation that would be given by one of ordinary skill in the art at the time the invention was made. MPEP 2173.02. Applicants may be their own lexicographers. MPEP 2173.01.

Ta Decl., Ex. F at 23. Nowhere in their arguments to the examiner, however, did the applicants explicitly state that they were providing a definition of "passive port."

B. "a plurality of modules each comprising"

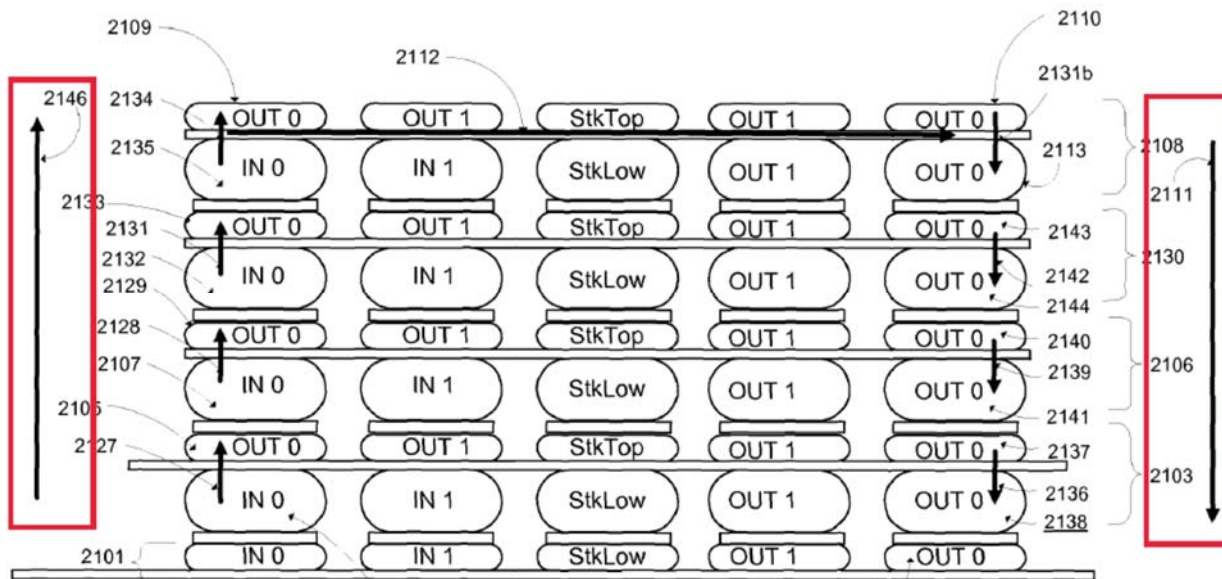
Patent	BiTMICRO's Proposal	Intel's Proposal
'243 Patent Claim 1	Part of the preamble and not a limitation of the claim.	"each module in the stacked module comprises"

Claim 1 of the '243 Patent begins as follows:

1. A stacked module comprising a plurality of modules each comprising:
 one or more active ports for carrying one or more active signal;
 one or more passive ports for passing through the one or more active signals;

As shown in the patent, the applicants structured the claim to show that the entire phrase "[a] stacked module comprising a plurality of modules each comprising" appearing before the colon is the preamble, as it introduces the subject matter of the rest of the claim. *See NetJumper Software, L.L.C. v. Google, Inc.*, No. 04-70366, 2008 WL 835819, at *3 (E.D. Mich. Mar. 29, 2008) (finding the claims-in-suit "begin with a preamble which is the part of the claim that appears before the first colon."); *Application of Dean*, 291 F.2d 947, 951 (C.C.P.A. 1961) (the preamble "is all that portion at the beginning of the claim preceding the colon."); *Omega Patents, LLC v. Calamp Corp.*, No. 6:13-cv-1950-Orl-40DAB, 2015 WL 12830497, at *3 (M.D. Fla. Dec. 23, 2015) ("The preamble ends with the phrase, 'the control system comprising,' followed by a colon."). The words "each comprising" in the preamble refers to the fact that each "stacked module" includes the limitations that appear after the first colon in the claim.

Intel incorrectly asserts that the phrase “a plurality of modules each comprising” is not part of the preamble. Under Intel’s construction breaking off this language from the rest of the preamble, all of the limitations following the “each comprising” would be required in each module within the stack. This construction does not make sense in light of the specification. Claim 1 includes the limitations of “a first serial chain route” and “a second serial chain route.” Under Intel’s construction, each module within the stack would require both of these limitations. But the specification describes Figure 21a as showing a “connection technique to be able to connect a serial chain route from *multiple modules in a stack*.” ’243 Patent, at 3:39-42 (emphasis added). The specification further describes that “at least two serial chain connections connected in series are herein after referred to as a ‘serial chain route’, such as serial chain route 2146 or 2111.” Ex. 5 (’243 Certificate of Correction) at 10:2. Those serial chain routes are highlighted in red in Figure 21a below:



As shown in Figure 21a, a “serial chain route” is a route that runs through multiple modules within a single stack.⁷ It therefore does not make sense for each module within the stack to

⁷ The specification also states that “[a] signal route that includes a serial chain circuit coupling an ball and pad is herein after referred to as a ‘serial chain connection’, and at least **two serial chain connections connected in series** are herein after referred to as a ‘serial chain route’, such as serial chain 2146 or 2111.” Ex. 5 (’243 Certificate of Correction) at 10:2 (emphasis added). This further supports that a single module cannot have a “serial chain route.” Rather, a “serial chain route” requires multiple modules.

separately have its own first and second “serial chain routes,” as Intel’s construction would require. Rather, consistent with the specification and BiTMICRO’s construction, the “first serial chain route” and “second serial chain route” in claim 1 must be limitations of the entire “stacked module,” rather than limitations of each of the “plurality of modules” within the stack.

In addition, claim 1 also includes the limitation “a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module.” In the Figure 21a example shown above, there is only one module in the stack that can contain such a control circuit – namely, the topmost module 2108 (the “end module”), which provides the “routing path” 2112. *Ta Decl., Ex. F* at 4-5. Intel’s construction requiring each module in the stack to have all the limitations of claim 1 again does not make sense in light of the Figure 21a embodiment, as that figure has only one module in the stack serving as an “end module” that contains the recited “control circuit for enabling a routing path . . . within an end module.” Thus, Intel’s construction is directly at odds with the specification, and should be rejected.

Intel’s antecedent basis argument also lacks merit. A phrase in the preamble that provides antecedent basis for a limitation in the body of the claim “*may* limit claim scope,” but does not always do so. *Catalina Marketing Int’l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002) (emphasis added). Here, the body of claim 1 “defines a structurally complete invention,” as evidenced by the fact that “plurality of modules” could be deleted from the preamble and the scope of claim 1 would remain unchanged. *See id.* at 810. “Plurality of modules” is therefore not a limitation of the claims. And even if it were a limitation, Intel misinterprets the “each comprising” language that follows this phrase, which as discussed above relates back to the term “stacked module,” not the “plurality of modules.”

IV. ’740 PATENT

The ’740 Patent describes a mapping table for optimizing memory operations in an electronic storage device. Prior to the inventions in the ’740 Patent, memory operations in solid state storage devices were subject to a number of inefficiencies. As described in the ’740 specification, SSDs such as those that include NAND flash memory “suffer from write cycle

limitations and to a certain degree, bad blocks. In addition, flash drives use block addressing rather than byte addressing, and these flash drives use block addresses that are usually much larger than the block address used by the host. Block addressing may impose an additional level of complexity and additional processing cycles when performing a write operation, and which in turn, may increase write operation latency. This additional level of complexity may include performing a read-modify-write transaction to complete the write operation.” See ’740 Patent (Ex. 6), 1:42-53.

To address these issues and increase the speed and efficiency of memory operations in their products, SSD manufacturers tried solutions such as adding complex algorithms to handle the management of memory operations and adding more powerful processing devices to run these complex algorithms. *Id.* at 1:54-2:10. These solutions, however, increased both the cost and design complexity of the SSDs. *Id.*

The ’740 Patent overcame this problem by providing a solution that optimizes memory operations in a solid state storage device while minimizing the amount of additional cost and complexity to the design of the device. *Id.* at 2:11-14. The ’740 Patent achieves this through an improved mapping table that “increas[es] the likelihood that, in response to an I/O transaction initiated by a host, the operational load imposed on the storage device by these memory operations will be optimally distributed across different storage device resources, such as by interleaving or parallel memory operations, reducing memory operation latency, increasing operational device efficiency, or both.” *Id.* at 2:14-21; 3:12-31. For example, the ’740 Patent describes a mapping table that includes a set of logical fields that represent a plurality of logical block address (LBA) sets. The mapping table also includes a set of physical block address (PBA) fields that represent a set of PBAs and access parameters for the PBAs, as well as information that associates the LBA sets with the PBA sets in a highly efficient manner. The mapping table enables the storage device to perform optimized memory operations on memory locations based on the information in the table regarding the relationship between the LBA and PBA sets and the access parameters. *Id.* at 2:27-49.

A. “optimized memory operations”

Patent	BiTMICRO’s Proposal	Defendants’ Proposal
’740 Patent Claim 1	Plain and ordinary meaning; not indefinite.	Indefinite.

This phrase needs no construction because “optimized” is a term that is readily understandable to both a layperson as well as a POSITA. *See* Ex. 7 (The Authoritative Dictionary of IEEE Standards Terms (7th ed. 2000)) (“optimization: The procedure used in the design of a system to maximize or minimize some performance index. May entail the selection of a component, a principle of operation, or a technique”). In addition, Defendants do not argue that there is anything unclear about the term “memory operations.” The Court should therefore adopt a plain and ordinary meaning for “optimized memory operations.”

Defendants’ indefiniteness argument lacks merit for several reasons. First, Defendants wholly ignore the discussion of this term in the file history of the ’740 Patent. During prosecution, the examiner initially rejected the applicants’ claims under 35 U.S.C. § 112, stating that “[t]he specification does not describe how the mapping table causes the storage device to perform **optimized memory operation** on memory location in such a way that is understood by one having ordinary skill in the art.” Ex. 8 (Office Action) at 2-3 (emphasis added). The applicants responded by arguing that “the Specification teaches how a ‘mapping table’ causes a ‘storage device to perform optimized memory operations,’” and cited to specific paragraphs in the specification disclosing different examples of such optimized memory operations. Ex. 9 (Reply and Amendment) at 17-23. The examiner agreed, finding that “[a]pplicant arguments regarding rejection of claims 1-40 under 35 U.S.C. 112, first paragraph is persuasive,” and allowed the claims to issue. Ex. 10 (Notice of Allowability) at 4. A POSITA reviewing the ’740 file history would therefore understand that “optimized memory operations” has a definite meaning based on the arguments presented by the applicants during prosecution and the examiner’s acceptance of those arguments. *See Aladdin Mfg. Corp. v. Brumlow Mills, Inc.*, No. 4:19-cv-00058-WMR, 2020 WL 9594314, at *8 (N.D. Ga. June 25, 2020) (term “not predictable” was not indefinite in light of

prosecution history where applicant overcame indefiniteness rejection by directing examiner to supporting portions of specification).

Defendants also incorrectly assert that the only example in the specification of “optimized memory operations” is “to map LBA sets to PBA fields such that memory transactions across multiple LBA sets can be conducted in parallel.” Defs. Br. at 20. In fact, the ’740 specification discloses multiple optimizations, such as contiguous arrangement of LBA sets (6:46-54, 6:63-7:2), adjacency between LBA sets (6:55-62), and adjacent PBAs differing by at least one access parameter (7:3-6). Each of these has benefits depending on the application, such as data coherency across sets or enabling parallelism. *Id.* at 7:9-14. Also, by varying which access parameters differ, a variety of interleaving types or parallel operations can be achieved. *Id.* at 7:9-18, 9:30-57. Thus, the examples in the specification are not limited to parallel memory operations, as argued by Defendants. Defendants’ claim differentiation argument therefore fails because, contrary to Defendant’s position, the specification discloses more than one way to perform “optimized memory operations,” so there is no claim differentiation problem between claims 1 and 2.

Defendants’ claim differentiation argument also fails because, even if different access parameters were required for “optimized memory operations,” claim 1 would not have the same scope as claim 2. Defendants ignore that claim 2 also includes the additional limitation “said first and second LBA sets are adjacent LBA sets,” which is not present in claim 1. Thus, claim 2 does not simply cover systems where the two access parameters are different. Rather, claim 2 also requires that the two LBA sets are **adjacent**. Thus, even under Defendants’ interpretation that different access parameters are required for “optimized memory operations,” the scope of claim 1 is different from claim 2 because claim 2 is limited to optimized memory operations where LBA sets are adjacent, whereas claim 1 also covers optimized memory operations where LBA sets are non-adjacent. For example, in Figure 2, LBA sets 40 and 42 “are disposed in adjacent rows and thus are adjacent to each other.” ’740 patent, 6:61-62. That means that LBA sets 40 and 45, for example, are not adjacent, but they have different access parameters, as highlighted in red below:

9

Logical Fields 26	PBA Fields 28			
	Access Parameter Fields 30			Memory Index Fields 32
	Bus Id Fields 34	FDE Id Fields 36	Group Id Fields 38	
40 LBA 00-07	8-0	22-01	15-0	0x00
42 LBA 08-15	8-0	22-02	15-1	0x08
44 LBA 16-23	8-1	22-11	15-0	0x00
45 LBA 24-31	8-1	22-12	15-1	0x08
⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮

FIG. 2

Distributing memory operations across LBA sets 40 and 45 based on their different access parameters would therefore constitute “optimized memory operations” falling within the scope of claim 1, but not claim 2. Indeed, the specification specifically discusses an example of interleaving memory operations between these non-adjacent LBA sets “[u]sing different group identifiers, such as group identifiers 15-0 and 15-1 in mapping table 9” ’740 Patent, 9:46-49. Thus, there is no claim differentiation problem.

Furthermore, claim 2 also has a third additional limitation that “said LBAs from said first and second LBA sets are logical block addresses used by the host for addressing said data.” Since claim 2 adds multiple limitations beyond claim 1, claim differentiation is simply not applicable here. See *Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1325-26 (Fed. Cir. 2001) (doctrine of claim differentiation has less force where dependent claim adds multiple limitations); *Covidien LP v. Advanced Skeletal Innovations LLC*, 81 F.Supp.3d 27, 37 (D.D.C. 2015) (“[W]here, as here, the dependent claim has multiple limitations, claim differentiation arguments are routinely discounted in claim construction analyses.”); *Allergan Sales, LLC v. Lupin Ltd.*, No. 2:11-CV-530-JRG, 2013 WL 4519609, at *6 (E.D. Tex. Aug. 21, 2013) (claim differentiation “is

less applicable, if at all, where other elements are present, differentiating one claim from another.”).

Finally, Defendants offer no expert testimony to support their assertions regarding what is taught in the ’740 specification. Defendants cannot meet their burden of proving indefiniteness by clear and convincing evidence absent such expert testimony, particularly in this case where the applicants explained “optimized memory operations” to the examiner during prosecution and the examiner accepted that explanation. *See Williamson*, 2017 WL 3232582, at *10 (defendant could not meet its burden on indefiniteness without expert opinion supporting its assertion that POSITA would not understand claim term “best suited” based on examples in specification); *WesternGeco*, 876 F. Supp. 2d. at 875 (“Defendants’ unsupported attorney argument fails to prove indefiniteness by clear and convincing evidence.”); *Cacace*, 812 F. Supp. 2d at 561 (“[M]ere attorney argument is insufficient to establish invalidity based on indefiniteness.”).

B. “optimally distributed”

Patent	BiTMICRO’s Proposal	Defendants’ Proposal
’740 Patent Claim 32	Plain and ordinary meaning; not indefinite.	Indefinite.

Defendants’ indefiniteness argument for “optimally distributed” fails for the same reasons that its indefiniteness argument for “optimized memory operations” fails. As discussed above, Defendants incorrectly assert that there is only one example of “optimized memory operations” in the ’740 specification. Rather, the specification discusses multiple examples of optimally distributing data operations across storage device resources based on, for example, particular arrangements of LBA sets and the varying of different access parameters. And during prosecution the applicants pointed out to the examiner, with specific reference to claim 32, the portions of the specification where examples of “optimally distributed” are taught. Ex. 9 (Reply and Amendment) at 21-23. A POSITA reviewing the ’740 patent and its file history would therefore understand with reasonable certainty the meaning of “optimally distributed.”

Defendants incorrectly argue that claim 32 is indefinite because the claim could cover

optimal distribution where there is only a single set of LBAs. To the contrary, claim 32 includes the limitation “a mapping table which maps a first LBA set to a first PBA, and a second LBA set to a second PBA, said first and second LBA sets including respective sets of consecutive LBAs.” ’740 patent, 13:36-39. On its face, then, claim 32 explicitly requires two sets of LBAs. Nor is there any claim differentiation issue comparing claim 32 with claim 34. Claim 34 simply specifies that the memory operations to be performed are “using said first PBA and . . . said second PBA,” whereas claim 32 leaves open the possibility that the mapping table is used for optimally distributing memory operations over other PBAs.

C. “memory store”

Patent	BiTMICRO’s Proposal	Defendants’ Proposal
’740 Patent Claims 1, 15, 32	“non-volatile, solid-state storage, e.g., flash”	Plain and ordinary meaning.

BiTMICRO’s proposed construction is consistent with the ’740 specification, which provides the following description of the “memory store”:

Memory store 6 may be configured to include a set of solid state memory devices that are coupled to a set of buses and that are controlled by a set of FDEs. In FIG. 1, these memory devices, buses, and FDEs are implemented in the form of flash memory devices 12-01 and 12-02; buses 8-0 and 8-1; and FDEs 22-01, 22-02, 22-11, and 22-12, respectively. The term “flash memory device” is intended to include any form of non-volatile memory, including those that use blocks of nonvolatile memory cells, named flash blocks.

’740 Patent, 4:54-62. The specification therefore equates “memory store” with solid-state storage, with flash as one example of such storage.

Defendants incorrectly argue that the phrase “may be configured” in this description means that the “memory store” can be a device other than solid-state memory. “May be configured” here refers to the possibility of different configurations of the solid-state memory in terms of the components they are connected to, such as the recited buses and FDEs; it does not refer to different types of memory devices that are not solid-state storage.

Defendants also incorrectly rely on the language in this portion of the specification stating that “[t]he term ‘flash memory device’ is intended to include any form of non-volatile memory.”

'740 Patent, 4:59-62. Defendants argue that this “establishes that the claims are not limited to solid-state storage devices.” Defs. Br. at 24. This argument makes no sense, as the specification uses the term “solid state storage” interchangeably with “non-volatile memory.” '740 Patent, 1:28-32 (“Electronic storage devices . . . that use non-volatile memory cells are commonly known and are sometimes referred to as solid state storage devices.”). Thus, this portion of the specification supports BiTMICRO’s construction, not Defendants’.

Defendants’ claim differentiation arguments also lack merit. Defendant cites to dependent claims 7, 8, 15, 17, and 19, but in all of those claims there are multiple additional limitations on top of the ones recited in claim 1, from which all of these claims ultimately depend. As discussed above, claim differentiation is inapplicable where a dependent claim adds multiple additional limitations. *See Telemac*, 247 F.3d at 1325-26; *Covidien*, 81 F.Supp.3d at 37; *Allergan*, 2013 WL 4519609, at *6.

Claims 15 and 32 also do not support Defendants’ argument. Claim 15 does not simply recite that it “includes a set of solid state memory devices.” Rather, the claim requires “a set of solid states memory devices that are coupled to a set of buses and that are controlled by a set of FDEs.” Likewise, claim 32 does not simply include “a set of flash devices,” but rather also requires that “said set of flash devices includes a first physical memory location and a second physical memory location that are addressable by said first and second PBAs respectively.” The “includes” language in these claims therefore does not leave open the possibility of other non-solid-state or non-flash devices being used as the “memory store.” Rather, this language leaves open the possibility that the “memory store” might have a different configuration than that recited in the claims.

Finally, Defendants incorrectly rely on BiTMICRO’s contentions in its Complaint regarding the operation of Intel’s accused products. Those contentions were made long before the claim construction process, and before Intel had produced any technical documentation for its products. What BiTMICRO may have stated in earlier contentions without the benefit of discovery therefore has no bearing on claim construction.

V. '190 PATENT

Prior to the inventions in the '190 Patent, memory controllers were designed to operate with memory locations and memory devices that all shared the same set of characteristics. Due to this limitation, there was no way of varying how a memory controller performed read and write operations on different memory locations or devices. The '190 Patent overcame this limitation by disclosing and claiming a multi-profile memory controller that can operate differently with different memory locations and/or memory devices based on the attributes thereof. '190 Patent (Ex. 11), 1:20-60. As described in the '190 Patent, a memory store includes multiple addressable memory locations, and each location is associated with a set of memory attributes, which can include, for example, the type of memory device in which the memory location is located, the data size used by the memory device, or the memory protocol of the device. *Id.* at 2:63-3:1. These attributes are organized into device profiles that can be used by a memory controller connected to the memory store to determine how memory transactions are to be performed with each location. *Id.* at 3:14-4:25. By analyzing the requirements of the requested memory transaction and comparing those requirements to the device profiles, the memory controller selects the appropriate memory location for the memory transaction. The criteria used by the controller to select the optimal memory location for the memory transaction based on the stored attributes within the device profiles can be programmed in any number of ways. *Id.* at 7:60-9:48. For example, a memory controller may treat a portion of the device as a temporary cache memory to store data prior to writing the data to a permanent storage location. This eliminates the need for a separate memory cache, often composed of volatile memory. This has the additional advantage of maintaining the temporary data in the non-volatile cache partition in the event of an unexpected power loss.

A. "optimal"

Patent	BiTMICRO's Proposal	Defendants' Proposal
'190 Patent Claims 1, 29, 45, 59, 80, 98	Plain and ordinary meaning; not indefinite.	Indefinite.

No construction of this term is necessary. The term “optimal” is an ordinary word that both laypersons and POSITAs will readily understand,⁸ whose meaning is clear from the context in which it is used in the claims—*i.e.*, “wherein said first device profile is optimal for a data type subject to a memory transaction, wherein said data type comprises one of a random data type or a sequential data type.” ’190 Patent, Cls. 1, 29, 45, 59, 80, 98. Other claim limitations make clear the “first device profile represent[s] a first set of attributes of said first memory location,” while a “second device profile represent[s] a second set of attributes of [a] second memory location, and a difference exists between said first and second device profiles.” *Id.*, Cl. 1. In other words, the attributes of the first memory location are better for a data type than the second memory location, where the data type is either random or sequential.

The plain meaning of this term is consistent with the specification, which, Defendants admit, “notes a ‘multi-profile’ memory controller can ‘support[] memory locations that have different device profiles’ that are optimal for different data types” and “[o]ne target memory location’ ‘is optimal for the type of data subject to a memory transaction request,’ while ‘another memory location’ ‘is associated with another device profile that is optimal for the type of data subject to another memory transaction request.’” Defs. Br., at 28 (citing ’190 Patent, 9:7-16). As Defendants also admit, the specification also provides examples—almost an entire column of disclosure—of how that determination could be made, including but not limited to, “the largest available” block size attribute for sequential data types, the “smallest available” block size attribute for random data types, and “partial page size attribute” “at most equal” to “the data size of the data” being written for random data types. Defs. Br., at 28 (citing ’190 Patent, 9:16-43).

In view of these admissions, Defendants’ request that this Court invalidate all 101 claims in the ’190 Patent (which has been cited by, *e.g.*, SanDisk, Micron, Western Digital, and Microsoft), on the grounds that this term is indefinite should be dismissed out of hand. For

⁸ Ex. 7 (The Authoritative Dictionary of IEEE Standards Terms (7th ed. 2000)) (“optimization: The procedure used in the design of a system to maximize or minimize some performance index. May entail the selection of a component, a principle of operation, or a technique”).

example, Defendants claim “it is unclear from the specification what criteria would make a device profile optimal for a particular data type,” but that is contradicted by the many examples of such criteria they admit are in the specification, such as block size and partial page size. Defs. Br., at 28 (citing ‘190 Patent, 9:16-43).

Furthermore, as noted in the Background of the ‘190 specification, “[f]lash memory devices that have a relatively large block size generally provide better sequential memory access performance than flash memory devices that use smaller block sizes.” ‘190 Patent, 1:27-31. Large block size, however, creates problems for random data because “it suffers from . . . higher random memory access latency and lower random IOPS (input/output operations per second).” *Id.* at 1:38-43. In other words, a device profile that has a larger block size attribute is more “optimal” for sequential data than random data, and vice versa. The specification therefore provides ample guidance for a POSITA to understand how to determine whether a device profile is “optimal” for the two recited data types of random and sequential data.

Defendants complain that the specification states that the example device profiles in column 9 are not limiting, but comprehensiveness is not a requirement for definiteness. After all, definiteness is evaluated from the perspective of someone skilled in the art. *Nautilus*, 572 U.S. at 909. And Defendants have not put forward any evidence that a POSITA would have any trouble understanding the metes and bounds of this invention. *See Williamson*, 2017 WL 3232582, at *10 (defendant could not meet its burden on indefiniteness without expert opinion supporting its assertion that POSITA would not understand claim term “best suited” based on examples in specification); *In re Bill of Lading Transmission and Processing Sys. Patent Litig.*, MDL No. 1:09-md-2050, 2013 WL 12248192, at *8-9 (S.D. Ohio Dec. 31, 2013) (term “optimize” not indefinite because Background and Summary of the Invention sections of the specification provided sufficient teaching of when load optimization occurs). Accordingly, this term is not indefinite.⁹

⁹ The *IV* cases cited by Defendants are inapposite. In both, the critical reason in finding terms (continued...)

VI. '084 AND '694 PATENTS

The '084 and '694 Patents describe methods and systems for efficiently, reliably, and securely booting and initializing an embedded system directly from a storage device. See '084 Patent (Ex. 12), 1:31-55; '694 Patent (Ex. 13), 1:29-53. The claimed inventions do so by using a power-on reset (POR) sequencer descriptor, or portion thereof, stored in nonvolatile memory of the embedded system. A POR sequencer descriptor may contain data necessary for setting up the configuration registers and managing other initialization processes. When the system is powered on, the POR sequencer attempts to retrieve a POR sequencer descriptor from nonvolatile memory, transfers it to RAM, and optionally performs an integrity check to determine if there are any errors. It then uses the POR sequencer descriptor to, among other things, initialize the configuration registers as well as coordinate further data transfers for the initialization process—using DMA descriptors and DMA controllers of the system. See '084 Patent, 2:13-4:4; '694 Patent, 2:10-4:2.

A. “Direct Memory Access (DMA) descriptors” / “DMA controller descriptor”

Patent	BiTMICRO's Proposal	Intel's Proposal
'084 Patent: Claims 1, 19 '694 Patent: Claims 1, 6, 12	Plain and ordinary meaning.	“data structure including at least a source and destination address and byte count”

No construction of this term is necessary. The subsidiary components—“Direct Memory Access (DMA),” “DMA controller,” and “descriptor” are all ordinary terms that POSITAs would readily understand,¹⁰ as is the relationship between those components—specifically, “DMA” and/or “DMA controller” modifies “descriptor,” and thus the plain meaning is “a descriptor that

like “optimiz[ing] . . . QoS” indefinite is that the specification specifically said that QoS was “a relative term, finding different meanings for different users.” *Intellectual Ventures I LLC v. T-Mobile USA, Inc.*, 902 F.3d 1372, 1381 (Fed. Cir. 2018); see also *Intellectual Ventures I LLC v. T-Mobile USA, Inc.*, No. 2:17-CV-00577-JRG, 2018 WL 5809267 (E.D. Tex. Nov. 6, 2018). Here, there is no suggestion, much less admission, that the “optimal” profile for a data type has “different meanings for different users,” or that a POSITA would have difficulty with the term.

¹⁰ See e.g., Ex. 14 (Merriam Webster's Collegiate Dictionary (10th ed. 1999)) (“descriptor: a word or phrase (as an index term) used to identify an item (as a subject or document) in an information retrieval system”); Ex. 15 (Microsoft Computer Dictionary (5th ed. 2002)) (“descriptor: 2. In programming, a piece of stored information used to describe something else, often in terms of structure, content, or some other property”).

may be used in a DMA process / by a DMA controller.” Foty Decl. ¶¶ 12-16. Intel’s paid expert admits that DMA descriptors are known to ordinary embedded systems designers and can take a variety of formats—but attempts to impose improper format limitations anyway, untethered to any intrinsic evidence, in pursuit of non-infringement positions.

The plain meaning of the terms is consistent with how descriptors are used in the claims and specification, providing information to the DMA controller to, *e.g.*, identify and fetch data.

'084 Patent	'694 Patent
10. An apparatus, comprising: an embedded system configured to release components of the embedded system from reset; wherein the embedded system comprises a power-on reset (POR) sequencer configured to detect a (POR) sequencer descriptor in a nonvolatile memory, [...] wherein the POR sequencer descriptor comprises information to initialize configuration registers of the embedded system, <u>Direct Memory Access (DMA) descriptors used to fetch other POR sequencer descriptor fragments</u>, and a system firmware; [...] 15. The apparatus of claim 10, wherein the components comprises a processor bus, a reset controller, <u>a direct memory access (DMA) controller</u>, a storage device controller, a RAM controller, nonvolatile memory controller, and a POR sequencer.	1. An apparatus, comprising: an embedded system comprising one or more processors, a reset controller, a storage device controller, <u>one or more direct memory access (DMA) controllers</u>, a random access memory (RAM) and a memory controller, a nonvolatile memory and a nonvolatile memory controller, a debug interface, and a power-on reset (POR) sequencer configured to detect, in the nonvolatile memory, a descriptor used in a boot process and configured to copy the descriptor from the nonvolatile memory to the RAM, [...] wherein the POR sequencer descriptor includes register information and <u>DMA controller descriptors</u>, and wherein the POR sequencer reads and uses the register information to update configuration registers of the embedded system. 3. The apparatus of claim 1, wherein the POR sequencer loads <u>DMA descriptors</u> to the DMA controllers.

See '084 Patent, Cls. 1, 6, 10, 15, 19; '694 Patent, Claims 1, 3-4, 6, 8, 10, 12-13; Foty Decl. ¶¶ 17-18. The specification discloses, for example, an apparatus comprising “at least one direct memory access (DMA) controller which initiates and tracks data transfers”, where “[t]he POR Sequencer descriptor contains ... direct memory access (DMA) controller descriptors,” and “[t]he DMA descriptors are loaded ... to the DMA controllers of the system.” '084 Patent, 2:40-60, 4:52-53, 5:3-23, 6:1-8. The specification does not specify a particular format for descriptors. *See, e.g., id.*, 2:52-54, 2:61-65 (“not limited to a single data structure”); Ex. 16 (Alpert Dep. Tr. (rough)) at 23:6-24:7, 32:22-33:25. It does, however, describe in detail the use of descriptors in the claimed system. *See, e.g.*, '084 Patent, 3:28-60, 7:19-8:24, Figs. 7-8; Foty Decl. ¶ 19.

Intel has not, and cannot, overcome the “heavy presumption” that this term carries its plain

and ordinary meaning, much less justify importing Intel’s litigation-driven limitations—requiring a specific “byte count,” or that **every** descriptor have **both** a source and destination address. *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005). Those limitations do not appear in the specification at all. See ’084 Patent; Foty Decl. ¶ 21; Ex. 16 at 25:5-22.¹¹ Intel’s argument relies instead entirely on selectively curated extrinsic evidence in the form of a declaration from its expert, Dr. Alpert. Defs. Br. at 31-32. But Intel has not provided any reason for the Court to resort to extrinsic evidence.

And anyway, Dr. Alpert fails to support the proposed constructions. For example, even if a length parameter were always called for—setting aside cases where the transfer length is fixed and thus need not be specified in the data structure—there is no support for limiting to a “byte count.” Foty Decl. ¶ 22. Indeed, Dr. Alpert agreed the length could be a word count or double-word count (46:3-47:21), a sector count (48:15-24, 49:20-50:6), a variable-sized chunk count (98:20-99:4), or even just an arbitrary “size” or “length” (50:7-15). Ex. 16. Only jury confusion could arise from specifying a count, “byte” or otherwise, here.

Similarly, Dr. Alpert fails to show why the claims should be limited such that **every** descriptor must have **both** a source and destination address. For example, he agreed that in many situations, one side of the transfer always goes to/from the same fixed place. Ex. 16 at 26:14-30:2 (always to same port), 38:8-39:6 (always start at first word), 51:21-53:23 (fixed FIFO location). This makes specifying an address in the descriptor practically redundant. Indeed, his own extrinsic evidence citations give an example where “we specify **either** the source or the destination, depending on the direction of the transfer.” Alpert Decl., Ex. D at 218 (emphasis added); Ex. 16 at 54:4-55:6, 59:6-60:23. And BiTMICRO’s expert, Dr. Foty, confirms that DMA descriptors do not need to include both a “source address” and a “destination address.” Foty Decl. ¶¶ 23-25.

Dr. Alpert was shown other extrinsic examples **from Intel’s own use of DMA descriptors**:

¹¹ Dr. Alpert mentions a cited “related art” reference that mentions “source and target device addresses and an initial transfer length.” Alpert Decl. ¶18. But there is no reason given, and it would be error, to limit claims to this one example indirectly referenced in the specification—the famous “cardinal sin” of claim construction. *Phillips*, 415 F.3d at 1320.

where *one address was always set to zero* (Ex. 16 at 62:1-64:20, 68:20-69:6; Ex. 17 (Intel Embedded Peripherals IP User Guide) at 27, 421-422, 453); [REDACTED]

[REDACTED] Dr. Alpert disclaimed understanding or opinion about these examples from Intel's use. Ex. 16 at 85:4, 88:1-7; 105:2-109:13. But his willingness to opine about extrinsic examples that support Intel's improper limitation but not examples that contradict it merely highlights why resort to such evidence is disfavored—when, as here, there is an acknowledged plain meaning consistent with the claims and descriptions of the patents.

VII. CONCLUSION

BiTMICRO respectfully requests that the Court adopt BiTMICRO's proposed constructions and decline Defendants' invitation to improperly limit the claims or invalidate them for indefiniteness.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a true and correct copy of the above and foregoing document, as well as the supporting declarations and exhibits cited therein, have been served on November 30, 2022 to all counsel of record by electronic means to the email addresses for all counsel of record.

/s/ Michael Flynn-O'Brien
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