AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:22-cv-335	3/30/2022	Western District of Texas

PLAINTIFF	DEFENDANT
BITMICRO LLC	INTEL CORPORATION

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,826,243	11/2/2010	BITMICRO LLC
2	9,135,190	9/15/2015	BITMICRO LLC
3	8,010,740	8/30/2011	BITMICRO LLC
4	9,858,084	1/2/2018	BITMICRO LLC
5	10,120,694	11/6/2018	BITMICRO LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgment issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

INTEL-1002
7,826,243

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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6:22-cv-335	3/30/2022	Western District of Texas

PLAINTIFF	DEFENDANT
BITMICRO LLC	INTEL CORPORATION

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
6	6,496,939	12/17/2002	BiTMICRO LLC
2			
3			
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
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DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	REQUEST ID
11/322,442	7826243	2825	148918

PAIR Correspondence Address/Fee Address Change

The following fields have been changed to Customer Number 183214 on 10/05/2021 via Private PAIR in view of the certification copied below that authorized the change.

- Maintenance Fee Address

The address for Customer Number 183214 is:
183214
Jackson Walker LLP
Bitmicro / Oyster Optics
100 CONGRESS AV
STE 1100
AUSTIN, TX 78701

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

An attorney or Agent of Record registered to practice before the Patent and Trademark Office who has been given power of attorney in this application

Signature:	/joseph p lally/
Name:	Joseph P. Lally
Registration Number:	38947

UNITED STATES PATENT AND TRADEMARK OFFICE

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AUSTIN, TX 78701

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

An attorney or Agent of Record registered to practice before the Patent and Trademark Office who has been given power of attorney in this application

Signature:	/joseph p lally/
Name:	Joseph P. Lally
Registration Number:	38947

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY.DOCKET NO./TITLE	REQUEST ID
11/322,442	12/29/2005	Rey Bruce	150962.00011	148545

Acknowledgement of Loss of Entitlement to Entity Status Discount

The entity status change request below filed through Private PAIR on 09/27/2021 has been accepted.

CERTIFICATIONS:

Change of Entity Status:

X Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be notification of loss of entitlement to small or micro entity status, as applicable.

This portion must be completed by the signatory or signatories making the entity status change in accordance with 37 CFR 1.4(d)(4).

Signature:	/joseph p lally/
Name:	Joseph P. Lally
Registration Number:	38947

Trials@uspto.gov
571-272-7822

Paper 32
Entered: June 25, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC. and SK HYNIX AMERICA INC.,
Petitioner,

v.

BITMICRO, LLC,
Patent Owner.

IPR2018-01410 and IPR2018-01411 (Patent 6,529,416 B2)
IPR2018-01545 (Patent 8,093,103 B2)
IPR2018-01720 (Patent 7,826,243 B2)[1]

Before KEN B. BARRETT, KRISTINA M. KALAN, and KEVIN C. TROCK, *Administrative Patent Judges*.

PER CURIAM.

ORDER
Termination of the Proceedings
35 U.S.C. § 317; 37 C.F.R. §§ 42.72, 42.74

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[1] This Order addresses issues that are the same in each of the above-identified proceedings. We exercise our discretion to issue one Order to be entered in each proceeding. The Parties are not authorized to use this joint heading and filing style in their papers.

Petitioner and Patent Owner (collectively, "the parties") have requested that the above-identified proceedings be terminated pursuant to a settlement. The Board authorized the parties to file a joint motion to terminate the above-identified proceedings on May 21, 2019.

On June 13, 2019, and pursuant to 35 U.S.C. § 317(a), the parties filed Joint Motions to Terminate each of these proceedings (collectively "Joint Motions to Terminate") (Paper 30[2]) and Joint Requests to file the settlement agreement as business confidential information and to be kept separate from the patent file pursuant to 35 U.S.C. § 317(b) and 37 C.F.R. § 42.74(c) (collectively "Joint Requests") (Paper 31[3]), along with a copy of the written settlement agreement in each proceeding (Ex. 1014[4]).

Under 35 U.S.C. § 317(a), "[a]n inter partes review instituted under this chapter shall be terminated with respect to any petitioner upon the joint request of the petitioner and the patent owner, unless the Office has decided the merits of the proceeding before the request for termination is filed." It is also provided in 35 U.S.C. § 317(a) that if no petitioner remains in the *inter partes* review, the Office may terminate the review.

Additionally, the Board expects that a proceeding will terminate after

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[2] For purposes of expediency, we cite to Papers filed in IPR2018-01410. Petitioner filed a similar Joint Motion to Terminate in IPR2018-01411 (Paper 30), IPR2018-01545 (Paper 20), and IPR2018-01720 (Paper 20).
[3] Petitioner filed similar Joint Requests in IPR2018-01411 (Paper 31), IPR2018-01545 (Paper 21), and IPR2018-01720 (Paper 21).
[4] For purposes of expediency, we cite to the copy of the written settlement agreement filed in IPR2018-01410. Petitioner also filed a copy of the written settlement agreement in each of IPR2018-01411 (Ex. 1108), IPR2018-01545 (Ex. 1034), and IPR2018-01720 (Ex. 1035).

the filing of a settlement agreement. *See, e.g.*, Office Patent Trial Practice Guide, 77 Fed. Reg. 48756, 48768 (Aug. 14, 2012). We instituted trial in each of the above-identified proceedings (IPR2018-01410, Paper 14 (dated January 23, 2019); IPR2018-01411, Paper 14 (dated January 23, 2019); IPR2018-01545, Paper 14 (dated March 7, 2019); and IPR2018-01720, Paper 14 (dated March 29, 2019)). Thus, each of the above-identified proceedings is a trial subject to termination under 37 C.F.R. § 42.72. *See* 37 C.F.R. § 42.72. We have not yet decided the merits of the above-identified proceedings, and final written decisions have not been entered in these proceedings. Notwithstanding that these proceedings have moved beyond the preliminary stage, the parties have shown adequately that the termination of these proceedings is appropriate. Under these circumstances, we determine that good cause exists to terminate these proceedings with respect to the parties.

The parties represent that Exhibit 1014 is a true copy of the settlement agreement between the parties. Paper 30, 3. The parties state "[t]his settlement agreement is the only agreement or understanding between SK Hynix [i.e., SK Hynix Inc. and SK Hynix America Inc.] and Patent Owner made in connection with, or in contemplation of dismissing SK Hynix." *Id.* at 1, 3. The parties represent that, pursuant to the settlement agreement, they have agreed to terminate not only the above-identified proceedings but also the underlying district court litigation between them (18-CV-03505 (N.D. Cal.)) and the underlying International Trade Commission investigation (ITC Inv. No. 337-TA-1097). *Id.* at 2–3.

Based on the facts of these proceedings, and in view of the parties'

Joint Motions to Terminate, we are persuaded that it is appropriate to terminate these proceedings with respect to both Petitioner and Patent Owner without rendering any further decisions. *See* 37 C.F.R. §§ 42.5(a), 42.72. Therefore, the Joint Motions to Terminate and the Joint Requests to treat the settlement agreement as business confidential information are *granted.*

This Order does not constitute a final written decision pursuant to 35 U.S.C. § 318(a).

Accordingly, it is

ORDERED that the Joint Requests that the settlement agreements (IPR2018-01410, Ex. 1014; IPR2018-01411, Ex. 1108; IPR2018-01545, Ex. 1034; and IPR2018-01720, Ex. 1035) be treated as business confidential information and be kept separate from the files of the above-identified proceedings and from the files of the involved patents under the provisions of 35 U.S.C. § 317(b) and 37 C.F.R. § 42.74(c), are *granted*;

FURTHER ORDERED that the Joint Motions to Terminate the above-identified proceedings are *granted*; and

FURTHER ORDERED that the above-identified proceedings are *terminated* with respect to both Petitioner and Patent Owner pursuant to 35 U.S.C. § 317(a) and 37 C.F.R. § 42.72.

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Paper No. 14
Entered: March 29, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., SK HYNIX INC, and SK HYNIX AMERICA INC.,
Petitioner,

v.

BITMICRO, LLC,
Patent Owner.

Case IPR2018-01720
Patent 7,826,243 B2

Before KEN B. BARRETT, KRISTINA M. KALAN, and KEVIN C. TROCK, *Administrative Patent Judges*.

TROCK, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background

Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., SK Hynix America Inc., and SK Hynix Inc. (collectively, "Petitioner") filed a Petition requesting an *inter partes* review of claims 1, 2, 11, and 12 ("the challenged claims") of U.S. Patent No. 7,826,243 B2 (Ex. 1001, "the '243 patent"). Paper 6 ("Pet."). BiTMICRO, LLC ("Patent Owner") filed a Preliminary Response to the Petition. Paper 10 ("Prelim. Resp."). Petitioner, with Board authorization, filed a Reply. Paper 11 ("Reply"). Patent Owner, with Board authorization, filed a Sur-Reply. Paper 13 ("Sur-Reply").

We have jurisdiction under 35 U.S.C. § 314, which provides that an *inter partes* review may not be instituted "unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). Upon consideration of the Petition, the Preliminary Response, Reply, Sur-Reply, and the evidence of record, we determine that Petitioner has shown a reasonable likelihood that it would prevail in showing the unpatentability of at least one of the challenged claims. Accordingly, we institute an *inter partes* review.

B. Related Proceedings

The parties identify the following proceedings as related to the '243 patent: *Samsung Semiconductor, Inc. v. BiTMICRO, LLC*, Case No. 3-18-cv-03502 (N.D. Cal.); *SK Hynix Inc. v. BiTMICRO, LLC*, Case No. 3-18-cv-03505 (N.D. Cal.); *Certain Solid State Storage Drives, Stacked Electronics Components, and Products Containing Same*, Inv. No. 337-TA-1097 (ITC); IPR2018-01410; IPR2018-01411; and IPR2018-01545. Pet. 1; Paper 8, 2–3.

C. The '243 Patent (Ex. 1001)

The '243 patent, titled *Multiple Chip Module And Package Stacking For Storage Devices*, relates to computer systems using flash memory based semiconductor disk drives and "a method of using multiple chip module (MCM) and Package Stacking technique to support miniaturization and memory scalability." Ex. 1001, 1:9–12. The '243 patent states that semiconductor disk drives "typically use separate packages for the interface controller, the DMA controller, the processor and separate packages for the Flash devices, the FPROMs and the RAMs." *Id.* at 1:14–17. This method, the '243 patent contends, "limits the miniaturization of the entire storage device." *Id.* at 1:18–20. Stacking both on the chip module and the package level, the '243 patent contends, "maximizes the capacity in a limited area, thus realizing the move to miniaturize of the entire storage device." *Id.* at 1:21–24. The '243 patent describes a method where the semiconductor dies (e.g., flash devices) are mounted in a module and then "stacked to create the desired memory capacity," and "different packages are stacked to create desired function." *Id.* at 1:47–49. The '243 patent contends that "[a] wide range of capacity can be configured through variation of die capacities and stacking modules and/or packages." *Id.* at 1:65–67.

Figure 1a from the '243 patent, shown below, depicts a block diagram of a flash storage system.

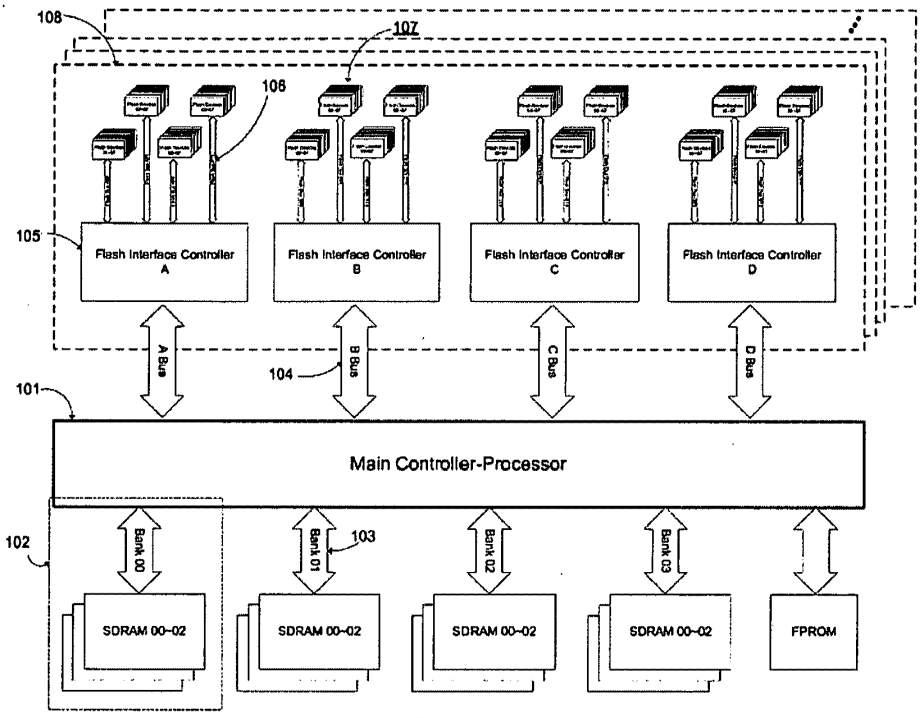


Figure 1a

Figure 1a, shown above, illustrates a block diagram of a stackable system for high performance, high capacity devices according to an embodiment of the '243 patent. *Id.* at 2:17–19.

D. Challenged Claims

Claim 1 is independent. Claims 2, 11, and 12 are dependent claims. Annotated claim 1 is shown below:

1. [1a] A stacked module comprising a plurality of modules each comprising:
[1b] one or more active ports for carrying one or more active signal;
[1c] one or more passive ports for passing through the one or more active signals;
[1d] a first serial chain route that includes at least one serial chain connection, the serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output, said serial

chain input coupled to said serial chain output through said serial chain circuit;

[1e] a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module; and

[1f] said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module.

Ex. 1101, 10:42–60 (bracketed annotations added).

E. Relevant References

Petitioner relies upon the following prior art references:

(1) International Patent Application No. WO 2004/072667, published Aug. 26, 2004 ("Sato") (Ex. 1004);

(2) U.S. Patent No. 6,236,115, issued May 22, 2001 ("Gaynes") (Ex. 1005);

(3) U.S. Patent No. 5,612,570, issued Mar. 18, 1997 ("Eide") (Ex. 1006);

(4) U.S. Patent Application Publication No. 2003/0178228, published Sept. 25, 2003 ("Sung") (Ex. 1007); and

(5) U.S. Patent Application Publication No. 2004/0257847, published Apr. 21, 2004 ("Matsui") (Ex. 1011). Pet. 3.

F. Asserted Grounds of Unpatentability

Ground	Reference(s)	Basis	Claims Challenged
1	Sato	§ 103	1, 2, 11, 12
2	Sato and Gaynes	§ 103	1, 2, 11, 12

Ground	Reference(s)	Basis	Claims Challenged
3	Sato and Eide	§ 103	1, 2, 11, 12
4	Sung	§ 103	1, 2, 11, 12
5	Sung and Matsui	§ 103	1, 2, 11, 12

II. ANALYSIS

A. Level of Ordinary Skill

In determining whether an invention would have been obvious at the time it was made, we consider the level of ordinary skill in the pertinent art at the time of the invention. *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). "The importance of resolving the level of ordinary skill in the art lies in the necessity of maintaining objectivity in the obviousness inquiry." *Ryko Mfg. Co. v. Nu-Star, Inc.*; 950 F.2d 714, 718 (Fed. Cir. 1991).

Petitioner asserts that a person of ordinary skill in the art at the time of the invention would have had at least a bachelor's degree in electrical engineering or a similar field, and at least two to three years of experience in the fields of memory stacking and integrated circuits. Pet. 7 (citing Ex. 1002 ¶¶ 33–37). Patent Owner does not provide any view as to the level of ordinary skill in the art. *See generally* Prelim. Resp.

For purposes of this decision, and based on the preliminary record before us, we adopt Petitioner's assessment of the level of ordinary skill in the art.

B. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are interpreted according to their broadest reasonable constructions in light of the specification of the patent in which they appear. *See* 37 C.F.R.

§ 42.100(b) (2018);[1] *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2142 (2016). Under the broadest reasonable construction standard, claim terms are presumed to have their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017); *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

With respect to claim construction, Petitioner states "[n]o terms need to be construed." Pet. 4. Patent Owner does not propose construction for any claim terms. *See generally* Prelim. Resp. For purposes of this decision, we determine that no claim terms require an explicit construction at this time.

C. Prior Art

i. Sato (Ex. 1004)

Sato relates to a boundary scan controller that allows a boundary scan to be executed and also allows a semiconductor device to be manufactured in such a manner that the same type of semiconductor circuit chips are

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[1] Because the Petition was filed before November 13, 2018, the revised claim construction standard for interpreting claims in *inter partes* review proceedings as set forth in the final rule published October 11, 2018 does not apply to this proceeding. Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51340 (Oct. 11, 2018) (to be codified at 37 C.F.R. pt. 42) (stating the new "rule is effective on November 13, 2018 and applies to all IPR, PGR and CBM petitions filed on or after the effective date").

stacked. Ex. 1004, 2. Sato describes a boundary scan controller for testing connection states of input/output terminals of a plurality of semiconductor circuit chips, which constitute a semiconductor device. *Id.* at 4. Sato explains that, as demand for high density packaging of semiconductor circuit chips has increased, it has been proposed to enhance packaging by stacking semiconductor circuit chips. *Id.* Sato further explains that in a semiconductor device for achieving high density packaging, there are mounted circuits for electrically testing whether or not the packaged chips are connected, that is, boundary scan controllers. *Id.* at 7.

Sato explains that boundary scan controllers include five signal lines; DI (Test Data Input), TDO (Test Data Output), TCK (Test Clock input), TMS (Test Mode Select input), and TSRT (Test Reset input). *Id.* at 7. Sato explains that in a boundary scan that conforms to the standards of JTAG (Joint European Test Action Group), the signal lines TDI and TDO of the boundary scan controller incorporated in the individual chips in the semiconductor device are connected in the shape of a chain, i.e. a "daisy-chain." *Id.*

Figure 3 from Sato, shown below, depicts a block diagram of a semiconductor device.

FIG. 3

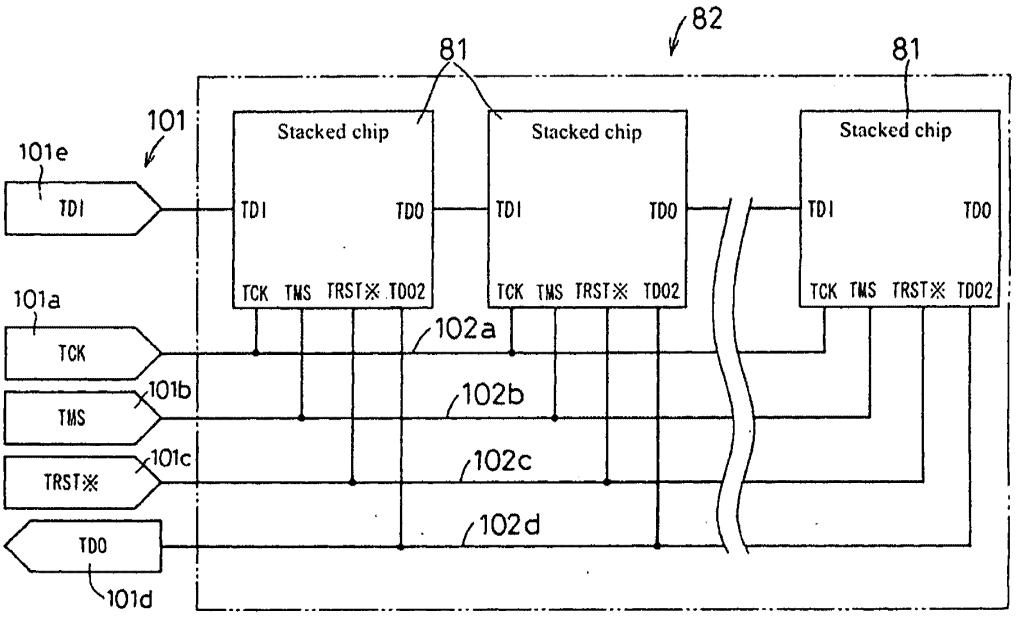


Figure 3, shown above, illustrates the signal lines of a semiconductor device configured by stacking a plurality of semiconductor circuit chip assemblies. *Id.* at 15, 45.

ii. Sung (Ex. 1007)

Sung relates to a three-dimensional stacked integrated circuit system in which every layer of the stack is identical. Ex. 1007, Abstract. Sung's stacking methods can "increase processing power, chip integration, operating speed and data storage density in the same planar area while minimizing global interconnect lengths." *Id.* ¶ 6. The layers of Sung's "three-dimensional stack" communicate using connectors having "vertical conductors" and "terminators" connected by "conditional connection[s]" designed to be "aligned with the necessary offset, d, and then fused together." *Id.* ¶¶ 25, 44.

Figure 3 of Sung, shown below, depicts a staggered die offset alignment.

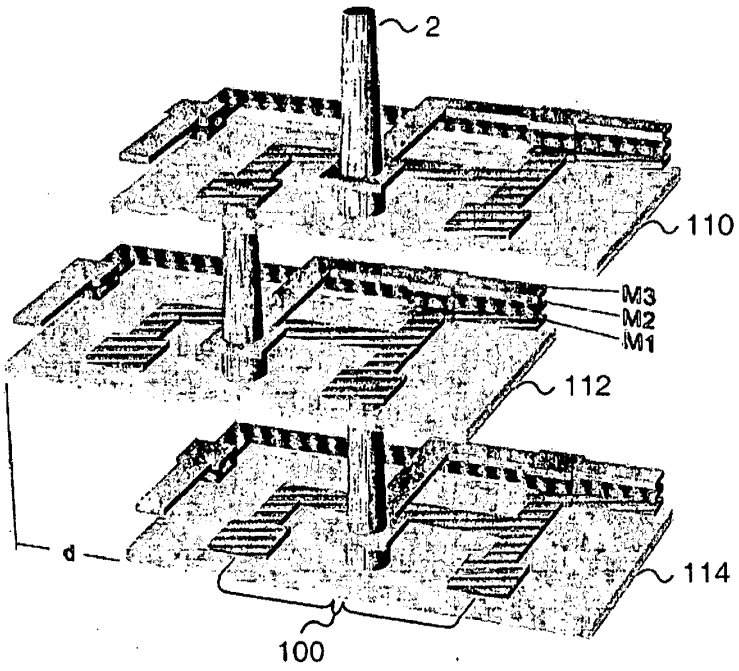


Figure 3 of Sung, shown above, illustrates how a die connector can be used to form connections between dies, where alternating dies are offset. Ex. 1007 ¶ 30.

Sung also describes circuits for "defin[ing] a communications boundary in a vertical stack." *Id.* ¶ 20. Each layer of the stack includes tristate buffers that are controlled by "top and bottom die identifier circuits" designed to determine whether the layer is the top or bottom layer in the stack, and to enable or disable the tristate buffers to route data so that it does not flow past the stack. *Id.* ¶¶ 32, 49.

D. Asserted Obviousness Based on Sato (Ground 1)

Petitioner asserts claims 1, 2, 11, and 12 of the '243 patent are unpatentable as obvious under 35 U.S.C. § 103 over Sato. Pet. 11–32.

Petitioner argues that Sato teaches [1a] a stacked device containing a plurality of memory modules, because Sato describes the "semiconductor circuit chips are stacked" and "the semiconductor circuit chip is a memory chip." Pet. 11 (quoting Ex. 1004, Abstract, 10:29–11:10). Petitioner points to Sato's Figure 3, shown *supra*, depicting a two dimensional block diagram of stacked modules. *Id.* at 11–12.

Petitioner argues Sato teaches [1b] one or more active ports for carrying one or more active signals (connection terminals TDO 86A, TDI 83A, TDO2 89A, and TCK 83A as shown in annotated Figures 2, 5 below). *Id.* at 13–14.

FIG. 2

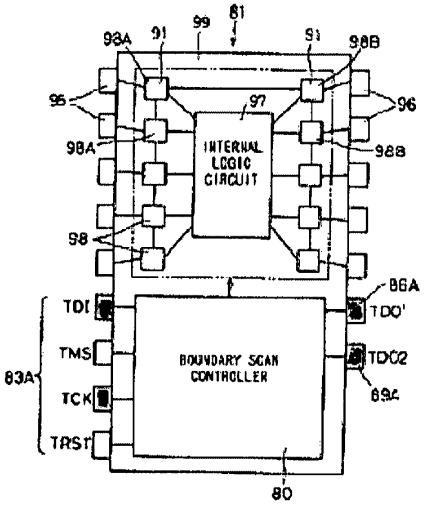
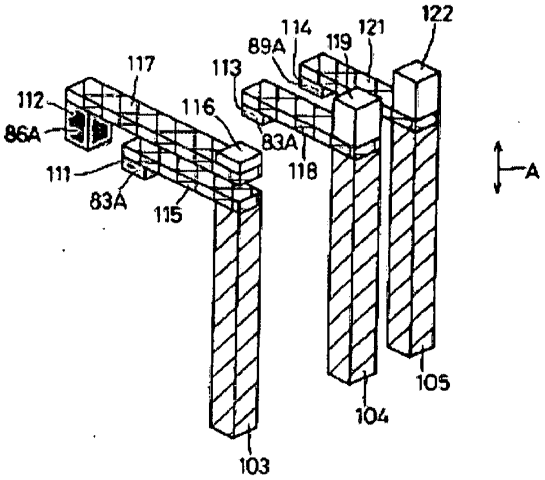


FIG. 5



Petitioner's annotated Figure 2, shown above, is a block diagram illustrating a semiconductor circuit chip assembly. Petitioner's annotated

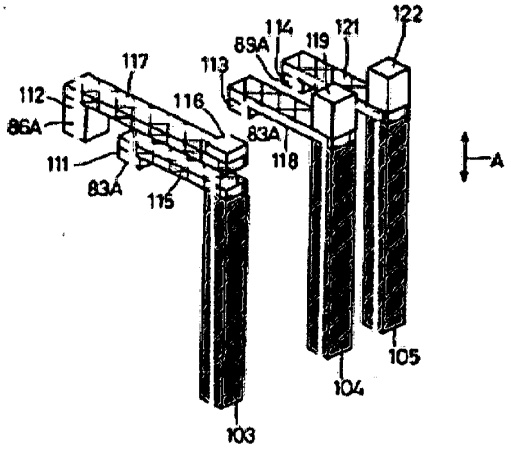
Figure 5, shown above, is a perspective view illustrating part of the wiring pattern of a semiconductor circuit chip assembly. Ex. 1004, 75.

Petitioner argues the connection terminals are active ports, because they are electrical connections that carry active signals (TDO, TDO2, TDI, and TCK). Pet. 14. Petitioner argues signals TDO, TDO2, TDI, and TCK are active signals because they are transmitted digital signals that carry information. *Id.* at 15.

Petitioner argues Sato teaches [1c] one or more passive ports for passing through one or more active signals, because Sato describes at least three passive ports on each module, penetrating electrodes 103–105, that pass the active signals (e.g. TDI/TDO, TDO2, and TCK) from one surface of a memory module to the other. Pet. 15. Petitioner argues the penetrating electrodes, shown below in red on annotated Figure 5, are passive ports because they are vertical electronic connections that pass an active signal through the memory module from one surface to another. *Id.* at 17.

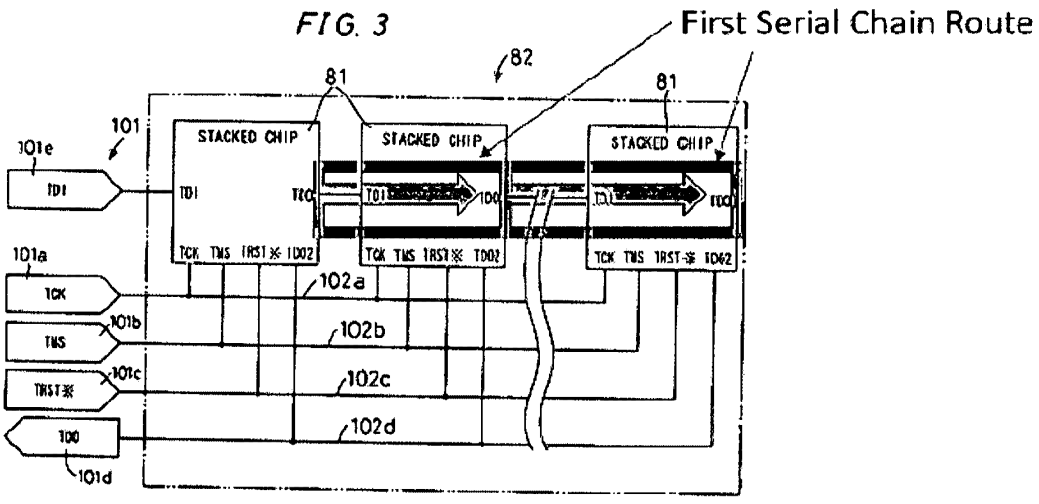
Petitioner's annotated Figure 5 from Sato is shown below.

FIG. 5



Petitioner's annotated Figure 5, shown above, is a perspective view illustrating part of the wiring pattern of a semiconductor circuit chip assembly.

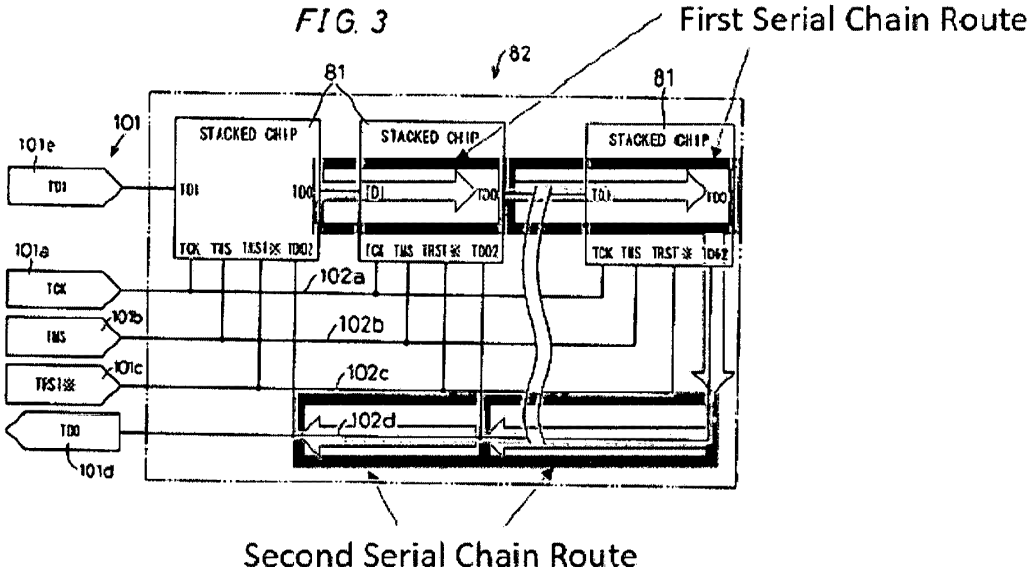
Petitioner argues Sato teaches [1d] a first serial chain route that includes at least one serial chain connection, the serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output; said serial chain input coupled to said serial chain output through said serial chain circuit, because Sato describes serial connections among memory modules to form a "daisy chain," which allows all the memory modules to be "simultaneously subjected" to a JTAG boundary scan test. *Id.* Petitioner argues the daisy chain is "the signal lines TDI and TDO of the boundary scan controller ... [that] are connected in the shape of a chain," as depicted in annotated Figure 3 below. *Id.* at 17–18.



Petitioner's annotated Figure 3, shown above, illustrates the signal lines of a semiconductor device configured by stacking a plurality of semiconductor circuit chip assemblies.

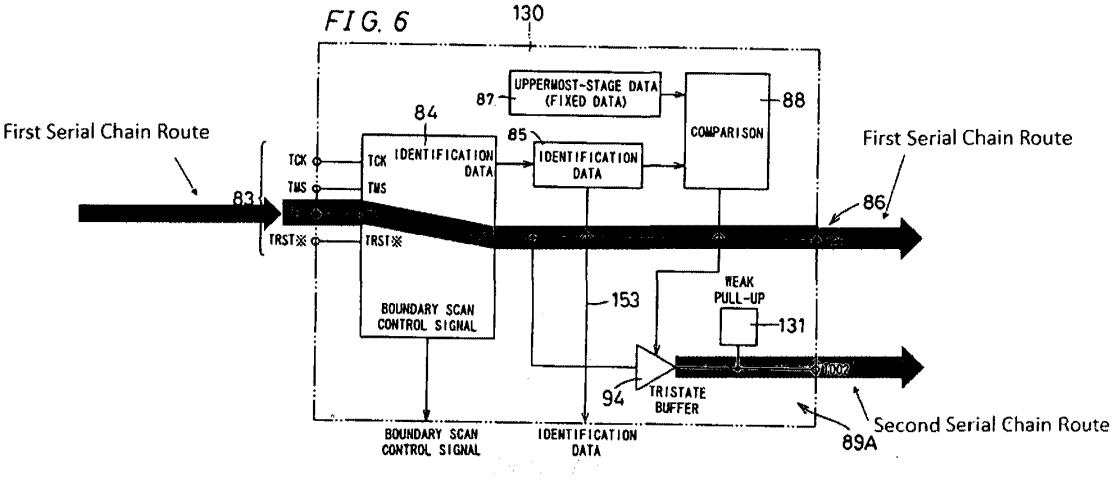
Petitioner argues Sato's connections between stacked memory modules are the claimed serial chain connections because "a first serial chain route, which includes at least one serial chain connection, is formed in each module when the memory modules are stacked. Multiple serial chain connections that are connected in series can also be considered the first serial chain route." *Id.* at 18.

Petitioner argues Sato teaches [1e] a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module, because Sato shows TDO2 signal being routed across each module connected in series, as depicted below in Petitioner's annotated Figure 3, below. *Id.* at 21.



Petitioner's annotated Figure 3, shown above, illustrates the signal lines of a semiconductor device configured by stacking a plurality of semiconductor circuit chip assemblies. Petitioner argues connection terminal 89A and connection line 121 in each module are (individually or collectively) a serial chain input because they receive the TDO2 signal. *Id.*

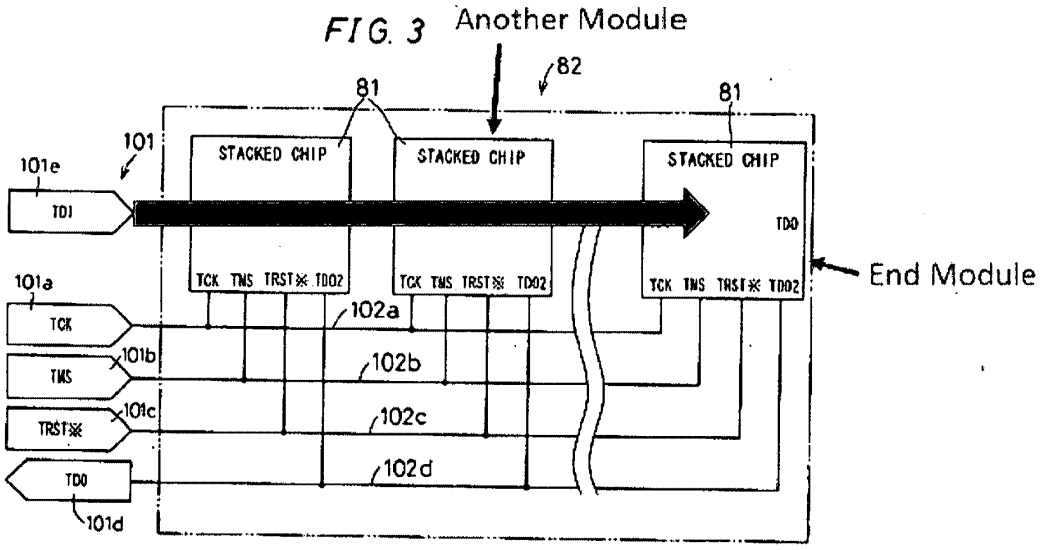
at 22. Petitioner argues that when the memory modules are stacked, at least one of these serial chain connections forms a second serial chain route in each module. *Id.* at 23. Petitioner argues that Sato's control circuitry (tri-state buffer 94 and comparison means 88) in each stacked memory module that can enable a routing path that connects the first serial chain route with the second serial chain route, as shown below in annotated Figure 6. *Id.* at 24–25.



Petitioner's annotated Figure 6, above, is a block diagram illustrating a boundary scan controller. Petitioner argues Sato's routing path is enabled by a control circuit: tri-state buffer 94 and comparison means 88. *Id.* at 25.

Petitioner argues Sato teaches [1f] the control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module, because Sato explains that the tri-state buffer 94 and comparison means 88 enable the routing path by comparing a control input signal (identification data 85) to uppermost-stage data 87. *Id.* at 26. Petitioner explains that the end module's control circuit receives identification data 85 from the penultimate memory module—"another

module"— because identification data 85 is sent over the daisy chain route from JTAG tester connector pins 101, as shown in annotated Figure 3 below. *Id.*



Petitioner's annotated Figure 3, shown above, illustrates the signal lines of a semiconductor device configured by stacking a plurality of semiconductor circuit chip assemblies.

Petitioner presents arguments that the limitations of dependent claims 2, 11, and 12 challenged in this ground are taught by Sato, and presents evidence supporting the same. *Id.* at 27–32.

In discussing certain claim limitations, Petitioner asserts it would have been obvious to one of ordinary skill to understand the disclosures of Sato in a particular manner. For example, Petitioner argues that one of ordinary skill in the art would have understood that each of Sato's "terminals" is a contact pad made from a conductive material. *Id.* at 14 (citing Ex. 1002 ¶¶ 98–100). Petitioner also argues a person of ordinary skill would have understood that Sato's connection terminals are pads that would necessarily be connected to the penetrating electrode of an adjacent module by

conductive material (i.e., a solder ball). *Id.* at 17 n.4 (citing Ex. 1002, ¶¶ 107–109.)

As described above, Petitioner presents arguments that the limitations of the challenged claims are taught by Sato and presents evidence supporting the same. Petitioner relies on the testimony of Dr. R. Jacob Baker to support its contentions. *See* Ex. 1002, 45–79. Dr. Baker testifies, for example, what a person of ordinary skill in the art would have understood about Sato's teachings. *See, e.g.*, Ex. 1002 ¶¶ 92–93, 96–98. At this stage in the proceeding, we credit Dr. Baker's testimony in support of Petitioner's arguments.

Patent Owner does not present any arguments directed to the merits of Petitioner's obviousness position. *See generally* Prelim. Resp. Rather, Patent Owner focuses its Preliminary Response on arguments that we discuss in more detail below.

Based on this preliminary record, we are persuaded that Petitioner has demonstrated a reasonable likelihood that it would prevail in showing that claims 1, 2, 11, and 12 are obvious over Sato.

E. Asserted Obviousness Based on Sato, Gaynes, Eide, Sung, and Matsui (Grounds 2, 3, 5)

Petitioner asserts claims 1, 2, 11, and 12 of the '243 patent are obvious over the combination of Sato and Gaynes (Ground 2) and Sato and Eide (Ground 3). Pet. 32–56.

With respect to Ground 2, Petitioner states, "Patent Owner may argue that the claimed "active port" or "passive port" requires the particular ball and pad structures described in the '243 specification (e.g., Ex. 1001, 9:8). Pet. 32.

With respect to Ground 3, Petitioner states, "Patent Owner may argue that the claimed 'module' is limited to a semiconductor chip mounted on a PCB substrate." Pet. 43.

With respect to Ground 5, Petitioner argues, "to the extent that Patent Owner argues the claimed plurality of modules must be SDRAM modules, Sung, in view of Matsui, renders obvious a stacked module comprising a plurality of SDRAM modules." Pet. 87.

Patent Owner has not yet responded substantively to Petitioner's assertions of obviousness regarding the combinations of Sato and Gaynes (Ground 2), Sato and Eide (Ground 3), and Sung and Matsui (Ground 5). Because Petitioner makes these assertions of obviousness to address what Patent Owner *may* argue, we consider it premature for us to address Petitioner's arguments at this point in the proceeding. Accordingly, we defer our analysis of Grounds 2, 3, and 5 until such time as Patent Owner raises the arguments Petitioner anticipates.

F. Asserted Obviousness Based on Sung (Ground 4)

Petitioner asserts claims 1, 2, 11, and 12 of the '243 patent are unpatentable as obvious under 35 U.S.C. § 103 over Sung. Pet. 56–87.

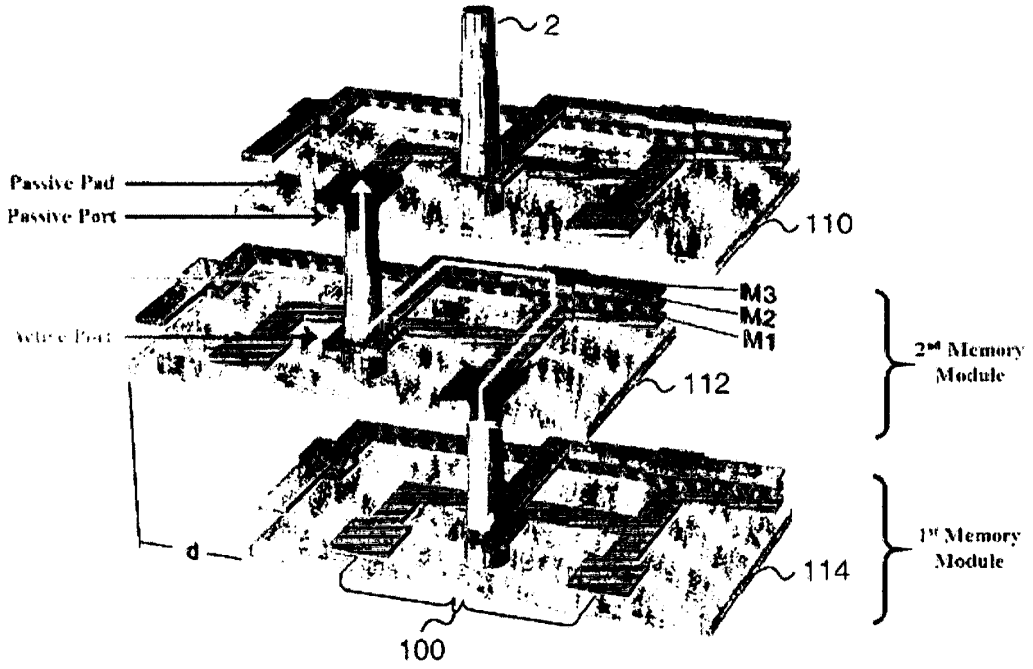
Petitioner argues Sung teaches [1a] a stacked module comprising a plurality of modules, because Sung teaches "methods and circuits" for constructing "three-dimensional integrated circuit systems" that include "layers" of "stacked multi-chip modules," and that Sung's "three-dimensional stack" applies to "stacks of dies" as well as "stacked multi-chip modules." *Id.* at 56–57.

Petitioner also argues that one of ordinary skill in the art would have understood that Sung contemplates using memory modules in its three-

dimensional stacked integrated circuit. *Id.* at 57 (citing Ex. 1002 ¶¶ 72–80, 237–245).

With respect to limitation [1b], one or more active ports for carrying one or more active signal, Petitioner argues Sung teaches forming one or more active ports on each stacked memory module, such as the pads of conditional connection 104. *Id.* at 58. Petitioner argues conditional connection 104, which is present in each layer of the stack, is an active port because it is an electrical connection that broadcasts active signals, such as addr_in signal. *Id.* at 59.

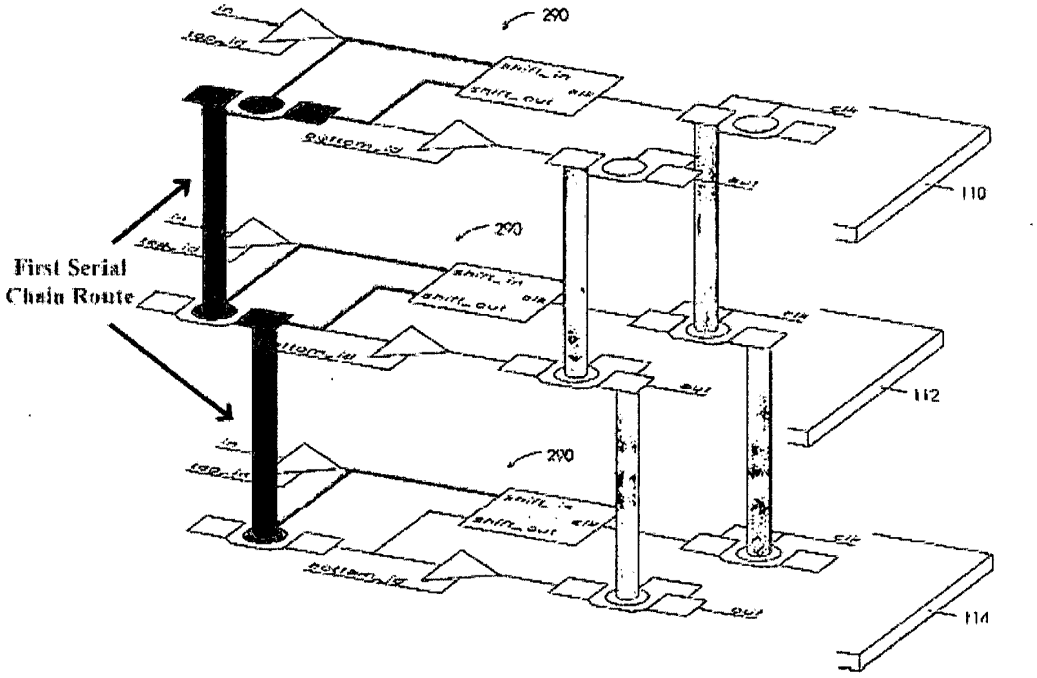
With respect to limitation [1c], one or more passive ports for passing through the one or more active signals, Petitioner argues Sung teaches that each module has passive ports—through vias—that pass through the active signals from one surface of a module to the other. *Id.* Petitioner argues Sung teaches that "a 'connector 100 with [a] vertical conductor 2' that includes a through via that passes 'through the thickness of a substrate' and is 'coupled 104 to its terminators 4.' The through via of the connector performs 'broadcasting' by passing through an active signal from a preceding layer to a next layer in the stack." *Id.* at 60. Petitioner argues a person of ordinary skill in the art would have understood "that the portion of the vertical conductor that is not formed within the aperture in the substrate is a passive ball," citing annotated Figure 3, below. *Id.*



Petitioner's annotated Figure 3, above, illustrates how the die connector can be used to form connections between dies. Ex. 1007 ¶ 30.

With respect to limitation [1d], a first serial chain route that includes at least one serial chain connection, the serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output; said serial chain input coupled to said serial chain output through said serial chain circuit, Petitioner argues Sung teaches that each module has a first serial chain route that includes at least one serial chain connection (connectors 100) and that Sung "describes an inter-die scan chain that accomplishes 'communication between multiple dies.'" Pet. 64 (quoting Ex. 1007 ¶ 49).

Petitioner argues that annotated Figure 10 of Sung, shown below, depicts an "inter-die scan chain 290 across three dies 110, 112, and 114," although the inter-die scan chain could extend across any number of layers. *Id.*



Petitioner's annotated Figure 10, shown above, illustrates how a circuit appears in a stack of identical dies. Ex. 1007 ¶ 37. Petitioner argues, "[t]he inter-die scan chain portion that extends across each module and includes connector 100 is the claimed first serial chain route of that module." *Id.* at 65. Petitioner explains, "[w]hen a signal travels down the stack, ball portions of the vertical conductors 2 receive a signal from the module above, and terminator 4 pads provide the signal to the module below." *Id.* at 66.

With respect to limitation [1e], a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module," Petitioner argues Sung's modules each have a serial chain connection (connectors 100), where at least one of those serial chain connections in each module further form a second serial chain route—a part of the broadcasting circuit 250 in each module. Petitioner argues, "[a person of ordinary skill in the art]

would have understood that the connector of each module forming the broadcasting circuit depicted at [annotated] Figure 10, [shown below] or multiple connectors that together form the broadcasting circuit, is a second serial chain route formed by other serially connected connectors." *Id.* at 71.

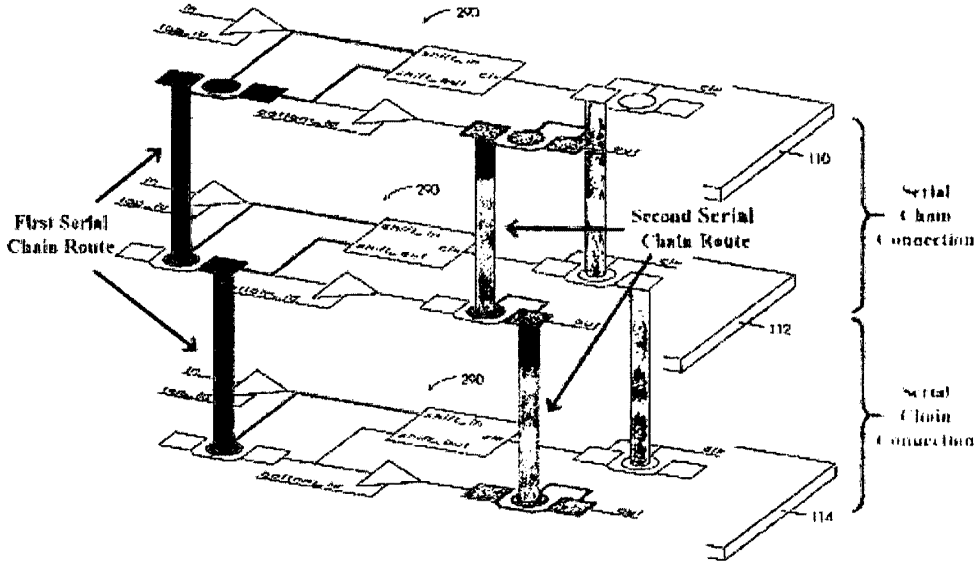


Figure 10: Inter-die communications chain for multiple dies.

Petitioner's annotated Figure 10, shown above, illustrates inter-die communications chain for multiple dies. Petitioner also argues Sung teaches a control circuit (die identifier circuit 230 and tristate buffer 296) for enabling the claimed routing path, where a "bottom_id" signal is generated at the die identifier circuit in the bottom module. *Id.* at 73. Petitioner explains, "the die identifier circuit and tristate buffer in the bottom die enables a routing path between the first serial chain route and the second serial chain route." *Id.* at 74.

With respect to limitation [1f], control circuit is disposed to enable said routing path in response to a control input signal received from another module from the plurality of modules when said end module is coupled to

said another module, Petitioner argues Sung teaches a control circuit (die identifier circuit 230 and tristate buffer 296) that enables a routing path connecting first and second serial chain routes in an end module, where the control circuit is disposed to enable the routing path in response to a control input signal received from another module when the end module is coupled to the other module. *Id.* at 76. Petitioner argues Sung's "tristate buffer 296" has a control line that tri-states the input when pulled low to disable a routing path between the first and second serial chain routes, and to enable the routing path when pulled high. *Id.*

Petitioner presents arguments that the limitations of dependent claims 2, 11, and 12 are taught by Sung, and presents evidence supporting the same. *Id.* at 80–87.

In discussing certain claim limitations, Petitioner asserts it would have been obvious to one of ordinary skill to understand the disclosures of Sung in a particular manner. For example, Petitioner argues a person of ordinary skill in the art would have understood that Sung contemplates using memory modules in its three-dimensional stacked integrated circuit. Pet. 57 (citing Ex. 1002, ¶¶ 72-80, 237-245). Petitioner relies on the testimony of Dr. Baker to support its contentions, and at this stage in the proceeding, we credit his testimony in support of Petitioner's arguments.

Patent Owner does not present any arguments directed to the merits of Petitioner's obviousness position. *See generally* Prelim. Resp. Rather, Patent Owner focuses its Preliminary Response on arguments that we discuss in more detail below.

Based on this preliminary record, we are persuaded that Petitioner has demonstrated a reasonable likelihood that it would prevail in showing that claims 1, 2, 11, and 12 are obvious over Sung.

G. Discretionary Denial of Institution

The Board has discretion to decline to institute an *inter partes* review. *See* 35 U.S.C. § 314(a) (authorizing institution of an *inter partes* review under particular circumstances, but not requiring institution under any circumstances); 37 C.F.R. § 42.108(a) (stating "the Board may authorize the review to proceed"); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (explaining that under § 314(a), "the PTO is permitted, but never compelled, to institute an IPR proceeding"). Patent Owner contends that we should exercise our discretion and not institute trial in this proceeding. Prelim. Resp. 3–14; Sur-Reply 1–3. Petitioner disagrees. Reply 1–4.

Patent Owner encourages us to exercise our discretion under § 314(a) "because institution will not be an efficient use of judicial or private resources." Prelim. Resp. 4. More particularly, Patent Owner argues that the Board should exercise its discretion to deny institution in view of the timing and scope of Petitioner's invalidity challenge before the International Trade Commission ("ITC"). *Id.* Patent Owner compares the events and dates in the related ITC case's procedural schedule against hypothetical corresponding events in an instituted IPR proceeding in this case to argue that, by the time a final decision would issue in an instituted IPR, "redundant work will have already been done at the ITC, as corresponding due dates at the ITC will have occurred well before dates in this IPR for similar activities." *Id.* at 5.

Patent Owner also argues that the factors enumerated in *General Plastic* weigh in favor of denial of institution. *Id.* at 6–14. In *General Plastic*, the Board set forth non-exhaustive factors that the Board would consider in exercising discretion on instituting *inter partes* review,

especially as to "follow-on" petitions challenging the same patent as challenged previously in an *inter partes* review. *General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha,* Case IPR2016-01357, slip op. at 16 (PTAB Sept. 6, 2017) (Paper 19) (§ II.B.4.i precedential); *see* Office Trial Practice Guide, August 2018 Update, 83 Fed. Reg. 39989 (Aug. 13, 2018) (Notice of update) ("Trial Practice Guide Update") (August 2018), 9–10 (Considerations in Instituting a Review (discussing *General Plastic*)). The non-exhaustive *General Plastic* factors are

> 1. whether the same petitioner previously filed a petition directed to the same claims of the same patent;
> 2. whether at the time of filing of the first petition the petitioner knew of the prior art asserted in the second petition or should have known of it;
> 3. whether at the time of filing of the second petition the petitioner already received the patent owner's preliminary response to the first petition or received the Board's decision on whether to institute review in the first petition;
> 4. the length of time that elapsed between the time the petitioner learned of the prior art asserted in the second petition and the filing of the second petition;
> 5. whether the petitioner provides adequate explanation for the time elapsed between the filings of multiple petitions directed to the same claims of the same patent;
> 6. the finite resources of the Board; and
> 7. the requirement under 35 U.S.C. § 316(a)(11) to issue a final determination not later than 1 year after the date on which the Director notices institution of review.

General Plastic, slip op. at 9–10; *see also NVIDIA Corp. v. Samsung Elec. Co.*, Case IPR2016-00134 (PTAB May 4, 2016) (Paper 9) (cited by *General Plastic*). As the Trial Practice Guide explains, the *General Plastic* factors are not dispositive, but are part of a balanced assessment of the relevant circumstances in a particular case. Trial Practice Guide Update 10.

Patent Owner also directs us to the portion of the Trial Practice Guide Update that provides:

> There may be other reasons besides the "follow-on" petition context where the "effect . . . on the economy, the integrity of the patent system, the efficient administration of the Office, and the ability of the Office to timely complete proceedings," 35 U.S.C. § 316(b), favors denying a petition . . . . This includes, for example, events in other proceedings related to the same patent, either at the Office, in district courts, ***or the ITC***.

Prelim. Resp. 6 (quoting Trial Practice Guide Update, 10–11 (emphasis added by Patent Owner)). Patent Owner argues that *General Plastic* factors 1, 2, and 4 weigh against institution, and that "[f]actors 6 and 7 . . . should also consider the substantial resources and effort that will be expended at the ITC." Prelim. Resp. 8–11 (citing *NetApp Inc. v. Realtime Data LLC,* IPR2017-01195, slip op. at 12–13 (PTAB Oct. 12, 2017) (Paper 9) (denying institution because the final written decision would not issue until well after the scheduled trial date)).

In support of these assertions, Patent Owner argues that "Petitioners' IPR challenges are redundant to validity questions Petitioners raised, could have raised, or could still raise, against the same claims of the '243 patent in the ITC and district court proceedings." *Id.* at 8 (regarding Factor 1). Patent Owner further argues that "in this IPR, Petitioners redundantly challenged validity in comparison to their validity challenges that have been pending for months in the ITC proceeding." *Id.* at 9 (regarding Factors 2 and 4).

Petitioner urges us not to exercise our discretion to decline institution under § 314(a). Reply 1–3. Petitioner argues, quoting a recent decision by the Board, "the ITC does not have the authority to invalidate a patent, and ITC decisions do not necessarily pertain to the issues raised in an *inter*

partes review petition. . . . Thus, while the ITC decision in the copending investigation may inform our decision, it does not render our proceeding duplicative or amount to a waste of the Board's resources." *Id.* at 1 (quoting IPR2018-01410 (Paper 14) at 181; IPR2018-01411 (Paper 14) at 17 (same)). Petitioner also argues that "decisions of the ITC involving patent issues have ***no preclusive effect in other forums***." *Id.* at 1–2 (citing *Texas Instr. Inc. v. Cypress Semiconductor Corp.*, 90 F.3d 1558, 1569 (Fed. Cir. 1996)).

Petitioner further argues that a final written decision would issue in this IPR before final resolution of the ITC case and before the district court proceedings even begin. *Id.* at 2–3. More particularly, Petitioner argues the final written decision in this IPR would issue within a few months of a Final Determination by the ITC, and any appeal of the Board's final written decision would substantially overlap with the appeal of the ITC case which may lead the Federal Circuit to consolidate the appeals. *Id.* at 2. Petitioner argues, "[n]othing in the 2018 Trial Practice Guide Update, however, suggests that the mere existence of an ITC action is a basis for denying institution. To the contrary, the PTAB routinely institutes IPR proceedings notwithstanding a pending ITC investigation, even in instances where the ITC investigation is further along than the one here is." *Id.* at 3.

We are persuaded by Petitioner's arguments on this issue. As noted by Petitioner, the ITC does not have the authority to invalidate a patent, and thus ITC decisions do not preempt issues addressed in an *inter partes* review proceeding. In addition, different evidentiary standards and burdens apply to ITC proceedings as compared to *inter partes* review proceedings. Thus, although the ITC decision in the co-pending investigation may inform our decision, it does not render our proceeding duplicative or amount to a waste of the Board's resources. Furthermore, the petitions at issue in *General*

Plastic were follow-on petitions, rather than related filings or proceedings in other tribunals. Patent Owner does not direct us to any authority requiring us to treat an ITC petition as a first-filed petition for purposes of a *General Plastic* analysis. We also have considered the timing of the ITC proceeding relative to the anticipated schedule in this IPR, and do not find the weight attributable to any judicial inefficiencies to be an overriding factor meriting a discretionary denial of the Petition, as Patent Owner urges. For these reasons, we decline to exercise our discretion under 35 U.S.C. § 314(a) to deny institution.

H. Patent Owner's Arguments under 35 U.S.C. § 315(a)(1)

An "*inter partes* review may not be instituted if, before the date on which the petition for such a review is filed, the petitioner or real party in interest filed a civil action challenging the validity of a claim of the patent." 35 U.S.C. § 315(a)(1). Samsung Semiconductor, Inc., Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc., filed a Complaint for Declaratory Judgment of Non-Infringement on June 12, 2018. Ex. 2002. SK Hynix Inc. and SK Hynix America Inc. filed a Complaint for Declaratory Judgment on June 12, 2018. Ex. 2003. Each complaint contains four counts directed to declaratory judgment of non-infringement of the '243 patent and three other patents. Ex. 2002; Ex. 2003.

Patent Owner argues that Petitioner "filed district court complaints concerning the '243 patent on June 12, 2018, more than two months before filing" the present IPR petition. Prelim. Resp. 14. Patent Owner directs us to 35 U.S.C. § 282(b)(2) and its provision that "in ***any action involving*** ... ***infringement*** of a patent," "[i]nvalidity of the patent or any claim in suit" "***shall*** be defenses." *Id.* at 15 (emphasis added by Patent Owner). Patent Owner does not allege that either of the complaints (Exs. 2002, 2003)

explicitly challenge the validity of the '243 patent. *Id.* Patent Owner, however, interprets § 282(b)(2) to mean that "an action involving 'infringement,' from a statutory perspective, implicates and includes validity challenges." *Id.* According to Patent Owner, "[s]ection 282(b)(2)'s implicit inclusion of validity defenses in actions involving infringement preclude a petitioner from obtaining the benefit of first filing a district court complaint, and then filing an IPR petition before explicitly submitting an infringement defense based on invalidity in district court." *Id.* at 17.

Petitioner argues that 35 U.S.C. § 315(a)(1) "applies where a petitioner has 'filed a civil action challenging the validity of a claim of the patent,'" but, as "Patent Owner concedes in its brief, . . . Petitioner only sought a declaratory judgment of noninfringement." Reply 4. According to Petitioner, that is not an action "challenging the validity" of the '243 patent. *Id.* (citing *LG Elecs., Inc. v. Straight Path IP Grp., Inc.*, Case IPR2015-00196, 2016 WL 2640549, at *7 (PTAB May 9, 2016); *Ariosa Diagnostics v. Isis Innovation Ltd.*, Case IPR2012–00022, slip. op. at 14 (PTAB Sept. 2, 2014) (Paper 166)).

We are not directed to any authority demonstrating that we have interpreted 35 U.S.C. § 315(a)(1) or 35 U.S.C. § 282(b)(2) in the manner proposed by Patent Owner. Rather, as Petitioner points out, we have consistently held that a complaint that "only alleges a cause of action for noninfringement," not invalidity, is "not considered a filing of a civil action for invalidity under 35 U.S.C. § 315(a)(1)." *LG Elecs., Inc.*, 2016 WL 2640549 at *7; *Ariosa*, Paper 166, slip op. at 14 ("A civil action for a declaratory judgment of non-infringement is not a civil action challenging the validity of a patent."); *cf. Colas Sol'ns Inc. v. Blacklidge Emulsions, Inc.*, Case IPR2018-00242, slip op. at 6–7 (PTAB Feb. 27, 2018) (Paper 9)

(informative) (denying institution and joinder because the petition was barred under § 315(a)(1) due to the petitioner's prior declaratory judgment action that challenged validity). Here, the complaints filed by Petitioner (Exs. 2002, 2003) allege causes of action only for non-infringement and do not allege a cause of action for invalidity. Thus, we are not persuaded that Petitioner is barred from filing its Petition under 35 U.S.C. § 315(a)(1).

III. CONCLUSION

For the foregoing reasons, we are persuaded that the Petition establishes a reasonable likelihood that Petitioner would prevail in showing at least one of the challenged claims is unpatentable on an asserted ground. Because Petitioner has satisfied the threshold for institution as to at least one claim, we institute *inter partes* review on all claims and all grounds raised in the Petition. *See SAS Institute Inc. v. Iancu,* 138 S. Ct. 1348, 1359–60 (2018) (holding that a decision to institute under 35 U.S.C. § 314 may not institute on fewer than all claims challenged in the petition).

IV. ORDER

Accordingly, it is

ORDERED that an *inter partes* review is instituted as to all challenged claims and all grounds raised in the Petition; and

FURTHER ORDERED that *inter partes* review is instituted commencing on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial.

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TO: **Mail Stop 8** **Director of the U.S. Patent & Trademark Office** **P.O. Box 1450** **Alexandria, VA 22313-1450**	**REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK**

In Compliance with 35 § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the **U.S. District Court for the Northern District of California** on the following:
(X) Patents or ( ) Trademarks

DOCKET NO:	**DATE FILED:**	**UNITED STATES DISCTRICT COURT**
18-cv-03502-LB	June 12, 2018	**Phillip Burton Federal Building** **450 Golden Gate Avenue** **San Francisco, CA 94102**

PLAINTIFF:	**DEFENDANT:**
Samsung Semiconductor, Inc., et al	BiTMICRO, LLC, et al

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1. 6529416		
2. 7826243		
3. 8093103		~~"Pls. see attached copy of the Complaint"~~
4.		
5.		

In the above-entitled case, the following patent(s) have been included.

DATE INCLUDED INCLUDED BY:
( ) Amendment ( ) Answer ( ) Cross Bill ( ) Other Pleading

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1.		
2.		
3.		
4.		
5.		

In the above-entitled case, the following decision has been rendered or judgment issued:

DECISION/JUDGEMENT:

Susan Y. Soong
Susan Y. Soong, Clerk

(by) Deputy Clerk, Thelma Nudo

Copy 1 – Upon initiation of action, mail this copy to Commissioner
Copy 2 – Upon filing document adding patent(s) mail this copy to Commissioner
Copy 3 – Upon termination of action, mail this copy to the Commissioner
Copy 4 – Case file copy

TO: **Mail Stop 8** **Director of the U.S. Patent & Trademark Office** **P.O. Box 1450** **Alexandria, VA 22313-1450**	**REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK**

In Compliance with 35 § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Northern District of California on the following:
(X) Patents or ( ) Trademarks

DOCKET NO:	DATE FILED:	UNITED STATES DISCTRICT COURT
18-cv-03505-NC	June 12, 2018	Robert F. Peckham Federal Building 280 South 1st Street San Jose, CA 95113

PLAINTIFF:	DEFENDANT:
SK hynix Inc.	BiTMICRO, LLC

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1. No. 6,529,416	March 4, 2003	BiTMICRO
2. No. 7,826,243	November 2, 2010	BiTMICRO
3.No. 8,093,103	January 10, 2012	BiTMICRO
4.No 9,135,190	September 15, 2015	BiTMICRO
5.		

In the above-entitled case, the following patent(s) have been included.

DATE INCLUDED INCLUDED BY:
( ) Amendment ( ) Answer ( ) Cross Bill ( ) Other Pleading

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1.		
2.		
3.		
4.		
5.		

In the above-entitled case, the following decision has been rendered or judgment issued:

DECISION/JUDGEMENT:

Susan Y. Soong
Susan Y. Soong, Clerk

Susie F. Barrera
(by) Deputy Clerk, Susie F. Barrera

Copy 1 – Upon initiation of action, mail this copy to Commissioner
Copy 2 – Upon filing document adding patent(s) mail this copy to Commissioner
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY.DOCKET NO./TITLE	REQUEST ID
11/322,442	12/29/2005	Rey Bruce	150962.00011	62795

Acknowledgement of Change to Small Entity Status

The entity status change request below filed through Private PAIR on 04/30/2018 has been accepted.

CERTIFICATIONS:

Change of Entity Status:

X Applicant asserting small entity status. See 37 CFR 1.27.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

This portion must be completed by the signatory or signatories making the entity status change in accordance with 37 CFR 1.4(d)(4).

Signature:	/raman n. dewan/
Name:	Raman N. Dewan
Registration Number:	38787

Organization _____ Bldg./Room _____

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/322,442	12/29/2005	Rey Bruce	6005.011

CONFIRMATION NO. 5045

POWER OF ATTORNEY NOTICE

64180
Uriarte Law
5255 Stevens Creek Blvd.
Santa Clara, CA 95051

OPAP
FEB 16 2018
PATENT & TRADEMARK OFFICE

OC000000094429964

Date Mailed: 09/29/2017

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/26/2017.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/atesfai/

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,826,243 B2
APPLICATION NO. : 11/322442
DATED : November 2, 2010
INVENTOR(S) : Rey Bruce et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Drawings

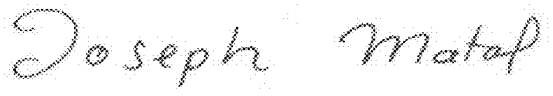
Please insert Figure 5b by replacing Drawing Sheet 6 of 28 with Replacement Sheet 6 of 28 attached hereto.

In the Specification

Column 3, Line 39, replace "to be able to connect" with --for creating--;
Column 3, Line 39, replace "chain route from" with --chain route through--;
Column 3, Line 40, after "in a stack" insert --by connecting a set of serial chain connections,--;
Column 3, Line 40, replace "to an example" with --to another example--;

Column 9, Line 3, before "The controller" insert --An active pad may be also referred to herein as an "active port."--;
Column 9, Line 3, replace "is connected" with --is ultimately connected--;
Column 9, Line 4, delete "SDRAM module 0's";
Column 9, Line 4, replace "ball 1903, pad 01" with --ball 1903 of SDRAM module 0, active pad 01--;
Column 9, Line 4, after "pad 01" insert --is connected--;
Column 9, Lines 4-5, replace "SDRAM module 1's X0 ball 1902" with --X0 ball 1902 of SDRAM module 1--;
Column 9, Line 5, replace "The X0 balls" with --These X0 balls--;
Column 9, Line 6, replace "for the SDRAM modules." with --for these SDRAM modules. Thus, as illustrated in Figure 19, there is one active ball, such as X0, ultimately coupled to one active pad per module.--;
Column 9, Line 6, before "All SDRAM modules" insert paragraph break;
Column 9, Line 7, replace "identical which" with --identical, and in the example shown in FIG. 19,--;
Column 9, Line 7, replace "include the connections as follows:" with --include the following:--;
Column 9, Line 7, replace "X1 ball" with --an X1 passive ball--;
Column 9, Line 8, replace "X1 pad" with --an X1 passive pad--;
Column 9, Line 8, replace "X2 ball to X2 pad" with --an X2 passive ball to X2 passive pad--;

Signed and Sealed this
Twenty-eighth Day of November, 2017



Joseph Matal
Performing the Functions and Duties of the
Under Secretary of Commerce for Intellectual Property and
Director of the United States Patent and Trademark Office

Column 9, Line 8, after "and so on." insert --The connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module, such as the X1 passive ball and X1 passive pad connection in FIG. 19, is named "passive port", as as passive ports 1909 illustrated in FIG. 19.--;
Column 9, Line 12, after "module in the stack." insert --Thus, an active signal applied at an active pad, such as active pad 02, shown with reference number 1904 on controller module 1910, is routed through at least one passive port connecting a passive ball and passive pad, such as the passive ports 1905 connecting passive ball X2 to passive pad X2 and passive ball X1 to passive pad X2, respectively, so that this active signal eventually reaches an active ball, such as X0 ball SDRAM Module 2, in Figure 19.--;
Column 9, Line 16, after "the repeating pattern." insert --For example in Figure 19, an X1 passive ball is connected to an X1 passive pad, X2 passive ball to X2 passive pad, etc.--;
Column 9, Lines 16-17, replace "The importance is the approach using" with --By using--;
Column 9, Line 19, delete "also";
Column 9, Line 19, replace "in other embodiment" with --in alternative embodiments--;
Column 9, Lines 19-20, replace "invention, e.g. using" with --invention. For example, an alternative embodiment may include using--;
Column 9, Lines 21-22, replace "The example embodiment does not limit" with --This alternative embodiment is not intended to limit--;
Column 9, Line 22, replace "the present invention." with --the present invention in any way.--;
Column 9, Line 67, after "module 2103." insert --The modules, including base module 2103, stack modules 2106 and 2130, and an end module, such as top module 2108, each have a ball and a pad that are coupled together by a serial chain circuit. For example, base module 2103 includes a serial chain circuit 2127 that couples IN ball 2104 with OUT pad 2105, and a serial chain circuit 2136 that couples OUT pad 1237 with OUT ball 2138; module 2106 includes a serial chain circuit 2128 that couples IN ball 2107 with OUT pad 2129, and a serial chain circuit 2139 that couples OUT pad 2140 with OUT ball 2141; module 2130 includes a serial chain circuit 2131 that couples IN ball 2132 with OUT pad 2133, and a serial chain circuit 2142 that couples OUT pad ball 2143 with OUT ball 2144; and top module 2108 incudes a serial chain circuit 2134 that couples IN ball 2135 with OUT pad 2109 and a serial chain circuit 2145 that couples OUT pad 2110 with OUT ball 2113.--;
Column 9, Line 67, replace "The base module's" with --Thus, the base module's--;

Column 10, Line 2, after "so on." insert --A signal route that includes a serial chain circuit coupling an ball and pad is herein after referred to as a "serial chain connection", and at least two serial chain connections connected in series are herein after referred to as a "serial chain route", such as serial chain route 2146 or 2111.--;
Column 10, Line 4, replace "another pad 2110 which" with --another pad, such as OUT pad 2110, which--;
Column 10, Line 5, replace "ball 2113 underneath." with --ball underneath, such as OUT ball 2113.--;
Column 10, Line 6, replace "passes through the pads and balls 2111 of the" with --passes through another set of serial chain connections that comprise another serial chain route, such as serial chain route 2111 for the--;
Column 10, Line 8, after "access," insert --A serial chain connection includes a serial chain input and a serial chain output. A serial chain input is disposed to receive a signal, while a serial chain output is disposed to provide the signal. For example in Figure 21a, IN balls 2014, 2107, 2132, and 2135, and OUT pads 2110, 2143, and 2140 are serial chain inputs, respectively, OUT pads 2105, 2129, 2133,

and 2109, and OUT balls 2113, 2144, 2141, and 2138 are serial chain outputs, respectively. At least one of the balls and pads that are coupled to their respective chain circuit may be in the form of a passive ball and passive pad, respectively, since an active signal, such as signal 2102, applied at active pad 2101, can be routed through a series of serial chain circuits that couple respective balls and pads. In effect, each of these serial chain circuits functions as a passive port. A serial chain circuit, however, can also terminate a serial chain route, such as serial chain route 2146, and branching or routing this serial chain route to another pad that functions as a serial chain input of another serial chain route, such as serial chain route 2111, as described further below.--;

Column 10, Line 8, replace "How the top module terminates the serial" with --"Regarding the top module, the serial"--;

Column 10, Line 9, after "chain" insert --termination--;

Column 10, Line 9, replace "branches them out" with --branching--;

Column 10, Line 10, after "have" insert --a control circuit that includes--;

Column 10, Line 33, replace "diver" with --driver--.

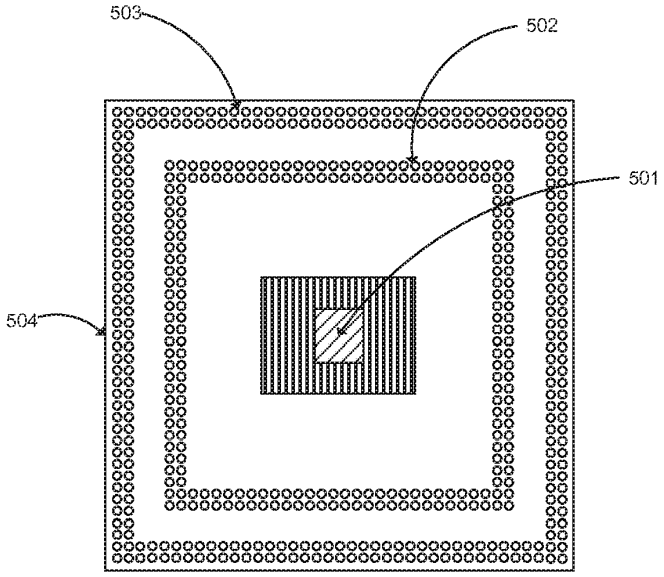


Figure 5a

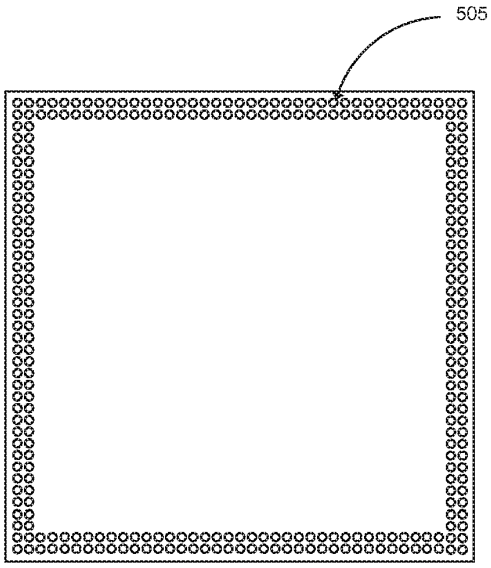


Figure 5b

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/322,442	12/29/2005	Rey Bruce	150962.00011	5045

67942 7590 11/07/2017

JACKSON WALKER L.L.P.
ATTN: INTELLECTUAL PROPERTY DEPARTMENT
100 CONGRESS AVENUE
SUITE 1100
AUSTIN, TX 78701

EXAMINER
SOFOCLEOUS, ALEXANDER

ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
11/07/2017	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Commissioner for Patents
United States Patent and Trademark Office
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Patent No. 7826243
Issued Date: 02 November, 2010
Appl. No: 11/322,442
Filed.: 29 December 2005

PART (A) RESPONSE FOR CERTIFICATES OF CORRECTION

This is a decision on the Certificate of Correction request filed 27 September 2017.

The request for issuance of Certificate of Correction for the above-identified correction(s) under the provisions of 37 CFR 1.322 and/or 1.323 is hereby:

(Check one)
☒ Approved ☐ Approved in Part ☐ Denied

Comments: The Specification amendments and replacement drawings filed 11/13/2009 were approved.

PART (B) PETITION UNDER 37 CFR 1.324 OR 37 CFR 1.48

☐ This is a decision on the petition filed to correct inventorship under 37 CFR 1.324.

☐ This is a decision on the request under 37 CFR 1.48, petition filed . In view of the fact that the patent has already issued, the request under 37 CFR 1.48 has been treated as a petition to correct inventorship under 37 CFR 1.324.

The petition is hereby: ☐ Granted ☐ Dismissed

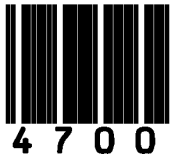
Comment:

The patented filed is being forwarded to Certificate of Corrections Branch for issuance of a certificate naming only the actual inventor or inventors.

/ALEXANDER SOFOCLEOUS/
Supervisory Patent Examiner, Art Unit 2825
Technology Center 2800
Phone: 571-272-2800

Certificates of Correction Branch email: CustomerServiceCoC@uspto.gov CoC Central Phone Number: (703) 756-1814

Office of Petitions: Routing Sheet



Application No. 11322442

This application is being forwarded to your office for further processing. A decision has been rendered on a petition filed in this application, as indicated below. For details of this decision, please see the document PET.OP.DEC filed on the same date as this document.

- [X] **GRANTED**
- [ ] **DISMISSED**
- [ ] **DENIED**

Office of Petitions: Decision Count Sheet

Mailing Month 10

Application No. 11322442

For US serial numbers: enter number only, no slashes or commas. Ex: 10123456
For PCT: enter "51+single digit of year of filing+last 5 numbers", Ex. for PCT/US05/12345, enter 51512345

Deciding Official: WISE, APRIL M.

Count (1) - Palm Credit 11322442

Decision: GRANT

FINANCE WORK NEEDED
☐ Select Check Box for YES

Decision Type: 519 - 37 CFR 1.182 for INVENTOR NAME CHANGE, ORDE

Notes:

Count (2)

Decision: n/a

FINANCE WORK NEEDED
☐ Select Check Box for YES

Decision Type: NONE

Notes:

Count (3)

Decision: n/a

FINANCE WORK NEEDED
☐ Select Check Box for YES

Decision Type: NONE

Notes:

Initials of Approving Official (if required)

If more than 3 decisions, attach 2nd count sheet & mark this box ☐

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/322,442	12/29/2005	Rey Bruce	150962.00001	5045

67942 7590 10/30/2017

JACKSON WALKER L.L.P.
ATTN: INTELLECTUAL PROPERTY DEPARTMENT
100 CONGRESS AVENUE
SUITE 1100
AUSTIN, TX 78701

EXAMINER
SOFOCLEOUS, ALEXANDER

ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
10/30/2017	PAPER

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The time period for reply, if any, is set in the attached communication.

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Commissioner for Patents
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In re Patent No. 7,826,243	:	
Issue Date: November 2, 2010	:	
Application No. 11/322,442	:	DECISION ON PETITION
Filed: December 29, 2005	:	
Attorney Docket No. 150962.00001	:	

This is a decision on the petition under 37 CFR 1.182, filed July 10, 2017, requesting issuance of a duplicate Letters Patent for the above-identified patent.

The petition is **GRANTED**.

The Office of Data Management is directed to issue the duplicate Letters Patent.

As authorized, the $400 fee for the petition under 37 CFR 1.182 has been assessed to petitioner's deposit account.

A copy of this decision is being faxed to the Office of Data Management for issuance of the duplicate Letters Patent.

Telephone inquiries concerning this decision may be directed to undersigned at (571) 272-1642. All other inquiries regarding the issuance of the duplicate Letters Patent may be directed to Kimberly Terrell in the Office of Data Management at (571) 272-4200.

/April M. Wise/
April M. Wise
Paralegal Specialist
Office of Petitions

cc: Kimberly Terrell, Randolph Square, 9th Floor, D33 (Fax No. (571) 270-9958)

Doc Code: ECOMM.AUTH/ECOMM.WTDW
Doc Description: Internet Communications Authorized/Internet Communications Authorization Withdrawn

PTO/SB/439 (11-15)

AUTHORIZATION FOR INTERNET COMMUNICATIONS IN A PATENT APPLICATION OR REQUEST TO WITHDRAW AUTHORIZATION FOR INTERNET COMMUNICATIONS		
	Application No.	11/322,442
	Filing Date	12/29/2005
	First Named Inventor	REY, BRUCE
	Art Unit	2825
	Examiner Name	SOFOCLEOUS, ALEXANDER
	Practitioner Docket No.	150962.00001

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I. To authorize permission for Internet Communications.

☑ Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with the undersigned and practitioners in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application via video conferencing, instant messaging, or electronic mail. I understand that a copy of these communications will be made of record in the application file. (MPEP 502.03)

II. To withdraw authorization for Internet Communications.

☐ The authorization given on _____, to the USPTO to communicate with the undersigned and any practitioner in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application via Internet communications such as video conferencing, instant messaging, or electronic mail is hereby withdrawn. I understand that the withdrawal is effective when approved rather than when received.

I am the

☐ applicant.

☑ attorney or agent of record. Registration number 38,947.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/joseph lally/ — Signature

October 24, 2017 — Date

JOSEPH LALLY — Typed or printed name

512 236 2019 — Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Juristic entities must be represented by a patent practitioner (see 37 CFR 1.31, which is applicable to any paper filed on or after September 16, 2012, that is presented on behalf of a juristic entity, regardless of application filing date). Submit multiple forms if more than one signature is required, see below*.

☐ * Total of _____ forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	30740855
Application Number:	11322442
International Application Number:	
Confirmation Number:	5045
Title of Invention:	MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES
First Named Inventor/Applicant Name:	Rey Bruce
Customer Number:	67942
Filer:	Joseph Patrick Lally
Filer Authorized By:	
Attorney Docket Number:	150962.00001
Receipt Date:	24-OCT-2017
Filing Date:	29-DEC-2005
Time Stamp:	12:19:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Internet Communications Authorized	Internet_Communications.pdf	115409 79044d423d06478750d75f650ad4cc342a14c8b1	no	2

Warnings:

Information:	
Total Files Size (in bytes):	115409

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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11/322,442	12/29/2005	Rey Bruce	6005.011

CONFIRMATION NO. 5045

64180
Uriarte Law
5255 Stevens Creek Blvd.
Santa Clara, CA 95051

POWER OF ATTORNEY NOTICE

OC000000094429964

Date Mailed: 09/29/2017

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/26/2017.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/atesfai/

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/322,442	12/29/2005	Rey Bruce	150962.00001

CONFIRMATION NO. 5045

67942
JACKSON WALKER L.L.P.
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100 CONGRESS AVENUE
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AUSTIN, TX 78701

POA ACCEPTANCE LETTER

OC000000094429966

Date Mailed: 09/29/2017

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/26/2017.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/atesfai/

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT NO.	**:**	**US 7,826,243 B2**
DATED	**:**	**NOVEMBER 2, 2010**
APPLICATION	**:**	**11/322,442**
INVENTORS	**:**	**BRUCE ET AL.**
PATENTEE	**:**	**BITMICRO LLC**

REQUEST FOR CERTIFICATE OF CORRECTION
UNDER 37 CFR 1.322

EXPEDITED PROCESSING REQUESTED

Commissioner for Patents
OFFICE OF DATA MANAGEMENT ATTENTION: CERTIFICATES OF CORRECTION BRANCH
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

BITMICRO LLC (Patentee) submits this paper in connection with the above referenced patent (the Patent). The Patent contains errors and, accordingly, a Certificate of Correction is respectfully requested. A proposed Certificate of Correction (PTO/SB/44) and copies of documents supporting Patentee's assertions are submitted herewith. Pursuant to MPEP 1480.01, Patentee respectfully requests Expedited Consideration.

Remarks Supporting Expedited Consideration begin on page 2 of this paper.

Documentation Supporting Patentee's Assertions is described on page 3 of this paper.

A Replacement Sheet for Drawing Sheet 6 is attached as page 5 of this paper.

Attachment "A" through **Attachment "E"** are attached following page 6 of this paper.

Remarks Supporting Expedited Consideration under MPEP § 1480.01

- The requested corrections are set forth in the PTO/SB/44 submitted contemporaneously herewith.
- The PTO/SB/44 indicates the location of the errors in the printed patent by column and line number.
- The errors necessitating the corrections are clearly disclosed in the records of the Office.
- Documentation that unequivocally supports Patentee's assertions is provided as described below.
- The supporting documentation consists of photocopies of correspondence dated and received by the Office and photocopies of Examiners' responses regarding entry of amendments supporting Patentee's request.
- The supporting documentation makes it possible to process this request without the corresponding patent file.

Accordingly, consistent with MPEP § 1480.01 Patentee respectfully requests expedited consideration resulting in an expeditiously issued Certificate of Correction.

Documentation Supporting Patentee's Assertions

The corrections consist of Specification corrections and a Drawing correction. The Specification corrections are set forth on pages 1-4 of the PTO/SB/44. The Drawing correction is set forth as the last line item on page 4 of the PTO/SB/44.

Specification corrections

- All of the requested specification corrections correspond to specification amendments included in an amendment dated 13-Nov-2009 (the "November 2009 amendment") (ATTACHMENT "A")
- USPTO approval of the specification amendments included in the November 2009 amendment was indicated in a Notice of Allowability accompanying a Notice of Allowance mailed 09-Apr-2010 ("the April 2010 Allowance") (ATTACHMENT "B"). *See*, pp. 2-3 of the Notice of Allowability (pp. 5-6 of the Notice of Allowance).
- None of the requested specification corrections appear in the Patent (ATTACHMENT "C").

Drawing correction

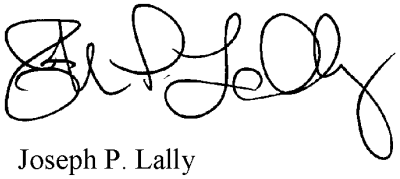
- The drawing correction pertains to Figure 5b.
- Sheet 6 of 28 of the Original Drawings (ATTACHMENT "D") included Figure 5a and Figure 5b. *See*, Original Drawings, p. 6.
- A Substitute Specification filed 13-Feb-2009 (ATTACHMENT "E") included Replacement Drawings for all 28 sheets of the Original Drawings. S*ee*, Substitute Specification, pp. 77-104).
- Sheet 6 of the Replacement Drawings included Figure 5a and Figure 5b. S*ee*, Substitute Specification, p. 83.
- USPTO approval of the Replacement Drawings was indicated in the April 2010 Allowance, *See*, p. 3 of the Notice of Allowability (p. 6 of the Notice of Allowance).
- Sheet 6 of the drawings in the Patent included Figure 5a, but not Figure 5b. *See*, Patent, p. 7.

Conclusion

Because all corrections requested herein were necessitated by U.S. Patent and Trademark Office error, no fee is required under the provisions of 37 CFR 1.322. If, however, a fee is required, the Commissioner is authorized to charge any such fee to Jackson Walker L.L.P. Deposit Account No. 10-0096.

If any questions arise during the processing of this request, please do not hesitate to contact the undersigned at the number listed below.

Respectfully submitted,
JACKSON WALKER L.L.P.
ATTORNEYS FOR ASSIGNEE



Joseph P. Lally
Reg. No. 38,947

SEND CORRESPONDENCE TO:
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19122471v.1

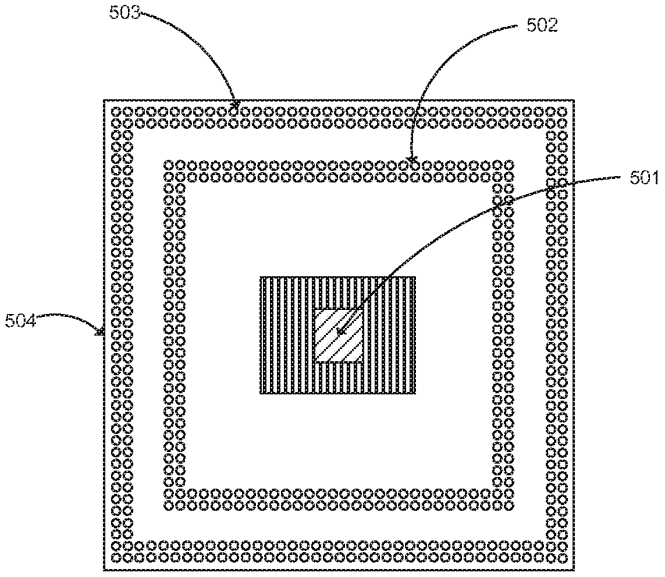


Figure 5a

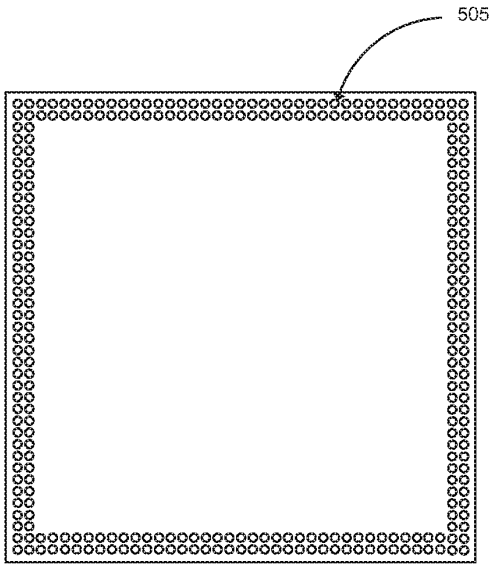


Figure 5b

Attorney Docket: 6005.011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: BRUCE et al.	Group Art Unit: 2892
Serial No.: 11/322,442	Examiner: ULLAH, Elias
Application Filing Date: 29 Dec 2005	
For: MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND REPLY TO SECOND OFFICE ACTION

Dear Examiner:

In response to the Office Action, mailed 13 May 2009, please kindly amend this Application as follows and consider the remarks set forth below.

Amendments to the Specification begin on page 2;

A listing of claims begins on page 7;

Amendment(s) to the Drawings begins on page 19; and

Remarks begin on page 21 of this paper.

Replacement sheets of drawings incorporating the changes proposed in the Amendments to the Drawings and corresponding to the written description, respectively, are attached to this paper.

Amendments to the Specification

Text in underline indicates new text, while text in strike-out format or between a pair of double brackets indicates deletion of the text.

In the Specification, as previously amended, please enter the amendments shown with respect to the replacement paragraphs identified below.

Please replace the title on page 1, lines 1-2, with the following replacement title.

Multiple Chip Module and Package Stacking For Storage Devices

Please replace the paragraph on page 8, line 13 through 15, with the following replacement paragraph.

Figure 21a shows another pin assignment and connection technique for creating ~~be able to connect~~ a serial chain route through ~~from~~ multiple modules in a stack by connecting a set of serial chain connections, according to another ~~example~~ embodiment of the present invention.

Please replace the paragraph on page 20, line 19 through page 21, line 16, with the following replacement paragraphs.

Figure 19 shows a first pin assignment and connection technique that enables a selection of specific module in a multiple module stack. The figure illustrates the controller and SDRAM modules as an example. The SDRAM module balls, such as **1907**, are represented by big oblong shapes, and the pads such as **1908** are represented by smaller oblong shapes. A pad to ball connection is represented by a rectangle, such as **1906**. The controller module has four active pads such as **1904**, one each for the four SDRAM modules such as **1901**. An active pad may be also

referred to herein as an "active port". The controller module's active pad 00 **1904** is ultimately connected to ~~SDRAM module 0's~~ X0 ball **1903** of SDRAM module 0, active pad 01 is connected to ~~SDRAM module 1's~~ X0 ball **1902** of SDRAM module 1, and so on. These[[The]] X0 balls are the active balls for these[[the]] SDRAM modules. Thus, as illustrated in Figure 19, there is one active ball, such as X0, ultimately coupled to one active pad per module.

All SDRAM modules are identical, and in the example shown in Figure 19, [[which]] include the following connections ~~as follows~~: an X1 passive ball is connected to an X1 passive pad, an X2 passive ball to X2 passive pad, and so on. The connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module, such as the X1 passive ball and X1 passive pad connection in Figure 19, is named "passive port", such as passive ports 1909 illustrated in Figure 19. The technique involves using a ladder-like routing path, such as **1905** on the stacked modules. This technique enables the controller module's active pad to be routed to the desired specific module in the stack. Thus, an active signal applied at an active pad, such as active pad 02, shown with reference number 1904 on controller module 1910, is routed through at least one passive port connecting a passive ball and passive pad, such as the passive ports 1905 connecting passive ball X2 to passive pad X2 and passive ball X1 to passive pad X2, respectively, so that this active signal eventually reaches an active ball, such as X0 ball SDRAM Module 2 in fig. 19. The example embodiment illustrated in Figure~~figure~~ 19 comprises a repeating pattern for the balls and pads. Passive balls are connected within each module to passive pads with an offset distance equaling one periodic distance of the repeating pattern. For example in Figure 19, an X1 passive ball is connected to an X1 passive pad, X2 passive ball to X2 passive pad, etc. ~~The importance is the approach~~ By using repeating patterns and offsetting of the passive ball to passive pad within each module, other offset distances

can be used [[also]] in alternativeother embodiments of the present invention.[[,]] e.g. For example, an alternative embodiment may include using an offset of two or any multiple of the periodic distance of the repeating pattern. This[[The]] alternative example embodiment is not intended todoes not limit the scope of the present invention in any way.

Please amend the paragraph on page 23, line 1 through page 24, line 6, with the following replacement paragraphs.

The last connection technique is used for serial routing of all modules in the stack and allowing them to be externally accessible for horizontal expansion on a PCB, such as a main board. Figure 21a shows how this technique is implemented in the stacking method. The main board **2101** [[ ]]contains the input signals **2102** which will then be connected to IN ball **2104** of the base module **2103**. The modules, including base module **2103**, stack modules **2106** and **2130**, and an end module, such as top module **2108**, each have a ball and a pad that are coupled together by a serial chain circuit. For example, base module **2103** includes a serial chain circuit **2127** that couples IN ball **2104** with OUT pad **2105**, and a serial chain circuit **2136** that couples OUT pad **2137** with OUT ball **2138**; module **2106** includes a serial chain circuit **2128** that couples IN ball **2107** with OUT pad **2129**, and a serial chain circuit **2139** that couples OUT pad **2140** with OUT ball **2141**; module **2130** includes a serial chain circuit **2131** that couples IN ball **2132** with OUT pad **2133**, and a serial chain circuit **2142** that couples OUT pad ball **2143** with OUT ball **2144**; and top module **2108** includes a serial chain circuit **2134** that couples IN ball **2135** with OUT pad **2109** and a serial chain circuit **2145** that couples OUT pad **2110** with OUT ball **2113**. Thus, the[[The]] base module's OUT pad **2105** is connected to IN ball **2107** of the first stack module **2106**, and so on.

A signal route that includes a serial chain circuit coupling an ball and pad is herein after referred to as a "serial chain connection", and at least two serial chain connections connected in

series are herein after referred to as a "serial chain route", such as serial chain route **2146** or **2111**. The top module **2108**[[,]] terminates the signal to the top pad **2109** and routes, with connection **2112,** the signal internally to another pad, such as OUT pad **2110**, which is connected directly to the ball [[**2113**]] underneath, such as OUT ball **2113**. Since the modules are identical, this routed signal passes through another set of [[the]] serial chain connections that comprise another serial chain route, such as serial chain route ~~pads and balls~~ **2111** for[[of]] the stack until it reaches the OUT pad **2114** of the main board for external access. A serial chain connection includes a serial chain input and a serial chain output. A serial chain input is disposed to receive a signal, while a serial chain output is disposed to provide the signal. For example in Figure 21a, IN balls **2104**, **2107**, **2132**, and **2135**, and OUT pads **2110**, **2143**, and **2140** are serial chain inputs, respectively. OUT pads **2105**, **2129**, **2133**, and **2109**, and OUT balls **2113**, **2144**, **2141**, and **2138** are serial chain outputs, respectively. At least one of the balls and pads that are coupled to their respective chain circuit may be in the form of a passive ball and passive pad, respectively, since an active signal, such as signal **2102**, applied at active pad **2101**, can be routed through a series of serial chain circuits that couple respective balls and pads. In effect, each of these serial chain circuits functions as a passive port. A serial chain circuit, however, can also terminate a serial chain route, such as serial chain route **2146**, and branching or routing this serial chain route to another pad that functions as a serial chain input of another serial chain route, such as serial chain route **2111**, as described further below.

Regarding~~How~~ the top module, ~~terminates~~ the serial chain termination and branch~~inges them out~~ to other pads is shown in Figure 21b. All modules have a control circuit that includes a selectable buffer **2115** that tri-states the input when pulled low. The signal from the IN balls **2116** enters the internal circuit **2117** and exits the circuit connecting to the OUT pad **2118**. The buffer's **2115** control line is weakly pulled up internally. The "StkLow" ball is connected internally to

GND **2119**, thus pulling down the buffer control line when a module is stacked above it, and it is pulled up when no module is stacked directly above it. When the buffer control line is pulled high, it will let the input signal branch out **2120** to the other pads, thus creating a connection route or trace that loops back to the base module solder balls. When a module is stacked above a module that is disposed with selectable buffer **2115** in the manner shown, the buffer control signal is pulled low, tri-stating the input signal and disallowing the branching effect. This technique allows the signal to be accessible to the external balls of the base module, thus horizontal expansion for a serial signal is achievable. The balls are then routed, with connection **2121**, to the other modules **2122** on the other locations. The same technique is used on the main board **2123**, when no package is detected on the "StkLow" pad, the buffer allows the input to connect to the designated pads on the other locations. The tri-stated buffer technique is redundant to all locations. An example is the JTAG TDI-TDO signal. The driver [[diver]] circuit **2125** sends out TDI signals to the pads and the closing TDO signal **2124** loops back to the driver circuit.

Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (PREVIOUSLY CANCELLED) A method for stacking a plurality of modules comprising the steps of:

providing one or more active port on the plurality of modules for carrying one or more active signal;

providing one or more passive port on the plurality of modules for passing through the one or more active signals; and

stacking the plurality of modules.

2. (PREVIOUSLY CANCELLED) The method of claim 1 wherein the one or more passive port forms a ladder like routing path.

3. (PREVIOUSLY CANCELLED) The method of claim 1 wherein one or more of the plurality of module is rotated before being stacked and the one or more passive port forms a rotational routing path.

4. (PREVIOUSLY CANCELLED) The method of claim 1 further comprising the step of providing one or more pair of daisy chain input port and daisy chain output port for forming a first daisy chain connection wherein each pair of the daisy chain input port and the daisy chain output port are connected through a daisy chain circuit.

5. (PREVIOUSLY CANCELLED) The method of claim 4 further comprising the step of providing one or more control port for enabling a routing path extending the first daisy chain connection within an end module.

6. (PREVIOUSLY CANCELLED) The method of claim 5 wherein the routing path within the end module is connected to a second daisy chain connection.

7. (PREVIOUSLY CANCELLED) The method of claim 1 wherein one or more of the plurality of modules is a main board.

8. (PREVIOUSLY CANCELLED) The method of claim 7 wherein one or more vertically stacked module is connected to the main board.

9. (PREVIOUSLY CANCELLED) The method of claim 2:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located between a pre-determined distance to each other in a repeating pattern, the pre-determined distance equaling a multiple of a

periodic distance of the repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the ladder like routing path; and

wherein the ladder like routing path comprises one or more passive ball and one

or more passive pad.

10. (PREVIOUSLY CANCELLED) The method of claim 3:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located opposite each other in a repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the rotational routing path; and

wherein the rotational routing path comprises one or more passive ball and one

or more passive pad.

11. (PREVIOUSLY CANCELLED) The method of claim 4:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive
pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection; and

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad.

12. (PREVIOUSLY CANCELLED) The method of claim 5:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive
pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad; and

wherein the routing path comprises one or more tri-state driver controlled by the one or more control port.

13. (PREVIOUSLY CANCELLED) The method of claim 6:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive
pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad;

wherein the routing path comprises one or more tri-state driver controlled by the one or more control port; and

wherein one or more daisy chain connection are extended through one or more vertically stacked module connected to a main board.

14. (CURRENTLY AMENDED) A stacked module comprising a plurality of modules each comprising:

one or more active ports for carrying one or more active signal; [[and]]

one or more passive ports for passing through the one or more active signals;[[.]]

a first serial chain route that includes at least one serial chain connection, the serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output; said serial chain input coupled to said serial chain output through said serial chain circuit;

a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module; and

said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module.

15. (CURRENTLY AMENDED) The stacked module of claim 14 wherein the one or more passive port forms a ladder like routing path, and the passive port connects a passive ball on one surface of a module to a passive pad on another surface of the module.

16. (CURRENTLY AMENDED) The stacked module of claim 14 wherein one or more of the plurality of modules is rotated before being stacked and the one or more passive port forms a rotational routing path.

17. (CANCELLED) The stacked module of claim 1 further comprising one or more pair of daisy chain input port and daisy chain output port for forming a first daisy chain connection wherein each pair of the daisy chain input port and the daisy chain output port are connected through a daisy chain circuit.

18. (CANCELLED) The stacked module of claim 17, further comprising one or more control port for enabling a routing path extending the first daisy chain connection within an end module.

19. (CANCELLED) The stacked module of claim 18 wherein the routing path within the end module ~~is~~ connected to a second daisy chain connection.

20. (CURRENTLY AMENDED) The stacked module of claim 14 wherein one or more of the plurality of modules includes ~~is~~ a main board.

21. (ORIGINAL) The method of claim 20 wherein one or more vertically stacked module is connected to the main board.

22. (CURRENTLY AMENDED) The stacked module of claim 15:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located between a pre-determined distance to each other in a repeating pattern, the pre-determined distance equaling a multiple of a periodic distance of the repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the ladder like routing path; and

wherein at least one of the ~~ladder like routing path comprises~~ one or more passive ball and one or more passive pad forms a ladder like routing path.

23. (CURRENTLY AMENDED) The stacked module of claim 16:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located opposite each other in a repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the rotational routing path; and

wherein at least one of the ~~rotational routing path comprises~~ one or more passive ball and one or more passive pad form a rotational routing path.

24. (CURRENTLY AMENDED) The stacked module of claim 14[[17]]:

wherein each of the plurality of modules comprises a first side and a second side, and the one or more passive ports includes a first passive port connected to a passive ball disposed on the first side and to a passive pad disposed on the second side of a module from the plurality of modules;

wherein the ~~one or more~~ serial[[daisy]] chain input ~~port is~~ includes ~~connected to~~ the ~~one or more~~ passive ball ~~on the first side~~ and the ~~one or more~~ serial ~~daisy~~ chain output ~~port~~ includes the ~~is connected to one or more~~ passive pad ~~on the second side of one or more corresponding module~~;

wherein ~~each of~~ the ~~one or more~~ passive ball and ~~each of~~ the ~~one or more~~ passive pad ~~corresponding to a same daisy chain port~~ are located opposite each other; and

further including a base module having an active port for providing a signal, said signal routed to a same location on the plurality of modules through the first serial chain route.

~~wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection; and~~

~~wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad.~~

25. (CURRENTLY AMENDED) The stacked module of claim 14[[18]]:

~~wherein each of the plurality of modules comprises a first side and a second side;~~

~~wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;~~

~~wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;~~

~~wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;~~

~~wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad; and~~

wherein the routing path includes ~~comprises~~ one or more tri-state driver controlled by the ~~one or more~~ control circuit ~~port~~.

26. (CURRENTLY AMENDED) The stacked module of claim 25[[19]] further including:

~~wherein each of the plurality of modules comprises a first side and a second side;~~

~~wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;~~

~~wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;~~

~~wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;~~

~~wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad;~~

~~wherein the routing path comprises one or more tri state driver controlled by the one or more control port;~~

~~wherein one or more daisy chain connection are extended through one or more vertically stacked module connected to a main board.~~

a main board coupled to another stacked module having a third serial chain route; and

another control circuit for enabling another routing path that connects the second serial chain route with the third serial chain route.

27. (CURRENTLY AMENDED) The stacked module of claim 15, wherein:

the stacked module further includes a first outside surface and a second outside surface, the first and second outside surfaces disposed to face opposite each other; and

at least one of the plurality of modules includes a first module having a first target location terminating between the first and second outside surfaces.

28 (PREVIOUSLY ADDED) The stacked module of claim 27, wherein the plurality of modules further includes a second module and a third module, the

second module including a second module surface that includes the first outside surface and the third module including a third module surface that includes the second outside surface.

29. (PREVIOUSLY ADDED) The stacked module of claim 15, further including a second ladder like routing path; and wherein:

the plurality of modules includes a first module and a second module, the first and second modules respectively including a first target location and a second target location, the second target location located within the stacked module; and

the ladder like routing path for routing one of the active port to the first target location, and the second ladder like routing path for routing another one of the active port to the second target location.

30. (PREVIOUSLY ADDED) The stacked module of claim 29, further including a second ladder like routing path; and wherein:

the stacked module includes a first outside surface and a second outside surface, the first and second outside surfaces disposed to face opposite each other;

the ladder like routing path terminates at the first target location; and

the second ladder like routing path terminates at the second target location, the second target terminating within the stacked module and located between the first and second outside surfaces;

31. (PREVIOUSLY ADDED) The stacked module of claim 29, wherein the second target location is located between the first and second outside surfaces.

Amendment(s) to the Drawings

The following proposed amendments to the Drawings are provided in the form of replacement drawing sheets, which are each labeled "Replacement Sheet" in their respective page headers pursuant to 37 CFR 1.84(c). Support for the amendments below is provided on pages XX in the Substitute Specification previously submitted on 12 February 2009. No new matter has been added.

Figure 19 has been amended as described below.

A set of parenthesis has been placed around the text "Controller Module".

Reference number "1910" has been placed above the text "(Controller Module)".

Multiple instances of reference number "1909" has been inserted as shown in the Replacement Sheet; Reference number "1909" corresponds to the element named "passive port" in the Specification as amended at p. 22.

Multiple instances of reference number "1904" has been inserted to the drawing elements annotated with "01", "02", and "03", and referred to in the Specification as "active pads" or "active ports" at p. 21.

Figure 21a in drawing sheet 27/28 has been amended as described below:

Element numbers 2103, 2106, and 2108 have been moved from the left to the right side of the Drawing sheet.

Element numbers 2127 through 2135, inclusive, element numbers 2137, 2138, 2140, 2141, and 2143 have been added as shown.

Drawing elements corresponding to new element numbers 2136, 2139, 2142, 2145, 2146 have been added.

Drawing element corresponding to element number 2111 has been adjusted in length and position as shown.

The figure in drawing sheet 28/28 has been amended by replacing the figure label "Figure 21a" to "Figure 21b". The drawing on drawing sheet 28/28 as originally filed was represented with the figure label of "Figure 21b" but the Amendments to the Drawings submitted on 13 February 2009 was inadvertently amended to include "Figure 21a".

Remarks

The specification and drawings have been amended to correct minor errors noted in the Office Action and otherwise. These corrections are of a clerical nature and do not add "new matter".

Claims 1 and 13 have been previously cancelled without prejudice.

Claims 14-16, 20 and 22-27 are amended.

Claims 17-19 are cancelled without prejudice.

The text of original claim 21 and of previously added claims 28-31 remain unchanged but their meaning have changed because they depend from amended claims.

Request for Acknowledgement and Acceptance of Substitute Drawings Submitted on 13 February 2009

In the Office Action, the drawings filed on "29 December 2005", named the "Acknowledgment Date", were "accepted" by the Examiner. Applicants kindly note that the Drawings were amended and provided in the form of Replacement Sheets, collectively referred to herein as the "Amended Drawings", with the USPTO by the Applicants through the Response and Amendment to Office Action submitted with the USPTO on 13 February 2009, named the "Prior Response". The Acknowledgment Date used in the Office Action, however, reflects the original Application filing date of this application and thus, refers to the original Drawings rather than the Amended Drawings. With due respect, the Acknowledgement seems to be inadvertent, and consequently, Applicants request that the Amended Drawings previously submitted

in the Prior Response also be reviewed and acknowledged if applicable.

Amendments to The Current Drawings

Figures 19 and 21a, and the Figure on sheet 28/28 have been amended, and are provided in the form of replacement drawing sheets in accordance with 37 CFR 1.121. These amendments are described in detail in the "Amendments to the Drawings" section above.

Examiner Interview Conducted on 8 May 2009

Withdrawn claims 17-19 and 24-26 have been reconsidered by the Examiner because claim 17 has been amended to depend from claim 14 instead of claim 1 during the telephone interview, named "Examiner Interview", conducted between the undersigned and the Examiner on 8 May 2009. Accordingly, claims 17-19 and 24-26 have been entered for further consideration by the Examiner. The undersigned on behalf of the applicants extend much thanks to the Examiner for his responsiveness during the Examiner Interview.

The First 35 USC §112, Second Paragraph, Rejection

Claims 14-26 are rejected under 35 USC, second paragraph, as being indefinite for failing to particularly point out and distinctly claiming the subject matter which the applicant regards as the invention. The Applicants respectfully traverse this rejection.

In the Office Action, it is asserted that in:

base claim 1, applicants claimed "one or more passive port for passing though the one or more active signals". However, in light of applicants'

> discloser, as it would be interpreted by one of ordinary skill in the art, above claim limitations do not set out and define the invention with a reasonable degree of precision and particularity. For purpose of examination, Examiner assumes the "passive port" is a connection on active port for carrying signal.

Definiteness of claim language must be analyzed, not in a vacuum, but in light of Applicants written disclosure, the prior art, and the claim interpretation that would be given by one of ordinary skill in the art at the time the invention was made. MPEP 2173.02. Applicants may be their own lexicographers. MPEP 2173.01. The Specification at p. 21, line 7 through p. 22, line 4, as amended in the "Amendments to the Specification" section above, recites in part:

> ...A ***connection*** between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module, such as the X1 passive ball and X1 passive pad connection in Figure 19, is named "passive port", such as passive ports 1909 illustrated in Figure 19. (Emphasis added).

The above description should be read in conjunction with amended Figure 19, which shows that a passive port 1909 ***connects*** "a passive ball", such as passive ball X2, "on one surface of a SDRAM module", such as SDRAM module 0, and a passive pad", such as passive pad X3, "on another surface of the same DRAM module", such as SDRAM module 0. Thus, "a connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module" is a "passive port". The above amendments render moot the First 35 USC § 112,

Second Paragraph rejection as to claims 14-26, and the Specification and claims now comply with the statutory requirements.

In order to properly provide a complete response to the Office Action, please kindly note that the Office Action refers to "base claim 1". The applicants believe that this reference to "base claim 1" is inadvertent because base claim 1 has been withdrawn from consideration due to the earlier received Restriction Requirement, and consequently, the applicants have responded to this rejection with respect to base claim 14 from which claims 15 through 26 depend.

The Second 35 USC §112, Second Paragraph, Rejection

Claims 22-26 are rejected under 35 USC, second paragraph, as being indefinite for failing to particularly point out and distinctly claiming the subject matter which the applicant regards as the invention. The Applicants respectfully traverse this rejection.

In the Office Action, it is asserted that

> in claims 22-23, applicants claimed "one or more passive ball and one or more passive pad". However, in light of applicants' discloser, as it would be interpreted by one of ordinary skill in the art, above claim limitations do not set out and define the invention with a reasonable degree of precision and particularity. For purpose of examination, Examiner assumes the "passive port inherently comprises passive ball and passive pad".

The Specification as amended beginning from p. 21, line 7 through p. 22, line 4,

recites in part:

> ...A ***connection*** between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module, such as the X1 passive ball and X1 passive pad connection in Figure 19, is named "passive port", such as passive ports 1909 illustrated in Figure 19. (Emphasis added).

The above description should be read in conjunction with amended Figure 19, which shows that a passive port 1909 ***connects*** "a passive ball", such as passive ball X2, "on one surface of a SDRAM module", such as SDRAM module 0, and a passive pad", such as passive pad X3, "on another surface of the same DRAM module", such as SDRAM module 0. Thus, the recitation of "one or more passive ball and one or more passive pad" by the rejected claims particularly points out and distinctly claims the invention. By these amendments, the Second 35 USC § 112, Second Paragraph rejection has been rendered moot as to claims 14-26, and the Specification and claims now comply with the statutory requirements.

The Third 35 USC §112, Second Paragraph, Rejection

Claims 17-19 and 24-26 are rejected under 35 USC, second paragraph, as being indefinite for failing to particularly point out and distinctly claiming the subject matter which the applicant regards as the invention. The Applicants respectfully traverse this rejection.

In the Office Action with respect to claim 17, it is asserted that:

> ...applicants claimed "one or more pair of daisy chain input port and daisy chain output port ". However, in light of applicants' discloser, as it would be interpreted by one of ordinary skill in the art, above claim limitations do not set out and define the invention with a reasonable degree of precision and particularity. For purpose of examination, Examiner assumes the "limitation associated with daisy chain will read as ladder like routing path connection".

The Specification at page 23, line 14 through page 24, line 20; Figure 21a; and the above claims have been amended so that these claims now particularly point out and distinctly claim the subject matter regarded as the invention by the Applicants. Support for the amendment made in the Specification is supported by the originals claims, including claim 17, 18, 24, and 25. The Specification and these claims now comply with the statutory requirements, rendering the Third Section 112 Rejection moot.

The First 35 USC §102 Rejection

Claims 14-15 and 17-31 are rejected under 35 USC 102(b) as being anticipated by Kyougoku et al. (Kyougoku, US 5,995,379) of record.

The First 35 USC §102(b) Rejection

In the Office Action, claims 14-15 and 17-31 have been rejected under 35 USC 102(b) as being allegedly anticipated by Kyougoku et al. (Kyougoku, US 5,995,379) of record. This rejection is respectfully traversed.

In the Office Action it is asserted that with respect to claim 14, "Kyougoku

shows a stacked module (Fig. 5) comprising: one or more active port (B1) for carrying one or more active signal (Fig. 5); and one or more passive port (L1, L4) for passing through the one or more active signals (Fig. 5).

Independent Claim 14

Amended claim 14, recites in part:

> a first serial chain route that includes at least one serial chain connection, the serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output; said serial chain input coupled to said serial chain output through said serial chain circuit;
>
> a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module; and
>
> said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module.

Kyougoku fails to teach or disclose the above claim limitations, and hence, claim 14 is allowable.

Dependent Claim 15

In the Office Action it is also asserted that with respect to claim 15, "Kyougoku shows the one or more passive port forms a ladder like routing path (L1-L6)." Applicants respectfully traverse this rejection.

Claim 15 depends on allowable base claim 14. Thus, claim 15 is also allowable for the same reasons stated for base claim 14 since an allowable base claim renders its dependent claim(s) also allowable.

Dependent Claims 17-19

Dependent claims 17-19 have been cancelled without prejudice. In addition, claim 14, recites additional claim limitations that are not shown or disclosed by the arguments presented in the Office Action with respect to claims 17-19. For example, claim 14, recites a "control circuit disposed to enable the routing path in response to a control input signal", which is not shown in Kyougoku. Consequently, claim 14 is also allowable for this additional reason.

Dependent Claims 20-21

Claims 20-21 ultimately depend on allowable base claim 14. Thus, claims 20-21 are also allowable for the same reasons stated for base claim 14 above since an allowable base claim renders its dependent claims also allowable.

Dependent Claims 22-23

Claims 22-23 ultimately depend on allowable base claim 14. Thus, claims 22-23 are also allowable for the same reasons stated for base claim 14 above since an allowable base claim renders its dependent claims also allowable.

Dependent Claims 24-26

Claims 24-26 ultimately depend on allowable base claim 14. Thus, claims 24-26 are also allowable for the same reasons stated for base claim 14 above since an allowable base claim renders its dependent claims also allowable.

In addition, claim 25 recites in part, "wherein the routing path includes one or more tri-state driver controlled by the control circuit", which is not taught or disclosed in Kyougoku. For this additional, reason claim 25 is allowable.

In addition, claim 26 recites one or more additional claim limitations that are not disclosed or taught in Kyougoku. For example, claim 26 recites in part, "a main board coupled to another stacked module having a third serial chain route". In another example, claim 26 recites in part, "another control circuit for enabling another routing path that connects the second serial chain route with the third serial chain route". Consequently, since Kyougoku does not disclose or teach one or both of these additional claim limitations, claim 26 is allowable for these additional reasons.

Dependent Claims 27-31

Claims 27-31 ultimately depend on allowable base claim 14. Thus, claims 27-31 are also allowable for the same reasons stated for base claim 14 above since an allowable base claim renders its dependent claims also allowable.

The Second 35 USC §102(b) Rejection

In the Office Action, claims 14-15 have been rejected under 35 USC 102(b) as being allegedly anticipated by Beausoleil et al. (Beausoleil, US 6,469, 375). This rejection is respectfully traversed.

In the Office Action it is asserted that with respect to claim 14, "Beausoleil shows a plurality of modules each comprising comprising: one or more active port 18 (see attached Fig. 1) for carrying one or more active signal (Fig. 1); and one or

more passive port (see attached Fig. 1) for passing through the one or more active signals.

Independent Claim 14

Amended claim 14, recites in part:

> a first serial chain route that includes at least one serial chain connection, the serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output; said serial chain input coupled to said serial chain output through said serial chain circuit;
>
> a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module; and
>
> said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module.

Beausoleil fails to teach or disclose the above claim limitations, and hence, claim 14 is allowable.

Dependent Claim 15

In the Office Action it is also asserted that with respect to claim 15, "Beausoleil shows wherein the one or more passive port forms a ladder like routing path (see attached Fig. 1)." Applicants respectfully traverse this rejection.

Claim 15 depends on allowable base claim 14. Thus, claim 15 is also allowable

for the same reasons stated for base claim 14 since an allowable base claim renders its dependent claim(s) also allowable.

The First 35 USC §103 Rejection

The Examiner rejects claim 16 by asserting this claim is allegedly unpatentable over Beausoleil et al. (Beausoleil, US 6,469,375). This rejection is respectfully traversed.

In the Office Action it is asserted that with respect to claim 16:

> Beausoleil teaches one or more of the plurality of module 14 (Fig. 1) and stacked one or more passive port (see attached Fig. 1), but fails teach module is rotated before being stacked and the one or more passive port forms a rotational routing path. However, Applicants have no support data, which convinces that the particular claimed configuration is significant or is anything more than one of numerous configurations a person of ordinary skill in the art would find obvious for the purpose of providing mating surfaces. In re Dailey 149 USPQ 47,50 (CCPA 1966). See also Glue Co. v. Upton 97 US 3,24 (USSC 1878)., see MPEP 2144.04.

Claim 16 depends from claim 1, which recites limitations not taught or suggested by Beausoleil. For example, claim 1 recites in part:

> a first serial chain route that includes at least one serial chain connection, the serial chain connection including: a serial chain circuit, a

serial chain input, and serial chain output; said serial chain input coupled to said serial chain output through said serial chain circuit;

a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module; and

said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module.

Consequently, claim 1 is not rendered obvious by Beausoliel for the above reason, rendering this Section 103 Rejection inapplicable here since an allowable base claim renders its dependent claims also allowable.

In addition, Applicants agree with the Examiner that Beausoleil "fails to teach" module is rotated before being stacked and the one or more passive port forms a rotational routing path." Applicants, however, kindly disagree that the limitation in claim 16 that recites "one or more passive port forms a rotational routing path" is without significance or "is anything more than one of a numerous configurations a person of ordinary skill in the art would find obvious". The cases cited in the Office Action do not apply here because In re Daily or Glue Co. v. Upton, simply hold that structures that are a "mere matter of choice", or are not a new means "by which a desirable change in the form of a common article of commerce is obtained", respectively. Indeed, if the configuration recited by this claim limitation is so "numerous" so that it would be found obvious, a suitable prior art reference would be

readily available. The lack of such a reference precludes the Applicants from adequately responding to the Section 103 rejection on the merits.

Further, pursuant to MPEP 2144.04, the significance of the limitations recited in claim 16 is presented in by the Specification (Substitute Specification submitted on 13 February 2009) at p. 21, line 18 through p. 22, line 21; and Figures 20a and 20b.

Consequently, under any of the above additional reasons, the Section 103 rejection does not apply here, rendering claim 16 allowable.

Petition for Extension of Time

A Petition for an Extension of Time is submitted in a separate paper and filed on even date herewith.

Request for Allowance

It is believed that this Amendment places this Application into condition for allowance. Early favorable consideration of this Amendment is earnestly solicited.

Respectfully submitted,

Dated: 13 November 2009

/Stephen R. Uriarte/
Stephen R. Uriarte, Reg. No. 40,854

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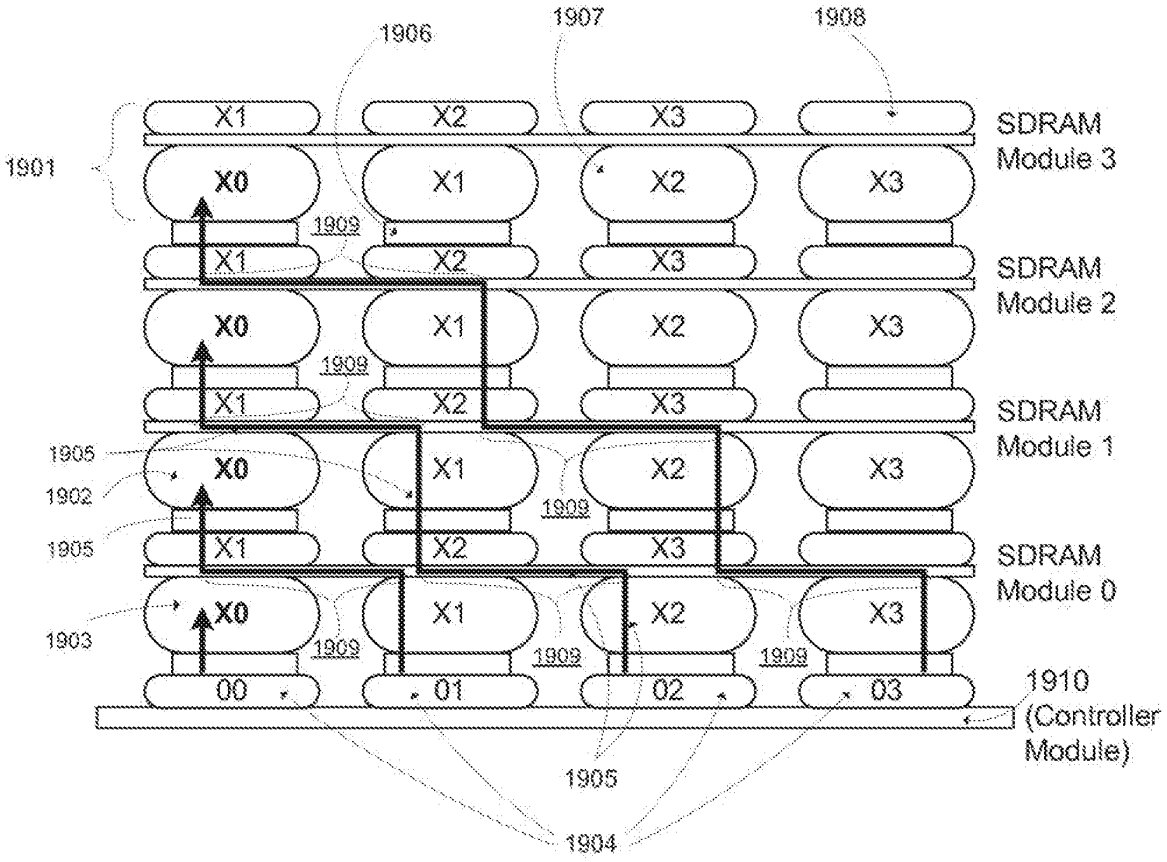

1906
1907
1908
1901
X1
X2
X3
X0
SDRAM Module 3
SDRAM Module 2
SDRAM Module 1
SDRAM Module 0
1909
1905
1902
1903
00
01
02
03
1910
(Controller Module)
1904

Figure 19

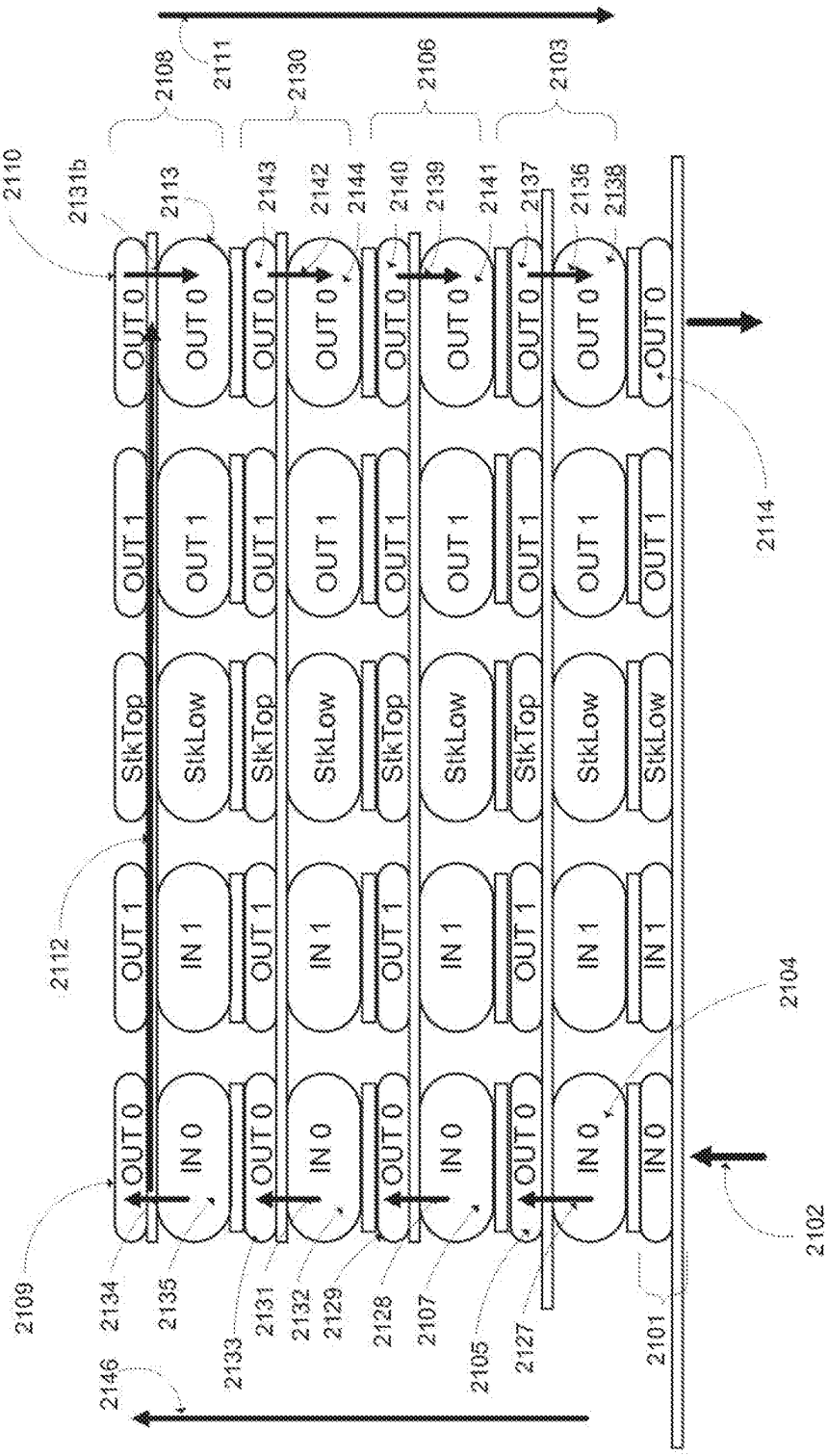

2108
2111
2130
2106
2103
2110
2131b
2113
2143
2142
2144
2140
2139
2141
2137
2136
2138
OUT 0
OUT 1
StkTop
StkLow
IN 1
IN 0
2114
2112
2104
2102
2109
2134
2135
2133
2131
2132
2129
2128
2107
2105
2127
2101
2146

Figure 21a

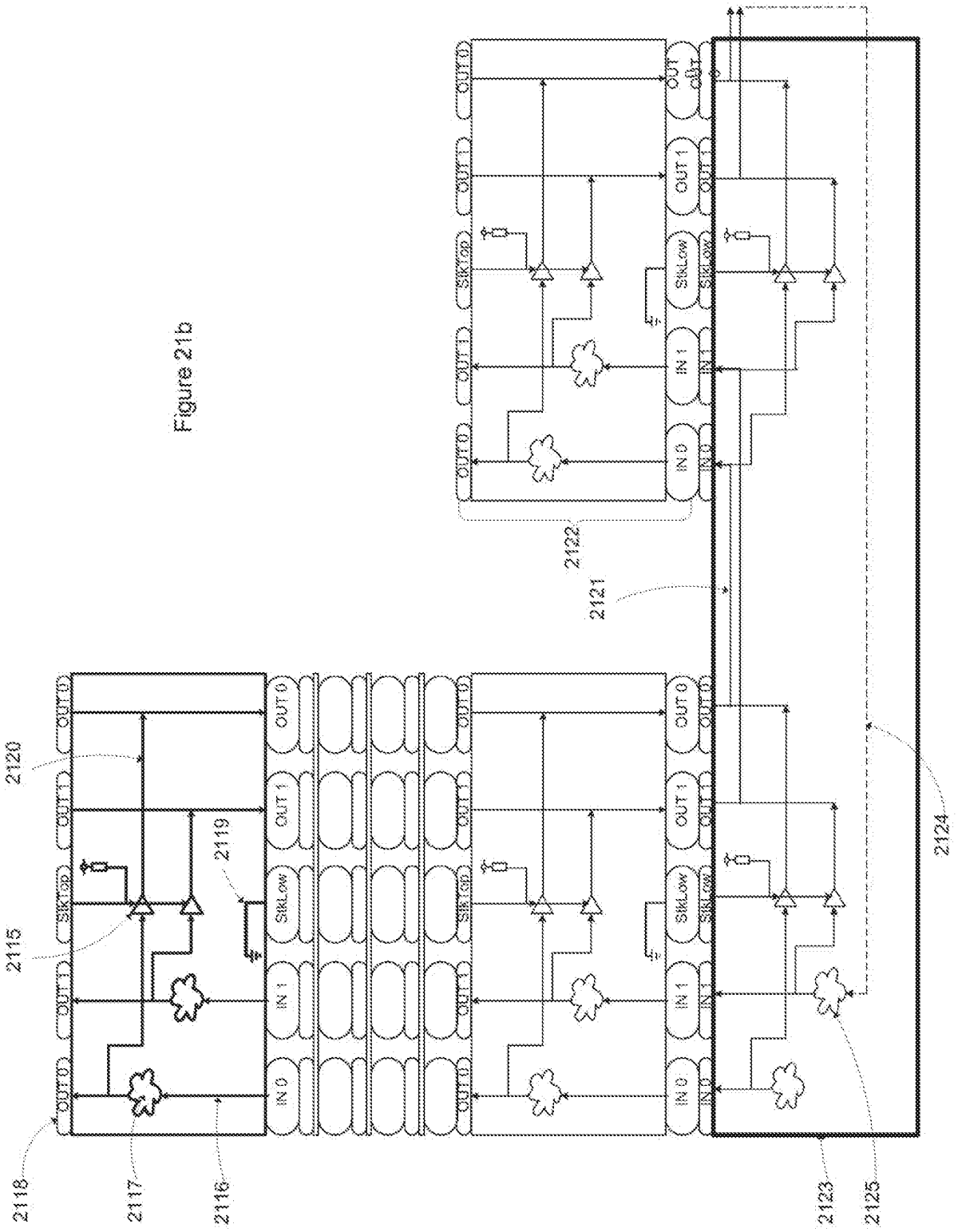

OUT 0
OUT 1
SIKTop
SIKLow
IN 1
IN 0
2120
2119
2115
2118
2117
2116
2122
2121
2124
2123
2125

Figure 21b

Attorney Docket#: 6005.011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: BRUCE et al.	Group Art Unit: 2892
Serial No.: 11/322,442	Examiner: ULLAH, Elias
Application Filing Date: 29 Dec 2005	
For: MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)

Dear Sir:

In conjunction with the Response to the Office Action, submitted on even date herewith, this is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and fee are as follows, indicated below:

Fees Paid:

____	One month (37 CFR 1.17(a)(1))	Fee (small entity: $65.00)	0.00
____	Two months (37 CFR 1.17(a)(2))	Fee (small entity: $245.00)	0.00
X	Three months (37 CFR 1.17(a)(3))	Fee (small entity: **$555.00**)	**Paid**

Entity Status:

X Applicant claims small entity status. (See 37 CFR 1.27)

Payment Method:

X Payment by credit card through EFS-web is provided.

Authorization to Charge/Credit Fees and Constructive Petition for Extension of Time –All Replies

X The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number: **50-4068**.

Please treat this authorization to charge all required fees under 37 CFR 1.17 as a constructive petition for an extension of time in accordance with 37 CFR 1.136(a)(3).

The undersigned is the attorney of record. Registration #: 40,854

Sincerely,

Signature:	/Stephen R. Uriarte/	Date:	13 November 2009
Name:	Stephen R. Uriarte	Telephone:	408.244.2164x111

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Electronic Patent Application Fee Transmittal	
Application Number:	11322442
Filing Date:	29-Dec-2005
Title of Invention:	Multiple chip module and package stacking method for storage devices
First Named Inventor/Applicant Name:	Rey Bruce
Filer:	Stephen Radcliff Uriarte
Attorney Docket Number:	6005.011
Filed as Small Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 3 months with $0 paid	2253	1	555	555

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	555

Electronic Acknowledgement Receipt

EFS ID:	6455114
Application Number:	11322442
International Application Number:	
Confirmation Number:	5045
Title of Invention:	Multiple chip module and package stacking method for storage devices
First Named Inventor/Applicant Name:	Rey Bruce
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.011
Receipt Date:	13-NOV-2009
Filing Date:	29-DEC-2005
Time Stamp:	21:34:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$555
RAM confirmation Number	8435
Deposit Account	504068
Authorized User	URIARTE,STEPHEN R.

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

File Listing: ATTACHMENT "A"

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	6005_011_2ndRsp2OA_20091113F.pdf	206580	no	33
Warnings:					
Information:					
2	Drawings-only black and white line drawings	6005_011_F19_F21a_21b_rplcmnt_20091113.pdf	87810	no	3
Warnings:					
Information:					
3	Extension of Time	6005_011_2ndRsp2OA_NON_ExtTime_20091113.pdf	96809	no	2
Warnings:					
Information:					
4	Fee Worksheet (PTO-875)	fee-info.pdf	29792	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	420991		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 11/322,442	Filing Date 12/29/2005	☐ To be Mailed

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☒		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 = *		X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 = *		X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	11/13/2009	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 28	Minus	** 26	= 2	X $26 =	52	OR	X $ =	
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $110 =	0	OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE	52	OR	TOTAL ADD'L FEE	

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/ADRIENE D. SELLMAN/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

64180 7590 04/09/2010

URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

EXAMINER	
SOFOCLEOUS, ALEXANDER	
ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 04/09/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/322,442	12/29/2005	Rey Bruce	6005.011	5945

TITLE OF INVENTION: MULTIPLE CHIP MODULE AND PACKAGE STACKING METHOD FOR STORAGE DEVICES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$755	$300	$0	$1055	07/09/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

ATTACHMENT "B"

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

64180 7590 04/09/2010

URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/322,442	12/29/2005	Rey Bruce	6005.011	5045

TITLE OF INVENTION: MULTIPLE CHIP MODULE AND PACKAGE STACKING METHOD FOR STORAGE DEVICES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$755	$300	$0	$1055	07/09/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
SOFOCLEOUS, ALEXANDER	2824	365-063000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 .....
2 .....
3 .....

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies .....

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number ..... (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature ..... Date .....

Typed or printed name ..... Registration No. .....

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/322,442	12/29/2005	Rey Bruce	6005.011	5045

64180 7590 04/09/2010

URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

EXAMINER	
SOFOCLEOUS, ALEXANDER	
ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 04/09/2010

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 304 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 304 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Notice of Allowability	Application No. 11/322,442	Applicant(s) BRUCE ET AL.	
	Examiner ALEXANDER SOFOCLEOUS	Art Unit 2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Amendment filed November 13, 2009*.

2. ☒ The allowed claim(s) is/are *14-16 and 20-31*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Dang T Nguyen/
Primary Examiner, Art Unit 2824

DETAILED ACTION

1. This action is responsive to the following communication: the Amendment filed November 13, 2009.

2. Claims 14-16 and 20-31 are pending. Claims 1-13 and 17-19 are cancelled. Claims 14-16, 20, and 22-27 are currently amended. Claim 14 is independent.

EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Stephen Uriarte (Reg. No. 40,854) on March 18, 2010.

In the Claims, cancel **Claims 1-13** and **17-19**.[1]

In the Claims, **Claim 21**, line 1, change "The method of claim 20" to --The stacked module of claim 20--.

Specification

4. The substitute specification filed February 13, 2009 is acknowledged and acceptable. The proposed specification corrections received on November 13,

[1] While it is noted that each of claims 1-13 and 17-19 have the "(PREVIOUSLY CANCELLED)" status identifier, these claims include claim text and for purposes of promoting clarity during processing, claims 1-13 and 17-19 are formally cancelled by Examiner's Amendment.

2009 are acceptable.

Drawings

5. The replacement drawings (Figs. 1-21b) filed February 13, 2009 are acknowledged and acceptable. The replacement drawings (Figs. 19-21b) filed November 13, 2009 are acknowledged and acceptable.

Allowable Subject Matter

6. **Claims 14-16 and 20-31 are allowed.**

7. The following is an examiner's statement of reasons for allowance:

With respect to independent claim 14, there is no teaching, suggestion, or motivation for combination in the prior art to a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module, and the control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module, in combination with the other limitations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CONCLUSION

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Corisis et al. (U.S. Patent 6,381,141), Sasaki et al. (U.S. Patent 6,624,506), Gheewala (U.S. Patent 6,991,947), Adelmann (U.S. Patent 7,098,541), Koide (U.S. Patent 7,212,422), and Janzen (U.S. Patent 7,352,602).

Corisis et al. teach stacked module with signals serially coupled to each module.

Sasaki et al. teach a multichip memory device having stacked chips

Gheewala teaches plural IC dies with programmable interconnectivity.

Adelmann teaches a stacked die structure with blank pins and select lines.

Koide teaches a stacked memory device wherein each stacked memory chip includes a program circuit to set an address for selecting the chip.

Janzen teaches stacked memory with configurable input/output.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on M-F 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGS

/Dang T Nguyen/
Primary Examiner, Art Unit 2824

(12) **United States Patent**
Bruce et al.

(10) **Patent No.: US 7,826,243 B2**
(45) **Date of Patent: Nov. 2, 2010**

(54) **MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES**

(75) Inventors: **Rey Bruce**, San Jose, CA (US); **Ricardo Bruce**, Union City, CA (US); **Patrick Digamon Bugayong**, Mandaluyong (PH); **Joel Alonzo Baylon**, Cavite (PH)

(73) Assignee: **BiTMICRO Networks, Inc.**, Fremont, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 747 days.

(21) Appl. No.: **11/322,442**

(22) Filed: **Dec. 29, 2005**

(65) **Prior Publication Data**

US 2007/0158808 A1 Jul. 12, 2007

(51) **Int. Cl.**
G11C 5/02 (2006.01)

(52) **U.S. Cl.** **365/51**; 257/686; 257/777; 365/63; 365/230.03; 365/230.05

(58) **Field of Classification Search** 257/686, 257/777; 365/51, 63, 230.03, 230.05
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,854,507	A	12/1998	Miremadi et al.	
5,995,379	A *	11/1999	Kyougoku et al.	361/803
6,172,874	B1	1/2001	Bartilson	
6,381,141	B2 *	4/2002	Corisis et al.	361/735
6,392,896	B1	5/2002	Stoller	
6,469,375	B2 *	10/2002	Beausoleil et al.	257/686
6,624,506	B2 *	9/2003	Sasaki et al.	257/686
6,900,528	B2	5/2005	Mess et al.	
6,991,947	B1 *	1/2006	Gheewala	438/15
7,098,541	B2 *	8/2006	Adelmann	257/777
7,212,422	B2 *	5/2007	Koide	365/51
7,352,602	B2 *	4/2008	Janzen	365/63

FOREIGN PATENT DOCUMENTS

WO	9406210	A1	3/1994

OTHER PUBLICATIONS

Jeffrey C. Demmin, Novel 3-D Packaging Approaches Simplifying the Assembly and Test Supply Chain, Business Briefing: Global Semiconductor Manufacturing Technology, 2003, pp. 1-5.

Moody Dreiza, Akito Yoshida, Jonathan Micksch and Lee Smith, Stacked Package-on-Package Design Guidelines, Chip Scale Review, Jul. 2005, pp. 1-4, Reprinted by Amkor Technology, Inc. Chandler, Arizona.

ISA/US (Blaine Copenheaver), International Search Report and Written Opinion for International Application No. PCT/US06/62747, nine pages.

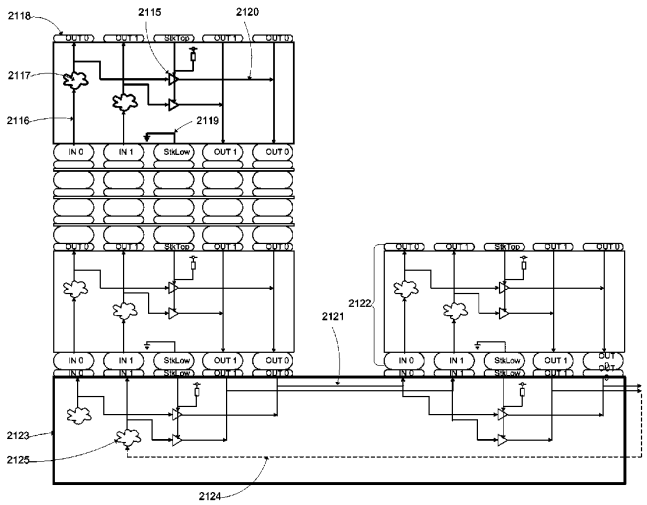
* cited by examiner

Primary Examiner—Dang T Nguyen
Assistant Examiner—Alexander Sofocleous
(74) *Attorney, Agent, or Firm*—Uriarte Law

(57) **ABSTRACT**

Stacking techniques are illustrated in example embodiments of the present invention wherein semiconductor dies are mounted in a module to become a MCM which serves as the basic building block. A combination of these modules and dies in a substrate creates a package with specific function or a range of memory capacity. Several example system configurations are provided using BGA and PGA to illustrate the stacking technique. Several pin assignment and signal routing techniques are illustrated wherein internal and external signals are routed from main board to various stacked modules. Expansion can be done both on the vertical and horizontal orientations.

15 Claims, 28 Drawing Sheets



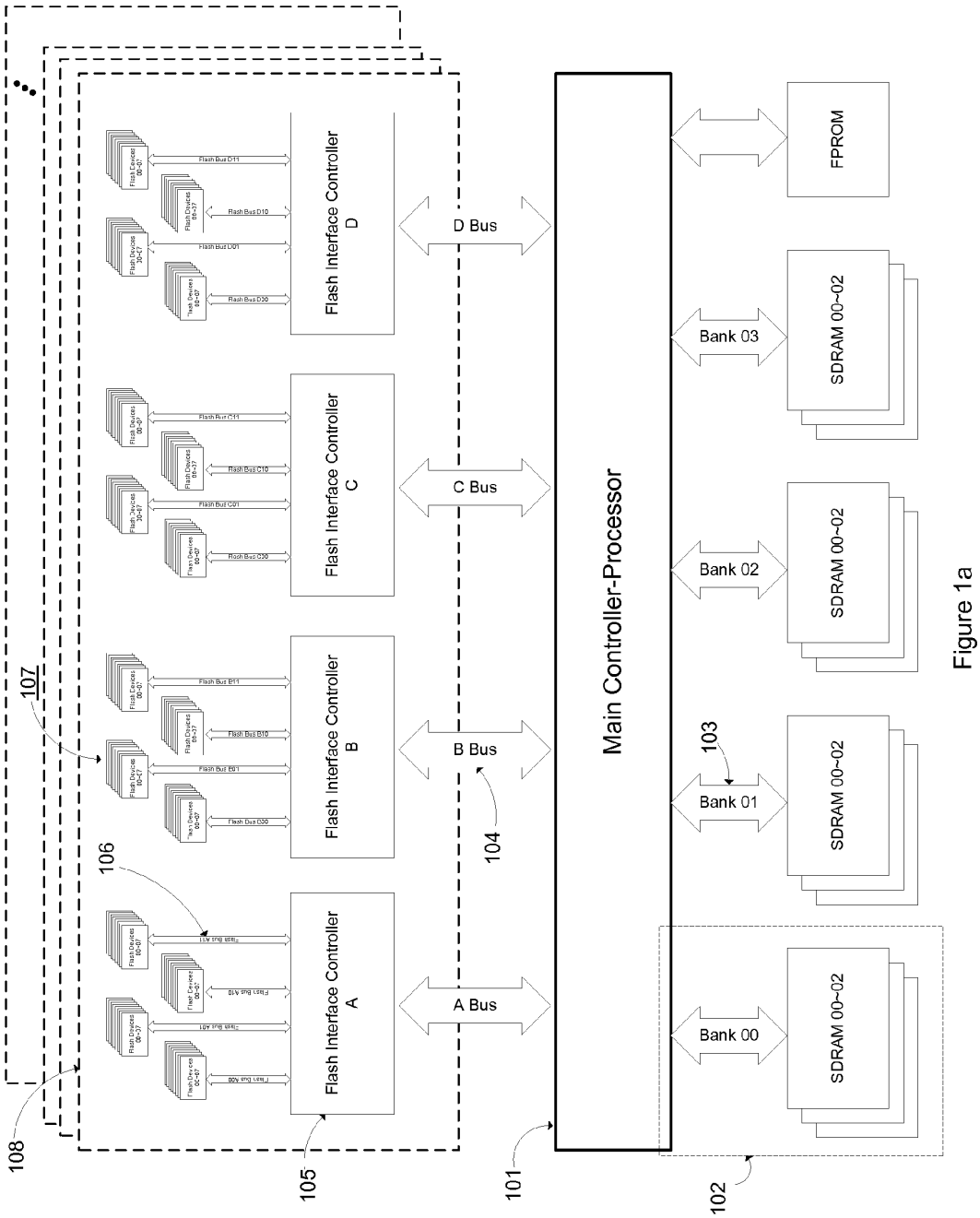

Flash Interface Controller D
Flash Interface Controller C
Flash Interface Controller B
Flash Interface Controller A
D Bus
C Bus
B Bus
A Bus
Main Controller-Processor
FPROM
Bank 03
Bank 02
Bank 01
Bank 00
SDRAM 00~02
SDRAM 00~02
SDRAM 00~02
SDRAM 00~02
101
102
103
104
105
106
107
108

Figure 1a

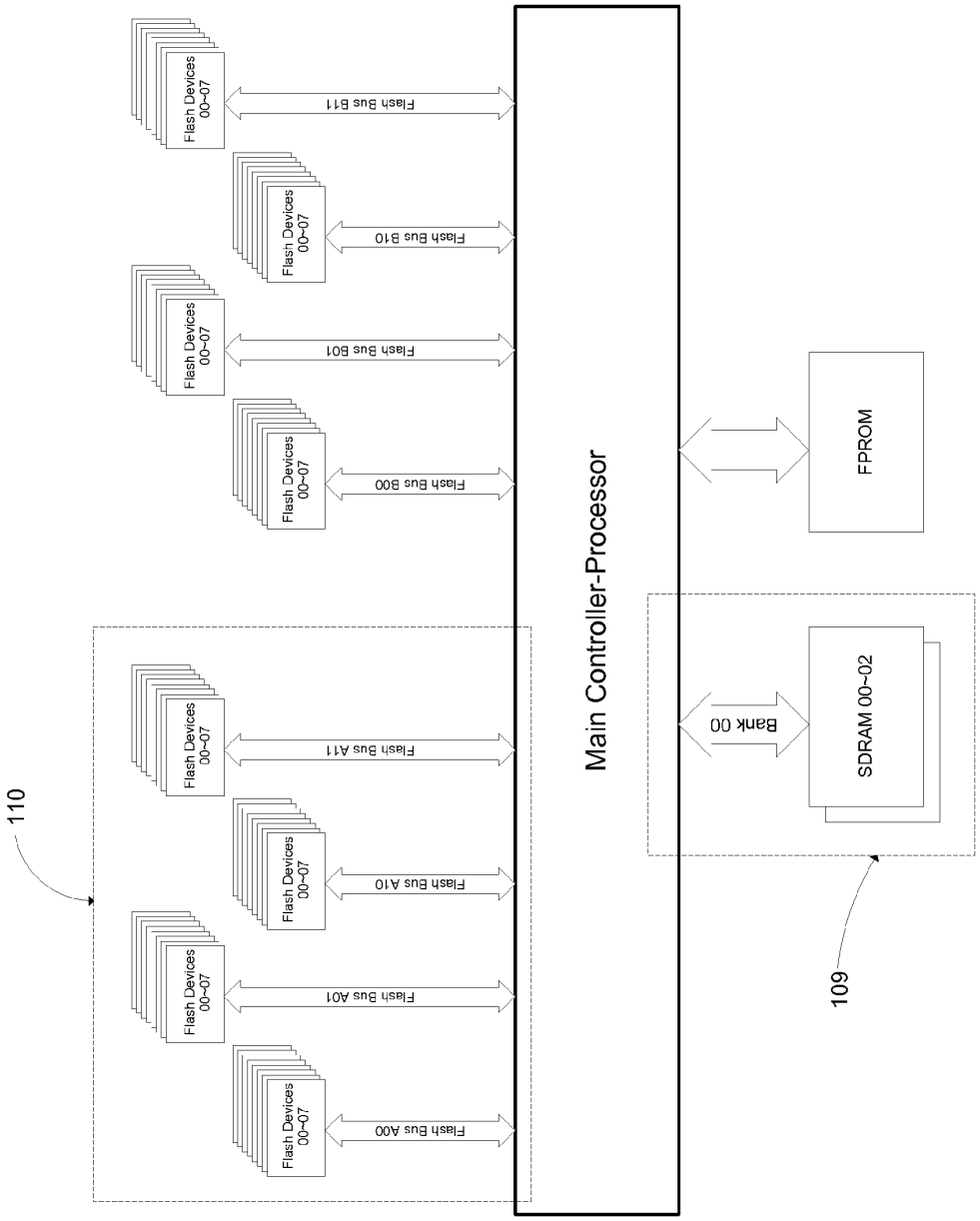

Flash Devices 00~07
Flash Bus B11
Flash Devices 00~07
Flash Bus B10
Flash Devices 00~07
Flash Bus B01
Flash Devices 00~07
Flash Bus B00
Main Controller-Processor
FPROM
Bank 00
SDRAM 00~02
109
110
Flash Devices 00~07
Flash Bus A11
Flash Devices 00~07
Flash Bus A10
Flash Devices 00~07
Flash Bus A01
Flash Devices 00~07
Flash Bus A00

Figure 1b

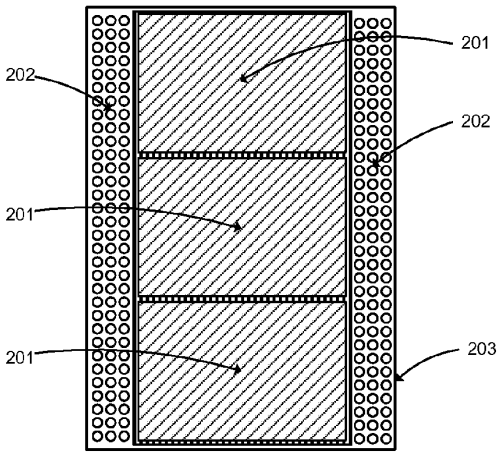


Figure 2a

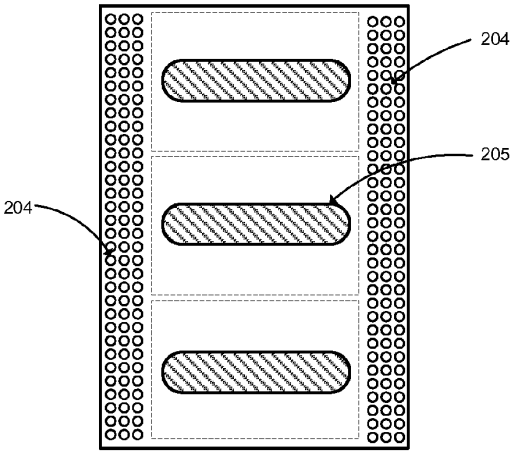


Figure 2b

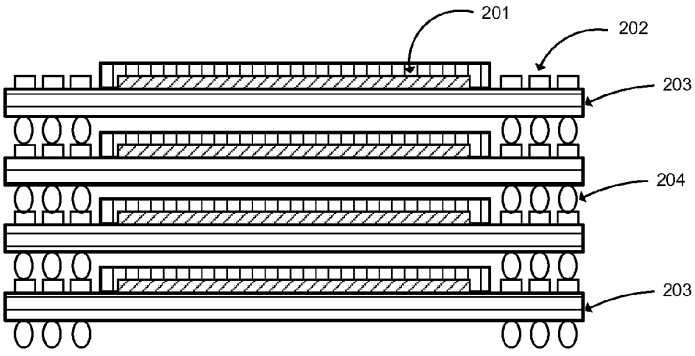


Figure 2c

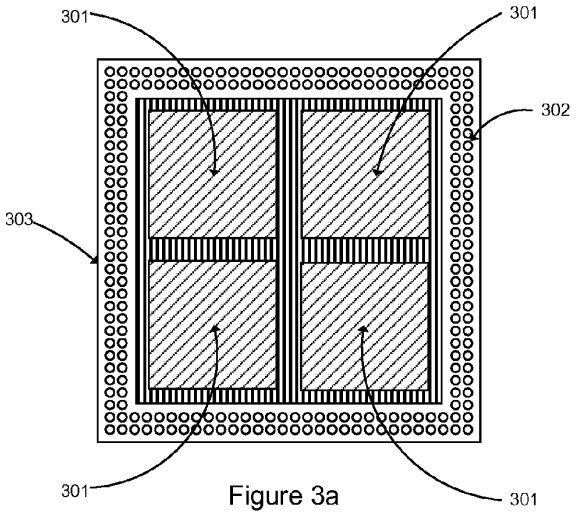


Figure 3a

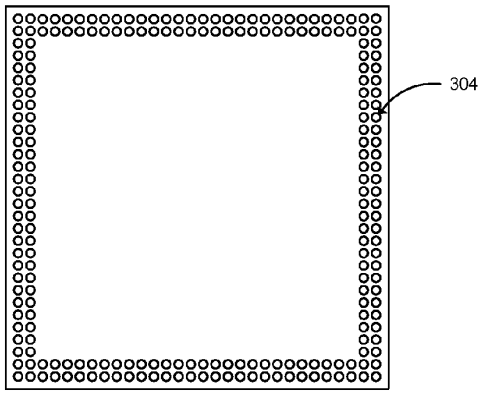


Figure 3b

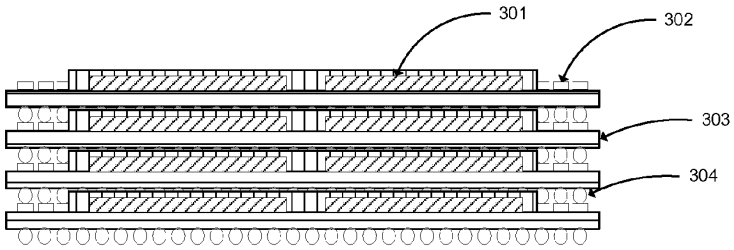


Figure 3c

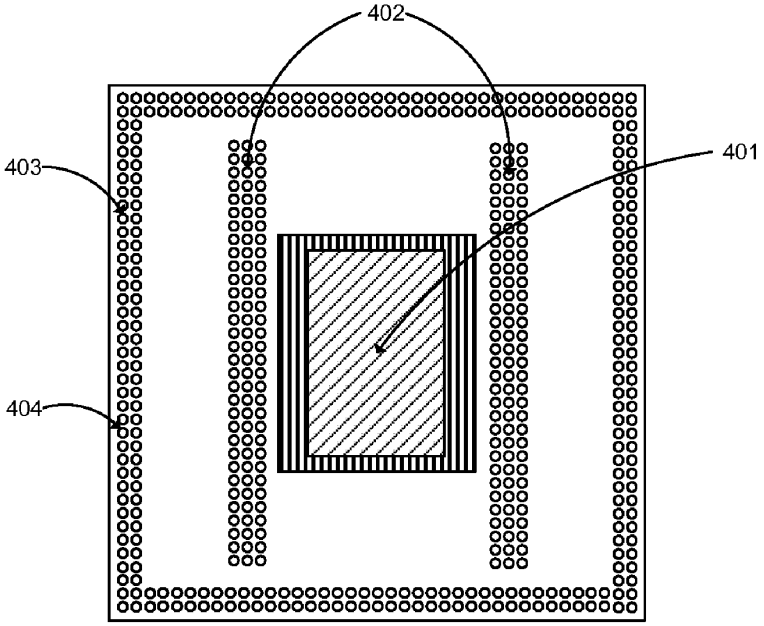


Figure 4a

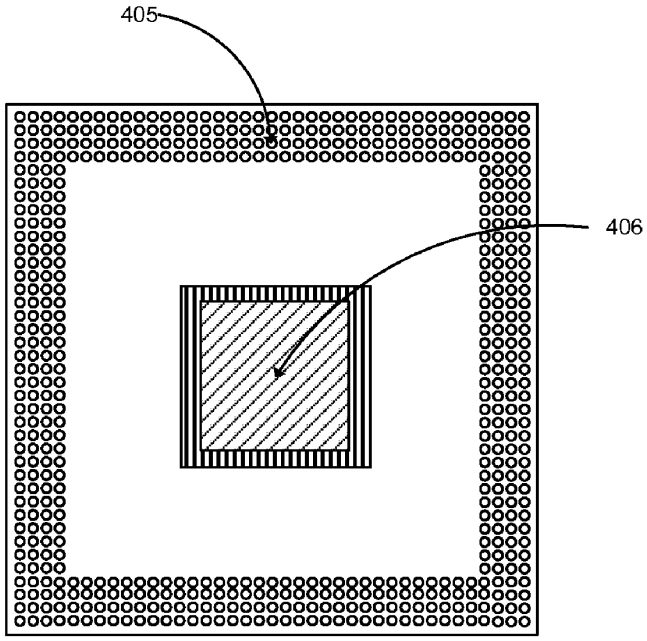


Figure 4b

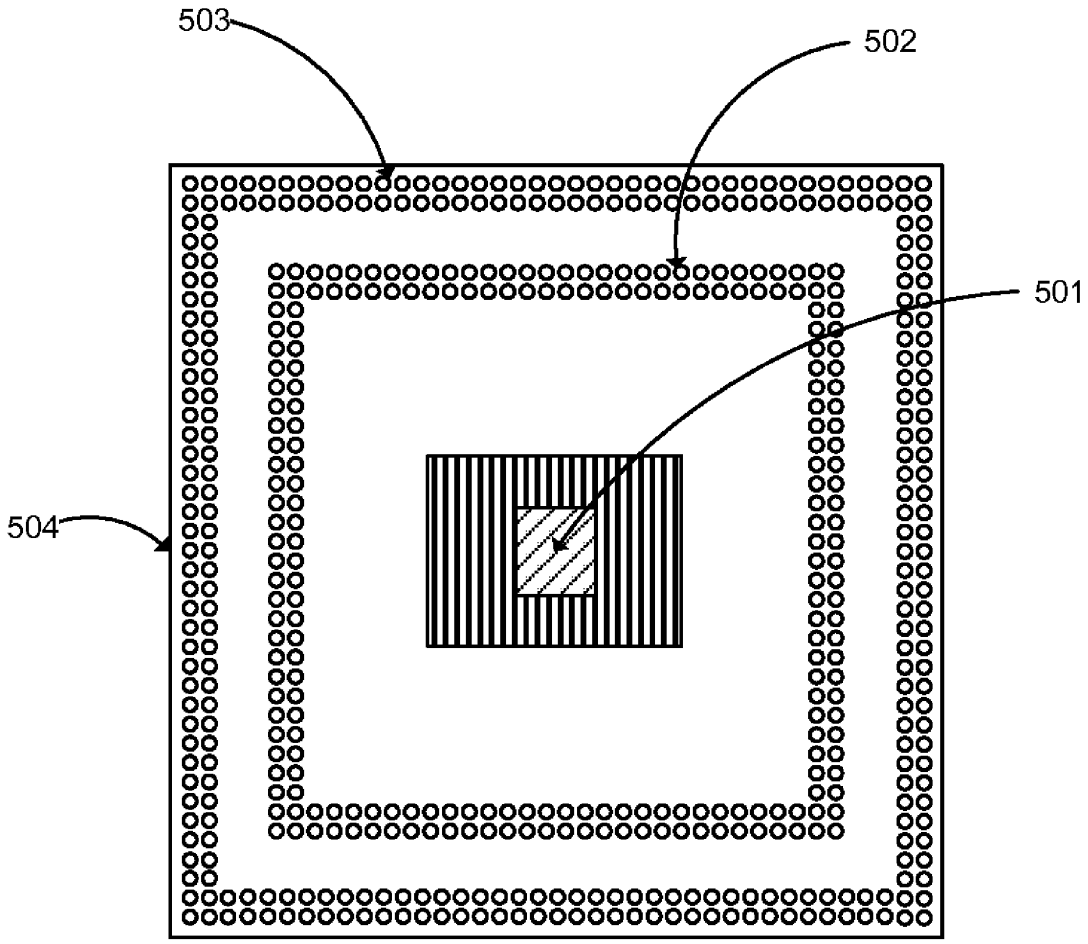


Figure 5a

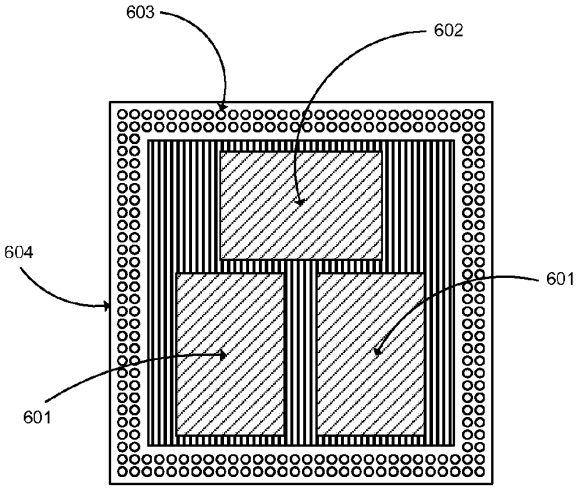


Figure 6a

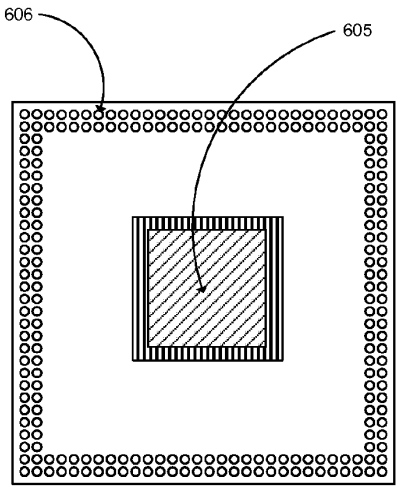


Figure 6b

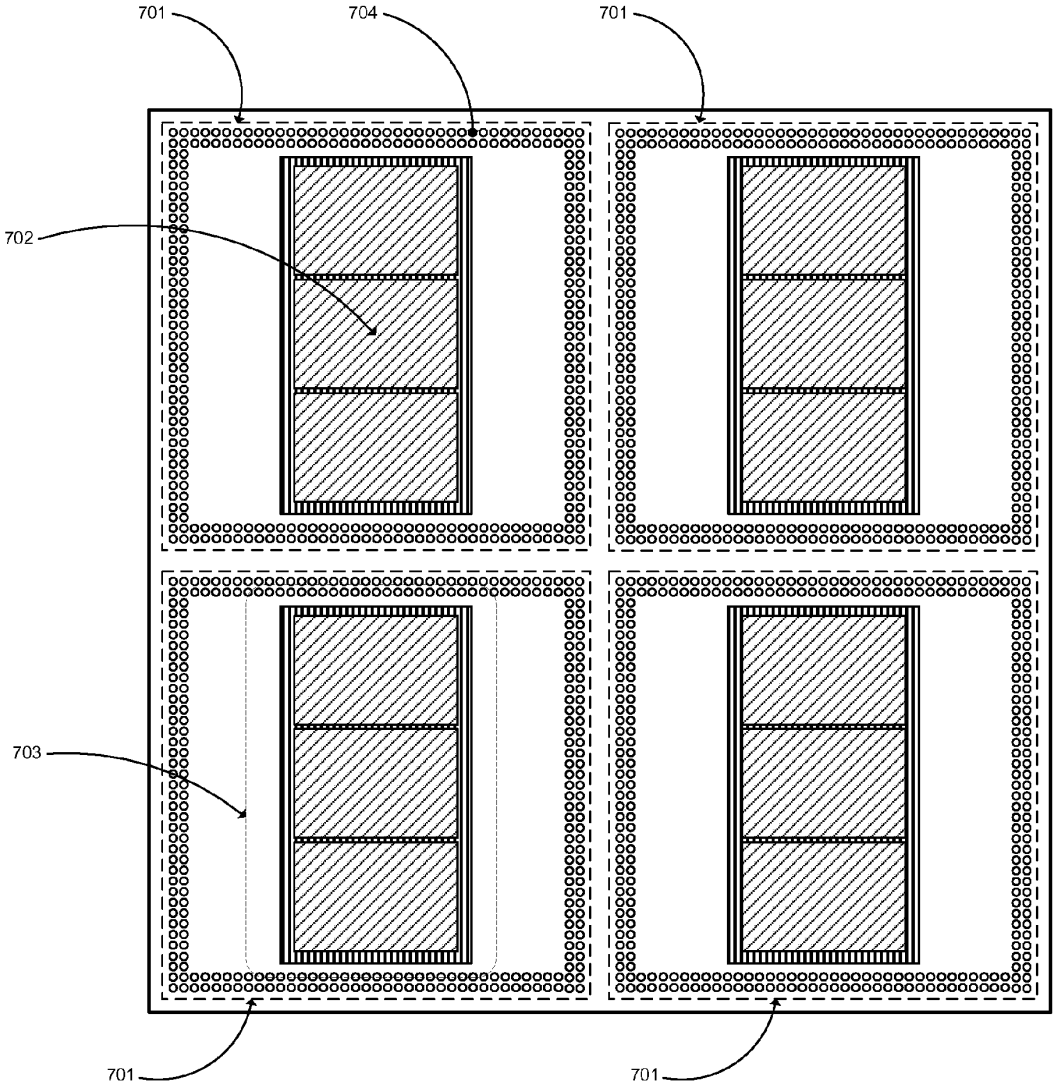


Figure 7a

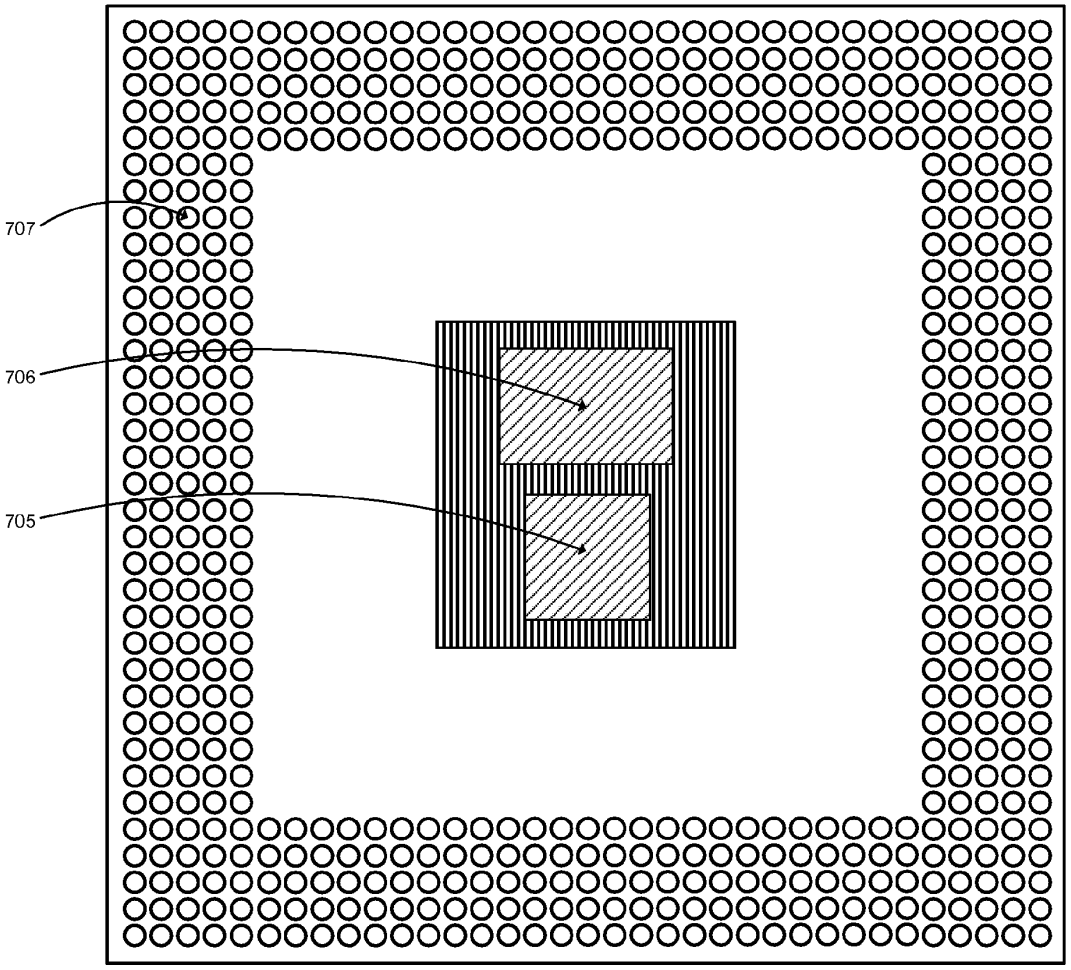


Figure 7b

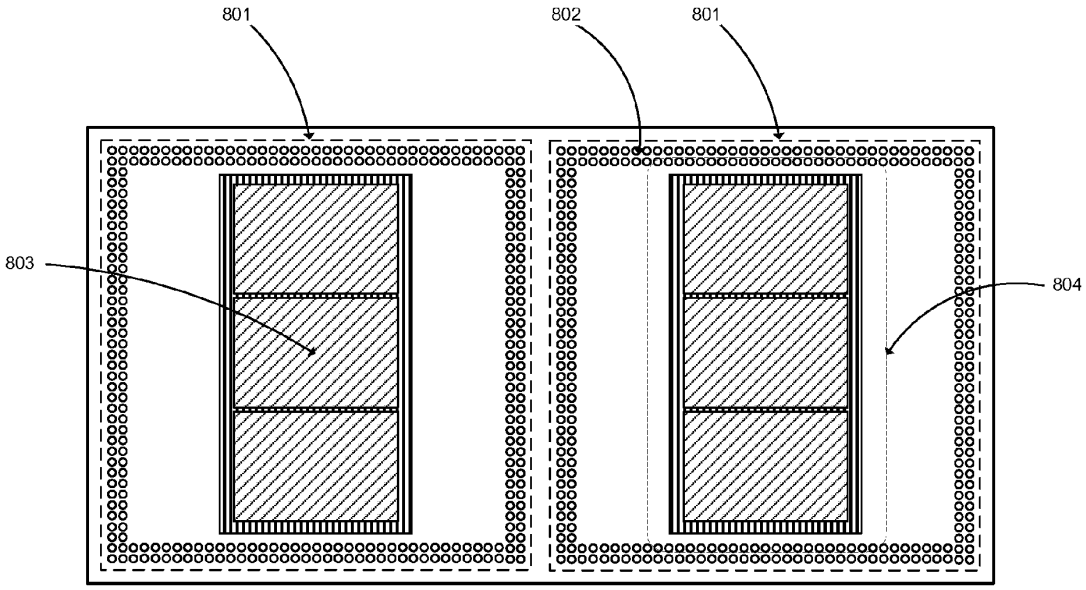


Figure 8a

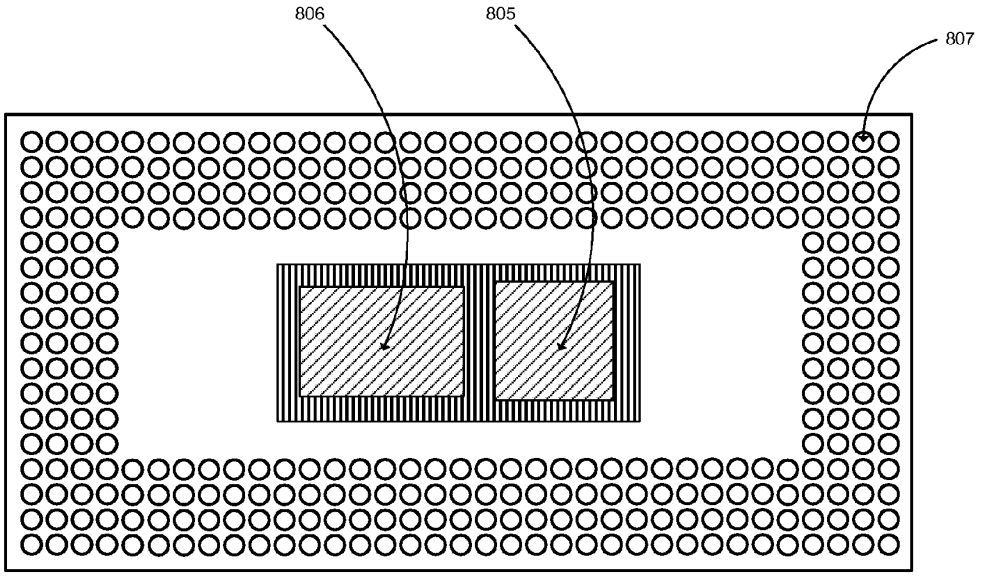


Figure 8b

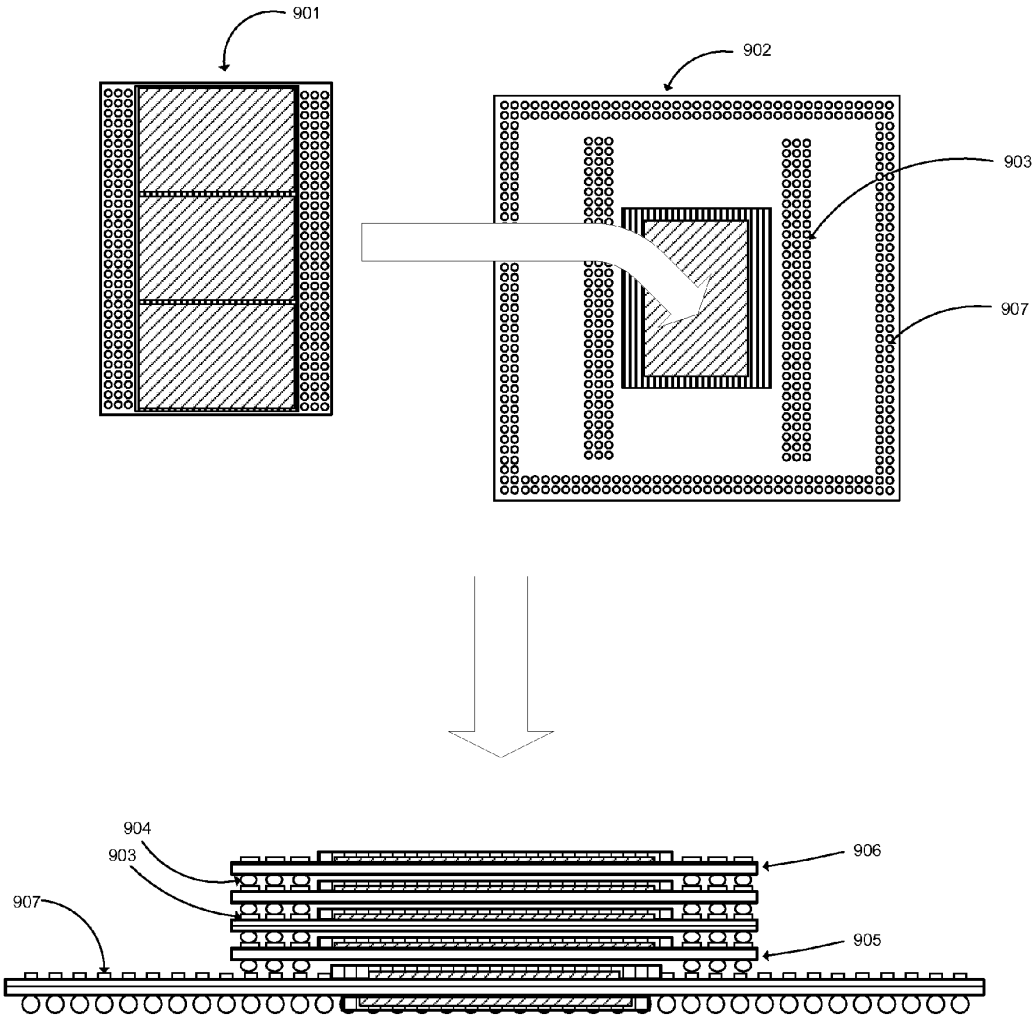


Figure 9

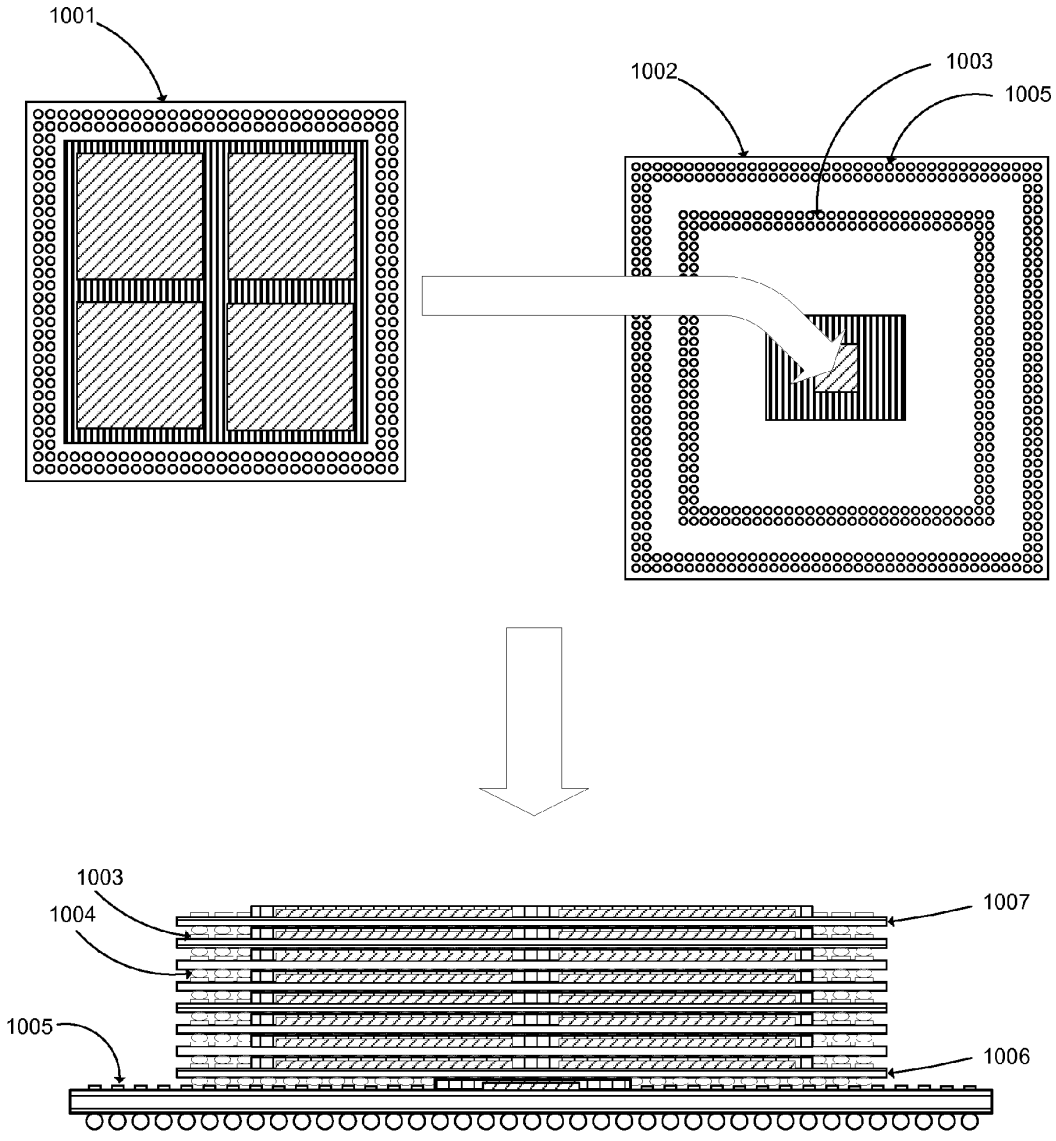


Figure 10

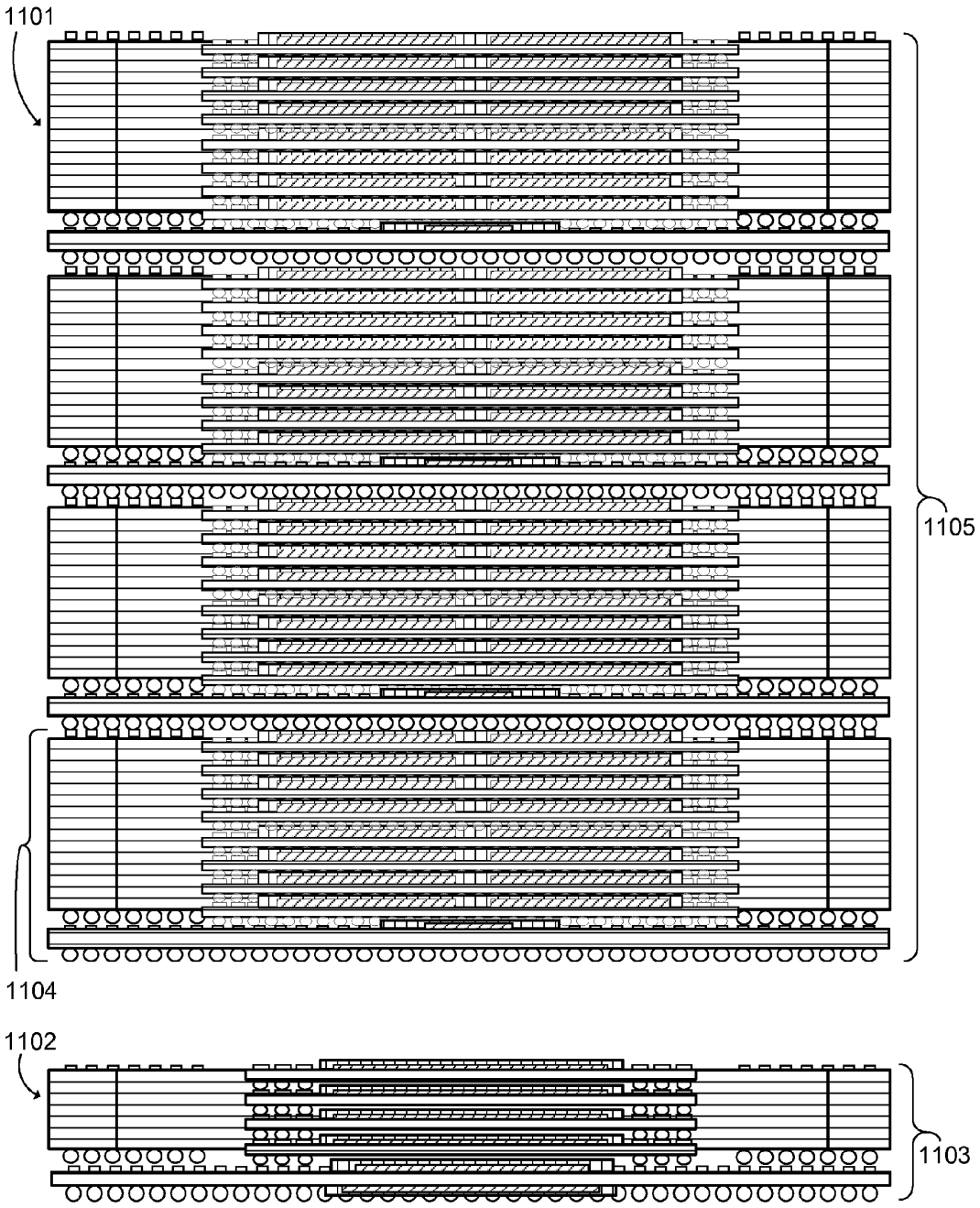


Figure 11

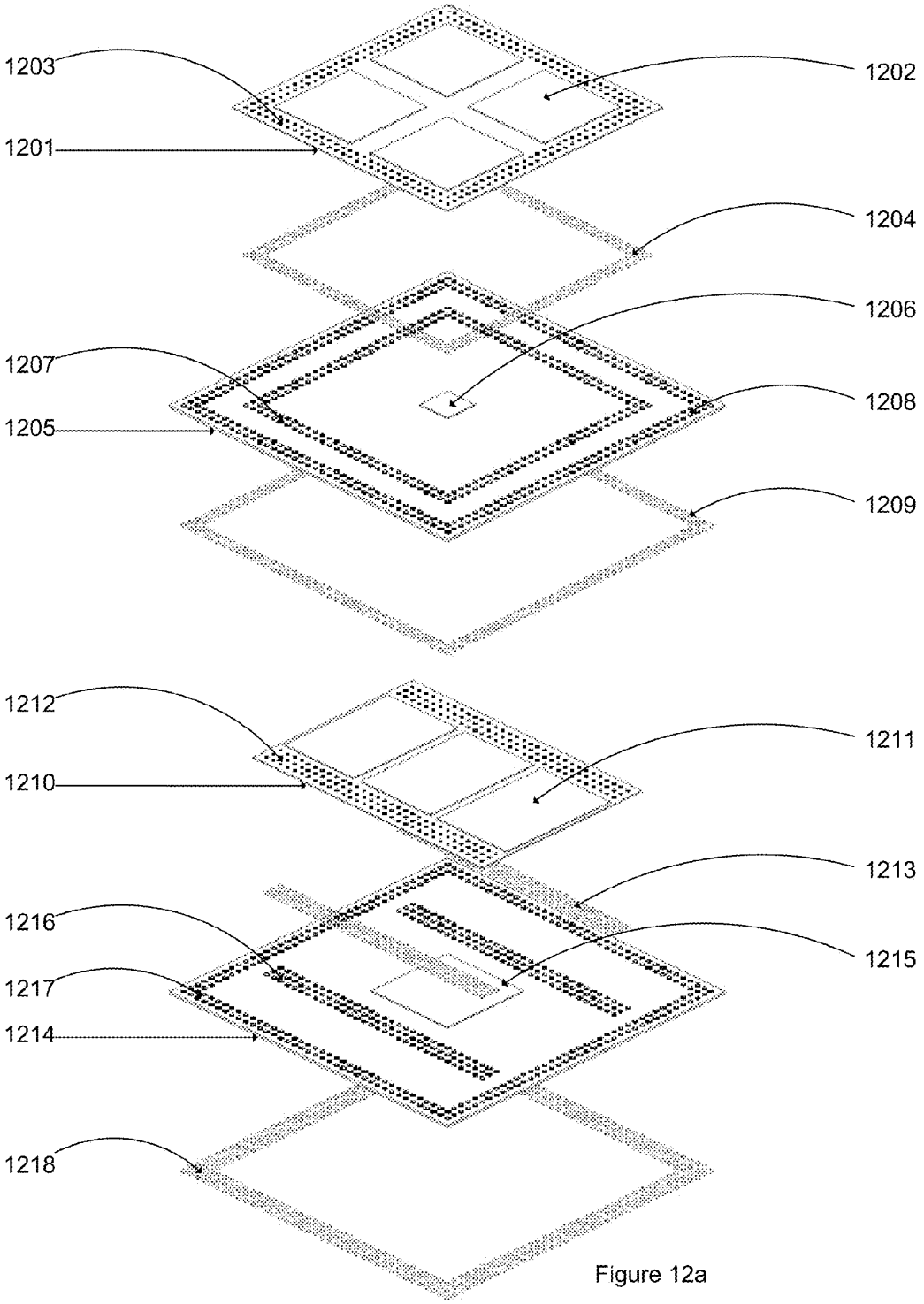

1203
1202
1201
1204
1206
1207
1208
1205
1209
1212
1211
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1216
1215
1217
1214
1218

Figure 12a

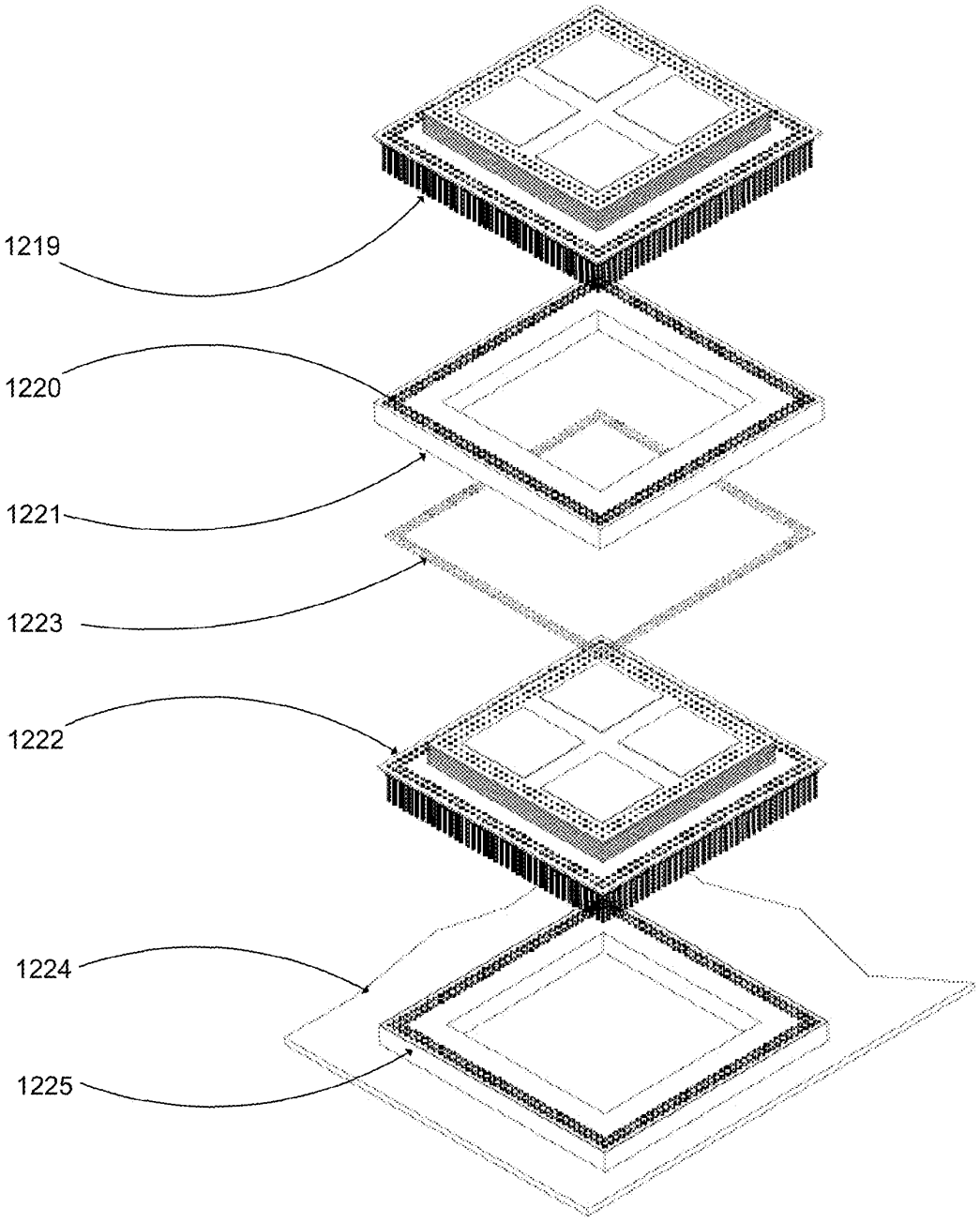


Figure 12b

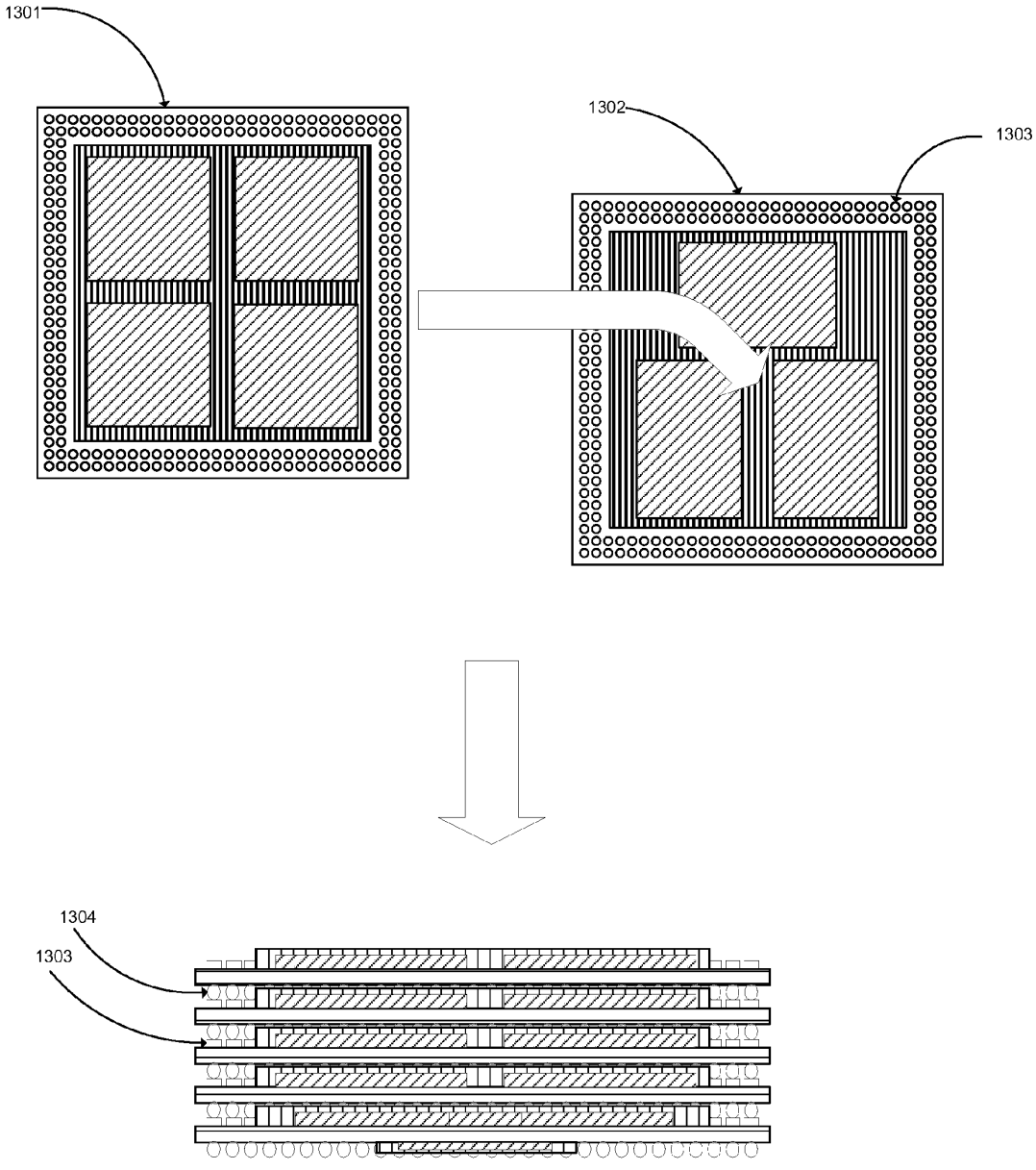


Figure 13

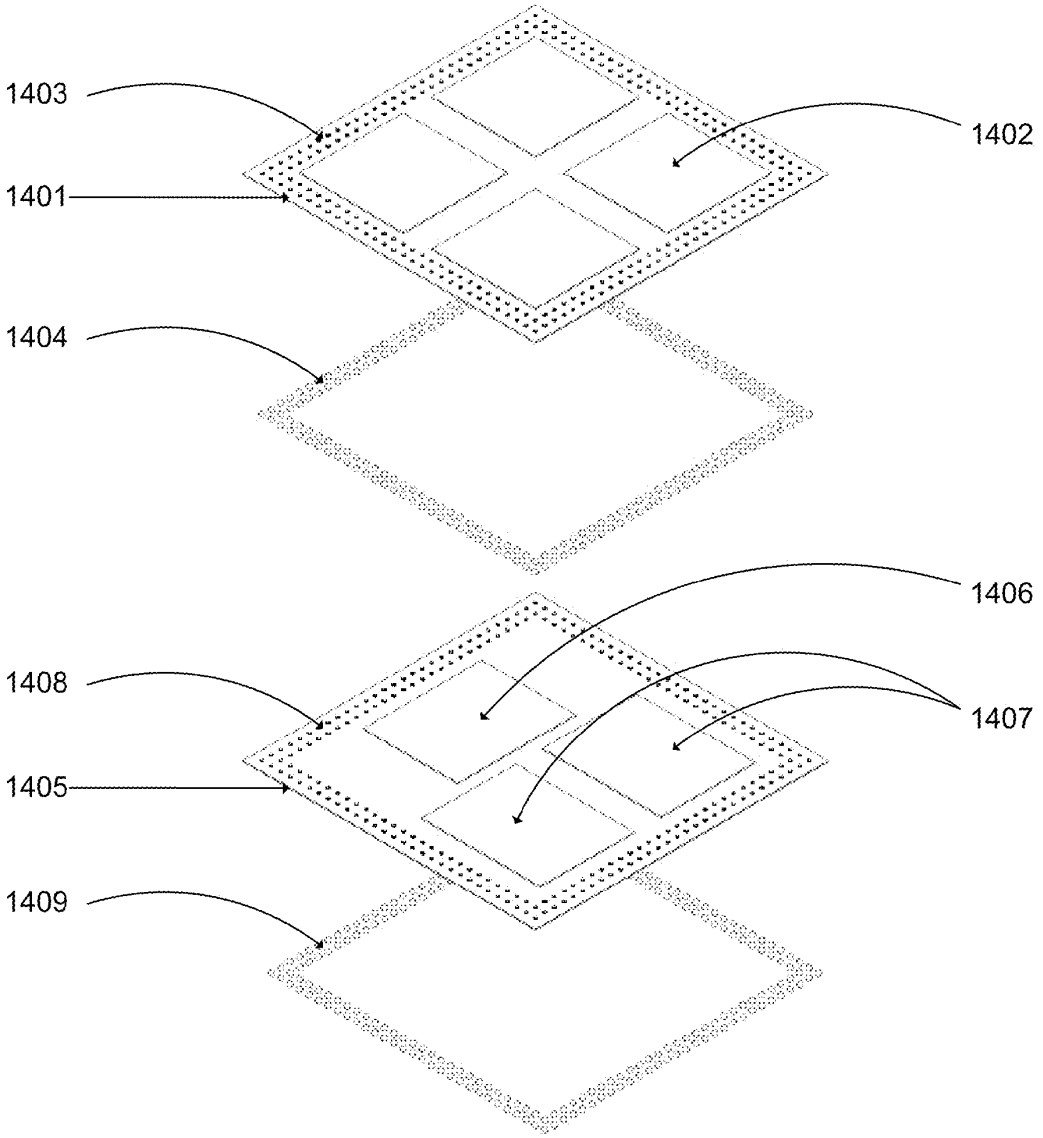


Figure 14

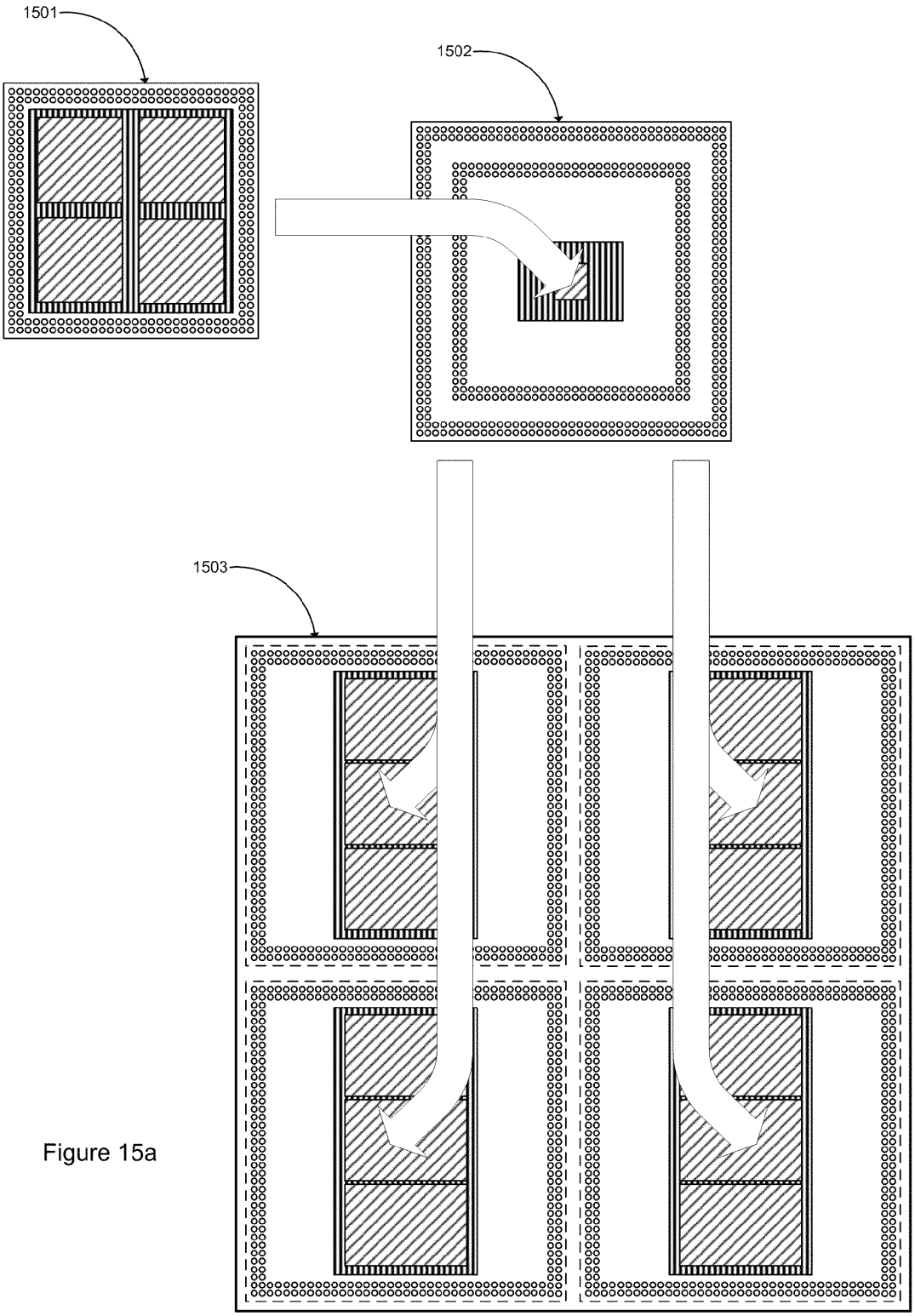


Figure 15a

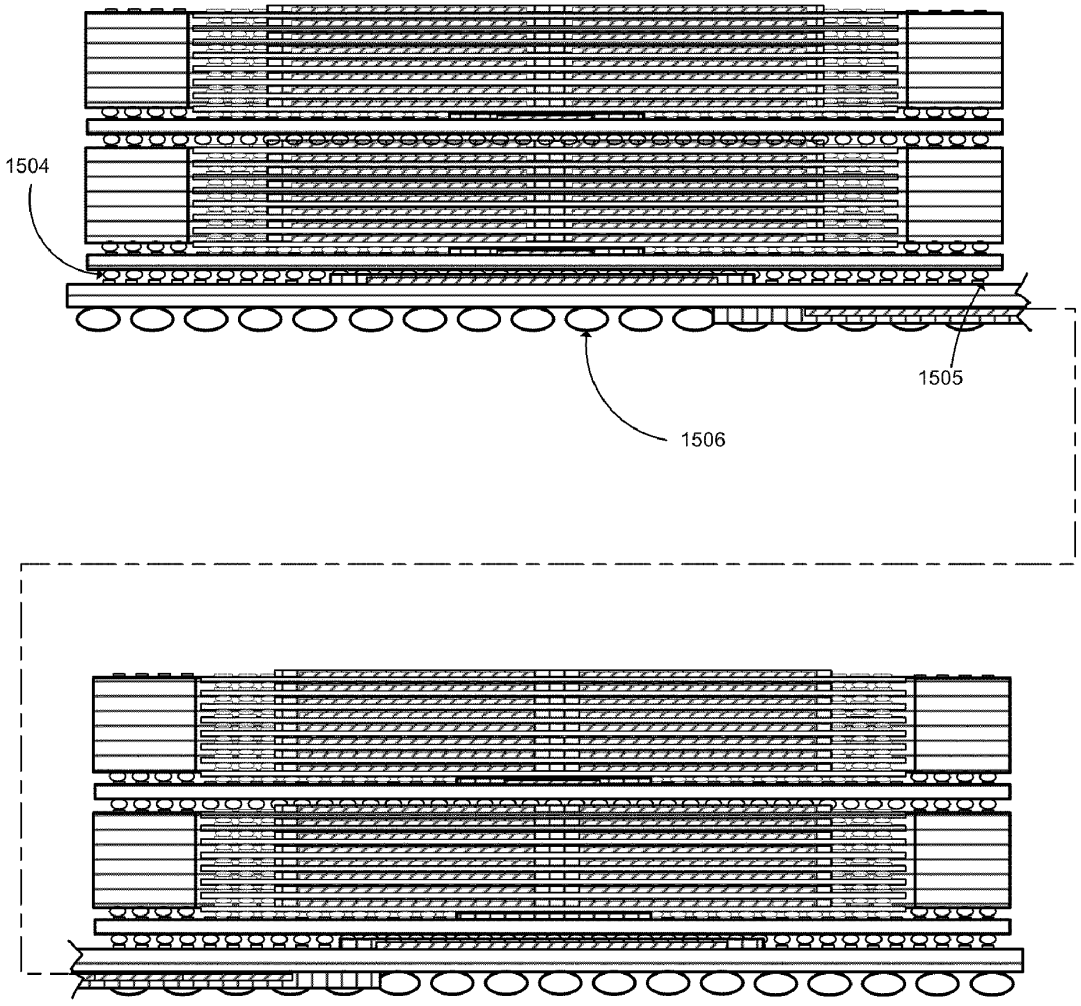


Figure 15b

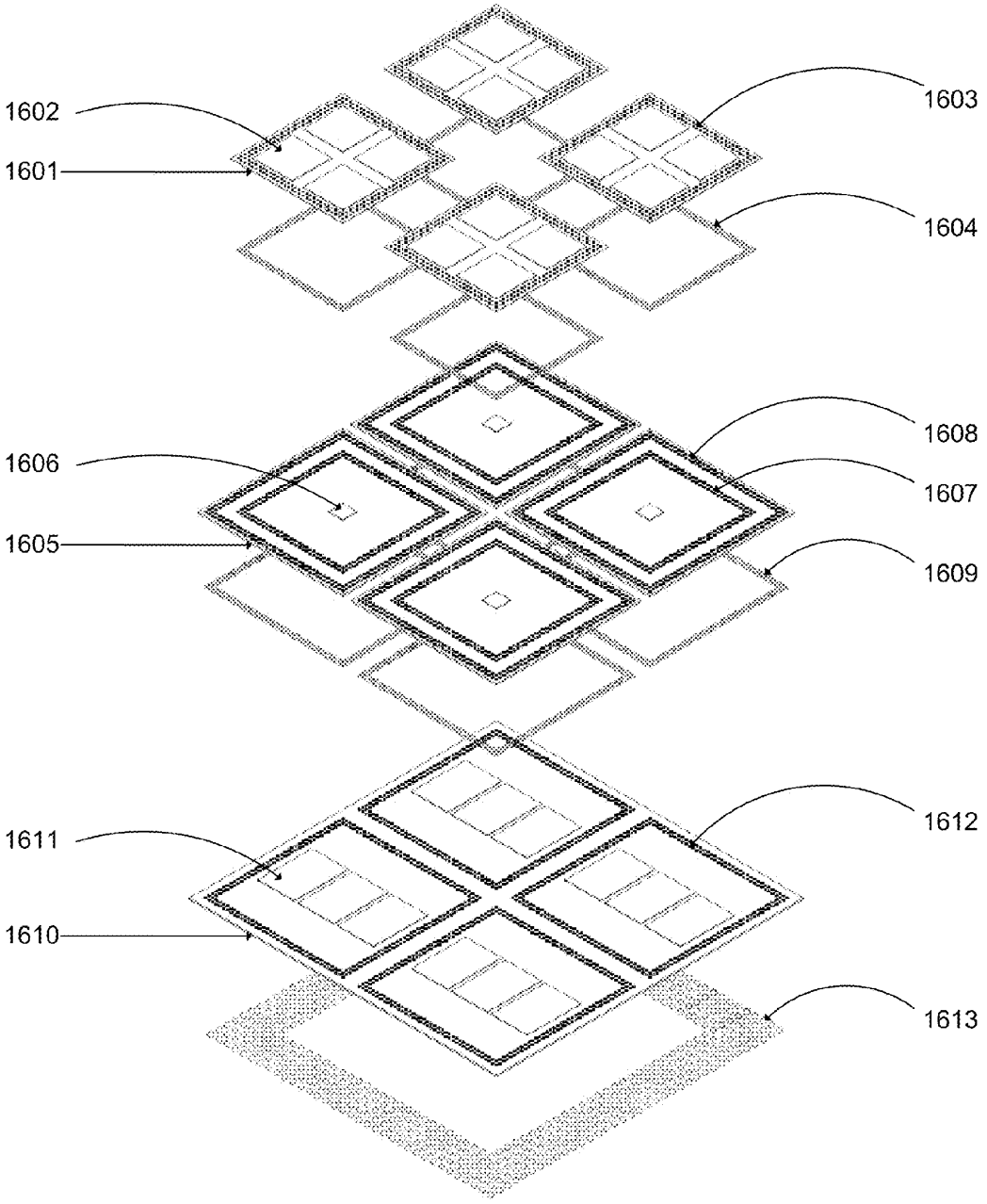

1602
1601
1603
1604
1606
1605
1608
1607
1609
1611
1610
1612
1613

Figure 16

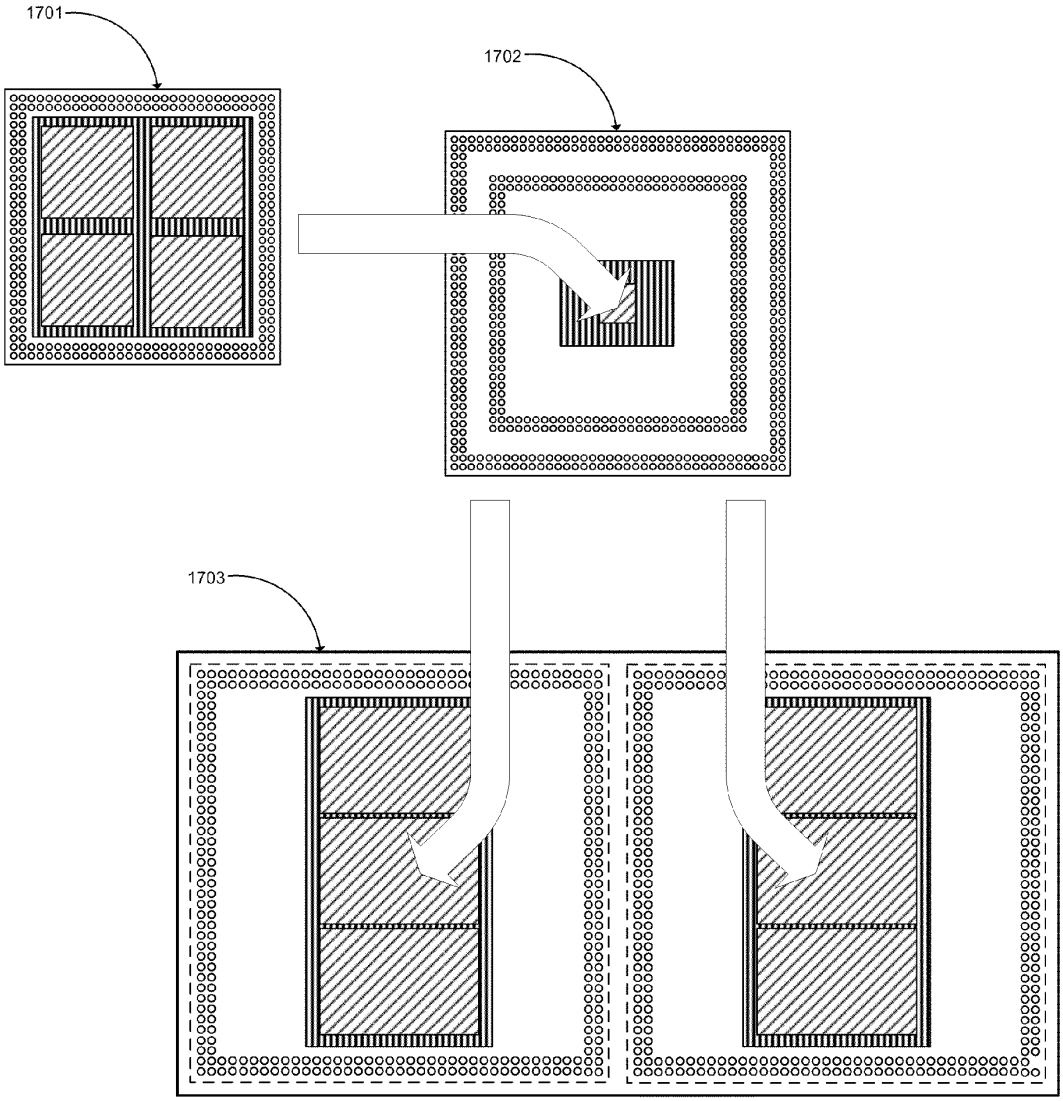


Figure 17a

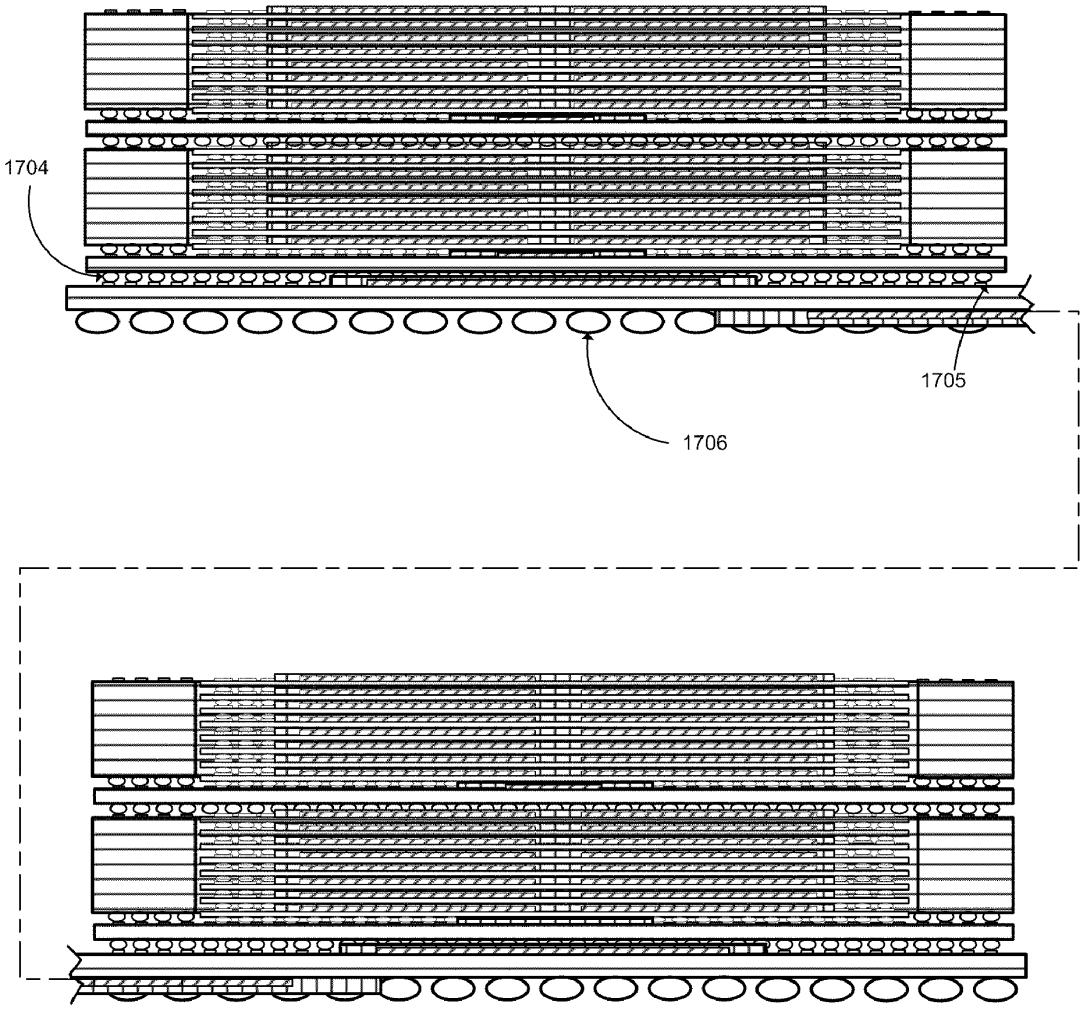


Figure 17b

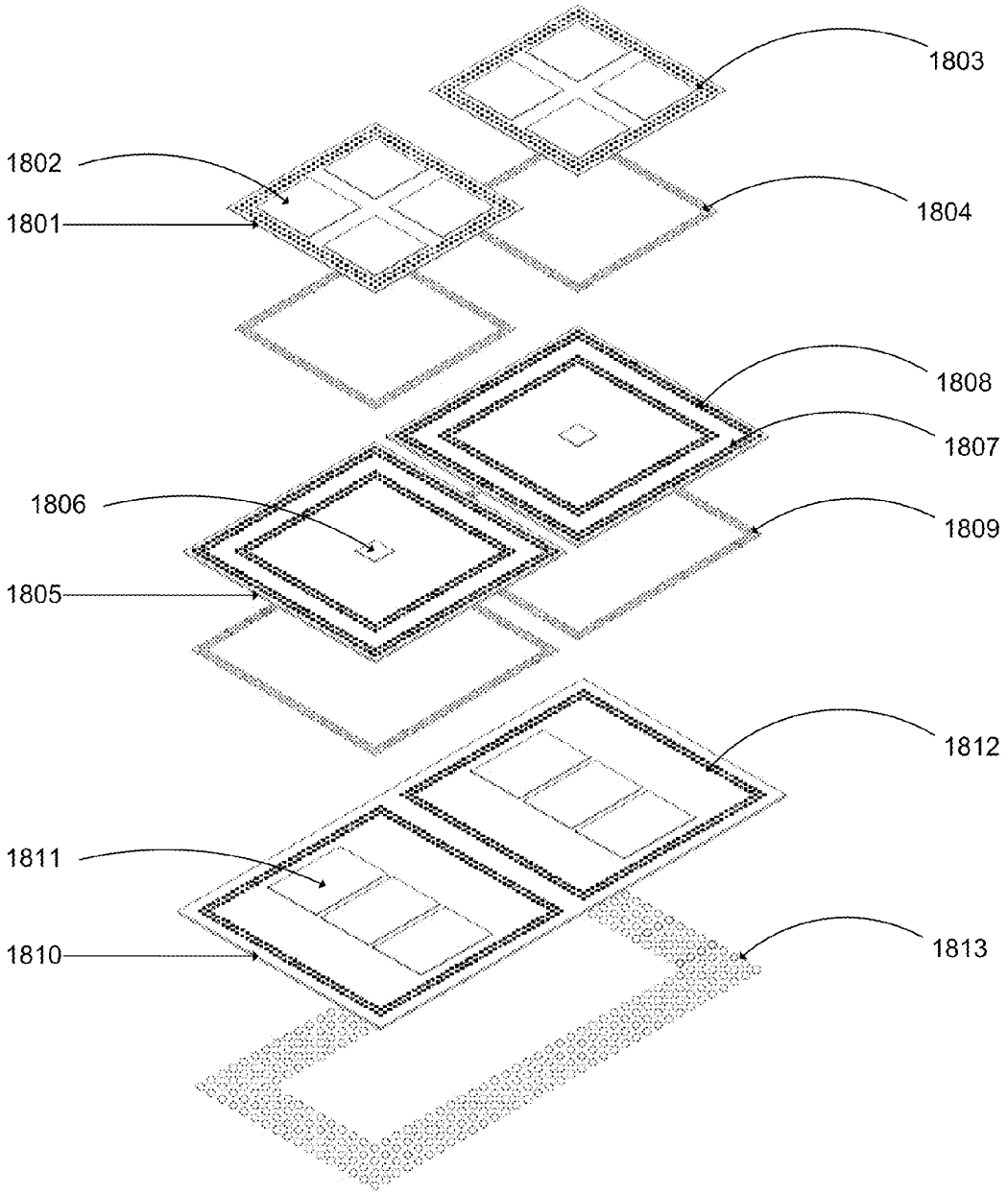

1803
1802
1801
1804
1808
1807
1806
1809
1805
1812
1811
1810
1813

Figure 18

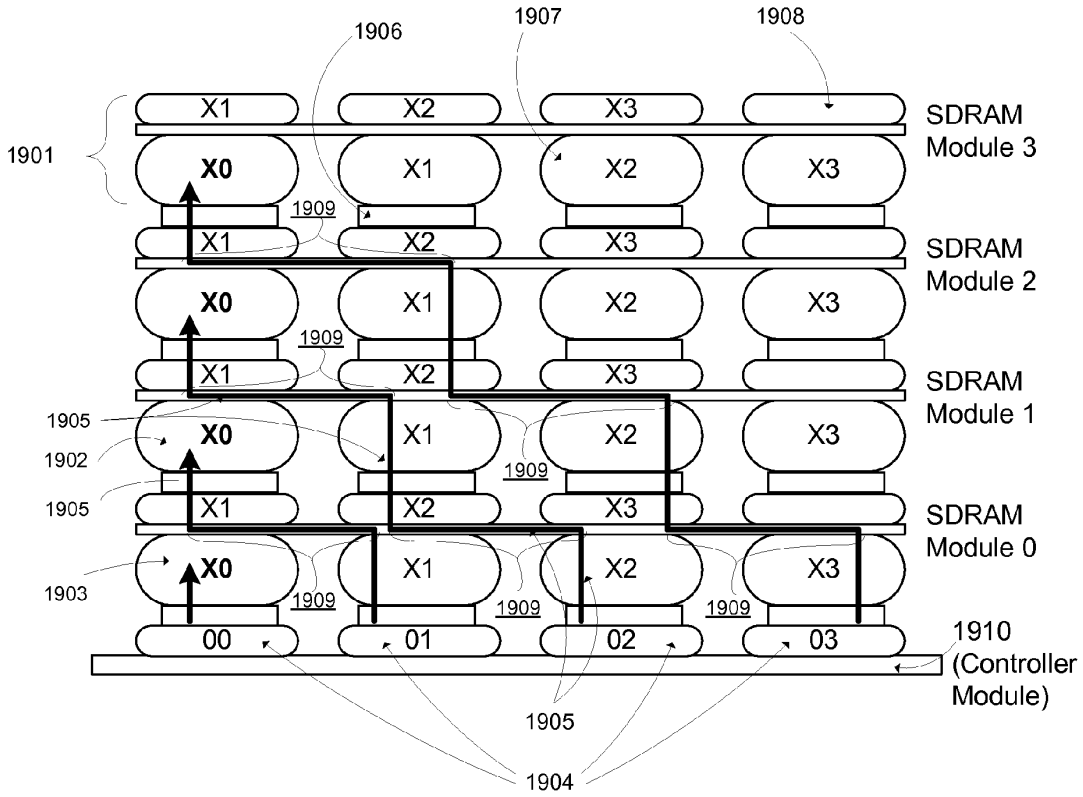

1906
1907
1908
1901
X1
X2
X3
X0
SDRAM Module 3
SDRAM Module 2
SDRAM Module 1
SDRAM Module 0
1909
1905
1902
1903
00
01
02
03
1910 (Controller Module)
1904

Figure 19

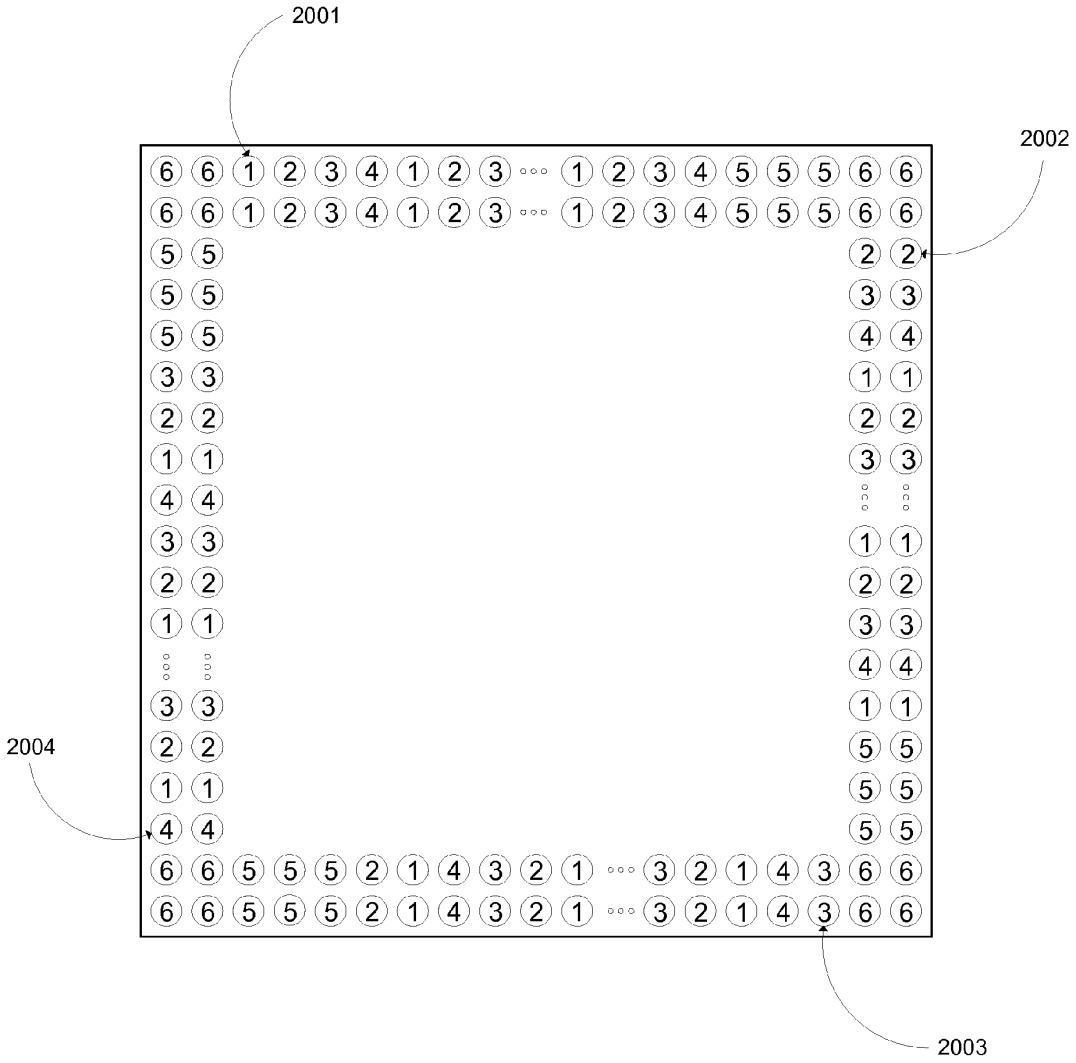


Figure 20a

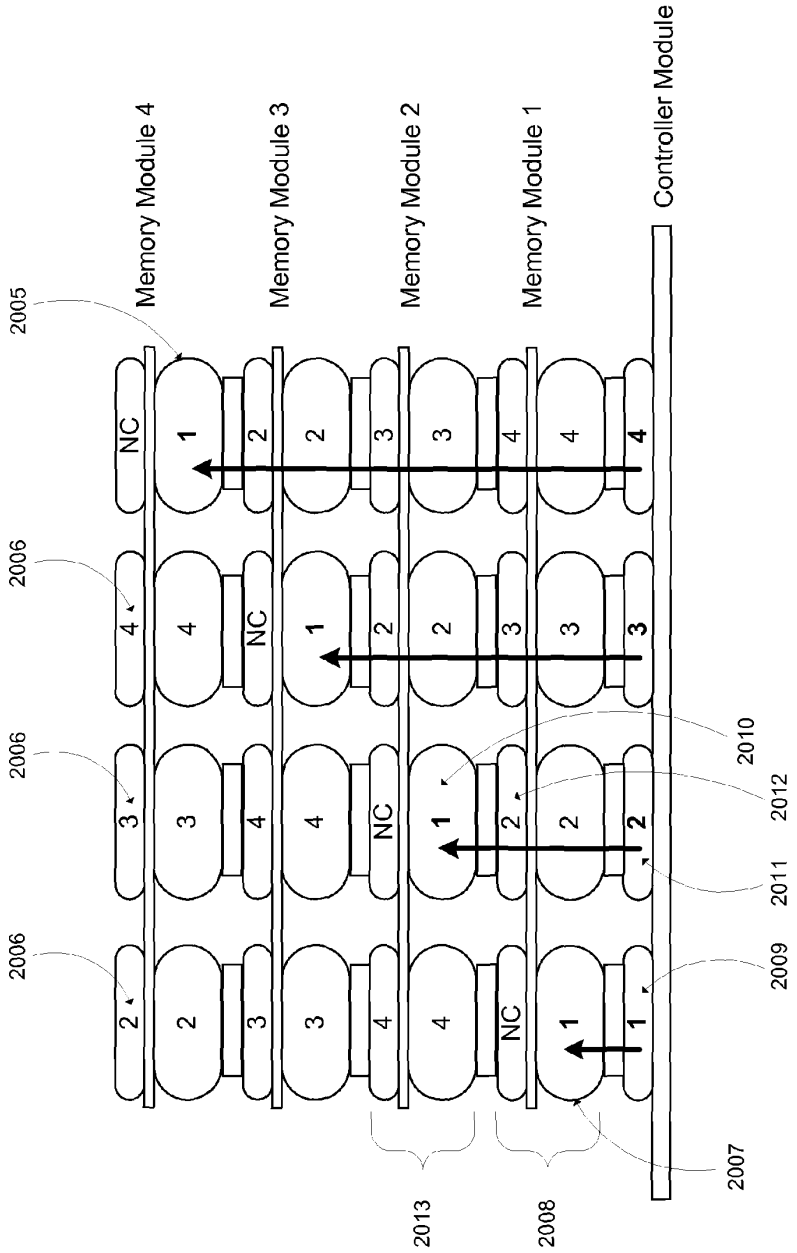

Memory Module 4
Memory Module 3
Memory Module 2
Memory Module 1
Controller Module
2005
2006
2006
2006
2010
2012
2011
2009
2007
2013
2008
NC

Figure 20b

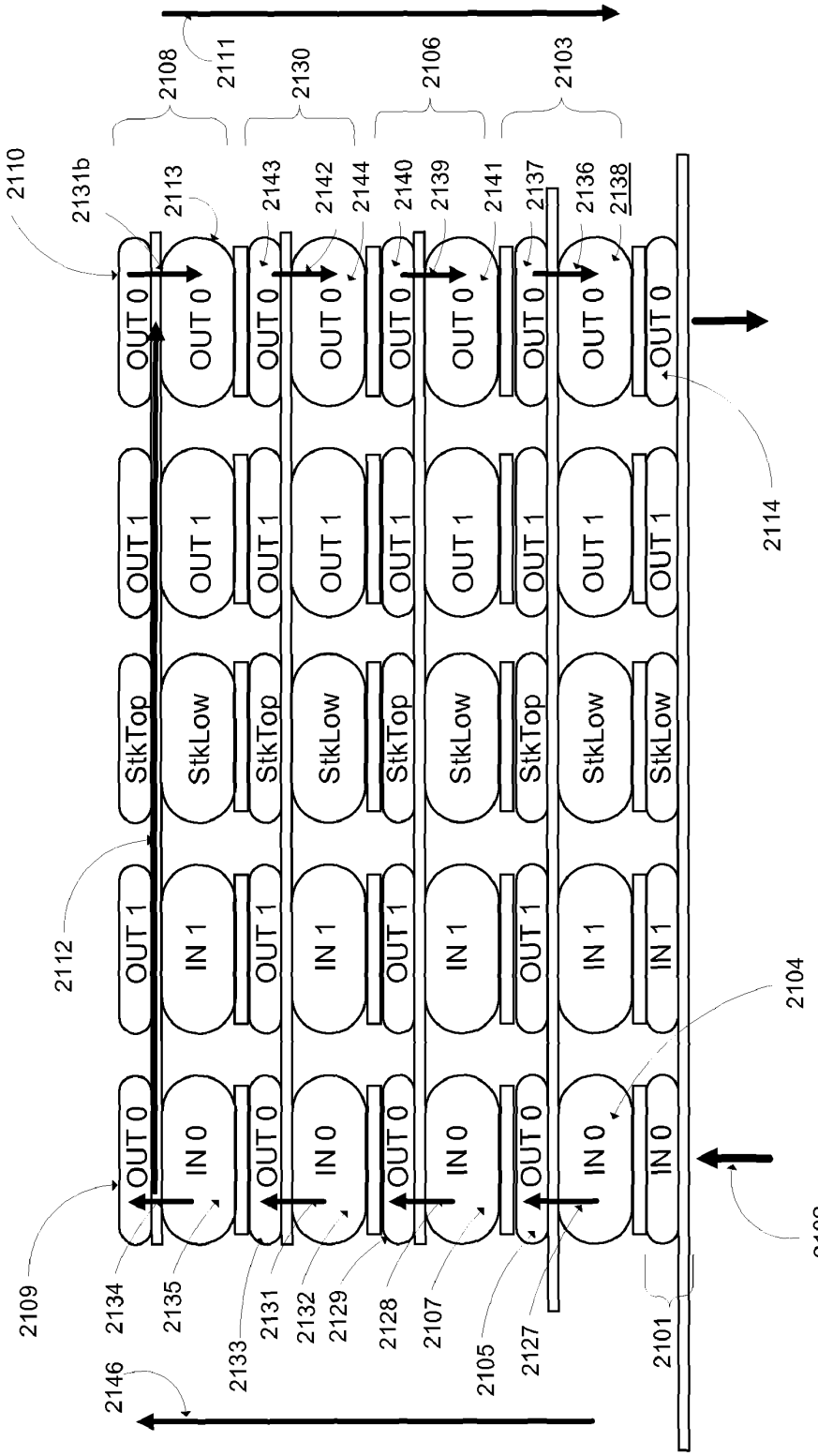

2108
2111
2130
2106
2103
2110
2131b
2113
2143
2142
2144
2140
2139
2141
2137
2136
2138
OUT 0
OUT 1
StkTop
StkLow
IN 1
IN 0
2114
2112
2104
2102
2109
2134
2135
2133
2131
2132
2129
2128
2107
2105
2127
2101
2146

Figure 21a

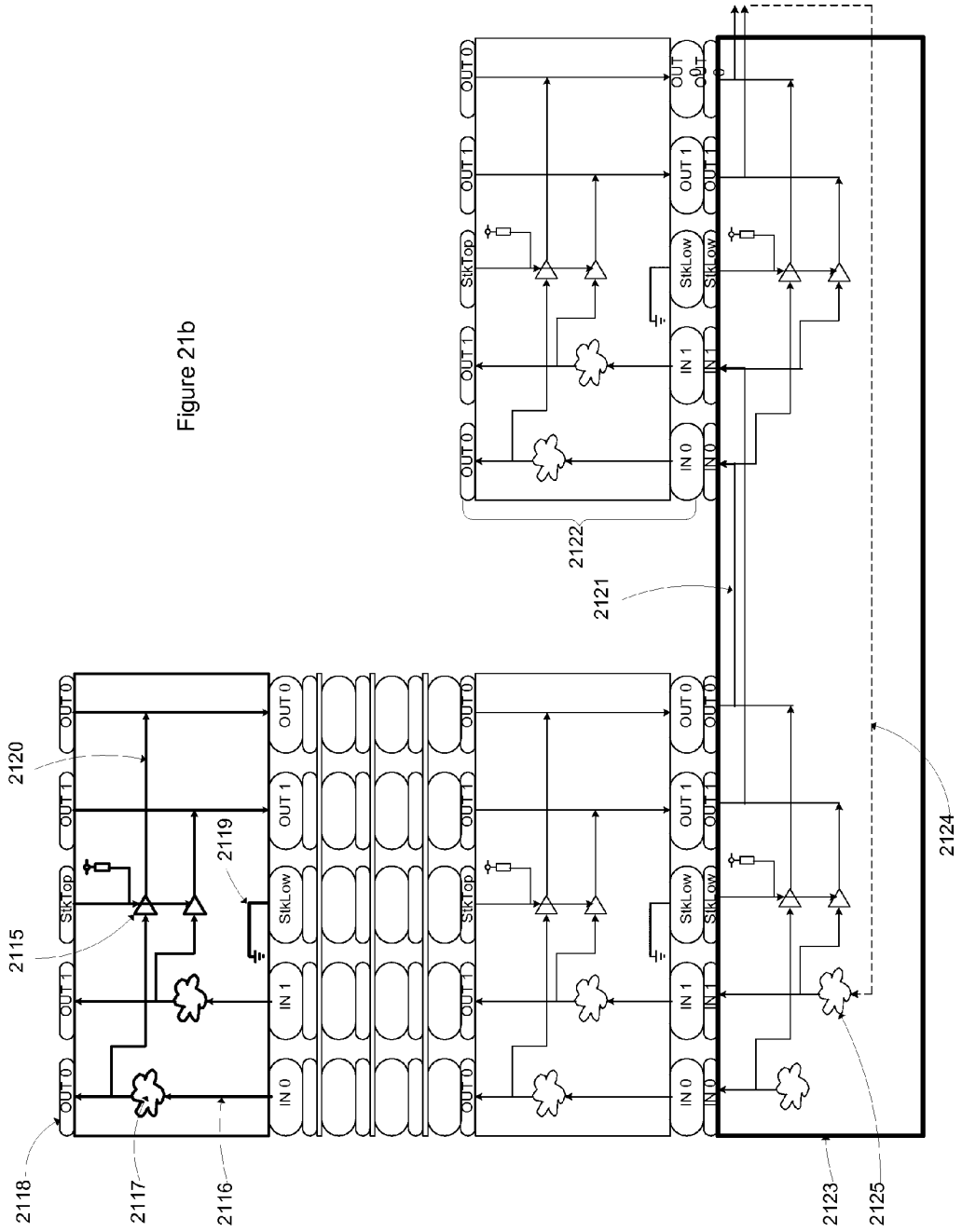

OUT 0
OUT 1
StkTop
StkLow
IN 1
IN 0
2118
2117
2116
2115
2120
2119
2121
2122
2123
2124
2125

Figure 21b

MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES

BACKGROUND

1. Field

The present invention relates to computer systems. More particularly, the present invention relates to flash memory based semiconductor disk drives and a method of using multiple chip module (MCM) and Package Stacking technique to support miniaturization and memory scalability.

2. Description of Related Art

A flash memory based semiconductor disk drive typically use separate packages for the interface controller, the DMA controller, the processor and separate packages for the Flash devices, the FPROMs and the RAMs. This current method limits the miniaturization of the entire storage device. In order to achieve the move to miniaturization, chip modules and packages need to be stacked. Stacking both on chip module and package level maximizes the capacity in a limited area thus realizing the move to miniaturize the entire storage device. A technique in stacking chip modules and packages strategically to support miniaturization and memory scalability in both vertical and horizontal orientation is therefore proposed.

SUMMARY OF THE INVENTION

In the stacking technique illustrated in example embodiments of the present invention, semiconductor dies are mounted in a module to become a MCM which serves as the basic building block. Combination of these modules and dies in a substrate creates a package with specific function or a range of memory capacity. These packages are stacked to increase capacity or add functions. A combination of different existing technology such as flip chip, wire bond, MCM, module stacking, advance packaging, etc. are used to accomplish highly reliable module to module and package to package interconnection and scalability. A single package can have a wide range of capacity depending on the memory capacity of the die used and the number of modules stacked within the package. In the proposed package stacking technique, the stacked modules in a package serve as the building blocks for the package level stacking. Multiple packages are stacked to create the desired memory capacity and different packages are stacked to create desired function. Expansion can be done both on the vertical and horizontal orientations. The technique is in the assignment of pins. Small capacity miniature storage devices can use the vertical expansion, while high capacity devices with larger form factors can use both vertical and horizontal expansion to maximize capacity. By using this technique, large capacity storage devices are implemented in a small package device, and larger form factors achieve bigger memory capacities.

The present invention takes advantage of the existing stacking technology both on the module and package level. This maximizes the capacity in a small area, realizing the miniaturization transition. Modular approach is used in creating basic building blocks which can be tested individually and replaced easily prior to final packaging, making the technique reliable, and cost effective. A wide range of capacity can be configured through variation of die capacities and stacking modules and/or packages. Expanding capacity may be implemented vertically, horizontally or both, depending on board area and desired capacity.

BRIEF DESCRIPTION OF DRAWINGS

So that the manner in which the above recited features, advantages and objects of the present invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the present invention may admit to other equally effective embodiments.

FIG. **1***a* shows the block diagram of the stackable system for high performance, high capacity devices according to an example embodiment of the present invention.

FIG. **1***b* shows the block diagram of the stackable system for lower performance, lower capacity devices according to an example embodiment of the present invention.

FIG. **2***a*, **2***b*, **2***c* depict the SDRAM module's top and bottom drawings and a cross sectional representation of stacked multiple SDRAM modules according to an example embodiment of the present invention.

FIG. **3***a*, **3***b*, **3***c* depict the flash module's top and bottom drawings and a cross sectional representation of stacked multiple flash modules according to an example embodiment of the present invention.

FIG. **4***a*, **4***b* depict the first high-end controller module's top and bottom drawings according to an example embodiment of the present invention.

FIG. **5***a*, **5***b* depict the memory module's top and bottom drawings according to an example embodiment of the present invention.

FIG. **6***a*, **6***b* depict the first low-end controller module's top and bottom drawings according to an example embodiment of the present invention.

FIG. **7***a*, **7***b* depict the second high-end controller module's top and bottom drawings according to an example embodiment of the present invention.

FIG. **8***a*, **8***b* depict the second low-end controller module's top and bottom drawings according to an example embodiment of the present invention.

FIG. **9** depicts the stacked SDRAM modules further stacked on the controller module according to an example embodiment of the present invention. This configuration is used for high end applications. The figure also shows how the balls have corresponding pads for inter-module connection.

FIG. **10** depicts stacked flash modules further stacked on the memory module according to an example embodiment of the present invention. The figure also shows how the balls have corresponding pads for inter-module connection.

FIG. **11** depicts the possible stacking options for the first high-end controller module and the memory modules according to an example embodiment of the present invention. A substrate interface is used to attach one group of stacked modules to another.

FIG. **12***a* is an isometric exploded drawing of the stacking technique presented in FIG. **11** according to an example embodiment of the present invention. Multiple identical stacking is not included in this drawing.

FIG. **12***b* is another package stacking technique using Pin Grid Array (PGA) rather than Ball Grid Array (BGA) according to an example embodiment of the present invention. This is used for easy replacement and expansion.

FIG. **13** depicts the low-end controller module configuration with stacked flash module according to an example embodiment of the present invention. The figure also shows how the balls have corresponding pads for inter-module connection.

FIG. **14** is an isometric exploded version of the stacking technique presented in FIG. **11** according to an example embodiment of the present invention.

FIG. **15***a*, **15***b* depict the second high-end controller module configuration with stacked memory modules according to an example embodiment of the present invention. The figures also show how the balls have corresponding pads for inter-module connection.

FIG. **16** is an isometric exploded version of the stacking technique presented in FIG. **14** according to an example embodiment of the present invention.

FIG. **17***a*, **17***b* depict the second low-end controller module configuration with stacked memory modules according to an example embodiment of the present invention. The figures also show how the balls have corresponding pads for inter-module connection.

FIG. **18** is an isometric exploded version of the stacking technique presented in FIG. **17** according to an example embodiment of the present invention.

FIG. **19** shows a pin assignment and connection technique to be able to select specific layer in a multi-stacked module according to an example embodiment of the present invention.

FIG. **20***a* shows another pin assignment technique which uses a rotational stacking orientation to allow stacking of four identical modules representing different bus interfaces according to an example embodiment of the present invention.

FIG. **20***b* shows a cross-section representation of the four stacked modules on a rotational stacking technique and how their pins mates according to an example embodiment of the present invention.

FIG. **21***a* shows another pin assignment and connection technique to be able to connect a serial chain route from multiple modules in a stack according to an example embodiment of the present invention.

FIG. **21***b* shows the routing of a serial chain connection from one stack location to another allowing application of both vertical and horizontal expansion independently or simultaneously according to an example embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. **1***a* is a block diagram of a flash storage system according to a first example embodiment of the present invention. The block diagram shows the entire high-end system that is modularized, stacked, and packaged to achieve the desired features of the technique. The heart of the system is the main controller-processor **101** which interfaces with the flash memory, the flash PROM and the SDRAM memory blocks. The SDRAM is configured from a single bank **102** to a maximum of four banks depending on the desired capacity. Each bank such as **102** includes 3 SDRAMs. The flash devices such as **107** are controlled by the Flash Interface Controller such as **105**. Each controller supports four flash buses such as flash bus A11 **106**, and each flash bus supports a maximum of 8 flash devices. The main controller-processor supports four flash interface controllers through 4 different busses such as B bus **104**. The four flash interface controllers with their corresponding flash devices comprise the memory set **108**. The main controller-processor can support from one memory set to a maximum of 15 memory sets. This is a maximum support of 1,920 flash devices.

FIG. **1***b* is a block diagram of a flash storage system according to a second example embodiment of the present invention. The block diagram shows the entire low-end system that is modularized, stacked, and packaged to achieve the desired features of the technique. Since a low-end system may not require a large amount of memory capacity, SDRAM may be limited to one bank **109**, or none at all, and the supported flash devices may also be limited to only two sets of flash buses. One set of flash buses **110** consists of four flash bus with 8 flash devices supported per flash bus, which results in a maximum supported number of 64 flash devices.

From the basic dies; SDRAM, FPROM, flash memory, flash interface controller, and the main controller-processor, single and multiple chip modules are created to become the basic building blocks for the stacking technique presented in the present invention. Referring to FIG. **2***a* which is a top view of an SDRAM module, three SDRAM dies **201** are placed in a single substrate **203** to become the SDRAM module which is one of the basic building blocks. The SDRAM module is represented in FIG. **1** as a single bank **102** composed of SDRAM 00, SDRAM 01, and SDRAM 02 connected to the SDRAM interface **103**. All signals needed to interface to the controller module and other SDRAM modules are assigned in both the bottom balls **204** and top pads **202** respectively. Bottom balls **204** are shown in FIG. **2***b* which is a bottom view of the SDRAM module, three slots **205** are created under the SDRAM die's pad attach area to accommodate bottom wire bonding. FIG. **2***c* is the stacked module cross sectional representation. Top pads **202** and bottom balls **204** act as the vertical interconnects between all SDRAM modules and to the controller module. Varying the SDRAM die capacity and the stack quantity, results in wide range of total SDRAM capacity depending on the product application. The SDRAM device organization, capacity and bank limitations are defined by the main controller-processor's SDRAM interface specifications. The main controller-processor intended to be used for this example embodiment of the present invention supports a 32-bit wide 4 banks maximum SDRAM configuration.

FIG. **3***a* is a top view that shows four flash dies **301** in a single substrate **303** that collectively form part of a flash module, which can also function as a basic building block. All signals needed to interface with the memory module and other flash modules are assigned in both the bottom balls **304** and the top pads **302**, respectively, as shown in FIGS. **3***a*, **3***b* and **3***c*. In FIG. **3***c*, the flash modules are stacked. Maximum stack quantity depends on the flash interface controller specifications. Top pads **302** and bottom balls **304** acts as the vertical interconnects between stacked flash modules and to the memory module. Varying the flash die capacity and the stacking quantity, results in a wide range of total flash capacity depending on the product application and capacity requirements. The flash device organization and capacity limitations are defined by the flash interface controller's specifications. The flash interface controller intended to be used for this used for this example embodiment of the present invention supports 8 flash devices per flash bus, thus allowing a maximum stacking of 8 flash modules.

FIG. **4***a* shows the top view of the first example embodiment of the present invention illustrated in a first high-end controller module configuration. A single FPROM die **401** is placed at the center of the substrate **404**. Pads are composed of two sections, one for the SDRAM module interface shown as **402** and another for the memory module interface shown as

403. This technique enables multiple stacking of both SDRAM modules and memory modules in a single package. FIG. 4*b* shows the bottom view of the controller module. A single main controller-processor die **406** is placed at the center of the substrate. The controller module becomes a base module for the package. The balls **405** are used to connect to the main substrate which is typically a printed circuit board (PCB).

FIG. 5*a* shows the top view of the memory module which is also a basic building block. A single flash interface controller die **501** is placed on the center of the substrate **504**. Pads are composed of two sections, one for the flash module interface shown as **502** and another for the other memory module interface shown as **503**. This technique enables multiple stacking of flash modules and memory modules in a single package. The memory module becomes a base module for the package. FIG. 5*b* shows the bottom view of the memory module. The memory module balls **505** are used to connect to the main substrate PCB, to the controller modules or to the other memory modules depending on the type of configuration desired.

FIG. 6*a* shows the top view of the second example embodiment of the present invention illustrated in a first low-end controller module configuration. Two SDRAMs **601** and a single FPROM **602** are placed on top of the module. This configuration is flexible. The SDRAMs can be unpopulated in a low performance application. Internal SRAMs in the main controller-processor will take over the SDRAM functions. The main controller-processor **605** is placed at the bottom of the module. This configuration does not allow stacking of the SDRAM which is not necessary for low capacity applications. Flash modules are stacked on top, interfacing to the pads **603**. The substrate **604** is the same size as the flash module making its final package smaller. The bottom balls **606** are used to interface with the main PCB.

FIG. 7*a* shows the top view of the first example embodiment of the present invention illustrated in a second high-end controller module configuration, where four memory modules **701** can be mounted on separate locations adjacent to each other. Memory module interface pads **704** are allocated for multiple stack configurations. In the middle of the memory module interface pads, 3 SDRAM dies **702** are mounted. Each area corresponds to one SDRAM bank **703**, totaling to a maximum of 4 SDRAM banks in the package. The bottom view is presented in FIG. 7*b*, where the main controller-processor die **705** and the FPROM die **706** are mounted adjacent to each other. The module's balls **707** are used for external interface to the main PCB.

FIG. 8*a* shows the top view of the second example embodiment of the present invention illustrated in a second low-end controller module configuration, where only two memory modules **801** can be mounted side-by-side. Memory module interface pads **802** are allocated for multiple stacking configurations. In the middle of the memory module interface pads, 3 SDRAM dies **803** are mounted. Each area corresponds to one SDRAM bank **804**, totaling to only a maximum of 2 SDRAM banks in a package. The SDRAM can either be mounted or not depending on the application. Internal SRAMs can also be used instead of the SDRAMs. The stacked memory modules can also be configured to support both internal and external flash interface controller applications. The bottom view is presented in FIG. 8*b*, where the main controller-processor die **805** and the FPROM die **806** are mounted adjacent to each other. The module balls **807** are used for external interface to the main PCB.

FIG. **9** shows the stacking of SDRAM module **901** and controller module **902**. A single or stacked SDRAM module can be placed on top of a controller module. The pads for the SDRAM module interface **903** must align with the SDRAM module balls **904**. The bottom-most SDRAM module **905** serves as bank 0, and the top-most module **906** serves as bank 3. For low capacity SDRAM requirements, only a single or dual bank is enough. High capacity devices needs to have a maximum SDRAM capacity, thus stacking the maximum of 4 modules. The outer pads **907** are for the memory module interface.

FIG. **10** shows the stacking of flash modules **1001** and memory module **1002**. A four-stack or eight-stack flash module is placed on top of a memory module. The pads for the flash module interface **1003** must align with the flash module balls **1004**. The outer pads **1005** are for other memory module interface. The flash interface controller intended to be used for this example embodiment of the present invention supports a maximum of 4 flash buses and each flash bus supports a maximum of 8 flash devices. The bottom-most flash module **1006** contains the 4 flash buses' Flash 00 devices and the top-most module **1007** contains the 4 flash buses' Flash 07 devices.

FIG. **11** shows a sample of a maximized stacking technique that can be configured through vertical, horizontal or combined expansion. Multiple staking will increase the overall height of the module, thus requiring a filler **1101** to physically interconnect two stacked modules. A thinner filler **1102** may be used depending on the height differential between the modules which is dependent to the number of stacks applied. A controller module with the stacked SDRAM modules act as the controller package **1103**. A memory module with stacked flash modules acts as the memory package **1104**. Four memory packages stacked together form the memory set **1105**. Vertical expansion happens when the controller package is stacked with a single or multiple memory sets. The figure shows a single memory set to be stacked to the controller package. Horizontal expansion happens when the controller package is located on a different site on the PCB relative to the memory sets. Also multiple memory sets can be located on different sites on a PCB. Combo expansion happens when both vertical and horizontal expansion technique is implemented simultaneously. The expansion technique is very flexible depending on the desired memory capacity, main PCB size limitations and also height limitations.

FIG. **12***a* shows the isometric and exploded drawing of the stacking technique for the first high-end controller configuration. Pins are assigned strategically and modules are stacked to make possible the miniaturization of the entire system in a package.

1201—The Flash Module
1202—The Flash Die
1203—The Flash Module Pad Interface to other Flash Modules
1204—The Flash Module Solder Balls
1205—The Memory Module
1206—The Flash Interface Controller Die
1207—The Memory Module Pad Interface for the Flash Module
1208—The Memory Module Pad Interface for the other Memory Modules
1209—The Memory Module Solder Balls
1210—The SDRAM Module
1211—The SDRAM Die
1212—The SDRAM Module Pad Interface to other SDRAM Modules
1213—The SDRAM Module Solder Balls
1214—The Controller Module

1215—The FPROM Die on top side and the Main Controller-Processor Die at the bottom side.

1216—The Controller Module Pad Interface to the SDRAM Modules

1217—The Controller Module Pad Interface to the Memory Modules

1218—The Controller Module Solder Balls

FIG. **12***b* is another technique used in this invention to ease replacement and facilitate expansion. Instead of using Ball Grid Array (BGA), Pin Grid Array (PGA) **1219** is used. This method makes it more flexible due to the technology's inherent feature where replacement is done swiftly without any assembly process involved. Horizontal expansion is also benefited in this technology. The figure shows the stacked memory module as an example. The memory module is packaged using the PGA technology, where the top portion of the package becomes the socket **1220** and the bottom portion the pin arrays **1219**. The filler **1221** becomes the package's top socket and is interfaced into the base module **1222** through the BGA **1223**. The base module uses PGA to interface to the bottom package or to the main board **1224**. Filler **1225** is also mounted into the main board to interface the stacked memory modules.

FIG. **13** shows the stacking of the flash module **1301** and the first low-end type of controller module **1302**. A single or stacked flash module can be placed on top of the controller module. The pads for the flash module interface **1303** must align with the flash module balls **1304**. This configuration is for low capacity low performance applications. The number of flash modules to be stacked depends on the desired capacity and is limited to the supported feature of the main controller-processor. The main controller-processor's flash interface can support a maximum of 8 buses and a maximum of 8 flash devices per bus.

FIG. **14** shows the isometric and exploded drawing of the stacking technique for the first low-end controller configuration. Pins are assigned strategically and modules are stacked to make possible the miniaturization of the entire system in a package.

1401—The Flash Module

1402—The Flash Die

1403—The Flash Module Pad Interface to other Flash Modules

1404—The Flash Module Solder Balls

1405—The Controller Module

1406—The FPROM Die and the Main Controller-Processor Die at the bottom

1407—The SDRAM Die

1408—The Controller Module Pad Interface to the Flash Modules

1409—The Controller Module Solder Balls

FIG. **15***a* shows the stacking technique for the second high-end controller configuration. The stacked flash modules **1501** are further stacked on top of the memory modules **1502** which are then mounted on the controller module **1503** on four different locations. Four memory modules can be mounted on four different locations on the controller module creating a memory set. Stacking more memory sets increases the total capacity. The cross-sectional representation of the said stacking technique is shown in FIG. **15***b*. The memory module balls **1504** must align to the pad interface **1505** on the controller module. As previously discussed in FIG. **11**, fillers are used to physically connect two successively stacked modules. The controller balls **1506** will become the external interface to the main board. The final package is 4× bigger than the first high end option.

FIG. **16** shows the isometric and exploded drawing of the stacking technique discussed in FIG. **15**. Pins are assigned strategically and modules stacked to make possible the maximum stacking and interconnection between modules. As previously discussed in FIG. **11**, fillers are used to physically connect two stacked successively stacked modules.

1601—The Flash Module

1602—The Flash Dies

1603—The Flash Module Pads Interface to other Flash Modules

1604—The Flash Module Solder Balls

1605—The Memory Module

1606—The Flash Interface Controller Dies

1607—The Memory Module Pad Interface to Flash Modules

1608—The Memory Module Pad Interface to other Memory Modules

1609—The Memory Module Solder Balls

1610—The Controller Module

1611—The SDRAM Dies on top side and the FPROM and Main Controller-Processor at the bottom side

1612—The Controller Module Pads Interface to the Memory Modules

1613—The Controller Module Solder Balls

FIG. **17***a* shows the stacking technique for the second low-end configuration. The stacked flash modules **1701** are further stacked on top of the memory modules **1702** which are then mounted on the controller module **1703** on two different locations. This technique can use both internal and external flash interface controller configurations, making this technique flexible. The cross-sectional view is shown in FIG. **17***b*. The memory module balls **1704** must align to the pad interface **1705** on the controller module. The controller balls **1706** will become the external interface to the main board. The final package is twice the size of the first high end option.

FIG. **18** shows the isometric and exploded drawing of the stacking technique discussed in FIG. **17**. Pins are assigned strategically and modules stacked to make possible the maximum stacking and interconnection between modules. As previously discussed in FIG. **11**, fillers are used to physically connect two stacked successively stacked modules.

1801—The Flash Module

1802—The Flash Dies

1803—The Flash Module Pads Interface to other Flash Modules

1804—The Flash Module Solder Balls

1805—The Memory Module

1806—The Flash Interface Controller Dies

1807—The Memory Module Pad Interface to Flash Modules

1808—The Memory Module Pad Interface to other Memory Modules

1809—The Memory Module Solder Balls

1810—The Controller Module

1811—The SDRAM Dies on top side and the FPROM and Main Controller-Processor at the bottom side

1812—The Controller Module Pads Interface to the Memory Modules

1813—The Controller Module Solder Balls

A more detailed technique on how the pins are assigned and how modules are placed with different orientation in the stack is discussed in the following paragraphs.

FIG. **19** shows a first pin assignment and connection technique that enables a selection of specific module in a multiple module stack. The figure illustrates the controller and SDRAM modules as an example. The SDRAM module balls, such as **1907**, are represented by big oblong shapes, and the pads such as **1908** are represented by smaller oblong shapes. A pad to ball connection is represented by a rectangle, such as

1906. The controller module has four active pads such as 1904, one each for the four SDRAM modules such as 1901. The controller module's active pad 00 1904 is connected to SDRAM module 0's X0 ball 1903, pad 01 to SDRAM module 1's X0 ball 1902, and so on. The X0 balls are the active balls for the SDRAM modules. All SDRAM modules are identical which include the connections as follows: X1 ball is connected to X1 pad, X2 ball to X2 pad, and so on. The technique involves using a ladder-like routing path, such as 1905 on the stacked modules. This technique enables the controller module's active pad to be routed to the desired specific module in the stack. The example embodiment illustrated in FIG. 19 comprises a repeating pattern for the balls and pads. Passive balls are connected within each module to passive pads with an offset distance equaling one periodic distance of the repeating pattern. The importance is the approach using repeating pattern and offsetting of the passive ball to passive pad within each module, other offset distances can be used also in other embodiment of the present invention, e.g. using an offset of two or any multiple of the periodic distance of the repeating pattern. The example embodiment does not limit the scope of the present invention.

Another pin assignment, connection, and stacking combo method introduced in this invention is the rotational stacking technique. FIG. 20*a* shows the pad interconnects for a certain base module and strategic numbering is assigned. Pads labeled with numbers 1 to 4 represent the four different groups of signals. Pads labeled with the number 5 are used for the vertical stacking IOs (more details are illustrated in FIG. 21*a*). Pads labeled with the number 6 are reserved for power and ground which are common to all modules in the stack. Since the stacked modules are identical, we can use rotational stacking to connect one module to one group of signals and the following rotated stacked module connects to another group of signals, and so on. This way ensures four identical modules to be stacked and connected to four different groups of signals from the base module which is typically a controller. Pad 1 2001, upon the substrate being rotated 90 degrees clockwise, occupies pad 2 2002 location relative to an unrotated substrate such as the base substrate which is typically a controller. In a similar manner pad 1 2001 can be located at pad 3 2003 location, then pad 4 2004 location upon the substrate being rotated 180 and 270 degrees clockwise respectively.

FIG. 20*b* shows a cross-sectional view of four such modules stacked over the base module. Memory and Controller modules are used as example. Pin 1s such as 2005 on the stacked modules are the only active signal pins for the module. The rest (numbered 2 to 4) 2006 are directly connected to the balls underneath them but have no other connections. This way connection is continued from bottom to top. The active pin 2007 of the first module 2008 is aligned to pin 1 pad 2009 on the base module, and the second module's active pin 2010 is aligned on pin 2 2011 of the base module with second module being rotated 90 degrees clockwise. Since pin 2 2012 on the first module is directly connected to the ball underneath, this allows the pin 1 on the second module 2013 to be connected to pin 2 2011 of the base module. Rotating the next stacked module 90 degrees more, will align it's active pin to the base module pin 3 and so on until the forth rotation.

The last connection technique is used for serial routing of all modules in the stack and allowing them to be externally accessible for horizontal expansion on a PCB, such as a main board. FIG. 21*a* shows how this technique is implemented in the stacking method. The main board 2101 contains the input signals 2102 which will then be connected to IN ball 2104 of the base module 2103. The base module's OUT pad 2105 is connected to IN ball 2107 of the first stack module 2106, and so on. The top module 2108 terminates the signal to the top pad 2109 and routes, with connection 2112, the signal internally to another pad 2110 which is connected directly to the ball 2113 underneath. Since the modules are identical, this routed signal passes through the pads and balls 2111 of the stack until it reaches the OUT pad 2114 of the main board for external access. How the top module terminates the serial chain and branches them out to other pads is shown in FIG. 21*b*. All modules have a selectable buffer 2115 that tri-states the input when pulled low. The signal from the IN balls 2116 enters the internal circuit 2117 and exits the circuit connecting to the OUT pad 2118. The buffer's 2115 control line is weakly pulled up internally. The "StkLow" ball is connected internally to GND 2119, thus pulling down the buffer control line when a module is stacked above it, and it is pulled up when no module is stacked directly above it. When the buffer control line is pulled high, it will let the input signal branch out 2120 to the other pads, thus creating a connection route or trace that loops back to the base module solder balls. When a module is stacked above a module that is disposed with selectable buffer 2115 in the manner shown, the buffer control signal is pulled low, tri-stating the input signal and disallowing the branching effect. This technique allows the signal to be accessible to the external balls of the base module, thus horizontal expansion for a serial signal is achievable. The balls are then routed, with connection 2121, to the other modules 2122 on the other locations. The same technique is used on the main board 2123, when no package is detected on the "StkLow" pad, the buffer allows the input to connect to the designated pads on the other locations. The tri-stated buffer technique is redundant to all locations. An example is the JTAG TDI-TDO signal. The diver circuit 2125 sends out TDI signals to the pads and the closing TDO signal 2124 loops back to the driver circuit.

Combining these stacking, pin assigning and connection techniques allow interconnection between modules with both parallel and series signals to both vertical and horizontal expansion. The technique is very flexible depending on the specific application, capacity, board size and height limit.

We claim:

1. A stacked module comprising a plurality of modules each comprising:

one or more active ports for carrying one or more active signal;

one or more passive ports for passing through the one or more active signals;

a first serial chain route that includes at least one serial chain connection, the serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output; said serial chain input coupled to said serial chain output through said serial chain circuit;

a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module; and

said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module.

2. The stacked module of claim 1 wherein the one or more passive port forms a ladder like routing path, and the passive port connects a passive ball on one surface of a module to a passive pad on another surface of the module.

3. The stacked module of claim 2:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located between a pre-determined distance to each other in a repeating pattern, the pre-determined distance equaling a multiple of a periodic distance of the repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the ladder like routing path; and

wherein at least one of the one or more passive ball and one or more passive pad forms a ladder like routing path.

4. The stacked module of claim **2**, wherein:

the stacked module further includes a first outside surface and a second outside surface, the first and second outside surfaces disposed to face opposite each other; and

at least one of the plurality of modules includes a first module having a first target location terminating between the first and second outside surfaces.

5. The stacked module of claim **4**, wherein the plurality of modules further includes a second module and a third module, the second module including a second module surface that includes the first outside surface and the third module including a third module surface that includes the second outside surface.

6. The stacked module of claim **2**, further including a second ladder like routing path; and wherein:

the plurality of modules includes a first module and a second module, the first and second modules respectively including a first target location and a second target location, the second target location located within the stacked module; and

the ladder like routing path for routing one of the active port to the first target location, and the second ladder like routing path for routing another one of the active port to the second target location.

7. The stacked module of claim **6**, further including a second ladder like routing path; and wherein:

the stacked module includes a first outside surface and a second outside surface, the first and second outside surfaces disposed to face opposite each other;

the ladder like routing path terminates at the first target location; and

the second ladder like routing path terminates at the second target location, the second target terminating within the stacked module and located between the first and second outside surfaces.

8. The stacked module of claim **6**, wherein the second target location is located between the first and second outside surfaces.

9. The stacked module of claim **1** wherein one or more of the plurality of modules is rotated before being stacked and the one or more passive port forms a rotational routing path.

10. The stacked module of claim **9**:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located opposite each other in a repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the rotational routing path; and

wherein at least one of the one or more passive ball and one or more passive pad form a rotational routing path.

11. The stacked module of claim **1** wherein one or more of the plurality of modules includes a main board.

12. The stacked module of claim **11** wherein one or more vertically stacked module is connected to the main board.

13. The stacked module of claim **1**:

wherein each of the plurality of modules comprises a first side and a second side, and the one or more passive ports includes a first passive port connected to a passive ball disposed on the first side and to a passive pad disposed on the second side of a module from the plurality of modules;

wherein the serial chain input includes the passive ball and the serial chain output includes the passive pad

wherein the passive ball and the passive pad are located opposite each other; and

further including a base module having an active port for providing a signal, said signal routed to a same location on the plurality of modules through the first serial chain route.

14. The stacked module of claim **1**:

wherein the routing path includes one or more tri-state driver controlled by the control circuit.

15. The stacked module of claim **14** further including:

a main board coupled to another stacked module having a third serial chain route; and

another control circuit for enabling another routing path that connects the second serial chain route with the third serial chain route.

* * * * *

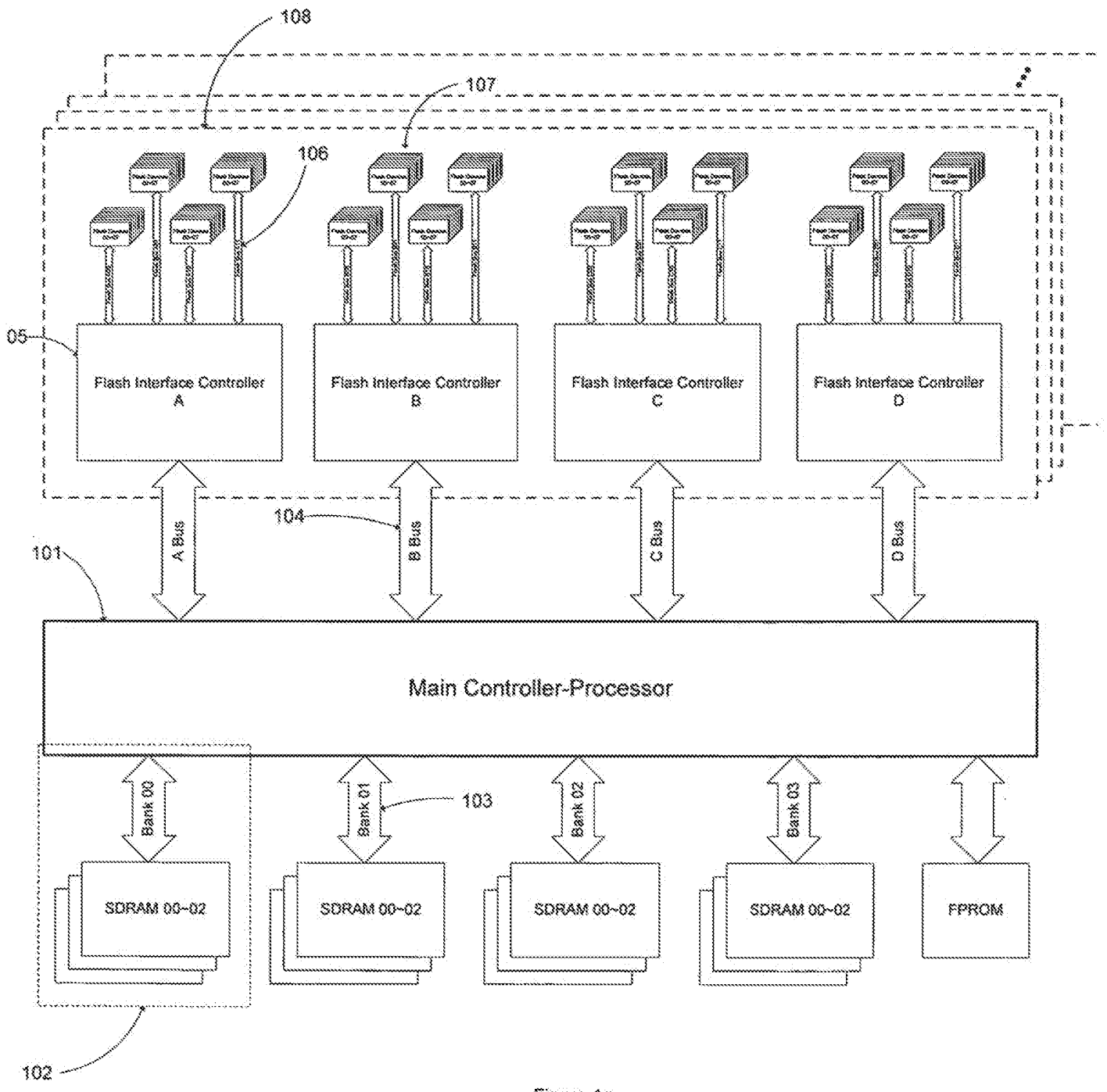

108
107
106
105
Flash Interface Controller A
Flash Interface Controller B
Flash Interface Controller C
Flash Interface Controller D
104
A Bus
B Bus
C Bus
D Bus
101
Main Controller-Processor
Bank 00
Bank 01
Bank 02
Bank 03
103
SDRAM 00~02
SDRAM 00~02
SDRAM 00~02
SDRAM 00~02
FPROM
102

Figure 1a

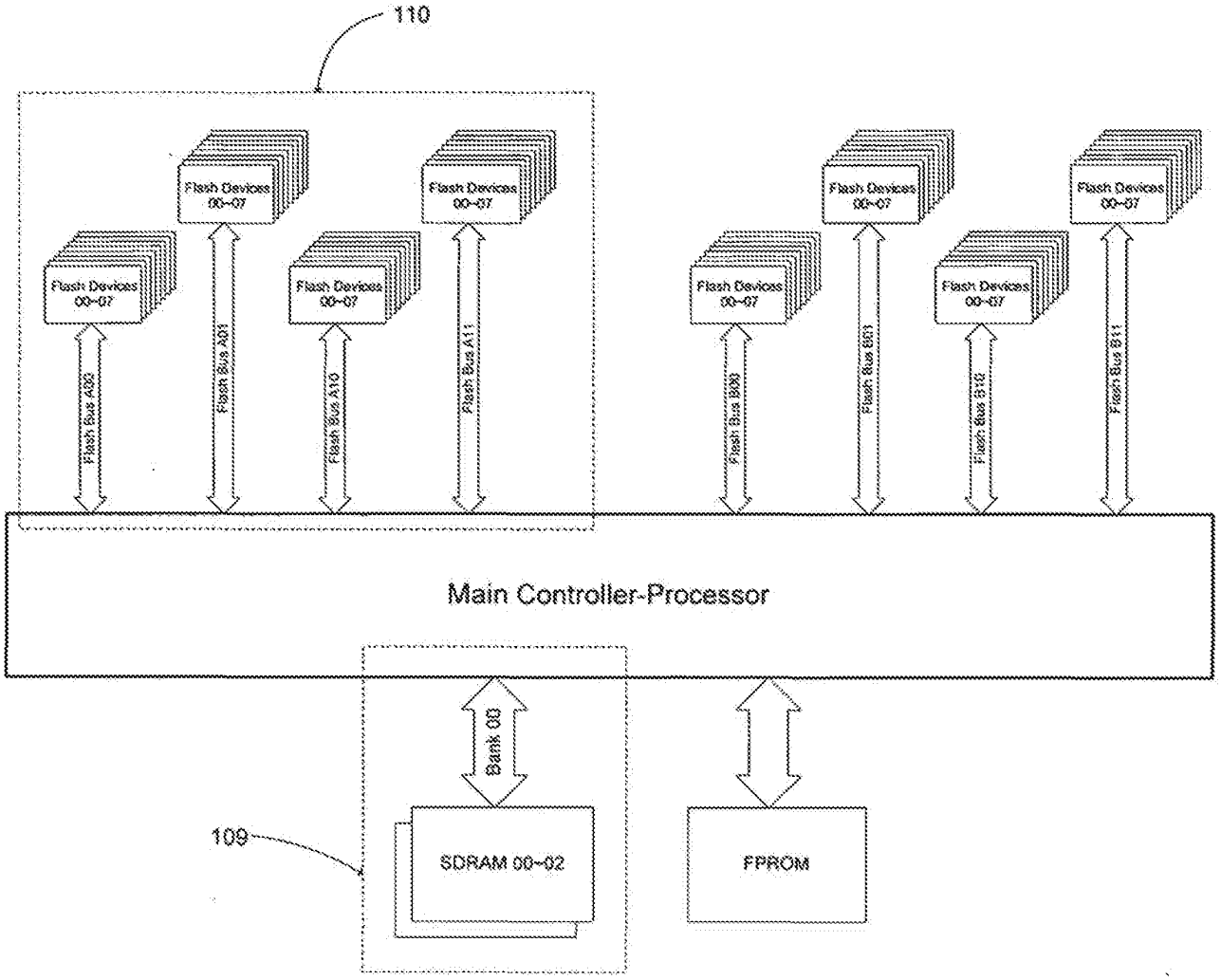


Figure 1b

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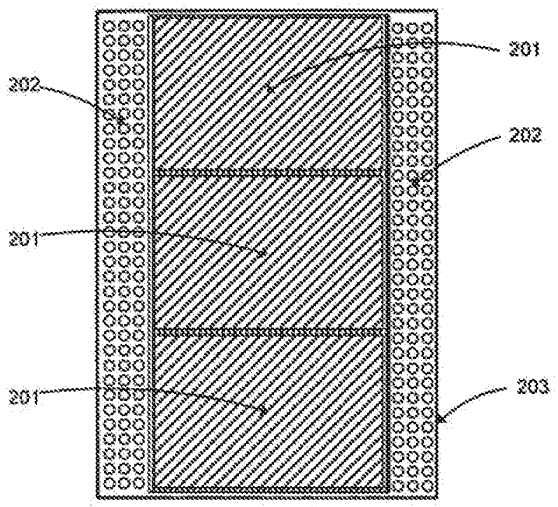


Figure 2a

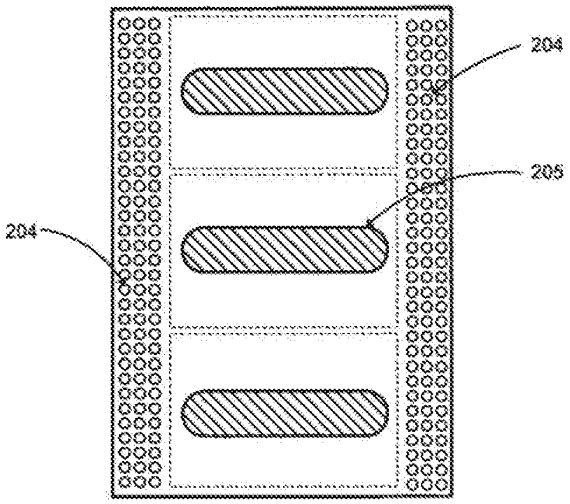


Figure 2b

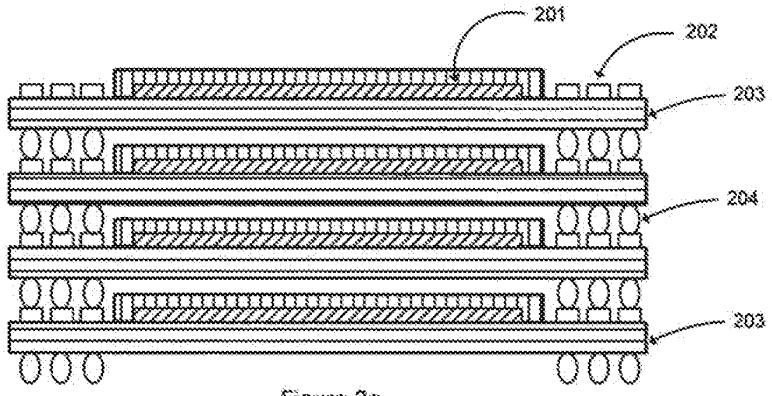


Figure 2c

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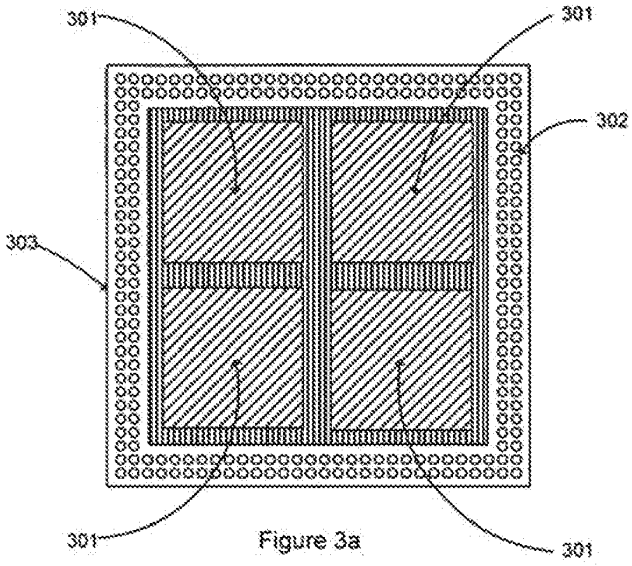


Figure 3a

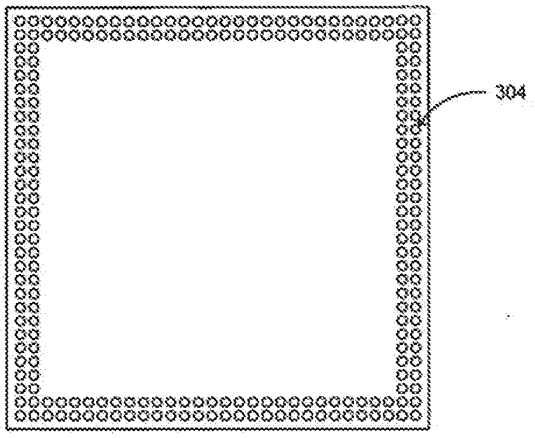


Figure 3b

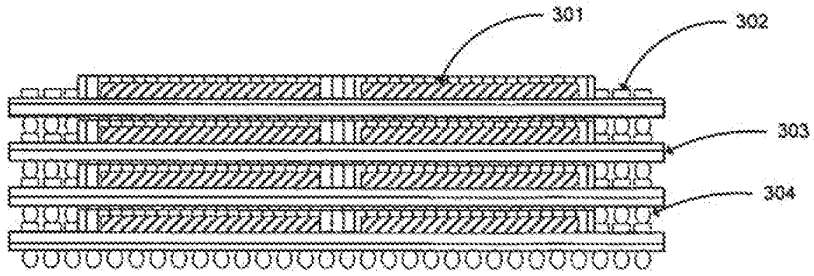


Figure 3c

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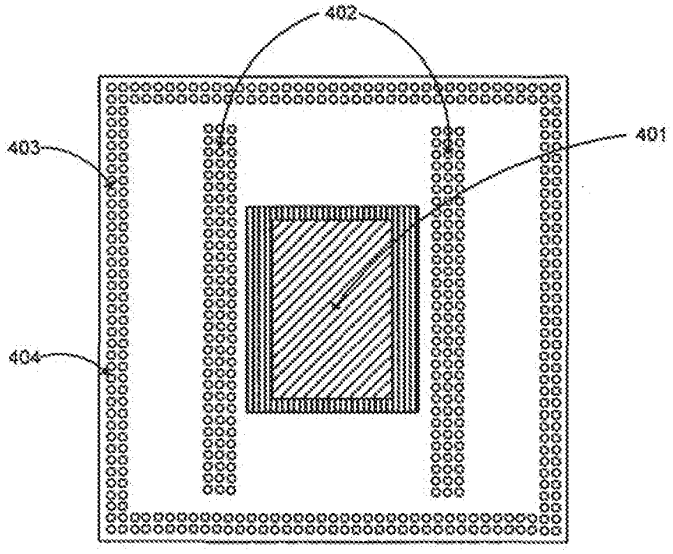


Figure 4a

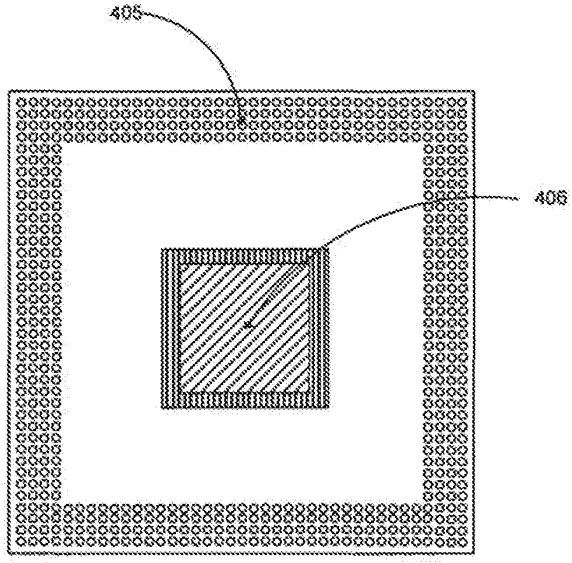


Figure 4b

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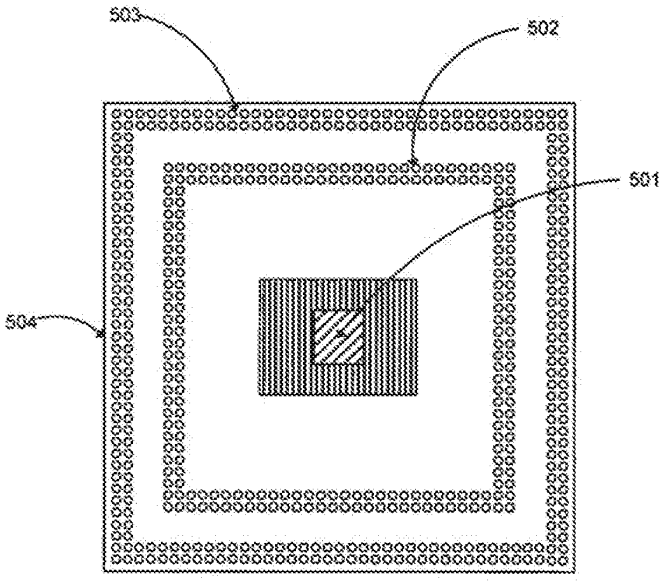


Figure 5a

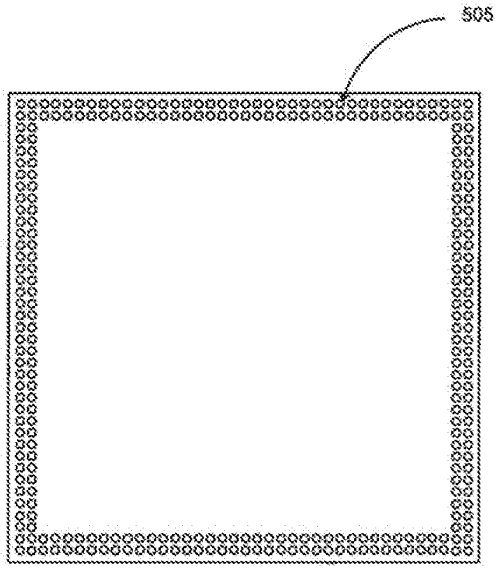


Figure 5b

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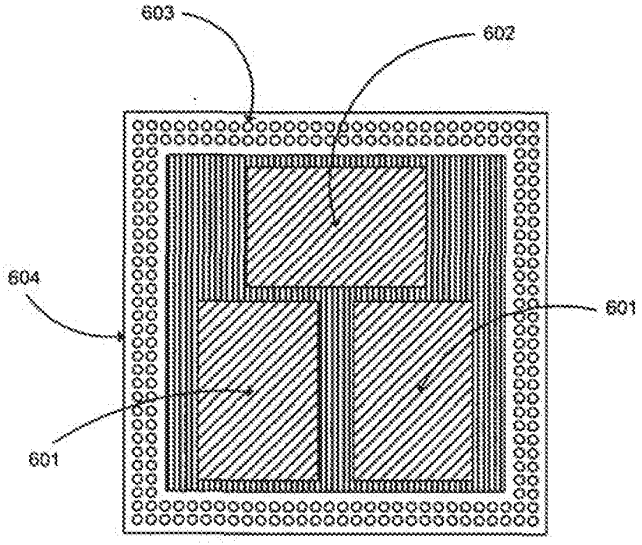


Figure 6a

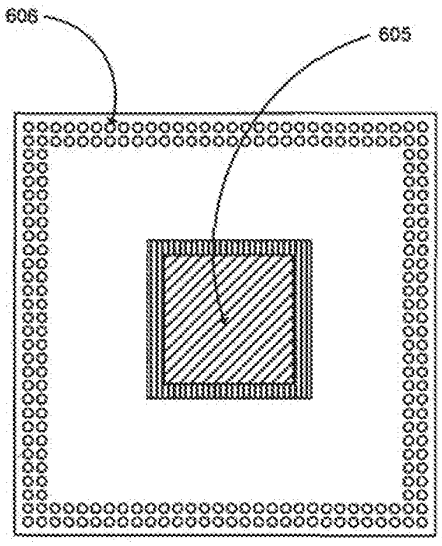


Figure 6b

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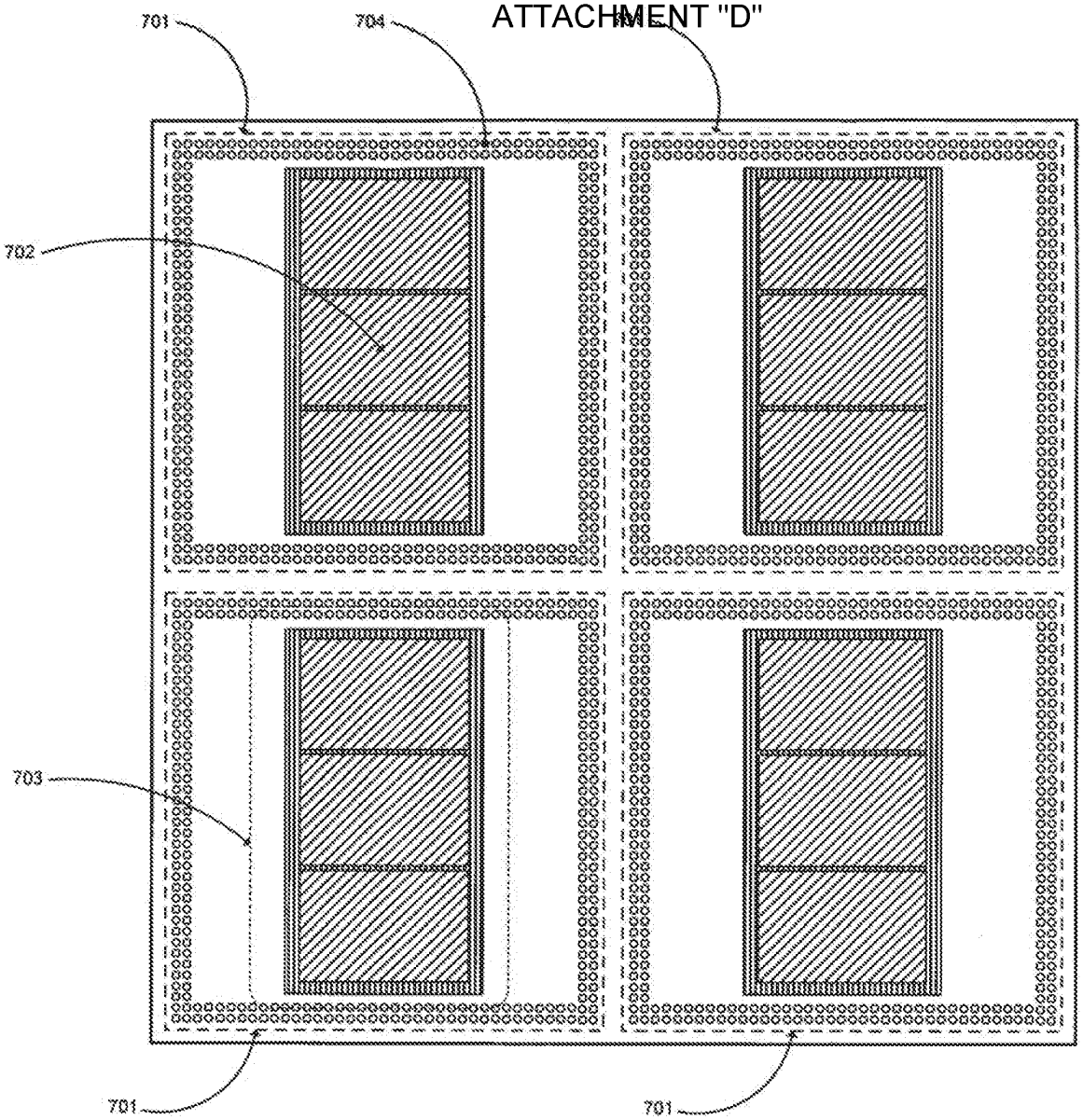


Figure 7a

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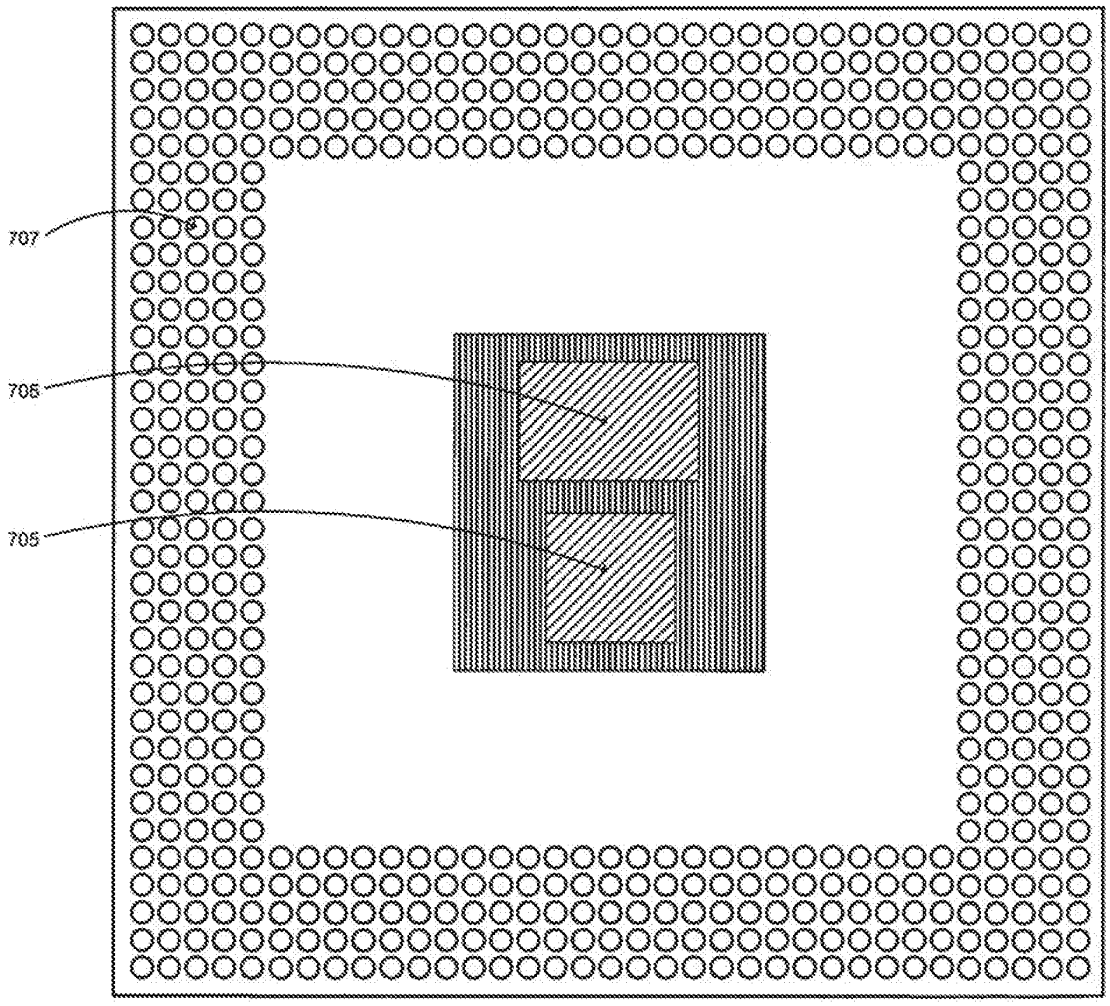


Figure 7b

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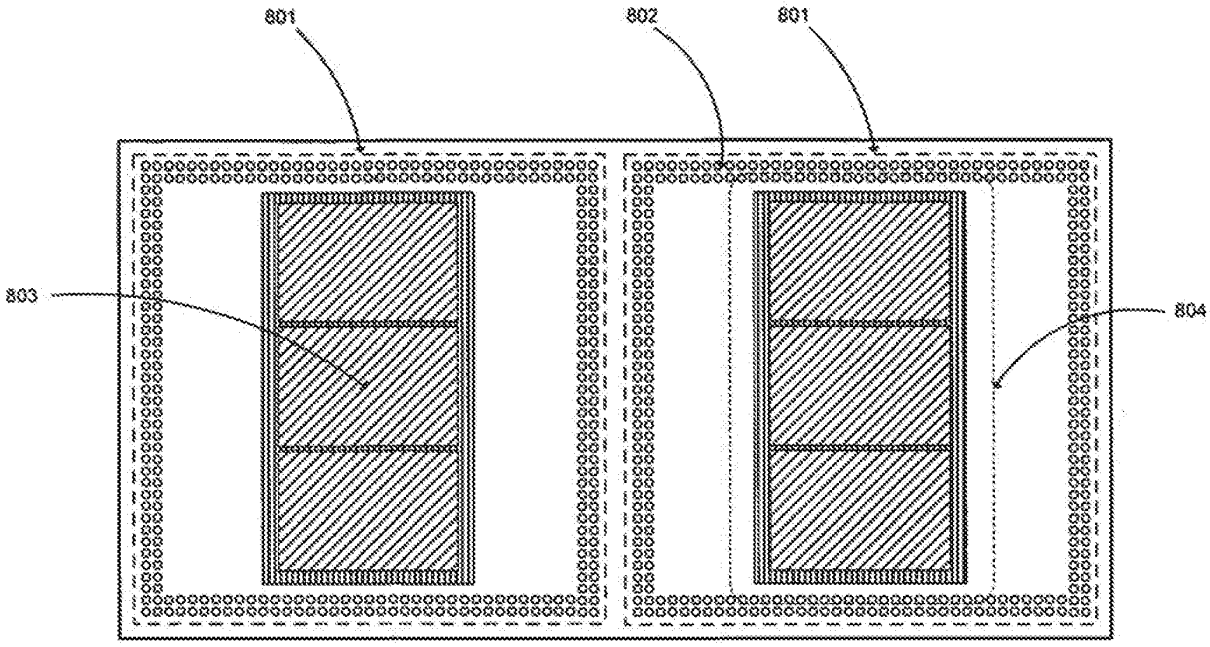


Figure 8a

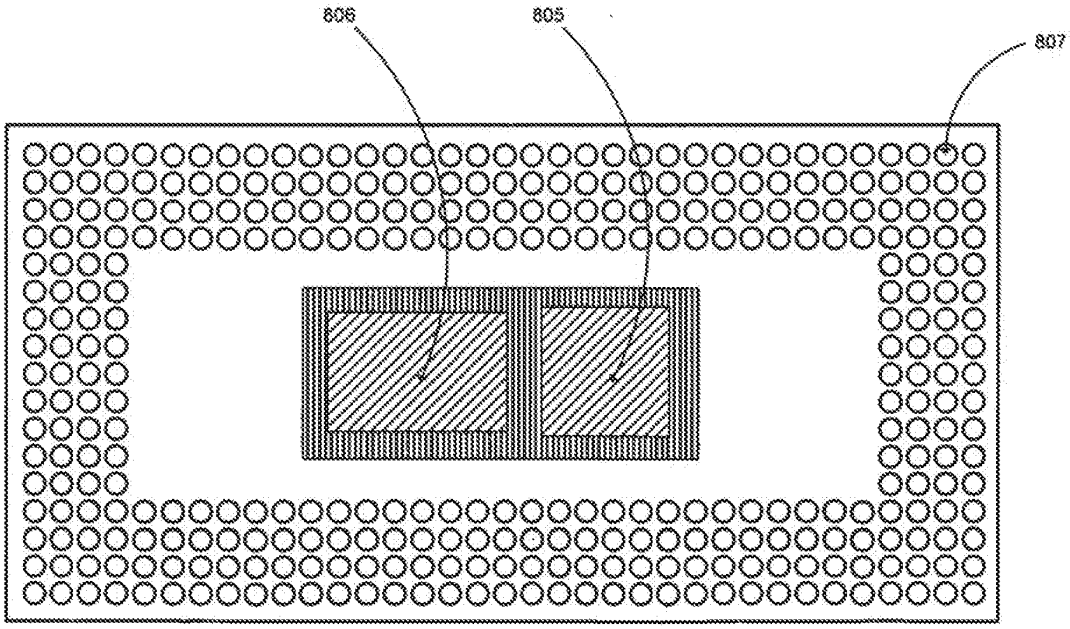


Figure 8b

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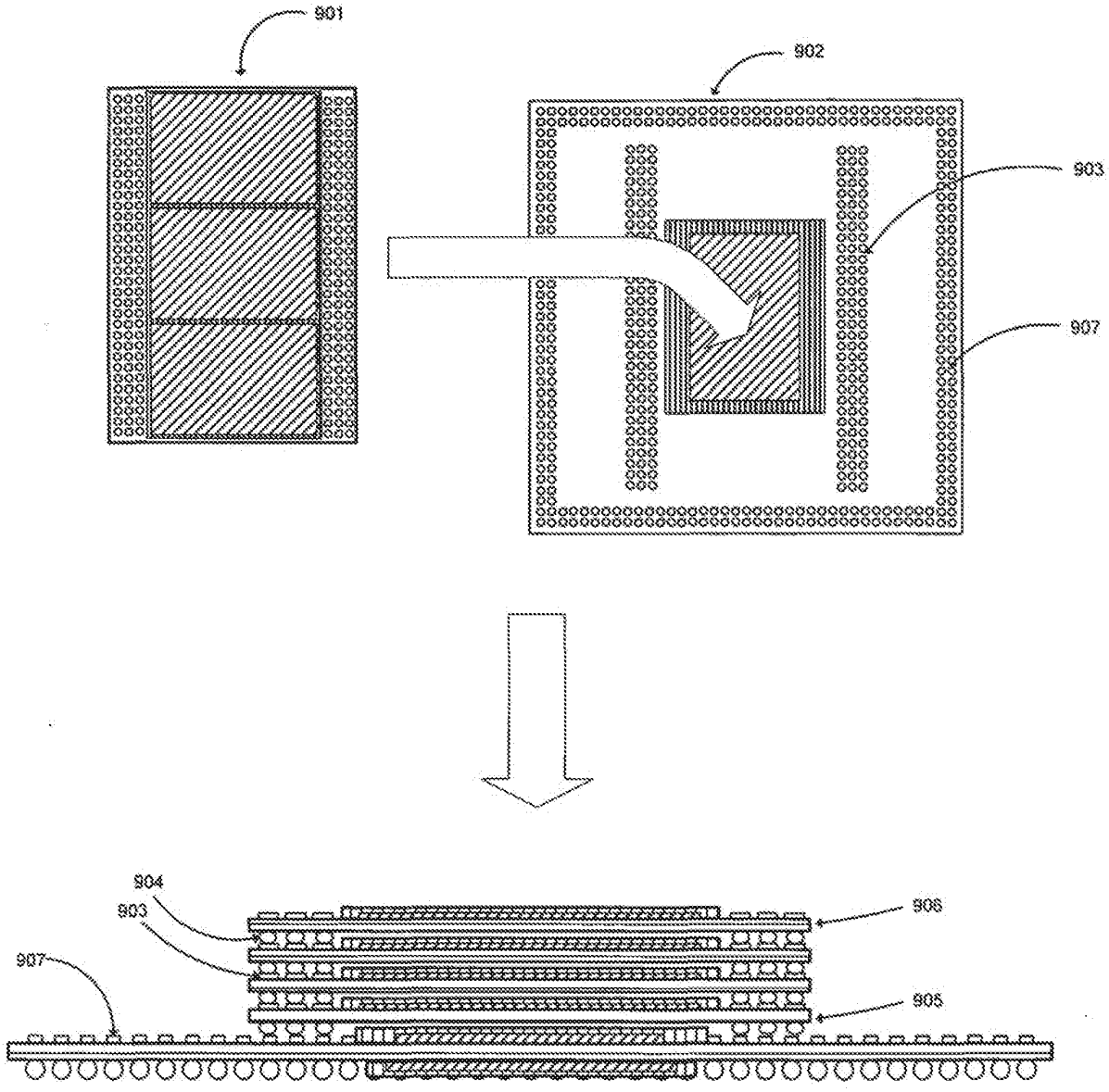


Figure 9

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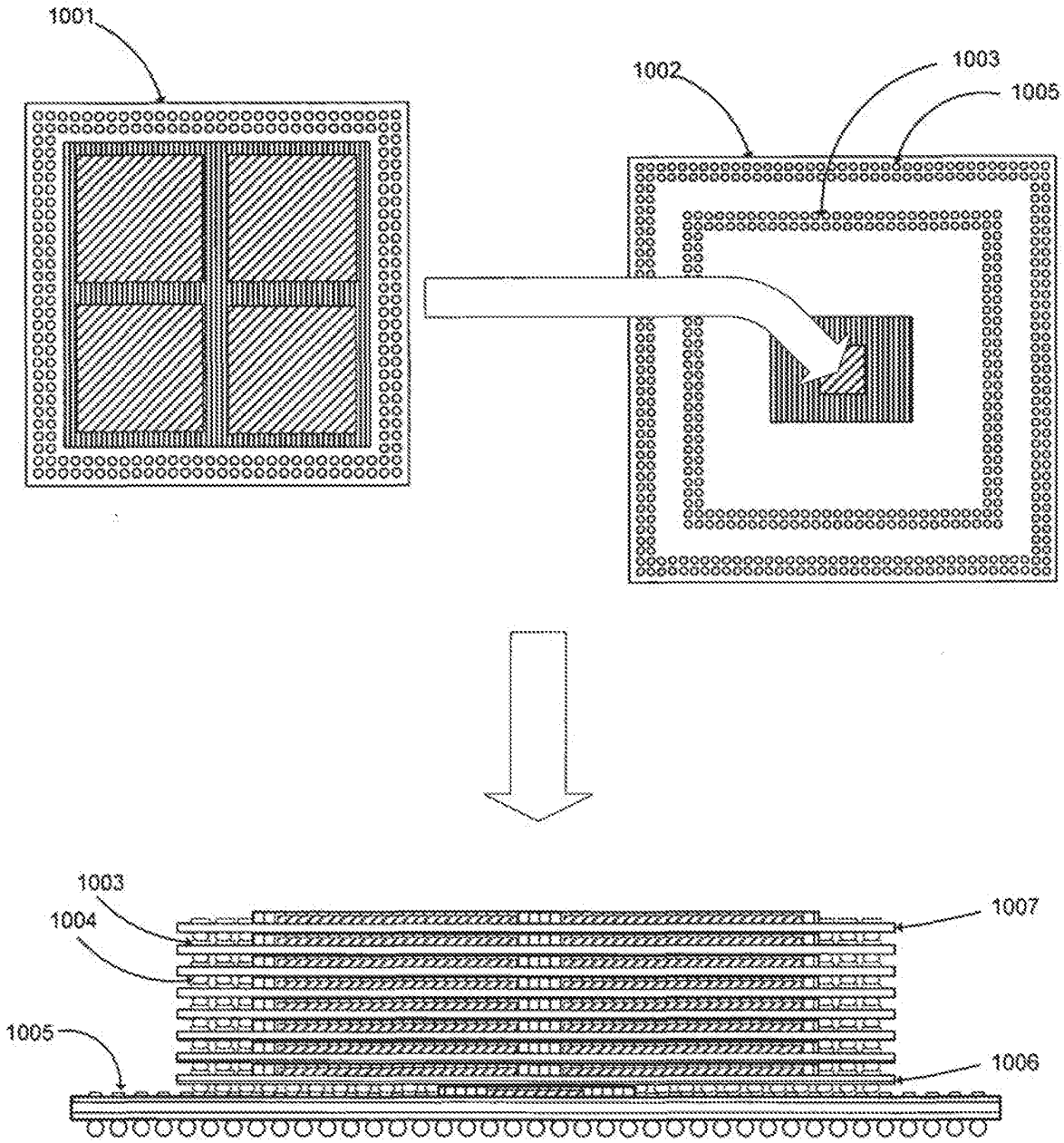


Figure 10

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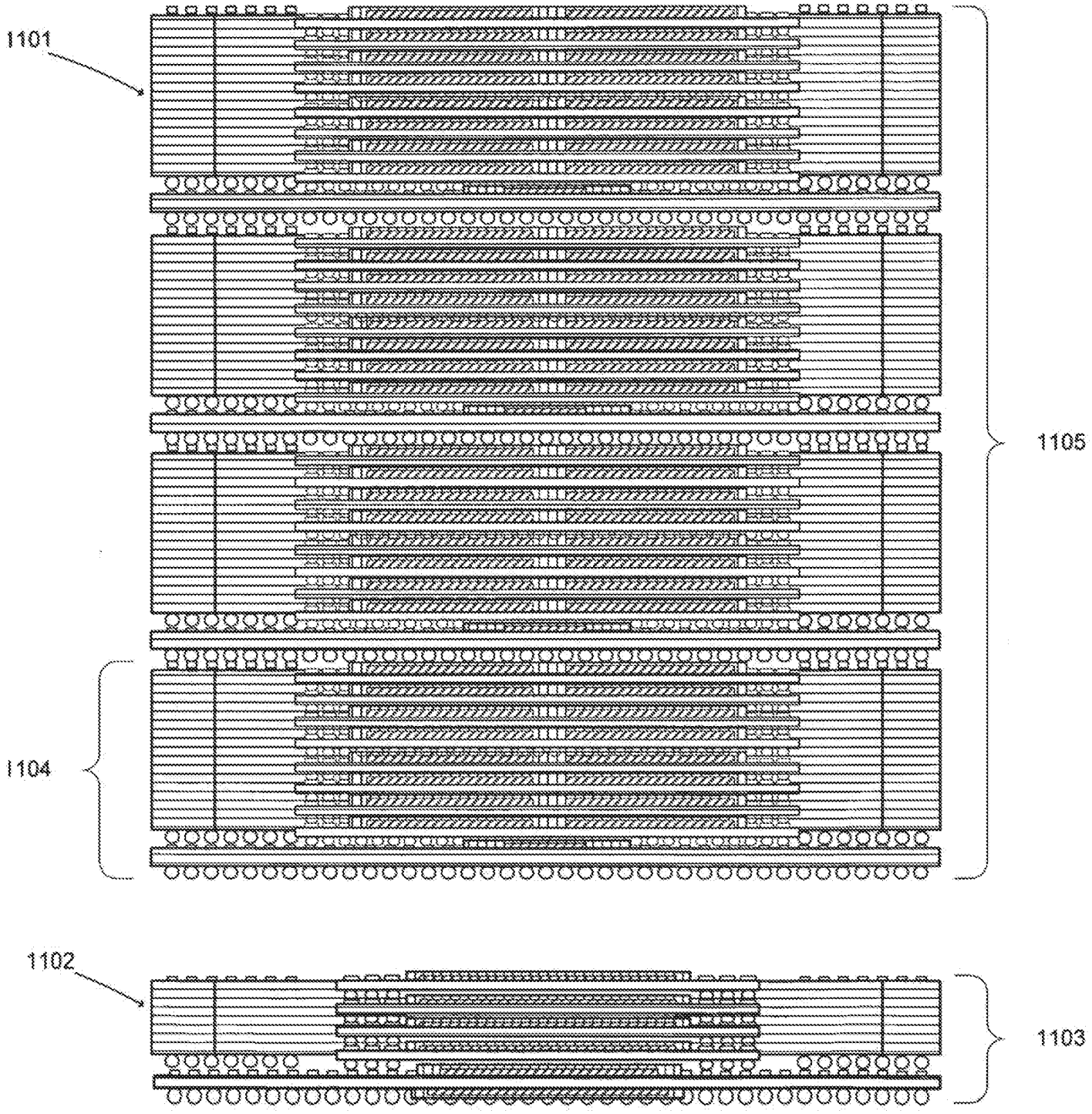


Figure 11

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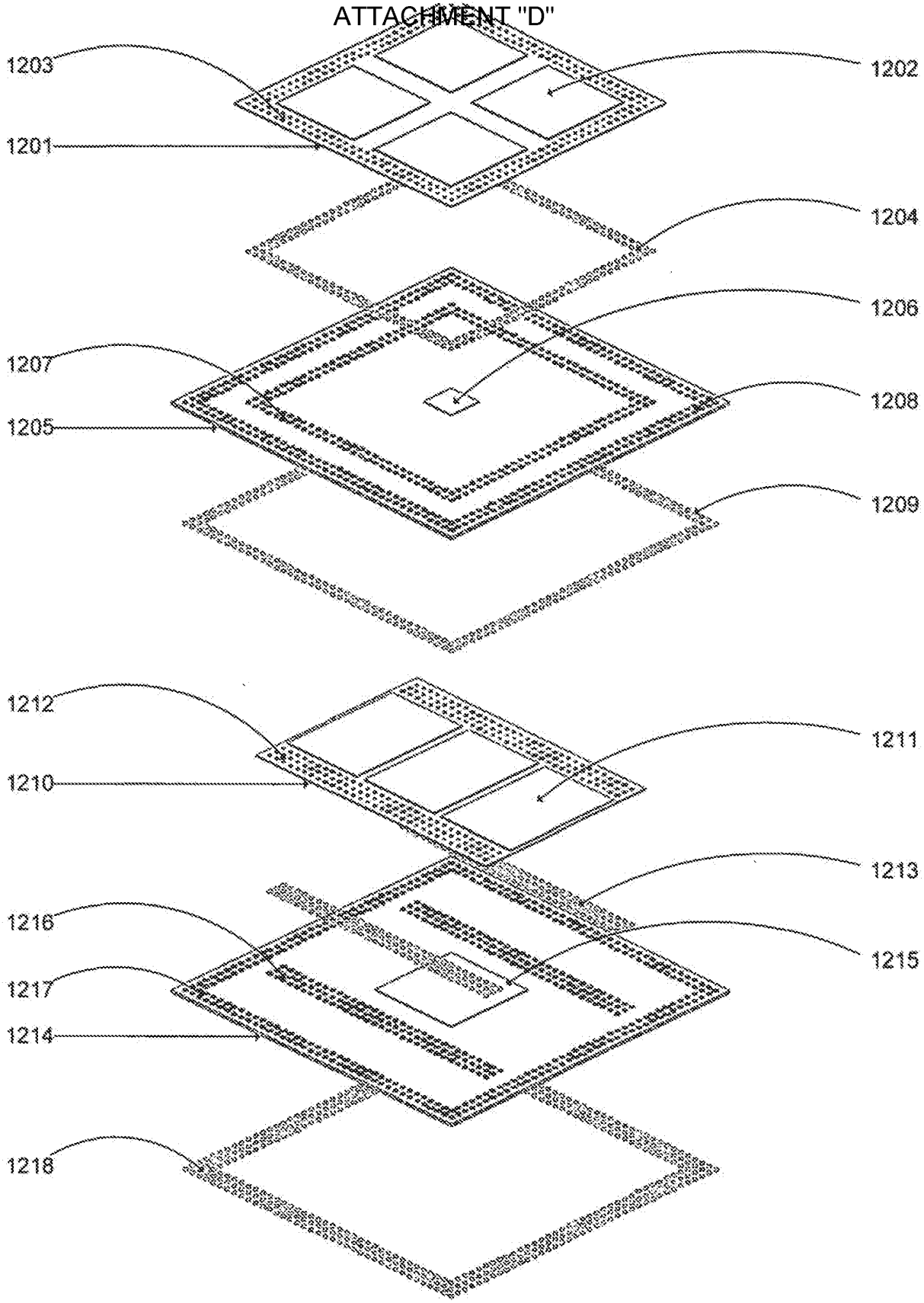


Figure 12a

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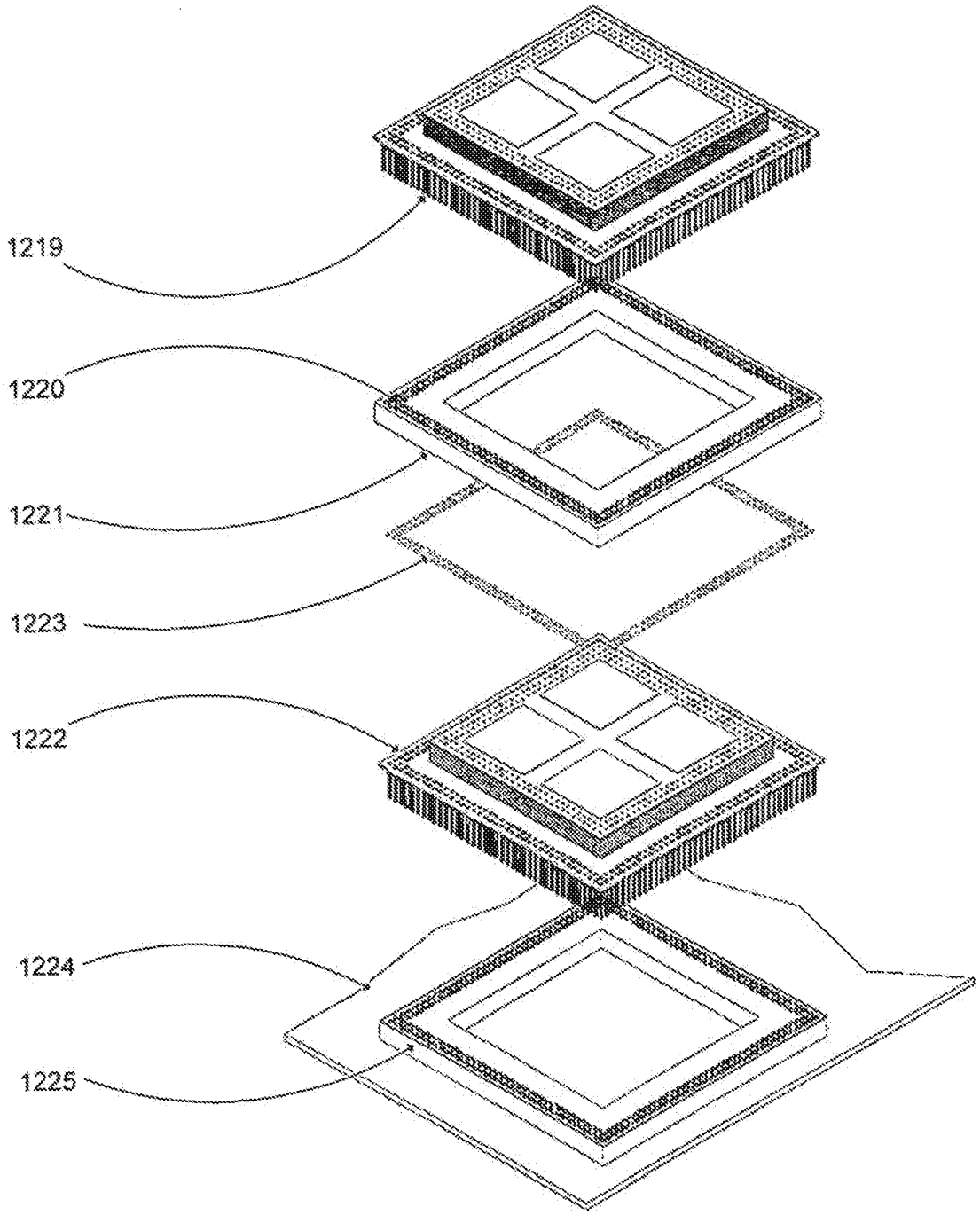


Figure 12b

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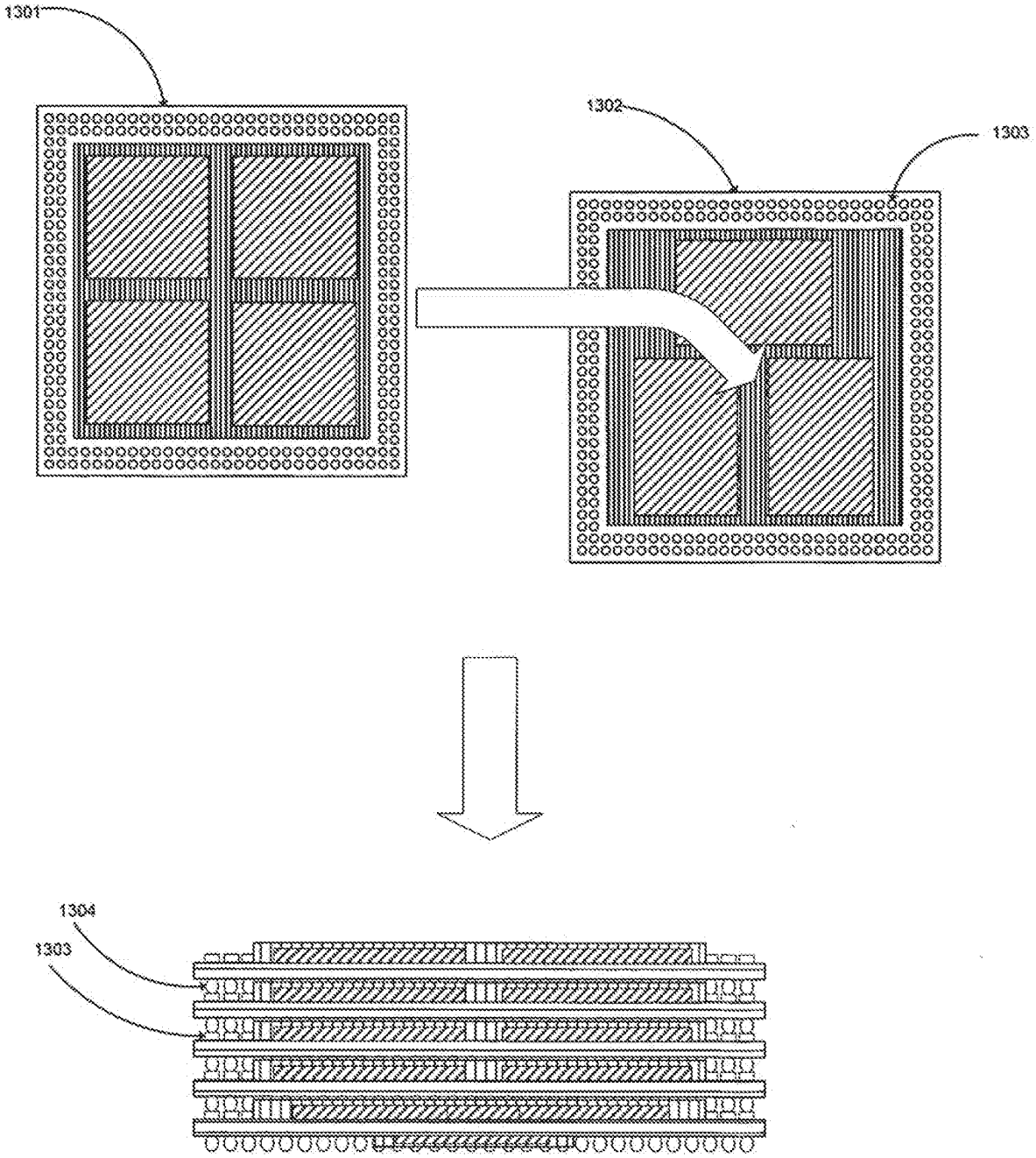


Figure 13

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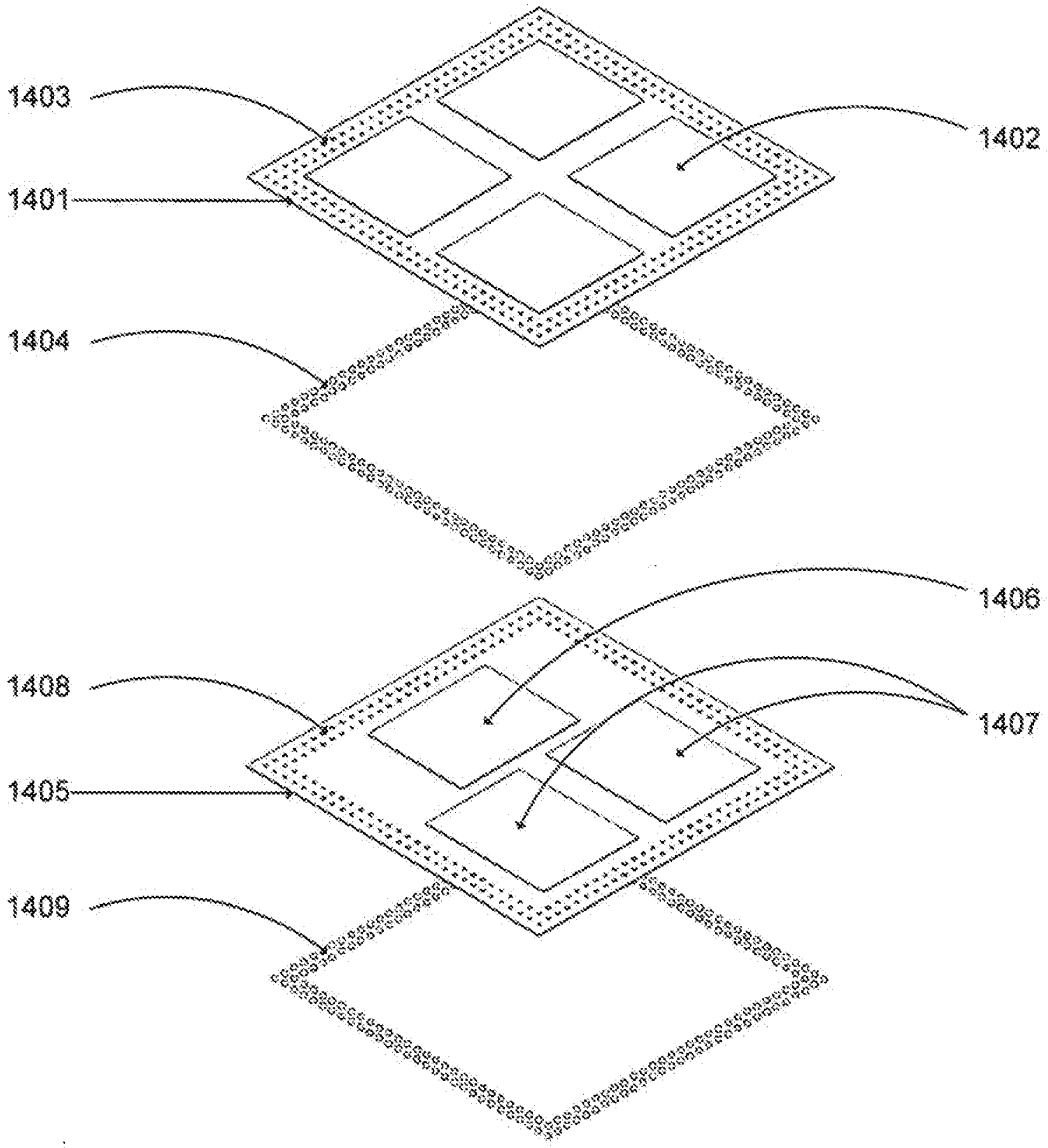


Figure 14

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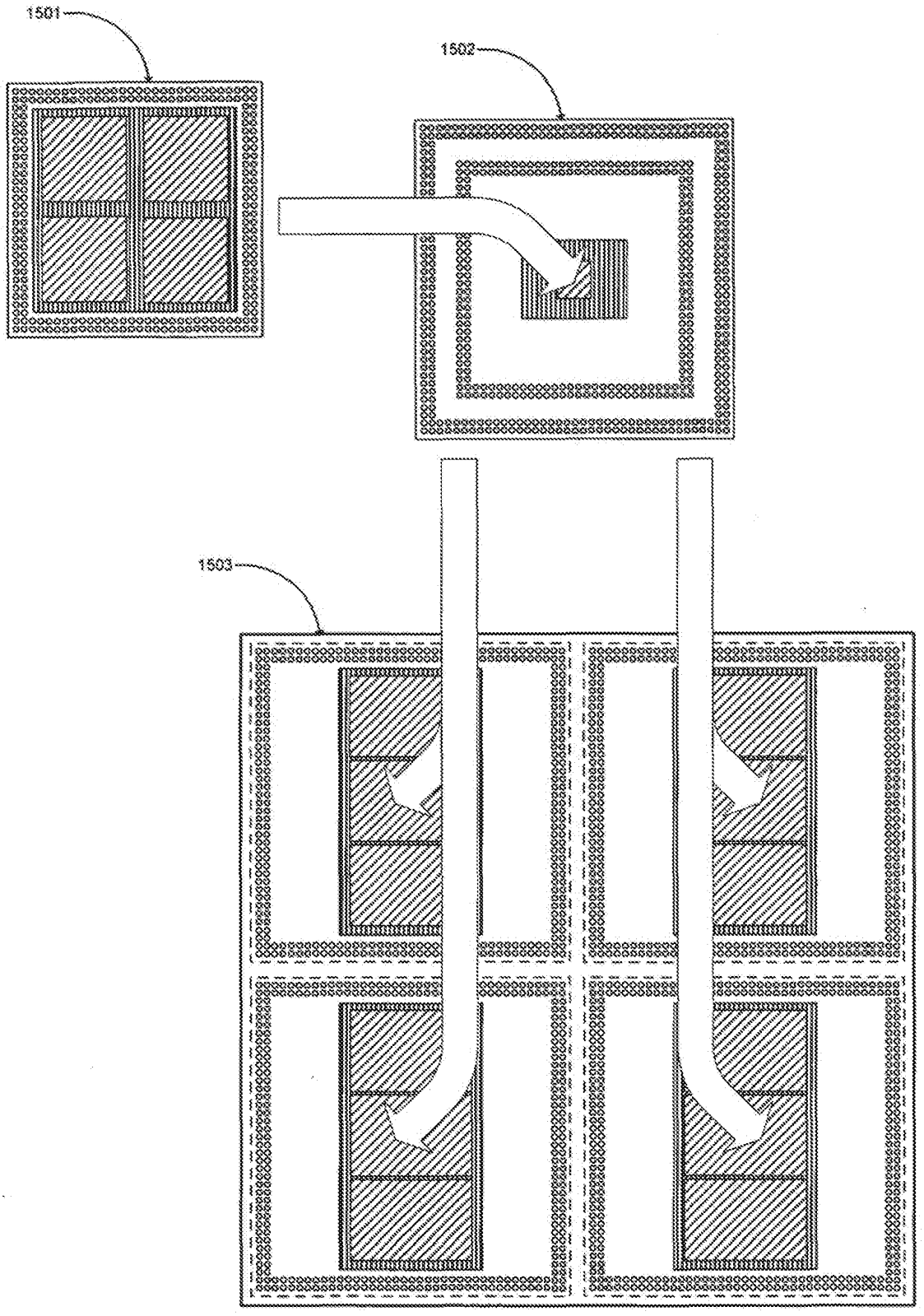


Figure 15a

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Figure 15b

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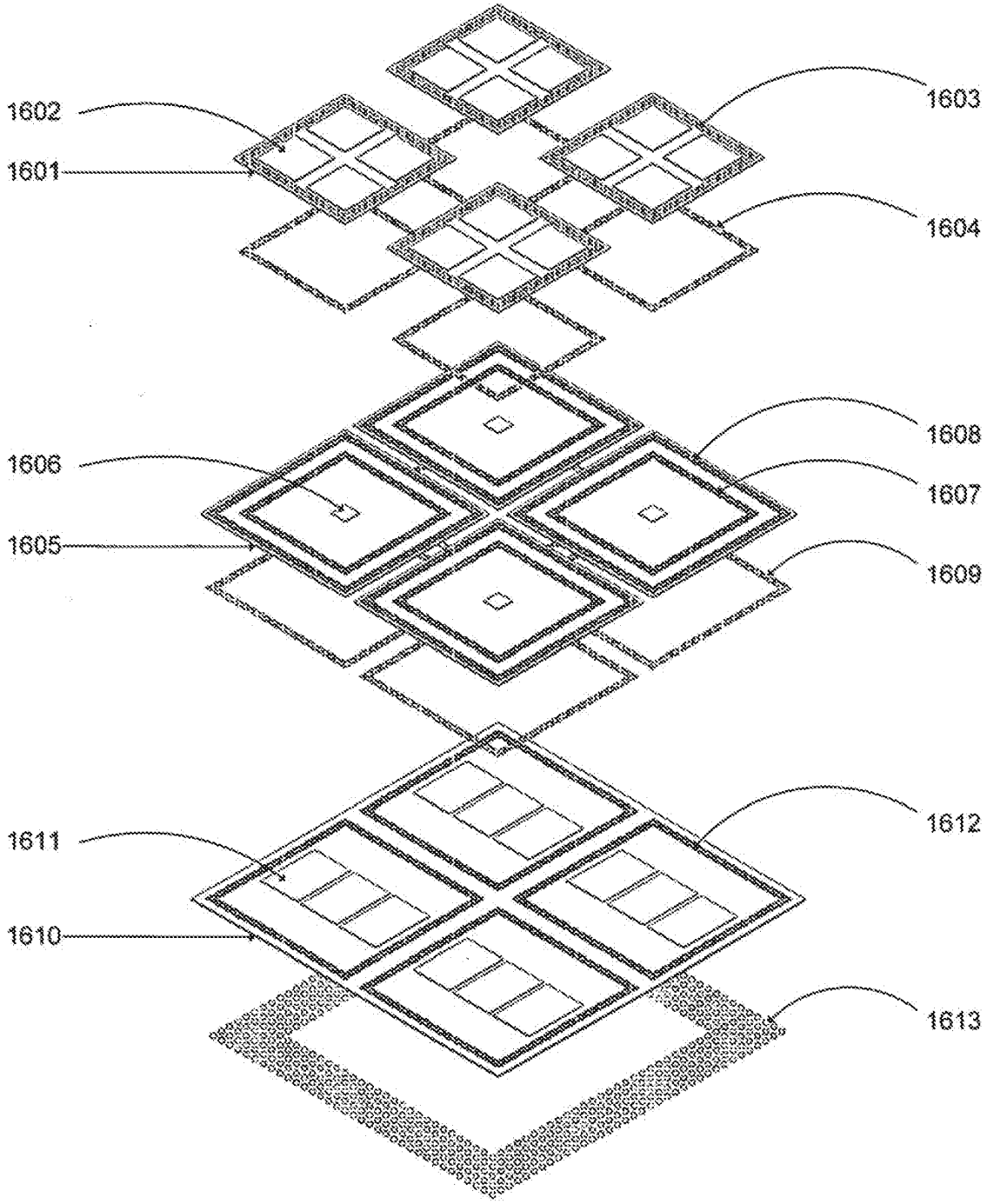


Figure 16

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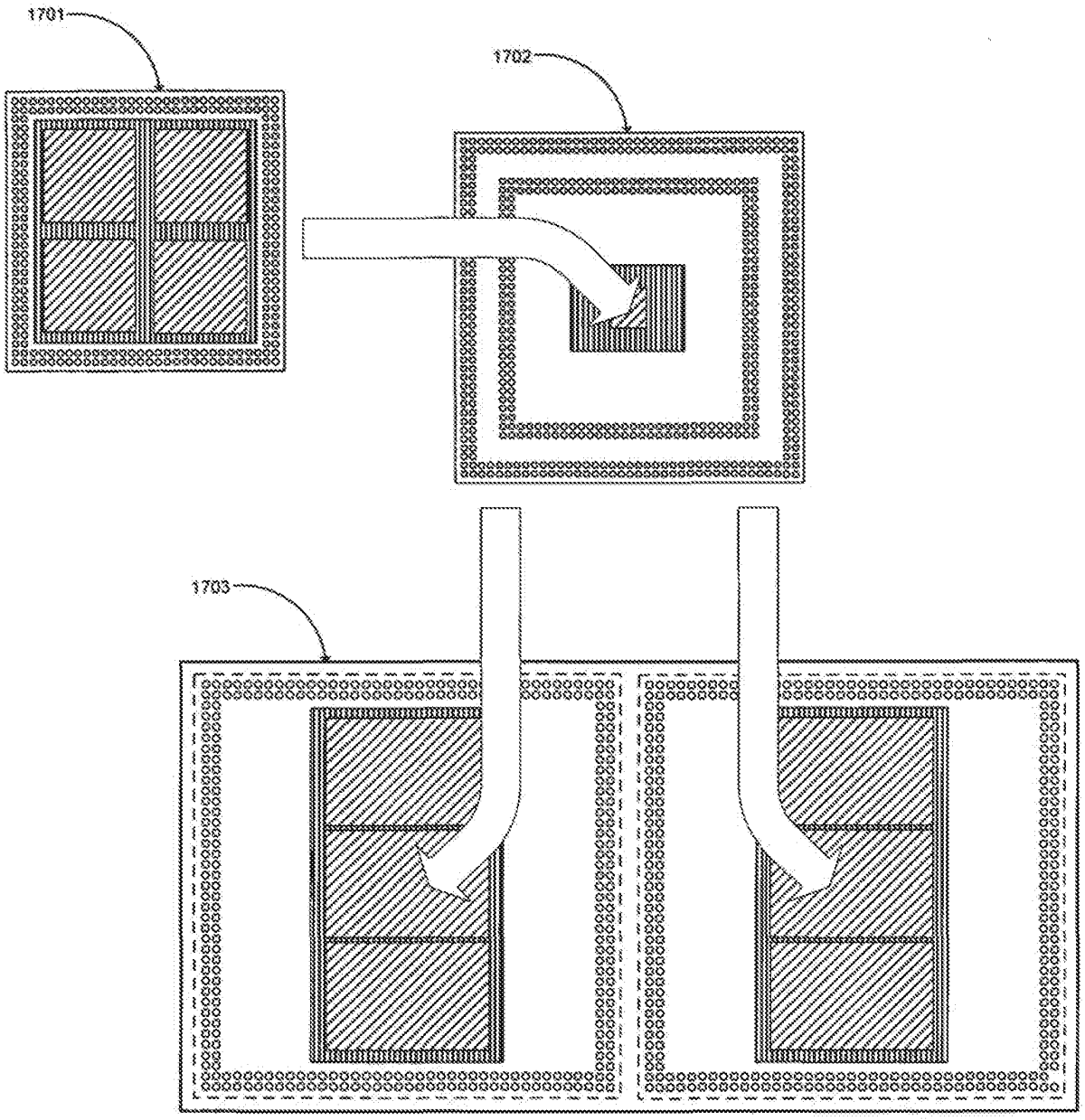


Figure 17a

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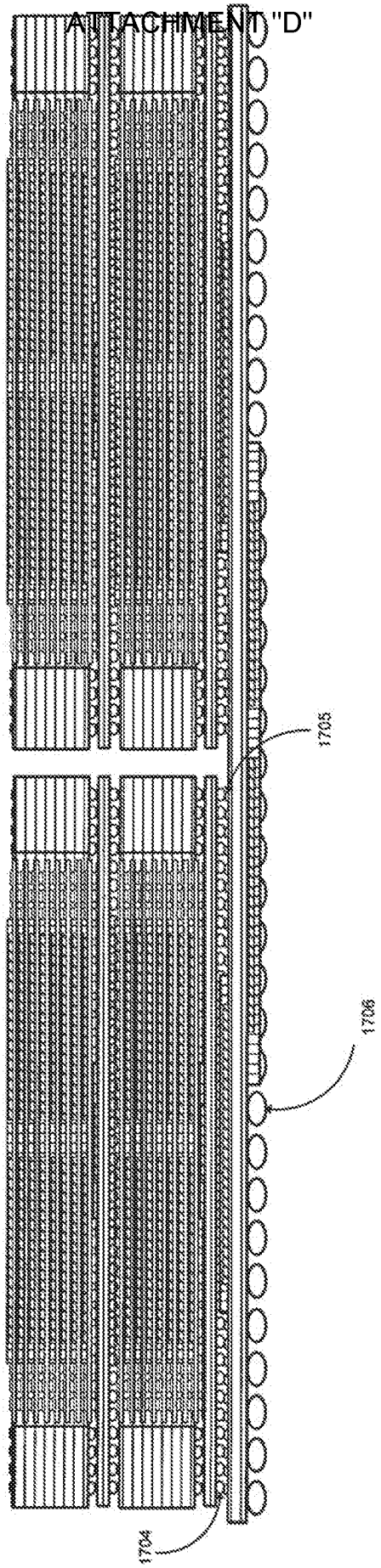


Figure 17b

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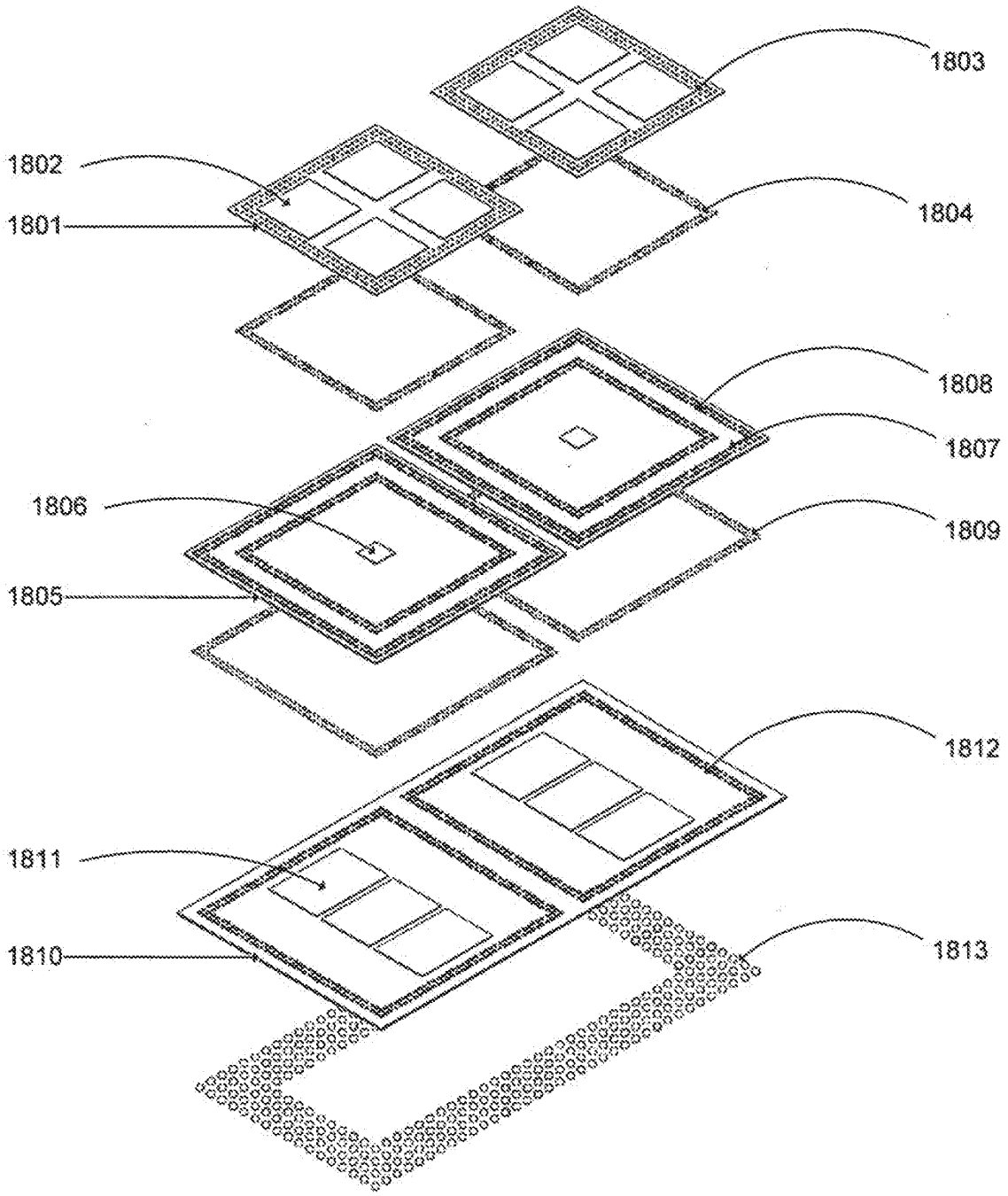

1803
1802
1801
1804
1808
1807
1806
1809
1805
1812
1811
1810
1813

Figure 18

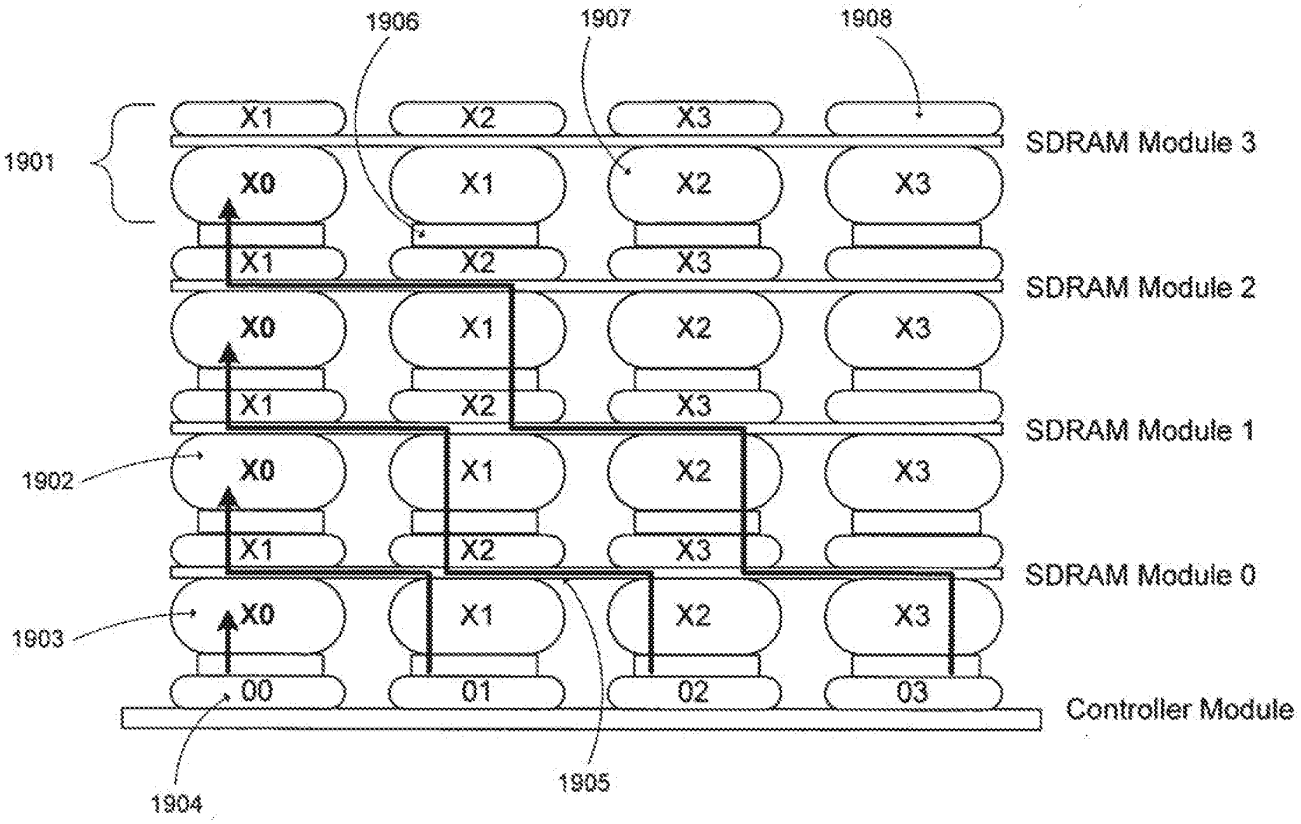

1906
1907
1908
1901
X1
X2
X3
X0
SDRAM Module 3
SDRAM Module 2
SDRAM Module 1
SDRAM Module 0
1902
1903
00
01
02
03
Controller Module
1904
1905

Figure 19

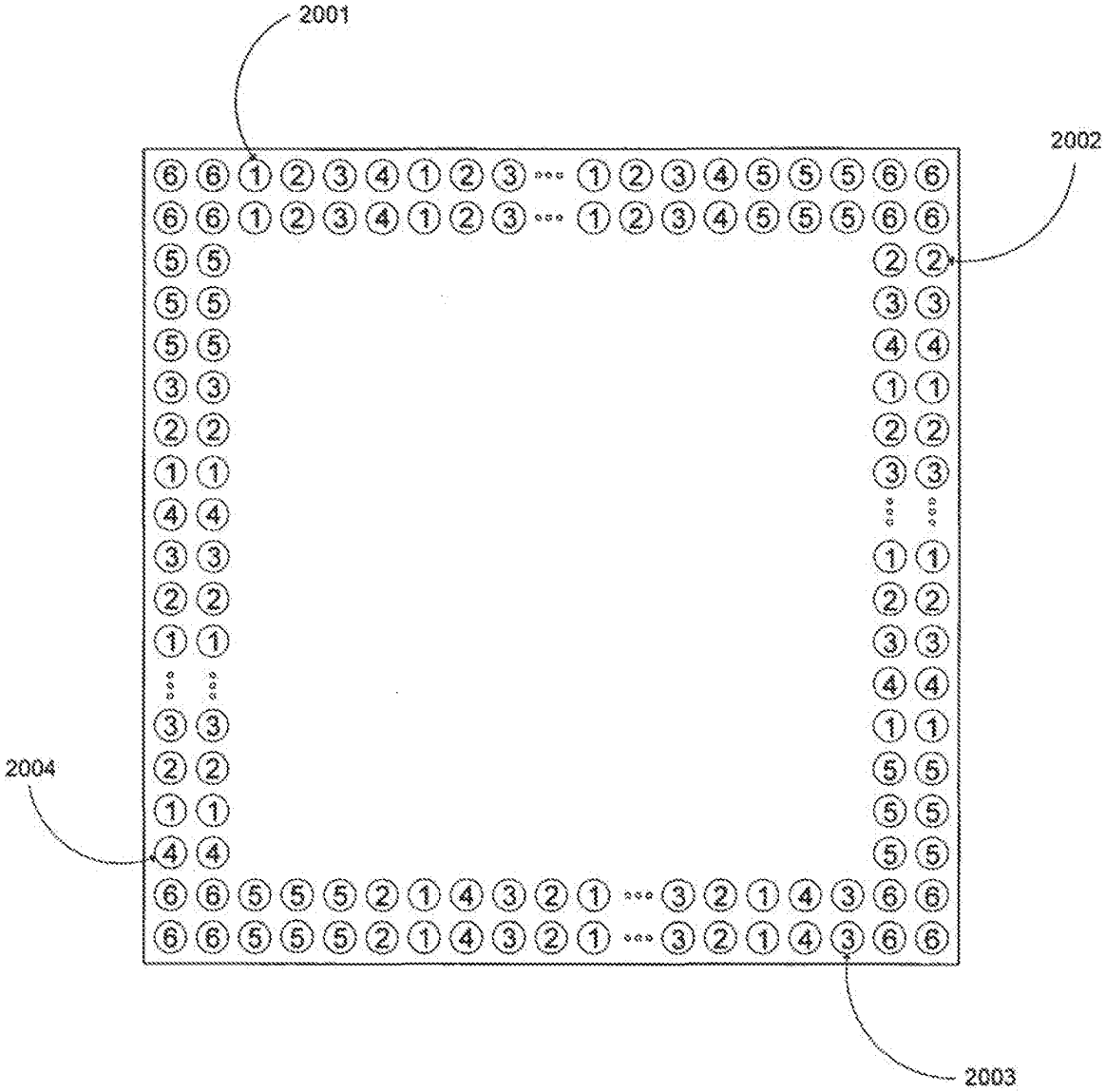


Figure 20a

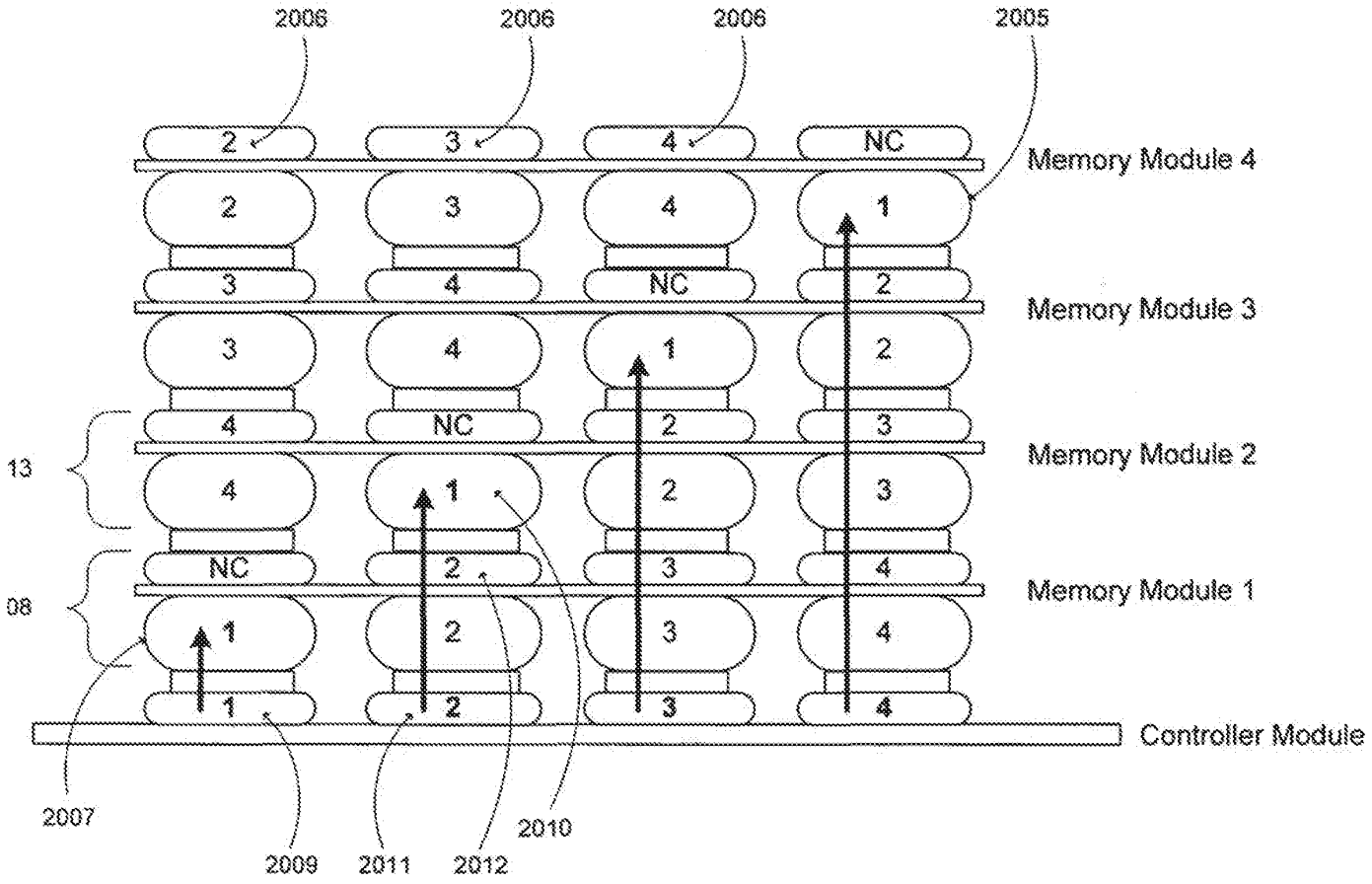

2006
2006
2006
2005
Memory Module 4
Memory Module 3
Memory Module 2
Memory Module 1
Controller Module
13
08
NC
2007
2009
2011
2012
2010

Figure 20b

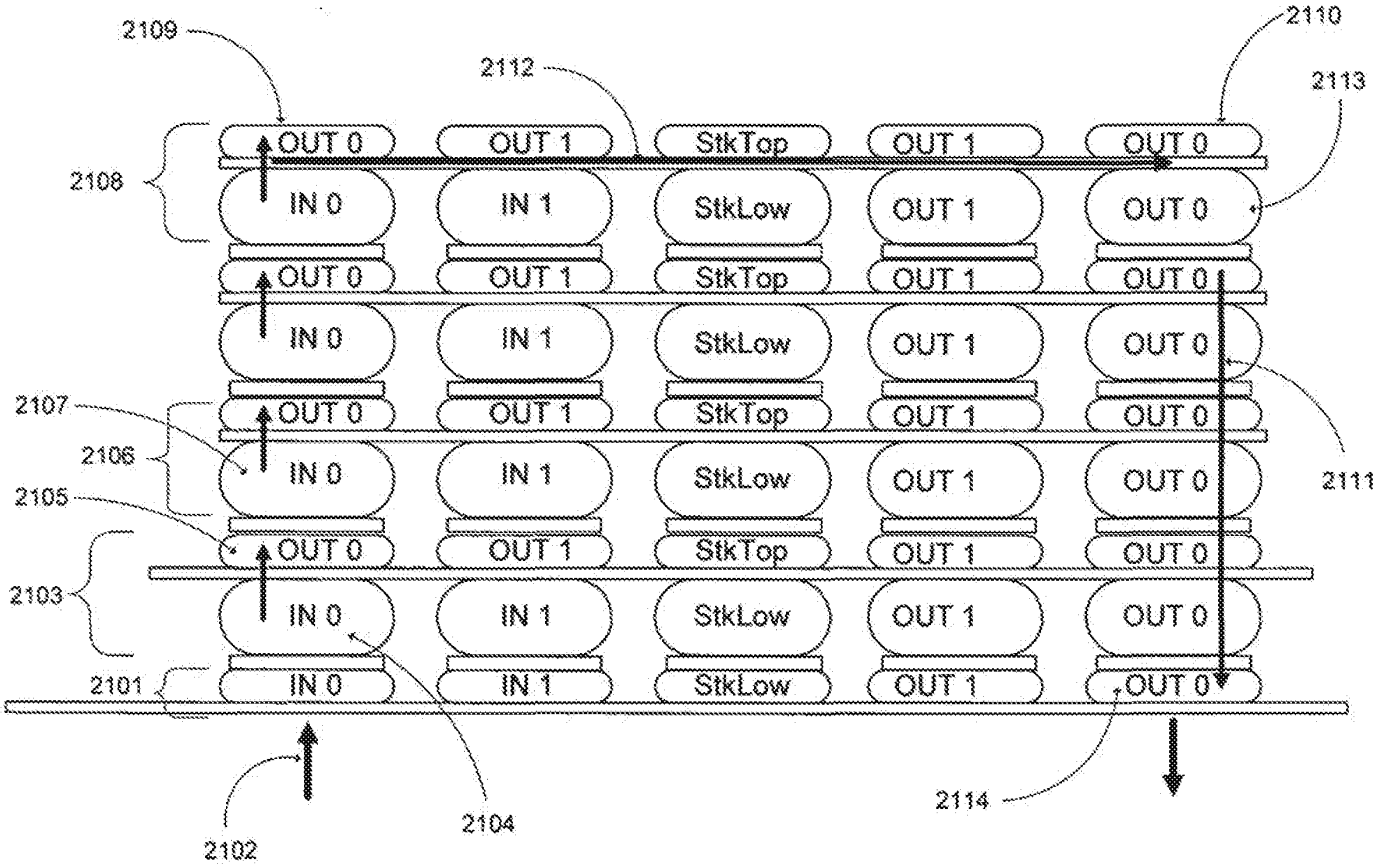

2109
2112
2110
2113
2108
OUT 0
OUT 1
StkTop
OUT 1
OUT 0
IN 0
IN 1
StkLow
OUT 1
OUT 0
2107
2106
2105
2103
2101
2111
2102
2104
2114

Figure 21a

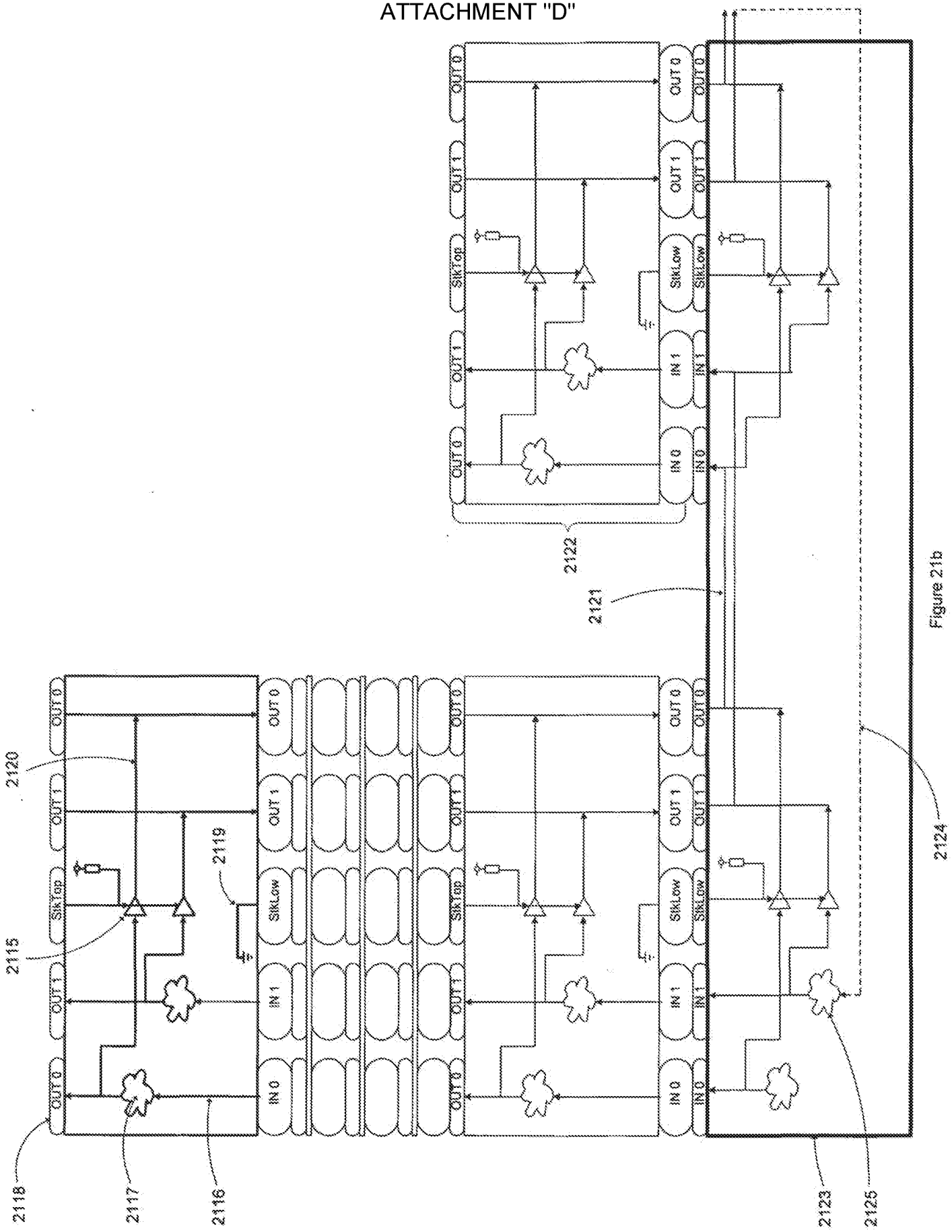

OUT 0
OUT 1
SlkTop
SlkLow
IN 1
IN 0
2120
2115
2119
2118
2117
2116
2122
2121
2124
2123
2125

Figure 21b

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: BRUCE et al.	)	Group Art Unit: 2892
Serial No.: 11/322,442	)	Examiner: ULLAH, Elias
Application Filing Date: 29 Dec 2005	)	
For: MULTIPLE CHIP MODULE AND PACKAGE AND PACKAGE STACKING METHOD FOR STORAGE DEVICE	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY TO FIRST OFFICE ACTION ON THE MERITS

Dear Examiner:

In response to the Office Action, mailed 13 August 2008, please kindly amend this Application as follows and consider the remarks set forth below.

Amendments to the Specification begin on page 2;

A listing of claims begins on page 3;

Amendment(s) to the Drawings begins on page 13; and

Remarks begin on page 16 of this paper.

Replacement sheets of drawings and a substitute specification incorporating the changes proposed in the Amendments to the Drawings and to the Specification, respectively, are attached to this paper.

Amendment(s) to the Specification

The specification has been amended to correct minor grammatical errors. These amendments are provided by submitting a substitute specification (excludes Claims but includes Abstract) in accordance with MPEP 608.01. No new matter has been added. A marked up copy of the substitute specification is attached, showing all changes relative to the immediate prior version as required under MPEP 608.01(q). In addition, a copy of the substitute specification without markings is also attached in accordance with 37 CFR 1.125(c). No new matter has been added to the specification.

Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (CANCELLED) A method for stacking a plurality of modules comprising the steps of:

providing one or more active port on the plurality of modules for carrying one or more active signal;

providing one or more passive port on the plurality of modules for passing through the one or more active signals; and

stacking the plurality of modules.

2. (CANCELLED) The method of claim 1 wherein the one or more passive port forms a ladder like routing path.

3. (CANCELLED) The method of claim 1 wherein one or more of the plurality of module is rotated before being stacked and the one or more passive port forms a rotational routing path.

4. (CANCELLED) The method of claim 1 further comprising the step of providing one or more pair of daisy chain input port and daisy chain output port for forming a first daisy chain connection wherein each pair of the daisy chain input port and the daisy chain output port are connected through a daisy chain circuit.

5. (CANCELLED) The method of claim 4 further comprising the step of providing one or more control port for enabling a routing path extending the first daisy chain connection within an end module.

6. (CANCELLED) The method of claim 5 wherein the routing path within the end module is connected to a second daisy chain connection.

7. (CANCELLED) The method of claim 1 wherein one or more of the plurality of modules is a main board.

8. (CANCELLED) The method of claim 7 wherein one or more vertically stacked module is connected to the main board.

9. (CANCELLED) The method of claim 2:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located between a pre-determined distance to each other in a repeating pattern, the pre-determined distance equaling a multiple of a periodic distance of the repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the ladder like routing path; and

wherein the ladder like routing path comprises one or more passive ball and one or more passive pad.

10. (CANCELLED) The method of claim 3:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located opposite each other in a repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the rotational routing path; and

wherein the rotational routing path comprises one or more passive ball and one or more passive pad.

11. (CANCELLED) The method of claim 4:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive

pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection; and

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad.

12. (CANCELLED) The method of claim 5:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad; and

wherein the routing path comprises one or more tri-state driver controlled by the one or more control port.

13. (CANCELLED) The method of claim 6:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad;

wherein the routing path comprises one or more tri-state driver controlled by the one or more control port; and

wherein one or more daisy chain connection are extended through one or more vertically stacked module connected to a main board.

14. (ORIGINAL) A stacked module comprising a plurality of modules each comprising:

one or more active port for carrying one or more active signal; and

one or more passive port for passing through the one or more active signals.

15. (ORIGINAL) The stacked module of claim 14 wherein the one or more passive port forms a ladder like routing path.

16. (ORIGINAL) The stacked module of claim 14 wherein one or more of the plurality of module is rotated before being stacked and the one or more passive port forms a rotational routing path.

17. (WITHDRAWN) The stacked module of claim 1 further comprising one or more pair of daisy chain input port and daisy chain output port for forming a first daisy chain connection wherein each pair of the daisy chain input port and the daisy chain output port are connected through a daisy chain circuit.

18. (WITHDRAWN) The stacked module of claim 17 further comprising one or more control port for enabling a routing path extending the first daisy chain connection within an end module.

19. (WITHDRAWN) The stacked module of claim 18 wherein the routing path within the end module is connected to a second daisy chain connection.

20. (ORIGINAL) The stacked module of claim 14 wherein one or more of the plurality of modules is a main board.

21. (ORIGINAL) The method of claim 20 wherein one or more vertically stacked module is connected to the main board.

22. (ORIGINAL) The stacked module of claim 15:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located between a pre-determined distance to each other in a repeating pattern, the pre-determined distance equaling a multiple of a periodic distance of the repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the ladder like routing path; and

wherein the ladder like routing path comprises one or more passive ball and one or more passive pad.

23. (ORIGINAL) The stacked module of claim 16:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located opposite each other in a repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the rotational routing path; and

wherein the rotational routing path comprises one or more passive ball and one or more passive pad.

24. (WITHDRAWN) The stacked module of claim 17:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection; and

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad.

25. (WITHDRAWN) The stacked module of claim 18:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad; and

wherein the routing path comprises one or more tri-state driver controlled by the one or more control port.

26. (WITHDRAWN) The stacked module of claim 19:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad;

wherein the routing path comprises one or more tri-state driver controlled by the one or more control port; and

wherein one or more daisy chain connection are extended through one or more vertically stacked module connected to a main board.

27. (NEW) The stacked module of claim 15, wherein:

the stacked module further includes a first outside surface and a second outside surface, the first and second outside surfaces disposed to face opposite each other;

at least one of the plurality of modules includes a first module having a first target location terminating between the first and second outside surfaces.

28 (NEW) The stacked module of claim 27, wherein the plurality of modules further includes a second module and a third module, the second module including a second module surface that

includes the first outside surface and the third module including a third module surface that includes the second outside surface.

29. (NEW) The stacked module of claim 15, further including a second ladder like routing path; and wherein:

the plurality of modules includes a first module and a second module, the first and second modules respectively including a first target location and a second target location, the second target location located within the stacked module; and

the ladder like routing path for routing one of the active port to the first target location, and the second ladder like routing path for routing another one of the active port to the second target location.

30. (NEW) The stacked module of claim 29, further including a second ladder like routing path; and wherein:

the stacked module includes a first outside surface and a second outside surface, the first and second outside surfaces disposed to face opposite each other;

the ladder like routing path terminates at the first target location; and

the second ladder like routing path terminates at the second target location, the second target terminating within the stacked module and located between the first and second outside surfaces;

31. (NEW) The stacked module of claim 29, wherein the second target location is located between the first and second outside surfaces.

Amendment(s) to the Drawings

The following proposed amendments to the Drawings are provided in the form of replacement drawing sheets, which are each labeled "Replacement Sheet" in their respective page headers pursuant to 37 CFR 1.84(c). No new matter has been added.

Please amend FIGS. 1 through 21b to include sight lines and larger figure label font sizes to their respective drawing sheets.

In addition, please further amend the specific figures as described below:

In FIG. 1a, please change the orientation of the figure from portrait to landscape. In addition, please reduce the length of Bus 104 and height of Main Controller-Processor 101 so that the entire figure fits within the sight lines of the drawing sheet;

In FIG. 1b, please change the orientation of the figure from portrait to landscape;

In FIGS. 2a and 2b please change the position of these figures so that they are within the sight lines of the drawing sheet;

In FIGS. 3a and 3b, please change the position of these figures so that they are within the sight lines of the drawing sheet;

In FIGS. 4a and 4b, please change the position of these figures so that they are with the sight lines of the drawing sheet;

In FIGS. 5a and 5b, please change the position of these figures so that they are with the sight lines of the drawing sheet;

In FIGS. 6a and 6b, please change the position of these figures so that they are with the sight lines of the drawing sheet;

In FIG. 7b, please change the position of the figure so that it is with the sight lines of the drawing sheet;

In FIG. 11, please change the position of element numbers so that they fit within the sight lines of the drawing sheet;

In FIG. 12a, please reduce the size of the figure, while maintaining its original aspect ration, so that the figure fits within the sight lines of the drawing sheet;

In FIG. 12b, please change the position of the figure so that it is with the sight lines of the drawing sheet;

In FIG. 13, please change the position of the figure so that it is with the sight lines of the drawing sheet;

In FIG. 14, please change the position of the figure so that it is with the sight lines of the drawing sheet;

In FIG. 15a, please change the position of the figure so that it is with the sight lines of the drawing sheet;

In FIG. 15b, please amend the figure so that if fits within the sight lines of the drawing sheet by splitting the figure into two portions and adding projection lines to illustrate their connection details;

In FIG. 16, please change the position of the figure so that it is with the sight lines of the

drawing sheet;

In FIG. 17a, please change the position of the figure so that it is with the sight lines of the drawing sheet;

In FIG. 17b, please amend the figure so that if fits within the sight lines of the drawing sheet by splitting the figure into two portions and adding projection lines to illustrate their connection details;

In FIG. 18, please change the position of the figure so that it is with the sight lines of the drawing sheet;

In FIG. 19, please amend the figure so that it is with the sight lines of the drawing sheet by moving the element numbers towards the center of the figure and changing the element text that begins with "SDRAM Module" so that are converted for one to two lines of text;

In FIG. 20b, please change the orientation of the figure from portrait to landscape;

In FIG. 21a, please change the orientation of the figure from portrait to landscape;

In FIG. 21b, please amend the figure so that if fits within the sight lines of the drawing sheet by reducing the size of the figure, while maintaining its original aspect ration, and by changing the orientation of the figure from portrait to landscape.

Remarks

The specification and drawings have been amended to correct minor errors noted in the Office Action and otherwise. These corrections are of a clerical nature and do not add "new matter".

Claims 1 and 13 have been previously cancelled without prejudice in an earlier filed Response to Restriction Requirement.

Claims 17-19 and 24-26 have been withdrawn by the Examiner.

The text of original claims 14-16 and 20-23 remain unchanged.

Claims 27 through 31 are new, do not recite new matter, or present new grounds for a new search.

Examiner's Withdrawal of Claims 17-19 and 24-26 & Examiner Interview Conducted on 9 Jan 2008

Claims 17-19 and 24-26 have been withdrawn in the Office Action. Applicants respectfully traverse the withdrawal of these claims and kindly request a new Restriction Requirement for at least two reasons. First, the Examiner in the Restriction Requirement, having mail date of 3 June 2008, considered these claims to fall within Invention II which were specifically elected by the Applicants in the Applicants Election provided on 27 June 2008. Thus, the withdrawal of claims 17-19 and 24-26 in the Office Action is improper because the Applicants did not withdraw these claims but instead specifically elected these claims in accordance with the examination restrictions defined in the Restriction Requirement. Second, the withdrawal of claims 17-19 and 24-26 in the Office Action directly contradicts the Restriction Requirement statement

that "Claims 14-26" are "drawn to a stacked module for carrying one or more active signal, classified in class 257, subclass 686." (See page 2, Restriction Requirement dated 3 June 2008). Consequently, the Applicants with respect assert that the withdrawal of claims 17-19 and 24-26 is improper.

The undersigned extends much thanks to the Examiner for agreeing to an Examiner's interview on 9 January 2009, which was conducted by telephone. The undersigned and the Examiner discussed the withdrawal of claims 17-19 and 24-26 and issues related to these claims and the Restriction Requirement. The undersigned communicated that it is believed that this withdrawal is unwarranted and unsupported (by the Patent Rules and MPEP). The undersigned also communicated that the Restriction Requirement and Election were incorrect as originally presented, and that the proper action should not include withdrawal of these claims but should instead permit the Applicants to amend the claims so that they conform to the Examiner's original restriction requirement. The undersigned believes that such an approach is warranted and does not represent a shift in the elected invention (see MPEP 821.03) because claims 17-19 and 24-26 are directed to a stacked module, which is an apparatus, whereas the unelected invention is drawn to a method. The dependency to claim 1 is merely an inadvertent typographical error (missing numeral "4" after the numeral "1") since the preamble in each of claims 17-19 and 24-26 clearly states that it depends on a "stacked module" rather than the method recited in claim 1.

In addition, Applicants Election did not traverse the Restriction because the Restriction Requirement stated that claims 14-26 are readable on the same invention ("stacked module"). Consequently, Applicants believe that MPEP 821.02 does not apply here since, had the Restriction Requirement originally stated that claims 17-19 and 24-26 did not read on a stacked module, Applicants would have made an election *with* traverse or at least made an election with an

amendment to claims 17-19 and 24-26 that renders the text of the claims consistent with their preamble and that corrects their dependency from claim 1 to claim 14 had the Restriction Requirement asserted that claims 17-19 and 24-26 did not read on the same invention ("stacked module") as the remaining pending claims 14-16 and 20-23.

Consequently, for the reasons stated above, Applicants kindly request that the withdrawal of claims 17-19 and 24-26 be withdrawn, and a new Restriction Requirement issued.

The Section 102(a) Rejection

Claims 14-15 and 18-23 are rejected as allegedly being anticipated by Kyougoku (USP 5,995,379). This rejection is respectfully traversed.

Independent Claim 14

In the Office Action it is asserted that with respect to claim 14, "Kyougoku shows a stacked module (Fig. 5) comprising a modules (100-1002) each comprising: one or more active port (B1-B3) for carrying one or more active signal (col. 6, lines 45-50); and one or more passive port (L1-L6) for passing through the one or more active signals (col. 6, lines 45-50)." Applicants respectfully disagree. The alleged active signals, such as chip select signals B1 and B2 (Kyougoku at col. 6, lines 45-50), begin from an outside surface of the ***stacked*** module but terminate on the other side (or outside opposite surface) of the stack module. See also, Kyougoku, D1,' D2' and D3' in FIG. 5 (FIG. 5 is a partial section view). See also, col. 3, line 65 to col. 4, line 15. The claimed invention, however, enables a controller module active pad(s) to be routed to a desired specific module ***within*** the stacked module. Consequently, Kyougoku fails to teach or suggest each element of the invention recited in claim 14, rendering claim 14 allowable.

Dependent Claims 15 and 16

In the Office Action it is also asserted that with respect to claim 15, "Kyougoku shows the one or more passive port forms a ladder like routing path (L1-L6)." Applicants respectfully traverse this rejection.

Claim 15 depends on allowable base claim 14, and thus claim 15 is also allowable for the same reasons.

In the Office Action it is also asserted that with respect to claim 16, "Kyougoku shows the plurality of module 1000-1002 is rotated before being stacked and the one or more passive port L1-L6 forms a rotational routing path (Fig. 5)." Applicants respectfully traverse this rejection.

Claim 16 depends on allowable base claim 14, and thus claim 16 is also allowable for the same reasons.

In addition, with respect to claims 15 and 16, the Office Action uses L1-L6 in Kyougoku to assert that Kyougoku discloses a "ladder like routing path" but also uses the same structure (L1-L6) to assert that Kyougoku also discloses a "rotational routing path". This interpretation of L1-L6 is inherently contradictory because a ladder like routing path cannot be a rotational routing path and vice versa although a ladder like routing path may be used with a rotational routing path and vice versa. See, Applicants' Drawings in FIG. 19, showing an embodiment of a "ladder like routing path"; and FIGS. 20a-20b, showing an embodiment of a "rotational routing path".

Dependent Claim 18

The Office Action rejects claim 18 by alleging that "Kyougoku shows one or more control port (1000) for enabling a routing path (L4) extending the first daisy chain connection 5 with an

end module 1002 (Fig. 5)." This rejection is respectfully traversed.

Element number 1000 in Kyougoku, Fig. 5, represents a semiconductor ***substrate*** rather than a "control port". Kyougoku at col. 7, lines 27-29. Consequently, Kyougoku fails to disclose or suggest control port, rendering this rejection improper and claim 18 allowable.

Dependent Claims 20-21

The Office Action rejects claims 20 and 21 by asserting that that "Kyougoku shows one or more of the plurality of modules is a main board (Col. 6, lines 55-57) and one more vertically stacked modules 1000-1002 in (Fig. 5) is connected to the main board (Col. 6, lines 55-57). This rejection is respectfully traversed.

Claims 20 and 21 depend on allowable base claim 14, and thus claims 20 and 21 are also allowable for the same reasons stated above for claim 14.

Dependent Claim 22

The Office Action rejects claim 22 by alleging that "Kyougoku shows each of the plurality of modules (1000-1002) comprises a first side (B1-B3 area) and a second side (B1'-B3' area) (Fig. 5) wherein the wherein the one or more active port (B3) is connected to one or more active ball 5 on the first side of one or more corresponding module 1000; wherein the one or more passive port L1 is connected to one or more passive ball (not labeled, ball connected to B2) on the first side and one or more passive pad B1' on the second side of one or more corresponding module 1000; wherein each of the one or more passive ball (no labeled, ball connected to B2) and each of the one or more passive pad B1' connected to a same passive port are located between a pre-determined distance to each other in a repeating pattern, the pre-determined distance equaling a multiple of a periodic distance of the repeating pattern (Fig. 5); wherein one or more active port of

a base module is routed to a same location on one or more modules 1001-1002 through the ladder like routing path L1-L6; and wherein the ladder like routing path comprises one or more passive ball and one or more passive pad (Fig. 5)." This rejection is respectfully traversed.

Claim 22 ultimately depends on allowable claim 14, and thus is allowable for the same reasons stated for claims 14 and any intervening dependent claims.

In addition, at least one of the elements recited in claim 22 is not taught or disclosed in Kyougoku. In the Office Action it is asserted that Kyougoku teaches or discloses that "the one ore more passive port L1 is connected to one or more passive ball (not labeled, ***ball connected to B2***)." (Emphasis added). The "ball connected to B2", however, is not a passive ball because B2 is disposed to receive a chip select signal. See, Kyougoku at col. 7, lines 29-30 ("chip select electrode pads B1 to B3…are formed on the surfaces of the substrates…") and Fig. 5.

Consequently, for the reasons stated above, Kyougoku fails to teach or disclose each and every element recited in claim 22, rendering claim 22 allowable.

Dependent Claim 23

The Office Action rejects claim 23 by alleging that "Kyougoku shows each of the plurality of modules (1000-1002) comprises a first side (B1-B3 area) and a second side (B1`-B3' area) wherein the one or more active port (B3) is connected to one or more active ball 5 on the first side of one or more corresponding module 1000; wherein the one or more passive port L1-L6 is connected to one or more passive ball (not labeled, ball connected to B2) on the first side and one or more passive pad B1' on the second side of one or more corresponding module 1000; wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port L1 are located opposite each other in a repeating pattern (L1-L6); wherein one or

more active port of a base module 1000 is routed to a same location on one or more modules 1001-1002 through the rotational routing path (L1-L6); and wherein the ladder like routing path comprises one or more passive ball and one or more passive pad (Fig. 5)." This rejection is respectfully traversed.

Claim 23 ultimately depends on allowable claims 14, and thus is allowable for the same reasons stated for claims 14 and any intervening dependent claims, including claim 16.

In addition, at least one of the elements recited in claim 23 is not taught or disclosed in Kyougoku. In the Office Action it is asserted that Kyougoku teaches or discloses that "the one ore more passive port L1-L6 is connected to one or more passive ball (not labeled, ***ball connected to B2***)." (Emphasis added). The "ball connected to B2", however, is not a passive ball because B2 is disposed to receive a chip select signal. See, Kyougoku at col. 7, lines 29-30 ("chip select electrode pads B1 to B3…are formed on the surfaces of the substrates…") and Fig. 5.

Further still and solely for the sake of argument, even if the Office Action is correct in asserting that the "ball connected to B2" is a passive ball, claim 23 recites "…wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located opposite each other in repeating pattern…" Kyougoku fails to teach this recited element because, unlike in claim 23, the passive balls and passive pads that are connected to a passive port are ***not*** "located opposite each other in a repeating pattern". Cf. Kyougoku at FIG. 5 (unlabeled ball connected to B2, which is asserted to be a passive ball in the Office Action, is coupled to pad B1' via L1 but the unlabeled ball connected to B2 is not located opposite to pad B1' but is offset from B1').

Consequently, for at least one or the reasons stated above, Kyougoku fails to teach or

disclose each and every element recited in claim 23, rendering claim 23 allowable.

The First Section 103(a) Rejection

The Examiner rejects claim 16 by asserting this claim is allegedly unpatentable over Kyougoku. This rejection is respectfully traversed.

In the Office Action, it is asserted that with respect to claim 16, "Kyougoku shows the plurality of module 1000-1002 is rotated before being stacked and the one or more passive port L1-L6 forms a rotational routing path (Fig. 5). With respect, Applicants disagree.

A proper section 103 rejection, among other things, requires some suggestion or motivation in Kyougoku in Fig. 5 that would render the claimed invention obvious to one of ordinary skill in the art. Fig. 5 is a sectional view (Kyougoku at col. 7, lines 20-21), and thus, would not render the claimed invention obvious. Indeed, Kyougoku teaches away from a rotational routing path as recited in claim 16 because Kyougoku emphasizes that for ***each*** substrate, "the first chip select electrode is positioned at the endmost of N-number of chip select electrodes". Kyougoku at col. 3, line 56 through col. 4, line 30, Figs 1through Fig. 3, and Fig. 6. Positioning the first chip select electrode in the manner taught in Kyougoku precludes rotating one substrate relative to another substrate before stacking because each substrate is also disposed to have the same wiring structure (Id. at col. 3, lines 34-35), and all respective chip select electrodes from each substrate are aligned with each other when the substrates are stacked without rotation. (Id. at col. 3, lines 43-51 and elements B1/11 and C1/41 in Figs. 1 and 6), which would result in a misalignment of the respective first chip select electrodes (such as B1/11 and C1/41 of the substrates 1 and 2, respectively) should these substrates be rotated before stacking. Consequently, Kyougoku would not provide any teaching or suggestion that would render claim 16 obvious to

one or ordinary skill in the art because Kyougoku not only teaches away from the claimed invention but also its teachings would render the claimed invention inoperable.

In addition, claim 16 depends on allowable independent claim 14. Claim 14 is allowable because Kyougoku fails to teach or suggest each and every element recited in claim 1. For example, the alleged active signals, such as chip select signals B1 and B2 (Kyougoku at col. 6, lines 45-50), begin from an outside surface of the ***stacked*** module but are taught by Kyougoku to terminate on the other side (or outside opposite surface) of the stack module. See also, Kyougoku, D1,' D2' and D3' in FIG. 5 (FIG. 5 is a partial section view). See also, *Id. at* col. 3, line 65 to col. 4 line 15. The claimed invention, however, enables a controller module active pad(s) to be routed to a desired specific module ***within*** the stacked module. Consequently, Kyougoku fails to teach or suggest each element of the invention recited in claim 14, rendering claim 14 allowable. Since claim 14 is allowable, claim 16 is also allowable.

New Claims 27-31

Claims 27 through 31 are new but do not present new grounds for rejection, or add new matter.

Petition for Extension of Time and Payment of New Claim Fees

A Petition for an Extension of Time and Payment of New Claim Fees, if any, are submitted in a separate paper, respectively, and filed concurrently herewith.

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Request for Allowance

It is believed that this Amendment places this Application into condition for allowance.

Early favorable consideration of this Amendment is earnestly solicited.

Respectfully submitted,

Dated: 13 Feb 2009

/Stephen R. Uriarte/
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Application

For

United States Non-Provisional Utility Patent

Title:

Multiple Chip Module and Package Stacking Method For Storage Devices

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Multiple Chip Module and Package Stacking Method For Storage Devices

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BACKGROUND

Field

The present invention relates to computer systems. More particularly, the present invention relates to flash memory based semiconductor disk drives [[drive]] and a method of using multiple chip module (MCM) and Package Stacking technique to support miniaturization and memory scalability.

Description of Related Art

A flash [[Flash]] memory based semiconductor disk drive typically use separate packages for the interface controller, the DMA controller, the processor and separate packages for the Flash devices, the FPROMs and the RAMs. This current method limits the miniaturization of the entire storage device. In order to achieve the move to miniaturization, chip modules and packages need to be stacked. Stacking both on chip module and package level maximizes the capacity in a limited area thus realizing the move to miniaturize the entire storage device. A technique in stacking chip modules and

packages strategically to support miniaturization and memory scalability in both vertical and horizontal orientation is therefore proposed.

SUMMARY OF THE INVENTION

In the stacking technique illustrated in example embodiments of the present invention, semiconductor dies are mounted in a module to become a MCM which serves as the basic building block. ¸Combination of these modules and dies in a substrate creates a package with specific function or a range of memory capacity. ¸These packages are stacked to increase capacity or add functions. ¸A combination of different existing technology such as flip chip, wire bond, MCM, module stacking, advance packaging, etc. are used to accomplish highly reliable module to module and package to package interconnection and scalability. ¸A single package can have a wide range of capacity depending on the memory capacity of the die used and the number of modules stacked within the package. In the proposed package stacking technique, the stacked modules in a package serve as the building blocks for the package level stacking. ¸Multiple packages are stacked to create the desired memory capacity and different packages are stacked to create desired function. Expansion can be done both on the vertical and horizontal orientations. ¸The technique is in the assignment of pins. Small capacity miniature storage devices can use the vertical expansion, while high capacity devices with larger form factors can use both vertical and horizontal expansion to maximize capacity. ¸By using this technique, large capacity storage devices are implemented in a small package device, and larger form factors achieve bigger memory capacities.

The present invention takes advantage of the existing stacking technology both on the module and package level. This maximizes the capacity in a small area, realizing the miniaturization transition. Modular approach is used in creating basic building blocks which can be tested individually and replaced easily prior to final packaging, making the technique reliable, and cost effective ~~effectively~~. A wide [[Wide]] range of capacity can be configured through variation of die capacities and stacking modules and/or packages. Expanding capacity may be implemented vertically, horizontally or both, depending on board area and desired capacity. ~~Expansions are implemented both vertically and horizontally depending on board area and desired capacity.~~

[[

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BRIEF DESCRIPTION OF DRAWINGS

So that the manner in which the above recited features, advantages and objects of the present invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the present invention may admit to other equally effective embodiments.

Figure 1a shows the block diagram of the stackable system for high performance, high capacity devices according to an example embodiment of the present invention.
Figure 1b shows the block diagram of the stackable system for lower performance, lower capacity devices according to an example embodiment of the present invention.

Figure 2a, 2b, 2c depict the SDRAM module's top and bottom drawings and a cross sectional representation of stacked multiple SDRAM modules according to an example embodiment of the present invention.

Figure 3a, 3b, 3c depict the flash module's top and bottom drawings and a cross sectional representation of stacked multiple flash modules according to an example embodiment of the present invention.

Figure 4a, 4b depict the first high-end controller module's top and bottom drawings according to an example embodiment of the present invention.

Figure 5a, 5b depict the memory module's top and bottom drawings according to an example embodiment of the present invention.

Figure 6a, 6b depict the first low-end controller module's top and bottom drawings according to an example embodiment of the present invention.

Figure 7a, 7b depict the second high-end controller module's top and bottom drawings according to an example embodiment of the present invention.

Figure 8a, 8b depict the second low-end controller module's top and bottom drawings according to an example embodiment of the present invention.

Figure 9 depicts the stacked SDRAM modules further stacked on the controller module according to an example embodiment of the present invention. This configuration is used for high end applications. The figure also shows how the balls have corresponding pads for inter-module connection.

Figure 10 depicts stacked flash modules further stacked on the memory module according to an example embodiment of the present invention. The figure also shows how the balls have corresponding pads for inter-module connection.

Figure 11 depicts the possible stacking options for the first high-end controller module and the memory modules according to an example embodiment of the present invention. A substrate interface is used to attach one group of stacked modules to another.

Figure 12a is an isometric exploded drawing of the stacking technique presented in Figure 11 according to an example embodiment of the present invention. ¸Multiple identical stacking is not included in this drawing.

Figure 12b is another package stacking technique using Pin Grid Array (PGA) rather than Ball Grid Array (BGA) according to an example embodiment of the present invention. ¸This is used for easy replacement and expansion.

Figure 13 depicts the low-end controller module configuration with stacked flash module according to an example embodiment of the present invention. ¸The figure also shows how the balls have corresponding pads for inter-module connection.

Figure 14 is an isometric exploded version of the stacking technique presented in Figure 11 according to an example embodiment of the present invention.

Figure 15a, 15b depict the second high-end controller module configuration with stacked memory modules according to an example embodiment of the present invention. ¸The figures also show how the balls have corresponding pads for inter-module connection.

Figure 16 is an isometric exploded version of the stacking technique presented in Figure 14 according to an example embodiment of the present invention.

Figure 17a, 17b depict the second low-end controller module configuration with stacked memory modules according to an example embodiment of the present invention. The figures also show how the balls have corresponding pads for inter-module connection.

Figure 18 is an isometric exploded version of the stacking technique presented in Figure 17 according to an example embodiment of the present invention.

Figure 19 shows a pin assignment and connection technique to be able to select specific layer in a multi-stacked module according to an example embodiment of the present invention.

Figure 20a shows another pin assignment technique which uses a rotational stacking orientation to allow stacking of four identical modules representing different bus interfaces according to an example embodiment of the present invention.

Figure 20b shows a cross-section representation of the four stacked modules on a rotational stacking technique and how their pins mates according to an example embodiment of the present invention.

Figure 21a shows another pin assignment and connection technique to be able to connect a serial chain route from multiple modules in a stack according to an example embodiment of the present invention.

Figure 21b shows the routing of [[how]] a serial chain connection ~~is routed~~ from one stack location to another allowing application of both vertical and horizontal expansion independently or simultaneously according to an example embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1a is a block diagram of a flash storage system according to a first example embodiment of the present invention. The block diagram shows the entire high-end system that is modularized, stacked, and packaged to achieve the desired features of the technique. The heart of the system is the main controller-processor **101** which interfaces with the flash memory, the flash PROM and the SDRAM memory blocks. The SDRAM is configured from a single bank **102** to a maximum of four banks depending on the desired capacity. Each bank such as **102** includes 3 SDRAMs. The flash devices such as **107** are controlled by the Flash Interface Controller such as **105**. Each controller supports four flash buses such as flash bus A11 **106**, and each flash bus supports a maximum of 8 flash devices. The main controller-processor supports four flash interface controllers through 4 different busses such as B bus **104**. The four flash interface controllers with their corresponding flash devices comprise the memory set **108**. The main controller-processor can support from one memory set to a maximum of 15 memory sets. This is a maximum support of 1,920 flash devices.

Figure 1b is a block diagram of a flash storage system according to a second example embodiment of the present invention. The block diagram shows the entire low-end system that is modularized, stacked, and packaged to achieve the desired features of the technique. Since a low-end system may [[does]] not require a large amount [[lot]] of memory capacity, SDRAM may [[can]] be limited to one bank **109**, or none at all, and the supported flash devices may [[is]] also be limited ~~minimal~~ to only two sets of flash buses. One set of flash buses **110** consists of four flash bus with 8 flash devices supported per flash bus, which results in [[. This is]] a maximum supported number of 64 flash devices.

From the basic dies; SDRAM, FPROM, flash memory, flash interface controller, and the main controller-processor, single and multiple chip modules are created to become the basic building blocks for the stacking technique presented in the present invention. Referring to figure 2a which is a top view of an SDRAM module, three SDRAM dies **201** are placed in a single substrate **203** to become the SDRAM module which is one of the basic building blocks. The SDRAM module is represented in figure 1 as a single bank **102** composed of SDRAM 00, SDRAM 01, and SDRAM 02 connected to the SDRAM interface **103**. All signals needed to interface to the controller module and other SDRAM modules are assigned in both the bottom balls **204** and top pads **202** respectively. Bottom balls **204** are shown in figure 2b which is a bottom view of the SDRAM module, three slots **205** are created under the SDRAM die's pad attach area to accommodate bottom wire bonding. Figure 2c is the stacked module cross sectional

representation. Top pads **202** and bottom balls **204** act as the vertical interconnects between all SDRAM modules and to the controller module. Varying the SDRAM die capacity and the stack quantity result in wide range of total SDRAM capacity depending on the product application. The SDRAM device organization, capacity and bank limitations are defined by the main controller-processor's SDRAM interface specifications. The main controller-processor intended to be used for this example embodiment of the present invention supports a 32-bit wide 4 banks maximum [[max]] SDRAM configuration.

Figure 3a is a top view[[,]] that shows four flash dies **301** in a single substrate **303** that collectively form part of a ~~becoming the~~ flash module, which can [[is]] also function as a basic building block. All signals needed to interface with the memory module and other flash modules are assigned in both the bottom balls **304** and the top pads **302**, respectively, as shown in FIGS. 3a, 3b and 3c. In figure 3c, the flash modules are stacked. Maximum stack quantity depends on the flash interface controller specifications. Top pads **302** and bottom balls **304** acts as the vertical interconnects between stacked flash modules and to the memory module. Varying the flash die capacity and the stacking quantity, results in a wide range of total flash capacity depending on the product application and capacity requirements. The flash device organization and capacity limitations are defined by the flash interface controller's specifications. The flash interface controller intended to be used for this used for this example embodiment of the present invention supports 8 flash devices per flash bus, thus allowing a maximum stacking of 8 flash modules.

Figure 4a shows the top view of the first example embodiment of the present invention illustrated in a first high-end controller module configuration. A single FPROM die **401** is placed at the center of the substrate **404**. Pads are composed of two sections, one for the SDRAM module interface shown as **402** and another for the memory module interface shown as **403**. This technique enables multiple stacking of both SDRAM modules and memory modules in a single package. Figure 4b shows the bottom view of the controller module. A single main controller-processor die **406** is placed at the center of the substrate. The controller module becomes a base module for the package. The [[balls**405**]]balls **405** are used to connect to the main substrate which is typically a printed circuit board (PCB).

Figure 5a shows the top view of the memory module which is also a basic building block. A single flash interface controller die **501** is placed on the center of the substrate **504**. Pads are composed of two sections, one for the flash module interface shown as **502** and another for the other memory module interface shown as **503**. This technique enables multiple stacking of flash modules and memory modules in a single package. The memory module becomes a base module for the package. Figure 5b shows the bottom view of the memory module. The memory module balls **505** are used to connect to the main substrate PCB, to the controller modules or to the other memory modules depending on the type of configuration desired.

Figure 6a shows the top view of the second example embodiment of the present invention illustrated in a first low-end controller module configuration. Two SDRAMs

601 and a single FPROM **602** are placed on top of the module. ¸This configuration is flexible. The SDRAMs can be unpopulated in a low performance application. ¸Internal SRAMs in the main controller-processor will take over the SDRAM functions. ¸The main controller-processor **605** is placed at the bottom of the module. This configuration does not allow stacking of the SDRAM which is not necessary for low capacity applications. Flash modules are stacked on top, [[top]] interfacing to the pads **603.** ¸The substrate **604** is the same size as the flash module making its final package smaller. The bottom balls **606** are used to interface with the main PCB.

Figure 7a shows the top view of the first example embodiment of the present invention illustrated in a second high-end controller module configuration, where four memory modules **701** can be mounted on separate locations adjacent to each other. Memory module interface pads **704** are allocated for multiple stack configurations. In the middle of the memory module interface pads, 3 SDRAM dies **702** are mounted. Each area corresponds to one SDRAM bank **703,** totaling to a maximum of 4 SDRAM banks in the package. The bottom view is presented in Figure 7b, where the main controller-processor die **705** and the FPROM die **706** are mounted adjacent to each other. The module's balls **707** are used for external interface to the main PCB.

Figure 8a shows the top view of the second example embodiment of the present invention illustrated in a second low-end controller module configuration, where only two memory modules **801** can be mounted side-by-side. Memory module interface pads **802** are allocated for multiple stacking configurations. In the middle of the memory

module interface pads, 3 SDRAM dies **803** are mounted. Each area corresponds to one SDRAM bank **804**, totaling to only a maximum of 2 SDRAM banks in a package. The SDRAM can either be mounted or not depending on the application. Internal SRAMs can also be used instead of the SDRAMs. The stacked memory modules can also be configured to support both internal and external flash interface controller applications. The bottom view is presented in Figure 8b, where the main controller-processor die **805** and the FPROM die **806** are mounted adjacent to each other. The module balls **807** are used for external interface to the main PCB.

Figure 9 shows the stacking of SDRAM module **901** and controller module **902**. A single or stacked SDRAM module can be placed on top of a controller module. The pads for the SDRAM module interface **903** must align with the SDRAM module balls **904**. The bottom-most SDRAM module **905** serves as bank 0, and the top-most module **906** serves as bank 3[[,]]. For low capacity SDRAM requirements, only a single or dual bank is enough. High capacity devices needs to have a maximum SDRAM capacity, thus stacking the maximum of 4 modules. The outer pads **907** are for the memory module interface.

Figure 10 shows the stacking of flash modules **1001** and memory module **1002**. A four-stack or eight-stack flash module is placed on top of a memory module. The pads for the flash module interface **1003** must align with the flash module balls **1004**. The outer pads **1005** are for other memory module interface. The flash interface controller intended to be used for this example embodiment of the present invention supports a maximum of

4 flash buses and each flash bus supports a maximum of 8 flash devices. The bottom-most flash module **1006** contains the 4 flash buses' Flash 00 devices and the top-most module **1007** contains the 4 flash buses' Flash 07 devices.

Figure 11 shows a sample of a maximized stacking technique that can be configured through vertical, horizontal or combined expansion. Multiple staking will increase the overall height of the module, thus requiring a filler **1101** to physically interconnect two stacked modules. A thinner filler **1102** may be used depending on the height differential between the modules which is dependent to the number of stacks applied. A controller module with the stacked SDRAM modules act as the controller package **1103**. A memory module with stacked flash modules acts as the memory package **1104**. Four memory packages stacked together form the memory set **1105**. Vertical expansion happens when the controller package is stacked with a single or multiple memory sets. The figure shows a single memory set to be stacked to the controller package. Horizontal expansion happens when the controller package is located on a different site on the PCB relative to the memory sets. Also multiple memory sets can be located on different sites on a PCB. Combo expansion happens when both vertical and horizontal expansion technique is implemented simultaneously. The expansion technique is very flexible depending on the desired memory capacity, main PCB size limitations and also height limitations.

Figure 12a shows the isometric and exploded drawing of the stacking technique for the first high-end controller configuration. Pins are assigned strategically and modules are stacked to make possible the miniaturization of the entire system in a package.

1201 – The Flash Module

1202 – The Flash Die

1203 – The Flash Module Pad Interface to other Flash Modules

1204 – The Flash Module Solder Balls

1205 – The Memory Module

1206 – The Flash Interface Controller Die

1207 – The Memory Module Pad Interface for the Flash Module

1208 – The Memory Module Pad Interface for the other Memory Modules

1209 – The Memory Module Solder Balls

1210 – The SDRAM Module

1211 – The SDRAM Die

1212 – The SDRAM Module Pad Interface to other SDRAM Modules

1213 – The SDRAM Module Solder Balls

1214 – The Controller Module

1215 – The FPROM Die on top side and the Main Controller-Processor Die at the bottom side.

1216 – The Controller Module Pad Interface to the SDRAM Modules

1217 – The Controller Module Pad Interface to the Memory Modules

1218 – The Controller Module Solder Balls

Figure 12b is another technique used in this invention to ease replacement and facilitate expansion. Instead of using Ball Grid Array (BGA), Pin Grid Array (PGA) **1219** is used. This method makes it more flexible due to the technology's inherent feature where replacement is done swiftly without any assembly process involved. Horizontal expansion is also benefited in this technology. The figure shows the stacked memory module as an example. The memory module is packaged using the PGA technology, where the top portion of the package becomes the socket **1220** and the bottom portion the pin arrays **1219**. The filler **1221** becomes the package's top socket and is interfaced into the base module **1222** through the BGA **1223**. The base module uses PGA to interface to the bottom package or to the main board **1224**. Filler **1225** is also mounted into the main board to interface the stacked memory modules.

Figure 13 shows the stacking of the flash module **1301** and the first low-end type of controller module **1302**. A single or stacked flash module can be placed on top of the controller module. The pads for the flash module interface **1303** must align with the flash module balls **1304**. This configuration is for low capacity low performance applications. The number of flash modules to be stacked depends on the desired capacity and is limited to the supported feature of the main controller-processor. The main controller-processor's flash interface can support a maximum of 8 buses and a maximum of 8 flash devices per bus.

Figure 14 shows the isometric and exploded drawing of the stacking technique for the first low-end controller configuration. Pins are assigned strategically and modules are stacked to make possible the miniaturization of the entire system in a package.

1401 – The Flash Module

1402 – The Flash Die

1403 – The Flash Module Pad Interface to other Flash Modules

1404 – The Flash Module Solder Balls

1405 – The Controller Module

1406 – The FPROM Die and the Main Controller-Processor Die at the bottom

1407 – The SDRAM Die

1408 – The Controller Module Pad Interface to the Flash Modules

1409 – The Controller Module Solder Balls

Figure 15a shows the stacking technique for the second high-end controller configuration. The stacked flash modules **1501** are further stacked on top of the memory modules **1502** which are then mounted on the controller module **1503** on four different locations. Four memory modules can be mounted on four different locations on the controller module creating a memory set. Stacking more memory sets increases the total capacity. The cross-sectional representation of the said stacking technique is shown in Figure 15b. The memory module balls **1504** must align to the pad interface **1505** on the controller module. As previously discussed in figure 11, fillers are used to physically connect two successively stacked modules. The controller balls **1506** will become the external interface to the main board. The final package is 4X bigger than the first high end option.

Figure 16 shows the isometric and exploded drawing of the stacking technique discussed in Figure 15. Pins are assigned strategically and modules stacked to make possible the maximum stacking and interconnection between modules. As previously discussed in figure 11, fillers are used to physically connect two stacked successively stacked modules.

1601 – The Flash Module

1602 – The Flash Dies

1603 – The Flash Module Pads Interface to other Flash Modules

1604 – The Flash Module Solder Balls

1605 – The Memory Module

1606 – The Flash Interface Controller Dies

1607 – The Memory Module Pad Interface to Flash Modules

1608 – The Memory Module Pad Interface to other Memory Modules

1609 – The Memory Module Solder Balls

1610 – The Controller Module

1611 – The SDRAM Dies on top side and the FPROM and Main Controller-Processor at the bottom side

1612 – The Controller Module Pads Interface to the Memory Modules

1613 – The Controller Module Solder Balls

Figure 17a shows the stacking technique for the second low-end configuration. The stacked flash modules **1701** are further stacked on top of the memory modules **1702** which are then mounted on the controller module **1703** on two different locations. This

technique can use both internal and external flash interface controller configurations, making this technique flexible. The cross-sectional view is shown in figure 17b. The memory module balls **1704** must align to the pad interface **1705** on the controller module. The controller balls **1706** will become the external interface to the main board. The final package is twice the size of the first high end option.

Figure 18 shows the isometric and exploded drawing of the stacking technique discussed in Figure 17. Pins are assigned strategically and modules stacked to make possible the maximum stacking and interconnection between modules. As previously discussed in figure 11, fillers are used to physically connect two stacked successively stacked modules.

1801 – The Flash Module

1802 – The Flash Dies

1803 – The Flash Module Pads Interface to other Flash Modules

1804 – The Flash Module Solder Balls

1805 – The Memory Module

1806 – The Flash Interface Controller Dies

1807 – The Memory Module Pad Interface to Flash Modules

1808 – The Memory Module Pad Interface to other Memory Modules

1809 – The Memory Module Solder Balls

1810 – The Controller Module

1811 – The SDRAM Dies on top side and the FPROM and Main Controller-Processor at the bottom side

1812 – The Controller Module Pads Interface to the Memory Modules

1813 – The Controller Module Solder Balls

A more detailed technique on how the pins are assigned and how modules are placed with different orientation in the stack is discussed in the following paragraphs.

Figure 19 shows a first pin assignment and connection technique that enables a selection of specific module in a multiple module stack. The figure illustrates the controller and SDRAM modules as an example. The SDRAM module[['s]] balls, such as **1907**, are represented by big oblong shapes, and the pads such as **1908** are represented by smaller oblong shapes. A pad[[Pad]] to ball connection is represented by a rectangle, such as **1906**. The controller module has four active pads such as **1904,** one each for the four SDRAM modules such as **1901**. The controller module's active pad 00 **1904** is connected to SDRAM module 0's X0 ball **1903**, pad 01 to SDRAM module 1's X0 ball **1902**, and so on. The X0 balls are the active balls[[ball]] for the SDRAM modules. All SDRAM modules are identical which include the connections as follows: X1 ball is connected to X1 pad, X2 ball to X2 pad, and so on. The technique involves using a ladder-like routing path, ~~a ladder like routing~~ such as **1905** on the stacked modules. This technique enables the controller module's active pad to be routed to the desired specific module in the stack. The example embodiment illustrated in figure 19 comprises a repeating pattern for the balls and pads. Passive balls are connected within each module to passive pads with an offset distance equaling one periodic distance of the repeating pattern. The importance is the approach using repeating pattern and offsetting

of the passive ball to passive pad within each module, other offset distances[[distance]] can be used also in other embodiment of the present invention, e.g. using an offset of two [[2]] or any multiple of the periodic distance of the repeating pattern. The example embodiment does not limit the scope of the present invention.

Another pin assignment, connection, and stacking combo method introduced in this invention is ~~the rotational stacking technique~~ the rotational stacking technique. Figure 20a shows the pad interconnects for a certain base module and strategic numbering is assigned. Pads labeled with numbers 1 to 4 represent the four[[4]] different groups of signals. Pads labeled with the number 5 are used for the vertical stacking IOs (more details are illustrated in figure 21a). Pads labeled with the number 6 are reserved for power and ground which are common to all modules in the stack. Since the stacked modules are identical, we can use rotational stacking to connect one module to one group of signals and the following rotated stacked module connects to another group of signals, and so on. This way ensures four identical modules to be stacked and connected to four different groups of signals from the base module which is typically a controller. Pad 1 **2001,** upon the substrate being rotated 90 degrees clockwise, occupies pad 2 **2002** location relative to an un-rotated substrate such as the base substrate which is typically a controller. In a similar manner pad 1 **2001** can be located at pad 3 **2003** location, then pad 4 **2004** location upon the substrate being rotated 180 and 270 degrees clockwise respectively.

Figure 20b shows a cross-sectional view of four such modules stacked over the base module. Memory and Controller modules are used as example. Pin 1s such as **2005** on the stacked modules are the only active signal pins for the module. The rest (numbered 2 to 4) **2006** are directly connected to the balls underneath them but have[[has]] no other connections. This way connection is continued from bottom to top. The active pin **2007** of the first module **2008** is aligned to pin 1 pad **2009** on the base module, and the second module's active pin **2010** is aligned on pin 2 **2011** of the base module with second module being rotated 90 degrees clockwise. Since pin 2 **2012** on the first module is directly connected to the ball underneath, this allows the pin 1 on the second module **2013** to be connected to pin 2 **2011** of the base module. Rotating the next stacked module 90 degrees more, will align it's active pin to the base module[[s]] pin 3 and so on until the forth rotation.

The last connection technique is used for serial routing of all modules in the stack and allowing them to be externally accessible for horizontal expansion on a PCB, such as a main board. Figure 21a shows how this technique is implemented in the stacking method. The main board **2101** contains the input signals **2102** which will then be connected to IN ball **2104** of the base module **2103**. The base module's OUT pad **2105** is connected to IN ball **2107** of the first stack module **2106**, and so on. The top module **2108** terminates the signal to the top pad **2109** and routes, with connection **2112**, the signal internally to another pad **2110** which is connected directly to the ball **2113** underneath, [[.]] Since the modules are identical, this routed signal passes through the pads and balls **2111** of the stack until it reaches the OUT pad **2114** of the main board for

external access. How the top module terminates the serial chain and branches them out to other pads is shown in Figure 21b. All modules[[module]] have a selectable buffer **2115** that tri-states the input when pulled low. The signal from the IN balls **2116** enters the internal circuit **2117** and exits the circuit connecting to the OUT pad **2118**. The buffer's **2115** control line is weakly pulled up internally. The "StkLow" ball is connected internally to GND **2119**, thus pulling down the buffer control line when a module is stacked above it, and it is[[it's]] pulled up when no module is stacked directly above it. When the buffer control line is pulled high, it will let the input signal branch out **2120** to the other pads, thus creating a connection route or trace that loops~~making possible the trace to loop~~ back to the base module~~module's~~ solder balls. When a module is stacked above a module that is disposed with selectable buffer **2115** in the manner shown, the buffer control signal is pulled low, tri-stating the input signal and disallowing the branching effect. This technique allows the signal to be accessible to the external balls of the base module, thus horizontal expansion for a serial signal is achievable. The balls are then routed, with connection **2121,** to the other modules **2122** on the other locations. The same technique is used on the main board **2123**, when no package is detected on the "StkLow" pad, the buffer allows the input to connect to the designated pads on the other locations. The tri-stated buffer technique is redundant to all locations. An example is the JTAG TDI-TDO signal. The diver circuit **2125** sends out TDI signals to the pads and the closing TDO signal **2124** loops back to the driver circuit.

Combining these stacking, pin assigning and connection techniques allow interconnection between modules with both parallel and series signals to both vertical and

horizontal expansion. The technique is very flexible depending on the specific application, capacity, board size and height limit.

ABSTRACT

Stacking techniques are illustrated in example embodiments of the present invention wherein semiconductor dies are mounted in a module to become a MCM which serves as the basic building block. A combination~~Combination~~ of these modules and dies in a substrate creates a package with specific function or a range of memory capacity. Several example system configurations are provided using BGA and PGA to illustrate the stacking technique. Several pin assignment and signal routing techniques are illustrated wherein internal and external signals are routed from main board to various stacked modules. Expansion can be done both on the vertical and horizontal orientations.

Application

For

United States Non-Provisional Utility Patent

Title:

Multiple Chip Module and Package Stacking Method For Storage Devices

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Multiple Chip Module and Package Stacking Method For Storage Devices

BACKGROUND

Field

The present invention relates to computer systems. More particularly, the present invention relates to flash memory based semiconductor disk drives and a method of using multiple chip module (MCM) and Package Stacking technique to support miniaturization and memory scalability.

Description of Related Art

A flash memory based semiconductor disk drive typically use separate packages for the interface controller, the DMA controller, the processor and separate packages for the Flash devices, the FPROMs and the RAMs. This current method limits the miniaturization of the entire storage device. In order to achieve the move to miniaturization, chip modules and packages need to be stacked. Stacking both on chip module and package level maximizes the capacity in a limited area thus realizing the move to miniaturize the entire storage device. A technique in stacking chip modules and packages strategically to support miniaturization and memory scalability in both vertical and horizontal orientation is therefore proposed.

SUMMARY OF THE INVENTION

In the stacking technique illustrated in example embodiments of the present invention, semiconductor dies are mounted in a module to become a MCM which serves as the basic building block. Combination of these modules and dies in a substrate creates a package with specific function or a range of memory capacity. These packages are stacked to increase capacity or add functions. A combination of different existing technology such as flip chip, wire bond, MCM, module stacking, advance packaging, etc. are used to accomplish highly reliable module to module and package to package interconnection and scalability. A single package can have a wide range of capacity depending on the memory capacity of the die used and the number of modules stacked within the package. In the proposed package stacking technique, the stacked modules in a package serve as the building blocks for the package level stacking. Multiple packages are stacked to create the desired memory capacity and different packages are stacked to create desired function. Expansion can be done both on the vertical and horizontal orientations. The technique is in the assignment of pins. Small capacity miniature storage devices can use the vertical expansion, while high capacity devices with larger form factors can use both vertical and horizontal expansion to maximize capacity. By using this technique, large capacity storage devices are implemented in a small package device, and larger form factors achieve bigger memory capacities.

The present invention takes advantage of the existing stacking technology both on the module and package level. This maximizes the capacity in a small area, realizing the miniaturization transition. Modular approach is used in creating basic building blocks

which can be tested individually and replaced easily prior to final packaging, making the technique reliable, and cost effective. A wide range of capacity can be configured through variation of die capacities and stacking modules and/or packages. Expanding capacity may be implemented vertically, horizontally or both, depending on board area and desired capacity.

BRIEF DESCRIPTION OF DRAWINGS

So that the manner in which the above recited features, advantages and objects of the present invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the present invention may admit to other equally effective embodiments.

Figure 1a shows the block diagram of the stackable system for high performance, high capacity devices according to an example embodiment of the present invention.

Figure 1b shows the block diagram of the stackable system for lower performance, lower capacity devices according to an example embodiment of the present invention.

Figure 2a, 2b, 2c depict the SDRAM module's top and bottom drawings and a cross sectional representation of stacked multiple SDRAM modules according to an example embodiment of the present invention.

Figure 3a, 3b, 3c depict the flash module's top and bottom drawings and a cross sectional representation of stacked multiple flash modules according to an example embodiment of the present invention.

Figure 4a, 4b depict the first high-end controller module's top and bottom drawings according to an example embodiment of the present invention.

Figure 5a, 5b depict the memory module's top and bottom drawings according to an example embodiment of the present invention.

Figure 6a, 6b depict the first low-end controller module's top and bottom drawings according to an example embodiment of the present invention.

Figure 7a, 7b depict the second high-end controller module's top and bottom drawings according to an example embodiment of the present invention.

Figure 8a, 8b depict the second low-end controller module's top and bottom drawings according to an example embodiment of the present invention.

Figure 9 depicts the stacked SDRAM modules further stacked on the controller module according to an example embodiment of the present invention. This configuration is used for high end applications. The figure also shows how the balls have corresponding pads for inter-module connection.

Figure 10 depicts stacked flash modules further stacked on the memory module according to an example embodiment of the present invention. The figure also shows how the balls have corresponding pads for inter-module connection.

Figure 11 depicts the possible stacking options for the first high-end controller module and the memory modules according to an example embodiment of the present invention. A substrate interface is used to attach one group of stacked modules to another.

Figure 12a is an isometric exploded drawing of the stacking technique presented in Figure 11 according to an example embodiment of the present invention. Multiple identical stacking is not included in this drawing.

Figure 12b is another package stacking technique using Pin Grid Array (PGA) rather than Ball Grid Array (BGA) according to an example embodiment of the present invention. This is used for easy replacement and expansion.

Figure 13 depicts the low-end controller module configuration with stacked flash module according to an example embodiment of the present invention. The figure also shows how the balls have corresponding pads for inter-module connection.

Figure 14 is an isometric exploded version of the stacking technique presented in Figure 11 according to an example embodiment of the present invention.

Figure 15a, 15b depict the second high-end controller module configuration with stacked memory modules according to an example embodiment of the present invention. The figures also show how the balls have corresponding pads for inter-module connection.

Figure 16 is an isometric exploded version of the stacking technique presented in Figure 14 according to an example embodiment of the present invention.

Figure 17a, 17b depict the second low-end controller module configuration with stacked memory modules according to an example embodiment of the present invention. The figures also show how the balls have corresponding pads for inter-module connection.

Figure 18 is an isometric exploded version of the stacking technique presented in Figure 17 according to an example embodiment of the present invention.

Figure 19 shows a pin assignment and connection technique to be able to select specific layer in a multi-stacked module according to an example embodiment of the present invention.

Figure 20a shows another pin assignment technique which uses a rotational stacking orientation to allow stacking of four identical modules representing different bus interfaces according to an example embodiment of the present invention.

Figure 20b shows a cross-section representation of the four stacked modules on a rotational stacking technique and how their pins mates according to an example embodiment of the present invention.

Figure 21a shows another pin assignment and connection technique to be able to connect a serial chain route from multiple modules in a stack according to an example embodiment of the present invention.

Figure 21b shows the routing of a serial chain connection from one stack location to another allowing application of both vertical and horizontal expansion independently or simultaneously according to an example embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1a is a block diagram of a flash storage system according to a first example embodiment of the present invention. The block diagram shows the entire high-end system that is modularized, stacked, and packaged to achieve the desired features of the technique. The heart of the system is the main controller-processor **101** which interfaces with the flash memory, the flash PROM and the SDRAM memory blocks. The SDRAM is configured from a single bank **102** to a maximum of four banks depending on the desired capacity. Each bank such as **102** includes 3 SDRAMs. The flash devices such as **107** are controlled by the Flash Interface Controller such as **105**. Each controller supports four flash buses such as flash bus A11 **106**, and each flash bus supports a maximum of 8 flash devices. The main controller-processor supports four flash interface controllers through 4 different busses such as B bus **104**. The four flash interface controllers with their corresponding flash devices comprise the memory set **108**. The main controller-processor can support from one memory set to a maximum of 15 memory sets. This is a maximum support of 1,920 flash devices.

Figure 1b is a block diagram of a flash storage system according to a second example embodiment of the present invention. The block diagram shows the entire low-end system that is modularized, stacked, and packaged to achieve the desired features of the technique. Since a low-end system may not require a large amount of memory capacity, SDRAM may be limited to one bank **109**, or none at all, and the supported flash devices may also be limited to only two sets of flash buses. One set of flash buses **110**

consists of four flash bus with 8 flash devices supported per flash bus, which results in a maximum supported number of 64 flash devices.

From the basic dies; SDRAM, FPROM, flash memory, flash interface controller, and the main controller-processor, single and multiple chip modules are created to become the basic building blocks for the stacking technique presented in the present invention. Referring to figure 2a which is a top view of an SDRAM module, three SDRAM dies **201** are placed in a single substrate **203** to become the SDRAM module which is one of the basic building blocks. The SDRAM module is represented in figure 1 as a single bank **102** composed of SDRAM 00, SDRAM 01, and SDRAM 02 connected to the SDRAM interface **103**. All signals needed to interface to the controller module and other SDRAM modules are assigned in both the bottom balls **204** and top pads **202** respectively. Bottom balls **204** are shown in figure 2b which is a bottom view of the SDRAM module, three slots **205** are created under the SDRAM die's pad attach area to accommodate bottom wire bonding. Figure 2c is the stacked module cross sectional representation. Top pads **202** and bottom balls **204** act as the vertical interconnects between all SDRAM modules and to the controller module. Varying the SDRAM die capacity and the stack quantity, results in wide range of total SDRAM capacity depending on the product application. The SDRAM device organization, capacity and bank limitations are defined by the main controller-processor's SDRAM interface specifications. The main controller-processor intended to be used for this example embodiment of the present invention supports a 32-bit wide 4 banks maximum SDRAM configuration.

Figure 3a is a top view that shows four flash dies **301** in a single substrate **303** that collectively form part of a flash module, which can also function as a basic building block. All signals needed to interface with the memory module and other flash modules are assigned in both the bottom balls **304** and the top pads **302**, respectively, as shown in FIGS. 3a, 3b and 3c. In figure 3c, the flash modules are stacked. Maximum stack quantity depends on the flash interface controller specifications. Top pads **302** and bottom balls **304** acts as the vertical interconnects between stacked flash modules and to the memory module. Varying the flash die capacity and the stacking quantity, results in a wide range of total flash capacity depending on the product application and capacity requirements. The flash device organization and capacity limitations are defined by the flash interface controller's specifications. The flash interface controller intended to be used for this used for this example embodiment of the present invention supports 8 flash devices per flash bus, thus allowing a maximum stacking of 8 flash modules.

Figure 4a shows the top view of the first example embodiment of the present invention illustrated in a first high-end controller module configuration. A single FPROM die **401** is placed at the center of the substrate **404**. Pads are composed of two sections, one for the SDRAM module interface shown as **402** and another for the memory module interface shown as **403**. This technique enables multiple stacking of both SDRAM modules and memory modules in a single package. Figure 4b shows the bottom view of the controller module. A single main controller-processor die **406** is placed at the center of the substrate. The controller module becomes a base module for the package.

The balls **405** are used to connect to the main substrate which is typically a printed circuit board (PCB).

Figure 5a shows the top view of the memory module which is also a basic building block. ¸A single flash interface controller die **501** is placed on the center of the substrate **504**. ¸Pads are composed of two sections, one for the flash module interface shown as **502** and another for the other memory module interface shown as **503**. ¸This technique enables multiple stacking of flash modules and memory modules in a single package. The memory module becomes a base module for the package. ¸Figure 5b shows the bottom view of the memory module. ¸The memory module balls **505** are used to connect to the main substrate PCB, to the controller modules or to the other memory modules depending on the type of configuration desired.

Figure 6a shows the top view of the second example embodiment of the present invention illustrated in a first low-end controller module configuration. Two SDRAMs **601** and a single FPROM **602** are placed on top of the module. This configuration is flexible. The SDRAMs can be unpopulated in a low performance application. Internal SRAMs in the main controller-processor will take over the SDRAM functions. The main controller-processor **605** is placed at the bottom of the module. This configuration does not allow stacking of the SDRAM which is not necessary for low capacity applications. Flash modules are stacked on top, interfacing to the pads **603.** The substrate **604** is the same size as the flash module making its final package smaller. The bottom balls **606** are used to interface with the main PCB.

Figure 7a shows the top view of the first example embodiment of the present invention illustrated in a second high-end controller module configuration, where four memory modules **701** can be mounted on separate locations adjacent to each other. Memory module interface pads **704** are allocated for multiple stack configurations. In the middle of the memory module interface pads, 3 SDRAM dies **702** are mounted. Each area corresponds to one SDRAM bank **703**, totaling to a maximum of 4 SDRAM banks in the package. The bottom view is presented in Figure 7b, where the main controller-processor die **705** and the FPROM die **706** are mounted adjacent to each other. The module's balls **707** are used for external interface to the main PCB.

Figure 8a shows the top view of the second example embodiment of the present invention illustrated in a second low-end controller module configuration, where only two memory modules **801** can be mounted side-by-side. Memory module interface pads **802** are allocated for multiple stacking configurations. In the middle of the memory module interface pads, 3 SDRAM dies **803** are mounted. Each area corresponds to one SDRAM bank **804**, totaling to only a maximum of 2 SDRAM banks in a package. The SDRAM can either be mounted or not depending on the application. Internal SRAMs can also be used instead of the SDRAMs. The stacked memory modules can also be configured to support both internal and external flash interface controller applications. The bottom view is presented in Figure 8b, where the main controller-processor die **805** and the FPROM die **806** are mounted adjacent to each other. The module balls **807** are used for external interface to the main PCB.

Figure 9 shows the stacking of SDRAM module **901** and controller module **902**. A single or stacked SDRAM module can be placed on top of a controller module. The pads for the SDRAM module interface **903** must align with the SDRAM module balls **904**. The bottom-most SDRAM module **905** serves as bank 0, and the top-most module **906** serves as bank 3. For low capacity SDRAM requirements, only a single or dual bank is enough. High capacity devices needs to have a maximum SDRAM capacity, thus stacking the maximum of 4 modules. The outer pads **907** are for the memory module interface.

Figure 10 shows the stacking of flash modules **1001** and memory module **1002**. A four-stack or eight-stack flash module is placed on top of a memory module. The pads for the flash module interface **1003** must align with the flash module balls **1004**. The outer pads **1005** are for other memory module interface. The flash interface controller intended to be used for this example embodiment of the present invention supports a maximum of 4 flash buses and each flash bus supports a maximum of 8 flash devices. The bottom-most flash module **1006** contains the 4 flash buses' Flash 00 devices and the top-most module **1007** contains the 4 flash buses' Flash 07 devices.

Figure 11 shows a sample of a maximized stacking technique that can be configured through vertical, horizontal or combined expansion. Multiple staking will increase the overall height of the module, thus requiring a filler **1101** to physically interconnect two stacked modules. A thinner filler **1102** may be used depending on the height differential between the modules which is dependent to the number of stacks

applied. A controller module with the stacked SDRAM modules act as the controller package **1103**. A memory module with stacked flash modules acts as the memory package **1104**. Four memory packages stacked together form the memory set **1105**. Vertical expansion happens when the controller package is stacked with a single or multiple memory sets. The figure shows a single memory set to be stacked to the controller package. Horizontal expansion happens when the controller package is located on a different site on the PCB relative to the memory sets. Also multiple memory sets can be located on different sites on a PCB. Combo expansion happens when both vertical and horizontal expansion technique is implemented simultaneously. The expansion technique is very flexible depending on the desired memory capacity, main PCB size limitations and also height limitations.

Figure 12a shows the isometric and exploded drawing of the stacking technique for the first high-end controller configuration. Pins are assigned strategically and modules are stacked to make possible the miniaturization of the entire system in a package.

1201 – The Flash Module

1202 – The Flash Die

1203 – The Flash Module Pad Interface to other Flash Modules

1204 – The Flash Module Solder Balls

1205 – The Memory Module

1206 – The Flash Interface Controller Die

1207 – The Memory Module Pad Interface for the Flash Module

1208 – The Memory Module Pad Interface for the other Memory Modules

1209 – The Memory Module Solder Balls

1210 – The SDRAM Module

1211 – The SDRAM Die

1212 – The SDRAM Module Pad Interface to other SDRAM Modules

1213 – The SDRAM Module Solder Balls

1214 – The Controller Module

1215 – The FPROM Die on top side and the Main Controller-Processor Die at the bottom side.

1216 – The Controller Module Pad Interface to the SDRAM Modules

1217 – The Controller Module Pad Interface to the Memory Modules

1218 – The Controller Module Solder Balls

Figure 12b is another technique used in this invention to ease replacement and facilitate expansion. Instead of using Ball Grid Array (BGA), Pin Grid Array (PGA) **1219** is used. This method makes it more flexible due to the technology's inherent feature where replacement is done swiftly without any assembly process involved. Horizontal expansion is also benefited in this technology. The figure shows the stacked memory module as an example. The memory module is packaged using the PGA technology, where the top portion of the package becomes the socket **1220** and the bottom portion the pin arrays **1219**. The filler **1221** becomes the package's top socket and is interfaced into the base module **1222** through the BGA **1223**. The base module uses PGA to interface to the bottom package or to the main board **1224**. Filler **1225** is also mounted into the main board to interface the stacked memory modules.

Figure 13 shows the stacking of the flash module **1301** and the first low-end type of controller module **1302**. A single or stacked flash module can be placed on top of the controller module. The pads for the flash module interface **1303** must align with the flash module balls **1304**. This configuration is for low capacity low performance applications. The number of flash modules to be stacked depends on the desired capacity and is limited to the supported feature of the main controller-processor. The main controller-processor's flash interface can support a maximum of 8 buses and a maximum of 8 flash devices per bus.

Figure 14 shows the isometric and exploded drawing of the stacking technique for the first low-end controller configuration. Pins are assigned strategically and modules are stacked to make possible the miniaturization of the entire system in a package.

1401 – The Flash Module

1402 – The Flash Die

1403 – The Flash Module Pad Interface to other Flash Modules

1404 – The Flash Module Solder Balls

1405 – The Controller Module

1406 – The FPROM Die and the Main Controller-Processor Die at the bottom

1407 – The SDRAM Die

1408 – The Controller Module Pad Interface to the Flash Modules

1409 – The Controller Module Solder Balls

Figure 15a shows the stacking technique for the second high-end controller configuration. The stacked flash modules **1501** are further stacked on top of the memory modules **1502** which are then mounted on the controller module **1503** on four different locations. Four memory modules can be mounted on four different locations on the controller module creating a memory set. Stacking more memory sets increases the total capacity. The cross-sectional representation of the said stacking technique is shown in Figure 15b. The memory module balls **1504** must align to the pad interface **1505** on the controller module. As previously discussed in figure 11, fillers are used to physically connect two successively stacked modules. The controller balls **1506** will become the external interface to the main board. The final package is 4X bigger than the first high end option.

Figure 16 shows the isometric and exploded drawing of the stacking technique discussed in Figure 15. Pins are assigned strategically and modules stacked to make possible the maximum stacking and interconnection between modules. As previously discussed in figure 11, fillers are used to physically connect two stacked successively stacked modules.

1601 – The Flash Module

1602 – The Flash Dies

1603 – The Flash Module Pads Interface to other Flash Modules

1604 – The Flash Module Solder Balls

1605 – The Memory Module

1606 – The Flash Interface Controller Dies

1607 – The Memory Module Pad Interface to Flash Modules

1608 – The Memory Module Pad Interface to other Memory Modules

1609 – The Memory Module Solder Balls

1610 – The Controller Module

1611 – The SDRAM Dies on top side and the FPROM and Main Controller-Processor at the bottom side

1612 – The Controller Module Pads Interface to the Memory Modules

1613 – The Controller Module Solder Balls

Figure 17a shows the stacking technique for the second low-end configuration. The stacked flash modules **1701** are further stacked on top of the memory modules **1702** which are then mounted on the controller module **1703** on two different locations. This technique can use both internal and external flash interface controller configurations, making this technique flexible. The cross-sectional view is shown in figure 17b. The memory module balls **1704** must align to the pad interface **1705** on the controller module. The controller balls **1706** will become the external interface to the main board. The final package is twice the size of the first high end option.

Figure 18 shows the isometric and exploded drawing of the stacking technique discussed in Figure 17. Pins are assigned strategically and modules stacked to make possible the maximum stacking and interconnection between modules. As previously discussed in figure 11, fillers are used to physically connect two stacked successively stacked modules.

1801 – The Flash Module

1802 – The Flash Dies

1803 – The Flash Module Pads Interface to other Flash Modules

1804 – The Flash Module Solder Balls

1805 – The Memory Module

1806 – The Flash Interface Controller Dies

1807 – The Memory Module Pad Interface to Flash Modules

1808 – The Memory Module Pad Interface to other Memory Modules

1809 – The Memory Module Solder Balls

1810 – The Controller Module

1811 – The SDRAM Dies on top side and the FPROM and Main Controller-Processor at the bottom side

1812 – The Controller Module Pads Interface to the Memory Modules

1813 – The Controller Module Solder Balls

A more detailed technique on how the pins are assigned and how modules are placed with different orientation in the stack is discussed in the following paragraphs.

Figure 19 shows a first pin assignment and connection technique that enables a selection of specific module in a multiple module stack. The figure illustrates the controller and SDRAM modules as an example. The SDRAM module balls, such as **1907**, are represented by big oblong shapes, and the pads such as **1908** are represented by smaller oblong shapes. A pad to ball connection is represented by a rectangle, such as

1906. The controller module has four active pads such as **1904,** one each for the four SDRAM modules such as **1901**. The controller module's active pad 00 **1904** is connected to SDRAM module 0's X0 ball **1903**, pad 01 to SDRAM module 1's X0 ball **1902**, and so on. The X0 balls are the active balls for the SDRAM modules. All SDRAM modules are identical which include the connections as follows: X1 ball is connected to X1 pad, X2 ball to X2 pad, and so on. The technique involves using a ladder-like routing path, such as **1905** on the stacked modules. This technique enables the controller module's active pad to be routed to the desired specific module in the stack. The example embodiment illustrated in figure 19 comprises a repeating pattern for the balls and pads. Passive balls are connected within each module to passive pads with an offset distance equaling one periodic distance of the repeating pattern. The importance is the approach using repeating pattern and offsetting of the passive ball to passive pad within each module, other offset distances can be used also in other embodiment of the present invention, e.g. using an offset of two or any multiple of the periodic distance of the repeating pattern. The example embodiment does not limit the scope of the present invention.

Another pin assignment, connection, and stacking combo method introduced in this invention is the rotational stacking technique. Figure 20a shows the pad interconnects for a certain base module and strategic numbering is assigned. Pads labeled with numbers 1 to 4 represent the four different groups of signals. Pads labeled with the number 5 are used for the vertical stacking IOs (more details are illustrated in figure 21a). Pads labeled with the number 6 are reserved for power and ground which are common to

all modules in the stack. Since the stacked modules are identical, we can use rotational stacking to connect one module to one group of signals and the following rotated stacked module connects to another group of signals, and so on. This way ensures four identical modules to be stacked and connected to four different groups of signals from the base module which is typically a controller. Pad 1 **2001,** upon the substrate being rotated 90 degrees clockwise, occupies pad 2 **2002** location relative to an un-rotated substrate such as the base substrate which is typically a controller. In a similar manner pad 1 **2001** can be located at pad 3 **2003** location, then pad 4 **2004** location upon the substrate being rotated 180 and 270 degrees clockwise respectively.

Figure 20b shows a cross-sectional view of four such modules stacked over the base module. Memory and Controller modules are used as example. Pin 1s such as **2005** on the stacked modules are the only active signal pins for the module. The rest (numbered 2 to 4) **2006** are directly connected to the balls underneath them but have no other connections. This way connection is continued from bottom to top. The active pin **2007** of the first module **2008** is aligned to pin 1 pad **2009** on the base module, and the second module's active pin **2010** is aligned on pin 2 **2011** of the base module with second module being rotated 90 degrees clockwise. Since pin 2 **2012** on the first module is directly connected to the ball underneath, this allows the pin 1 on the second module **2013** to be connected to pin 2 **2011** of the base module. Rotating the next stacked module 90 degrees more, will align it's active pin to the base module pin 3 and so on until the forth rotation.

The last connection technique is used for serial routing of all modules in the stack and allowing them to be externally accessible for horizontal expansion on a PCB, such as a main board. Figure 21a shows how this technique is implemented in the stacking method. The main board **2101** contains the input signals **2102** which will then be connected to IN ball **2104** of the base module **2103**. The base module's OUT pad **2105** is connected to IN ball **2107** of the first stack module **2106**, and so on. The top module **2108** terminates the signal to the top pad **2109** and routes, with connection **2112**, the signal internally to another pad **2110** which is connected directly to the ball **2113** underneath. Since the modules are identical, this routed signal passes through the pads and balls **2111** of the stack until it reaches the OUT pad **2114** of the main board for external access. How the top module terminates the serial chain and branches them out to other pads is shown in Figure 21b. All modules have a selectable buffer **2115** that tri-states the input when pulled low. The signal from the IN balls **2116** enters the internal circuit **2117** and exits the circuit connecting to the OUT pad **2118**. The buffer's **2115** control line is weakly pulled up internally. The "StkLow" ball is connected internally to GND **2119**, thus pulling down the buffer control line when a module is stacked above it, and it is pulled up when no module is stacked directly above it. When the buffer control line is pulled high, it will let the input signal branch out **2120** to the other pads, thus creating a connection route or trace that loops back to the base module solder balls. When a module is stacked above a module that is disposed with selectable buffer **2115** in the manner shown, the buffer control signal is pulled low, tri-stating the input signal and disallowing the branching effect. This technique allows the signal to be accessible to the external balls of the base module, thus horizontal expansion for a serial signal is

achievable. The balls are then routed, with connection **2121**, to the other modules **2122** on the other locations. The same technique is used on the main board **2123**, when no package is detected on the "StkLow" pad, the buffer allows the input to connect to the designated pads on the other locations. The tri-stated buffer technique is redundant to all locations. An example is the JTAG TDI-TDO signal. The diver circuit **2125** sends out TDI signals to the pads and the closing TDO signal **2124** loops back to the driver circuit.

Combining these stacking, pin assigning and connection techniques allow interconnection between modules with both parallel and series signals to both vertical and horizontal expansion. The technique is very flexible depending on the specific application, capacity, board size and height limit.

ABSTRACT

Stacking techniques are illustrated in example embodiments of the present invention wherein semiconductor dies are mounted in a module to become a MCM which serves as the basic building block. A combination of these modules and dies in a substrate creates a package with specific function or a range of memory capacity. Several example system configurations are provided using BGA and PGA to illustrate the stacking technique. Several pin assignment and signal routing techniques are illustrated wherein internal and external signals are routed from main board to various stacked modules. Expansion can be done both on the vertical and horizontal orientations.

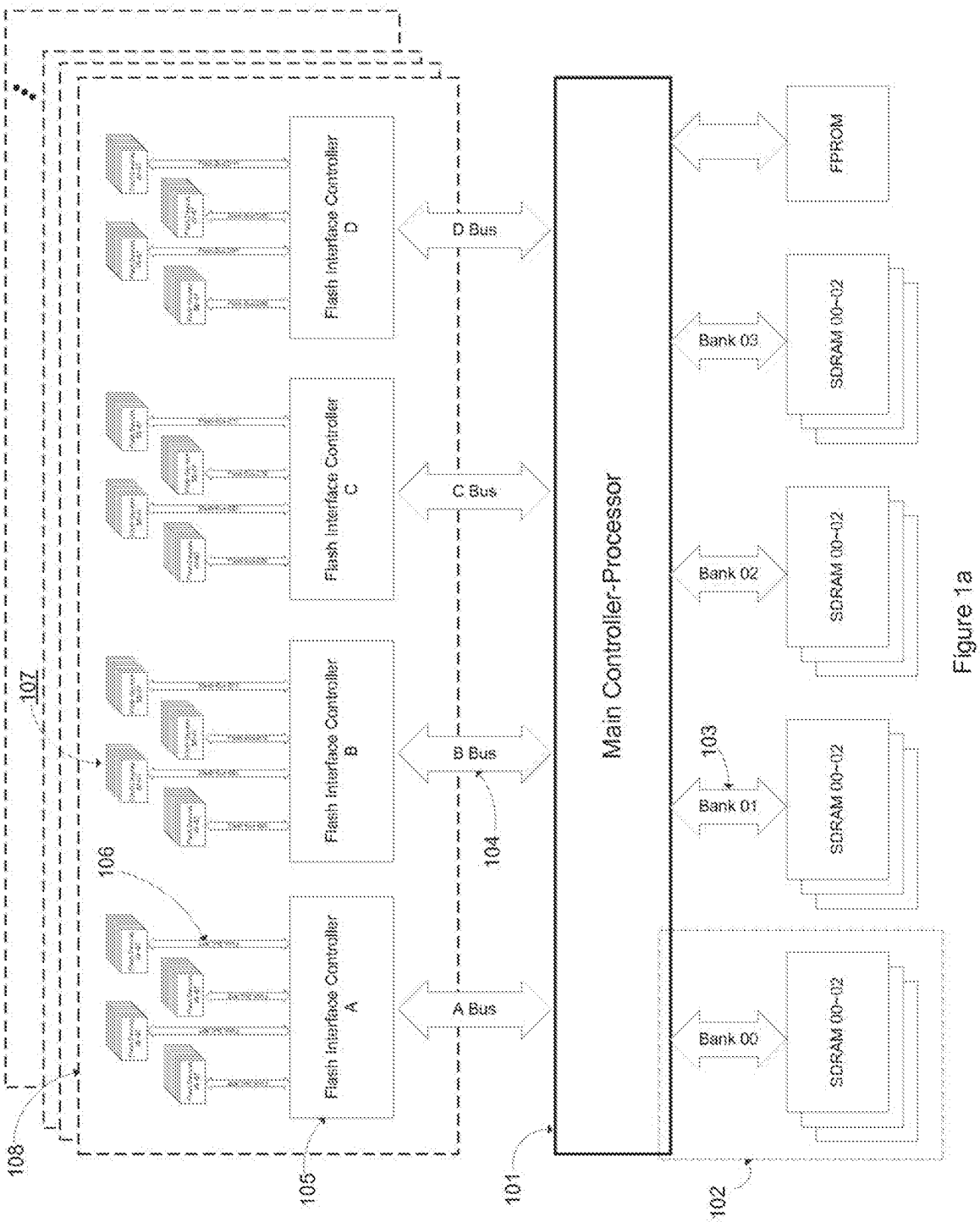

Main Controller-Processor
Flash Interface Controller A
Flash Interface Controller B
Flash Interface Controller C
Flash Interface Controller D
A Bus
B Bus
C Bus
D Bus
FPROM
SDRAM 00~02
Bank 00
Bank 01
Bank 02
Bank 03
101
102
103
104
105
106
107
108

Figure 1a

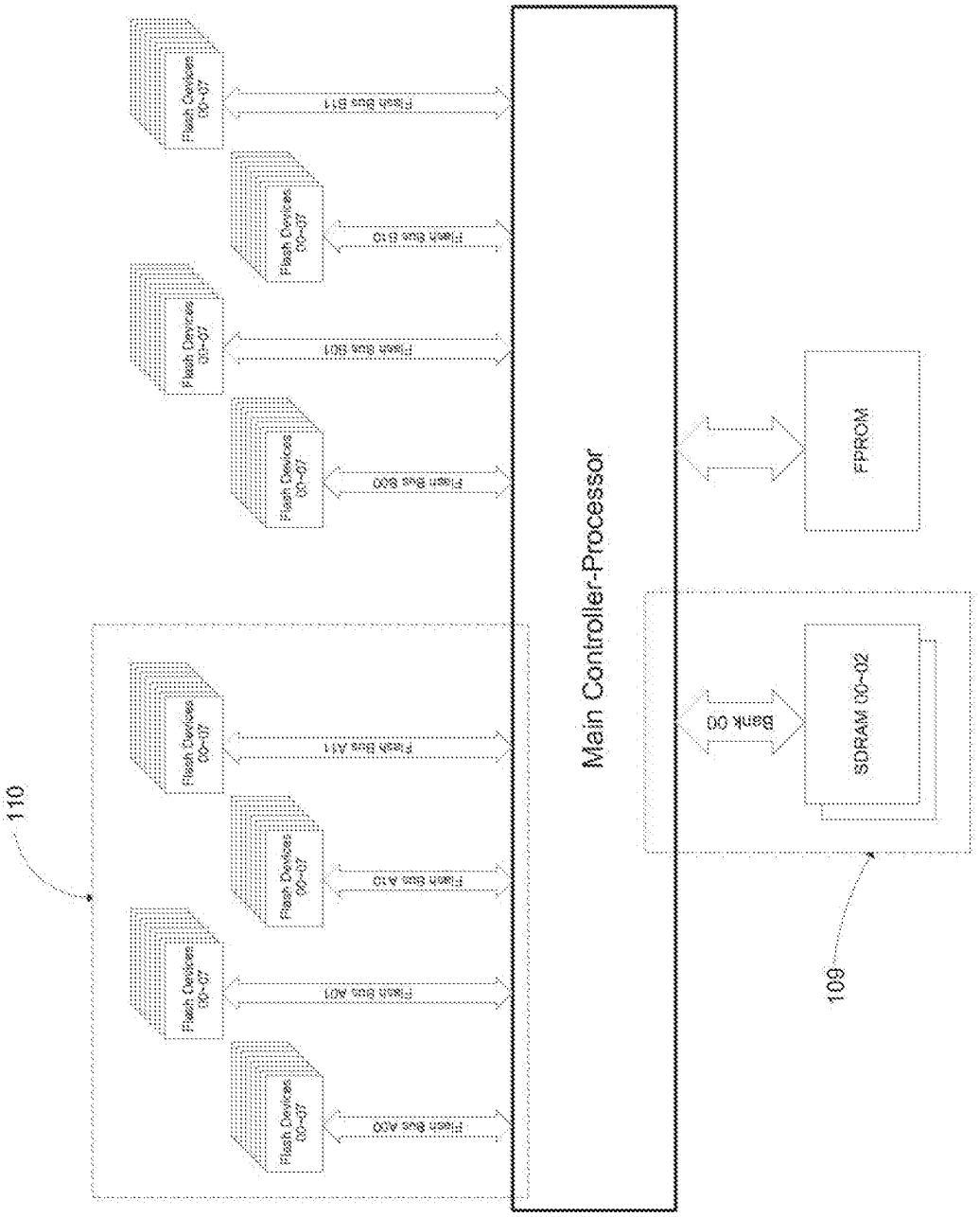

Flash Devices 00~07
Flash Bus B11
Flash Bus B10
Flash Bus B01
Flash Bus B00
Flash Bus A11
Flash Bus A10
Flash Bus A01
Flash Bus A00
Main Controller-Processor
FPROM
Bank 00
SDRAM 00~02
110
109

Figure 1b

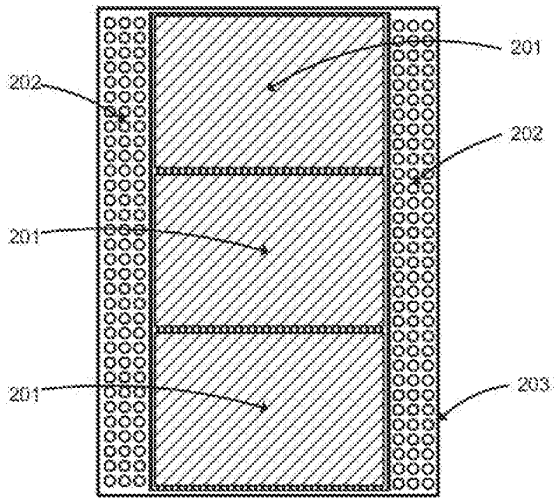


Figure 2a

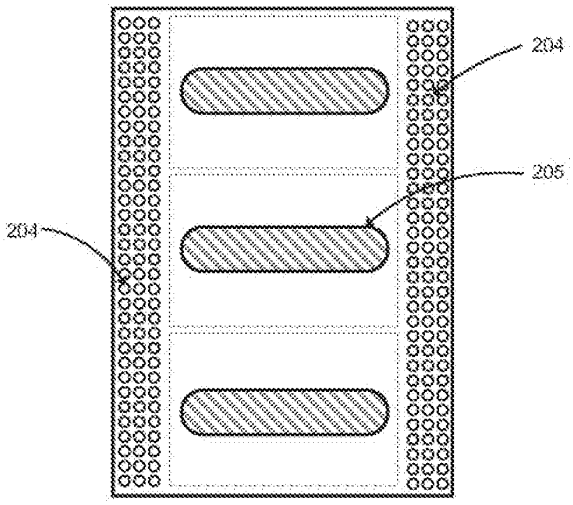


Figure 2b

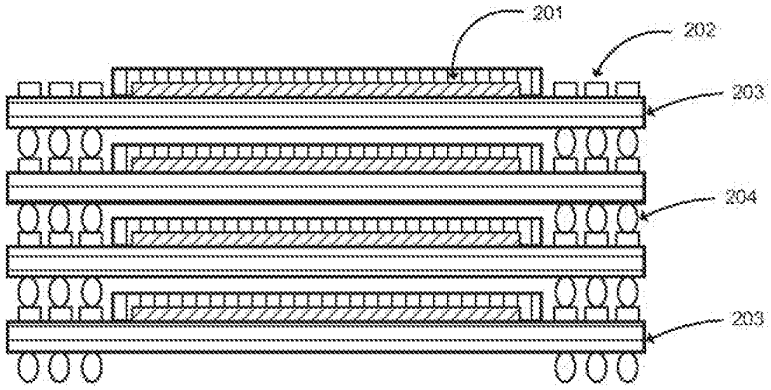


Figure 2c

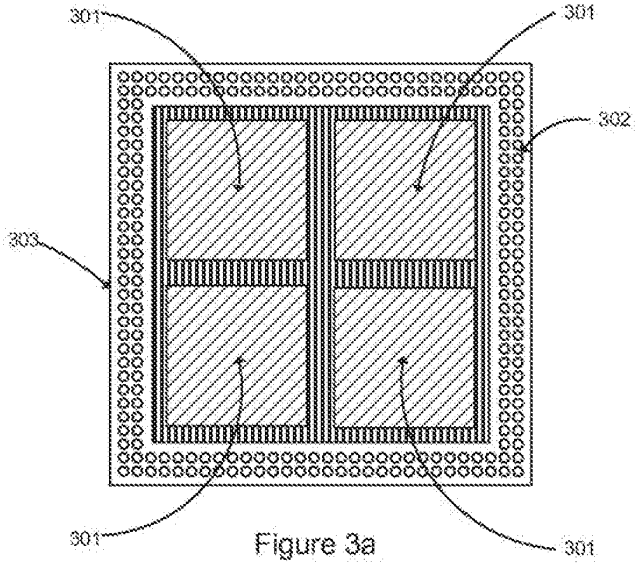


Figure 3a

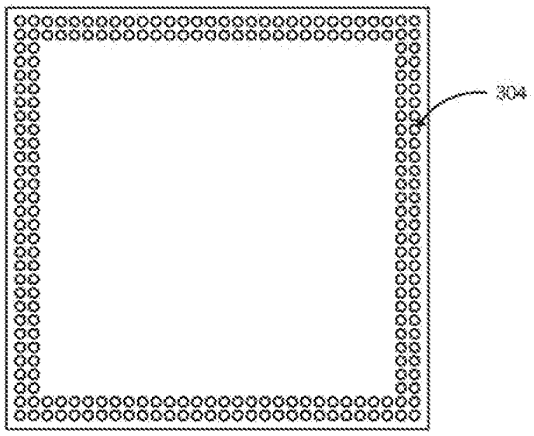


Figure 3b

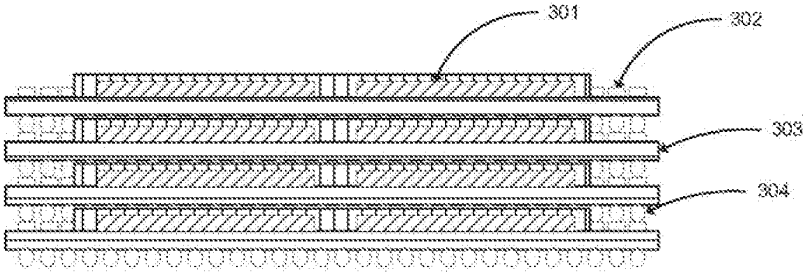


Figure 3c

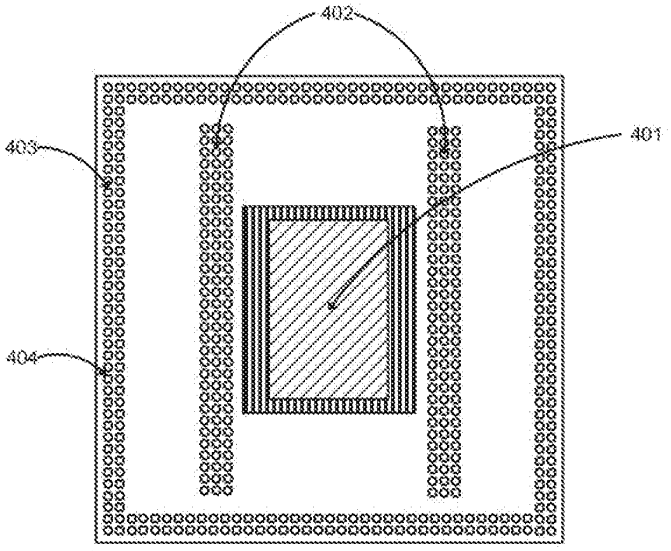


Figure 4a

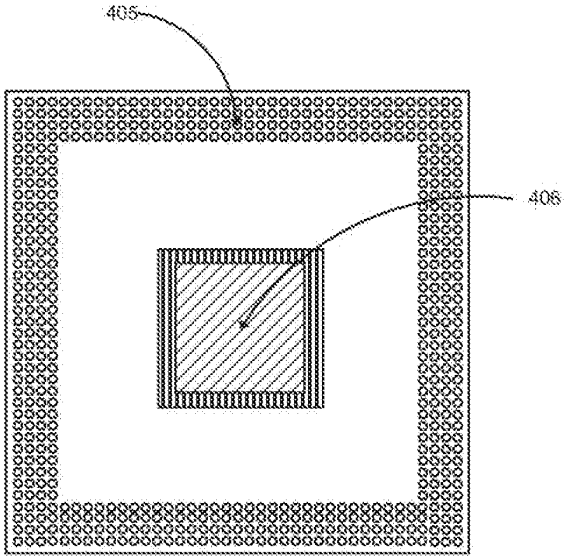


Figure 4b

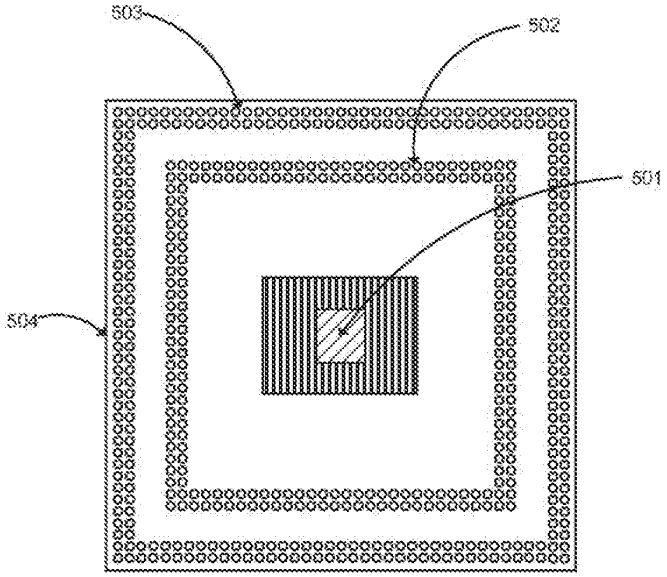


Figure 5a

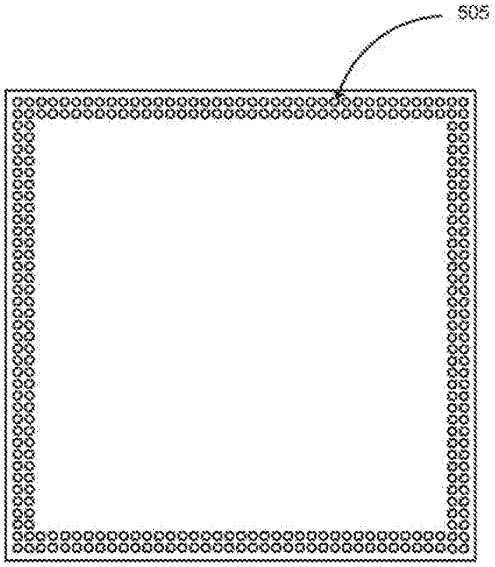


Figure 5b

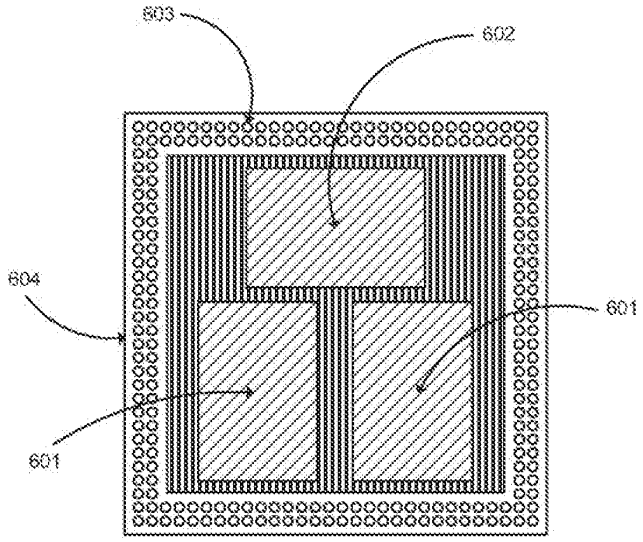


Figure 6a

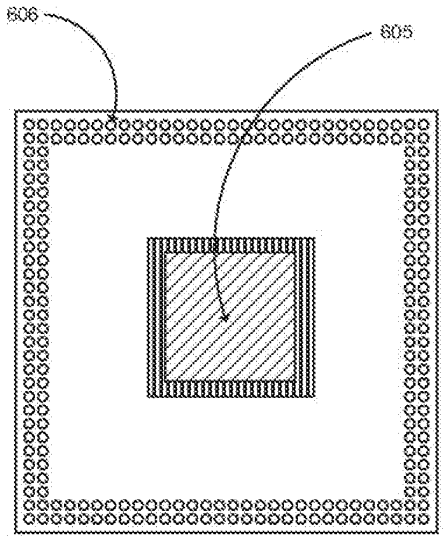


Figure 6b

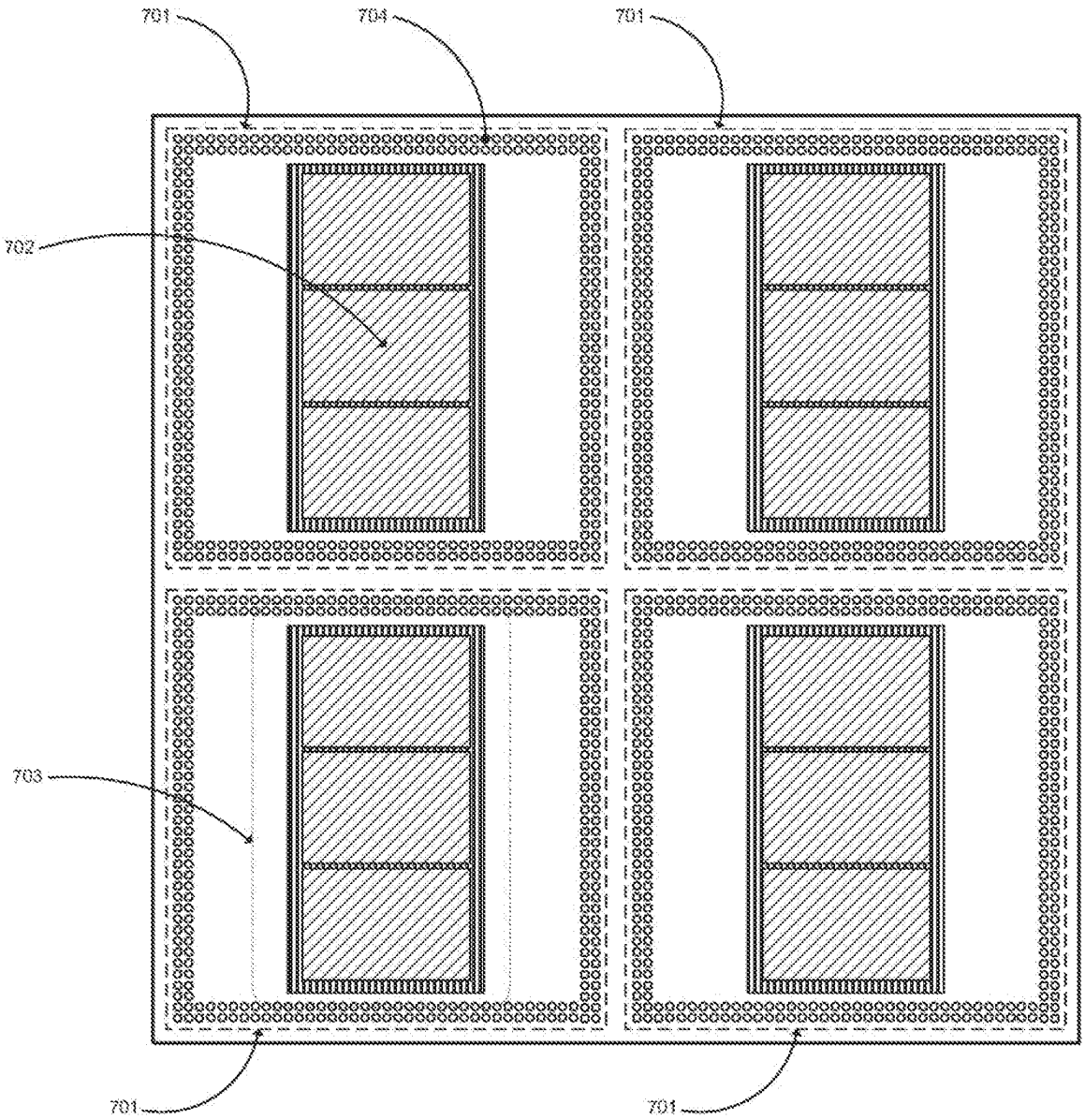


Figure 7a

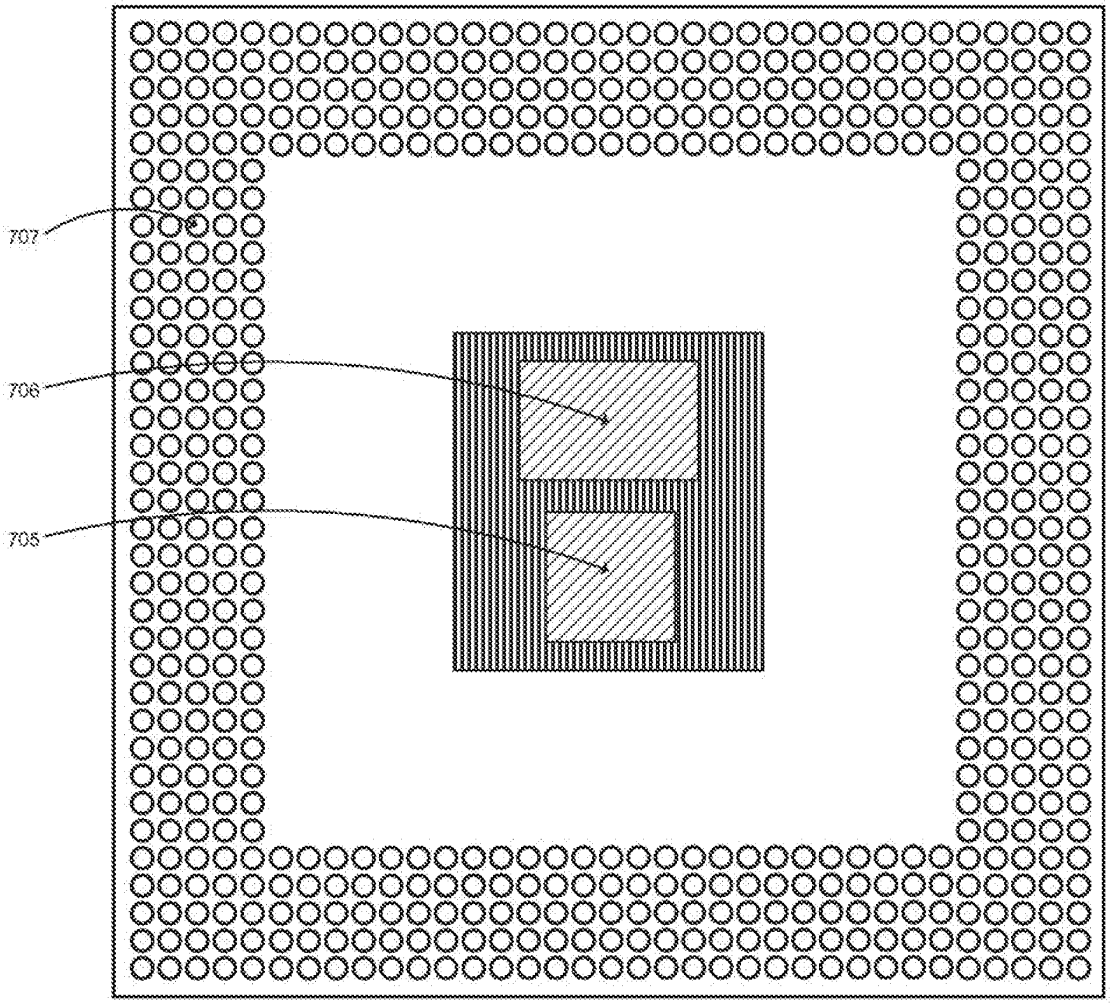


Figure 7b

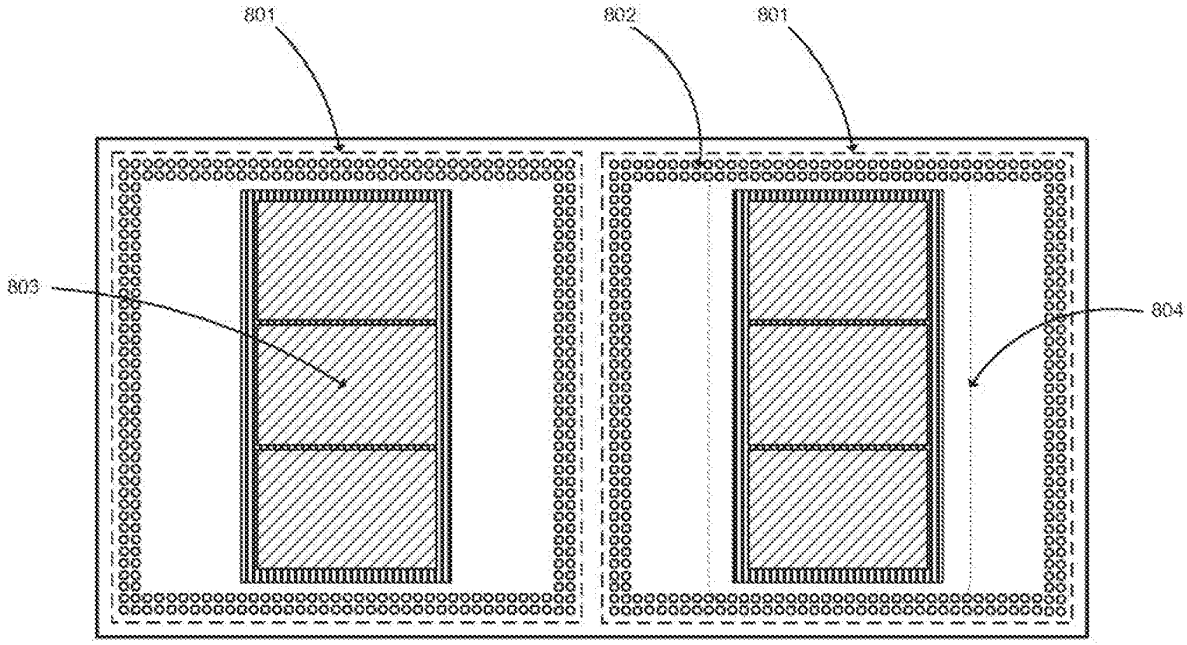


Figure 8a

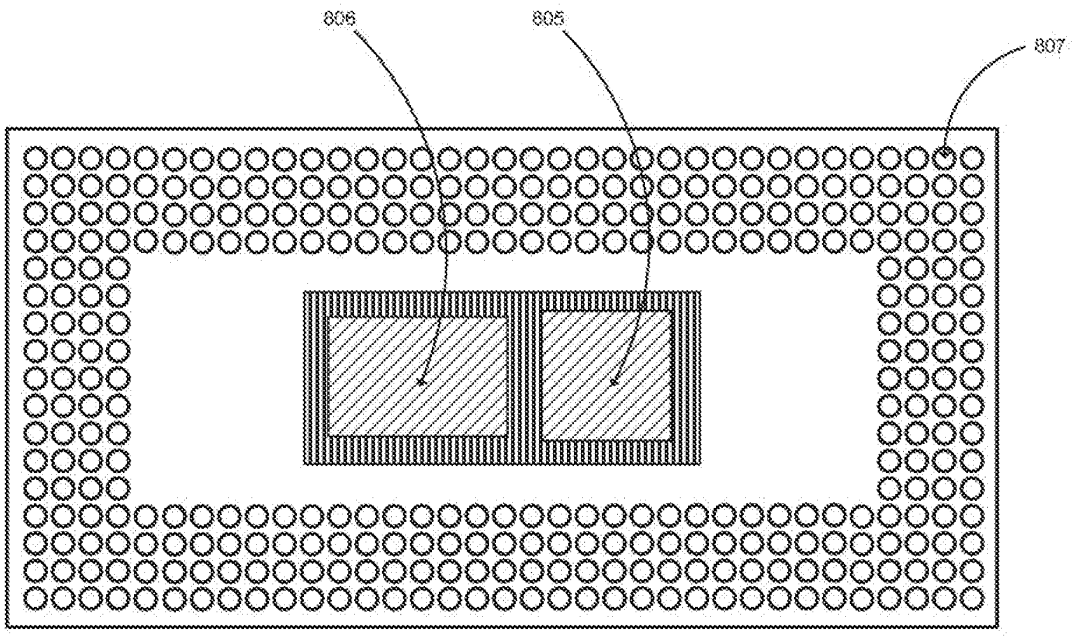


Figure 8b

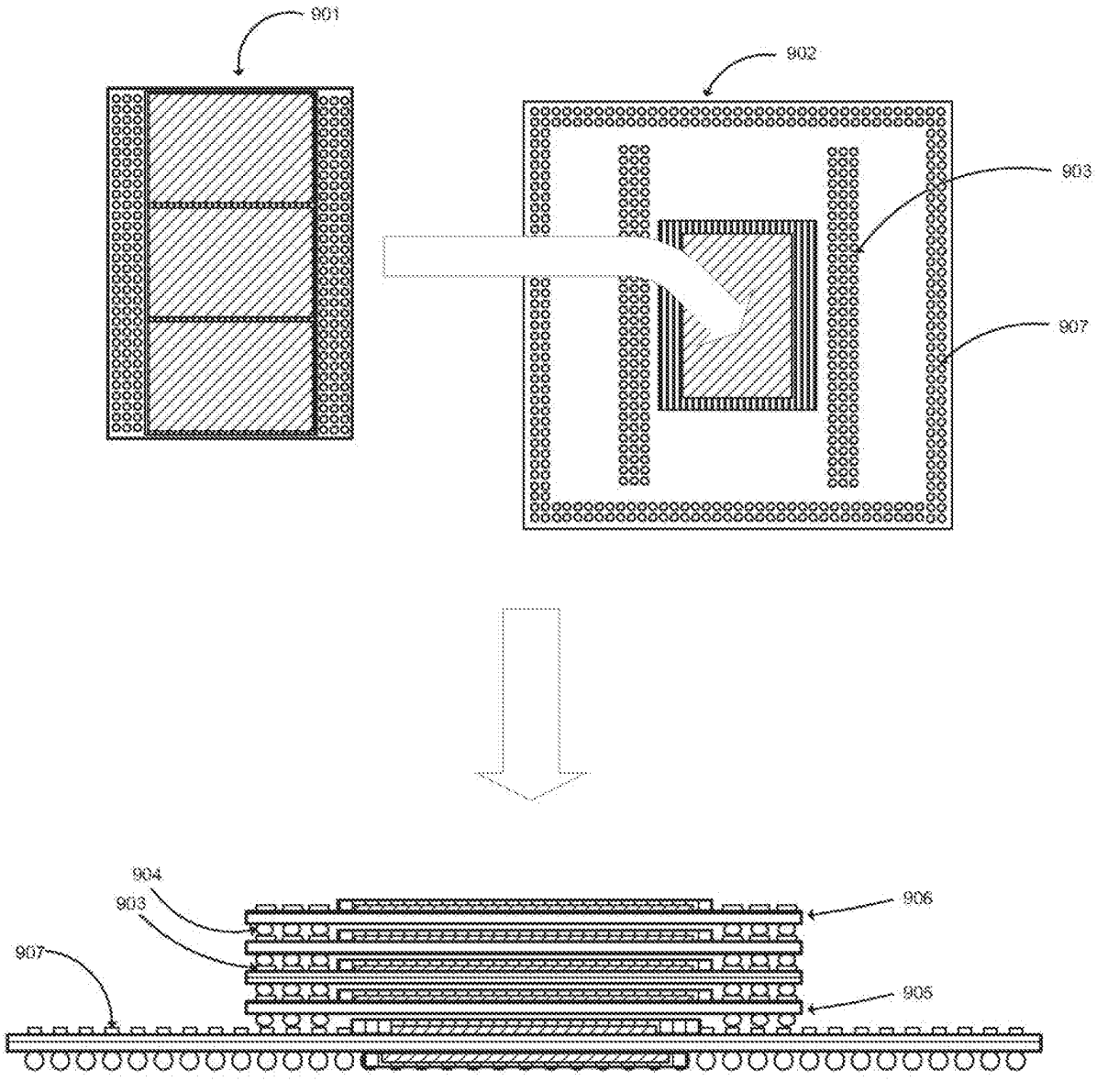


Figure 9

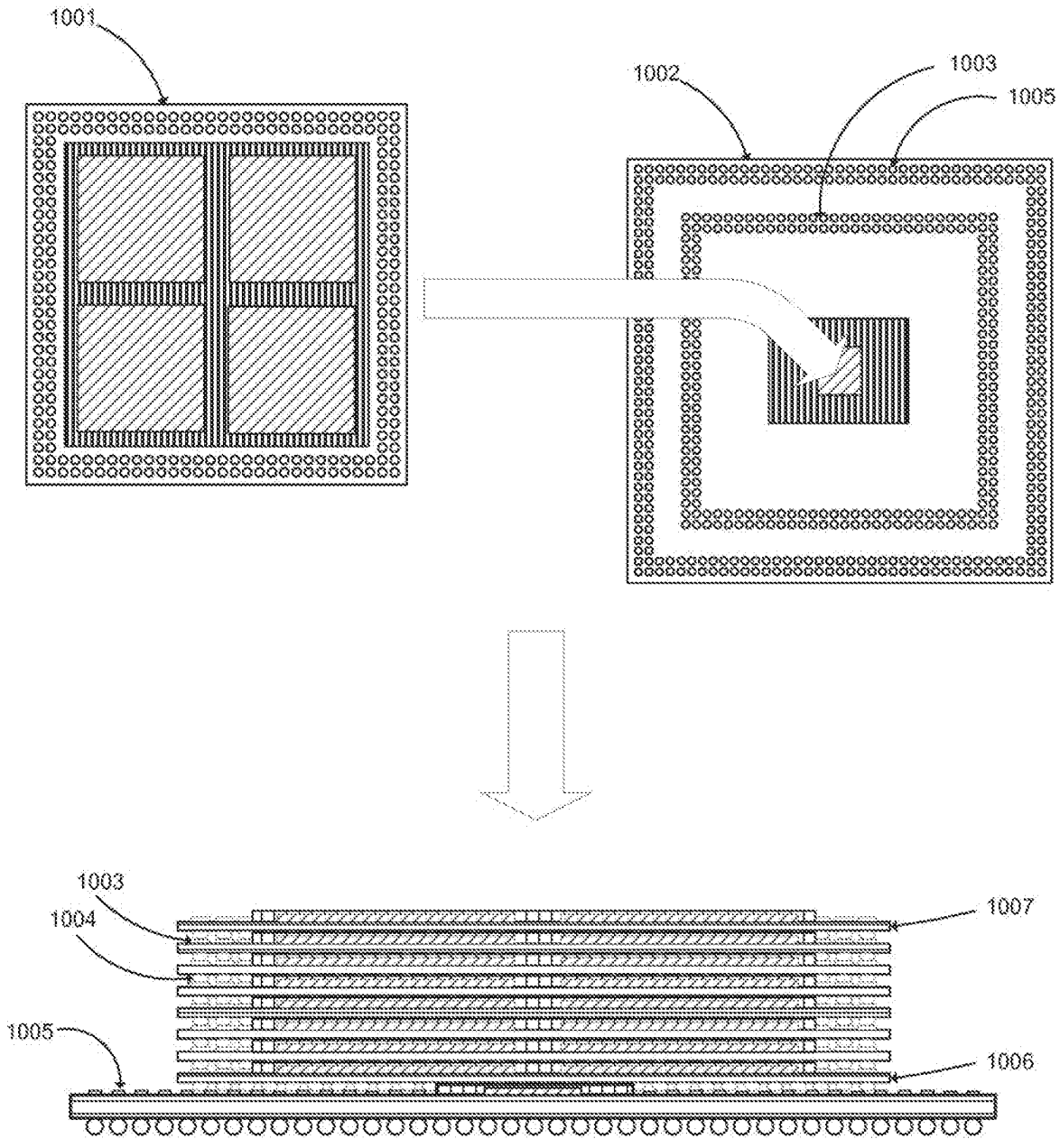


Figure 10

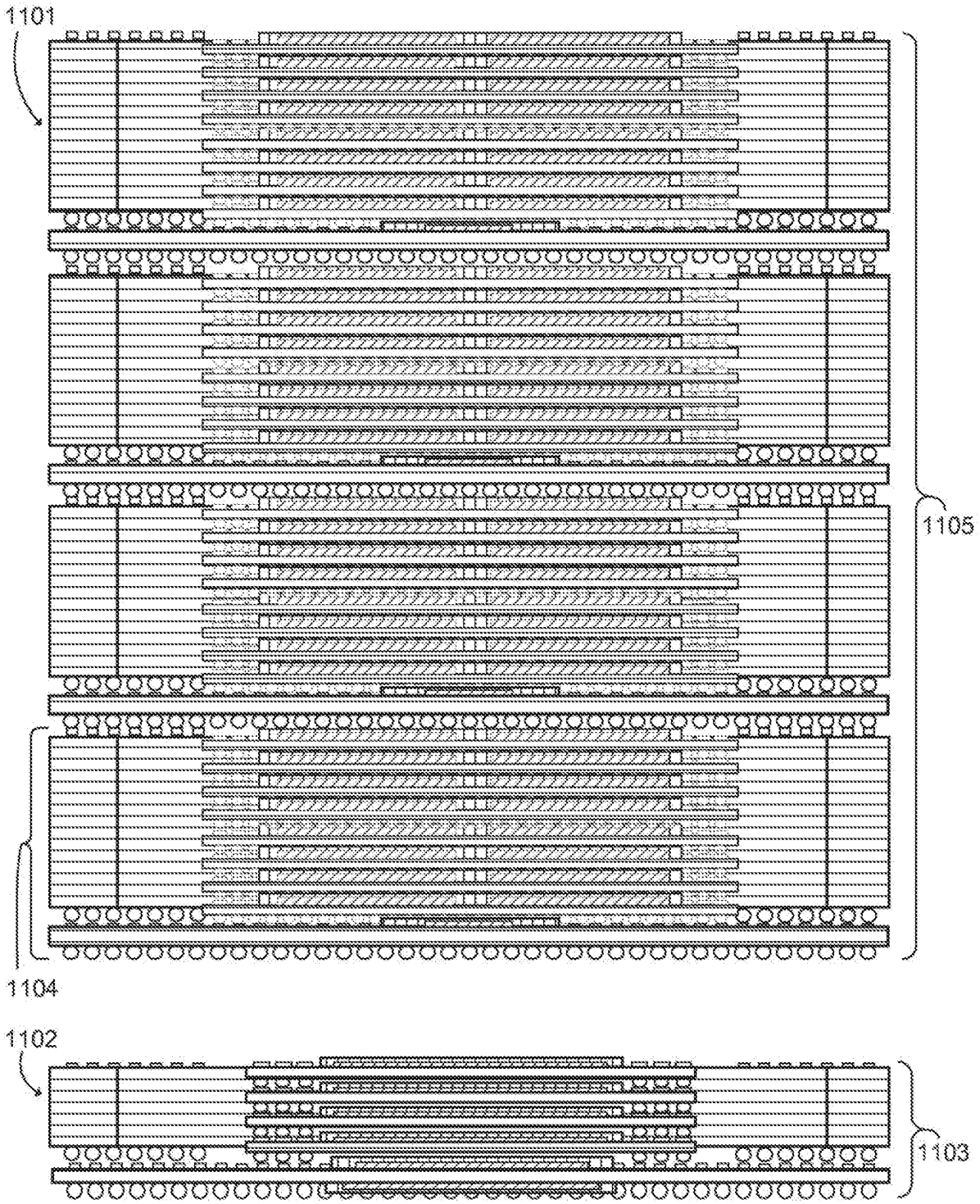


Figure 11

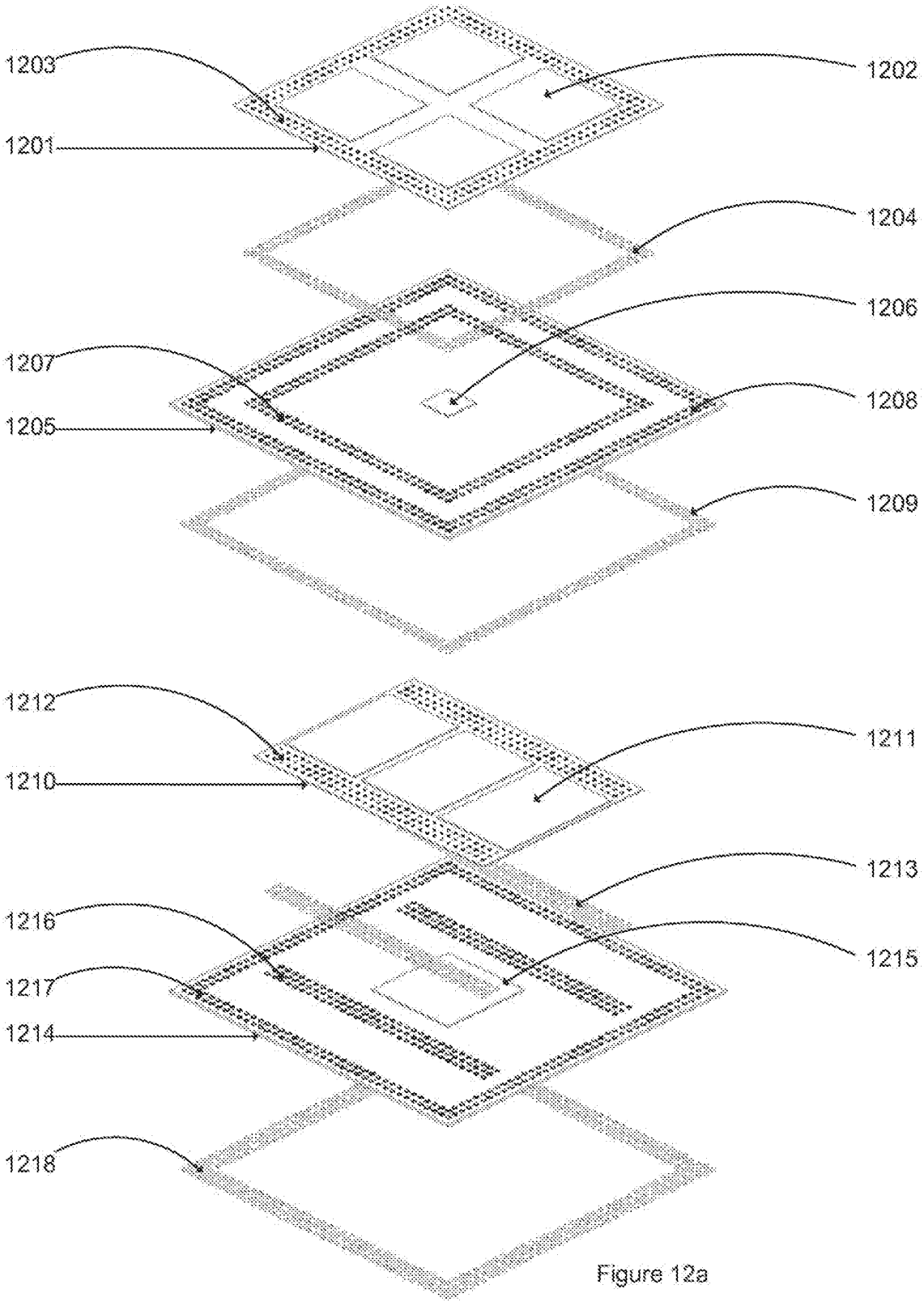

1203
1202
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1218

Figure 12a

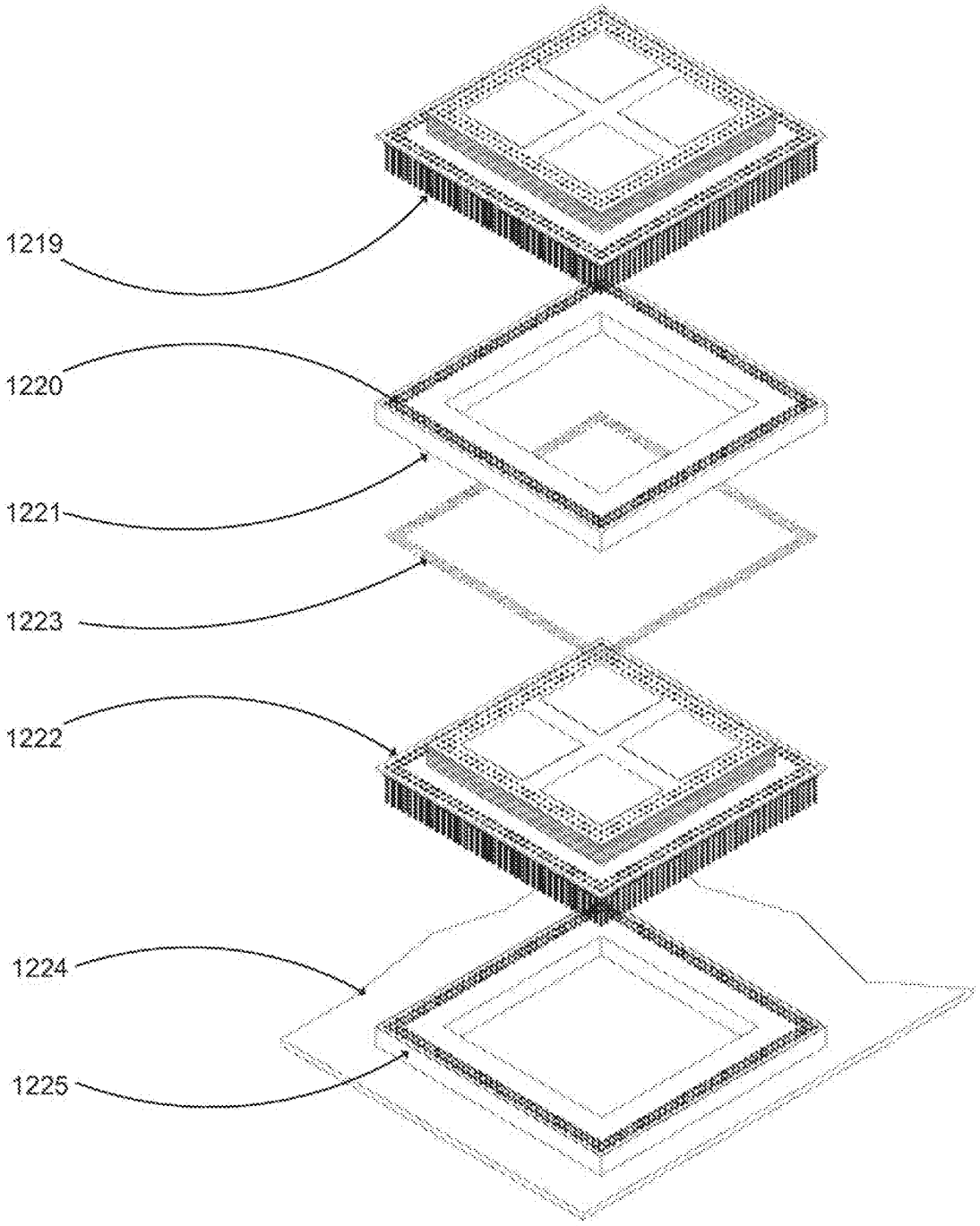


Figure 12b

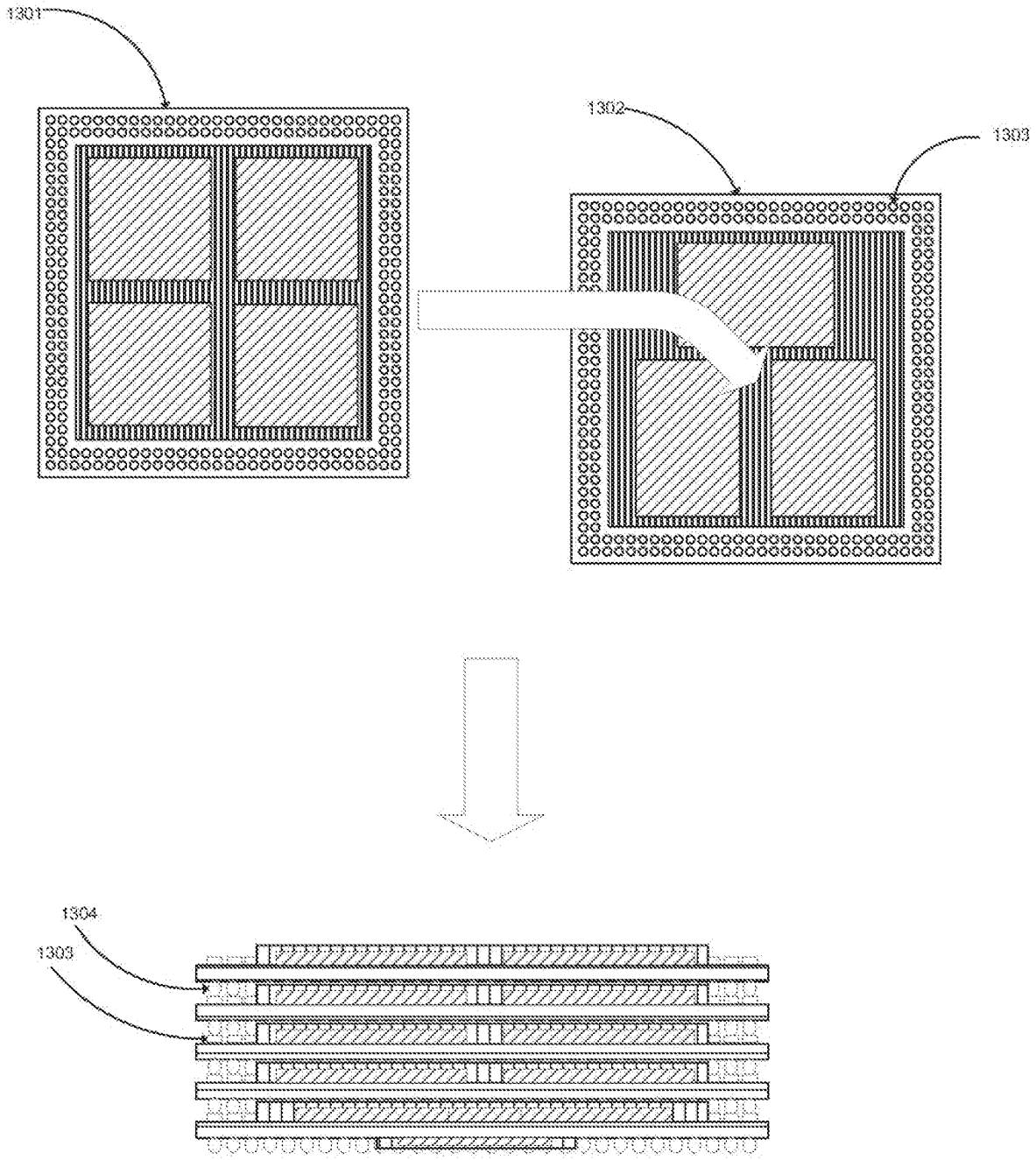


Figure 13

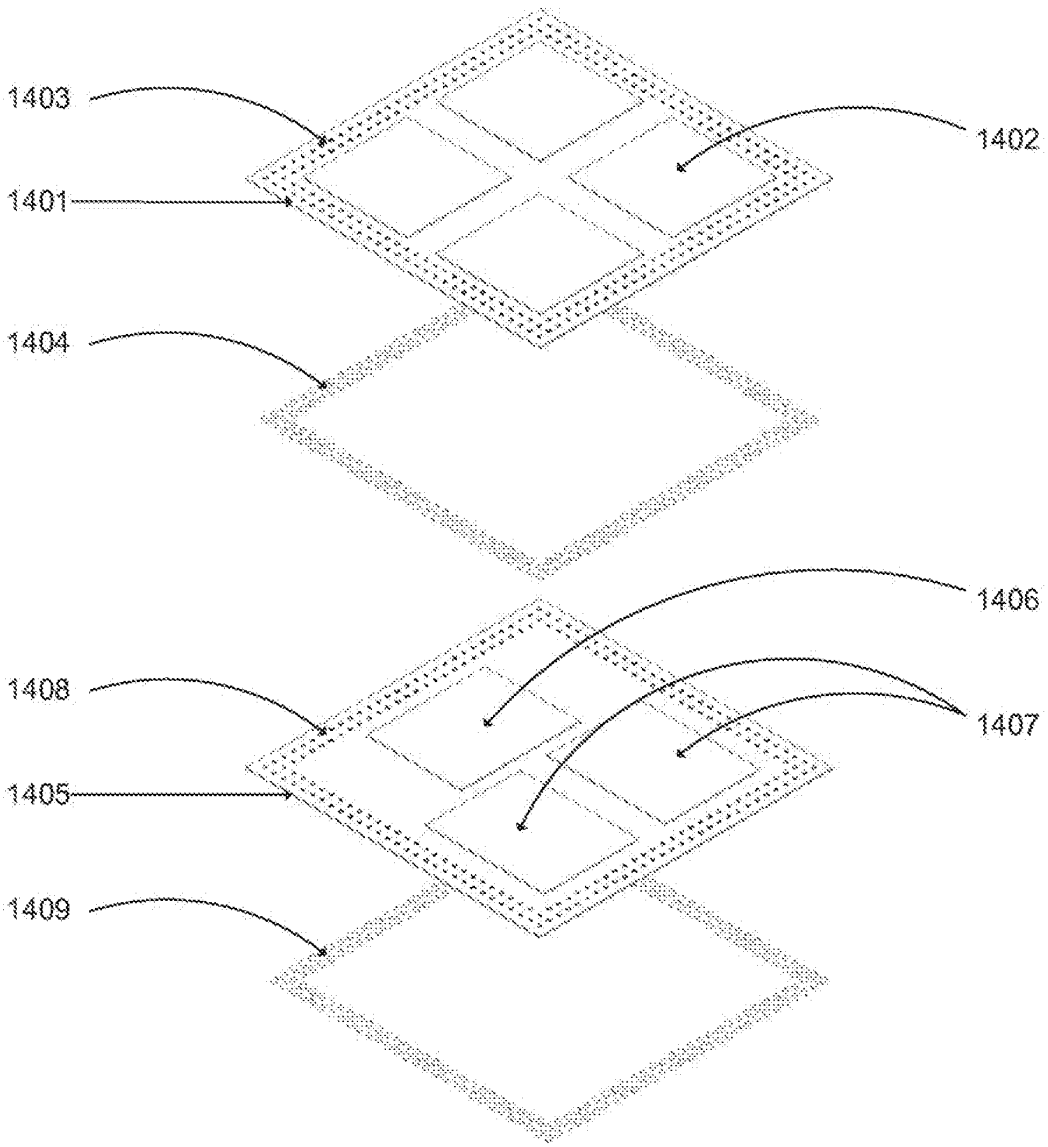


Figure 14

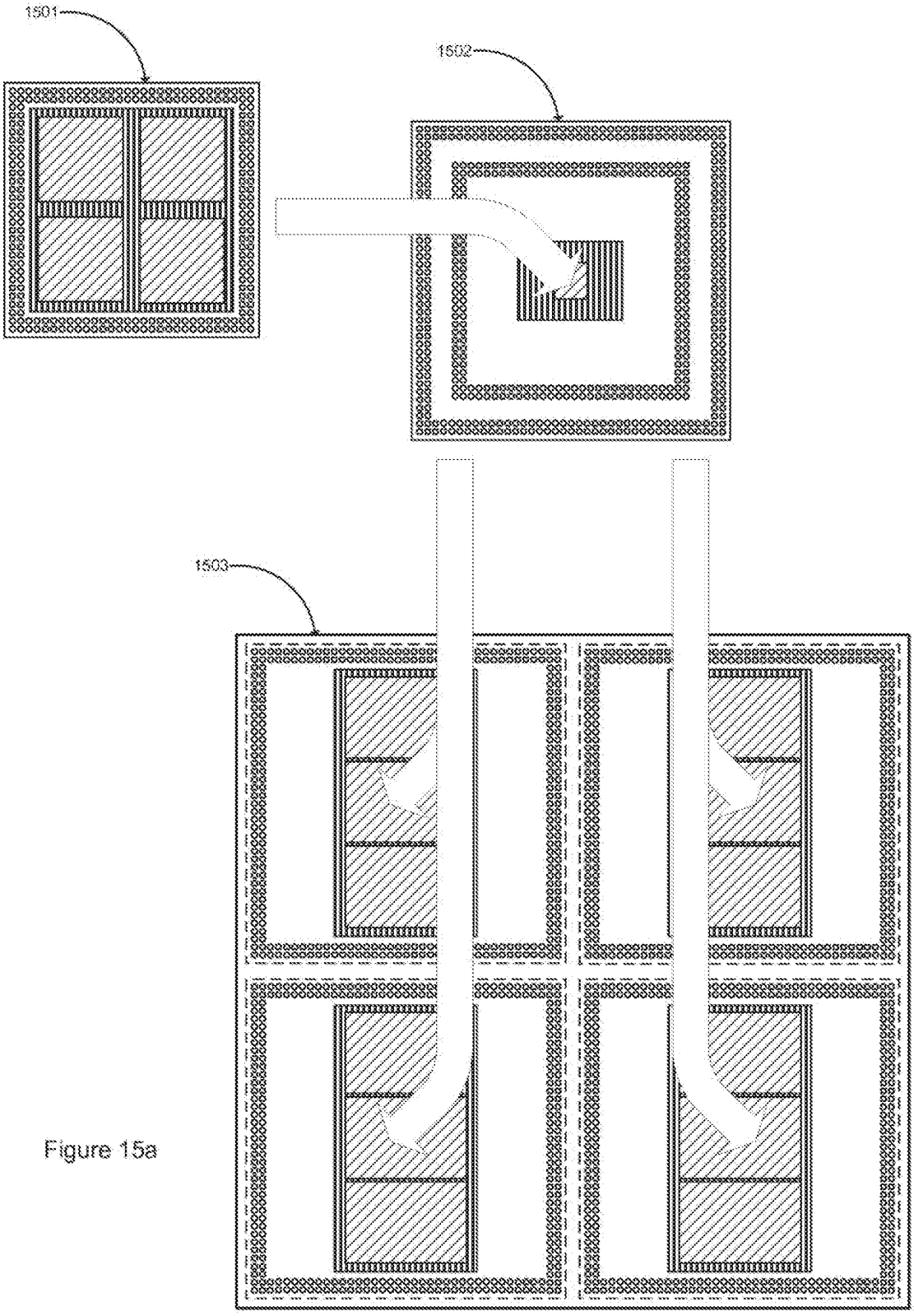


Figure 15a

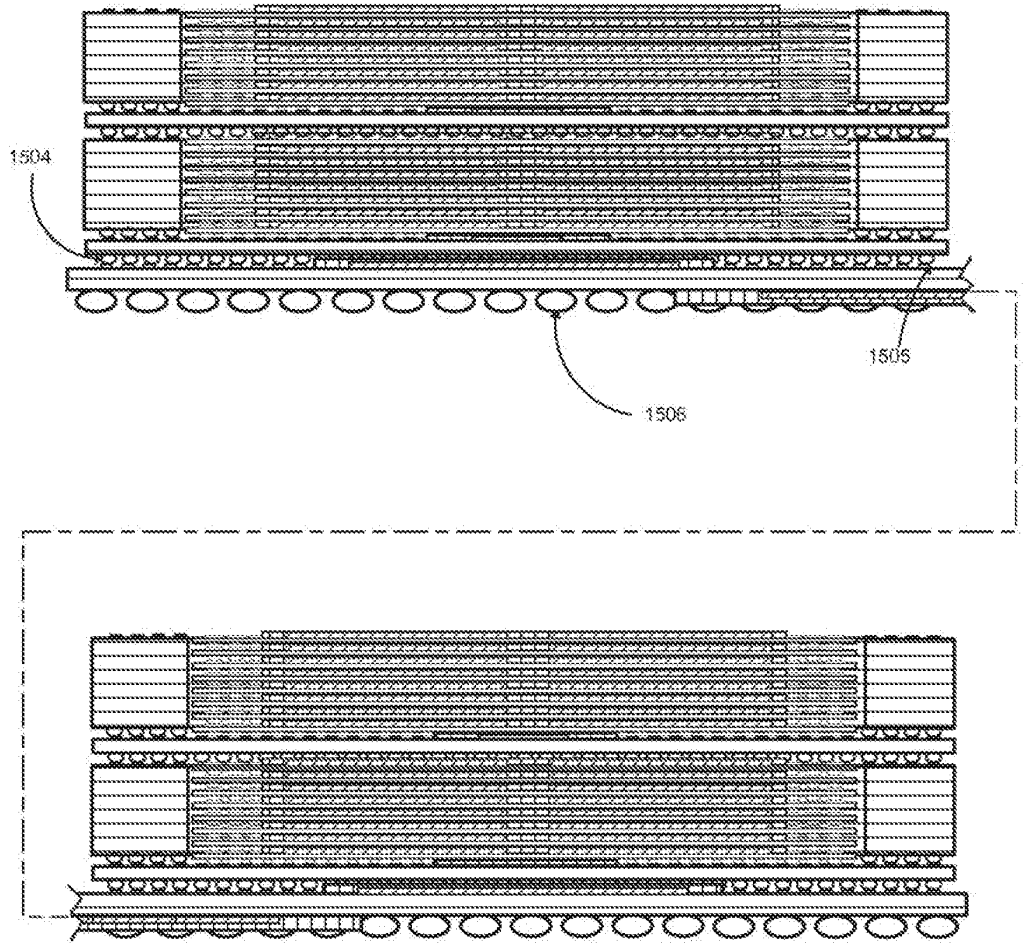


Figure 15b

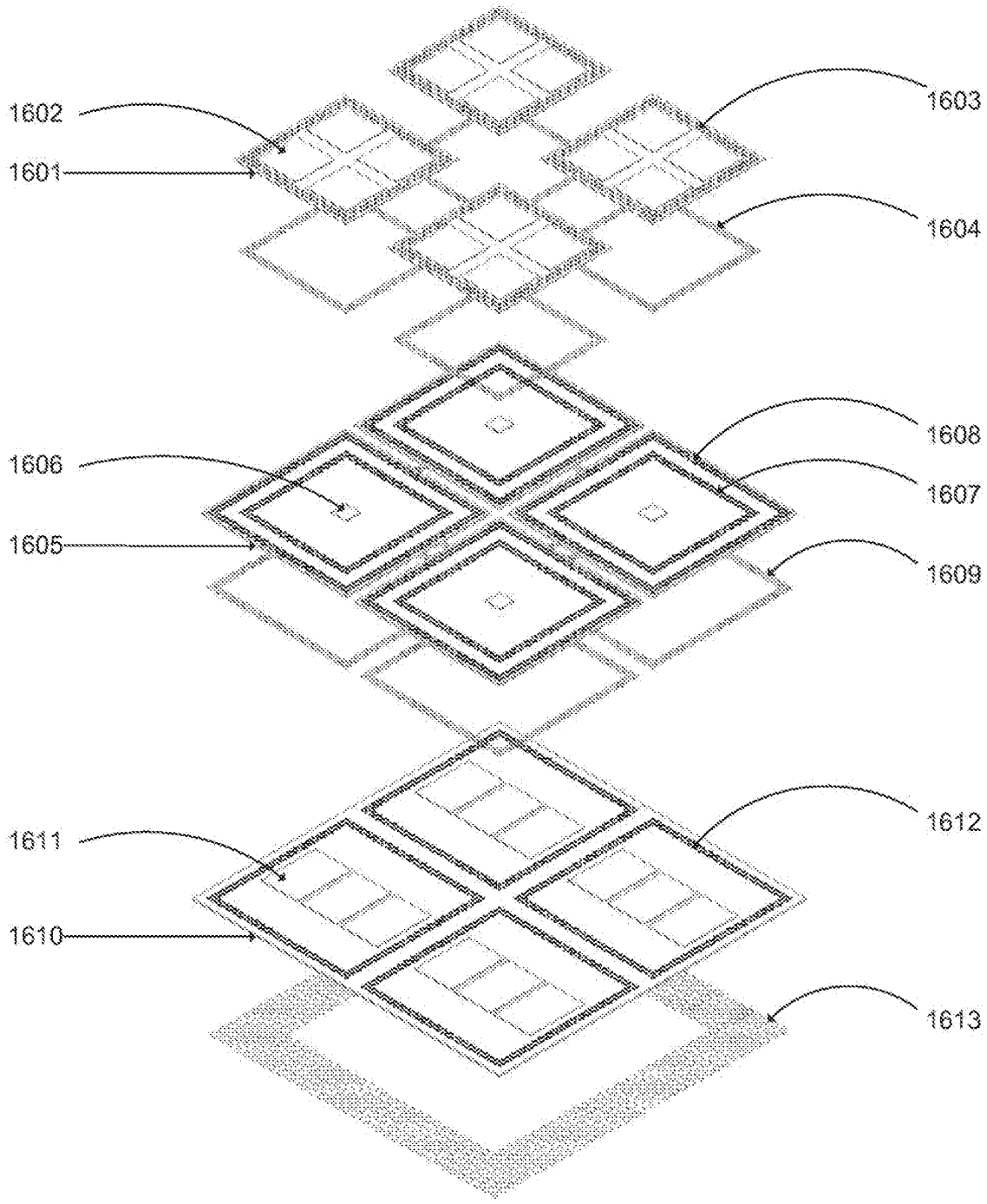

1602
1601
1603
1604
1606
1605
1608
1607
1609
1611
1610
1612
1613

Figure 16

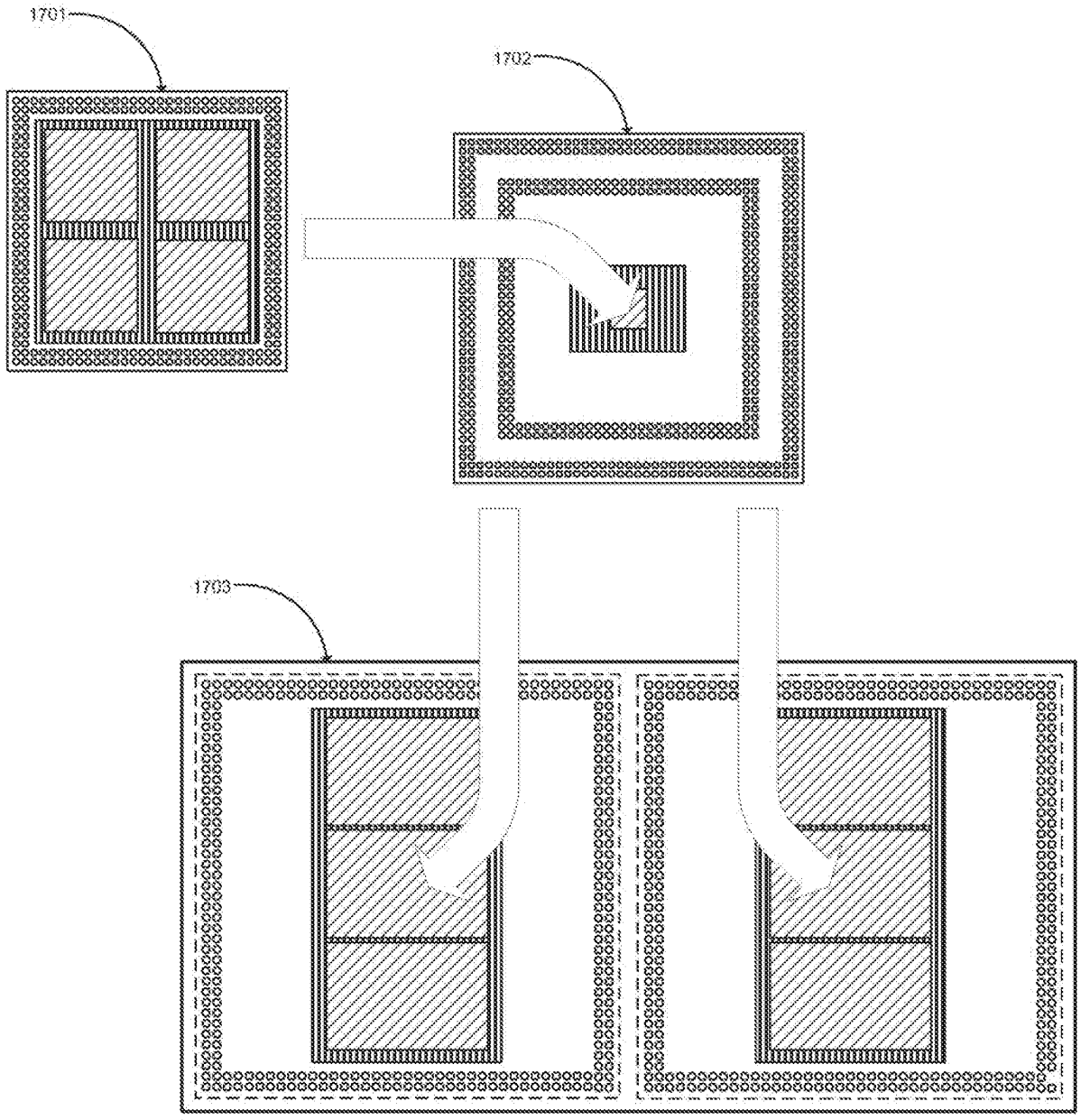


Figure 17a

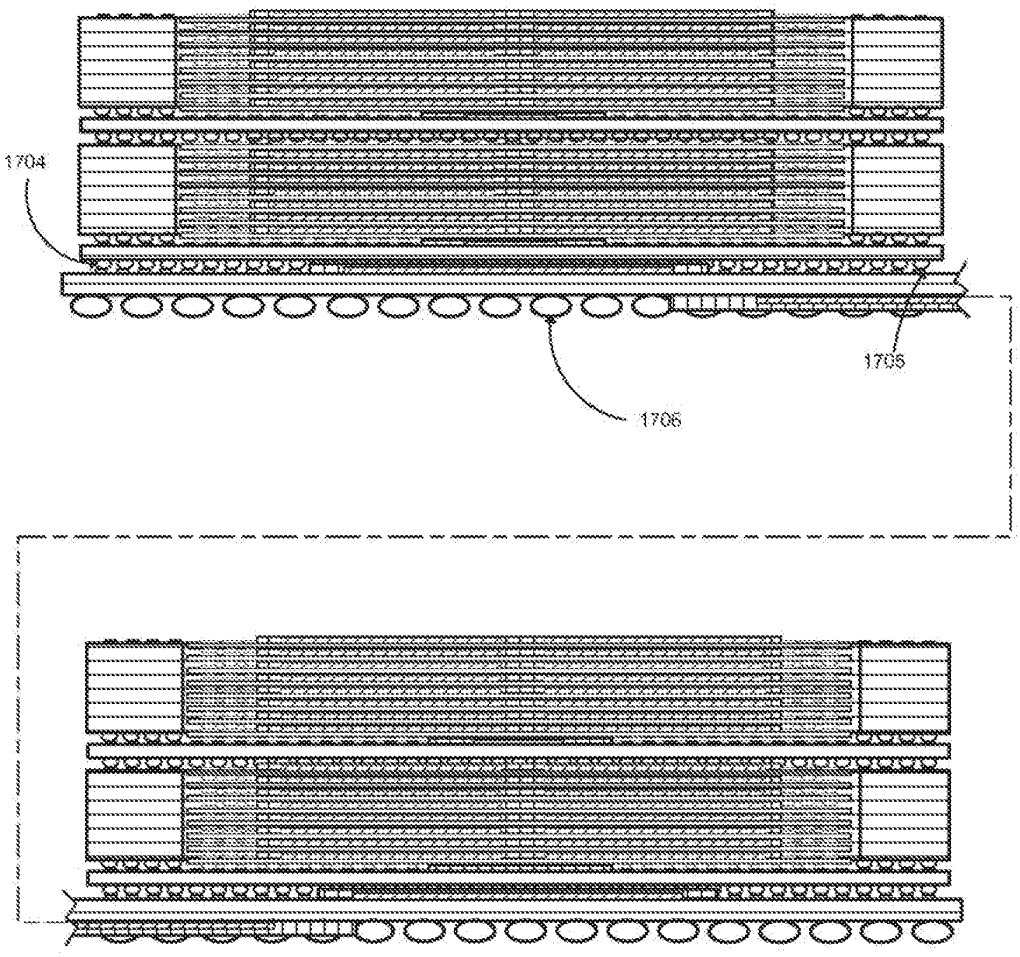


Figure 17b

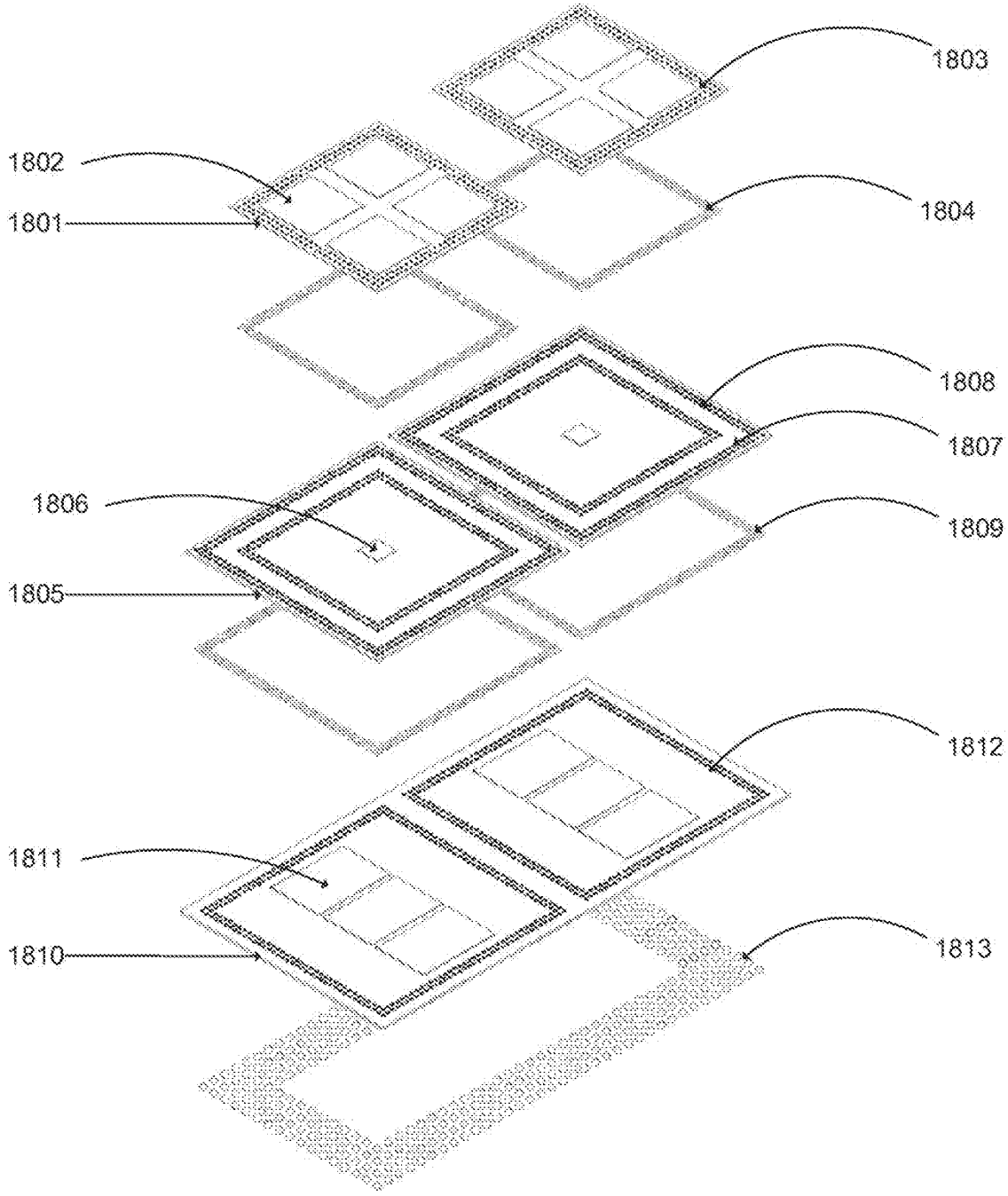

1803
1802
1801
1804
1808
1807
1806
1809
1805
1812
1811
1810
1813

Figure 18

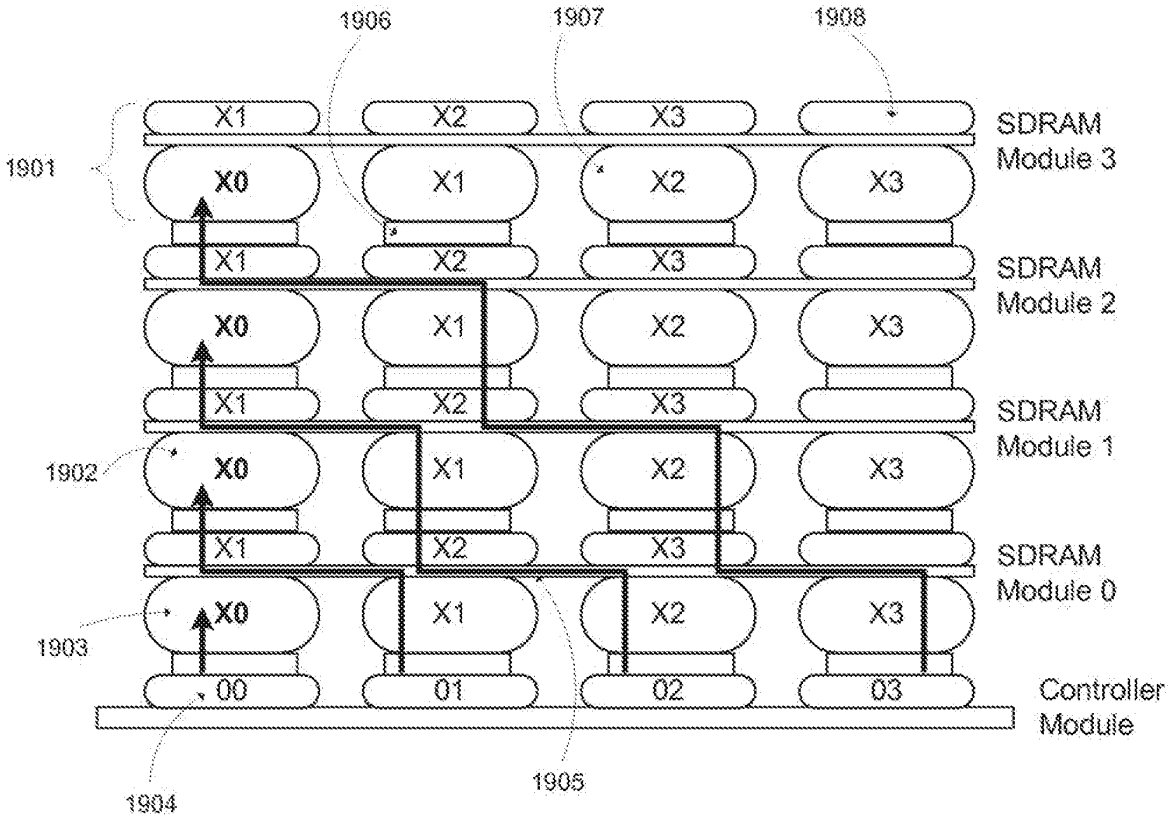

1906
1907
1908
1901
X1
X2
X3
X0
SDRAM Module 3
SDRAM Module 2
SDRAM Module 1
SDRAM Module 0
1902
1903
00
01
02
03
Controller Module
1904
1905

Figure 19

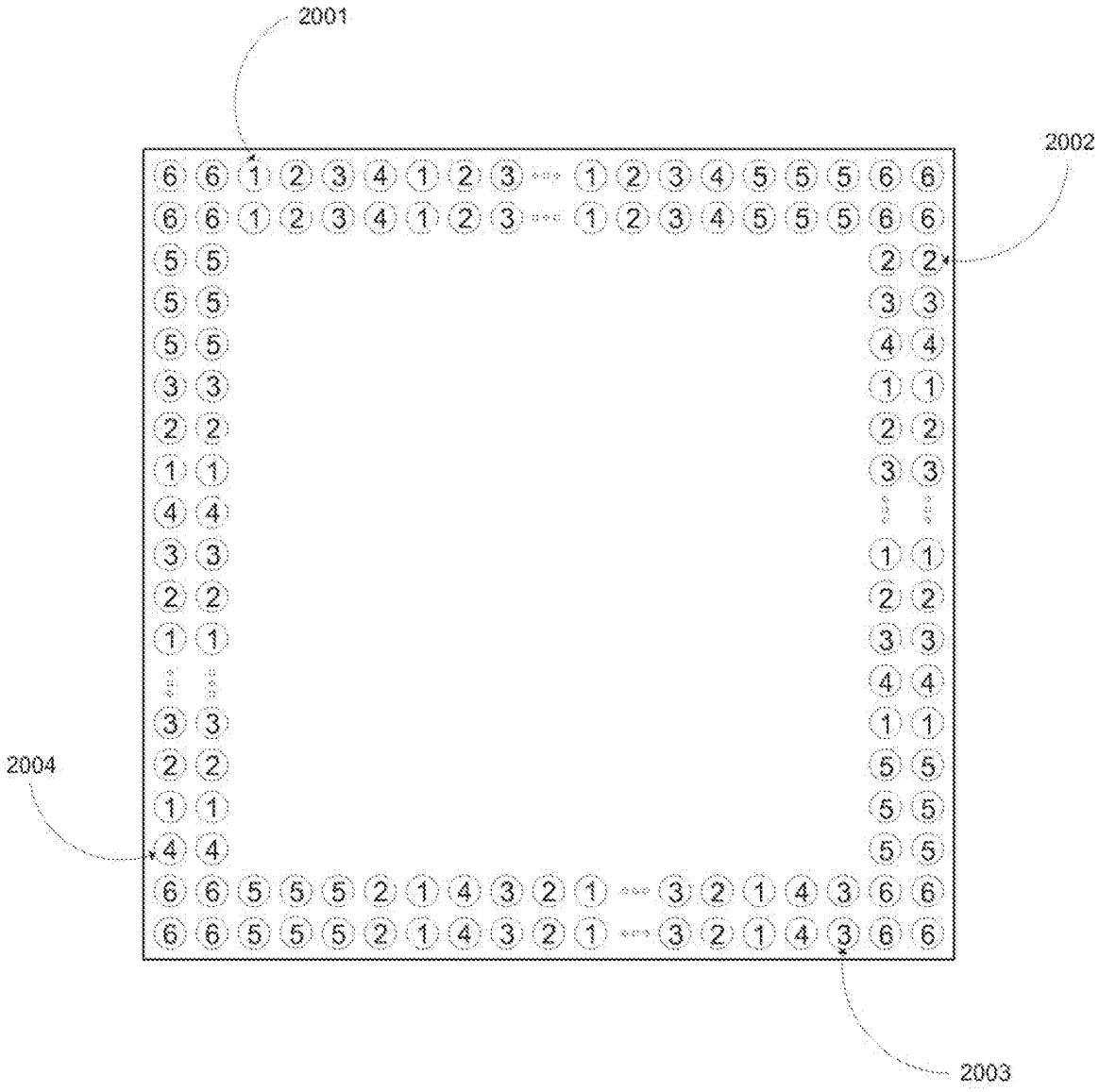


Figure 20a

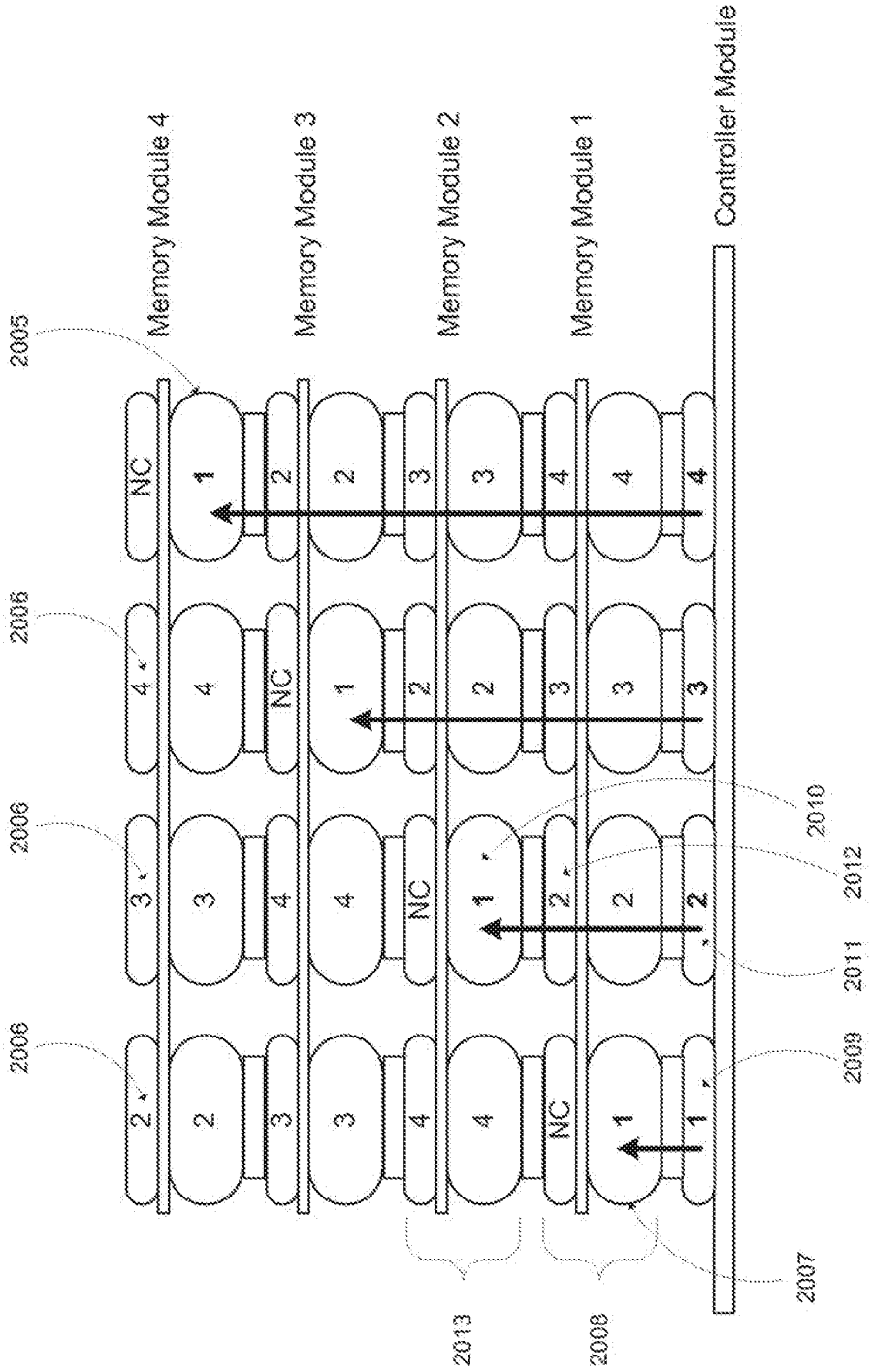

Memory Module 4
Memory Module 3
Memory Module 2
Memory Module 1
Controller Module
2005
2006
2006
2006
2010
2012
2011
2009
2007
2013
2008
NC
1
2
3
4
1'
2'
3'
4'

Figure 20a

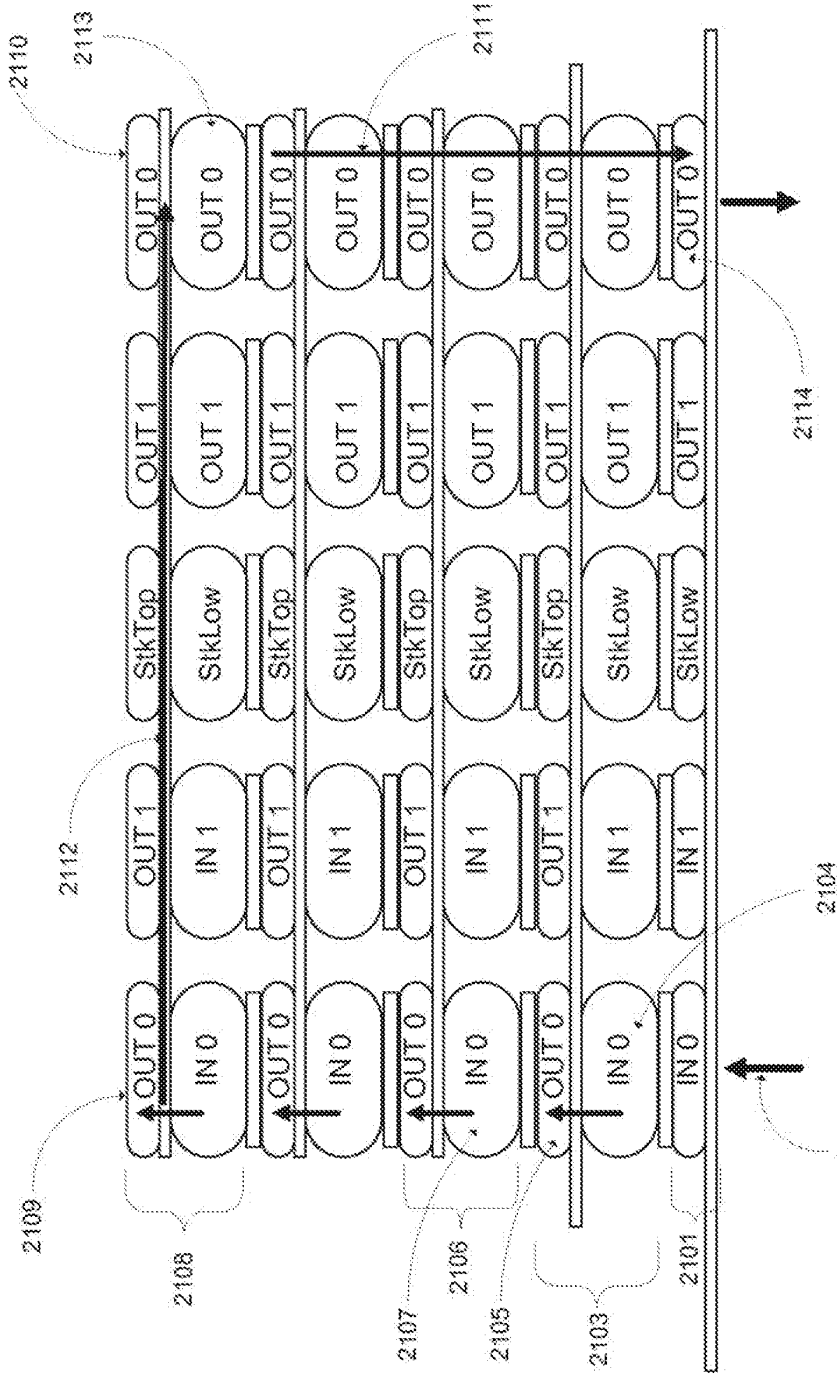

2110
2113
2111
2114
2112
2104
2109
2102
2108
2107
2106
2105
2103
2101
OUT 0
OUT 1
StkTop
StkLow
IN 1
IN 0

Figure 21a

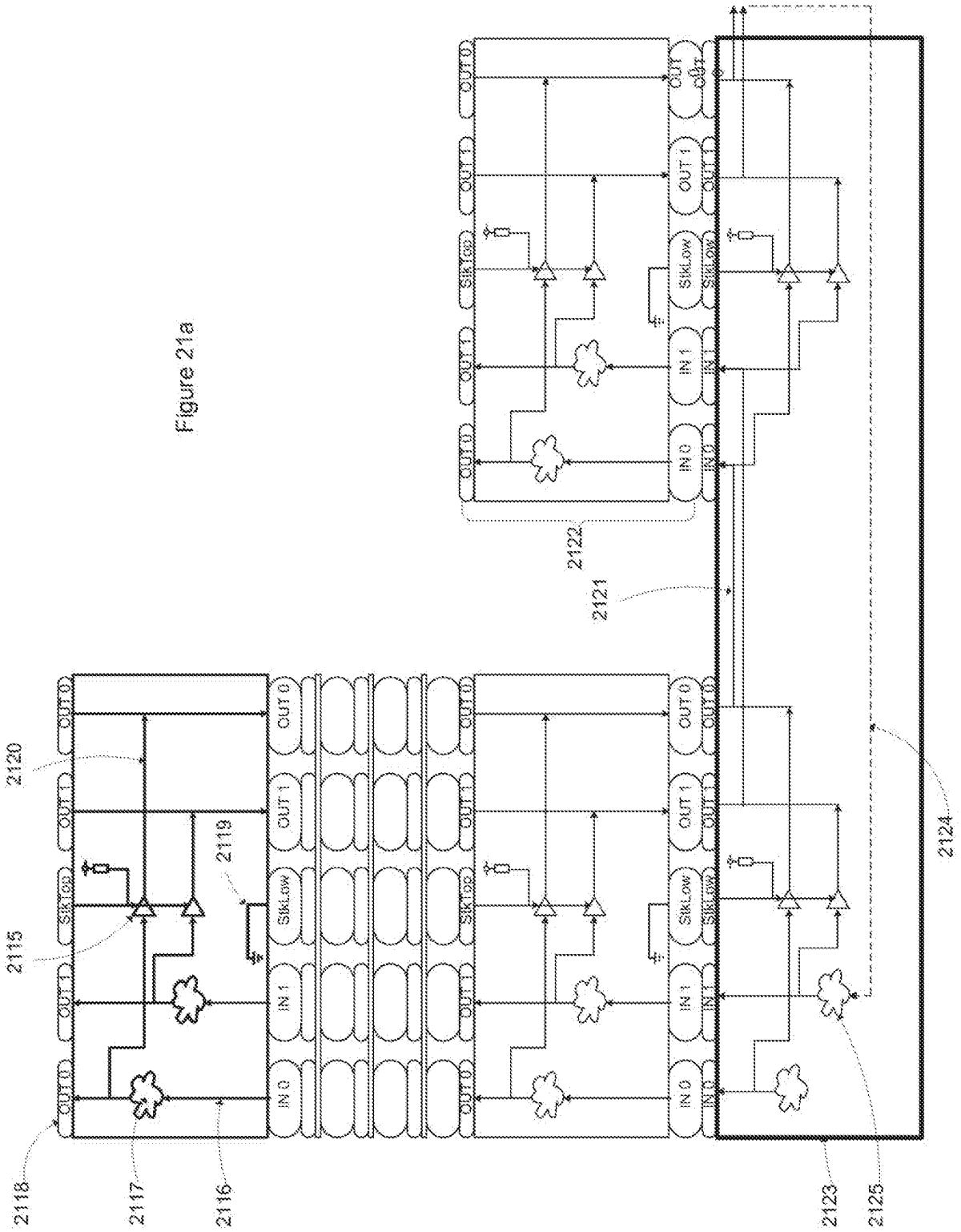

OUT 0
OUT 1
SIKLOW
SIKLOW
IN 1
IN 0
2118
2117
2116
2115
2120
2119
2122
2121
2123
2125
2124

Figure 21a

Attorney Docket#: 6005.011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: BRUCE et al.	Group Art Unit: 2892
Serial No.: 11/322,442	Examiner: ULLAH, Elias
Application Filing Date: 29 Dec 2005	
For: MULTIPLE CHIP MODULE AND PACKAGE AND PACKAGE STACKING METHOD FOR STORAGE DEVICE	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)

Dear Sir:

In conjunction with the Response to the Office Action, submitted on even date herewith, this is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and fee are as follows, indicated below:

Fees Paid:

___	One month (37 CFR 1.17(a)(1))	Fee (small entity: $65.000)	0.00
___	Two months (37 CFR 1.17(a)(2))	Fee (small entity: $245.00)	0.00
X	Three months (37 CFR 1.17(a)(3))	Fee (small entity: $555.00)	**Paid**

Entity Status:

X Applicant claims small entity status. (See 37 CFR 1.27)

Attorney Docket#: 6005.011

Payment Method:

X Payment by credit card through EFS-web is provided.

Authorization to Charge/Credit Fees and Constructive Petition

X The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number: 50-4068. Please treat this authorization to charge all required fees under 37 CFR 1.17 as a constructive petition for an extension of time in accordance with 37 CFR 1.136(a)(3).

The undersigned is the attorney of record. Registration #: 40,854

Sincerely,

Signature:	/Stephen R. Uriarte/	Date:	27 June 2008
Name:	Stephen R. Uriarte	Telephone:	408.244.2164x111

Uriarte Law
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San Jose, CA 95126
Tel: 408.244.2164 ext. 111
Fax: 408.716.2651
Email: mail@uriartelaw.com

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

EXCESS CLAIM FEE PAYMENT AND DEPOSIT ACCOUNT AUTHORIZATION

Dear Sir:

Authorization of Payment of Excess Claim Fees, If Required

It is believed that any additional fee required for new claims 27-31 has been previously paid since claims 1 through 13 were previously cancelled/withdrawn by the Applicants in a previously filed Response to Restriction requirement. In the event of any deficiency or overpayment involving excess claim fees or otherwise, the credit card account of the undersigned should be charged or credited in accordance to the instructions selected during filing of the attached Response and Amendment to Office Action filed on even date herewith via EFS-Web; or by using the following deposit account:

Account Number: 50-4068
Account Name: Uriarte Law

Respectfully submitted,
On behalf of the Applicants

Dated: 13 February 2009

/Stephen R. Uriarte/
Stephen R. Uriarte, Reg. No. 40,854

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Electronic Patent Application Fee Transmittal	
Application Number:	11322442
Filing Date:	29-Dec-2005
Title of Invention:	Multiple chip module and package stacking method for storage devices
First Named Inventor/Applicant Name:	Rey Bruce
Filer:	Stephen Radcliff Uriarte
Attorney Docket Number:	6005.011
Filed as Small Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 3 months with $0 paid	2253	1	555	555

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	555

Electronic Acknowledgement Receipt	
EFS ID:	4795792
Application Number:	11322442
International Application Number:	
Confirmation Number:	5045
Title of Invention:	Multiple chip module and package stacking method for storage devices
First Named Inventor/Applicant Name:	Rey Bruce
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.011
Receipt Date:	13-FEB-2009
Filing Date:	29-DEC-2005
Time Stamp:	20:48:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$555
RAM confirmation Number	4321
Deposit Account	504068
Authorized User	URIARTE,STEPHEN R.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:	ATTACHMENT "E"				
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		6005_011_1stRsp2OA_20090213B.pdf	175877	yes	25
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	15	
	Applicant Arguments/Remarks Made in an Amendment		16	25	
Warnings:					
Information:					
2	Specification	6005_011_SubstitueSpecMarked_20090213.pdf	189782	no	26
Warnings:					
Information:					
3	Specification	6005_011_SubstitueSpecCLEAN_20090213.pdf	185457	no	25
Warnings:					
Information:					
4	Drawings-only black and white line drawings	6005_011_FIGS1_11_rplcmnt_20090213.pdf	510087	no	13
Warnings:					
Information:					
5	Drawings-only black and white line drawings	6005_011_FIGS12a_17b_rplcmnt_20090213.pdf	608961	no	9
Warnings:					
Information:					
6	Drawings-only black and white line drawings	6005_011_FIGS18_21b_rplcmnt_20090130.pdf	141127	no	6
Warnings:					
Information:					
7	Extension of Time	6005_011_PetitionExtTime_20090213emb.pdf	29322	no	2
Warnings:					
Information:					

ATTACHMENT "E"

8	Refund Request	6005_011_Excess_Claims_20090213_wOff.pdf	75884	no	1
Warnings:					
Information:					
9	Fee Worksheet (PTO-06)	fee-info.pdf	29793	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	1946290	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

DocCode - SCORE

SCORE Placeholder Sheet for IFW Content

Application Number: 11322442 Document Date: 2/13/2009

The presence of this form in the IFW record indicates that the following document type was received in paper and is scanned and stored in the SCORE database.

- Design Drawings

The original paper documents are in the physical artifact folder. The original documents are scanned using a higher quality capture process and stored in SCORE. A copy of these documents are scanned in IFW using the standard quality scanning process. Defects visible in both IFW and SCORE are indicative of defects in the original paper documents.

To access the documents in the SCORE database, refer to instructions developed by SIRA.

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- Examiners may access SCORE content via the eDAN interface.
- Other USPTO employees can bookmark the current SCORE URL (http://es/ScoreAccessWeb/).
- External customers may access SCORE content via the Public and Private PAIR interfaces.

Form Revision Date: October 12, 2006

PTO/SB/06 (07-06)
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PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/322,442	12/29/2005	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☒		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	02/13/2009	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 18	Minus	** 26	= 0	X $26 =	0	OR	X $ =	
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $110 =	0	OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE	

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/CHRISTINE MOLLISH/

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PTO/SB/44 (09-07)
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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,826,243

APPLICATION NO.: 11/322,442

ISSUE DATE : 11-02-2010

INVENTOR(S) : Rey Bruce, Ricardo Bruce, Patrick Digamon Bugayong, Joel Alonzo Baylon

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the specification
Column 3, Line 39, replace "to be able to connect" with --for creating--;
Column 3, Line 39, replace "chain route from" with --chain route through--;
Column 3, Line 40, after "in a stack" insert --by connecting a set of serial chain connections,--;
Column 3, Line 40, replace "to an example" with --to another example--;
Column 9, Line 3, before "The controller" insert --An active pad may be also referred to herein as an "active port."--;

Column 9, Line 3, replace "is connected" with --is ultimately connected--;
Column 9, Line 4, delete "SDRAM module 0's";
Column 9, Line 4, replace "ball 1903, pad 01" with --ball 1903 of SDRAM module 0, active pad 01--;
Column 9, Line 4, after "pad 01" insert --is connected--;
Column 9, Lines 4-5, replace "SDRAM module 1's X0 ball 1902" with --X0 ball 1902 of SDRAM module 1--;
Column 9, Line 5, replace "The X0 balls" with --These X0 balls--;
Column 9, Line 6, replace "for the SDRAM modules." with --for these SDRAM modules. Thus, as illustrataed in Figure 19, there is one active ball, such as X0, ultimately coupled to one active pad per module.--;

Column 9, Line 6, before "All SDRAM modules" insert paragraph break;
Column 9, Line 7, replace "identical which" with --identical, and in the example shown in FIG. 19,--;
Column 9, Line 7, replace "include the connections as follows:" with --include the following:--;
Column 9, Line 7, replace "X1 ball" with --an X1 passive ball--;
Column 9, Line 8, replace "X1 pad" with --an X1 passive pad--;
Column 9, Line 8, replace "X2 ball to X2 pad" with --an X2 passive ball to X2 passive pad--;

MAILING ADDRESS OF SENDER (Please do not use Customer Number below):
Joseph Lally, Jackson Walker LLP, 100 Congress Ave, Suite 1100, Austin TX 78701

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,826,243

APPLICATION NO.: 11/322,442

ISSUE DATE : 11-02-2010

INVENTOR(S) : Rey Bruce, Ricardo Bruce, Patrick Digamon Bugayong, Joel Alonzo Baylon

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 9, Line 8, after "and so on." insert --The connection between a passive ball on one surace of a SDRAM module and a psssive pad on another surface of the same SDRAM module, such as the X1 passive ball and X1 passive pad connection in FIG. 19, is named "passive port", as as passive ports 1909 illustrated in FIG. 19.--;

Column 9, Line 12, after "module in the stack." insert --Thus, an active signal applied at an active pad, such as active pad 02, shown with reference number 1904 on controller module 1910, is routed through at least one passive port connecting a passive ball and passive pad, such as the passive ports 1905 connecting passive ball X2 to passive pad X2 and passive ball X1 to passive pad X2, respectively, so that this active signal eventually reaches an active ball, such as X0 ball SDRAM Module 2, in Figure 19.--;

Column 9, Line 16, after "the repeating pattern." insert --For example in Figure 19, an X1 passive ball is connected to an X1 passive pad, X2 passive ball to X2 passive pad, etc.--;

Column 9, Lines 16-17, replace "The importance is the approach using" with --By using--;
Column 9, Line 19, delete "also";
Column 9, Line 19, replace "in other embodiment" with --in alternative embodiments--;
Column 9, Lines 19-20, replace "invention, e.g. using" with --invention. For example, an alternative embodiment may include using--;

Column 9, Lines 21-22, replace "The example embodiment does not limit" with --This alternative embodiment is not intended to limit--;

MAILING ADDRESS OF SENDER (Please do not use Customer Number below):

Joseph Lally, Jackson Walker LLP, 100 Congress Ave, Suite 1100, Austin TX 78701

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PATENT NO. : 7,826,243

APPLICATION NO.: 11/322,442

ISSUE DATE : 11-02-2010

INVENTOR(S) : Rey Bruce, Ricardo Bruce, Patrick Digamon Bugayong, Joel Alonzo Baylon

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 9, line 22, replace "the present invention." with --the present invention in any way.--;
Column 9, line 67, after "module 2103." insert --The modules, including base module 2103, stack modules 2106 and 2130, and an end module, such as top module 2108, each have a ball and a pad that are coupled together by a serial chain circuit. For example, base module 2103 includes a serial chain circuit 2127 that couples IN ball 2104 with OUT pad 2105, and a serial chain circuit 2136 that couples OUT pad 1237 with OUT ball 2138; module 2106 includes a serial chain circuit 2128 that couples IN ball 2107 with OUT pad 2129, and a serial chain circuit 2139 that couples OUT pad 2140 with OUT ball 2141; module 2130 includes a serial chain circuit 2131 that couples IN ball 2132 with OUT pad 2133, and a serial chain circuit 2142 that couples OUT pad ball 2143 with OUT ball 2144; and top module 2108 incudes a serial chain circuit 2134 that couples IN ball 2135 with OUT pad 2109 and a serial chain circuit 2145 that couples OUT pad 2110 with OUT ball 2113.--";

Column 9, Line 67, replace "The base module's" with --Thus, the base module's--;
Column 10, Line 2, after "so on." insert --A signal route that includes a serial chain circuit coupling an ball and pad is herein after referred to as a "serial chain connection", and at least two serial chain connections connected in series are herein after referred to as a "serial chain route", such as serial chain route 2146 or 2111.--;

Column 10, Line 4, replace "another pad 2110 which" with --another pad, such as OUT pad 2110, which--;
Column 10, Line 5, replace "ball 2113 underneath." with --ball underneath, such as OUT ball 2113.--;
Column 10, Line 6, replace "passes through the pads and balls 2111 of the" with --passes through another set of serial chain connections that comprise another serial chain route, such as serial chain route 2111 for the--;

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,826,243

APPLICATION NO.: 11/322,442

ISSUE DATE : 11-02-2010

INVENTOR(S) : Rey Bruce, Ricardo Bruce, Patrick Digamon Bugayong, Joel Alonzo Baylon

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 10, Line 8, after "access." insert --A serial chain connection includes a serial chain input and a serial chain output. A serial chain input is disposed to receive a signal, while a serial chain output is disposed to provide the signal. For example in Figure 21a, IN balls 2014, 2107, 2132, and 2135, and OUT pads 2110, 2143, and 2140 are serial chain inputs, respectively, OUT pads 2105, 2129, 2133, and 2109, and OUT balls 2113, 2144, 2141, and 2138 are serial chain outputs, respectively. At least one of the balls and pads that are coupled to their respective chain circuit may be in the form of a passive ball and passive pad, respectively, since an active signal, such as signal 2102, applied at active pad 2101, can be routed through a series of serial chain circuits that couple respective balls and pads. In effect, each of these serial chain circuits functions as a passive port. A serial chain circuit, however, can also terminate a serial chain route, such as serial chain route 2146, and branching or routing this serial chain route to another pad that functions as a serial chain input of another serial chain route, such as serial chain route 2111, as described further below.--;

Column 10, Line 8, replace "How the top module terminates the serial" with --"Regarding the top module, the serial"--;

Column 10, Line 9, after "chain" insert --termination--;
Column 10, Line 9, replace "branches them out" with --branching--;
Column 10, Line 10, after "have" insert --a control circuit that includes--;
Column 10, Line 33, replace "diver" with --driver--.

In the Drawings
Please insert Figure 5b by replacing Drawing Sheet 6 of 28 with Replacement Sheet 6 of 28 attached hereto.

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Electronic Acknowledgement Receipt	
EFS ID:	30497980
Application Number:	11322442
International Application Number:	
Confirmation Number:	5045
Title of Invention:	MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES
First Named Inventor/Applicant Name:	Rey Bruce
Customer Number:	64180
Filer:	Joseph Patrick Lally
Filer Authorized By:	
Attorney Docket Number:	6005.011
Receipt Date:	27-SEP-2017
Filing Date:	29-DEC-2005
Time Stamp:	21:08:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		CofC_submission_part_1.pdf	15715749 c23c85713b08a2e795bd985b74d3403317e118ac	yes	120

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Request for Certificate of Correction	1	4
	Drawings-only black and white line drawings	5	5
	Miscellaneous Incoming Letter	6	120

Warnings:					
Information:					
2	Miscellaneous Incoming Letter	CofC_submission_part_2.pdf	17186512 93784b71e359f1460831a338e8bf9aa3d771087b	no	114
Warnings:					
Information:					
3	Request for Certificate of Correction	SB44.pdf	145009 92c4a5ce48e3553ef3d91534c7fa888bb8edcccb	no	4
Warnings:					
Information:					
		Total Files Size (in bytes):	33047270		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/81A (12-08)
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PATENT - POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS

Patent Number	7826243
Issue Date	11/02/2010
First Named Inventor	Rey Bruce
Title	MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES
Attorney Docket No.	150962.00001

I hereby revoke all previous powers of attorney given in the above-identified patent.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the Customer Number identified in the box at right as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith: 67942

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified patent to:

▩ The address associated with the above-identified Customer Number.

OR

☐ The address associated with the Customer Number identified in the box at right:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the:

☐ inventor, having ownership of the patent.

OR

☒ Patent owner.

Statement under 37 CFR 3.73(c) (Form PTO/SB/96) submitted herewith or filed on _____

SIGNATURE of Inventor or Patent Owner

Signature		Date	8-26-2017
Name	Boris M. Lagerman	Telephone	
Title and Company	Manager, BITMICRO LLC		

NOTE: Signatures of all the inventors or patent owners of the entire interest or their representative(s) are required. If more than one signature is required, submit multiple forms, check the box below, and identify the total number of forms submitted in the blank below.

☐ A total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 15 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Bitmicro LLC

Application No./Patent No.: 7826243 Filed/Issue Date: 11/02/2010

Titled: MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES

Bitmicro LLC, a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. [✓] The assignee of the entire right, title, and interest.

2. [ ] An assignee of less than the entire right, title, and interest (check applicable box):

   [ ] The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   [ ] There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. [ ] The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. [ ] The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. [ ] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. [✓] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

   1. From: Inventors To: Bitmicro Networks, Inc.

      The document was recorded in the United States Patent and Trademark Office at Reel 018594, Frame 0240, or for which a copy thereof is attached.

   2. From: Bitmicro Networks, Inc. To: Bitmicro, LLC

      The document was recorded in the United States Patent and Trademark Office at Reel 043536, Frame 0407, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Bruce K. Lagerman — Signature

9-26-2017 — Date

Bruce K. Lagerman — Printed or Typed Name

Manager — Title or Registration Number

[Page 2 of 2]

Electronic Acknowledgement Receipt	
EFS ID:	30474233
Application Number:	11322442
International Application Number:	
Confirmation Number:	5045
Title of Invention:	MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES
First Named Inventor/Applicant Name:	Rey Bruce
Customer Number:	64180
Filer:	Raman N. Dewan/Mindy Mayer
Filer Authorized By:	Raman N. Dewan
Attorney Docket Number:	6005.011
Receipt Date:	26-SEP-2017
Filing Date:	29-DEC-2005
Time Stamp:	12:53:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		7826243_POA.pdf	3802217 b59f6b4c79141d523a6f990ea02bcd367a75ea0e	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Power of Attorney	1	1
	Assignee showing of ownership per 37 CFR 3.73	2	3
Warnings:			
Information:			
	Total Files Size (in bytes):	3802217	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT4586333

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
BITMICRO NETWORKS, INC.	06/30/2017

RECEIVING PARTY DATA

Name:	BITMICRO LLC
Street Address:	1620 N. WACCAMAW DRIVE
Internal Address:	SUITE 109
City:	MURRELLS INLET
State/Country:	SOUTH CAROLINA
Postal Code:	29576

PROPERTY NUMBERS Total: 34

Property Type	Number
Patent Number:	6496939
Patent Number:	9372755
Patent Number:	6970890
Patent Number:	7729370
Patent Number:	7826243
Patent Number:	8093103
Patent Number:	6317330
Patent Number:	9423457
Patent Number:	9552848
Patent Number:	6744635
Patent Number:	7716389
Patent Number:	8165301
Patent Number:	7620748
Patent Number:	9400617
Patent Number:	9672178
Patent Number:	9043669
Patent Number:	7613876
Patent Number:	8032700
Patent Number:	9430386

Property Type	Number
Patent Number:	9734067
Patent Number:	6000006
Patent Number:	5822251
Patent Number:	9099187
Patent Number:	8560804
Patent Number:	9484103
Patent Number:	8010740
Patent Number:	7506098
Patent Number:	8447908
Patent Number:	8788725
Application Number:	14297628
Patent Number:	6529416
Patent Number:	5956743
Patent Number:	9135190
Patent Number:	6757845

CORRESPONDENCE DATA

Fax Number: (512)391-2173

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 512.236.2023

Email: rdewanipdocket@jw.com

Correspondent Name: JACKSON WALKER L.L.P.

Address Line 1: 100 CONGRESS AVENUE

Address Line 2: SUITE 1100

Address Line 4: AUSTIN, TEXAS 78701

NAME OF SUBMITTER:	HEATHER BUCEK
SIGNATURE:	/heather bucek/
DATE SIGNED:	09/08/2017
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 8

source=BitMicro Recordable Assigment#page1.tif
source=BitMicro Recordable Assigment#page2.tif
source=BitMicro Recordable Assigment#page3.tif
source=BitMicro Recordable Assigment#page4.tif
source=BitMicro Recordable Assigment#page5.tif
source=BitMicro Recordable Assigment#page6.tif
source=BitMicro Recordable Assigment#page7.tif
source=BitMicro Recordable Assigment#page8.tif

RECORDABLE ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, **BiTMICRO Networks, Inc.,** a California company having offices at 47929 Fremont Blvd., Fremont, CA 94538 (***"Assignor"***) and **BiTMICRO LLC,** a Delaware Company having offices at 1620 N. Waccamaw Drive, Suite 109, Murrells Inlet, SC 29576 does hereby sell, assign, transfer, and convey unto (hereafter "***Assignee***") all its right, title, and interest in and to any and all of the following (collectively, the ***"Patent Rights"***):

(a) the patent applications and patents listed in the table below and any issued patent or patent application that directly or indirectly claims or is amended to claim priority to any of the above, in whole or in part (the "***Patents***");

(b) to the extent not included in Section (a) above, all issued patents, rights to inventions and pending and future applications for patents under U.S. law or regulation or any foreign country with respect to the patentable inventions from which such Patents arise, including without limitation, utility patents, utility models, design patents, invention certificates, provisional, reissues, reexaminations, extensions, continuations, continuations-in-part, continuing prosecution applications, requests for continuing examinations, divisionals, renewals, and registrations in all countries of the world, as well as any patents and patent applications to which any of the Patents or the foregoing directly or indirectly claim priority, in whole or in part;

(c) all related patent filing and prosecution documents;

(d) rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections, or other governmental grants or issuances of any type related to any of the Patents and the inventions, invention disclosures, and discoveries therein;

(e) all inventions and discoveries described in any of the Patents or subject matter capable of being reduced to a patent claim in any of the Patents based on the specification of any of the Patents;

(f) priority rights in any and all patent filings available from and/or through the Patents; and

(g) causes of action (whether known or unknown or whether currently pending, filed, or otherwise) and other enforcement rights under, or on account of any of the Patents or of any patent that issues from any of the Patents, including, without limitation, all causes of action and other enforcement rights for (1) damages, (2) injunctive relief, and (3) any other remedies of any kind for past, current and future infringement and all of the proceeds from the foregoing, that are accrued and unpaid or that are hereafter accruing;

(h) rights to collect royalties or other payments under or on account of any of the Patents and/or any of the foregoing categories (a) through (g); and

(i) rights of cooperation assigned or granted by any third party under or on account of any of the Patents and/or any of the foregoing categories (a) through (h).

Assignor represents, warrants and covenants that:

Assignor has the full power and authority, and has obtained all third-party consents, approvals and/or other authorizations required to enter into this Agreement and to carry out its obligations hereunder, including the assignment of the Patent Rights to Assignee.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

The terms and conditions of this Assignment of Patent Rights will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed at Fremont, CA on 30 June 2017.

Assignor:

BITMICRO Networks, Inc.

By: _____

Name: Stephen R. Ungaretti

Title: President & Chief Executive Officer

STATE OF CALIFORNIA)
) ss.
COUNTY OF Alameda)

On June 30th, 2017, before me, DAPINDER BHAGRATH, Notary Public in and for said State, personally appeared STEPHEN R. UNGARETTI, personally known to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed to the within instrument and acknowledged to me that he/she executed the same in his/her authorized capacity, and that by his/her signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

WITNESS my hand and official seal.

Signature _____ (Seal)

DAPINDER BHAGRATH
COMM. #2176448
NOTARY PUBLIC - CALIFORNIA
ALAMEDA COUNTY
My Comm. Exp. Jan. 18, 2021

Group No. 1: PowerGuard and Data Recovery				NVM-only. (Volatile RAM + NVM) Solutions
Group No.	Country	Patent Number	Issue/Priority	Title
1	(A) US	6496939**	2002-12-17/ 1999-09-21	Method and System for Controlling data in a Computer System in the event of a power failure
1	(A) Taiwan	189445	2004-02-20 / 1999-09-21	Method and System for Controlling data in a Computer System
1	(A) Canada	2,388,496	2002-12-17/ 1999-09-21	Method and System for Controlling data in a Computer System
1	(A) EP	App. No: 00961417.3	Filed 2002-04-18 / Priority 1999-09-21	Method and System for Controlling data in a Computer System
1	(B) US	9,372,755	2106-06-21/ 2011-10-05	Adaptive power cycle sequences for data recovery
1	(B) US	App. No. 15/176,156	Filed 2016-06-08 / Priority 2011-10-05	Adaptive power cycle sequences for data recovery
1	US	6,970,890	2005-11-29/ 2000-12-20	Method and apparatus for data recovery

(A & B) Identifies Different Priority Families; All Others Are Single Patents

Group No. 2: Networking+ Flash				Networked-attached Storage Devices (Filesystem / Block IO)
Group No.	Country	Patent Number	Issue/Priority	
2	US	6981070**	2005-12-27/ 2000-07-12 (+552 PTA)	Network storage device having solid-state non-volatile memory
2	US	7,729,370	2010-06-01/ 2005-08-19 (+861 PTA)	Apparatus for networking devices having fibre channel node functionality

Group No. 3: Casings, PCB, and ASIC				SSD/Acceleration Devices/ASIC design
Group No.	Country	Patent Number	Issue/Priority	
3	(C) US	7826243**	2010-11-2 / 2005-12-29 (+747 PTA)	Multiple chip module and package stacking for storage devices
3	(C) US	8093103	2012-1-10 / 2005-12-29	Multiple chip module and package stacking for storage devices
3	(C) Taiwan	I332701853	2010-11-1 / 2005-12-29	Multiple Chip Module and Package Stacking Method For Storage Devices
3	(C) Korea	10-1391068	2014-4-24 / 2005-12-29	Multiple Chip Module and Package Stacking Method For Storage Devices
3	(C) Japan	5,745,730	2015-04-27 / 2005-12-29	Multiple Chip Module and Package Stacking Method For Storage Devices
3	(C) Japan	5,859,181	2015-12-08 / 2005-12-29	Multiple Chip Module and Package Stacking Method For Storage Devices
3	(C) China	1013753918	2010-12-28 / 2005-12-29	Multiple Chip Module and Package Stacking Method For Storage Devices
3	(D) US	6317330	2001-11-13 / 2000-2-15	Printed circuit board assembly
3	(D) China	CN 1423917	2006-02-08 / 2000-2-15	Printed circuit board assembly
3	(D) Israel	151278	2007-06-01 / 2000-2-15	Printed circuit board assembly
3	(D) Taiwan	I228211	2005-02-21 / 2000-2-15	Printed circuit board assembly
3	(D) Japan	4,397,143	2009-10-30 / 2000-2-15	Printed circuit board assembly
3	(E) US	9,423,457	2016-8-23 / 2013-3-14 (+102 PTA)	Self-Test Solution For Delay Locked Loops
3	(E) US	App. No. 15/232,801	Filed 2016-08-09 / priority 2013-3-14	Self-Test Solution For Delay Locked Loops
3	(F) US	8665601	2014-3-4 / 2009-9-4 (+500 PTA)	Solid state drive with improved enclosure assembly
3	(F) US	9,552,848	Filed 2014--2-18 / priority 2010-9-4	Solid state drive with improved enclosure assembly

3	(F) US	App. No. 15/414,504	Filed 2017-1-24 / priority 2010-9-4	Solid state drive with improved enclosure assembly
3	US	6,744,635	2004-6-1 / 2000-2-15	Removable Visual Indication Structure For A Printed Circuit Board

(C thru F) Identifies Different Priority Families; All Others Are Single Patents

Group No. 4: DMA and Security				Performance, Hardware Acceleration, Security for NVM and Non-NVM
Group No.	Country	Patent Number	Issue/Priority	
4	US	7716389	2010-05-11 / 2006-03-17	Direct memory access controller with encryption and decryption for non-blocking high bandwidth I/O transactions
4	US	8165301	2012-04-24 / 2006-04-04	Input-output device and storage controller handshake protocol using key exchange for data security
4	US	7620748	2009-11-17 / 2006-04-06	Hardware assisted non-volatile memory-to-input/output direct memory access (DMA) transfer
4	(G) US	9400617	2016-07-26 / 2013-03-15	Hardware-assisted DMA transfer with dependency table configured to permit-in parallel-data drain from cache without processor intervention when filled or drained
4	(G) US	App. No. 15/217,947	Filed 2016-07-22 / Priority 2013-03-15	Hardware-Assisted DMA Transfer with Dependency
4	(G) US	9672178	2017-06-06 / Priority 2013-03-15	Bit-Mapped Dependency Table
4	(G) US	App. No. 15/603,434	Filed 2017-05-23 / Priority 2013-03-15	Bit-Mapped Dependency Table

(G) Identifies A Priority Family; All Others Are Single Patents

Group No. 5: Flash-and ECC related Patents				SSDs / FlashDevices (Flash, Profile, ECC, Firmware)
Group No.	Country	Patent Number	Issue/Priority	
5	(H) US	9043669++	2015-05-26 / 2012-05-18	Distributed ECC engine for storage media
5	(H) US	App. No. 14/708,246	Filed 2015-05-09 / Priority 2012-05-18	Storage System With Distributed ECC Capability
5	(I) US	8959307++	2015-02-17 / 2007-11-16	Reduced latency memory read transactions in storage devices

5	(I) US	App. No. 14/616,700	Filed 2015-02-02 / Priority 2007-11-16	Memory Transaction With Reduced Latency
5	(I) US	App. No. 14/866,946	Filed 2015-09-26 / Priority 2007-11-16	Reduced latency memory read transactions in storage devices
5	(I) US	App. No. 15/268,533	Filed 2016-09-16/ Priority 2007-11-16	Memory Interface With An Expandable Architecture That Provides Reduced Latency
5	(I) US	App. No. 15/268,536	Filed 2016-09-16/ Priority 2007-11-16	Multi-Dimensional Memory
5	(I) US	App. No. 15/368,598	Filed 2016-12-03 / Priority 2006-11-16	Computer Storage System With Reduced Latency
5	(J) US	7613876++	2009-11-03 / 2006-06-08	HYBRID MULTI-TIERED CACHING STORAGE SYSTEM
5	(J) US	8032700++	2011-10-04 / 2006-06-08	HYBRID MULTI-TIERED CACHING STORAGE SYSTEM
5	(J) Taiwan	I438628	2014-05-21 / 2006-06-08	DATA STORAGE SYSTEM AND DATA STORAGE MEDIUM
5	(J) Taiwan	I525431	Filed 2014-02-17 / 2006-06-08	Data Storage System, Data Structure and Data Storage Method
5	(N) Taiwan	I420307	2013-12-21 / 2006-06-08	Optimized placement policy for solid state storage devices
5	(N) Taiwan	I540430	2016-07-01 / 2005-06-08	Method for data storage
5	(K) US	9430386++	2016-08-30 / 2013-03-15	Multi-leveled cache management in a hybrid storage system
5	(K) US	App. No. 15/249,475	Filed 2016-08-29 / Priority 2013-03-15	Multi-leveled cache management in a hybrid storage system
5	(K) US	App. No. 14/689,045	Filed 2015-04-16/ Priority 2013-03-15	Write Buffering
5	(L) US	6000006	1999-12-07 / 1997-08-25	UNIFIED RE-MAP AND CACHE-INDEX TABLE WITH DUAL WRITE-COUNTERS FOR WEAR-LEVELING OF NON-VOLATILE FLASH RAM MASS STORAGE

5	(L) US	5822251	1998-10-13 / 1997-09-29	Expandable flash-memory mass-storage using shared buddy lines and intermediate flash-bus between device-specific buffers and flash-intelligent DMA controllers
5	(M) US	9099187	2015-08-04 / 2009-09-14	Reducing erase cycles in an electronic storage device that uses at least one erase-limited memory device
5	(M) US	8560804	2013-10-15 / 2009-09-14	Reducing erase cycles in an electronic storage device that uses at least one erase-limited memory device
5	(M) US	9484103	2016-11-1/ 2009-09-14	Electronic Storage Device
5	(M) US	App. No. 15/269,967	Filed 2016-09-19 / priority 2009-09-14	Electronic Storage Device
5	(N) US	8010740	2011-08-30/ 2008-11-25	Optimizing memory operations in an electronic storage device
5	(N) US	7506098	2009-03-17 / 2006-06-08	Optimized placement policy for solid state storage devices
5	(O) US	8447908	2013-04-21 / 2009-09-07	Multilevel memory bus system for solid-state mass storage
5	(O) US	8788725	2014-7-22 / 2009-09-07	Multilevel memory bus system for solid-state mass storage
5	(O) US	App. No. 14/297,628	2014-06-06 / 2009-09-07	Multilevel memory bus system
5	US	6529416	2003-03-04 / 2000-11-30	Parallel erase operations in memory systems
5	US	5956743	1999-09-21 / 1997-09-29	TRANSPARENT MANAGEMENT AT HOST INTERFACE OF FLASH-MEMORY OVERHEAD-BYTES USING FLASH-SPECIFIC DMA HAVING PROGRAMMABLE PROCESSOR-INTERRUPT OF HIGH-LEVEL OPERATIONS
5	US	9135190	2015-09-15 / 2009-09-04	Multi-profile memory controller for computing devices
5	US	6757845	2004-06-29 / 2000-11-30	Method and apparatus for testing a storage device
5	US	Appl. No. 15/482,684	Filed 2017-04-07	Multi-Dimensional Computer Storage System Note: this application was decided to be filed without any priority claim; option available for this application to be a continuation application that claims benefit to 15/268,536 and/or 15/268,533 (family (I))

(H thru O) Identifies Different Priority Families; All Others Are Single Patents

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: Rey Bruce et al. Patent No. 7,826,243 Issued: November 2, 2010 Serial No.: 11/322,442 Filing Date: December 29, 2005 Title: Multiple Chip Module And Package Stacking For Storage Devices	Confirmation No.: 5045 Atty. Docket No.: 6005.011 Customer No. 64180

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION UNDER RULE 1.182 FOR OBTAINING REPLACEMENT OF LETTERS OF PATENT

Dear Sir:

Pursuant to 37 CFR § 1.182, BiTMICRO Networks, Inc., the Assignee of United States Patent No. 7,826,243 ("the '243 Patent"), respectfully submits the following petition: petition for obtaining a replacement Letters Patent.

The assignment concerning the '243 Patent is recorded at reel 018594 and frame 0240.

A Power of Attorney and a Statement Under 37 CFR § 3.73(b) were previously filed in the application for the ‘243 patent on December 7, 2006.

The petition is based on the following facts. The ‘243 Patent Letters Patent was inadvertently lost. It is believed that the United States Patent and Trademark Office forwarded the original Letters Patent to the Assignee’s U.S. attorney, who forwarded the original Letters Patent to the Assignee. However, the Assignee currently does not have the original Letters Patent. It is believed the Letters Patent was lost in the mail or was lost due to another unknown reason or reasons.

In view of the foregoing, the Assignee respectfully requests that a duplicate Letters Patent be furnished to Assignee’s undersigned attorney.

A payment of $400 is being submitted herewith via EFS to cover the petition fee for the duplicate Letters Patent as set forth in 37 CFR § 1.17.

Favorable action is respectfully requested.

Conclusion

If the Petitions Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (805) 569-1600.

Date: July 10, 2017

Respectfully submitted,

_/Arnold de Guzman/_____
Arnold de Guzman
Attorney for Applicant(s)
Reg. No. 39,955

Please send correspondence to:
Customer No. 64180

CERTIFICATE OF TRANSMISSION OR MAILING 37 C.F.R. 1.8			
I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office in accordance with 37 C.F.R. § 1.6(d), or is being transmitted via the Office electronic filing system in accordance with 37 C.F.R. § 1.6(a)(4), or is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below:			
Signature:	/Arnold de Guzman/		
Typed or Printed Name:	Arnold de Guzman	Dated:	**July 10, 2017**
Express Mail Mailing Number (*optional*):			

Electronic Patent Application Fee Transmittal

Application Number:	11322442
Filing Date:	29-Dec-2005
Title of Invention:	MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES
First Named Inventor/Applicant Name:	Rey Bruce
Filer:	Stephen Radcliff Uriarte/Arnold deGuzman
Attorney Docket Number:	6005.011

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
PETITION FEE- 37 CFR 1.17(F) (GROUP I)	1462	1	400	400
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**400**

Electronic Acknowledgement Receipt	
EFS ID:	29741019
Application Number:	11322442
International Application Number:	
Confirmation Number:	5045
Title of Invention:	MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES
First Named Inventor/Applicant Name:	Rey Bruce
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte/Arnold deGuzman
Filer Authorized By:	Stephen Radcliff Uriarte
Attorney Docket Number:	6005.011
Receipt Date:	10-JUL-2017
Filing Date:	29-DEC-2005
Time Stamp:	23:38:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$400
RAM confirmation Number	071117INTEFSW23430401
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Petition for review by the Office of Petitions	6005_011_petition.pdf	28589 3417c177454101a5eb2b2ae685d7232ef636cca4	no	3
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30726 af3c9a39061cd6ad7711ee4afd2bf6b3e535260f	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	59315		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Attorney Docket#: 6005.011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	BRUCE et al.
Serial #:	11/322,442
Patent #:	**7,826,243**
Issue Date:	**02 NOV 2010**
Confirmation Number:	5045
Application Filing Date:	29 Dec 2005
For:	MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES

Certificate of EFS-Web Transmission

I hereby certify that this correspondence is being transmitted via the U.S. Patent and Trademark Office(USPTO) electronic filing system (EFS-Web) to the USPTO on **08 August 2014**.

Certificate Signer: Arnold de Guzman
Signature: /Arnold de Guzman/
Registration Number: 39,955

Director of the United States Patent & Trademark Office
Attn: Maintenance Fee
Alexandria, VA 22314

Notification of Loss of Entitlement to Small Entity Status

Dear Sir/Madam:

Entity Status Change from Small to Large Entity:

X In accordance with 37 CFR 1.27 and 1.33(b), please accept this paper as notice of a *loss* of entitlement to small entity status for the above-referred issued U.S. patent.

Thank you for your assistance.

Sincerely,

Signature: /Arnold de Guzman/ Date: 08 August 2014
Name: Arnold de Guzman USPTO Reg. #: 39,955

Bitmicro Networks, Inc.
47929 Fremont Blvd
Fremont, CA 94538
Tel: 510.743.3173
Fax: 510.623.2342

Electronic Acknowledgement Receipt	
EFS ID:	19822563
Application Number:	11322442
International Application Number:	
Confirmation Number:	5045
Title of Invention:	MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES
First Named Inventor/Applicant Name:	Rey Bruce
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte/Arnold deGuzman
Filer Authorized By:	Stephen Radcliff Uriarte
Attorney Docket Number:	6005.011
Receipt Date:	08-AUG-2014
Filing Date:	29-DEC-2005
Time Stamp:	20:52:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Notification of loss of entitlement to small entity status	6005_011_Entity_change_request.pdf	50308 5e30bb8e5f695f44c035a6f3d74127c7cb57e991	no	1

Warnings:
Information:

Total Files Size (in bytes):	50308

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/322,442	11/02/2010	7826243	6005.011	5045

64180 7590 10/13/2010

URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 747 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Rey Bruce, San Jose, CA;
Ricardo Bruce, Union City, CA;
Patrick Digamon Bugayong, Mandaluyong City, PHILIPPINES;
Joel Alonzo Baylon, Tanza, PHILIPPINES;

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

64180 7590 06/23/2010

URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/322,442	12/29/2005	Rey Bruce	6005.011	5045

TITLE OF INVENTION: MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$755	$300	$0	$1055	09/23/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
SOFOCLEOUS, ALEXANDER	2824	365-051000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Uriarte Law

2 Fernandez & Associates

3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: BiTMICRO Networks, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Fremont, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee

☒ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.

☒ Payment by credit card. Form PTO-2038 is attached. **(Payment by EFS-Web)**

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 504068 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☒ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Stephen R.Uriarte/ Date 22 September 2010

Typed or printed name Stephen R. Uriarte Registration No. 40,854

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal

Application Number:	11322442
Filing Date:	29-Dec-2005
Title of Invention:	MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES
First Named Inventor/Applicant Name:	Rey Bruce
Filer:	Stephen Radcliff Uriarte
Attorney Docket Number:	6005.011

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	2501	1	755	755
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1055**

Electronic Acknowledgement Receipt	
EFS ID:	8478324
Application Number:	11322442
International Application Number:	
Confirmation Number:	5045
Title of Invention:	MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES
First Named Inventor/Applicant Name:	Rey Bruce
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.011
Receipt Date:	22-SEP-2010
Filing Date:	29-DEC-2005
Time Stamp:	20:56:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1055
RAM confirmation Number	7554
Deposit Account	504068
Authorized User	URIARTE,STEPHEN R.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	6005_011_IssueFeePayment_20100922.pdf	119124 5f5b85c225146dbf1a244905344ce88576c15844	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	31703 d04d70fd0ac8f2428b776b51f046d8f3514d68e7	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	150827		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: BRUCE et al.	Group Art Unit: 2824
Serial No.: 11/322,442	Examiner: SOFOCLEOUS, Alexander
Application Filing Date: 29 Dec 2005	
For: MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND REPLY TO NOTICE TO FILE CORRECTED APPLICATION PAPERS (Notice of Allowance Mailed)

Dear Examiner:

In response to a Notice to File Corrected Application Papers, mailed 12 July 2010 and hereinafter named the "Notice", please kindly amend this Application as follows and consider the remarks set forth below.

Amendment(s) to the Drawings begins on page 2; and

Remarks begin on page 3 of this paper.

The replacement sheet of the figure amended in the Amendment(s) to the Drawings is attached to this paper.

Amendment(s) to the Drawings

The following proposed amendment to the Drawings is provided in the form of a replacement drawing sheet, which is labeled "Replacement Sheet" on its page header pursuant to 37 CFR 1.84(c). No new matter has been added.

Please amend drawing sheet 26/28 by replacing the figure number from "Figure 20a" to Figure 20b". The figure on drawing sheet 26/28 was originally labeled with the figure number "Figure 20b" but during the amendment filed on 13 Feb 2009, was inadvertently submitted as amended with the incorrect figure number of "Figure 20a", causing the figure number of "Figure 20a" to appear twice in the Drawings. Consequently, please accept this amendment to the Drawings.

Remarks

The Drawings have been amended in accordance with 37 CFR 1.121 to correct minor errors described in the Notice. These corrections are of a clerical nature and do not add "new matter".

Request to Proceed to Issuance

It is believed that this Amendment places this Application into condition for issuance. Early favorable consideration of this Amendment is earnestly solicited since this application has been previously accorded an Allowance Date.

Respectfully submitted,

Dated: 9 September 2010

/Stephen R. Uriarte/
Stephen R. Uriarte, Reg. No. 40,854

Uriarte Law
2021 The Alameda,
Suite 225
San Jose, CA 95126
Tel: 408.244.2164 x111
Fax: 408.716.2651
Email: mail@uriartelaw.com

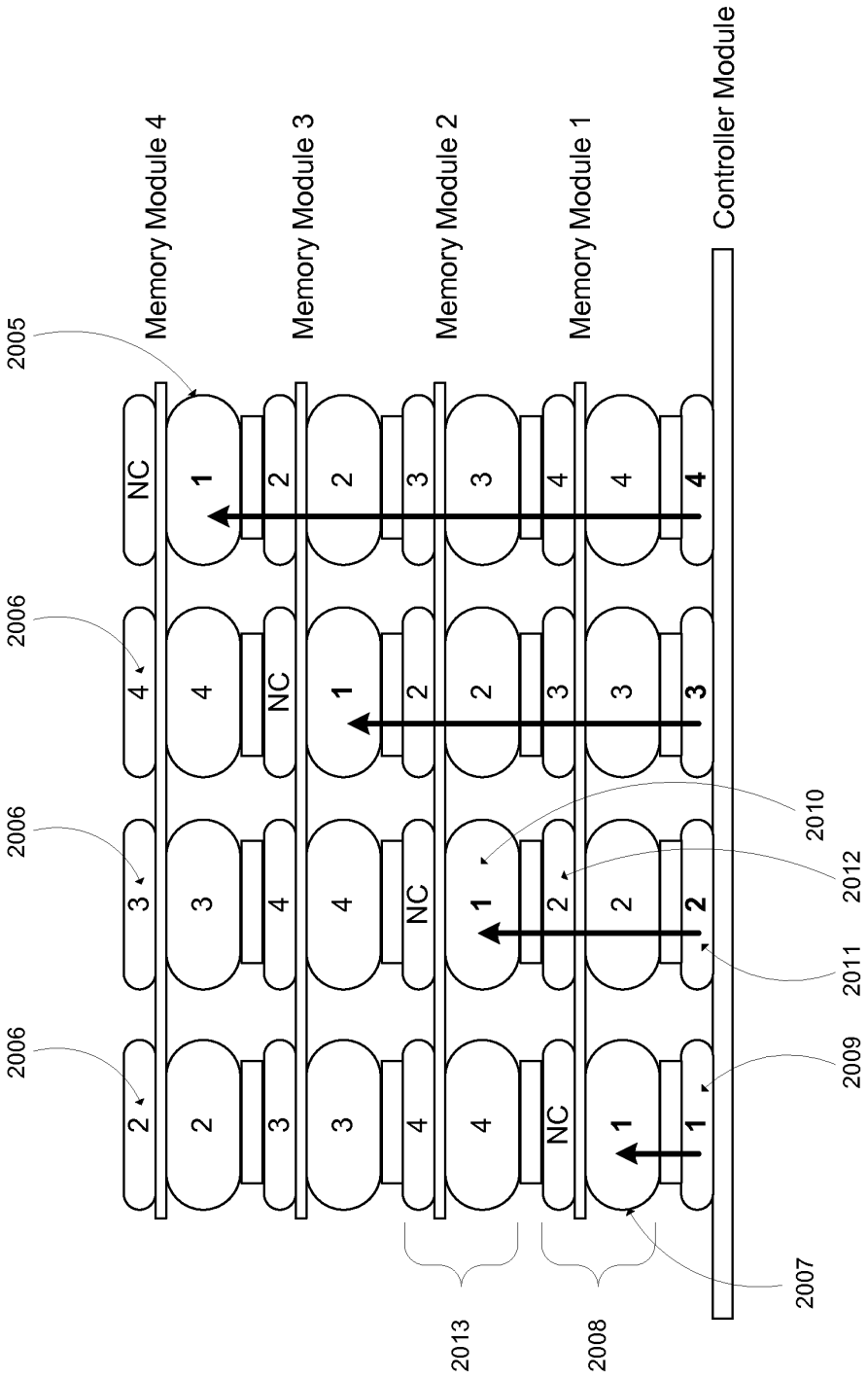

Memory Module 4
Memory Module 3
Memory Module 2
Memory Module 1
Controller Module
2005
2006
2006
2006
2010
2012
2011
2009
2007
2013
2008
NC

Figure 20b

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Application No. : 11322442
Applicant : Bruce
Filing Date : 12/29/2005
Date Mailed : 07/12/2010

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Notice of Allowance Mailed

This application has been accorded an Allowance Date and is being prepared for issuance. The application, however, is incomplete for the reasons below.

Applicant is given 2 month(s) from the mail date of this Notice within which to respond.

The informalities requiring correction are indicated in the attachment(s). If the informality pertains to the abstract, specification (including claims) or drawings, the informality must be corrected with an amendment in compliance with 37 CFR 1.121 (or, if the application is a reissue application, 37 CFR 1.173). Such an amendment may be filed after payment of the issue fee if limited to correction of informalities noted herein. See Waiver of 37 CFR 1.312 for Documents Required by the Office of Patent Publication, 1280 Off. Gaz. Patent Office 918 (March 23, 2004). In addition, if the informality is not corrected until after payment of the issue fee, for purposes of 35 U.S.C. 154(b)(1)(iv), "all outstanding requirements" will be considered to have been satisfied when the informality has been corrected. A failure to respond within the above-identified time period will result in the application being ABANDONED. **This period for reply is NOT extendable under 37 CFR 1.136(a).**

See attachment(s).

A copy of this notice MUST be returned with the reply. Please address response to "Mail Stop Issue Fee,Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450".

/Doug Gemmill/
Publishing Division
Office of Data Management
(571) 272-4200

Application No. 11322442 **Drawings filed 02/13/2009**

IDENTIFICATION OF DRAWING DEFICIENCIES

- [ ] There is a hole or the image thereof within the illustration. FIG(s)
- [ ] The illustration is penetrated or traversed by a solid or broken line that is not intended to be part of the drawing, such as a dark line caused by a flaw in the copying process. FIG(s)
- [ ] An ink stamp or the image thereof obscures part of the illustration. FIG(s)
- [ ] The drawing is marred by black smudges, obliterations, or fax/copier marks (for example, speckles or dots in a substantial portion of the drawing). FIG(s)
- [X] Figure numbers are duplicated or missing. FIG(s) 20A
- [ ] Drawing sheet or figure is missing. FIG(s)
- [ ] Numbers, letters, or reference characters in the drawing have been crossed out or are illegibly handwritten. FIG(s)
- [ ] The character of the lines, numbers, and letters is poor. FIG(s)
- [ ] The drawing's background shows that the original drawing was made on graph paper or other paper with a pattern or decoration. FIG(s)
- [ ] The FIG. number label is placed in a location that causes the drawing to be read upside down. FIG(s)
- [ ] Data, a reference number, or part of the drawing is truncated or missing, or a lead line has no reference number. FIG(s)
- [ ] The drawing is continued onto a second page (or more) without proper labeling under 37 CFR 1.84(u)(1). FIG(s)
- [ ] The drawing and/or the FIG. label contain(s) foreign language. FIG(s)
- [ ] A petition under 37 CFR 1.84(a)(2) to accept color drawings has been granted, but the brief description of the drawings in the specification does not contain (or has not been amended to contain) the paragraph required by 37 CFR 1.84(a)(2)(iv).

COMMENTS:
FIG. 20A appears twice.

Electronic Acknowledgement Receipt	
EFS ID:	8388783
Application Number:	11322442
International Application Number:	
Confirmation Number:	5045
Title of Invention:	MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES
First Named Inventor/Applicant Name:	Rey Bruce
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.011
Receipt Date:	09-SEP-2010
Filing Date:	29-DEC-2005
Time Stamp:	20:12:38
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment after Notice of Allowance (Rule 312)	6005_011_1stRsp2Correct_20100909.pdf	96122 c5246a6e29d1d9b88c6828932a04ffbf822a1210	no	3
Warnings:					
Information:					