2	Amendment after Notice of Allowance (Rule 312)	6005_011_FIG8_20b_rplcmnt_20100909.pdf	43050 d71b596ce06283e25c74c6a48c937cd7d7734911	no	1
Warnings:					
Information:					
3	Amendment after Notice of Allowance (Rule 312)	6005_011_Notice2CorrCopy_20100712B.pdf	84484 4b21dffd5a9582d3f87db2c602c29017b30e55d6	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	223656		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/322,442	12/29/2005	Rey Bruce	6005.011	5045

64180 7590 07/12/2010

URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

EXAMINER	
SOFOCLEOUS, ALEXANDER	
ART UNIT	**PAPER NUMBER**
2824	

NOTIFICATION DATE	DELIVERY MODE
07/12/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mail@URIARTELAW.COM
stephen@uriartelaw.com
labid@uriartelaw.com

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Application No. : 11322442
Applicant : Bruce
Filing Date : 12/29/2005
Date Mailed : 07/12/2010

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Notice of Allowance Mailed

This application has been accorded an Allowance Date and is being prepared for issuance. The application, however, is incomplete for the reasons below.

Applicant is given 2 month(s) from the mail date of this Notice within which to respond.

The informalities requiring correction are indicated in the attachment(s). If the informality pertains to the abstract, specification (including claims) or drawings, the informality must be corrected with an amendment in compliance with 37 CFR 1.121 (or, if the application is a reissue application, 37 CFR 1.173). Such an amendment may be filed after payment of the issue fee if limited to correction of informalities noted herein. See Waiver of 37 CFR 1.312 for Documents Required by the Office of Patent Publication, 1280 Off. Gaz. Patent Office 918 (March 23, 2004). In addition, if the informality is not corrected until after payment of the issue fee, for purposes of 35 U.S.C. 154(b)(1)(iv), "all outstanding requirements" will be considered to have been satisfied when the informality has been corrected. A failure to respond within the above-identified time period will result in the application being ABANDONED. **This period for reply is NOT extendable under 37 CFR 1.136(a).**

See attachment(s).

A copy of this notice MUST be returned with the reply. Please address response to "Mail Stop Issue Fee,Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450".

/Doug Gemmill/
Publishing Division
Office of Data Management
(571) 272-4200

Application No. 11322442 **Drawings filed 02/13/2009**

IDENTIFICATION OF DRAWING DEFICIENCIES

- [ ] There is a hole or the image thereof within the illustration. FIG(s)
- [ ] The illustration is penetrated or traversed by a solid or broken line that is not intended to be part of the drawing, such as a dark line caused by a flaw in the copying process. FIG(s)
- [ ] An ink stamp or the image thereof obscures part of the illustration. FIG(s)
- [ ] The drawing is marred by black smudges, obliterations, or fax/copier marks (for example, speckles or dots in a substantial portion of the drawing). FIG(s)
- [X] Figure numbers are duplicated or missing. FIG(s) 20A
- [ ] Drawing sheet or figure is missing. FIG(s)
- [ ] Numbers, letters, or reference characters in the drawing have been crossed out or are illegibly handwritten. FIG(s)
- [ ] The character of the lines, numbers, and letters is poor. FIG(s)
- [ ] The drawing's background shows that the original drawing was made on graph paper or other paper with a pattern or decoration. FIG(s)
- [ ] The FIG. number label is placed in a location that causes the drawing to be read upside down. FIG(s)
- [ ] Data, a reference number, or part of the drawing is truncated or missing, or a lead line has no reference number. FIG(s)
- [ ] The drawing is continued onto a second page (or more) without proper labeling under 37 CFR 1.84(u)(1). FIG(s)
- [ ] The drawing and/or the FIG. label contain(s) foreign language. FIG(s)
- [ ] A petition under 37 CFR 1.84(a)(2) to accept color drawings has been granted, but the brief description of the drawings in the specification does not contain (or has not been amended to contain) the paragraph required by 37 CFR 1.84(a)(2)(iv).

COMMENTS:
FIG. 20A appears twice.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

64180 7590 06/23/2010

URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

EXAMINER	
SOFOCLEOUS, ALEXANDER	
ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 06/23/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/322,442	12/29/2005	Rey Bruce	6005.011	5045

TITLE OF INVENTION: MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$755	$300	$0	$1055	09/23/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

64180 7590 06/23/2010

URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/322,442	12/29/2005	Rey Bruce	6005.011	5045

TITLE OF INVENTION: MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$755	$300	$0	$1055	09/23/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
SOFOCLEOUS, ALEXANDER	2824	365-051000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/322,442	12/29/2005	Rey Bruce	6005.011	5045

64180 7590 06/23/2010

URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

EXAMINER	
SOFOCLEOUS, ALEXANDER	
ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 06/23/2010

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 304 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 304 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	11/322,442	BRUCE ET AL.	
	Examiner	Art Unit	
	ALEXANDER SOFOCLEOUS	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the RCE filed June 8, 2010*.

2. ☒ The allowed claim(s) is/are *14-16 and 20-31*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 6/8/2010
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Dang T Nguyen/
Primary Examiner, Art Unit 2824

DETAILED ACTION

1. This action is responsive to the following communication: the Request for Continued Examination filed June 8, 2010 and the Information Disclosure Statement filed June 8, 2010.

2. Claims 14-16 and 20-31 are pending. Claims 1-13 and 17-19 are cancelled. Claim 14 is independent.

Continued Examination Under 37 CFR 1.114 After Allowance

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under Ex Parte Quayle, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on June 8, 2010 has been entered.

Specification

4. The specification amendment (Title) filed June 8, 2010 is acceptable.

Information Disclosure Statement

5. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) filed on June 8, 2010. This IDS has been considered.

Allowable Subject Matter

6. **Claims 14-16 and 20-31 are allowed.**

7. The following is an examiner's statement of reasons for allowance:

With respect to independent claim 14, the record of the prosecution history as a whole makes clear the reasons for allowance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CONCLUSION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on M-F 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGS

/Dang T Nguyen/

Primary Examiner, Art Unit 2824

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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BIB DATA SHEET

CONFIRMATION NO. 5045

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/322,442	12/29/2005	257	2824	6005.011

APPLICANTS

Rey Bruce, San Jose, CA;
Ricardo Bruce, Union City, CA;
Patrick Digamon Bugayong, Mandaluyong City, PHILIPPINES;
Joel Alonzo Baylon, Tanza, PHILIPPINES;

**** CONTINUING DATA **************************

**** FOREIGN APPLICATIONS **************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **
02/10/2006

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /ALEXANDER SOFOCLEOUS/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	28	26	2

ADDRESS

URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126
UNITED STATES

TITLE

MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES

FILING FEE RECEIVED		
702	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11322442	BRUCE ET AL.
	Examiner	Art Unit
	ALEXANDER SOFOCLEOUS	2824

ORIGINAL		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
365	51	G	1	1	C	5 / 02 (2006.01.01)					

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
257	686	777			
365	63	230.03	230.05		

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17												
	2		18												
	3		19												
	4	11	20												
	5	12	21												
	6	3	22												
	7	10	23												
	8	13	24												
	9	14	25												
	10	15	26												
	11	4	27												
	12	5	28												
	13	6	29												
1	14	7	30												
2	15	8	31												
9	16														

/ALEXANDER SOFOCLEOUS/ Examiner.Art Unit 2824 (Assistant Examiner)	06/14/2010 (Date)	Total Claims Allowed: 15	
/DANG T NGUYEN/ Primary Examiner.Art Unit 2824 (Primary Examiner)	06/17/2010 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 21b

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S5	941	S2 S3 memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/01 14:38
S4	1182	S2 S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/01 14:38
S3	33158	(module with stack$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/01 14:38
S2	13942	((257/686) or (365/51,52,63,230.03,230.05)).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/03/01 14:38
S6	1	S2 S3 memory (serial adj chain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/01 14:39
S7	4	(("6469375") or ("5995379") or ("6172874") or ("6900528")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/01 15:04
S8	316	S2 S3 memory (pad with ball)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/01 15:39
S11	2974	(257/777).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/03/01 15:43
S10	1042	(257/776).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/03/01 15:43

S9	3813	(257/774).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/03/01 15:43
S14	160	S11 S3 memory (pad with ball)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/01 15:44
S13	3	S10 S3 memory (pad with ball)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/01 15:44
S12	29	S9 S3 memory (pad with ball)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/01 15:44
S16	14	("5216278" | "5506756" | "5521435" | "5640048" | "5734201" | "5835355" | "5895231" | "6078506" | "6313522" | "6381141" | "6388333" | "6479758").PN. OR ("6791193").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/01 15:49
S17	1	(S2 or S9 or S10 or S11) S3 (passive adj2 (port or pad or ball))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/01 15:50
S18	10	("20050044305" | "6313522" | "6603198" | "6740546" | "6791193" | "6977440" | "7193306" | "7279786" | "7335995").PN. OR ("7439615").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/01 15:53
S19	104	("5012323" | "5121293" | "5128831" | "5189505" | "5289337" | "5291061" | "5323060" | "5385869" | "5422435" | "5434745" | "5474957" | "5495398" | "5513076" | "5607099" | "5963430" | "6020629").PN. OR ("6313522").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/01 15:54
S20	147	("20020074669" | "20030111709" | "20030218235" | "20040018693" | "20040031972" | "20040257780" | "3390308" | "3614832" | "3683105" | "3832769" | "3868724" | "3923359" | "4216577" | "4371744" | "4371912" | "4489364" | "4540226" | "4551746" | "4558397" | "4627151" | "4628406" | "4638348" | "4681654" | "4685998" | "4701999" | "4710798" | "4734825" | "4746392" | "4754316" | "4761681" | "4772936" | "4812421" | "4823234" | "4829666" | "4837184" | "4841355" | "4855867" | "4855868" | "4868712" | "4878098" | "4893172" | "4897534" | "4897918" | "4918811" | "4937203" |	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/01 15:56

		"4956694" | "4967261" | "4982265" | "4994902" | "4996583" | "4996587" | "4999319" | "5028986" | "5029325" | "5037779" | "5045921" | "5055913" | "5117282" | "5127570" | "5128831" | "5138438" | "5148265" | "5148266" | "5172303" | "5198888" | "5222014" | "5247423" | "5258330" | "5266912" | "5281852" | "5289346" | "5304252" | "5304512" | "5311401" | "5313096" | "5334875" | "5337077" | "5346861" | "5350947" | "5376825" | "5379191" | "5384689" | "5390844" | "5394009" | "5397916" | "5397921" | "5409865" | "5412247" | "5455740" | "5479318" | "5489749" | "5543664" | "5548091" | "5552631" | "5552963" | "5564181" | "5600541" | "5608265" | "5616958" | "5625221" | "5637536" | "5639695" | "5642261" | "5656856" | "5659952" | "5663106" | "5668405" | "5677566" | "5681777" | "5701031" | "5734555" | "5751063" | "5783870" | "5784264" | "5801439" | "5804874" | "5834339" | "5835988" | "5844315" | "5861666" | "5883426" | "5912507" | "6030856").PN. OR ("6072233" | "6093029" | "6108212" | "6180881" | "6195268" | "6218848" | "6232152" | "6268649" | "6272744" | "6291259" | "6303997" | "6313522" | "6335565" | "6342728" | "6369445" | "6388264" | "6462421" | "6496026" | "6515870" | "6555918" | "6740981").PN. OR ("7335995").URPN.				
S21	8	(passive adj port) same memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 08:25
S22	6	(passive adj port) (stack$4 with memory)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 08:26
S23	1	11/322442	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 08:29
S24	1495	(memory with module with stack$4) (rout $3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 12:19

S26	10	(memory with module with stack$4) same (port with rout$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 13:42
S25	162	(memory with module with stack$4) same (rout$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 13:42
S28	8	(memory with module with stack$4) same (rout$3) same serial$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 13:43
S27	8	(memory with module with stack$4) same (rout$3) same serial	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 13:43
S29	18	("20040030794" | "20040183795" | "20050166026" | "20050198458" | "20060020740" | "20060024541" | "6295586" | "6502161" | "6571325" | "6725314" | "6882082" | "6889304" | "6922770" | "6941428" | "7017022" | "7032092" | "7051151" | "7257129").PN. OR ("7409491").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/15 13:45
S30	2	("20050047250").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/03/15 13:53
S32	13	("20030061447" | "6233650" | "6349050" | "6530033").PN. OR ("7078793").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/15 13:56
S31	1	(10/927312).APP.	USPAT; USOCR	AND	ON	2010/03/15 13:56
S33	15	("20050086417" | "20050138267" | "20050259504" | "20050273679" | "20050278495" | "20070189049" | "6754117" | "6820181" | "6901475" | "6979895" | "6982892" | "6993612" | "7078793").PN. OR ("7471538").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/15 13:59
S34	70	("3654394" | "4513368" | "4645944" | "4985703" | "5261068" | "5289062").PN. OR ("6233650").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/15 14:01
S36	6	(memory with module with stack$4) (reconfigur$4 with rout$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 14:11

S35	0	(memory with module with stack$4) same (reconfigur$4 with rout$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 14:11
S37	26	(memory with module with stack$4) same reconfigur$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 14:13
S38	164	("4754316" | "4983533" | "5019943" | "5311401" | "5313096").PN. OR ("5432729").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/15 14:18
S39	53	("5585675" | "5652904" | "5838060" | "6051887" | "6092174" | "6313522" | "6449170").PN. OR ("6627985").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/15 14:24
S40	53	("5585675" | "5652904" | "5838060" | "6051887" | "6092174" | "6313522" | "6449170").PN. OR ("6627985").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/15 14:25
S41	2	("6747478").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/03/15 14:26
S42	17	("5798282" | "5946545" | "6545501" | "6614267" | "6627985" | "6861865").PN. OR ("6991947").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/15 14:31
S43	32	("4574331" | "4727410" | "4813129" | "5007841" | "5016138" | "5051865" | "5177594" | "5224918" | "5252857" | "5281852" | "5311401" | "5327327" | "5343075" | "5406565" | "5414637" | "5432729" | "5434745" | "5502333" | "5561593" | "5686843" | "5691041").PN. OR ("5781413").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/15 14:46
S44	33	("4574331" | "4727410" | "4813129" | "5007841" | "5016138" | "5039628" | "5051865" | "5177594" | "5224918" | "5252857" | "5281852" | "5311401" | "5327327" | "5343075" | "5414637" | "5432729" | "5434745" | "5477933" | "5483421").PN. OR ("5815374").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/15 14:47
S45	8	(memory with module with stack$4) same ((re$1rout$3 or re$1configur$4 or re $1program$4) near4 interconnect$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 14:53
S46	15	(memory with module with stack$4) same ((re$1rout$4 or re$1configur$4 or re $1program$5 or rout$4 or configur$4 or program$5) near4 interconnect$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 08:26

S47	211	(memory with module with stack$4) same (re$1rout$3 or rout$3 or ((program$5 or re $1program$5 or configur$4 or re$1configur $4) with interconnect$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/17 14:44
L1	4	(("5854507") or ("6392896")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/06/14 13:04
L3	105	("5594275" | "5715144" | "5751060" | "5760478").PN. OR ("5854507").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/06/14 13:07
L2	11	("4739446" | "5034349" | "5397747" | "5530623" | "6059173" | "6115260").PN. OR ("6392896").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/06/14 13:07
L4	116	2 or 3	US-PGPUB; USPAT; USOCR	AND	ON	2010/06/14 13:08
L7	226	(memory with module with stack$4) same (re$1rout$3 or rout$3 or ((program$5 or re $1program$5 or configur$4 or re$1configur $4) with interconnect$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/06/14 13:33
L35	58	7 34	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/06/14 13:42
L34	16302	((257/686,777) or (365/51,52,63,230.03,230.05)).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/06/14 13:42

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S48	14	(memory with module with stack$4) same ((re $1rout$4 or re$1configur$4 or re$1program$5 or rout$4 or configur$4 or program$5) near4 interconnect$4)	US-PGPUB; USPAT; UPAD	AND	ON	2010/03/17 14:43
S50	18186	((257/686,773,777) or (365/51,52,63,230.03,230.05)).CCLS.	US-PGPUB; USPAT; UPAD	OR	OFF	2010/03/17 14:44
S49	204	(memory with module with stack$4) same (re $1rout$3 or rout$3 or ((program$5 or re $1program$5 or configur$4 or re$1configur$4) with interconnect$3))	US-PGPUB; USPAT; UPAD	AND	ON	2010/03/17 14:44
S51	58	S49 S50	US-PGPUB; USPAT; UPAD	AND	ON	2010/03/17 14:45

L29	60	L27 L28	US-PGPUB; USPAT; UPAD	AND	ON	2010/06/14 13:33
L28	18583	((257/686,773,777) or (365/51,52,63,230.03,230.05)).CCLS.	US-PGPUB; USPAT; UPAD	OR	OFF	2010/06/14 13:33
L27	215	(memory with module with stack$4) same (re $1rout$3 or rout$3 or ((program$5 or re $1program$5 or configur$4 or re$1configur$4) with interconnect$3))	US-PGPUB; USPAT; UPAD	AND	ON	2010/06/14 13:33
L26	15	(memory with module with stack$4) same ((re $1rout$4 or re$1configur$4 or re$1program$5 or rout$4 or configur$4 or program$5) near4 interconnect$4)	US-PGPUB; USPAT; UPAD	AND	ON	2010/06/14 13:33

6/14/2010 1:46:04 PM
C:\Documents and Settings\asofocleous\My Documents\EAST\Workspaces\11322442.wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11322442	BRUCE ET AL.
	Examiner	Art Unit
	ALEXANDER SOFOCLEOUS	2824

SEARCHED

Class	Subclass	Date	Examiner
257	686	5/9/2009	EU
257	686, 777	03/17/2010	AGS
365	51, 63, 230.03, 230.05	03/17/2010	AGS
257	686,777	06/14/2010	AGS
365	51, 53, 230.03, 230.05	06/14/2010	AGS

SEARCH NOTES

Search Notes	Date	Examiner
EAST database serarch	5/9/2009	EU
consulted VanThu Nguyen regarding class 365	03/16/2010	AGS
see updated EAST search history	03/17/2010	AGS
see updated EAST search history	06/14/2010	AGS

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner
257	686, 777	03/17/2010	AGS
365	51, 63, 230.03, 230.05	03/17/2010	AGS
257	686, 777	06/14/2010	AGS
365	51, 63, 230.03, 230.05	06/14/2010	AGS

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11322442	BRUCE ET AL.
	Examiner	Art Unit
	ALEXANDER SOFOCLEOUS	2824

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/23/2008	08/07/2008	05/09/2009	03/17/2010	06/14/2010				
	1	÷	-	-	-	-				
	2	÷	-	-	-	-				
	3	÷	-	-	-	-				
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3	22	÷	✓	✓	=	=				
10	23	÷	✓	✓	=	=				
13	24	÷	N	✓	=	=				
14	25	÷	N	✓	=	=				
15	26	÷	N	✓	=	=				
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5	28			✓	=	=				
6	29			✓	=	=				
7	30			✓	=	=				
8	31			✓	=	=				

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11322442
	Filing Date	2005-12-29
	First Named Inventor	BRUCE, Rey
	Art Unit	2824
	Examiner Name	SOFOCLEOUS, Alexander
	Attorney Docket Number	6005.011

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5854507		1998-12-29	Jian Miremadi et al.	All (defines general state of the art)
	2	6392896	B1	2002-05-21	Herbert Stoller	All (defines general state of the art)

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Receipt date: 06/08/2010	Application Number	11322442 11322442 - GAU: 2824
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2005-12-29
	First Named Inventor	BRUCE, Rey
	Art Unit	2824
	Examiner Name	SOFOCLEOUS, Alexander
	Attorney Docket Number	6005.011

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		☐

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EXAMINER SIGNATURE

Examiner Signature	/Alexander Sofocleous/	Date Considered	06/14/2010

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /AGS/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: BRUCE et al.	Group Art Unit: 2824
Serial No.: 11/322,442	Examiner: SOFOCLEUS, Alexander
Application Filing Date: 29 Dec 2005	
For: MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Dear Examiner:

Please kindly amend this Application as follows and consider the remarks set forth below.

Amendments to the Specification begin on page 2; and

Remarks begin on page 3 of this paper.

Amendments to the Specification

Text in underline indicates new text, while text in strike-out format or between a pair of double brackets indicates deletion of the text.

In the Specification, as previously amended, please enter the amendments shown with respect to the replacement paragraphs identified below.

Please replace the Title of Invention by replacing in its entirety the title listed on page 2, lines 1-2, with the following replacement Title of Invention:

Multiple Chip Module and Package Stacking ~~Method~~ For Storage Devices

Remarks

A Request for Continued Examination was recently filed for this application in a response to a Notice of Allowance. The Notice of Allowance did not reflect a prior request to amend the Title of Invention in an Amendment and Reply to Office Action, which was submitted on behalf of the Applicants on 13 November 2009. Consequently, please accept this amendment as indicated on page 2 above. This requested amendment does not add "new matter".

Request for Allowance

It is believed that this Amendment places this Application into condition for allowance. Early favorable consideration of this Amendment is earnestly solicited.

Respectfully submitted,

Dated: 11 June 2010

/Stephen R. Uriarte/
Stephen R. Uriarte, Reg. No. 40,854

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Fax: 408.716.2651
Email: mail@uriartelaw.com

Electronic Acknowledgement Receipt

EFS ID:	7800167
Application Number:	11322442
International Application Number:	
Confirmation Number:	5045
Title of Invention:	MULTIPLE CHIP MODULE AND PACKAGE STACKING METHOD FOR STORAGE DEVICES
First Named Inventor/Applicant Name:	Rey Bruce
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.011
Receipt Date:	11-JUN-2010
Filing Date:	29-DEC-2005
Time Stamp:	17:36:56
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Preliminary Amendment	6005_011_Amend_Title_20100611B.pdf	79442 9642b345dfb888e18b221c057d4c2d0cd88bd865	no	3
Warnings:					
Information:					

Total Files Size (in bytes):	79442

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/322,442	12/29/2005	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☒		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	06/11/2010	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 15	Minus	** 28	= 0	X $26 =	0	OR	X $ =	
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $110 =	0	OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE	

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/CHRISTINE MOLLISH/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	11/322,442	Filing Date	2005-12-29	Docket Number (if applicable)	6005.011	Art Unit	2824
First Named Inventor	BRUCE, Rey			Examiner Name	SOFOCLEOUS, Alex		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☐ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 504068

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Stephen R. Uriarte/	Date (YYYY-MM-DD)	2010-06-07
Name	Stephen R. Uriarte	Registration Number	40854

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	11322442
Filing Date	2005-12-29
First Named Inventor	BRUCE, Rey
Art Unit	2824
Examiner Name	SOFOCLEOUS, Alexander
Attorney Docket Number	6005.011

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5854507		1998-12-29	Jian Miremadi et al.	All (defines general state of the art)
	2	6392896	B1	2002-05-21	Herbert Stoller	All (defines general state of the art)

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11322442
	Filing Date	2005-12-29
	First Named Inventor	BRUCE, Rey
	Art Unit	2824
	Examiner Name	SOFOCLEOUS, Alexander
	Attorney Docket Number	6005.011

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	11322442
	Filing Date	2005-12-29
	First Named Inventor	BRUCE, Rey
	Art Unit	2824
	Examiner Name	SOFOCLEOUS, Alexander
	Attorney Docket Number	6005.011

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Stephen R. Uriarte/	Date (YYYY-MM-DD)	2010-06-07
Name/Print	Stephen R. Uriarte	Registration Number	40854

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal	
Application Number:	11322442
Filing Date:	29-Dec-2005
Title of Invention:	MULTIPLE CHIP MODULE AND PACKAGE STACKING METHOD FOR STORAGE DEVICES
First Named Inventor/Applicant Name:	Rey Bruce
Filer:	Stephen Radcliff Uriarte
Attorney Docket Number:	6005.011
Filed as Small Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	2801	1	405	405
		Total in USD ($)		**405**

Electronic Acknowledgement Receipt	
EFS ID:	7764686
Application Number:	11322442
International Application Number:	
Confirmation Number:	5045
Title of Invention:	MULTIPLE CHIP MODULE AND PACKAGE STACKING METHOD FOR STORAGE DEVICES
First Named Inventor/Applicant Name:	Rey Bruce
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.011
Receipt Date:	08-JUN-2010
Filing Date:	29-DEC-2005
Time Stamp:	01:46:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$405
RAM confirmation Number	6849
Deposit Account	504068
Authorized User	URIARTE,STEPHEN R.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	6005_011_RCE_20100607.pdf	697432 15b870b6147c40bd04ccc36feed86b13f006ac5d	no	3
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Filed (SB/08)	6005_011_RCE_IDSsubmission_20100607.pdf	611742 3220eb31ea98c7a0a20410d1f9195cebe1b43d71	no	4
Warnings:					
Information:					
3	Fee Worksheet (PTO-875)	fee-info.pdf	30409 ec78a37d439fdd4411deb914effaeeec9dec0395	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1339583		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

64180 7590 04/09/2010

URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

EXAMINER	
SOFOCLEOUS, ALEXANDER	
ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 04/09/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/322,442	12/29/2005	Rey Bruce	6005.011	5045

TITLE OF INVENTION: MULTIPLE CHIP MODULE AND PACKAGE STACKING METHOD FOR STORAGE DEVICES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$755	$300	$0	$1055	07/09/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

64180 7590 04/09/2010

URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/322,442	12/29/2005	Rey Bruce	6005.011	5045

TITLE OF INVENTION: MULTIPLE CHIP MODULE AND PACKAGE STACKING METHOD FOR STORAGE DEVICES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$755	$300	$0	$1055	07/09/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
SOFOCLEOUS, ALEXANDER	2824	365-063000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/322,442	12/29/2005	Rey Bruce	6005.011	5045

64180 7590 04/09/2010

URIARTE LAW
Attn: Stephen R. Uriarte
2021 The Alameda
Suite 225
San Jose, CA 95126

EXAMINER	
SOFOCLEOUS, ALEXANDER	
ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 04/09/2010

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 304 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 304 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	11/322,442	BRUCE ET AL.	
	Examiner	Art Unit	
	ALEXANDER SOFOCLEOUS	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Amendment filed November 13, 2009*.

2. ☒ The allowed claim(s) is/are *14-16 and 20-31*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Dang T Nguyen/
Primary Examiner, Art Unit 2824

DETAILED ACTION

1. This action is responsive to the following communication: the Amendment filed November 13, 2009.

2. Claims 14-16 and 20-31 are pending. Claims 1-13 and 17-19 are cancelled. Claims 14-16, 20, and 22-27 are currently amended. Claim 14 is independent.

EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Stephen Uriarte (Reg. No. 40,854) on March 18, 2010.

In the Claims, cancel **Claims 1-13** and **17-19**.[1]

In the Claims, **Claim 21**, line 1, change "The method of claim 20" to --The stacked module of claim 20--.

Specification

4. The substitute specification filed February 13, 2009 is acknowledged and acceptable. The proposed specification corrections received on November 13,

[1] While it is noted that each of claims 1-13 and 17-19 have the "(PREVIOUSLY CANCELLED)" status identifier, these claims include claim text and for purposes of promoting clarity during processing, claims 1-13 and 17-19 are formally cancelled by Examiner's Amendment.

2009 are acceptable.

Drawings

5. The replacement drawings (Figs. 1-21b) filed February 13, 2009 are acknowledged and acceptable. The replacement drawings (Figs. 19-21b) filed November 13, 2009 are acknowledged and acceptable.

Allowable Subject Matter

6. **Claims 14-16 and 20-31 are allowed.**

7. The following is an examiner's statement of reasons for allowance:

With respect to independent claim 14, there is no teaching, suggestion, or motivation for combination in the prior art to a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module, and the control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module, in combination with the other limitations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CONCLUSION

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Corisis et al. (U.S. Patent 6,381,141), Sasaki et al. (U.S. Patent 6,624,506), Gheewala (U.S. Patent 6,991,947), Adelmann (U.S. Patent 7,098,541), Koide (U.S. Patent 7,212,422), and Janzen (U.S. Patent 7,352,602).

Corisis et al. teach stacked module with signals serially coupled to each module.

Sasaki et al. teach a multichip memory device having stacked chips

Gheewala teaches plural IC dies with programmable interconnectivity.

Adelmann teaches a stacked die structure with blank pins and select lines.

Koide teaches a stacked memory device wherein each stacked memory chip includes a program circuit to set an address for selecting the chip.

Janzen teaches stacked memory with configurable input/output.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on M-F 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGS

/Dang T Nguyen/
Primary Examiner, Art Unit 2824

Notice of References Cited	Application/Control No. 11/322,442	Applicant(s)/Patent Under Reexamination BRUCE ET AL.	
	Examiner ALEXANDER SOFOCLEOUS	Art Unit 2824	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,381,141	04-2002	Corisis et al.	361/735
*	B	US-6,624,506	09-2003	Sasaki et al.	257/686
*	C	US-6,991,947	01-2006	Gheewala, Tushar	438/15
*	D	US-7,098,541	08-2006	Adelmann, Todd C.	257/777
*	E	US-7,212,422	05-2007	Koide, Yasunori	365/51
*	F	US-7,352,602	04-2008	Janzen, Jeffery W.	365/63
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11322442	BRUCE ET AL.
	Examiner	Art Unit
	ALEXANDER SOFOCLEOUS	2824

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/23/2008	08/07/2008	05/09/2009	03/17/2010					
	1	÷	-	-	-					
	2	÷	-	-	-					
	3	÷	-	-	-					
	4	÷	-	-	-					
	5	÷	-	-	-					
	6	÷	-	-	-					
	7	÷	-	-	-					
	8	÷	-	-	-					
	9	÷	-	-	-					
	10	÷	-	-	-					
	11	÷	-	-	-					
	12	÷	-	-	-					
	13	÷	-	-	-					
1	14	÷	✓	✓	=					
2	15	÷	✓	✓	=					
9	16	÷	✓	✓	=					
	17	÷	N	✓	-					
	18	÷	N	✓	-					
	19	÷	N	✓	-					
11	20	÷	✓	✓	=					
12	21	÷	✓	✓	=					
3	22	÷	✓	✓	=					
10	23	÷	✓	✓	=					
13	24	÷	N	✓	=					
14	25	÷	N	✓	=					
15	26	÷	N	✓	=					
4	27			✓	=					
5	28			✓	=					
6	29			✓	=					
7	30			✓	=					
8	31			✓	=					

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11322442	BRUCE ET AL.
	Examiner	Art Unit
	ALEXANDER SOFOCLEOUS	2824

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
365	51	G 1 1 C 5 / 02 (2006.01.01)	

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
257	686	777			
365	63	230.03	230.05		

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17												
	2		18												
	3		19												
	4	11	20												
	5	12	21												
	6	3	22												
	7	10	23												
	8	13	24												
	9	14	25												
	10	15	26												
	11	4	27												
	12	5	28												
	13	6	29												
1	14	7	30												
2	15	8	31												
9	16														

/ALEXANDER SOFOCLEOUS/ Examiner.Art Unit 2824 (Assistant Examiner)	03/19/2010 (Date)	**Total Claims Allowed:** 15
/DANG T NGUYEN/ Primary Examiner.Art Unit 2824 (Primary Examiner)	03/26/2010 (Date)	O.G. Print Claim(s) 1 O.G. Print Figure 21b

U.S. Patent and Trademark Office

Part of Paper No. 20100317

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11322442	BRUCE ET AL.
	Examiner	Art Unit
	ALEXANDER SOFOCLEOUS	2824

SEARCHED			
Class	Subclass	Date	Examiner
257	686	5/9/2009	EU
257	686, 777	03/17/2010	AGS
365	51, 63, 230.03, 230.05	03/17/2010	AGS

SEARCH NOTES		
Search Notes	Date	Examiner
EAST database serarch	5/9/2009	EU
consulted VanThu Nguyen regarding class 365	03/16/2010	AGS
see updated EAST search history	03/17/2010	AGS

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
257	686, 777	03/17/2010	AGS
365	51, 63, 230.03, 230.05	03/17/2010	AGS

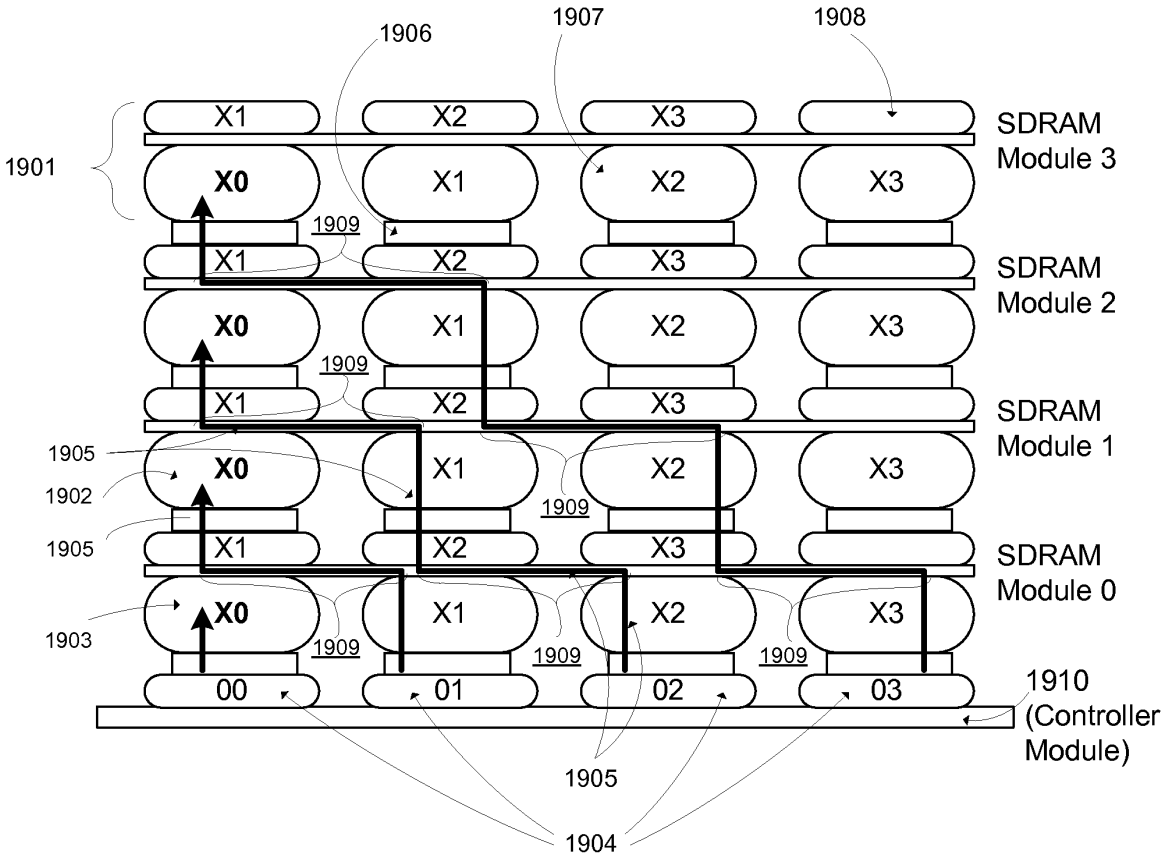

1906
1907
1908
1901
X1
X2
X3
X0
SDRAM Module 3
SDRAM Module 2
SDRAM Module 1
SDRAM Module 0
1909
1905
1902
1903
00
01
02
03
1910 (Controller Module)
1904

Figure 19

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S5	941	S2 S3 memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/01 14:38
S4	1182	S2 S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/01 14:38
S3	33158	(module with stack$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/01 14:38
S2	13942	((257/686) or (365/51,52,63,230.03,230.05)).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/03/01 14:38
S6	1	S2 S3 memory (serial adj chain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/01 14:39
S7	4	(("6469375") or ("5995379") or ("6172874") or ("6900528")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/01 15:04
S8	316	S2 S3 memory (pad with ball)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/01 15:39
S11	2974	(257/777).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/03/01 15:43
S10	1042	(257/776).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/03/01 15:43

S9	3813	(257/774).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/03/01 15:43
S14	160	S11 S3 memory (pad with ball)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/01 15:44
S13	3	S10 S3 memory (pad with ball)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/01 15:44
S12	29	S9 S3 memory (pad with ball)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/01 15:44
S15	1	(10/382020).APP.	USPAT; USOCR	AND	ON	2010/03/01 15:48
S16	14	("5216278" | "5506756" | "5521435" | "5640048" | "5734201" | "5835355" | "5895231" | "6078506" | "6313522" | "6381141" | "6388333" | "6479758").PN. OR ("6791193").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/01 15:49
S17	1	(S2 or S9 or S10 or S11) S3 (passive adj2 (port or pad or ball))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/01 15:50
S18	10	("20050044305" | "6313522" | "6603198" | "6740546" | "6791193" | "6977440" | "7193306" | "7279786" | "7335995").PN. OR ("7439615").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/01 15:53
S19	104	("5012323" | "5121293" | "5128831" | "5189505" | "5289337" | "5291061" | "5323060" | "5385869" | "5422435" | "5434745" | "5474957" | "5495398" | "5513076" | "5607099" | "5963430" | "6020629").PN. OR ("6313522").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/01 15:54
S20	147	("20020074669" | "20030111709" | "20030218235" | "20040018693" | "20040031972" | "20040257780" | "3390308" | "3614832" | "3683105" | "3832769" | "3868724" | "3923359" | "4216577" | "4371744" | "4371912" | "4489364" | "4540226" | "4551746" | "4558397" | "4627151" | "4628406" | "4638348" | "4681654" | "4685998" | "4701999" | "4710798" | "4734825" | "4746392" | "4754316" | "4761681" | "4772936" | "4812421" | "4823234" | "4829666" | "4837184" | "4841355" |	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/01 15:56

		"4855867" | "4855868" | "4868712" | "4878098" | "4893172" | "4897534" | "4897918" | "4918811" | "4937203" | "4956694" | "4967261" | "4982265" | "4994902" | "4996583" | "4996587" | "4999319" | "5028986" | "5029325" | "5037779" | "5045921" | "5055913" | "5117282" | "5127570" | "5128831" | "5138438" | "5148265" | "5148266" | "5172303" | "5198888" | "5222014" | "5247423" | "5258330" | "5266912" | "5281852" | "5289346" | "5304252" | "5304512" | "5311401" | "5313096" | "5334875" | "5337077" | "5346861" | "5350947" | "5376825" | "5379191" | "5384689" | "5390844" | "5394009" | "5397916" | "5397921" | "5409865" | "5412247" | "5455740" | "5479318" | "5489749" | "5543664" | "5548091" | "5552631" | "5552963" | "5564181" | "5600541" | "5608265" | "5616958" | "5625221" | "5637536" | "5639695" | "5642261" | "5656856" | "5659952" | "5663106" | "5668405" | "5677566" | "5681777" | "5701031" | "5734555" | "5751063" | "5783870" | "5784264" | "5801439" | "5804874" | "5834339" | "5835988" | "5844315" | "5861666" | "5883426" | "5912507" | "6030856").PN. OR ("6072233" | "6093029" | "6108212" | "6180881" | "6195268" | "6218848" | "6232152" | "6268649" | "6272744" | "6291259" | "6303997" | "6313522" | "6335565" | "6342728" | "6369445" | "6388264" | "6462421" | "6496026" | "6515870" | "6555918" | "6740981").PN. OR ("7335995").URPN.				
S21	8	(passive adj port) same memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 08:25
S22	6	(passive adj port) (stack$4 with memory)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 08:26
S23	1	11/322442	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 08:29
S24	1495	(memory with module with stack$4) (rout $3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 12:19

S26	10	(memory with module with stack$4) same (port with rout$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 13:42
S25	162	(memory with module with stack$4) same (rout$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 13:42
S28	8	(memory with module with stack$4) same (rout$3) same serial$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 13:43
S27	8	(memory with module with stack$4) same (rout$3) same serial	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 13:43
S29	18	("20040030794" | "20040183795" | "20050166026" | "20050198458" | "20060020740" | "20060024541" | "6295586" | "6502161" | "6571325" | "6725314" | "6882082" | "6889304" | "6922770" | "6941428" | "7017022" | "7032092" | "7051151" | "7257129").PN. OR ("7409491").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/15 13:45
S30	2	("20050047250").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/03/15 13:53
S32	13	("20030061447" | "6233650" | "6349050" | "6530033").PN. OR ("7078793").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/15 13:56
S31	1	(10/927312).APP.	USPAT; USOCR	AND	ON	2010/03/15 13:56
S33	15	("20050086417" | "20050138267" | "20050259504" | "20050273679" | "20050278495" | "20070189049" | "6754117" | "6820181" | "6901475" | "6979895" | "6982892" | "6993612" | "7078793").PN. OR ("7471538").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/15 13:59
S34	70	("3654394" | "4513368" | "4645944" | "4985703" | "5261068" | "5289062").PN. OR ("6233650").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/15 14:01
S36	6	(memory with module with stack$4) (reconfigur$4 with rout$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 14:11

S35	0	(memory with module with stack$4) same (reconfigur$4 with rout$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 14:11
S37	26	(memory with module with stack$4) same reconfigur$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 14:13
S38	164	("4754316" | "4983533" | "5019943" | "5311401" | "5313096").PN. OR ("5432729").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/15 14:18
S39	53	("5585675" | "5652904" | "5838060" | "6051887" | "6092174" | "6313522" | "6449170").PN. OR ("6627985").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/15 14:24
S40	53	("5585675" | "5652904" | "5838060" | "6051887" | "6092174" | "6313522" | "6449170").PN. OR ("6627985").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/15 14:25
S41	2	("6747478").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/03/15 14:26
S42	17	("5798282" | "5946545" | "6545501" | "6614267" | "6627985" | "6861865").PN. OR ("6991947").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/15 14:31
S43	32	("4574331" | "4727410" | "4813129" | "5007841" | "5016138" | "5051865" | "5177594" | "5224918" | "5252857" | "5281852" | "5311401" | "5327327" | "5343075" | "5406565" | "5414637" | "5432729" | "5434745" | "5502333" | "5561593" | "5686843" | "5691041").PN. OR ("5781413").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/15 14:46
S44	33	("4574331" | "4727410" | "4813129" | "5007841" | "5016138" | "5039628" | "5051865" | "5177594" | "5224918" | "5252857" | "5281852" | "5311401" | "5327327" | "5343075" | "5414637" | "5432729" | "5434745" | "5477933" | "5483421").PN. OR ("5815374").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/15 14:47
S45	8	(memory with module with stack$4) same ((re$1rout$3 or re$1configur$4 or re $1program$4) near4 interconnect$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/15 14:53
S46	15	(memory with module with stack$4) same ((re$1rout$4 or re$1configur$4 or re $1program$5 or rout$4 or configur$4 or program$5) near4 interconnect$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 08:26

L2	211	(memory with module with stack$4) same (re$1rout$3 or rout$3 or ((program$5 or re $1program$5 or configur$4 or re$1configur $4) with interconnect$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/17 14:44

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	14	(memory with module with stack$4) same ((re $1rout$4 or re$1configur$4 or re$1program$5 or rout$4 or configur$4 or program$5) near4 interconnect$4)	US-PGPUB; USPAT; UPAD	AND	ON	2010/03/17 14:43
L4	18186	((257/686,773,777) or (365/51,52,63,230.03,230.05)).CCLS.	US-PGPUB; USPAT; UPAD	OR	OFF	2010/03/17 14:44
L3	204	(memory with module with stack$4) same (re $1rout$3 or rout$3 or ((program$5 or re $1program$5 or configur$4 or re$1configur$4) with interconnect$3))	US-PGPUB; USPAT; UPAD	AND	ON	2010/03/17 14:44
L5	58	3 4	US-PGPUB; USPAT; UPAD	AND	ON	2010/03/17 14:45

3/17/2010 2:50:38 PM
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**** CONTINUING DATA **************************

**** FOREIGN APPLICATIONS **************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **
02/10/2006

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /ALEXANDER SOFOCLEOUS/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	28	26	2

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TITLE

Multiple chip module and package stacking method for storage devices

FILING FEE RECEIVED		
702	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: BRUCE et al.	Group Art Unit: 2892
Serial No.: 11/322,442	Examiner: ULLAH, Elias
Application Filing Date: 29 Dec 2005	
For: MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND REPLY TO SECOND OFFICE ACTION

Dear Examiner:

In response to the Office Action, mailed 13 May 2009, please kindly amend this Application as follows and consider the remarks set forth below.

Amendments to the Specification begin on page 2;

A listing of claims begins on page 7;

Amendment(s) to the Drawings begins on page 19; and

Remarks begin on page 21 of this paper.

Replacement sheets of drawings incorporating the changes proposed in the Amendments to the Drawings and corresponding to the written description, respectively, are attached to this paper.

Amendments to the Specification

Text in underline indicates new text, while text in strike-out format or between a pair of double brackets indicates deletion of the text.

In the Specification, as previously amended, please enter the amendments shown with respect to the replacement paragraphs identified below.

Please replace the title on page 1, lines 1-2, with the following replacement title.

Multiple Chip Module and Package Stacking For Storage Devices

Please replace the paragraph on page 8, line 13 through 15, with the following replacement paragraph.

Figure 21a shows another pin assignment and connection technique for creating ~~be able to connect~~ a serial chain route through ~~from~~ multiple modules in a stack by connecting a set of serial chain connections, according to another ~~example~~ embodiment of the present invention.

Please replace the paragraph on page 20, line 19 through page 21, line 16, with the following replacement paragraphs.

Figure 19 shows a first pin assignment and connection technique that enables a selection of specific module in a multiple module stack. The figure illustrates the controller and SDRAM modules as an example. The SDRAM module balls, such as **1907**, are represented by big oblong shapes, and the pads such as **1908** are represented by smaller oblong shapes. A pad to ball connection is represented by a rectangle, such as **1906**. The controller module has four active pads such as **1904,** one each for the four SDRAM modules such as **1901**. An active pad may be also

referred to herein as an "active port". The controller module's active pad 00 **1904** is ultimately connected to ~~SDRAM module 0's~~ X0 ball **1903** of SDRAM module 0, active pad 01 is connected to ~~SDRAM module 1's~~ X0 ball **1902** of SDRAM module 1, and so on. These[[The]] X0 balls are the active balls for these[[the]] SDRAM modules. Thus, as illustrated in Figure 19, there is one active ball, such as X0, ultimately coupled to one active pad per module.

All SDRAM modules are identical, and in the example shown in Figure 19, [[which]] include the following connections ~~as follows~~: an X1 passive ball is connected to an X1 passive pad, an X2 passive ball to X2 passive pad, and so on. The connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module, such as the X1 passive ball and X1 passive pad connection in Figure 19, is named "passive port", such as passive ports 1909 illustrated in Figure 19. The technique involves using a ladder-like routing path, such as **1905** on the stacked modules. This technique enables the controller module's active pad to be routed to the desired specific module in the stack. Thus, an active signal applied at an active pad, such as active pad 02, shown with reference number 1904 on controller module 1910, is routed through at least one passive port connecting a passive ball and passive pad, such as the passive ports 1905 connecting passive ball X2 to passive pad X2 and passive ball X1 to passive pad X2, respectively, so that this active signal eventually reaches an active ball, such as X0 ball SDRAM Module 2 in fig. 19. The example embodiment illustrated in Figure~~figure~~ 19 comprises a repeating pattern for the balls and pads. Passive balls are connected within each module to passive pads with an offset distance equaling one periodic distance of the repeating pattern. For example in Figure 19, an X1 passive ball is connected to an X1 passive pad, X2 passive ball to X2 passive pad, etc. ~~The importance is the approach~~ By using repeating patterns and offsetting of the passive ball to passive pad within each module, other offset distances

can be used [[also]] in alternative~~other~~ embodiments of the present invention.[[,]] ~~e.g.~~ For example, an alternative embodiment may include using an offset of two or any multiple of the periodic distance of the repeating pattern. This[[The]] alternative ~~example~~ embodiment is not intended to~~does not~~ limit the scope of the present invention in any way.

Please amend the paragraph on page 23, line 1 through page 24, line 6, with the following replacement paragraphs.

The last connection technique is used for serial routing of all modules in the stack and allowing them to be externally accessible for horizontal expansion on a PCB, such as a main board. Figure 21a shows how this technique is implemented in the stacking method. The main board **2101** [[ ]]contains the input signals **2102** which will then be connected to IN ball **2104** of the base module **2103**. The modules, including base module **2103**, stack modules **2106** and **2130**, and an end module, such as top module **2108**, each have a ball and a pad that are coupled together by a serial chain circuit. For example, base module **2103** includes a serial chain circuit **2127** that couples IN ball **2104** with OUT pad **2105**, and a serial chain circuit **2136** that couples OUT pad **2137** with OUT ball **2138**; module **2106** includes a serial chain circuit **2128** that couples IN ball **2107** with OUT pad **2129**, and a serial chain circuit **2139** that couples OUT pad **2140** with OUT ball **2141**; module **2130** includes a serial chain circuit **2131** that couples IN ball **2132** with OUT pad **2133**, and a serial chain circuit **2142** that couples OUT pad ball **2143** with OUT ball **2144**; and top module **2108** includes a serial chain circuit **2134** that couples IN ball **2135** with OUT pad **2109** and a serial chain circuit **2145** that couples OUT pad **2110** with OUT ball **2113**. Thus, the[[The]] base module's OUT pad **2105** is connected to IN ball **2107** of the first stack module **2106**, and so on.

A signal route that includes a serial chain circuit coupling an ball and pad is herein after referred to as a "serial chain connection", and at least two serial chain connections connected in

series are herein after referred to as a "serial chain route", such as serial chain route **2146** or **2111**. The top module **2108**[[,]] terminates the signal to the top pad **2109** and routes, with connection **2112,** the signal internally to another pad, such as OUT pad **2110,** which is connected directly to the ball [[**2113**]] underneath, such as OUT ball **2113**. Since the modules are identical, this routed signal passes through another set of [[the]] serial chain connections that comprise another serial chain route, such as serial chain route ~~pads and balls~~ **2111** for[[of]] the stack until it reaches the OUT pad **2114** of the main board for external access. A serial chain connection includes a serial chain input and a serial chain output. A serial chain input is disposed to receive a signal, while a serial chain output is disposed to provide the signal. For example in Figure 21a, IN balls **2104**, **2107**, **2132**, and **2135**, and OUT pads **2110**, **2143**, and **2140** are serial chain inputs, respectively. OUT pads **2105**, **2129**, **2133**, and **2109**, and OUT balls **2113**, **2144**, **2141**, and **2138** are serial chain outputs, respectively. At least one of the balls and pads that are coupled to their respective chain circuit may be in the form of a passive ball and passive pad, respectively, since an active signal, such as signal **2102**, applied at active pad **2101**, can be routed through a series of serial chain circuits that couple respective balls and pads. In effect, each of these serial chain circuits functions as a passive port. A serial chain circuit, however, can also terminate a serial chain route, such as serial chain route **2146**, and branching or routing this serial chain route to another pad that functions as a serial chain input of another serial chain route, such as serial chain route **2111**, as described further below.

Regarding~~How~~ the top module, ~~terminates~~ the serial chain termination and branching~~es them out~~ to other pads is shown in Figure 21b. All modules have a control circuit that includes a selectable buffer **2115** that tri-states the input when pulled low. The signal from the IN balls **2116** enters the internal circuit **2117** and exits the circuit connecting to the OUT pad **2118**. The buffer's **2115** control line is weakly pulled up internally. The "StkLow" ball is connected internally to

GND **2119**, thus pulling down the buffer control line when a module is stacked above it, and it is pulled up when no module is stacked directly above it. When the buffer control line is pulled high, it will let the input signal branch out **2120** to the other pads, thus creating a connection route or trace that loops back to the base module solder balls. When a module is stacked above a module that is disposed with selectable buffer **2115** in the manner shown, the buffer control signal is pulled low, tri-stating the input signal and disallowing the branching effect. This technique allows the signal to be accessible to the external balls of the base module, thus horizontal expansion for a serial signal is achievable. The balls are then routed, with connection **2121,** to the other modules **2122** on the other locations. The same technique is used on the main board **2123**, when no package is detected on the "StkLow" pad, the buffer allows the input to connect to the designated pads on the other locations. The tri-stated buffer technique is redundant to all locations. An example is the JTAG TDI-TDO signal. The driver [[diver]] circuit **2125** sends out TDI signals to the pads and the closing TDO signal **2124** loops back to the driver circuit.

Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (PREVIOUSLY CANCELLED) A method for stacking a plurality of modules comprising the steps of:

providing one or more active port on the plurality of modules for carrying one or more active signal;

providing one or more passive port on the plurality of modules for passing through the one or more active signals; and

stacking the plurality of modules.

2. (PREVIOUSLY CANCELLED) The method of claim 1 wherein the one or more passive port forms a ladder like routing path.

3. (PREVIOUSLY CANCELLED) The method of claim 1 wherein one or more of the plurality of module is rotated before being stacked and the one or more passive port forms a rotational routing path.

4. (PREVIOUSLY CANCELLED) The method of claim 1 further comprising the step of providing one or more pair of daisy chain input port and daisy chain output port for forming a first daisy chain connection wherein each pair of the daisy chain input port and the daisy chain output port are connected through a daisy chain circuit.

5. (PREVIOUSLY CANCELLED) The method of claim 4 further comprising the step of providing one or more control port for enabling a routing path extending the first daisy chain connection within an end module.

6. (PREVIOUSLY CANCELLED) The method of claim 5 wherein the routing path within the end module is connected to a second daisy chain connection.

7. (PREVIOUSLY CANCELLED) The method of claim 1 wherein one or more of the plurality of modules is a main board.

8. (PREVIOUSLY CANCELLED) The method of claim 7 wherein one or more vertically stacked module is connected to the main board.

9. (PREVIOUSLY CANCELLED) The method of claim 2:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located between a pre-determined distance to each other in a repeating pattern, the pre-determined distance equaling a multiple of a

periodic distance of the repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the ladder like routing path; and

wherein the ladder like routing path comprises one or more passive ball and one

or more passive pad.

10. (PREVIOUSLY CANCELLED) The method of claim 3:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located opposite each other in a repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the rotational routing path; and

wherein the rotational routing path comprises one or more passive ball and one

or more passive pad.

11. (PREVIOUSLY CANCELLED) The method of claim 4:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive

pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection; and

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad.

12. (PREVIOUSLY CANCELLED) The method of claim 5:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive

pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad; and

wherein the routing path comprises one or more tri-state driver controlled by the one or more control port.

13. (PREVIOUSLY CANCELLED) The method of claim 6:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive

pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad;

wherein the routing path comprises one or more tri-state driver controlled by the one or more control port; and

wherein one or more daisy chain connection are extended through one or more vertically stacked module connected to a main board.

14. (CURRENTLY AMENDED) A stacked module comprising a plurality of modules each comprising:

one or more active ports for carrying one or more active signal; [[and]]

one or more passive ports for passing through the one or more active signals;[[.]]

a first serial chain route that includes at least one serial chain connection, the serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output; said serial chain input coupled to said serial chain output through said serial chain circuit;

a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module; and

said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module.

15. (CURRENTLY AMENDED) The stacked module of claim 14 wherein the one or more passive port forms a ladder like routing path, and the passive port connects a passive ball on one surface of a module to a passive pad on another surface of the module.

16. (CURRENTLY AMENDED) The stacked module of claim 14 wherein one or more of the plurality of modules is rotated before being stacked and the one or more passive port forms a rotational routing path.

17. (CANCELLED) The stacked module of claim 1 further comprising one or more pair of daisy chain input port and daisy chain output port for forming a first daisy chain connection wherein each pair of the daisy chain input port and the daisy chain output port are connected through a daisy chain circuit.

18. (CANCELLED) The stacked module of claim 17, further comprising one or more control port for enabling a routing path extending the first daisy chain connection within an end module.

19. (CANCELLED) The stacked module of claim 18 wherein the routing path within the end module is connected to a second daisy chain connection.

20. (CURRENTLY AMENDED) The stacked module of claim 14 wherein one or more of the plurality of modules includes ~~is~~ a main board.

21. (ORIGINAL) The method of claim 20 wherein one or more vertically stacked module is connected to the main board.

22. (CURRENTLY AMENDED) The stacked module of claim 15:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located between a pre-determined distance to each other in a repeating pattern, the pre-determined distance equaling a multiple of a periodic distance of the repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the ladder like routing path; and

wherein at least one of the ~~ladder like routing path comprises~~ one or more passive ball and one or more passive pad forms a ladder like routing path.

23. (CURRENTLY AMENDED) The stacked module of claim 16:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located opposite each other in a repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the rotational routing path; and

wherein at least one of the ~~rotational routing path comprises~~ one or more passive ball and one or more passive pad form a rotational routing path.

24. (CURRENTLY AMENDED) The stacked module of claim 14[[17]]:

wherein each of the plurality of modules comprises a first side and a second side, and the one or more passive ports includes a first passive port connected to a passive ball disposed on the first side and to a passive pad disposed on the second side of a module from the plurality of modules;

wherein the ~~one or more~~ serial[[daisy]] chain input ~~port is~~ includes ~~connected to~~ the ~~one or more~~ passive ball ~~on the first side~~ and the ~~one or more~~ serial ~~daisy~~ chain output ~~port~~ includes the ~~is connected to one or more~~ passive pad ~~on the second side of one or more corresponding module~~;

wherein ~~each of~~ the ~~one or more~~ passive ball and ~~each of~~ the ~~one or more~~ passive pad ~~corresponding to a same daisy chain port~~ are located opposite each other; and

further including a base module having an active port for providing a signal, said signal routed to a same location on the plurality of modules through the first serial chain route.

~~wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection; and~~

~~wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad.~~

25. (CURRENTLY AMENDED) The stacked module of claim 14[[18]]:

~~wherein each of the plurality of modules comprises a first side and a second side;~~

~~wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;~~

~~wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;~~

~~wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;~~

~~wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad; and~~

wherein the routing path includes ~~comprises~~ one or more tri-state driver controlled by the ~~one or more~~ control circuit ~~port~~.

26. (CURRENTLY AMENDED) The stacked module of claim 25[[19]] further including:

~~wherein each of the plurality of modules comprises a first side and a second side;~~

~~wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module~~;

~~wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;~~

~~wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;~~

~~wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad;~~

~~wherein the routing path comprises one or more tri-state driver controlled by the one or more control port;~~

~~wherein one or more daisy chain connection are extended through one or more vertically stacked module connected to a main board.~~

a main board coupled to another stacked module having a third serial chain route; and

another control circuit for enabling another routing path that connects the second serial chain route with the third serial chain route.

27. (CURRENTLY AMENDED) The stacked module of claim 15, wherein:

the stacked module further includes a first outside surface and a second outside surface, the first and second outside surfaces disposed to face opposite each other; and

at least one of the plurality of modules includes a first module having a first target location terminating between the first and second outside surfaces.

28 (PREVIOUSLY ADDED) The stacked module of claim 27, wherein the plurality of modules further includes a second module and a third module, the

second module including a second module surface that includes the first outside surface and the third module including a third module surface that includes the second outside surface.

29. (PREVIOUSLY ADDED) The stacked module of claim 15, further including a second ladder like routing path; and wherein:

the plurality of modules includes a first module and a second module, the first and second modules respectively including a first target location and a second target location, the second target location located within the stacked module; and

the ladder like routing path for routing one of the active port to the first target location, and the second ladder like routing path for routing another one of the active port to the second target location.

30. (PREVIOUSLY ADDED) The stacked module of claim 29, further including a second ladder like routing path; and wherein:

the stacked module includes a first outside surface and a second outside surface, the first and second outside surfaces disposed to face opposite each other;

the ladder like routing path terminates at the first target location; and

the second ladder like routing path terminates at the second target location, the second target terminating within the stacked module and located between the first and second outside surfaces;

31. (PREVIOUSLY ADDED) The stacked module of claim 29, wherein the second target location is located between the first and second outside surfaces.

Amendment(s) to the Drawings

The following proposed amendments to the Drawings are provided in the form of replacement drawing sheets, which are each labeled "Replacement Sheet" in their respective page headers pursuant to 37 CFR 1.84(c). Support for the amendments below is provided on pages XX in the Substitute Specification previously submitted on 12 February 2009. No new matter has been added.

Figure 19 has been amended as described below.

A set of parenthesis has been placed around the text "Controller Module".

Reference number "1910" has been placed above the text "(Controller Module)".

Multiple instances of reference number "1909" has been inserted as shown in the Replacement Sheet; Reference number "1909" corresponds to the element named "passive port" in the Specification as amended at p. 22.

Multiple instances of reference number "1904" has been inserted to the drawing elements annotated with "01", "02", and "03", and referred to in the Specification as "active pads" or "active ports" at p. 21.

Figure 21a in drawing sheet 27/28 has been amended as described below:

Element numbers 2103, 2106, and 2108 have been moved from the left to the right side of the Drawing sheet.

Element numbers 2127 through 2135, inclusive, element numbers 2137, 2138, 2140, 2141, and 2143 have been added as shown.

Drawing elements corresponding to new element numbers 2136, 2139, 2142, 2145, 2146 have been added.

Drawing element corresponding to element number 2111 has been adjusted in length and position as shown.

The figure in drawing sheet 28/28 has been amended by replacing the figure label "Figure 21a" to "Figure 21b". The drawing on drawing sheet 28/28 as originally filed was represented with the figure label of "Figure 21b" but the Amendments to the Drawings submitted on 13 February 2009 was inadvertently amended to include "Figure 21a".

Remarks

The specification and drawings have been amended to correct minor errors noted in the Office Action and otherwise. These corrections are of a clerical nature and do not add "new matter".

Claims 1 and 13 have been previously cancelled without prejudice.

Claims 14-16, 20 and 22-27 are amended.

Claims 17-19 are cancelled without prejudice.

The text of original claim 21 and of previously added claims 28-31 remain unchanged but their meaning have changed because they depend from amended claims.

Request for Acknowledgement and Acceptance of Substitute Drawings Submitted on 13 February 2009

In the Office Action, the drawings filed on "29 December 2005", named the "Acknowledgment Date", were "accepted" by the Examiner. Applicants kindly note that the Drawings were amended and provided in the form of Replacement Sheets, collectively referred to herein as the "Amended Drawings", with the USPTO by the Applicants through the Response and Amendment to Office Action submitted with the USPTO on 13 February 2009, named the "Prior Response". The Acknowledgment Date used in the Office Action, however, reflects the original Application filing date of this application and thus, refers to the original Drawings rather than the Amended Drawings. With due respect, the Acknowledgement seems to be inadvertent, and consequently, Applicants request that the Amended Drawings previously submitted

in the Prior Response also be reviewed and acknowledged if applicable.

Amendments to The Current Drawings

Figures 19 and 21a, and the Figure on sheet 28/28 have been amended, and are provided in the form of replacement drawing sheets in accordance with 37 CFR 1.121. These amendments are described in detail in the "Amendments to the Drawings" section above.

Examiner Interview Conducted on 8 May 2009

Withdrawn claims 17-19 and 24-26 have been reconsidered by the Examiner because claim 17 has been amended to depend from claim 14 instead of claim 1 during the telephone interview, named "Examiner Interview", conducted between the undersigned and the Examiner on 8 May 2009. Accordingly, claims 17-19 and 24-26 have been entered for further consideration by the Examiner. The undersigned on behalf of the applicants extend much thanks to the Examiner for his responsiveness during the Examiner Interview.

The First 35 USC §112, Second Paragraph, Rejection

Claims 14-26 are rejected under 35 USC, second paragraph, as being indefinite for failing to particularly point out and distinctly claiming the subject matter which the applicant regards as the invention. The Applicants respectfully traverse this rejection.

In the Office Action, it is asserted that in:

base claim 1, applicants claimed "one or more passive port for passing though the one or more active signals". However, in light of applicants'

> discloser, as it would be interpreted by one of ordinary skill in the art, above claim limitations do not set out and define the invention with a reasonable degree of precision and particularity. For purpose of examination, Examiner assumes the "passive port" is a connection on active port for carrying signal.

Definiteness of claim language must be analyzed, not in a vacuum, but in light of Applicants written disclosure, the prior art, and the claim interpretation that would be given by one of ordinary skill in the art at the time the invention was made. MPEP 2173.02. Applicants may be their own lexicographers. MPEP 2173.01. The Specification at p. 21, line 7 through p. 22, line 4, as amended in the "Amendments to the Specification" section above, recites in part:

> …A ***connection*** between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module, such as the X1 passive ball and X1 passive pad connection in Figure 19, is named "passive port", such as passive ports 1909 illustrated in Figure 19. (Emphasis added).

The above description should be read in conjunction with amended Figure 19, which shows that a passive port 1909 ***connects*** "a passive ball", such as passive ball X2, "on one surface of a SDRAM module", such as SDRAM module 0, and a passive pad", such as passive pad X3, "on another surface of the same DRAM module", such as SDRAM module 0. Thus, "a connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module" is a "passive port". The above amendments render moot the First 35 USC § 112,

Second Paragraph rejection as to claims 14-26, and the Specification and claims now comply with the statutory requirements.

In order to properly provide a complete response to the Office Action, please kindly note that the Office Action refers to "base claim 1". The applicants believe that this reference to "base claim 1" is inadvertent because base claim 1 has been withdrawn from consideration due to the earlier received Restriction Requirement, and consequently, the applicants have responded to this rejection with respect to base claim 14 from which claims 15 through 26 depend.

The Second 35 USC §112, Second Paragraph, Rejection

Claims 22-26 are rejected under 35 USC, second paragraph, as being indefinite for failing to particularly point out and distinctly claiming the subject matter which the applicant regards as the invention. The Applicants respectfully traverse this rejection.

In the Office Action, it is asserted that

> in claims 22-23, applicants claimed "one or more passive ball and one or more passive pad". However, in light of applicants' discloser, as it would be interpreted by one of ordinary skill in the art, above claim limitations do not set out and define the invention with a reasonable degree of precision and particularity. For purpose of examination, Examiner assumes the "passive port inherently comprises passive ball and passive pad".

The Specification as amended beginning from p. 21, line 7 through p. 22, line 4,

recites in part:

> …A ***connection*** between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module, such as the X1 passive ball and X1 passive pad connection in Figure 19, is named "passive port", such as passive ports 1909 illustrated in Figure 19. (Emphasis added).

The above description should be read in conjunction with amended Figure 19, which shows that a passive port 1909 ***connects*** "a passive ball", such as passive ball X2, "on one surface of a SDRAM module", such as SDRAM module 0, and a passive pad", such as passive pad X3, "on another surface of the same DRAM module", such as SDRAM module 0. Thus, the recitation of "one or more passive ball and one or more passive pad" by the rejected claims particularly points out and distinctly claims the invention. By these amendments, the Second 35 USC § 112, Second Paragraph rejection has been rendered moot as to claims 14-26, and the Specification and claims now comply with the statutory requirements.

The Third 35 USC §112, Second Paragraph, Rejection

Claims 17-19 and 24-26 are rejected under 35 USC, second paragraph, as being indefinite for failing to particularly point out and distinctly claiming the subject matter which the applicant regards as the invention. The Applicants respectfully traverse this rejection.

In the Office Action with respect to claim 17, it is asserted that:

> …applicants claimed "one or more pair of daisy chain input port and daisy chain output port ". However, in light of applicants' discloser, as it would be interpreted by one of ordinary skill in the art, above claim limitations do not set out and define the invention with a reasonable degree of precision and particularity. For purpose of examination, Examiner assumes the "limitation associated with daisy chain will read as ladder like routing path connection".

The Specification at page 23, line 14 through page 24, line 20; Figure 21a; and the above claims have been amended so that these claims now particularly point out and distinctly claim the subject matter regarded as the invention by the Applicants. Support for the amendment made in the Specification is supported by the originals claims, including claim 17, 18, 24, and 25. The Specification and these claims now comply with the statutory requirements, rendering the Third Section 112 Rejection moot.

The First 35 USC §102 Rejection

Claims 14-15 and 17-31 are rejected under 35 USC 102(b) as being anticipated by Kyougoku et al. (Kyougoku, US 5,995,379) of record.

The First 35 USC §102(b) Rejection

In the Office Action, claims 14-15 and 17-31 have been rejected under 35 USC 102(b) as being allegedly anticipated by Kyougoku et al. (Kyougoku, US 5,995,379) of record. This rejection is respectfully traversed.

In the Office Action it is asserted that with respect to claim 14, "Kyougoku

shows a stacked module (Fig. 5) comprising: one or more active port (B1) for carrying one or more active signal (Fig. 5); and one or more passive port (L1, L4) for passing through the one or more active signals (Fig. 5).

Independent Claim 14

Amended claim 14, recites in part:

> a first serial chain route that includes at least one serial chain connection, the serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output; said serial chain input coupled to said serial chain output through said serial chain circuit;
>
> a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module; and
>
> said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module.

Kyougoku fails to teach or disclose the above claim limitations, and hence, claim 14 is allowable.

Dependent Claim 15

In the Office Action it is also asserted that with respect to claim 15, "Kyougoku shows the one or more passive port forms a ladder like routing path (L1-L6)." Applicants respectfully traverse this rejection.

Claim 15 depends on allowable base claim 14. Thus, claim 15 is also allowable for the same reasons stated for base claim 14 since an allowable base claim renders its dependent claim(s) also allowable.

Dependent Claims 17-19

Dependent claims 17-19 have been cancelled without prejudice. In addition, claim 14, recites additional claim limitations that are not shown or disclosed by the arguments presented in the Office Action with respect to claims 17-19. For example, claim 14, recites a "control circuit disposed to enable the routing path in response to a control input signal", which is not shown in Kyougoku. Consequently, claim 14 is also allowable for this additional reason.

Dependent Claims 20-21

Claims 20-21 ultimately depend on allowable base claim 14. Thus, claims 20-21 are also allowable for the same reasons stated for base claim 14 above since an allowable base claim renders its dependent claims also allowable.

Dependent Claims 22-23

Claims 22-23 ultimately depend on allowable base claim 14. Thus, claims 22-23 are also allowable for the same reasons stated for base claim 14 above since an allowable base claim renders its dependent claims also allowable.

Dependent Claims 24-26

Claims 24-26 ultimately depend on allowable base claim 14. Thus, claims 24-26 are also allowable for the same reasons stated for base claim 14 above since an allowable base claim renders its dependent claims also allowable.

In addition, claim 25 recites in part, "wherein the routing path includes one or more tri-state driver controlled by the control circuit", which is not taught or disclosed in Kyougoku. For this additional, reason claim 25 is allowable.

In addition, claim 26 recites one or more additional claim limitations that are not disclosed or taught in Kyougoku. For example, claim 26 recites in part, "a main board coupled to another stacked module having a third serial chain route". In another example, claim 26 recites in part, "another control circuit for enabling another routing path that connects the second serial chain route with the third serial chain route". Consequently, since Kyougoku does not disclose or teach one or both of these additional claim limitations, claim 26 is allowable for these additional reasons.

Dependent Claims 27-31

Claims 27-31 ultimately depend on allowable base claim 14. Thus, claims 27-31 are also allowable for the same reasons stated for base claim 14 above since an allowable base claim renders its dependent claims also allowable.

The Second 35 USC §102(b) Rejection

In the Office Action, claims 14-15 have been rejected under 35 USC 102(b) as being allegedly anticipated by Beausoleil et al. (Beausoleil, US 6,469, 375). This rejection is respectfully traversed.

In the Office Action it is asserted that with respect to claim 14, "Beausoleil shows a plurality of modules each comprising comprising: one or more active port 18 (see attached Fig. 1) for carrying one or more active signal (Fig. 1); and one or

more passive port (see attached Fig. 1) for passing through the one or more active signals.

Independent Claim 14

Amended claim 14, recites in part:

> a first serial chain route that includes at least one serial chain connection, the serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output; said serial chain input coupled to said serial chain output through said serial chain circuit;
>
> a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module; and
>
> said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module.

Beausoleil fails to teach or disclose the above claim limitations, and hence, claim 14 is allowable.

Dependent Claim 15

In the Office Action it is also asserted that with respect to claim 15, "Beausoleil shows wherein the one or more passive port forms a ladder like routing path (see attached Fig. 1)." Applicants respectfully traverse this rejection.

Claim 15 depends on allowable base claim 14. Thus, claim 15 is also allowable

for the same reasons stated for base claim 14 since an allowable base claim renders its dependent claim(s) also allowable.

The First 35 USC §103 Rejection

The Examiner rejects claim 16 by asserting this claim is allegedly unpatentable over Beausoleil et al. (Beausoleil, US 6,469,375). This rejection is respectfully traversed.

In the Office Action it is asserted that with respect to claim 16:

> Beausoleil teaches one or more of the plurality of module 14 (Fig. 1) and stacked one or more passive port (see attached Fig. 1), but fails teach module is rotated before being stacked and the one or more passive port forms a rotational routing path. However, Applicants have no support data, which convinces that the particular claimed configuration is significant or is anything more than one of numerous configurations a person of ordinary skill in the art would find obvious for the purpose of providing mating surfaces. In re Dailey 149 USPQ 47,50 (CCPA 1966). See also Glue Co. v. Upton 97 US 3,24 (USSC 1878)., see MPEP 2144.04.

Claim 16 depends from claim 1, which recites limitations not taught or suggested by Beausoleil. For example, claim 1 recites in part:

> a first serial chain route that includes at least one serial chain connection, the serial chain connection including: a serial chain circuit, a

serial chain input, and serial chain output; said serial chain input coupled to said serial chain output through said serial chain circuit;

a second serial chain route and a control circuit for enabling a routing path that connects the first serial chain route with the second serial chain route within an end module; and

said control circuit is disposed to enable the routing path in response to a control input signal received from another module from the plurality of modules when the end module is coupled to the another module.

Consequently, claim 1 is not rendered obvious by Beausoliel for the above reason, rendering this Section 103 Rejection inapplicable here since an allowable base claim renders its dependent claims also allowable.

In addition, Applicants agree with the Examiner that Beausoleil "fails to teach" module is rotated before being stacked and the one or more passive port forms a rotational routing path." Applicants, however, kindly disagree that the limitation in claim 16 that recites "one or more passive port forms a rotational routing path" is without significance or "is anything more than one of a numerous configurations a person of ordinary skill in the art would find obvious". The cases cited in the Office Action do not apply here because In re Daily or Glue Co. v. Upton, simply hold that structures that are a "mere matter of choice", or are not a new means "by which a desirable change in the form of a common article of commerce is obtained", respectively. Indeed, if the configuration recited by this claim limitation is so "numerous" so that it would be found obvious, a suitable prior art reference would be

readily available. The lack of such a reference precludes the Applicants from adequately responding to the Section 103 rejection on the merits.

Further, pursuant to MPEP 2144.04, the significance of the limitations recited in claim 16 is presented in by the Specification (Substitute Specification submitted on 13 February 2009) at p. 21, line 18 through p. 22, line 21; and Figures 20a and 20b.

Consequently, under any of the above additional reasons, the Section 103 rejection does not apply here, rendering claim 16 allowable.

Petition for Extension of Time

A Petition for an Extension of Time is submitted in a separate paper and filed on even date herewith.

Request for Allowance

It is believed that this Amendment places this Application into condition for allowance. Early favorable consideration of this Amendment is earnestly solicited.

Respectfully submitted,

Dated: 13 November 2009

/Stephen R. Uriarte/
Stephen R. Uriarte, Reg. No. 40,854

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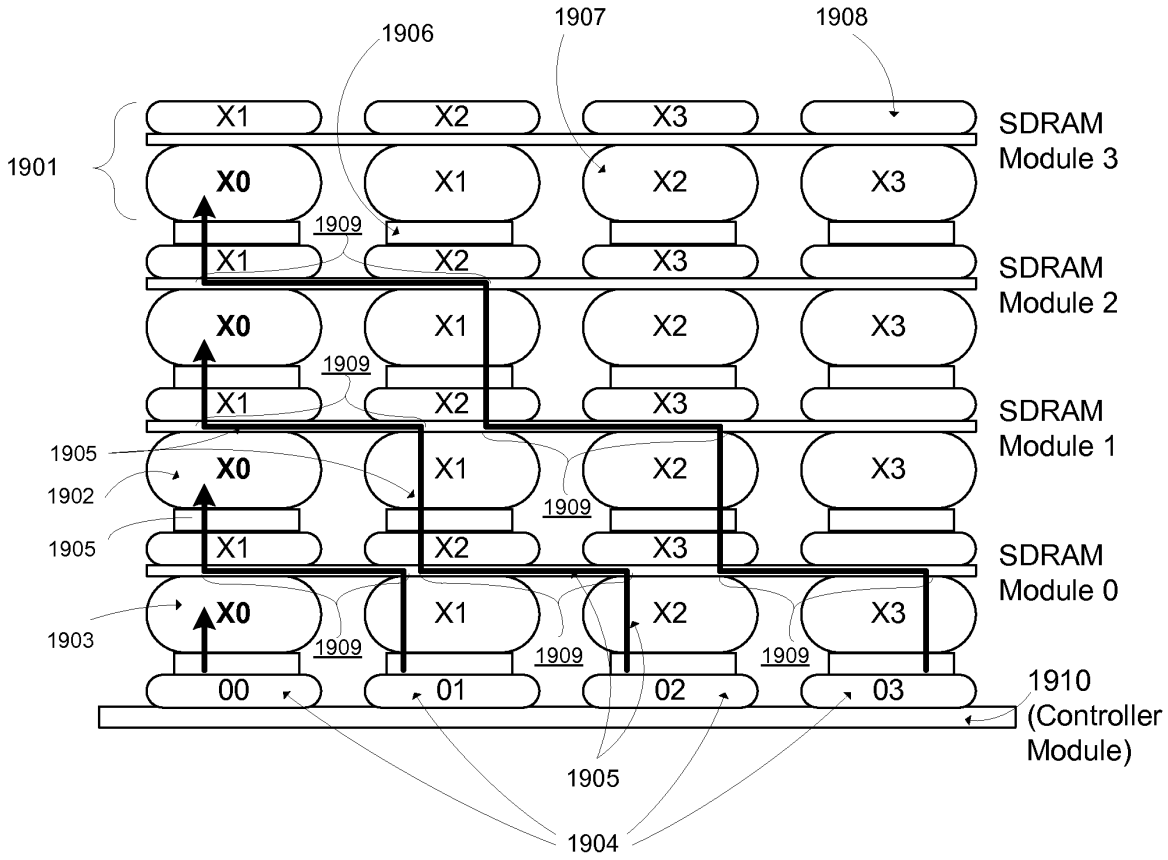

1906
1907
1908
1901
X1
X2
X3
X0
SDRAM Module 3
SDRAM Module 2
SDRAM Module 1
SDRAM Module 0
1909
1905
1902
1903
00
01
02
03
1910 (Controller Module)
1904

Figure 19

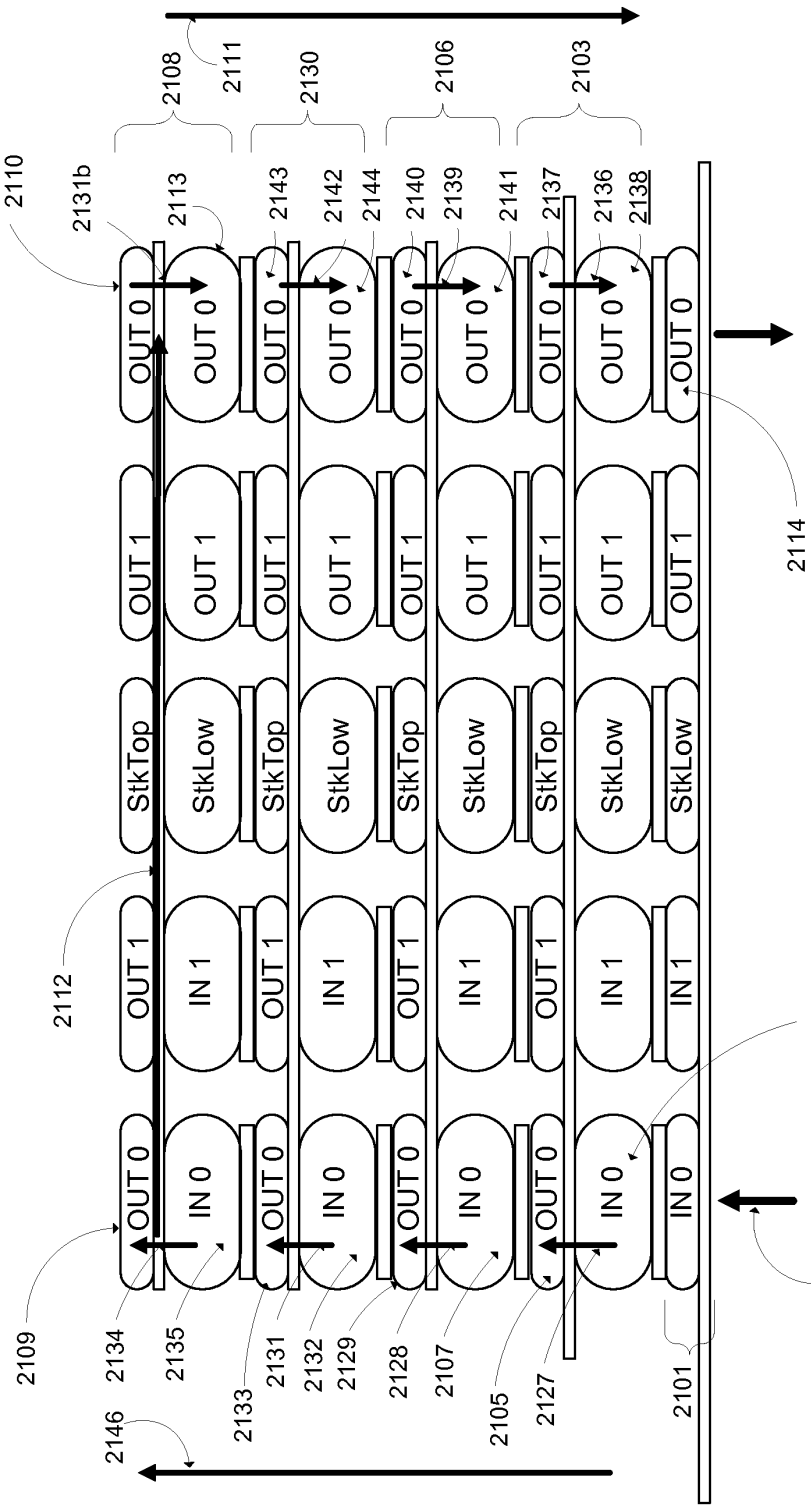

2108
2111
2130
2106
2103
2110
2131b
2113
2143
2142
2144
2140
2139
2141
2137
2136
2138
OUT 0
OUT 1
StkTop
StkLow
IN 1
IN 0
2114
2112
2104
2102
2109
2134
2135
2131
2132
2129
2128
2107
2105
2127
2133
2146
2101

Figure 21a

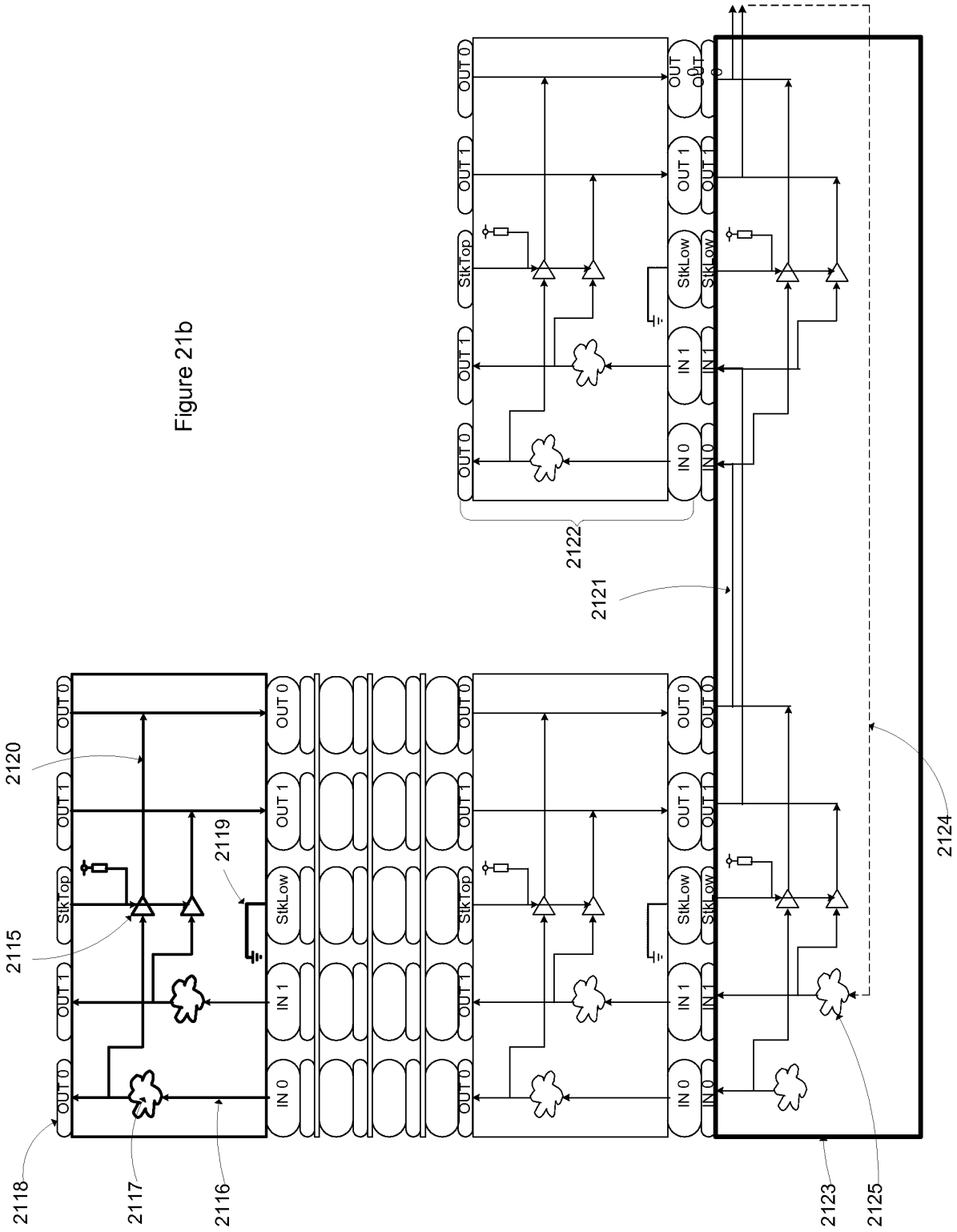

OUT 0
OUT 1
StkTop
IN 1
IN 0
StkLow
2120
2115
2119
2118
2117
2116
2122
2121
2124
2123
2125

Figure 21b

Attorney Docket#: 6005.011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: BRUCE et al.	Group Art Unit: 2892
Serial No.: 11/322,442	Examiner: ULLAH, Elias
Application Filing Date: 29 Dec 2005	
For: MULTIPLE CHIP MODULE AND PACKAGE STACKING FOR STORAGE DEVICES	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)

Dear Sir:

In conjunction with the Response to the Office Action, submitted on even date herewith, this is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and fee are as follows, indicated below:

Fees Paid:

___	One month (37 CFR 1.17(a)(1))	Fee (small entity: $65.00)	0.00
___	Two months (37 CFR 1.17(a)(2))	Fee (small entity: $245.00)	0.00
X	Three months (37 CFR 1.17(a)(3))	Fee (small entity: **$555.00**)	**Paid**

Entity Status:

X Applicant claims small entity status. (See 37 CFR 1.27)

Payment Method:

_X_ Payment by credit card through EFS-web is provided.

Authorization to Charge/Credit Fees and Constructive Petition for Extension of Time –All Replies

_X_ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number: **50-4068**.

Please treat this authorization to charge all required fees under 37 CFR 1.17 as a constructive petition for an extension of time in accordance with 37 CFR 1.136(a)(3).

The undersigned is the attorney of record. Registration #: 40,854

Sincerely,

Signature:	/Stephen R. Uriarte/	Date:	13 November 2009
Name:	Stephen R. Uriarte	Telephone:	408.244.2164x111

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Electronic Patent Application Fee Transmittal

Application Number:	11322442
Filing Date:	29-Dec-2005
Title of Invention:	Multiple chip module and package stacking method for storage devices
First Named Inventor/Applicant Name:	Rey Bruce
Filer:	Stephen Radcliff Uriarte
Attorney Docket Number:	6005.011

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 3 months with $0 paid	2253	1	555	555

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**555**

Electronic Acknowledgement Receipt	
EFS ID:	6455114
Application Number:	11322442
International Application Number:	
Confirmation Number:	5045
Title of Invention:	Multiple chip module and package stacking method for storage devices
First Named Inventor/Applicant Name:	Rey Bruce
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.011
Receipt Date:	13-NOV-2009
Filing Date:	29-DEC-2005
Time Stamp:	21:34:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
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Payment was successfully received in RAM	$555
RAM confirmation Number	8435
Deposit Account	504068
Authorized User	URIARTE,STEPHEN R.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	6005_011_2ndRsp2OA_20091113F.pdf	206580 9bbbb287c58481340be1d8245c4b48dd89f76293	no	33
Warnings:					
Information:					
2	Drawings-only black and white line drawings	6005_011_F19_F21a_21b_rplcmnt_20091113.pdf	87810 e38eba3a523bd3a93e5160f802ca452359b509b9	no	3
Warnings:					
Information:					
3	Extension of Time	6005_011_2ndRsp2OA_NON_ExtTime_20091113.pdf	96809 31f79d766c8244472fb215a5adbcb97cd59dfd6d	no	2
Warnings:					
Information:					
4	Fee Worksheet (PTO-875)	fee-info.pdf	29792 39a8b55905c6929a60626172a99704766581c7a7	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	420991		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/322,442	12/29/2005	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☒		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	11/13/2009	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 28	Minus	** 26	= 2	X $26 =	52	OR	X $ =	
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $110 =	0	OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE	52	OR	TOTAL ADD'L FEE	

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/ADRIENE D. SELLMAN/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Document code: WFEE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/322,442	12/29/2005	Rey Bruce	6005.011	5045

64180 7590 05/13/2009

URIARTE LAW
257 RODONOVAN DRIVE
SANTA CLARA, CA 95051

EXAMINER	
ULLAH, ELIAS	
ART UNIT	PAPER NUMBER
2892	

MAIL DATE	DELIVERY MODE
05/13/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/322,442	BRUCE ET AL.	
	Examiner	Art Unit	
	ELIAS ULLAH	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to an amendment filed on 2/13/2009

Election/Restrictions

1. Applicant's election without traverse of claims 14-26 in the reply filed on 6/27/2008 is acknowledged.

2. A request for reconsideration of previously withdrawn claims 17-19 and 24-26 have been carefully reviewed and considered. Accordingly, claims 17-19 and 24-26 have been entered for further consideration. Now, claim 17 is dependent on claim 14 instead of cancelled claim 1.

3. Claim 17 is dependent on claim 14 instead of cancelled claim 1 was discussed by a telephone interview on May 8th, 2009 with Mr. Stephen R Uriarte.

Claim Rejections - 35 USC § 112

3. Claims 14-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In base claim 1, applicants claimed "one or more passive port for passing though the one or more active signals". However, in light of applicants' discloser, as it would be interpreted by one of ordinary skill in the art, above claim limitations do not set out and define the invention with a reasonable degree of precision and particularity. For purpose of examination, Examiner assumes the "passive port" is a connection on active port for carrying signal.

4. Claims 22-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention. In claims 22-23, applicants claimed "one or more passive ball and one or more passive pad". However, in light of applicants' discloser, as it would be interpreted by one of ordinary skill in the art, above claim limitations do not set out and define the invention with a reasonable degree of precision and particularity. For purpose of examination, Examiner assumes the "passive port inherently comprises passive ball and passive pad".

4. Claims 17-19 and 24-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In claims 17, applicants claimed "one or more pair of daisy chain input port and daisy chain output port ". However, in light of applicants' discloser, as it would be interpreted by one of ordinary skill in the art, above claim limitations do not set out and define the invention with a reasonable degree of precision and particularity. For purpose of examination, Examiner assumes the "limitation associated with daisy chain will read as ladder like routing path connection".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 14-15 and 17-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Kyougoku et al. (Kyougoku, US 5,995,379) of record.

With regard to claim 14, Kyougoku shows a stacked module (Fig. 5) comprising a plurality of modules (100-1002) each comprising: one or more active port (B1) for carrying one or more active signal (Fig. 5); and one more passive port (L1, L4) for passing through the one or more active signals (Fig. 5).

With regard to claim 15, Kyougoku shows the one or more passive port forms a ladder like routing path (L1, L4).

With regard to claims 17-19, Kyougoku shows one or more pair of daisy chain input port and daisy chain output port for forming a first daisy chain connection wherein each pair of the daisy chain input port and the daisy chain output port are connected through a daisy chain circuit; one or more control port for enabling a routing path extending the first daisy chain connection within an end module and wherein the routing path within the end module is connected to a second daisy chain connection (above limitations interpret as ladder lire routing path connection thus see Fig. 5 for ladder like connection).

With regard to claims 20-21, Kyougoku shows one or more of the plurality of modules is a main board (Col. 6, lines 55-57) and one more vertically stacked modules 1000-1002 in (Fig. 5) is connected to the main board (Col. 6, lines 55-57).

With regard to claims 22-23, Kyougoku shows each of the plurality of modules (1000-1002) comprises a first side (B1-B3 area) and a second side (B1'-B3' area) (Fig. 5) wherein the one or more active port (B1) is connected to one or more active ball 5 on the first side (B1-B3 area) of one or more corresponding module 1000; wherein the one or more passive port L1 is connected to one or more passive ball (L1 has inherently

comprises a passive ball due to passive ball is indefinite) on the first side and one or more passive pad (L1 has inherently comprises a passive pad due to passive pad is indefinite) on the second side of one or more corresponding module 1000; wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port L1 are located between a pre-determined distance to each other in a repeating pattern, the pre-determined distance equaling a multiple of a periodic distance of the repeating pattern (Fig. 5); wherein one or more active port B1 of a base module not shown (see col. 6, liens 55-57) is routed to a same location on one or more modules 1000-1002 through the ladder like routing path L1; and wherein the ladder like routing path comprises one or more passive ball and one or more passive pad (Fig. 5).

With regard to claims 24-26, Kyougoku shows wherein each of the plurality of modules comprises a firs side (B1 area) and second side (B1' area). wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module (L1 and L 3 ladder like routing path will inherently comprises above limitation as discussed above section 3-4); wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other; wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection; and wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more

passive pad L1 and L 3 ladder like routing path will inherently comprises above limitation as discussed above section 3-4).

With regard to claims 27- 28, Kyougoku shows the stacked module (100-1002) further includes a first outside surface (B1 area) and a second outside surface (B1' area) the first and second outside surface disposed to face opposite each other (see module 1000); at least one of the plurality of modules includes a first module 1000 having a first target location (see dotted line in the module 1000) terminating between the fist and second outside surfaces (Fig. 5); the plurality of modules (1000-1002) further includes a second module 1001 and a third module 1002 the second module including a second module surface (C1 area) that includes the fist outside surface (C1') and the third module 1002 including a third module surface D1 that includes the second outside surface D1'.

With regard to claim 29, Kyougoku shows a second ladder like routing path; and wherein: the plurality of modules includes a first module1000 and a second module 1001, the first and second modules respectively including a first target location (dotted line in the module 1000) and a second target location (dotted line in the module 1001), the second target location located within the stacked module 1001; and the ladder like routing path L1 for routing one of the active port B2 to the first target location (1000), and the second ladder like routing path L4 for routing another one of the active port B3 to the second target location 1001.

With regard to claim 30 Kyougoku shows, further including a second ladder like routing path L4; and wherein the stacked module includes a first outside surface (B1

area) and a second outside surface (B1' area), the first and second outside surfaces disposed to face opposite each other (Fig. 5); the ladder like routing path terminates at the first target location (dotted area of module 1000); and the second ladder like routing path L4 terminates at the second target location (dotted area of of module 1001) , the second target terminating within the stacked module 1001 and located between the first and second outside surfaces (See Fig. 5).

With regard to claim 31, Kyougoku shows wherein the second target location (dotted area of module 1001) is located between the first and second outside surfaces (C1 and C1')

6. Claims 14-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Beausoleil et al. (Beausoleil, US 6,469,375).

With regard to claim 14, Beausoleil shows a stacked module comprising a plurality of modules each comprising: one or more active port 18 (see attached Fig. 1) for carrying one or more active signal (Fig. 1); and one or more passive port (see attached Fig. 1) for passing through the one or more active signals.

With regard to claim 15, Beausoleil shows wherein the one or more passive port forms a ladder like routing path (see attached Fig. 1).

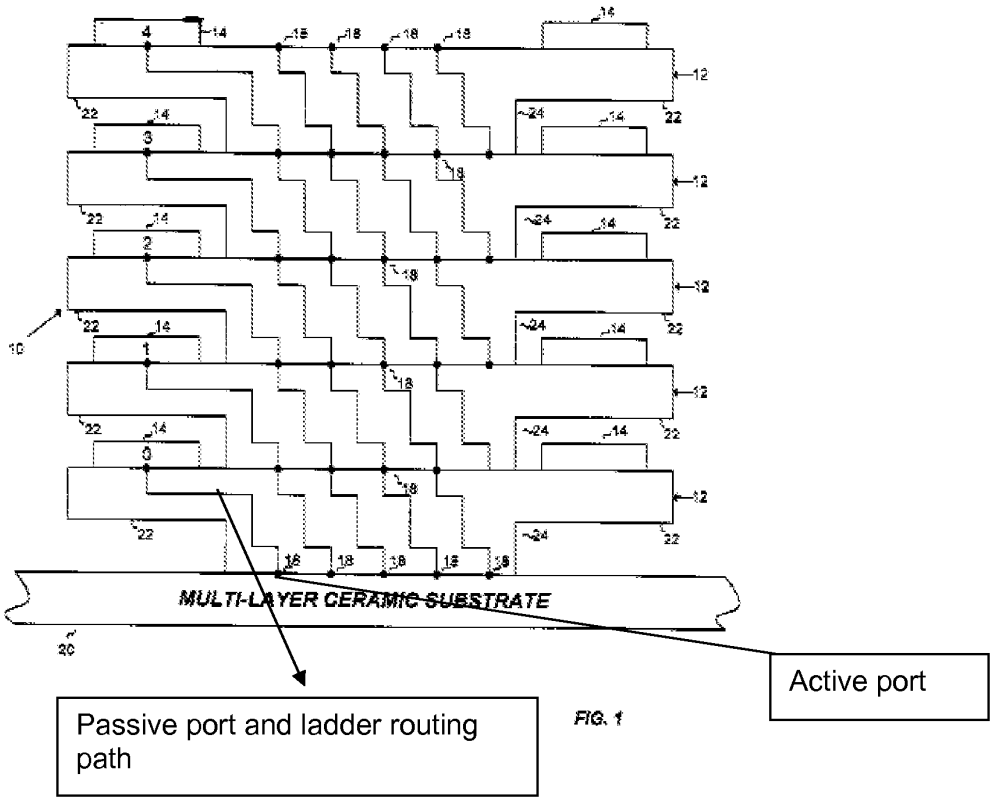


FIG. 1

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beausoleil et al. (Beausoleil, US 6,469,375).

With regard to claim 16, Beausoleil teaches one or more of the plurality of module 14 (Fig. 1) and stacked one or more passive port (see attached Fig. 1), but fails teach module is rotated before being stacked and the one or more passive port forms a rotational routing path.

However, Applicants have no support data, which convinces that the particular claimed configuration is significant or is anything more than one of numerous configurations a person of ordinary skill in the art would find obvious for the purpose of providing mating surfaces. In re Dailey 149 USPQ 47, 50 (CCPA 1966). See also Glue Co. v. Upton 97 US 3,24 (USSC 1878)., see MPEP 2144.04.

Response to Arguments

9. Applicant's arguments filed 2/13/2009 have been fully considered but they are not persuasive. With regard to claim 14, applicants assert that a controller module active pad(s) to be routed to a desired specific module within the stack module. However, Kyougoku clearly shows a controller module (col. 6, lines 55-57) active pad(s) to be routed L4 to a desired specific module i.e. 1001 within the stacked module

(Fig. 5). Furthermore, the claimed invention " within the stacked module" may be disclosed in the SPEC, but not recited in the claim 14 thus it should not be read into the claim 14. See MPEP 2145 section VI.

In light of above remarks, applicants request allowance of claim 14 is not convincing and claim 14 is stand rejected as noted. Thus claims 15-16 and 20-21 are also stand rejected as noted above office action.

With respect claims 22-23, Applicants assert that Kyougoku fails to teach or disclose each and every element recited in claims 22-23. However, applicants respectfully requested to review new ground of rejection i.e. 112 second paragraph and further clarification of those elements in the above noted office action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ELIAS ULLAH whose telephone number is (571)272-1415. The examiner can normally be reached on weekdays, between 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Elias Ullah/
Examiner, Art Unit 2892

/Thao X Le/
Supervisory Patent Examiner, Art Unit 2892

Notice of References Cited	Application/Control No. 11/322,442	Applicant(s)/Patent Under Reexamination BRUCE ET AL.	
	Examiner ELIAS ULLAH	Art Unit 2892	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,995,379	11-1999	Kyougoku et al.	361/803
*	B	US-6,469,375	10-2002	Beausoleil et al.	257/686
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11322442	BRUCE ET AL.
	Examiner	Art Unit
	ELIAS ULLAH	2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/23/2008	08/07/2008	05/09/2009						
	1	÷	-	-						
	2	÷	-	-						
	3	÷	-	-						
	4	÷	-	-						
	5	÷	-	-						
	6	÷	-	-						
	7	÷	-	-						
	8	÷	-	-						
	9	÷	-	-						
	10	÷	-	-						
	11	÷	-	-						
	12	÷	-	-						
	13	÷	-	-						
	14	÷	✓	✓						
	15	÷	✓	✓						
	16	÷	✓	✓						
	17	÷	N	✓						
	18	÷	N	✓						
	19	÷	N	✓						
	20	÷	✓	✓						
	21	÷	✓	✓						
	22	÷	✓	✓						
	23	÷	✓	✓						
	24	÷	N	✓						
	25	÷	N	✓						
	26	÷	N	✓						
	27			✓						
	28			✓						
	29			✓						
	30			✓						
	31			✓						

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11322442	BRUCE ET AL.
	Examiner	Art Unit
	ELIAS ULLAH	2892

SEARCHED			
Class	Subclass	Date	Examiner
257	686	5/9/2009	EU

SEARCH NOTES		
Search Notes	Date	Examiner
EAST database serarch	5/9/2009	EU

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	(("6172874" | "6900528").PN.").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/07/31 10:02
S2	4	("6172874" | "6900528").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/31 10:03
S3	2	"20070158808".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/31 10:07
S4	41	("5018005" | "5041903" | "5103375" | "5561593" | "5790380" | "5861666").PN. OR ("6172874").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/31 10:53
S5	2909	257/686.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/31 11:01
S6	183	S5 and (stack$2 adj module)	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/31 11:01
S7	418352	(signal same active or passive)	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/31 11:02
S8	272545	(signal same (active or passive))	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/31 11:02
S9	19	S6 and (signal same (active or passive))	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/31 11:02
S10	1	"20060206745".pn.	US-PGPUB; USPAT; USOCR	OR	ON	2008/08/04 08:57
S11	1	"20070158808".pn.	US-PGPUB; USPAT; USOCR	OR	ON	2008/08/04 09:00
S12	1	"5995379".pn.	US-PGPUB; USPAT; USOCR	OR	ON	2008/08/04 09:45
S13	1	"5995379".pn.	US-PGPUB; USPAT; USOCR	OR	ON	2008/08/06 12:57
S14	1	11/322442	US-PGPUB; USPAT; USOCR	OR	ON	2008/08/07 08:06
S15	1	"5995379".pn.	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/08 15:15

S16	47	("5130894" | "5198888" | "5343075" | "5397916" | "5434452" | "5434745" | "5585675" | "5854507"). PN. OR ("5995379"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/08 15:15
S17	89	("20010008482" | "20010028114" | "20010036063" | "20020075662" | "20020176233" | "20030022464" | "3746934" | "4698267" | "4773868" | "5130894" | "5172303" | "5222014" | "5334875" | "5394303" | "5434745" | "5455385" | "5502667" | "5544017" | "5574630" | "5586010" | "5666272" | "5699234" | "5701233" | "5702984" | "5712768" | "5715144" | "5721671" | "5748452" | "5781415" | "5783870" | "5798567" | "5854507" | "5857858" | "5883426" | "5898575" | "5907903" | "5953210" | "5963430" | "5973392" | "5977640" | "5995379" | "6014316" | "6025648" | "6049467" | "6093029" | "6125039" | "6133626" | "6137164" | "6163462" | "6180881" | "6188127" | "6195268" | "6222265" | "6239496" | "6265772" | "6274929" | "6297960" | "6303997" | "6331939" | "6339254" | "6381141" | "6388333" | "6414391" | "6437990" | "6448506" | "6451624" | "6462421" | "6477058" | "6504241" | "6507107" | "6521984" | "6522022" | "6525943" | "6525945" | "6529385" | "6531337" | "6538332" | "6542393" | "6545868" | "6549421" | "6583503" | "6597062" | "6617695" | "6703697" | "6714418" | "6717812" | "6740981" | "6781241" | "6809421").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/08 15:18

S18	13	("5057041" | "5213522" | "5624277" | "5761036" | "6142831").PN. OR ("6529385").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/08 15:20
S19	3186	257/686.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/08 17:54
S20	1	"11322442"	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/08 17:55
S21	22	((control$3 adj module) same (ram with module)) same (ladder or rotation or (daisy adj chain) with (path or connection))	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/08 21:11
S22	14	S21 and @ad<"20021225"	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/08 21:12
S23	2	"6469,375".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/05/08 21:37

5/9/2009 9:00:15 PM
C:\Documents and Settings\eullah\My Documents\EAST\Workspaces\11322442.wsp

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: BRUCE et al.	Group Art Unit: 2892
Serial No.: 11/322,442	Examiner: ULLAH, Elias
Application Filing Date: 29 Dec 2005	
For: MULTIPLE CHIP MODULE AND PACKAGE AND PACKAGE STACKING METHOD FOR STORAGE DEVICE	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY TO FIRST OFFICE ACTION ON THE MERITS

Dear Examiner:

In response to the Office Action, mailed 13 August 2008, please kindly amend this Application as follows and consider the remarks set forth below.

Amendments to the Specification begin on page 2;

A listing of claims begins on page 3;

Amendment(s) to the Drawings begins on page 13; and

Remarks begin on page 16 of this paper.

Replacement sheets of drawings and a substitute specification incorporating the changes proposed in the Amendments to the Drawings and to the Specification, respectively, are attached to this paper.

Amendment(s) to the Specification

The specification has been amended to correct minor grammatical errors. These amendments are provided by submitting a substitute specification (excludes Claims but includes Abstract) in accordance with MPEP 608.01. No new matter has been added. A marked up copy of the substitute specification is attached, showing all changes relative to the immediate prior version as required under MPEP 608.01(q). In addition, a copy of the substitute specification without markings is also attached in accordance with 37 CFR 1.125(c). No new matter has been added to the specification.

Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (CANCELLED) A method for stacking a plurality of modules comprising the steps of:

providing one or more active port on the plurality of modules for carrying one or more active signal;

providing one or more passive port on the plurality of modules for passing through the one or more active signals; and

stacking the plurality of modules.

2. (CANCELLED) The method of claim 1 wherein the one or more passive port forms a ladder like routing path.

3. (CANCELLED) The method of claim 1 wherein one or more of the plurality of module is rotated before being stacked and the one or more passive port forms a rotational routing path.

4. (CANCELLED) The method of claim 1 further comprising the step of providing one or more pair of daisy chain input port and daisy chain output port for forming a first daisy chain connection wherein each pair of the daisy chain input port and the daisy chain output port are connected through a daisy chain circuit.

5. (CANCELLED) The method of claim 4 further comprising the step of providing one or more control port for enabling a routing path extending the first daisy chain connection within an end module.

6. (CANCELLED) The method of claim 5 wherein the routing path within the end module is connected to a second daisy chain connection.

7. (CANCELLED) The method of claim 1 wherein one or more of the plurality of modules is a main board.

8. (CANCELLED) The method of claim 7 wherein one or more vertically stacked module is connected to the main board.

9. (CANCELLED) The method of claim 2:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located between a pre-determined distance to each other in a repeating pattern, the pre-determined distance equaling a multiple of a
periodic distance of the repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the ladder like routing path; and

wherein the ladder like routing path comprises one or more passive ball and one or more passive pad.

10. (CANCELLED) The method of claim 3:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located opposite each other in a repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the rotational routing path; and

wherein the rotational routing path comprises one or more passive ball and one or more passive pad.

11. (CANCELLED) The method of claim 4:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive

pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection; and

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad.

12. (CANCELLED) The method of claim 5:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad; and

wherein the routing path comprises one or more tri-state driver controlled by the one or more control port.

13. (CANCELLED) The method of claim 6:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad;

wherein the routing path comprises one or more tri-state driver controlled by the one or more control port; and

wherein one or more daisy chain connection are extended through one or more vertically stacked module connected to a main board.

14. (ORIGINAL) A stacked module comprising a plurality of modules each comprising:

one or more active port for carrying one or more active signal; and

one or more passive port for passing through the one or more active signals.

15. (ORIGINAL) The stacked module of claim 14 wherein the one or more passive port forms a ladder like routing path.

16. (ORIGINAL) The stacked module of claim 14 wherein one or more of the plurality of module is rotated before being stacked and the one or more passive port forms a rotational routing path.

17. (WITHDRAWN) The stacked module of claim 1 further comprising one or more pair of daisy chain input port and daisy chain output port for forming a first daisy chain connection wherein each pair of the daisy chain input port and the daisy chain output port are connected through a daisy chain circuit.

18. (WITHDRAWN) The stacked module of claim 17 further comprising one or more control port for enabling a routing path extending the first daisy chain connection within an end module.

19. (WITHDRAWN) The stacked module of claim 18 wherein the routing path within the end module is connected to a second daisy chain connection.

20. (ORIGINAL) The stacked module of claim 14 wherein one or more of the plurality of modules is a main board.

21. (ORIGINAL) The method of claim 20 wherein one or more vertically stacked module is connected to the main board.

22. (ORIGINAL) The stacked module of claim 15:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located between a pre-determined distance to each other in a repeating pattern, the pre-determined distance equaling a multiple of a periodic distance of the repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the ladder like routing path; and

wherein the ladder like routing path comprises one or more passive ball and one or more passive pad.

23. (ORIGINAL) The stacked module of claim 16:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located opposite each other in a repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the rotational routing path; and

wherein the rotational routing path comprises one or more passive ball and one or more passive pad.

24. (WITHDRAWN) The stacked module of claim 17:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection; and

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad.

25. (WITHDRAWN) The stacked module of claim 18:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad; and

wherein the routing path comprises one or more tri-state driver controlled by the one or more control port.

26. (WITHDRAWN) The stacked module of claim 19:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad;

wherein the routing path comprises one or more tri-state driver controlled by the one or more control port; and

wherein one or more daisy chain connection are extended through one or more vertically stacked module connected to a main board.

27. (NEW) The stacked module of claim 15, wherein:

the stacked module further includes a first outside surface and a second outside surface, the first and second outside surfaces disposed to face opposite each other;

at least one of the plurality of modules includes a first module having a first target location terminating between the first and second outside surfaces.

28 (NEW) The stacked module of claim 27, wherein the plurality of modules further includes a second module and a third module, the second module including a second module surface that

includes the first outside surface and the third module including a third module surface that includes the second outside surface.

29. (NEW) The stacked module of claim 15, further including a second ladder like routing path; and wherein:

the plurality of modules includes a first module and a second module, the first and second modules respectively including a first target location and a second target location, the second target location located within the stacked module; and

the ladder like routing path for routing one of the active port to the first target location, and the second ladder like routing path for routing another one of the active port to the second target location.

30. (NEW) The stacked module of claim 29, further including a second ladder like routing path; and wherein:

the stacked module includes a first outside surface and a second outside surface, the first and second outside surfaces disposed to face opposite each other;

the ladder like routing path terminates at the first target location; and

the second ladder like routing path terminates at the second target location, the second target terminating within the stacked module and located between the first and second outside surfaces;

31. (NEW) The stacked module of claim 29, wherein the second target location is located between the first and second outside surfaces.

Amendment(s) to the Drawings

The following proposed amendments to the Drawings are provided in the form of replacement drawing sheets, which are each labeled "Replacement Sheet" in their respective page headers pursuant to 37 CFR 1.84(c). No new matter has been added.

Please amend FIGS. 1 through 21b to include sight lines and larger figure label font sizes to their respective drawing sheets.

In addition, please further amend the specific figures as described below:

In FIG. 1a, please change the orientation of the figure from portrait to landscape. In addition, please reduce the length of Bus 104 and height of Main Controller-Processor 101 so that the entire figure fits within the sight lines of the drawing sheet;

In FIG. 1b, please change the orientation of the figure from portrait to landscape;

In FIGS. 2a and 2b please change the position of these figures so that they are within the sight lines of the drawing sheet;

In FIGS. 3a and 3b, please change the position of these figures so that they are within the sight lines of the drawing sheet;

In FIGS. 4a and 4b, please change the position of these figures so that they are with the sight lines of the drawing sheet;

In FIGS. 5a and 5b, please change the position of these figures so that they are with the sight lines of the drawing sheet;

In FIGS. 6a and 6b, please change the position of these figures so that they are with the sight lines of the drawing sheet;

In FIG. 7b, please change the position of the figure so that it is with the sight lines of the drawing sheet;

In FIG. 11, please change the position of element numbers so that they fit within the sight lines of the drawing sheet;

In FIG. 12a, please reduce the size of the figure, while maintaining its original aspect ration, so that the figure fits within the sight lines of the drawing sheet;

In FIG. 12b, please change the position of the figure so that it is with the sight lines of the drawing sheet;

In FIG. 13, please change the position of the figure so that it is with the sight lines of the drawing sheet;

In FIG. 14, please change the position of the figure so that it is with the sight lines of the drawing sheet;

In FIG. 15a, please change the position of the figure so that it is with the sight lines of the drawing sheet;

In FIG. 15b, please amend the figure so that if fits within the sight lines of the drawing sheet by splitting the figure into two portions and adding projection lines to illustrate their connection details;

In FIG. 16, please change the position of the figure so that it is with the sight lines of the

drawing sheet;

In FIG. 17a, please change the position of the figure so that it is with the sight lines of the drawing sheet;

In FIG. 17b, please amend the figure so that if fits within the sight lines of the drawing sheet by splitting the figure into two portions and adding projection lines to illustrate their connection details;

In FIG. 18, please change the position of the figure so that it is with the sight lines of the drawing sheet;

In FIG. 19, please amend the figure so that it is with the sight lines of the drawing sheet by moving the element numbers towards the center of the figure and changing the element text that begins with "SDRAM Module" so that are converted for one to two lines of text;

In FIG. 20b, please change the orientation of the figure from portrait to landscape;

In FIG. 21a, please change the orientation of the figure from portrait to landscape;

In FIG. 21b, please amend the figure so that if fits within the sight lines of the drawing sheet by reducing the size of the figure, while maintaining its original aspect ration, and by changing the orientation of the figure from portrait to landscape.

Remarks

The specification and drawings have been amended to correct minor errors noted in the Office Action and otherwise. These corrections are of a clerical nature and do not add "new matter".

Claims 1 and 13 have been previously cancelled without prejudice in an earlier filed Response to Restriction Requirement.

Claims 17-19 and 24-26 have been withdrawn by the Examiner.

The text of original claims 14-16 and 20-23 remain unchanged.

Claims 27 through 31 are new, do not recite new matter, or present new grounds for a new search.

Examiner's Withdrawal of Claims 17-19 and 24-26 & Examiner Interview Conducted on 9 Jan 2008

Claims 17-19 and 24-26 have been withdrawn in the Office Action. Applicants respectfully traverse the withdrawal of these claims and kindly request a new Restriction Requirement for at least two reasons. First, the Examiner in the Restriction Requirement, having mail date of 3 June 2008, considered these claims to fall within Invention II which were specifically elected by the Applicants in the Applicants Election provided on 27 June 2008. Thus, the withdrawal of claims 17-19 and 24-26 in the Office Action is improper because the Applicants did not withdraw these claims but instead specifically elected these claims in accordance with the examination restrictions defined in the Restriction Requirement. Second, the withdrawal of claims 17-19 and 24-26 in the Office Action directly contradicts the Restriction Requirement statement

that "Claims 14-26" are "drawn to a stacked module for carrying one or more active signal, classified in class 257, subclass 686." (See page 2, Restriction Requirement dated 3 June 2008). Consequently, the Applicants with respect assert that the withdrawal of claims 17-19 and 24-26 is improper.

The undersigned extends much thanks to the Examiner for agreeing to an Examiner's interview on 9 January 2009, which was conducted by telephone. The undersigned and the Examiner discussed the withdrawal of claims 17-19 and 24-26 and issues related to these claims and the Restriction Requirement. The undersigned communicated that it is believed that this withdrawal is unwarranted and unsupported (by the Patent Rules and MPEP). The undersigned also communicated that the Restriction Requirement and Election were incorrect as originally presented, and that the proper action should not include withdrawal of these claims but should instead permit the Applicants to amend the claims so that they conform to the Examiner's original restriction requirement. The undersigned believes that such an approach is warranted and does not represent a shift in the elected invention (see MPEP 821.03) because claims 17-19 and 24-26 are directed to a stacked module, which is an apparatus, whereas the unelected invention is drawn to a method. The dependency to claim 1 is merely an inadvertent typographical error (missing numeral "4" after the numeral "1") since the preamble in each of claims 17-19 and 24-26 clearly states that it depends on a "stacked module" rather than the method recited in claim 1.

In addition, Applicants Election did not traverse the Restriction because the Restriction Requirement stated that claims 14-26 are readable on the same invention ("stacked module"). Consequently, Applicants believe that MPEP 821.02 does not apply here since, had the Restriction Requirement originally stated that claims 17-19 and 24-26 did not read on a stacked module, Applicants would have made an election *with* traverse or at least made an election with an

amendment to claims 17-19 and 24-26 that renders the text of the claims consistent with their preamble and that corrects their dependency from claim 1 to claim 14 had the Restriction Requirement asserted that claims 17-19 and 24-26 did not read on the same invention ("stacked module") as the remaining pending claims 14-16 and 20-23.

Consequently, for the reasons stated above, Applicants kindly request that the withdrawal of claims 17-19 and 24-26 be withdrawn, and a new Restriction Requirement issued.

The Section 102(a) Rejection

Claims 14-15 and 18-23 are rejected as allegedly being anticipated by Kyougoku (USP 5,995,379). This rejection is respectfully traversed.

Independent Claim 14

In the Office Action it is asserted that with respect to claim 14, "Kyougoku shows a stacked module (Fig. 5) comprising a modules (100-1002) each comprising: one or more active port (B1-B3) for carrying one or more active signal (col. 6, lines 45-50); and one or more passive port (L1-L6) for passing through the one or more active signals (col. 6, lines 45-50)." Applicants respectfully disagree. The alleged active signals, such as chip select signals B1 and B2 (Kyougoku at col. 6, lines 45-50), begin from an outside surface of the ***stacked*** module but terminate on the other side (or outside opposite surface) of the stack module. See also, Kyougoku, D1,' D2' and D3' in FIG. 5 (FIG. 5 is a partial section view). See also, col. 3, line 65 to col. 4, line 15. The claimed invention, however, enables a controller module active pad(s) to be routed to a desired specific module ***within*** the stacked module. Consequently, Kyougoku fails to teach or suggest each element of the invention recited in claim 14, rendering claim 14 allowable.

Dependent Claims 15 and 16

In the Office Action it is also asserted that with respect to claim 15, "Kyougoku shows the one or more passive port forms a ladder like routing path (L1-L6)." Applicants respectfully traverse this rejection.

Claim 15 depends on allowable base claim 14, and thus claim 15 is also allowable for the same reasons.

In the Office Action it is also asserted that with respect to claim 16, "Kyougoku shows the plurality of module 1000-1002 is rotated before being stacked and the one or more passive port L1-L6 forms a rotational routing path (Fig. 5)." Applicants respectfully traverse this rejection.

Claim 16 depends on allowable base claim 14, and thus claim 16 is also allowable for the same reasons.

In addition, with respect to claims 15 and 16, the Office Action uses L1-L6 in Kyougoku to assert that Kyougoku discloses a "ladder like routing path" but also uses the same structure (L1-L6) to assert that Kyougoku also discloses a "rotational routing path". This interpretation of L1-L6 is inherently contradictory because a ladder like routing path cannot be a rotational routing path and vice versa although a ladder like routing path may be used with a rotational routing path and vice versa. See, Applicants' Drawings in FIG. 19, showing an embodiment of a "ladder like routing path"; and FIGS. 20a-20b, showing an embodiment of a "rotational routing path".

Dependent Claim 18

The Office Action rejects claim 18 by alleging that "Kyougoku shows one or more control port (1000) for enabling a routing path (L4) extending the first daisy chain connection 5 with an

end module 1002 (Fig. 5)." This rejection is respectfully traversed.

Element number 1000 in Kyougoku, Fig. 5, represents a semiconductor ***substrate*** rather than a "control port". Kyougoku at col. 7, lines 27-29. Consequently, Kyougoku fails to disclose or suggest control port, rendering this rejection improper and claim 18 allowable.

Dependent Claims 20-21

The Office Action rejects claims 20 and 21 by asserting that that "Kyougoku shows one or more of the plurality of modules is a main board (Col. 6, lines 55-57) and one more vertically stacked modules 1000-1002 in (Fig. 5) is connected to the main board (Col. 6, lines 55-57). This rejection is respectfully traversed.

Claims 20 and 21 depend on allowable base claim 14, and thus claims 20 and 21 are also allowable for the same reasons stated above for claim 14.

Dependent Claim 22

The Office Action rejects claim 22 by alleging that "Kyougoku shows each of the plurality of modules (1000-1002) comprises a first side (B1-B3 area) and a second side (B1'-B3' area) (Fig. 5) wherein the wherein the one or more active port (B3) is connected to one or more active ball 5 on the first side of one or more corresponding module 1000; wherein the one or more passive port L1 is connected to one or more passive ball (not labeled, ball connected to B2) on the first side and one or more passive pad B1' on the second side of one or more corresponding module 1000; wherein each of the one or more passive ball (no labeled, ball connected to B2) and each of the one or more passive pad B1' connected to a same passive port are located between a pre-determined distance to each other in a repeating pattern, the pre-determined distance equaling a multiple of a periodic distance of the repeating pattern (Fig. 5); wherein one or more active port of

a base module is routed to a same location on one or more modules 1001-1002 through the ladder like routing path L1-L6; and wherein the ladder like routing path comprises one or more passive ball and one or more passive pad (Fig. 5)." This rejection is respectfully traversed.

Claim 22 ultimately depends on allowable claim 14, and thus is allowable for the same reasons stated for claims 14 and any intervening dependent claims.

In addition, at least one of the elements recited in claim 22 is not taught or disclosed in Kyougoku. In the Office Action it is asserted that Kyougoku teaches or discloses that "the one ore more passive port L1 is connected to one or more passive ball (not labeled, ***ball connected to B2***)." (Emphasis added). The "ball connected to B2", however, is not a passive ball because B2 is disposed to receive a chip select signal. See, Kyougoku at col. 7, lines 29-30 ("chip select electrode pads B1 to B3…are formed on the surfaces of the substrates…") and Fig. 5.

Consequently, for the reasons stated above, Kyougoku fails to teach or disclose each and every element recited in claim 22, rendering claim 22 allowable.

Dependent Claim 23

The Office Action rejects claim 23 by alleging that "Kyougoku shows each of the plurality of modules (1000-1002) comprises a first side (B1-B3 area) and a second side (B1'-B3' area) wherein the one or more active port (B3) is connected to one or more active ball 5 on the first side of one or more corresponding module 1000; wherein the one or more passive port L1-L6 is connected to one or more passive ball (not labeled, ball connected to B2) on the first side and one or more passive pad B1' on the second side of one or more corresponding module 1000; wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port L1 are located opposite each other in a repeating pattern (L1-L6); wherein one or

more active port of a base module 1000 is routed to a same location on one or more modules 1001-1002 through the rotational routing path (L1-L6); and wherein the ladder like routing path comprises one or more passive ball and one or more passive pad (Fig. 5)." This rejection is respectfully traversed.

Claim 23 ultimately depends on allowable claims 14, and thus is allowable for the same reasons stated for claims 14 and any intervening dependent claims, including claim 16.

In addition, at least one of the elements recited in claim 23 is not taught or disclosed in Kyougoku. In the Office Action it is asserted that Kyougoku teaches or discloses that "the one ore more passive port L1-L6 is connected to one or more passive ball (not labeled, ***ball connected to B2***)." (Emphasis added). The "ball connected to B2", however, is not a passive ball because B2 is disposed to receive a chip select signal. See, Kyougoku at col. 7, lines 29-30 ("chip select electrode pads B1 to B3…are formed on the surfaces of the substrates…") and Fig. 5.

Further still and solely for the sake of argument, even if the Office Action is correct in asserting that the "ball connected to B2" is a passive ball, claim 23 recites "…wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located opposite each other in repeating pattern…" Kyougoku fails to teach this recited element because, unlike in claim 23, the passive balls and passive pads that are connected to a passive port are ***not*** "located opposite each other in a repeating pattern". Cf., Kyougoku at FIG. 5 (unlabeled ball connected to B2, which is asserted to be a passive ball in the Office Action, is coupled to pad B1' via L1 but the unlabeled ball connected to B2 is not located opposite to pad B1' but is offset from B1').

Consequently, for at least one or the reasons stated above, Kyougoku fails to teach or

disclose each and every element recited in claim 23, rendering claim 23 allowable.

The First Section 103(a) Rejection

The Examiner rejects claim 16 by asserting this claim is allegedly unpatentable over Kyougoku. This rejection is respectfully traversed.

In the Office Action, it is asserted that with respect to claim 16, "Kyougoku shows the plurality of module 1000-1002 is rotated before being stacked and the one or more passive port L1-L6 forms a rotational routing path (Fig. 5). With respect, Applicants disagree.

A proper section 103 rejection, among other things, requires some suggestion or motivation in Kyougoku in Fig. 5 that would render the claimed invention obvious to one of ordinary skill in the art. Fig. 5 is a sectional view (Kyougoku at col. 7, lines 20-21), and thus, would not render the claimed invention obvious. Indeed, Kyougoku teaches away from a rotational routing path as recited in claim 16 because Kyougoku emphasizes that for ***each*** substrate, "the first chip select electrode is positioned at the endmost of N-number of chip select electrodes". Kyougoku at col. 3, line 56 through col. 4, line 30, Figs 1through Fig. 3, and Fig. 6. Positioning the first chip select electrode in the manner taught in Kyougoku precludes rotating one substrate relative to another substrate before stacking because each substrate is also disposed to have the same wiring structure (Id. at col. 3, lines 34-35), and all respective chip select electrodes from each substrate are aligned with each other when the substrates are stacked without rotation. (Id. at col. 3, lines 43-51 and elements B1/11 and C1/41 in Figs. 1 and 6), which would result in a misalignment of the respective first chip select electrodes (such as B1/11 and C1/41 of the substrates 1 and 2, respectively) should these substrates be rotated before stacking. Consequently, Kyougoku would not provide any teaching or suggestion that would render claim 16 obvious to

one or ordinary skill in the art because Kyougoku not only teaches away from the claimed invention but also its teachings would render the claimed invention inoperable.

In addition, claim 16 depends on allowable independent claim 14. Claim 14 is allowable because Kyougoku fails to teach or suggest each and every element recited in claim 1. For example, the alleged active signals, such as chip select signals B1 and B2 (Kyougoku at col. 6, lines 45-50), begin from an outside surface of the ***stacked*** module but are taught by Kyougoku to terminate on the other side (or outside opposite surface) of the stack module. See also, Kyougoku, D1,' D2' and D3' in FIG. 5 (FIG. 5 is a partial section view). See also, *Id. at* col. 3, line 65 to col. 4 line 15. The claimed invention, however, enables a controller module active pad(s) to be routed to a desired specific module ***within*** the stacked module. Consequently, Kyougoku fails to teach or suggest each element of the invention recited in claim 14, rendering claim 14 allowable. Since claim 14 is allowable, claim 16 is also allowable.

New Claims 27-31

Claims 27 through 31 are new but do not present new grounds for rejection, or add new matter.

Petition for Extension of Time and Payment of New Claim Fees

A Petition for an Extension of Time and Payment of New Claim Fees, if any, are submitted in a separate paper, respectively, and filed concurrently herewith.

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Request for Allowance

It is believed that this Amendment places this Application into condition for allowance.

Early favorable consideration of this Amendment is earnestly solicited.

Respectfully submitted,

Dated: 13 Feb 2009

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Application

For

United States Non-Provisional Utility Patent

Title:

Multiple Chip Module and Package Stacking Method For Storage Devices

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Multiple Chip Module and Package Stacking Method For Storage Devices

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BACKGROUND

Field

The present invention relates to computer systems. More particularly, the present invention relates to flash memory based semiconductor disk drives [[drive]] and a method of using multiple chip module (MCM) and Package Stacking technique to support miniaturization and memory scalability.

Description of Related Art

A flash [[Flash]] memory based semiconductor disk drive typically use separate packages for the interface controller, the DMA controller, the processor and separate packages for the Flash devices, the FPROMs and the RAMs. This current method limits the miniaturization of the entire storage device. In order to achieve the move to miniaturization, chip modules and packages need to be stacked. Stacking both on chip module and package level maximizes the capacity in a limited area thus realizing the move to miniaturize the entire storage device. A technique in stacking chip modules and

packages strategically to support miniaturization and memory scalability in both vertical and horizontal orientation is therefore proposed.

SUMMARY OF THE INVENTION

In the stacking technique illustrated in example embodiments of the present invention, semiconductor dies are mounted in a module to become a MCM which serves as the basic building block. Combination of these modules and dies in a substrate creates a package with specific function or a range of memory capacity. These packages are stacked to increase capacity or add functions. A combination of different existing technology such as flip chip, wire bond, MCM, module stacking, advance packaging, etc. are used to accomplish highly reliable module to module and package to package interconnection and scalability. A single package can have a wide range of capacity depending on the memory capacity of the die used and the number of modules stacked within the package. In the proposed package stacking technique, the stacked modules in a package serve as the building blocks for the package level stacking. Multiple packages are stacked to create the desired memory capacity and different packages are stacked to create desired function. Expansion can be done both on the vertical and horizontal orientations. The technique is in the assignment of pins. Small capacity miniature storage devices can use the vertical expansion, while high capacity devices with larger form factors can use both vertical and horizontal expansion to maximize capacity. By using this technique, large capacity storage devices are implemented in a small package device, and larger form factors achieve bigger memory capacities.

The present invention takes advantage of the existing stacking technology both on the module and package level. This maximizes the capacity in a small area, realizing the miniaturization transition. Modular approach is used in creating basic building blocks which can be tested individually and replaced easily prior to final packaging, making the technique reliable, and cost effective ~~effectively~~. A wide [[Wide]] range of capacity can be configured through variation of die capacities and stacking modules and/or packages. Expanding capacity may be implemented vertically, horizontally or both, depending on board area and desired capacity. ~~Expansions are implemented both vertically and horizontally depending on board area and desired capacity.~~

[[

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BRIEF DESCRIPTION OF DRAWINGS

So that the manner in which the above recited features, advantages and objects of the present invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the present invention may admit to other equally effective embodiments.

Figure 1a shows the block diagram of the stackable system for high performance, high capacity devices according to an example embodiment of the present invention.

Figure 1b shows the block diagram of the stackable system for lower performance, lower capacity devices according to an example embodiment of the present invention.

Figure 2a, 2b, 2c depict the SDRAM module's top and bottom drawings and a cross sectional representation of stacked multiple SDRAM modules according to an example embodiment of the present invention.

Figure 3a, 3b, 3c depict the flash module's top and bottom drawings and a cross sectional representation of stacked multiple flash modules according to an example embodiment of the present invention.

Figure 4a, 4b depict the first high-end controller module's top and bottom drawings according to an example embodiment of the present invention.

Figure 5a, 5b depict the memory module's top and bottom drawings according to an example embodiment of the present invention.

Figure 6a, 6b depict the first low-end controller module's top and bottom drawings according to an example embodiment of the present invention.

Figure 7a, 7b depict the second high-end controller module's top and bottom drawings according to an example embodiment of the present invention.

Figure 8a, 8b depict the second low-end controller module's top and bottom drawings according to an example embodiment of the present invention.

Figure 9 depicts the stacked SDRAM modules further stacked on the controller module according to an example embodiment of the present invention. This configuration is used for high end applications. The figure also shows how the balls have corresponding pads for inter-module connection.

Figure 10 depicts stacked flash modules further stacked on the memory module according to an example embodiment of the present invention. The figure also shows how the balls have corresponding pads for inter-module connection.

Figure 11 depicts the possible stacking options for the first high-end controller module and the memory modules according to an example embodiment of the present invention. A substrate interface is used to attach one group of stacked modules to another.

Figure 12a is an isometric exploded drawing of the stacking technique presented in Figure 11 according to an example embodiment of the present invention. _Multiple identical stacking is not included in this drawing.

Figure 12b is another package stacking technique using Pin Grid Array (PGA) rather than Ball Grid Array (BGA) according to an example embodiment of the present invention. _This is used for easy replacement and expansion.

Figure 13 depicts the low-end controller module configuration with stacked flash module according to an example embodiment of the present invention. _The figure also shows how the balls have corresponding pads for inter-module connection.

Figure 14 is an isometric exploded version of the stacking technique presented in Figure 11 according to an example embodiment of the present invention.

Figure 15a, 15b depict the second high-end controller module configuration with stacked memory modules according to an example embodiment of the present invention. _The figures also show how the balls have corresponding pads for inter-module connection.

Figure 16 is an isometric exploded version of the stacking technique presented in Figure 14 according to an example embodiment of the present invention.

Figure 17a, 17b depict the second low-end controller module configuration with stacked memory modules according to an example embodiment of the present invention. _The figures also show how the balls have corresponding pads for inter-module connection.

Figure 18 is an isometric exploded version of the stacking technique presented in Figure 17 according to an example embodiment of the present invention.

Figure 19 shows a pin assignment and connection technique to be able to select specific layer in a multi-stacked module according to an example embodiment of the present invention.

Figure 20a shows another pin assignment technique which uses a rotational stacking orientation to allow stacking of four identical modules representing different bus interfaces according to an example embodiment of the present invention.

Figure 20b shows a cross-section representation of the four stacked modules on a rotational stacking technique and how their pins mates according to an example embodiment of the present invention.

Figure 21a shows another pin assignment and connection technique to be able to connect a serial chain route from multiple modules in a stack according to an example embodiment of the present invention.

Figure 21b shows the routing of [[how]] a serial chain connection ~~is routed~~ from one stack location to another allowing application of both vertical and horizontal expansion independently or simultaneously according to an example embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1a is a block diagram of a flash storage system according to a first example embodiment of the present invention. The block diagram shows the entire high-end system that is modularized, stacked, and packaged to achieve the desired features of the technique. The heart of the system is the main controller-processor **101** which interfaces with the flash memory, the flash PROM and the SDRAM memory blocks. _The SDRAM is configured from a single bank **102** to a maximum of four banks depending on the desired capacity. Each bank such as **102** includes 3 SDRAMs. _The flash devices such as **107** are controlled by the Flash Interface Controller such as **105**. _Each controller supports four flash buses such as flash bus A11 **106**, and each flash bus supports a maximum of 8 flash devices. _The main controller-processor supports four flash interface controllers through 4 different busses such as B bus **104**. _The four flash interface controllers with their corresponding flash devices comprise the memory set **108**. _The main controller-processor can support from one memory set to a maximum of 15 memory sets. _This is a maximum support of 1,920 flash devices.

Figure 1b is a block diagram of a flash storage system according to a second example embodiment of the present invention. The block diagram shows the entire low-end system that is modularized, stacked, and packaged to achieve the desired features of the technique. Since a low-end system may [[does]] not require a large amount [[lot]] of memory capacity, SDRAM may [[can]] be limited to one bank **109**, or none at all, and the supported flash devices may [[is]] also be limited ~~minimal~~ to only two sets of flash buses. One set of flash buses **110** consists of four flash bus with 8 flash devices supported per flash bus, which results in [[. This is]] a maximum supported number of 64 flash devices.

From the basic dies; SDRAM, FPROM, flash memory, flash interface controller, and the main controller-processor, single and multiple chip modules are created to become the basic building blocks for the stacking technique presented in the present invention. Referring to figure 2a which is a top view of an SDRAM module, three SDRAM dies **201** are placed in a single substrate **203** to become the SDRAM module which is one of the basic building blocks. The SDRAM module is represented in figure 1 as a single bank **102** composed of SDRAM 00, SDRAM 01, and SDRAM 02 connected to the SDRAM interface **103**. All signals needed to interface to the controller module and other SDRAM modules are assigned in both the bottom balls **204** and top pads **202** respectively. Bottom balls **204** are shown in figure 2b which is a bottom view of the SDRAM module, three slots **205** are created under the SDRAM die's pad attach area to accommodate bottom wire bonding. Figure 2c is the stacked module cross sectional

representation. Top pads **202** and bottom balls **204** act as the vertical interconnects between all SDRAM modules and to the controller module. Varying the SDRAM die capacity and the stack quantity result in wide range of total SDRAM capacity depending on the product application. The SDRAM device organization, capacity and bank limitations are defined by the main controller-processor's SDRAM interface specifications. The main controller-processor intended to be used for this example embodiment of the present invention supports a 32-bit wide 4 banks maximum [[max]] SDRAM configuration.

Figure 3a is a top view[[,]] that shows four flash dies **301** in a single substrate **303** that collectively form part of a ~~becoming the~~ flash module, which can [[is]] also function as a basic building block. All signals needed to interface with the memory module and other flash modules are assigned in both the bottom balls **304** and the top pads **302**, respectively, as shown in FIGS. 3a, 3b and 3c. In figure 3c, the flash modules are stacked. Maximum stack quantity depends on the flash interface controller specifications. Top pads **302** and bottom balls **304** acts as the vertical interconnects between stacked flash modules and to the memory module. Varying the flash die capacity and the stacking quantity, results in a wide range of total flash capacity depending on the product application and capacity requirements. The flash device organization and capacity limitations are defined by the flash interface controller's specifications. The flash interface controller intended to be used for this used for this example embodiment of the present invention supports 8 flash devices per flash bus, thus allowing a maximum stacking of 8 flash modules.

Figure 4a shows the top view of the first example embodiment of the present invention illustrated in a first high-end controller module configuration. A single FPROM die **401** is placed at the center of the substrate **404**. Pads are composed of two sections, one for the SDRAM module interface shown as **402** and another for the memory module interface shown as **403**. This technique enables multiple stacking of both SDRAM modules and memory modules in a single package. Figure 4b shows the bottom view of the controller module. A single main controller-processor die **406** is placed at the center of the substrate. The controller module becomes a base module for the package. The [[balls**405**]]balls **405** are used to connect to the main substrate which is typically a printed circuit board (PCB).

Figure 5a shows the top view of the memory module which is also a basic building block. A single flash interface controller die **501** is placed on the center of the substrate **504**. Pads are composed of two sections, one for the flash module interface shown as **502** and another for the other memory module interface shown as **503**. This technique enables multiple stacking of flash modules and memory modules in a single package. The memory module becomes a base module for the package. Figure 5b shows the bottom view of the memory module. The memory module balls **505** are used to connect to the main substrate PCB, to the controller modules or to the other memory modules depending on the type of configuration desired.

Figure 6a shows the top view of the second example embodiment of the present invention illustrated in a first low-end controller module configuration. Two SDRAMs

601 and a single FPROM **602** are placed on top of the module. This configuration is flexible. The SDRAMs can be unpopulated in a low performance application. Internal SRAMs in the main controller-processor will take over the SDRAM functions. The main controller-processor **605** is placed at the bottom of the module. This configuration does not allow stacking of the SDRAM which is not necessary for low capacity applications. Flash modules are stacked on top, [[top]] interfacing to the pads **603.** The substrate **604** is the same size as the flash module making its final package smaller. The bottom balls **606** are used to interface with the main PCB.

Figure 7a shows the top view of the first example embodiment of the present invention illustrated in a second high-end controller module configuration, where four memory modules **701** can be mounted on separate locations adjacent to each other. Memory module interface pads **704** are allocated for multiple stack configurations. In the middle of the memory module interface pads, 3 SDRAM dies **702** are mounted. Each area corresponds to one SDRAM bank **703**, totaling to a maximum of 4 SDRAM banks in the package. The bottom view is presented in Figure 7b, where the main controller-processor die **705** and the FPROM die **706** are mounted adjacent to each other. The module's balls **707** are used for external interface to the main PCB.

Figure 8a shows the top view of the second example embodiment of the present invention illustrated in a second low-end controller module configuration, where only two memory modules **801** can be mounted side-by-side. Memory module interface pads **802** are allocated for multiple stacking configurations. In the middle of the memory

module interface pads, 3 SDRAM dies **803** are mounted. Each area corresponds to one SDRAM bank **804**, totaling to only a maximum of 2 SDRAM banks in a package. The SDRAM can either be mounted or not depending on the application. Internal SRAMs can also be used instead of the SDRAMs. The stacked memory modules can also be configured to support both internal and external flash interface controller applications. The bottom view is presented in Figure 8b, where the main controller-processor die **805** and the FPROM die **806** are mounted adjacent to each other. The module balls **807** are used for external interface to the main PCB.

Figure 9 shows the stacking of SDRAM module **901** and controller module **902**. A single or stacked SDRAM module can be placed on top of a controller module. The pads for the SDRAM module interface **903** must align with the SDRAM module balls **904**. The bottom-most SDRAM module **905** serves as bank 0, and the top-most module **906** serves as bank 3[[,]]. For low capacity SDRAM requirements, only a single or dual bank is enough. High capacity devices needs to have a maximum SDRAM capacity, thus stacking the maximum of 4 modules. The outer pads **907** are for the memory module interface.

Figure 10 shows the stacking of flash modules **1001** and memory module **1002**. A four-stack or eight-stack flash module is placed on top of a memory module. The pads for the flash module interface **1003** must align with the flash module balls **1004**. The outer pads **1005** are for other memory module interface. The flash interface controller intended to be used for this example embodiment of the present invention supports a maximum of

4 flash buses and each flash bus supports a maximum of 8 flash devices. The bottom-most flash module **1006** contains the 4 flash buses' Flash 00 devices and the top-most module **1007** contains the 4 flash buses' Flash 07 devices.

Figure 11 shows a sample of a maximized stacking technique that can be configured through vertical, horizontal or combined expansion. Multiple staking will increase the overall height of the module, thus requiring a filler **1101** to physically interconnect two stacked modules. A thinner filler **1102** may be used depending on the height differential between the modules which is dependent to the number of stacks applied. A controller module with the stacked SDRAM modules act as the controller package **1103**. A memory module with stacked flash modules acts as the memory package **1104**. Four memory packages stacked together form the memory set **1105**. Vertical expansion happens when the controller package is stacked with a single or multiple memory sets. The figure shows a single memory set to be stacked to the controller package. Horizontal expansion happens when the controller package is located on a different site on the PCB relative to the memory sets. Also multiple memory sets can be located on different sites on a PCB. Combo expansion happens when both vertical and horizontal expansion technique is implemented simultaneously. The expansion technique is very flexible depending on the desired memory capacity, main PCB size limitations and also height limitations.

Figure 12a shows the isometric and exploded drawing of the stacking technique for the first high-end controller configuration. Pins are assigned strategically and modules are stacked to make possible the miniaturization of the entire system in a package.

1201 – The Flash Module

1202 – The Flash Die

1203 – The Flash Module Pad Interface to other Flash Modules

1204 – The Flash Module Solder Balls

1205 – The Memory Module

1206 – The Flash Interface Controller Die

1207 – The Memory Module Pad Interface for the Flash Module

1208 – The Memory Module Pad Interface for the other Memory Modules

1209 – The Memory Module Solder Balls

1210 – The SDRAM Module

1211 – The SDRAM Die

1212 – The SDRAM Module Pad Interface to other SDRAM Modules

1213 – The SDRAM Module Solder Balls

1214 – The Controller Module

1215 – The FPROM Die on top side and the Main Controller-Processor Die at the bottom side.

1216 – The Controller Module Pad Interface to the SDRAM Modules

1217 – The Controller Module Pad Interface to the Memory Modules

1218 – The Controller Module Solder Balls

Figure 12b is another technique used in this invention to ease replacement and facilitate expansion. Instead of using Ball Grid Array (BGA), Pin Grid Array (PGA) **1219** is used. This method makes it more flexible due to the technology's inherent feature where replacement is done swiftly without any assembly process involved. Horizontal expansion is also benefited in this technology. The figure shows the stacked memory module as an example. The memory module is packaged using the PGA technology, where the top portion of the package becomes the socket **1220** and the bottom portion the pin arrays **1219**. The filler **1221** becomes the package's top socket and is interfaced into the base module **1222** through the BGA **1223**. The base module uses PGA to interface to the bottom package or to the main board **1224**. Filler **1225** is also mounted into the main board to interface the stacked memory modules.

Figure 13 shows the stacking of the flash module **1301** and the first low-end type of controller module **1302**. A single or stacked flash module can be placed on top of the controller module. The pads for the flash module interface **1303** must align with the flash module balls **1304**. This configuration is for low capacity low performance applications. The number of flash modules to be stacked depends on the desired capacity and is limited to the supported feature of the main controller-processor. The main controller-processor's flash interface can support a maximum of 8 buses and a maximum of 8 flash devices per bus.

Figure 14 shows the isometric and exploded drawing of the stacking technique for the first low-end controller configuration. Pins are assigned strategically and modules are stacked to make possible the miniaturization of the entire system in a package.

1401 – The Flash Module

1402 – The Flash Die

1403 – The Flash Module Pad Interface to other Flash Modules

1404 – The Flash Module Solder Balls

1405 – The Controller Module

1406 – The FPROM Die and the Main Controller-Processor Die at the bottom

1407 – The SDRAM Die

1408 – The Controller Module Pad Interface to the Flash Modules

1409 – The Controller Module Solder Balls

Figure 15a shows the stacking technique for the second high-end controller configuration. The stacked flash modules **1501** are further stacked on top of the memory modules **1502** which are then mounted on the controller module **1503** on four different locations. Four memory modules can be mounted on four different locations on the controller module creating a memory set. Stacking more memory sets increases the total capacity. The cross-sectional representation of the said stacking technique is shown in Figure 15b. The memory module balls **1504** must align to the pad interface **1505** on the controller module. As previously discussed in figure 11, fillers are used to physically connect two successively stacked modules. The controller balls **1506** will become the external interface to the main board. The final package is 4X bigger than the first high end option.

Figure 16 shows the isometric and exploded drawing of the stacking technique discussed in Figure 15. Pins are assigned strategically and modules stacked to make possible the maximum stacking and interconnection between modules. As previously discussed in figure 11, fillers are used to physically connect two stacked successively stacked modules.

1601 – The Flash Module

1602 – The Flash Dies

1603 – The Flash Module Pads Interface to other Flash Modules

1604 – The Flash Module Solder Balls

1605 – The Memory Module

1606 – The Flash Interface Controller Dies

1607 – The Memory Module Pad Interface to Flash Modules

1608 – The Memory Module Pad Interface to other Memory Modules

1609 – The Memory Module Solder Balls

1610 – The Controller Module

1611 – The SDRAM Dies on top side and the FPROM and Main Controller-Processor at the bottom side

1612 – The Controller Module Pads Interface to the Memory Modules

1613 – The Controller Module Solder Balls

Figure 17a shows the stacking technique for the second low-end configuration. The stacked flash modules **1701** are further stacked on top of the memory modules **1702** which are then mounted on the controller module **1703** on two different locations. This

technique can use both internal and external flash interface controller configurations, making this technique flexible. The cross-sectional view is shown in figure 17b. The memory module balls **1704** must align to the pad interface **1705** on the controller module. The controller balls **1706** will become the external interface to the main board. The final package is twice the size of the first high end option.

Figure 18 shows the isometric and exploded drawing of the stacking technique discussed in Figure 17. Pins are assigned strategically and modules stacked to make possible the maximum stacking and interconnection between modules. As previously discussed in figure 11, fillers are used to physically connect two stacked successively stacked modules.

1801 – The Flash Module

1802 – The Flash Dies

1803 – The Flash Module Pads Interface to other Flash Modules

1804 – The Flash Module Solder Balls

1805 – The Memory Module

1806 – The Flash Interface Controller Dies

1807 – The Memory Module Pad Interface to Flash Modules

1808 – The Memory Module Pad Interface to other Memory Modules

1809 – The Memory Module Solder Balls

1810 – The Controller Module

1811 – The SDRAM Dies on top side and the FPROM and Main Controller-Processor at the bottom side

1812 – The Controller Module Pads Interface to the Memory Modules

1813 – The Controller Module Solder Balls

A more detailed technique on how the pins are assigned and how modules are placed with different orientation in the stack is discussed in the following paragraphs.

Figure 19 shows a first pin assignment and connection technique that enables a selection of specific module in a multiple module stack. The figure illustrates the controller and SDRAM modules as an example. The SDRAM module[['s]] balls, such as **1907**, are represented by big oblong shapes, and the pads such as **1908** are represented by smaller oblong shapes. A pad[[Pad]] to ball connection is represented by a rectangle, such as **1906**. The controller module has four active pads such as **1904,** one each for the four SDRAM modules such as **1901**. The controller module's active pad 00 **1904** is connected to SDRAM module 0's X0 ball **1903**, pad 01 to SDRAM module 1's X0 ball **1902**, and so on. The X0 balls are the active balls[[ball]] for the SDRAM modules. All SDRAM modules are identical which include the connections as follows: X1 ball is connected to X1 pad, X2 ball to X2 pad, and so on. The technique involves using a ladder-like routing path, ~~**a ladder like routing**~~ such as **1905** on the stacked modules. This technique enables the controller module's active pad to be routed to the desired specific module in the stack. The example embodiment illustrated in figure 19 comprises a repeating pattern for the balls and pads. Passive balls are connected within each module to passive pads with an offset distance equaling one periodic distance of the repeating pattern. The importance is the approach using repeating pattern and offsetting

of the passive ball to passive pad within each module, other offset distances[[distance]] can be used also in other embodiment of the present invention, e.g. using an offset of two [[2]] or any multiple of the periodic distance of the repeating pattern. The example embodiment does not limit the scope of the present invention.

Another pin assignment, connection, and stacking combo method introduced in this invention is ~~**the rotational stacking technique**~~.the rotational stacking technique. Figure 20a shows the pad interconnects for a certain base module and strategic numbering is assigned. Pads labeled with numbers 1 to 4 represent the four[[4]] different groups of signals. Pads labeled with the number 5 are used for the vertical stacking IOs (more details are illustrated in figure 21a). Pads labeled with the number 6 are reserved for power and ground which are common to all modules in the stack. Since the stacked modules are identical, we can use rotational stacking to connect one module to one group of signals and the following rotated stacked module connects to another group of signals, and so on. This way ensures four identical modules to be stacked and connected to four different groups of signals from the base module which is typically a controller. Pad 1 **2001,** upon the substrate being rotated 90 degrees clockwise, occupies pad 2 **2002** location relative to an un-rotated substrate such as the base substrate which is typically a controller. In a similar manner pad 1 **2001** can be located at pad 3 **2003** location, then pad 4 **2004** location upon the substrate being rotated 180 and 270 degrees clockwise respectively.

Figure 20b shows a cross-sectional view of four such modules stacked over the base module. Memory and Controller modules are used as example. Pin 1s such as **2005** on the stacked modules are the only active signal pins for the module. The rest (numbered 2 to 4) **2006** are directly connected to the balls underneath them but have[[has]] no other connections. This way connection is continued from bottom to top. The active pin **2007** of the first module **2008** is aligned to pin 1 pad **2009** on the base module, and the second module's active pin **2010** is aligned on pin 2 **2011** of the base module with second module being rotated 90 degrees clockwise. Since pin 2 **2012** on the first module is directly connected to the ball underneath, this allows the pin 1 on the second module **2013** to be connected to pin 2 **2011** of the base module. Rotating the next stacked module 90 degrees more, will align it's active pin to the base module[[s]] pin 3 and so on until the forth rotation.

The last connection technique is used for serial routing of all modules in the stack and allowing them to be externally accessible for horizontal expansion on a PCB, such as a main board. Figure 21a shows how this technique is implemented in the stacking method. The main board **2101** contains the input signals **2102** which will then be connected to IN ball **2104** of the base module **2103**. The base module's OUT pad **2105** is connected to IN ball **2107** of the first stack module **2106**, and so on. The top module **2108** terminates the signal to the top pad **2109** and routes, with connection **2112,** the signal internally to another pad **2110** which is connected directly to the ball **2113** underneath. [[.]] Since the modules are identical, this routed signal passes through the pads and balls **2111** of the stack until it reaches the OUT pad **2114** of the main board for

external access. How the top module terminates the serial chain and branches them out to other pads is shown in Figure 21b. All modules[[module]] have a selectable buffer **2115** that tri-states the input when pulled low. The signal from the IN balls **2116** enters the internal circuit **2117** and exits the circuit connecting to the OUT pad **2118**. The buffer's **2115** control line is weakly pulled up internally. The "StkLow" ball is connected internally to GND **2119**, thus pulling down the buffer control line when a module is stacked above it, and it is[[it's]] pulled up when no module is stacked directly above it. When the buffer control line is pulled high, it will let the input signal branch out **2120** to the other pads, thus creating a connection route or trace that loops~~making possible the trace to loop~~ back to the base module~~module's~~ solder balls. When a module is stacked above a module that is disposed with selectable buffer **2115** in the manner shown, the buffer control signal is pulled low, tri-stating the input signal and disallowing the branching effect. This technique allows the signal to be accessible to the external balls of the base module, thus horizontal expansion for a serial signal is achievable. The balls are then routed, with connection **2121,** to the other modules **2122** on the other locations. The same technique is used on the main board **2123**, when no package is detected on the "StkLow" pad, the buffer allows the input to connect to the designated pads on the other locations. The tri-stated buffer technique is redundant to all locations. An example is the JTAG TDI-TDO signal. The diver circuit **2125** sends out TDI signals to the pads and the closing TDO signal **2124** loops back to the driver circuit.

Combining these stacking, pin assigning and connection techniques allow interconnection between modules with both parallel and series signals to both vertical and

horizontal expansion. The technique is very flexible depending on the specific application, capacity, board size and height limit.

ABSTRACT

Stacking techniques are illustrated in example embodiments of the present invention wherein semiconductor dies are mounted in a module to become a MCM which serves as the basic building block. A combination~~Combination~~ of these modules and dies in a substrate creates a package with specific function or a range of memory capacity. Several example system configurations are provided using BGA and PGA to illustrate the stacking technique. Several pin assignment and signal routing techniques are illustrated wherein internal and external signals are routed from main board to various stacked modules. Expansion can be done both on the vertical and horizontal orientations.

Application

For

United States Non-Provisional Utility Patent

Title:

Multiple Chip Module and Package Stacking Method For Storage Devices

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Multiple Chip Module and Package Stacking Method For Storage Devices

BACKGROUND

Field

The present invention relates to computer systems. More particularly, the present invention relates to flash memory based semiconductor disk drives and a method of using multiple chip module (MCM) and Package Stacking technique to support miniaturization and memory scalability.

Description of Related Art

A flash memory based semiconductor disk drive typically use separate packages for the interface controller, the DMA controller, the processor and separate packages for the Flash devices, the FPROMs and the RAMs. This current method limits the miniaturization of the entire storage device. In order to achieve the move to miniaturization, chip modules and packages need to be stacked. Stacking both on chip module and package level maximizes the capacity in a limited area thus realizing the move to miniaturize the entire storage device. A technique in stacking chip modules and packages strategically to support miniaturization and memory scalability in both vertical and horizontal orientation is therefore proposed.

SUMMARY OF THE INVENTION

In the stacking technique illustrated in example embodiments of the present invention, semiconductor dies are mounted in a module to become a MCM which serves as the basic building block. Combination of these modules and dies in a substrate creates a package with specific function or a range of memory capacity. These packages are stacked to increase capacity or add functions. A combination of different existing technology such as flip chip, wire bond, MCM, module stacking, advance packaging, etc. are used to accomplish highly reliable module to module and package to package interconnection and scalability. A single package can have a wide range of capacity depending on the memory capacity of the die used and the number of modules stacked within the package. In the proposed package stacking technique, the stacked modules in a package serve as the building blocks for the package level stacking. Multiple packages are stacked to create the desired memory capacity and different packages are stacked to create desired function. Expansion can be done both on the vertical and horizontal orientations. The technique is in the assignment of pins. Small capacity miniature storage devices can use the vertical expansion, while high capacity devices with larger form factors can use both vertical and horizontal expansion to maximize capacity. By using this technique, large capacity storage devices are implemented in a small package device, and larger form factors achieve bigger memory capacities.

The present invention takes advantage of the existing stacking technology both on the module and package level. This maximizes the capacity in a small area, realizing the miniaturization transition. Modular approach is used in creating basic building blocks

which can be tested individually and replaced easily prior to final packaging, making the technique reliable, and cost effective. A wide range of capacity can be configured through variation of die capacities and stacking modules and/or packages. Expanding capacity may be implemented vertically, horizontally or both, depending on board area and desired capacity.

BRIEF DESCRIPTION OF DRAWINGS

So that the manner in which the above recited features, advantages and objects of the present invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the present invention may admit to other equally effective embodiments.

Figure 1a shows the block diagram of the stackable system for high performance, high capacity devices according to an example embodiment of the present invention.

Figure 1b shows the block diagram of the stackable system for lower performance, lower capacity devices according to an example embodiment of the present invention.

Figure 2a, 2b, 2c depict the SDRAM module's top and bottom drawings and a cross sectional representation of stacked multiple SDRAM modules according to an example embodiment of the present invention.

Figure 3a, 3b, 3c depict the flash module's top and bottom drawings and a cross sectional representation of stacked multiple flash modules according to an example embodiment of the present invention.

Figure 4a, 4b depict the first high-end controller module's top and bottom drawings according to an example embodiment of the present invention.

Figure 5a, 5b depict the memory module's top and bottom drawings according to an example embodiment of the present invention.

Figure 6a, 6b depict the first low-end controller module's top and bottom drawings according to an example embodiment of the present invention.

Figure 7a, 7b depict the second high-end controller module's top and bottom drawings according to an example embodiment of the present invention.

Figure 8a, 8b depict the second low-end controller module's top and bottom drawings according to an example embodiment of the present invention.

Figure 9 depicts the stacked SDRAM modules further stacked on the controller module according to an example embodiment of the present invention. This configuration is used for high end applications. The figure also shows how the balls have corresponding pads for inter-module connection.

Figure 10 depicts stacked flash modules further stacked on the memory module according to an example embodiment of the present invention. The figure also shows how the balls have corresponding pads for inter-module connection.

Figure 11 depicts the possible stacking options for the first high-end controller module and the memory modules according to an example embodiment of the present invention. A substrate interface is used to attach one group of stacked modules to another.

Figure 12a is an isometric exploded drawing of the stacking technique presented in Figure 11 according to an example embodiment of the present invention. Multiple identical stacking is not included in this drawing.

Figure 12b is another package stacking technique using Pin Grid Array (PGA) rather than Ball Grid Array (BGA) according to an example embodiment of the present invention. This is used for easy replacement and expansion.

Figure 13 depicts the low-end controller module configuration with stacked flash module according to an example embodiment of the present invention. The figure also shows how the balls have corresponding pads for inter-module connection.

Figure 14 is an isometric exploded version of the stacking technique presented in Figure 11 according to an example embodiment of the present invention.

Figure 15a, 15b depict the second high-end controller module configuration with stacked memory modules according to an example embodiment of the present invention. The figures also show how the balls have corresponding pads for inter-module connection.

Figure 16 is an isometric exploded version of the stacking technique presented in Figure 14 according to an example embodiment of the present invention.

Figure 17a, 17b depict the second low-end controller module configuration with stacked memory modules according to an example embodiment of the present invention. The figures also show how the balls have corresponding pads for inter-module connection.

Figure 18 is an isometric exploded version of the stacking technique presented in Figure 17 according to an example embodiment of the present invention.

Figure 19 shows a pin assignment and connection technique to be able to select specific layer in a multi-stacked module according to an example embodiment of the present invention.

Figure 20a shows another pin assignment technique which uses a rotational stacking orientation to allow stacking of four identical modules representing different bus interfaces according to an example embodiment of the present invention.

Figure 20b shows a cross-section representation of the four stacked modules on a rotational stacking technique and how their pins mates according to an example embodiment of the present invention.

Figure 21a shows another pin assignment and connection technique to be able to connect a serial chain route from multiple modules in a stack according to an example embodiment of the present invention.

Figure 21b shows the routing of a serial chain connection from one stack location to another allowing application of both vertical and horizontal expansion independently or simultaneously according to an example embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1a is a block diagram of a flash storage system according to a first example embodiment of the present invention. The block diagram shows the entire high-end system that is modularized, stacked, and packaged to achieve the desired features of the technique. The heart of the system is the main controller-processor **101** which interfaces with the flash memory, the flash PROM and the SDRAM memory blocks. The SDRAM is configured from a single bank **102** to a maximum of four banks depending on the desired capacity. Each bank such as **102** includes 3 SDRAMs. The flash devices such as **107** are controlled by the Flash Interface Controller such as **105**. Each controller supports four flash buses such as flash bus A11 **106**, and each flash bus supports a maximum of 8 flash devices. The main controller-processor supports four flash interface controllers through 4 different busses such as B bus **104**. The four flash interface controllers with their corresponding flash devices comprise the memory set **108**. The main controller-processor can support from one memory set to a maximum of 15 memory sets. This is a maximum support of 1,920 flash devices.

Figure 1b is a block diagram of a flash storage system according to a second example embodiment of the present invention. The block diagram shows the entire low-end system that is modularized, stacked, and packaged to achieve the desired features of the technique. Since a low-end system may not require a large amount of memory capacity, SDRAM may be limited to one bank **109**, or none at all, and the supported flash devices may also be limited to only two sets of flash buses. One set of flash buses **110**

consists of four flash bus with 8 flash devices supported per flash bus, which results in a maximum supported number of 64 flash devices.

From the basic dies; SDRAM, FPROM, flash memory, flash interface controller, and the main controller-processor, single and multiple chip modules are created to become the basic building blocks for the stacking technique presented in the present invention. Referring to figure 2a which is a top view of an SDRAM module, three SDRAM dies **201** are placed in a single substrate **203** to become the SDRAM module which is one of the basic building blocks. The SDRAM module is represented in figure 1 as a single bank **102** composed of SDRAM 00, SDRAM 01, and SDRAM 02 connected to the SDRAM interface **103**. All signals needed to interface to the controller module and other SDRAM modules are assigned in both the bottom balls **204** and top pads **202** respectively. Bottom balls **204** are shown in figure 2b which is a bottom view of the SDRAM module, three slots **205** are created under the SDRAM die's pad attach area to accommodate bottom wire bonding. Figure 2c is the stacked module cross sectional representation. Top pads **202** and bottom balls **204** act as the vertical interconnects between all SDRAM modules and to the controller module. Varying the SDRAM die capacity and the stack quantity, results in wide range of total SDRAM capacity depending on the product application. The SDRAM device organization, capacity and bank limitations are defined by the main controller-processor's SDRAM interface specifications. The main controller-processor intended to be used for this example embodiment of the present invention supports a 32-bit wide 4 banks maximum SDRAM configuration.

Figure 3a is a top view that shows four flash dies **301** in a single substrate **303** that collectively form part of a flash module, which can also function as a basic building block. All signals needed to interface with the memory module and other flash modules are assigned in both the bottom balls **304** and the top pads **302**, respectively, as shown in FIGS. 3a, 3b and 3c. In figure 3c, the flash modules are stacked. Maximum stack quantity depends on the flash interface controller specifications. Top pads **302** and bottom balls **304** acts as the vertical interconnects between stacked flash modules and to the memory module. Varying the flash die capacity and the stacking quantity, results in a wide range of total flash capacity depending on the product application and capacity requirements. The flash device organization and capacity limitations are defined by the flash interface controller's specifications. The flash interface controller intended to be used for this used for this example embodiment of the present invention supports 8 flash devices per flash bus, thus allowing a maximum stacking of 8 flash modules.

Figure 4a shows the top view of the first example embodiment of the present invention illustrated in a first high-end controller module configuration. A single FPROM die **401** is placed at the center of the substrate **404**. Pads are composed of two sections, one for the SDRAM module interface shown as **402** and another for the memory module interface shown as **403**. This technique enables multiple stacking of both SDRAM modules and memory modules in a single package. Figure 4b shows the bottom view of the controller module. A single main controller-processor die **406** is placed at the center of the substrate. The controller module becomes a base module for the package.

The balls **405** are used to connect to the main substrate which is typically a printed circuit board (PCB).

Figure 5a shows the top view of the memory module which is also a basic building block. _A single flash interface controller die **501** is placed on the center of the substrate **504**. _Pads are composed of two sections, one for the flash module interface shown as **502** and another for the other memory module interface shown as **503**. _This technique enables multiple stacking of flash modules and memory modules in a single package. The memory module becomes a base module for the package. _Figure 5b shows the bottom view of the memory module. _The memory module balls **505** are used to connect to the main substrate PCB, to the controller modules or to the other memory modules depending on the type of configuration desired.

Figure 6a shows the top view of the second example embodiment of the present invention illustrated in a first low-end controller module configuration. Two SDRAMs **601** and a single FPROM **602** are placed on top of the module. This configuration is flexible. The SDRAMs can be unpopulated in a low performance application. Internal SRAMs in the main controller-processor will take over the SDRAM functions. The main controller-processor **605** is placed at the bottom of the module. This configuration does not allow stacking of the SDRAM which is not necessary for low capacity applications. Flash modules are stacked on top, interfacing to the pads **603.** The substrate **604** is the same size as the flash module making its final package smaller. The bottom balls **606** are used to interface with the main PCB.

Figure 7a shows the top view of the first example embodiment of the present invention illustrated in a second high-end controller module configuration, where four memory modules **701** can be mounted on separate locations adjacent to each other. Memory module interface pads **704** are allocated for multiple stack configurations. In the middle of the memory module interface pads, 3 SDRAM dies **702** are mounted. Each area corresponds to one SDRAM bank **703**, totaling to a maximum of 4 SDRAM banks in the package. The bottom view is presented in Figure 7b, where the main controller-processor die **705** and the FPROM die **706** are mounted adjacent to each other. The module's balls **707** are used for external interface to the main PCB.

Figure 8a shows the top view of the second example embodiment of the present invention illustrated in a second low-end controller module configuration, where only two memory modules **801** can be mounted side-by-side. Memory module interface pads **802** are allocated for multiple stacking configurations. In the middle of the memory module interface pads, 3 SDRAM dies **803** are mounted. Each area corresponds to one SDRAM bank **804**, totaling to only a maximum of 2 SDRAM banks in a package. The SDRAM can either be mounted or not depending on the application. Internal SRAMs can also be used instead of the SDRAMs. The stacked memory modules can also be configured to support both internal and external flash interface controller applications. The bottom view is presented in Figure 8b, where the main controller-processor die **805** and the FPROM die **806** are mounted adjacent to each other. The module balls **807** are used for external interface to the main PCB.

Figure 9 shows the stacking of SDRAM module **901** and controller module **902**. A single or stacked SDRAM module can be placed on top of a controller module. The pads for the SDRAM module interface **903** must align with the SDRAM module balls **904**. The bottom-most SDRAM module **905** serves as bank 0, and the top-most module **906** serves as bank 3. For low capacity SDRAM requirements, only a single or dual bank is enough. High capacity devices needs to have a maximum SDRAM capacity, thus stacking the maximum of 4 modules. The outer pads **907** are for the memory module interface.

Figure 10 shows the stacking of flash modules **1001** and memory module **1002**. A four-stack or eight-stack flash module is placed on top of a memory module. The pads for the flash module interface **1003** must align with the flash module balls **1004**. The outer pads **1005** are for other memory module interface. The flash interface controller intended to be used for this example embodiment of the present invention supports a maximum of 4 flash buses and each flash bus supports a maximum of 8 flash devices. The bottom-most flash module **1006** contains the 4 flash buses' Flash 00 devices and the top-most module **1007** contains the 4 flash buses' Flash 07 devices.

Figure 11 shows a sample of a maximized stacking technique that can be configured through vertical, horizontal or combined expansion. Multiple staking will increase the overall height of the module, thus requiring a filler **1101** to physically interconnect two stacked modules. A thinner filler **1102** may be used depending on the height differential between the modules which is dependent to the number of stacks

applied. A controller module with the stacked SDRAM modules act as the controller package **1103**. A memory module with stacked flash modules acts as the memory package **1104**. Four memory packages stacked together form the memory set **1105**. Vertical expansion happens when the controller package is stacked with a single or multiple memory sets. The figure shows a single memory set to be stacked to the controller package. Horizontal expansion happens when the controller package is located on a different site on the PCB relative to the memory sets. Also multiple memory sets can be located on different sites on a PCB. Combo expansion happens when both vertical and horizontal expansion technique is implemented simultaneously. The expansion technique is very flexible depending on the desired memory capacity, main PCB size limitations and also height limitations.

Figure 12a shows the isometric and exploded drawing of the stacking technique for the first high-end controller configuration. Pins are assigned strategically and modules are stacked to make possible the miniaturization of the entire system in a package.

1201 – The Flash Module

1202 – The Flash Die

1203 – The Flash Module Pad Interface to other Flash Modules

1204 – The Flash Module Solder Balls

1205 – The Memory Module

1206 – The Flash Interface Controller Die

1207 – The Memory Module Pad Interface for the Flash Module

1208 – The Memory Module Pad Interface for the other Memory Modules

1209 – The Memory Module Solder Balls

1210 – The SDRAM Module

1211 – The SDRAM Die

1212 – The SDRAM Module Pad Interface to other SDRAM Modules

1213 – The SDRAM Module Solder Balls

1214 – The Controller Module

1215 – The FPROM Die on top side and the Main Controller-Processor Die at the bottom side.

1216 – The Controller Module Pad Interface to the SDRAM Modules

1217 – The Controller Module Pad Interface to the Memory Modules

1218 – The Controller Module Solder Balls

Figure 12b is another technique used in this invention to ease replacement and facilitate expansion. Instead of using Ball Grid Array (BGA), Pin Grid Array (PGA) **1219** is used. This method makes it more flexible due to the technology's inherent feature where replacement is done swiftly without any assembly process involved. Horizontal expansion is also benefited in this technology. The figure shows the stacked memory module as an example. The memory module is packaged using the PGA technology, where the top portion of the package becomes the socket **1220** and the bottom portion the pin arrays **1219**. The filler **1221** becomes the package's top socket and is interfaced into the base module **1222** through the BGA **1223**. The base module uses PGA to interface to the bottom package or to the main board **1224**. Filler **1225** is also mounted into the main board to interface the stacked memory modules.

Figure 13 shows the stacking of the flash module **1301** and the first low-end type of controller module **1302**. A single or stacked flash module can be placed on top of the controller module. The pads for the flash module interface **1303** must align with the flash module balls **1304**. This configuration is for low capacity low performance applications. The number of flash modules to be stacked depends on the desired capacity and is limited to the supported feature of the main controller-processor. The main controller-processor's flash interface can support a maximum of 8 buses and a maximum of 8 flash devices per bus.

Figure 14 shows the isometric and exploded drawing of the stacking technique for the first low-end controller configuration. Pins are assigned strategically and modules are stacked to make possible the miniaturization of the entire system in a package.

1401 – The Flash Module

1402 – The Flash Die

1403 – The Flash Module Pad Interface to other Flash Modules

1404 – The Flash Module Solder Balls

1405 – The Controller Module

1406 – The FPROM Die and the Main Controller-Processor Die at the bottom

1407 – The SDRAM Die

1408 – The Controller Module Pad Interface to the Flash Modules

1409 – The Controller Module Solder Balls

Figure 15a shows the stacking technique for the second high-end controller configuration. The stacked flash modules **1501** are further stacked on top of the memory modules **1502** which are then mounted on the controller module **1503** on four different locations. Four memory modules can be mounted on four different locations on the controller module creating a memory set. Stacking more memory sets increases the total capacity. The cross-sectional representation of the said stacking technique is shown in Figure 15b. The memory module balls **1504** must align to the pad interface **1505** on the controller module. As previously discussed in figure 11, fillers are used to physically connect two successively stacked modules. The controller balls **1506** will become the external interface to the main board. The final package is 4X bigger than the first high end option.

Figure 16 shows the isometric and exploded drawing of the stacking technique discussed in Figure 15. Pins are assigned strategically and modules stacked to make possible the maximum stacking and interconnection between modules. As previously discussed in figure 11, fillers are used to physically connect two stacked successively stacked modules.

1601 – The Flash Module

1602 – The Flash Dies

1603 – The Flash Module Pads Interface to other Flash Modules

1604 – The Flash Module Solder Balls

1605 – The Memory Module

1606 – The Flash Interface Controller Dies

1607 – The Memory Module Pad Interface to Flash Modules

1608 – The Memory Module Pad Interface to other Memory Modules

1609 – The Memory Module Solder Balls

1610 – The Controller Module

1611 – The SDRAM Dies on top side and the FPROM and Main Controller-Processor at the bottom side

1612 – The Controller Module Pads Interface to the Memory Modules

1613 – The Controller Module Solder Balls

Figure 17a shows the stacking technique for the second low-end configuration. The stacked flash modules **1701** are further stacked on top of the memory modules **1702** which are then mounted on the controller module **1703** on two different locations. This technique can use both internal and external flash interface controller configurations, making this technique flexible. The cross-sectional view is shown in figure 17b. The memory module balls **1704** must align to the pad interface **1705** on the controller module. The controller balls **1706** will become the external interface to the main board. The final package is twice the size of the first high end option.

Figure 18 shows the isometric and exploded drawing of the stacking technique discussed in Figure 17. Pins are assigned strategically and modules stacked to make possible the maximum stacking and interconnection between modules. As previously discussed in figure 11, fillers are used to physically connect two stacked successively stacked modules.

1801 – The Flash Module

1802 – The Flash Dies

1803 – The Flash Module Pads Interface to other Flash Modules

1804 – The Flash Module Solder Balls

1805 – The Memory Module

1806 – The Flash Interface Controller Dies

1807 – The Memory Module Pad Interface to Flash Modules

1808 – The Memory Module Pad Interface to other Memory Modules

1809 – The Memory Module Solder Balls

1810 – The Controller Module

1811 – The SDRAM Dies on top side and the FPROM and Main Controller-Processor at the bottom side

1812 – The Controller Module Pads Interface to the Memory Modules

1813 – The Controller Module Solder Balls

A more detailed technique on how the pins are assigned and how modules are placed with different orientation in the stack is discussed in the following paragraphs.

Figure 19 shows a first pin assignment and connection technique that enables a selection of specific module in a multiple module stack. The figure illustrates the controller and SDRAM modules as an example. The SDRAM module balls, such as **1907**, are represented by big oblong shapes, and the pads such as **1908** are represented by smaller oblong shapes. A pad to ball connection is represented by a rectangle, such as

1906. The controller module has four active pads such as **1904,** one each for the four SDRAM modules such as **1901**. The controller module's active pad 00 **1904** is connected to SDRAM module 0's X0 ball **1903**, pad 01 to SDRAM module 1's X0 ball **1902**, and so on. The X0 balls are the active balls for the SDRAM modules. _All SDRAM modules are identical which include the connections as follows: X1 ball is connected to X1 pad, X2 ball to X2 pad, and so on. The technique involves using a ladder-like routing path, such as **1905** on the stacked modules. This technique enables the controller module's active pad to be routed to the desired specific module in the stack. The example embodiment illustrated in figure 19 comprises a repeating pattern for the balls and pads. Passive balls are connected within each module to passive pads with an offset distance equaling one periodic distance of the repeating pattern. The importance is the approach using repeating pattern and offsetting of the passive ball to passive pad within each module, other offset distances can be used also in other embodiment of the present invention, e.g. using an offset of two or any multiple of the periodic distance of the repeating pattern. The example embodiment does not limit the scope of the present invention.

Another pin assignment, connection, and stacking combo method introduced in this invention is the rotational stacking technique. Figure 20a shows the pad interconnects for a certain base module and strategic numbering is assigned. _Pads labeled with numbers 1 to 4 represent the four different groups of signals. Pads labeled with the number 5 are used for the vertical stacking IOs (more details are illustrated in figure 21a). Pads labeled with the number 6 are reserved for power and ground which are common to

all modules in the stack. Since the stacked modules are identical, we can use rotational stacking to connect one module to one group of signals and the following rotated stacked module connects to another group of signals, and so on. This way ensures four identical modules to be stacked and connected to four different groups of signals from the base module which is typically a controller. Pad 1 **2001,** upon the substrate being rotated 90 degrees clockwise, occupies pad 2 **2002** location relative to an un-rotated substrate such as the base substrate which is typically a controller. In a similar manner pad 1 **2001** can be located at pad 3 **2003** location, then pad 4 **2004** location upon the substrate being rotated 180 and 270 degrees clockwise respectively.

Figure 20b shows a cross-sectional view of four such modules stacked over the base module. Memory and Controller modules are used as example. Pin 1s such as **2005** on the stacked modules are the only active signal pins for the module. The rest (numbered 2 to 4) **2006** are directly connected to the balls underneath them but have no other connections. This way connection is continued from bottom to top. The active pin **2007** of the first module **2008** is aligned to pin 1 pad **2009** on the base module, and the second module's active pin **2010** is aligned on pin 2 **2011** of the base module with second module being rotated 90 degrees clockwise. Since pin 2 **2012** on the first module is directly connected to the ball underneath, this allows the pin 1 on the second module **2013** to be connected to pin 2 **2011** of the base module. Rotating the next stacked module 90 degrees more, will align it's active pin to the base module pin 3 and so on until the forth rotation.

The last connection technique is used for serial routing of all modules in the stack and allowing them to be externally accessible for horizontal expansion on a PCB, such as a main board. Figure 21a shows how this technique is implemented in the stacking method. The main board **2101** contains the input signals **2102** which will then be connected to IN ball **2104** of the base module **2103**. The base module's OUT pad **2105** is connected to IN ball **2107** of the first stack module **2106**, and so on. The top module **2108** terminates the signal to the top pad **2109** and routes, with connection **2112,** the signal internally to another pad **2110** which is connected directly to the ball **2113** underneath. Since the modules are identical, this routed signal passes through the pads and balls **2111** of the stack until it reaches the OUT pad **2114** of the main board for external access. How the top module terminates the serial chain and branches them out to other pads is shown in Figure 21b. All modules have a selectable buffer **2115** that tri-states the input when pulled low. The signal from the IN balls **2116** enters the internal circuit **2117** and exits the circuit connecting to the OUT pad **2118**. The buffer's **2115** control line is weakly pulled up internally. The "StkLow" ball is connected internally to GND **2119**, thus pulling down the buffer control line when a module is stacked above it, and it is pulled up when no module is stacked directly above it. When the buffer control line is pulled high, it will let the input signal branch out **2120** to the other pads, thus creating a connection route or trace that loops back to the base module solder balls. When a module is stacked above a module that is disposed with selectable buffer **2115** in the manner shown, the buffer control signal is pulled low, tri-stating the input signal and disallowing the branching effect. This technique allows the signal to be accessible to the external balls of the base module, thus horizontal expansion for a serial signal is

achievable. The balls are then routed, with connection **2121,** to the other modules **2122** on the other locations. The same technique is used on the main board **2123**, when no package is detected on the "StkLow" pad, the buffer allows the input to connect to the designated pads on the other locations. The tri-stated buffer technique is redundant to all locations. An example is the JTAG TDI-TDO signal. The diver circuit **2125** sends out TDI signals to the pads and the closing TDO signal **2124** loops back to the driver circuit.

Combining these stacking, pin assigning and connection techniques allow interconnection between modules with both parallel and series signals to both vertical and horizontal expansion. The technique is very flexible depending on the specific application, capacity, board size and height limit.

ABSTRACT

Stacking techniques are illustrated in example embodiments of the present invention wherein semiconductor dies are mounted in a module to become a MCM which serves as the basic building block. A combination of these modules and dies in a substrate creates a package with specific function or a range of memory capacity. Several example system configurations are provided using BGA and PGA to illustrate the stacking technique. Several pin assignment and signal routing techniques are illustrated wherein internal and external signals are routed from main board to various stacked modules. Expansion can be done both on the vertical and horizontal orientations.

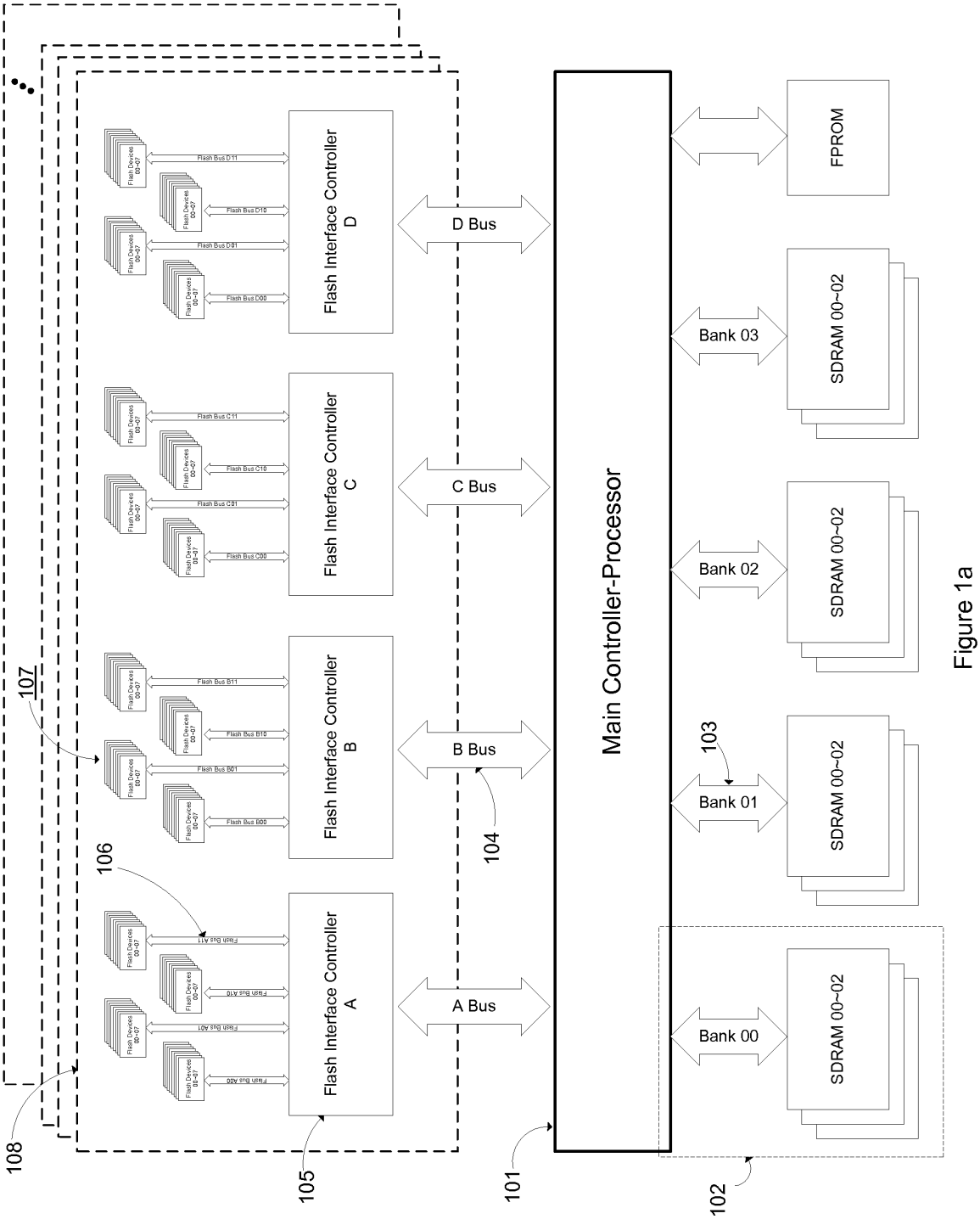

Flash Interface Controller D
Flash Interface Controller C
Flash Interface Controller B
Flash Interface Controller A
D Bus
C Bus
B Bus
A Bus
Main Controller-Processor
FPROM
Bank 03
Bank 02
Bank 01
Bank 00
SDRAM 00~02
SDRAM 00~02
SDRAM 00~02
SDRAM 00~02
Flash Devices 00~07
Flash Bus D11
Flash Bus D10
Flash Bus D01
Flash Bus D00
Flash Bus C11
Flash Bus C10
Flash Bus C01
Flash Bus C00
Flash Bus B11
Flash Bus B10
Flash Bus B01
Flash Bus B00
Flash Bus A11
Flash Bus A10
Flash Bus A01
Flash Bus A00
101
102
103
104
105
106
107
108

Figure 1a

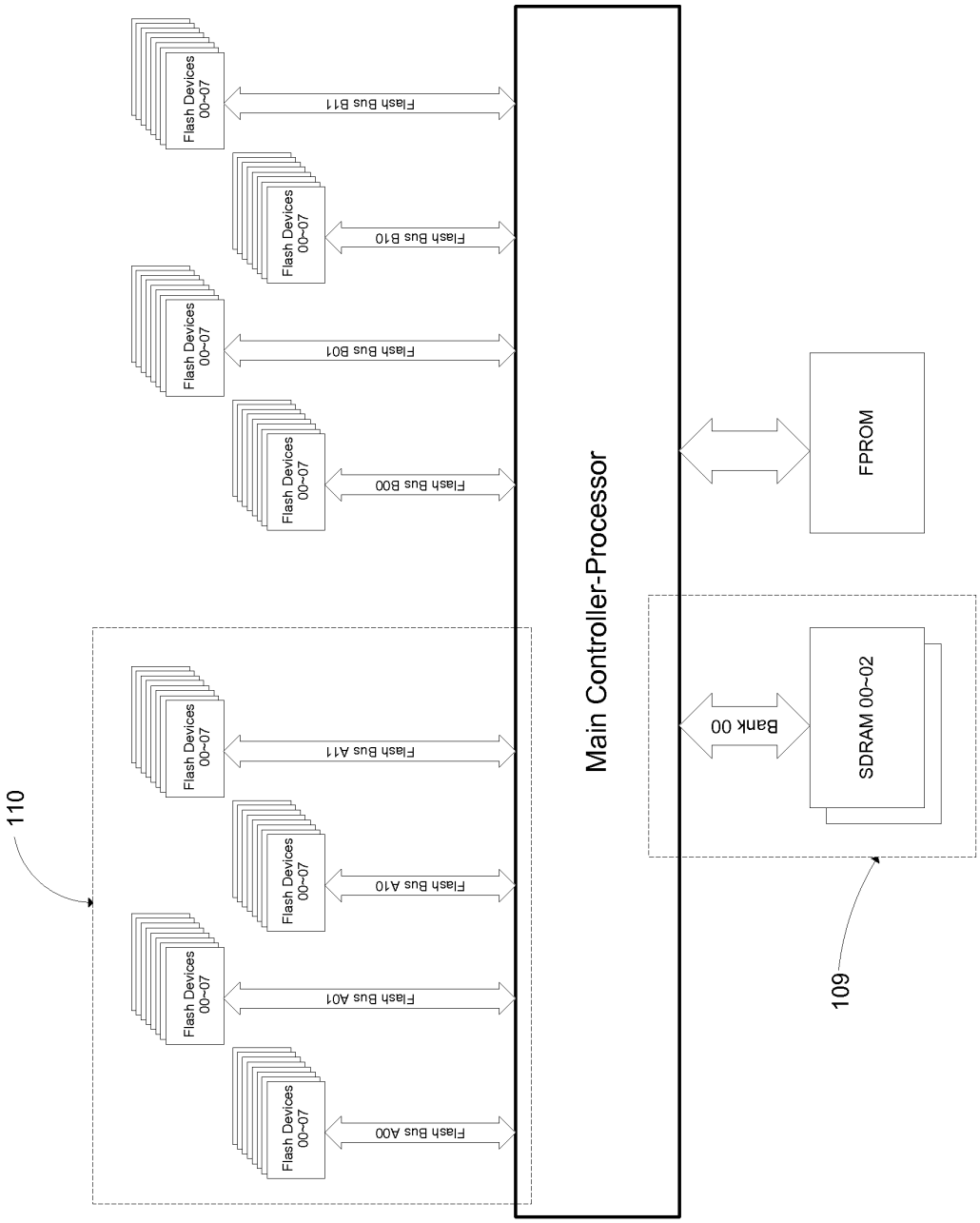

Flash Devices 00~07
Flash Bus B11
Flash Devices 00~07
Flash Bus B10
Flash Devices 00~07
Flash Bus B01
Flash Devices 00~07
Flash Bus B00
Main Controller-Processor
FPROM
Bank 00
SDRAM 00~02
109
110
Flash Devices 00~07
Flash Bus A11
Flash Devices 00~07
Flash Bus A10
Flash Devices 00~07
Flash Bus A01
Flash Devices 00~07
Flash Bus A00

Figure 1b

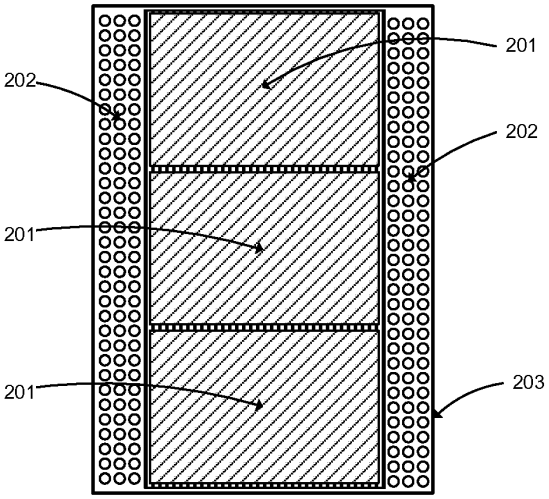


Figure 2a

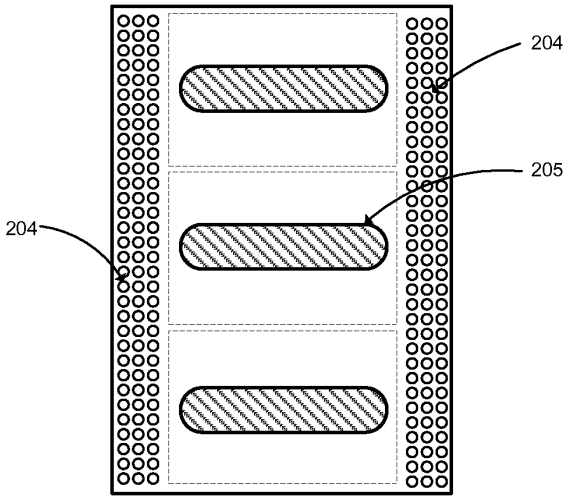


Figure 2b

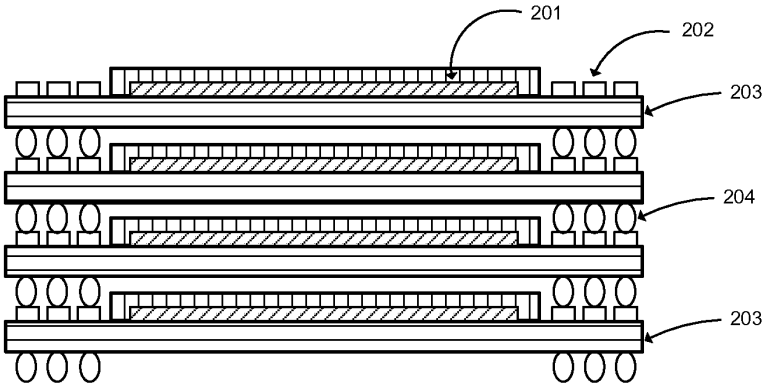


Figure 2c

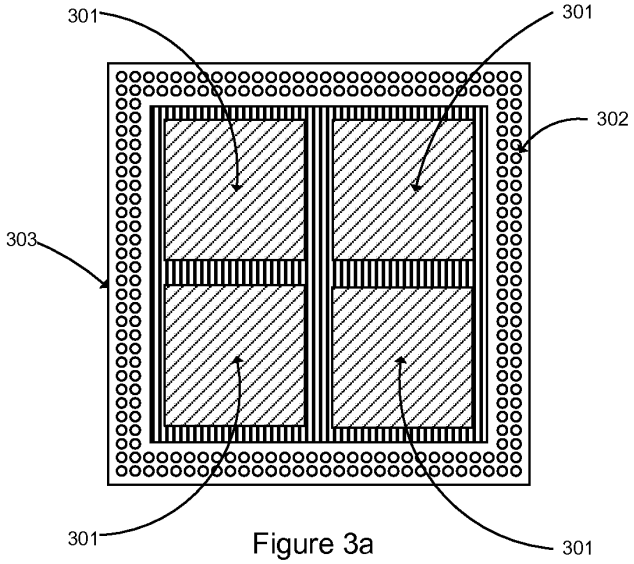


Figure 3a

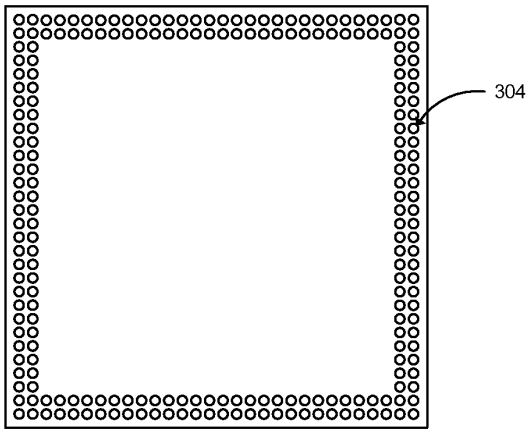


Figure 3b

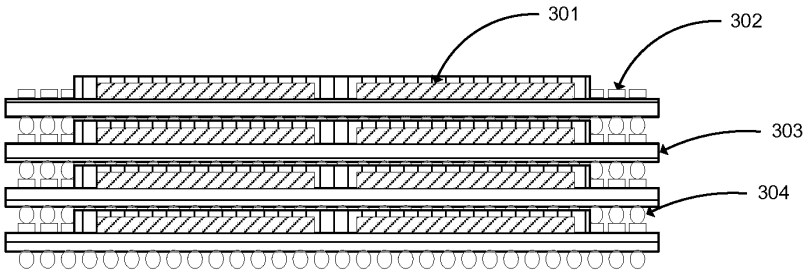


Figure 3c

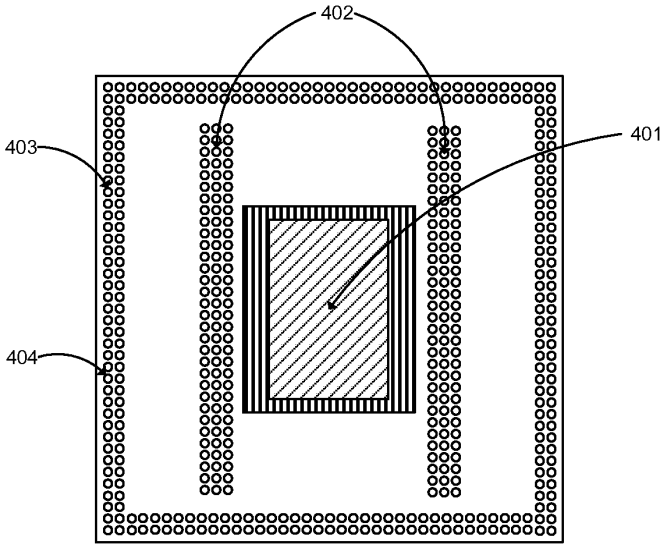


Figure 4a

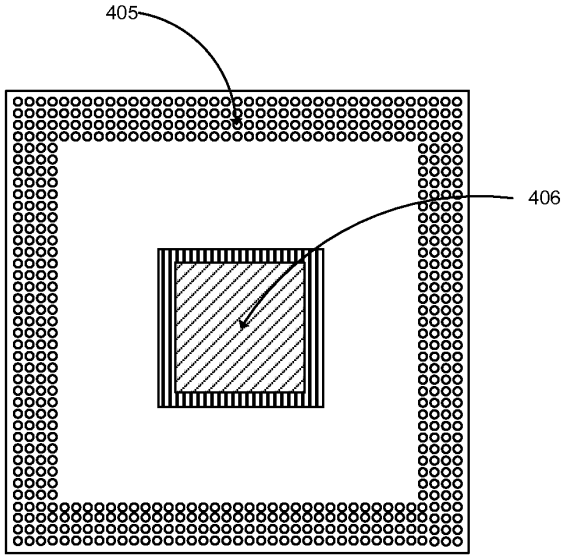


Figure 4b

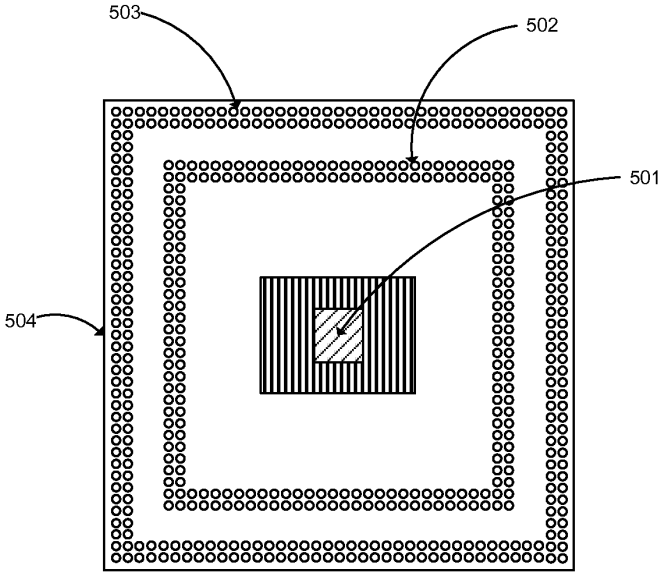


Figure 5a

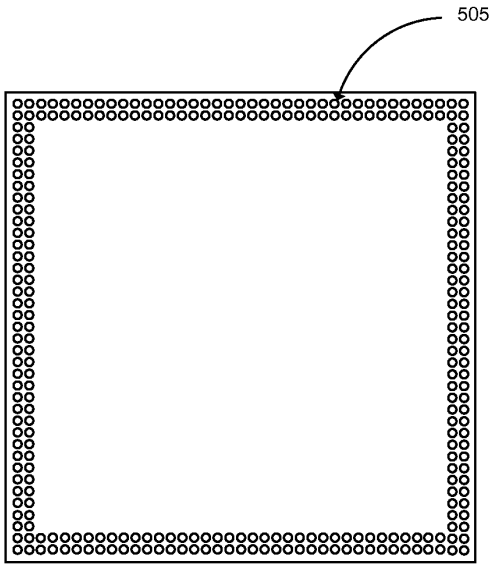


Figure 5b

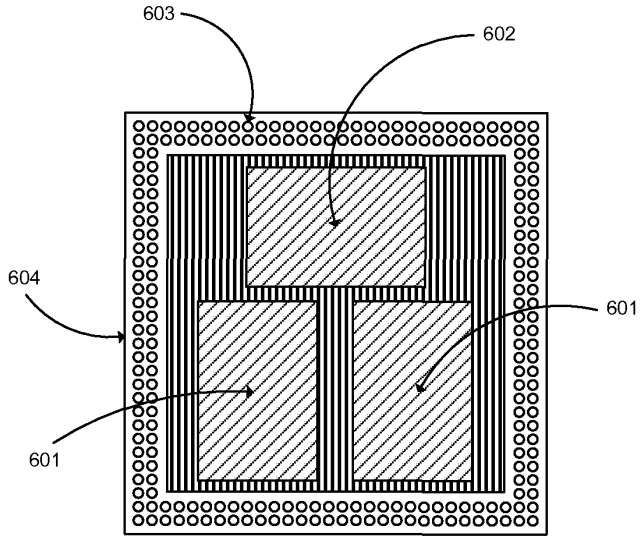


Figure 6a

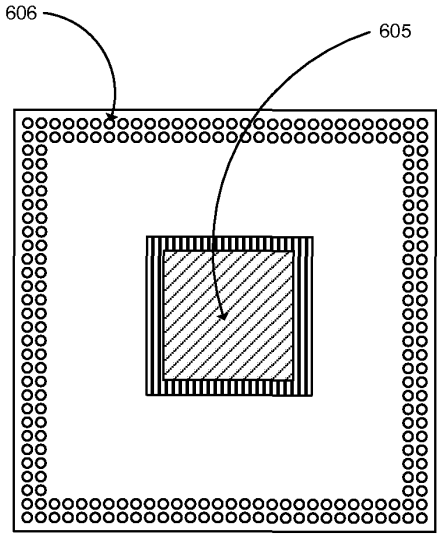


Figure 6b

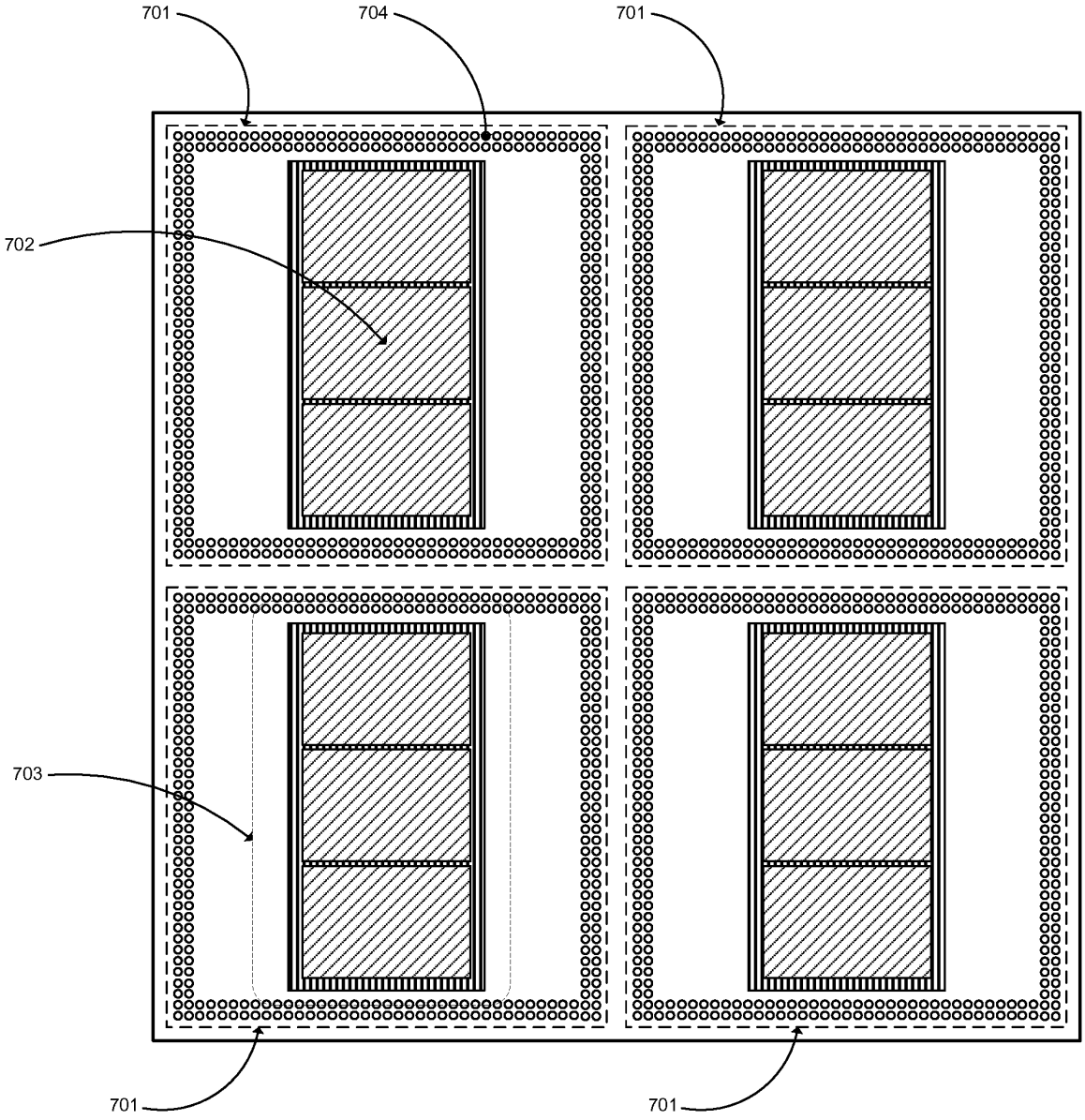


Figure 7a

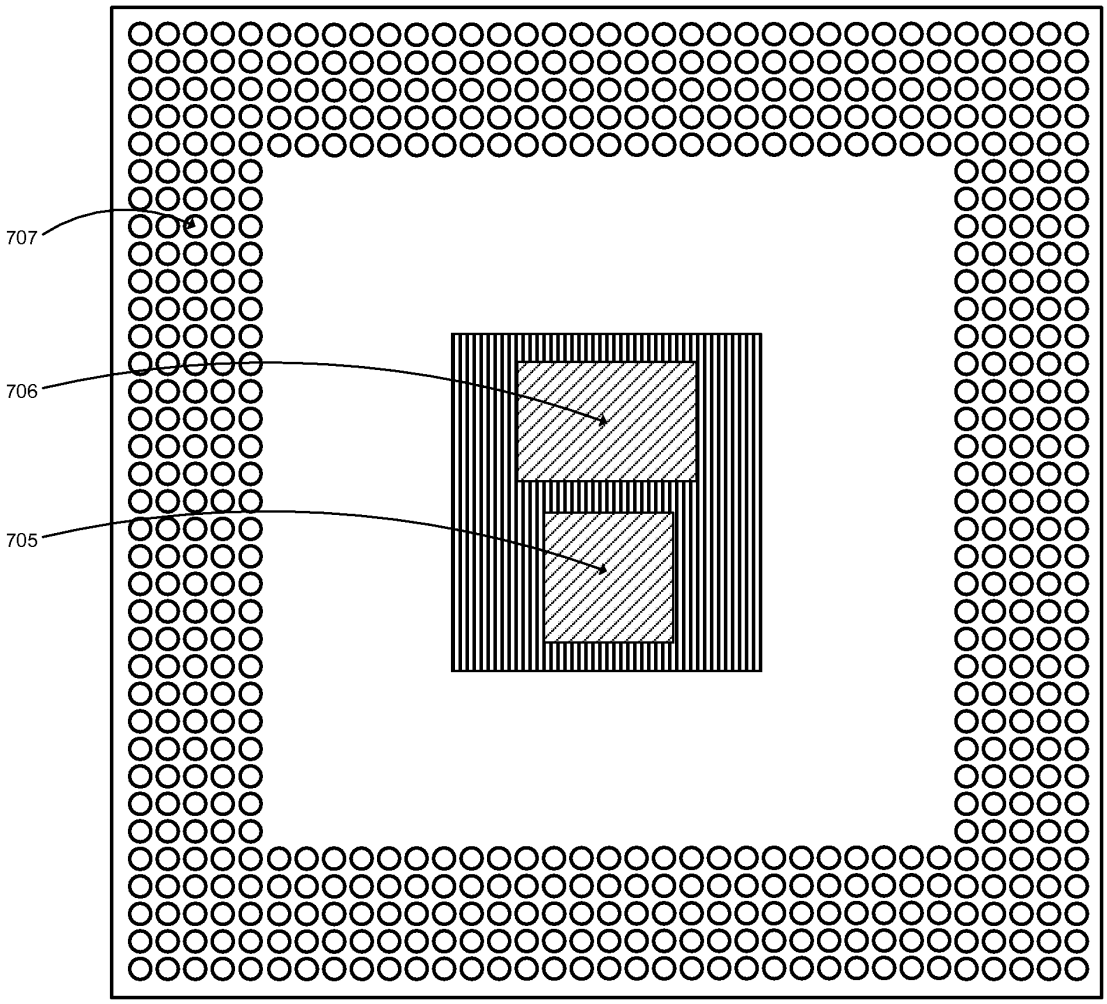


Figure 7b

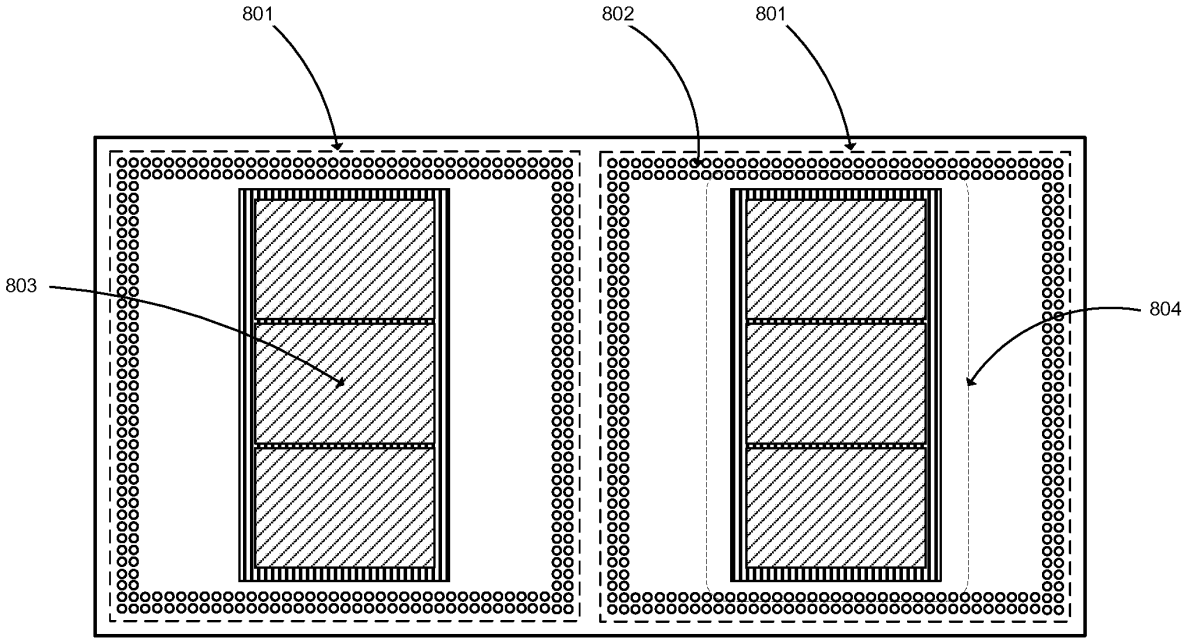


Figure 8a

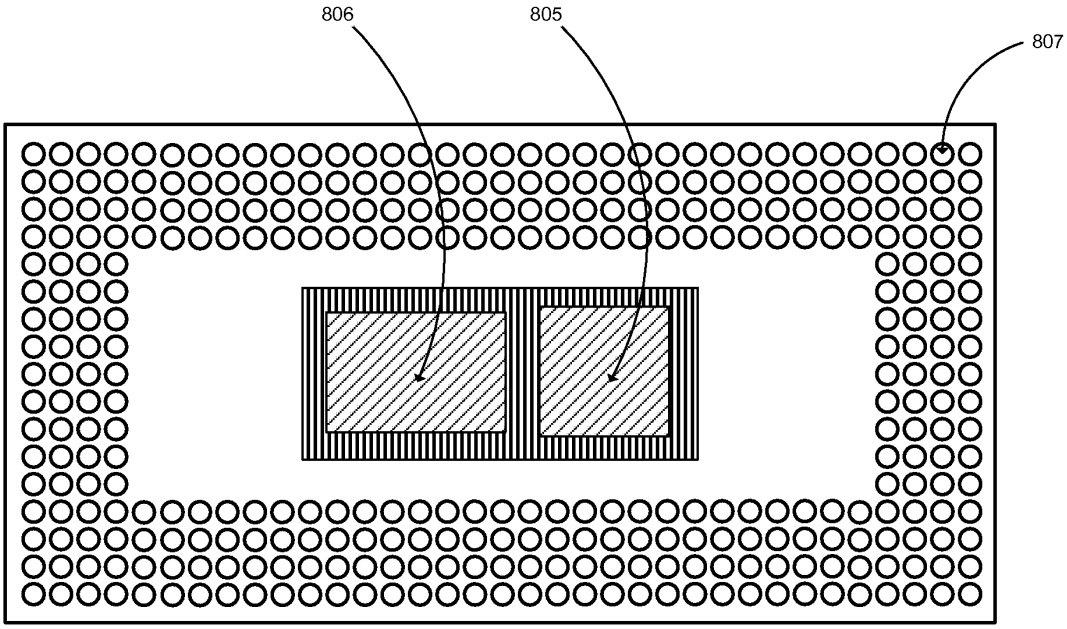


Figure 8b

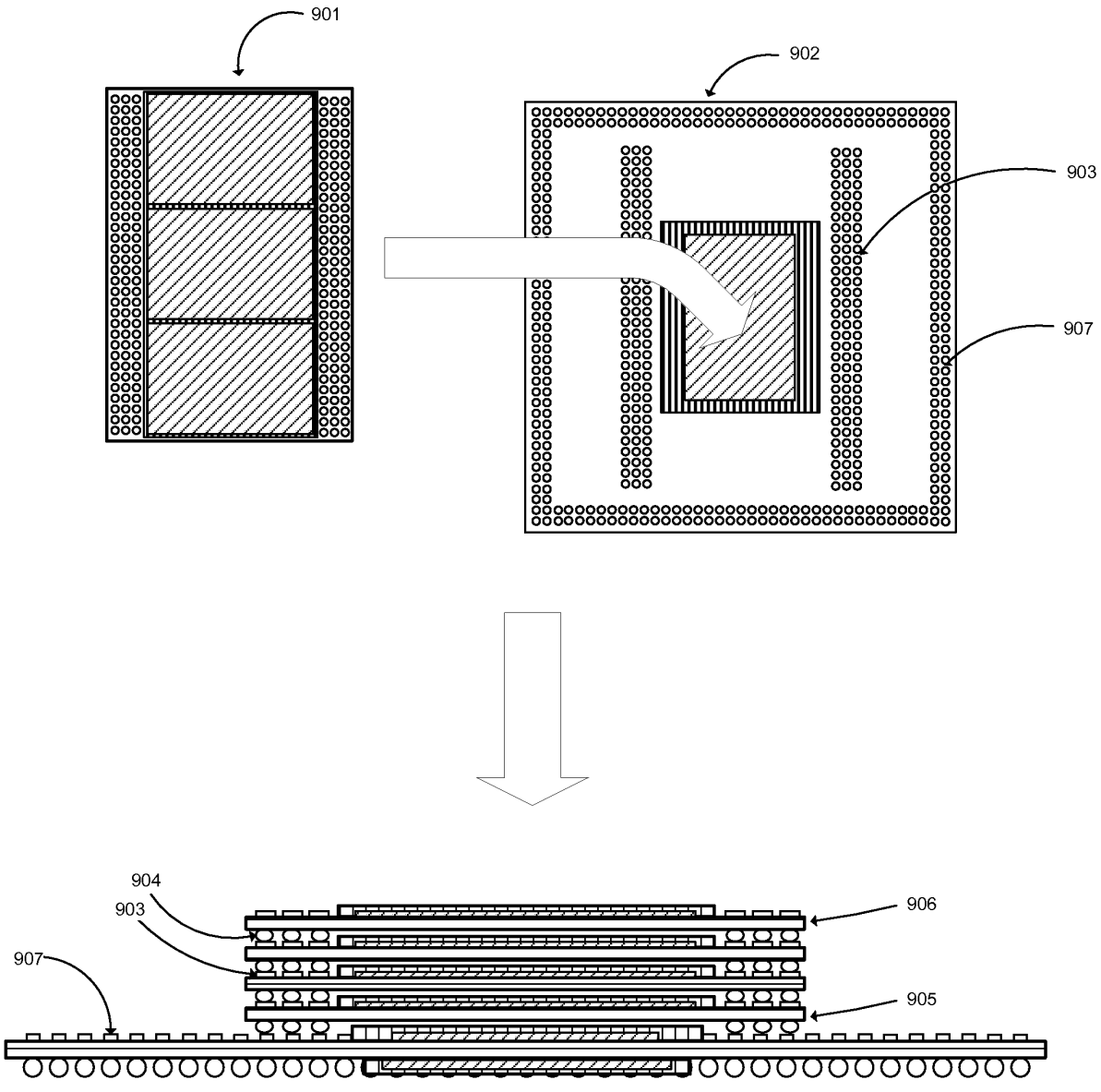


Figure 9

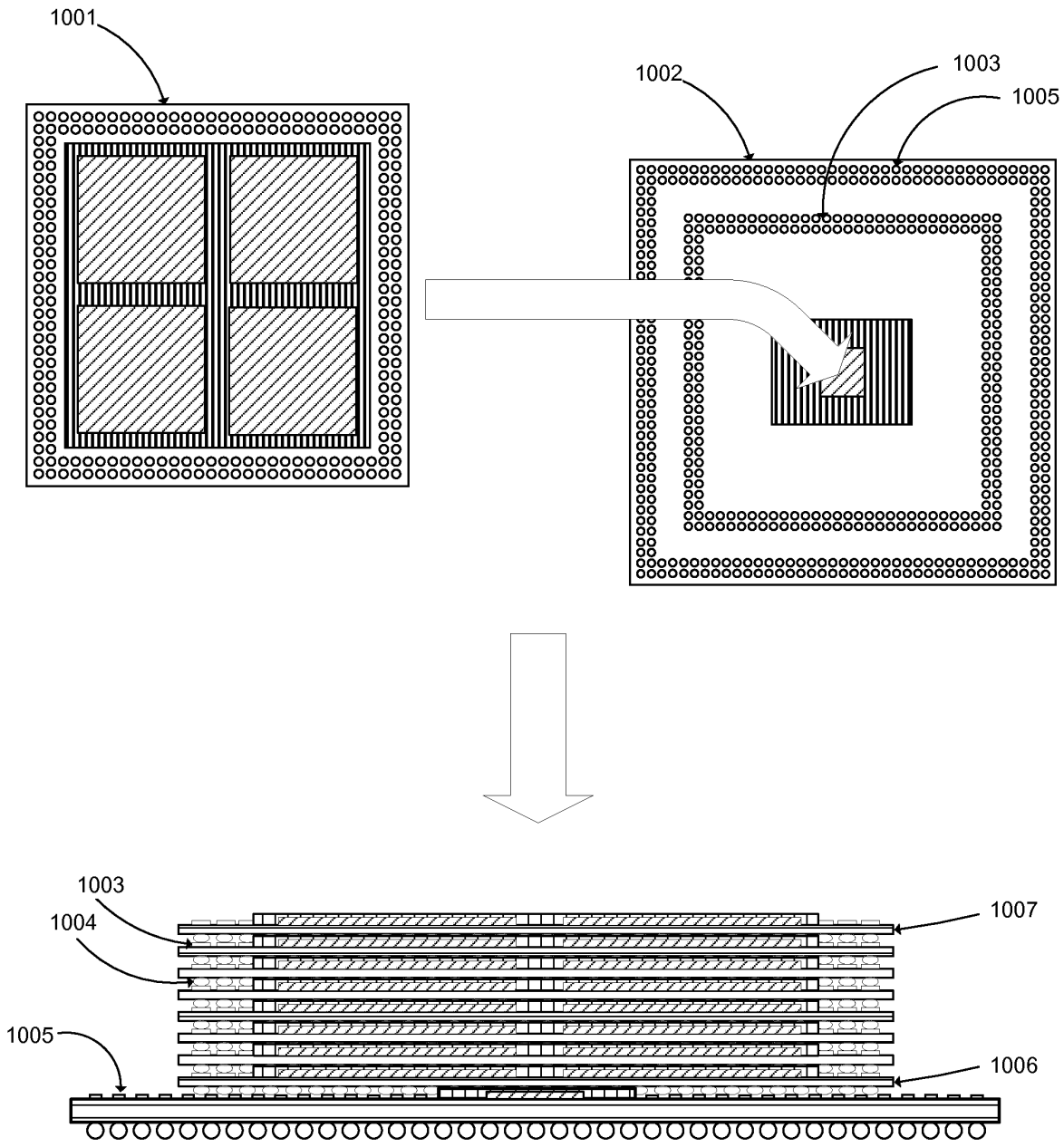


Figure 10

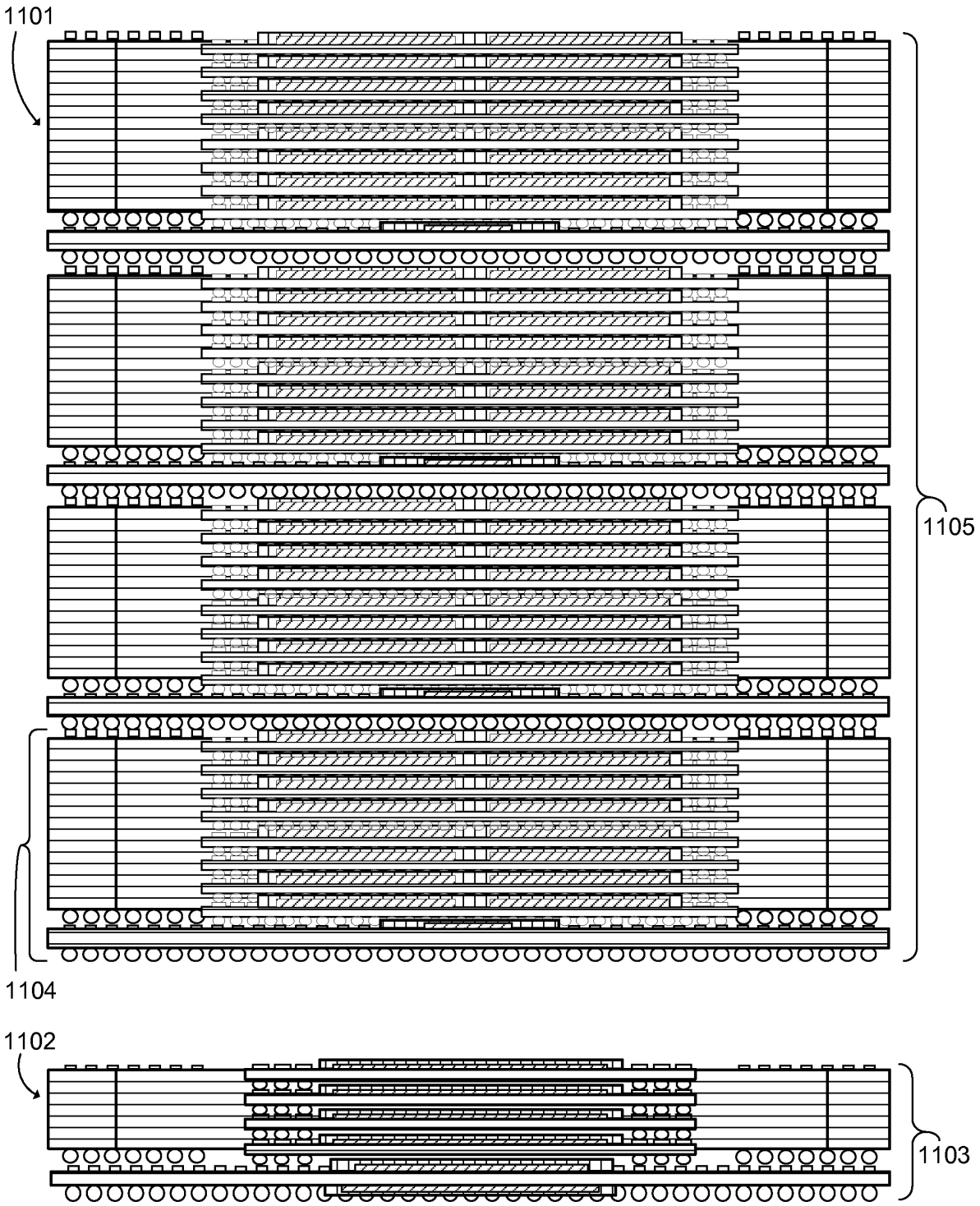


Figure 11

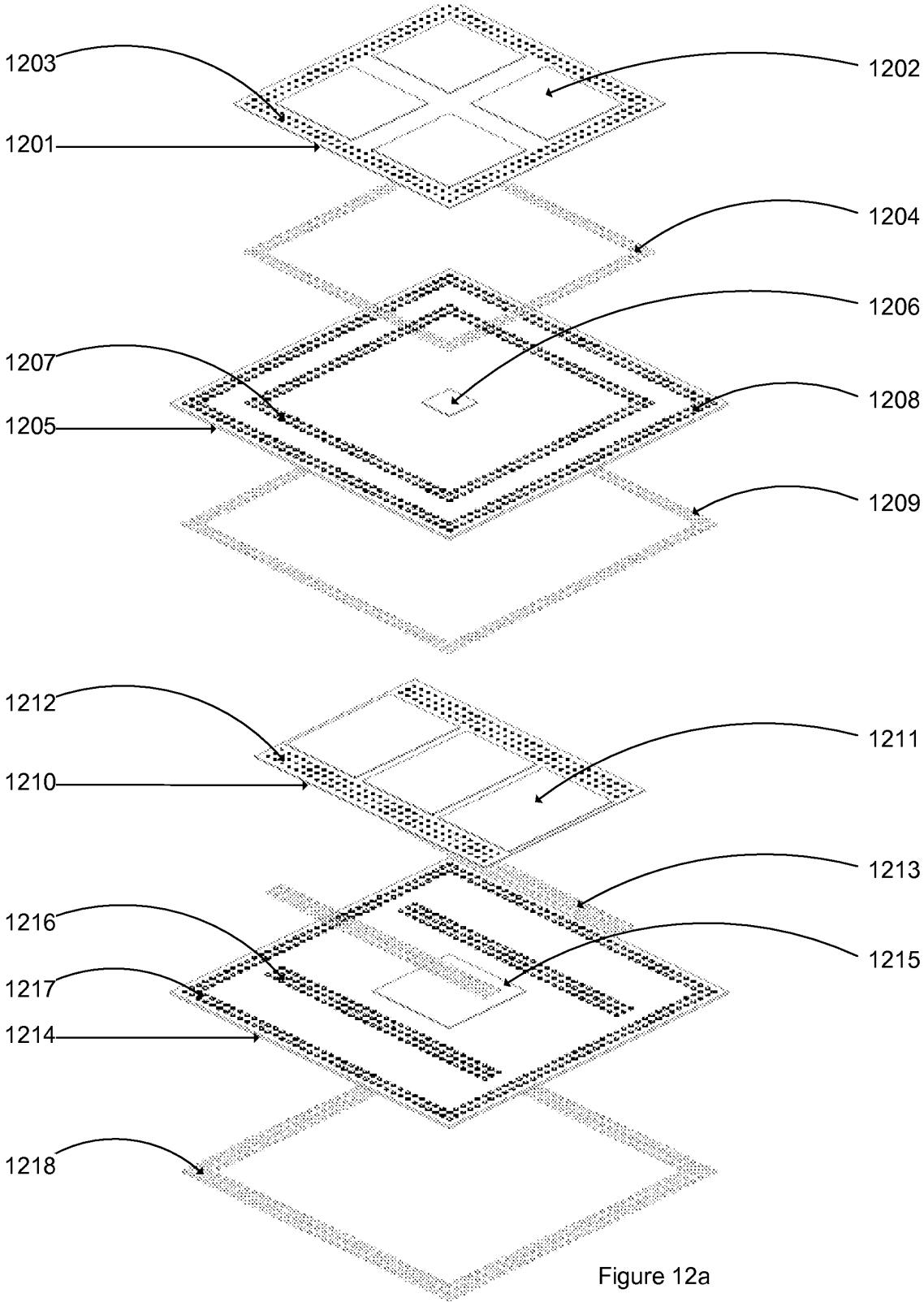

1203
1202
1201
1204
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1214
1218

Figure 12a

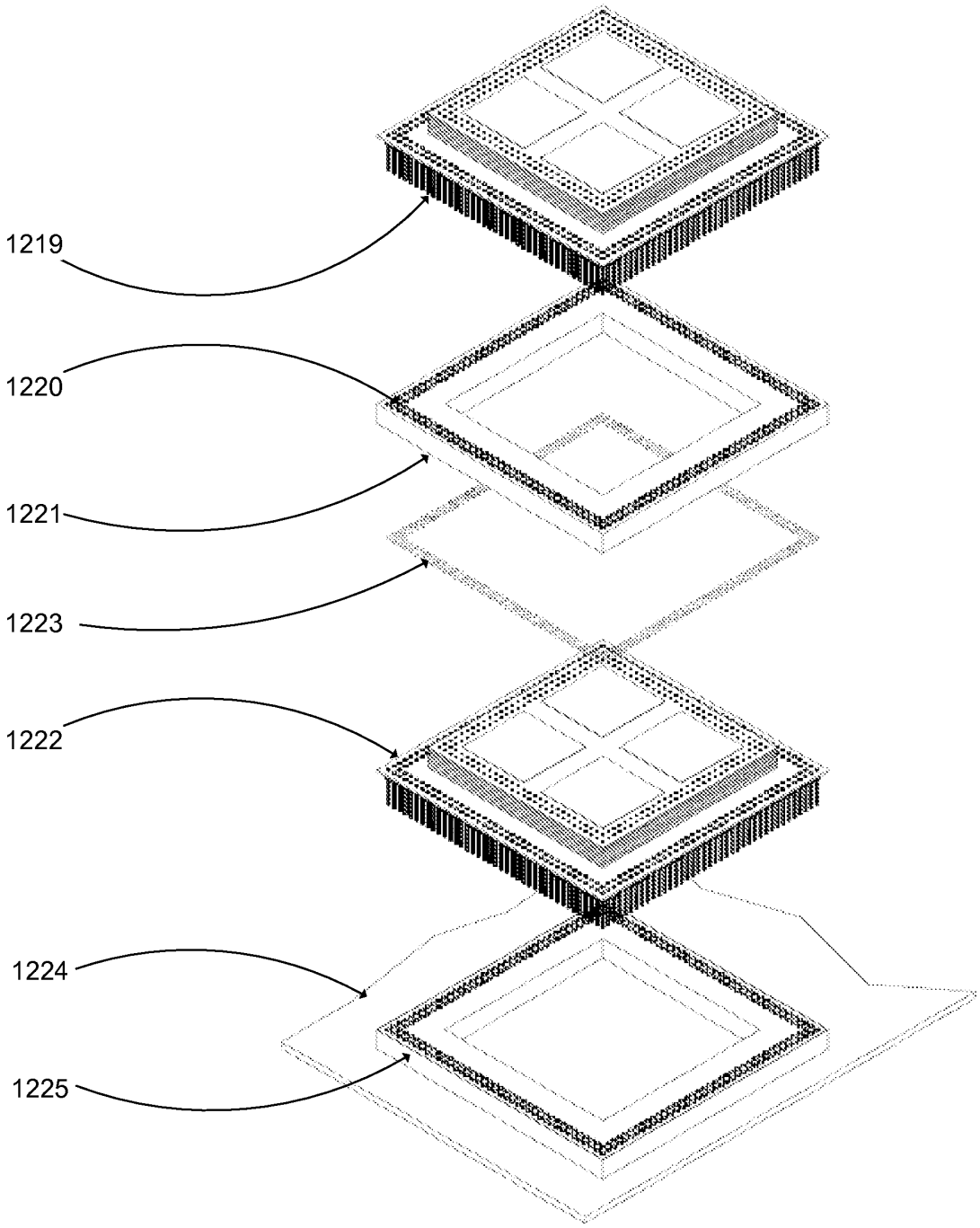


Figure 12b

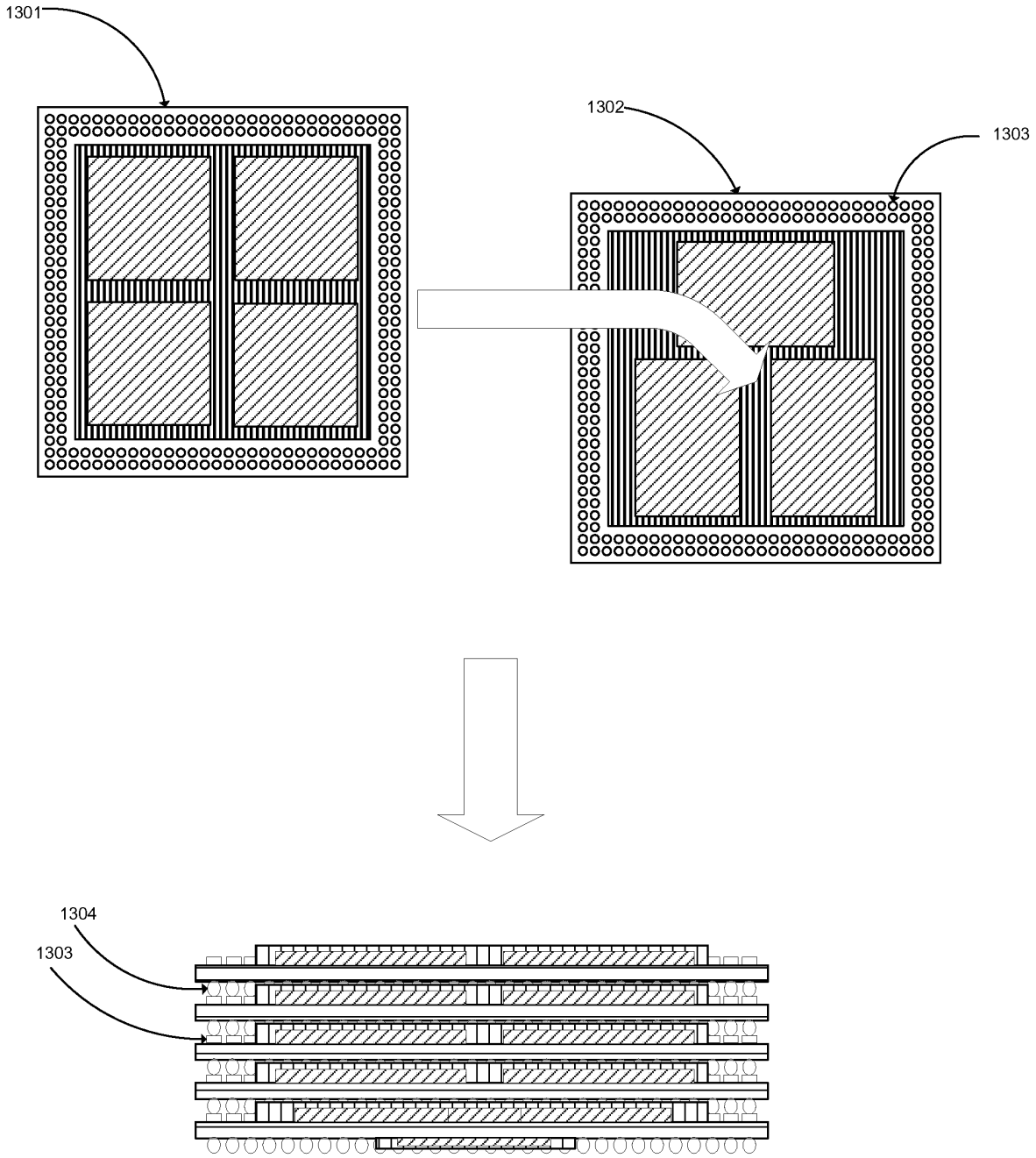


Figure 13

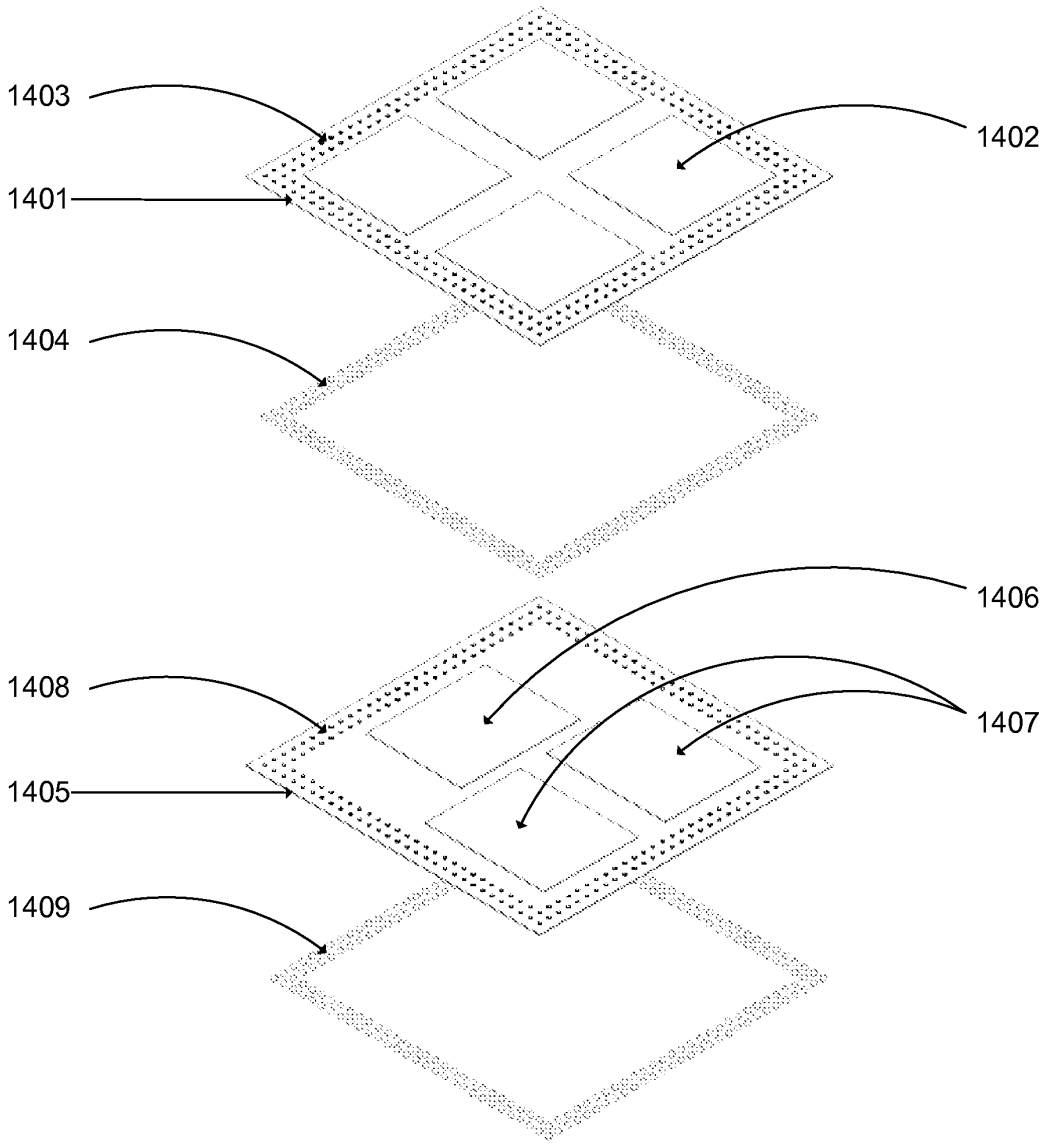


Figure 14

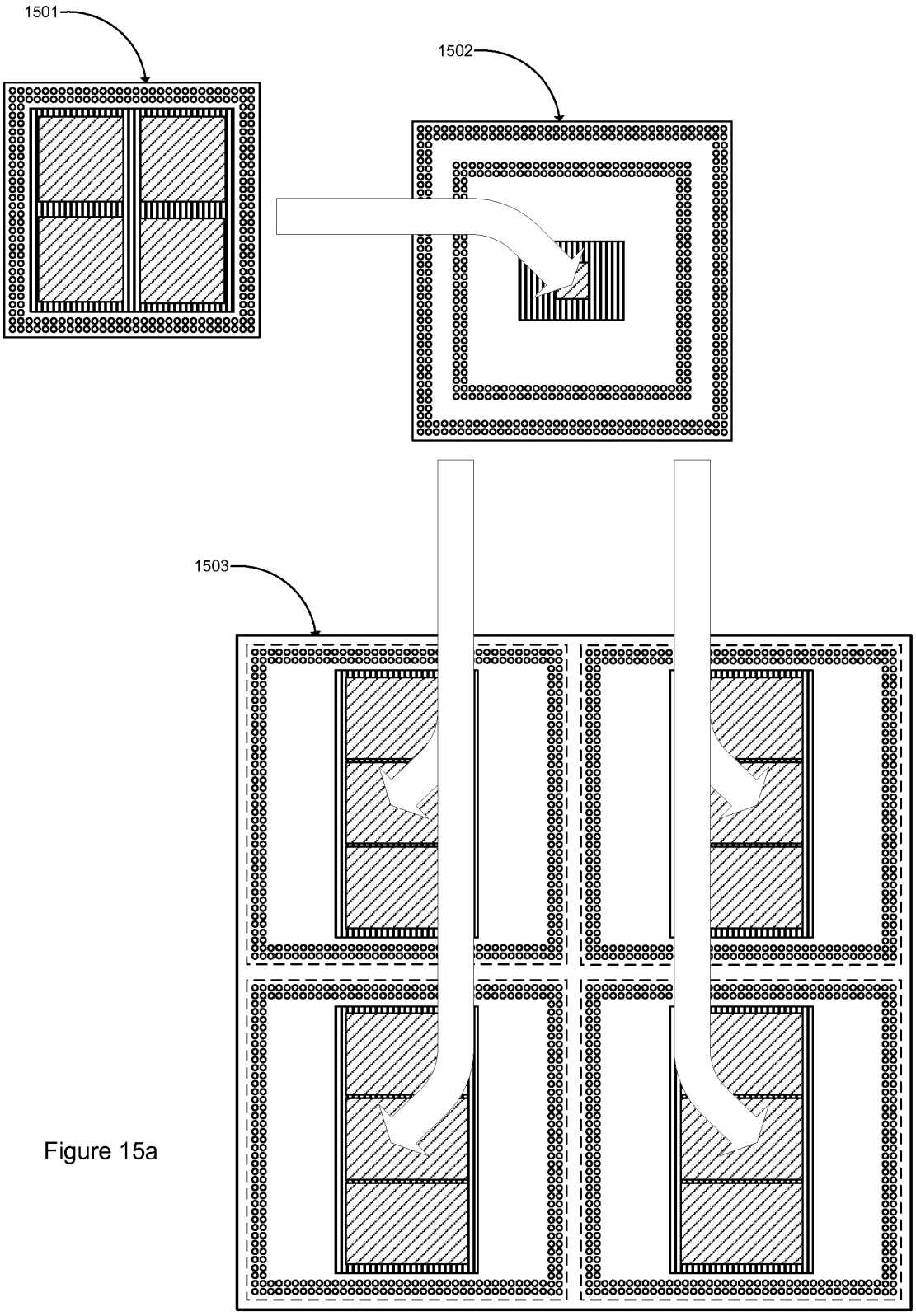


Figure 15a

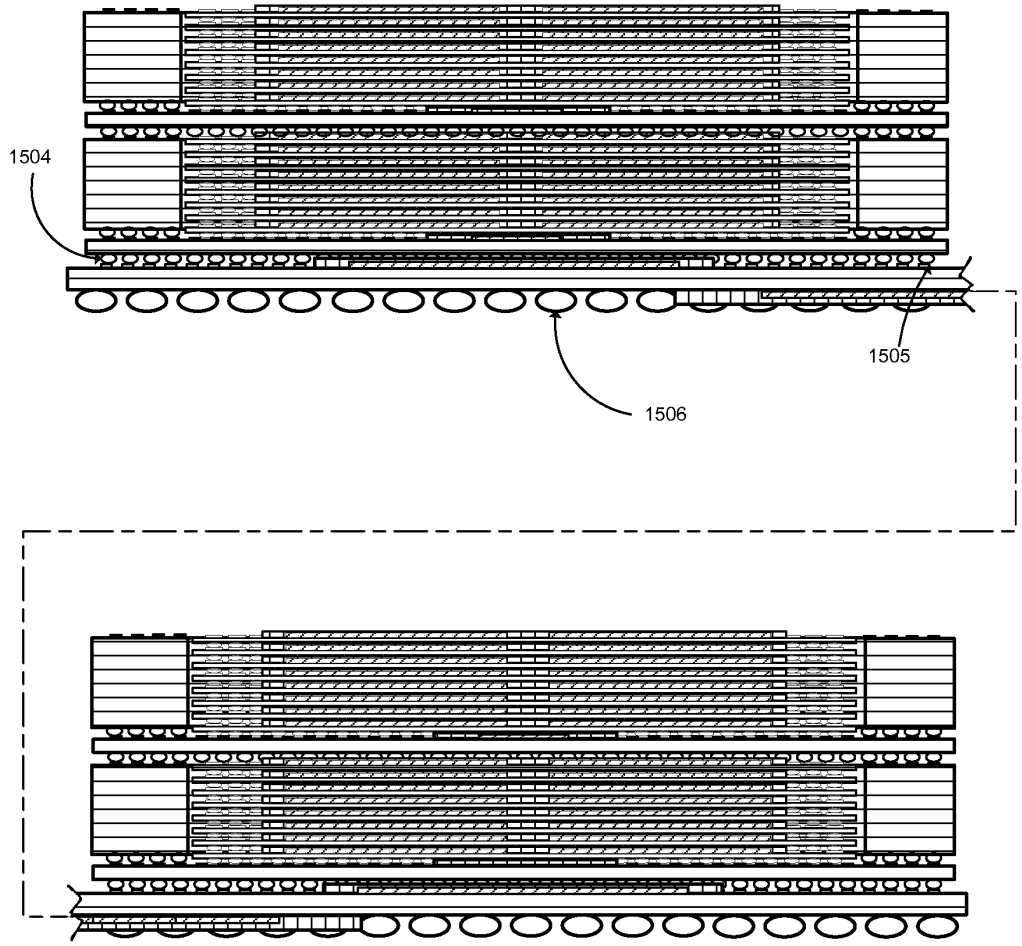


Figure 15b

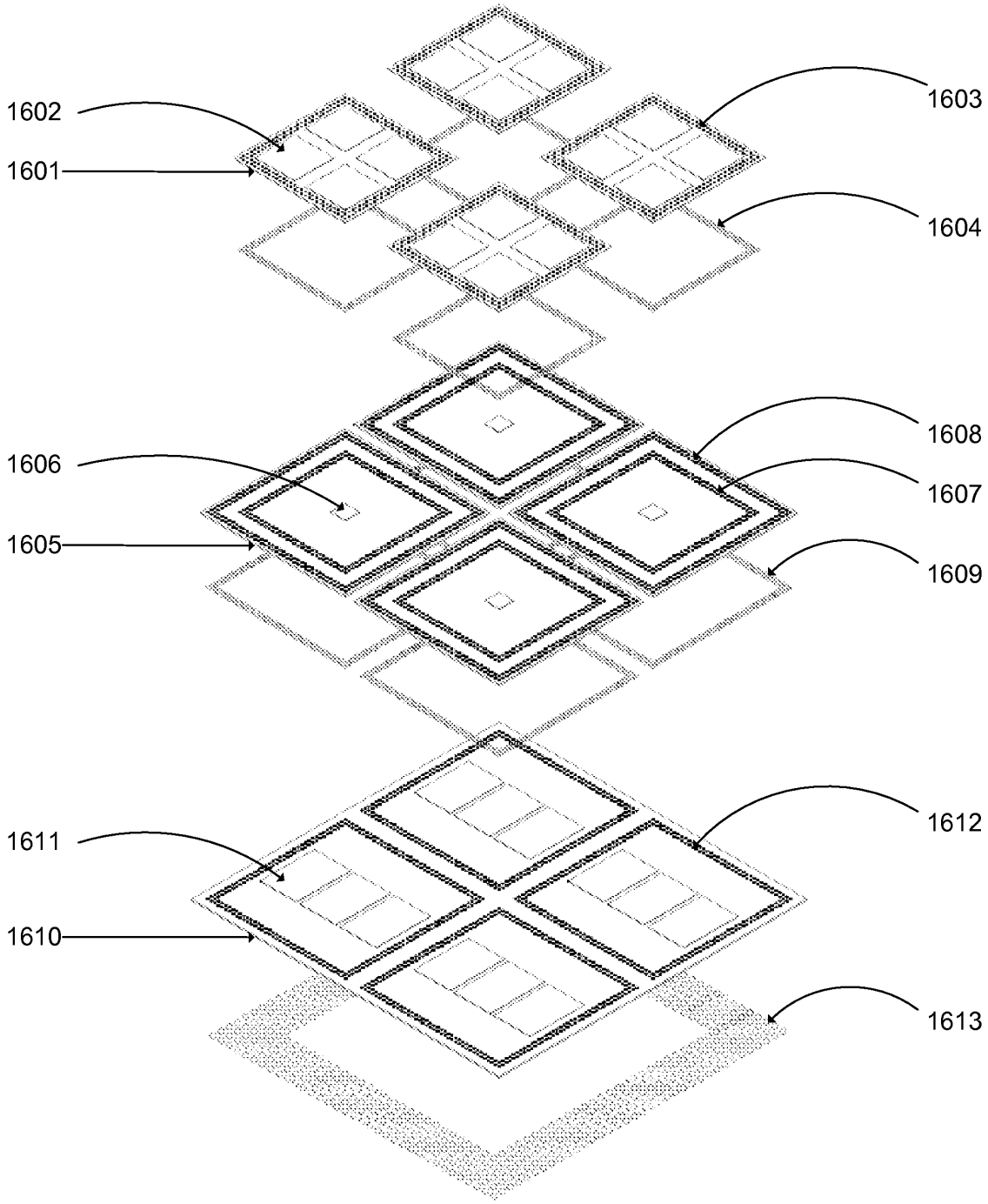

1602
1601
1603
1604
1606
1605
1608
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1609
1611
1610
1612
1613

Figure 16

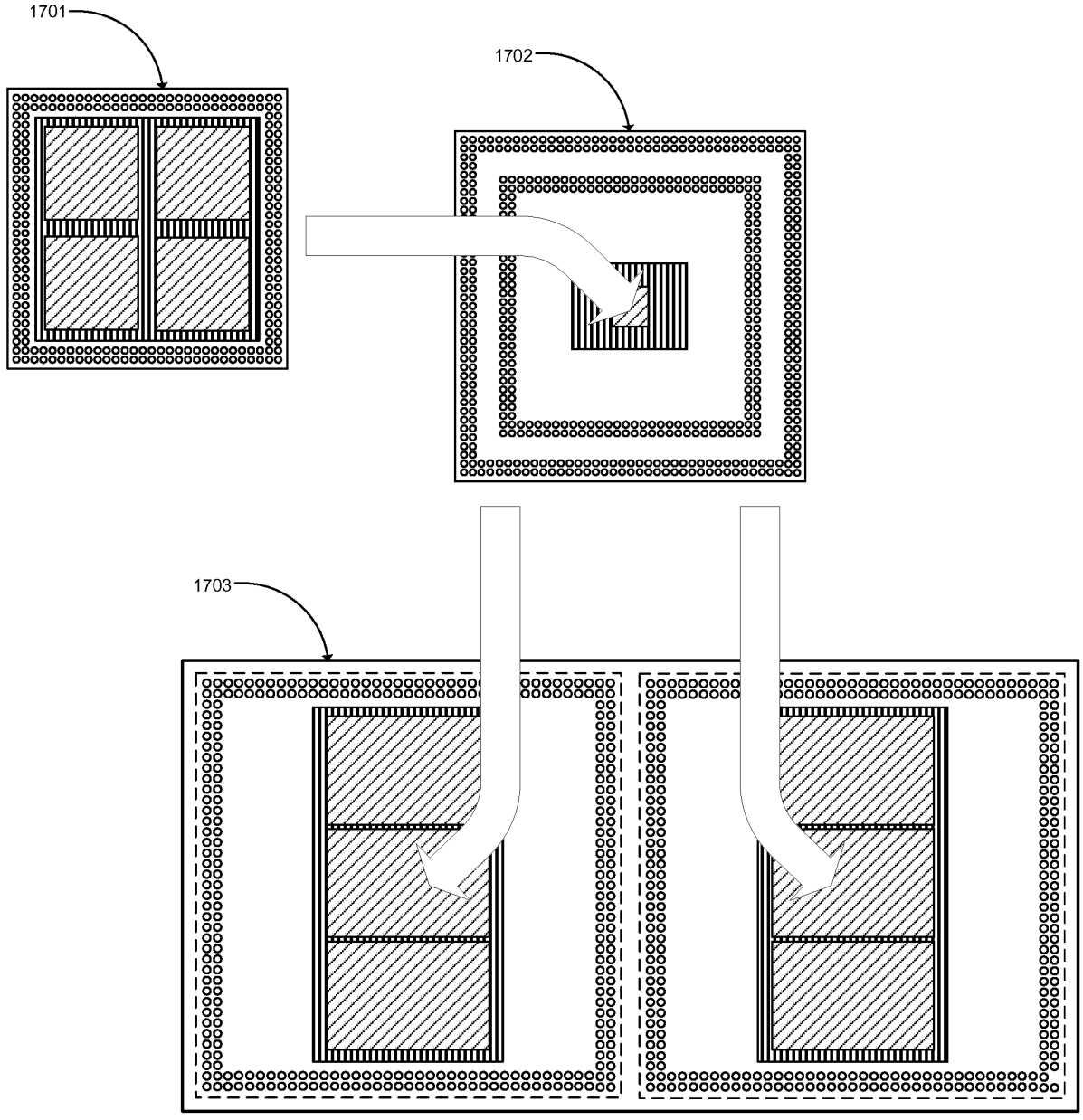


Figure 17a

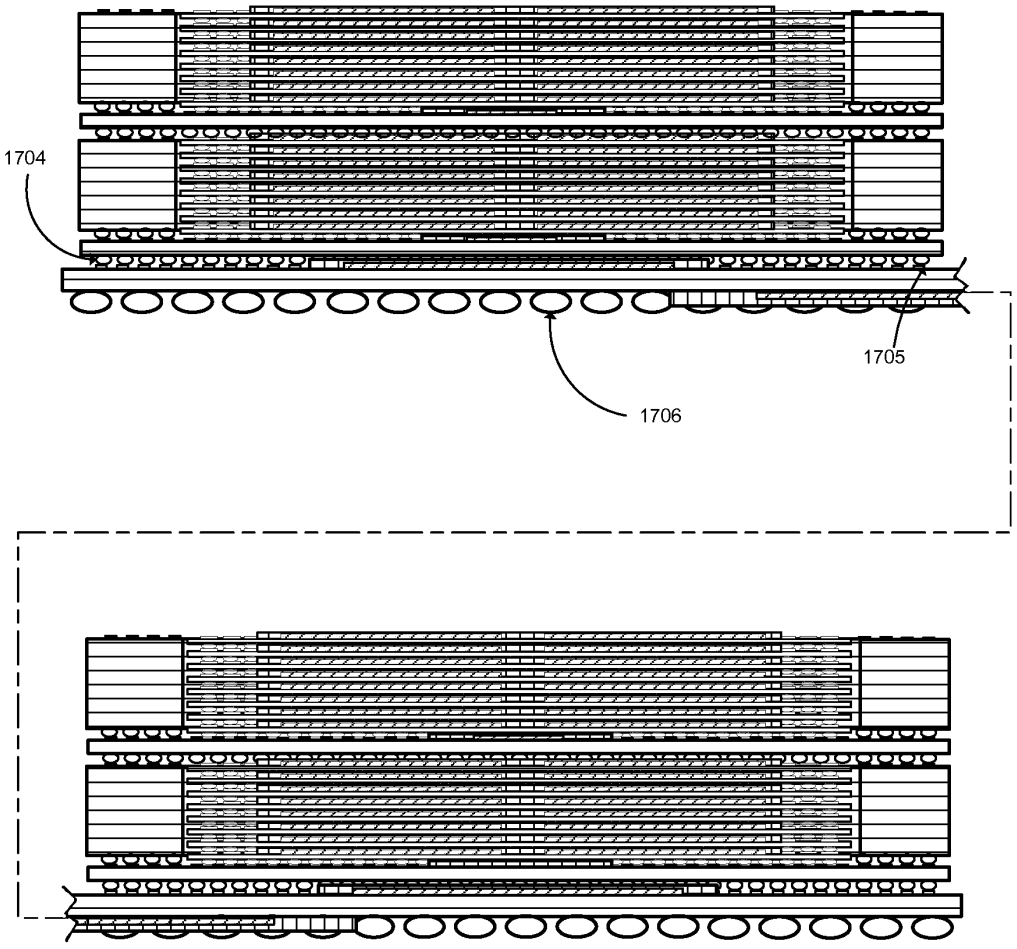


Figure 17b

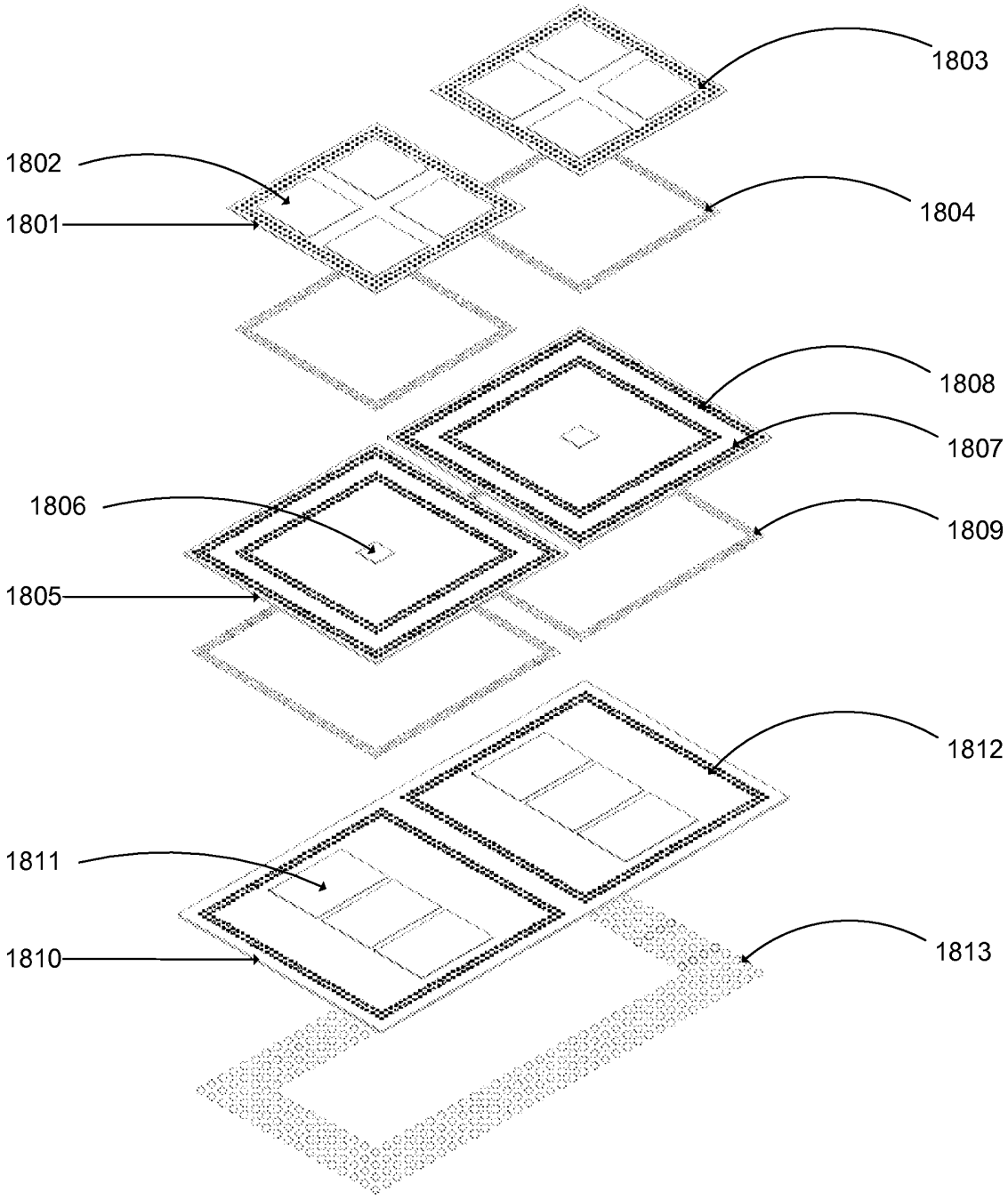

1803
1802
1801
1804
1808
1807
1806
1809
1805
1812
1811
1810
1813

Figure 18

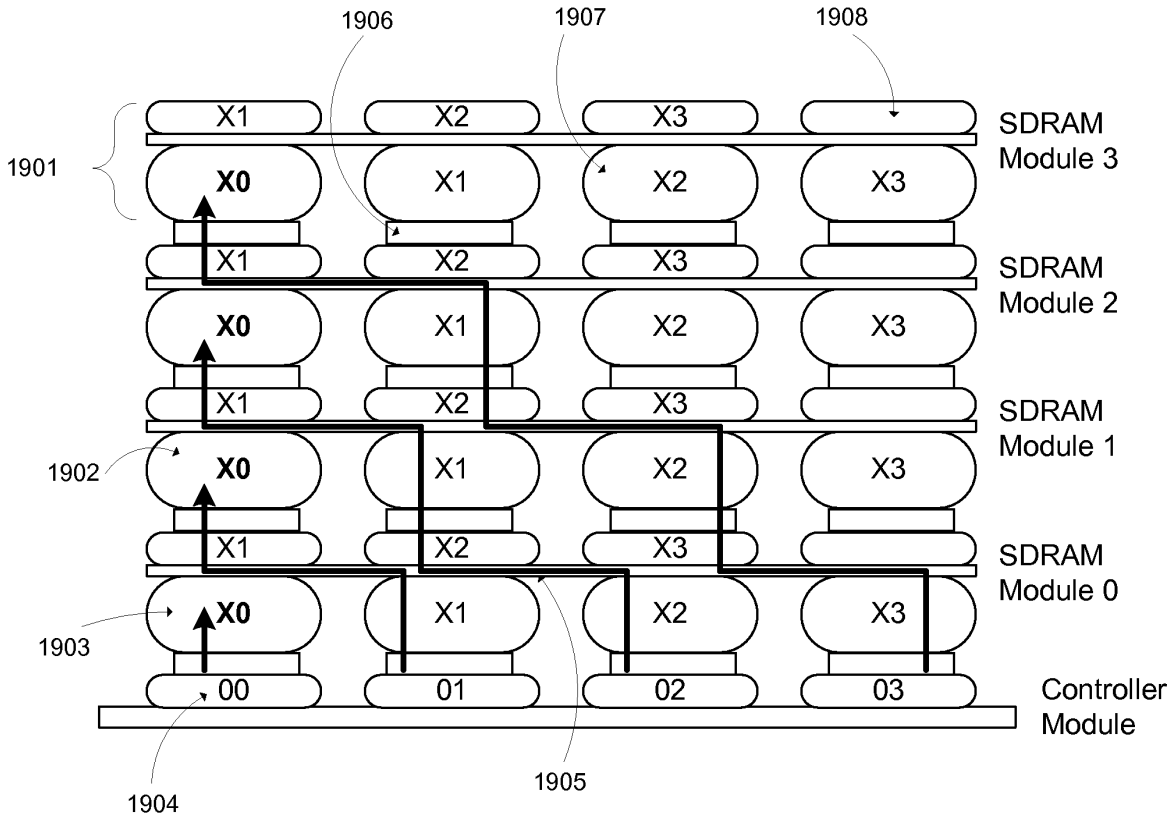

1906
1907
1908
1901
X1
X2
X3
X0
SDRAM Module 3
SDRAM Module 2
SDRAM Module 1
SDRAM Module 0
1902
1903
00
01
02
03
Controller Module
1904
1905

Figure 19

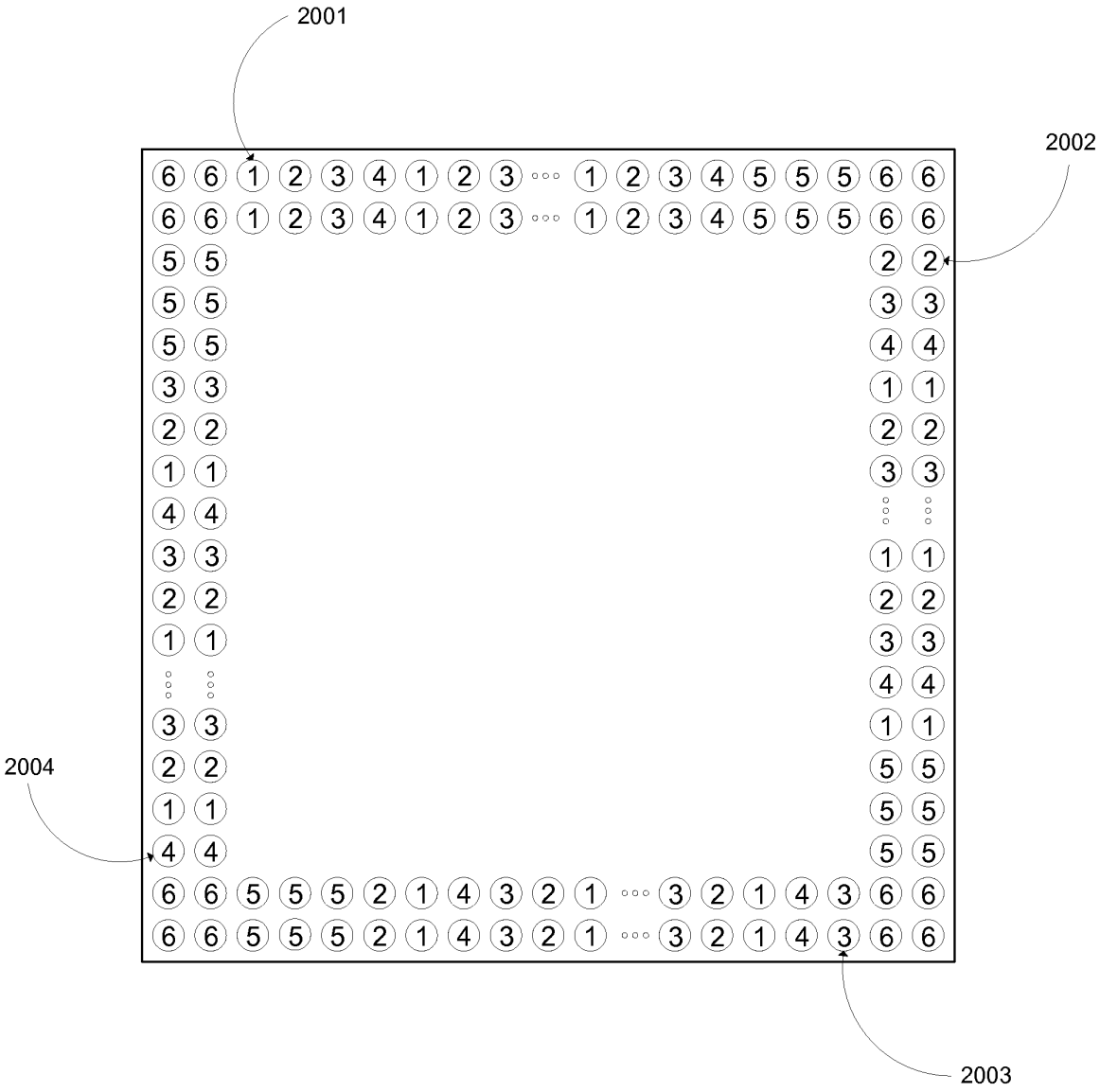


Figure 20a

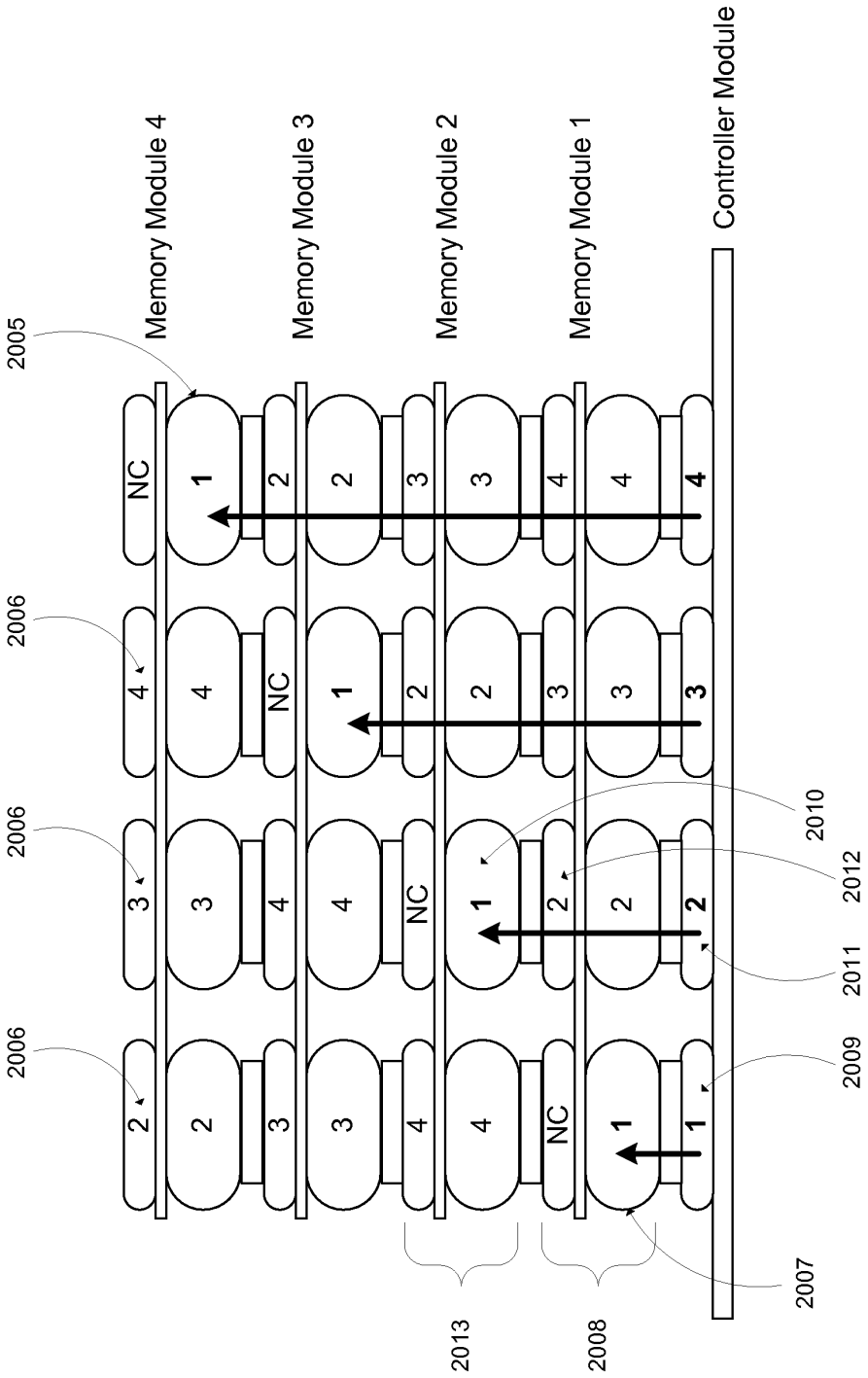

Memory Module 4
Memory Module 3
Memory Module 2
Memory Module 1
Controller Module
2005
2006
2006
2006
2007
2008
2009
2010
2011
2012
2013
NC

Figure 20a

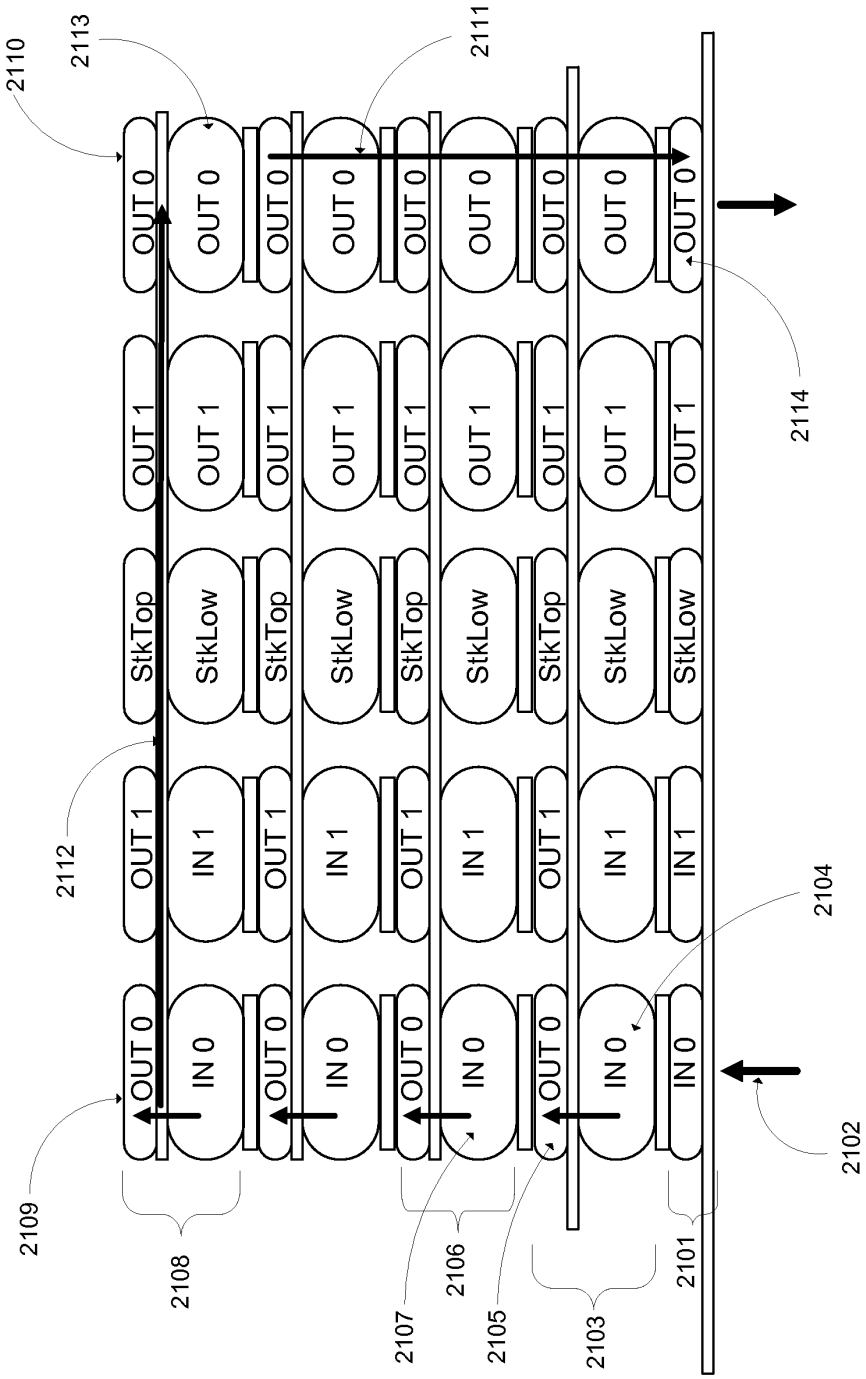
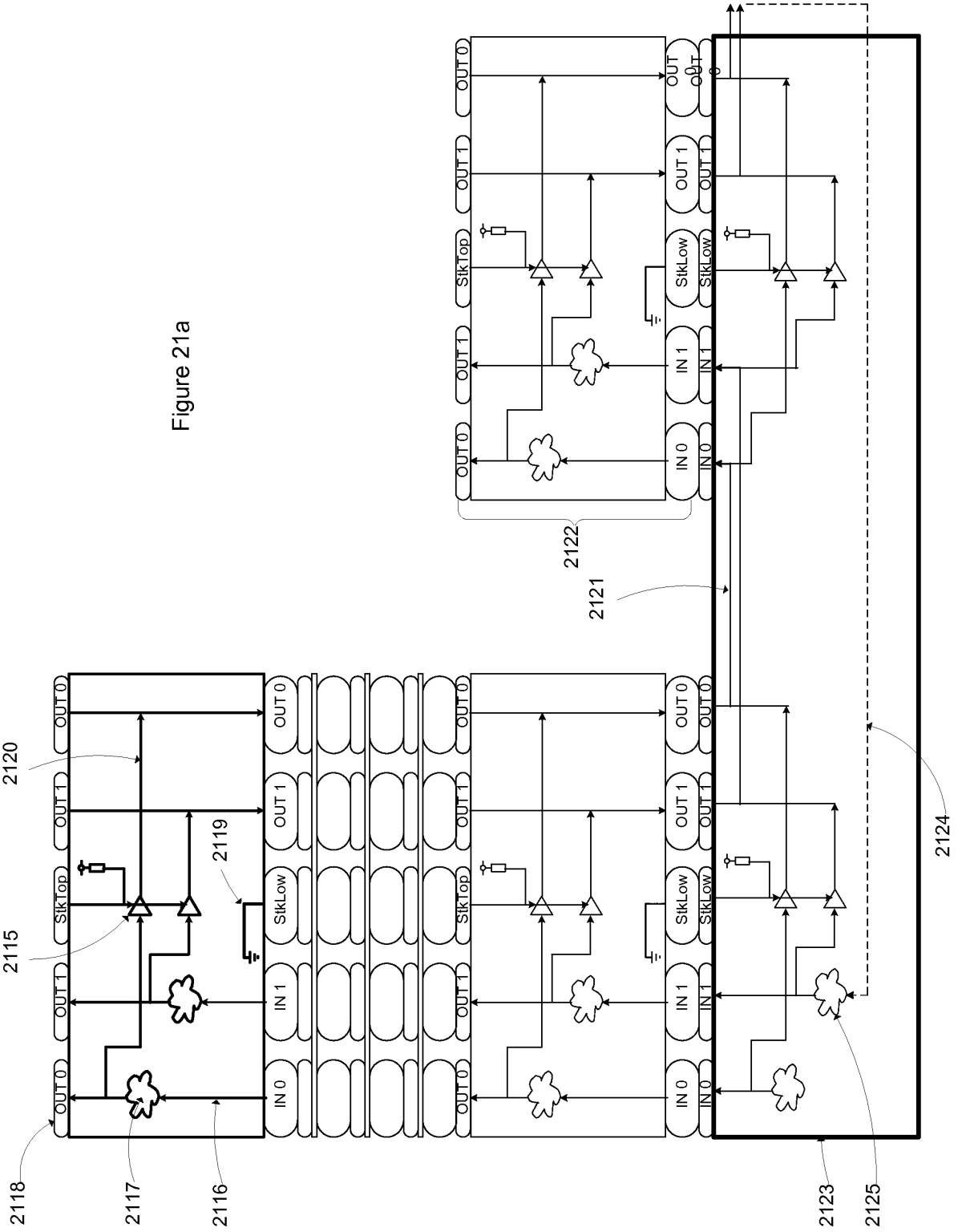

2110
2113
2111
2114
2112
2104
2109
2102
2108
2107
2106
2105
2103
2101
OUT 0
IN 0
OUT 1
IN 1
StkTop
StkLow

Figure 21a

Figure 21a


OUT 0
OUT 1
StkTop
IN 1
IN 0
StkLow
2118
2117
2116
2115
2120
2119
2122
2121
2124
2123
2125

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: BRUCE et al.	Group Art Unit: 2892
Serial No.: 11/322,442	Examiner: ULLAH, Elias
Application Filing Date: 29 Dec 2005	
For: MULTIPLE CHIP MODULE AND PACKAGE AND PACKAGE STACKING METHOD FOR STORAGE DEVICE	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)

Dear Sir:

In conjunction with the Response to the Office Action, submitted on even date herewith, this is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and fee are as follows, indicated below:

Fees Paid:

___	One month (37 CFR 1.17(a)(1))	Fee (small entity: $65.000)	0.00
___	Two months (37 CFR 1.17(a)(2))	Fee (small entity: $245.00)	0.00
X	Three months (37 CFR 1.17(a)(3))	Fee (small entity: $555.00)	**Paid**

Entity Status:

X Applicant claims small entity status. (See 37 CFR 1.27)

Payment Method:

_X_ Payment by credit card through EFS-web is provided.

Authorization to Charge/Credit Fees and Constructive Petition

_X_ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number: 50-4068. Please treat this authorization to charge all required fees under 37 CFR 1.17 as a constructive petition for an extension of time in accordance with 37 CFR 1.136(a)(3).

The undersigned is the attorney of record. Registration #: 40,854

Sincerely,

Signature:	/Stephen R. Uriarte/	Date:	27 June 2008
Name:	Stephen R. Uriarte	Telephone:	408.244.2164x111

Uriarte Law
2021 The Alameda, Suite 225
San Jose, CA 95126
Tel: 408.244.2164 ext. 111
Fax: 408.716.2651
Email: mail@uriartelaw.com

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: BRUCE et al.	)	Group Art Unit: 2892
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Serial No.: 11/322,442	)	Examiner: ULLAH, Elias
	)	
Application Filing Date: 29 Dec 2005	)	
	)	
For: MULTIPLE CHIP MODULE AND PACKAGE AND PACKAGE STACKING METHOD FOR STORAGE DEVICE	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

EXCESS CLAIM FEE PAYMENT AND DEPOSIT ACCOUNT AUTHORIZATION

Dear Sir:

Authorization of Payment of Excess Claim Fees, If Required

It is believed that any additional fee required for new claims 27-31 has been previously paid since claims 1 through 13 were previously cancelled/withdrawn by the Applicants in a previously filed Response to Restriction requirement. In the event of any deficiency or overpayment involving excess claim fees or otherwise, the credit card account of the undersigned should be charged or credited in accordance to the instructions selected during filing of the attached Response and Amendment to Office Action filed on even date herewith via EFS-Web; or by using the following deposit account:

Account Number: 50-4068
Account Name: Uriarte Law

Respectfully submitted,
On behalf of the Applicants

Dated: 13 February 2009

/Stephen R. Uriarte/
Stephen R. Uriarte, Reg. No. 40,854

The Uriarte Law Firm
2021 The Alameda, Suite 225
San Jose, CA 95126
Tel: 408.244.2164 x111
Fax: 408.716.2651
Email: mail@uriartelaw.com

Electronic Patent Application Fee Transmittal

Application Number:	11322442
Filing Date:	29-Dec-2005
Title of Invention:	Multiple chip module and package stacking method for storage devices
First Named Inventor/Applicant Name:	Rey Bruce
Filer:	Stephen Radcliff Uriarte
Attorney Docket Number:	6005.011

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 3 months with $0 paid	2253	1	555	555

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**555**

Electronic Acknowledgement Receipt	
EFS ID:	4795792
Application Number:	11322442
International Application Number:	
Confirmation Number:	5045
Title of Invention:	Multiple chip module and package stacking method for storage devices
First Named Inventor/Applicant Name:	Rey Bruce
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.011
Receipt Date:	13-FEB-2009
Filing Date:	29-DEC-2005
Time Stamp:	20:48:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$555
RAM confirmation Number	4321
Deposit Account	504068
Authorized User	URIARTE,STEPHEN R.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		6005_011_1stRsp2OA_20090213B.pdf	175877 e6c062da928c0ecaf1bcdf947fde67c5bbfc91f1	yes	25
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	15	
	Applicant Arguments/Remarks Made in an Amendment		16	25	
Warnings:					
Information:					
2	Specification	6005_011_SubstitueSpecMarked_20090213.pdf	189782 7bd50e8f0c7932370e77aa0fd138d6181d7fd67f	no	26
Warnings:					
Information:					
3	Specification	6005_011_SubstitueSpecCLEAN_20090213.pdf	185457 5c2710cf5cfa261d6382d012673ac7bd884f51aa	no	25
Warnings:					
Information:					
4	Drawings-only black and white line drawings	6005_011_FIGS1_11_rplcmnt_20090213.pdf	510087 9c602775ce3caf49e701b7cb45d18e2064505bb3	no	13
Warnings:					
Information:					
5	Drawings-only black and white line drawings	6005_011_FIGS12a_17b_rplcmnt_20090213.pdf	608961 d62e9cea6a423862ea4d341a5854068c34175af9	no	9
Warnings:					
Information:					
6	Drawings-only black and white line drawings	6005_011_FIGS18_21b_rplcmnt_20090130.pdf	141127 703df7f1222026935032 8c7bba1e4736e7f92792	no	6
Warnings:					
Information:					
7	Extension of Time	6005_011_PetitionExtTime_20090213emb.pdf	29322 b31629b356ce7c09c183488ffbe430dc9eb7a125	no	2
Warnings:					
Information:					

8	Refund Request	6005_011_Excess_Claims_20090213_wOff.pdf	75884 17432dc2f0f7318656c5521b438e5eef31bb8f8c	no	1
Warnings:					
Information:					
9	Fee Worksheet (PTO-06)	fee-info.pdf	29793 6cc62d133a58ffd44c7d60bfb4719ca2023c01e7	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1946290		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

DocCode - SCORE

SCORE Placeholder Sheet for IFW Content

Application Number: 11322442 Document Date: 2/13/2009

The presence of this form in the IFW record indicates that the following document type was received in paper and is scanned and stored in the SCORE database.

- Design Drawings

The original paper documents are in the physical artifact folder. The original documents are scanned using a higher quality capture process and stored in SCORE. A copy of these documents are scanned in IFW using the standard quality scanning process. Defects visible in both IFW and SCORE are indicative of defects in the original paper documents.

To access the documents in the SCORE database, refer to instructions developed by SIRA.

At the time of document entry (noted above):

- Examiners may access SCORE content via the eDAN interface.
- Other USPTO employees can bookmark the current SCORE URL (http://es/ScoreAccessWeb/).
- External customers may access SCORE content via the Public and Private PAIR interfaces.

Form Revision Date: October 12, 2006

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/322,442	12/29/2005	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☒		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
	02/13/2009	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	* 18	Minus	** 26	= 0	X $26 =	0	OR	X $ =	
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $110 =	0	OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE	

		(Column 1)		(Column 2)	(Column 3)					
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/CHRISTINE MOLLISH/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/322,442	12/29/2005	Rey Bruce	6005.011	5045

64180 7590 08/13/2008

URIARTE LAW
257 RODONOVAN DRIVE
SANTA CLARA, CA 95051

EXAMINER	
ULLAH, ELIAS	
ART UNIT	PAPER NUMBER
2892	
MAIL DATE	DELIVERY MODE
08/13/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/322,442	BRUCE ET AL.	
	Examiner	Art Unit	
	ELIAS ULLAH	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-26* is/are pending in the application.

4a) Of the above claim(s) *17-19,24 -26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-16,20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/24/2008, 3/18/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to an election restriction filed on 6/27/2008.

Election/Restrictions

1. Applicant's election without traverse of claims 14-26 in the reply filed on 6/27/2008 is acknowledged. Claims 17-19 and 24-26 are withdrawn for further consideration since claims 17-19 and 24-26 are dependent on cancelled claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 14-15 and 18-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Kyougoku et al. (Kyougoku, US 5,995,379).

With regard to claim 14, Kyougoku shows a stacked module (Fig. 5) comprising a plurality of modules (100-1002) each comprising: one or more active port (B1-B3) for carrying one or more active signal (col.6, lines 45-50); and one more passive port (L1-L6) for passing through the one or more active signals (col.6, lines 45-50).

With regard to claim 15, Kyougoku shows the one or more passive port forms a ladder like routing path (L1-L6).

With regard to claim 16, Kyougoku shows the plurality of module 1000-1002 is rotated before being stacked and the one or more passive port L1-L6 forms a rotational routing path (Fig. 5).

With regard to claim 18, Kyougoku shows one or more control port (1000) for enabling a routing path (L4) extending the first daisy chain connection 5 within an end module 1002 (Fig. 5).

With regard to claims 20-21, Kyougoku shows one or more of the plurality of modules is a main board (Col. 6, lines 55-57) and one more vertically stacked modules 1000-1002 in (Fig. 5) is connected to the main board (Col. 6, lines 55-57).

With regard to claim 22, Kyougoku shows each of the plurality of modules (1000-1002) comprises a first side (B1-B3 area) and a second side (B1'-B3' area) (Fig. 5) wherein the one or more active port (B3) is connected to one or more active ball 5 on the first side of one or more corresponding module 1000; wherein the one or more passive port L1 is connected to one or more passive ball (not labeled, ball connected to B2) on the first side and one or more passive pad B1' on the second side of one or more corresponding module 1000; wherein each of the one or more passive ball (not labeled, ball connected to B2) and each of the one or more passive pad B1' connected to a same passive port are located between a pre-determined distance to each other in a repeating pattern, the pre-determined distance equaling a multiple of a periodic distance of the repeating pattern (Fig. 5); wherein one or more active port of a base module 1000 is routed to a same location on one or more modules 1001-1002 through

the ladder like routing path L1-L6; and wherein the ladder like routing path comprises one or more passive ball and one or more passive pad (Fig. 5).

With regard to claim 23, Kyougoku shows each of the plurality of modules (1000-1002) comprises a first side (B1-B3 area) and a second side (B1'-B3' area); wherein the one or more active port (B3) is connected to one or more active ball 5 on the first side of one or more corresponding module 1000; wherein the one or more passive port L1-L6 is connected to one or more passive ball (not labeled, ball connected to B2) on the first side and one or more passive pad B1' on the second side of one or more corresponding module 1000; wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port L1 are located opposite each other in a repeating pattern (L1-L6); wherein one or more active port of a base module 1000 is routed to a same location on one or more modules through the rotational routing path (L1-L6); and wherein the rotational routing path comprises one or more passive ball and one or more passive pad (Fig. 5).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes

that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kyougoku.

With regard to claim 16, Kyougoku shows the plurality of module 1000-1002 is rotated before being stacked and the one or more passive port L1-L6 forms a rotational routing path (Fig. 5).

With the recitations of the plurality of module is rotated before being stacked is statement of product-by-process. Claims are limited by and defined by the process; determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985), MPEP 2113.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ELIAS ULLAH whose telephone number is

(571)272-1415. The examiner can normally be reached on weekdays, between 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Elias Ullah/
Examiner, Art Unit 2892

/Thao X Le/
Supervisory Patent Examiner, Art Unit 2892

Notice of References Cited	Application/Control No. 11/322,442	Applicant(s)/Patent Under Reexamination BRUCE ET AL.	
	Examiner ELIAS ULLAH	Art Unit 2892	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,995,379	11-1999	Kyougoku et al.	361/803
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11322442	BRUCE ET AL.
	Examiner	Art Unit
	ELIAS ULLAH	2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/23/2008	08/07/2008							
	1	÷	-							
	2	÷	-							
	3	÷	-							
	4	÷	-							
	5	÷	-							
	6	÷	-							
	7	÷	-							
	8	÷	-							
	9	÷	-							
	10	÷	-							
	11	÷	-							
	12	÷	-							
	13	÷	-							
	14	÷	✓							
	15	÷	✓							
	16	÷	✓							
	17	÷	N							
	18	÷	N							
	19	÷	N							
	20	÷	✓							
	21	÷	✓							
	22	÷	✓							
	23	÷	✓							
	24	÷	N							
	25	÷	N							
	26	÷	N							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11322442	BRUCE ET AL.
	Examiner	Art Unit
	ELIAS ULLAH	2892

SEARCHED			
Class	Subclass	Date	Examiner
257	686	8/7/2008	EU

SEARCH NOTES		
Search Notes	Date	Examiner
EAST database serarch	8/7/2008	EU

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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BIB DATA SHEET

CONFIRMATION NO. 5045

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/322,442	12/29/2005 RULE	257	2892	6005.011

APPLICANTS

Rey Bruce, San Jose, CA;
Ricardo Bruce, Union City, CA;
Patrick Digamon Bugayong, Mandaluyong City, PHILIPPINES;
Joel Alonzo Baylon, Tanza, PHILIPPINES;

**** CONTINUING DATA **************************

**** FOREIGN APPLICATIONS **************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **
02/10/2006

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /ELIAS ULLAH/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	28	26	2

ADDRESS

URIARTE LAW
257 RODONOVAN DRIVE
SANTA CLARA, CA 95051
UNITED STATES

TITLE

Multiple chip module and package stacking method for storage devices

FILING FEE RECEIVED		
650	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	("("6172874" | "6900528").PN.").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/07/31 10:02
S2	4	("6172874" | "6900528").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/31 10:03
S3	2	"20070158808".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/31 10:07
S4	41	("5018005" | "5041903" | "5103375" | "5561593" | "5790380" | "5861666").PN. OR ("6172874").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/31 10:53
S5	2909	257/686.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/31 11:01
S6	183	S5 and (stack$2 adj module)	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/31 11:01
S7	418352	(signal same active or passive)	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/31 11:02
S8	272545	(signal same (active or passive))	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/31 11:02
S9	19	S6 and (signal same (active or passive))	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/31 11:02
S10	1	"20060206745".pn.	US-PGPUB; USPAT; USOCR	OR	ON	2008/08/04 08:57
S11	1	"20070158808".pn.	US-PGPUB; USPAT; USOCR	OR	ON	2008/08/04 09:00
S12	1	"5995379".pn.	US-PGPUB; USPAT; USOCR	OR	ON	2008/08/04 09:45
S13	1	"5995379".pn.	US-PGPUB; USPAT; USOCR	OR	ON	2008/08/06 12:57

S14	1	11/322442	US-PGPUB; USPAT; USOCR	OR	ON	2008/08/07 08:06

8/7/2008 12:00:51 PM
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PTO/SB/08a (03-08)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	11322442
Filing Date	2005-12-29
First Named Inventor	Rey H. Bruce
Art Unit	2811
Examiner Name	
Attorney Docket Number	6005.011

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Examiner Name	
Attorney Docket Number	6005.011

	1	JEFFREY C. DEMMIN, Novel 3-D Packaging Approaches Simplifying the Assembly and Test Supply Chain, Business Briefing: Global Semiconductor Manufacturing Technology, 2003, pp. 1-5	☒
	2	MOODY DREIZA, AKITO YOSHIDA, JONATHAN MICKSCH AND LEE SMITH, Stacked Package-on-Package Design Guideliness, Chip Scale Review, July 2005, pp.1-4, Reprinted by Amkor Technology, Inc. Chandler, Arizona	☒

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EXAMINER SIGNATURE

Examiner Signature	/Elias Ullah/	Date Considered	08/07/2008

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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PTO/SB/08a (03-08)
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(Not for submission under 37 CFR 1.99)

Application Number	11322442
Filing Date	2005-12-29
First Named Inventor	BRUCE et al.
Art Unit	2892
Examiner Name	ULLAH, Elias
Attorney Docket Number	6005.011

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6172874	B1	2001-01-09	BARTILSON	Entire Document
	2	6900528	B2	2005-05-31	MESS et al.	Entire Document

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	1994006210	WO	A1	1994-03-17	GOEL	Entire Document	☐

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Application Number	11322442
Filing Date	2005-12-29
First Named Inventor	BRUCE et al.
Art Unit	2892
Examiner Name	ULLAH, Elias
Attorney Docket Number	6005.011

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	ISA/US (Blaine Copenheaver), International Search Report and Written Opinion for International Application No. PCT/US06/62747, nine pages.	☐

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EXAMINER SIGNATURE

Examiner Signature	/Elias Ullah/	Date Considered	08/07/2008

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: BRUCE, et al.	)	Group Art Unit: 2892
	)	
Serial No.: 11/322,442	)	Examiner: ULLAH, Elias
	)	
Application Filing Date: 29 Dec 2005	)	
	)	
For: MULTIPLE CHIP MODULE & PACKAGE STACKING METHOD FOR STORAGE DEVICES	)	
	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY TO RESTRICTION REQUIREMENT

Dear Sir:

In response to the Office Action, mailed 3 June 2008, please kindly amend this Application as follows and consider the remarks set forth below.

A listing of claims begin on page 2; and

Remarks begin on page 11 of this paper.

Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (CANCELLED) A method for stacking a plurality of modules comprising the steps of:

providing one or more active port on the plurality of modules for carrying one or more active signal;

providing one or more passive port on the plurality of modules for passing through the one or more active signals; and

stacking the plurality of modules.

2. (CANCELLED) The method of claim 1 wherein the one or more passive port forms a ladder like routing path.

3. (CANCELLED) The method of claim 1 wherein one or more of the plurality of module is rotated before being stacked and the one or more passive port forms a rotational routing path.

4. (CANCELLED) The method of claim 1 further comprising the step of providing one or more pair of daisy chain input port and daisy chain output port for forming a first daisy chain connection wherein each pair of the daisy chain input port and the daisy chain output port are connected through a daisy chain circuit.

5. (CANCELLED) The method of claim 4 further comprising the step of providing one or more control port for enabling a routing path extending the first daisy chain connection within an end module.

6. (CANCELLED) The method of claim 5 wherein the routing path within the end module is connected to a second daisy chain connection.

7. (CANCELLED) The method of claim 1 wherein one or more of the plurality of modules is a main board.

8. (CANCELLED) The method of claim 7 wherein one or more vertically stacked module is connected to the main board.

9. (CANCELLED) The method of claim 2:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located between a pre-determined distance to each other in a repeating pattern, the pre-determined distance equaling a multiple of a periodic distance of the repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the ladder like routing path; and

wherein the ladder like routing path comprises one or more passive ball and one or more passive pad.

10. (CANCELLED) The method of claim 3:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located opposite each other in a repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the rotational routing path; and

wherein the rotational routing path comprises one or more passive ball and one or more passive pad.

11. (CANCELLED) The method of claim 4:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection; and

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad.

12. (CANCELLED) The method of claim 5:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad; and

wherein the routing path comprises one or more tri-state driver controlled by the one or more control port.

13. (CANCELLED) The method of claim 6:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad;

wherein the routing path comprises one or more tri-state driver controlled by the one or more control port; and

wherein one or more daisy chain connection are extended through one or more vertically stacked module connected to a main board.

14. (ORIGINAL) A stacked module comprising a plurality of modules each comprising:

one or more active port for carrying one or more active signal; and

one or more passive port for passing through the one or more active signals.

15. (ORIGINAL) The stacked module of claim 14 wherein the one or more passive port forms a ladder like routing path.

16. (ORIGINAL) The stacked module of claim 14 wherein one or more of the plurality of module is rotated before being stacked and the one or more passive port forms a rotational routing path.

17. (ORIGINAL) The stacked module of claim 1 further comprising one or more pair of daisy chain input port and daisy chain output port for forming a first daisy chain connection wherein each pair of the daisy chain input port and the daisy chain output port are connected through a daisy chain circuit.

18. (ORIGINAL) The stacked module of claim 17 further comprising one or more control port for enabling a routing path extending the first daisy chain connection within an end module.

19. (ORIGINAL) The stacked module of claim 18 wherein the routing path within the end module is connected to a second daisy chain connection.

20. (ORIGINAL) The stacked module of claim 14 wherein one or more of the plurality of modules is a main board.

21. (ORIGINAL) The method of claim 20 wherein one or more vertically stacked module is connected to the main board.

22. (ORIGINAL) The stacked module of claim 15:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located between a pre-determined distance to each other in a repeating pattern, the pre-determined distance equaling a multiple of a periodic distance of the repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the ladder like routing path; and

wherein the ladder like routing path comprises one or more passive ball and one or more passive pad.

23. (ORIGINAL) The stacked module of claim 16:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located opposite each other in a repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the rotational routing path; and

wherein the rotational routing path comprises one or more passive ball and one or more passive pad.

24. (ORIGINAL) The stacked module of claim 17:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection; and

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad.

25. (ORIGINAL) The stacked module of claim 18:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad; and

wherein the routing path comprises one or more tri-state driver controlled by the one or more control port.

26. (ORIGINAL) The stacked module of claim 19:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad;

wherein the routing path comprises one or more tri-state driver controlled by the one or more control port; and

wherein one or more daisy chain connection are extended through one or more vertically stacked module connected to a main board.

Remarks

Invention II, directed to a stacked module comprising a plurality of modules, is elected without traverse. The claims 14-26 are readable thereon, and encompass the elected invention.

Claims 1-13 are readable to non-elected invention I, and thus, are cancelled without prejudice.

If, in the opinion of the Examiner, an interview would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney at the number indicated below.

Respectfully submitted,

Dated: 27 June 2008

/Stephen R. Uriarte/
Stephen R. Uriarte, Reg. No. 40,854

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Email: mail@uriartelaw.com

Electronic Acknowledgement Receipt

EFS ID:	3533907
Application Number:	11322442
International Application Number:	
Confirmation Number:	5045
Title of Invention:	Multiple chip module and package stacking method for storage devices
First Named Inventor/Applicant Name:	Rey Bruce
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.011
Receipt Date:	27-JUN-2008
Filing Date:	29-DEC-2005
Time Stamp:	16:29:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

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1	Response to Election / Restriction Filed	6005_011_1stRsp2OA_RR_20080627.pdf	96980 69e23bf2d892202f0595972f3bdce0c204030ac0	no	11
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New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 11/322,442	Filing Date 12/29/2005	☐ To be Mailed

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☒		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
AMENDMENT	**06/27/2008**	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 13	Minus	** 26	= 0	X $25 =	0	OR	X $ =	
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $105 =	0	OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE	

		(Column 1)		(Column 2)	(Column 3)					
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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Art Unit	2892
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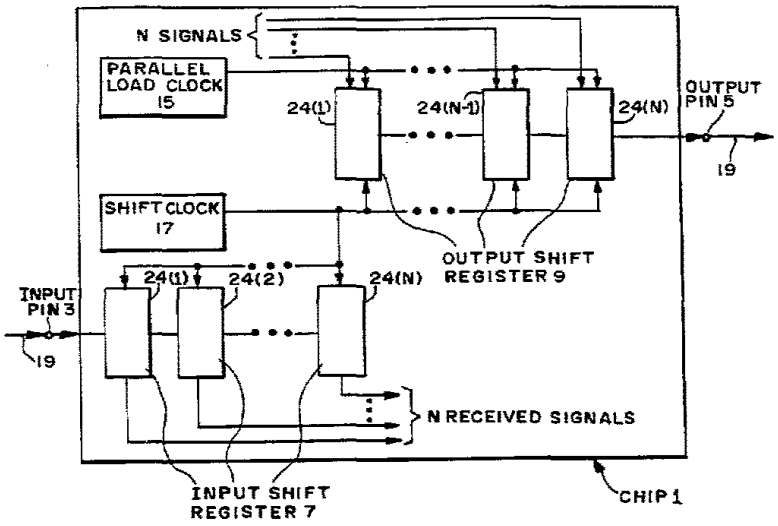
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(54) Title: MULTICHIP IC DESIGN USING TDM



(57) Abstract

In a multichip integrated circuit module (4), the number of effective input/output pins (3, 5, respectively) is increased by using techniques of TDM (time division multiplexing). A first chip (1) has at least one output shift register (9). A second chip (1) has at least one input shift register (7). Interconnection wires (19) couple the output shift registers (9) and the input shift registers (7). Means (15) are provided for loading data in parallel to the output shift registers (9). Means (17) are provided for sequentially shifting data through the output shift registers (9) over the interconnections (19) and into the shift input registers (7). Embodiments of the invention are described for use in conjunction with bi-directional pins (25), tri-state output drivers (21), and asynchronous logic (18).

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Description
MULTICHIP IC DESIGN USING TDM

Field of the Invention

This invention pertains to the field of designing circuits having a plurality of integrated circuit (i.c.) chips, said design using techniques of TDM (time division multiplexing).

Description of Background Art

Dobbelaere et al., "Field Programmable MCM Systems -- Design of an Interconnection Frame", IEEE 1992 Custom Integrated Circuits Conference, pp. 4.6.1-4.6.4, addresses the same problem addressed by the present invention -- increasing the number of effective input/output pins in a multichip i.c. module -- by different techniques. The references teaches programming a matrix at the corner of each chip to determine the interconnects among the inputs and outputs. The chips are FPGA's (field programmable gate arrays). The reference does not disclose the use of shift registers or TDM.

"Programmable Interconnect Architecture", Aptix Corporation Technology Backgrounder, Nov. 1991, pp. 1-14, and an Aptix press release dated January 1, 1992, describe use of an areal grid to preserve the ability to change the interconnects among a set of integrated circuit chips in applications where a logic is being implemented onto a set of multiple i.c.'s. These references do not disclose techniques of TDM. Shift registers are used, but only to determine which i.c.'s get connected to each other. The present invention uses shift registers to convey signal information from chip to chip.

U.S. patent 5,036,473 uses dedicated FPGA's solely to determine what active FPGA's get connected to which others. The reference discloses the use of software to drive and observe signals, but does not disclose the use of shift registers or TDM.

U.S. patent 5,109,353 discloses an array of programmable gate elements for emulating electronic

circuits and systems. It does not disclose the use of shift registers or TDM.

"Handbook of Hardware Modeling", Logic Modeling Systems Incorporated, February 1992, describes the use of software to drive and observe signals in a multichip module. Techniques disclosed in this reference can be used in conjunction with the invention described herein.

"Computer-Aided Prototyping", Quickturn Systems, Inc., 1991, pp. 1-4, discloses partitioning logic for a set of interconnected FPGA's and providing software stimulus to capture and observe the response. There is no disclosure of shift registers or TDM. This technology is further described in "FastForward", LSI Logic, September 1991, and "MARS Product Overview", PiE Design Systems, Inc. Similar technology is described in three press releases by InCA Integrated Circuit Applications: "InCA 'Virtual ASIC' Emulation System supports Xilinx 4000 family FPGAS", June 8, 1992; "Virtual ASIC, Automatic ASIC Emulation from InCA", 1991; and "Concept Silicon partitions your design onto multiple FPGAs".

Disclosure of Invention

The present invention is a multichip integrated circuit module (4) comprising at least two integrated circuit chips (1). The first chip (1) has at least one output shift register (9). The second chip (1) has at least one input shift register (7). Interconnections (19) couple the output register(s) (9) and the input shift register(s) (7). Means (15) are provided for loading data in parallel to the output shift register(s) (9). Means (17) are provided for sequentially shifting data through the output shift register(s) (9) over the interconnections (19) and into the input shift register(s) (7).

Brief Description of the Drawings

These and other more detailed and specific objects and features of the present invention are more fully disclosed in the following specification, reference being had to the accompanying drawings, in which:

Figure 1 is a sketch of an embodiment of the present invention in which an integrated circuit chip 1 uses at least one input shift register 7 and one output shift register 9.

Figure 2 is a sketch showing how the techniques of the present invention reduce the number of interconnection wires 19 among chips 1.

Figure 3 is a sketch of an embodiment of the present invention in which the number of stages 24 in an input shift register 7 and output shift register 9 can be reduced by one.

Figure 4 is a sketch of a chip 1 using tri-state output drivers 21.

Figure 5 is a sketch of an embodiment of the present invention in which two output shift registers 9 are used in conjunction with a single output driver 21.

Figure 6 is a sketch showing a plurality of tri-state output drivers 21, each having a common gating signal 23.

Figure 7 is a sketch showing how a single output shift register 9 can be used when the output drivers 21 have a common gating signal 23.

Figure 8 is a sketch showing the use of bi-directional pins and a plurality of tri-state output drivers 21 having a common gating signal 23.

Figure 9 is a sketch showing how a single bi-directional pin 25 can be used when a plurality of tri-state output drivers 21 have a common gating signal 23.

Figure 10 shows a chip 1 having a plurality of bi-directional pins 25, each coupled to an output driver 21 that has a different gating signal.

Figure 11 shows a single pin 25 equivalent to the embodiment depicted in Figure 10.

Figure 12 shows an embodiment of the present invention in which asynchronous logic 18 is employed.

Figure 13 shows an embodiment of the present invention in which a plurality of output shift registers 9 are daisy chained together.

Figure 14 shows an embodiment of the present invention in which a plurality of test shift registers 12 are multiplexed together.

Figure 15 shows an embodiment of the present invention in which the TDM sequence must be applied twice.

Figure 16 shows an embodiment of the present invention in which an interconnect 19 couples two chips 1.

Figure 17 shows how the interconnect 19 of Figure 16 can be reconfigured by reprogramming the first chip 1(1).

Figure 18 shows a single interconnect 19 coupling four chips 1.

Figure 19 shows how the interconnect 19 of Figure 18 can be reprogrammed by reprogramming the source chip 1(1).

Figure 20 shows an embodiment of the present invention in which an interconnect wire 19 couples two chips 1.

Figure 21 shows how the interconnect 19 of Figure 20 can be reprogrammed by adding a new signal S3 to the source chip 1(1).

Figure 22 shows an embodiment of the present invention in which the number of stages 24 in an input shift register 7 can be reduced by one.

Detailed Description of the Preferred Embodiments

A major purpose of this invention is to increase the effective number of input/output (I/O) pins 3,5 on integrated circuit chips 1 within a module 4 that comprises a plurality of said chips 1. The invention can be thought of as creating a number of virtual I/O pins 3,5 that is greater than the number of actual pins 3,5. The invention also eases pressures on the system designer when the number of interconnect wires 19 on the module 4 is limited. Further, the invention enhances the reconfigurability of signal flow across chips 1.

An example where the invention is useful is in the design of a system 4 in which there is a need to fit a given amount of logic, which may be provided in the form of a netlist, into one or more of the chips 1. Normally, said chips 1 come with a fixed number of I/O pins 3,5 that are used for interconnections 19 among the chips 1.

The limited number of I/O pins 3,5 can greatly reduce the efficiency of utilizing the chips 1, and in some cases make the task of fitting the logic into the chips 1 extremely difficult.

The module 4 can be a production module, in which the chips 1 are executable and application-ready. Alternatively, module 4 can be a prototype module, in which the chips 1 are experimented with by the designer to create a system design. Changes in such a prototyping environment are typically done by a combination of hardware and software changes. Alternatively, module 4 can contain some production chips 1 and some programmable chips 1.

Chips 1 are any chips for which the user has control over the contents, such as FPGA's (field programmable gate arrays), non-field-programmable gate arrays, custom i.c.'s, semi-custom i.c.'s (application specific integrated circuits), and standard cell i.c.'s. FPGA's are normally preferable, because of their flexibility.

The present invention makes use of techniques of TDM (time division multiplexing or time domain multiplexing). The execution of the system embodied in module 4 takes longer because of this, but in many applications this is of no concern. The TDM process is transparent to the operation of the logic embodied in module 4.

Typically the TDM is implemented by shift registers 7,9, as illustrated in Figure 1. Each input pin 3 and each output pin 5 on a chip 1 is assigned a dedicated shift register, 7,9, respectively. The number of stages 24 in a shift register 7,9 is referred to as N. N is any positive integer greater than or equal to 2, and could be typically between 2 and 5. Preferably, N is the same for all shift registers 7,9 on a chip 1. If N were not the same, a separate shift clock 17 would be needed for each different value of N. In the chip 1 illustrated in Figure 1, the value of N is the same, and therefore there is but one shift clock 17.

Each chip 1 can have a plurality of input pins 3 and a different number of output pins 5. The different chips 1 on a module 4 can have different numbers of input pins 3 and output pins 5.

The individual stages 24 of the shift registers 7,9 can be, for example, flip-flops, edge triggered latches, and pairs of polarity hold latches. When polarity hold latches are used, a pair of shift clocks 17 is required for use with the corresponding shift register 7,9.

The shift register 9 attached to an output pin 5 is referred to as an output shift register (OSR) 9, and functions as N virtual output pins 5. N internal signals from within the chip 1 can be loaded into the OSR 9 in parallel by means of activating a parallel load clock 15 associated with the OSR 9. These signals are then serially shifted out of the OSR 9 over the corresponding output pin 5 using the shift clock 17 associated with said OSR 9. The signals travel over interconnection wires 19 to other chips 1 that need to receive the signals.

Similarly, the shift register 7 attached to an input pin 3 is referred to as an input shift register (ISR) 7, and functions as N virtual input pins 3. It can receive serially N signals from a board interconnect 19 through the associated input pin 3 by means of the shift clock 17 that is connected to said ISR 7. The received signals can then simultaneously be applied inside the chip 1 using their stored states within the stages of the ISR 7. No special clock is needed to unload the signals from the ISR 7, because once these signals are in the ISR 7, they are visible to the logic within the chip 1.

Preferably, a single parallel load clock 15 and a single shift clock 17 are used for all the ISR's 7 and OSR's 9 on the board 4.

Preferably, the OSR's 9, ISR's 7, and attendant parallel load and shift clocks 15, 17 are customized within peripheral regions of the gate arrays 1. Alternatively, the OSR's 9 and ISR's 7 are fabricated from logic normally present on the gate arrays 1.

Figure 2 illustrates how the invention minimizes the number of interconnect wires 19 among chips 1,2 and minimizes the number of I/O pins 3,5 within a chip 1. Figure 2 illustrates the interconnections of OSR 9 within a source chip 1 and three ISR's 7 residing within three target (sink) chips 1. The target chips 1 could be identical or different in a hardware sense. A single interconnect wire 19 couples the chips 1. Three signals S1, S2, and S3 from the source chip 1 are conveyed to the three sink chips 1. If the TDM and shift register technique were not used, three interconnects 19 would be required. The interconnect wire 19 can be thought of as a TDM bus which bundles in the time domain the three signals S1, S2 and S3. Said TDM bus 19 is visible to all three sink chips 1.

As illustrated in Figure 2, not all of the three signals need to be used in each sink chip 1. (The signals within the sink chips 1 are primed for notational purposes.)

The TDM process described herein is transparent to the intended logic design. This transparency can be achieved in different ways, depending upon the degree of transparency needed. For example, if all chips 1 on the module 4 are synchronously clocked (which is preferable), the following two-step TDM process can be used, at a safe time after the application of each pulse from the system clock (not illustrated). The safe time is that amount of time needed for all of the signals in the logic to achieve a steady state, i.e., when the intended design has been programmed into the chips 1.

Step 1. The parallel load clock 15 (which is preferably a single clock applied to all output shift registers 9 on the board 4) is applied to effect a parallel capture of signals into all of the OSR's 9 on all the chips 1.

Step 2. Using the shift clock 17 (preferably a single clock used by all the ISR's 7 and OSR's 9 on all the chips 1), the contents of all of the OSR's 9 are shifted into the target ISR's 7 via the interconnects

19. This shifting process involves N applications of shift clock 17 to all of the chips 1.

Exceptions to the above scheme exist for various reasons, such as: (1) Certain I/O pins are bi-directional pins 25 (see Figure 8). Such bi-directional pins 25 could be left unmodified. Signals involving such pins 25 are not affected by the above two steps. (2) Inputs 3 that receive direct clock signals (as opposed to data signals) do not require the use of an ISR 7. Such would be undesirable, because it would cause the clock to jiggle. Similarly, output pins 5 that carry clock signals going to other chips 1 do not require the use of OSR's 9. Clock signals cannot be transferred across chips 1 using TDM without significant impact to the intended logic. As such, it is not desirable to use such techniques for I/O pins 3,5 that carry clock signals.

Figure 12 shows that if the logic being prototyped is asynchronous, an additional latch 29 is needed for each ISR 7 stage 24 that drives a piece of asynchronous logic 18. Such a latch 29 is a voltage level or logic level sensitive latch that receives its data from an ISR 7 stage output and is clocked by yet another clock called the P clock 27. P clock 27 is shared among all chips 1 that have asynchronous logic. The function of this added latch 29 is to screen the shifting of the ISR 7 from the asynchronous logic 18. P clock 27 is pulsed once after the completion of the two usual TDM steps, described earlier, that are used to effectuate the transfer of signals across chip 1 boundaries using TDM. As shown in Figure 12, some of the stages 24 of the ISR 7 can drive synchronous logic 16, and others of the stages 24 can drive asynchronous logic 18.

As illustrated in Figures 13 and 14, multiple OSR's 9 can be connected into one daisy-chained composite "test shift register" (TSR) 12 on each chip 1 to facilitate the observation of the captured signals externally by shifting out the TSR 12. All of the observation can be performed at the output of pin 5(M). These observed signals can be used for debugging the prototype hardware,

depending upon the availability of extra board 4 logic and pins 3,5. The contents of the TSR 12 can then be reloaded from the output 5(M) of the TSR 12 to the shift register data input 3 on the same chip 1 if it is desired to continue with the operation of the hardware. A preferred way of accomplishing this reloading is to make a connection on the chip 1 itself from output 5(M) to input 3, thereby creating a circular shift register.

The set of TSR's 12 can be multiplexed to be observable at the output 10 of the board 4 as illustrated in Figure 14. Multiplexer select signals 14 control the selection of the individual TSR 12 outputs by multiplexer 8. The input to all the TSR's 12 is injected via board input 6. The scheme depicted in Figure 14 is useful when there are more chip output pins 5 that the designer wants to observe than there are available board output pins 10.

Since the OSR's 9 are usable for debugging purposes, the designer can choose to provide extra, initially unused, stages 24 within some OSR's 9. These stages 24 are then available to be used for observing internal signals that the hardware designer may not have thought about earlier, for example, by changing the programming on the chip 1 to look at these stages 24.

It is possible to reconfigure the interconnects 19 among the chips 1 by sending a different set of signals on each interconnect 19 than was previously intended. When combined with the internal reconfigurability of the FPGA 1 itself, a powerful new type of reconfigurability is thereby created. Figure 14 shows a module 4 with a number of FPGA's 1 and set up for using TDM. To achieve a reprogrammable board 4, it is required that one must able to reprogram both the logic on the chips 1 as well as the interconnects 19. The on-chip logic is already rather reprogrammable through the use of the FPGA's 1. To reprogram the interconnects 19, an FPGA 1 can be used as a programmable interconnect chip as in U.S. patent 5,036,473, cited above; or a programmable interconnect chip as described in the Aptix references cited above can be used. Alternatively, several programmable

interconnect chips 1 may be used. A limited reprogrammability of interconnects is described in Figures 16-21.

Figure 16 shows three signals, S1, S2, S3, TDM'ed between chips 1(1) and 1(2). By reprogramming the first FPGA 1(1), the manner in which the three signals S1, S2, S3 connect can be changed, as shown in Figure 17. In effect, the connections 19 between the two chips 1 have been rewired.

Figure 18 shows four chips 1 with signals S1, S2, S3 connected as shown. By reprogramming the first chip 1(1), as shown in Figure 19, signal S3 crossing between chips 1(1) and chips 1(4) is changed to S4.

In Figure 20, two interconnected chips 1 are shown. Figure 21 shows how a signal can be added to the interconnect 19 just by reprogramming the individual chip 1(1) and not touching the interconnect 19.

The flexibility described herein results from chip 1 being able to reprogram a number of signals that are TDM'ed across to other chips 1. Traditional techniques limit the reprogramability to a single signal.

Once the value N is fixed for a given system 4, the total number of signals that can be moved across the chip 1 boundaries is predetermined. The total number of signals movable is N multiplied by the number of unique interconnect wires 19 on the board 4. It is apparent that by increasing N, a capacity greater than what is initially needed for the total number of signals can be achieved. The additional capability is usable for greater flexibility in reconfiguring the interconnects 19.

Theoretically, it is possible to accomplish all interconnections between any two chips 1 by using two interconnect wires 19 between them: one to carry signals flowing in one direction, and the second to carry signals flowing in the opposition direction. In this extreme situation of maximum multiplexing, the shift registers 7,9 must have an N greater than or equal to the larger of the number of the input signals and the number of the

output signals on any single chip 1. (One signal is associated with each stage 24 of a shift register 7,9.)

The techniques of the present invention can be selectively applied to areas of logic that are considered susceptible to change or require use of TDM to accommodate the number of signals that need to traverse across chip 1 boundaries. As such, ISR's 7 and OSR's 9 need not be placed on all qualifying I/O pins 3,5. Instead, if there are insufficient resources on the chip 1, the ISR's and OSR's 7,9 may be deployed only on enough I/O pins 3,5 to allow adequate signal flow through the chips 1. It should be noted that an interconnect 19 must have either ISR's 7 and OSR's 9 on all terminals of that interconnect 19, or else must have no ISR's 7 or OSR's 9 at all.

When the chips 1 are FPGA's, it is possible to make engineering changes to prototype hardware 4 by reprogramming the affected FPGA's 1 to (1) change the logic realized by certain FPGA's 1 and/or (2) modify the effective interconnects 19 by capturing different signals into one or more of the OSR's 9 and/or (3) change the signals that are made observable by capturing them into unused stages 24 of OSR's 9.

Figure 22 shows an optimized version of the scheme in Figure 2. Here, the contents of the OSR 9 can be made observable, while reducing the number of stages 24 in an ISR 7 by one. In this embodiment, the state of the last stage 24 of an OSR 9 is used as a substitute for the eliminated stage 24 of an ISR 7.

In certain prototyping situations, it may not be necessary to observe the contents of the OSR's 9. In these cases, the number of stages 24 needed in an ISR 7 and OSR 9 can be reduced by one, corresponding to the stage 24 the system designer does not need to observe. This reduction is achieved by using the scheme depicted in Figure 3. Figure 3 shows how N equals 2 can provide the capability to multiplex three signals across a single interconnect 19. In this embodiment, the final state of the interconnect 19 after application of the TDM sequence

is used as one of the multiplexed signals for the sink chip 1(2). In contrast, the scheme depicted in Figure 2 does not have the sink chips 1 dependent upon the final state of the interconnect 19, but only on the states of the ISR's 7.

The scheme depicted in Figure 1 uses ISR's 7 and OSR's 9 to multiplex signals across chip 1 boundaries. Such a TDM sequence serves to transfer signals once across an interconnect 19. However, if there is a logic path that is not interrupted by a latch or other sequential logic (other than ISR's 7 and OSR's 9) and spans more than two FPGA chips 1, then the TDM sequence needs to be repeated. The total number of TDM sequence applications required is equal to the number of distinct board level interconnect wires 19 that are included in the logic path. Figure 15 shows a logic path of combinational logic 22 that spans two board level interconnect wires 19(1) and 19(2). There are no latches other than ISR's 7 and OSR's 9 in the path. As such, the TDM sequence needs to be applied twice to move the signal through the three chips 1. Notice that ISR's 7 and OSR's 9 force the use of TDM. Without ISR's 7 and OSR's 9, the signal from chip 1(1) to chip 1(2) to chip 1(3) would flow without any clocking.

The techniques of the present invention can be extended to bi-directional pins 25 and/or three state output drivers 21. (See Figure 4). Such a driver 21 typically has outputs of logical zero, logical one, and high impedance.

Buses 19 generally employ tri-state drivers 21 to allow multiple source chips 1 onto a single wire. Such buses 19 are intended by the designer to achieve efficient interconnects between a multitude of source chips 1 and some number of sink chips 1. Generally, one source chip output driver 21 is active while others are in a high impedance state, so that one source chip output driver 21 is driving all receivers in the bus 19. The architecture shown in Figure 1 cannot be employed directly in such a case. Figure 4 shows N output pins 5,

with a tri-state driver 21 on each pin 5. The OSR 9 scheme of Figure 1 will not work here, because the high impedance state cannot be transmitted via an OSR 9 and an ISR 7. Instead, the scheme shown in Figure 5 needs to be employed. It should be noted that this scheme uses two OSR's 9 instead of one: the first OSR 9(1) to capture the N gating signals and the second OSR 9(2) to capture the N data signals. Output driver 21 sees the corresponding gate-data combination as the OSR's 9 are shifted out. Thus, output pin 5 sees the gated output from output driver 21. The generated TDM sequence of signals on output pin 5 combines with similarly generated TDM sequences from other output pins 5 that are connected with this first output pin 5.

Figure 6 shows N output pins 5 with high impedance drivers 21 that share a common output gating signal 23. Signal 23 either produces a high impedance on the outputs of drivers 21 or else transmits the input signals to the outputs. Figure 7 shows a corresponding single pin architecture that avoids the use of two OSR's 9 but still places output driver 21 between the single OSR 9 and the output pin 5. The use of two OSR's 9 is avoided because of the presence of the common gating signal 23.

Figure 8 shows a typical N bi-directional pin 25 configuration with a common output gating signal 23. In Figure 8, the same pin 25 is used to both output a signal from the chip 1 as well as to receive signals from the outside. To achieve a single pin 25 architecture for TDM of the N signals, the scheme of Figure 9 is employed. In Figure 9, the architecture of Figure 7 is used to feed the outputs of the N drivers 21, and a single ISR 7 is used for the N input signals as in the Figure 1 embodiment.

Figure 10 shows N bi-directional pins 25, each with a different gating output signal. The single-pin 25 architecture equivalent for TDM of the N signals uses the scheme shown in Figure 11. In Figure 11, the architecture of Figure 5 is employed for the N output

drivers 21, and a single ISR 7 is applied to the N input signals as in the Figure 1 embodiment.

Personalization instructions are injected into module 4, e.g., by techniques described in U.S. patent 5,109,353 cited above. More than one logic design can be introduced into the module 4 by different personalization instructions. Software that is intended to provide automatic or interactive partitioning of the intended system design, such as Concept Silicon from InCA cited above, can exploit the knowledge of the existence of ISR's 7 and OSR's 9 to help pack more logic into each of the programmable chips 1 and/or to minimize the number of interconnection wires 19.

The software is executed on a computer external to module 4, e.g., a workstation. The software can be standalone (not physically coupled to module 4) software that exploits the hardware architecture of the module 4 as introduced by the invention. Alternatively, there can be physical coupling between the software and the module 4, e.g., the computer on which the software is executed can have an electrical connection to the module 4, over which the personalization created by the software is downloaded into the module 4.

The benefit of minimizing the number of chips 1 is obvious. The benefit of minimizing the number of interconnects 19 is significant. If the prototype board 4 is intended to utilize Aptix-type programmable interconnect chips, minimizing the number of interconnects 19 will reduce the number of Aptix components needed to achieve programmable interconnects. Either the software is told the number of virtual I/O's 3,5 rather than the actual number; or else the software is told all about the ISR's 7 and OSR's 9 so that it will take this information into account when it does the partitioning. The programmable interconnect chip does not always need to be changed. Rather, ISR's 7 and/or OSR's 9 are placed on the chips 1 to which the programmable interconnect chip is connected, thereby enhancing the programmable interconnect chip.

Combining the use of the present invention with the use of one or more programmable interconnect chips can allow the board 4 designer the flexibility of creating additional interconnects 19 among chips 1. Programmable interconnect chips are used to interconnect among two or more I/O pins 3,5. These I/O pins 3,5 could also have ISR's 7 and OSR's 9 on board the chip 1, thus providing a greatly increased number of programmable interconnects.

The configuration of the prototype board 4 is changed by a combination of hardware and software. For hardware changes, interconnects 19 are reprogrammed, FPGA's and/or programmable interconnect chips 1 are reprogrammed, FPGA's 1 are added or subtracted, and connections are obliterated using lasers. For software changes, software other than the partitioning software is used to, e.g., reprogram the Aptix chip(s) 1.

The above description is included to illustrate the operation of the preferred embodiments and is not meant to limit the scope of the invention. The scope of the invention is to limited only by the following claims. From the above discussion, many variations will be apparent to one skilled in the art that would yet be encompassed by the spirit and scope of the invention.

What is claimed is:

Claims

1. A multichip i.c. module comprising:

at least two integrated circuit chips, a first chip having at least one output shift register and a second chip having at least one input shift register;

interconnections coupling the output shift register(s) and the input shift register(s);

means for loading signals in parallel to the output shift register(s); and

means for sequentially shifting signals through the output shift register(s) over the interconnections and into the input shift register(s).

2. The multichip i.c. module of claim 1 wherein all chips are clocked synchronously.

3. The multichip i.c. module of claim 1 wherein at least one chip contains asynchronous logic, said chip comprising an input shift register that is coupled to said asynchronous logic via a polarity hold latch; wherein:

said polarity hold latch is clocked by a P clock.

4. The multichip i.c. module of claim 1 wherein at least some of the chips are gate arrays from the set comprising FPGA's and non-field-programmable gate arrays.

5. The multichip i.c. module of claim 4 wherein the output shift register(s), the input shift register(s), and associated clocking are customized within peripheral regions of the gate arrays.

6. The multichip i.c. module of claim 4 wherein the output shift register(s) and input shift register(s) are fabricated from logic normally present on the gate arrays.

7. The multichip i.c. module of claim 1 wherein the means for loading signals is a parallel load clock.

8. The multichip i.c. module of claim 1 wherein the module is a production module containing executable chips.

9. The multichip i.c. module of claim 1 wherein the multichip module is a prototype module containing at least some experimental chips.

10. The multichip i.c. module of claim 1 further comprising software means to partition logic among the chips, said software means exploiting information concerning the particular architecture of the module.

11. The multichip i.c. module of claim 1 wherein said module contains a programmable interconnect chip.

12. In a multichip i.c. module comprising at least two integrated circuit chips, each chip having a plurality of I/O pins, said module having inter-i.c. connection wires interconnecting said pins, a method for increasing the effective number of I/O pins, said method comprising the steps of:

time division multiplexing signals at an output pin of a first chip; and

sending said signals over a connection wire to an input pin of a second chip.

13. The method of claim 12 wherein all chips are clocked synchronously.

14. The method of claim 12 wherein said step of time division multiplexing comprises the substeps of:

parallel loading signals into an output shift register within a first chip; and

accessing signals in parallel from an input shift register within a second chip.

15. The method of claim 14 wherein at least some of the chips are gate arrays from the set comprising FPGA's and non-field-programmable gate arrays.

16. The method of claim 15 wherein the output shift register(s) and input shift register(s) are customized within peripheral regions of said gate arrays.

17. The method of claim 15 wherein the output shift register(s) and input shift register(s) are fabricated from logic normally present on said gate arrays.

18. The method of claim 14 wherein the input and output shift registers comprise stages fabricated from

items from the group of items comprising flip-flops, edge triggered latches, and pairs of polarity hold latches.

19. The method of claim 18 wherein one of said stages in reserved for debugging purposes.

20. The method of claim 12 further comprising the additional step of determining a logic design for the module by use of partitioning software that exploits information concerning the particular architecture of the module.

21. The method of claim 12 further comprising the step of observing said signals at said output pin for test purposes.

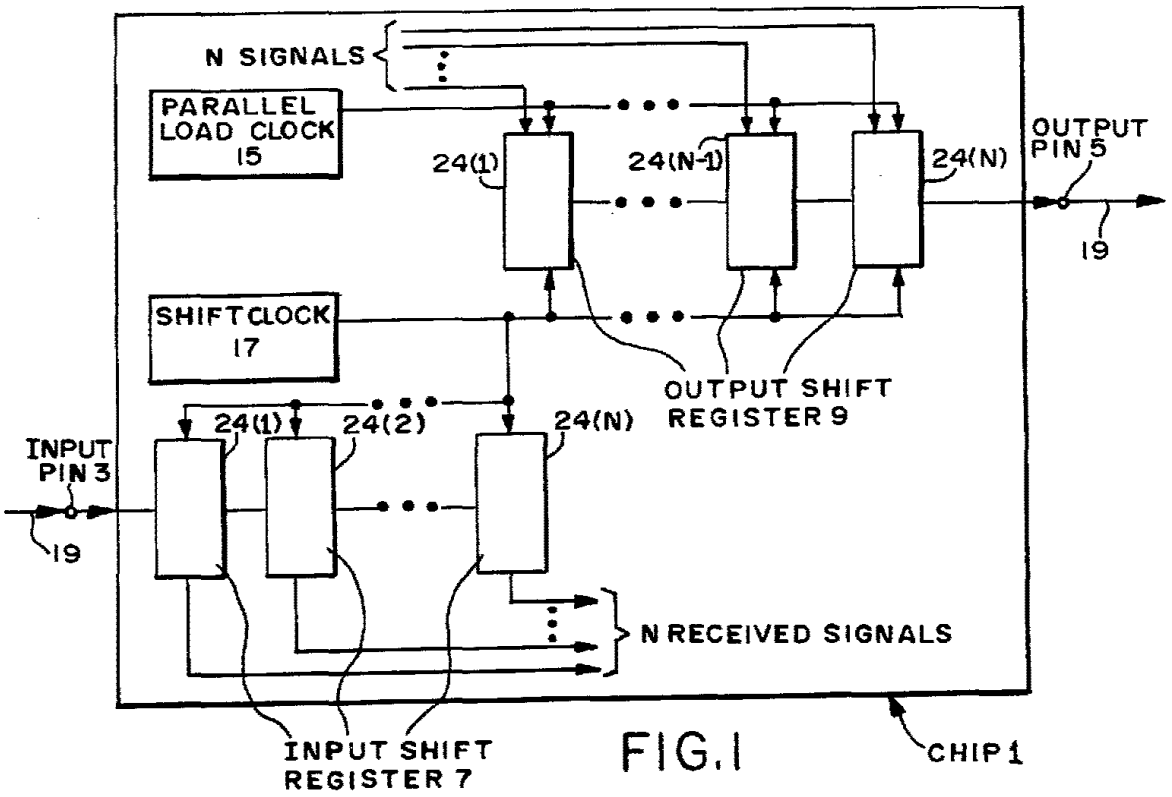
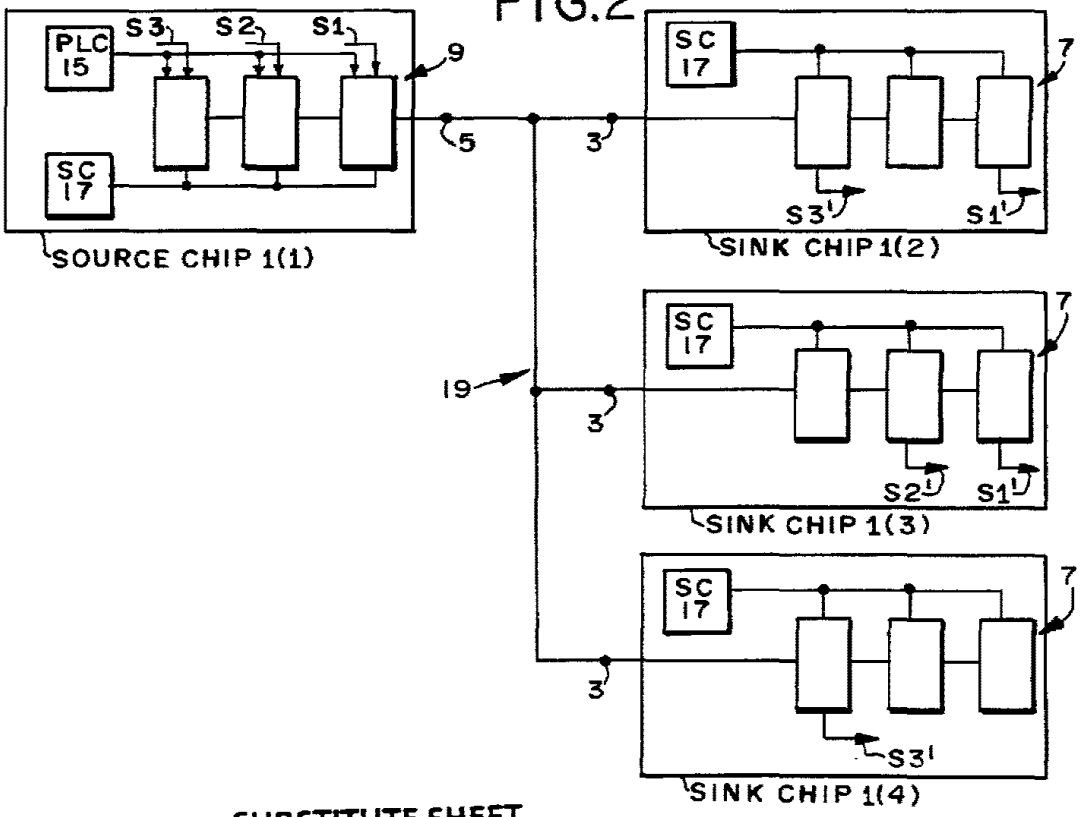

N SIGNALS
PARALLEL LOAD CLOCK 15
24(1)
24(N-1)
24(N)
OUTPUT PIN 5
19
SHIFT CLOCK 17
OUTPUT SHIFT REGISTER 9
24(1)
24(2)
24(N)
INPUT PIN 3
19
N RECEIVED SIGNALS
INPUT SHIFT REGISTER 7
CHIP 1

FIG.1

FIG.2


PLC 15
S3
S2
S1
9
SC 17
5
3
SOURCE CHIP 1(1)
SC 17
7
S3'
S1'
SINK CHIP 1(2)
19
3
SC 17
7
S2'
S1'
SINK CHIP 1(3)
3
SC 17
7
S3'
SINK CHIP 1(4)

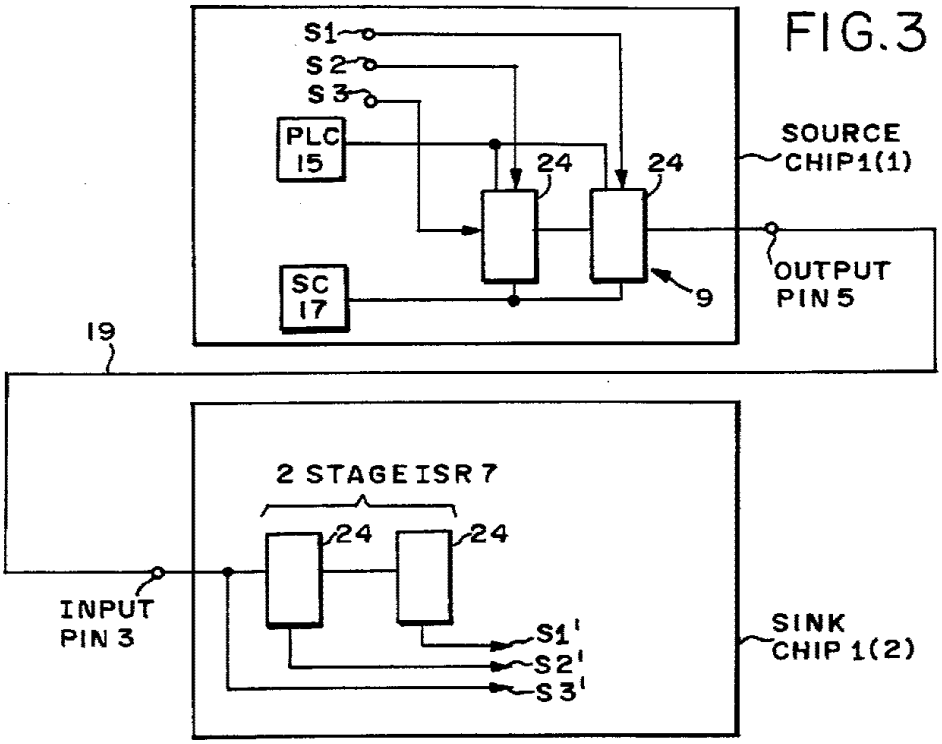

S1
S2
S3
PLC
15
24
24
SOURCE
CHIP1(1)
OUTPUT
PIN 5
SC
17
9
19
2 STAGE ISR 7
24
24
INPUT
PIN 3
S1'
S2'
S3'
SINK
CHIP 1(2)

FIG.3

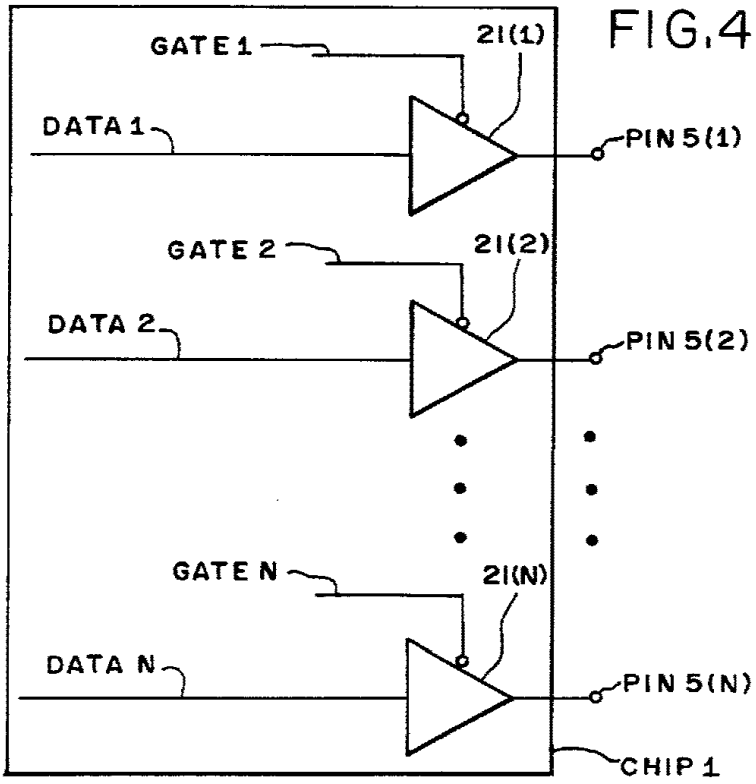

GATE 1
21(1)
DATA 1
PIN 5(1)
GATE 2
21(2)
DATA 2
PIN 5(2)
GATE N
21(N)
DATA N
PIN 5(N)
CHIP 1

FIG.4

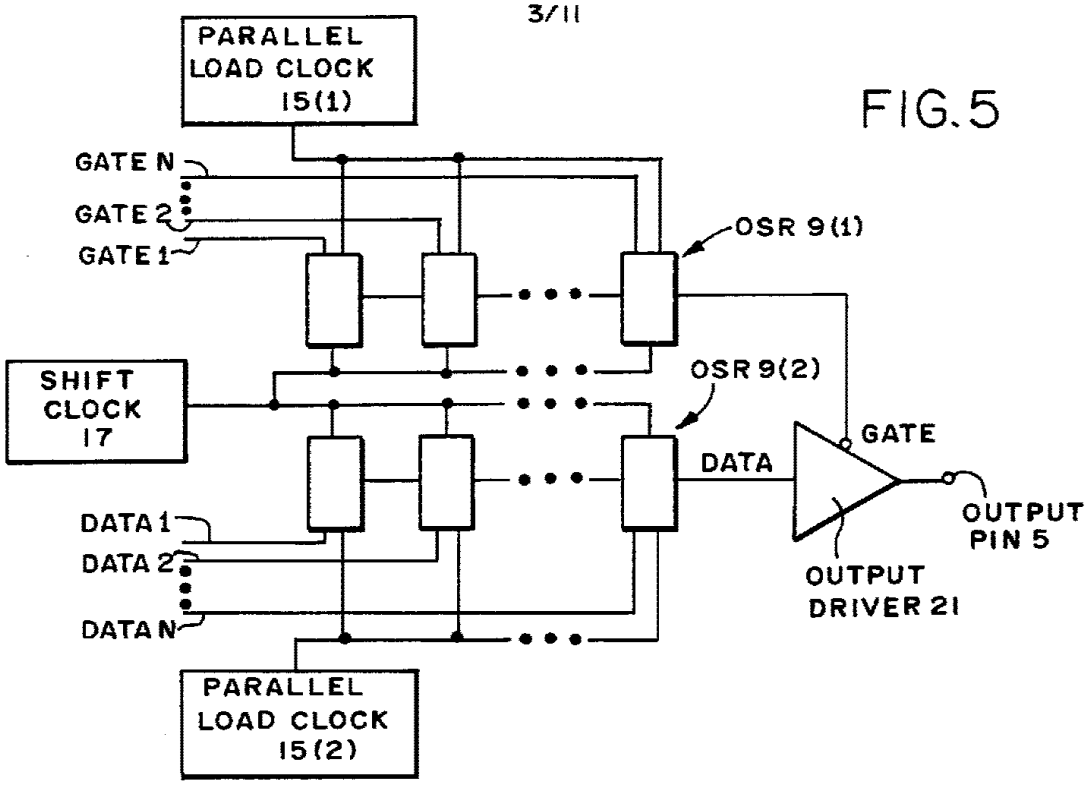

PARALLEL LOAD CLOCK 15(1)
GATE N
GATE 2
GATE 1
OSR 9(1)
SHIFT CLOCK 17
OSR 9(2)
GATE
DATA
OUTPUT PIN 5
DATA 1
DATA 2
DATA N
OUTPUT DRIVER 21
PARALLEL LOAD CLOCK 15(2)

FIG.5

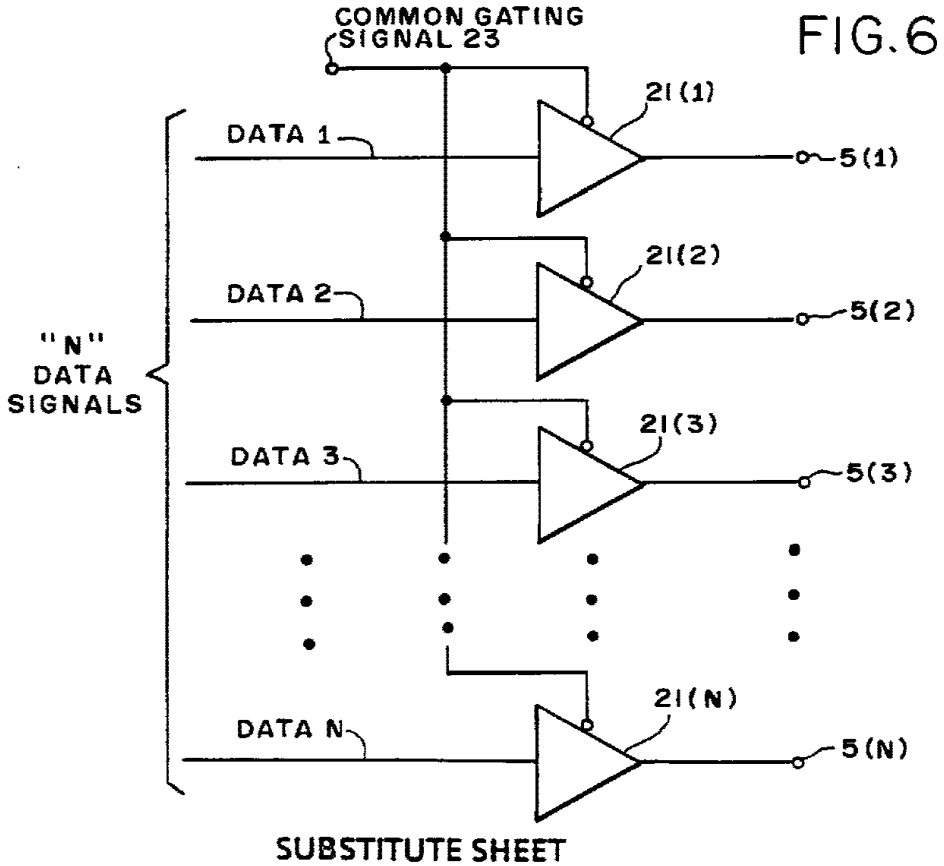

COMMON GATING SIGNAL 23
21(1)
DATA 1
5(1)
21(2)
DATA 2
5(2)
"N" DATA SIGNALS
21(3)
DATA 3
5(3)
21(N)
DATA N
5(N)

FIG.6

FIG.7

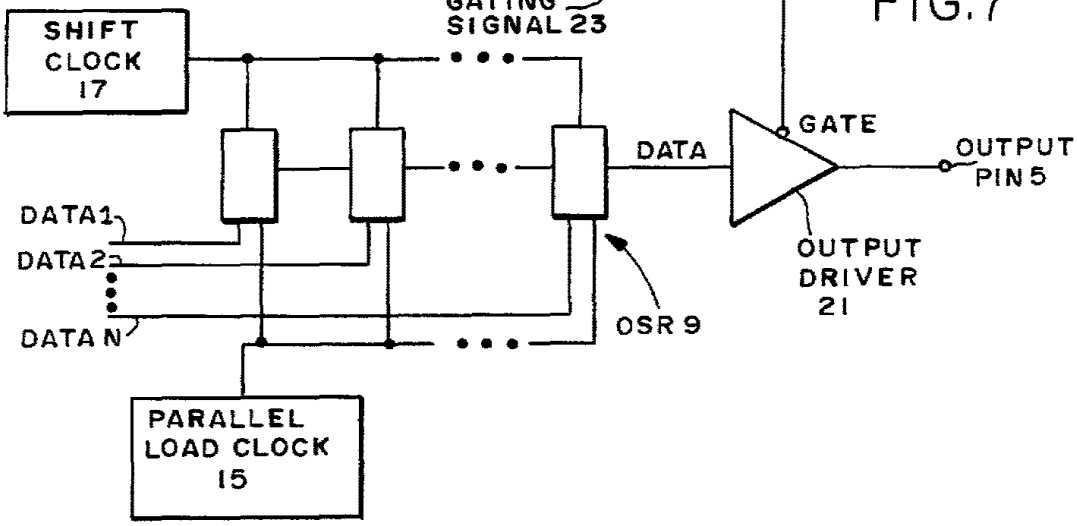
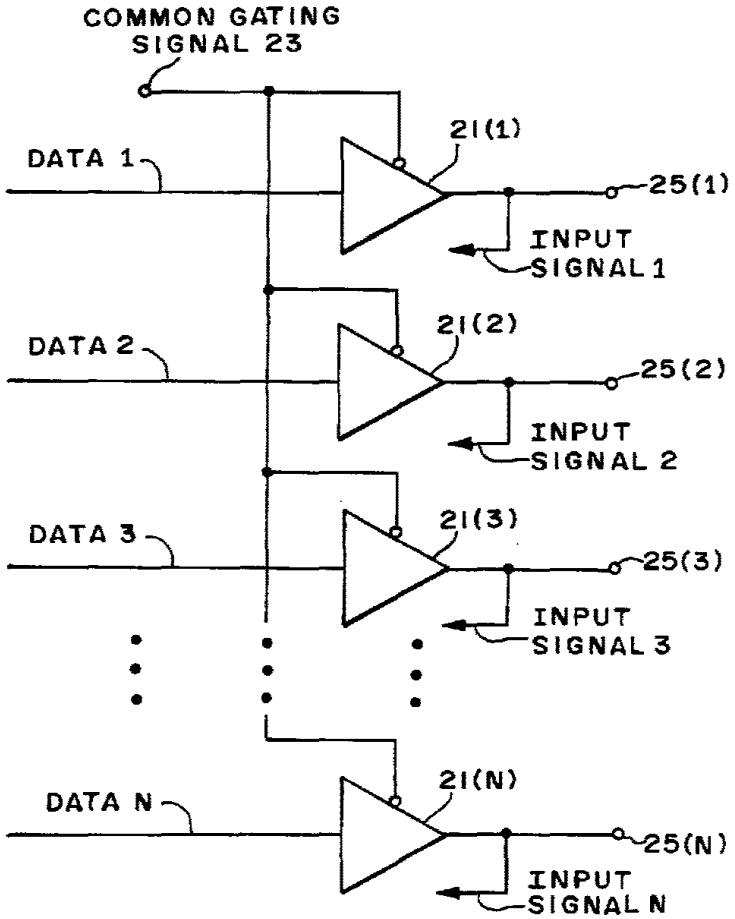


FIG.8



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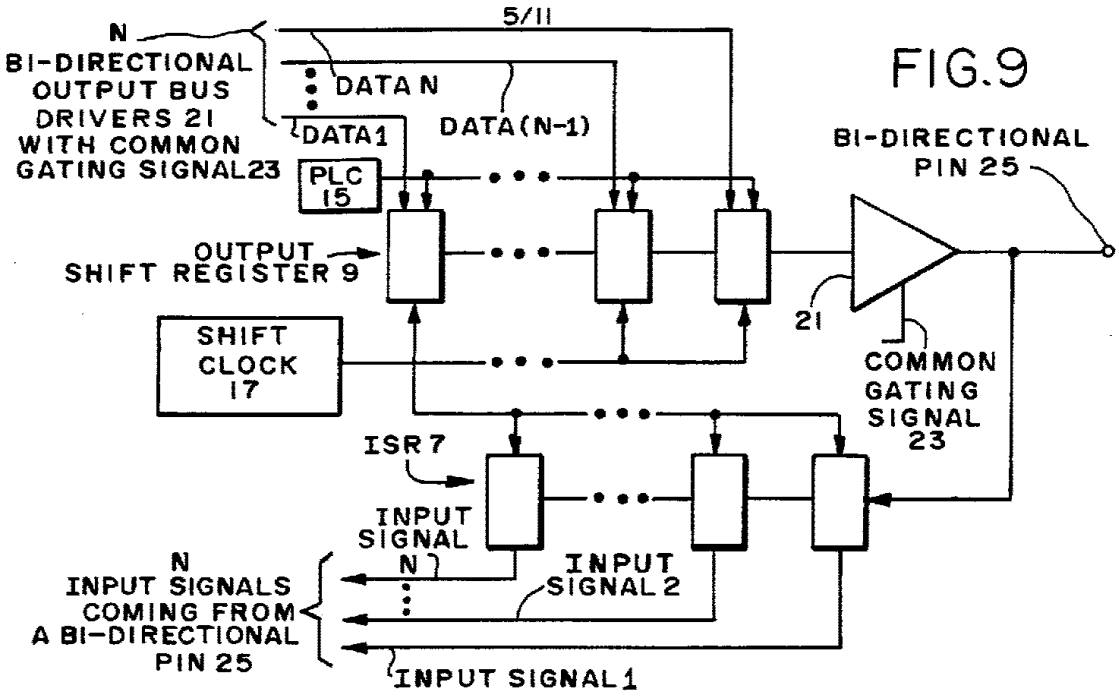

N
BI-DIRECTIONAL
OUTPUT BUS
DRIVERS 21
WITH COMMON
GATING SIGNAL 23
DATA N
DATA 1
DATA (N-1)
PLC
15
OUTPUT
SHIFT REGISTER 9
SHIFT
CLOCK
17
BI-DIRECTIONAL
PIN 25
21
COMMON
GATING
SIGNAL
23
ISR 7
INPUT
SIGNAL
N
INPUT
SIGNAL 2
N
INPUT SIGNALS
COMING FROM
A BI-DIRECTIONAL
PIN 25
INPUT SIGNAL 1

FIG.9

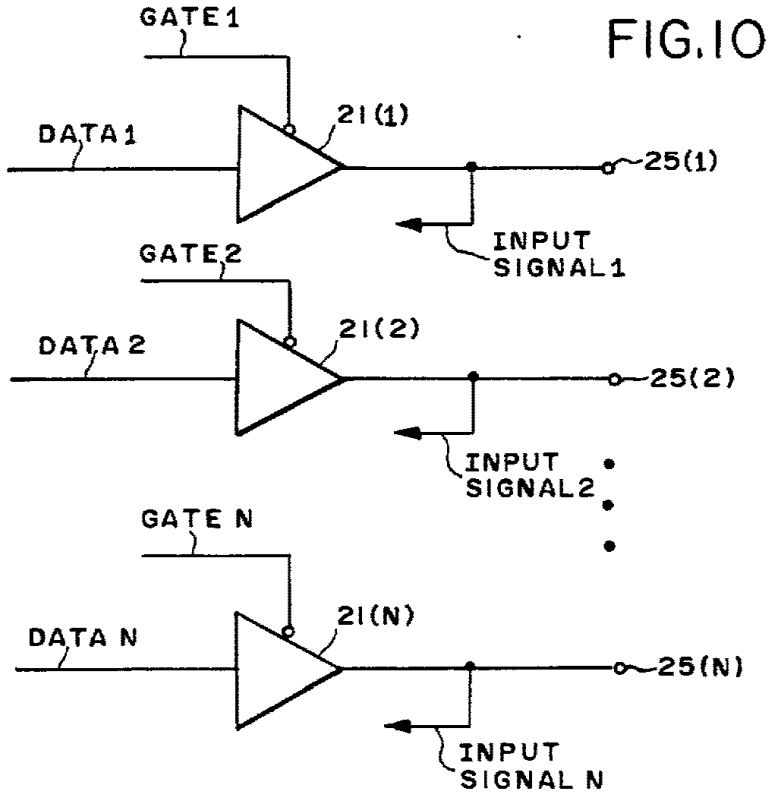

GATE 1
DATA 1
21(1)
25(1)
INPUT
SIGNAL 1
GATE 2
DATA 2
21(2)
25(2)
INPUT
SIGNAL 2
GATE N
DATA N
21(N)
25(N)
INPUT
SIGNAL N

FIG.10

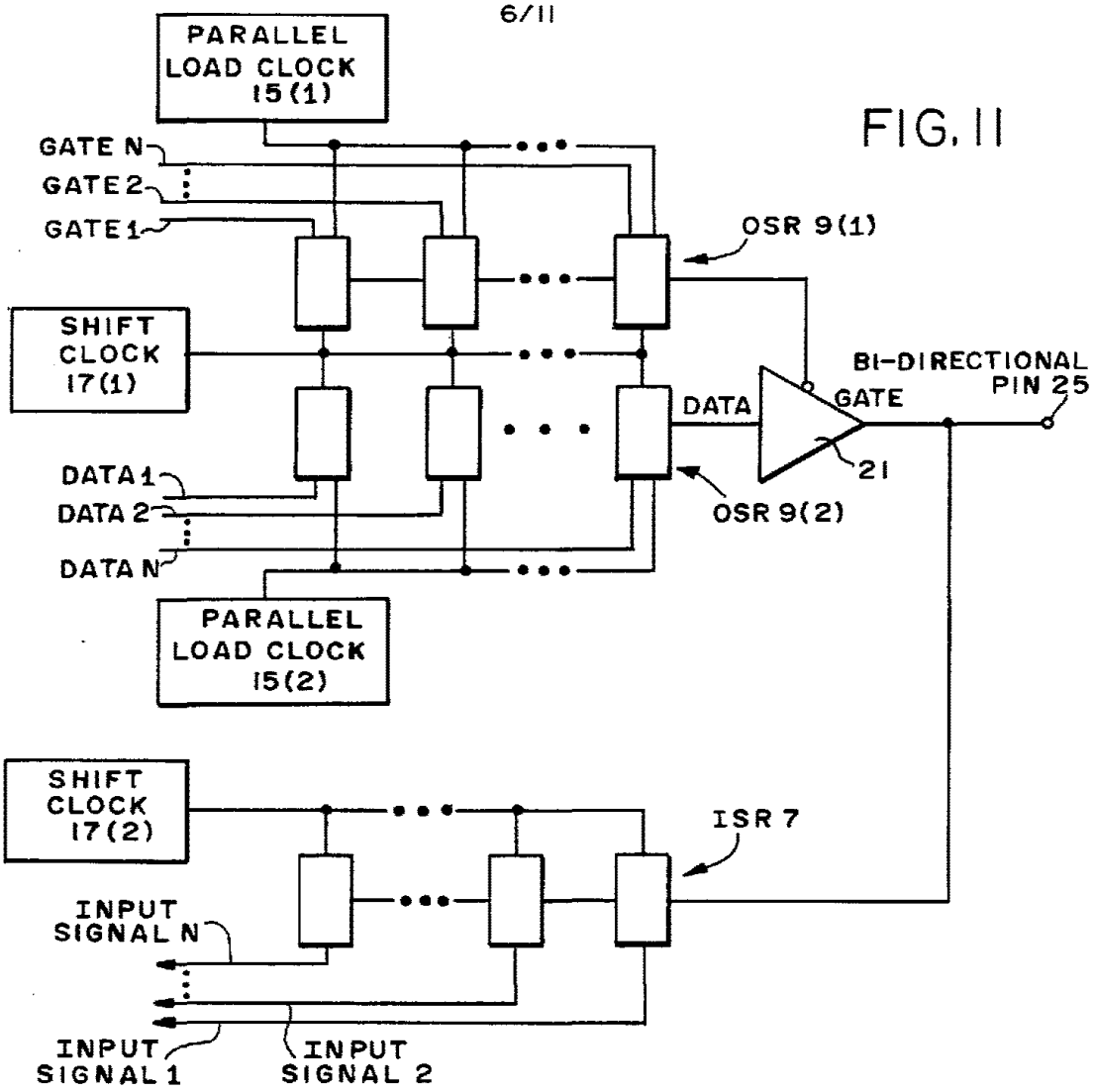

PARALLEL LOAD CLOCK 15(1)
GATE N
GATE 2
GATE 1
OSR 9(1)
SHIFT CLOCK 17(1)
BI-DIRECTIONAL PIN 25
DATA
GATE
21
DATA 1
DATA 2
DATA N
OSR 9(2)
PARALLEL LOAD CLOCK 15(2)
SHIFT CLOCK 17(2)
ISR 7
INPUT SIGNAL N
INPUT SIGNAL 1
INPUT SIGNAL 2

FIG. 11

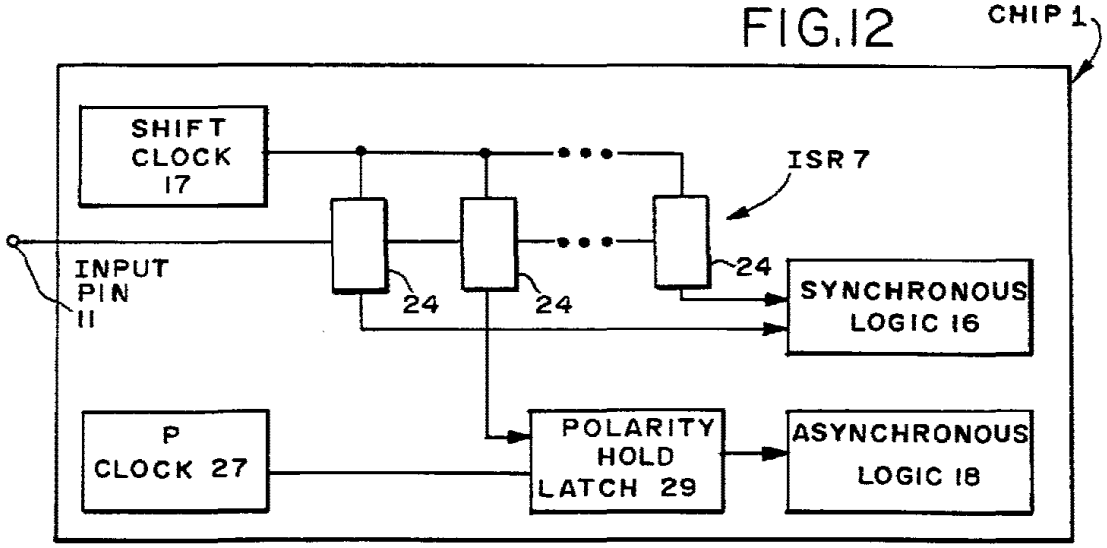

CHIP 1
SHIFT CLOCK 17
ISR 7
INPUT PIN 11
24
24
24
SYNCHRONOUS LOGIC 16
P CLOCK 27
POLARITY HOLD LATCH 29
ASYNCHRONOUS LOGIC 18

FIG. 12

FIG.13

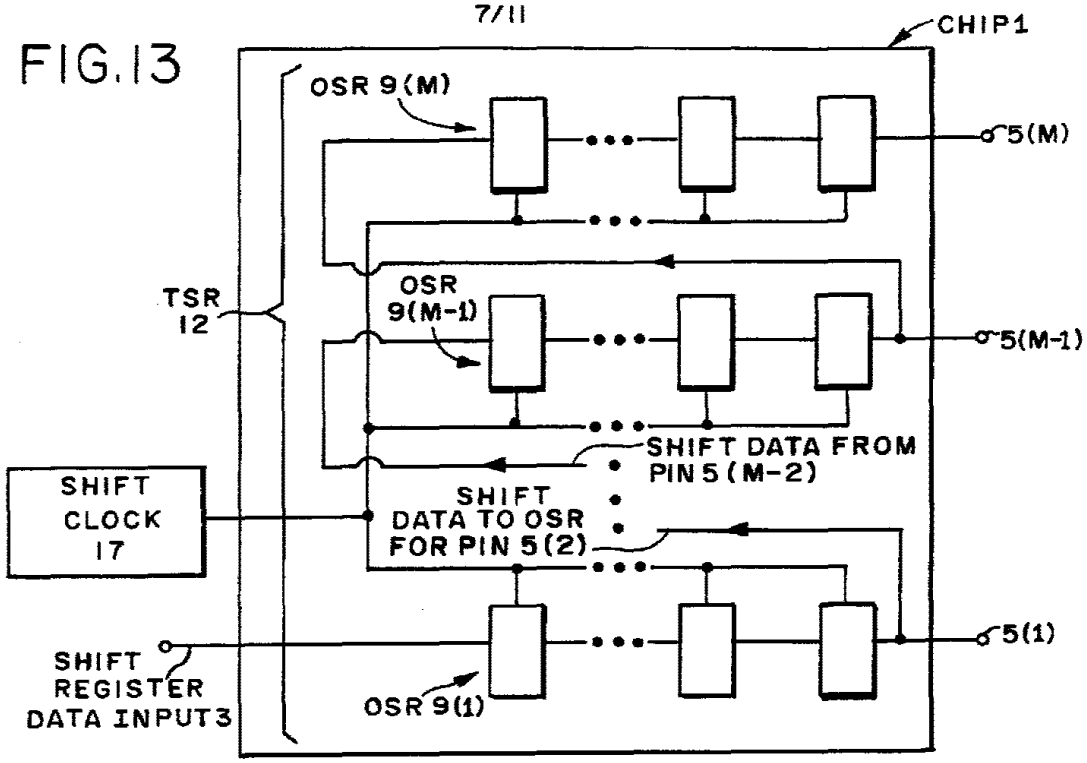

CHIP1
OSR 9(M)
5(M)
TSR
12
OSR
9(M-1)
5(M-1)
SHIFT DATA FROM
PIN 5(M-2)
SHIFT
CLOCK
17
SHIFT
DATA TO OSR
FOR PIN 5(2)
5(1)
SHIFT
REGISTER
DATA INPUT 3
OSR 9(1)

FIG.14

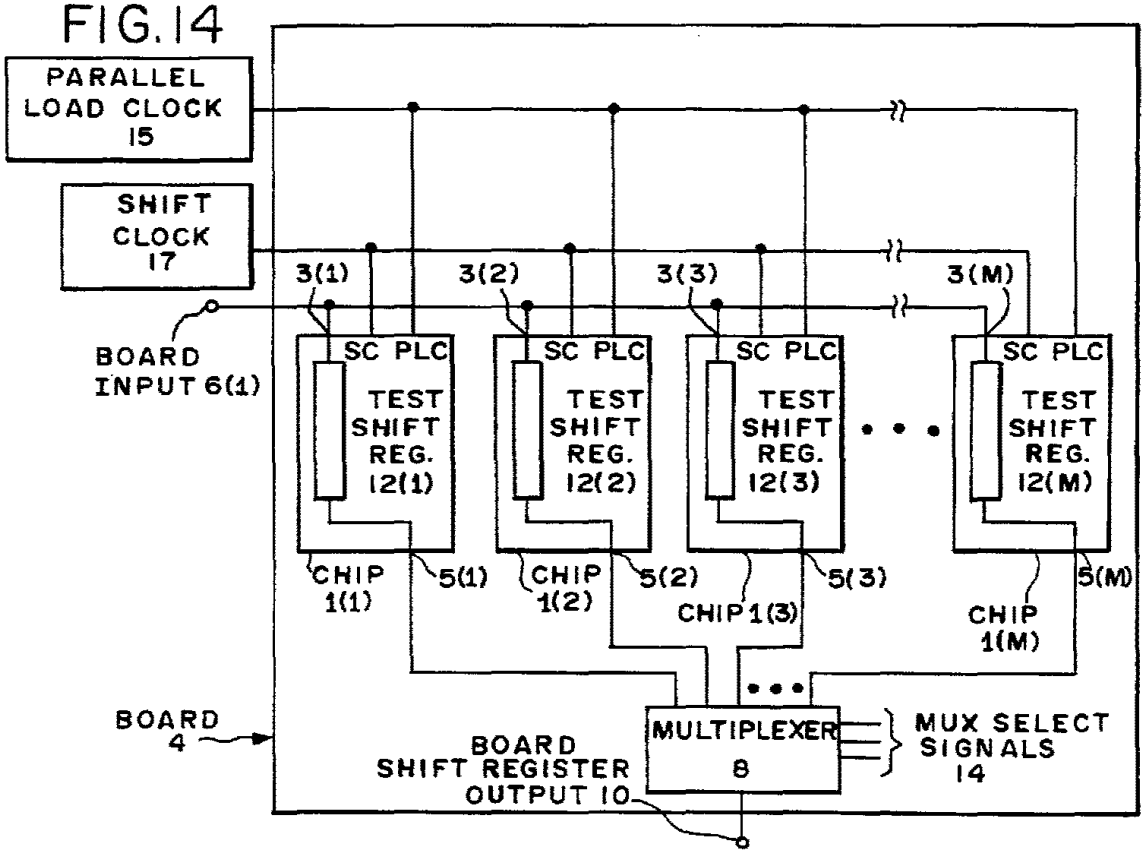

PARALLEL
LOAD CLOCK
15
SHIFT
CLOCK
17
3(1)
3(2)
3(3)
3(M)
BOARD
INPUT 6(1)
SC PLC
TEST
SHIFT
REG.
12(1)
12(2)
12(3)
12(M)
CHIP
1(1)
5(1)
CHIP
1(2)
5(2)
CHIP 1(3)
5(3)
CHIP
1(M)
5(M)
BOARD
4
MULTIPLEXER
8
MUX SELECT
SIGNALS
14
BOARD
SHIFT REGISTER
OUTPUT 10

FIG.15

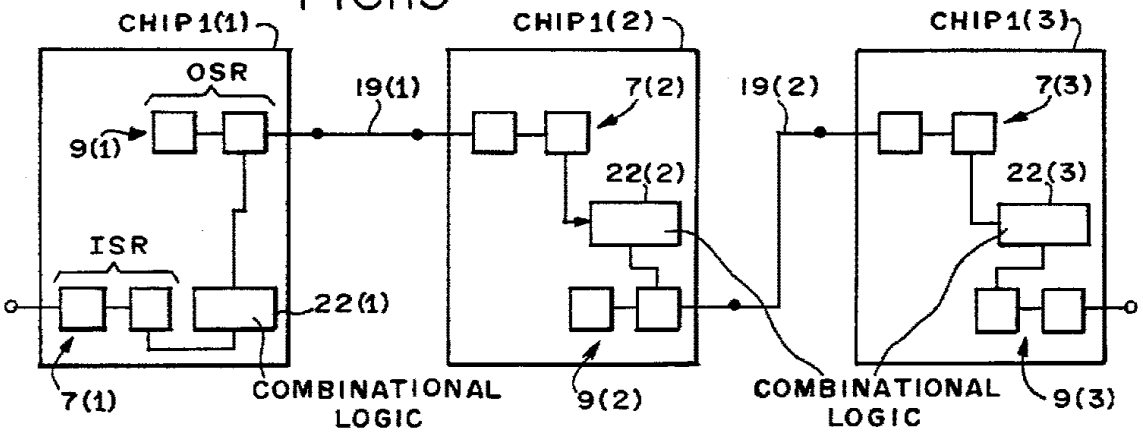


FIG.16

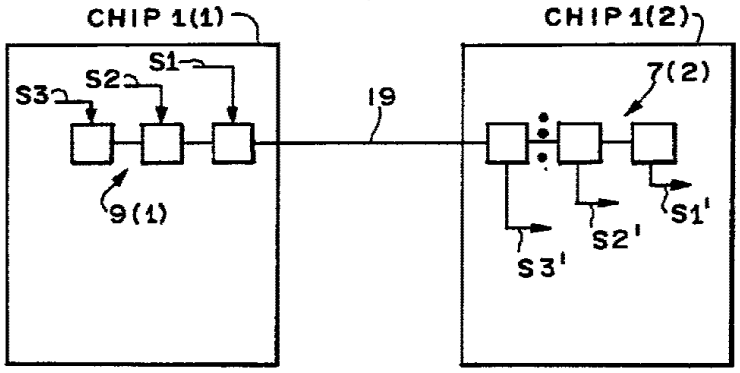


FIG.17

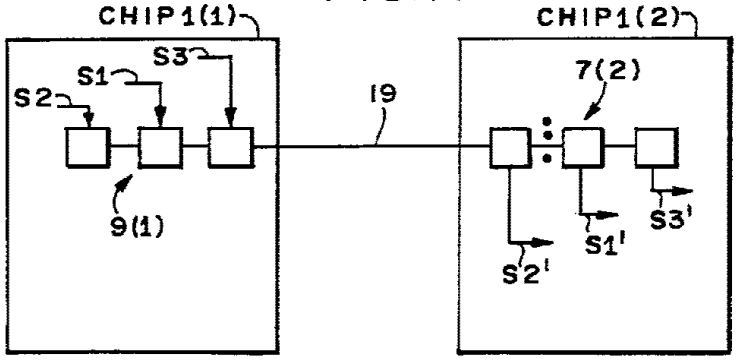
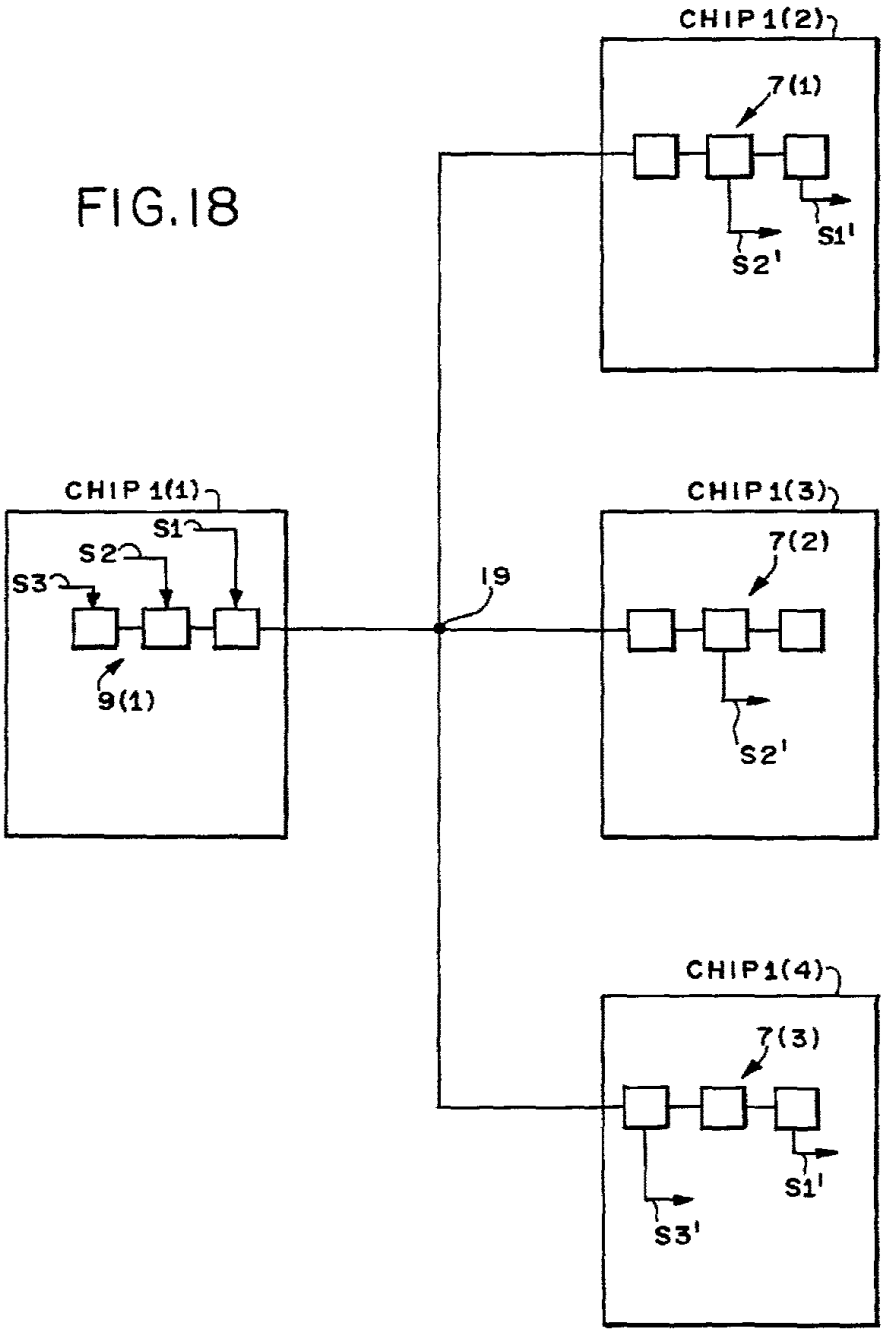


FIG.18


CHIP 1(2)
7(1)
S1'
S2'
CHIP 1(1)
S1
S2
S3
9(1)
19
CHIP 1(3)
7(2)
S2'
CHIP 1(4)
7(3)
S1'
S3'

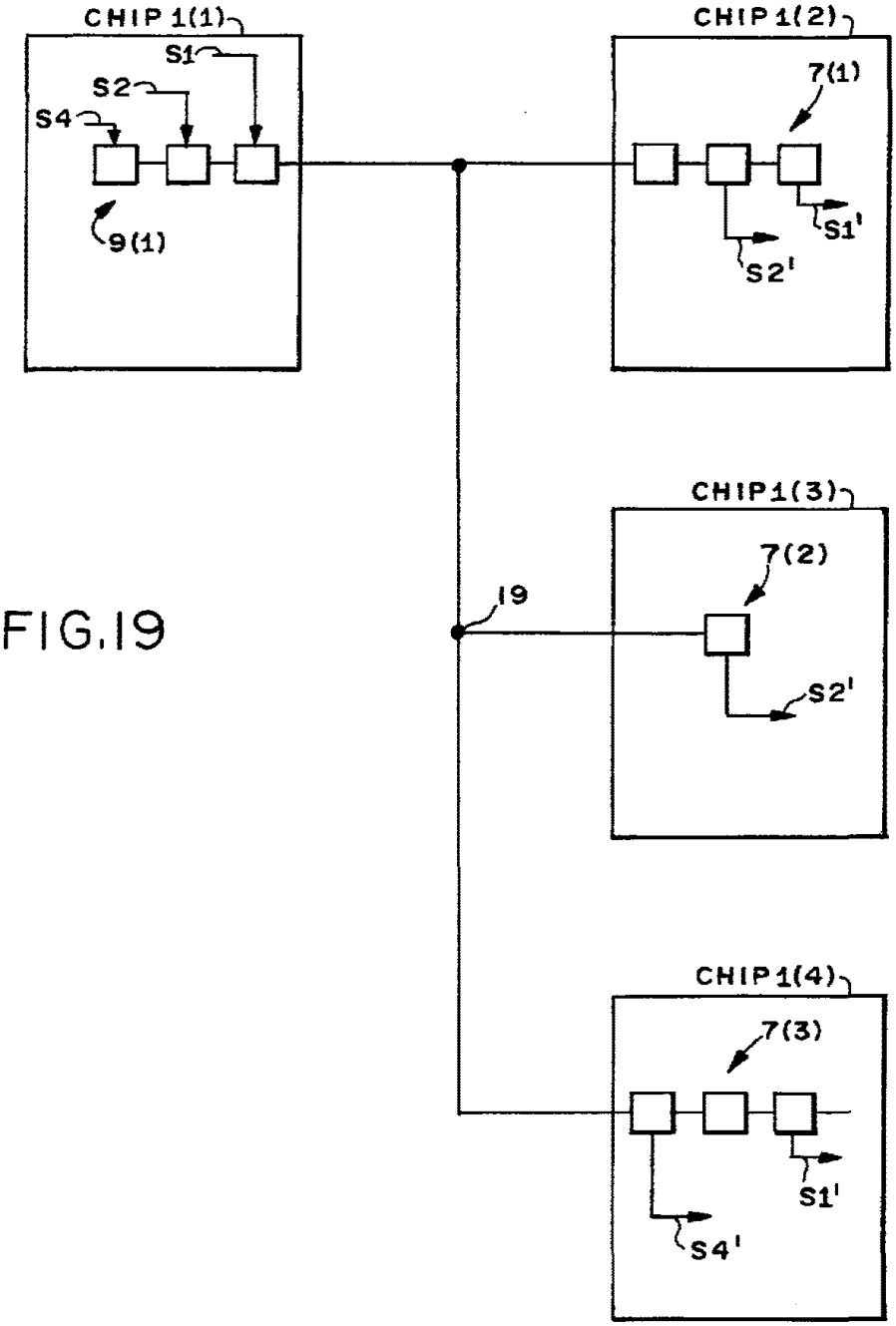

CHIP 1(1)
S1
S2
S4
9(1)
CHIP 1(2)
7(1)
S1'
S2'
CHIP1(3)
7(2)
19
S2'
CHIP1(4)
7(3)
S1'
S4'

FIG.19

FIG.20

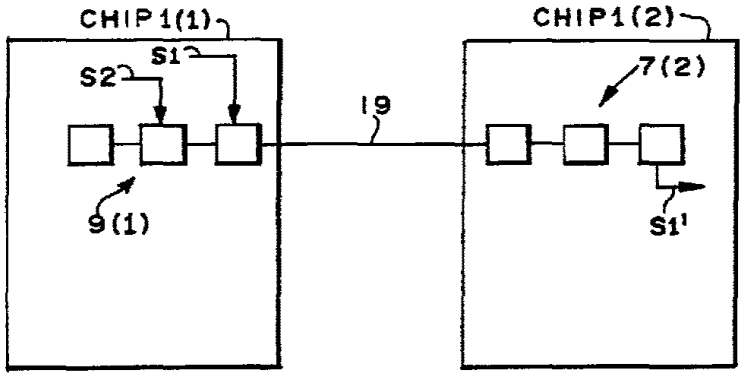


FIG.21

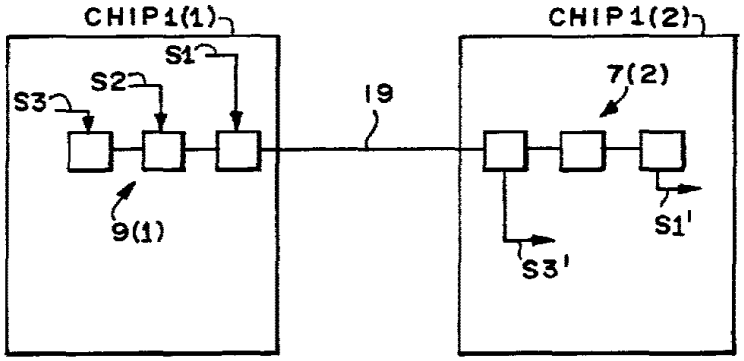
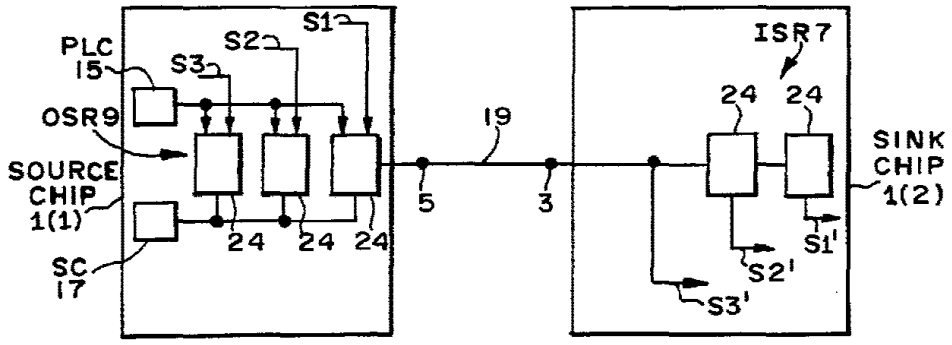


FIG.22



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INTERNATIONAL SEARCH REPORT

International Application No PCT/US 92/07299

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H03K19/173; G06F1/22

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	H03K ; G06F

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
X	MINI MICRO CONFERENCE RECORD May 1984, NEW YORK US pages 1 - 6 STANLEY 'versatile serial protocol for a microcomputer-peripheral interface' see the whole document	1,2,7, 12,13,14
Y	---	3
Y	GB,A,2 164 769 (INTERNATIONAL STANDARD ELECTRIC CORPORATION) 26 March 1986 see the whole document	3
A	---	4
A	PATENT ABSTRACTS OF JAPAN vol. 14, no. 238 (P-1050)21 May 1990 & JP,A,20 58 790 (MITSUBISHI ELECTRIC CORP.) 27 February 1990 see abstract	1,6,7

	-/--	

° Special categories of cited documents :[10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
28 APRIL 1993	1 1. 05. 93
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	FEUER F.S.

Form PCT/ISA/210 (second sheet) (January 1985)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A	EP,A,0 439 199 (ADVANCED MICRO DEVICES INC.) 31 July 1991 see the whole document -----	1,4

Form PCT/ISA/210 (extra sheet) (January 1985)

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO.

US 9207299
SA 64251

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information. 28/04/93

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB-A-2164769	26-03-86	US-A- 4656620	07-04-87
EP-A-0439199	31-07-91	US-A- 4758747	19-07-88
		EP-A- 0247809	02-12-87
		EP-A- 0428504	22-05-91
		JP-A- 63001215	06-01-88
		US-A- 4939391	03-07-90
		US-A- 5168177	01-12-92

EPO FORM P0479

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

Electronic Acknowledgement Receipt

EFS ID:	3505797
Application Number:	11322442
International Application Number:	
Confirmation Number:	5045
Title of Invention:	Multiple chip module and package stacking method for storage devices
First Named Inventor/Applicant Name:	Rey Bruce
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.011
Receipt Date:	24-JUN-2008
Filing Date:	29-DEC-2005
Time Stamp:	03:22:13
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed	6005_011_2dIDS_20080624.pdf	574268 937fdb378af5476d12310508ff96d06196b5c902	no	4
Warnings:					
Information:					

2	Foreign Reference	WO1994006210A1.pdf	695296 11b42930d0b8783f68d73a27278e3c8a9f75f043	no	34
Warnings:					
Information:					
3	NPL Documents	6005_011_PCTUS0662747_ISR_WO.pdf	516323 d5fb87085708ef7d1123e5906e64ec13b0229aea	no	9
Warnings:					
Information:					
			Total Files Size (in bytes):	1785887	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/322,442	12/29/2005	Rey Bruce	6005.011	5045

64180 7590 06/03/2008

URIARTE LAW
257 RODONOVAN DRIVE
SANTA CLARA, CA 95051

EXAMINER	
ULLAH, ELIAS	
ART UNIT	PAPER NUMBER
2892	
MAIL DATE	DELIVERY MODE
06/03/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/322,442	BRUCE ET AL.	
	Examiner	Art Unit	
	ELIAS ULLAH	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2005*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-26* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to an application filed on 12/29/2005

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-13, drawn to a method for stacking a plurality of modules for carrying one or more active signal, classified in class 438, subclass 1+.

   II. Claims 14-26, drawn to a stacked module for carrying one or more active signal, classified in class 257, subclass 686.

The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are related as product and process of use. The inventions can be shown to be distinct if either or both of the following can be shown: (1) the process for using the product as claimed can be practiced with another materially different product or (2) the product as claimed can be used in a materially different process of using that product. See MPEP § 806.05(h). In the instant case the product as claimed can be used in a materially different process such as forming a plurality of modules putting them side by side instead of stacking.

Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and examination burden if restriction were not required because one or more of the following reasons apply:

(a) the inventions have acquired a separate status in the art in view of their different classification;

(b) the inventions have acquired a separate status in the art due to their recognized divergent subject matter;

(c) the inventions require a different field of search (for example, searching different classes/subclasses or electronic resources, or employing different search queries);

(d) the prior art applicable to one invention would not likely be applicable to another invention;

(e) the inventions are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention**.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected invention.

If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

Conclusion

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ELIAS ULLAH whose telephone number is (571)272-1415. The examiner can normally be reached on weekdays, between 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Elias Ullah/
Examiner, Art Unit 2892

/Thao X Le/
Supervisory Patent Examiner, Art Unit 2892

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11322442	BRUCE ET AL.
	Examiner	Art Unit
	ELIAS ULLAH	2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/23/2008								
	1	÷								
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PTO/SB/08a (03-08)
Approved for use through 03/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11322442
	Filing Date	2005-12-29
	First Named Inventor	Rey H. Bruce
	Art Unit	2811
	Examiner Name	
	Attorney Docket Number	6005.011

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
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NON-PATENT LITERATURE DOCUMENTS			Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11322442
	Filing Date	2005-12-29
	First Named Inventor	Rey H. Bruce
	Art Unit	2811
	Examiner Name	
	Attorney Docket Number	6005.011

	1	JEFFREY C. DEMMIN, Novel 3-D Packaging Approaches Simplifying the Assembly and Test Supply Chain, Business Briefing: Global Semiconductor Manufacturing Technology, 2003, pp. 1-5	☒
	2	MOODY DREIZA, AKITO YOSHIDA, JONATHAN MICKSCH AND LEE SMITH, Stacked Package-on-Package Design Guideliness, Chip Scale Review, July 2005, pp.1-4, Reprinted by Amkor Technology, Inc. Chandler, Arizona	☒

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	11322442
	Filing Date	2005-12-29
	First Named Inventor	Rey H. Bruce
	Art Unit	2811
	Examiner Name	
	Attorney Docket Number	6005.011

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Stephen R. Uriarte/	Date (YYYY-MM-DD)	2008-03-17
Name/Print	Stephen R. Uriarte	Registration Number	40,854

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	3013248
Application Number:	11322442
International Application Number:	
Confirmation Number:	5045
Title of Invention:	Multiple chip module and package stacking method for storage devices
First Named Inventor/Applicant Name:	Rey Bruce
Customer Number:	64180
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	6005.011
Receipt Date:	18-MAR-2008
Filing Date:	29-DEC-2005
Time Stamp:	00:57:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed	6005_011_1stIDS_20080317.pdf	574084 a22f5ab18bf2384230de811deb8ee80edf0631ce	no	4
Warnings:					
Information:					

A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.

2	NPL Documents	6005_011_NPL1_Tessera_Novel_3D_Packaging_Approaches.pdf	1515562 6c5bbc259c42792eade5a322f7747ab01d92fd82	no	5
Warnings:					
Information:					
3	NPL Documents	6005_016_NPL2_AMKOR_Stacked_Package_on_Package.pdf	363087 b160ac1c7cd7bddaa6f29e5c24daf0f9e400cc93	no	4
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		Total Files Size (in bytes):	2452733		

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New Applications Under 35 U.S.C. 111
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National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/322,442	12/29/2005	Rey Bruce	6005.011

CONFIRMATION NO. 5045

64180
URIARTE LAW
257 RODONOVAN DRIVE
SANTA CLARA, CA95051

Title: Multiple chip module and package stacking method for storage devices

Publication No. US-2007-0158808-A1
Publication Date: 07/12/2007

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Pre-Grant Publication Division, 703-605-4283

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/322,442	12/29/2005	Rey Bruce	6005.011

CONFIRMATION NO. 5045

64180
URIARTE LAW
257 RODONOVAN DRIVE
SANTA CLARA, CA95051

Title: Multiple chip module and package stacking method for storage devices

Publication No. US-2007-0158808-A1
Publication Date: 07/12/2007

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

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Pre-Grant Publication Division, 703-605-4283

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/322,442	12/29/2005	Rey Bruce	6005.011

CONFIRMATION NO. 5045

64180
URIARTE LAW
257 RODONOVAN DRIVE
SANTA CLARA, CA95051

Date Mailed. 12/14/2006

NOTICE OF NEW OR REVISED PROJECTED PUBLICATION DATE

The above-identified application has a new or revised projected publication date. The current projected publication date for this application is 07/05/2007. If this is a new projected publication date (there was no previous projected publication date), the application has been cleared by Licensing & Review or a secrecy order has been rescinded and the application is now in the publication queue.

If this is a revised projected publication date (one that is different from a previously communicated projected publication date), the publication date has been revised due to processing delays in the USPTO or the abandonment and subsequent revival of an application. The application is anticipated to be published on a date that is more than six weeks different from the originally-projected publication date.

More detailed publication information is available through the private side of Patent Application Information Retrieval (PAIR) System. The direct link to access PAIR is currently http://pair.uspto.gov. Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at (703) 305-3028.

Questions relating to this Notice should be directed to the Office of Patent Publication at (703) 305-8283.

PART 1 - ATTORNEY/APPLICANT COPY

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/322,442	12/29/2005	Rey Bruce	6005.011

CONFIRMATION NO. 5045

Fernandez & Associates, LLP
PO Box D
Menlo Park, CA 94025-6204

OC000000021612999

Date Mailed: 12/14/2006

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/07/2006.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

HUAN LE
PTOSS (703) 308-9150 EXT 149

OFFICE COPY

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/322,442	12/29/2005	Rey Bruce	6005.011

CONFIRMATION NO. 5045

64180
URIARTE LAW
257 RODONOVAN DRIVE
SANTA CLARA, CA 95051

OC000000021613030

Date Mailed: 12/14/2006

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/07/2006.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

HUAN LE
PTOSS (703) 308-9150 EXT 149

OFFICE COPY

POWER OF ATTORNEY and CORRESPONDENCE ADDRESS INDICATION FORM

Application Number	11/322,442
Filing Date	December 29, 2005
First Named Inventor	Rey Bruce, et al.
Title	Multiple Chip Module & Package Stacking...
Art Unit	2811
Examiner Name	Not Yet Assigned
Attorney Docket Number	6005.011

I hereby revoke all previous powers of attorney given in the above-identified application.

I hereby appoint:

☒ Practitioners associated with the Customer Number: 64180

OR

☐ Practitioner(s) named below:

Name	Registration Number
Stephen R. Uriarte	40,854

as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

Please recognize or change the correspondence address for the above-identified application to:

☒ The address associated with the above-mentioned Customer Number:

OR

☐ The address associated with Customer Number: 64180

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the:

☐ Applicant/Inventor.

☒ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

SIGNATURE of Applicant or Assignee of Record

Signature	Rey H Bruce	Date	11-30-06
Name	Rey H. Bruce	Telephone	510.377.8876
Title and Company	Chairman & CEO		

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒ *Total of 1 forms are submitted.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: BiTMICRO Networks, Inc.

Application No./Patent No./Control No.: 11/322,442 Filed/Issue Date: December 29, 2005

Entitled: MULTIPLE CHIP MODULE AND PACKAGE STACKING METHOD FOR STORAGE DEVICES

BiTMICRO Networks, Inc., a Corporation
(Name of Assignee) (Type of Assignee: corporation, partnership, university, government agency, etc.)

states that it is:

1. [X] the assignee of the entire right, title, and interest; or

2. [ ] an assignee of less than the entire right, title and interest
(The extent (by percentage) of its ownership interest is _____%)

in the patent application/patent identified above by virtue of either:

A. [X] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or a true copy of the original assignment is attached.

OR

B. [ ] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet.

As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Rev H Bruce — Signature

11-30-06 — Date

Rev H. Bruce — Printed or Typed Name

510.623.2341 — Telephone Number

Chairman & Chief Executive Officer — Title

ASSIGNMENT

For good and valuable consideration, the receipt of which is hereby acknowledged, the person(s) named below (referred to as "INVENTOR" whether singular or plural) has sold, assigned, and transferred and does hereby sell, assign, and transfer to **BiTMICRO Networks, Inc., a California corporation, having a place of business at 47929 Fremont Blvd., Fremont, CA 94538** ("ASSIGNEE"), for itself and its successors, transferees, and assignees, the following:

1. The entire worldwide right, title, and interest in all inventions and improvements ("SUBJECT MATTER") that are disclosed in the application for United States Letters Patent entitled: **Multiple Chip Module and Package Stacking Method for Storage Devices** ("APPLICATION"), which:

☐ is to be filed herewith

☒ was filed on **December 29, 2005**, now bearing U.S. serial number **11/322,442** and for which a Declaration was executed by INVENTOR on the date(s) below; and

2. The entire worldwide right, title, and interest in and to: (a) the APPLICATION, including any right of priority; (b) any divisional, continuation, substitute, renewal, reissue, and other related applications thereto which have been or may be filed in the United States or elsewhere in the world; and (c) any patents which may be granted on the applications set forth in (a) and (b) above.

INVENTOR agrees that ASSIGNEE may apply for and receive patents for SUBJECT MATTER in ASSIGNEE's own name.

INVENTOR agrees to do the following, when requested, and without further consideration, in order to carry out the intent of this Assignment: (1) execute all oaths, assignments, powers of attorney, applications, and other papers necessary or desirable to fully secure to ASSIGNEE the rights, titles and interests herein conveyed; (2) communicate to ASSIGNEE all known facts relating to the SUBJECT MATTER; and (3) generally do all lawful acts that ASSIGNEE shall consider desirable for securing, maintaining, and enforcing worldwide patent protection relating to the SUBJECT MATTER and for vesting in ASSIGNEE the rights, titles, and interests herein conveyed. INVENTOR further agrees to provide any successor, assign, or legal representative of ASSIGNEE with the benefits and assistance provided to ASSIGNEE hereunder.

INVENTOR represents that INVENTOR has the rights, titles, and interests to convey as set forth herein, and covenants with ASSIGNEE that the INVENTOR has made or will make hereafter no assignment, grant, mortgage, license, or other agreement affecting the rights, titles, and interests herein conveyed.

INVENTOR grants the attorney of record the power to insert on this Assignment any further identification which may be necessary or desirable in order to comply with the rules of the United States Patent and Trademark Office for recordation of this document.

Title of Document:	ASSIGNMENT
In Re Application of:	Bruce et al.
Title:	Multiple Chip Module and Package Stacking Method for Storage Devices
Filed: (if applicable)	December 29, 2005
Serial No.: (if applicable)	11/322,442

This Assignment may be executed in one or more counterparts, each of which shall be deemed an original and all of which may be taken together as one and the same Assignment.

Inventor Signature	Date of Signature	Date Invention Declaration Signed by Inventor
Printed Name: Rey H. Bruce	_____, 2006	December 20, 2005
Printed Name: Ricardo H. Bruce	NOVEMBER 28, 2006	December 20, 2005
Printed Name: Patrick Digamon Bugayong	NOVEMBER 28, 2006	December 20, 2005
Printed Name: Joel Alonzo Baylon	NOVEMBER 28, 2006	December 20, 2005

ASSIGNMENT

For good and valuable consideration, the receipt of which is hereby acknowledged, the person(s) named below (referred to as "INVENTOR" whether singular or plural) has sold, assigned, and transferred and does hereby sell, assign, and transfer to **BiTMICRO Networks, Inc., a California corporation, having a place of business at 47929 Fremont Blvd., Fremont, CA 94538** ("ASSIGNEE"), for itself and its successors, transferees, and assignees, the following:

1. The entire worldwide right, title, and interest in all inventions and improvements ("SUBJECT MATTER") that are disclosed in the application for United States Letters Patent entitled: **Multiple Chip Module and Package Stacking Method for Storage Devices** ("APPLICATION"), which:

☐ is to be filed herewith

☒ was filed on **December 29, 2005**, now bearing U.S. serial number **11/322,442** and for which a Declaration was executed by INVENTOR on the date(s) below; and

2. The entire worldwide right, title, and interest in and to: (a) the APPLICATION, including any right of priority; (b) any divisional, continuation, substitute, renewal, reissue, and other related applications thereto which have been or may be filed in the United States or elsewhere in the world; and (c) any patents which may be granted on the applications set forth in (a) and (b) above.

INVENTOR agrees that ASSIGNEE may apply for and receive patents for SUBJECT MATTER in ASSIGNEE's own name.

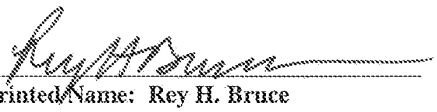
INVENTOR agrees to do the following, when requested, and without further consideration, in order to carry out the intent of this Assignment: (1) execute all oaths, assignments, powers of attorney, applications, and other papers necessary or desirable to fully secure to ASSIGNEE the rights, titles and interests herein conveyed; (2) communicate to ASSIGNEE all known facts relating to the SUBJECT MATTER; and (3) generally do all lawful acts that ASSIGNEE shall consider desirable for securing, maintaining, and enforcing worldwide patent protection relating to the SUBJECT MATTER and for vesting in ASSIGNEE the rights, titles, and interests herein conveyed. INVENTOR further agrees to provide any successor, assign, or legal representative of ASSIGNEE with the benefits and assistance provided to ASSIGNEE hereunder.

INVENTOR represents that INVENTOR has the rights, titles, and interests to convey as set forth herein, and covenants with ASSIGNEE that the INVENTOR has made or will make hereafter no assignment, grant, mortgage, license, or other agreement affecting the rights, titles, and interests herein conveyed.

INVENTOR grants the attorney of record the power to insert on this Assignment any further identification which may be necessary or desirable in order to comply with the rules of the United States Patent and Trademark Office for recordation of this document.

Title of Document:	**ASSIGNMENT**
In Re Application of:	Bruce et al.
Title:	Multiple Chip Module and Package Stacking Method for Storage Devices
Filed: (if applicable)	December 29, 2005
Serial No.: (if applicable)	11/322,442

This Assignment may be executed in one or more counterparts, each of which shall be deemed an original and all of which may be taken together as one and the same Assignment.

Inventor Signature	Date of Signature	Date Invention Declaration Signed by Inventor
	11-30, 2006	December 20, 2005
Printed Name: Rey H. Bruce		
Inventor Signature	**Date of Signature**	**Date Invention Declaration Signed by Inventor**
	, 2006	December 20, 2005
Printed Name: Ricardo H. Bruce		
Inventor Signature	**Date of Signature**	**Date Invention Declaration Signed by Inventor**
	, 2006	December 20, 2005
Printed Name: Patrick Digamon Bugayong		
Inventor Signature	**Date of Signature**	**Date Invention Declaration Signed by Inventor**
	, 2006	December 20, 2005
Printed Name: Joel Alonzo Baylon		

Electronic Acknowledgement Receipt	
EFS ID:	1357581
Application Number:	11322442
International Application Number:	
Confirmation Number:	5045
Title of Invention:	Multiple chip module and package stacking method for storage devices
First Named Inventor/Applicant Name:	Rey Bruce
Correspondence Address:	Fernandez & Associates, LLP - PO Box D - Menlo Park CA 94025-6204 US 6503251203 -
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	BIT-P009
Receipt Date:	07-DEC-2006
Filing Date:	29-DEC-2005
Time Stamp:	02:18:13
Application Type:	Utility

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	6005_011_POA_20061206.pdf	536908	no	1
Warnings:					
Information:					
2	Assignee showing of ownership per 37 CFR 3.73(b).	6005_011_3_73b_Sttmnt_20061206.pdf	526605	no	1
Warnings:					
Information:					
3	Assignee showing of ownership per 37 CFR 3.73(b).	6005_011_Assign1_20061127.pdf	351935	no	2
Warnings:					
Information:					
4	Assignee showing of ownership per 37 CFR 3.73(b).	6005_011_Assign2_20061206.pdf	988999	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2404447		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: BRUCE et al.	Group Art Unit: Not Yet Assigned
Serial No.: 11/322,442	Examiner: Not Yet Assigned
Confirmation No.: 5045	
Filed: 29 December 2005	
For: MULTIPLE CHIP MODULE AND PACKAGE STACKING METHOD FOR STORAGE DEVICES	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ATTORNEY DOCKET NUMBER CHANGE REQUEST

Dear Sir/Madam:

Please accept this request to change the attorney docket number for the above-referred patent application from BIT-P009 to 6005.011. A power of attorney and correspondence address indication form for the undersigned has been filed with this Office on 6 December 2006.

Respectfully submitted,

Dated: 6 December 2006

/Stephen R. Uriarte/
Stephen R. Uriarte, Reg. No. 40,854

Customer Number: 000064180

Mailing Address
Uriarte Law
257 Rodonovan Dr., Suite 100
Santa Clara, CA 95051
Tel: 408.876.4470
Fax: 408.716.2651
Email: stephen@uriartelaw.com

Electronic Acknowledgement Receipt	
EFS ID:	1357584
Application Number:	11322442
International Application Number:	
Confirmation Number:	5045
Title of Invention:	Multiple chip module and package stacking method for storage devices
First Named Inventor/Applicant Name:	Rey Bruce
Correspondence Address:	Fernandez & Associates, LLP - PO Box D - Menlo Park CA 94025-6204 US 6503251203 -
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	BIT-P009
Receipt Date:	07-DEC-2006
Filing Date:	29-DEC-2005
Time Stamp:	02:32:07
Application Type:	Utility

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	6005_011_Req2ChngDocket_20061206.pdf	23150	no	1
Warnings:					
Information:					
		Total Files Size (in bytes):	23150		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

PTO/SB/36 (09-06)
Approved for use through 03/31/2007. OMB 0651-0031
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

RESCISSION OF PREVIOUS NONPUBLICATION REQUEST
(35 U.S.C. 122(b)(2)(B)(ii))
AND, IF APPLICABLE,
NOTICE OF FOREIGN FILING
(35 U.S.C. 122(b)(2)(B)(iii))

Send completed form to:
Mail Stop PG Pub
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
FAX: (571) 273-8300

Application Number	11/322,442
Filing Date	December 29, 2005
First Named Inventor	Rey H. Bruce
Title	Multiple Chip Module & Package Stacking...
Atty Docket Number	6005.011
Art Unit	2811
Examiner	Not Yet Assigned

A request that the above-identified application not be published under 35 U.S.C. 122(b) (nonpublication request) was included with the above-identified application on filing pursuant to 35 U.S.C. 122(b)(2)(B)(i).
I hereby **rescind** the previous nonpublication request.

If a notice of foreign or international filing is or will be required by 35 U.S.C. 122(b)(2)(B)(iii) and 37 CFR 1.213(c), I hereby provide such notice. This notice is being provided no later than forty-five (**45**) days after the date of such foreign or international filing.

*If a notice of subsequent foreign or international filing required by 35 U.S.C. 122(b)(2)(B)(iii) and 37 CFR 1.213(c) was not filed within forty-five (**45**) days after the date of filing of the foreign or international application, the application is ABANDONED, and a petition to revive under 37 CFR 1.137(b) is required. See 37 CFR 1.137(f).*

/Stephen R. Uriarte/ — Signature
07 December 2006 — Date

Stephen R. Uriarte — Typed or printed name
40,874 — Registration Number, if applicable

408.874.4476 — Telephone Number

This request must be signed in compliance with 37 CFR 1.33(b).

If information or assistance is needed in completing this form, please contact the Pre-Grant Publication Division at (703)605-4283 or by e-mail at PGPub@USPTO.gov.

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop PG Pub, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature

Name (Print/Type) | Date

This collection of information is required by 37 CFR 1.213(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop PG Pub, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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Electronic Acknowledgement Receipt	
EFS ID:	1357592
Application Number:	11322442
International Application Number:	
Confirmation Number:	5045
Title of Invention:	Multiple chip module and package stacking method for storage devices
First Named Inventor/Applicant Name:	Rey Bruce
Correspondence Address:	Fernandez & Associates, LLP - PO Box D - Menlo Park CA 94025-6204 US 6503251203 -
Filer:	Stephen Radcliff Uriarte
Filer Authorized By:	
Attorney Docket Number:	BIT-P009
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Application Type:	Utility

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Rescind Nonpublication Request for Pre Grant Pub	6005_011_RscdNonPub.pdf	205125	no	2
Warnings:					
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
11/322,442	12/29/2005	Rey Bruce	6005.011

CONFIRMATION NO. 5045

Fernandez & Associates, LLP
PO Box D
Menlo Park, CA 94025-6204

Date Mailed: 12/07/2006

Communication Regarding Rescission Of Nonpublication Request and/or Notice of Foreign Filing

Applicant's rescission of the previously-filed nonpublication request and/or notice of foreign filing is acknowledged. The paper has been reflected in the Patent and Trademark Office's (USPTO's) computer records so that the earliest possible projected publication date can be assigned.

The projected publication date is 07/05/2007.

If applicant rescinded the nonpublication request before or on the date of "foreign filing,"[1] then no notice of foreign filing is required.

If applicant foreign filed the application after filing the above application and before filing the rescission, and the rescission did not also include a notice of foreign filing, then a notice of foreign filing (not merely a rescission) is required to be filed within 45 days of the date of foreign filing. See 35 U.S.C. § 122(b)(2)(B)(iii), and Clarification of the United States Patent and Trademark Office's Interpretation of the Provisions of 35 U.S.C. § 122(b)(2)(B)(ii)-(iv), 1272 Off. Gaz. Pat. Office 22 (July 1, 2003).

If a notice of foreign filing is required and is not filed within 45 days of the date of foreign filing, then the application becomes abandoned pursuant to 35 U.S.C. § 122(b)(2)(B)(iii). In this situation, applicant should either file a petition to revive or notify the Office that the application is abandoned. See 37 CFR 1.137(f). Any such petition to revive will be forwarded to the Office of Petitions for a decision. Note that the filing of the petition will not operate to stay any period of reply that may be running against the application.

Questions regarding petitions to revive should be directed to the Office of Petitions at (571) 272-3282. Questions regarding publications of patent applications should be directed to the patent application publication hotline at (703) 605-4283 or by e-mail pgpub@uspto.gov.

[1] Note, for purpose of this notice, that "foreign filing" means "filing an application directed to the same invention in another country, or under a multilateral international agreement, that requires publication of applications 18 months after filing".

17667 U.S. PTO
122905

112974 U.S. PTO
11/322442
122905

The Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Re: U.S. Utility Patent Application
Appl. No. (Not yet assigned); Filed _12/29/2005_
For: **Multiple Chip Module and Package Stacking Method For Storage Devices**
Inventor(s): **Bruce, et al.**
Docket No.: **BIT-P009**

Sir:
The following documents are forwarded herewith for action by the U.S. Patent and Trademark Office:

1. U.S. UTILITY APPLICATION
   entitled: **Multiple Chip Module and Package Stacking Method For Storage Devices**
   having named inventor(s):
   Bruce, et al.
   a. a specification consisting:
      (i) _24_ pages prior to the claims, including title page;
      (ii) _10__ pages of claims;
      (iii) _1_page abstract;
   b. __28__ sheets of drawings: (FIGs. 1a, 1b, 2a,2b,2c, 3a, 3b, 3c, 4a, 4b, 5a, 5b, 6a, 6b, 7a, 7b, 8a, 8b, 9, 10, 11, 12a, 12b, 13, 14, 15a, 15b, 16, 17a, 17b, 18, 19, 20a, 20b, 21a, 21b);
2. An **executed** Combined Declaration and Power of Attorney by named inventors;
3. Form PTO-1082 (in duplicate);
4. Request and Certification Form PTO/SB/35 (11-00);
5. Check No. ___1480_____ For $ _690.00__ to cover:

Basic Application Fee:	$ 150.00
Utility Search Fee:	$ 250.00
Utility Examination Fee:	$ 100.00
Assignment Recordation fee:	$ 40.00
Excess claims fee:	$ 150 .00

6. Application Data Sheet(__6__ sheets); and
7. A return post card

It is respectfully requested that the attached postcard be stamped with the filing date of the above documents and unofficial application number and returned to the addressee as soon as possible.

12/29/05
Date

Respectfully submitted,

DENNIS S. FERNANDEZ, ESQ
Reg. No. 34,160

FERNANDEZ & ASSOCIATES, LLP
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The PTO did not receive the following listed item(s) Assignment Recordal Sheet

122905 17667 U.S. PTO

Certificate of Mailing By "U.S. Express Mail" Under 37 C.F.R. 1.10(c)
"EXPRESS MAIL" Mailing Label Number: EV749607634US Date of Deposit: 12/29/05
I hereby certify that this paper and/or fee is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to the Commissioner For Patents, P.O. Box 1450, Alexandria 22313-1450

Name: Chris Vo
Signature
12/29/05
Date

Docket No.: BIT-P009

APPLICATION TRANSMITTAL LETTER

Commissioner for Patents
P.O. Box 1450.
Alexandria, VA 22313-1450

Sir:
Transmitted herewith for filing is the patent application of
Inventor(s): **Bruce, et al.**
Entitled: **"Multiple Chip Module and Package Stacking Method For Storage Devices"**

35 No. pages of specification, including title page, claims and abstract
28 No. sheets of drawings

Also enclosed are:
X Executed Combined Declaration and Power of Attorney for Patent Application
___ An Original Executed Assignment of the Application
___ Form PTO-1595 (Recordation Cover Sheet for Assignment)
X Request and Certification Form PTO/SB/35 (11-00)
X Application Data Sheet (6 sheets)
___ An Information Disclosure Statement (Form PTO/SB/08A and Form PTO/SB/08B)
___ A copy of References cited in Information Disclosure: _____ documents

If a continuing application:
___Continuation ___Divisional ____Continuation-in-part ___of prior application No.:
Prior application examiner:
Prior application art unit:

FEES DUE
X Applicant Claims Small Entity Status (37 CFR 1.27)

The fees due for filing the application pursuant to 37 C.F.R. 1.16 and for recording the Assignment, if any, are determined as follow:

CLAIMS					
	No. of Claims		Extra Claims	Rate	Fees
Basic Application Fee ($300.00 large entity; $150.00 small entity)					$ 150.00
Utility Application Size Fee – for each additional 50 sheets that exceeds 100 sheets ($250 large entity; $125 small entity)					.00
Utility Search Fee ($500.00 large entity; $250.00 small entity)					$250.00

Repln. Ref: 01/05/2006 YPOLITE1 0012082400
DA#:500482 Name/Number:11322442
FC: 9204 $40.00 CR

Utility Examination Fee ($200.00 large entity; $100.00 small entity)					$100.00
Total Claims	26	Minus 20 =	6	X $50 = X $ 25 (small) =	150.00
Total Independent Claims	2	Minus 3 =	0	X $200 = X $100 (small) =	.00
If Multiple Dependent Claims are presented, add $360.00 or $180.00(small)					
If Assignment enclosed, add Assignment Recording Fee $40.00					40.00
TOTAL APPLICATION FEE DUE					$ 690.00

PAYMENT OF FEES
The full fee due in connection with this communication is $ 690.00
and is provided as follows:

____ The Commissioner is hereby authorized to charge the fees associated with this communication or credit any overpayment to **Deposit Account No: 500482**. A duplicate copy of this authorization is enclosed.

__X__ A Check No. __1480__ for the above-specified full fee is enclosed. However, in case Applicant inadvertently miscalculated any required fee, the Commissioner is hereby authorized to charge the necessary additional amount associated with this communication or credit any overpayment to **Deposit Account No: 500482**. A duplicate copy of this authorization is enclosed.

NO 18 MONTHS PUBLICATION

REQUEST AND CERTIFICATION UNDER 35. U.S.C. 122(b) (2) (B) (i)

__X__ I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen month after filing. **I hereby request that the attached application not to be published under 35 U.S.C. 122(b).**

This application is filed pursuant to 37 C.F.R. 1.53 in the name of the above-identified Inventor(s).

Please direct all correspondence concerning the above-identified application to the following Custom Number and Address:

Customer No: 22877

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Respectfully submitted,

DENNIS S. FERNANDEZ, ESQ
Reg. No. 34,160

12/29/05
Date

Application

For

United States Non-Provisional Utility Patent

Title:

Multiple Chip Module and Package Stacking Method For Storage Devices

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Multiple Chip Module and Package Stacking Method For Storage Devices

BACKGROUND

Field

The present invention relates to computer systems. More particularly, the present invention relates to flash memory based semiconductor disk drive and a method of using multiple chip module (MCM) and Package Stacking technique to support miniaturization and memory scalability.

Description of Related Art

Flash memory based semiconductor disk drive typically use separate packages for the interface controller, the DMA controller, the processor and separate packages for the Flash devices, the FPROMs and the RAMs. This current method limits the miniaturization of the entire storage device. In order to achieve the move to miniaturization, chip modules and packages need to be stacked. Stacking both on chip module and package level maximizes the capacity in a limited area thus realizing the move to miniaturize the entire storage device. A technique in stacking chip modules and packages strategically to support miniaturization and memory scalability in both vertical and horizontal orientation is therefore proposed.

SUMMARY OF THE INVENTION

In the stacking technique illustrated in example embodiments of the present invention, semiconductor dies are mounted in a module to become a MCM which serves as the basic building block. Combination of these modules and dies in a substrate creates a package with specific function or a range of memory capacity. These packages are stacked to increase capacity or add functions. A combination of different existing technology such as flip chip, wire bond, MCM, module stacking, advance packaging, etc. are used to accomplish highly reliable module to module and package to package interconnection and scalability. A single package can have a wide range of capacity depending on the memory capacity of the die used and the number of modules stacked within the package. In the proposed package stacking technique, the stacked modules in a package serve as the building blocks for the package level stacking. Multiple packages are stacked to create the desired memory capacity and different packages are stacked to create desired function. Expansion can be done both on the vertical and horizontal orientations. The technique is in the assignment of pins. Small capacity miniature storage devices can use the vertical expansion, while high capacity devices with larger form factors can use both vertical and horizontal expansion to maximize capacity. By using this technique, large capacity storage devices are implemented in a small package device, and larger form factors achieve bigger memory capacities.

The present invention takes advantage of the existing stacking technology both on the module and package level. This maximizes the capacity in a small area, realizing the miniaturization transition. Modular approach is used in creating basic building blocks

which can be tested individually and replaced easily prior to final packaging, making the technique reliable, and cost effectively. Wide range of capacity can be configured through variation of die capacities and stacking modules and/or packages. Expansions are implemented both vertically and horizontally depending on board area and desired capacity.

BRIEF DESCRIPTION OF DRAWINGS

So that the manner in which the above recited features, advantages and objects of the present invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the present invention may admit to other equally effective embodiments.

Figure 1a shows the block diagram of the stackable system for high performance, high capacity devices according to an example embodiment of the present invention.

Figure 1b shows the block diagram of the stackable system for lower performance, lower capacity devices according to an example embodiment of the present invention.

Figure 2a, 2b, 2c depict the SDRAM module's top and bottom drawings and a cross sectional representation of stacked multiple SDRAM modules according to an example embodiment of the present invention.

Figure 3a, 3b, 3c depict the flash module's top and bottom drawings and a cross sectional representation of stacked multiple flash modules according to an example embodiment of the present invention.

Figure 4a, 4b depict the first high-end controller module's top and bottom drawings according to an example embodiment of the present invention.

Figure 5a, 5b depict the memory module's top and bottom drawings according to an example embodiment of the present invention.

Figure 6a, 6b depict the first low-end controller module's top and bottom drawings according to an example embodiment of the present invention.

Figure 7a, 7b depict the second high-end controller module's top and bottom drawings according to an example embodiment of the present invention.

Figure 8a, 8b depict the second low-end controller module's top and bottom drawings according to an example embodiment of the present invention.

Figure 9 depicts the stacked SDRAM modules further stacked on the controller module according to an example embodiment of the present invention. This configuration is used for high end applications. The figure also shows how the balls have corresponding pads for inter-module connection.

Figure 10 depicts stacked flash modules further stacked on the memory module according to an example embodiment of the present invention. The figure also shows how the balls have corresponding pads for inter-module connection.

Figure 11 depicts the possible stacking options for the first high-end controller module and the memory modules according to an example embodiment of the present invention. A substrate interface is used to attach one group of stacked modules to another.

Figure 12a is an isometric exploded drawing of the stacking technique presented in Figure 11 according to an example embodiment of the present invention. Multiple identical stacking is not included in this drawing.

Figure 12b is another package stacking technique using Pin Grid Array (PGA) rather than Ball Grid Array (BGA) according to an example embodiment of the present invention. This is used for easy replacement and expansion.

Figure 13 depicts the low-end controller module configuration with stacked flash module according to an example embodiment of the present invention. The figure also shows how the balls have corresponding pads for inter-module connection.

Figure 14 is an isometric exploded version of the stacking technique presented in Figure 11 according to an example embodiment of the present invention.

Figure 15a, 15b depict the second high-end controller module configuration with stacked memory modules according to an example embodiment of the present invention. The figures also show how the balls have corresponding pads for inter-module connection.

Figure 16 is an isometric exploded version of the stacking technique presented in Figure 14 according to an example embodiment of the present invention.

Figure 17a, 17b depict the second low-end controller module configuration with stacked memory modules according to an example embodiment of the present invention. The figures also show how the balls have corresponding pads for inter-module connection.

Figure 18 is an isometric exploded version of the stacking technique presented in Figure 17 according to an example embodiment of the present invention.

Figure 19 shows a pin assignment and connection technique to be able to select specific layer in a multi-stacked module according to an example embodiment of the present invention.

Figure 20a shows another pin assignment technique which uses a rotational stacking orientation to allow stacking of four identical modules representing different bus interfaces according to an example embodiment of the present invention.

Figure 20b shows a cross-section representation of the four stacked modules on a rotational stacking technique and how their pins mates according to an example embodiment of the present invention.

Figure 21a shows another pin assignment and connection technique to be able to connect a serial chain route from multiple modules in a stack according to an example embodiment of the present invention.

Figure 21b shows how a serial chain connection is routed from one stack location to another allowing application of both vertical and horizontal expansion independently or simultaneously according to an example embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1a is a block diagram of a flash storage system according to a first example embodiment of the present invention. The block diagram shows the entire high-end system that is modularized, stacked, and packaged to achieve the desired features of the technique. The heart of the system is the main controller-processor **101** which interfaces with the flash memory, the flash PROM and the SDRAM memory blocks. The SDRAM is configured from a single bank **102** to a maximum of four banks depending on the desired capacity. Each bank such as **102** includes 3 SDRAMs. The flash devices such as **107** are controlled by the Flash Interface Controller such as **105**. Each controller supports four flash buses such as flash bus A11 **106**, and each flash bus supports a maximum of 8 flash devices. The main controller-processor supports four flash interface controllers through 4 different busses such as B bus **104**. The four flash interface controllers with their corresponding flash devices comprise the memory set **108**. The main controller-processor can support from one memory set to a maximum of 15 memory sets. This is a maximum support of 1,920 flash devices.

Figure 1b is a block diagram of a flash storage system according to a second example embodiment of the present invention. The block diagram shows the entire low-end system that is modularized, stacked, and packaged to achieve the desired features of the technique. Since a low-end system does not require a lot of memory capacity, SDRAM can be one bank **109** or none at all and the supported flash devices is also minimal to only two sets of flash bus. One set of flash bus **110** consists of four flash bus

with 8 flash devices supported per flash bus. This is a maximum support of 64 flash devices.

From the basic dies; SDRAM, FPROM, flash memory, flash interface controller, and the main controller-processor, single and multiple chip modules are created to become the basic building blocks for the stacking technique presented in the present invention. Referring to figure 2a which is a top view of an SDRAM module, three SDRAM dies **201** are placed in a single substrate **203** to become the SDRAM module which is one of the basic building blocks. The SDRAM module is represented in figure 1 as a single bank **102** composed of SDRAM 00, SDRAM 01, and SDRAM 02 connected to the SDRAM interface **103**. All signals needed to interface to the controller module and other SDRAM modules are assigned in both the bottom balls **204** and top pads **202** respectively. Bottom balls **204** are shown in figure 2b which is a bottom view of the SDRAM module, three slots **205** are created under the SDRAM die's pad attach area to accommodate bottom wire bonding. Figure 2c is the stacked module cross sectional representation. Top pads **202** and bottom balls **204** act as the vertical interconnects between all SDRAM modules and to the controller module. Varying the SDRAM die capacity and the stack quantity result in wide range of total SDRAM capacity depending on the product application. The SDRAM device organization, capacity and bank limitations are defined by the main controller-processor's SDRAM interface specifications. The main controller-processor intended to be used for this example embodiment of the present invention supports a 32-bit wide 4 banks max SDRAM configuration.

Figure 3a is a top view, shows four flash dies **301** in a single substrate **303** becoming the flash module which is also a basic building block. All signals needed to interface with the memory module and other flash modules are assigned in both the bottom balls **304** and the top pads **302** respectively. In figure 3c, the flash modules are stacked. Maximum stack quantity depends on the flash interface controller specifications. Top pads **302** and bottom balls **304** acts as the vertical interconnects between stacked flash modules and to the memory module. Varying the flash die capacity and the stacking quantity results in a wide range of total flash capacity depending on the product application and capacity requirements. The flash device organization and capacity limitations are defined by the flash interface controller's specifications. The flash interface controller intended to be used for this used for this example embodiment of the present invention supports 8 flash devices per flash bus, thus allowing a maximum stacking of 8 flash modules.

Figure 4a shows the top view of the first example embodiment of the present invention illustrated in a first high-end controller module configuration. A single FPROM die **401** is placed at the center of the substrate **404**. Pads are composed of two sections, one for the SDRAM module interface shown as **402** and another for the memory module interface shown as **403**. This technique enables multiple stacking of both SDRAM modules and memory modules in a single package. Figure 4b shows the bottom view of the controller module. A single main controller-processor die **406** is placed at the center of the substrate. The controller module becomes a base module for the package. The balls**405** are used to connect to the main substrate which is typically a printed circuit

board (PCB).

Figure 5a shows the top view of the memory module which is also a basic building block. A single flash interface controller die **501** is placed on the center of the substrate **504**. Pads are composed of two sections, one for the flash module interface shown as **502** and another for the other memory module interface shown as **503**. This technique enables multiple stacking of flash modules and memory modules in a single package. The memory module becomes a base module for the package. Figure 5b shows the bottom view of the memory module. The memory module balls **505** are used to connect to the main substrate PCB, to the controller modules or to the other memory modules depending on the type of configuration desired.

Figure 6a shows the top view of the second example embodiment of the present invention illustrated in a first low-end controller module configuration. Two SDRAMs **601** and a single FPROM **602** are placed on top of the module. This configuration is flexible. The SDRAMs can be unpopulated in a low performance application. Internal SRAMs in the main controller-processor will take over the SDRAM functions. The main controller-processor **605** is placed at the bottom of the module. This configuration does not allow stacking of the SDRAM which is not necessary for low capacity applications. Flash modules are stacked on top interfacing to the pads **603.** The substrate **604** is the same size as the flash module making its final package smaller. The bottom balls **606** are used to interface with the main PCB.

Figure 7a shows the top view of the first example embodiment of the present invention illustrated in a second high-end controller module configuration, where four memory modules **701** can be mounted on separate locations adjacent to each other. Memory module interface pads **704** are allocated for multiple stack configurations. In the middle of the memory module interface pads, 3 SDRAM dies **702** are mounted. Each area corresponds to one SDRAM bank **703**, totaling to a maximum of 4 SDRAM banks in the package. The bottom view is presented in Figure 7b, where the main controller-processor die **705** and the FPROM die **706** are mounted adjacent to each other. The module's balls **707** are used for external interface to the main PCB.

Figure 8a shows the top view of the second example embodiment of the present invention illustrated in a second low-end controller module configuration, where only two memory modules **801** can be mounted side-by-side. Memory module interface pads **802** are allocated for multiple stacking configurations. In the middle of the memory module interface pads, 3 SDRAM dies **803** are mounted. Each area corresponds to one SDRAM bank **804**, totaling to only a maximum of 2 SDRAM banks in a package. The SDRAM can either be mounted or not depending on the application. Internal SRAMs can also be used instead of the SDRAMs. The stacked memory modules can also be configured to support both internal and external flash interface controller applications. The bottom view is presented in Figure 8b, where the main controller-processor die **805** and the FPROM die **806** are mounted adjacent to each other. The module balls **807** are used for external interface to the main PCB.

Figure 9 shows the stacking of SDRAM module **901** and controller module **902**. A single or stacked SDRAM module can be placed on top of a controller module. The pads for the SDRAM module interface **903** must align with the SDRAM module balls **904**. The bottom-most SDRAM module **905** serves as bank 0, and the top-most module **906** serves as bank 3,. For low capacity SDRAM requirements, only a single or dual bank is enough. High capacity devices needs to have a maximum SDRAM capacity, thus stacking the maximum of 4 modules. The outer pads **907** are for the memory module interface.

Figure 10 shows the stacking of flash modules **1001** and memory module **1002**. A four-stack or eight-stack flash module is placed on top of a memory module. The pads for the flash module interface **1003** must align with the flash module balls **1004**. The outer pads **1005** are for other memory module interface. The flash interface controller intended to be used for this example embodiment of the present invention supports a maximum of 4 flash buses and each flash bus supports a maximum of 8 flash devices. The bottom-most flash module **1006** contains the 4 flash buses' Flash 00 devices and the top-most module **1007** contains the 4 flash buses' Flash 07 devices.

Figure 11 shows a sample of a maximized stacking technique that can be configured through vertical, horizontal or combined expansion. Multiple staking will increase the overall height of the module, thus requiring a filler **1101** to physically interconnect two stacked modules. A thinner filler **1102** may be used depending on the height differential between the modules which is dependent to the number of stacks

applied. A controller module with the stacked SDRAM modules act as the controller package **1103**. A memory module with stacked flash modules acts as the memory package **1104**. Four memory packages stacked together form the memory set **1105**. Vertical expansion happens when the controller package is stacked with a single or multiple memory sets. The figure shows a single memory set to be stacked to the controller package. Horizontal expansion happens when the controller package is located on a different site on the PCB relative to the memory sets. Also multiple memory sets can be located on different sites on a PCB. Combo expansion happens when both vertical and horizontal expansion technique is implemented simultaneously. The expansion technique is very flexible depending on the desired memory capacity, main PCB size limitations and also height limitations.

Figure 12a shows the isometric and exploded drawing of the stacking technique for the first high-end controller configuration. Pins are assigned strategically and modules are stacked to make possible the miniaturization of the entire system in a package.

1201 – The Flash Module

1202 – The Flash Die

1203 – The Flash Module Pad Interface to other Flash Modules

1204 – The Flash Module Solder Balls

1205 – The Memory Module

1206 – The Flash Interface Controller Die

1207 – The Memory Module Pad Interface for the Flash Module

1208 – The Memory Module Pad Interface for the other Memory Modules

1209 – The Memory Module Solder Balls

1210 – The SDRAM Module

1211 – The SDRAM Die

1212 – The SDRAM Module Pad Interface to other SDRAM Modules

1213 – The SDRAM Module Solder Balls

1214 – The Controller Module

1215 – The FPROM Die on top side and the Main Controller-Processor Die at the bottom side.

1216 – The Controller Module Pad Interface to the SDRAM Modules

1217 – The Controller Module Pad Interface to the Memory Modules

1218 – The Controller Module Solder Balls

Figure 12b is another technique used in this invention to ease replacement and facilitate expansion. Instead of using Ball Grid Array (BGA), Pin Grid Array (PGA) **1219** is used. This method makes it more flexible due to the technology's inherent feature where replacement is done swiftly without any assembly process involved. Horizontal expansion is also benefited in this technology. The figure shows the stacked memory module as an example. The memory module is packaged using the PGA technology, where the top portion of the package becomes the socket **1220** and the bottom portion the pin arrays **1219**. The filler **1221** becomes the package's top socket and is interfaced into the base module **1222** through the BGA **1223**. The base module uses PGA to interface to the bottom package or to the main board **1224**. Filler **1225** is also mounted into the main board to interface the stacked memory modules.

Figure 13 shows the stacking of the flash module **1301** and the first low-end type of controller module **1302**. A single or stacked flash module can be placed on top of the controller module. The pads for the flash module interface **1303** must align with the flash module balls **1304**. This configuration is for low capacity low performance applications. The number of flash modules to be stacked depends on the desired capacity and is limited to the supported feature of the main controller-processor. The main controller-processor's flash interface can support a maximum of 8 buses and a maximum of 8 flash devices per bus.

Figure 14 shows the isometric and exploded drawing of the stacking technique for the first low-end controller configuration. Pins are assigned strategically and modules are stacked to make possible the miniaturization of the entire system in a package.

1401 – The Flash Module

1402 – The Flash Die

1403 – The Flash Module Pad Interface to other Flash Modules

1404 – The Flash Module Solder Balls

1405 – The Controller Module

1406 – The FPROM Die and the Main Controller-Processor Die at the bottom

1407 – The SDRAM Die

1408 – The Controller Module Pad Interface to the Flash Modules

1409 – The Controller Module Solder Balls

Figure 15a shows the stacking technique for the second high-end controller configuration. The stacked flash modules **1501** are further stacked on top of the memory modules **1502** which are then mounted on the controller module **1503** on four different locations. Four memory modules can be mounted on four different locations on the controller module creating a memory set. Stacking more memory sets increases the total capacity. The cross-sectional representation of the said stacking technique is shown in Figure 15b. The memory module balls **1504** must align to the pad interface **1505** on the controller module. As previously discussed in figure 11, fillers are used to physically connect two successively stacked modules. The controller balls **1506** will become the external interface to the main board. The final package is 4X bigger than the first high end option.

Figure 16 shows the isometric and exploded drawing of the stacking technique discussed in Figure 15. Pins are assigned strategically and modules stacked to make possible the maximum stacking and interconnection between modules. As previously discussed in figure 11, fillers are used to physically connect two stacked successively stacked modules.

1601 – The Flash Module

1602 – The Flash Dies

1603 – The Flash Module Pads Interface to other Flash Modules

1604 – The Flash Module Solder Balls

1605 – The Memory Module

1606 – The Flash Interface Controller Dies

1607 – The Memory Module Pad Interface to Flash Modules

1608 – The Memory Module Pad Interface to other Memory Modules

1609 – The Memory Module Solder Balls

1610 – The Controller Module

1611 – The SDRAM Dies on top side and the FPROM and Main Controller-Processor at the bottom side

1612 – The Controller Module Pads Interface to the Memory Modules

1613 – The Controller Module Solder Balls

Figure 17a shows the stacking technique for the second low-end configuration. The stacked flash modules **1701** are further stacked on top of the memory modules **1702** which are then mounted on the controller module **1703** on two different locations. This technique can use both internal and external flash interface controller configurations, making this technique flexible. The cross-sectional view is shown in figure 17b. The memory module balls **1704** must align to the pad interface **1705** on the controller module. The controller balls **1706** will become the external interface to the main board. The final package is twice the size of the first high end option.

Figure 18 shows the isometric and exploded drawing of the stacking technique discussed in Figure 17. Pins are assigned strategically and modules stacked to make possible the maximum stacking and interconnection between modules. As previously discussed in figure 11, fillers are used to physically connect two stacked successively stacked modules.

1801 – The Flash Module

1802 – The Flash Dies

1803 – The Flash Module Pads Interface to other Flash Modules

1804 – The Flash Module Solder Balls

1805 – The Memory Module

1806 – The Flash Interface Controller Dies

1807 – The Memory Module Pad Interface to Flash Modules

1808 – The Memory Module Pad Interface to other Memory Modules

1809 – The Memory Module Solder Balls

1810 – The Controller Module

1811 – The SDRAM Dies on top side and the FPROM and Main Controller-Processor at the bottom side

1812 – The Controller Module Pads Interface to the Memory Modules

1813 – The Controller Module Solder Balls

A more detailed technique on how the pins are assigned and how modules are placed with different orientation in the stack is discussed in the following paragraphs.

Figure 19 shows a first pin assignment and connection technique that enables a selection of specific module in a multiple module stack. The figure illustrates the controller and SDRAM modules as example. The SDRAM module's balls such as **1907** are represented by big oblong and the pads such as **1908** are represented by smaller oblong. Pad to ball connection is represented by rectangle such as **1906**. The controller

module has four active pads such as **1904,** one each for the four SDRAM modules such as **1901**. The controller module's pad 00 **1904** is connected to SDRAM module 0's X0 ball **1903**, pad 01 to SDRAM module 1's X0 ball **1902**, and so on. The X0 balls are the active ball for the SDRAM modules. All SDRAM modules are identical which include the connections as follows: X1 ball is connected to X1 pad, X2 ball to X2 pad, and so on. The technique involves **a ladder like routing** such as **1905** on the stacked modules. This technique enables the controller module's active pad to be routed to the desired specific module in the stack. The example embodiment illustrated in figure 19 comprises a repeating pattern for the balls and pads. Passive balls are connected within each module to passive pads with an offset distance equaling one periodic distance of the repeating pattern. The importance is the approach using repeating pattern and offsetting of the passive ball to passive pad within each module, other offset distance can be used also in other embodiment of the present invention, e.g. using offset of 2 or any multiple of the periodic distance of the repeating pattern. The example embodiment does not limit the scope of the present invention.

Another pin assignment, connection, and stacking combo method introduced in this invention is **the rotational stacking technique**. Figure 20a shows the pad interconnects for a certain base module and strategic numbering is assigned. Pads labeled with numbers 1 to 4 represent the 4 different groups of signals. Pads labeled with number 5 are used for the vertical stacking IOs (more details are illustrated in figure 21). Pads labeled with number 6 are reserved for power and ground which are common to all modules in the stack. Since the stacked modules are identical, we can use rotational

stacking to connect one module to one group of signals and the following rotated stacked module connects to another group of signals, and so on. This way ensures four identical modules to be stacked and connected to four different groups of signals from the base module which is typically a controller. Pad 1 **2001,** upon the substrate being rotated 90 degrees clockwise, occupies pad 2 **2002** location relative to an un-rotated substrate such as the base substrate which is typically a controller. In a similar manner pad 1 **2001** can be located at pad 3 **2003** location, then pad 4 **2004** location upon the substrate being rotated 180 and 270 degrees clockwise respectively. Figure 20b shows a cross-sectional view of four such modules stacked over the base module. Memory and Controller modules are used as example. Pin 1s such as **2005** on the stacked modules are the only active signal pins for the module. The rest (numbered 2 to 4) **2006** are directly connected to the balls underneath them but has no other connections. This way connection is continued from bottom to top. The active pin **2007** of the first module **2008** is aligned to pin 1 pad **2009** on the base module and the second module's active pin **2010** is aligned on pin 2 **2011** of the base module with second module being rotated 90 degrees clockwise. Since pin 2 **2012** on the first module is directly connected to the ball underneath, this allows the pin 1 on the second module **2013** to be connected to pin 2 **2011** of the base module. Rotating the next stacked module 90 degrees more will align it's active pin to the base modules pin 3 and so on until the forth rotation.

The last connection technique is used for serial routing of all modules in the stack and allowing them to be externally accessible for horizontal expansion on a PCB. Figure 21a shows how this technique is implemented in the stacking method. The main board

2101 contains the input signals **2102** which will then be connected to IN ball **2104** of the base module **2103**. The base module's OUT pad **2105** is connected to IN ball **2107** of the first stack module **2106**, and so on. The top module **2108** terminates the signal to the top pad **2109** and routes, with connection **2112,** the signal internally to another pad **2110** which is connected directly to the ball **2113** underneath . Since the modules are identical, this routed signal passes through the pads and balls **2111** of the stack until it reaches the OUT pad **2114** of the main board for external access. How the top module terminates the serial chain and branches them out to other pads is shown in Figure 21b. All module have a selectable buffer **2115** that tri-states the input when pulled low. The signal from the IN balls **2116** enters the internal circuit **2117** and exits the circuit connecting to the OUT pad **2118**. The buffer's **2115** control line is weakly pulled up internally. The "StkLow" ball is connected internally to GND **2119**, thus pulling down the buffer control line when a module is stacked above it and it's pulled up when no module is stacked directly above it. When the buffer is pulled high, it will let the input signal branch out **2120** to the other pads, thus making possible the trace to loop back to the base module's solder balls. When a module is stacked above a module, the buffer control signal is pulled low, tri-stating the input signal disallowing the branching effect. This technique allows the signal to be accessible to the external balls of the base module, thus horizontal expansion for serial signal is achievable. The balls are then routed, with connection **2121,** to the other modules **2122** on the other locations. The same technique is used on the main board **2123**, when no package is detected on the "StkLow" pad, the buffer allows the input to connect to the designated pads on the other locations. The tri-stated buffer technique is redundant to all locations. An example is the JTAG TDI-TDO signal. The diver circuit

2125 sends out TDI signals to the pads and the closing TDO signal **2124** loops back to the driver circuit.

Combining these stacking, pin assigning and connection techniques allow interconnection between modules with both parallel and series signals to both vertical and horizontal expansion. The technique is very flexible depending on the specific application, capacity, board size and height limit.

CLAIMS

WE CLAIM:

1. A method for stacking a plurality of modules comprising the steps of:

providing one or more active port on the plurality of modules for carrying one or more active signal;

providing one or more passive port on the plurality of modules for passing through the one or more active signals; and

stacking the plurality of modules.

2. The method of claim 1 wherein the one or more passive port forms a ladder like routing path.

3. The method of claim 1 wherein one or more of the plurality of module is rotated before being stacked and the one or more passive port forms a rotational routing path.

4. The method of claim 1 further comprising the step of providing one or more pair of daisy chain input port and daisy chain output port for forming a first daisy chain connection wherein each pair of the daisy chain input port and the daisy chain output port are connected through a daisy chain circuit.

5. The method of claim 4 further comprising the step of providing one or more control port for enabling a routing path extending the first daisy chain connection within an end module.

6. The method of claim 5 wherein the routing path within the end module is connected to a second daisy chain connection.

7. The method of claim 1 wherein one or more of the plurality of modules is a main board.

8. The method of claim 7 wherein one or more vertically stacked module is connected to the main board.

9. The method of claim 2:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located between a pre-determined distance to each other in a repeating pattern, the pre-determined distance equaling a multiple of a

periodic distance of the repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the ladder like routing path; and

wherein the ladder like routing path comprises one or more passive ball and one or more passive pad.

10. The method of claim 3:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located opposite each other in a repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the rotational routing path; and

wherein the rotational routing path comprises one or more passive ball and one or more passive pad.

11. The method of claim 4:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection; and

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad.

12. The method of claim 5:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad; and

wherein the routing path comprises one or more tri-state driver controlled by the one or more control port.

13. The method of claim 6:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad;

wherein the routing path comprises one or more tri-state driver controlled by the one or more control port; and

wherein one or more daisy chain connection are extended through one or more vertically stacked module connected to a main board.

14. A stacked module comprising a plurality of modules each comprising:

one or more active port for carrying one or more active signal; and

one or more passive port for passing through the one or more active signals.

15. The stacked module of claim 14 wherein the one or more passive port forms a ladder like routing path.

16. The stacked module of claim 14 wherein one or more of the plurality of module is rotated before being stacked and the one or more passive port forms a rotational routing path.

17. The stacked module of claim 1 further comprising one or more pair of daisy chain input port and daisy chain output port for forming a first daisy chain connection wherein each pair of the daisy chain input port and the daisy chain output port are connected through a daisy chain circuit.

18. The stacked module of claim 17 further comprising one or more control port for enabling a routing path extending the first daisy chain connection within an end module.

19. The stacked module of claim 18 wherein the routing path within the end module is connected to a second daisy chain connection.

20. The stacked module of claim 14 wherein one or more of the plurality of modules is a main board.

21. The method of claim 20 wherein one or more vertically stacked module is connected to the main board.

22. The stacked module of claim 15:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located between a pre-determined distance to each other in a repeating pattern, the pre-determined distance equaling a multiple of a periodic distance of the repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the ladder like routing path; and

wherein the ladder like routing path comprises one or more passive ball and one or more passive pad.

23. The stacked module of claim 16:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more active port is connected to one or more active ball on the first side of one or more corresponding module;

wherein the one or more passive port is connected to one or more passive ball on the first side and one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad connected to a same passive port are located opposite each other in a repeating pattern;

wherein one or more active port of a base module is routed to a same location on one or more modules through the rotational routing path; and

wherein the rotational routing path comprises one or more passive ball and one or more passive pad.

24. The stacked module of claim 17:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection; and

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad.

25. The stacked module of claim 18:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad; and

wherein the routing path comprises one or more tri-state driver controlled by the one or more control port.

26. The stacked module of claim 19:

wherein each of the plurality of modules comprises a first side and a second side;

wherein the one or more daisy chain input port is connected to one or more passive ball on the first side and the one or more daisy chain output port is connected to one or more passive pad on the second side of one or more corresponding module;

wherein each of the one or more passive ball and each of the one or more passive pad corresponding to a same daisy chain port are located opposite each other;

wherein one or more active port of a base module is routed to a same location on one or more modules through the daisy chain connection;

wherein the daisy chain connection comprises one or more daisy chain circuit, one or more passive ball and one or more passive pad;

wherein the routing path comprises one or more tri-state driver controlled by the one or more control port; and

wherein one or more daisy chain connection are extended through one or more vertically stacked module connected to a main board.

ABSTRACT

Stacking techniques are illustrated in example embodiments of the present invention wherein semiconductor dies are mounted in a module to become a MCM which serves as the basic building block. Combination of these modules and dies in a substrate creates a package with specific function or a range of memory capacity. Several example system configurations are provided using BGA and PGA to illustrate the stacking technique. Several pin assignment and signal routing techniques are illustrated wherein internal and external signals are routed from main board to various stacked modules. Expansion can be done both on the vertical and horizontal orientations.

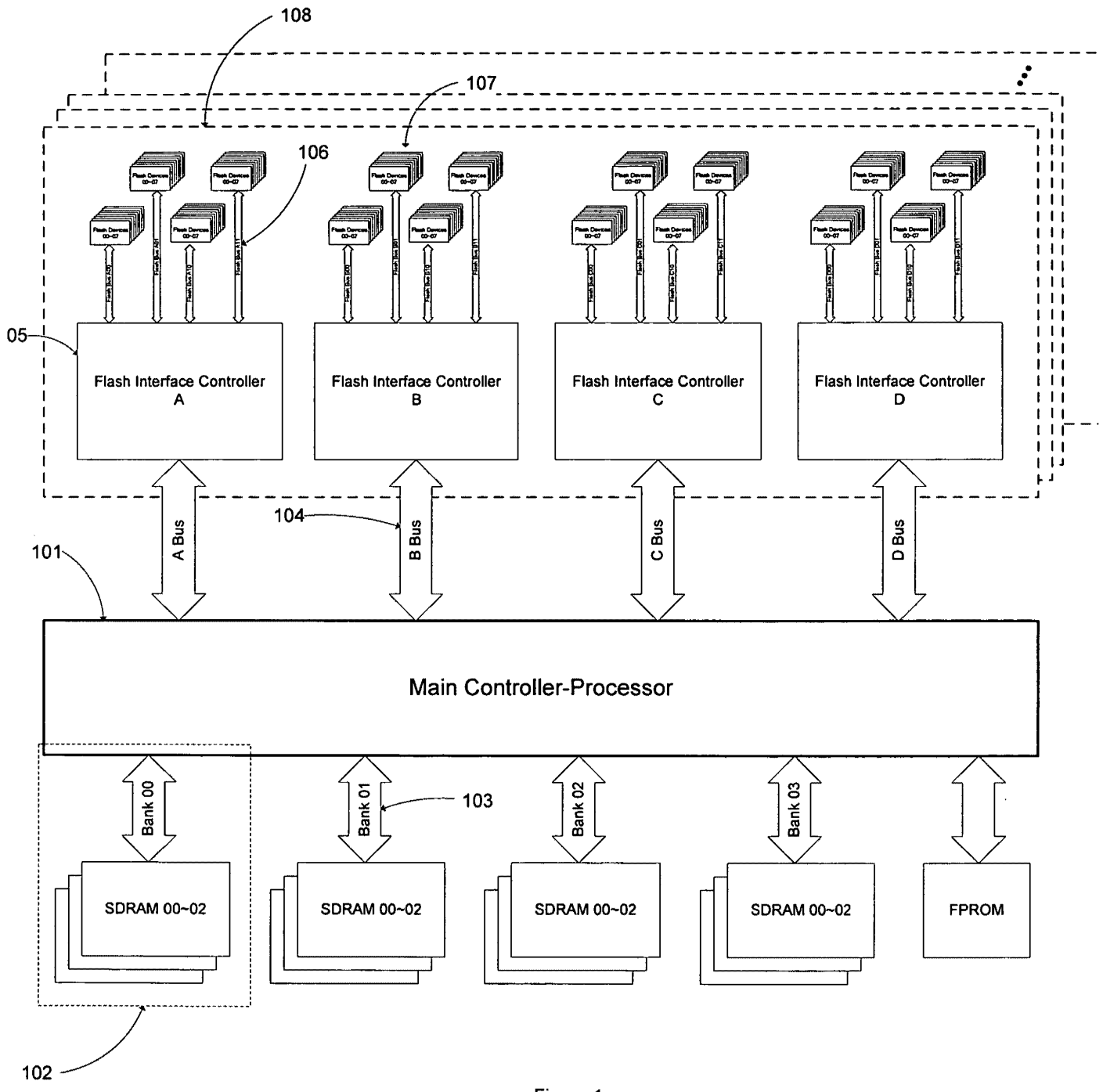

108
107
106
05
Flash Interface Controller A
Flash Interface Controller B
Flash Interface Controller C
Flash Interface Controller D
104
A Bus
B Bus
C Bus
D Bus
101
Main Controller-Processor
Bank 00
Bank 01
103
Bank 02
Bank 03
SDRAM 00~02
SDRAM 00~02
SDRAM 00~02
SDRAM 00~02
FPROM
102

Figure 1a

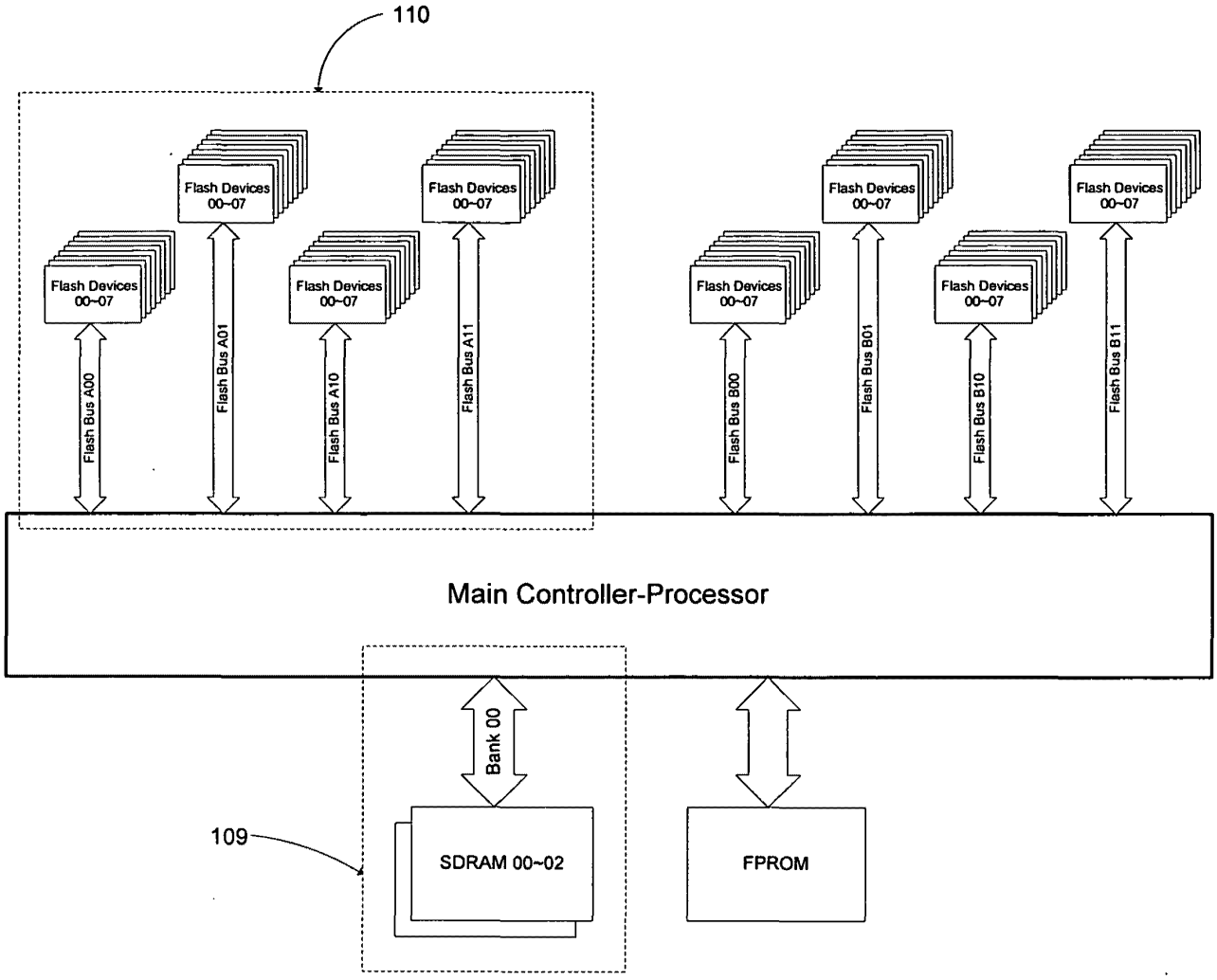


Figure 1b

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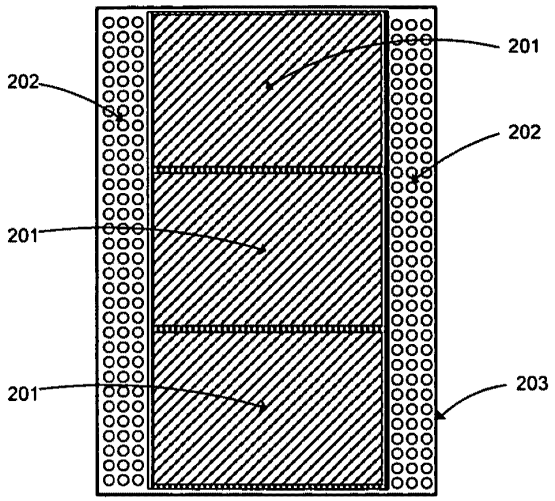


Figure 2a

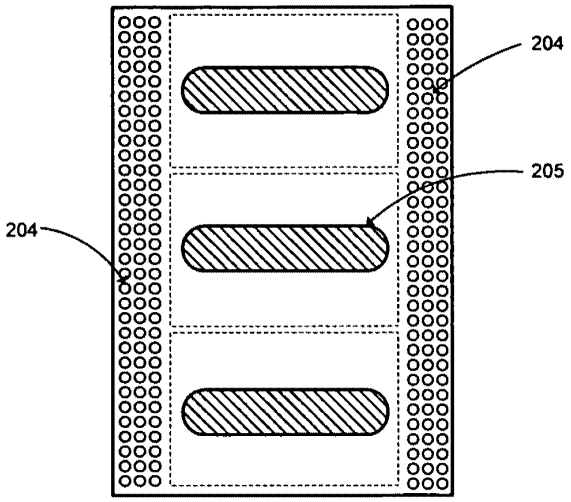


Figure 2b

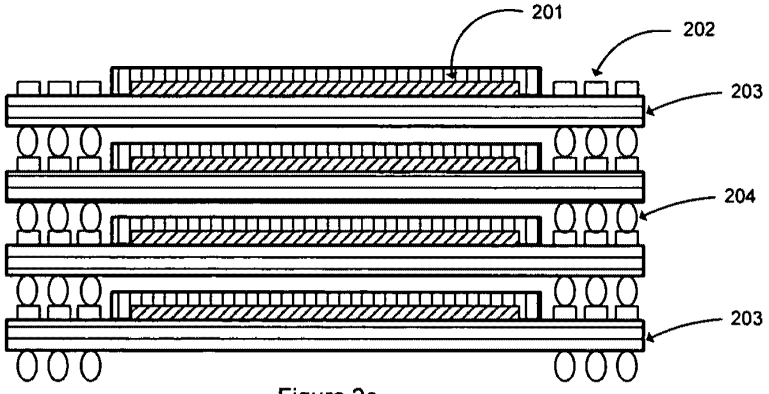


Figure 2c

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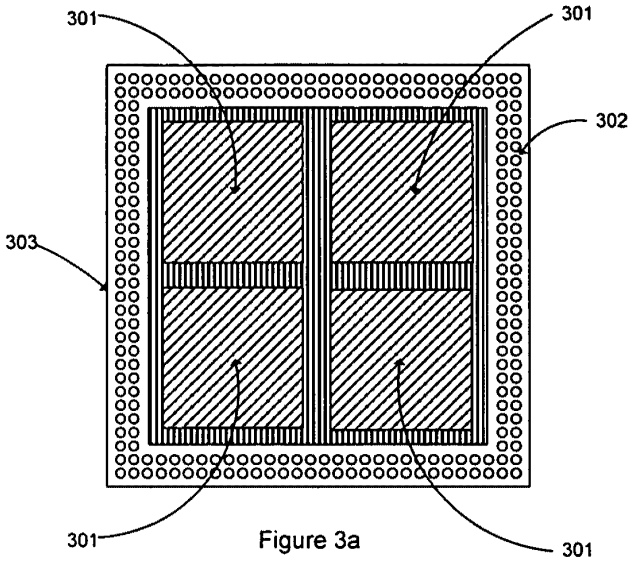


Figure 3a

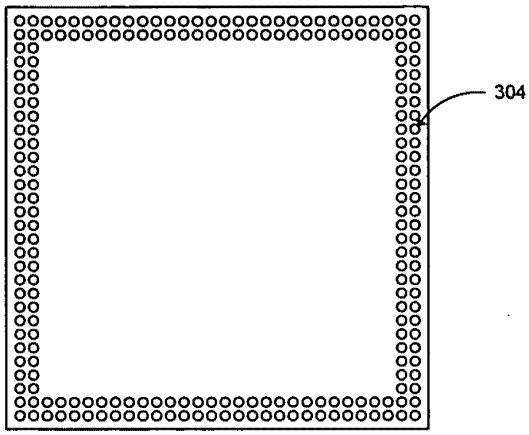


Figure 3b

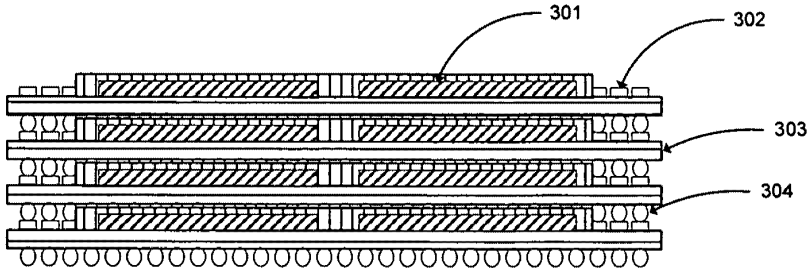


Figure 3c

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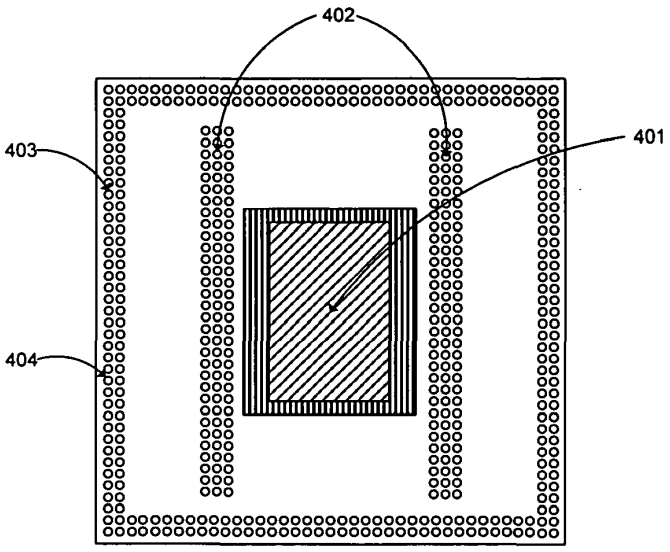


Figure 4a

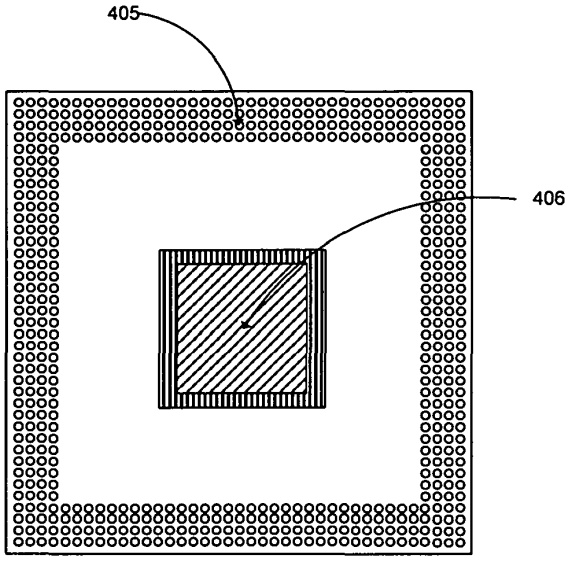


Figure 4b

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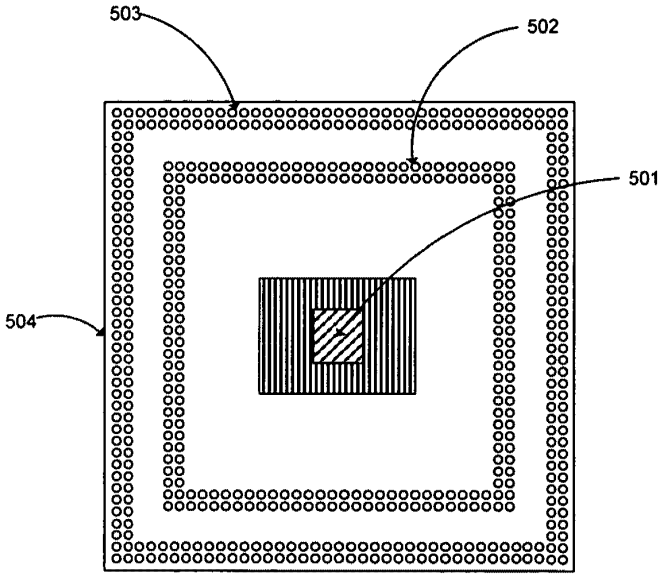


Figure 5a

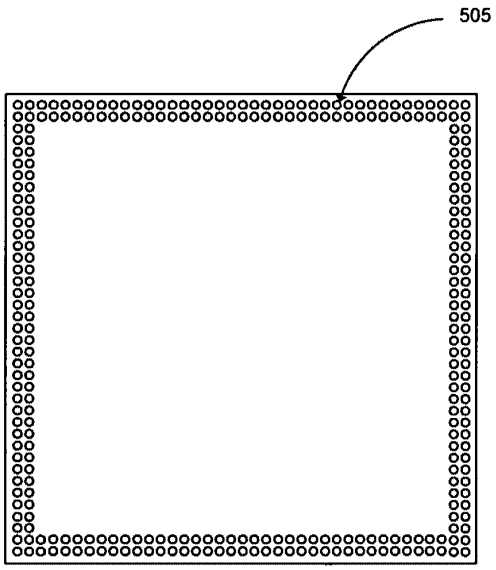


Figure 5b

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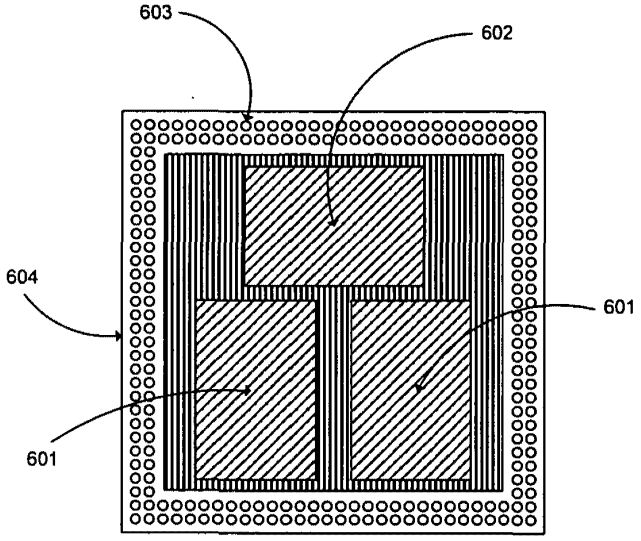


Figure 6a

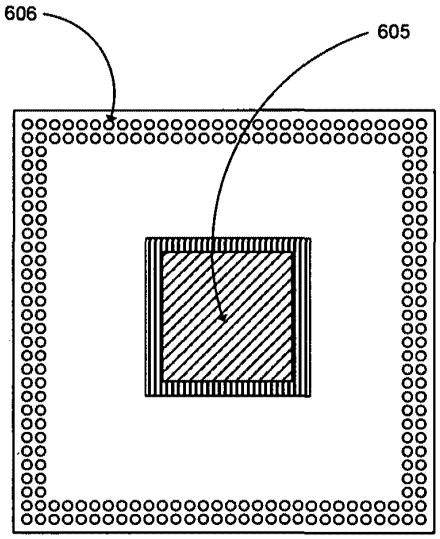


Figure 6b

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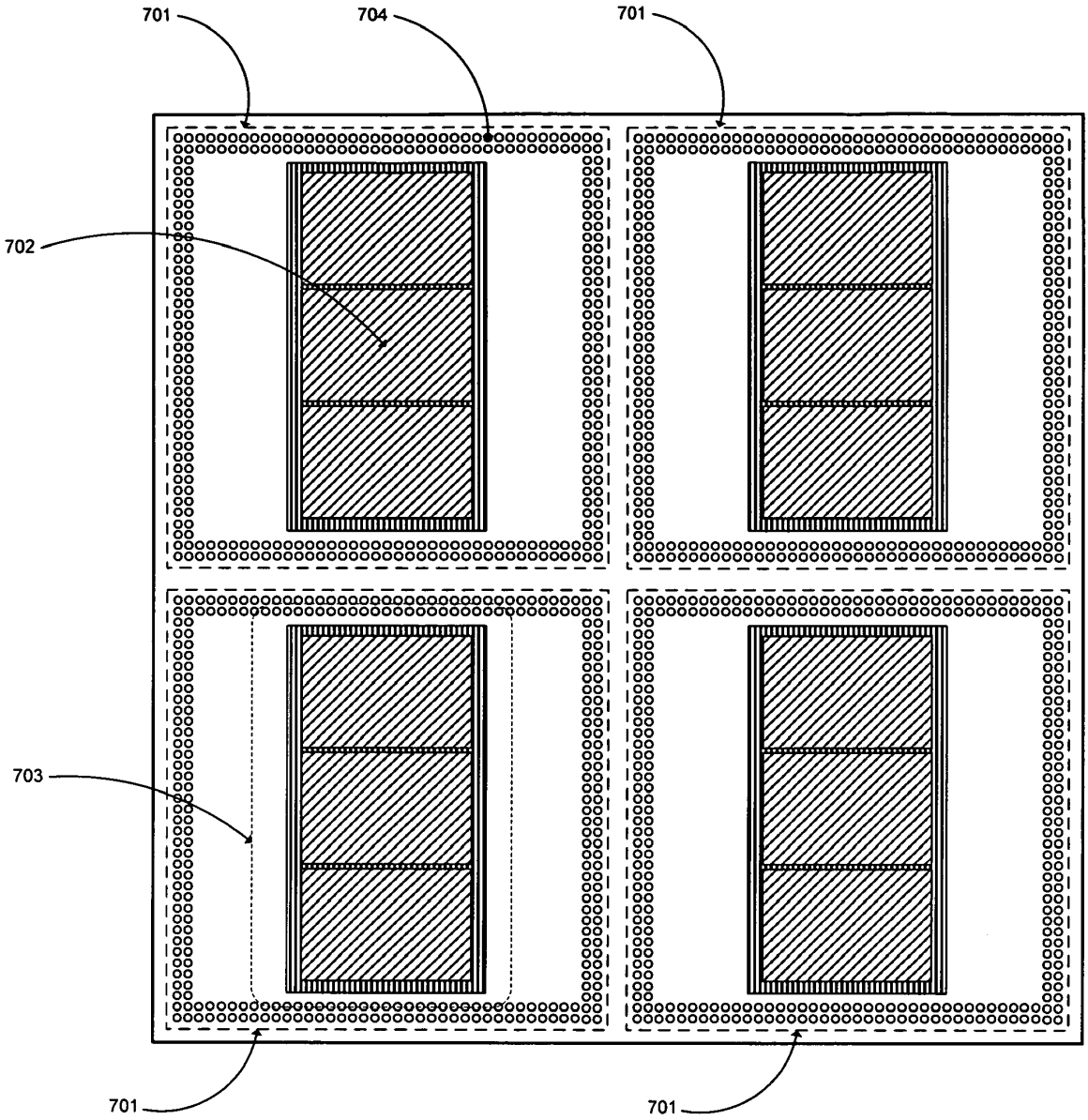


Figure 7a

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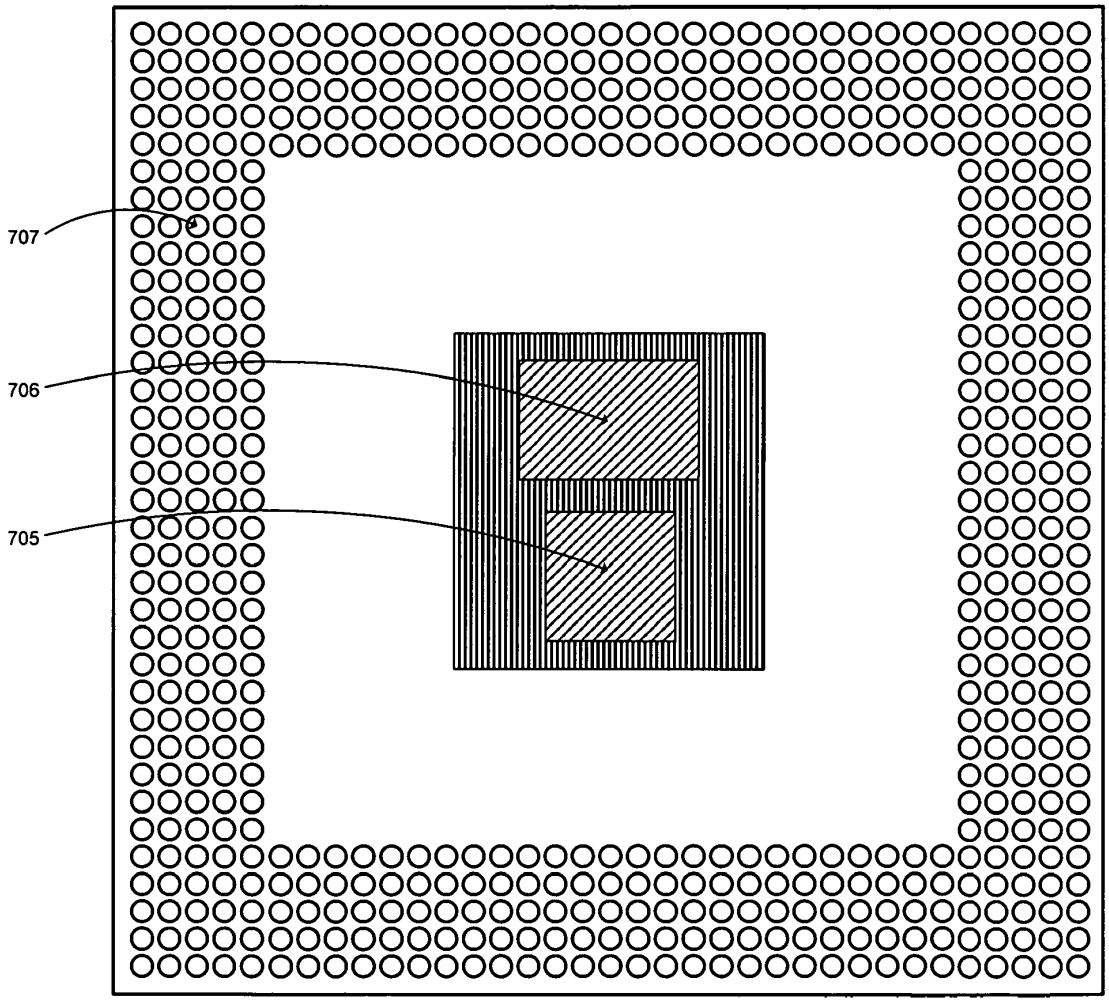


Figure 7b

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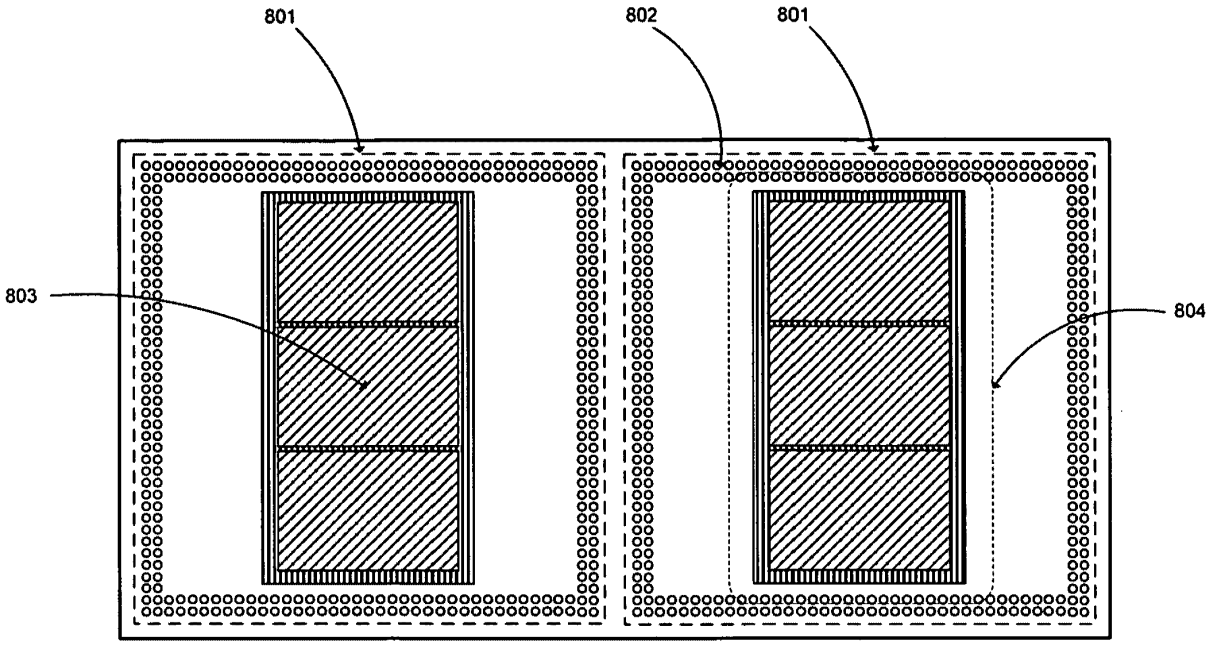


Figure 8a

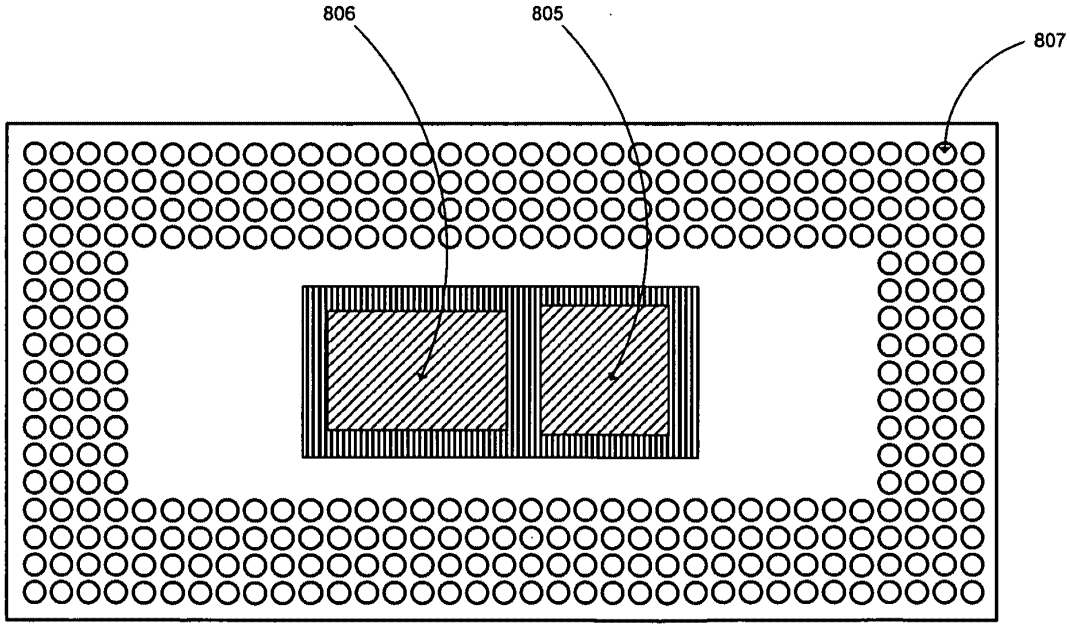


Figure 8b

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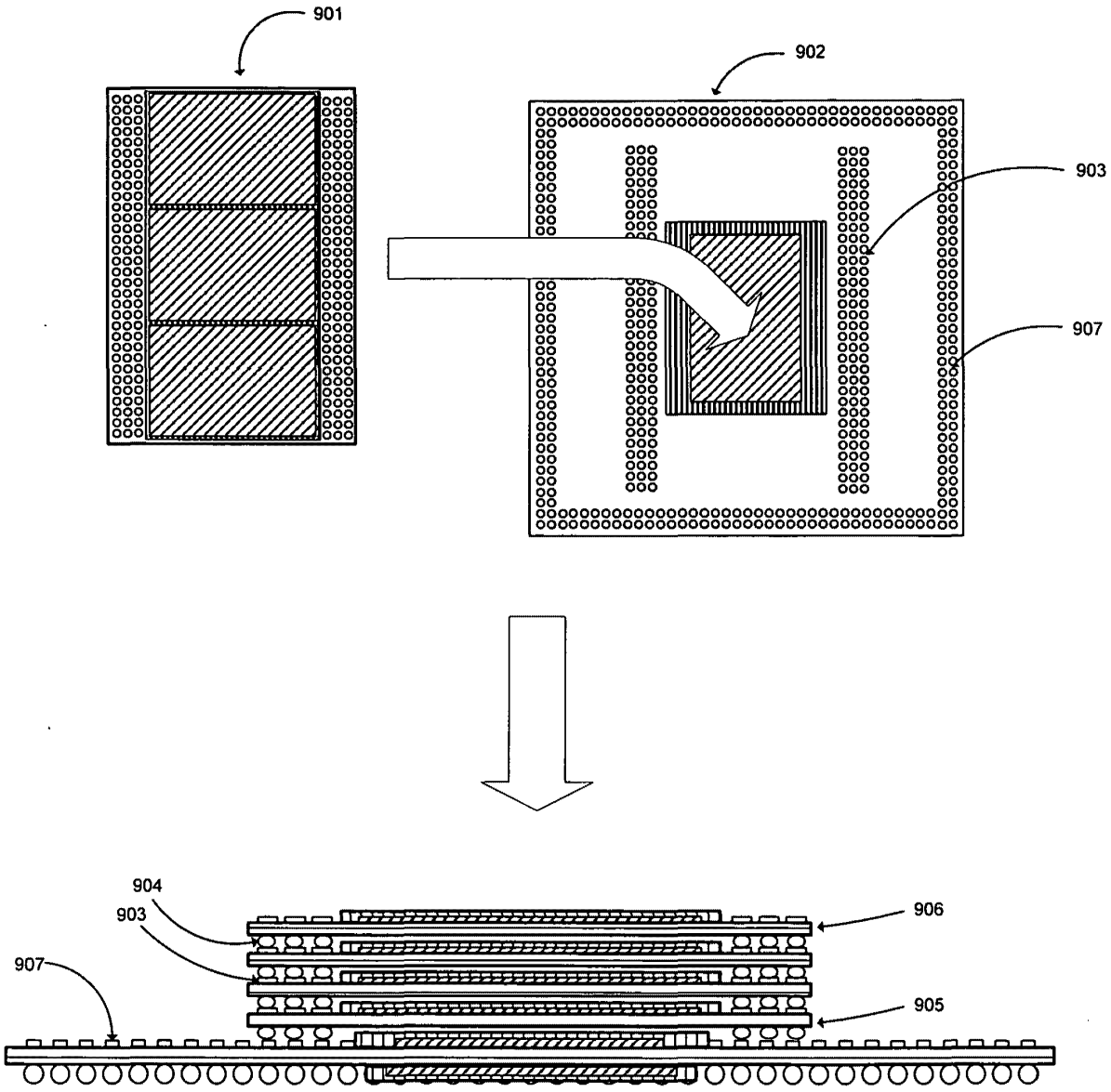


Figure 9

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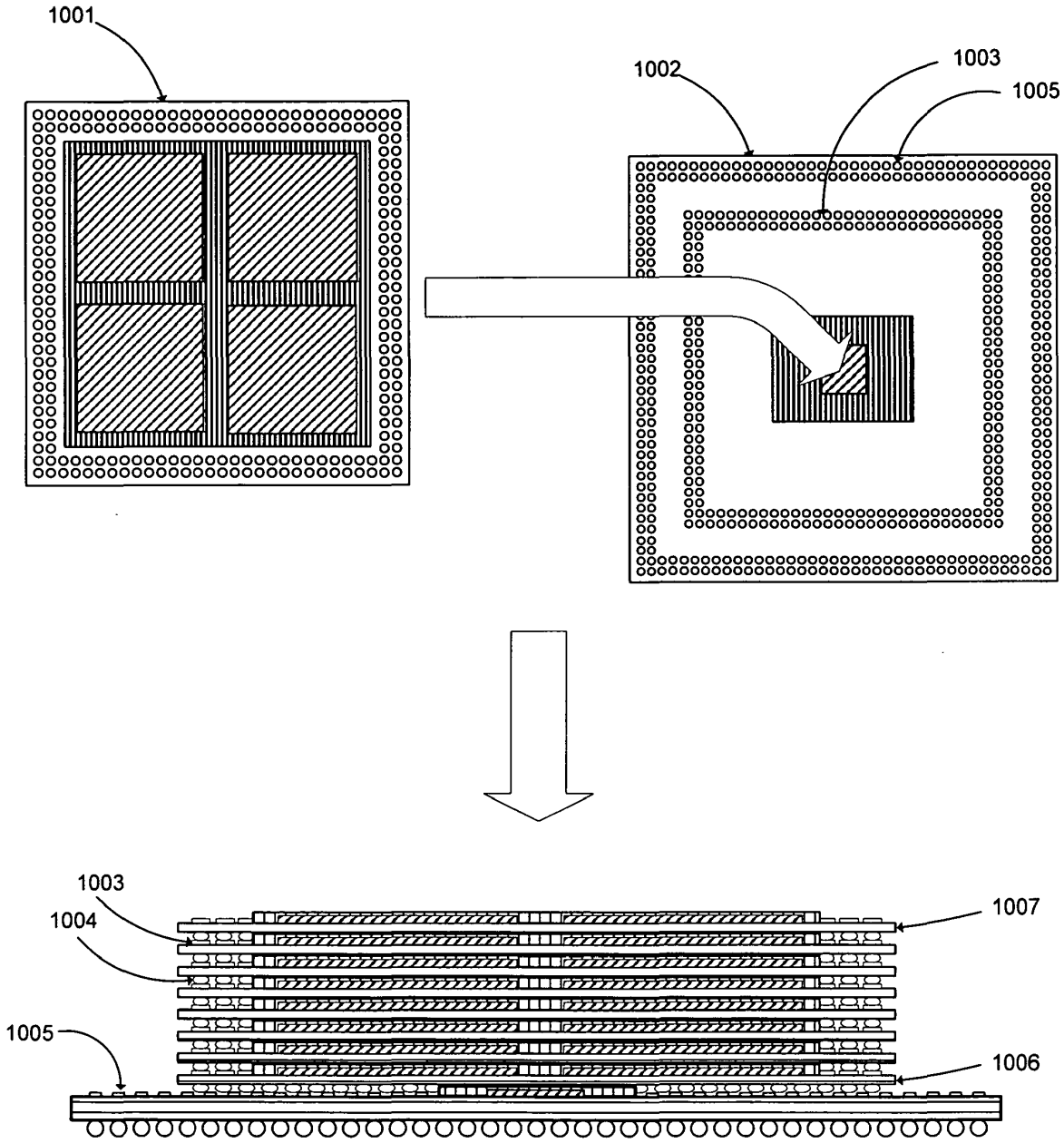


Figure 10

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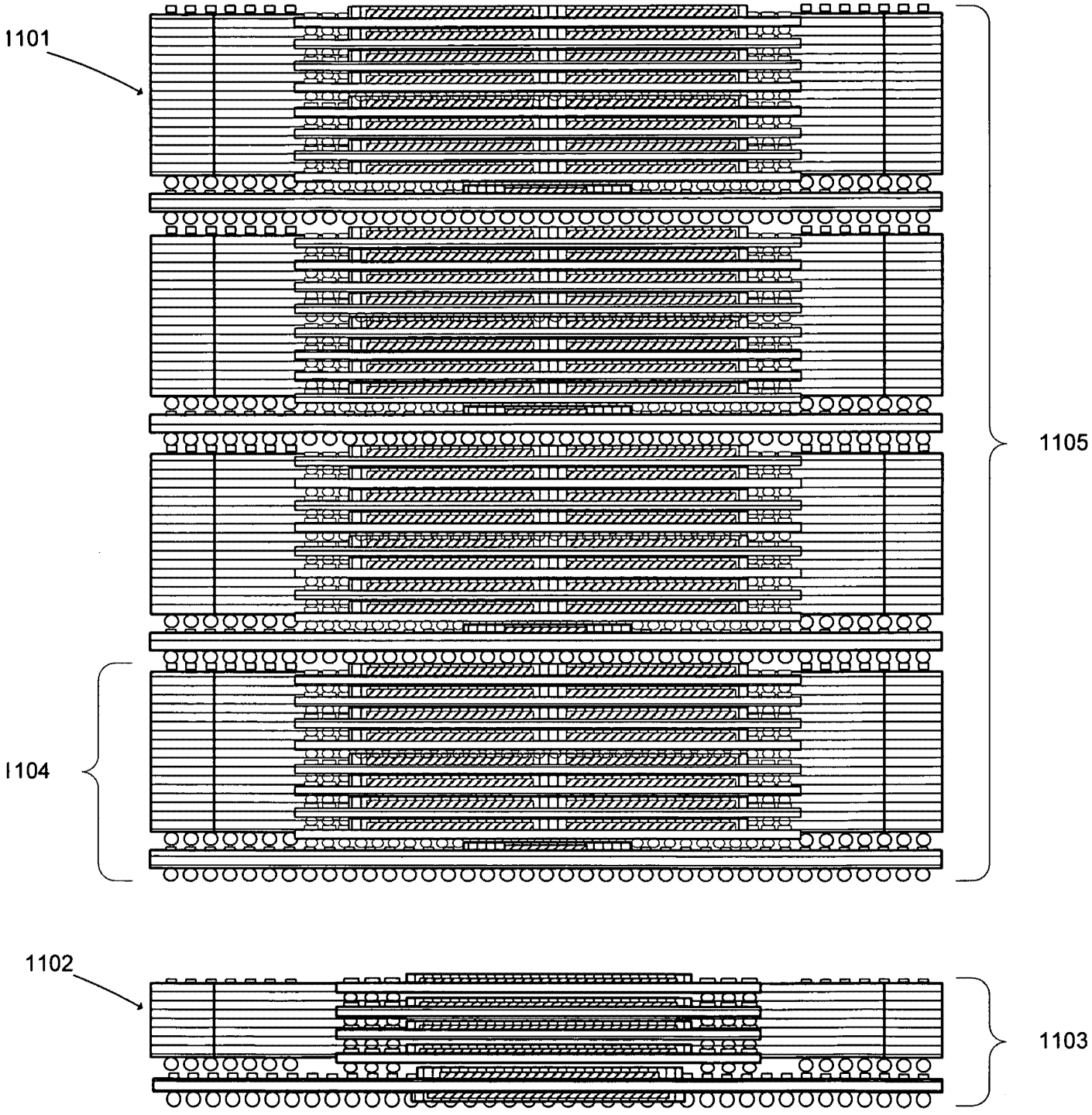


Figure 11

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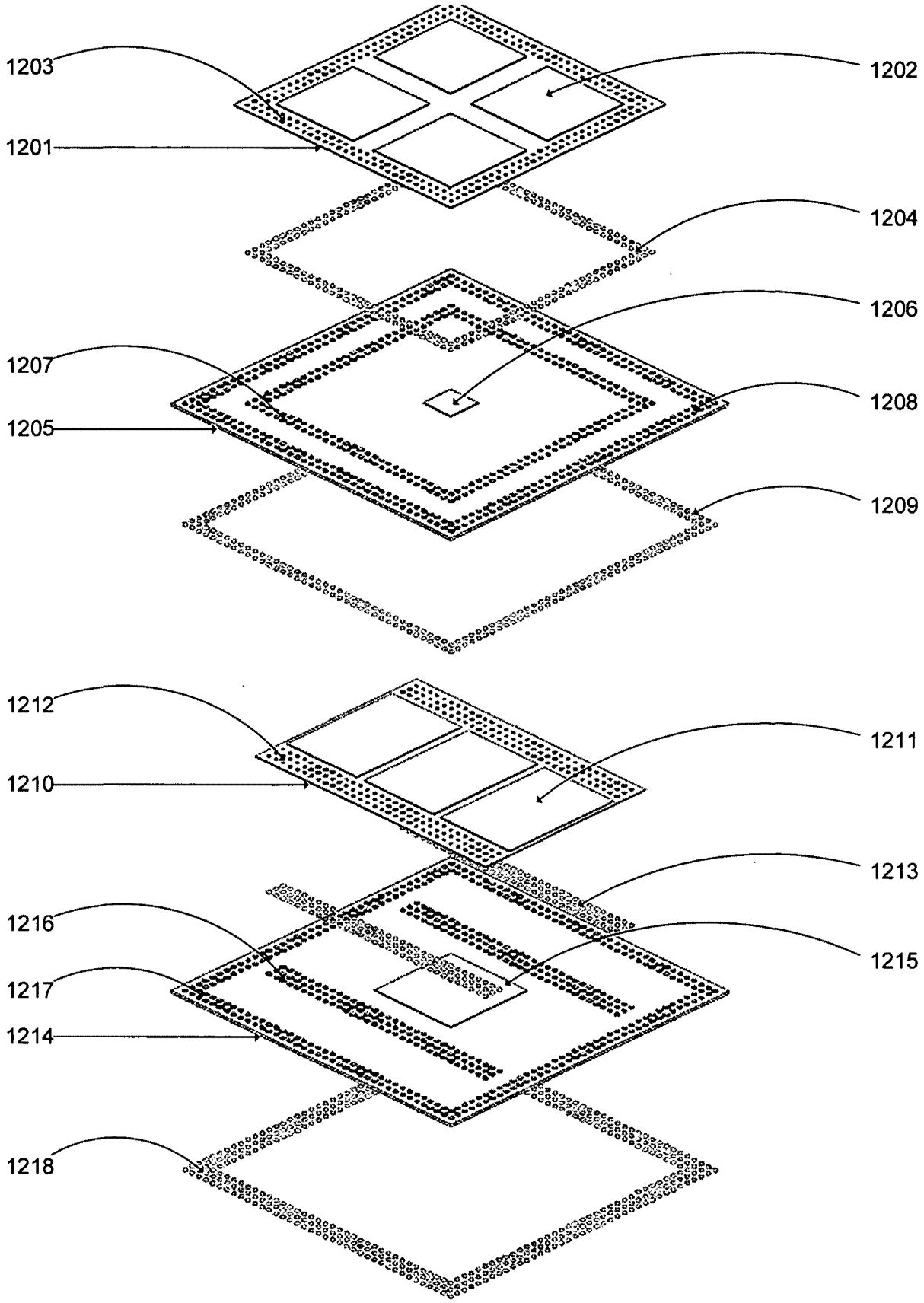


Figure 12a

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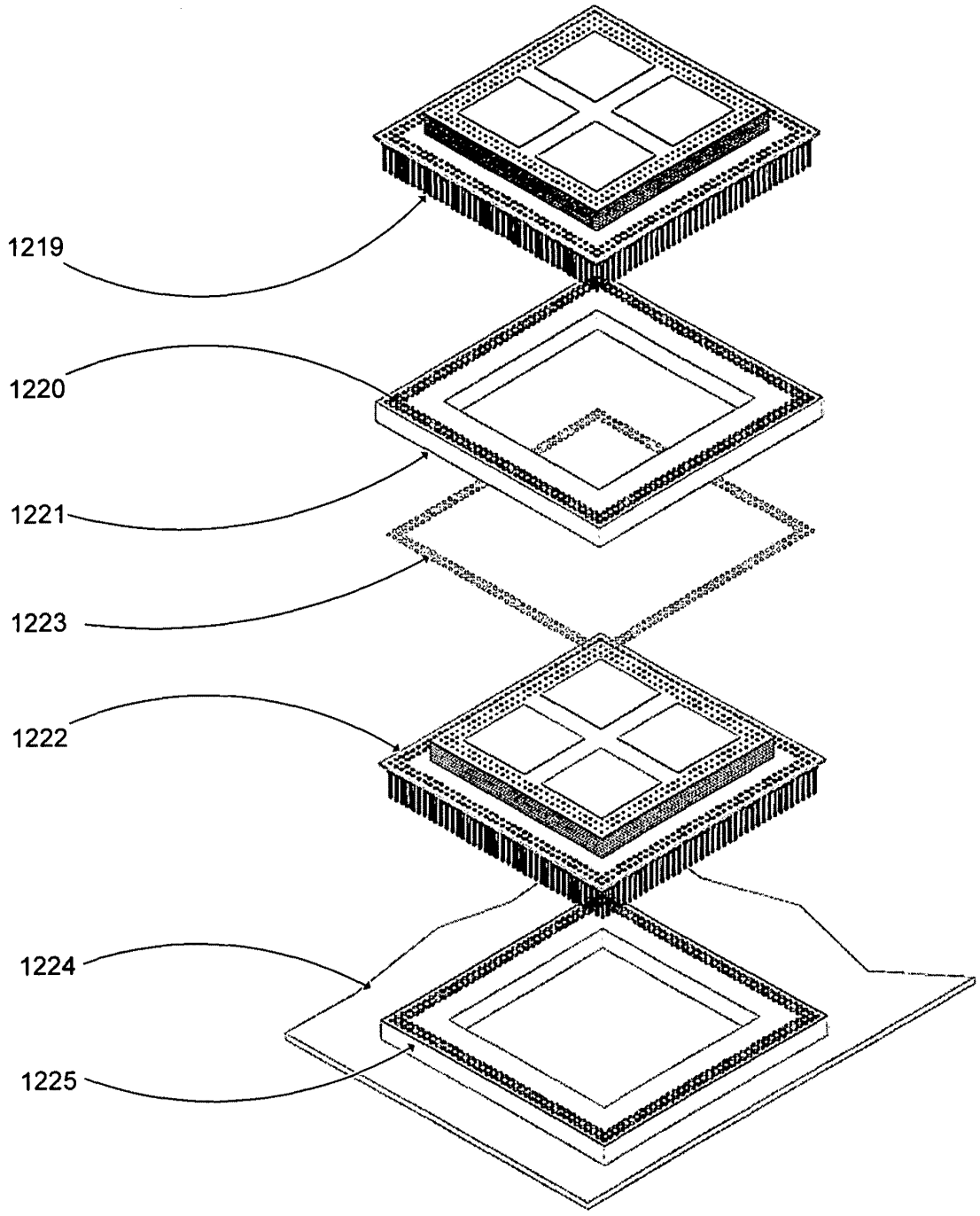


Figure 12b

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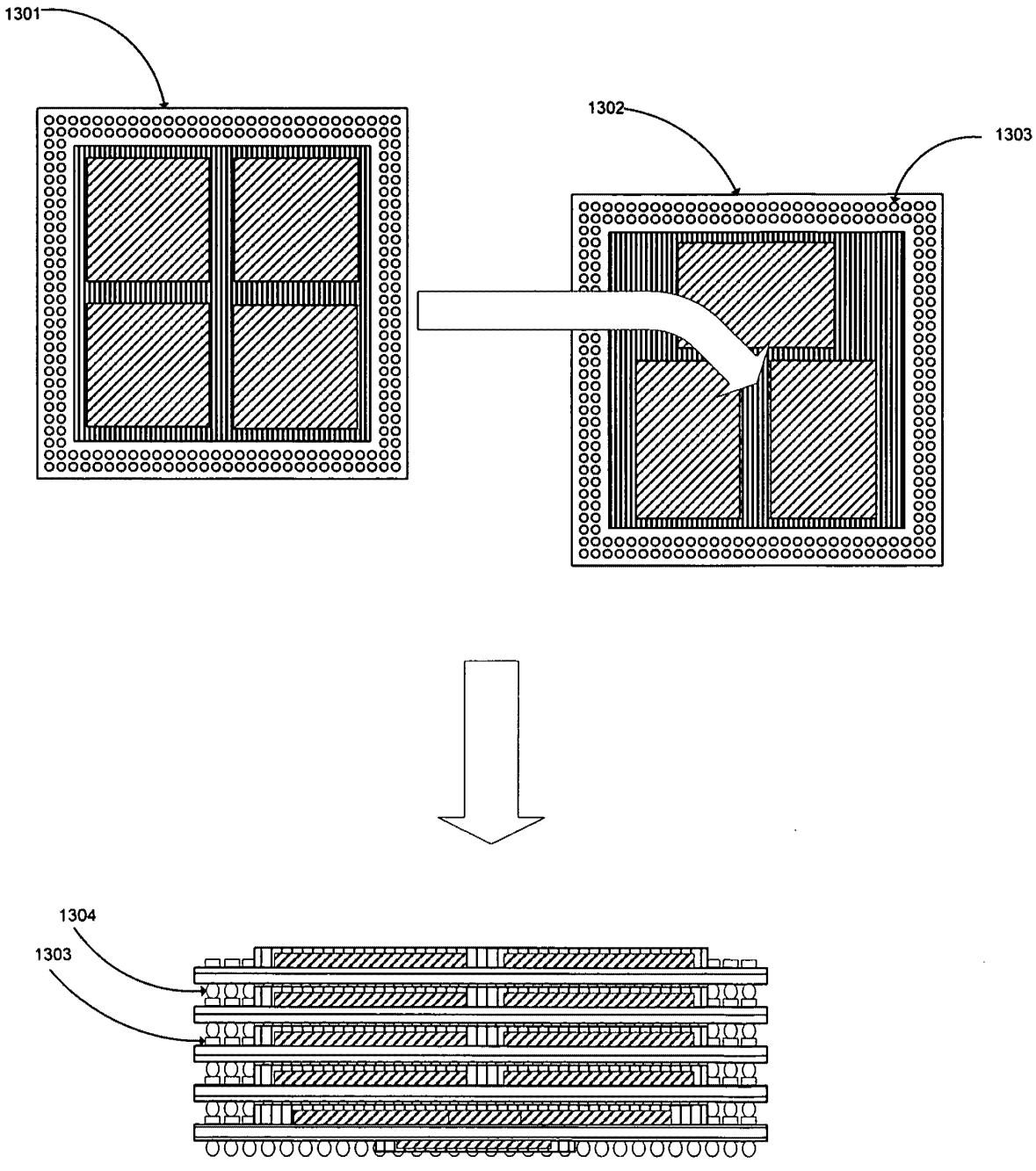


Figure 13

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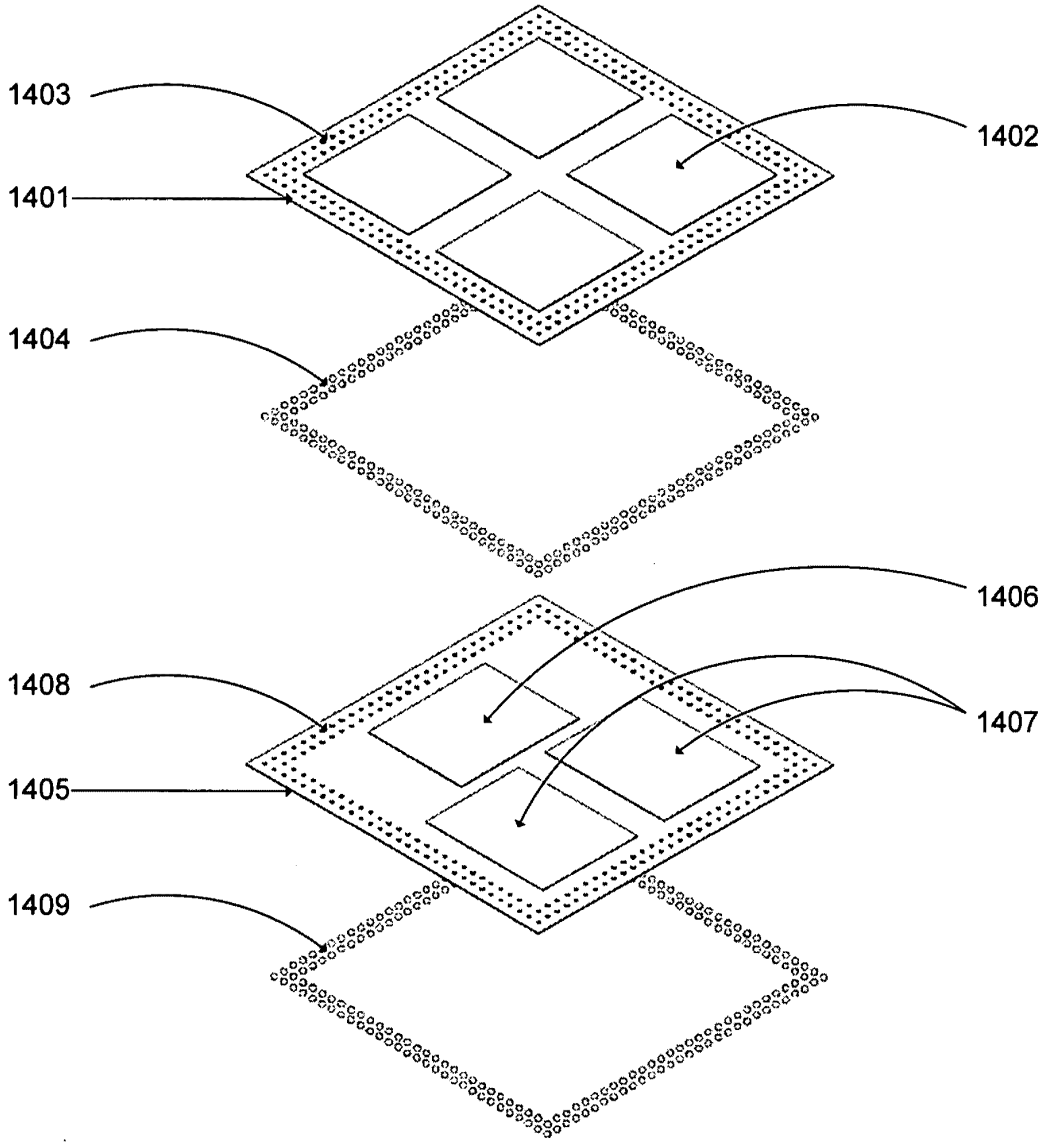


Figure 14

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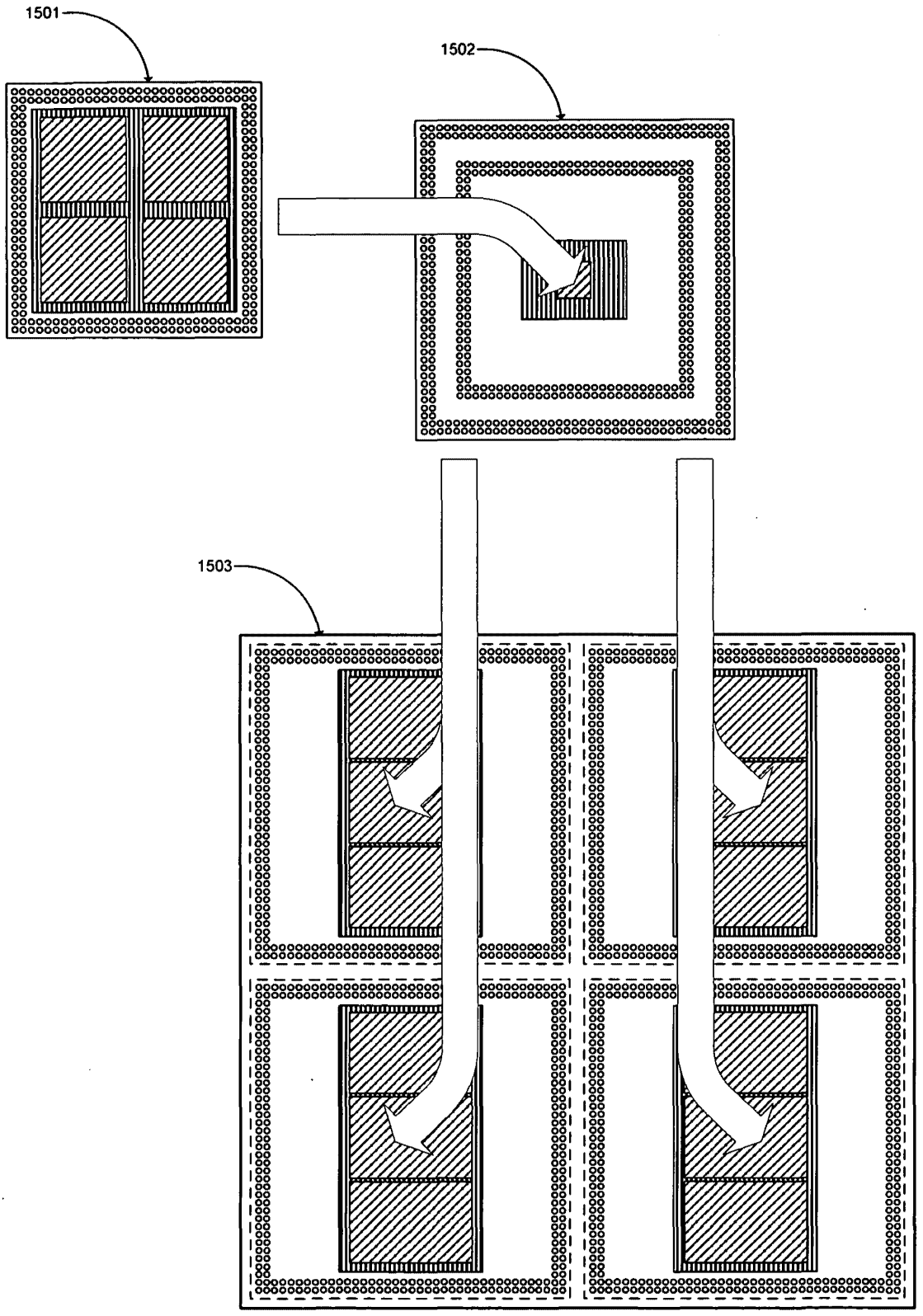


Figure 15a

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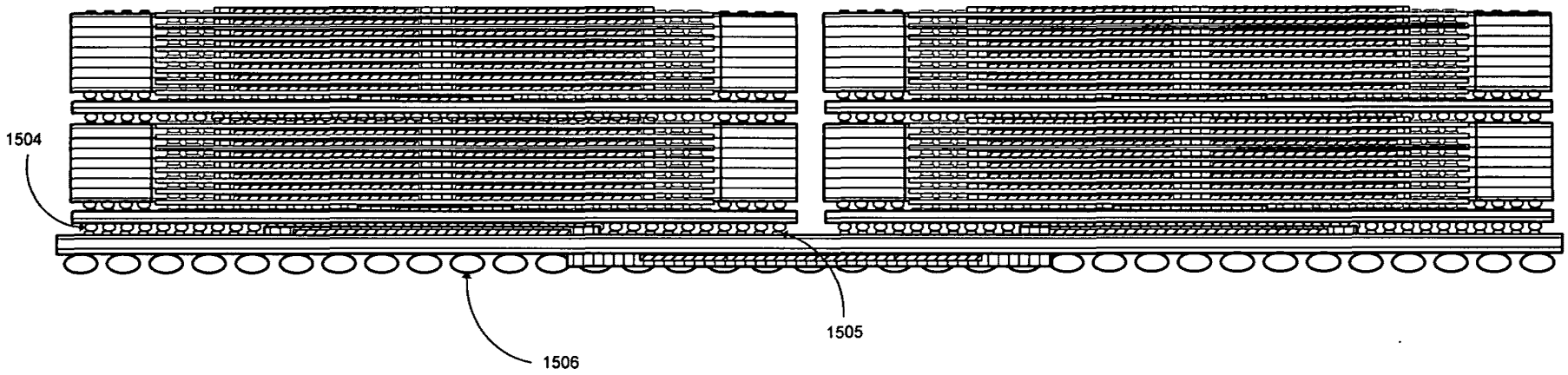


Figure 15b

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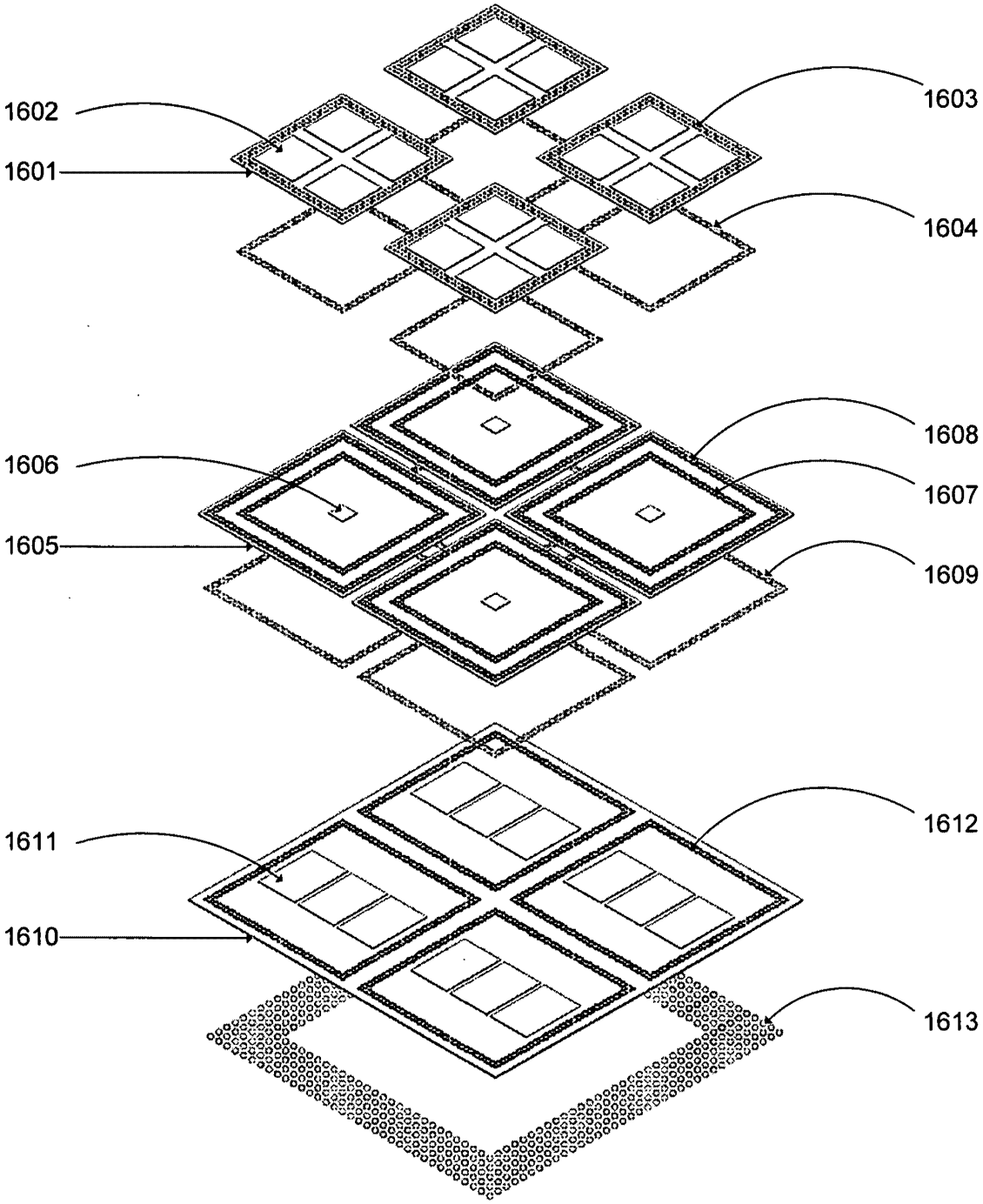


Figure 16

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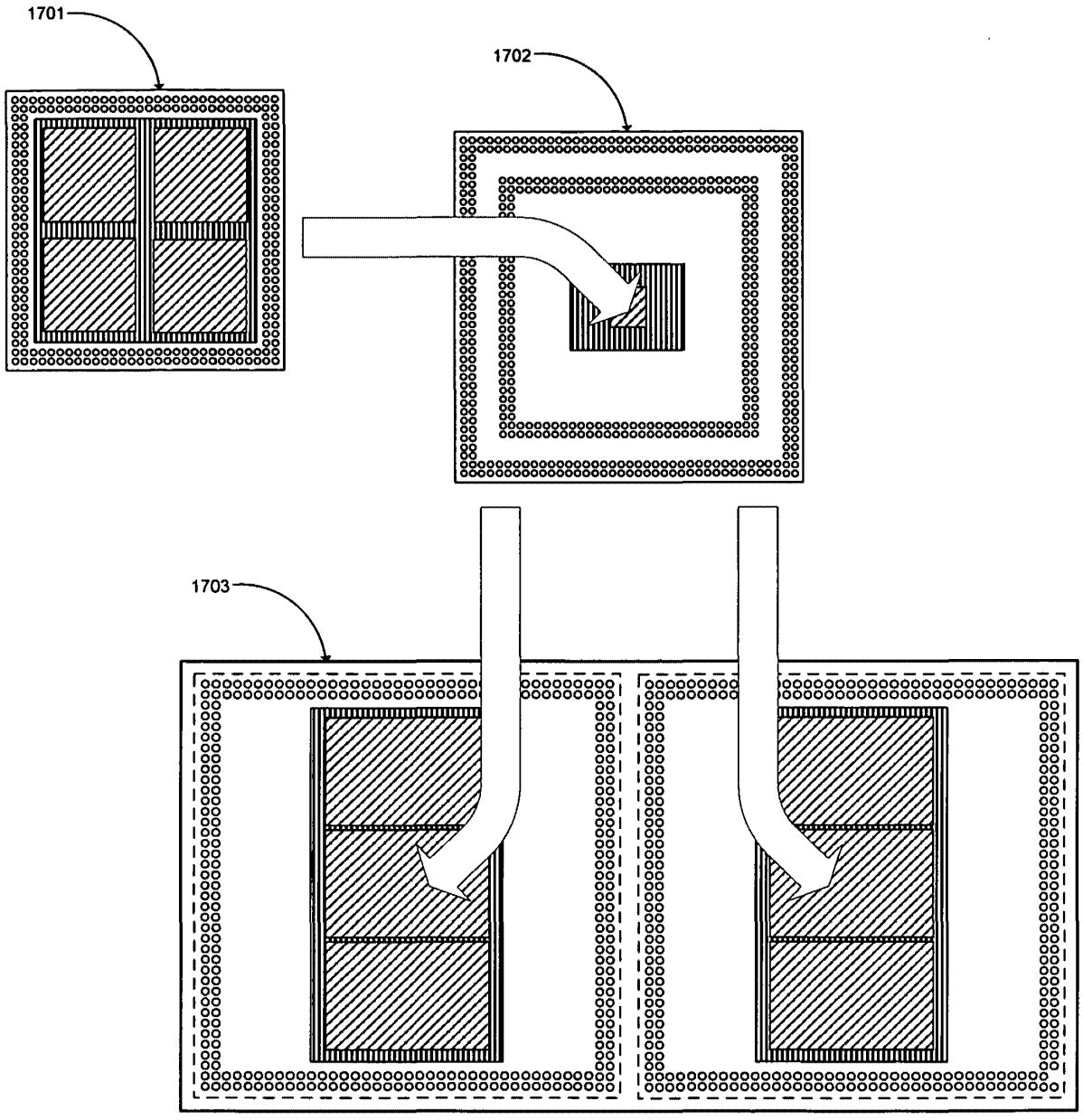


Figure 17a

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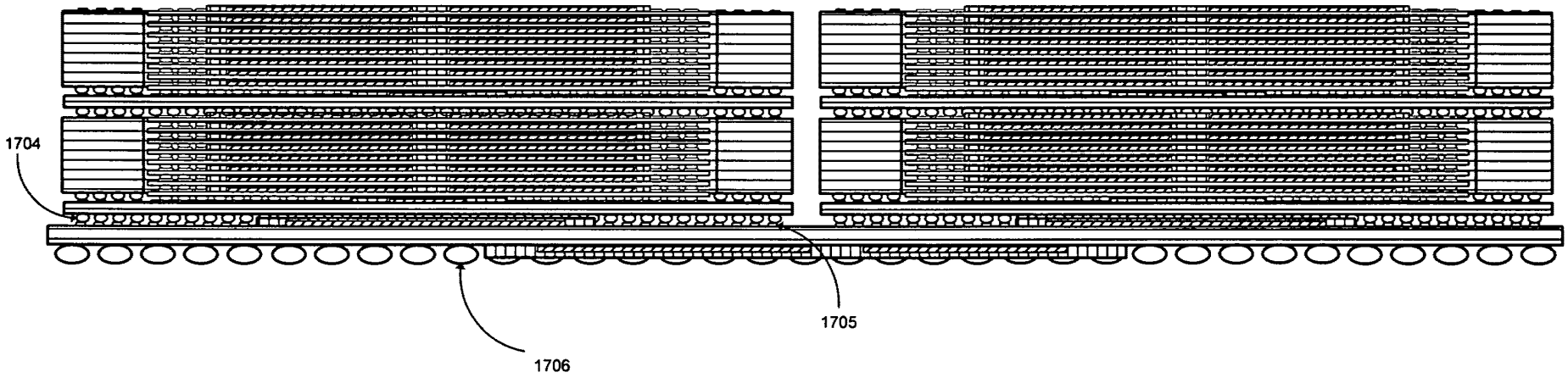


Figure 17b

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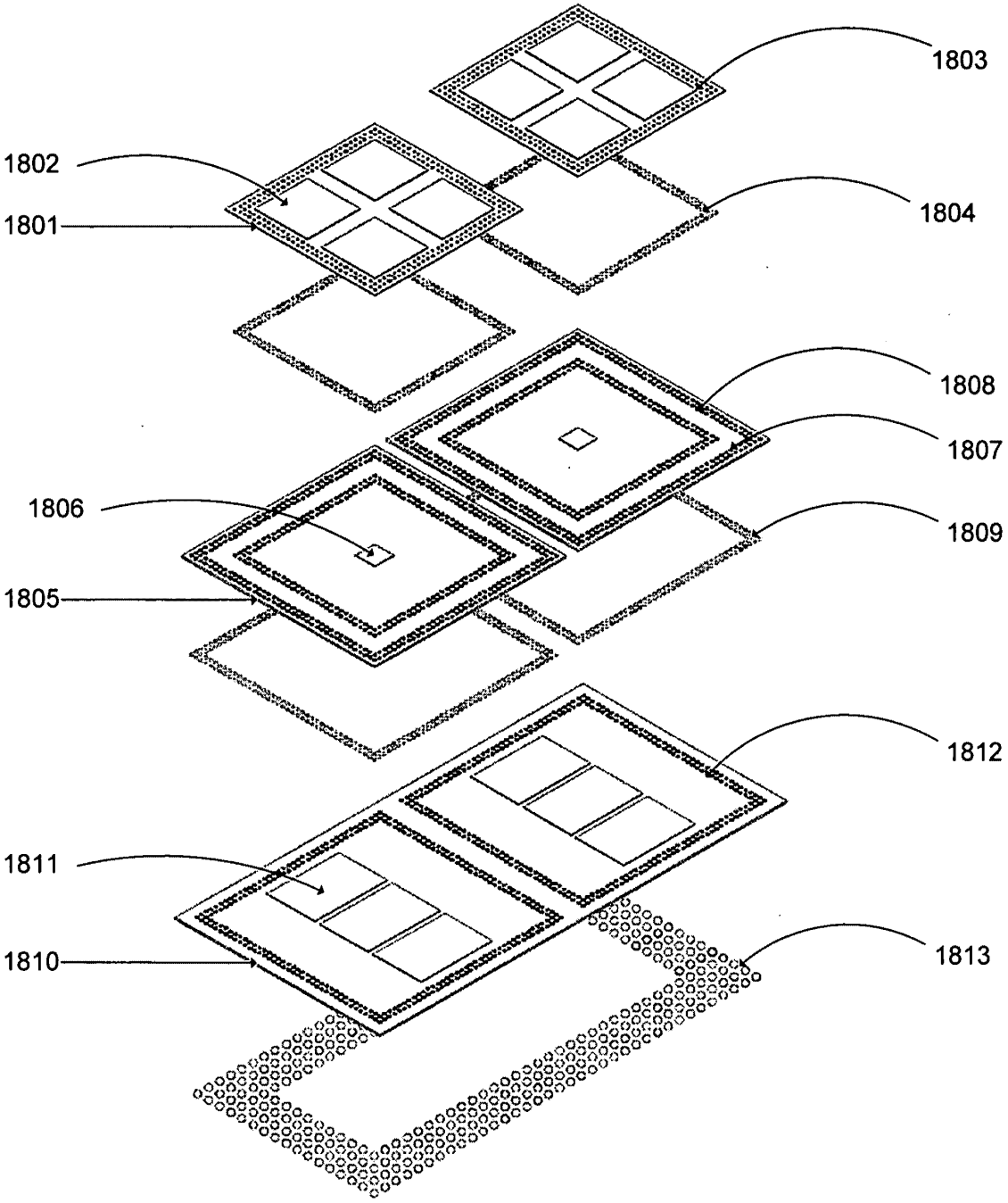

1803
1802
1801
1804
1808
1807
1806
1809
1805
1812
1811
1810
1813

Figure 18

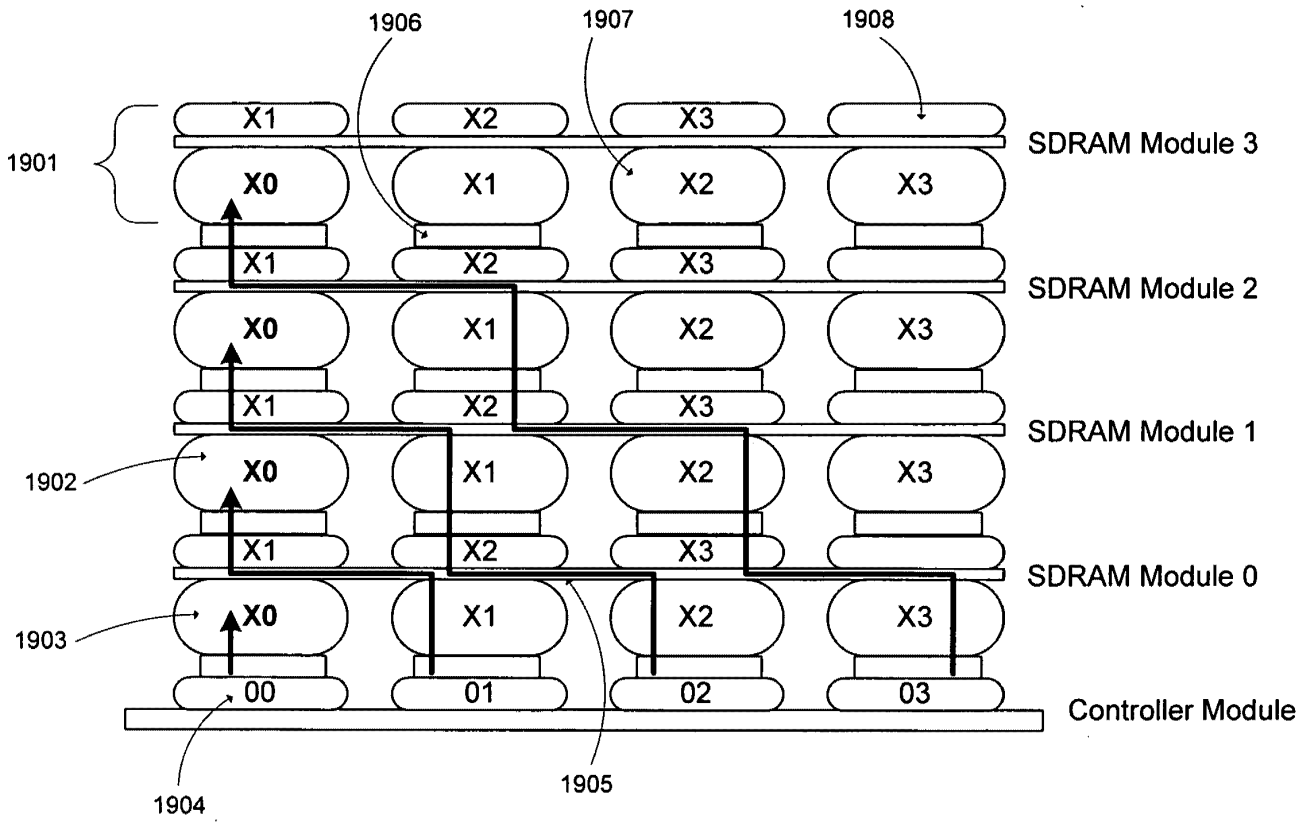

1906
1907
1908
1901
X1
X2
X3
X0
SDRAM Module 3
SDRAM Module 2
SDRAM Module 1
SDRAM Module 0
1902
1903
00
01
02
03
Controller Module
1904
1905

Figure 19

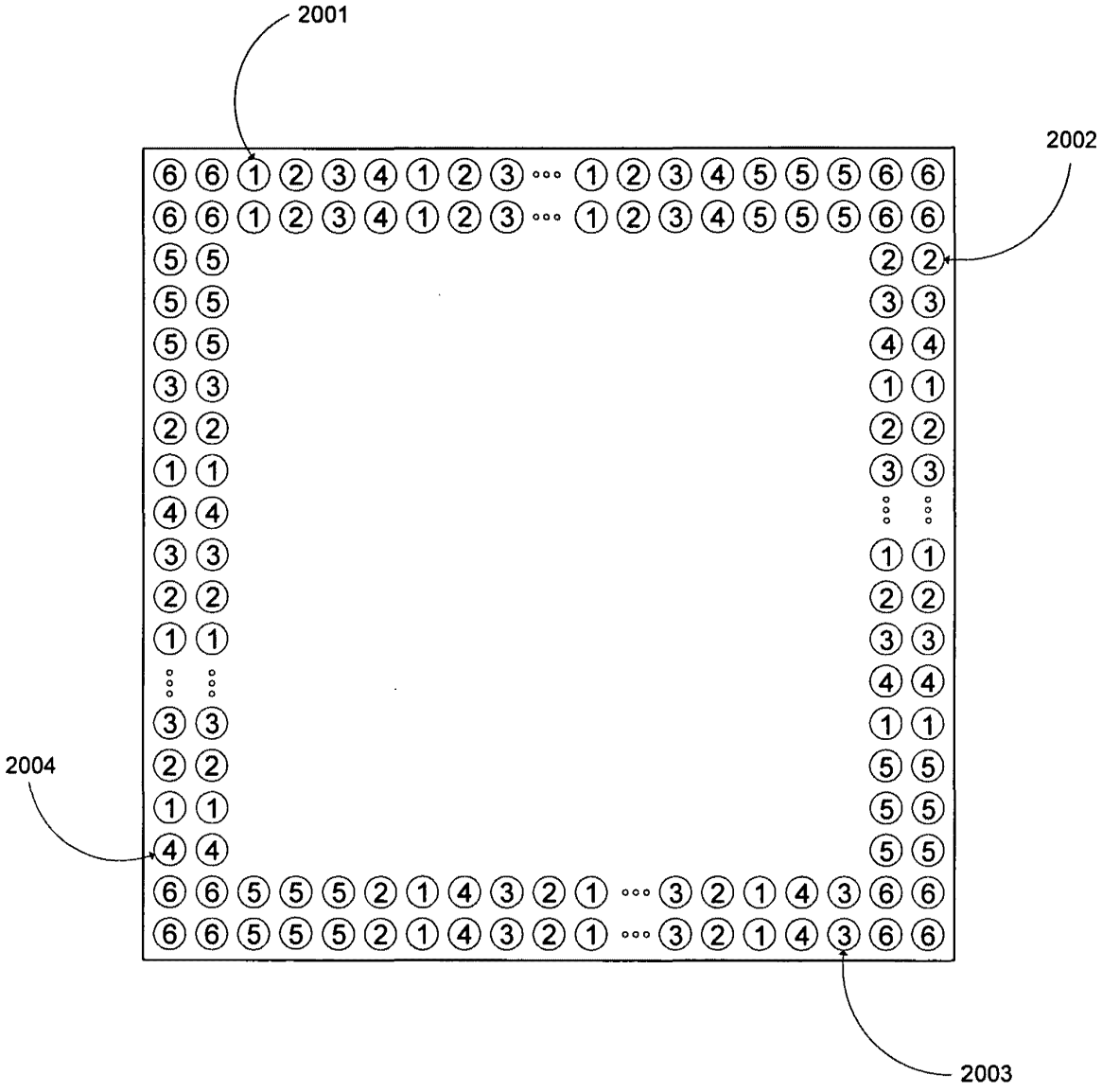


Figure 20a

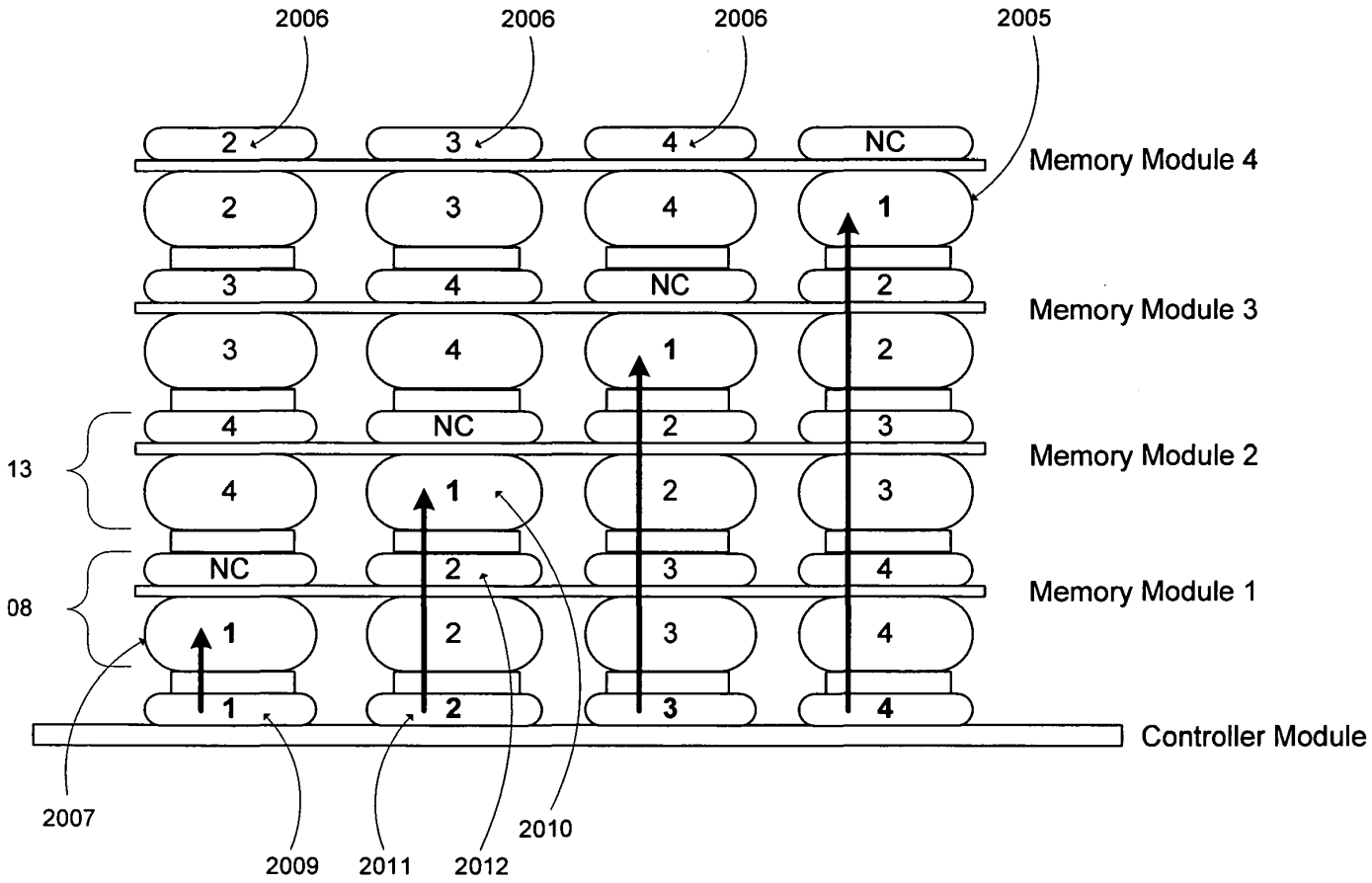

2006
2006
2006
2005
Memory Module 4
Memory Module 3
Memory Module 2
Memory Module 1
Controller Module
13
08
NC
2007
2009
2011
2012
2010

Figure 20b

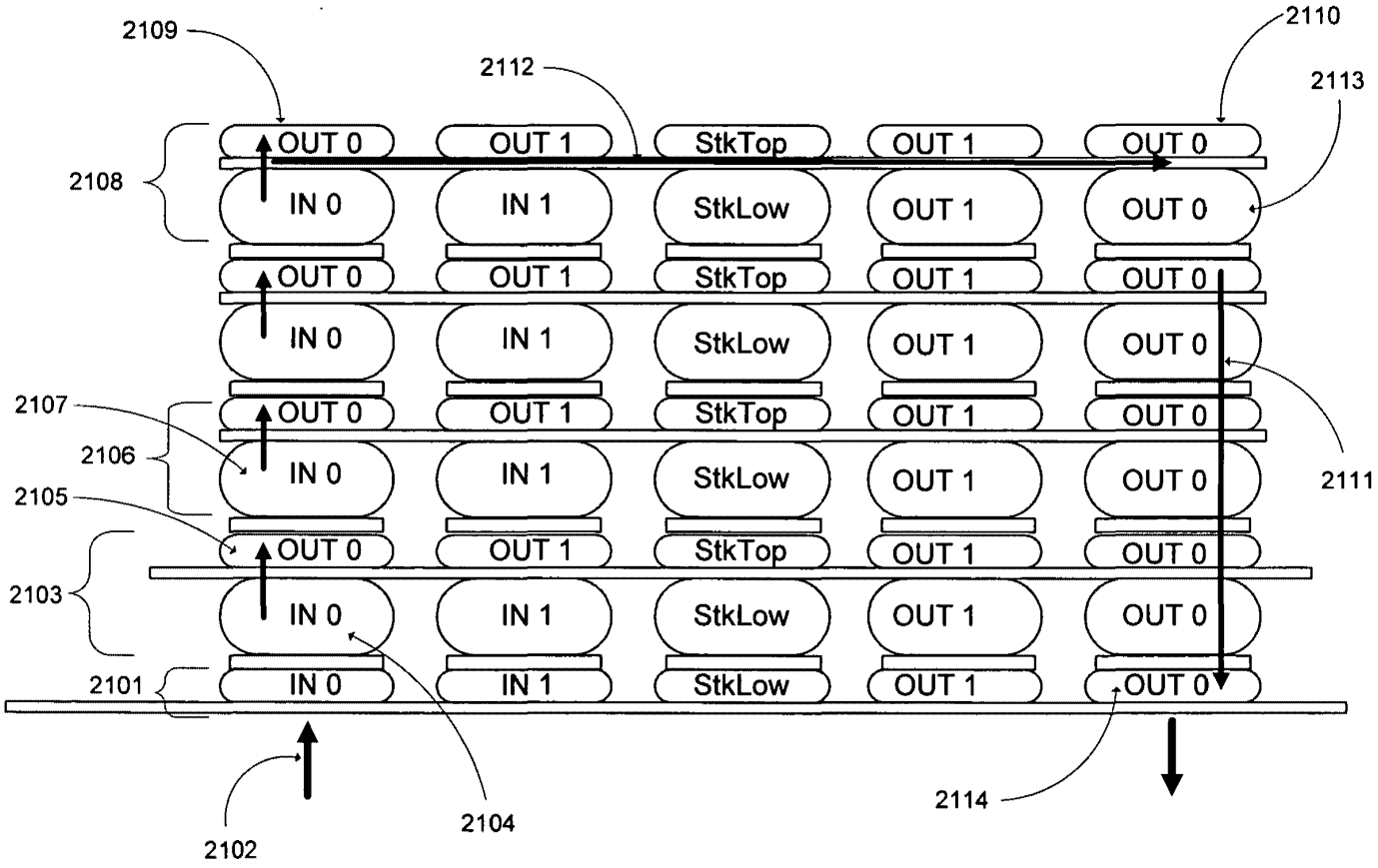

2109
2110
2112
2113
2108
OUT 0
OUT 1
StkTop
OUT 1
OUT 0
IN 0
IN 1
StkLow
OUT 1
OUT 0
2107
2106
2105
2103
2101
2111
2102
2104
2114

Figure 21a

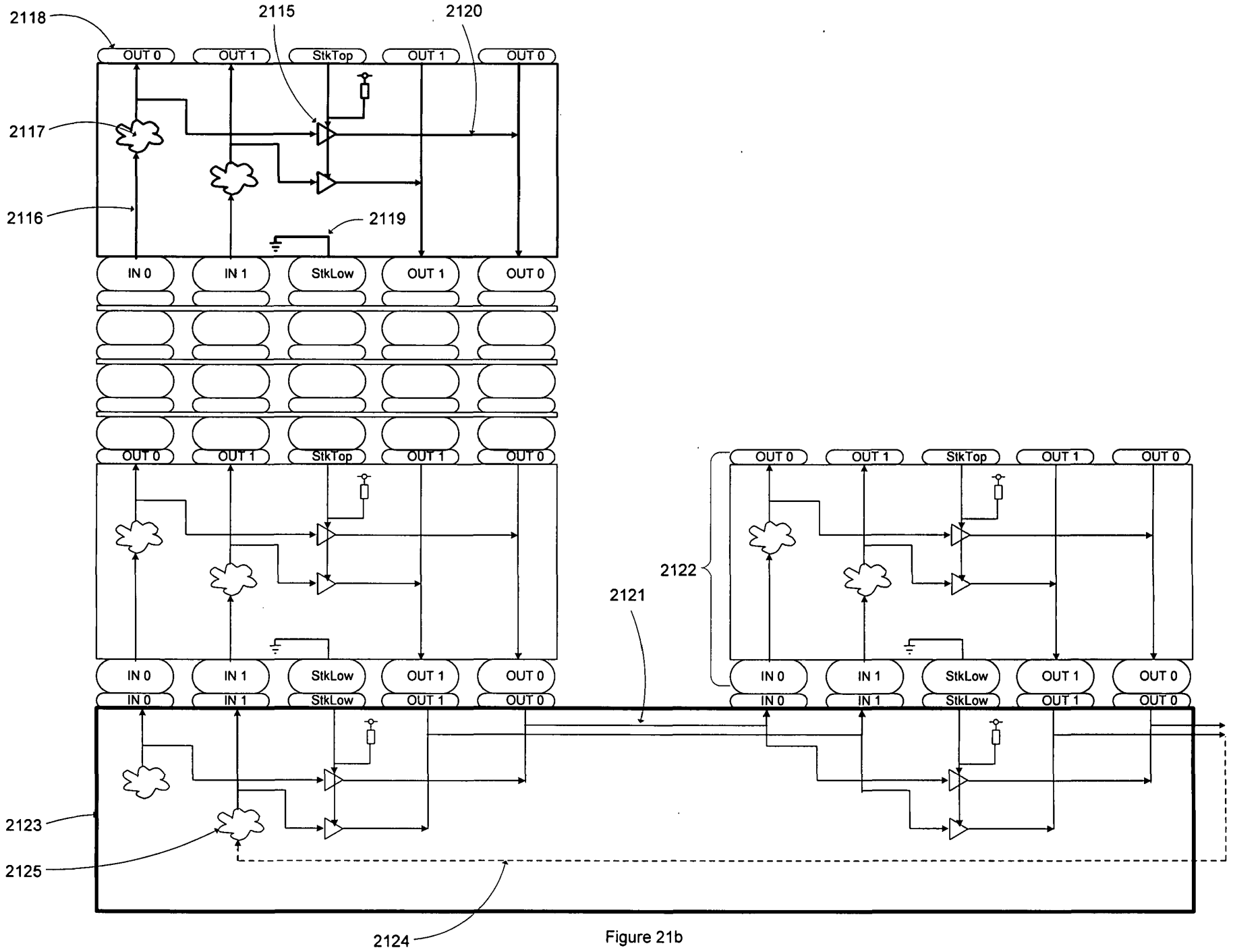

2118
2115
2120
OUT 0
OUT 1
StkTop
OUT 1
OUT 0
2117
2116
2119
IN 0
IN 1
StkLow
OUT 1
OUT 0
2122
2121
2123
2125
2124

Figure 21b

Docket No: BIT-P0099

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, postal address and citizenship are as stated below next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original first and joint inventor (if multiple names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MULTIPLE CHIP MODULE AND PACKAGE STACKING METHOD FOR STORAGE DEVICES

the specification of which is attached hereto unless the following information is indicated:

_____ was filed on _____;
as United States Application Number or PCT International Application Number _____;
and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendments referred to above.

I acknowledge the duty to disclose information that is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified, as so indicated below, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Claimed
_____	_____	_____	___ Yes ___ No
(Application No.)	(Country)	(Month/Day/Year Filed)	

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

_____	_____
(Application No.)	(Month/Day/Year Filed)

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. 1.56 that became available between the filing date of the prior application and the national or PCT International filing date of this application.

_____	_____	_____
(Application No.)	(Month/Day/Year Filed)	(Status - patented, pending, abandoned)

Application Serial No.:
Docket No: BIT-P009

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith:

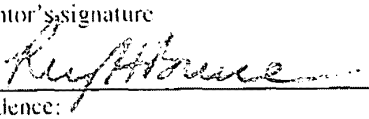
DENNIS S. FERNANDEZ, REG. NO. *34,160*
MIRCEA ACHIRILOAIE, REG. NO. *48,880*
JAMES HARRIS, REG. NO. *52,995*
RENEE JACOWITZ, REG. NO. *55,298*
KANIKA RADHAKRISHNAN, REG. NO. *49,093*
MICHELE LIU, REG. NO. *44,875*
KAREN KAUFMAN, REG. NO. 57,239
ROBERT KO, REG. NO. 56,968
ROBERT PURVY, REG. NO. 56,582

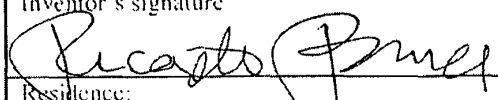
Send Correspondence and Communications to:

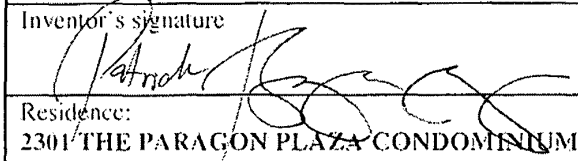
CUSTOMER NO: 22877

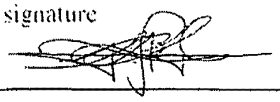
FERNANDEZ & ASSOCIATES, LLP
PATENT ATTORNEYS
PO BOX D
MENLO PARK, CA 94025-6204
PHONE: (650) 325-4999
FAX: (650) 325-1203
EMAIL: *iploft@iploft.com*

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and beliefs are believed to be true; and further that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: REY BRUCE
Inventor's signature  Date 12/20/2005
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Citizenship: U.S.A.
Postal Address: SAME AS RESIDENCE

Full name of sole or first inventor: RICARDO BRUCE
Inventor's signature  Date 12/20/2005
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Citizenship: U.S.A.
Postal Address: SAME AS RESIDENCE

Full name of sole or first inventor: PATRICK DIGAMON BUGAYONG
Inventor's signature  Date 12/20/2005
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Citizenship: PHILIPPINES
Postal Address: SAME AS RESIDENCE

Full name of sole or first inventor: JOEL ALONZO BAYLON
Inventor's signature  Date 12/20/2005
Residence: 82 HUGO ARCA STREET, BIWAS, TANZA, CAVITE,

Citizenship: **PHILIPINES**
Postal Address: **SAME AS RESIDENCE**

Application Data Sheet

Application Information

Filing Date::	12/29/2005
Application Type::	Regular
Subject Matter::	Utility
CD-ROM or CD-R?	None
Title::	Multiple Chip Module and Package Stacking Method For Storage Devices
Attorney Docket Number::	BIT-P009
Request for Early Publication?::	No
Request for Non-Publication?::	Yes
Suggested Drawing Figures::	36
Total Drawing Sheets::	28
Small Entity::	Yes
Petition included?::	No
Secrecy Order in Parent Appl.?::	No

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Status::	Full Capacity
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Country of mailing address::	US
State or Province of mailing address::	CA
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City of mailing address::	Union City
Country of mailing address::	US
State or Province of mailing address::	CA
Postal or Zip Code of mailing address::	94587

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State or Province of Residence::	
Country of Residence::	Philippines
Street of mailing address::	2301 The Paragon Plaza Condominiums
City of mailing address::	Mandaluyong City
Country of mailing address::	Philippines
State or Province of mailing address::	
Postal or Zip Code of mailing address::	
Applicant Authority type::	Inventor
Primary Citizenship Country::	Philipines
Status::	Full Capacity
Given Name::	Joel Alonzo
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State or Province of Residence::	
Country of Residence::	Philippines
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City of mailing address::	Biwas, Tanza, Cavite

Country of mailing address:: Philippines

State or Province of mailing address::

Postal or Zip Code of mailing address::

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State or Province of mailing address::	CA
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Telephone::	(650)-325-4999
Fax::	(650)-325-1203

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Representative Customer Number:: 22877

Representative Designation::	**Registration Number::**	**Name::**
Primary	34160	Dennis S. Fernandez, Esq
Patent Agent	48880	Mircea Achiriloaie, Esq
Patent Agent	52995	James Harris
Patent Agent	55298	Renee Jacowitz
Patent Agent	49093	Kanika Radhakrishnan, Esq
Patent Agent	44,875	Michele Liu, Esq
Patent Agent	57,239	Karen Kaufman
Patent Agent	56,968	Robert Ko
Patent Agent	56,582	Robert Purvy

PTO/SB/35 (11-00)
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REQUEST AND CERTIFICATION UNDER 35 U.S.C. 122(b)(2)(B)(i)		
	First Named Inventor	Bruce, et al.
	Title	Multiple Chip Module and Package Stacking Method For Storage Devices
	Atty Docket Number	BIT-P009

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing. I hereby request that the attached application not be published under 35 U.S.C. 122(b).

12/29/05
Date

Signature

Dennis S. Fernandez, ESQ, Reg. No. 34,160
Typed or printed name

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing.**

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

Burden Hour Statement: This collection of information is required by 37 CFR 1.213(a). The information is used by the public to request that an application not be published under 35 U.S.C. 122(b) (and the PTO to process that request). Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This form is estimated to take 6 minutes to complete. This time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: P.O. Box 1450, Alexandria, VA 22313-1450.

PATENT APPLICATION SERIAL NO _____

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PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

01/05/2006 YPOLITE1 00000066 11322442

01 FC:2011	150.00	OP
02 FC:2111	250.00	OP
03 FC:2311	100.00	OP
04 FC:2202	150.00	OP

Repln. Ref: 01/05/2006 YPOLITE1 0012082400
DA#:500482 Name/Number:11322442
FC: 9204 $40.00 CR

PTO-1556
(5/87)

U.S. Government Printing Office: 2002 — 466-247/69033

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875 Effective December 8, 2004

Application or Docket Number: 11322462

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	150.00		N/A	300.00
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	$250		N/A	$500
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	$100		N/A	$200
TOTAL CLAIMS (37 CFR 1.16(i))	26 minus 20 =	* 6	X$ 25 =	150	OR	X$50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	* 0	X100 =		OR	X200 =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			+180=			+360=	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	650		TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X$ 25 =		OR	X$50 =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X100 =		OR	X200 =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					+180=		OR	+360=	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X$ 25 =		OR	X$50 =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X100 =		OR	X200 =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					+180=		OR	+360=	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

17667 U.S. PTO
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112974 U.S. PTO
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122905

The Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Re: U.S. Utility Patent Application
Appl. No. (Not yet assigned); Filed _12/29/2005_
For: **Multiple Chip Module and Package Stacking Method For Storage Devices**
Inventor(s): **Bruce, et al.**
Docket No.: **BIT-P009**

Sir:
The following documents are forwarded herewith for action by the U.S. Patent and Trademark Office:

1. U.S. UTILITY APPLICATION
   entitled: **Multiple Chip Module and Package Stacking Method For Storage Devices**
   having named inventor(s):
   Bruce, et al.
   a. a specification consisting:
      (i) _24_ pages prior to the claims, including title page;
      (ii) _10__ pages of claims;
      (iii) _1_page abstract;
   b. __28__ sheets of drawings: (FIGs. 1a, 1b, 2a,2b,2c, 3a, 3b, 3c, 4a, 4b, 5a, 5b, 6a, 6b, 7a, 7b, 8a, 8b, 9, 10, 11, 12a, 12b, 13, 14, 15a, 15b, 16, 17a, 17b, 18, 19, 20a, 20b, 21a, 21b);
2. An **executed** Combined Declaration and Power of Attorney by named inventors;
3. Form PTO-1082 (in duplicate);
4. Request and Certification Form PTO/SB/35 (11-00);
5. Check No. ___1480_____ For $ _690.00__ to cover:

Basic Application Fee:	$ 150.00
Utility Search Fee:	$ 250.00
Utility Examination Fee:	$ 100.00
Assignment Recordation fee:	$ 40.00
Excess claims fee:	$ 150 .00

6. Application Data Sheet(__6__ sheets); and
7. A return post card

It is respectfully requested that the attached postcard be stamped with the filing date of the above documents and unofficial application number and returned to the addressee as soon as possible.

12/29/05
Date

Respectfully submitted,

DENNIS S. FERNANDEZ, ESQ
Reg. No. 34,160

FERNANDEZ & ASSOCIATES, LLP
PATENT ATTORNEYS
PO BOX D
MENLO PARK, CA 94025-6204
(650) 325-4999
(650) 325-1203 FAX
EMAIL: *iploft@iploft.com*

The PTO did not receive the following listed item(s) Assignment Recordal Sheet

17667 U.S. PTO
122905

Certificate of Mailing By "U.S. Express Mail" Under 37 C.F.R. 1.10(c)
"EXPRESS MAIL" Mailing Label Number: EV749607634US Date of Deposit: 12/29/05
I hereby certify that this paper and/or fee is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to the Commissioner For Patents, P.O. Box 1450, Alexandria 22313-1450

Name: Chris Vo
Signature
12/29/05
Date

Docket No.: BIT-P009

APPLICATION TRANSMITTAL LETTER

Commissioner for Patents
P.O. Box 1450.
Alexandria, VA 22313-1450

Sir:
Transmitted herewith for filing is the patent application of
Inventor(s): **Bruce, et al.**
Entitled: **"Multiple Chip Module and Package Stacking Method For Storage Devices"**

__35__ No. pages of specification, including title page, claims and abstract
__28__ No. sheets of drawings

Also enclosed are:
__X__ Executed Combined Declaration and Power of Attorney for Patent Application
___ An Original Executed Assignment of the Application
___ Form PTO-1595 (Recordation Cover Sheet for Assignment)
__X__ Request and Certification Form PTO/SB/35 (11-00)
__X__ Application Data Sheet (_6__ sheets)
___ An Information Disclosure Statement (Form PTO/SB/08A and Form PTO/SB/08B)
___ A copy of References cited in Information Disclosure: _____ documents

If a continuing application:
___Continuation ___Divisional ____Continuation-in-part ___of prior application No.:
Prior application examiner:
Prior application art unit:

FEES DUE
__X__ Applicant Claims Small Entity Status (37 CFR 1.27)

The fees due for filing the application pursuant to 37 C.F.R. 1.16 and for recording the Assignment, if any, are determined as follow:

CLAIMS					
	No. of Claims		Extra Claims	Rate	Fees
Basic Application Fee ($300.00 large entity; $150.00 small entity)					$ 150.00
Utility Application Size Fee – for each additional 50 sheets that exceeds 100 sheets ($250 large entity; $125 small entity)					.00
Utility Search Fee ($500.00 large entity; $250.00 small entity)					$250.00

Repln. Ref: 01/05/2006 YPOLITE1 0012082400
DA#:500482 Name/Number:11322442
FC: 9204 $40.00 CR

Utility Examination Fee ($200.00 large entity; $100.00 small entity)					$100.00
Total Claims	26	Minus 20 =	6	X $50 = X $ 25 (small) =	150.00
Total Independent Claims	2	Minus 3 =	0	X $200 = X $100 (small) =	.00
If Multiple Dependent Claims are presented, add $360.00 or $180.00(small)					
If Assignment enclosed, add Assignment Recording Fee $40.00					40.00
TOTAL APPLICATION FEE DUE					$ 690.00

PAYMENT OF FEES
The full fee due in connection with this communication is $ 690.00
and is provided as follows:

____ The Commissioner is hereby authorized to charge the fees associated with this communication or credit any overpayment to **Deposit Account No: 500482**. A duplicate copy of this authorization is enclosed.

__X__ A Check No. 1480 for the above-specified full fee is enclosed. However, in case Applicant inadvertently miscalculated any required fee, the Commissioner is hereby authorized to charge the necessary additional amount associated with this communication or credit any overpayment to **Deposit Account No: 500482**. A duplicate copy of this authorization is enclosed.

NO 18 MONTHS PUBLICATION

REQUEST AND CERTIFICATION UNDER 35. U.S.C. 122(b) (2) (B) (i)

__X__ I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen month after filing. **I hereby request that the attached application not to be published under 35 U.S.C. 122(b).**

This application is filed pursuant to 37 C.F.R. 1.53 in the name of the above-identified Inventor(s).

Please direct all correspondence concerning the above-identified application to the following Custom Number and Address:

Customer No: 22877

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PO BOX D
MENLO PARK, CA 94025-6204
(650) 325-4999
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EMAIL: *iploft@iploft.com*

Respectfully submitted,

DENNIS S. FERNANDEZ, ESQ
Reg. No. 34,160

12/29/05
Date